UNIVERSITA' DEGLI STUDI DI BOLOGNA

FACOLTA' DI INGEGNERIA

SCUOLA DI DOTTORATO IN SCIENZE ED INGEGNERIA DELL'INFORMAZIONE

DOTTORATO IN INGEGNERIA ELETTRONICA, INFORMATICA E DELLE TELECOMUNICAZIONI

XX° CICLO

MODELS AND METHODS FOR POWER MONOLITHIC MICROWAVE INTEGRATED CIRCUITS

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ANNO ACCADEMICO 2007-2008

Settore Scientifico Disciplinare: ING-INF/01

ACKNOWLEDGMENTS

This thesis is the result of three and half years of work whereby I have been accompanied and supported by many people. It is a pleasant aspect that I have now the opportunity to express my gratitude for all of them. Any merit in this thesis is in large measure due to them.

First and foremost, I gladly acknowledge my debt to my tutor Prof. Fabio Filicori, my co-tutor Prof. Alberto Santarelli, Prof. Giorgio Vannini and Doctor Pier Andrea Traverso, that taught me all I know about electron device modelling techniques. Without their constant friendship, encouragement and advice over many years this work would ever have been completed. Furthermore I would like to thank Prof. Vito Monaco that, together with Prof. Giorgio Vannini, first introduced me in the Laboratory of Electronics for Telecommunications of the University of Bologna, giving me the opportunity of participating as a PhD Student to its research activities.

Another important person I would like to thank is Prof. Antonio Raffo whom I could define my "spiritual instructor". During these years I have known Antonio as a sympathetic and principle-centered person. His overly enthusiasm and integral view on research and his mission for keeping me involved in these work, has made a deep impression on me. I owe him lots of gratitude for having me shown this way of research. He could not even realize how much I have learned from him.

Dr. Rafael Cignani belongs to the special persons I've known during these years. He always kept an eye on the progress of my work and always was available when I needed his advises.

Antonio and Rafael besides of being excellent supervisors, they are as close as relative and a good friends to me.

My colleagues of the Laboratory of Electronic for Telecommunications and of the Spin-Off MEC (Microwave Electronic for Communication) all gave me the feeling of being at home at work. Francesco Scappaviva, Julio Andres Lonac, Ilan Melczarsky, Massimo Pirazzini, Valeria Di Giacomo, Federico Fantini, Svevo Monaco, Valeria Vadalà, Antonio Musio, Sara D'Angelo, Corrado Florian, Rudi Paolo Paganelli, many thanks for being your colleague.

I feel a deep sense of gratitude for my father and mother who formed part of my vision and taught me, through simple words, the good things that really matter in life.

I am very grateful for all my friends of my little town for rendering me the sense and the value of brotherhood. I am glad to be one of them.

The last… The last is the most precious. I am very grateful for my girlfriend Valentina, for her love and patience during this period of my life. My knowledge and what you learn from me is all due to her.

INTRODUCTION

Computer aided design of Monolithic Microwave Integrated Circuits (MMICs) depends critically on active device models that are accurate, computationally efficient, and easily extracted from measurements or device simulators.

Empirical models of active electron devices, which are based on actual device measurements, do not provide a detailed description of the electron device physics. However they are numerically efficient and quite accurate. These characteristics make them very suitable for MMIC design in the framework of commercially available CAD tools.

In the empirical model formulation it is very important to separate linear memory effects (parasitic effects) from the nonlinear effects (intrinsic effects). Thus an empirical active device model is generally described by an extrinsic linear part which accounts for the parasitic passive structures connecting the nonlinear intrinsic electron device to the external world.

An important task circuit designers deal with is evaluating the ultimate potential of a device for specific applications. In fact once the technology has been selected, the designer would choose the best device for the particular application and the best device for the different blocks composing the overall MMIC. Thus in order to accurately reproducing the behaviour of different-in-size devices, good scalability properties of the model are necessarily required.

Another important aspect of empirical modelling of electron devices is the mathematical (or equivalent circuit) description of the nonlinearities inherently associated with the intrinsic device. Once the model has been defined, the proper measurements for the characterization of the device are performed in order to identify the model. Hence, the correct measurement of the device nonlinear characteristics (in the device characterization phase) and their reconstruction (in the identification or even simulation phase) are two of the more important aspects of empirical modelling.

This thesis presents an original contribution to nonlinear electron device empirical modelling treating the issues of model scalability and reconstruction of the device nonlinear characteristics.

The scalability of an empirical model strictly depends on the scalability of the linear extrinsic parasitic network, which should possibly maintain the link between technological process parameters and the corresponding device electrical response.

Since lumped parasitic networks, together with simple linear scaling rules, cannot provide accurate scalable models, either complicate technology-dependent scaling rules or computationally inefficient distributed models are available in literature.

This thesis shows how the above mentioned problems can be avoided through the use of commercially available electromagnetic (EM) simulators. They enable the actual device geometry and material stratification, as well as losses in the dielectrics and electrodes, to be taken into account for any given device structure and size, providing an accurate description of the parasitic effects which occur in the device passive structure. It is shown how the electron device behaviour can be described as an equivalent two-port intrinsic nonlinear block connected to a linear distributed four-port passive parasitic network, which is identified by means of the EM simulation of the device layout, allowing for better frequency extrapolation and scalability properties than conventional empirical models.

Concerning the issue of the reconstruction of the nonlinear electron device characteristics, a data approximation algorithm has been developed for the exploitation in the framework of empirical table look-up nonlinear models. Such an approach is based on the strong analogy between time-domain signal reconstruction from a set of samples and the continuous approximation of device nonlinear characteristics on the basis of a finite grid of measurements. According to this criterion, nonlinear empirical device modelling can be carried out by using, in the sampled voltage domain, typical methods of the time-domain sampling theory.

The research activity discussed in the thesis was partially performed in the context of the Network of Excellence TARGET (Top Amplifier Research Groups in a European Team) supported by the European Union.

A brief description of the contents of each chapter is provided in the following.

Chapter 1 provides an overview of different empirical models of high frequency electron devices which have been proposed in the literature. First, the most important phenomena related to the intrinsic device, such as non-quasi-static high frequency phenomena and low frequency dispersive phenomena, are discussed. Then, the most important conventional techniques for the identification of the linear extrinsic parasitic network are presented.

Chapter 2 deals with the model scalability. An example shows the poor accuracy obtained through conventional scaling rules applied to conventional empirical models. Then, more complicate extraction procedures, involving multiple measurements carried out on different devices, are discussed. Furthermore the definition of distributed empirical models is given, together with a discussion about their capability of reproducing different device behaviour at higher frequencies.

Chapter 3 represents the core of the thesis. The use of the EM simulation for the identification of the linear extrinsic parasitic network is discussed. Starting from a fully distributed EM-based linear model, two different procedures for the identification of a compact distributed parasitic network are presented. Such a compact distributed parasitic network allows for the definition of an empirical model described as an equivalent two-port intrinsic nonlinear block connected to the linear distributed compact parasitic network. This provides a nonlinear model which is as numerically efficient as conventional empirical models, maintaining also the frequency extrapolation and scalability properties of fully distributed models.

Chapter 4 provides a wide experimental validation of the compact distributed nonlinear model showing both its frequency extrapolation capability and its scaling properties. Such an experimental validation carried out on different technologies shows also the technology-independence of the EM-based approach.

Chapter 5 deals with the developed data approximation formula. Experimental validation is provided through the differentiability evaluation of the proposed approximation formula, in comparison with conventional cubic-spline interpolation, and through the IMD prediction of a GaAs-based PHEMT.

CHAPTER 1

REVIEW OF EMPIRICAL ELECTRON DEVICE MODELLING

1.1 Introduction to empirical modelling of Electron Devices.

The design of MMICs depends critically on device models that are accurate, computationally efficient, and easily extracted from measurements or device simulators.

Numerical-physical models are derived by fundamental equations describing the physic of charge transport in electron devices. They provide a direct link between technological process parameters, such as materials, geometry, doping profile, etc., and the device electrical response, but the required large amount of computation time precludes their use in circuit simulators for design purposes, making them only suitable for device design and analysis.

Empirical models, based on electron device measurements, may be either equivalent circuit (EC) models or black-box models. Equivalent circuit models use lumped circuit elements to describe the measured characteristics, while black-box models are based on integral/differential predictive equations and/or look-up tables to reproduce the observed device behaviour. Empirical models, despite they don't provide a detailed description of the electron device physics, are numerically efficient and quite accurate. These characteristics make them very suitable for MMIC design in the framework of commercially available CAD tools.

MMICs usually operate with the active electron devices showing some (maybe even gross) nonlinear behaviour. In fact Large-Signal RF operation of the electron devices involves nonlinear dynamic behaviour. The concurrent presence of memory effects and nonlinearity turns into high complexity in the model formulation. In compact empirical models the memory effects are

described by linear operators, i.e. time derivatives, integrals, delays, etc., while the nonlinearity is described by nonlinear algebraic (i.e. memoryless) functions which can be analytical, Look-Up-Table-based, Artificial-Neural-Network-based.

In order to obtain a good model formulation it is very important to separate linear memory effects (parasitic effects) from the nonlinear effects (intrinsic effects). Thus an empirical FET model is generally described by an extrinsic part which accounts for the parasitic passive structures connecting the intrinsic electron device to the external world. Typically, the parasitic network is supposed linear (i.e. *bias independent*) and it is usually modelled through different topologies according to specific technology/packaging choices (lumped or distributed). The intrinsic device, describing the basic physics of operation of the electron device, is nonlinear (i.e. *bias dependent*) with "short" memory at typical operating frequencies.

In empirical modelling, the main nonlinear functions describing the intrinsic device behaviour are current-voltage and charge-voltage relationships. They may be approximated by means of analytical functions depending on a restricted number of parameters or stored into look-up table and implemented into CAD with Data Access Components.

Fig.1.1 shows the general schematic representation of an empirical electron device model.

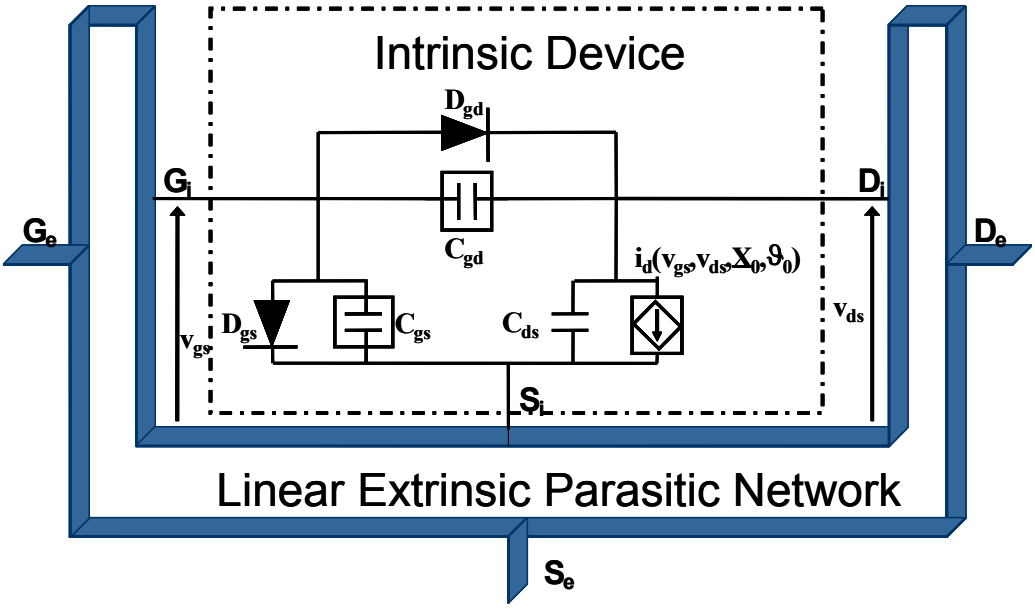

Fig. 1.1 Empirical electron device model. The model is composed by a linear extrinsic parasitic network connecting the nonlinear intrinsic device to the external world.

Since the late '70, different empirical models of high frequency electron devices have been proposed and accepted by the scientific community, according to different parasitic network topology and/or different intrinsic device formulations. In fact the empirical model properties, such

as accuracy, computational efficiency, scalability, easiness of identification, etc., strongly depend on both parasitic network and intrinsic device description. An overview of the most important intrinsic device and extrinsic parasitic network modelling approaches, which can be found in literature, is the main aim of this chapter.

1.2 Empirical Modelling of the Intrinsic Device.

1.2.1 Charge Controlled Quasi-Static Formulation

The intrinsic device must account for the conductive plus displacement current contributions which flow in the device channel depending on the selected quiescent condition of the device. As far as relatively low frequencies of operation are considered for the device, the intrinsic device behaviour can be described through a charge-controlled formulation:

$$\begin{aligned} \mathbf{i}(t) &= \mathbf{\Phi}\left\{\mathbf{q}(t), \mathbf{v}(t)\right\} + \frac{d\mathbf{q}(t)}{dt} \\ \mathbf{q}(t) &= \mathbf{\Psi}\left\{\mathbf{v}(t)\right\} \end{aligned} \tag{1.1}$$

where

$$\mathbf{i} = \begin{vmatrix} i_1 \\ i_2 \end{vmatrix}, \mathbf{v} = \begin{vmatrix} v_1 \\ v_2 \end{vmatrix}, \mathbf{q} = \begin{vmatrix} q_1 \\ q_2 \end{vmatrix}$$

are the vectors of the currents, voltages and charges at the two port of the device respectively.

The equivalent charges completely define the intrinsic device state (state variables) and they only depend on the instantaneous values of the intrinsic transistor voltages. Both numerical device simulations and experimental validation show that the simple formulation (1.1) correctly models the intrinsic device behaviour up to moderately high frequencies.

Since FETs are often controlled by the port voltages, substituting the second of (1.1) in the first of (1.1) the charge-controlled equations describing the intrinsic behaviour can be put in a voltage-controlled form (1.2).

$$\mathbf{i}(t) = \mathbf{F}\left\{\mathbf{v}(t)\right\} + \mathbf{C}\left\{\mathbf{v}(t)\right\} \cdot \frac{d\mathbf{v}(t)}{dt} \tag{1.2}$$

where

$$\mathbf{F}\{\mathbf{v}(t)\} \doteq \mathbf{\Phi}\{\ \mathbf{\Psi}\{\mathbf{v}(t)\}, \mathbf{v}(t)\ \}$$

$$\mathbf{C}\{\mathbf{v}(t)\} \doteq \frac{d\mathbf{\Psi}\{\mathbf{v}(t)\}}{d\mathbf{v}} \quad .$$

The current-voltage relationship in (1.2) is nonlinear with memory having an infinitely small duration

$$\frac{d\mathbf{v}}{dt} = \lim_{\tau \to 0} \frac{\mathbf{v}(t) - \mathbf{v}(t-\tau)}{\tau},$$

leading to a quasi-static (QS) model definition.

The hypothesis of vanishingly small duration of memory effects is not acceptable for device operation at higher frequencies. In fact the intrinsic small-signal FET admittance parameters, especially Y_{11} and Y_{21}, exhibit strong deviations from the quasi-static behaviour as shown in Fig.1.2.

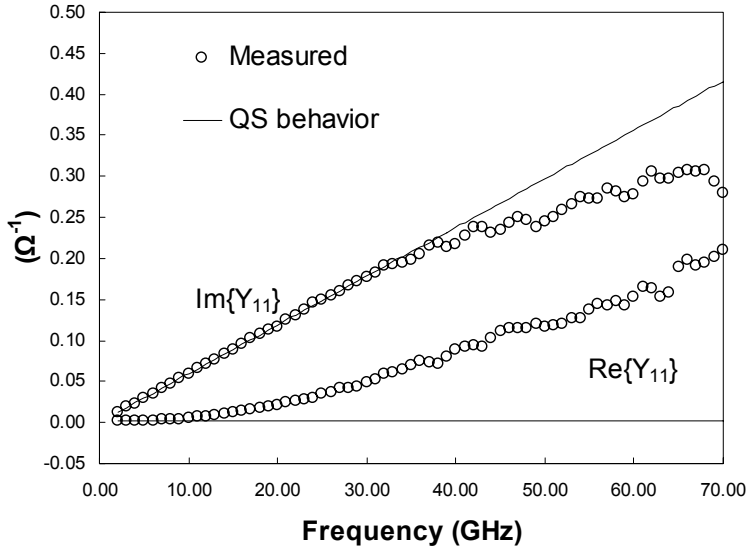

Fig. 1.2 Deviation from the quasi static behaviour of the measured intrinsic Y11 for a commercial FET.

1.2.2 Non-Quasi-Static Effects

The intrinsic device Non-Quasi-Static (NQS) effects can be theoretically explained by the fact that the charges depend on voltage values at both actual and past time instants within a finite memory time T_M. By considering such a dependence on the past values of the applied voltages, the charges of (1.1) becomes NQS as expressed in (1.3).

$$\begin{aligned}\mathbf{i}(t) &= \boldsymbol{\Phi}\left\{\mathbf{q}^{NQS}(t), \mathbf{v}(t)\right\} + \frac{d\mathbf{q}^{NQS}(t)}{dt} \\ \mathbf{q}^{NQS}(t) &= \boldsymbol{\Psi}^{NQS}\left|\mathbf{v}(t-\tau)\right|_{\tau=0}^{T_M}\end{aligned} \tag{1.3}$$

Many models adopt a charge perturbation approach $\mathbf{q}^{NQS}(t) \doteq \mathbf{q}^{QS}(t) + \boldsymbol{\Delta}\mathbf{q}(t)$, that is the NQS charges are obtained from the QS charges plus a charge perturbation $\boldsymbol{\Delta}\mathbf{q}(t)$. They also assume that the NQS phenomena affect the displacement current only, that is $\mathbf{i}(t) = \mathbf{F}\left\{\mathbf{v}(t)\right\} + d\mathbf{q}^{NQS}(t)/dt$.

In 1993 Daniels *et al.* [1], adopted a charged controlled formulation defining the following NQS model for FET devices:

$$\begin{aligned}\mathbf{i}(t) &= \mathbf{i}_c\left\{\mathbf{v}(t)\right\} + \frac{d\mathbf{q}^{NQS}(t)}{dt} \\ \mathbf{q}^{NQS}(t) &= \mathbf{q}^{QS}\left\{\mathbf{v}(t)\right\} - \boldsymbol{\tau}\left\{\mathbf{v}(t)\right\} \cdot \frac{d\mathbf{q}^{NQS}(t)}{dt}\end{aligned} \tag{1.4}$$

where $\mathbf{i}_c(\mathbf{v})$ are the quasi-static conductive currents, $\mathbf{q}^{QS}$ are the quasi-static charges and $\tau(\mathbf{v})$ is a voltage depending charge redistribution time. Considering the τ parameter voltage independent, it leads to the NQS model proposed by M. Fernandez-Barciela *et al.* in 2000 [2].

In 2006 A.Santarelli *et al.* [3] proposed a NQS model based on the description of the NQS effects as a charges perturbation. In fact the functional describing the NQS charges, the second of (1.3), is defined as follows:

$$\mathbf{q}^{NQS}(t) = \boldsymbol{\Psi}^{NQS}\left|\mathbf{v}(t-\tau)\right|_{\tau=0}^{T_M} \doteq \mathbf{q}^{QS}(t) + \boldsymbol{\Delta}\mathbf{q}(t). \tag{1.4}$$

The inverse function of the $\boldsymbol{\Psi}$ functional leads to the definition of the equivalent voltages:

$$\mathbf{v}^{QS}(t) \doteq \boldsymbol{\Psi}^{-1}\left\{\mathbf{q}^{QS}(t) + \boldsymbol{\Delta}\mathbf{q}(t)\right\} \doteq \mathbf{v}(t) + \boldsymbol{\Delta}\mathbf{v}(t) \tag{1.5}$$

where the charge perturbations $\boldsymbol{\Delta}\mathbf{q}(t)$ are modelled by means of suitable defined voltage deviations $\boldsymbol{\Delta}\mathbf{v}(t)$. Thus Nonlinear device is still described by a quasi-static model, but controlled by equivalent instead of actual voltages, as shown in Fig.1.3.

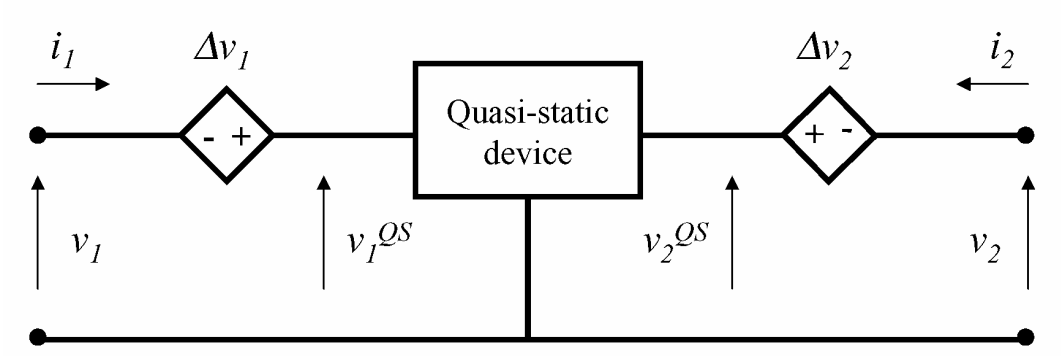

Fig. 1.3 Non-Quasi-Static Equivalent Voltage model as proposed in [3]. The NQS effects are taken into account by means of suitable voltage perturbations applied to the QS voltages.

The NQS effects may be taken into account by means of linear Voltage-Controlled Voltage-Sources (VCVS):

$$\Delta \mathbf{v}(t) = \int_0^{T_M} \mathbf{a}(\tau) \cdot \left[\mathbf{v}(t-\tau) - \mathbf{v}(t) \right] d\tau \,. \tag{1.6}$$

The effect of the voltage deviations vanishes when signal frequencies involved are in quasi-static range, that is when the actual and past voltage values coincide one another.

The charge-controlled-based formulation (1.2) is very suitable for the definition of equivalent circuit models. In fact the circuit-based interpretation of quasi-static model (1.2) is the parallel of nonlinear resistive and purely-capacitive elements, as shown in Fig.1.4.

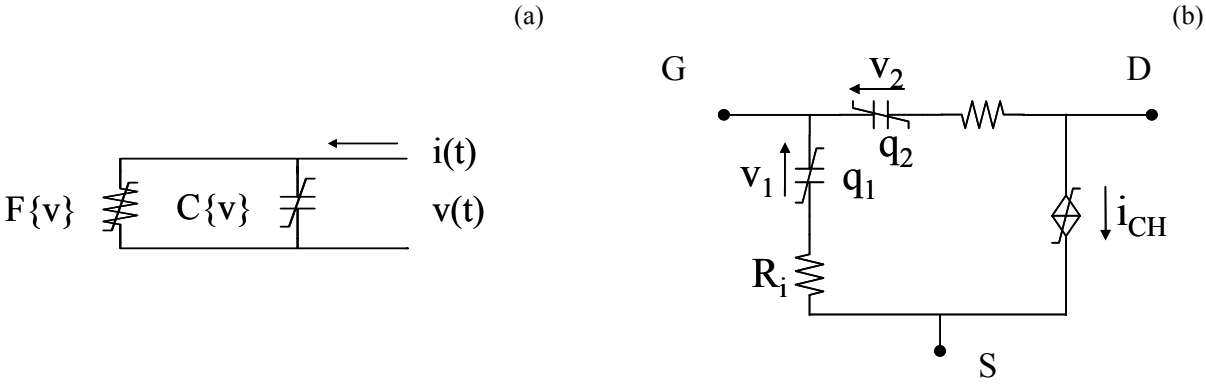

Fig. 1.4 (a) Quasi-static charge-controlled equation equivalent circuit representation. (b) Equivalent circuit of a two ports intrinsic device model accounting for non-quasi-static effects.

As stated for example by W. R. Curtice [4] and I. Angelov *et al.* [5], added series resistive elements may partially account for NQS phenomena. Owing to series resistors the capacitor charges q_1, q_2, the voltages v_1, v_2 and the controlled source i_{CH} of Fig.1.4 are also dependent on "past"

values of v_{GS}, v_{DS} applied to the intrinsic device. This is a circuit way for taking into account "memory" effects due to the NQS phenomena. Delays can also be explicitly considered in the controlled current source [4], [5].

1.2.3 Black-box empirical modelling of the intrinsic device

In black-box empirical models the electron device is studied with a behavioural perspective: theoretical and mathematical tools such as state-space nonlinear equations or Volterra Series expansions are used to describe the electron device behaviour. This results in the loss of the insight view of the internal physics of the device, but it provides, at least in principle, technology independent approaches.

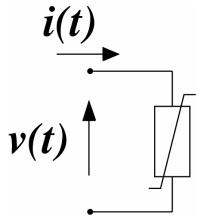

Fig. 1.5 Single-port intrinsic electron device described by the voltage controlled nonlinear dynamic functional (1.7).

Under the hypothesis of finite memory effects within the device and considering the single-port nonlinear electron device of Fig.1.5, the current can be expressed as a functional of the present and past voltage values in a "memory time" interval $0 \le \tau \le T_M$.

$$i(t) = \Psi\left[v(t-\tau)\right]_{\tau=0}^{T_M} \tag{1.7}$$

The most general modelling approach for systems characterized by nonlinear dynamic behaviour described by (1.7), is the Volterra Series expansion [6], which is based on a description of the nonlinear dynamic effects by means of multi-dimensional convolution integrals (1.8), which can be considered a generalization of the one-dimensional convolution integral for dynamic linear systems.

$$\begin{aligned} i(t) = &\int_0^{T_M} h_1(\tau_1)v(t-\tau_1)d\tau_1 + \iint h_2(\tau_1,\tau_2)v(t-\tau_1)v(t-\tau_2)d\tau_1 d\tau_2 + \\ &+ \iiint h_3(\tau_1,\tau_2,\tau_3)v(t-\tau_1)v(t-\tau_2)v(t-\tau_3)d\tau_1 d\tau_2 d\tau_3 + \ldots \end{aligned} \tag{1.8}$$

The identification of the Volterra kernels $h_1(\tau_1)$, $h_2(\tau_1, \tau_2)$, $h_3(\tau_1, \tau_2, \tau_3)$,… completely characterize the nonlinear dynamic system response.

The Volterra kernels identification is very difficult at microwave frequencies [7]: only few kernels can be identified and practically this description is well suited for the modelling of weak nonlinearities.

In 2003 Schreurs et al. [8] proposed a black-box modelling approach in which the nonlinear dynamic behaviour of the electron device is described by means of state-space-like equations:

$$\begin{aligned}\dot{\vec{\mathrm{X}}}(t) &= F_a\left(\vec{\mathrm{X}}(t), \vec{\mathrm{V}}(t)\right)\\ \vec{\mathrm{I}}(t) &= F_b\left(\vec{\mathrm{X}}(t), \vec{\mathrm{V}}(t)\right)\end{aligned} \tag{1.9}$$

where, in order to describe a voltage controlled device, the inputs are the controlling voltages $\vec{\mathrm{V}}(t)$, the outputs are the output currents $\vec{\mathrm{I}}(t)$ and $\vec{\mathrm{X}}(t)$ are the state variables of the device.

Considering a two-port device and rearranging (1.9), the space-state equations can be rewritten as

$$\begin{aligned}I_1(t) &= f_1\left(V_1(t), V_2(t), \dot{V}_1(t), \dot{V}_2(t), \ddot{V}_1(t), \cdots, \dot{I}_1(t), \dot{I}_2(t), \ldots\right)\\ I_2(t) &= f_2\left(V_1(t), V_2(t), \dot{V}_1(t), \dot{V}_2(t), \ddot{V}_1(t), \cdots, \dot{I}_1(t), \dot{I}_2(t), \ldots\right)\end{aligned} \tag{1.10}$$

where the required order of derivative must be determined. The identification of the functions f_1 and f_2 are carried out through fitting of large signal experimental data at various bias and input power levels by means of ANN.

1.2.4 Alternative Black-Box approach (The Modified Volterra Theory)

Considering a single-port electron device described by the functional (1.7), which holds under the hypothesis of finite duration of memory effects, after some algebraic manipulation the following equation can be written:

$$i(t) = \Psi\left|v(t-\tau)\right|_{\tau=0}^{T_M} = \Psi\left|v(t) + v(t-\tau) - v(t)\right|_{\tau=0}^{T_M}, \tag{1.11}$$

that is

$$i(t) = \tilde{\Psi}\left|v(t), e\left(t,\tau\right)\right|_{\tau=0}^{T_M} \tag{1.12}$$

where the new functional $\tilde{\Psi}$ explicitly depends on $e(t,\tau)=v(t-\tau)-v(t)$, the dynamic voltage deviation, which consider the difference between the past values of the controlling voltage, within the memory time of the device, and the present value of the controlling voltage.

If the Taylor expansion of $v(t-\tau)$ at $\tau=0$ is considered, i.e. $v(t-\tau)=v(t)-\dot{v}\cdot\tau+\ddot{v}\cdot\tau^2-...$, the functional (12) can be rewritten as:

$$i(t)=\tilde{\Psi}\left|v(t),-\frac{dv}{dt}\tau+\frac{d^2v}{dt^2}\tau^2-...\right|_{\tau=0}^{T_M}=f\left(v(t),\dot{v}(t),\ddot{v}(t),...\right) \tag{1.13}$$

which is analogous to the state-space description of the electron device.

The electron devices used for high frequency application show that their memory effects are also short with respect to their actual operating frequencies, that is $f<<1/T_M$. This basic feature of electron devices is justified both by experiment and by simulation and it is the so called *short duration of memory effects* phenomenon described by Filicori *et al.* in 1992 [9]. In that work it is also shown how the Volterra Series expansion can be rewritten as a function of the dynamic voltage deviations (Modified Volterra Series) and how under such an hypothesis the Volterra Series decrease their order.

Under the hypothesis of short duration of memory effects for an electron device described in a voltage controlled form, the voltage dynamic deviation in the functional (1.12) are small even with large voltage amplitudes which means that they are *small even at high nonlinear operations*.

This means that through the linearization of (1.12) with respect to $e(t,\tau)$, the modified Volterra Series expansion reduces its multi-dimensional order to the first order, without excessively increasing the linearization error [10]. This results in the following equation which describes the Nonlinear Integral Model (NIM) proposed in [9]:

$$i(t)=F\left[v(t)\right]+\int_0^{T_M} g\left[v(t),\tau\right]e(t,\tau)\,d\tau\,. \tag{1.14}$$

In (1.14) the first term $F\left[v(t)\right]$ represents the static behaviour of the electron device, while the second term represents a single-fold convolution integral between the small dynamic voltage deviations and the nonlinearly voltage-controlled impulse response $g\left[v(t),\tau\right]$. The NIM

formulation (1.14) is in analogy with the convolution which describes dynamic linear system, but is valid even in high nonlinear operating conditions.

This integral description of the high frequency nonlinear behaviour of an electron device is in analogy with the charge-controlled QS description of the intrinsic device also accounting for the high frequency NQS phenomena. In fact the Taylor expansion of $e(t-\tau)$ at $\tau = 0$, $v(t-\tau) - v(t) = -\dot{v}\cdot\tau + \ddot{v}\cdot\tau^2 - \ldots$, leads to the following modification of equation (1.14):

$$\begin{aligned} i(t) &= F\left[v(t)\right] + \left(-\int_0^{T_M} g\left[v(t),\tau\right]\ \tau\ d\tau \right)\frac{dv}{dt} + \left(\int_0^{T_M} g\left[v(t),\tau\right]\ \tau^2\ d\tau \right)\frac{d^2v}{dt^2} + \ldots = \\ &= F\left[v(t)\right] + F_1\left[v(t)\right]\frac{dv}{dt} + F_2\left[v(t)\right]\frac{d^2v}{dt^2} + \ldots \end{aligned} \tag{1.15}$$

where

$$F_1\left[v\right] = -\int_0^{T_M} g\left[v,\tau\right]\cdot\tau\, d\tau = C\left[v\right] \tag{1.16}$$

$$F_n\left[v\right] = \frac{(-1)^n}{n!}\int_0^{T_M} g\left[v,\tau\right]\cdot\tau^n\, d\tau \tag{1.17}$$

the term defined by (1.16) accounts for the quasi-static effects, while the terms defined by (1.17) account for the non-quasi-static effects. Hence (1.15), (1.16) and (1.17) show that the NIM is a black-box model which account for high frequency NQS effects and it is equivalent to the charge-controlled-based models. In fact at relatively low frequencies this limit holds

$$\lim_{\omega T_M \to 0}\left\{ \int_0^{T_M} g\left[v(t),\tau\right] e(t,\tau)\ d\tau \right\} = \mathrm{C}\left[\mathrm{v}\right]\frac{dv}{dt} \tag{1.18}$$

and the NIM is analogous to a conventional QS model, while at higher frequencies, the higher order terms (1.17) introduce their effects, accounting for non-quasi-static effects.

The model given by eq. (1.14) can be implemented with some suitable approximations in HB-based circuit simulators and is suitable for identification on the basis of conventional static and small-signal measurements. However, in order to make the model implementation and its empirical characterisation easier, the integral convolution in eq. (1.14) may be approximated by a discrete

convolution, where the memory time T_M is divided into N_D elementary time slots (that is, $T_M = N_D \cdot \Delta\tau$). In particular, the discretized model is expressed as

$$i(t) \cong F_{DC}\left[v(t)\right] + \sum_{p=1}^{N_D} g_p\left[v(t)\right] \cdot \left[v(t - p\Delta\tau) - v(t)\right] \tag{1.19}$$

where the dynamic current contribution, given by the summation term in (1.19), represents the nonlinear discrete convolution (NDC) model [10], which is fully identified by the N_D real functions $g_p[v(t)]$, identified through a linear least square fitting of the model to the measured DC and Small-Signal multi-bias device characteristics.

1.2.5 Modelling of the Low-Frequency Dispersive Phenomena

Electron devices used in high operating frequencies show low-frequency dispersive phenomena due to charge-trapping in spurious energy levels (in both deep-bulk and surface regions) and device self-heating. From a behavioural point of view, these phenomena results in the frequency dispersion of the measured trans-admittance and output impedance of the device (see Fig.1.6) and in a very different device I/V characteristics under static and dynamic conditions (see Fig.1.7).

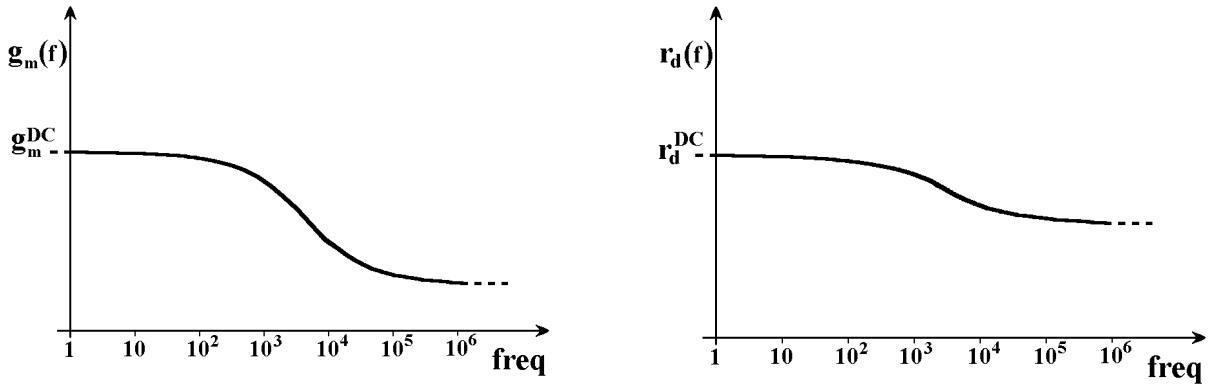

Fig. 1.6 Low frequency dispersion of the measured device trans-admittance and output impedance due to the charge-trapping phenomena and device self-heating.

Unfortunately, dynamic dispersive phenomena due to self-heating and charge-trapping effects must be also considered whenever accurate nonlinear modelling is needed. The time constants involved in this kind of dynamics are typically much longer than the quasi-static and non-quasi-static dynamics and much longer than the typical operation period at microwave frequencies. They are usually considered in the range from tens of [μs] to even [s], corresponding to a frequency dispersion of the device characteristics in the range from few [Hz] to hundreds of [kHz].

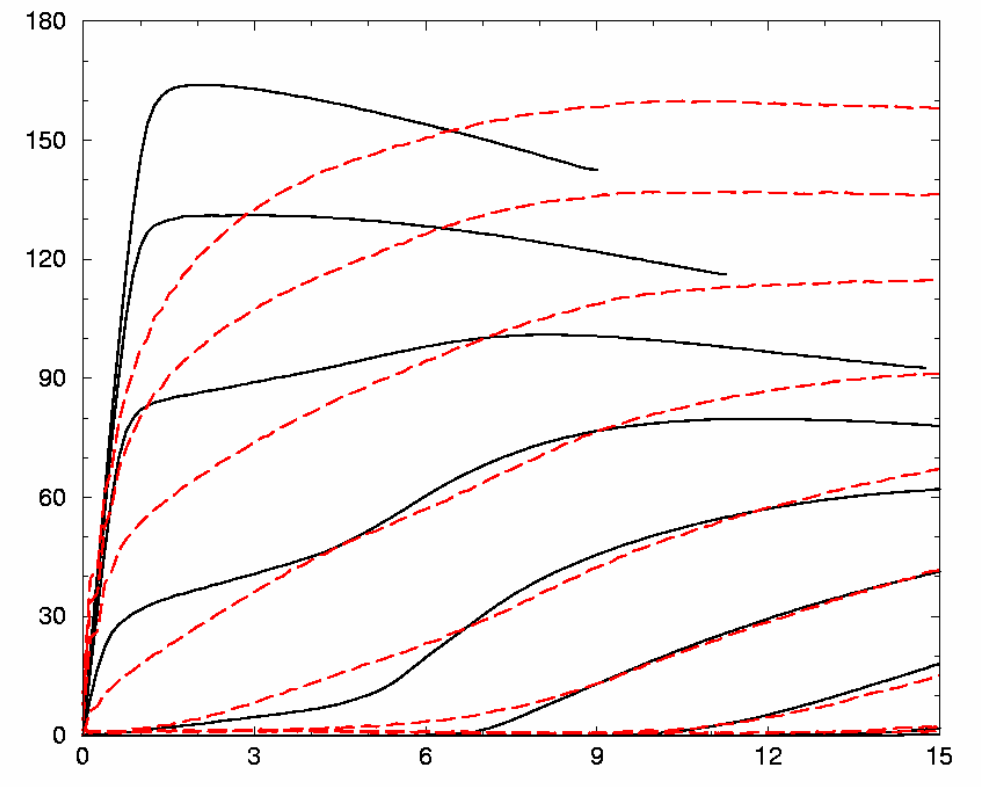

Fig. 1.7 Measured I/V characteristics of the device showing its different behaviour under static (black lines) and pulsed dynamic (dashed red lines) operations.

Considering the voltage-controlled description of the intrinsic electron device behaviour expressed by the functional (1.7) or, equivalently, by the functional (1.12), can be modelled by a new functional Φ which also depends on the additional state variables $\mathbf{x}(t)$ and $T_j(t)$, which are the trap filling status and the junction temperature respectively.

Considering a two-port electron device and hence a vectorial formulation, the device behaviour can be expressed as

$$\mathbf{i}(t) = \Phi\left|\mathbf{v}(t-\tau), T_j(t), \mathbf{x}(t)\right|_{\tau=0}^{T_M}. \qquad (1.20)$$

Since the empirical device model aimed at the prediction of the device nonlinear behaviour at microwave or millimetre-wave frequencies, the additional state variables may be simply replaced by their static values T_{j0} and $\mathbf{X}_0$, respectively. In fact, all the spectral components of the signals involved are in this case above the upper cut-off frequencies of the dispersive effects.

The junction temperature depends on the instantaneous dissipated power and on the case temperature of the electron device, while the trap-filling status depends on the instantaneous

voltages applied to the device ports. Considering the fact that only the static values of the additional state variables can be taken into account and considering a constant case temperature, the following equations hold:

$$\begin{aligned} T_{j0} &= F_T[P_0] \\ \mathbf{X}_0 &= F_{\mathbf{X}}[\mathbf{V}_0, T_{j0}] \end{aligned} \tag{1.21}$$

where F_T and $F_{\mathbf{X}}$ are suitable algebraic functions and $\mathbf{V}_0$ and P_0 are the average voltage and dissipated power values in the actual dynamic conditions. Substituting (1.21) in (1.20) the following modified functional can be obtained:

$$\mathbf{i}(t) = \tilde{\Phi}\left|\mathbf{v}(t-\tau), P_0, \mathbf{V}_0\right|_{\tau=0}^{T_M} \tag{1.22}$$

Eq. (1.22) is still too general to be directly used for device modelling; thus, it is simplified here by introducing a linearization with respect to suitable variables, which are now defined. To this aim, a new instantaneous entity is introduced as follows:

$$p_S(t) = F_{DC}^i[\mathbf{v}(t)] \cdot v_i(t) \tag{1.23}$$

where F_{DC}^i is the *i*-th component of the static current of the intrinsic device at a constant case temperature. The quantity $p_S(t)$ represents a virtual (that is, purely mathematical) instantaneous power corresponding at every time instant to the power which would be dissipated in the presence of a constant applied voltage equal to $v_i(t)$.

After some simple algebraic manipulation (1.23) becomes

$$\mathbf{i}(t) = \tilde{\Phi}\left|\mathbf{v}(t-\tau) - \mathbf{v}(t) + \mathbf{v}(t), P_0 - p_S(t) + p_S(t), \mathbf{V}_0 - \mathbf{v}(t) + \mathbf{v}(t)\right|_{\tau=0}^{T_M} \tag{1.24}$$

and considering that $p_S(t)$ is a purely algebraic function of $v_2(t)$, a new functional can be defined,

$$\mathbf{i}(t) = \Upsilon\left|\mathbf{v}(t), \mathbf{v}(t-\tau) - \mathbf{v}(t), p_S(t) - P_0, \mathbf{v}(t) - \mathbf{V}_0\right|_{\tau=0}^{T_M}. \tag{1.25}$$

Aside from its dependence on the instantaneous applied voltages, the new functional Υ depends on three new variables: the dynamic voltage deviation $\mathbf{v}(t-\tau) - \mathbf{v}(t)$, the instantaneous power

deviation $p_S(t)-P_0$, which is related to the device self heating and the instantaneous voltage deviations $\mathbf{v}(t)-\mathbf{V}_0$, which are related to the device trap filling status.

The linearization of (1.25) with respect of the dynamic voltage deviation leads to the following equation

$$\mathbf{i}(t)=\mathbf{F}_{LF}\left[\mathbf{v}(t),p_S(t)-P_0,\mathbf{v}(t)-\mathbf{V}_0\right]+\int_0^{T_M}\mathbf{g}\left[\mathbf{v}\left(t\right)\right]\left[\mathbf{v}(t-\tau)-\mathbf{v}(t)\right]d\tau \tag{1.26}$$

where the integral term accounts for the purely dynamic contribution to the device current due to reactive effects in the presence of very fast-varying signals (that is, microwave and millimetre-wave ranges), while the $\mathbf{F}_{LF}$ nonlinear function represents the static device current, when the case is kept at a constant temperature, including also the deviations of the dynamic device current due to self-heating and the charge-trapping phenomena. Substantially $\mathbf{F}_{LF}$ account for the nonlinear low-frequency dynamic behaviour of the electron device. Eq. (1.26) is the formulation of the NIM when low-frequency dispersive phenomena must be taken into account in the device empirical model.

Many empirical models based on (1.26) have been proposed (e.g. [10], [11]). In this paragraph only [11] will be exploited because it is identified on the basis of DC and Small-Signal (SS) low-frequency parameters [11] or low-frequency Large-Signal (LS) sinusoidal excitation (as recently proposed in [12]). It is also very suitable for the implementation in both equivalent circuit and Black-Box models. Such a model is based on the assumption that the macroscopic dynamic effect due to traps can be described in terms of a distributed electrical coupling (with very low cut-off frequency) between the gate-drain electrodes and the semi-insulator bulk ('self-backgating').

Such a 'self-backgating' model proposed in [11] expresses the $\mathbf{F}_{LF}$ function as follows

$$\mathbf{F}_{LF}\left[\cdot\right]=\begin{bmatrix}F_{LF}^1[\mathbf{v}(t)]\\ F_{LF}^2[\mathbf{v}(t),p_S(t)-P_0,\mathbf{v}(t)-\mathbf{V}_0]\end{bmatrix}=\begin{bmatrix}F_{DC}^1[\mathbf{v}(t)]\\ [1+k\cdot(p_S(t)-P_0)]\cdot F_{DC}^2[\mathbf{v}_m(t)]\end{bmatrix} \tag{1.27}$$

where

$$\mathbf{v}_m(t)=\mathbf{v}(t)+\begin{bmatrix}\alpha_G & \alpha_D\\ 0 & 0\end{bmatrix}\cdot\left(\mathbf{v}(t)-\mathbf{V}_0\right). \tag{1.28}$$

In (1.27) and (1.28), F_{DC}^i are the static current characteristics, and α_G, α_D, and k are suitable scalar coefficients to be determined.

This model treats the low-frequency dispersive phenomena by controlling the static drain current with an equivalent gate voltage, which accounts for the trapping phenomena within the device, and multiplying the obtained drain current by a correcting factor, which accounts for the device self-heating.

For what concern the equivalent circuit modelling of the low-frequency dispersive phenomena, many solutions have been also proposed [13]-[18].

1.3 Modelling of the Extrinsic Parasitic Network

The modelling of the linear extrinsic parasitic network of Fig.1.1 is another important aspect of the empirical modelling of electron devices.

Considering the typical device layout of a FET for on-wafer measurements of Fig.1.8 it is clear that the intrinsic device (which is physically related to the finger region of the device) is connected to the external world through the gate and drain access lines and the source via holes. Although the design of those structures aimed to minimize their parasitic effects, these latter cannot be neglected at the typical frequencies of operation of the device.

In conventional approaches, the modelling of the linear extrinsic parasitic network is carried out by means of an equivalent circuit (also for Black-Box modelling approaches), which is identified by means of the measured characteristics of the electron device.

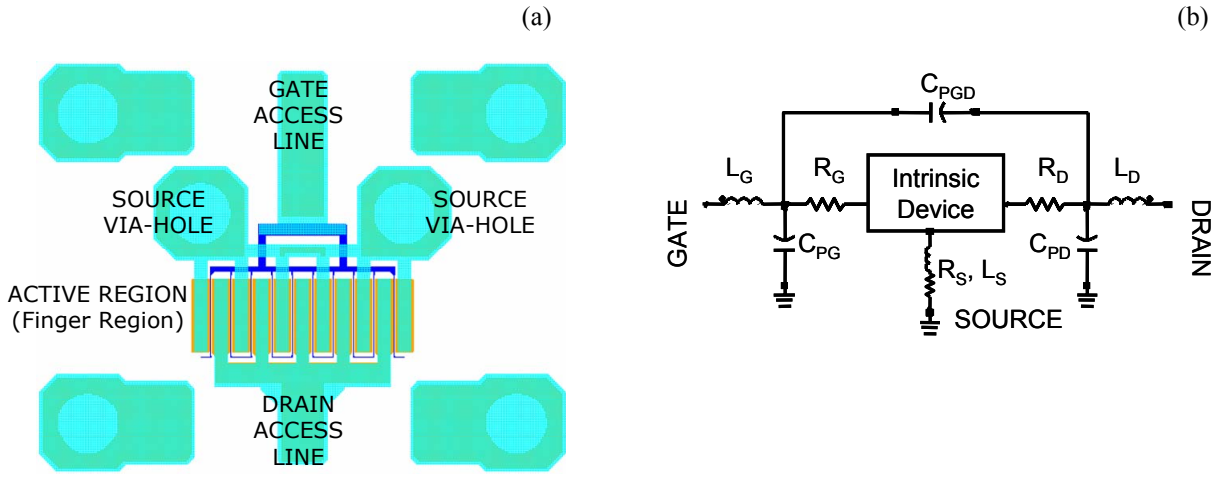

Fig. 1.8 (a) Typical layout of a multi-finger FET transistor for on-wafer measurements. (b) Typical topology of lumped component modelling the linear extrinsic parasitic network.

The topology of the equivalent circuit describing the extrinsic parasitic network, is shown in Fig.1.8. The series elements account for the series parasitic effects (resistive and inductive effects)

due to the gate and drain accesses, the gate and drain manifolds and the source via holes and air bridge. The capacitive parallel shell accounts for the pad capacitances and all the capacitive coupling between the finger metallizations. In many recent works the capacitance shell is placed outermost in order to simplify the de-embedding procedure.

The values of the lumped extrinsic elements can be obtained by several techniques proposed in many works which can be found in the literature. Most of them aimed to the extraction of a broadband multi-bias linear (i.e. Small-Signal) equivalent circuit electron device model, describing also the linear extrinsic element extraction procedure.

The linear Equivalent Circuit Parameters (ECP) extraction techniques are based on different methods. Optimizer-based extraction techniques are in widespread use, but they suffer from the non-uniqueness [19] of solutions. Improvements have been aimed e.g. at taking into account additional measurements [20], using a partitioning approach [21], or an automatic decomposition technique [22], but uncertainties are still existing with respect to the starting value problem. Fast analytical techniques [23]-[27] need special test structures or additional measurement steps such as dc and/or RF characterization of FET's under forward-bias condition. Such sequentially derived solutions may yield large errors in FET modelling [28]. Using multi-circuit measurements [29] the model parameters can uniquely be identified, but the number of optimization variables increases rapidly. A purely analytical reverse solution [30] can only be applied under the assumption of almost ideal measured S-parameters.

Both analytical and optimizer-based conventional techniques use some simplifications occurring at particular bias conditions. Analytical techniques use them in order to derive simpler analytical description of the electron device equations, while the optimizer-based techniques use them in order to derive the initial condition of the optimization problem. Often the simplifications used are those obtained with an unbiased drain with the device operating in the so called "Cold FET" conditions. F. Diamand *et al.* [23] in 1982 presented a new measurement method of the parasitic series impedances of microwave MESFETs based on "Cold FET" condition. "Cold FET" condition means that the common source device is biased at zero drain voltage, that is $V_{DS} = 0$ V. In such condition the region under the gate can be described by the distributed, uniform, R-C transmission line of Fig.1.9, leading to a simple analytical model.

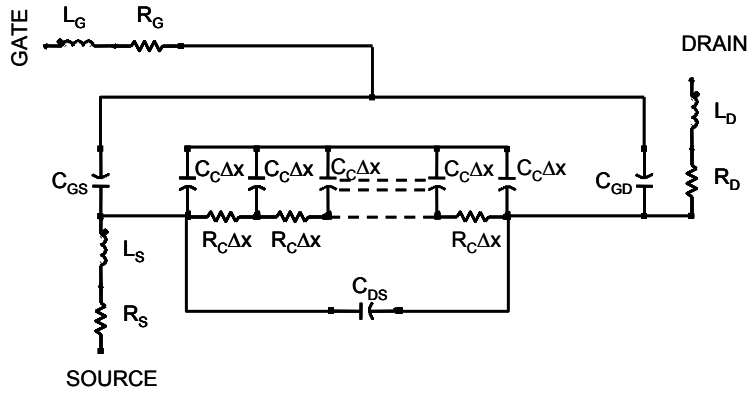

Fig. 1.9 Equivalent circuit model proposed in [23] for V_{DS} = 0 V.

In Fig.1.9 the pad capacitances are neglected. The device equivalent circuit is composed by the R-C transmission line modelling the region under the gate, the parasitic lumped series element and the lumped capacitances C_{GS}, C_{GD}, C_{DS}. The total capacitance of the depletion layer under the gate is C_c, the total channel resistance is R_C. C_{GS} and C_{GD} represent the fringing capacitances due to the extension of the depleted layer between the gate and source at one side and the gate and drain at the other side, and C_{DS} is the inter-electrode capacitance between the drain and source. Both pad capacitances C_{PG} and C_{PD} can be neglected throughout this section to ease the analysis without a loss of generality.

The analytic description of the network of Fig.1.9 can be simplified if the electrical length of the transmission line is short. This assumption can be satisfied under two conditions: a channel opening higher than 20% of the total channel height and a low frequency band. The former condition is important so that the value of R_C is reasonably small. This condition is already satisfied because the gate is always biased throughout the analysis at $V_{GS} \geq 0$. The latter condition is met for frequencies up to about 10 GHz. Therefore, a subfrequency band of the measurements should be used so that the maximum frequency of the subband is 10 GHz. This assumption it is called low-frequency-open-channel approximation. Assuming that it holds for all the capacitances of Fig.1.9, the impedance matrix which define the device $\mathbf{Z} = \mathbf{R} + j \cdot \mathbf{X}$ is given by

$$\mathbf{R} = \begin{bmatrix} R_S + R_G + \frac{1}{3}\frac{C_C + 3C_{DS} + 3C_{GD}}{C_C + C_{DS} + C_{GD}} R_C & R_S + \frac{1}{2}\frac{C_C + 2C_{GD}}{C_C + C_{DS} + C_{GD}} R_C \\ R_S + \frac{1}{2}\frac{C_C + 2C_{GD}}{C_C + C_{DS} + C_{GD}} R_C & R_S + R_D + R_C \end{bmatrix}$$

$$\mathbf{X} = \begin{bmatrix} \omega(L_S + L_G) - \frac{1}{\omega(C_C + C_{GS} + C_{GD})} & \omega L_S \\ \omega L_S & \omega(L_S + L_D) \end{bmatrix} \qquad (1.29)$$

In [23] is shown how starting from multi-bias "Cold FET" device measurements and fitting the measured Z-parameters to the analytical model (1.29), the values of the extrinsic parasitic elements can be found. Unfortunately the proposed technique requires that some technological parameters (such as the built-in potential) are known a priori.

In 1988 Dambrine et al. [24] extended the analytical technique proposed by Diamand considering the distributed R-C network of Fig.1.10 representing the FET channel under the gate at V_{DS} = 0 V.

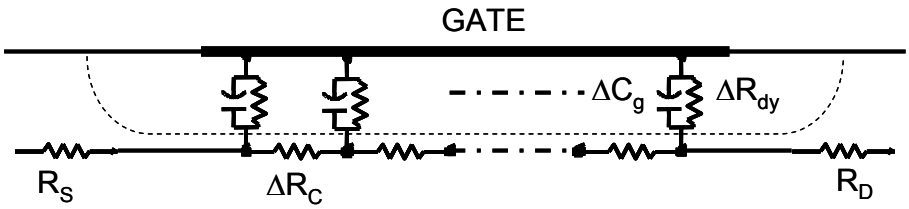

Fig. 1.10 Sketch of the distributed R-C network under the gate as proposed in [24].

According to Fig. 1.10, for any gate biasing condition, the following impedance matrix describing the intrinsic device can be written

$$\mathbf{Z} = \begin{bmatrix} R_C/3 + z_{dy} & R_C/2 \\ R_C/2 & R_C \end{bmatrix} \qquad (1.30)$$

where R_C is the channel resistance under the gate and z_{dy} is the equivalent impedance of the schottky barrier which can be written as follows:

$$z_{dy} = \frac{R_{dy}}{1 + j\omega C_g R_{dy}} \qquad \text{with} \quad R_{dy} = \frac{nkT}{qI_g} \qquad (1.31)$$

In (1.31) n is the ideality factor, k the Boltzmann constant, T the temperature, C_g the gate capacitance and I_g the dc gate current. As the gate current increases, R_{dy} decreases and C_g increases but the exponential behaviour of R_{dy} versus the gate-source voltage (which is increased as well) is the dominant factor; consequently the term $\omega R_{dy} C_g$ tends to zero for gate current densities close to 10^8 [A/m^2]. For such a gate current, the capacitive effect of the gate disappears and the z_{11} parameter becomes real. Besides the influence of the C_{PG} and C_{PD} parasitic capacitances of Fig.1.8 is negligible and consequently the extrinsic $\mathbf{Z}$ matrix is simply determined by adding the parasitic resistances and inductances of Fig.1.8 to the intrinsic $\mathbf{Z}$ matrix (1.30). Thus we have

$$\mathbf{Z} = \mathbf{R} + j\mathbf{X} = \begin{bmatrix} R_S + R_G + \dfrac{R_C}{3} + \dfrac{nkT}{qI_g} & R_S + \dfrac{R_C}{2} \\ R_S + \dfrac{R_C}{2} & R_S + R_D + R_C \end{bmatrix} + j \begin{bmatrix} \omega(L_S + L_G) & \omega L_S \\ \omega L_S & \omega(L_S + L_D) \end{bmatrix} \quad (1.32)$$

In (1.32) it is shown that the imaginary part of the Z-parameters increases linearly versus frequency while the real part is frequency independent. In addition it must be noted that the real part of z_{11} increases as $1/I_g$. As shown in [24], the theoretical expression (1.32) of the Z-parameters of the device are in quite good agreement with the experimental data.

From the imaginary parts of the measured the parasitic inductances can be uniquely determined. Besides the Z-parameters' real parts provide three relations between the four unknowns R_G, R_D, R_S and R_C. At this step, an additional relation is needed to separate the four unknowns. This additional relation can be:

1) The value of the sum $R_S + R_D$ determined by some conventional method for example with the network analyzer using the real part of z_{22}.
2) The value of R_G if it can be provided from the resistance measurement from pad to pad.
3) The value of R_S and R_D provided by dc measurement.
4) The value of R_C if the channel technological parameters are known.

It is important to note that (1.32) holds only at high gate current and for devices with low metallization resistances. If those conditions are not met, the distribution effect shown in Fig.1.10 and expressed by (1.30) and (1.31) has to be taken into consideration.

The C_{PG} and C_{PD} parasitic capacitances are measured by suppressing the conductivity of the channel. As a matter of fact, at zero drain bias and for a gate voltage lower than the pinch-off voltage V_P, the intrinsic gate capacitance (i.e., under the gate) cancels, as does the channel conductance. Under these biasing conditions, the FET equivalent circuit is shown in Fig.1.11. In this figure C_b represents the fringing capacitance due to the depleted layer extension at each side of the gate. For frequencies up to a few gigahertz, the resistances and inductances have no influence on the imaginary part of the Y-parameters and the $\mathbf{Y}$ matrix simply is

$$\mathbf{Y} = \begin{bmatrix} j\omega(C_{PG} + C_b) & -j\omega C_b \\ -j\omega C_b & j\omega(C_{PD} + C_b) \end{bmatrix} \tag{1.33}$$

The analytic behaviour stated by (1.33) is in quite good agreement with the Y-parameters measurements in "Cold FET" pinched-off conditions.

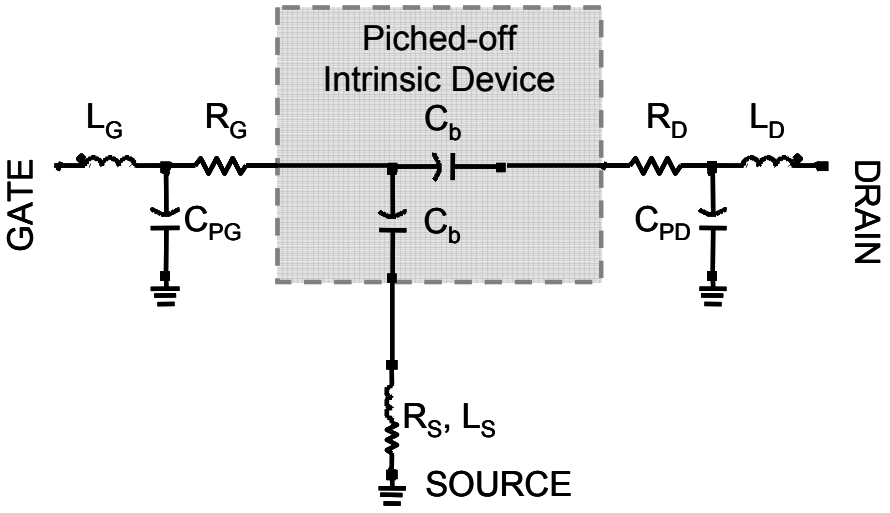

Fig. 1.11 Small-signal equivalent circuit of a FET at zero drain bias voltage and gate voltage lower than the pinch-off voltage.

In the context of empirical modelling, the "Cold FET" characteristics are very suitable for the identification of the extrinsic parasitic network of an electron device as shown by Dambrine [24] and by other authors. For example in 1990 Berroth and Bosh [25] extended the Dambrine's method in order to derive a broadband small-signal equivalent circuit for microwave FETs.

The main drawback of those techniques is the additional information needed in order to extract the correct values of the series resistances. Another problem is also shown in Fig.1.12.

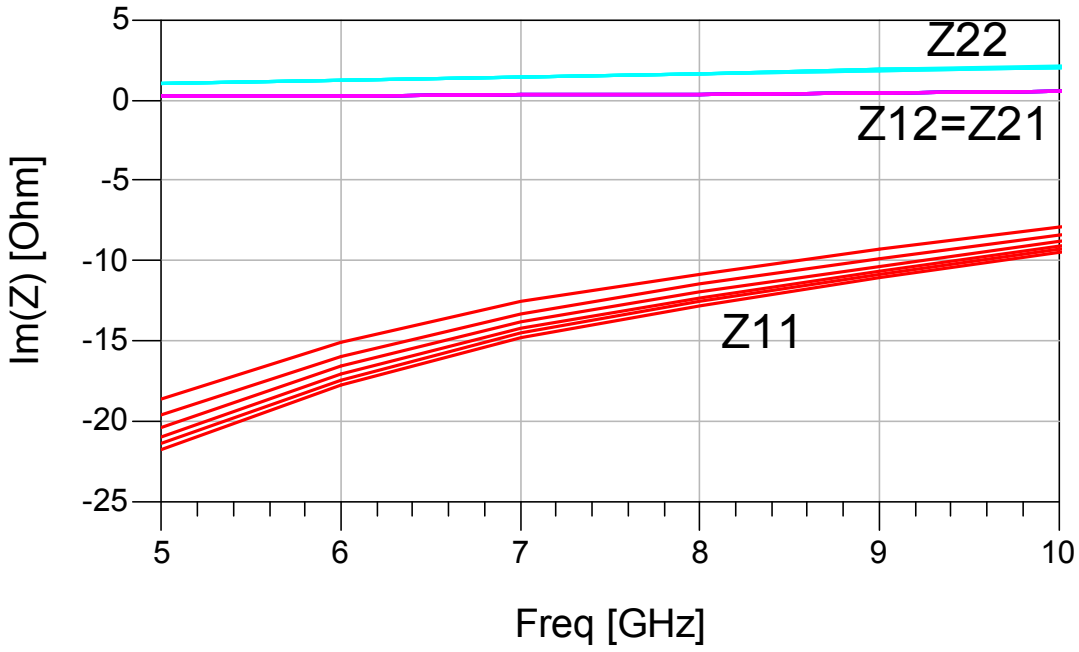

Fig. 1.12 Imaginary part of the measured Z-parameters of a 0.25x900 μm2 GaAs PHEMT for different forward gate bias conditions.

The figure shows that the measured z_{11} of an actual PHEMT device is in contrast with the analytic behavior of eq. (1.32). This is due to the fact that the hypothesis of high gate current densities is not verified and the measured imaginary part of z_{11} presents an high capacitive effect as expected in (1.29).

In literature can be found many works which solve the mentioned problems. For example in 1994 Lin and Kompa [31] proposed a method to estimate the parasitic elements of Fig.1.8 from pinch-off measurements, in order to generate the initial guess of their optimization-based technique. Their method had been extended in 2003 by Khalaf and Riad [32] using also "Cold FET" forward bias measurements in order to reduce the measurement noise dependence of the extracted values. In 1996, instead, Yanagawa *et al.* [33] proposed an analytical extraction procedure of all the parasitic elements of Fig.1.8 using only "Cold FET" pinched-off measurements.

Let consider for example the extraction of the extrinsic parasitic element of a 0.25x900 μm^2 GaAs PHEMT by means of the Yanagawa [33] direct method. Only a single bias broadband S-parameters measurement in pinch-off condition is needed. Thus the device has been biased at V_{GS} = -1.4 V ($V_P = -1.1\ V$) and V_{DS} = 0 V and its S-parameters have been measured in the frequency range [4 – 110 GHz]. Converting the S-parameters to Y-parameters it is found that for low-frequency (i.e. in the range [4 – 10 GHz]) these latter are in agreement with the behaviour expressed

in (1.33). Thus the value of C_{PG} and C_{PD} parasitic elements can be deduced. Since the equivalent circuit of Fig.1.12 neglect the effect of the inter-electrode capacitance C_{DS} and C_{PD} results overestimated, its value is selected equal to the value of C_{PG}: this is a good approximation when the device has equal gate and drain access structures. Fig.1.13 shows the model (1.33) fitting to the device measurement in the low-frequency range of validity of the model.

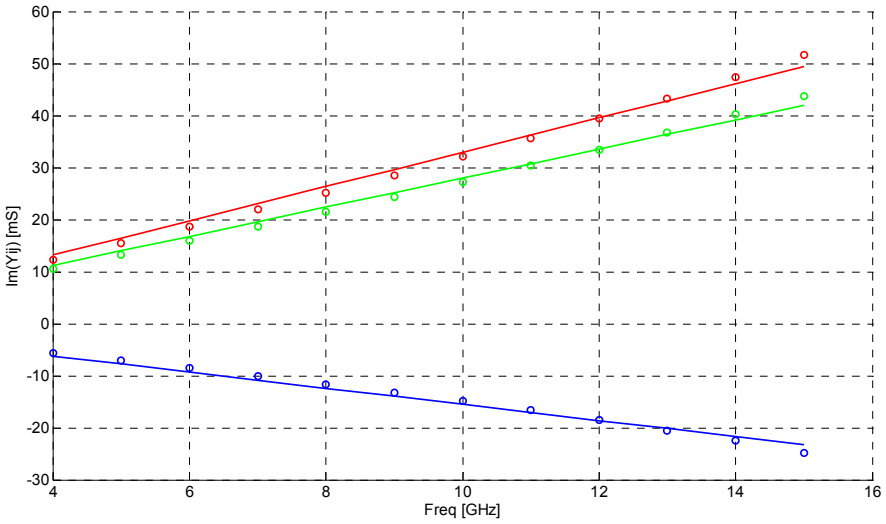

Fig. 1.13 Imaginary part of the admittance parameter of the 0.25x900 μm^2 GaAs PHEMT in the low-frequency range [4 – 10 GHz] of validity of model (1.33). Measured Y-parameters (circles) versus model fitting (lines). $Y_{12} = Y_{21}$ (blue), Y_{11} (red) and Y_{22} (green).

After de-embedding the effect of the extracted pad capacitances, the other six extrinsic elements can be determined from the Z-parameters as shown in [33]. In fact both inductances and resistances are extracted at very high frequencies (i.e. in the range [40 – 80 GHz]), in order to increase the accuracy of these extrinsic elements by decreasing the intrinsic capacitive effects. As shown in Fig.1.14 and Fig.1.15, the inductances are determined by the slopes of the straight lines approximating $\omega \mathrm{Im}(Z_{ij})$ vs. ω^2, while the resistances are obtained from the slope of the straight lines approximating $\omega^2 \mathrm{Re}(Z_{ij})$ vs. ω^2.

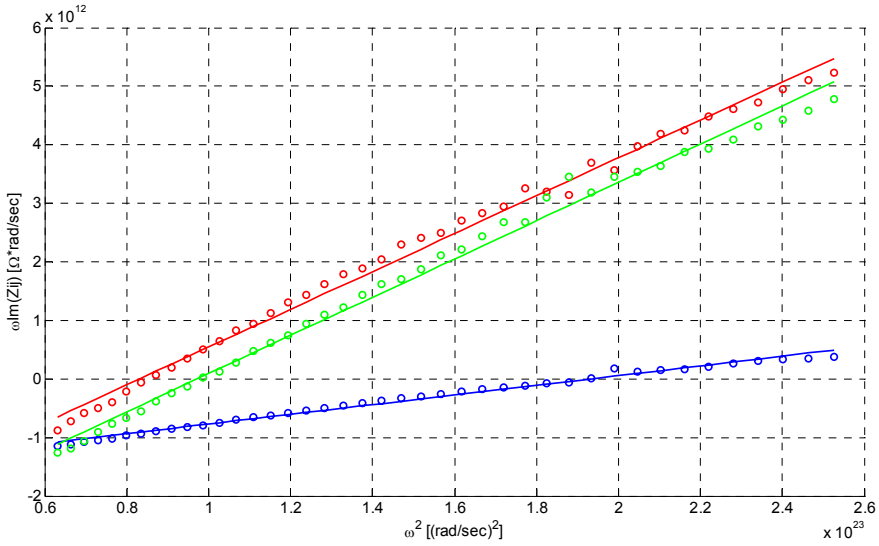

Fig. 1.14 Plot of $\omega \mathrm{Im}(Z_{ij})$ vs. ω^2 of the 0.25x900 μm^2 GaAs PHEMT in the high-frequency range [40 – 80 GHz]. $Z_{12} = Z_{21}$ (blue), Z_{11} (red) and Z_{22} (green).

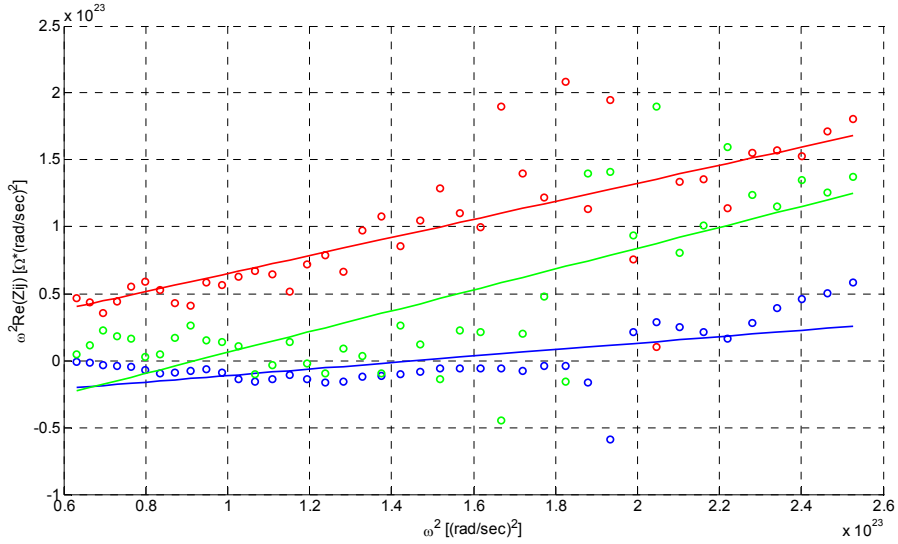

Fig. 1.15 Plot of $\omega^2 \mathrm{Re}(Z_{ij})$ vs. ω^2 of the 0.25x900 μm^2 GaAs PHEMT in the high-frequency range [40 – 80 GHz]. $Z_{12} = Z_{21}$ (blue), Z_{11} (red) and Z_{22} (green).

In this example the extracted values of the 0.25x900 μm^2 GaAs PHEMT extrinsic parasitic elements are: $C_{PG} = C_{PD} = 39.0$ fF, $R_G = 0.43$ Ω, $R_D = 0.54$ Ω, $R_S = 0.24$ Ω, $L_G = 24.0$ pH, $L_D = 24.4$ pH, $L_S = 8.3$ pH.

Although the above techniques are the most used for the identification of the extrinsic lumped parasitic elements, it should be noticed that the Cold FET conditions are potentially inaccurate because they use the device in operating conditions which are different from the actual conditions used in MMIC designs. Hence other techniques have been developed using so called "Hot FET"

measurements where the device is biased in the actual operating condition. This kind of techniques are used for example in [34] where the parasitic elements of Fig.1.8 are extracted once the resistances have been calculated from DC measurements.

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CHAPTER 2

SCALING OF EMPIRICAL MODELS

2.1 Introduction to the scalability problem.

Micro- and millimetre-wave Integrated Circuit (MMIC) design requires electron device models which accurately describe the linear and nonlinear behaviour up to extremely high frequencies. When incorporated into circuit simulation routines, accurate device models allow engineers to design and optimize circuit performance prior to fabrication. Standing alone, device models often provide the information required when choosing an appropriate device for a specific application or when making decision concerning device processing [1]. The combination of physically based models and monolithic circuit technology potentially allows designers to perform simultaneous device and circuit optimization during the design process.

An important task facing both circuit designers and design fabrication engineers is evaluating the ultimate potential of a device for specific applications. This information can be important for choosing an appropriate device for particular applications. Although such an evaluation can be accomplished by developing a model for the device and optimizing the performance using a circuit simulation routine, such an approach is usually prohibitively time consuming. Instead, the problem is often first approached using easily derive performance figures of merit (FOMs).

The FOMs strictly depend on the technological process, e.g. the device gate length [1], and their evaluation can be accomplished only through physically based models, but once the technology has been selected, many FOMs can be estimated directly from device empirical models.

In fact, in addiction to their dependence on the device bias conditions, most of the FOMs depend on some device geometrical parameters, such as the number of gate fingers and the gate width, dependences which can be somehow taken into account also by empirical models. Hence the

availability of empirical models of different-in-size device is a key aspect for MMIC's designers, avoiding the characterization and the extraction of an empirical model for each device size.

The scalability property of an empirical model could be comprehended as the extrapolation capability of the empirical model with respect to the device geometrical parameters. This important property allows the designer to select the best device for the particular application and the best device for the different blocks composing the overall MMIC (e.g. the driver stage and the power stage of a power amplifier).

Moreover, in order to extract an empirical model valid for the entire technological process, the availability of a scalable empirical model allows to the characterization of only one device (or only few devices), providing a less time consuming characterization phase.

Fig.2.1 represents again the general empirical model description showing the extrinsic parasitic network connecting the intrinsic device to the external terminals.

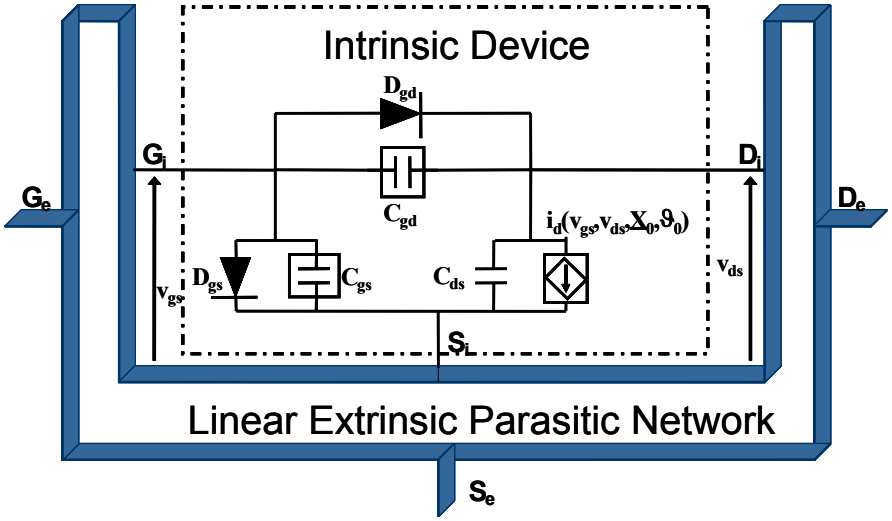

Fig. 2.1 Empirical electron device model. The model is composed by a linear extrinsic parasitic network connecting the nonlinear intrinsic device to the external world.

Many authors proposing scalable models [2]-[4], adopt the fundamental hypothesis that *the intrinsic device elements scale linearly with the periphery* of the device. This is a quite generally accepted conclusion which implicitly assumes that the intrinsic model is a sound representation of the "active part" of the electron device and, consequently, that the parasitic effects have been accurately modelled. In other words, the scalability of an electron device model strictly depends on the scalability of the linear extrinsic parasitic network of Fig.2.1.

The aim of this chapter is showing how conventional lumped parasitic networks, together with simple linear scaling rules, cannot provide the definition of accurate scalable models. In order to

overcome this problem either more complicate technology-dependent scaling rules or the use of distributed models had been proposed in the literature to provide scalability issues.

2.2 Conventional Scaling Rules

Conventional topologies adopted for the extrinsic parasitic networks of Fig.2.1 offer a poor link between technological process parameters and the corresponding device electrical response, providing poor model accuracy using conventional scaling rules [1]. Fig.2.2 shows the conventional description of the extrinsic parasitic network discussed in Chapter 1.3.

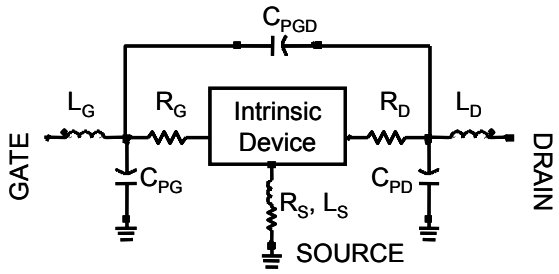

Fig. 2.2 Typical topology of lumped component modelling the linear extrinsic parasitic network.

Considering the gate series parasitic elements L_G, R_G, they account for the resistance and inductance associated to the gate fingers but also to the gate manifold. While the resistance and inductance of the paralleled gate fingers scale with linear relations with respect to the gate width and the number of fingers, the effect of the manifold cannot follow the linear rules and it may causes some inaccuracies in the scaled model. The same considerations hold for the drain series parasitic elements L_D, R_D. The source series parasitic elements L_S, R_S, instead, account for the resistance and inductance associated to the source metallization placed within the finger area and connected to the via holes through the air bridge. The air bridge and the via holes are responsible in this case of the inaccuracies which occur when using a simple linear approximation.

The shunt capacitance parasitic elements C_{PG}, C_{PD} and C_{PGD} account for both the gate and drain pad and manifold capacitive effects and the inter-electrode capacitances. All these capacitive effects don't scale linearly with the device periphery.

It is clear that simple linear rules lead to some inaccuracies which are emphasized at higher frequencies. This is the case of the scaling rules proposed in [1], where the extrinsic parasitic elements of Fig.2.2 scale according to the following rules:

$$\left(L_X\right)^{sc} = \left(L_X\right)^{ref}, \quad \text{where } x = G, D, S \tag{2.1a}$$

$$\left(C_X\right)^{sc} = \left(C_X\right)^{ref}, \quad \text{where x = PG, PD, PGD} \tag{2.1b}$$

$$\left(R_G\right)^{sc} = \left(R_G\right)^{ref} \cdot \frac{W^{sc} \cdot \left(N^{ref}\right)^2}{\left(N^{sc}\right)^2 \cdot W^{ref}}$$

$$\left(R_D\right)^{sc} = \left(R_D\right)^{ref} \cdot \frac{W^{ref}}{W^{sc}} \quad . \tag{2.1c}$$

$$\left(R_S\right)^{sc} = \left(R_S\right)^{ref} \cdot \frac{W^{ref}}{W^{sc}}$$

Rules (2.1a) and (2.1b) express that the parasitic inductances and capacitances do not scale with the device periphery, while rule (2.1c) expresses that the parasitic resistances scale with respect to the total gate width W (i.e. the total periphery of the device) and the number of gate fingers N. The subscripts 'sc' and 'ref' mean "scaled device" and "reference device" respectively.

In order to point out the inaccuracy of the scaling rules (2.1) a conventional Small-Signal (SS) Equivalent Circuit (EC) model has been extracted for a reference 4x50 μm PHEMT belonging to a 0.5 μm GaAs process. The SS-EC model has the linear extrinsic parasitic network defined as in Fig.2.2 and the conventional 7 element intrinsic EC of Fig.2.3.

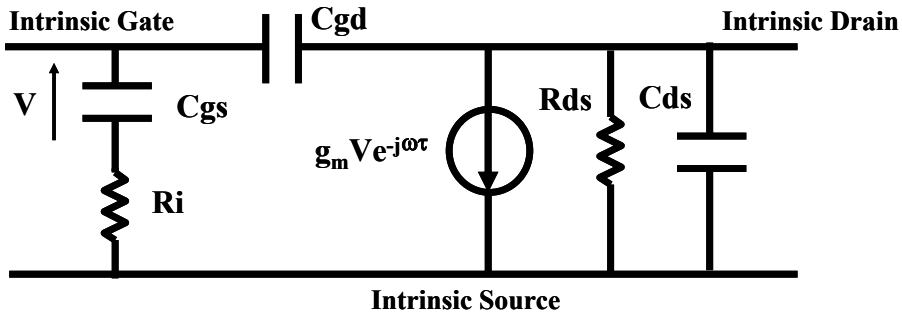

Fig. 2.3 Conventional 7 elements Small-Signal Equivalent Circuit for the intrinsic device.

The SS-EC model has been extracted for a typical class-A operation bias condition, identifying the extrinsic elements through the Yanagawa direct extraction method (as shown in Chapter 1.3) and the intrinsic element through CAD optimization. The values of the extracted parameters are shown in Table I.

TABLE I

Cpg [fF]	**Cpd [fF]**	**Rg [Ω]**	**Rd [Ω]**	**Rs [Ω]**	**Lg [pH]**	**Ld [pH]**	**Ls [pH]**
11.3	0.00	4.60	2.02	0.58	19.7	16.5	12.5
Cgs [fF]	**Cgd [fF]**	**Cds [fF]**	**Ri [Ω]**	**Rds [Ω]**	**gm [mS]**	**τ [ps]**	
262	18.6	46.6	0.75	472	66.0	1.45	

The SS-EC model predictions of the measured device behaviour is shown in Fig.2.4. It can be seen that the model is quite accurate up to the maximum measured frequency for all the scattering parameters.

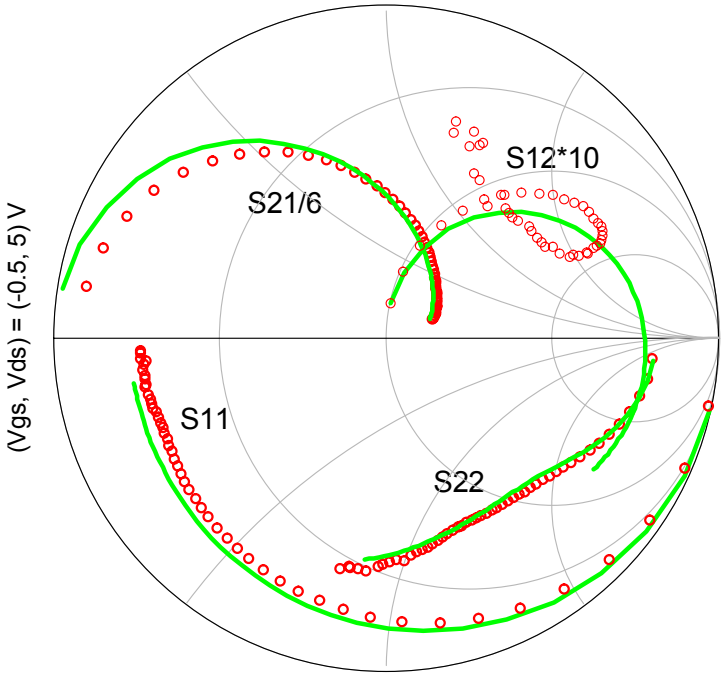

Fig. 2.4 SS-EC model prediction (lines) of the reference 4x50 μm PHEMT measured behaviour (circles). S-parameter in the frequency range [0.5 – 50 GHz] at V_{GS} = -0.5 V, V_{DS} = 5 V.

In order to predict the behaviour of different devices belonging to the same technological process, namely a 4x100 μm and a 2x100 μm PHEMTs, such a SS-EC model has been scaled according to rules (2.1) for the extrinsic parasitic elements and by linearly scaling the intrinsic elements according to [1].

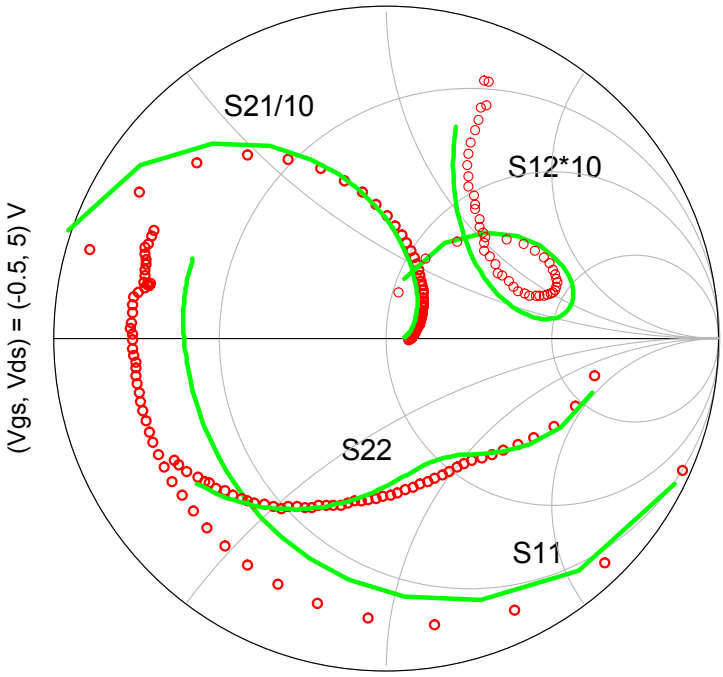

Fig. 2.5 SS-EC scaled model prediction (lines) of the 4x100 μm PHEMT measured behaviour (circles). S-parameter in the frequency range [0.5 – 50 GHz] at V_{GS} = -0.5 V, V_{DS} = 5 V.

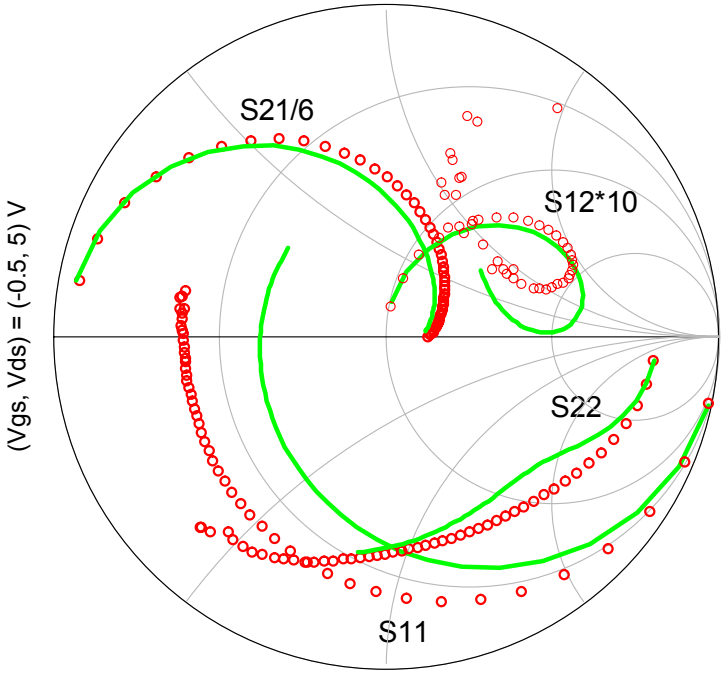

Fig. 2.6 SS-EC scaled model prediction (lines) of the 2x100 μm PHEMT measured behaviour (circles). S-parameter in the frequency range [0.5 – 50 GHz] at V_{GS} = -0.5 V, V_{DS} = 5 V.

The SS-EC scaled models predictions are shown in Fig.2.5 and Fig.2.6. These experimental results point out that the scaled models are inaccurate also at relatively low frequencies. This suggests that not only the conventional scaling rules (2.1) are inaccurate, but also that conventional

topologies adopted for the extrinsic parasitic networks offer a poor link between technological process parameters and the corresponding device electrical response.

This call for the definition of completely empirical and process-dependent scaling rules, based on the evaluation of the variation of the extrinsic elements with the dimension of the device [2]-[5], through very complicate procedures, even in conjunction with more complicate lumped networks [4], [5].

On the other hand, the solution is the use of purely distributed models [6]-[15], which maintain the link between the device geometrical parameters (such as number and width of fingers) by taking into account the propagation effects along and transversely the device fingers.

2.3 Lumped Topologies and Empirical Scaling Rules

In 1997 S. W. Chen *et al.* [2] report an approach for constructing scalable small-signal models for interdigitated power PHEMTs. The SS-EC model is defined by the topology of Fig.2.2 for the extrinsic parasitic network and the 7 element EC of Fig.2.3 for the intrinsic device. By using Dambrine's cold-FET direct extraction, the values of the equivalent circuit parameters (ECPs) have been extracted for a typical class-A operation bias condition, for five devices having different peripheries. By considering the extracted ECP values for the different peripheries, scaling rules for extrinsic components were found, and here briefly recalled:

$$\left(L_X\right)^{sc} = \left(L_X\right)^{ref}, \quad \text{where } x = G, D, S \tag{2.2a}$$

$$\left(C_X\right)^{sc} = \left(C_X\right)^{ref} \frac{N^{sc}}{N^{ref}} \cdot \left(\frac{S_{cpw}^{ref}}{S_{cpw}^{sc}}\right)^{0.38}, \quad \text{where } x = PG, PD \tag{2.2b}$$

$$\left(R_G\right)^{sc} = \left(R_G\right)^{ref} \cdot \frac{W^{ref}}{W^{sc}} \cdot \frac{L_g^{sc}}{L_g^{ref}}$$

$$\left(R_D\right)^{sc} = \left(R_D\right)^{ref} \cdot \frac{W^{ref}}{W^{sc}} \quad , \tag{2.2c}$$

$$\left(R_S\right)^{sc} = \left(R_S\right)^{ref} \cdot \frac{W^{ref}}{W^{sc}}$$

where the subscripts 'sc' and 'ref' mean "scaled device" and "reference device" respectively. N, W, L_g are the number of gate fingers, the width of gate finger and the length of gate finger respectively, while S_{cpw} is the spacing distance of the inner coplanar waveguide transmission line.

After taking a further look at the scaling rules (2.2) they are very similar to conventional rules (2.1). Considering the experimental results shown in [2] the proposed rules provide an improvement

in accuracy, specially on the S11 parameter prediction, but the overall predictions are still inaccurate at higher frequencies. Furthermore the empirical rule (2.2b) appears to be process-dependent at it must be reviewed when changing the technology.

The major drawback of approach [2] is the great amount of time required for characterization phase. In fact the same Cold FET measurements have to be carried out on different device sizes prior to derive the empirical scaling rules.

In 1997 Cojocaru and Brazil [3] addressed the issue of scalability in equivalent circuit-based models for FET's, emphasizing for the first time the particularly difficult problems associated with the scalability of DC/AC dispersion phenomena. The study had been carried out on devices from both MESFET (0.5 μm gate length) and PHEMT (0.25 μm gate length) foundry processes, with total gate widths between 60 – 1200 μm. They used a conventional topology for the extrinsic parasitic network and a slightly modified Cold FET direct extraction technique [3] as well as very simple linear scaling rules for the extrinsic ECPs. They put in evidence that the proper scaling of second order effects such as the DC/AC dispersion strongly influences the scalability of the model.

The shown experimental results point out that such a model scales very well with the periphery of the device, although the experimental validation is carried out only up to a relatively low-frequencies for the considered mm-wave process.

In 2000 Wood and Root [4] proposed a Small-Signal Multi-Bias (SS-MB) scalable model for mm-wave applications. The extrinsic parameters are a slightly more complex network than the conventional network of Fig.2.2, in an attempt to model the multi-finger gate and drain manifolds. As shown in Fig.2.7, two additional capacitance components are added to account for the interaction between the gate-source and gate-drain interdigitated metallizations.

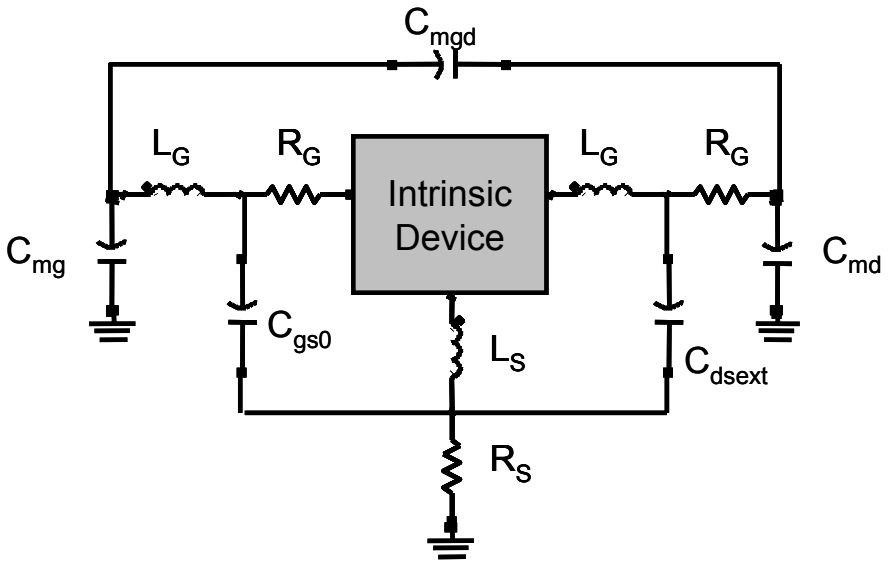

Fig. 2.7 The extrinsic parasitic network topology for the SS-MB scalable model proposed in [4].

An array of 0.25 μm gate length InGaAs-channel PHEMTs, with total gate widths from 30 to 480 μm and number of gate fingers from 2 to 12, was prepared and measured to determine the ECPs and their scaling rules [4].

A pinched-off gate condition was used to determine the extrinsic capacitances of the array of test FETs. First, the two-gate-finger devices were measured to estimate the variation with gate width of the gate capacitance and the drain-source capacitance. These relations were then used in the multi-finger devices to determine the influence of the manifold metallizations on the capacitances.

A new extraction method for the extrinsic Z-shell parameters had been proposed in [4]. It is based on optimizing the measured data over frequency. The drain-source voltage is set to zero, again eliminating the influence of the controlled current source from the equivalent circuit, and the gate bias is set to 0 V. Under these conditions, the intrinsic circuit of the FET can be reduced to a simple T-network in which the gate branch contains a parallel resistance/capacitance combination representing the gate-to-channel contact , and the source and drain branches are half the channel resistance, as shown in [4]. The value of the channel resistance was estimated by using a physical simulation to find the channel charge density at 0 V gate bias for the given device structures. After de-embedding the extrinsic capacitances, the branch impedance functions were fitted to the measured data using a rational function optimizer routine to determine the resistances and inductances. The complete extraction was accomplished in a two-pass process. In the first pass, *all* the extrinsic capacitance was subtracted from the measured data, and the optimizer produced initial values for the series resistances and inductances. In the second pass, the de-embedding process was

carried out in accordance with the equivalent circuit in Fig. 2.7. First, the outer capacitance shell was subtracted from the measured data, followed by the initial values of inductance, and then the second capacitance shell. At this point the optimizer was run to yield new values of branch inductance and resistance. The new value of inductance was added to the initial value to provide the final extrinsic inductance value. Two passes were considered sufficient.

That procedure had been carried out on some of the different devices of the array in order to derive the dependence on the gate width and number of finger of the ECPs. All the components in this equivalent circuit scale with gate width or number of fingers, or both according to the found empirical rules proposed in [4].

Although the SS-MB scalable model is very accurate up to millimetre-wave frequencies thank to the slight modification of extrinsic network of Fig.2.7, the approach [4] still needs a great amount of characterization data to find the empirical scaling rules. It also need the availability of two-gate-finger devices to derive the dependence of the capacitance shell on the gate width. Furthermore changing to another technological process, the proposed scaling rules could be different and de facto they must be newly evaluated.

In 2005 Jarndal and Kompa [5] proposed an extrinsic parasitic network topology similar to the one of Fig.2.7 in conjunction with a optimization-based extraction technique for the extrinsic ECPs. They declared that the new topology is more suitable for scalable model construction, as previously shown in [4]. In the work it is shown how the more complicate capacitance shell can be identified only by means of a single pinched off cold FET measurement of only one device, through a bidirectional search based optimization routine. Although the results of the extraction are quite good for the definition of the measured device model, it is questionable the fact that with simple scaling rules the extracted model is accurate in the prediction of the characteristics of other devices. Some further extraction on different geometries, as done in [4], could be necessary to derive more reliable scaling rules.

The use of simple lumped topologies may be not sufficiently accurate at relatively high operating frequencies, and a large number of measurements on different device structures could be needed in order to obtain a good scalable model. Besides the procedures should be repeated when modelling a new process because the defined scaling rules could be technology dependent.

2.4 Distributed Models.

Empirical modelling of the extrinsic parasitic network of electron devices have been modified with increasing frequency of operation, but, today, they still commonly consist of lumped elements (i.e. resistances, capacitances and inductances). As is well known from waveguide analysis, this approximation is valid, however, only up to a certain frequency for a given dimension. If these device dimensions are of the same order of magnitude as the wavelength, lumped-element considerations do not hold any more and distributed properties must be included. This is of greater interest the more the usual FET design criteria neglect these effects, and hence are restricted to such devices where lumped element concepts may be adopted. With FETs operating at several tens of [GHz] this problem is no longer negligible.

In fact in 1986 Heinrich [16] studied the maximum frequency of validity of lumped element description with respect to the dimension of the transistor. Clearly a trade off between the dimension of the device and the frequency of application must be paid when the device model is selected. Violating the limiting conditions that distributed phenomena are to be included means that wave propagation along the electrodes needs to be studied; otherwise erroneous results will be obtained.

In this context distributed models [6]-[15] are available accounting for the distributed phenomena within the device electrodes. As far as the model scalability is concerned, distributed models offer higher accuracy than conventional models. In fact the philosophy of distributed modelling is the extraction of an empirical model per unit gate width, which is then exploited to build up any device periphery of the same foundry process.

Since the middle of ‘80s many distributed models appeared in literature [6]-[13]. Whereas they are similar one to another, the model proposed by S. J. Nash *et al.* [12] is here took in exam.

In [12] the distributed model of the FET was developed from the equations for asymmetric coupled lines in an inhomogeneous medium. Fig.2.8 shows a schematic representation of the distributed model including also the correct boundary conditions.

The two port Z-parameters can be written as second order differential equations:

$$\begin{aligned} \frac{d^2V_g(x)}{dx^2} &= V_g(x)\alpha^2 + V_d(x)\beta^2 \\ \frac{d^2V_d(x)}{dx^2} &= V_g(x)\delta^2 + V_d(x)\gamma^2 \end{aligned} \tag{2.3}$$

where the propagation constants are

$$\alpha^2 = Y_{11}Z_g + j\omega MY_{21}, \quad \beta^2 = Y_{12}Z_g + j\omega MY_{22}$$
$$\delta^2 = Y_{21}Z_d + j\omega MY_{11}, \quad \gamma^2 = Y_{22}Z_d + j\omega MY_{12} \tag{2.4}$$

and $Z_g = R_g + j\omega L_g$, $Z_d = R_d + j\omega L_d$ and M are the per unit width values of the impedances and the mutual inductance associated with the gate and drain electrodes. Y_{ij} are the intrinsic per unit width elements of the Y matrix of the device.

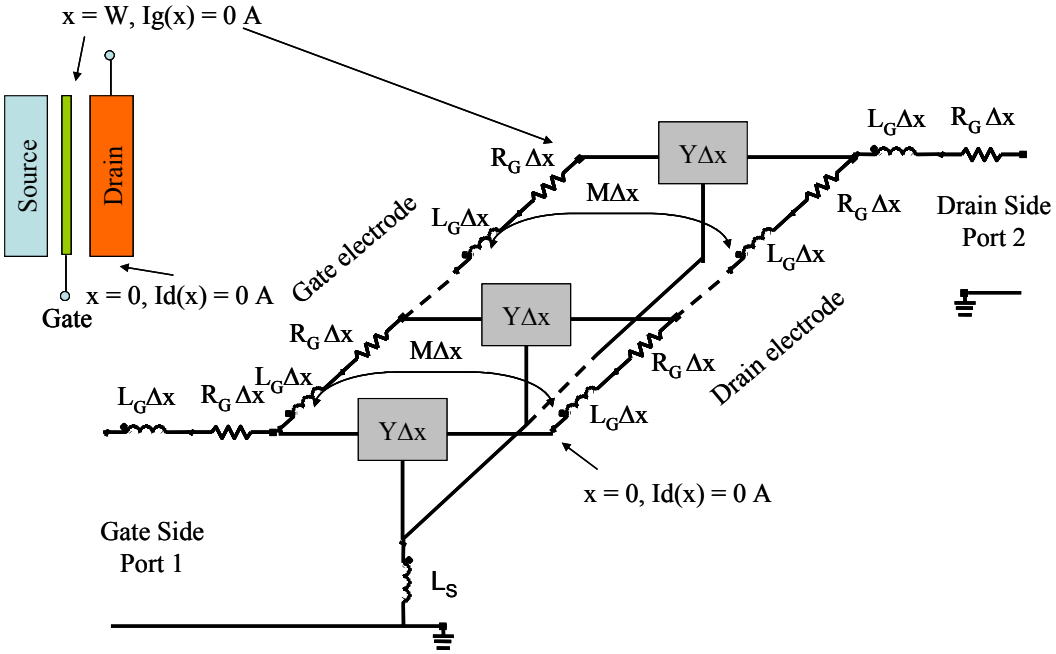

Fig. 2.8 Distributed model of a single finger FET as proposed in [12].

The propagation parameters (2.4) take into account the intrinsic impedances of the gate and drain electrodes (Z_g and Z_d) and the coupling between the gate and drain electrodes. The inductive mutual coupling M adds additional coupling between the gate and drain electrodes. The main coupling has contributions from the active region of the device and fringing electrode capacitances represented by Y_{12} and Y_{21} in the model. The resulting distributed model Z-parameters represent a continuous distributed model:

$$Z_{11} = \frac{Z_g}{(r^-)^2 - (r^+)^2} \cdot \left[\frac{(r^-)^2 - \alpha^2 - \frac{j\omega M \beta^2}{Z_g}}{(r^+)\tanh(r^+ \cdot l)} - \frac{(r^+)^2 - \alpha^2 - \frac{j\omega M \beta^2}{Z_g}}{(r^-)\tanh(r^- \cdot l)} \right]$$

$$Z_{21} = \frac{Z_g \delta^2}{(r^+)^2 - (r^-)^2} \cdot \left[\frac{1 - \frac{j\omega M \beta^2}{Z_g((r^-)^2 - \alpha^2)}}{(r^+)\sinh(r^+ \cdot l)} - \frac{1 - \frac{j\omega M \beta^2}{Z_g((r^+)^2 - \alpha^2)}}{(r^-)\sinh(r^- \cdot l)} \right] \tag{2.5}$$

where

$$(r^{\pm})^2 = \frac{1}{2}\left[(\alpha^2 + \gamma^2) \pm \sqrt{(\alpha^2 - \gamma^2) + 4\beta^2\delta^2} \right].$$

Since the network is symmetric, the expressions for Z_{22} and Z_{12} are obtained by replacing Z_g with Z_d, β^2 with δ^2, δ^2 with β^2, α^2 with γ^2 and r^+ with r^- in (2.5). In [12] the L_S is not distributed therefore, $j\omega L_S$ should be added to each one of the above Z-parameters to complete the device model.

The distributed model [12] introduces also an empirical formula taking into account a frequency dependent gate resistance. It is derived by curve fitting the modelled data with the measured data. The result of adding the frequency dependent resistance to the models showed a dramatic improvement in the prediction of the magnitude of S_{11}.

The distributed model of Fig.2.8 can be extended to multi-finger FETs by paralleling the elementary model (2.5) for each different finger. In order to account for transverse distributed phenomena occurring for devices with a great number of gate fingers, additional transversal elements can be included as proposed in [11].

The distributed models' experimental validation shows the high accuracy achieved up to millimetre-wave frequencies and the great scaling and frequency extrapolation capabilities of this kind of models. Those conventional distributed models [6]-[13], which usually consist of a cascade of elementary devices, representing the active area of the electron device, fed by lumped passive networks which should model signal propagation and other electromagnetic phenomena related to the passive structure, have not been extensively used in practice (probably due to the complexity of the identification procedures).

Recently, the progress in numerical device simulation and the development of electromagnetic analysis tools, together with the availability of powerful workstations, have led to modelling approaches aimed to the numerical solution of the electromagnetic and electron transport problems in a consistent way by means of the electromagnetic (EM) simulators. This is the case for example of models [14], [15] where the EM simulation is used for the identification of the distributed description of the device passive (i.e. parasitic) structure.

As far as nonlinear device modelling is concerned, the main problem of distributed model is due to the subdivision of the device in many slices of active devices (see Fig.2.8) which cause an increment in the computational effort, with respect to conventional models: in nonlinear circuit analysis tools (such as Harmonic Balance), the CPU effort grows more than linearly with the number of nonlinear nodes.

In the last few years the availability of commercial general purpose EM simulators has allowed the practical use of these tools to identify accurate and scalable distributed linear (i.e. Small-Signal) models. Although their extension to the nonlinear case suffer of the mentioned rise of CPU effort, some simplifications can be applied in order to overcome this problem.

Since the definition of a EM-based distributed description of the extrinsic parasitic network suitable for nonlinear electron device modelling is the heart of this thesis, the EM-based extrinsic parasitic network modelling is carried out in the next chapter.

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CHAPTER 3

EM-BASED PARASITIC NETWORK DESCRIPTION

3.1 Introduction.

The scalability issue of empirical models has been extensively discussed in Chapter 2. In fact full exploitation of a given technology for MMIC design would require the capability of choosing devices with an optimized number and width of fingers. Unfortunately, empirical models usually adopted for circuit design do not explicitly provide a link between technological process parameters (such as the device layout) and the corresponding device electrical response. Conventional modelling approaches based on lumped equivalent circuits may be inappropriate also for the following reasons:

- distributed effects and coupling phenomena occurring at very high frequencies may strongly affect the transistor performance. Such a behaviour is not easily described by standard lumped parasitic elements [1]-[3]. Either distributed effects should be taken into account in the device model or rather complicated equivalent circuit structures have to be considered [4]-[18].
- parameters of lumped equivalent circuits are usually scaled with device size and finger number according to different approaches, from very simple linear rules to completely empirical algorithms [19]-[21]. Some of these approaches may be not sufficiently accurate at relatively high operating frequencies, and a large number of measurements on different device structures could be needed in order to obtain a good scalable model. Particular care must be paid in any case to parasitic network modelling and identification.

In Chapter 2 is also put in evidence that the CPU efficiency is the main drawback of all distributed empirical models when extended to the nonlinear case. Since their frequency extrapolation and scaling capabilities are needed for accurately scale the model, some kind of simplification with respect to a fully distributed approach is required.

In this Chapter it is shown how the electron device behaviour can be described as an *equivalent* two-port intrinsic nonlinear block connected to a linear *distributed* four-port passive parasitic network. Such an approach has been developed starting from an EM-based small-signal distributed model found in literature [14].

3.2 EM-based fully distributed nonlinear models: CPU efficiency considerations.

The small-signal electron device model presented in [14] adopts a distributed description for both the active device area and the extrinsic structure. In particular, this model is based on a proper partitioning of the "active part" of the device in a convenient number of "internal elementary devices" (or "elementary intrinsic devices", EIDs) fed by a "passive distributed structure" characterized in terms of scattering parameters by means of an accurate electromagnetic simulation of the device layout. The EM simulation enables the actual device geometry and material stratification, as well as losses in the dielectrics and electrodes, to be taken into account for any given device structure and size by means of a multi-port S-matrix distributed description. The model has been extensively validated for MESFET and PHEMT devices, taking also into account its frequency extrapolation [14] and scaling [17] capabilities, up to 110 GHz.

As far as model identification is concerned, the device passive structure is characterized through its scattering matrix computed by means of electromagnetic simulation [22]. Thus, since electromagnetic propagation and coupling effects are accounted for by the passive structure, all the EIDs are described by the same scattering matrix, which can be identified once the scattering matrix of the whole electron device has been measured [14].

The number of active sections that must be considered strongly depends on the device geometry and operating frequency range. Many authors adopt the approximate dimension (being the electrical wavelength) as the limit above which distributed effects must be accounted for and as a thumb rule to introduce the proper number of EIDs along the gate metallization. More realistically, this number also depends on model accuracy versus complexity considerations.

It is worth noting that model identification does not require either parameter optimization or complex measurements. Clearly, in the identification procedure outlined in [14], the important assumption is made that current transport along the channel does not substantially affect the characterization of electromagnetic-field distribution in the passive structure. In particular, just undoped GaAs was assumed to be under the metal structure. Moreover, also having the active part of the electron device "concentrated" into a limited finite number of EIDs, clearly represents an approximation. These simplifications, which make it possible to use a conventional commercially available electromagnetic simulator for model identification, cannot be easily justified by purely theoretical considerations. However, the experimental results show that the errors introduced with the above assumptions are not so relevant for electron device scaling. In particular, in [14] is shown how an equivalent S-matrix per unit width of the electron device can be introduced and used to predict how electrical characteristics scale with gate width and number of fingers or, more generally, with device geometry variations.

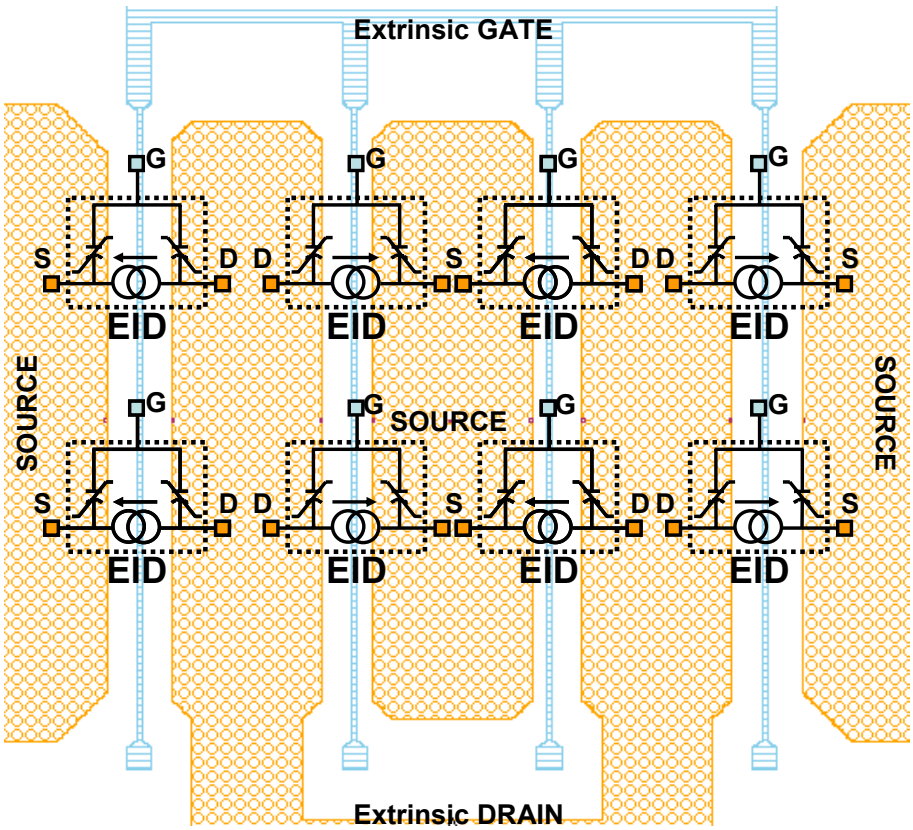

Fig. 3.1 Fully distributed nonlinear modelling through the EM-based method proposed in [14].

The small-signal approach proposed in [14], although very accurate, does not seem really suitable for a straightforward extension to the case of nonlinear device modelling. In fact, due to the

relatively large number of EIDs, a very cumbersome model would result when nonlinear descriptions are adopted for any EID. This can be intuitively seen in Fig.3.1, where a four finger device has been modelled considering two nonlinear EID model per device finger. In consideration of the extensive number of model evaluations required by any circuit design process and by Harmonic Balance solution algorithms, CPU time and memory occupation would make the model unpractical for design purpose. In fact the computational efficiency related to those algorithms (see [23]) grows very fast as the number of network nodes (at which a nonlinear element is connected) increase.

3.3 EM-based compact distributed modelling of electron devices.

In this paragraph it is shown how the device can be described as an *equivalent* two-port intrinsic nonlinear block connected to a linear *distributed* four-port passive parasitic network. Such an approach (see Fig.3.2) is based on the partition of the device geometry into a convenient number of *Elementary Intrinsic Devices* (EIDs) placed along the layout fingers. The EIDs are interconnected by a linear "passive distributed structure", which can be described in terms of a $2N$+2-port admittance matrix, where N is the total number of EIDs, through accurate electromagnetic (EM) simulations.

This kind of *compact* modelling, based on the fully distributed model [14], was first introduced in [15], where a preliminary validation under linear multi-bias conditions was also provided. More extensive validation may be found in [16], where conventional equivalent circuit scalable models are extracted (and compared) on the basis of both distributed and lumped parasitic networks. The linear multi-bias validation in [16] suggests that the four-port distributed parasitic network description, together with equivalent intrinsic device modelling, leads to great improvements in prediction accuracy with respect to conventional approaches, both for reference and scaled devices.

In the EM-based fully distributed empirical model described in [14], the electron device is assumed to consist of an "extrinsic passive network" connected with a finite number of elementary EIDs, as shown in Fig.3.2.

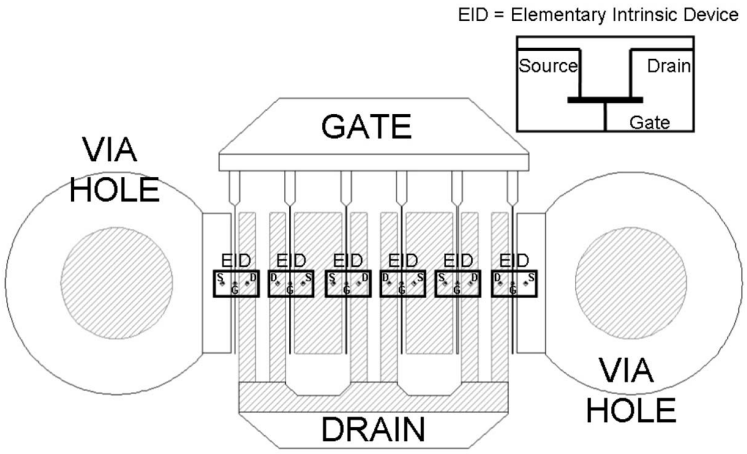

Fig. 3.2 Device layout example and EM simulator set-up using internal ports to define the Elementary Intrinsic Devices (EIDs).

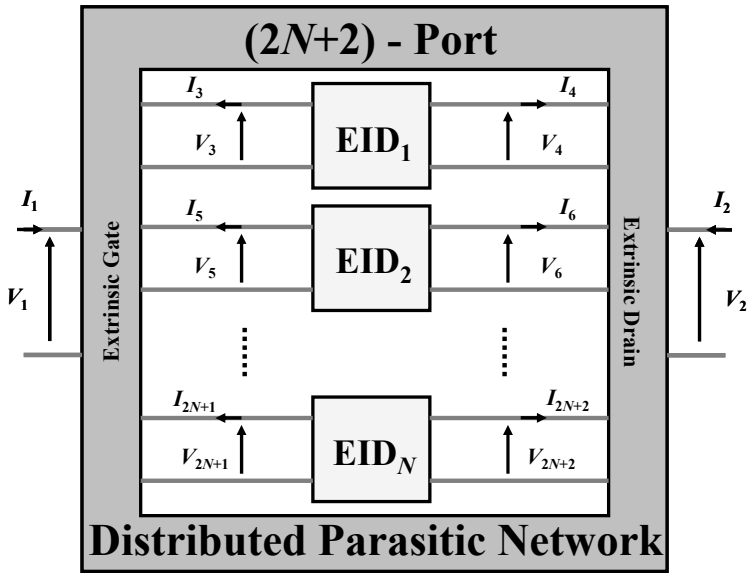

Fig. 3.3 Distributed parasitic network (gray pattern) directly obtained from the EM simulation of the device passive structure (described by the $\mathbf{Y}_{EM}$ admittance matrix). Voltage and current phasors at the external gate and drain terminals and at the gate and drain elementary intrinsic device (EID) terminals are also shown.

The distributed $2N$+2-port parasitic network, shown in Fig.3.3 and directly obtained by means of the EM simulation, is adopted in [14] for the definition of the above mentioned fully distributed linear model of electron devices. In order to develop a similar approach in the more general nonlinear case, a single, *Equivalent Intrinsic Device* (EqID) is considered in the following leading to the corresponding definition of a compact distributed parasitic 4-port network, described by the admittance matrix $\mathbf{Y}_C$ [4×4].

This paragraph aims to the description of the compact distributed parasitic network identification procedures. The first procedure consists in a closed-form identification approach which requires

solely the EM simulation of the device passive structure of Fig.3.2. Since in the closed-form procedure the main assumption of considering *all the EIDs equally fed*, could be considered questionable, at first sight, a more general iterative compacting procedure is discussed.

3.3.1 Closed-form Identification Approach

A simplified procedure consistent with the EqID concept have been proposed in [15]. The main assumptions that lead to the compact modelling of the linear parasitic network are the following: *every EID is considered equal to each other* (both from a geometrical and electrical point of view) and *equally excited*. The second hypothesis means that both attenuation and delay of signals travelling across the active area are assumed to be negligible. This is quite reasonable in "well-designed" devices since either non uniform current densities along the fingers or out-of-phase current combinations from different device fingers correspond to sub-optimal device performance.

On the basis of these two assumptions, the 2*N*+2-port distributed parasitic network in Fig.3.3 can be *compacted* into a 4-port description of parasitic effects, by imposing:

$$\begin{aligned} &\mathrm{V}_1 \doteq V_1 \\ &\mathrm{V}_2 \doteq V_2 \\ &\mathrm{V}_3 \doteq V_3 = V_5 = \ldots = V_{2N+1} \\ &\mathrm{V}_4 \doteq V_4 = V_6 = \ldots = V_{2N+2} \end{aligned} \tag{3.1}$$

and:

$$\begin{aligned} &\mathrm{I}_1 \doteq I_1 \\ &\mathrm{I}_2 \doteq I_2 \\ &\mathrm{I}_3 / N \doteq I_3 = I_5 = \ldots = I_{2N+1} \\ &\mathrm{I}_4 / N \doteq I_4 = I_6 = \ldots = I_{2N+2} \end{aligned} \tag{3.2}$$

where V_j, I_j (j = 1, …, 4) are the phasors of voltages and currents at the ports of the yet-unknown compact parasitic network (see Fig.3.4).

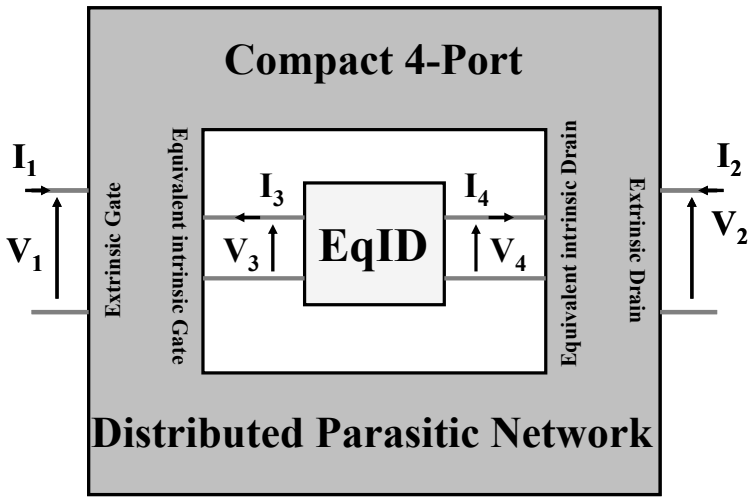

Fig. 3.4. Electron device model composed by the single, *Equivalent Intrinsic Device* (EqID) and the *compact* 4-ports distributed parasitic network identified directly from the electromagnetic simulation through equation (3.3).

The admittance matrix $\mathbf{Y}_C$ of the compact distributed parasitic network, can be evaluated on the basis of (3.1) and (3.2) after simple algebraic manipulation, through:

$$\mathbf{Y}_C = \begin{pmatrix} y_{11} & y_{12} & \sum_{j=2}^{N+1} y_{1,2j-1} & \sum_{j=2}^{N+1} y_{1,2j} \\ y_{21} & y_{22} & \sum_{j=2}^{N+1} y_{2,2j-1} & \sum_{j=2}^{N+1} y_{2,2j} \\ \sum_{i=2}^{N+1} y_{2i-1,1} & \sum_{i=2}^{N+1} y_{2i-1,2} & \sum_{i=2}^{N+1}\sum_{j=2}^{N+1} y_{2i-1,2j-1} & \sum_{i=2}^{N+1}\sum_{j=2}^{N+1} y_{2i-1,2j} \\ \sum_{i=2}^{N+1} y_{2i,1} & \sum_{i=2}^{N+1} y_{2i,2} & \sum_{i=2}^{N+1}\sum_{j=2}^{N+1} y_{2i,2j-1} & \sum_{i=2}^{N+1}\sum_{j=2}^{N+1} y_{2i,2j} \end{pmatrix} \tag{3.3}$$

where y_{ij} ($i, j = 1, \ldots, 2N+2$) are the elements of the $\mathbf{Y}_{EM}$ matrix.

Multi-frequency closed-form de-embedding of the parasitic network described by (3.3) from small-signal device measurements directly leads to the multi-bias, multi-frequency linear model of the EqID.

The closed-form de-embedding procedure is here also outlined. Let $\boldsymbol{\delta}$ and $\mathbf{Y}_{EqID}$ be the [2x2] matrices of the extrinsic and equivalent intrinsic device admittance parameters. Obviously, $\boldsymbol{\delta}$ is directly obtained from S-parameter measurements with well-known transformation formulas, while $\mathbf{Y}_{EqID}$ represents the unknown of our de-embedding procedure. We define now, for the notation simplicity sake, four [2x2] sub-matrices of $\mathbf{Y}_C$, namely $\mathbf{Y}_C^{EE}$, $\mathbf{Y}_C^{EI}$, $\mathbf{Y}_C^{IE}$, $\mathbf{Y}_C^{II}$, such that:

$$\begin{cases} \mathbf{i}_E = \mathbf{Y}_C^{EE}\mathbf{v}_E + \mathbf{Y}_C^{EI}\mathbf{v}_I \\ \mathbf{i}_I = \mathbf{Y}_C^{IE}\mathbf{v}_E + \mathbf{Y}_C^{II}\mathbf{v}_I \end{cases} \tag{3.4}$$

where $\mathbf{v}_E$, $\mathbf{v}_I$, $\mathbf{i}_E$, $\mathbf{i}_I$ represent the voltages and currents of the extrinsic (E) and intrinsic (I) device in vector form. After simple algebraic manipulation we obtain:

$$\mathbf{Y}_{EqID} = \mathbf{Y}_C^{IE}(\boldsymbol{\delta} - \mathbf{Y}_C^{EE})^{-1}\mathbf{Y}_C^{EI} + \mathbf{Y}_C^{II}. \tag{3.5}$$

3.3.2 Multi-bias Identification Approach

Two assumptions are made in the closed-form approach presented in the previous paragraph. First, every EID is equal to each other; second, every EID is fed by identical excitations. Both hypotheses are questionable at first sight. For instance, internal versus border-line EIDs could be affected differently by electromagnetic coupling with surrounding structures, especially at high frequencies, or important delays could be present in the excitations of different EIDs, especially in large size devices.

A compact distributed description of the parasitic network can be alternatively obtained by means of a more general procedure, where the second assumption is abandoned. In particular, a new procedure is presented here where possible different excitations of every EID are taken into account.

The procedure is based on a "*multi-bias iterative algorithm"*, whose goal is still to identify a compact 4-port distributed parasitic network, as shown in Fig.3.4. However, the desired goal consists now in identifying a 4-port compact admittance matrix $\mathbf{Y}_C$ which guarantees, at any bias condition, voltage and (scaled) current phasors at the single EqID ports to be coherent (in "a least square sense") with the corresponding quantities at the ports of every EID (out of the *N* considered in the distributed network in Fig.3.3).

As mentioned above, all the EIDs are still assumed to be equal in the generic bias condition. In addition, the unknown admittance matrix $\mathbf{Y}_{EqID}$ of the EqID is defined to be scaled up by a factor *N* with respect to the $\mathbf{Y}_{EID} \doteq \mathbf{Y}_{EID}^{(d)}$ (d = 1, …, N_d), representing the description of every EID (i.e.: $\mathbf{Y}_{EqID} = N \cdot \mathbf{Y}_{EID}$). Although, the EIDs are considered equal, no *"a priori"* assumption is made here on the relationships existing between their excitations.

Since the $\mathbf{Y}_C$ matrix describes a 4-port network, four linearly-independent (complex-valued) excitations should be theoretically applied in order to get a complete characterization. However, according to Fig.3.4, internal ports 3 and 4 are unfortunately not accessible in the actual case. Thus, two linearly-independent excitations are only applicable through the external device ports 1 and 2 (e.g.: [1V, 0V], [0V, 1V]). However, excitations of port 3 and 4 can be equivalently obtained by considering the device behaviour in (at least two) very different bias conditions (corresponding to very different couples of terminating impedances at ports 3 and 4).

The identification procedure is carried out according to the flow-chart shown in Fig.3.5.

At the first iteration, a suitable initial estimate for the unknown $\mathbf{Y}_C^{(k)}$, corresponding to index k = 0, must be provided. Since the problem is very well conditioned, a rough initial guess can be adopted, such as considering completely negligible parasitics.

Let $f = 1, \ldots, N_f$ be the frequency index, $e = 0, 1$ the external excitation index, $b = 1, \ldots, N_b$ the bias condition index and $d = 1, \ldots, N_d$ the EID location index, where N_f, N_b, N_d represent the number of frequencies, bias conditions and elementary intrinsic devices considered, respectively.

The iterative procedure consists in three nested loops: the outer loop (k) involves successive approximations of the unknown matrix $\mathbf{Y}_C$, while the mid and inner loops (f, b) cycle through different frequencies and bias conditions.

For each k and f index choice, a multi-bias over-determined system of equations is build up, whose solution leads to the identification of the compact $\mathbf{Y}_C^{(k+1)}$ matrix to be used in the (k+1)-th iteration. To this aim, the small-signal admittance measurements of the device, carried out over the selected bias points (index b), are de-embedded from $\mathbf{Y}_C^{(k)}$ in order to determine $\mathbf{Y}_{EqID}^{(k,b)}$ and $\mathbf{Y}_{EID}^{(k,b)} = \mathbf{Y}_{EqID}^{(k,b)}/N$, representing the admittance matrices (at frequency index f) of the EqID and of every EID at the (k)-th iteration, respectively.

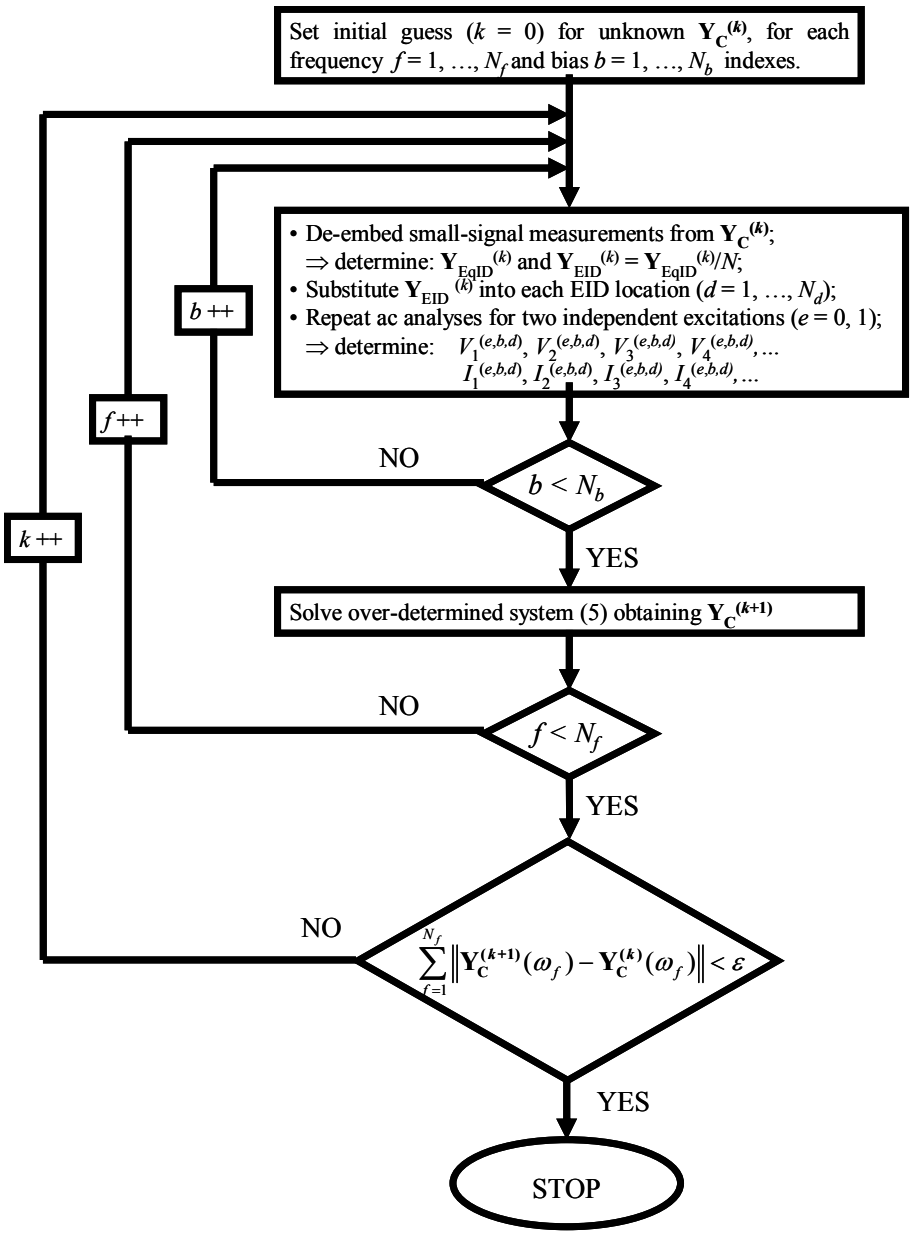

Fig. 3.5. Flow-Chart describing the multi-bias approach to the identification of the compact distributed parasitic network $\mathbf{Y}_C$.

Any obtained $\mathbf{Y}_{EID}^{(k,b)}$ matrix is then iteratively inserted into every EID location and connected to the $2N$+2-port distributed network of Fig.3.3. Each one of the resulting 2-port linear networks (one for each b index value) is then simulated twice, in the presence of two linearly-independent external excitations (e.g.: indexes e=0,1 corresponding to phasors $V_1^{(0,b,d)}$=1V; $V_2^{(0,b,d)}$=0V and $V_1^{(1,b,d)}$=0V; $V_2^{(1,b,d)}$=1V, respectively). The resulting voltage and current phasors at the extrinsic device ports and at the ports of each EID are then monitored by means of voltage and current probes. Namely, they are:

$$
\begin{array}{l}
V_1^{(e,b,d)},\ V_2^{(e,b,d)},\ I_1^{(e,b,d)},\ I_2^{(e,b,d)} \\
V_3^{(e,b,d)},\ V_4^{(e,b,d)},\ I_3^{(e,b,d)},\ I_4^{(e,b,d)}, \\
V_5^{(e,b,d)},\ V_6^{(e,b,d)},\ I_5^{(e,b,d)},\ I_6^{(e,b,d)} \\
\ldots \\
V_{2N+1}^{(e,b,d)},\ V_{2N+2}^{(e,b,d)},\ I_{2N+1}^{(e,b,d)},\ I_{2N+2}^{(e,b,d)}
\end{array}
\tag{3.6}
$$

where the f index is anywhere omitted for the sake of simplicity. Since the goal is to obtain a compact distributed description $\mathbf{Y}_C$ of the extrinsic parasitics, $4\times2\times N_b$ constraints are now imposed for each EID (thus a total of $4\times2\times N_b\times N_d$ equations are written), like:

$$
\begin{aligned}
\mathrm{I}_1^{(e,b,d)} &= \mathrm{Y}_{11}^{(k+1)}\cdot\mathrm{V}_1^{(e,b,d)} + \mathrm{Y}_{12}^{(k+1)}\cdot\mathrm{V}_2^{(e,b,d)} + \mathrm{Y}_{13}^{(k+1)}\cdot\mathrm{V}_3^{(e,b,d)} + \mathrm{Y}_{14}^{(k+1)}\cdot\mathrm{V}_4^{(e,b,d)} \\
\mathrm{I}_2^{(e,b,d)} &= \mathrm{Y}_{21}^{(k+1)}\cdot\mathrm{V}_1^{(e,b,d)} + \mathrm{Y}_{22}^{(k+1)}\cdot\mathrm{V}_2^{(e,b,d)} + \mathrm{Y}_{23}^{(k+1)}\cdot\mathrm{V}_3^{(e,b,d)} + \mathrm{Y}_{24}^{(k+1)}\cdot\mathrm{V}_4^{(e,b,d)} \\
\mathrm{I}_3^{(e,b,d)} &= \mathrm{Y}_{31}^{(k+1)}\cdot\mathrm{V}_1^{(e,b,d)} + \mathrm{Y}_{32}^{(k+1)}\cdot\mathrm{V}_2^{(e,b,d)} + \mathrm{Y}_{33}^{(k+1)}\cdot\mathrm{V}_3^{(e,b,d)} + \mathrm{Y}_{34}^{(k+1)}\cdot\mathrm{V}_4^{(e,b,d)} \\
\mathrm{I}_4^{(e,b,d)} &= \mathrm{Y}_{41}^{(k+1)}\cdot\mathrm{V}_1^{(e,b,d)} + \mathrm{Y}_{42}^{(k+1)}\cdot\mathrm{V}_2^{(e,b,d)} + \mathrm{Y}_{43}^{(k+1)}\cdot\mathrm{V}_3^{(e,b,d)} + \mathrm{Y}_{44}^{(k+1)}\cdot\mathrm{V}_4^{(e,b,d)}
\end{aligned}
\tag{3.7}
$$

where $\mathrm{Y}_{ij}^{(k+1)}$ ($i, j = 1, \ldots, 4$) are the admittance parameters of the $\mathbf{Y}_C$ matrix at the (k+1)-th iteration at the particular frequency corresponding to f, and:

$$
\begin{array}{l}
\mathrm{V}_1^{(e,b,d)} = V_1^{(e,b,d)},\ \mathrm{V}_2^{(e,b,d)} = V_2^{(e,b,d)}, \\
\mathrm{V}_3^{(e,b,d)} = V_{2d+1}^{(e,b,d)},\ \mathrm{V}_4^{(e,b,d)} = V_{2d+2}^{(e,b,d)}, \\
\mathrm{I}_1^{(e,b,d)} = I_1^{(e,b,d)},\ \mathrm{I}_2^{(e,b,d)} = I_2^{(e,b,d)}, \\
\mathrm{I}_3^{(e,b,d)} = N\cdot I_{2d+1}^{(e,b,d)},\ \mathrm{I}_4^{(e,b,d)} = N\cdot I_{2d+2}^{(e,b,d)}.
\end{array}
$$

The solution of the over-determined system (3.7) leads to the estimation of $\mathbf{Y}_C^{(k+1)}$ at the frequency index f (i.e., angular frequency ω_f).

The above steps are repeated, cycling through the outer loop (k) until the accuracy between two subsequent estimations of the $\mathbf{Y}_C$ matrix satisfies the final test:

$$
\sum_{f=1}^{N_f} \left\| \mathbf{Y}_C^{(k+1)}(\omega_f) - \mathbf{Y}_C^{(k)}(\omega_f) \right\| < \varepsilon
\tag{3.8}
$$

ε being a given tolerance.

Despite the poor initial guess of the unknown matrix $\mathbf{Y}_C$, convergence of the iterative multi-bias procedure to the solution is very fast and sound.

3.4 Compact Distributed Parasitic Network Identification: discussion.

As discussed in the previous sections, the method proposed in Chapter 3.3.1 (method 1) identifies the compact distributed parasitic network on the basis of the equally fed EIDs approximation, which could seem quite limiting at first glance, while the multi-bias iterative method proposed in Chapter 3.3.2 (method 2) relaxes such an hypothesis and is clearly more general. Moreover, the identification based on multi-bias small-signal measurements should be more robust with respect to the direct identification based on EM simulations obtained through method 1.

On the basis of the above considerations, method 2 can be reasonably used to verify the validity of the simpler method 1. In order to carry out the comparison, both approaches are applied to different devices of the same family, namely a 6x5 0μm, a 10x48 μm and a 12x75 μm GaAs PHEMT (L = 0.25μm).

Referring for instance to the 6x50 μm device method 1 is applied starting from a $2N$+2-port distributed parasitic network with $N = 6$, i.e., the EM simulation is carried out by considering only one EID per finger. The validity of such a choice has been verified also in previous papers [17], [18]; in fact, it should be considered that, if an electron device is accurately designed for its operating frequency range, the propagation effects along the structure width, in particular signal attenuation, should not be too relevant, otherwise there will be some parts of the active area not efficiently exploited. In addition, it must be observed that the adoption of more than one EID per finger, when using method 1, inherently leads to neglect the parasitic effects along the same finger due to the assumption of EIDs fed by identical signals. Thus, increasing the number of EIDs per finger does not provide higher accuracy in model identification through method 1.

Method 2 is applied starting from a $2N$+2-port distributed parasitic network with $N = 12$ (that is two EIDs per finger) and selecting 12 different bias points covering all the device operating regions. The choice of two sections of EIDs per finger is done in order to define a least square problem robustly over-determined with respect to the placement of the EID in the electron device structure. With this choice, the iterative method converges to the required result very fast (after 6 iterations the absolute error is less than 10^{-7}).

Fig.3.6 shows the comparison between the admittance parameters of the 4-port compact distributed parasitic networks identified with the two different methods in the frequency range [4 GHz – 65 GHz]. The lower frequency limit of 4 GHz is imposed by our TRL calibration standards.

As it can be seen the simplest method 1 provides results which are very similar to those obtained by applying the multi-bias iterative method 2.

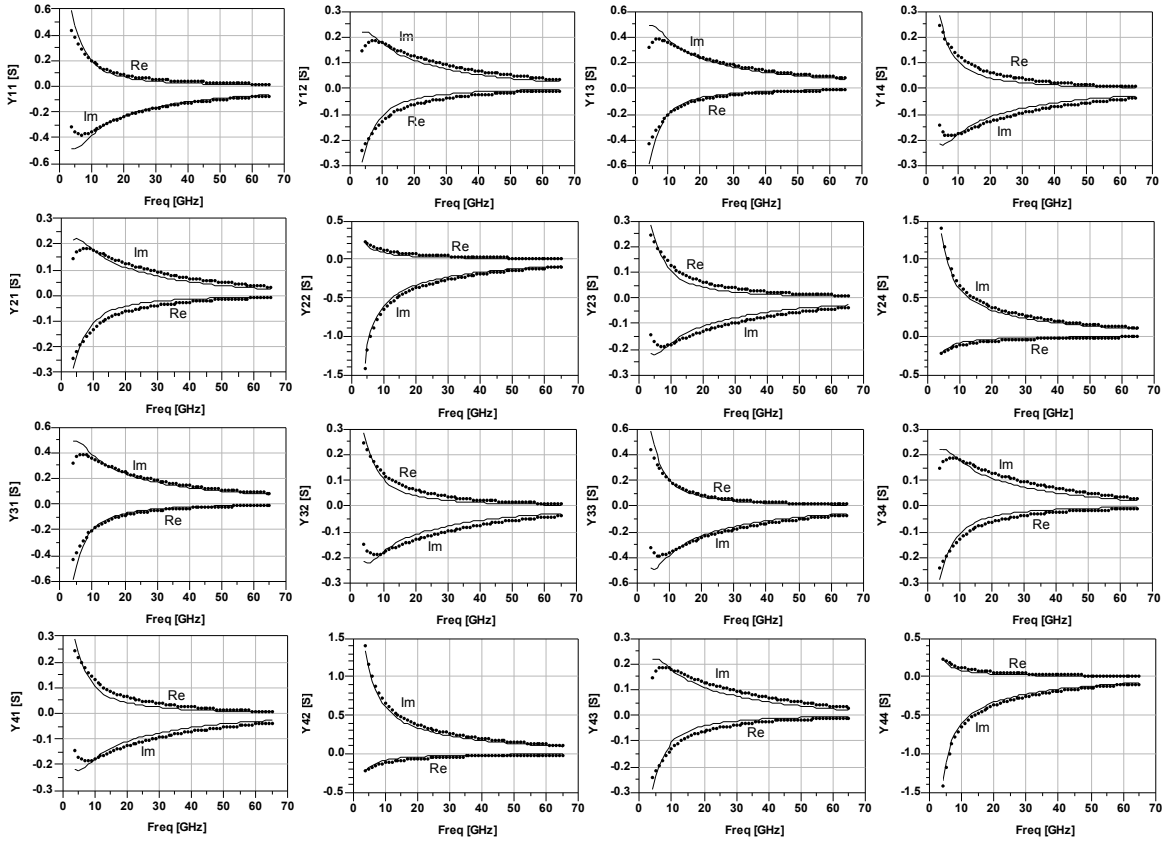

Fig. 3.6 Comparison of the 4-port compact distributed parasitic networks of the 6x50 μm PHEMT in terms of admittance parameters, from 4 to 65 GHz, obtained with the two proposed identification approaches: lines - method 1, dots - method 2.

In order to better compare the two proposed identification methods, the intrinsic device behaviour of the same 6x50 μm GaAs PHEMT, is investigated.

Fig.3.7 shows the comparison between the admittance parameters of the intrinsic devices obtained after de-embedding the measured data from the compact parasitic networks identified with the two different approaches. The results, corresponding to a pinched-off Cold FET bias condition, show that the intrinsic devices are quite similar. Moreover the intrinsic device in both cases shows the purely capacitive behaviour expected from the theory.

Fig.3.8, instead, shows the comparison between the admittance parameters of the intrinsic devices corresponding to $I_{DSS}/2$ bias condition, pointing out again that the intrinsic devices are quite similar.

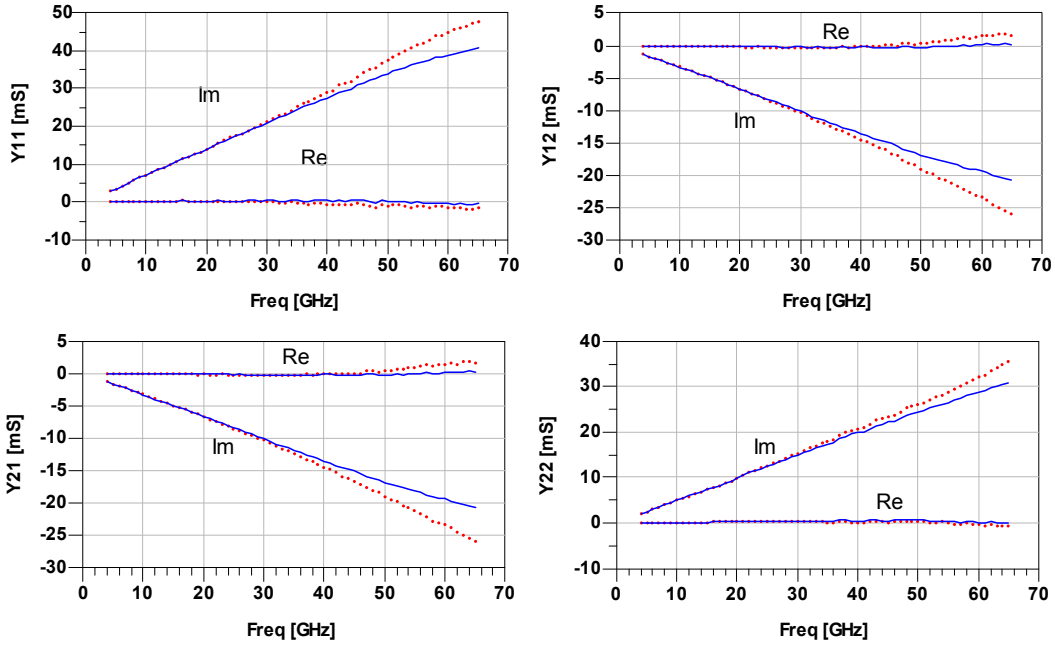

Fig. 3.7 Comparison of the intrinsic admittance parameters of the 6x50 µm PHEMT from 4 to 65 GHz, corresponding to a pinched-off Cold FET bias condition, obtained with the two proposed identification approaches: lines - method 1, dots - method 2.

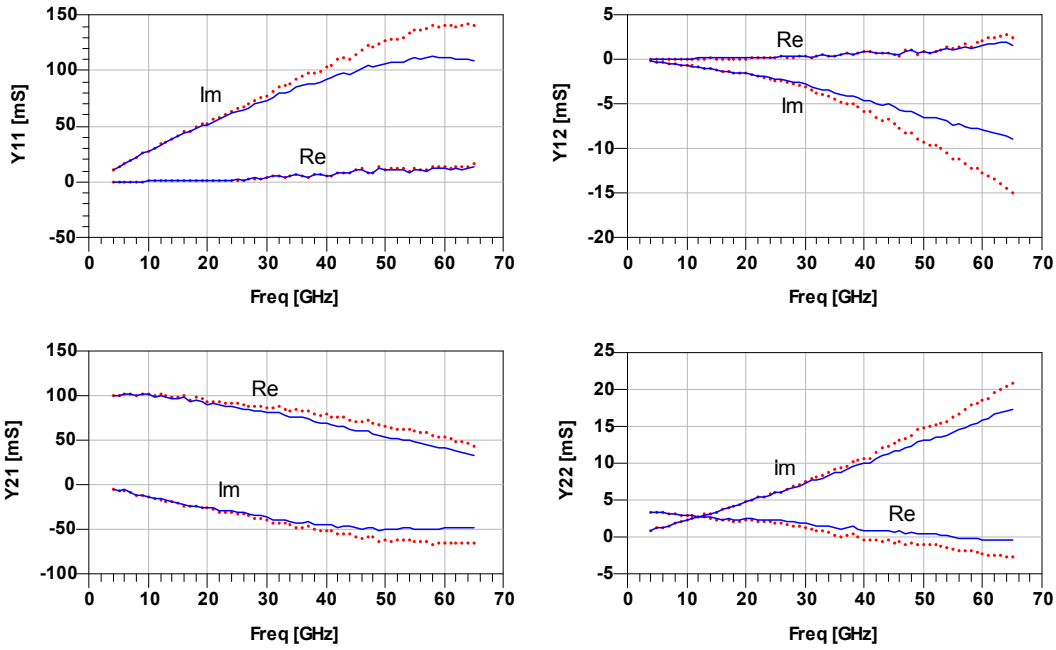

Fig. 3.8 Comparison of the intrinsic admittance parameters of the 6x50 µm PHEMT from 4 to 65 GHz, corresponding to $I_{DSS}/2$ bias condition, obtained with the two proposed identification approaches: lines - method 1, dots - method 2.

As a general consideration about the intrinsic admittance parameters shown in Fig.3.8, it can be appreciated the fair, nearly constant and linearly increasing behaviour of the real and imaginary parts, respectively. This corresponds to the *"short memory"* behaviour discussed in detail in [24]. The parameters displayed in Fig.3.8 suggest the physical soundness of the results which are coherent with the intrinsic behaviour of any electron device (conductive plus displacement current contribution) [25]-[33].

Analogous results are obtained after repeating the same comparisons on the 10x48 μm and 12x75 μm GaAs PHEMTs. Application of the two identification methods to devices having extremely large widths, e.g. due to a great number of (or to very long) fingers, could likely provide different results, highlighting the limits of method 1. This is proved however not the case, when considering typical widths used in MMIC power amplifier design.

Hence, since the multi-bias iterative procedure provides the same level of accuracy of the direct approach of chapter 3.3.1, it can be deduced that the EM simulation based on a single EID per finger is sufficiently accurate, at least for the overall widths investigated, in order to characterize the electron device parasitic effects and that the hypothesis of EIDs fed by identical signals is quite reasonable.

Since the identification of the parasitic distributed network through method 1 is based on EM simulations only, it is inherently free from obvious instrumentation frequency limits involved in method 2 that requires also S-parameter measurements on the electron device. Moreover, method 1 is most suitable when a scalable model must be identified. In fact, as will be discussed in this thesis, a scalable model can be obtained by experimentally characterizing just a single electron device sample and simply performing EM simulations for the different layouts involving different number and width of fingers.

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CHAPTER 4

EXPERIMENTAL VALIDATION OF EM-BASED SCALABLE NONLINEAR MODELS

4.1 Introduction.

This chapter aims at the experimental validation of the empirical modelling approach based on the EM-based identification of the linear extrinsic parasitic network. In Chapter 3.3.1 a closed-form procedure for the identification of a compact distributed parasitic network has been discussed [1].

Aiming at the extraction of a scalable nonlinear model, such a compact distributed parasitic network provides a single equivalent intrinsic device which solves the computational inefficiency of purely distributed models. As far as the scalability issue of the model is concerned, the compact distributed description of the extrinsic parasitic network should provide the same scalability and frequency extrapolation properties of purely distributed models.

The experimental validation carried out in this chapter aims at showing that such a compact distributed parasitic network not only provide a nonlinear model which is computationally efficient, but also a nonlinear model which has excellent prediction capabilities of both reference device and scaled devices.

The scaling procedure for the EM-based scalable empirical model consists in the EM simulation of the different device layouts and material properties, provided by the manufacturing foundry, while the intrinsic device is linearly scaled with respect to the device periphery. Thus only the measurements of the reference device are required.

A preliminary validation of the correctness of the compact distributed parasitic network is carried out under multi-bias linear operations (i.e. small-signal). In fact the EM-based linear

scalable empirical model of a 0.5 μm GaAs PHEMT technology [2] is validated also in comparison with a conventional scalable model. Then the proposed modelling approach is applied to the nonlinear case concerning two different technologies, namely a 0.25 μm GaAs PHEMT [3] and a 0.1 μm InP HEMT [4].

4.2 EM-based Model Scaling.

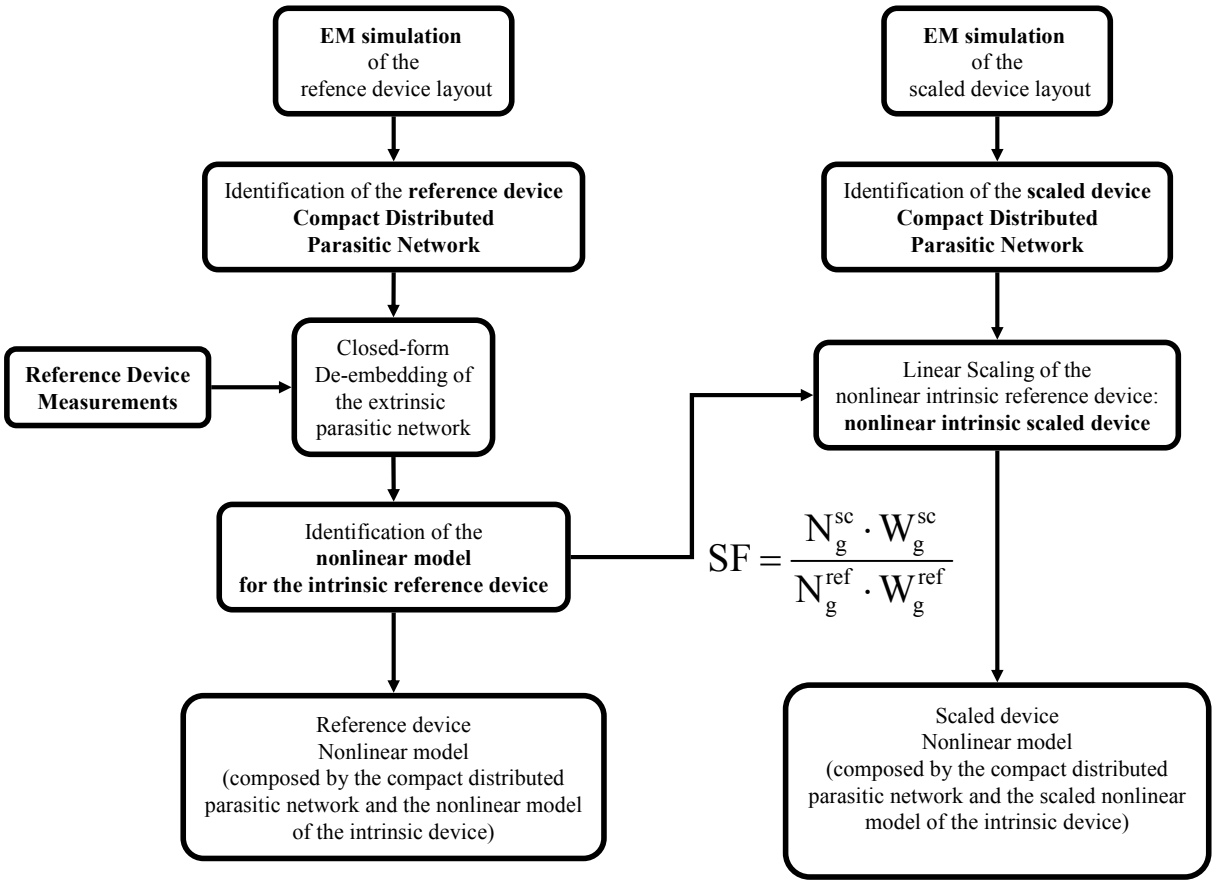


Fig. 4.1 Flow-chart which clarifies the scaling procedure. SF represents the linear Scaling Factor formula.

The scaling procedure is very straightforward and it is shown in the flow-chart of Fig.4.1. Such a figure refers to the scaling of a nonlinear model, but the procedure is clearly valid also in the case of a linear model. It consist in the EM simulation of the layout of the reference device and all the scaled devices. Then the closed-form compacting procedure of Chapter 3.3.1 is applied in order to identify the compact distributed parasitic network of all the different devices belonging to the same technological process. Knowing the measurements of the reference device and after the closed-form de-embedding procedure outlined in Chapter 3.3.1, the nonlinear model of the intrinsic reference device is extracted. To this point, the scaled device model is obtained by connecting the compact

distributed parasitic network of the new device together with the linearly scaled intrinsic reference device model.

Such a scaling procedure doesn't need integer relationships between the geometrical parameters, because the parasitic network identification of the scaled device involves the EM simulation of the new device layout: through this approach it is theoretically possible to scale any device of the same foundry process starting from the same reference device.

4.3 Preliminary experimental validation of the model scalability and frequency extrapolation properties.

The parasitic identification approach of Chapter 3.3.1 is here applied to a set of three different PHEMTs of the same foundry process, namely a 4x50 μm, a 2x100 μm and a 4x100 μm device, having all a gate length of 0.5 μm.

According to the scaling procedure of Fig.4.1, by means of electromagnetic simulations of the device layouts based on process parameters given by the foundry, the 4-port distributed parasitic network has been identified for each device. Then the 4x50 μm PHEMT has been considered as the "reference device" for the process, i.e. the device for which scattering-parameter measurements have been performed for a number of bias points and a bias-dependent small-signal equivalent circuit has been identified for the intrinsic device. More precisely, the conventional small-signal equivalent circuit (EC) model [5] shown in Fig.4.2, has been identified by de-embedding the distributed parasitic network and fitting S-parameter measurements from 1 to 30 GHz in three bias conditions: 1) V_{GS} = -0.5 V, V_{DS} = 5V, 2) V_{GS} = -1.5 V, V_{DS} = 5V, 3) V_{GS} = -1 V, V_{DS} = 8V. The model parameters for the three bias conditions are shown in Table I.

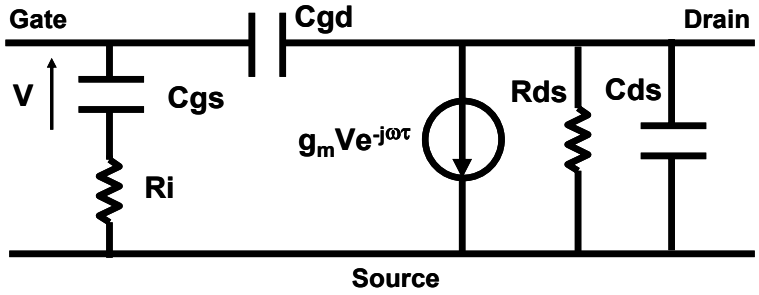


Fig. 4.2 Classical small-signal EC model used for the intrinsic device.

The EC model in Fig.4.2 has been also extracted for the same 4x50 μm "reference device", by fitting the S-parameter measurements from 1 to 30 GHz, after performing a classical cold FET

identification of linear lumped parasitic elements and de-embedding the measurements from this lumped parasitic network. The values of the lumped-parasitic EC model parameters are also shown in Table I, while the values of the lumped parasitic elements are shown in Table II.

TABLE I

	Distributed			**Lumped**		
	Bias (1)	Bias (2)	Bias (3)	Bias (1)	Bias (2)	Bias (3)
Cgs [fF]	237	35.5	257	262	54.5	281
Cgd [fF]	1.2	15.3	5.2	18.6	32.9	22.7
Cds [fF]	21.6	18.9	18.6	46.6	46.2	43.3
Ri [Ω]	4.82	18.1	6.72	0.75	0.00	2.44
Rds [Ω]	463	89.0K	521	472	1.00G	562
gm [mS]	64.0	0.00	57.0	66.0	0.00	59.0
τ [ps]	1.40	0.00	2.00	1.45	0.00	2.00

TABLE II

Cpg [fF]	**Cpd [fF]**	**Rg [Ω]**	**Rd [Ω]**	**Rs [Ω]**	**Lg [pH]**	**Ld [pH]**	**Ls [pH]**
11.3	0.00	4.60	2.02	0.58	19.7	16.5	12.5

Fig.4.3 shows a comparison between the admittance parameters of the 4-port parasitic networks obtained by means of the distributed and lumped approach. As it can be seen from the results, the 4-

port distributed parasitic network behaves similarly to the lumped one. This represents a preliminary justification of the validity of the approach since it provides results which are physically consistent with the lumped elements approximation.

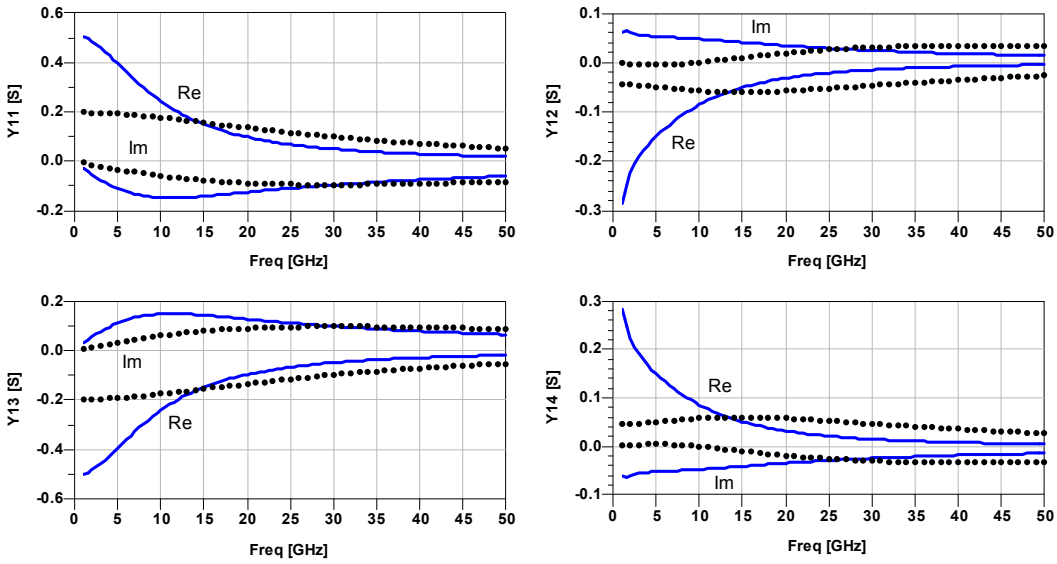


Fig. 4.3 Comparison between the compact distributed parasitic network (lines) and the lumped element parasitic network (dots) identified for the 4x50 μm PHEMT. In the figure the first row of the 4-port admittance matrix are shown (both real and imaginary part).

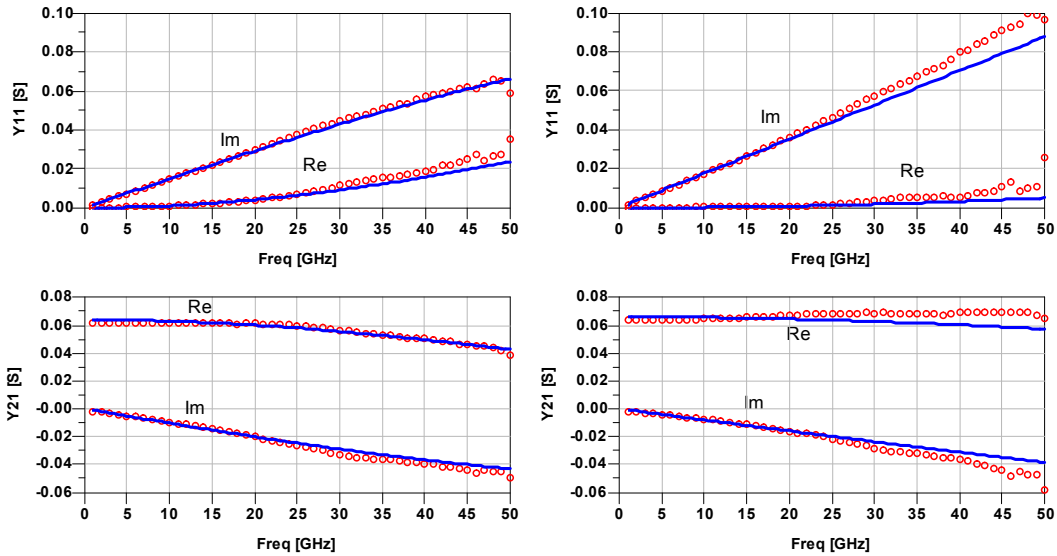


Fig. 4.4 Comparison between the measured (circles) and the EC model predictions up to 50 GHz for a 4x50 μm PHEMT, both for the EC extracted after de-embedding from the distributed parasitic network (left) as well as the EC extracted after de-embedding from the lumped parasitic network (rigth). The figure depicts the intrinsic admittance parameter at the bias V_{GS} = -0.5 V, V_{DS} = 5 V. Similar results are obtained for the other Y parameters and the other bias conditions.

Fig.4.4 shows the EC model intrinsic admittance parameter predictions up to 50 GHz in comparison with measurements; it can be seen that the intrinsic model obtained after de-embedding from the distributed parasitic network fits the measurements definitely better, especially at the highest frequencies, than the intrinsic model obtained after lumped parasitic de-embedding.

The extracted EC model of the intrinsic device was also used to predict the performance of scaled devices.

The scaled devices are a 4x100 μm PHEMT and a 2x100 μm PHEMT. In order to emphasize the better scaling properties of this distributed approach, the same devices were also scaled by using the lumped element model and simple scaling rules as explained in [5].

The scattering parameters predicted for the 2x100 μm and 4x100 μm PHEMT devices are shown in Fig.4.5 and 4.6, respectively. The figures point out that the proposed distributed approach is more accurate than the classical scaling approach based on the lumped parasitics since, due to the EM-based distributed parasitic network, the changes in the scaled device passive structure are more accurately taken into account. This is emphasized in Fig.4.7, where the proposed EM-based scaled model predicts reasonably well the resonant-like behaviour of the extrinsic admittance parameters of the largest PHEMT up to the maximum measured frequency (50 GHz), while the predictions based on the lumped parasitic approach are inaccurate.

Such an experimental validation puts in evidence also the frequency extrapolation properties of the proposed EM approach. In fact both models have been extracted by using the measurements up to 30 GHz, but their prediction capabilities are investigated up to 50 GHz. Fig.4.5, Fig.4.6 and especially Fig.4.7 show the better frequency extrapolation capabilities of the new distributed approach.

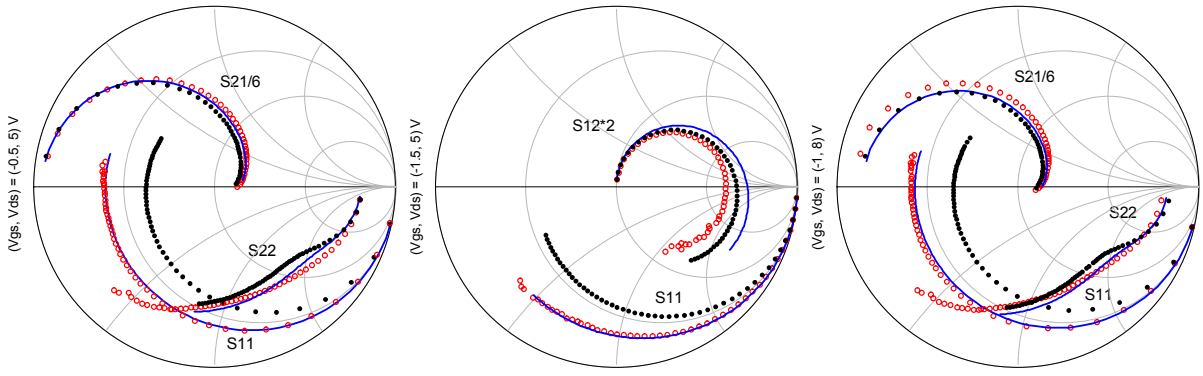


Fig. 4.5 Comparison between the 2x100μm PHEMT measured extrinsic scattering parameters (circles) up to 50 GHz and the EC scaled models predictions for three bias conditions: lines - EM-based scaled model; dots - classical scaled model.

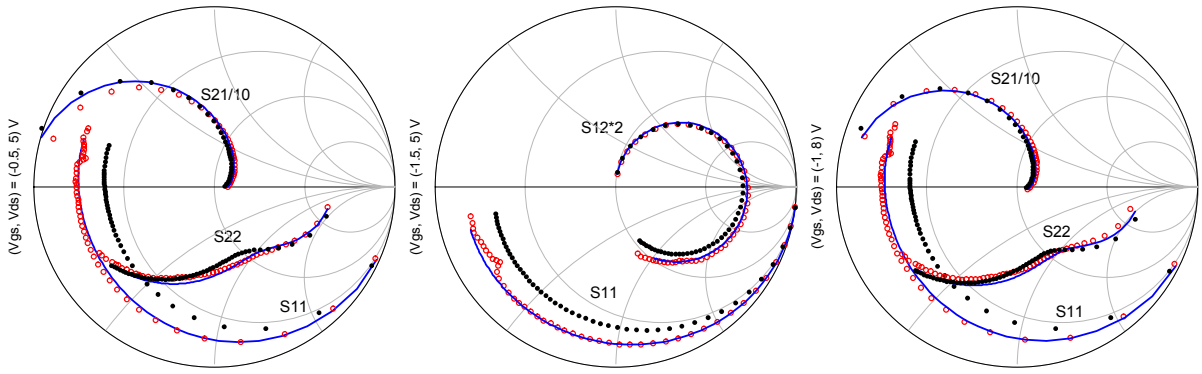


Fig. 4.6 Comparison between the 4x100 µm PHEMT measured extrinsic scattering parameters (circles) up to 50 GHz and the EC scaled models predictions for three bias conditions: lines - EM-based scaled model; dots - classical scaled model.

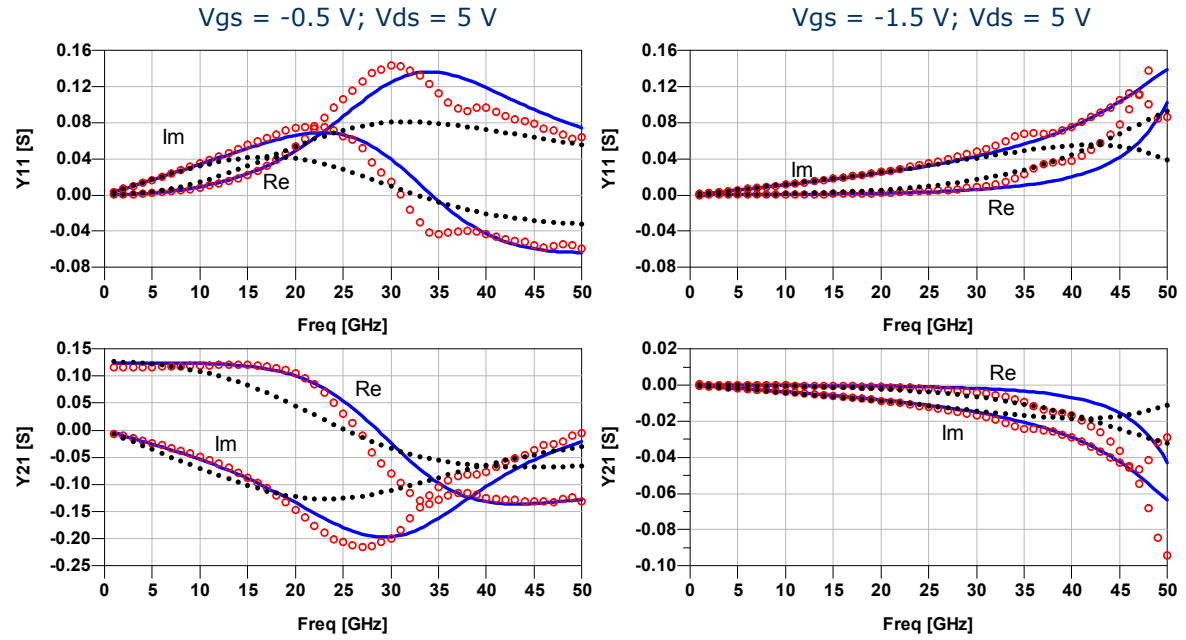


Fig. 4.7 Comparison between the 4x100µm PHEMT measured extrinsic admittance parameters Y_{11} and Y_{21} (circles) up to 50 GHz and the EC scaled models predictions: lines - EM-based scaled model; dots - classical scaled model. The figure refers to the Class-A bias point (left) and the pinched-off bias point (right).

4.4 Experimental Validation on a 0.25 µm GaAs PHEMT Technology.

Concerning the identification of nonlinear scalable model, the identification procedure of Chapter 3.3.1 can be applied to both equivalent circuit and look-up-table based modelling approaches. As an example, once identified the PHEMT compact distributed parasitic 4-port network, we decided to adopt the Nonlinear Discrete Convolution (NDC) Model described in [6]; in particular its current-voltage relationships are briefly recalled in Chapter 1.2.4. In order to take into account also low-frequency dispersive phenomena due to traps and device self heating, the

backgating model [7] have been also included in the nonlinear model. Its correction terms to the device low-frequency behaviour are briefly recalled in Chapter 1.2.5.

4.4.1 Reference Device

The closed-form method proposed in Chapter 3.3.1 is applied here to identify a scalable nonlinear device model of a 0.25 µm GaAs PHEMT having a total periphery equal to 300 µm (6x50 µm).

Once identified the PHEMT compact distributed parasitic 4-port network, DC and S-parameters measurements (carried out in the frequency range [4 GHz – 65 GHz]) have been exploited according to the identification procedure outlined in [6].

Fig.4.8, Fig.4.9 and Fig.4.10 show the model fitting to the intrinsic device measured admittance parameters, obtained after de-embedding the CW S-parameters measurements from the compact distributed parasitic network. In particular Fig.4.8 shows the NDC model fitting in the overall frequency range in the nominal bias condition, that is the bias point V_{GS} = -0.6 V, V_{DS} = 5 V where the backgating model has been extracted. Fig.4.9 and 4.10, instead, give an overall idea of the goodness of the extracted nonlinear model, showing the model fitting of the measured intrinsic admittance parameters at the frequency of 20 GHz as a function of the gate-source voltage and the gate-drain voltage respectively.

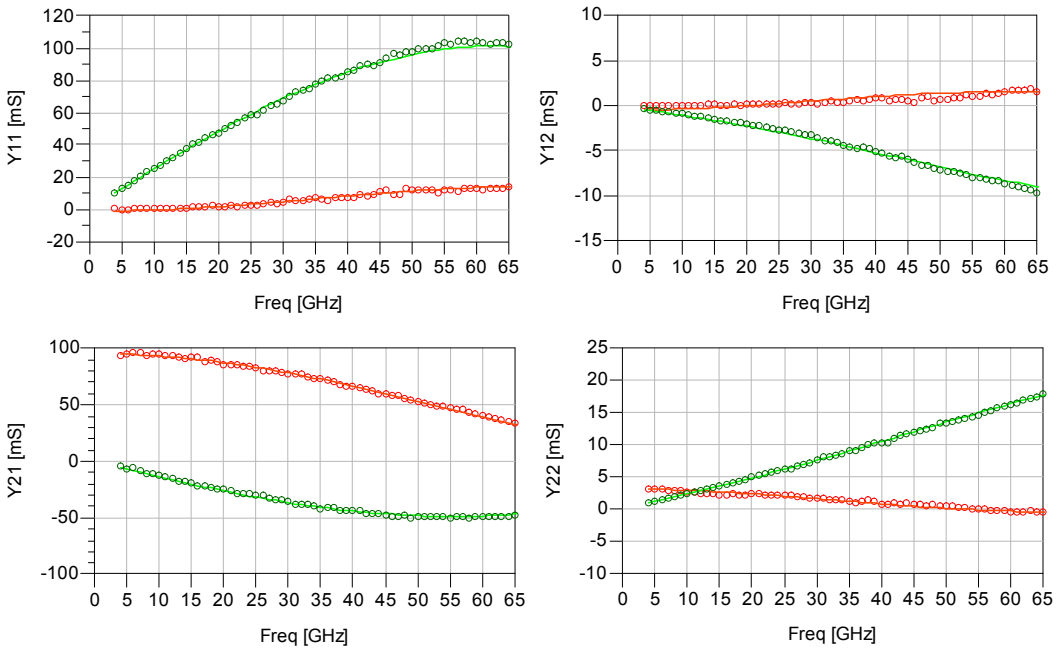


Fig.4.8 NDC model fitting (lines) to the measured intrinsic admittance parameters (circles) of the 6x50 µm PHEMT obtained after de-embedding from its compact distributed parasitic network. Bias condition: V_{GS} = -0.6 V, V_{DS} = 5 V, Freq. [4 – 65 GHz]. Real part – red, Imaginary part – green.

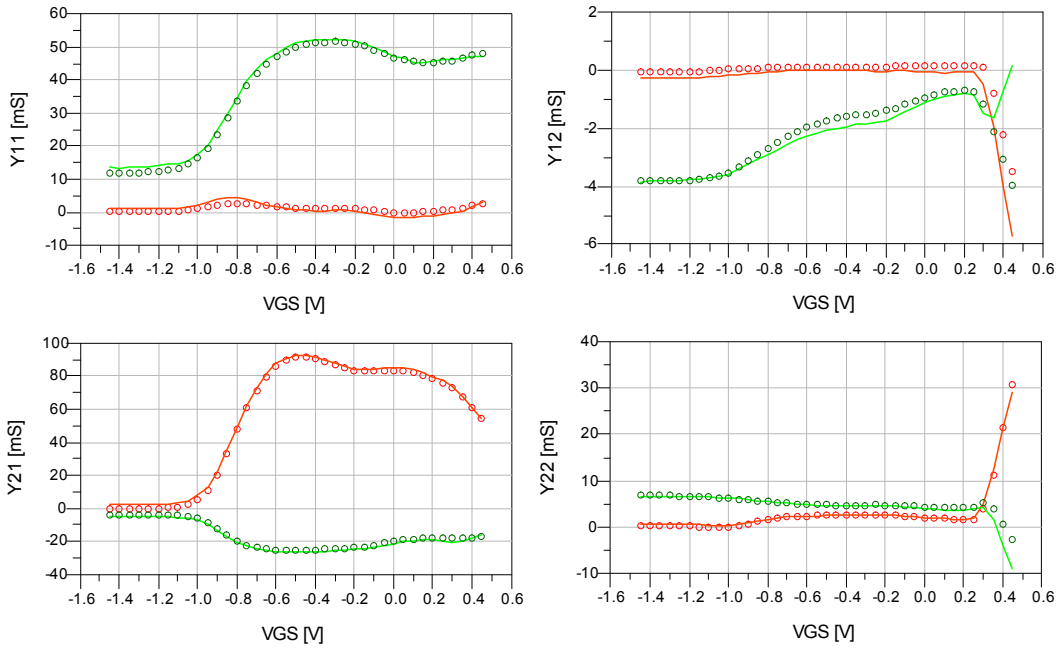


Fig.4.9 NDC model fitting (lines) to the measured intrinsic admittance parameters (circles) of the 6x50 µm PHEMT obtained after de-embedding from its compact distributed parasitic network. Comparison as a function of V_{GS}, V_{DS} = 5 V, Freq. = 20 GHz. Real part – red, Imaginary part – green.

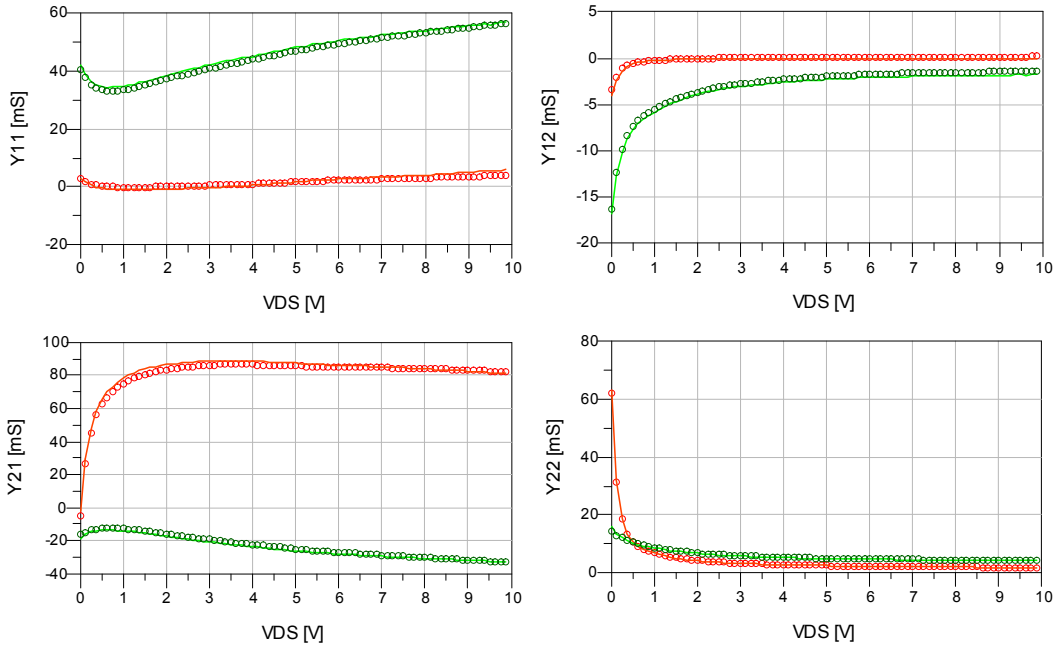


Fig.4.10 NDC model fitting (lines) to the measured intrinsic admittance parameters (circles) of the 6x50 µm PHEMT obtained after de-embedding from its compact distributed parasitic network. Comparison as a function of V_{DS}, V_{GS} = -0.6 V, Freq. = 20 GHz. Real part – red, Imaginary part – green.

Once verified the correctness of the NDC model extraction, the model has been used to predict the device behaviour.

In Fig.4.11 measured extrinsic DC drain current characteristics are compared to model predictions; as expected the model perfectly fits the measured data.

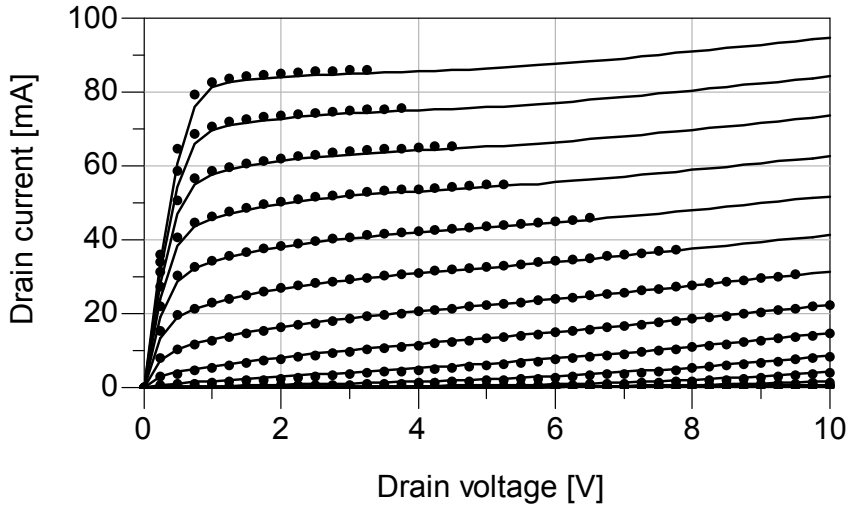


Fig. 4.11 DC I/V output characteristics of the 6x50 μm PHEMT. The curves are traced for V_{GS} from -1.4 to 0 V (step 0.1 V) and V_{DS} from 0 to 10 V (step 0.25 V). Model predictions – lines, device measurements – dots.

Figs.4.12 and Fig.4.13 exhibit model prediction versus measurements under small-signal operation. In particular, the good agreement of S-parameters versus frequency obtained in a class-A bias is shown in Fig.4.12, while small-signal predictions versus the gate-source voltage at 20 GHz is presented in Fig.4.13.

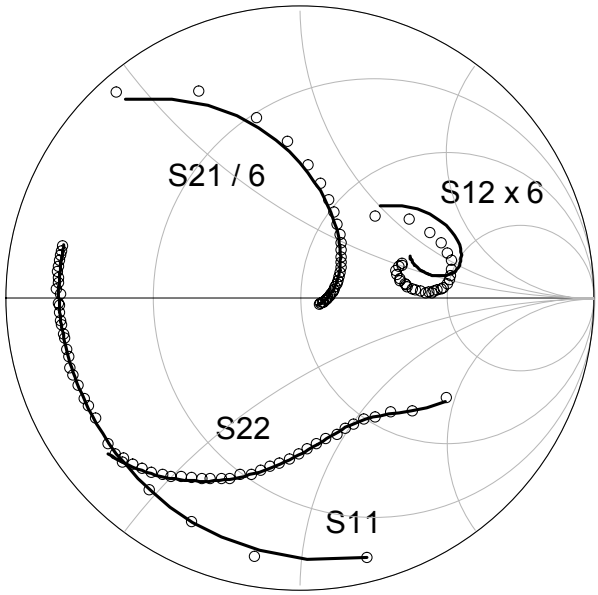


Fig. 4.12 Extrinsic S-parameters of the 6x50 μm PHEMT in the bias condition V_{GS} = -0.6 V, V_{DS} = 5 V. Comparison between the model predictions (lines) and the device measurements (circles). Frequency from 4 to 65 GHz.

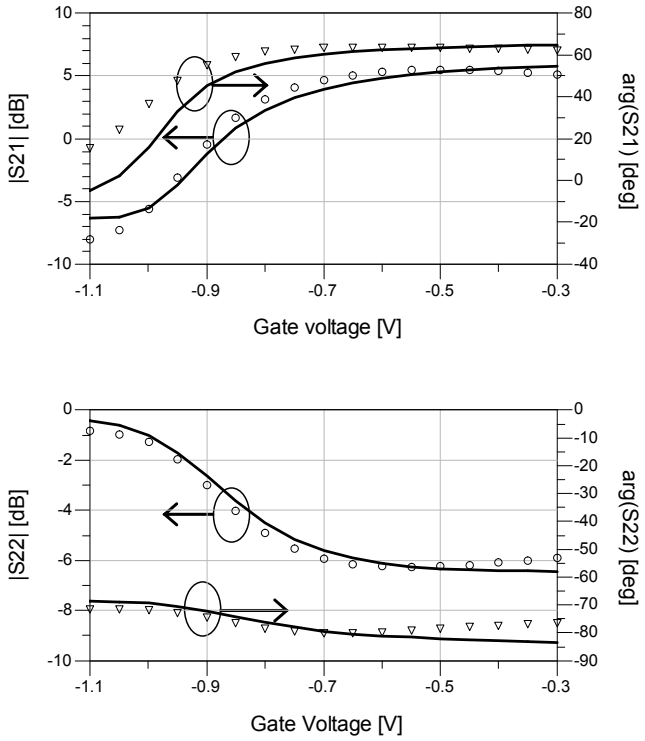


Fig. 4.13 Extrinsic S-parameters of the 6x50 μm PHEMT as a function of the gate-source voltage and V_{DS} = 5 V (freq = 20 GHz). Comparison between the model predictions (lines) and the device measurements – magnitude, circles and phase, triangles.

In order to validate the model under nonlinear dynamic operation we exploited measurements carried out by means of an LSNA (Large-Signal Network Analyzer) [8]. This instrument enables to

characterize simultaneously the voltage and current waveforms at the device terminals. Thanks to the ability of correlating instantaneous voltages and currents, the source of possible discrepancies between measurements and model predictions can be straightforwardly put in evidence.

In Fig.4.14, measurements carried out on the 6x50 μm PHEMT at 5 GHz (50 Ω source and load terminations) are shown. In particular the device is here biased under class-A (V_{DS} = -0.6 V , V_{DS} = 6 V) and class-B (V_{GS} = -1.1 V , V_{DS} = 6 V) operations. The curves refer to the device nonlinear dynamic trans- and output characteristics. The class-A operation shown corresponds to 2 dB gain compression.

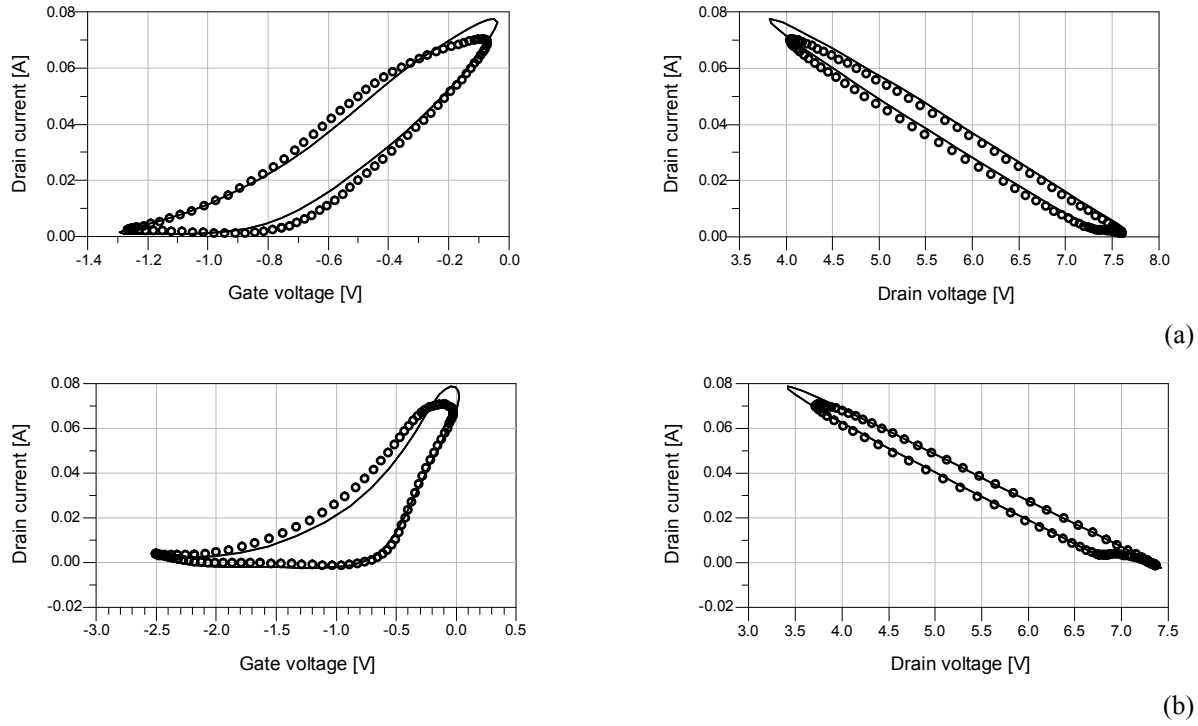


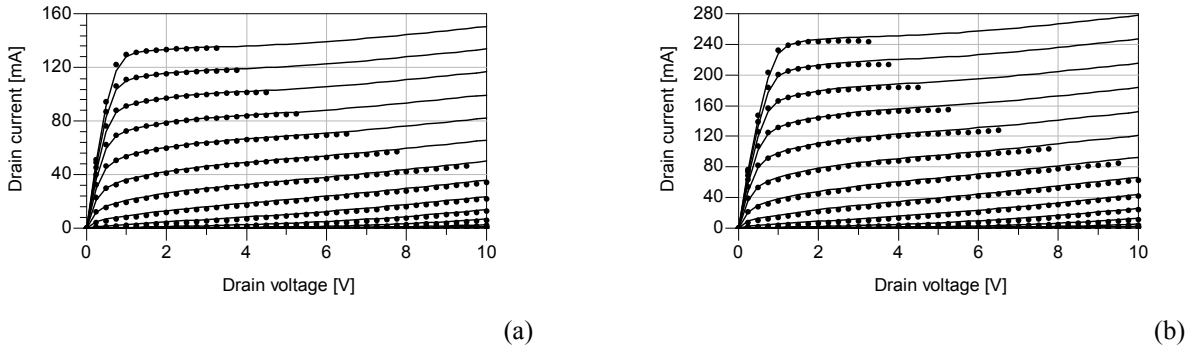
Fig. 4.14 6x50 μm PHEMT dynamic trans- and output characteristics at 5 GHz, 50 Ω source and load terminations. Comparison between model predictions (lines) and measurements (circles) for the device biased at V_{gs} = -0.6 V, V_{ds} = 6 V (a) and V_{gs} = -1.1 V, V_{ds} = 6 V (b).

4.4.2 Scaled Devices

As previously mentioned, the intrinsic device obtained by de-embedding S-parameter measurements from the parasitic distributed network, shows physically-consistent, short memory properties and is very suitable for the identification of a nonlinear device model. To definitely probe this issue, the 6x50 μm PHEMT, described in the previous section, has been considered as the "reference device" for the actual technological process. This choice allows testing the nonlinear

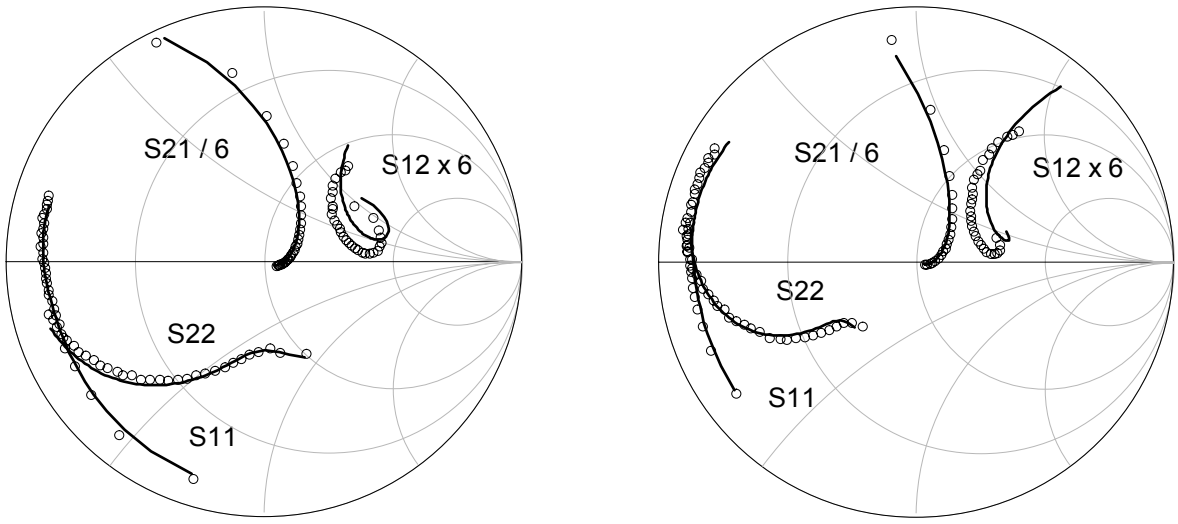
model scaling capabilities towards geometries having larger peripheries and a different number of gate fingers. In order to scale the 6x50 μm PHEMT nonlinear model to a different device geometry, the linearly scalable intrinsic NDC model is embedded in the compact distributed parasitic 4-port network (obtained through a new EM simulation and a new closed-form identification procedure) of the given device.

The extrinsic DC I/V characteristics for the two scaled devices, namely a 10x48 μm and a 12x75 μm PHEMTs, are shown in Fig.4.15. As it can be seen, the predicted DC curves for the scaled devices are in excellent agreement with measurements.



(a) (b)

Fig. 4.15 DC I/V output- characteristics of the (a) 10x48 μm and (b) 12x75 μm PHEMTs. The curves are traced for V_{GS} from -1.4 to 0 V (step 0.1 V) and V_{DS} from 0 to 10 V (step 0.25 V). Scaled model predictions – lines, device measurements – dots.



(a) (b)

Fig. 4.16 Extrinsic S-parameters of the 10x48 μm (a) and 12x75 μm (b) PHEMTs in the bias condition V_{GS} = -0.6 V, V_{DS} = 5 V. Comparison between the scaled model predictions (lines) and the device measurements (circles). Frequency from 4 to 65 GHz.

The extrinsic S-parameter predictions (4 to 65 GHz) for the two scaled devices are shown, for a typical class-A operation bias conditions, in Fig.4.16. Also in this case the agreement between model prediction and measurements is pretty good.

As an additional validation of the scalable nonlinear model predictions under linear operation, the extrinsic scattering parameters predictions of the scaled PHEMTs are shown as a function of the bias condition at fixed frequency in Fig.4.17.

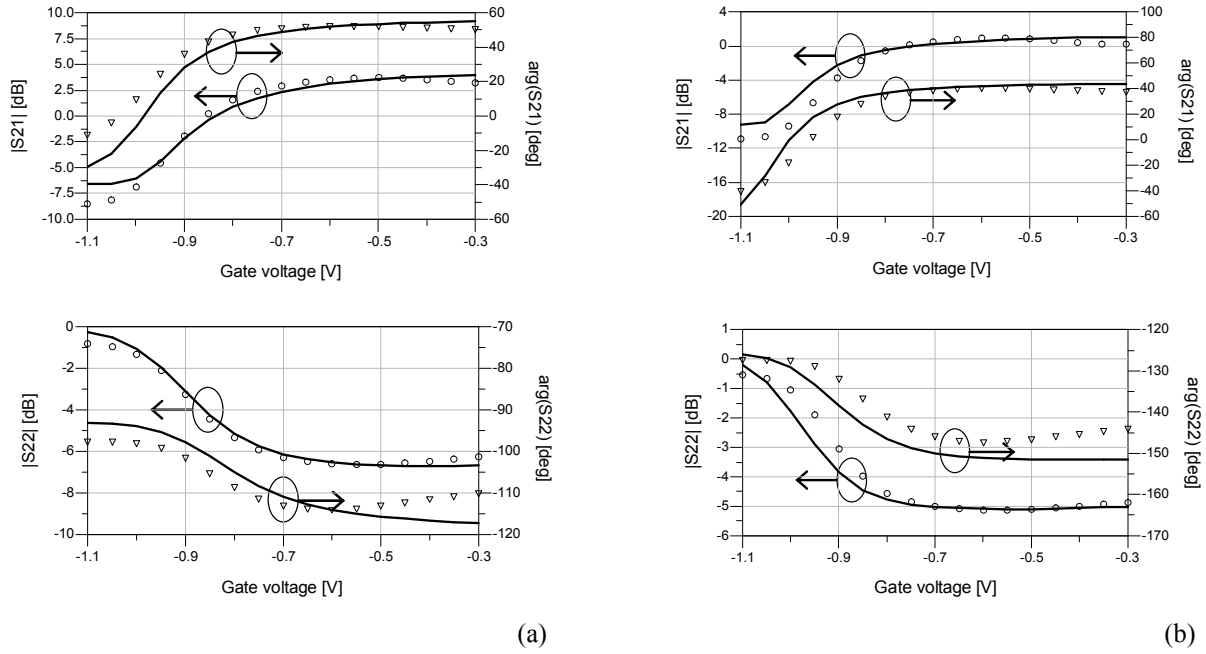


Fig. 4.17 Extrinsic S-parameters of the 10x48 μm PHEMT (a) and the 12x75 μm PHEMT as a function of the gate-source voltage and V_{DS} = 5 V (freq = 20 GHz). Comparison between the model predictions (lines) and the device measurements – magnitude, circles and phase, triangles.

In Figs. 4.18-4.19 nonlinear measurements carried out on the 10x48 and 12x75 μm PHEMTs at 5 GHz (50 Ω source and load terminations) are shown; in particular the devices were biased under class-A (V_{GS} = -0.6 V , V_{DS} = 6 V) and class-B (V_{GS} = -1.1 V , V_{DS} = 6 V) operations; the curves refer to the device nonlinear dynamic trans- and output characteristics.

Fig. 4.18 clearly shows that the model performances are practically the same when it is scaled with respect to the number of fingers. It should be noted that finger-number scaling is quite critical, since that the device access structure is dramatically modified. For this PHEMT device, class-A operation refers to 3.5 dB gain compression.

Considering the 12x75 μm device the "reference device" model is scaled with respect to the two parameters (number and width of fingers). Fig.4.19 quantifies the scaled model prediction accuracy. In this case, class-A operation refers to 2 dB gain compression.

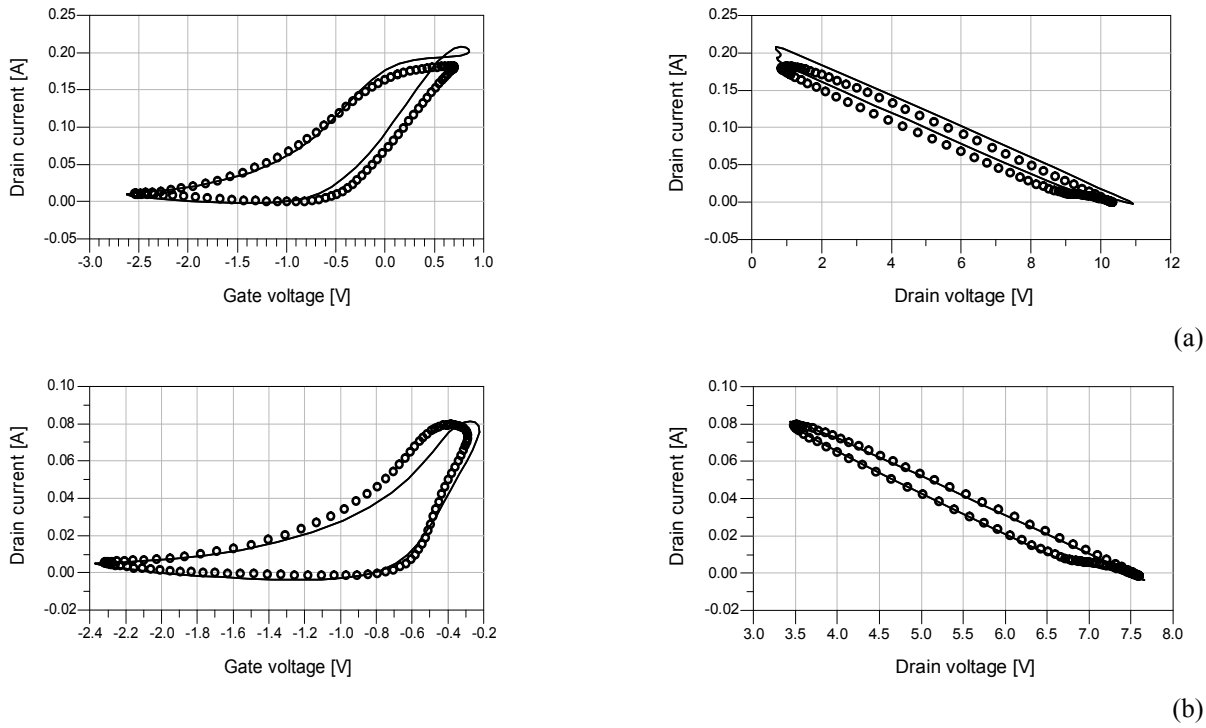


Fig. 4.18 10x48 μm PHEMT dynamic trans- and output characteristics at 5 GHz, 50 Ω source and load terminations. Comparison between model predictions (lines) and measurements (circles) for the device biased at V_{GS} = -0.6 V, V_{DS} = 6 V (a) and V_{GS} = -1.1 V, V_{DS} = 6 V (b).

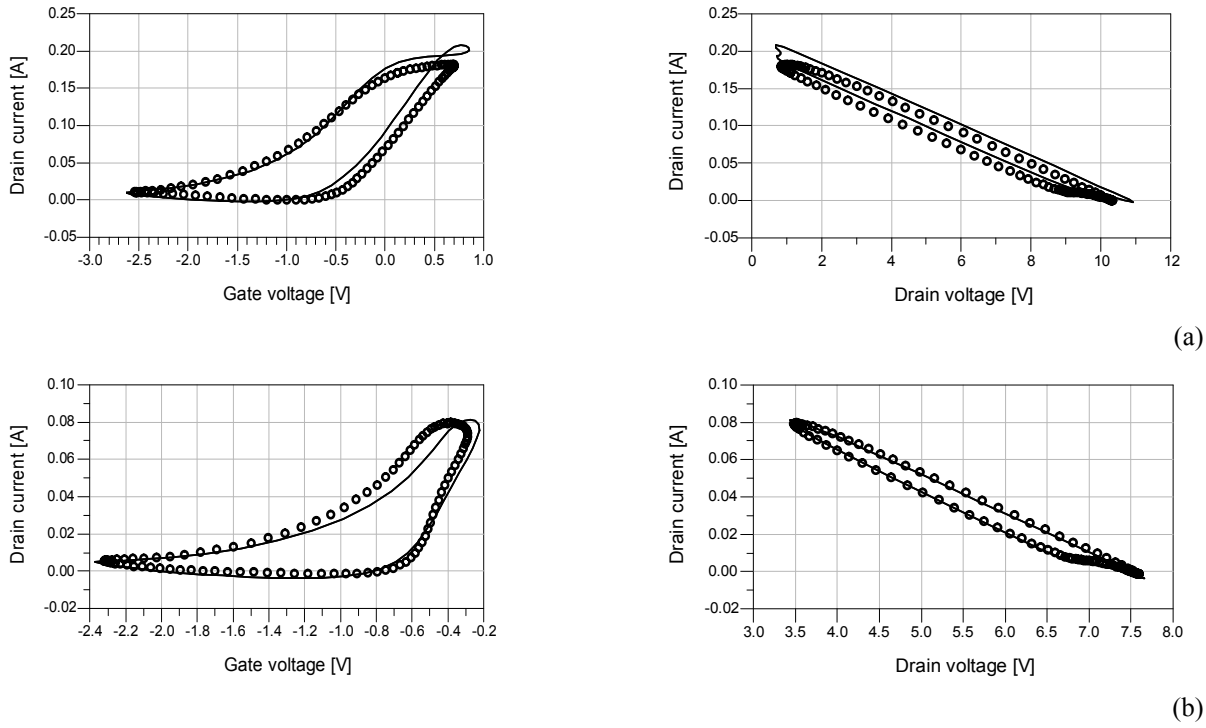
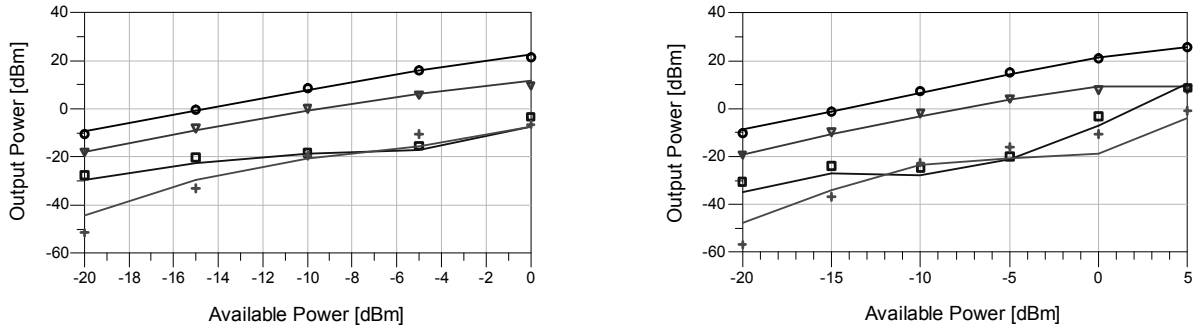


Fig. 4.19 12x75 μm PHEMT dynamic trans- and output characteristics at 5 GHz, 50 Ω source and load terminations. Comparison between model predictions (lines) and measurements (circles) for the device biased at V_{GS} = -0.6 V, V_{DS} = 6 V (a) and V_{GS} = -1.1 V, V_{DS} = 6 V (b).

To further put in evidence the fair prediction capabilities of the proposed modeling approach, output power predictions at fundamental and harmonic frequencies are compared to measurements for different power levels in Fig.4.20. In particular the two figures refer to the 10x48 μm and 12x75 μm devices in class B conditions, respectively.

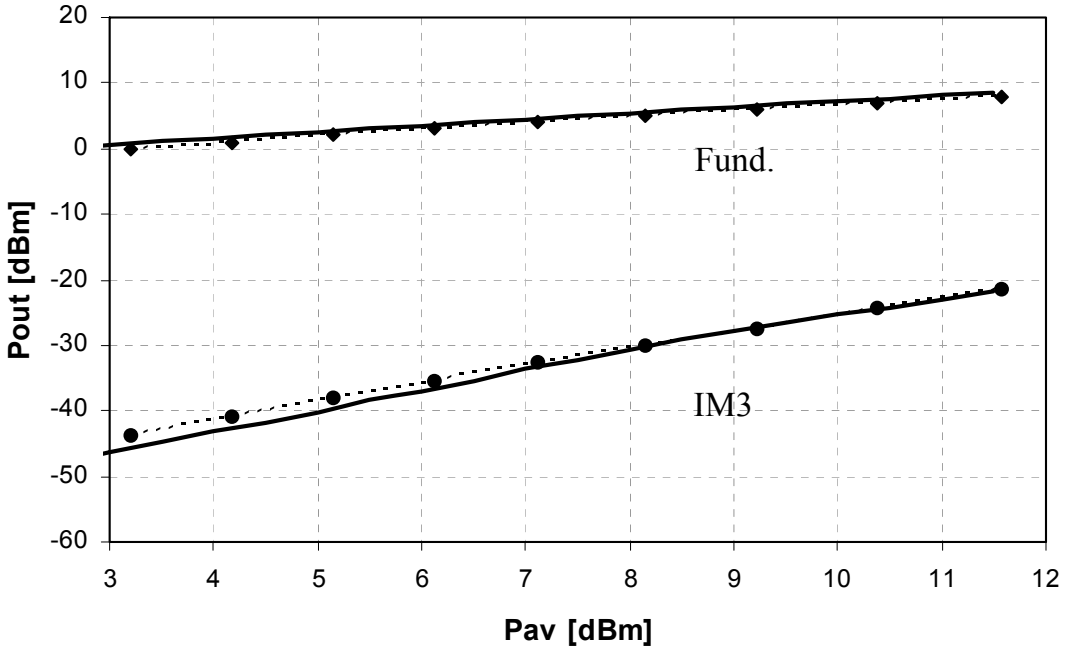


(a) (b)

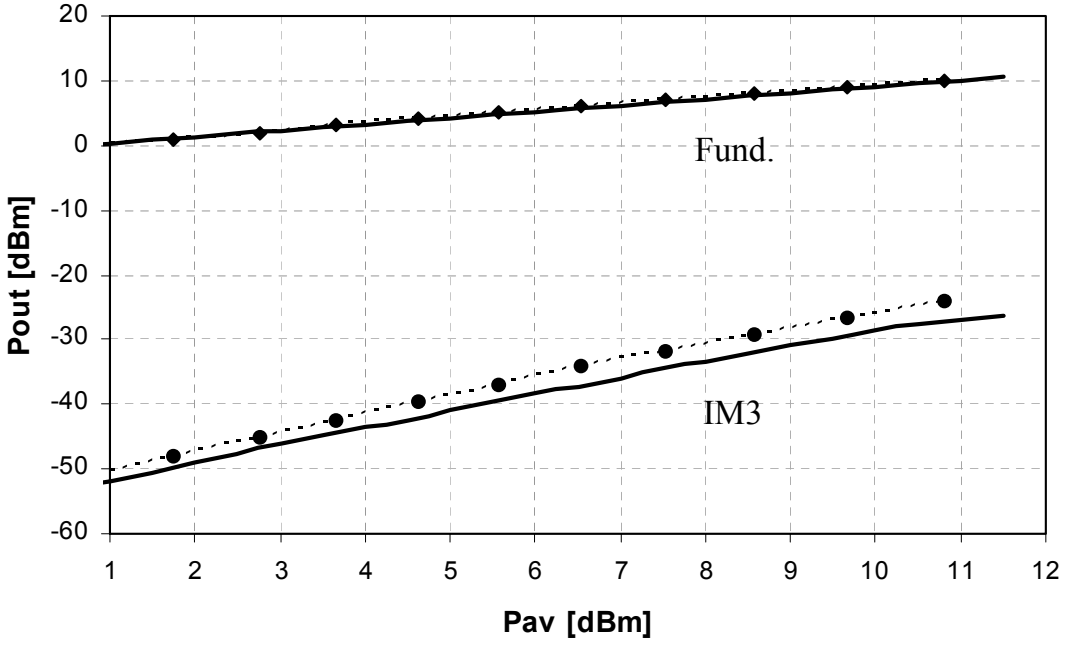
Fig. 4.20 Output power predictions at fundamental and harmonics (lines) are compared to measurements for different power levels (symbols). In particular the two figures refer to the class-B bias condition for the (a) 10x48 μm and (b) 12x75 μm PHEMTs.

In order to provide model validation at more realistic loading conditions and higher frequencies of operation, two-tone measurements have been carried out at 37 GHz (10 MHz tone spacing) for a 10x60μm PHEMT of the same foundry process, biased for class-A operation. Fig.4.20 shows the scaled 10x60μm PHEMT model predictions compared to the IMD measurements with two very different load terminations. The high accuracy achieved in the prediction of IMD makes the model suitable for millimetre-wave high linearity power amplifier design.

It is worth mentioning that model identification, as previously stated, has been here carried out on the basis of a single, "reference" electron device. However, the simplicity and closed-form feature of the identification algorithms can be easily extended to account for a larger set of "reference devices" having different peripheries. Definitely, this approach can be effectively exploited to obtain highly accurate scalable models over a very wide set of devices having remarkable different geometries as it is usually required in advanced, general-purpose foundry processes.



(a)



(b)

Fig. 4.21 IMD at 37 GHz (10 MHz tone spacing). Scaled 10x60μm PHEMT model prediction (lines) compared to the device measurement (symbols) both for the fundamental tone as well as for the 3rd order intermodulation tone. Device biased at VGS = -0.55 V, VDS = 6.5V and source impedance ZS = 49.547 – j 9.652. Load impedance: a) ZL = 30.7 – j 0.88; b) ZL = 14.4 + j 9.7.

4.5 Experimental Validation on a 0.1 μm InP HEMT Technology.

The simplified approach for the identification of a distributed parasitic network has been also adopted to extract a preliminary scalable nonlinear device model for a 0.1 μm InP HEMT transistor having a total periphery of 80 μm (2x40 μm). This device consists of a large bandgap InP channel on InP substrate containing an InP/AlInAs composite barrier, as reported in [9].

In particular, DC and CW S-parameter measurements (carried out in the frequency range [4 GHz – 65 GHz]) have been exploited according to the procedure outlined in [6] to identify the Nonlinear Discrete Convolution model.

In Fig.4.22 measured extrinsic DC drain current characteristics are compared to model predictions; as expected the model perfectly fits the measured data.

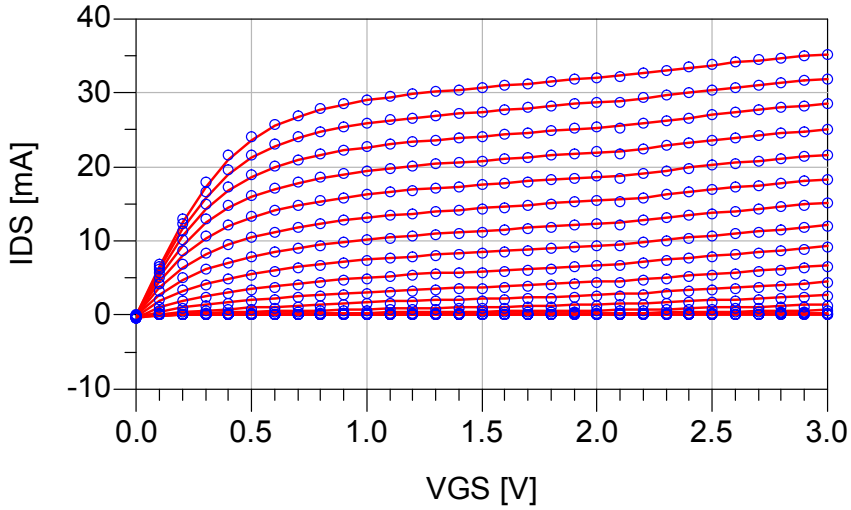


Fig. 4.22 DC I/V output characteristics of the 2x40 μm InP HEMT. The curves are drawn for Vgs from -0.8 V to 0 V (step 0.05 V) and Vds from 0 to 3 V (step 0.1 V). Model predictions – lines, device measurements – dots.

Fig.4.23 put in evidence model accuracy under small-signal operating conditions by comparing measured S-parameters and coherent model predictions. To further put in evidence the accuracy of the nonlinear model in linear operation on the entire identification grid, small-signal predictions, as a function of the gate-source voltage, at 40 GHz are displayed in Fig. 4.24.

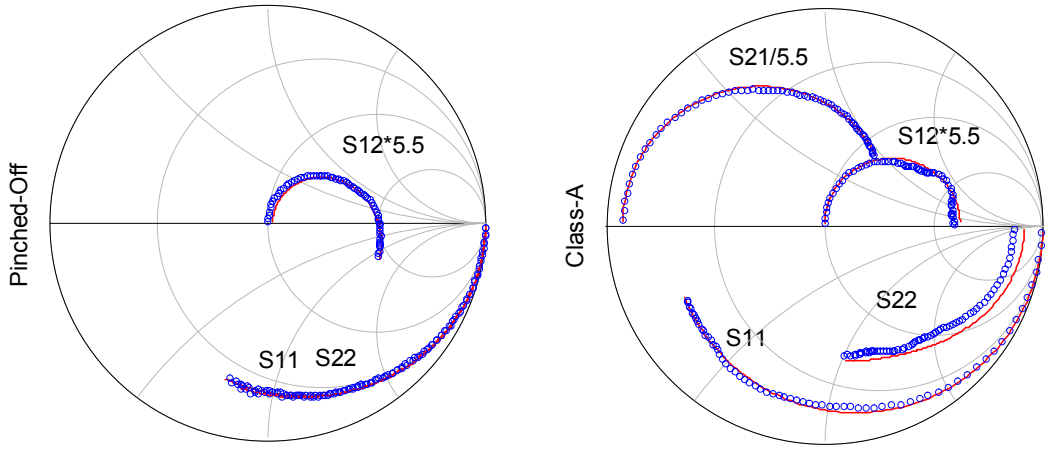


Fig. 4.23 Extrinsic S-parameters of the 2x40 µm InP HEMT in both pinched-off bias condition and class-A bias condition. Comparison between model predictions (lines) and device measurements (circles). Frequency from 0.5 to 67 GHz.

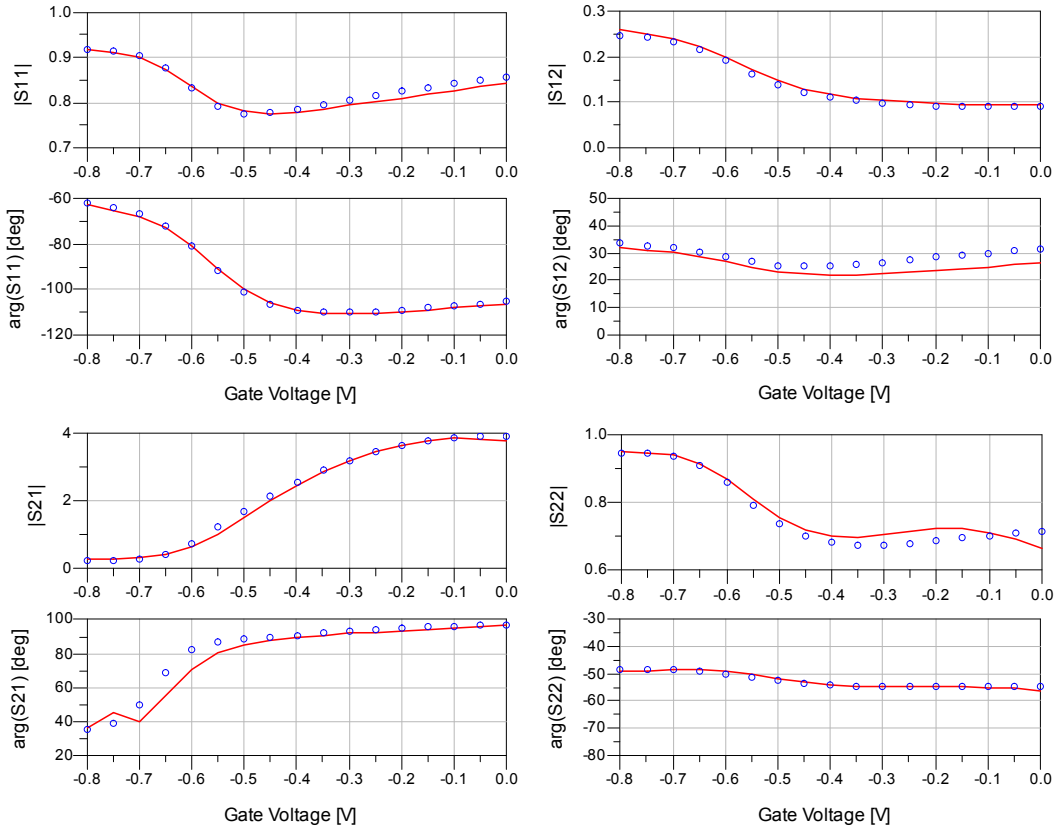
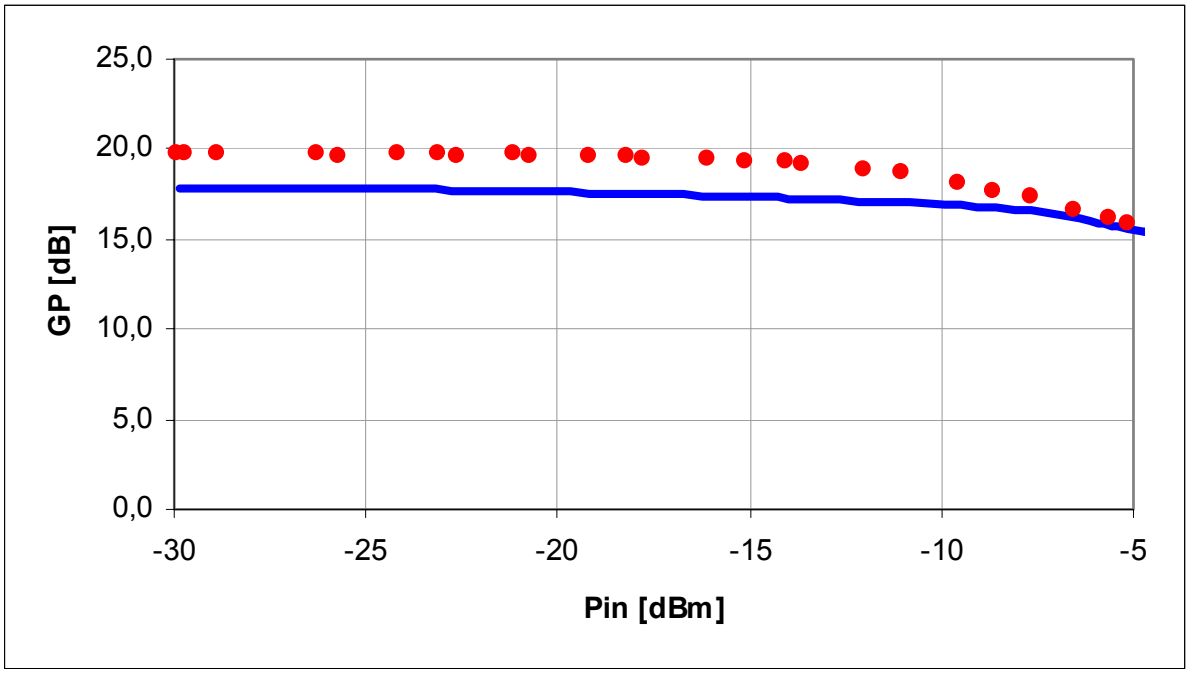
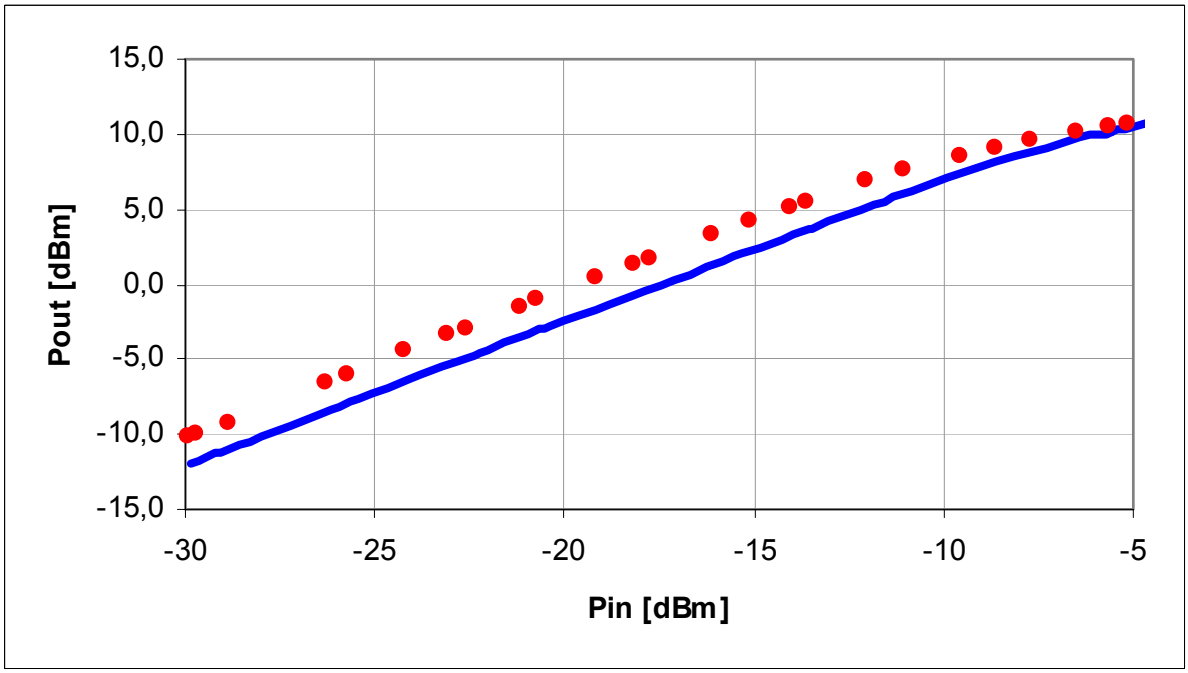


Fig. 4.24 Extrinsic S-parameters of the 2x40 µm InP HEMT as a function of the gate-source voltage and V_{d0} = 2 V (freq = 40 GHz). Comparison between model predictions (lines) and device measurements (circles).

In order to validate the model under nonlinear operation, load-pull measurements at 27 GHz in two different class-A operation bias conditions have been carried out on the 2x40 µm HEMT. The model predictions are compared with the device measurements in Fig.4.25 and Fig.4.26.

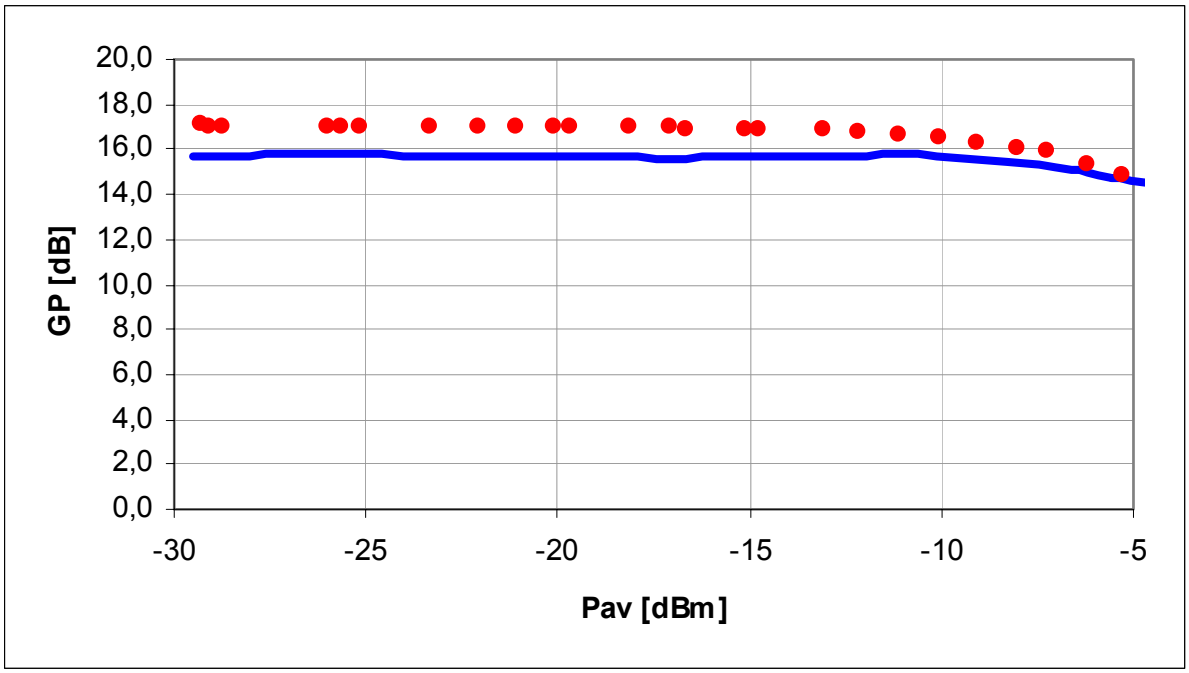


(a)

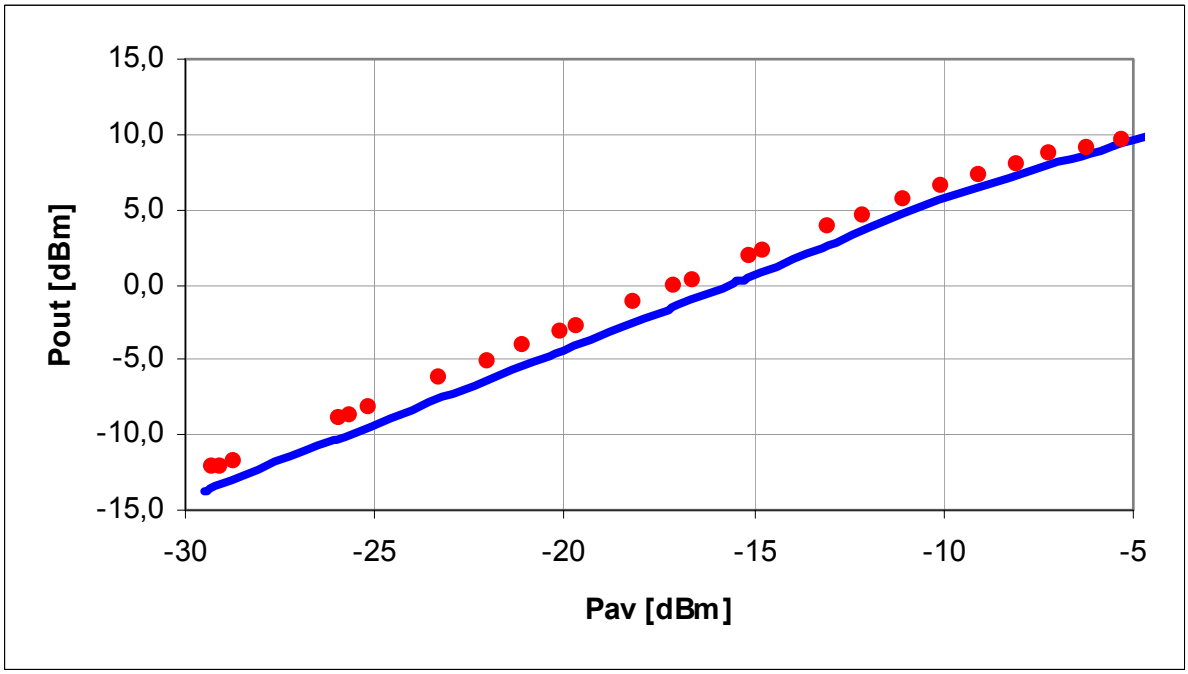


(b)

Fig.4.25 Power gain (a) and output power (b) as a function of the power at the input of the 2x40µm HEMT at 27 GHz. Bias: V_{GS} = -0.3 V, V_{DS} = 2 V. Load Termination: Γ_L = 0.33 ∠0.32. The model predictions (lines) are compared to the device measurement (symbols).



(a)



(b)

Fig.4.26 Power gain (a) and output power (b) as a function of the power at the input of the 2x40µm HEMT at 27 GHz. Bias: V_{GS} = -0.4 V, V_{DS} = 2 V. Load Termination: Γ_L = 0.39 ∠0.34. The model predictions (lines) are compared to the device measurement (symbols).

It is important to notice that this is only a preliminary nonlinear validation. In fact the model predictions shown in Fig.4.25 and Fig.4.26 are obtained without considering the modeling of low frequency dispersive effect whose model hasn't extracted yet.

4.6 Computational Efficiency Considerations.

This EM-based modelling approach doesn't involve real time electromagnetic and circuit co-simulations as proposed in many works, like for instance the procedure outlined in [10].

The EM simulation is here only used in order to identify a linear extrinsic distributed parasitic network. Successively, such a network is used for circuit simulations, as a table-based linear network (TB-LN), i.e. a CAD readable look-up table, embedded with an empirical dynamic nonlinear model for the intrinsic device. The flow chart reported in Fig.4.27 clarifies these points.

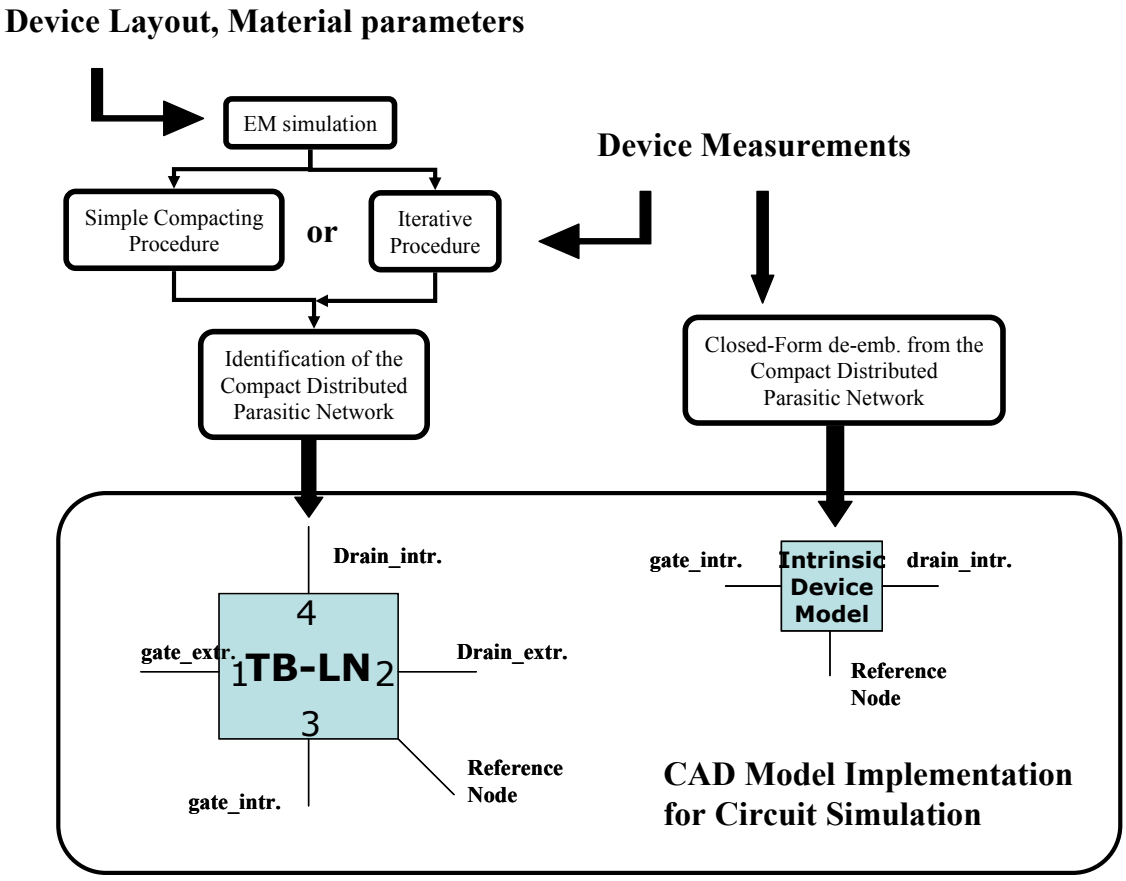


Fig. 4.27 Flow-chart which explains the steps to be carried out from the device characterization (EM simulations plus device measurements) to the CAD model implementation.

The major computational effort occurs in the device characterization phase. In fact this latter consists in performing the EM simulations (for the reference device and for all the scaled devices) and device measurements (at least DC and CW S-parameter measurements) only for the reference device.

The EM simulations and the use of one of the two compacting procedures (explained in Chapter 3.3.1 and 3.3.2) are necessary in order to identify the TB-LN of the reference device and the scaled devices, while the device measurements of the reference device are necessary in order to extract the nonlinear empirical model for the intrinsic core of the device. It is important to notice that the reference device measurements are used also to guarantee the over-determination, with respect to the bias, of the iterative method of Chapter 3.3.2.

Once the set of devices has been characterized and the nonlinear scalable model extracted, the model can be implemented in the circuit simulator (in the way outlined in Fig.4.27) and the computational effort associated to the nonlinear model is practically the same of conventional empirical models.

To summarize the proposed modelling approach requires an identification procedure with a time effort which is comparable to the time needed when using conventional procedures. The extracted model needs the same CPU time of any other conventional empirical model to run any circuit simulation.

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CHAPTER 5

OPTIMAL APPROXIMATION OF ELECTRON DEVICE NONLINEAR CHARACTERISTICS

5.1 Introduction.

Empirical models of electron devices are presented in Chapter 1. They are based on the measured electrical characteristics of the electron device and they are described in terms of an extrinsic linear parasitic network connecting the nonlinear intrinsic device to external world. The problems inherent to the modelling of the extrinsic parasitic network, including its scalability properties, are widely discussed in Chapter 2, 3 and 4. Chapter 1 provides also a brief review of the techniques adopted for the description of the nonlinear effects associated with the intrinsic device.

In order to correctly model the nonlinear behaviour of the intrinsic device, its mathematical (or equivalent circuit) description must be chosen first. Then it is possible to decide which measurements are necessary for the characterization of the device behaviour and the model can be identified.

Two of the more important aspect of empirical modelling are the correct measurement of the device nonlinearities in the device characterization phase, and the reconstruction of such nonlinear characteristics in the model identification phase. Being able of accomplish these two tasks allows the model to accurately predict the actual device behaviour in nonlinear regimes.

Since the nonlinear characteristics (such as static/pulsed I/V, C/V and Q/V relationships) are necessarily known (either directly measured or evaluated by means of numerical integration procedures) over a discrete grid of bias conditions, the problem arises of making the model able to

provide near optimal approximations of these algebraic nonlinear characteristics through continuous and differentiable functions.

Analogous problems are encountered in the behavioural modelling of communication system building blocks, such as, for instance, in power amplifiers, where AM/AM, AM/PM curves must be accurately reconstructed from sampled values.

Two alternatives are basically available: analytical or look-up-table (LUT) based approximations. Analytic functions, typically dependent on a limited number of scalar parameters, are widely adopted by many empirical modelling approaches (e.g. [1]). They usually provide fast numerical evaluation, good convergence properties of the Harmonic Balance solution algorithms and, above all, reasonably good predictive accuracy especially under saturated power operation. However, although the number of function parameters involved is typically quite small, their extraction quite often requires nonlinear optimization algorithms with consequent problems of either non-univocal (and sometimes non-physical) values identification and possible convergence to local minima. In some work available in literature, is shown how this kind of approach may also prove to be largely inadequate when accurate prediction of *local* nonlinearity, e.g. inter-modulation distortion (IMD), is needed, such as in the case of highly-linear Power Amplifier (PA) design.

In order to overcome the above-mentioned problems, an original, data approximation algorithm is proposed in this chapter for the exploitation in the framework of empirical table look-up nonlinear models (e.g. [2], [3]). The proposed approach is based on the strong analogy between time-domain signal reconstruction from a set of samples and the continuous approximation of device nonlinear characteristics on the basis of a finite grid of measurements. According to this criterion, nonlinear empirical device modelling can be carried out by using, in the sampled voltage domain, typical methods of the time-domain sampled-signal theory.

Experimental validation is provided through the differentiability evaluation of the proposed approximation formula, in comparison with conventional cubic-spline interpolation, and through the IMD prediction of a GaAs-based PHEMT by adopting the proposed approximation algorithm along with a previously presented nonlinear black-box model of electron devices [4].

5.2 Band-Limited Data Approximation.

We first consider the problem of the continuous approximation of a generic nonlinear characteristic $F(v)$ of a single port electron device through a general-purpose function $\tilde{F}(v,\underline{P}) \cong F(v)$ where P_k represents a set of scalar parameters. In order to improve reliability and

robustness in the parameter extraction phase general-purpose approximating functions having a linear dependence on parameters (P_k) can be conveniently adopted, i.e.:

$$\tilde{F}\left(v,\underline{P}\right)=\sum_k P_k h_k\left(v\right) \tag{5.1}$$

where the $h_k\left(v\right)$ in (5.1) are a suitable set of *base functions*. This is a convenient choice since robust (i.e., unambiguous) parameter extraction can be carried out by means of linear regression procedures, provided that a sufficiently large set of measurements is used.

For example, if the base functions are triangular, as shown in Fig.5.1, (5.1) express the interpolation formulae of the conventional Piece-Wise Linear interpolator (PWL). It is simple and computationally efficient, preserves monotonicity, no spurious oscillations occur and it is easily generalized to n-dimensional functions, but it is non differentiable and it doesn't provide any data smoothing. If the base functions are the 3rd order splines, as shown in Fig.5.2, (5.1) express the interpolation formulae of the conventional Cubic-Spline interpolator. Despite it is twice differentiable and computationally efficient, it does not necessarily preserve monotonicity and it might provide spurious oscillating behaviour in presence of noisy measurements.

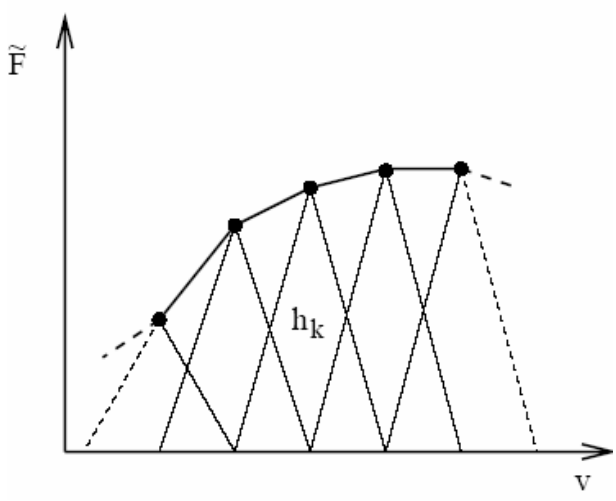

Fig. 5.1 Base functions of the conventional PWL interpolator.

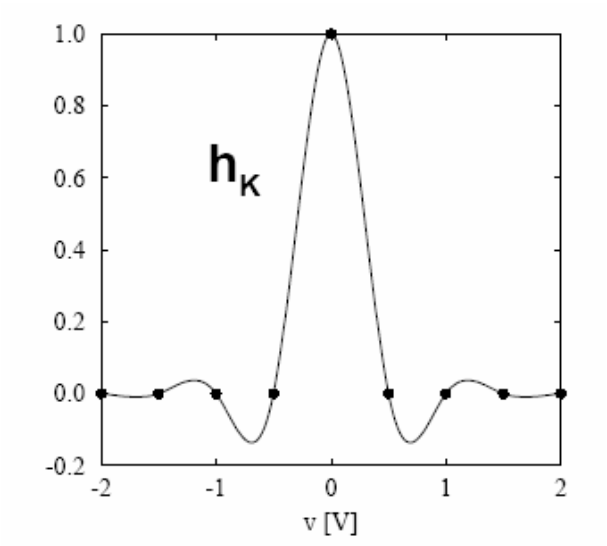

Fig. 5.2 Base functions of conventional cubic-spline interpolator.

Starting from this very general approach, a new method is proposed on the basis of the strict analogy between the approximation of nonlinear characteristics measured over a discrete voltage grid and the reconstruction of time-domain waveforms from sampled data. In particular, according to this analogy:

1) voltage-domain corresponds to a virtual time-domain
2) measurements represent samples of the actual characteristic in the voltage space (analogously to the time-domain samples of a signal)
3) function reconstruction (i.e., interpolation of samples) is carried out by low-pass filtering (LPF) the sampled function.

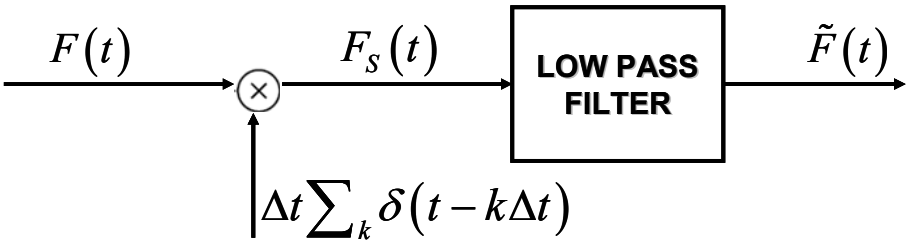

Fig. 5.3 Sampled signal processed by an ideal Low Pass Filter.

More precisely, according to Fig.5.3, by considering a uniform sampling (i.e., $v_k = k\,\Delta v$), the approximating function $\tilde{F}(v, \underline{P})$ can be obtained through the linear convolution of an LPF pulse response *h* and the voltage-domain sample function F_S:

$$\tilde{F}\left(v,\underline{P}\right) \doteq F_S\left(v,\underline{P}\right) * h\left(v\right) = \Delta v \sum\nolimits_k P_k h\left(v - k\Delta v\right) \tag{5.2}$$

where $F_S\left(v,\underline{P}\right) = \Delta v \sum\nolimits_k P_k \delta\left(v - k\Delta v\right)$ and $P_k = F\left(k\Delta v\right)$, $\delta\left(\cdot\right)$ being the Dirac function. Thus, according to signal sampling theory, if the actual nonlinear characteristic $F\left(v\right)$ is *band-limited*[1] with bandwidth B, the characteristic can be exactly reconstructed provided that an adequate sampling step Δv is chosen, i.e., $\Delta v < (2B)^{-1}$, and h coincides with the pulse response of an ideal LPF with cut-off frequency equal to the function bandwidth B.

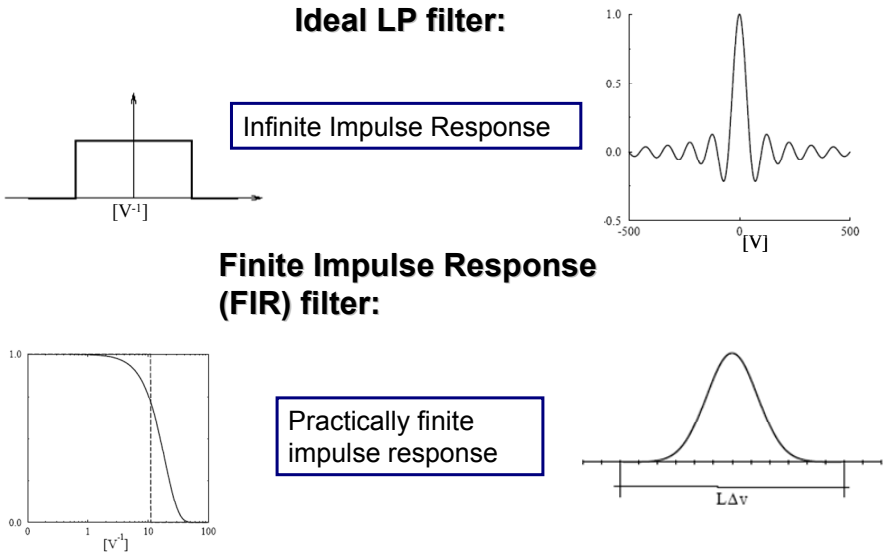

Fig. 5.4 Ideal versus FIR filter. The latter is practically feasible thank to its finite impulse response.

The above approach, with the same exactness property, can be generalized to the bi-dimensional case for the reconstruction of a characteristic $F\left(v_1, v_2\right)$, provided that the $h_{2D}\left(v_1, v_2\right)$ pulse response of an ideal 2D-LPF is defined. In the present work we assume:

$$h_{2D}\left(v_1, v_2\right) = \Delta v_1 \Delta v_2 \sum\nolimits_k h_1\left(v_1\right) h_2\left(v_2\right) \tag{5.3}$$

where $h_1\left(\cdot\right)$ and $h_2\left(\cdot\right)$ are the pulse responses of ideal 1D-LPF's having bandwidths B_1, B_2 with respect to the variables v_1, v_2, respectively.

Thus, if $P_{k,r} = F\left(k\Delta v_1, r\Delta v_2\right)$ are the 2D samples over the v_1, v_2, voltage grid, the bi-dimensional reconstructing formula for F becomes:

[1] In our analogy "bandwidth" actually corresponds to "nonlinearity", so that *practically limited bandwidth* involves *smooth nonlinearity*.

$$\tilde{F}\left(v_1, v_2, \underline{P}\right) = \Delta v_1 \Delta v_2 \sum_{k,r} P_{k,r} h_1\left(v_1 - k\Delta v_1\right) h_2\left(v_2 - r\Delta v_2\right) \tag{5.4}$$

According to Fig.5.4, since an ideal filter involving an infinitely long pulse response cannot be practically implemented, a Finite Impulse Response (FIR) filter must be adopted, which involves some approximations in the function reconstruction. However, the FIR-LPF filter has also the advantage of providing a smoothing effect on the noise-like measurement errors.

The shape of the 1D pulse responses $h_i\left(v_i\right)$ (i=1,2) in (5.3) can be chosen for a smooth function approximation, by taking also into account specific requirements of nonlinear ED modeling, in particular: linear exactness (i.e., linear $F\left(v\right)$ with linear sequence of P_k's), monotonic correctness (i.e., monotonic $F\left(v\right)$ with monotonic sequence of P_k's) and possibly fast asymptotic convergence (e.g., approximation error decreasing at least quadratically for $\Delta v \to 0$). In particular, we propose an "hybrid" filter consisting in the cascade of a Gaussian and a $sinc^2$ transfer functions in the 1/v (frequency equivalent) domain, as shown in Fig.5.5.

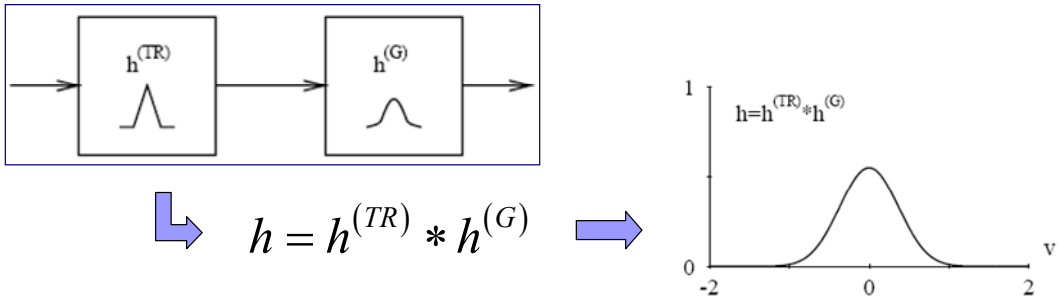

Fig. 5.5 The developed hybrid cascade FIR filter.

This leads to a good FIR approximation of an ideal LPF with a relatively short pulse response, which can be expressed analytically in the voltage domain as the convolution of triangular and Gaussian functions. This corresponds to a simple, yet quite efficient, smooth and non-oscillating interpolator, which can also be interpreted as the Gaussian filtering of a Piece-Wise Linear (PWL) interpolator.

Great accuracy in approximation can be obtained provided that an adequate sampling step Δv is used. The standard deviation σ of the gaussian filter is a tuning parameter which controls the number of samples considered in the computation of the impulse response of the hybrid filter.

5.3 Application to LUT-based nonlinear models.

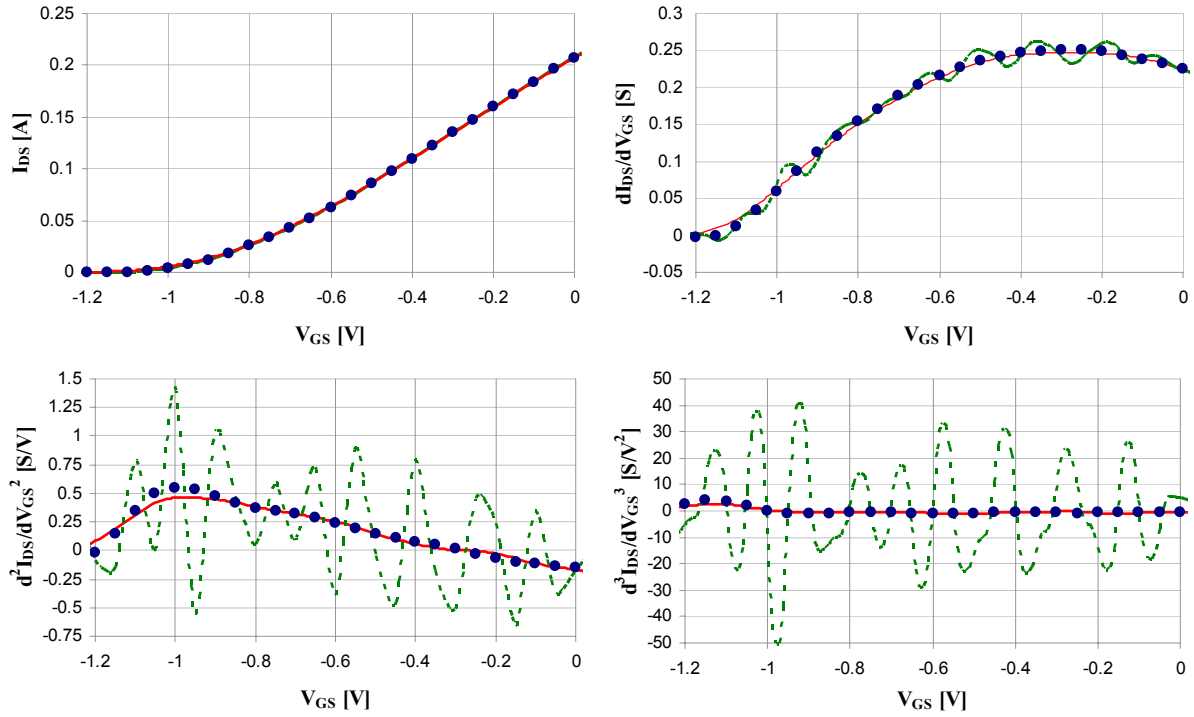

Fig. 5.6 Pulsed I/V trans-characteristic of the 0.25μm PHEMT at V_{DS} = 6 V and its derivatives with respect to V_{GS}. Comparison between the analytical functions (dots) and the approximated-interpolated functions using cubic-splines (dashed lines) and the proposed approximation formula (solid lines).

In order to evaluate the performances of the new data-approximating formula, different tests are carried out on a 0.25 μm GaAs-PHEMT. In particular, a library-available circuit equivalent model of this device, based on analytical functions describing its nonlinear components [1], is chosen as the "reference device". Then, its pulsed I/V characteristics (obtained through simulation) are sampled on a dense grid of voltages (ΔV_{GS}=50mV, ΔV_{DS}=100mV) and reconstructed both through the proposed approximating formula and a conventional cubic-spline interpolator [7]. In order to emulate the measurement uncertainties typically experienced in real-world I/V curve sampling procedures, a reasonable white Gaussian noise is explicitly added to the sampled data. The pulsed I/V trans-characteristic (at V_{DS} = 6 V) along with its first-, second- and third-order derivatives are plotted in Fig.5.6. The analytic behavior of the model is here compared with the corresponding reconstructions from sampled data. As it can be clearly seen, the proposed approximating formula provides a very accurate and regular prediction of the actual behavior up to the third-order derivative, showing also an excellent smoothing effect on the noisy characteristics. On the contrary,

the cubic-spline interpolator is very sensitive to the noise, exhibiting spurious oscillations already in the first-order derivative.

According to well known literature results [8], this suggests that accurate results can be also expected on IMD prediction capabilities. Intermodulation distortion predictions at 100 MHz based on the pulsed I/V curves (displacement current is negligible at this frequency) are shown in Fig.5.7 (class-A bias, 1 MHz tone displacement, 50 Ohm source and load impedances). As expected, extremely more accurate predictions are obtained by means of the proposed approximating formula even at very low levels of third-order IM products.

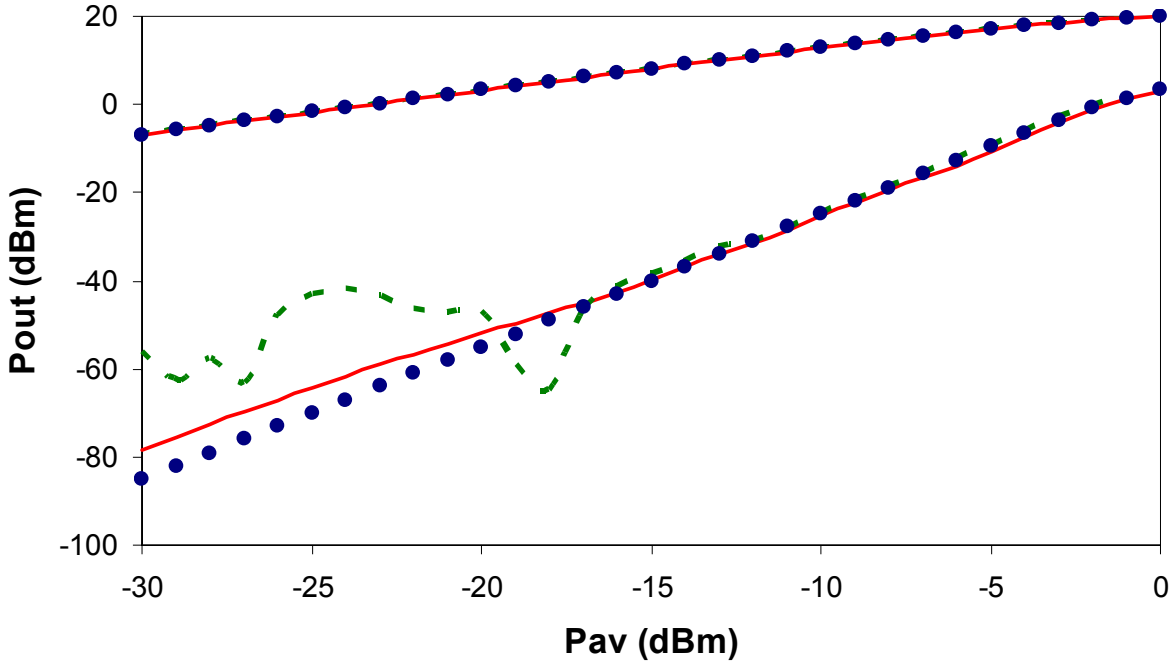

Fig. 5.7 IMD of the 0.25 µm PHEMT at 100 MHz. Analytic model (dots) vs. LUT-based model using different data approximation/interpolation. Proposed formula (solid line) vs. cubic-spline (dashed line).

IMD prediction capability of LUT-based models are eventually evaluated at microwave frequencies. To this aim, two different nonlinear models of the same 0.25 µm GaAs PHEMT are obtained from "on-wafer" measurements. In particular, the well-known EEHEMT1 model [5], [6] and the Equivalent Voltage model [4] are extracted and used for intermodulation distortion analysis at 37 GHz. IMD plots are presented in Fig.5.8 for a class-A power amplifier (10 MHz tone displacement). Similar results are obtained with different values of the bias voltages and input and output impedances.

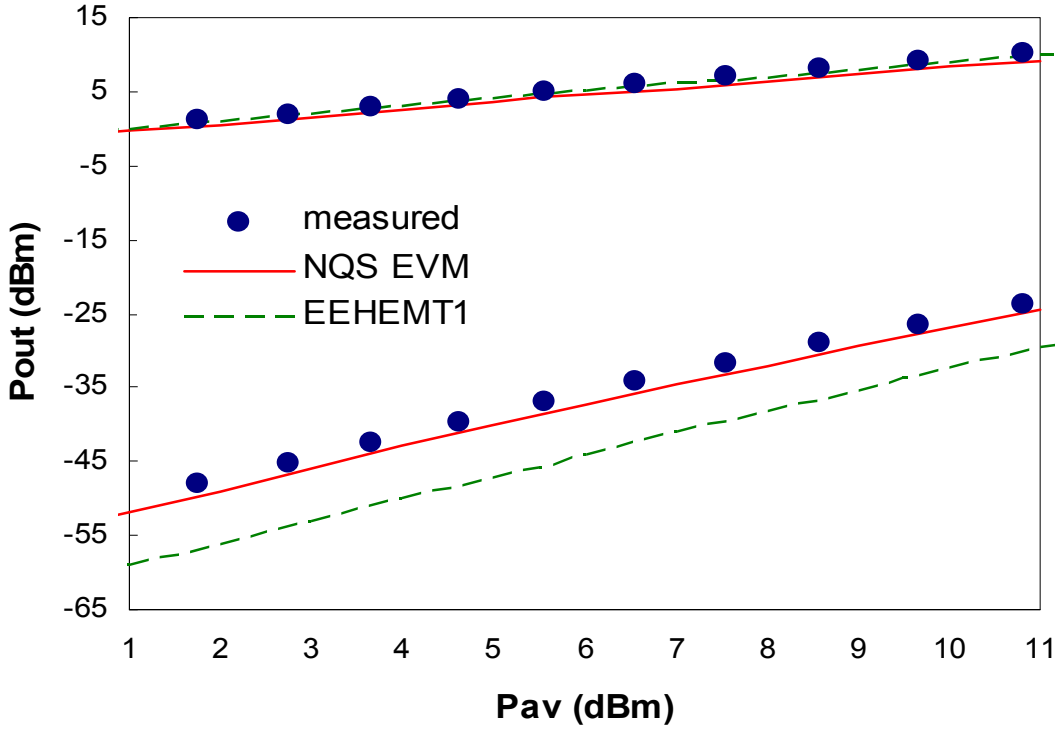

Fig. 5.8 IMD the 0.25 μm PHEMT at 37 GHz. Meas. (circles) vs. LUT-based Equivalent Voltage Model (solid line) and EEHEMT1 (dashed line). Z_S=49.547Ω-j*9.65Ω, Z_L=14.4Ω+j9.7Ω.

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CONCLUSION

In this thesis different contributions in the field of nonlinear modelling of electron devices have been described.

In Chapter 3 and 4, a distributed nonlinear electron device model has been proposed and different identification procedures have been presented and experimentally validated. The described approach enables a scalable nonlinear electron device model to be identified on the basis of EM device layout simulations and conventional DC and AC measurements carried out on a single, "reference device" structure. The capabilities of such an approach are not fully exploited yet, in fact they make the model a flexible tool not only for design purpose but also for new device development and/or optimization of the device layout, since electron device performances can be quite accurately predicted without actually manufacturing a given device structure.

Moreover, the simplicity and closed-form feature of the identification algorithms can be easily extended to account for a larger set of "reference devices" having different peripheries. Definitely, this approach can be exploited to obtain accurate scalable models over a very wide set of devices having remarkable different geometries as it is usually required in advanced, general-purpose foundry processes.

In Chapter 5 it is discussed how table-look-up modelling of microwave electron devices needs data interpolation algorithms with specific requirements. An original data approximating formula is adopted in the framework of a well-known LUT-based nonlinear device model. Accurate intermodulation distortion prediction for highly linear power amplifier design is proven to be strongly dependent on the data interpolation/approximation. The band-limited approximating formula provides more accurate reconstruction of sampled functions and related derivatives than conventional splines. The LUT-based model is shown to provide accurate predictions of the third order intermodulation product even at extremely low levels.

The new approximating formula is only preliminary experimentally validated and many other aspects related to its use remain not exploited yet. In fact in order to properly set the parameters of the approximating formula, the evaluation of the band of the nonlinear characteristic through the sampling theory could be investigated. Another interesting future work could be a further

investigation of the better itermodulation distortion prediction capabilities of LUT-based models with respect to analytical models.

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