Alma Mater Studiorum – Università di Bologna

DOTTORATO DI RICERCA IN

Meccanica e Scienze Avanzate dell'Ingegneria

Ciclo XXXII

Settore Concorsuale: 09/C1
Settore Scientifico Disciplinare: ING-IND/08

Design, production and testing of innovative key components of HEV/BEV powertrains

Presentata da

Dott. Stefano Patassa

Coordinatore Dottorato

Prof. Ing. Marco Carricato

Supervisore

Prof. Ing. Nicolò Cavina

Esame finale anno 2020

Abstract

This PhD thesis reports the activities I've carried out during the 3 years long "Mechanics and advanced engineering sciences" course at the Department of Industrial Engineering of the University of Bologna.
The research project title is "Design, production and testing of key components of HEV/BEV powertrains"
Through modelling activity, experimental campaigns, test bench and on-field validation, a complete powertrain for a BEV has been designed, assembled and used in a motorsport competition.
The activity can be split in three main subjects, representing the three key components of an BEV vehicle.
First of all a model of the entire powertrain has been developed in order to understand how the various design choices will influence the race lap-time. The data obtained was then used to design, build and test a first battery pack. After bench tests and track tests, it was understood that by using all the cell characteristics, without breaking the rules limitations, higher energy and power densities could have been achieved. An updated battery pack was then designed, produced and raced with at Motostudent 2018 resulting in a third place at debut.
The second topic of this PhD was the design of novel inverter topologies. Three inverters have been designed, two of them using Gallium Nitride devices, a promising semiconductor technology that can achieve high switching speeds while maintaining low switching losses. High switching frequency is crucial to reduce the DC-Bus capacitor and then increase the power density of 3 phase inverters. The third inverter uses classic Silicon devices but employs a ZVS (Zero Voltage Switching) topology. Despite the increased complexity of both the hardware and the control software, it can offer reduced switching losses by using conventional and established silicon mosfet technology.
Finally, the mechanical parts of a three phase permanent magnet motor have been designed with the aim to employ it in UniBo Motorsport's 2020 Formula Student car.

Index of contents

Introduction

With the term BEV we indicate a Battery Electric Vehicle. It is a vehicle where all the energy used to power it is stored in an electrical device. Typically it is a conventional cell (Pb, NiMH, Li-Ion) but other forms can be used such as supercapacitors. In that case they are usually combined with conventional cells to gain from the benefits of both.

A typical powertrain is comprised of an energy storage (the battery), an inverter and an electric motor coupled with the vehicle's transmission. More complex setups can use more than one of such devices considering that each motor is supplied by its own inverter.

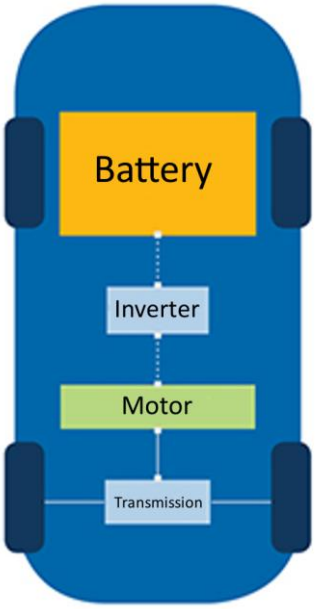


Fig. 1 – BEV Powertrain schematic

The battery obviously is demanded to store and supply the electrical energy used by the system. This is always a DC voltage. The motor can be any type but most of them are PMSM (Permanent Magnet Synchronous Motor) because of the clear advantages in terms of power density and cost. Since those machines requires an AC input power, an inverter is the component required to convert the DC voltage from the battery to an AC current to supply the motor.

The great advantage of the Battery respect to any other energy storage system (except flywheels) is the capability to reverse the power flow. This enables HEVs and BEVs to electrically brake and store back this energy. This process is called regenerative braking and it's a great contributor to the exceptionally high efficiency of these topologies.

However, the main drawback is that the cell technology is still relatively young and the energy density of a battery it's not comparable to conventional chemical energy storage. As an example, the battery designed during this PhD that will be presented later, has an exceptionally high energy density for a battery of its kind: 176Wh/kg for the single cell and 142Wh/kg for the complete assembly. If we consider that a single litre of gasoline stores 14.8 kWh/kg of chemical energy is it clear that there is still a lot of work to do.

In 2017, UniBo Motorsport, the racing team at University of Bologna, decided to participate to the Motostudent Electric, an international competition involving more than 70 universities where the students have to design, build and race their own motorbike. The main research activity within my PhD course was to develop methodologies and techniques to design build and test the three key components of a BEV powertrain, Battery, Inverter and motor to be used in such vehicle.

Since we were starting from scratch, in order to compare ideas, evaluate benefits and costs and choose wisely, the very first activity was to develop a simplified powertrain model and a laptime simulator.

1 Laptime simulator

The laptime simulator was developed to understand and evaluate various setup configuration and ideas in terms of overall performance of the vehicle and to extract laptime sensitivities of the vehicle with respect to global design targets such as overall weight, energy stored, amount of regenerative brake and so on.

It has been split in two parts: a basic vehicle dynamics model and a powertrain model. The first one takes as input the position on the track and calculates the maximum speed sustainable by the vehicle in that point on the track and the load force that the vehicle exhibit as a result of aerodynamic drag and mechanical frictions. The powertrain model takes the maximum speed reachable and applies to the vehicle the maximum torque available to reach such speed. When combined together those two model forms a rudimentary laptime simulator which was proven very useful in the design process of the motorbike and despite being very simple it gives reasonable results when compared with the on track behaviour of the vehicle.

1.1 Vehicle model

In a very first attempt of a vehicle model only the load force was calculated and the speed profile was fixed: it was the speed profile from a SBK telemetry scaled to match our expected maximum speed on the race circuit (Aragon). The circuit slope was extracted from data made available to the teams by the organization.

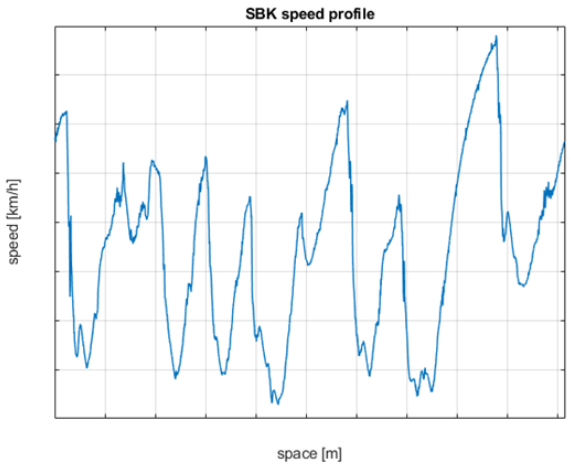


Fig. 2 – SBK speed profile
(scales intentionally omitted for confidentiality)

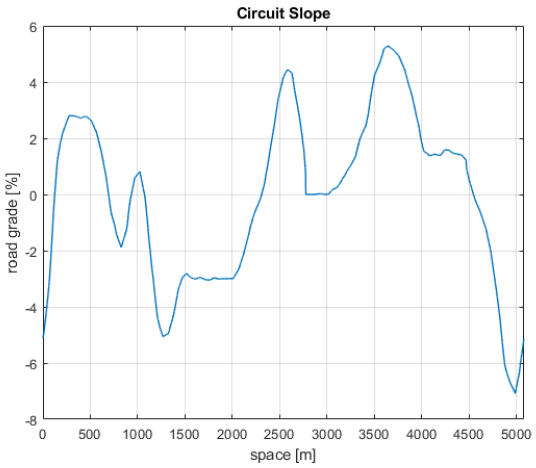


Fig. 3 – Aragon circuit slope

Given the speed and the position on the track, considering the vehicle fundamental parameters, the model calculated the load force by summing the following terms [1]

Aerodynamic drag: ……$F_{aero} = \frac{1}{2}\rho A C_x v^2$

Slope resistance: $F_{grade} = mgsen(\alpha)$

Rolling resistance: $F_{roll} = mgcos(\alpha)c_{rr}$

The initial parameters used to model the vehicle were:

- Vehicle mass: 80 kg
- Battery mass: 40 kg
- Driver mass: 80 kg
- Rolling coefficient: 0.02
- Front section: 0.7 m^2
- Drag coefficient: 0.5

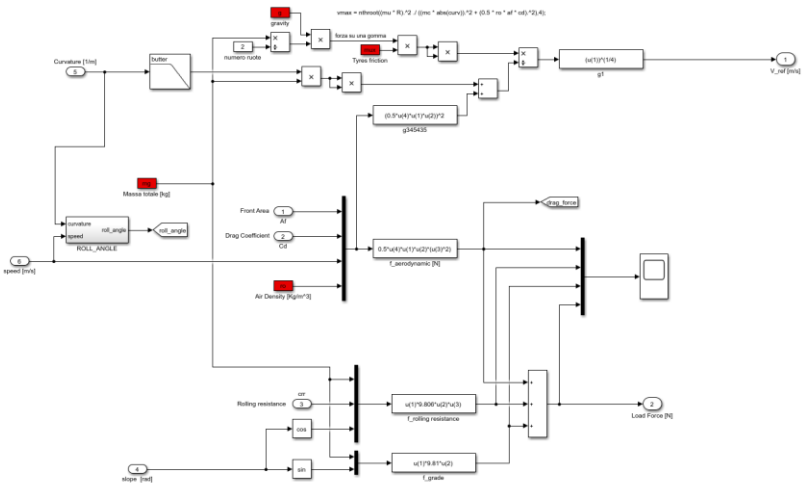


Fig. 4 – Initial vehicle model

In order to develop a laptime simulator that is representative of the vehicle, we must calculate the maximum speed achievable at a given point of the track by using only vehicle geometrical and mechanical parameters instead of a pre-recorded speed profile. This has been done through a matlab script developed by the vehicle dynamics department of the team.

It takes into account the circuit geometry and the vehicle's wheelbase, center of gravity, rolling radius, tyres GG-diagram, gear ratio, aerodynamic pressure point and many other vehicle parameters.

The output is the maximum speed profile achievable by the vehicle on a given circuit (Fig. 5).

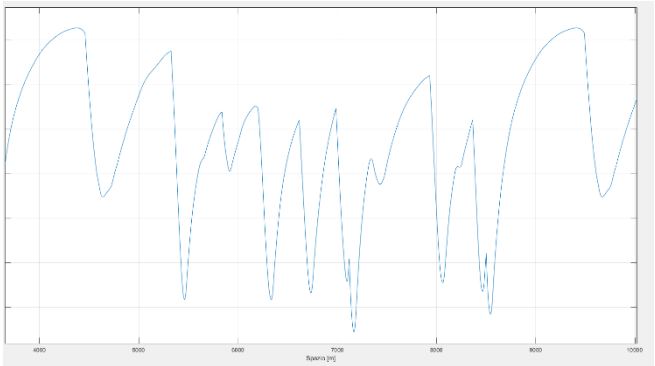


Fig. 5 - Speed profile calculated from detailed vehicle model (scales omitted for confidentiality reasons)

This basic vehicle model was developed together with other works related to this PhD thesis. In particular, it was used to model a HEV vehicle to study the optimal State of Charge control strategies for a given vehicle and a given mission profile [2] [3] [4].

1.2 Powetrain model

The second part of this laptime simulator is the powertrain model. It takes in input the vehicle maximum speed and load force to calculate the maximum available torque applied to the wheel and then the acceleration the vehicle will experience.

This is a simplified model because only the motor and the battery have been modelled, while the inverter has been represented just as a constant scaling the motor efficiency. This is a good approximation because in the operation scenario of the motorbike the inverter efficiency is almost constant.

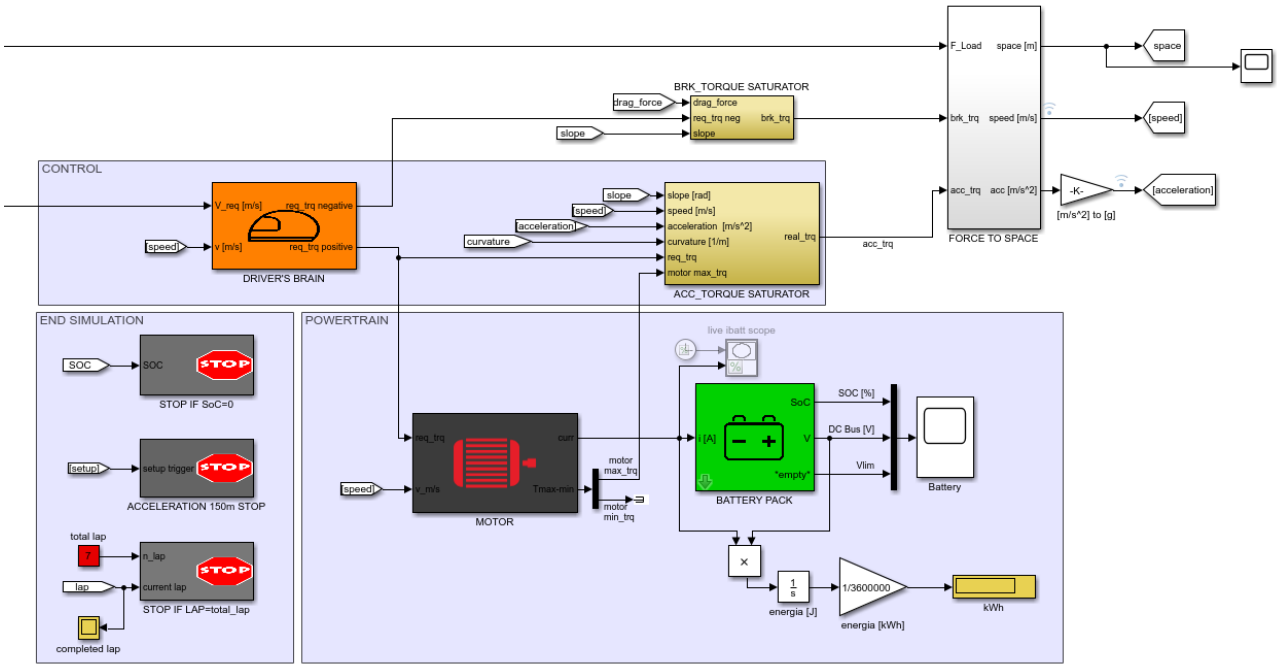


Fig. 6 – Powertrain model

The powertrain model is formed by 3 main blocks: a driver model, a motor model and a battery pack model.

The driver model is a basic PID controller requesting torque in order to follow the speed profile.

The motor model is the one of a classic PMSM [5], configured accordingly to the values of the motor datasheet [6]. Since it is mandatory to use a motor provided by the competition organizers and it has magnets embedded in the rotor, it exhibits also some saliency that is not accounted by the model used. To overcome this limitation the real motor has been characterized at the test bench and the real motor maps have been used.

Finally, the battery model is the combination of a configurable number of cells models connected in series/parallel to represent the hardware configuration of the battery pack. The cell model is a second order lumped elements subcircuit, visible in Fig.7. It is composed of two parts, the block on the left calculates the SoC (State Of Charge) given the current and the capacity of the cell while the block on the right calculates the OCV (Open Circuit Voltage) of the cell through a lookup table extrapolated from the cell datasheet and then applies the voltage drop due to the cell internal resistance and the dynamic behaviour of the cell chemistry modelled with two RC filters, for the short and long transients respectively [7] [8].

Some of the parameters for this model are coming directly from the cell's datasheet while the dynamic parameters have been identified through experimental tests.

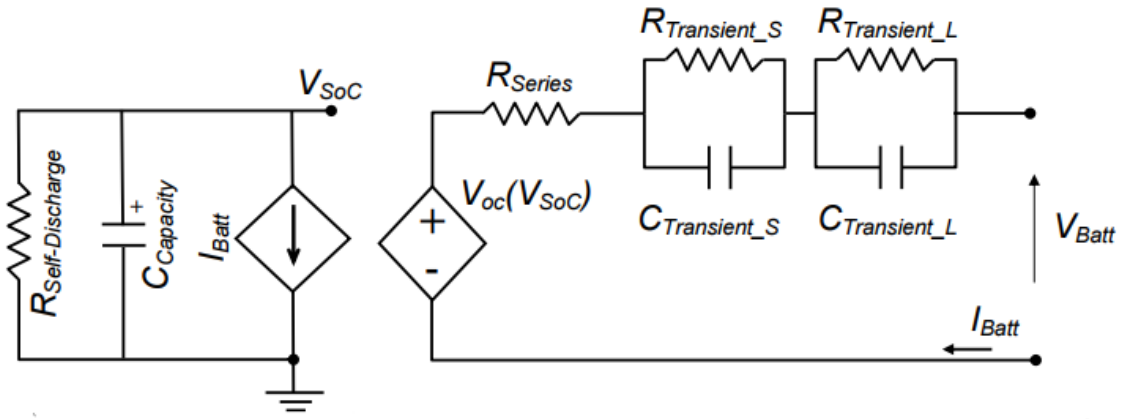


Fig. 7 – Lumped elements cell model

The test setup used to extract such parameters was comprised of an high current active load and a power supply. Through a Compact RIO both the load and the power supply where controlled to charge and discharge the cell under test. The discharge pattern was initially a constant current/constant discharge to evaluate the effect of the heat on the available energy. Since those cells were very high quality components, the loss in the available energy at high C rates was negligible and then in this model was deemed sufficient to have a constant $C_{capacity}$. Then another test campaign was performed with a series of "steps" of current. This allows to extract the time constant required to model the dynamic part.

Is it clear from the following figure that this approach successfully modelled the cell with a very low error using a very simple model, visible in Fig.8, to keep the simulation time low.

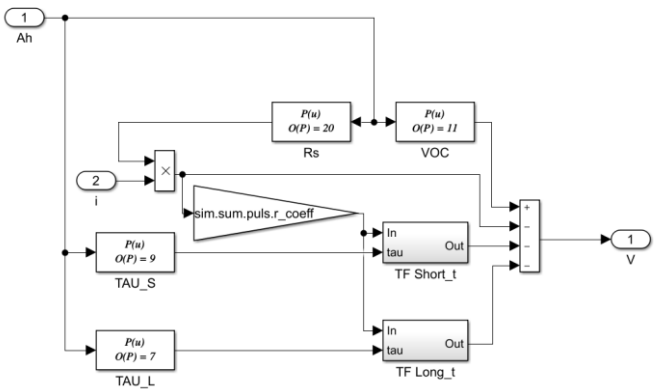


Fig. 8 – Simplified cell model in Simulink

This model starts calculating the OCV for the given cell. From this voltage all the losses are subtracted: an Rs term which models the internal resistance of the cell and two terms called TFShort and TFLong that models the fast and slow transient response respectively. The polynomial terms of this model are extracted from experimental data through a Matlab script.

Such model has been used also in other activities related to this PhD such as the optimization of energy and battery thermal management for HEV vehicles [9].

The comparison between model output and the experiments is reported in Fig.9.

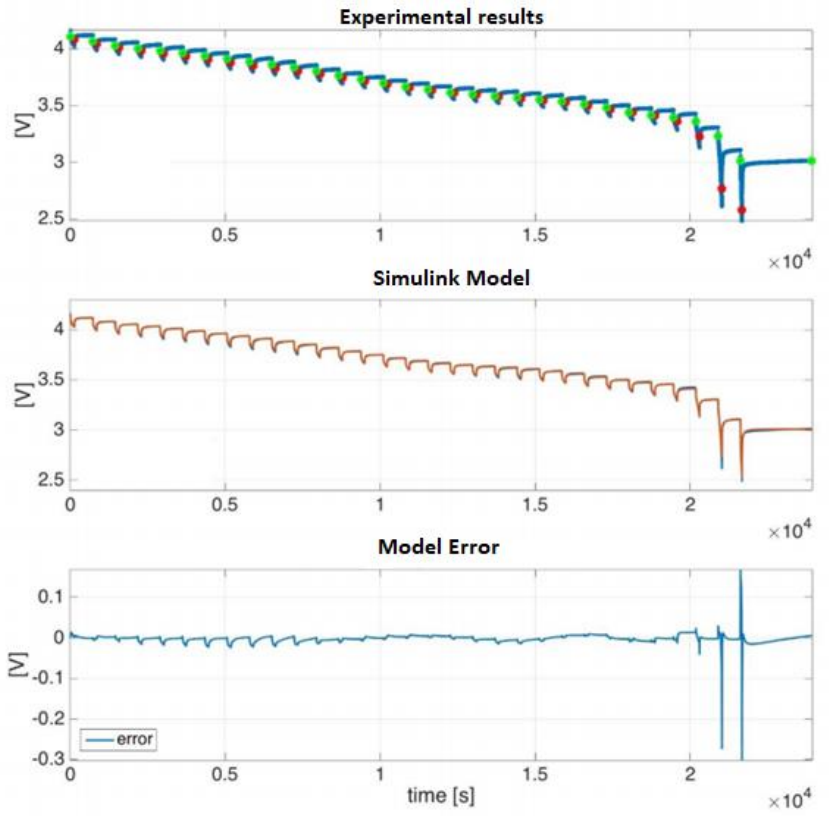


Fig. 9 – Cell model: Experimental results and model error

This laptime simulator has been used to estimate sensitivities of key design requirements of the motorbike to understand what is the best design compromise and where the points in the design that offer the best benefit in terms of performance.

In the following table are represented the results of different simulations changing one parameter at the time. The column “Laptime” represents the best lap time achievable by the vehicle in ideal conditions, while the column “Race time” is the time needed to complete all the 5 laps of the race and it takes into account the progressive degradation of laptime because of SoC decrease and motor and inverter temperature increase and subsequent derating.

Chassis weight [kg]	**Laptime [s]**	**Energy [kWh]**	**Speed [km/h]**	**Race time [s]**
80	153.039	5.843	177.9	845.43
81	153.099	5.844	177.8	845.45

Max Motor Current [PU]	**Laptime [s]**	**Energy [kWh]**	**Speed [km/h]**	**Race time [s]**
2.33	153.039	5.843	177.9	845.43
2.4	151.563	5.82	179.9	812.47

As expected a reduced weight of the chassis produces benefits in all areas, and then one design goal is to have the chassis as light as possible. Also an increase in the maximum motor current (exaggerated in this example) produces great performance increase even in the energy consumption. This is counter intuitive and without such tool it would have been missed. The explanation for this

behaviour is that the powertrain of the motorbike works, in the given circuit, for more time in a better area of the efficiency map.

Such considerations have been used also for the design of an improved battery pack. Due to the regulation that limit the maximum voltage to 110V, it was possible to prove that a 26S2P battery pack is able to store more energy with less weight than the original pack that had a 27S2P configuration. The details will be presented in the following sections.

2 Battery pack

2.1 Introduction

The battery pack was the first element designed for the motorbike because it is strictly connected to the geometrical size of the chassis and its position also affects the chassis performance. It has to comply with a number of requirements coming from both the competition rules and the chassis encumbrances and positioning.

The first step was a literature review of the state of the art cell technology in order to select the best cell technology to fulfil the needs. After the appropriate cell was selected a cell characterization was completed to model its behaviour both electrically and thermally. The latter was necessary to successfully design a cooling system for the battery pack. Then the mechanical assembly of the pack has been designed, taking care of some design challenges such as the cell welding due to the particular tab material of the selected cells and the design of the busbars to carry such amount of current with minimal space and weight. Finally a BMS (Battery Management System) which is a mandatory element to ensure the safety of any lithium based battery pack has been designed, and through a couple of design iteration a solution that avoids time consuming assembly has been developed.

Extensive tests have been carried out on this battery pack mostly to ensure that the cooling was sufficient to keep the cells in a safe condition throughout all the race.

The results of these tests, combined with the indications from the laptime simulator led to the design of a second battery pack that exploits a rules requirement to have a lighter battery pack but capable to store more energy despite having two cells less than the original.

2.2 Requirements

The requirements for this battery pack are coming both from the competition rules and from the vehicle department since it is the element of the motorbike that consumes the largest volume and then dictates the chassis geometry.

Regarding the rules, the main requirement is the following:

D.1.1.1: "The maximum permitted voltage of the HV system shall be 110VDC (fully charged)

This fixes the number of cells in series. Obliviously we want the highest possible voltage to reduce the current and use lighter conductors. Since most of the Li-Ion chemistries have around 4.2V @ 100%SoC we can estimate the number of cells in series to be around 26 or 27.

The other rules-related requirement comes from the motor, since in this competition it is given by the organizers and it is the same for all the competitors. From the datasheet it has 42kW peak power, so we have estimated the inverter to have 95% efficiency. That means the power output from the battery pack must be 50kW. Considering the cut-off voltage of the cells to be 2.5V, in the worst case scenario where we want full power at 0% SoC we can calculate the maximum current output from the pack:

$$Ipackmax = \frac{Pmax}{Vcutoff * Cells} = \frac{50kW}{2.5V * 26} = 769A$$

This result will be used as the target output current when selecting the cells and will impose the necessary number of cells in parallel needed to meet it. The requirements from the vehicle side are quite simple: the battery pack must be as light as possible, for obvious reasons in laptime and handling performances of the motorbike itself. It is also beneficial to have it as narrow as possible: this yelds to a narrow chassis and consequently a reduced aerodynamic drag and a comfortable riding position.

Finally, from the laptime simulator, using first tentative values for both the vehicle and powertrain models, we've understood that the amount of energy needed to complete all the race laps at full power is about 6kWh. This is the reference value used to select the required capacity for the cells, knowing that if it is underestimated we will be covered by derating due to motor overtemperature because it is air cooled and the datasheet clearly specify that the 42kW max power is not continuous.

2.3 Cells

At the current state of the art, the best cells for an EV in terms of energy density are the Lithium-based cells [10] [11] [12].In this field there are a number of chemistries, each one slightly different and incline to emphasize different desirable properties of the cell.

Those cells are available in a number of different packages but they can be basically classified in two macro categories: cylindrical or pouch cells. The main advantage of cylindrical cells is reduced cost due to a consolidated production process. The drawback is that there is an intrinsic energy density loss due to sub-optimal volume utilization in the assembly, Fig. 10. However this space is often used for cooling purposes, mitigating this issue.

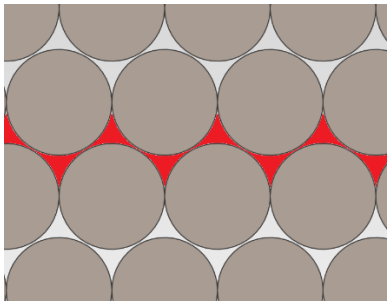


Fig. 10 – Section of a cylindrical cells optimal disposition
In red is highlighted the wasted volume

The pouch cells have a rectangular section and they do not suffer from this issue, resulting in optimal energy density. For this reason we have selected this kind of cells for our prototype.

One key parameter evaluated to discriminate the ability of a cell to deliver a certain amount of current is the C- Rate.

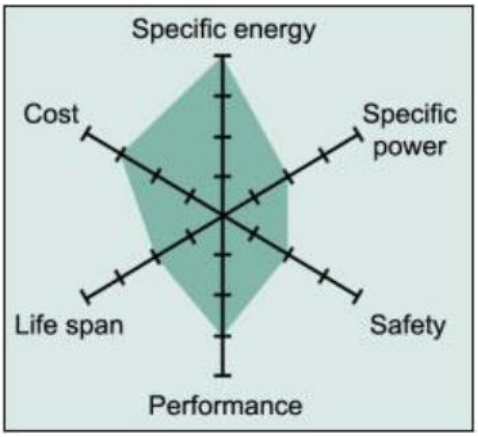
C-Rate is defined as the discharge current over the cell capacity: $C = \frac{I_{Cell}\,[A]}{E_{cell}\,[Ah]}$.

This figure gives an immediate idea of how deep a cell is charged or discharged and how long it will sustain such current demand. For example, a 2Ah cell with a maximum allowable C-Rate of 2 will deliver maximum 4A for 0.5 hours.

The most common chemistries available for pouch cells are the following [11] [13]

- **Lithium Cobal Oxide ($LiCoO_2$)**

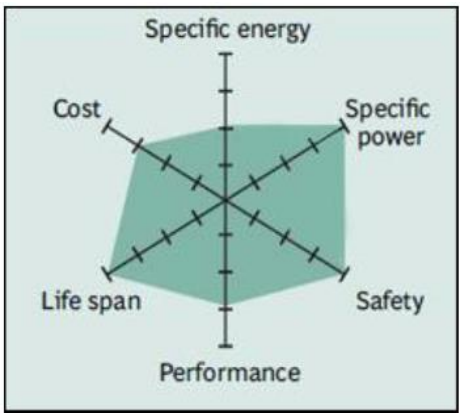
Those cells use $LiCoO_2$ as active material for the cathode. They do no tolerate C-rate greater than 1 and doing so produces excess heat. Those cells are considered to be "Energy-Intensive" cells. For this reason they are not suitable to be used in our battery pack.



Voltage	3.60V nominal, operating range: 3.0-4.2V/cell
Capacity	150-200Wh/kg
Charge	0.7-1C, charges to 4.2V. Fast charge shortens battery life
Discharge	1C, 2.5V cut-off. Discharge current above 1C shortens battery life.
Cycle life	500-1000, related to depth of discharge, load, temperature
Thermal runaway	150°C. Full charge promotes thermal runaway.

- **Lithium Iron Phosphate ($LiFePO_4$)**

Iron-Phosphate cells are "Power-Intensive" cells. They are very safe and tolerate very high C-rates. Despite this desirable property, it has a low energy density and thus it is not suitable for our purposes.



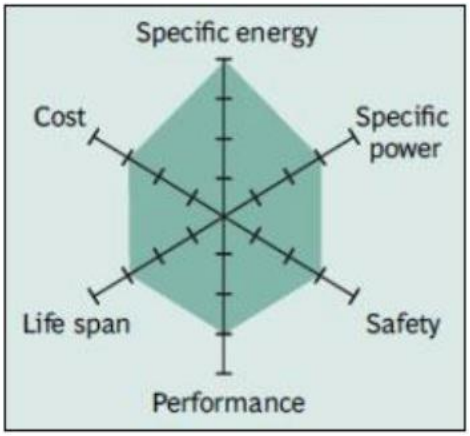
Voltage	3.30V nominal, operating range: 2.5-3.65V/cell
Capacity	90-120Wh/kg
Charge	0.7-1C, charges to 3.65V.
Discharge	1C, 25C on some cells 2.5V cut-off (lower than 2V causes damage)
Cycle life	1000-2000, related to depth of discharge, load, temperature
Thermal runaway	270°C. Very safe battery even if fully charged

- **Lithium Titanate ($Li_4Ti_5O_{12}$)**

Those cells are reported just for reference. They are long-life cells, capable to withstand many charge cycles. They are very expensive and they have a very low specific energy, which is not ideal for us.

- **Lithium Nickel Manganese Cobalt Oxide ($LiNiMnCoO_2$ or NMC)**

Those cells have excellent balance among all the desirable parameters. With recent technological achievements C-Rates of those cells are becoming very interesting. It is a chemistry already available in a number of packages and it is relatively safe. Those are the reasons why we've chosen this kind of chemistry for our pack.



Voltage	3.6-3.7V nominal, operating range: 2.7-4.2V/cell
Capacity	150-220Wh/kg
Charge	0.7-1C typical, charges to 4.2V
Discharge	1C, 5C possible on some cells. 2.5V cut-off
Cycle life	1000-2000, related to depth of discharge and temperature.
Thermal runaway	210°C typical. High charge promotes thermal runaway

2.3.1 Cell selection

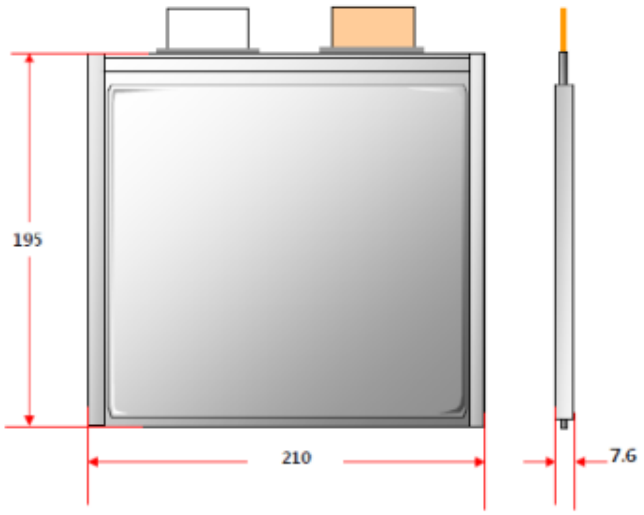
As discussed earlier, we've chosen the NMC chemistry. From an extensive search on cell manufacturer's catalogues we have selected 5 cells that were believed to be the ideal cells in terms of mechanical size and electrical properties. A preliminary dimensioning of the final pack configuration has been done using an excel spreadsheet, represented in a simplified version in the following table.

Cells part numbers have been intentionally omitted for confidentiality reasons.

Property		*NMC #1*	*NMC #2*	*NMC #3*	*NMC #4*	*NMC #5*
Continuous Discharge Rate (C)		1	2	1	1	2
Peak Discharge Rate (C)		8	4	6	18	10
Capacity [mAh]		21000	27000	30500	20000	31000
Weight [g]		398	384	682	496	690
Resistance [mΩ]		1,5	1,6	1,7	2	2,3
Dimensions (mm)	**L**	189	272	210	227	225
	W	90	95	195	160	225
	T	10,4	7,8	7,6	7,25	7,2
Number of series		27	27	27	27	27
Number of parallel		3	3	2	3	2
Total number of cells		81	81	54	81	54
Cell maximum voltage		4,2	4,2	4,2	4	4,2
Cell nominal voltage [V]		3,7	3,7	3,65	3,3	3,7
Cell minimum voltage [V]		3,2	2,7	2,7	2,6	2,7
Battery pack max voltage [V]		113,4	113,4	113,4	108	113,4
Battery pack nom. voltage [V]		99,9	99,9	98,55	89,1	99,9
Battery pack min voltage [V]		86,4	72,9	72,9	70,2	72,9
Cell peak current [A]		168	108	213,5	360	310
Battery pack peak current [A]		504	324	427	1080	620
Max power [kW]		57,2	36,7	48,4	116,6	70,3
Min power [kW]		43,5	23,6	31,1	75,8	45,2
Total Weight [kg]		32,2	31,1	33,0	40,2	37,3
Total volume [L]		14,3	16,3	16,8	21,3	19,7
Total Capacity [kWh]		6,3	8,1	6,0	5,3	6,2
Specific power [W/kg]		1561,81	1040,63	1273,33	2395,16	1662,32
Power density [W/L]		3513,77	1982,61	2503,94	4511,62	3146,78
Specific energy [Wh/kg]		195,23	260,16	181,9	133,06	166,23
Energy density [Wh/L]		439,22	495,65	357,71	250,65	314,68
Battery pack resistance [mΩ]		13,5	14,4	20,25	18	31,05
Max dissipated power [kW]		0,72	1,08	1,52	1,46	2,34

From this spreadsheet it looks like the cell NMC#1 should be the best option for our purposes and in fact it is one of the most common cells used in such competitions. However, the manufacturer is believed to be non-reliable because there is a record of some thermal runaway events leading to explosion of the battery pack and consequent fire. At that time we had no way to obtain samples of those cells and perform tests so only the datasheet values have been considered. This led us to choose cell NMC#3 which comes from a reliable and well known manufacturer and we had evidence from 3rd party that the values reported on the datasheet are representative of the real cell behaviour.

In Fig. 11 is visible a portion of the datasheet of NMC#3.



Item	APP042A01
Energy Density	365 Wh/L
Nominal Capacity	30.5 Ah
Nominal Voltage	3.65 V
Nominal Energy	111 Wh
Cycle Life (2C/2C)	>1500 cyc

Fig. 11 – NMC#3 Cell dimensions and key performances

2.3.2 Cell characterization

The immediate step after cell selection was the electrical and thermal characterization of the selected cell in order to verify if the considerations and approximations made during the cell selection process still hold true in the real scenario.

The cell has been mounted on a custom-made polystyrene stand, making sure the cell has minimal contact with it and then assume all the cooling during the test is due to natural convection in still air. The cell was then connected to a high current active load to simulate the discharge cycle and to a programmable power supply to simulate the charge cycle. Voltages, current and temperatures were recorded with a custom made data logger designed in Labview and running on a National Instruments Compact RIO [14]

The test was composed of multiple charge and discharge patterns at various C-rates, up to 7C where we hit the cutoff temperature and was not deemed safe to proceed with the test at higher rates.

Temperature was recorded through 3 thermocouples, one at the center of the cell and one on each tab. Also, a thermal camera was recording the scene to make sure we had no hotspots.

The voltage vs charge charts, both for discharge and recharge (Fig. 12) where used to develop the model presented in section 1.2 while the temperature logs (Fig. 13 where used to develop a LUT-based (or experimentally derived) model of the cooling system that will be used later to design the mechanical structure of the battery pack.

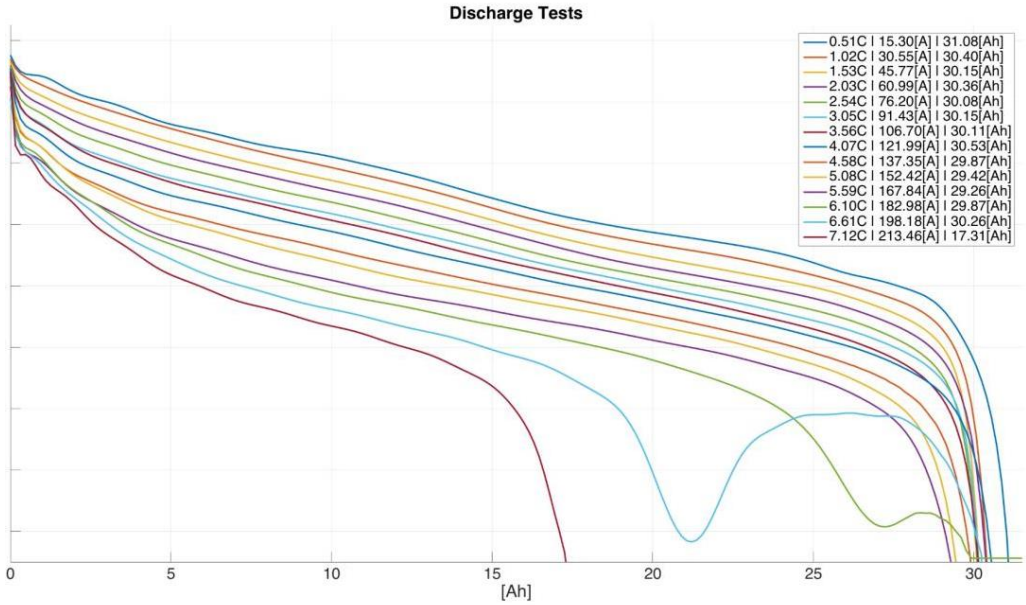


Fig. 12 – Cell Discharge test results (scales omitted for confidentiality reasons)

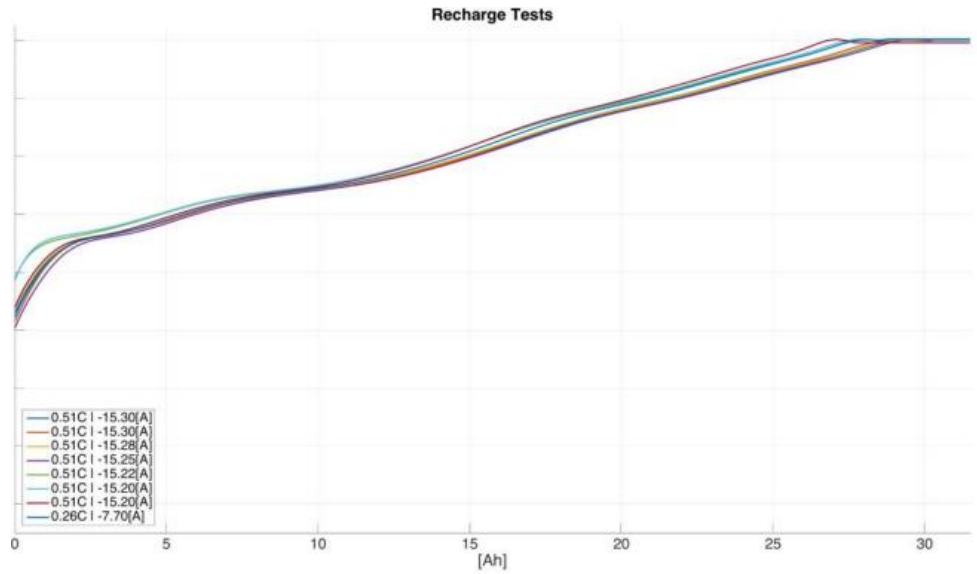


Fig. 13 – Cell Charge test results (scales omitted for confidentiality reasons)

From these tests we can understand that the cell quality is very good because the delivered charge is almost constant regardless of the applied C-rate. We've also understood that at high C-rates the cell exhibits an unusual behaviour, with the voltage rising back without hitting the cutoff voltage. This was discussed with the cell manufacturer and was attributed to an excessive increase in the cell temperature leading to an increased internal resistance. Obliviously this is not a safe operating condition and has been considered during the development of the BMS software in order to limit the torque request if this condition should happen in the real usage.

2.3.3 Cell thermal model

The cell thermal behaviour was modelled in two ways. An initial approximation was to extract from the discharge tests a lookup table representing the temperature derivative over time of the cell for a given C-Rate. This was a starting point for the design of the cooling system, but some error was expected because of the environmental conditions of the test setup: the cell was entirely placed in free air and then the extracted data was already taking into account some degree of cooling that is substantially different from the conditions inside the full battery pack.

In Fig. 14 the model used for this first attempt is represented, together with the experimental curve used to model the temperature increase.

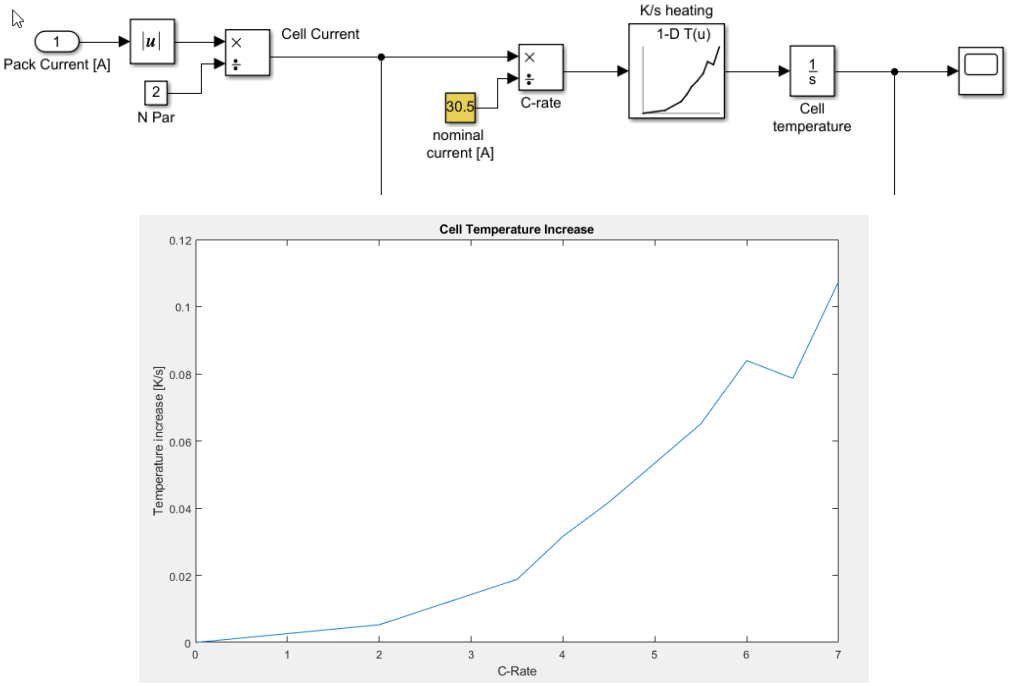


Fig. 14 – First tentative cell thermal model based on experimental data

Another attempt was to model the cell thermal behaviour analytically. For this approach to work, the exact specific heat capacity of the cell must be known. Since this data is not available, it was assumed as the weighted average of the material composing the cell, excluding the electrolyte and the plastic elements which represent a negligible fraction of the cell mass.

Material	***Specific Heat Capacity [J/kg*K]***	***Expected fraction of cell mass***	***Subtotal***
Lithium	3582	10%	358,2
Copper	897	45%	403,6
Aluminium	385	45%	173,2
Total		**100%**	**935,1**

The resulting model is represented in Fig. 15

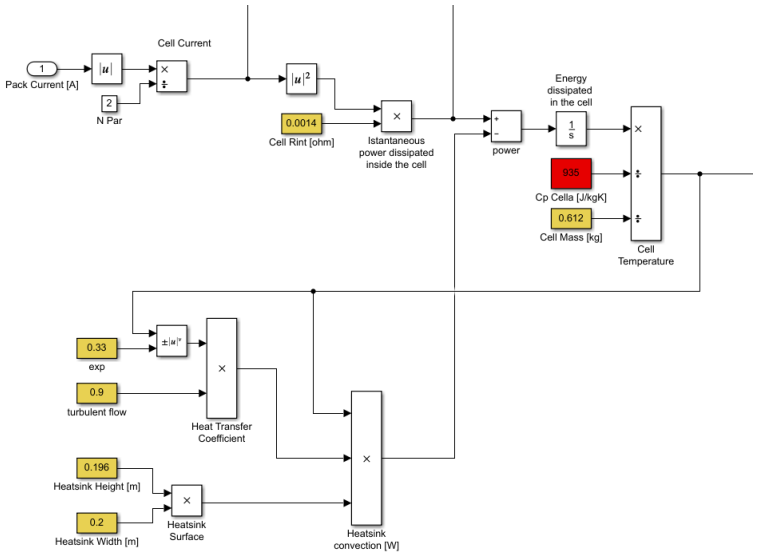


Fig. 15 – Analytical model of the cell thermal behaviour

In this model, the power generated by Joule effect inside the cell is calculated. Then the power dissipated by the cell in the surrounding ambient (modelled as convection) is subtracted from it and the resulting cell temperature is calculated. This gives us the advantage to simulate any kind of cell cooling without the non idealities of the experimental approach to interfere with the outcome of the simulation.

In the following figure, a comparison between the experimental model and the analytical model is reported.

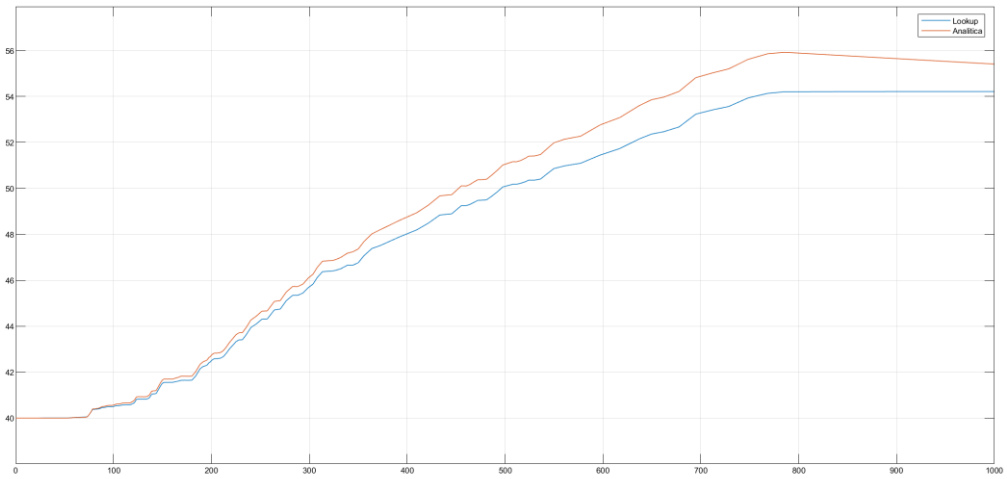


Fig. 16 – Comparison between analytical and experimental cell thermal model –

For the experimental model the cooling of the cell is “enclosed” in the data extracted from the discharge test while in the analytical approach we tried to model the same cooling effect we had in the experimental setup. The error of these two approaches is less than 2°C.

2.4 Battery pack design

Initially, based on energy (laptime simulator) and power (max motor power) requirements, the best pack configuration was estimated to be 27S2P. That means two paralleled strings of 27 cells each, for a total of 54 cells. A first prototypal pack has been produced but after the cell test results were available it was understood that a 26S2P configuration, for this specific application, would provide more energy and less weight. This is because the rules [15] state that the absolute maximum voltage should be 110V, or in other terms, each cell of the 27S pack should be charged to 4.074V instead of the 4.2V admissible by the cell fully charged. Since the OCV curve is steep in the high SoC area (as visible in Fig. 11 in the region below 1Ah), this 128mV voltage difference means each cell of the 27S pack must be charged maximum to the 92% of its capacity to stay within the rules. The 26S pack does not suffer this issue because the 100% SoC OCV is less than 110V:

$$V_{max,27S2P} = 27 * 4.2 = 113.4\,V$$
$$V_{max,26S2P} = 26 * 4.2 = 109.2\,V$$

The advantage in terms of stored energy may be not clear until we calculate the equivalent capacity for a rules-compliant battery pack:

$$Energy_{27S2P} = 27 * 3.65 * 30.5 * 2 * 0.92 = 5530.6\,Wh$$
$$Energy_{26S2P} = 26 * 3.65 * 30.5 * 2 * 1.0 = 5741.5\,Wh$$

With this simple consideration we can obtain a pack that is lighter because it uses less cells and yet stores more energy. Since the OCV curve is non linear, a simulation was carried out using the laptime simulator to obtain more confidence in such solution.

In Fig. 17 a comparison between those two solutions is shown. The plot represents the energy used from the battery pack over time. We can see two interesting things:

- The slope of the two curves is slightly different. The 27S2P pack is worse in terms of efficiency. This is because the motorbike is 1.2kg heavier having the pack two cells added.
- The 26S2P pack runs longer because it effectively stores more energy.

Thanks to those considerations, a second pack with the 26S2P configuration has been produced and used in the competition. This is the pack that will be presented in the following sections since it shares most of the elements with the first one.

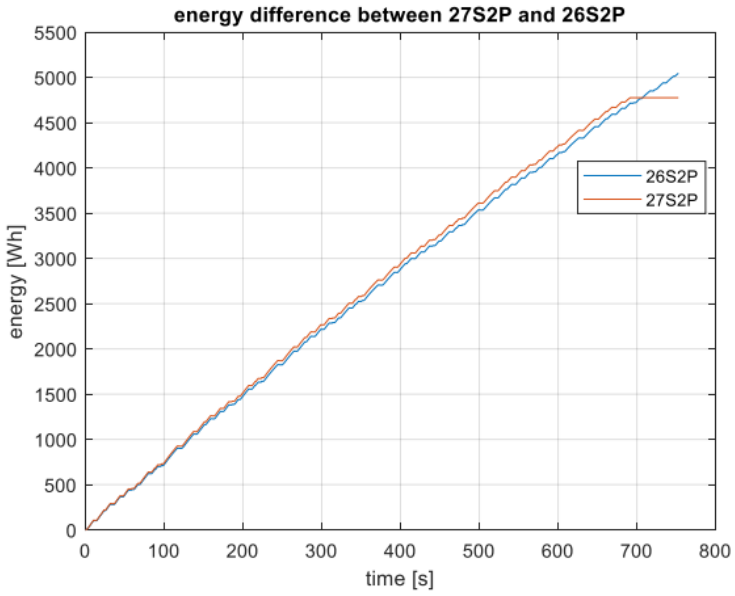


Fig. 17 – Energy delivered profiles of the two different battery pack

2.4.1 Electrical structure

Motostudent rules state that inside the battery pack there must be present:

- At least one line contactor, placed on the positive side of the battery pack
- At least one line fuse
- An IMD (Insulation Monitoring Device), provided by the organization
- A BMS (Battery Management System), monitoring all voltages and at least 4 temperatures
- A precharge circuit

Line contactor and fuse are bulky devices because they must carry all the current from the battery. For such reason they were mounted on the side walls of the pack and connected through heavy copper busbars, that also help cooling them.

The IMD is the industry standard Bender IR1555 and it monitors the insulation resistance from the battery terminals to the chassis. It commands the line contactor to open the circuit in the event an insulation loss is detected. This is a mandatory safety device to make sure no live voltage is present on the outside of the pack in case any component of the powertrain should suffer a loss of insulation.

The BMS is a custom made circuit board that monitors all the voltage of the cells, the temperature of each cell interconnection, the current flowing in the pack and performs all the preliminary check and actions to declare the pack safe to use and then close the contactor. It will be discussed in the appropriate section.

The precharge circuit is required to slowly charge the DC-Link capacitors before closing the main contactor. This is mandatory to avoid the extremely high inrush current we would have by closing the main contactor with the DC-Link capacitors discharged. This high current is by orders of magnitude above the main contactor rating and will result in contactor welding, the most severe event from a safety point of view.

All those elements must be connected in a specific way, Fig 18, to guarantee that all the safety aspects required by the rules are satisfied. In particular, the line contactor must be open in case any of the following event occurs:

- LVMS opened (Low Voltage Master Switch, operated by the rider)
- TSMS opened (Tractive Switch Master Switch, operated by the rider)
- EMCY operated (Emergency switch on the motorbike tail, accessible by the track marshals)
- BMS detects any event among overvoltage, undervoltage, overtemperature.
- IMD detects an insulation fault.

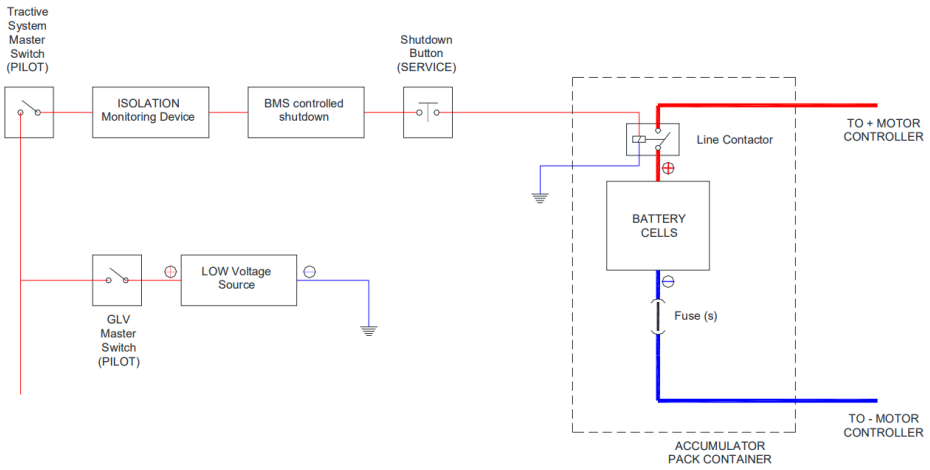


Fig. 18 – Prescribed interconnections of the mandatory elements of the tractive system circuit

2.4.4 Cell tab welding

From the rules of the competition [15] we can read:

D.3.3.6 It is not allowed the direct connection between cell terminals by means of welding or soldering. Indirect welding or soldering is permitted through a conductive material

This implies it is not possible to directly weld together two cell tabs but an interface material is needed. The selected cells have a copper tab for the negative terminal and an aluminium tab for the positive terminal. The interface material must be some low resistance material to minimize losses and self heating. If we consider the cost of better materials, this restricts the choice to copper or aluminium. Copper has been selected because it offers the best electrical conductivity per volume. It is not ideal if we consider the weight and this is being addressed in the 2020 battery pack that is currently in production: by using thicker aluminium bars it is possible to obtain same electrical resistance as copper with a reduced weight but in a space constrained situation as this was not possible at that time to free enough space to fit aluminium busbars.

There is then the need to weld aluminium foils to copper bars that is reliable, repeatable and fast. If we consider that the cell tab should be kept at low temperatures to avoid heating the cell during the welding process, the only method available is the laser welding [16].

The copper busbar is a thick copper bar of 1.5mm while the cell tabs are 0.4mm thick. This implies that the laser must melt the tab first and then penetrate in the copper bar to realize the join. It is extremely important for a good yield that the two materials are perfectly planar and well pressed together. For this reason a welding mask has been designed, visible in Fig. 19. Through 4 screws it is possible to compress the busbar and the tabs between the welding mask and two fiberglass blocks that will be removed after the welding. Fiberglass is necessary to avoid short circuit between two adjacent cell tabs.

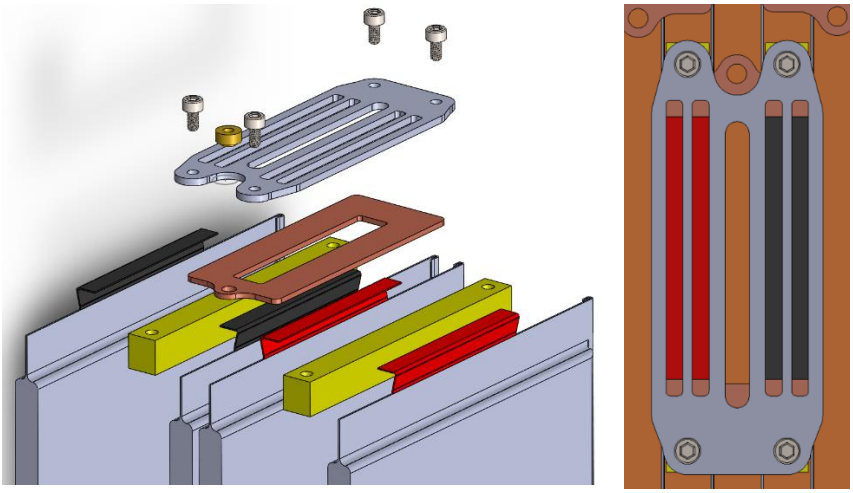


Fig. 19 – Exploded and top view of the welding mask assembly

The initial step was to perform welding trials to identify the best laser parameters that yield good mechanical strength of the joint and, even more important, a minimal electrical resistance.

The first question to answer was how many adjacent welding cords to perform: 1, 2 and 3 cords were tested. From a mechanical point of view, the more the cords the better is the mechanical resistance to traction with low benefit to the peeling resistance. The peeling stress in our assembly is predominant and the mechanical trials were already successful with a single cord. So the choice of how many cords was then a matter of electrical resistance. Three test samples were welded with,

respectively, 1, 2 and 3 cords. A current of 200A was then applied to the black painted samples and temperature recorded through a thermal camera.

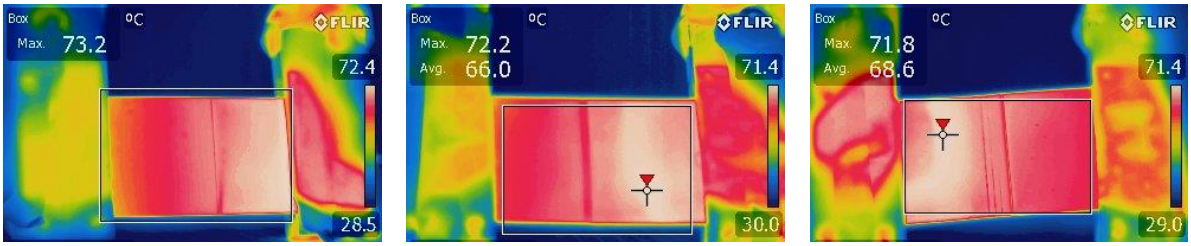


Fig. 20 – Thermal images of the welded cell tabs. From left to right, 1, 2 and 3 welding cords

As visible from Fig.20 there is no substantial difference between those 3 welding methods, leaving an open question on how many welding cords to perform. The welding resistance was then measured using a precision impedance meter (Hioki BT-3554, 1 uΩ sensitivity).

Experimental data evidenced that there is an improvement between 1 and 2 cords, while the improvement between 2 and 3 cords is not so evident. This is well explained in [3] and an extract is reported in Fig. 21.

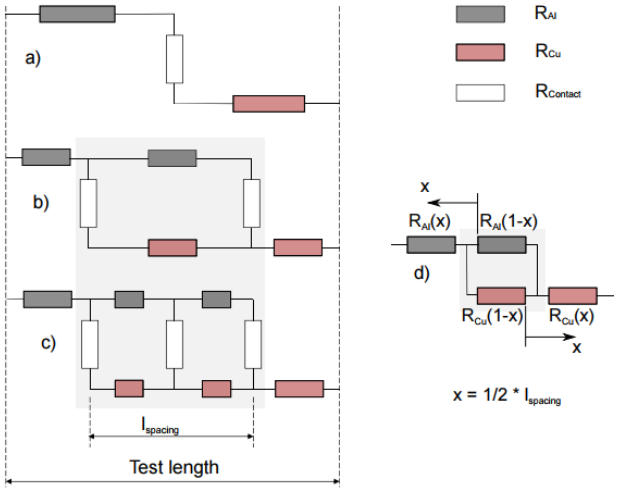


Fig. 21 – Welded tabs equivalent circuit

From this we can conclude that the resistance decrease due to an added cord is not justified by the increased space occupied by the welding. Considering also the increased welding time, the solution with two welding cords was chosen. In Fig. 22 is visible a welding test sample using two cords per tab

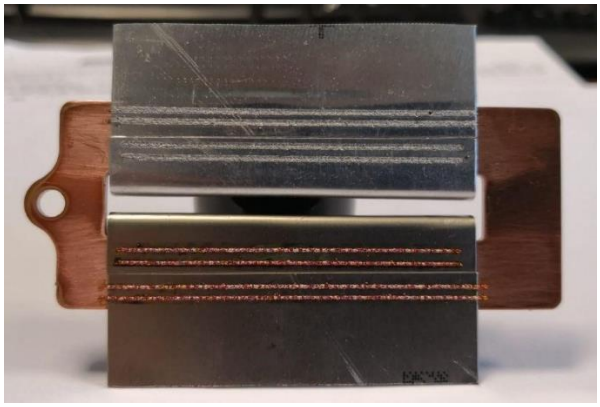


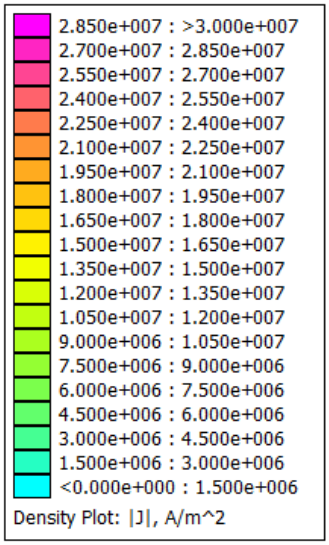
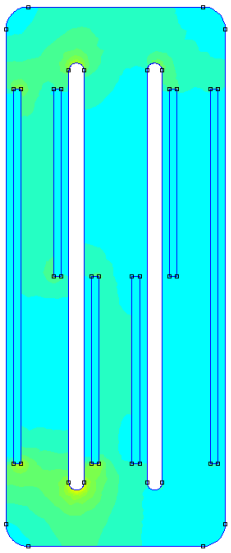
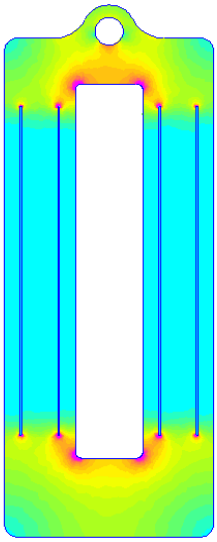
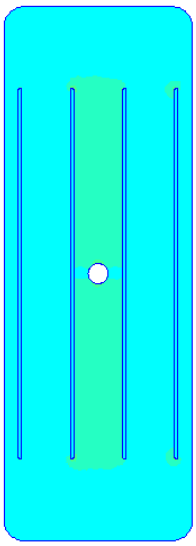
Fig. 22 – Busbar and cell tabs laser welded with two cords per tab

2.4.3 Busbar design

Since the rules forbid to directly weld together two cell tabs we had to design a busbar so that the cells are indirectly connected. The cell tabs of four cells (because of the 2P configuration of the pack) have to be welded together on a single conducting element. This element is the busbar and was subject to an extensive study in order to minimize the mass and the power loss due to Joule effect. It is particularly important that the busbars do not suffer of self heating because the cell tabs have a good thermal resistance to the internals of the cell and then if the busbar is colder than the cell's internals it effectively helps the cooling of the cell itself.

During the development of this component several designs have been simulated using FEMM. This is a free 2.5D FEM solver for electromagnetics problems. It was possible to simulate the current flow in the busbar as well as the power loss over the entire material.

In the following table, an extract of such simulations and design iterations is summarized. The plots show the current density in the busbar material.

	Busbar 2018 V1	***Busbar 2018 V2***	***Busbar 2020***
			
Material	Copper	Copper	Aluminium
Thickness	1.5mm	1.5mm	3mm
Power loss	97mW	89mW	110mW
Weight	25g	23g	17g

The very first design used the central cells tabs as an additional path for the current to flow from one side to the other of the busbar. This design was rapidly abandoned because of the increased complexity in the preparation, folding and welding of the cell tabs.

Since the current flow in the center of the V1 busbar was minimal it was decided to eliminate this material and use it on the top and bottom sides, where the current density was higher. This led to the V2 design, where both the power loss and the weight were reduced.

For the 2020 a new concept of busbar has been developed where the tabs are not anymore folded but they remain straight and slide into slots on the busbar. In this way we obtain an extremely simple production process avoiding folding the tabs and also avoiding the welding fixture: the busbar itself becomes the welding mask and there is no need anymore for accurate alignment of the tabs.

In this design the only mechanical stress on the welding joint will be traction, since the tab is not folded we do not have anymore peeling stress. This increases the long-term reliability of the battery pack when the tabs will be exposed to multiple thermal cycles due to Joule effect on the tab itself.

This design also offers another major benefit: the bottom material on the welding section is not required anymore to be the one with the higher melting point. That means we can use aluminium with a clear benefit on the parts weight if we impose identical electrical resistance:

	Aluminium	Copper
Density [kg/m^3]	2700	8920
Electrical conductivity [S/m]	$37{,}7 \times 10^6$	$59{,}6 \times 10^6$
Thermal conductivity [W/mK]	237	390
Specific electrical conductivity	13962	6681

In order to keep the same electrical resistance a thicker aluminium plate is required, roughly double thickness. The final mass of the aluminium busbar is however lower than copper.

Laser welding trials have been carried out on this aluminium busbars. This time it is possible to use a welding pattern called “wobbling” which leads to thicker welding, reducing the requirement on a good alignment of the laser source. In Fig.23 it is visible the preliminary result of this welding trials.

Fig. 23 – Welding trials on 2020 busbar design

After finding optimal parameters we obtained two methods for welding the tabs on the busbars: with 0,5mm tab protrusion from the busbar (sample 1) and with the tab at the same level of busbar surface (sample 4). By optical inspection the latter seems slightly worse in quality but the electrical resistance was comparable. From a mechanical point of view all the solder joints were strong enough so that a traction pull led to a failure of the tab material before the welding joint would fail.

Since maintaining 0.5mm protrusion on all the 120 tabs of the 2020 battery pack will be a very strict requirement to obtain, we decided to use the latest method (sample 4) since it offers both sufficient mechanical resistance and comparable electrical resistance.

2.4.5 Battery Management System

The BMS (Battery Management System) is a mandatory monitoring circuit for a lithium battery pack.

It monitors the voltage of each cell and the temperature of strategic points of the pack in order to avoid using the cells in unsafe operating conditions. In the event it detects undervoltage, overvoltage, overtemperature or undertemperature it limits the power available to the powertrain and in the eventuality that this is not enough to limit the stress condition on the cell, it requires the opening of the main contactor, effectively disconnecting the battery pack from the outside world.

Another important function of the BMS is the cell balancing. In order to maximize the available charge in the pack, it is required that all the cells are balanced. That means the voltage across each cell must be as uniform as possible among all the cells. Because of the production tolerances of the cells there will be little differences in capacity. During repeated charge/discharge cycles the weakest cell average voltage will decrease rapidly during discharge (or rise during charge). Since the overvoltage or undervoltage condition must be triggered immediately when a single cell reaches the limit this accumulated unbalance will limit the available energy in the pack. To overcome this limitation, the BMS will balance the pack periodically by discharging the most charged cells until all the voltages are within a given window.

There are a number of commercial BMS but given the space constraint in this design we have designed a custom BMS for this battery pack. This BMS is based around the LTC6804 chip from Linear technology as this is the state of the art chip for robustness and resolution [17] [18]. The architecture of the BMS is represented in Fig. 24

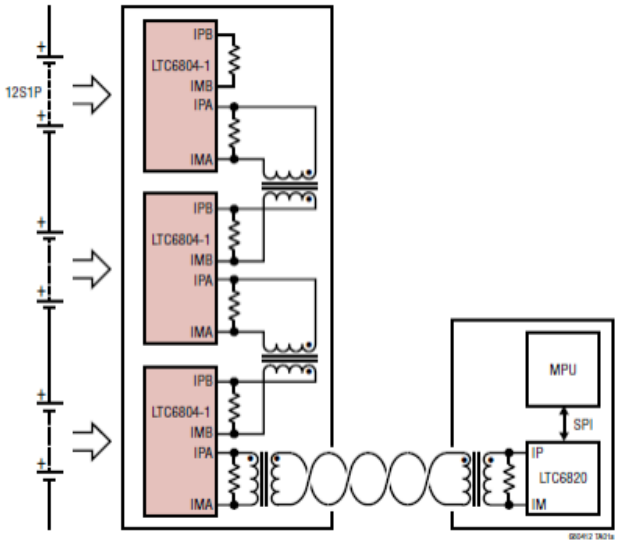


Fig. 24 – BMS Block diagram

Each chip can handle a maximum of 12 cells and 5 general purpose analog voltages, generally used for temperature measurement. It is an ISO26262 qualified chip for automotive use. It has the great advantage that the communication channel between each chip is galvanically insulated. This ensures safety of the circuit and the mandatory insulation required by the rules.

This chip can also handle the passive discharge of the cells trough an internal mosfet or an external one in case higher balancing currents are required. Since our cell is a high capacity cell, to obtain reasonable balancing times we need a high current and then an external mosfet and resistor have been employed. Those have been carefully dimensioned to obtain high discharge current and to keep the temperature of the balancing resistor within the cell limit to avoid heating up the cell during the

process. In Fig. 25 it is visible the thermal image of the BMS board during the balancing process. The temperature of the resistor is still within the operating range of the cell.

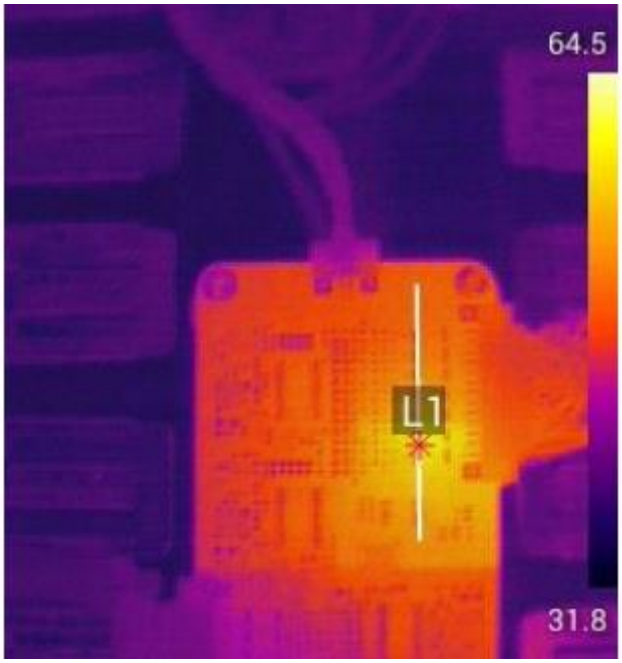


Fig. 25 – Thermal image of the balancing circuit in operation

Since our cell is composed by the parallel of two 30.5Ah cells, the resulting capacity is 61Ah.

We've imposed the maximum voltage dispersion to be 30mV, according to the OCV graph of the cell this corresponds to a worst case unbalance of 1.6% or 0.5Ah. Balancing often occurs at the end of the charging process, it is then reasonable to assume the voltage across the balancing resistor to be the full 100% SoC voltage or 4.2V.

The selected resistor is a 33 Ohm 2W thick film SMD. This gives a maximum discharge current of 127mA and a dissipated power of 0.5W, well within the power capability of the part.

With this resistor we can fix the 1.6% unbalance in 7.9 hours, which is a reasonable time to finish the balancing process overnight.

Despite the chip being ISO26262 qualified, since the rules states that the main contactor must open (and then retire from the competition) in the event of errors on the BMS it has been chosen to make the BMS redundant. There are two identical and separate BMSs on the same board.

The cell temperatures are measured in two ways: NTC placed on the cell side and PTC placed on the screw terminals that fix in place the BMS to the cell busbars. In this way, with the same screw we obtain electrical contact from the cell busbar to the BMS, mechanical attachment of the BMS and thermal interface between the cell busbar and the PTC sensor mounted on the PCB.

By mounting the PCB directly on the busbars we have the great advantage of removing the need for connection wires from the cell tab to the BMS. Those wires still exist, but they are embedded in the PCB itself instead. This has a huge impact on the assembly time (from 3 hours of wiring time of a conventional solution to the few minutes needed to fit 27 screws) and on the safety as well since the operator will never touches live connections.

A picture of the BMS assembled to the battery pack is visible in Fig. 26

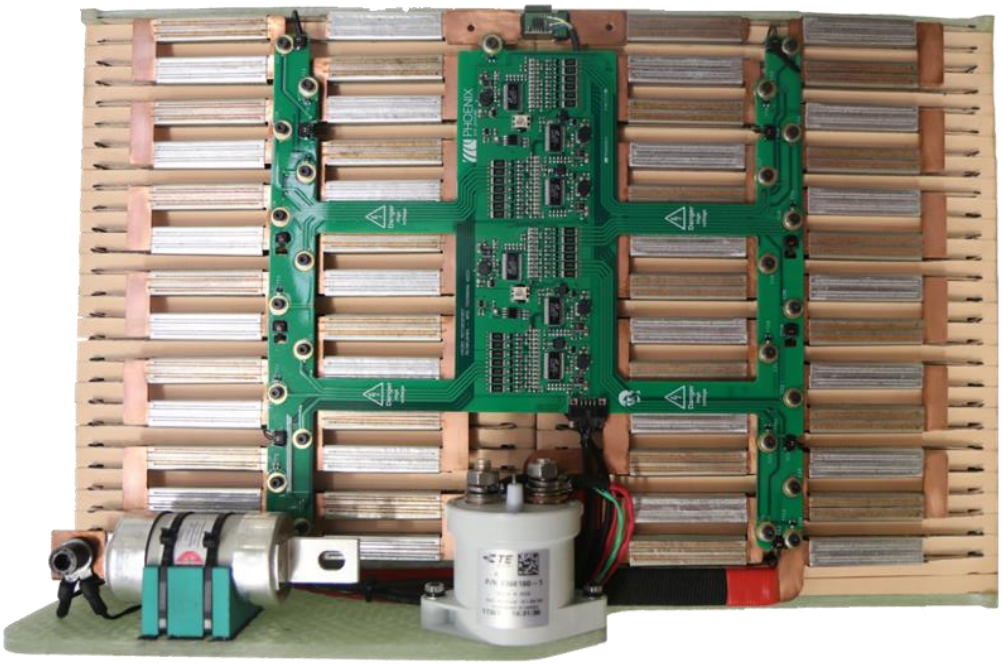


Fig. 26 – BMS PCB Assembly fitted to the battery pack

2.4.1 Mechanical structure

The mechanical structure of this battery pack is required to keep the cells in place during riding and to provide adequate cooling of the cells. It is also required to be as light as possible.

Lithium pouch cells like the one we've used also require some compression to operate at the best performance. We must also consider that the cells will slightly change their thickness because of thermal expansion and also because of the chemical reactions that take place inside the cell.

The mechanical element that keeps the cell in place and provides some compression and some compliance to address the cell expansion is the cell holder. It also has the function to keep separated the cells to form some ducts between them, where the cooling air will flow. This element is shown in Fig. 27.

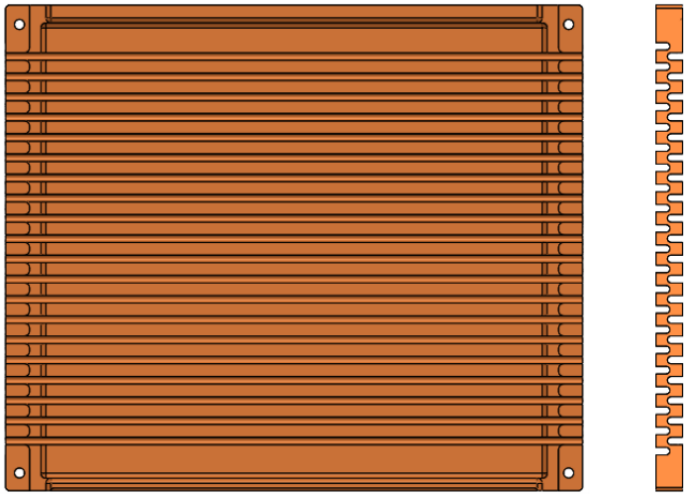


Fig. 27 – Cell Holder

This element has been realized by milling a solid block of B-Foam TF240 [19]. This is a rigid polyurethane foam with a density of 240kg/m^3 that is extremely light while retaining good mechanical properties and excellent electrical insulation. It is well suited to be milled with regular tools. The milled slots realize the cooling ducts where the air can be in direct contact of the cell surface.

A sandwich of cells and cell holders is composed and preload is applied through 4 threaded bars.

The sides of the pack are composed by two fiberglass panels that will sustain the loads to the motorbike chassis. The left side panel also provides mechanical attachment points for all the electronics: Line contactor and fuse, IMD, BMS, connectors.

2.4.2 Cooling

The cooling of this pack has been modelled and simulated in Matlab, taking into account the differences between the pack geometry and the data obtained during the characterization process of the cell. In particular, we have that a fraction of the cell surface is not exposed to air because in contact with the cell holder and the hypothesis of natural convection is now not applicable because the air will be pushed in the cooling channels by the means of cooling fans.

New parameters and approximations have been considered to set up this model: available thermal exchange surface (extracted by CAD data), specific heat of a Li-Ion cell (from literature and assumed constant), mass of a single cell, average ambient temperature in Aragon during race time.

A CFD simulation, visible in Fig. 28, has been carried on to choose the best compromise between cooling ducts geometries and extract the pressure drop the fans must sustain for a given airflow.

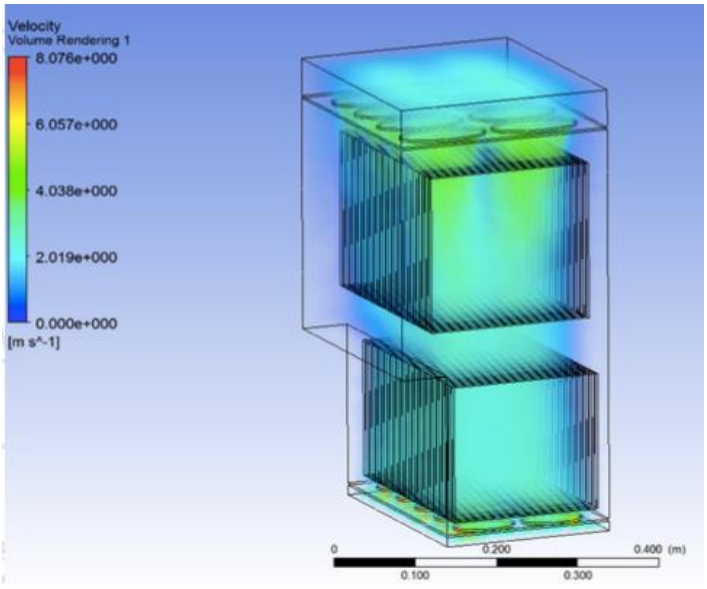


Fig. 28 – CFD Simulation of the cooling ducts

The model obtained has been integrated in the laptime simulator so that for a given ambient temperature we can obtain the required airflow the fans will need to sustain to keep the pack within safe limits. The fans are controlled in PWM by a PID controller with a setpoint of 45°C which is the optimal working temperature of such cell. This value gives also great margin to the 60°C recommended maximum cell temperature.

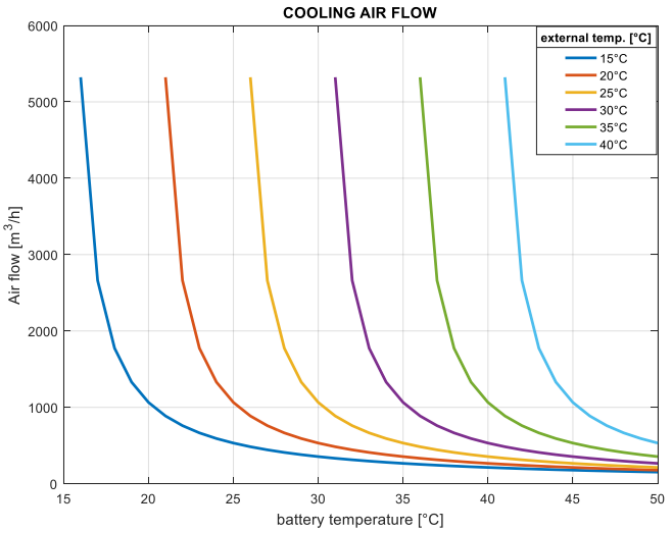


Fig. 29 – Simulated cooling airflow for a given ambient temperature and target cell temperature.

As a result of this study it was concluded that the required airflow to keep the cells in the optimal temperature range is about 1000m^3/h. Two fans from SPAL Automotive, VA168-A101-96A [20], were chosen. In this way a partial cooling was guaranteed even in case of one fan failure.

Telemetry from track tests confirmed the effectiveness of this cooling system showing that it is capable to keep the target battery temperature.

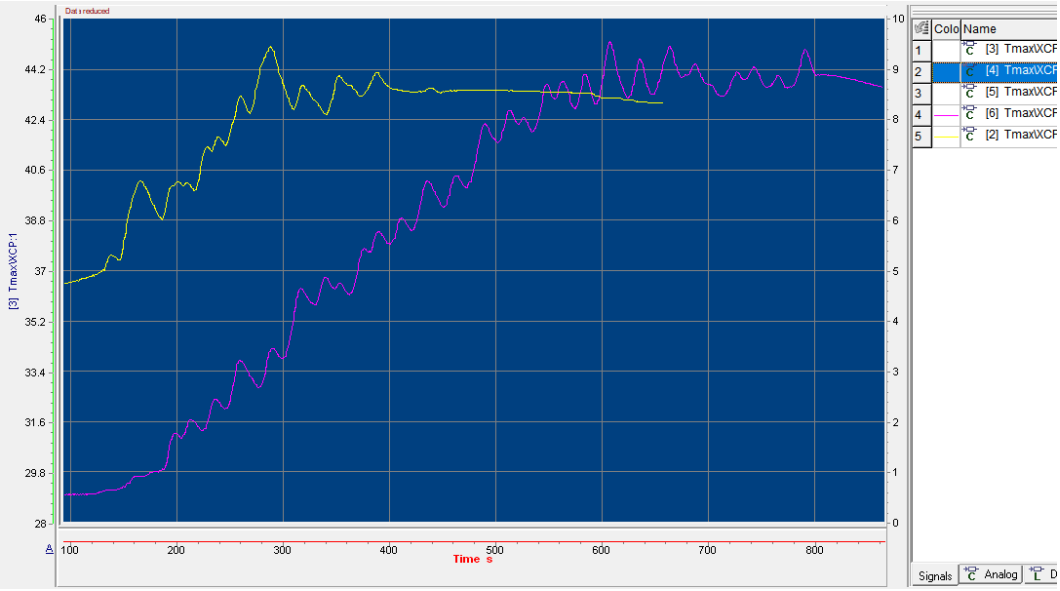


Fig. 30 .- Measured battery temperature during two different track tests (Cremona circuit, yellow and Adria circuit, violet)

In Fig- 30 is reported the maximum temperature measured by the BMS during two different track tests. It shows that the PID controller of the fans, thanks to an accurate design of the cooling system, is able to maintain the target temperature of the cells.

2.4.2 Packaging

The Motostudent rules state that the battery pack must be fully enclosed in the chassis structure. This is why it was decided that this battery case will be a structural element of the chassis itself (Fig. 31), simplifying the mechanical structure of the pack because all the loads will be sustained by the chassis.

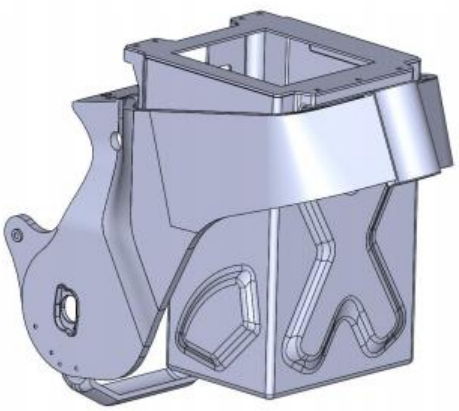


Fig. 31 - Carbon fibre chassis.
The rectangular box is the battery pack enclosure.

Fig. 32 - Fiberglass battery pack sidewall

The battery pack will be inserted from the top, electrically connected to the motorbike and then a cover lid is assembled with a given preload. This force will be sustained by the two fiberglass panels (Fig. 32) that form the battery pack sidewalls and will push the battery pack in place to prevent any relative movement during riding. Fiberglass was the material of choice because of the need to have electrical insulation towards the carbon fibre chassis combined with high mechanical properties and reduced cost.

For safety reasons, a fiberglass cover has been added to the pack in order to cover all the electrical connections to the cells. This is mandatory from the rules. It was also used as a mounting point for the inverter, in this way the electrical connection between the battery pack and the inverter is kept to a minimal length and the final result is a complete “power-unit” requiring only the motor connections and the BMS connections to the motorbike

The final result is represented in Fig. 33.

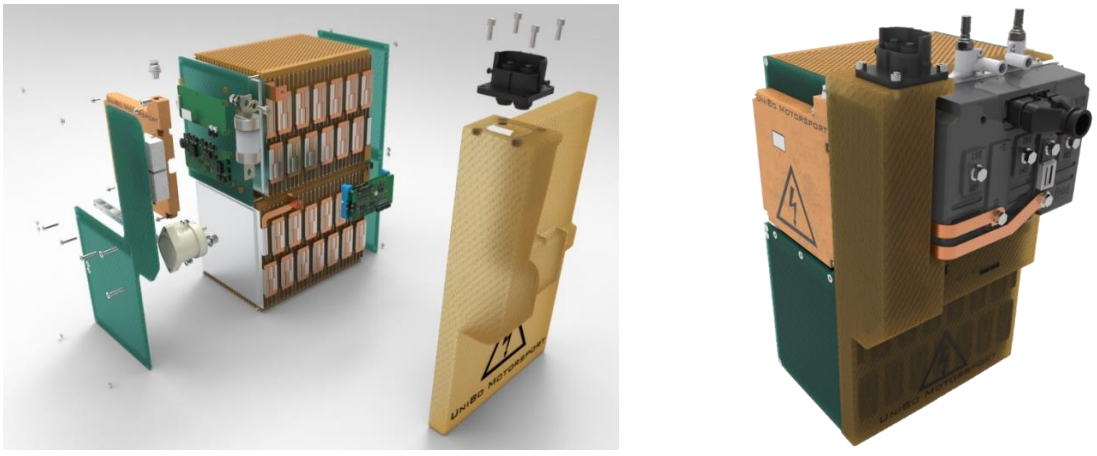


Fig. 33 – Complete battery pack, exploded view and finished assembly

2.5 Tests

After the pack has been assembled it was extensively tested in the lab to make sure it was able to deliver the required energy and all the temperatures and voltages were within safe values for all the length of the race.

From the laptime simulator the current profile requested from the pack during a race lap was extracted and used as a setpoint for an electronic dissipative load. The regeneration has not been tested during this phase because its effect on the cooling of the pack has been deemed negligible: laptime simulation shown that above 10% regeneration torque on the rear wheel is not beneficial to the laptime and also the riders confirmed that.

The lack of availability of a 50kW 110V electronic load forced us to design our own test device, composed of 50 1kW halogen lamps, individually controllable through a custom Labview application. This gave us a 1kW resolution on the applicable profile which is not ideal. This limitation was overcome by the simplicity of this solution and the extremely low cost, which is two orders of magnitude less than a professional equipment.

The very first test was a constant current charge/discharge profile. This was the first step to make sure no hotspots were visible through a thermal camera pointed to the cells welding joints and busbars. It also served as a test for the BMS operation, making sure it was effectively able to disconnect the pack in the event of an undervoltage/overvoltage or overtermperature. For obvious safety reasons the overtemperature was simulated by heating a real sensor connected to the bms but placed outside the pack assembly. Also during this test, the current sensor placed on the pack's internal busbar has been calibrated.

The following figures show the 1C discharge test (Fig. 34) and the 1C recharge test (Fig. 35).

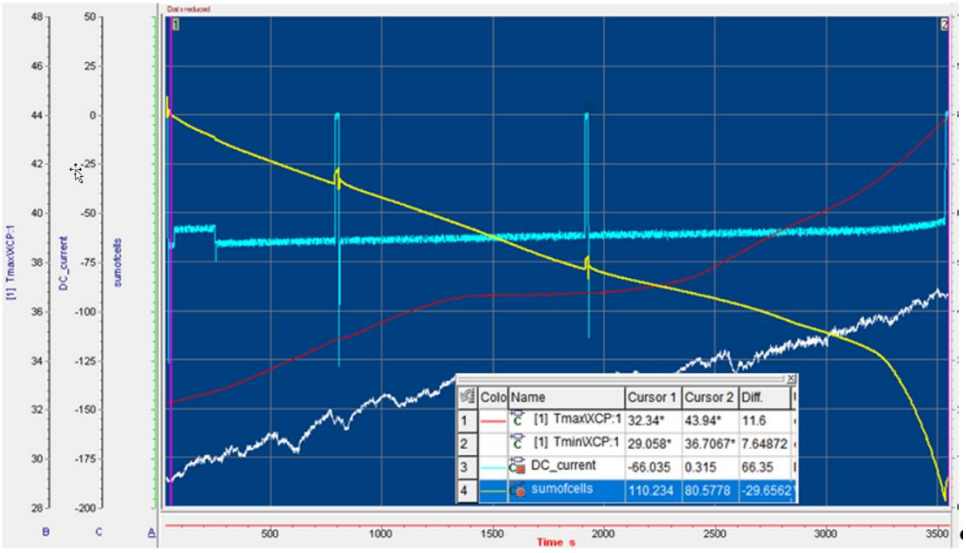


Fig. 34 – 1C Discharge test.

The blue trace is the current drawn by the active load, which is not perfectly constant because of the limitations of the active load used. In yellow the DC voltage across the entire pack. The red and white traces are respectively the maximum and the minimum temperature recorded by the BMS inside the pack. The maximum temperature is way below the absolute maximum working temperature of the cell and the temperature delta between the start and the end of the test is comparable to the laptime simulator output.

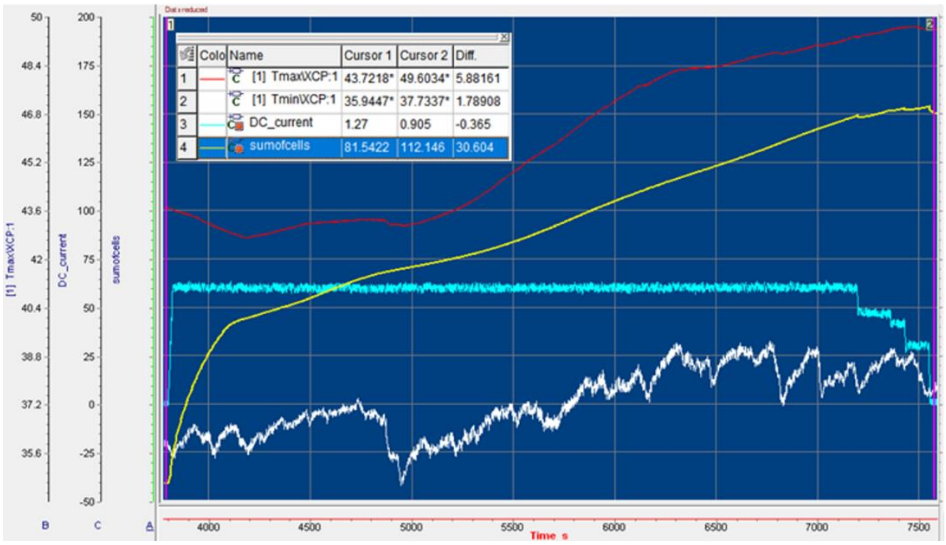


Fig. 35 – 1C charge test.

In both 1C charge and discharge tests the hottest point in the pack did not exceeded the cell's safe temperature limit. The discharge test started at 95% SoC and considering an end-of-discharge voltage of 2.7V the delivered energy was 58.9Ah while the theoretical energy at that SoC should be 58Ah. In the charge test the pack reached 99% SoC with a delivered energy of 61Ah. This difference between charge and discharge energy is consistent with the power lost by joule effect in the internal resistance of the cell itself.

The final test was to simulate the current profile requested through the race. This profile, visible in Fig. 36, was obtained from the laptime simulator and replicated for all the 6 laps of the race.

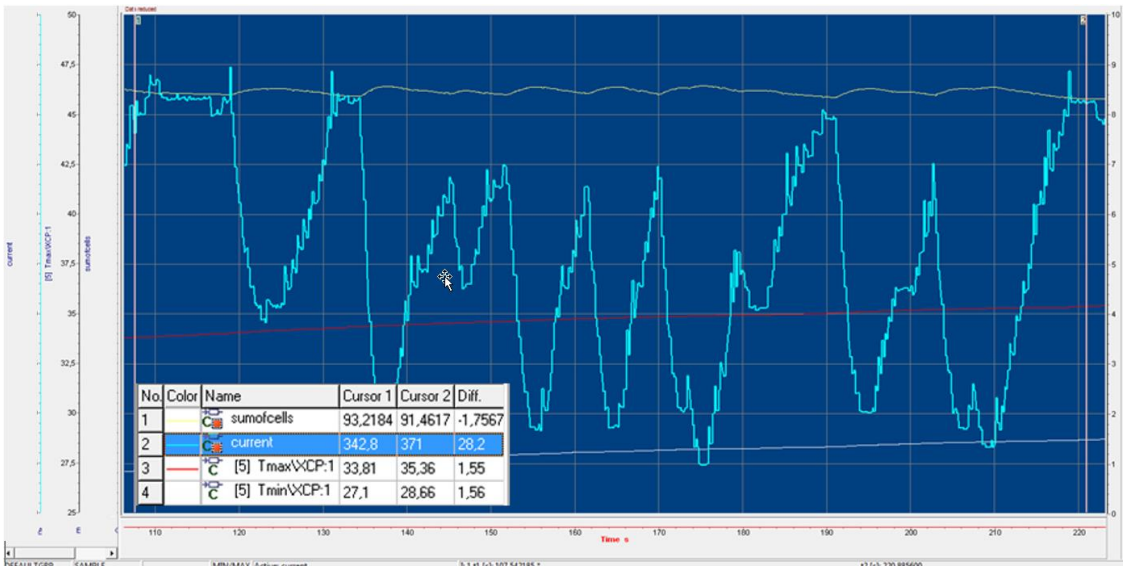


Fig. 36 – Current profile of a race lap used for the pack test

Since this lap profile was extracted without motor or inverter derating set, this is the most demanding situation the pack will ever experience. Having it successfully completed all the 6 laps at full power with all the temperatures within the limits it was declared fit to be used in the actual motorbike.

3 Inverter

3.1 Introduction

The inverter is the component responsible for the power conversion from the battery (DC current) to the motor (AC current) and vice-versa (in case of regenerative braking). Usually the motor is a three-phase electrical machine, so the inverter must be able to output a three-phase sinusoidal current. To achieve this it is usually composed of three separate half-bridge switches controlled in PWM in a way that the average voltage on each phase terminal is sinusoidal as well. In Fig. 37 is represented a typical three-phase inverter conceptual schematic. [21]

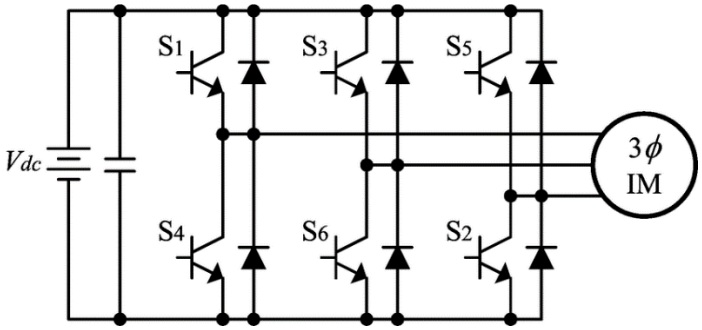


Fig. 37 – Three phase inverter simplified schematic

The switches S1 to S6 are the active devices that control the power flow in the inverter. Those are semiconductor devices capable to withstand the stressful conditions of operating in hard switching: the turn on happens with the full voltage across the terminals and the turn off will happen with the full current flowing through the device.

A key parameter of any inverter is the switching frequency: it is basically the PWM frequency that modulates the DC input voltage. The higher this frequency the lower is the current ripple in the motor and in the DC link capacitor, yielding to finer motor control and reduced capacitor size respectively.

To realize the switches there are several semiconductor technologies available nowadays. Those are summarized in the following table highlighting the benefits and the drawbacks of each one with respect to desirable properties of an inverter [22] [23] [21].

	Si Mosfet	**Si IGBT**	**SiC Mosfet**	**GaN HEMT**
Status	Mature	Obsolete	Active	New
Switching Freq	Moderate	Low	High	Very High
Max Voltage	+	+++	+++	++
Max Current	++	+++	+++	++
External diode	Body diode	Necessary	Body diode	Not needed
Design complexity	Low	Low	Moderate	High

For high power inverters, the DC Link capacitor is the larger component in terms of volume and a great fraction of the cost of the finished product. This is the main driver towards the development and adoption of fast switching technologies such as SiC and GaN.

SiC technology is well established, with several products already in the market. It is very well suited for high voltage, high power powertrains thanks to the exceptional thermal conduction properties of the material itself. The SiC manufacturers have pushed the development of such devices towards the 1200V class, leaving the <600V class without reasonable products to choose. Making a low voltage inverter with SiC devices is then counterproductive because we are forced to use 650V parts lacking availability of low-voltage optimized parts.

On the other side, GaN devices are relatively new and because of that the manufacturers are more focused on low voltage parts. At the moment on the market there are 200V and 650V devices (1200V devices are available but for particular applications only).

Since the maximum voltage for the Motostudent is 110V it is feasible and interesting to develop a GaN inverter using 200V parts. In this way we can benefit from the increased power density that they offer and further reduce the laptime considering the state of the art inverter for low voltage still uses conventional Si mosfets.

3.2 GaN semiconductors overview

At the present state of the semiconductor technology the GaN devices are sitting in between the Si and the SiC mosfets [24] [25].

It has the key advantage that the manufacturing can be done in the same facilities used for Si semiconducors.

In Fig. 38 is shown a comparison between key properties of Si, SiC and GaN semiconductors.

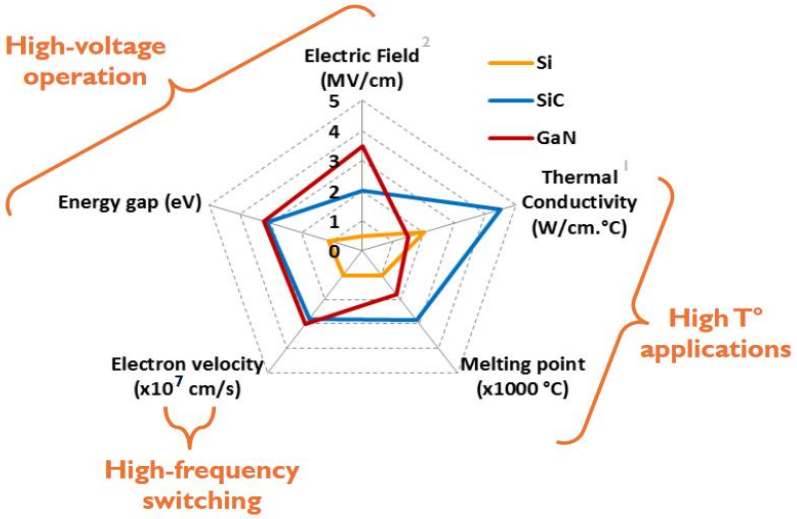


Fig. 38 – Comparison between semiconductor technologies

GaN is an high bandgap semiconductor (3.4eV, almost 3 times higher than Si semiconductor) and because of it can offer increased electron mobility and electric field.

Compared to Si, it has slightly lower thermal conductivity, that means it is harder to extract the heat produced due to the losses but this is mitigated thanks to reduced switching losses intrinsic to this technology and an higher melting point, so the chip can run hotter. [26]

GaN mosfets were commercially available in 2006 but those were depletion mode devices, that means the mosfet is normally ON and the gate terminal was used to turn them off. This is not practical to realize inverters because when the inverter is powered off the motor phases will be effectively shorted together. Since 2010 enhancement mode devices were developed and they are called eGaN

GaN mosfets have the key advantage that they can be produced using the same facilities of conventional Si devices. In fact the substrate material for a GaN mosfet is still a silicon wafer where a thick GaN layer is epitaxially grown. This is an high resistance material. On top of that a thin layer of AlGaN is deposited and creates a strain in the crystal structure of the device. Because GaN is piezoelectric material this strain attracts electron towards the interface between those two materials and forms a region called 2DEG (2 Dimensional Electron Gas). This is the area where the current flows. Further processing removes those electrons only in the region below the Gate contact. Finally an insulating layer is deposited and the metal contacts are created. [27]

By applying a voltage between Gate and source terminals, further electrons are attracted below the gate, restoring the 2DEG continuity and allowing the current to flow between Source and Drain terminals. In Fig. 39 the cross section of an eGaN mosfet is shown.

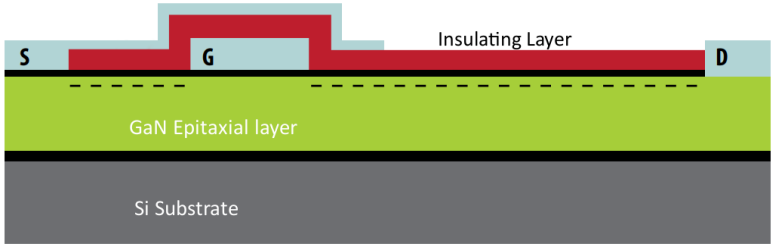


Fig. 39 – eGaN mosfet cross section

The production simplicity of such structures combined with the ability to use existing infrastructure makes those devices economically convenient. High electron mobility of the 2DEG layer leads to reduced On-Resistance , the absence of intrinsic parasitic in such simple structure is responsible for the high switching speed. Despite theoretical limit of the GaN semiconductor is still far away to be reached, this technology is already a competitor for Si mosfets. With the next generation of devices, GaN have the potential to become the material of choice to reach exceptionally high efficiencies and power densities.

Another important feature of this structure is the lack of an intrinsic “Body Diode” [28]. This diode is formed in the Si and SiC mosfet as a result of the production process and it is both a desirable feature and a source of switching losses because it has a non negligible reverse recovery time. GaN devices do not have such diode and then the recovery losses are eliminated.

However a body diode is desirable in an inverter since during the dead-time there are situations where the current must flow in the opposite direction and this is the reason why IGBT inverters require a separate diode external to each IGBT switch.

GaN mosfets do not need an external diode because despite lacking of a body diode they are capable of reverse conduction: when the Source-Drain voltage increases above a threshold voltage, because of the applied electric field, the 2DEG layer is formed anyway and reverse conduction can happen. This threshold voltage is in the range 2-3V and is much higher than threshold voltage of Si and SiC diodes leading to increased conduction losses. This is mitigated because, thanks to the fast switching behaviour, the dead time in GaN mosfets can be more than one order of magnitude less than Si devices.

Another aspect to be considered when using GaN mosfets in replacement to Si mosfets is that GaN devices do not tolerate avalanche [29]. Avalance is a phenomenon that occurs when the V_{DS} applied

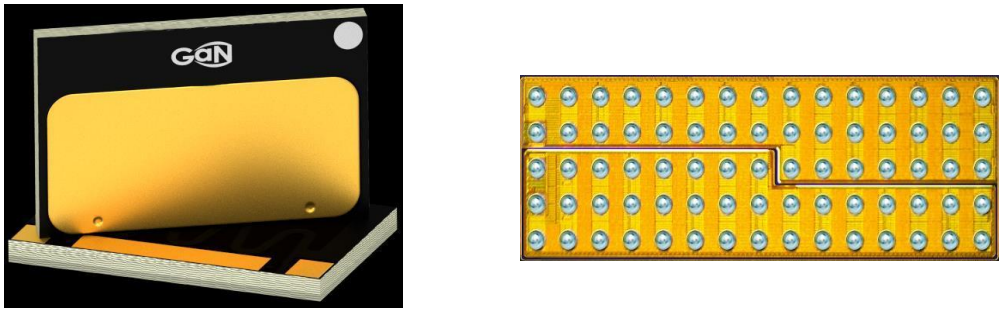
to a device rises above the breakdown voltage. In this case the electric field inside the device is so high that the device will conduct some current clamping the V_{DS} voltage to V_{DSBD}. In this situation VDS voltage is high and the current flowing into the device can be high as well. This leads to very high instantaneous power dissipated inside the device. Two failure modes are possible in a silicon mosfet because of this phenomenon: Latch-up or thermal destruction. Latch-up is a self turn-on of the mosfet due to the excitation of a parasitic NPN-like structure that is intrinsic in the device construction. Modern technologies have mitigated this phenomenon by using clever structures in the mosfet construction. Thermal destruction happens when the energy dissipated during avalanche rapidly increases the local temperature of the chip leading to deformation, cracks or melting of the chip structures. A certain amount of avalanche energy is then tolerated by the mosfet before one of this two phenomenon occurs and destroys the chip.

In GaN devices there is no intrinsic body diode and then no diode breakdown is possible. Avalanche will never happen in a GaN device. The failure mode for GaN devices in case of $V_{DS} > V_{DSBD}$ is a permanent damage in lattice structure of the chip and then immediate failure of the device. During the design process of a circuit using GaN mosfets is then important to choose a proper device such as we can have a very good margin with respect its V_{DSBD}.

Another aspect to consider is that GaN mosfets are much different in packages with respect to Si or SiC devices. The latter usually are packaged in industry standard enclosures such as TO-220, DPACK, D^2PACK, TO-274… Those packages have been developed for Silicon devices and their parasitic inductance, related to the pins and wire bonding, is optimized for their switching behaviour. A typical parasitic inductance for a TO-220 package is around 10nH. [30]

Such inductance in a GaN device will cancel all the benefit of a fast switching device: because of the higher di/dt capability of the GaN, this parasitic inductance will generate an induced voltage high enough to disrupt the V_{GS} signal, leading to instabilities in the gate, destruction of the gate oxide, EMI emission…

For this reason, GaN devices are usually delivered in ad-hoc packages designed to minimize this inductance. The two best packages at the moment available on the market are represented in Fig.40.



GaN Systems
GaNpx (proprietary package)

Efficient Power Conversion
Flip Chip BGA (Ball Grid Array)

Fig. 40 – Common GaN mosfets packages

Both packages require to be reflow soldered, slightly increasing the manufacturing cost, but they can achieve parasitic inductances as low as 0.5nH [27] [31]. GaNpx package is more suited for high voltage application (up to 650V) while BGA package is cheaper because it is already industry standard but offers lower breakdown voltage (up to 200V) because of the fine pitch between the balls (1mm or less).

3.3 110V GaN Inverter

We've chosen to design a GaN inverter for the electric motorbike for a number of reasons: first of all part of the score in the competition comes from a static evaluation of the overall project, called "Industrial Design" where points are awarded to the team based on how good they can motivate their design choices. Another award in the competition is the "Best Innovation" and since at the moment there are no automotive GaN inverters on the market it can be a good candidate to this award. Apart from the competition related motivations, we have serious packaging constraints in the motorbike and commercial Si-Mosfet based inverters are bulky and heavy.

The most used inverter in those application is the Sevcon Size 4 [32]. Starting from it's characteristics it was possible to set our design targets to match or overcome them. Those are summarized in the following table:

	Sevcon Gen4 Size4	**GaN Inverter requirement**
Max working voltage	116V	≥120V
Nominal current	160A	≥160A
Peak Current	420A	≥450A
Peak Power	35kW	≥48kW
Switching Frequency	8kHz	≥100kHz

Given those requirements a market research was carried on to find the best GaN device that can deliver those performances. Of course is not possible to reach those current levels with a single device and then multiple devices will be paralleled together.

The chosen device is EPC2034 [33] represented in Fig. 41 and the key parameters are summarized in the following table. It comes in a BGA package 4.6 x 2.6 x 0.7mm

Max working voltage	200V
Nominal current	48A
Pulsed current (1ms)	200A
On Resistance	10mΩ

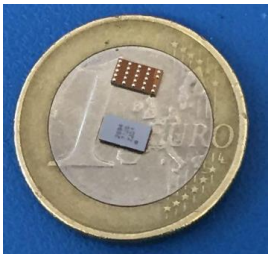


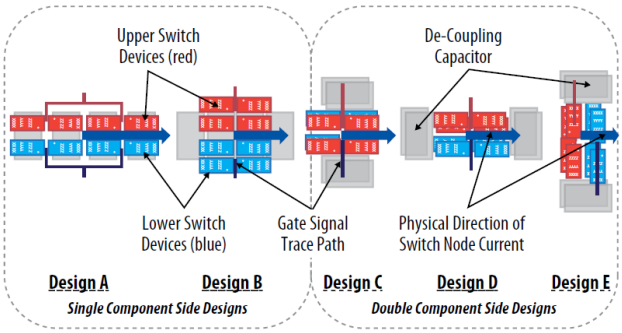
Fig. 41 – EPC2034 eGaN Mosfet

3.3.1 Design

The design for this 110V inverter was split in two different boards: a power board, containing the GaN mosfets with the associated gate drivers and a control board comprising all the electronics needed to generate the appropriate signals for the power stage.

The main design challenge for the power board was the high number of mosfets needed to meet the high output current specification. To obtain 450Arms output current the peak current in each switch must be at least $450\sqrt{2} = 634Apeak$. Since each mosfet can carry 48A maximum there is the need to parallel 13 devices. The GaN mosfets are extremely sensitive to layout parasitics and to minimize them a symmetric layout is mandatory. For this reason, it was decided to downgrade the current specification and use 12 devices in parallel. [34]

In literature there are available several studies [35] [36] [37] on the optimal layouts for GaN devices and the best compromise is to have a cluster of 4 devices in parallel (Design B) as shown in Fig. 42



	Design A	Design B	Design C	Design D	Design E
Gate Inductance [nH]	8.5* 4.2	4.4	4.9	3.1	3.6
Source Inductance [pH]	4100† 610	410	430	690	690

Fig. 42 – Different layouts and parasitics for paralleling 4 GaN devices.

The 12 devices will be split in 3 groups, each one with its own gate drive circuit. This is because the gate drivers circuit currently on the market cannot supply enough current to drive all the 12 mosfets together. This poses another constraint on the layout of the circuit because the 3 groups of mosfets must be turned on in the same instant to guarantee current sharing among the three groups. To obtain that, all the control signals traces between the control board and the gate drive are length matched to obtain same propagation delay. Fine tuning of this propagation delay will be done via software by the FPGA mounted on the control board.

As mentioned before, the GaN mosfets chosen for this application are enclosed in a BGA package. It is mandatory to mount them on a classic FR4 PCB. The downside of this kind of substrate is the difficulty to obtain a design that can carry such high currents. For this reason, we came up with the idea of directly soldering copper busbars on the PCB. The busbar will carry all the current so that the portion on PCB around each device will carry only the current of that device (<48A) which is very well below the limit of the classic PCB technology.

This busbar has been soldered on the PCB by using consolidated reflow soldering technology. On the first step the mosfets are soldered on the bottom side of the board using PB-Free solder paste that has a melting point of 215°C. Then the busbars are soldered on the top side using Sn/Pb solder paste that has a lower melting point of 188°C. This ensures that during the busbar reflow the GaN devices (which are now facing the ground) do not move or even worse fall from the PCB. The reduced

soldering temperature also helps to maintain short the pre-heating time of the copper mass contributing to reduce the thermal stress on the PCB.

A fixture has been developed to fix the busbar in place during the soldering process (Fig. 43). After some trials to find the optimal oven parameters, an X-Ray inspection of the mosfets solder joints (Fig. 44) confirmed that with this soldering method we are able to solder both tiny BGA devices and heavy copper bars on the same PCB.

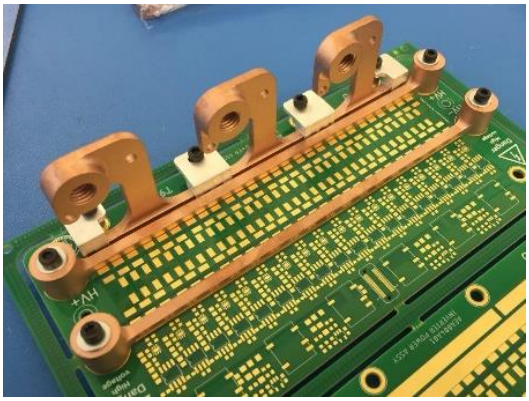


Fig. 43 – Busbar soldering fixtures

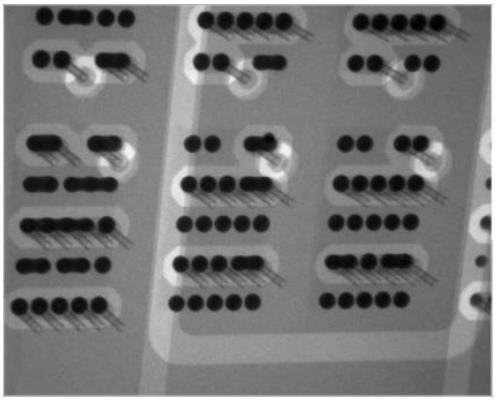


Fig. 44 – X-Ray analysis of the solder joints

In Fig. 45 the conceptual schematic of a single section of this power board is reported. Each phase of this inverter has 3 identical of such sections in parallel.

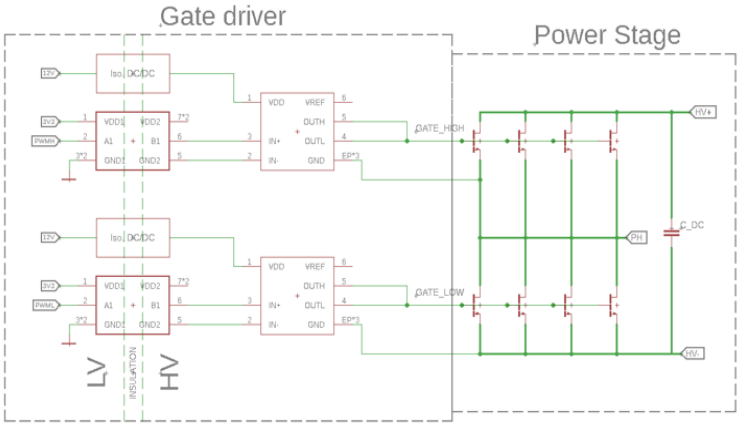


Fig. 45 – Conceptual schematic of one half-bridge section for the 110V inverter

The gate driver part is composed by a high speed digital isolator used to obtain galvanic isolation between the power stage and the control circuit. This isolator controls the Gate Drive chip that is an integrated circuit specialized in driving the gate signal for a GaN mosfet with the appropriate voltage levels. All the gate resistors, decoupling capacitors and auxiliary components have been omitted for clarity of the picture. The capacitor visible on the right is the DC- Link capacitor and it is composed by many ceramic capacitors in parallel distributed between the positive and negative busbars. By doing so the length of the trace between the capacitor and the mosfet, which is the main source for parasitic inductances, is optimally minimized. For 110V bus voltage, at least 200V rated parts must be used. Since this inverter is designed to switch at high frequencies the required total capacitance is in the order of few hundreds of µF. Relatively low voltage and low capacitance can be easily obtained with ceramic capacitors that are cheap and readily available. Moreover, they exhibit the lowest internal impedance in the range of frequency of interest for this application, minimizing the power loss. Another advantage is that they can be reflow soldered together with the busbars, with a clear advantage in assembly complexity and cost.

In Fig. 46 the final layout of the power board and the control board are represented.

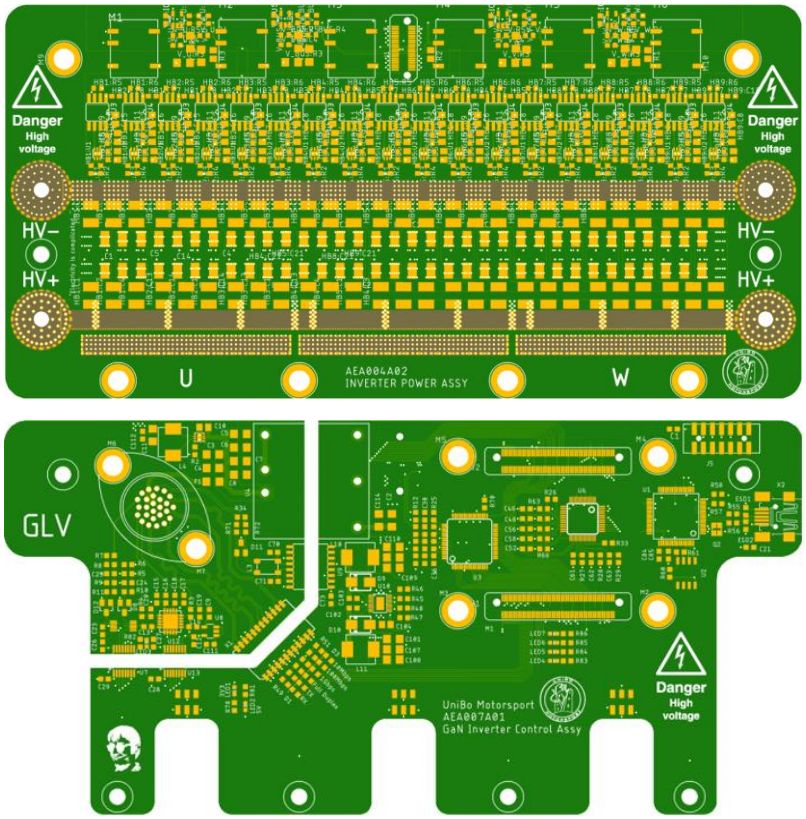


Fig. 46– Power board and Control Board layouts

The control board, through some connectors, is mounted on top of the power board to minimize the space. On the very bottom of the assembly there is the cooling plate, which is in contact with the top surface of the mosfets to extract the produced heat. Finally, a plastic support carries the mechanical loads for the vertical busbars and acts as a support for the hall effect sensors placed on top of the busbars to measure the phase current flowing in the motor.

In Fig. 47 is reported the 3D model of the assembled prototype.

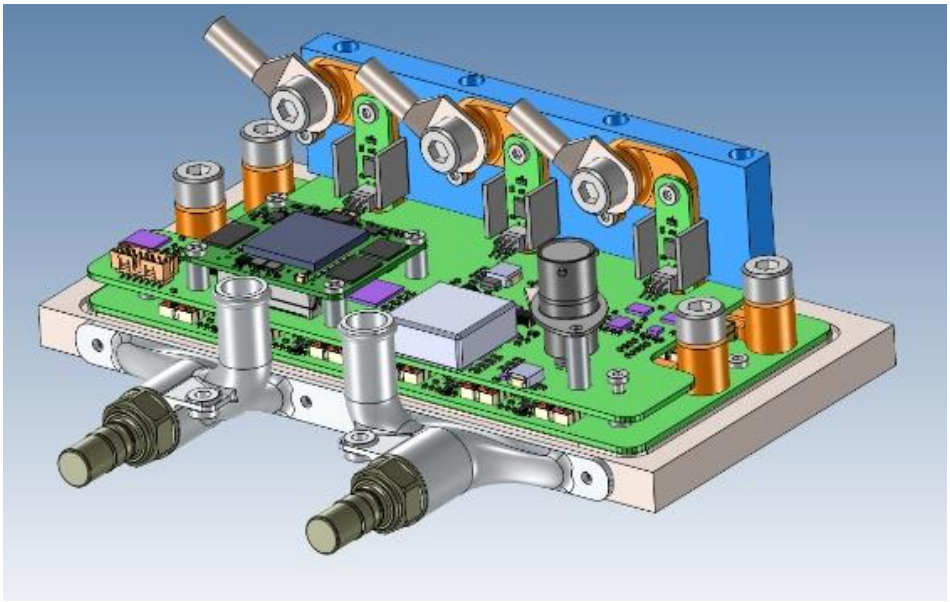


Fig. 47 – Assembled 3D model of the 110V inverter.

3.3.2 Test results

The assembled power board was subject to a number of tests to evaluate the correct behaviour and to characterize some properties that will be used later for a proper control of the entire inverter.

In Fig. 48 it is represented the physical test setup: an sbRIO9606 programmed in Labview has been used to generate precise and configurable test pulses. Those pulses were fed to the gate drive circuit on the main board. The wires going to the inductor were clamped inside a Tektronix TCP 0030 current probe, the V_{DS} voltages on the low side of the half-bridge were probed with Tektronix TPP1000 probes and the V_{DS} voltages for the high side were probed with Tektronix THDP 0200 probe. All this signals were recorded with a Tektronix MSO58 oscilloscope. Due to the very fast switching behaviour of these signals, to obtain sufficient time resolution on the waveform edges, an high bandwidth oscilloscope must be used.

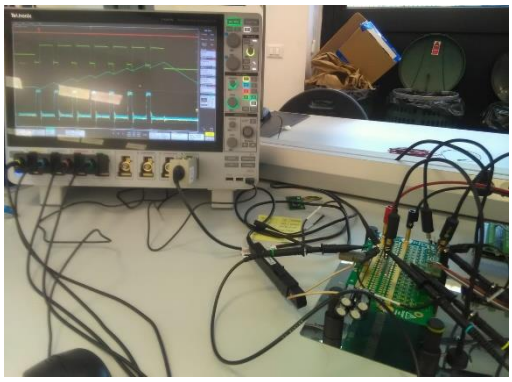


Fig. 48 – Double pulse test setup

Before carrying on with the high-power tests, a preliminary evaluation of the dead-time has been performed. The dead time is the time interval where both high-side and low-side devices are off and the current flows in the body diode in case of Si devices or in the reverse biased 2DEG channel in case of a GaN device. Since this mode of operation is a great contributor to the overall dissipated power we ideally want a null dead-time. Due to limitations of gate drives, interconnection parasitics and package parasitics it is not possible to instantaneously switch on or off a mosfet, then a dead-time must be always present and must be minimized. After some experiments the optimal dead time for this assembly has been found to be 20ns. Details are represented in Fig. 49.

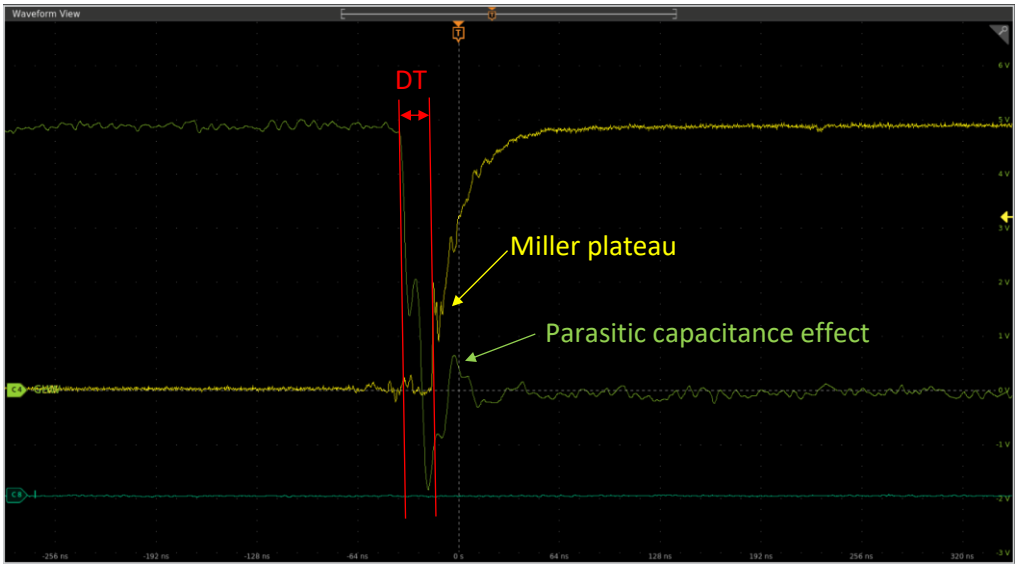


Fig. 49 – Minimum dead time evaluation and parasitic capacitance induced turn-on

From this preliminary test performed at low bus voltages (12V) we can immediately see that during the turn on of the low side switch (yellow trace) we have a parasitic voltage spike on the gate terminal of the high side switch. This is due to the extremely high dV/dt of such transitions, the parasitic capacitance intrinsic in the PCB structure inject some current in the gate of the turned-off

mosfet. This is a dangerous situation because if this voltage is high enough to rise above the V_{GSTH} of the mosfet, it will turn on generating a destructive shoot-through. Since the PCB parasitics are given by the PCB design, the only way to mitigate this is to slow down the transitions, degrading the efficiency in favour to the reliability.

This unwanted behaviour became an issue when this test was repeated at full bus voltage (110V).

The induced gate voltage was high enough to turn on the high mosfet and generate a shoot-through, leading to failure of both top and bottom devices. This was mitigated by increasing the gate resistor, effectively slowing down the switching transitions in order to restore the correct behaviour of the circuit. In Fig. 50 is reported the difference in the switching waveforms before and after this modification. It is clearly visible that before the modification the waveform was very noisy, a clear indication of uncontrolled current flowing in the device (shoot-through). After the modification the transition slope is slower and the induced voltage on the gate is below the V_{GSTH}.

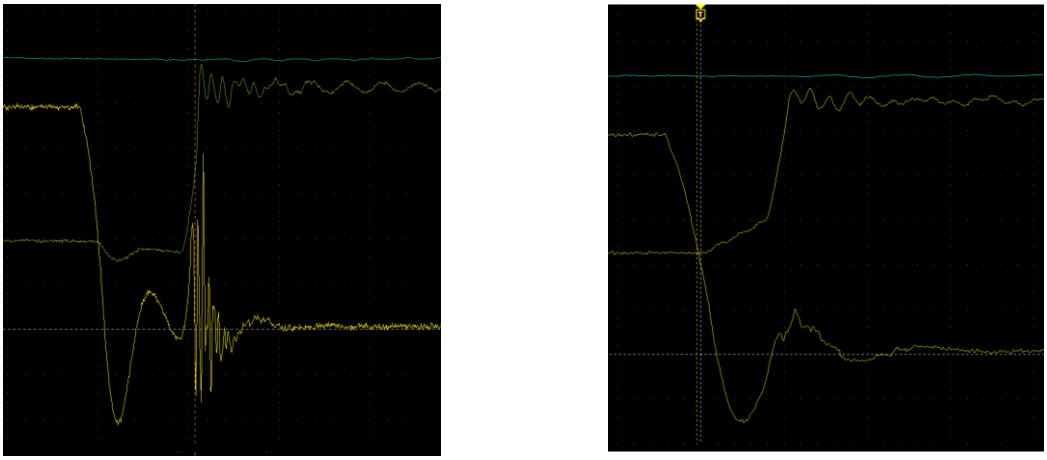


Fig. 50 – Gate waveforms before and after the gate resistor adjustment

After these preliminary tests, the “double pulse test” was performed. This is a standard test used to evaluate the switching behaviour of a power device. The device is externally loaded with an inductor, the equivalent schematic of the test setup is represented in Fig. 51.

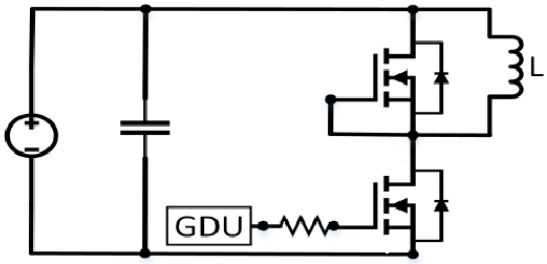


Fig. 51 – Double pulse test equivalent circuit

During a first phase the device is turned on and a current builds up on the inductor. When this current reaches the value of interest for the test, the device is rapidly turned off and then on again. In this way it is possible to evaluate how good the device can handle the rapid change in the drain current by measuring the voltage waveform across the drain-source terminals. Another advantage of such test is the short duration of the pulses, in this way we can assume the temperature of the device is constant across all the test.

The most important effect that we want to evaluate using this test is the VDS overshoot that is induced due to the high di/dt on the parasitic inductances intrinsic in the PCB design. It is needed that this overshoot stays below the absolute maximum rating of the device by a safety margin. This is particularly important for GaN devices because there is physical damage in the device in case of overvoltage. This is partially less important in Si devices since they can withstand it thanks to a phenomenon called avalanche, where in case of overvoltage the devices turns on by itself and forces

V_{DS} to zero. However it is a stressful phenomenon for the device and it is good practice to have this safety margin even with Si devices.

In Fig. 52 the double pulse test waveforms are reported.

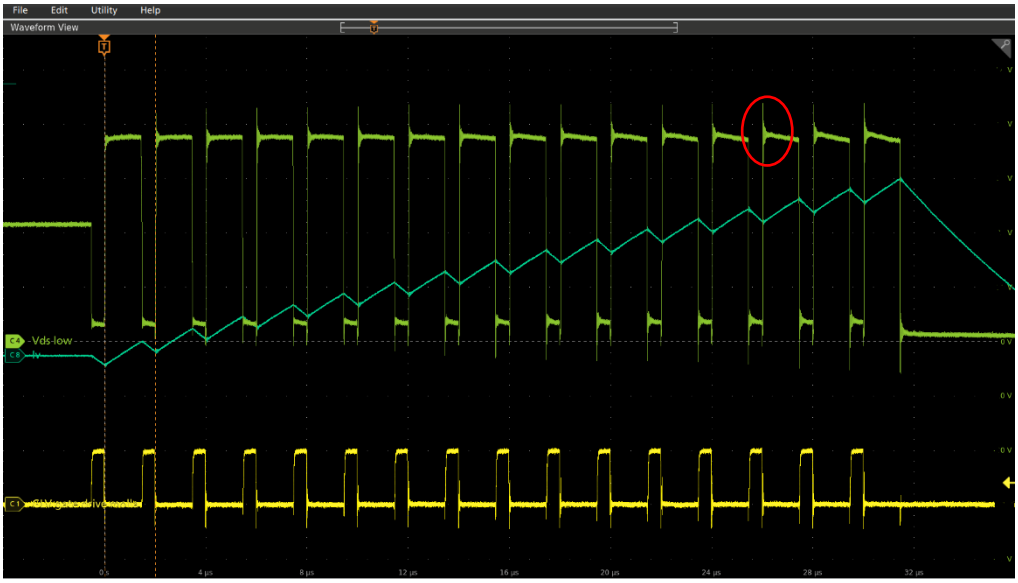


Fig. 5214 – VDS overshoot during double pulse test

In the red circle it is evidenced the voltage overshoot induced by the parasitic inductances.

This voltage was measured and it is was recorded a maximum spike of 128V when the DC-Bus voltage was 110V.

The EPC2034 mosfet is a 200V rated part but the manufacturer recommends to keep its VDS voltage below 160V for continuous operation. This gives us a worse case margin of 20% which is a reasonably safe margin for a motorsport inverter.

All those tests were carried on by driving only one cluster of 4 devices in parallel and is was possible to confirm that the circuit is switching properly, the gate drive is strong enough to properly drive the mosfets and the correct values for the gate resistors have been experimentally found.

More tests are currently ongoing by driving all the 3 paralleled clusters together to obtain the rated output current of this inverter.

3.4 500V GaN Inverter

From the knowledge gained during the development of the 110V inverter, it was decided to design another GaN inverter to be used on the Formula Student Electric prototype that UniBo Motorsport will race with in the 2020 season.

The rules of the Formula Student are quite different from the Motostudent ones and from the inverter perspective the two main differences are:

- Maximum DC Voltage is 600V instead of 110V
- Absolute maximum power drawn from the battery pack is 80kW. Regenerative braking power is not limited.
- Battery pack must be splitted in section of maximum 120V, 12kg, 6MJ, whichever greater.

The vehicle will be an AWD, that means there will be a motor for each wheel and then an inverter on each wheel. So the available 80kW power will be shared by the 4 wheels and then the inverter. The selected motor has a peak power of 35kW.

The high voltage GaN devices available on the market have a maximum V_{DS} of 650V, considering some headroom for the voltage overshoot mentioned before it was decided to use a DC-Bus voltage of maximum 504V which corresponds of a 120S battery pack that can be easily split in an even number of identical sections. Moreover the selected voltage is compatible with commercially available inverters, such as the Hybridpack DSC from Infineon, that can be used as a backup alternative in case this design will not be ready in due time.

In the following table the requirements of this inverter are reported and compared to the Hybridpack DSC:

	Hybridpack DSC	**GaN Inverter requirement**
Max working voltage	550V	≥504V
Nominal current	400A	≥80A
Peak Current	800A	≥160A
Peak Power	50kW	≥35kW
Switching Frequency	8kHz	≥100kHz

The GaN device selected to meet those requirements is the GaN Systems GS66516T [38]. This is a 60A, 650V device in a dedicated package which is optimized for extremely low parasitic inductance and a top cooling heatsink. In the following table the characteristics of this devices are summarized while in Fig. 53 a comparison of this package to conventional packages used for SiC devices is visible.

GaN Systems GS66516T	
Max working voltage	650V
Nominal current	60A
Pulsed current (100us)	144A
On Resistance	25mΩ

Fig. 53 – GS66516 Package comparison with a classic TO-247

3.4.1 Design

From the knowledge gained during the 110V inverter design, it was decided to start with a single half bridge prototype. This inverter uses high voltages and then the PCB layout become even more critical due to the need, from both design and sporting rules, of high creepage and clearance distances. By prototyping only one third of the inverter, in the case the prototype should need a new PCB to overcome eventual design issues, the complexity of the design and the manufacturing cost will be reduced. Moreover, this also reduces the overall prototype cost and assembly time.

To meet the design specifications, thanks to the high voltage involved, only 4 mosfets are needed in parallel. This is a clear advantage in reducing the complexity of the gate drive circuit and control pulses because there is only one cluster to drive simultaneously.

In the following table, the expected characteristics of the 4 paralleled mosfets are summarized:

Max working voltage	504V
Peak current ($T_j = 25°C$)	240A
Peak current ($T_j = 100°C$)	188A
On resistance	6.25mΩ

This first prototype is a single board with the mosfets placed on the bottom side and the gate drivers connected as close as possible to the gate terminals of the devices.

The equivalent circuit of this prototype is represented in Fig.54 and it is quite similar to the one used in the 110V inverter apart from the gate driver integrated circuit which is replaced because of the different gate threshold properties of the GaN mosfet employed in this design.

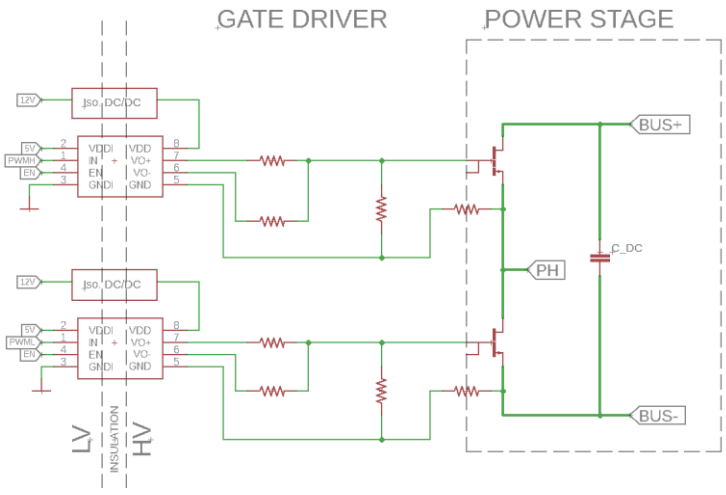


Fig. 54 – Equivalent circuit of the 500V GaN inverter prototype

As visible from this schematic, the GaN mosfets have two gate terminals. Those are two physical pins available on the device package that are electrically connected to the gate of the GaN chip and placed each one on one side of the package. This is a clever usage of the package properties and allows a layout that exhibit completely symmetrical traces from the gate driver chip to the GaN mosfet. By exploiting this feature a compact layout has been developed despite the 0.8mm clearance required at 500V by the IPC-2221B standard.

In Fig 55 the resulting layout is reported.

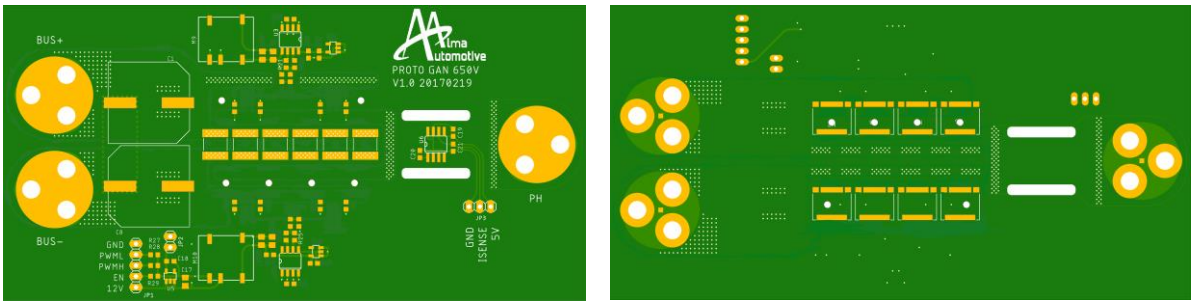


Fig. 55 – Top and Bottom layout of the 500V GaN inverter prototype

As visible in Fig. 55, the GaN devices are placed on the bottom side of the board and on the opposite side of the board, in direct proximity with the mosfets there are the decoupling capacitors. This layout allows minimal power loop inductance. An hall effect sensor has been placed directly on the board, on the right side of the top layer, to measure the phase output current.

Above and below the decoupling capacitors, the two identical isolated gate drivers are placed, making sure the length of the traces from the gate driver output to the mosfets are identical and symmetrical.

Two electrolytic capacitors, placed on the left side just next the DC input forms the DC-Bus capacitor.

3.4.2 Preliminary tests

This first prototype has been subject of preliminary tests to evaluate the effectiveness of this layout with respect to the parasitics and the ability of this new gate drive to correctly turn on the 650V GaN mosfet.

The same test performed on the 110V inverter to obtain the optimal dead-time has been replicated on this board, yielding to the result represented in Fig. 56.

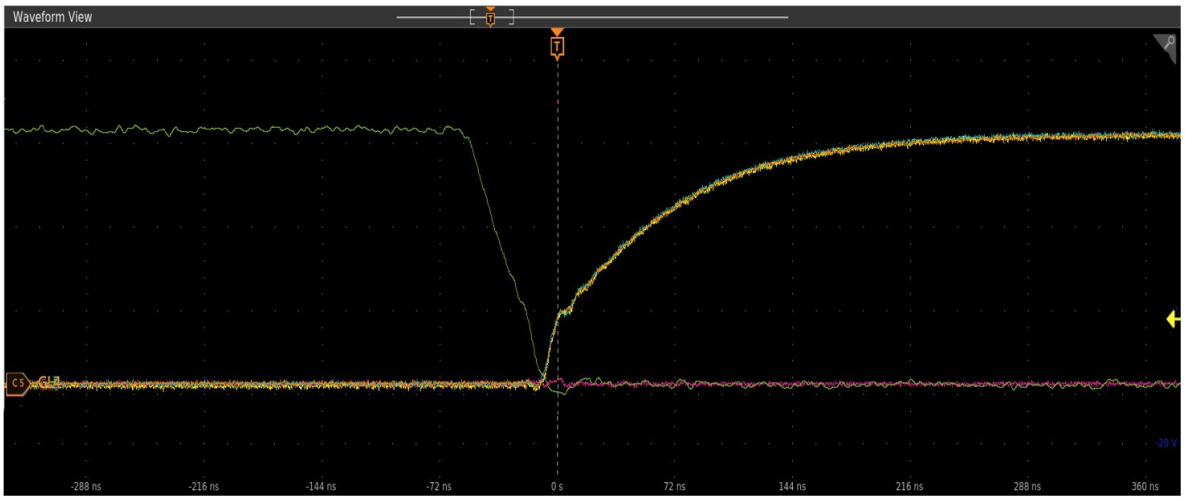


Fig. 56 – Dead time optimization on 500V inverter prototype

Following this test, a HV DC voltage has been applied to the input terminals and the switching behaviour using the classic double pulse method has been verified.

It was clear since the initial tests that this prototype is very sensitive to high dv/dt generated by the fast switching of the GaN devices.

In Fig. 57 is reported a measurement of the effect of this phenomenon, yielding to an accumulation of charge on the gate of the mosfet that should be off. This can lead to spurious turn-on and then destructive shoot-trough.

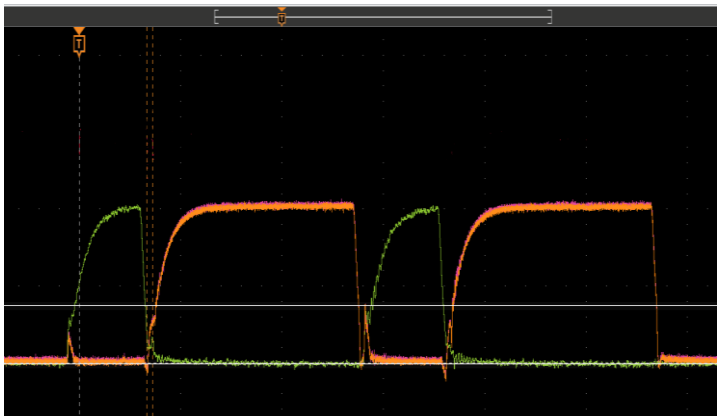


Fig. 57 – Spurious turn on due to dv/dt. (spikes on orange trace)

To overcome this unwanted behaviour we can slow down the transitions by increasing the gate resistors. This have a negative effect on the efficiency of the inverter and invalidate the benefit of using the GaN technology. However, it has been tried and the result is visible in the following figure.

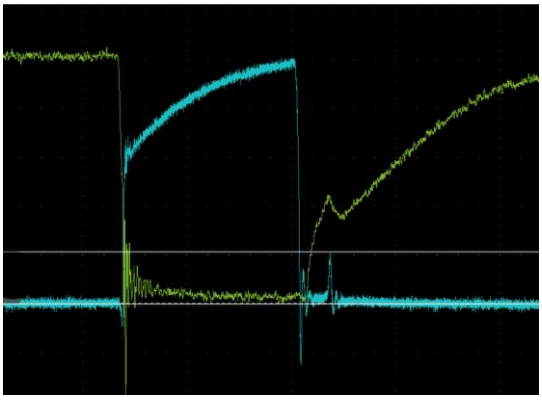


Fig. 58 – Spike on the blue trace reduced thanks to higher gate resistor

This simple modification is beneficial to mitigate the self-turn-on issue but yields to another problem that was not observed before. This issue, induced by an increased impedance of the gate loop, is an excessive undershoot on the mosfet's gate during turn-off. The GaN mosfet is rated for a +7/-10V absolute maximum and the undershoot, despite being within the limit, is something that should be avoided considering that this behaviour happened before reaching the full output current and it is

proportional to the di/dt of the output current. This phenomenon has been acquired and reported in Fig. 59.

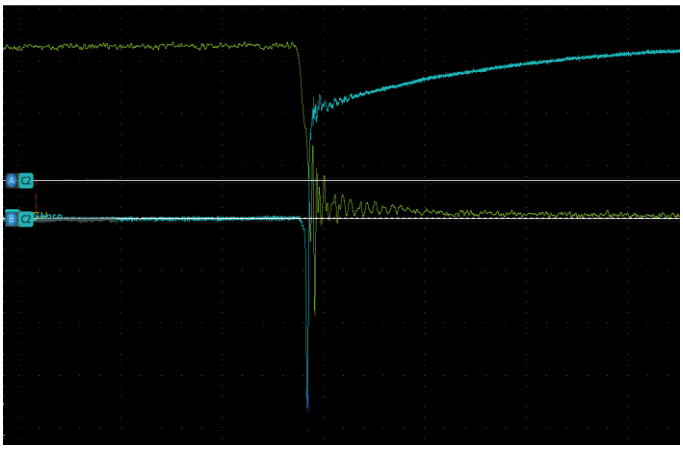


Fig. 59 – Undershoot on the gate terminal of top side mosfet

The conclusions obtained with the tests on this prototype are:

- A low gate loop impedance is critical to keep the gate voltages within the limits.
- A high gate loop impedance is beneficial to avoid self-turn-on, but degrades the switching behaviour.

A solution to both this problem is to use a gate drive capable to drive the gate terminal with a negative bias during the off period of the mosfet. In this way we can keep the loop impedance low and maintain safe margin during the dv/dt induced spike in the gate voltage.

Another design improvement that is possible to carry on is to have a layer buildup on the PCB made in such a way that the gate traces are placed on an inner layer and shielded by the two adjacent layers that will be connected to the source. However, given the voltage and current constraints required by this design, it is not practical. Another solution to obtain the same effect is to put the gate drive on a separate pcb mounted on top of the power board. In this way the wire connecting the gate drive to the power mosfet is orthogonal to the high current path and then the dv/dt effect is minimized by design.

3.4.3 Improved design

From the conclusions obtained during the prototype test, a new version of the inverter has been designed. It will be a complete prototype with all the three half bridges onboard.

The improvements implemented on this new version are:

- Stacked design, with three different boards for power circuit, gate drive circuit and control electronics. This helps to reduce the length of the signal path from the gate drive to the power devices and also makes this path orthogonal to the high current traces on the power board.
- Improved gate drive circuit, featuring a dedicated chip providing negative bias to the gate and a protection circuit, commonly used for classic IGBT but highly optimized for fast GaN devices, called desaturation detection.

The final layout of the complete assembly is represented in Fig. 60

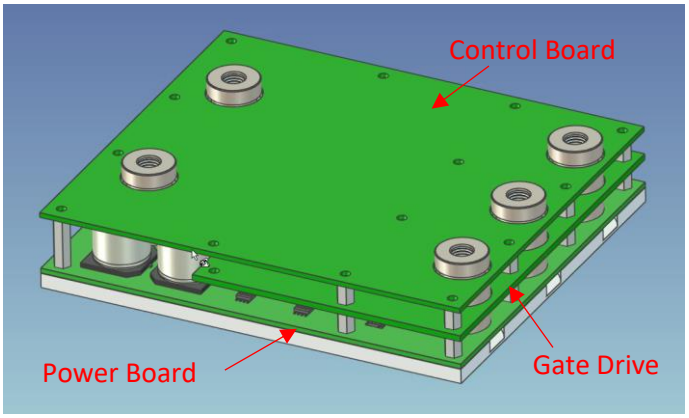


Fig. 60 – 500V GaN inverter assembly

The Power board only contains the power devices, the decoupling and DC Bus capacitors and the current sensors. This is connected through 1.27mm pitch connectors to the gate drive board that contains the gate drive and the desaturation detection circuit. The layout of those boards are visible in Fig. 61

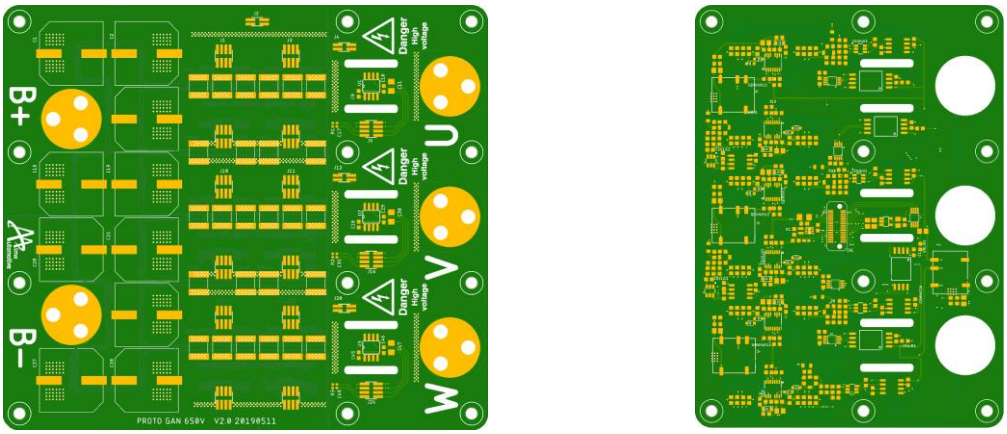


Fig. 61 – Power board and Gate drive board layout

The gate drive circuit is based on the chip 1EDF5673K from Infineon [39]. It contains all the circuitry needed to drive the gate of a GaN mosfet, including the generation of the negative bias to force the

turn-off of the mosfet. It is also galvanically insulated and it is the best available solution for a complete gate drive on a single chip.

The desaturation detection circuit was instead composed of discrete components due to the lack of dedicated chip available on the market.

Desaturation detection [40] [40] is a technique to detect when the current of the mosfet rises above a safety threshold, either because of output short circuit or shoot-through. A block diagram of such circuit is represented in Fig. 62.

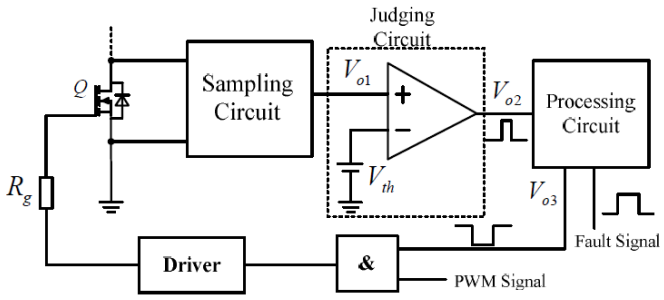


Fig. 6215 – Desaturation detection circuit block diagram

This circuit monitors the V_{DS} voltage when the device is on. If the V_{DS} rises above a certain threshold that means the current on the device is high enough to shift the operating point of the device outside the saturation zone, a situation that rapidly increases the power dissipated by the device usually ending with permanent damage to the device itself. When this situation is detected, the mosfet is turned off. Commercially available circuits are meant to be used with IGBT devices that can withstand short circuits of hundreds of microseconds. GaN devices are much more delicate, tolerating an overcurrent for just few microseconds. Then a much faster circuit is needed and has been designed and simulated in LTSpice. Simulation result, visible in Fig.63, show that the circuit is theoretically capable of detecting this event in few hundreds of nanoseconds. It was then implemented in this gate drive prototype.

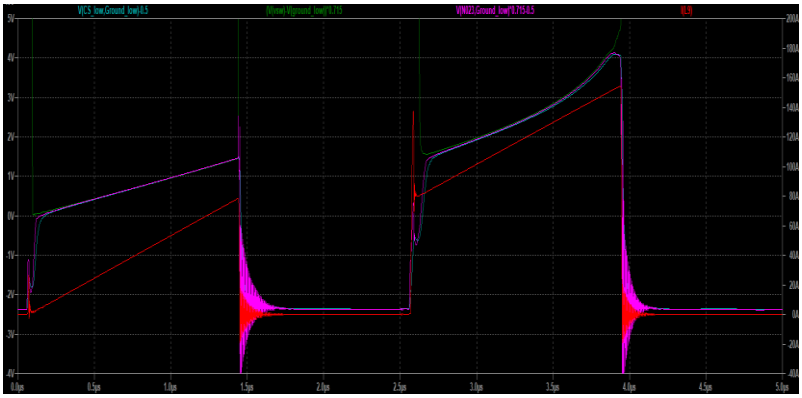


Fig. 6316 – Desaturation circuit simulation result

Currently the PCBs for this new version of the power board and the associated gate drive have been produced and are currently being assembled.

3.5 ZVS Inverter

In a power mosfet part of the power absorbed by the power supply is not delivered to the load but is instead dissipated inside the device because of many phenomenon. The most important are:

- Conduction losses: the gate channel of a mosfet device has an intrinsic resistance and the current flowing in it produces a voltage drop and then heat because of joule effect. This power loss can be assumed purely ohmic:
$$P_{LOSS} = R_{DSON} * {I_D}^2$$
- Gate charge loss: since the gate can be modelled as a capacitor, some power will be dissipated during turn-on and turn-off to charge and discharge this capacitor. This loss is proportional with the switching frequency:
$$P_{GATE} = Q_G * V_{GS} * f_{SW}$$
- Switching loss: during turn-on the gate channel pass from a depleted state to a fully enhanced state. During this transition the mosfet conducts current while the channel in not fully formed and then its resistance is not minimal, yielding to a considerable power loss. The opposite happens during turn-off. This is minimized by having very fast transitions or reduced switching frequency:
$$P_{SW} = \frac{1}{2} * V_{IN} * I_{OUT} * (t_r + t_f) * f_{sw}$$
- Dead time loss: when the device is reverse biased, the current flows in body diode instead of the gate channel. The body diode has a characteristic voltage drop that cannot be eliminated. Dead time is kept as small as possible by design so this kind of loss is usually low.

The overall power dissipated in the active device is then highly correlated with the switching frequency, as visible in Fig. 64, where losses have been calculated using real case values extrapolated from a Sevcon Gen4 Size4 inverter:

Fig. 64– Power mosfet losses vs switching frequency

This poses a limit to the maximum frequency a power converter can be operated because the power that a mosfet can dissipate is limited by its design. It is common practice to never go above the switching frequency where the switching loss is more than the conduction loss.

The downside of keeping the switching frequency low is that all the passive components, such as filter inductors and DC Bus capacitors have to increase in size, with obvious disadvantages in terms of occupied volume and cost. There is a general tendency in the power converters market to obtain devices that can switch fast (t_f and t_r low) so that the conduction loss will still dominate even at high switching frequencies.

On a three phase inverter for motor drive, the DC Bus capacitor is largest component in the entire assembly and the one that consumes the greatest fraction of the overall inverter volume. Reducing the capacitor size is one of the main issues when the power density is desirable, such as motorsport application. In literature there are several studies that aim to find the optimal method to minimize the capacitor size but the presented results are often discordant.

An LTSpice simulation has been performed to better understand the impact of the DC Bus capacitor. An ideal inverter has been modelled, driving an electrically modelled three phase motor. Other hypothesis done in this simulation are: DC Bus capacitor is 200uF, the inverter is connected through a 1uH inductor that models the parasitic inductance of the connection wires to a 110V 20mOhm generator that models the battery pack.

The result is presented in Fig. 65 and shows that the voltage ripple on the DC Bus capacitor scales with the square of the frequency.

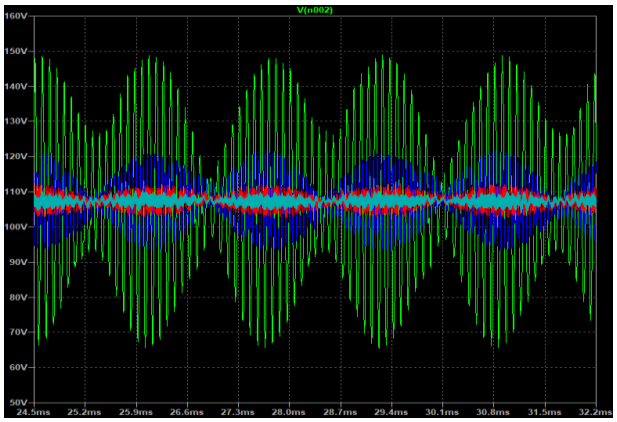


Fig. 65- Simulation of the voltage ripple on DC Bus capacitors

This has been found coherent with the results in [41] where the required capacitor size is calculated with the formula:

$$C = \frac{V_{BUS}}{32 * L * \Delta V * f_{SW}^2}$$

Plotting this formula with the same hypothesis of the simulation yields to the following graph:

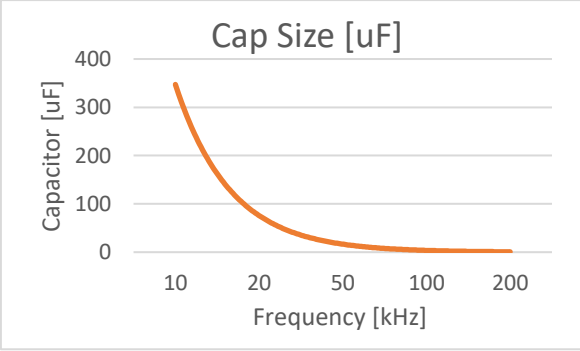


Fig. 66 – Required DC Bus capacitor for a given switching frequency

Is it clear then that by increasing the switching frequency the bulkiest component in an inverter assembly can be dramatically reduced in size.

To increase switching frequency it is required to reduce the switching losses, otherwise the thermal management of the active devices will become an issue. This is accomplished either by using wide bandgap devices such as SiC or GaN (thanks to their intrinsically low t_f and t_r) or employ complex topologies to reduce the switching loss by other means.

ZVS (Zero Voltage Switching) is one of this methods, that aims to force the VDS of a mosfet to zero during the turn-on and turn-off and then obtain zero power loss during such events. There are many circuit topologies capable to obtain such behaviour but when applied to inverter they are complex and unable to achieve ZVS in the full working range of the inverter.

During my abroad period at Infineon Technologies AG, a novel circuit architecture that can obtain ZVS in all the operating conditions of the converter has been studied and prototyped, showing that a substantial frequency increase can be obtained using conventional Si mosfets with a reduced added complexity.

3.5.1 Principle of operation

The circuit subject of this study is an evolution of what proposed in [42] and their simplified schematic diagram is reported in Fig. 67. For confidentiality reason it is not possible to represent the real schematic but this shares the same philosophy and principle of operation.

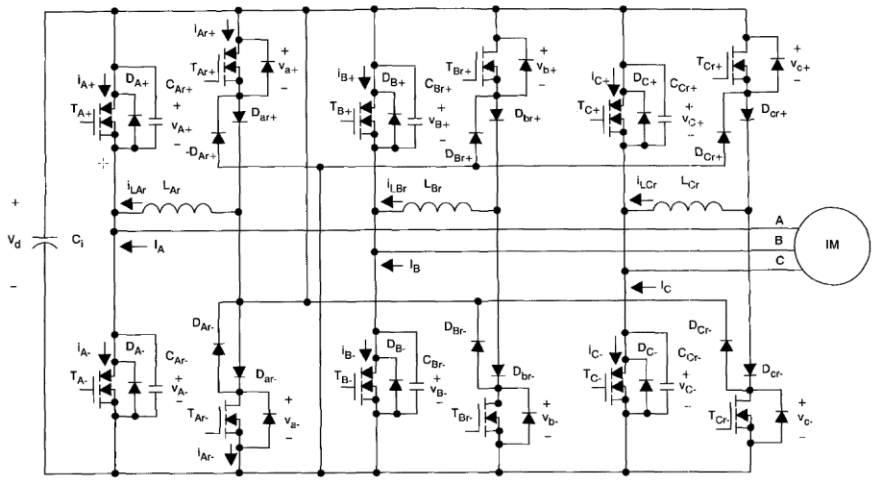


Fig. 67 – ZVS Inverter schematic

To understand the circuit operation only the first half bridge will be discussed as the others works in the same way. The mosfets TA+ and TA- are the main switches and they carry the full load current of the motor. The circuit composed of T_{AR+}, T_{AR-}, L_{AR}, C_{AR+} and C_{AR-} is called auxiliary half bridge and it is responsible for the main switches to obtain ZVS.

The sequence of events during a full switching period is the following:

1. Let's assume the initial state is T_{A-}=On and then V_{A-}=0, current I_A is flowing into T_{A-} and we are at the end of the switching period so TA- must be switched Off and TA+ must be switched On.

2. The current on L_{AR} is zero, T_{AR+} is switched On with zero current so it has no switching losses. L_{AR} current increases

3. T_{A-} is switched Off, the capacitor C_{AR-} maintains V_{A-}=0 because is discharged and then T_{A-} achieves zero voltage turn off.
4. Current flowing in L_{AR} charges C_{AR-} and discharges C_{AR+}.
5. When C_{AR+}.is discharged, T_{A+} is switched On, achieving zero voltage turn on.
6. At this point T_{AR+} can be switched off with zero current switching because all the load current is flowing in T_{A+}

After the PWM On time required by the motor control algorithm, the opposite transition will occur until the state at the point #1 is reached.

7. The current on L_{AR} is zero, T_{AR-} is switched On with zero current so it has no switching losses. L_{AR} current increases
8. T_{A+} is switched Off, the capacitor C_{AR-} maintains V_{A+}=0 because is discharged and then T_{A+} achieves zero voltage turn off.
9. Current flowing in L_{AR} charges C_{AR+} and discharges C_{AR-}.
10. When C_{AR-}.is discharged, T_{A+} is switched On, achieving zero voltage turn on.
11. At this point T_{AR-} can be switched off with zero current switching because all the load current is flowing in T_{A-}

All the transitions in all the switches are happening with zero voltage or zero current across the switch, with the result of zero switching losses.

The price to pay for this is an increased complexity in the control signals and an increased component count. However, the auxiliary switches is operating just during what in a normal hard switched topology will be the dead time, which is a small fraction of the overall switching period. This allow the auxiliary switches to be much smaller than the main switches.

A prototype of such inverter has been developed, built and tested during my mandatory abroad period and it cannot be disclosed due to confidentiality agreement with the institution where this activity took place.

3.5.3 Test results

The very first test was to determine if the auxiliary switches can drive the phase output so that the main switches are effectively switching with zero voltage. Double pulse test has been performed so that and the result is visible in Fig. 68.

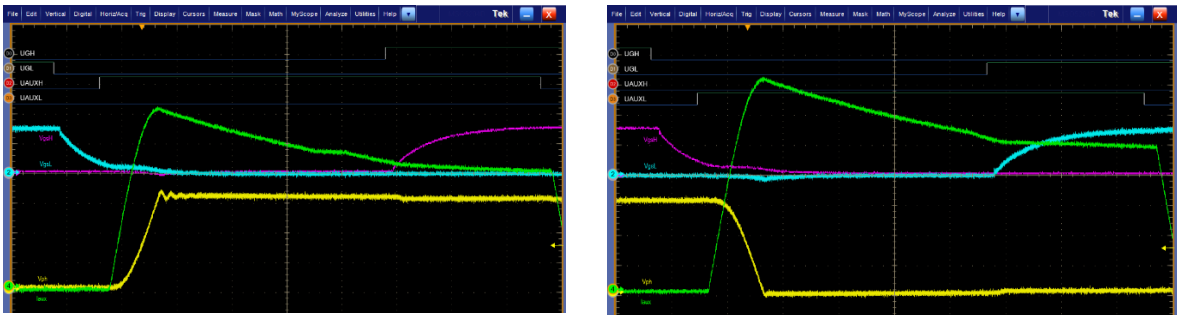


Fig. 68 – Switching waveforms of the ZVS inverter prototype

It is clear that both the top mosfet and the bottom mosfet (respectively left and right figure) are operating in zero voltage switching. The phase output voltage, yellow trace, reaches the final value before the relative mosfet is turned on (blue and purple traces are the gate voltages). Moreover the yellow trace transition smoothly from zero to the DC Bus voltage giving considerable benefits on the irradiated and conducted emissions on the motor windings.

After verifying that the auxiliary circuit can achieve ZVS on the main switches, the inverter prototype was connected to a physical asynchronous three phase motor and efficiency of the circuit was evaluated.

The prototype was controlled through a rapid prototyping platform such as the National Instruments sbRIO-9606. It can be programmed in Labview and it features an FPGA used for precise generation of the complex PWM pulses required to drive both the main and auxiliary switches. The advantage of this approach is that writing the software is very simple compared to classic VHDL programming approach and all the variables can be manipulated on a custom graphical interface, visible in Fig. 69.

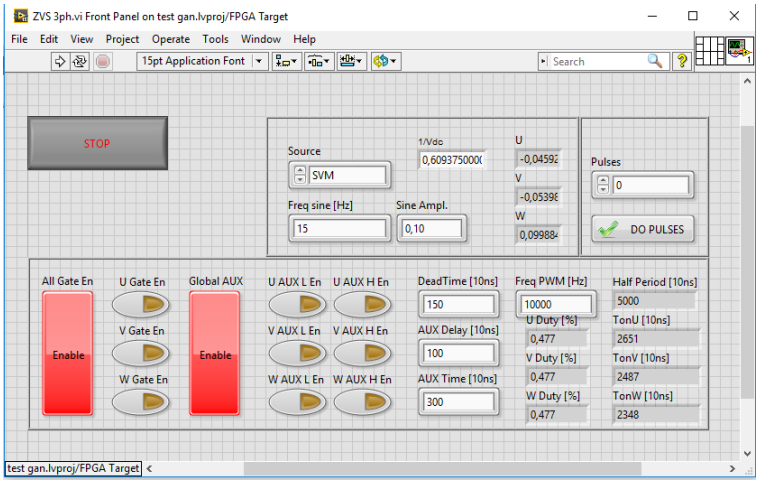


Fig. 6917 – ZVS Inverter control panel

It was possible to disable on-the-fly the aux switches, making it possible an immediate evaluation of the efficiency difference between the main switch only configuration (equivalent to a classic hard switching inverter) and with aux switches enabled to achieve ZVS.

The test result is summarized in Fig. 70.

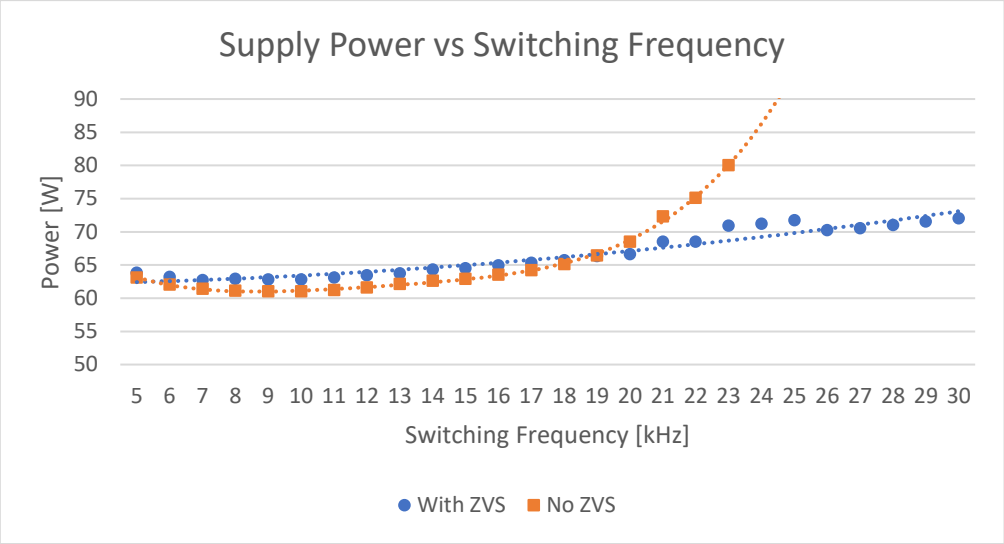


Fig. 70 – ZVS inverter power draw with and without Aux switches enabled.

From this figure we can see that below a certain frequency, where the switching losses are lower than conduction losses, the ZVS inverter is less efficient because some power is wasted to operate the Aux switches in a region where their contribution is not required. When the switching frequency rises above the threshold where the switching losses are higher than the conduction losses, the ZVS behaviour of this prototype gives clear efficiency advantage, enabling the prototype to run at higher frequency despite being composed of all classic silicon mosfets.

4 Electric Motor

4.1 Introduction

The last activity carried out during my PhD was the design of an electric motor to be used on the Formula Student Electric that the UniBo Motorsport team will use for the 2020 season.

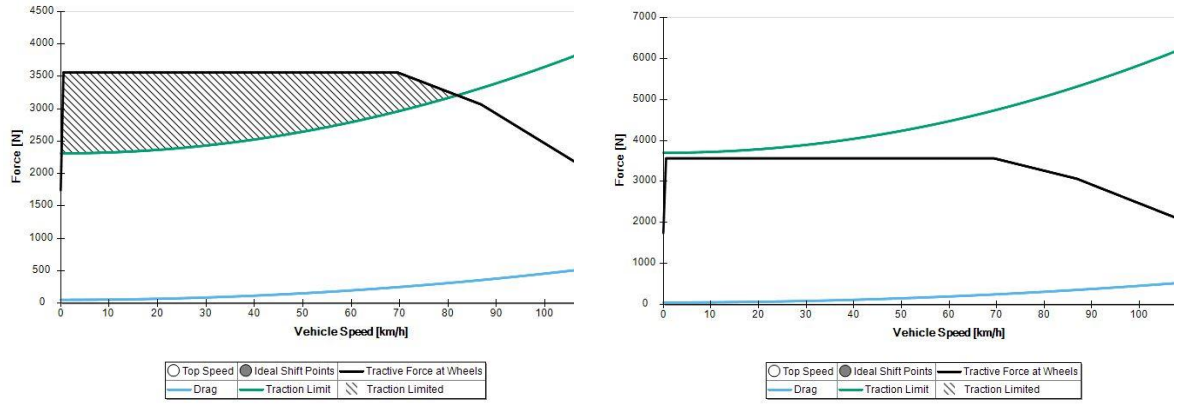
The Formula Student Electric rules [43] are much more permissive than the Motostudent rules [15], in particular:

- "EV.1.3.1 The maximum power **drawn** from the Accumulator must not exceed […] **80 kW."**
- "EV.1.3.2 The maximum permitted voltage that may occur between any two points must not exceed **600 V DC. "**
- "EV.2.1.1 Only electrical motors are allowed. Any type of electrical motor is allowed. The number of motors is not limited. "
- "EV.2.1.2 The rotating part of the motor must be contained within a structural casing."
- "EV.2.1.3 The motor casing may be the original motor casing, a team built motor casing or the original casing with additional material added to achieve the minimum required thickness […]

Since the number of motors is not limited that means any vehicle configuration can be used: single motor rear wheel drive, two motor rear wheel drive (RWD) or all wheel drive (AWD). The first solution was immediately discarded because it employs a differential, increasing the overall mass of the vehicle and also because it makes impossible to use torque vectoring algorithms.
To choose between the RWD or AWD configuration a preliminary evaluation was based on the fact that the 80kW maximum power is split respectively between 2 or 4 tires. Considering the following approximations:

- Vehicle mass equal for both the AWD and RWD cases and set to 250kg driver included.
- Motor to wheel gear ratio set to 14 (common value among all the competitors)
- Constant wheel radius
- Typical torque/power characteristic of a PMSM motor with 80kW max power.
- Longitudinal friction coefficient constant and set to $\mu_{max} = 1.87$ [44]
- Estimated aerodynamic drag and load

Thanks to a specialized software [45]capable to estimate the traction limit given the aforementioned parameters it was possible to obtain the traction limit for both the hypothetical configurations. This is visible in Fig.71



RWD vehicle AWD vehicle

Fig. 71 – Traction limit comparison for RWD and AWD vehicles

As visible from the figure, having one motor per wheel is beneficial since given the theoretical tires performances and the motor power curve we never hit the Traction limit. Despite the huge simplification in defining the problem, the outcome is a clear advantage of the AWD configuration.

A detailed simulation has been carried on using OptimumLap. This is a laptime simulation software specialized for racecars and it aims to simulate a full lap for a given vehicle, taking into account the entire vehicle dynamics.

A 75m acceleration test has been simulated for both the RWD and AWD scenarios and the results are summarized in Fig.72

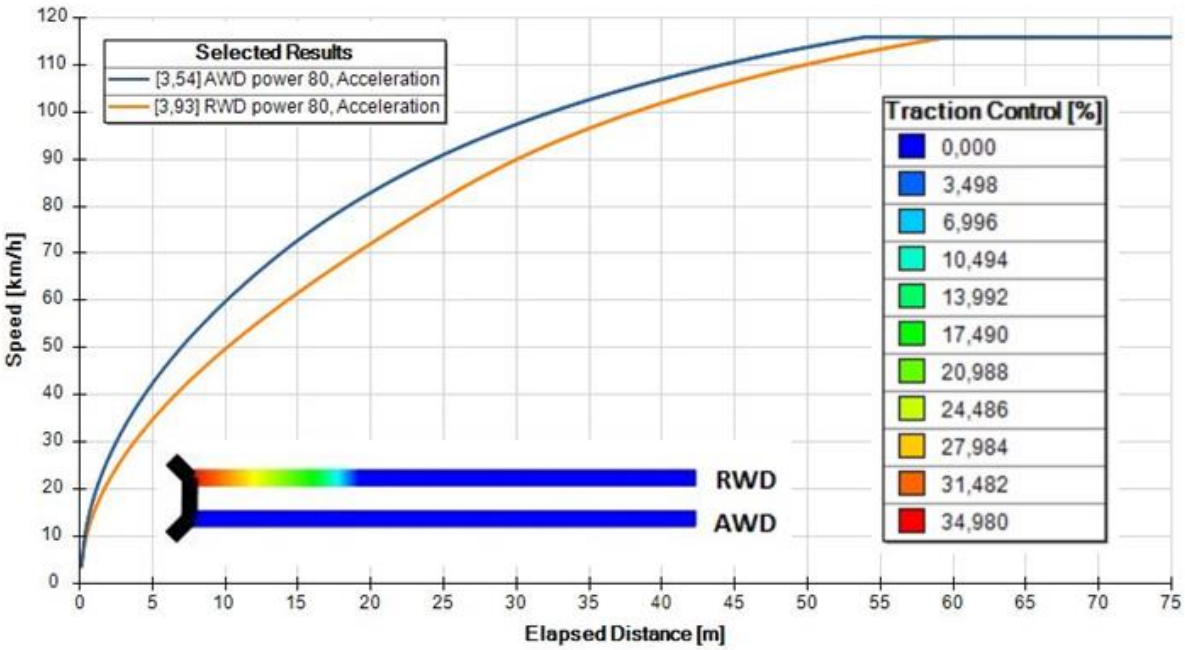


Fig. 72 – Acceleration performance comparison between RWD and AWD vehicle

Also OptimumLap simulations confirms the benefit of the AWD vehicle, and the performance increase can be attributed to capability of using all the 4 wheels to transfer torque to the ground without hitting the traction limit of the tires. This is clearly visible from the traction control request that is zero for the entire duration of the acceleration.

Despite the increased complexity of an AWD design, it has been chosen thanks to the superior potential performances compared to other solutions.

Because of the 600V limit, which represents a safety issue and a consistent design challenge, it was chosen not to design, at least for the very first car, the windings and then the magnetic parts of the motor. That means we have to select an off-the-shelf motor posing more constraints on the geometrical dimensions of the whole assembly and the cooling requirements.

To overcome this limitation we have selected a solution from Fischer Elektronik GmbH [46]. This company only supplies motor rotor and stators assembled on custom shaft and housing provided by the customer. This solution gives us the ability to design our own shaft and motor housing to optimize the geometrical dimensions and cooling circuit of the motor to our needs.

The electrical specifications of the motor are then imposed by the manufacturer and summarized in the following table and in Fig.73. Since the electrical part of the motor is given we will then concentrate on the mechanical design only.

Fischer TI085-052-070-04B7S-07S04BE2 motor data			
	Symbol	**Unit**	**Value**
Peak Torque	TPeak	Nm	29,1
Peak Current	IPeak	Arms	61
Speed at Peak Torque	nPeak	rpm	11600
Peak Power	PPeak	W	35366
Winding Losses[1] / *Total Losses*[1,2]	PDPeak	W	1843 *2167*
Torque Constant	kt	Nm/A_{rms}	0,492
BEMF Constant (Phase - Phase)	k_e	V_{rms}/(rad/s) V_{rms}/rpm	0,296 0,031
Motor Constant	km	Nm/√W	0,447
Idle Speed	nidle	rpm	13650
max. Speed (Fieldweaking)	nmax	rpm	20000
max. Frequency (Idle/*Fieldweaking*)	fmax	Hz	910 *133*
DC Bus Voltage	UDC	VDC	600
Ø Resistance per Phase (Winding only)	RPh20	Ω	0,126
Ø Inductance per Phase (Winding only)	LPh	mH	0,393
electr. Time Constant τ=L/R	τel	ms	3,11
Number of Polepairs	n		4
Winding Connection			Star

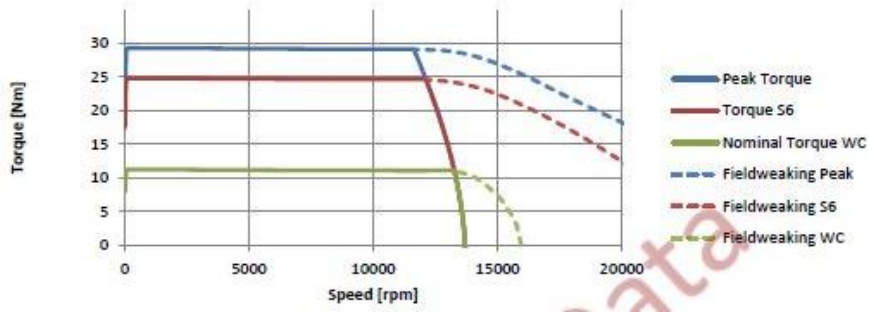


Fig. 73 – Fischer motor estimated torque

4.2 Requirements

It is common for this kind of vehicles that are using an AWD configuration to have in-hub motors. This gives a major weight and efficiency advantage by removing the need of driveshafts. The downside is that the motor and the associated gearbox have to be considered as unsprung masses degrading the dynamic performances of the chassis. This is mitigated by the typical characteristics of a Formula Student track circuit which is generally very flat and bumpless.

The decision was then do design in-hub motors, with epicyclic gearbox to obtain maximum compactness in the axial direction. From the laptime simulator the optimal gear reduction ratio has to be between 13 and 14. This gear ratio is easily obtainable in the available space by using a single stage epicyclic gearbox. A schematic layout of the design is represented in Fig. 74. To optimize compactness of the overall assembly, the motor itself will be the cover of the gearbox from the vehicle side.

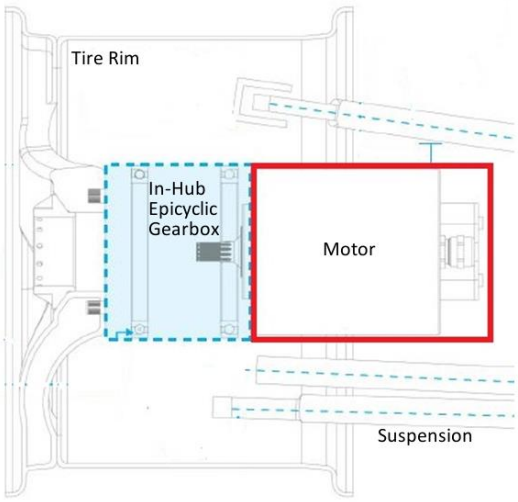


Fig. 74 – Typical layout of an in-hub motor assembly

The design of this motor is dominated by the cooling requirements prescribed by the stator manufacturer. It states that the maximum coolant inlet temperature must be 40°C with a maximum coolant temperature increase of 5°C, meaning the maximum coolant output temperature should never surpass 45°C. To meet this requirement an extensive study of a cooling circuit geometry has been performed through CFD simulations.

4.3 Mechanical design

The starting point in the mechanical design of this motor is a datasheet from Fischer [XX], reported in Fig. 75, stating the minimum mechanical features that the stator and rotor assemblies must satisfy for a correct manufacturing process.

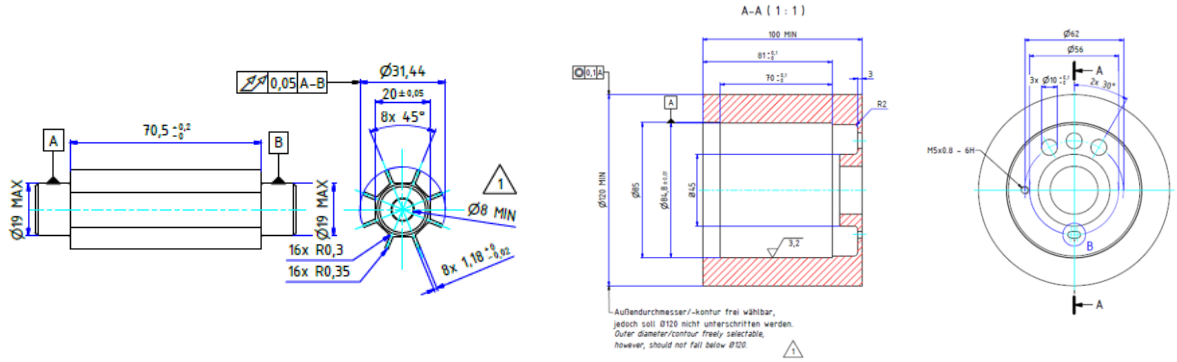


Fig. 75 – Mandatory features for the motor shaft and housing

The motor shaft is essentially the same design prescribed by Fischer with the addition of the bearing seats, a spline coupling for the connection to the sun gear of the epicyclic gearbox and on the opposite side a slot has been added to accommodate an adapter that will allow the connection of an Hall effect encoder or a magnetic resolver. Such devices are mandatory in a PMSM motor because the inverter needs to know with precision the real time position of the rotor for the correct execution of the FOC (Field Oriented Control) algorithm [47] [48].

The material used for the shaft must be nonmagnetic otherwise it will interfere with the rotor magnets. Recommended materials are 42CrMo4 or Ti6Al4V. To obtain minimum weight titanium was chosen. The final geometry, visible in section in Fig. 76 has been verified through FEM analysis using NX Nastran, modal analysis and fatigue calculations. The resulting safety factor is above 3, which is relatively high for motorsport application but given the lack of prior experience in using such motors and the high cost of the final assembly it was deemed reasonable to have some additional safety margin.

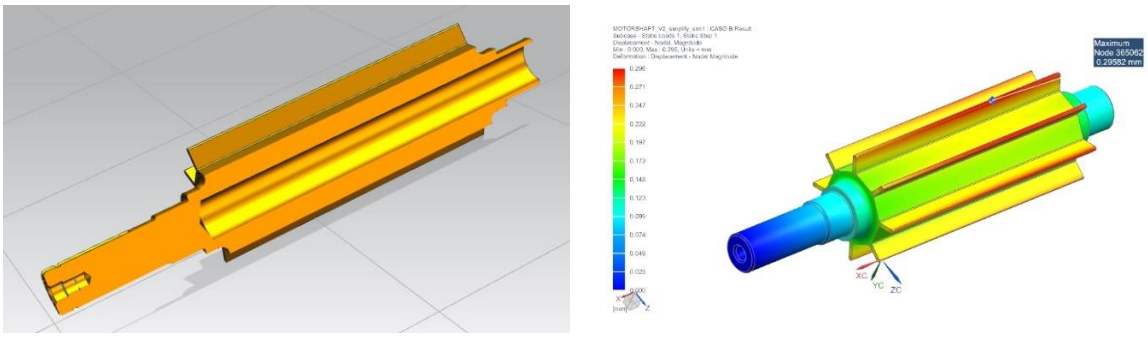


Fig. 76 – Section view and FEM analisys of the motor shaft

Regarding the bearings, single track steel bearing with Si_3N_4 ceramic balls have been chosen.

Because the high speed of this motor, ceramic bearings are the best choice to extend the bearing life. Other desirable benefit is that the balls are non conductive and then eventual parasitic currents flowing from the stator to the rotor shaft are eliminated. To choose the bearing it was considered as a worst case scenario that the radial force is the absolute maximum force generated by the stator on a single magnet, not balanced by the equal force generated from the other side of the rotor during normal operation. From the laptime simulation an average speed of 11000rpm has been found and given the estimated radial load of 0.8kN, the selected bearing (6001-2RSLTN9/HC5C3WT) should

have a lifetime of 470hrs which is comfortably above the amount of time this motor will run during an entire racing season.

The other component that has been designed is the stator case. It's main purpose is to provide all the mechanical features required to fix the motor to the car chassis, act as a bearing support and most important, extract the heat produced by the stator. For its good thermal conductivity and good machining properties, aluminium EN AW 6061 has been chosen.

This component is split in two parts: a main body, containing the actual stator and an endplate that will close the open side of the motor and provide mechanical fixing to the epicyclic gearbox.

The only relevant stresses in this component are the deformation of the main body due to the stator to be press-fitted into it and the stresses on the endplate because it will carry all the torque generated by the motor. FEM simulation has been performed for this components as well and the result is reported in Fig. 77.

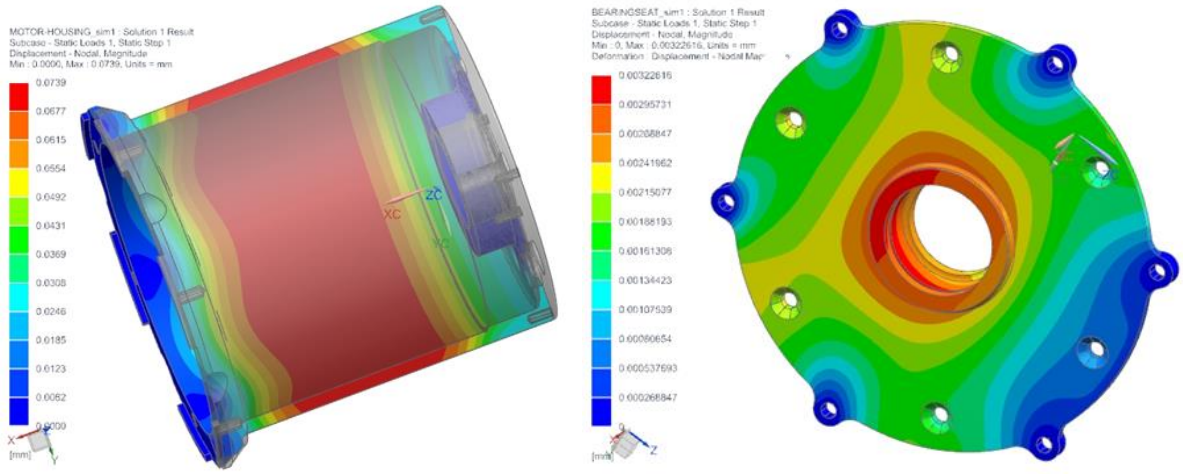


Fig. 77 – FEM analisys on the main body and endplate

From those simulations we can conclude that the stresses on these two components are negligible.

The final result of this work is a complete motor which is now in production. An exploded view and a section view of the entire motor assembly is reported in Fig.78.

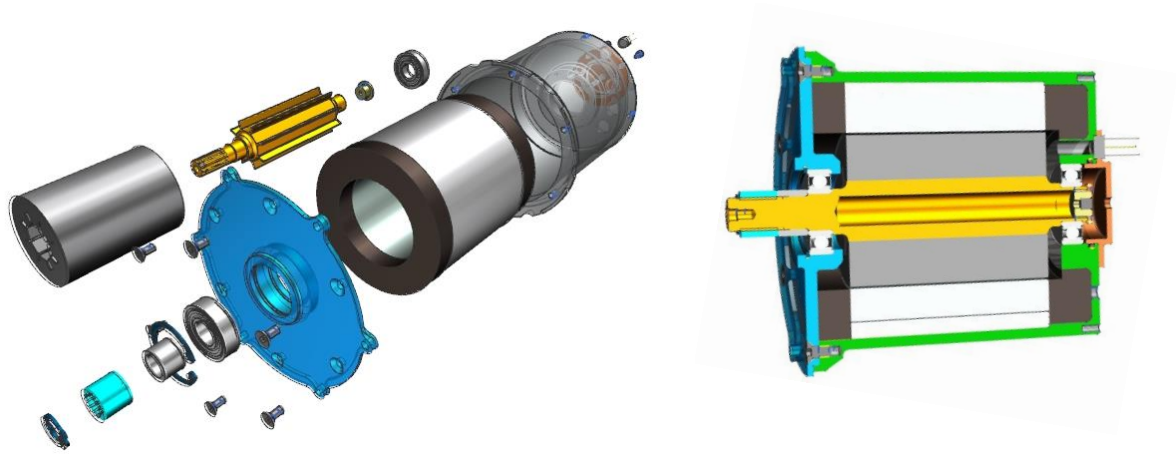


Fig. 78 – Exploded view and section view of the motor assembly

4.4 Cooling

For a PMSM motor of such high power density, cooling is mandatory. Despite the stator windings can withstand extremely high temperatures, the limit in the maximum operating temperature is given by the magnet temperature. Typical material for magnets in such motors is NdFeB and top grade magnets made of such material will permanently demagnetize if operated above 180°C. This limit is considered in free air, but when the motor is in operation the magnetic field generated from the stator further decreases this limit. For this motor, the manufacturer recommends a maximum coolant temperature of 40°C and a maximum coolant temperature increase of 5°C. Also the maximum power loss in the stator and rotor are given and it amounts to 2.2kW maximum. The value used in the following simulations has been scaled down by the average duty cycle of the motor during the race.

The cooling circuit will be machined directly on the outer surface of the main body, creating two square section spirals where the water can flow in opposite directions. This has two main benefits: average temperature of the housing will be more uniform and coolant inlet and outlet will be on the same side of the motor. The cooling ducts will be sealed by a plastic tube concentric with the motor, with o-rings on the two sides of the motor to prevent leakages. The proposed cooling circuit is visible in Fig. 79

Fig. 79 – Proposed cooling circuit, machined on the external surface of the motor main body

The cooling circuit geometry is the result of an extensive study through CFD simulation using Ansys software. The aim of this study was to find the best geometry that exhibits the minimum pressure drop while maintaining the prescribed 5°C ΔT between inlet and outlet. The final result of this optimization process is reported in Fig. 80.

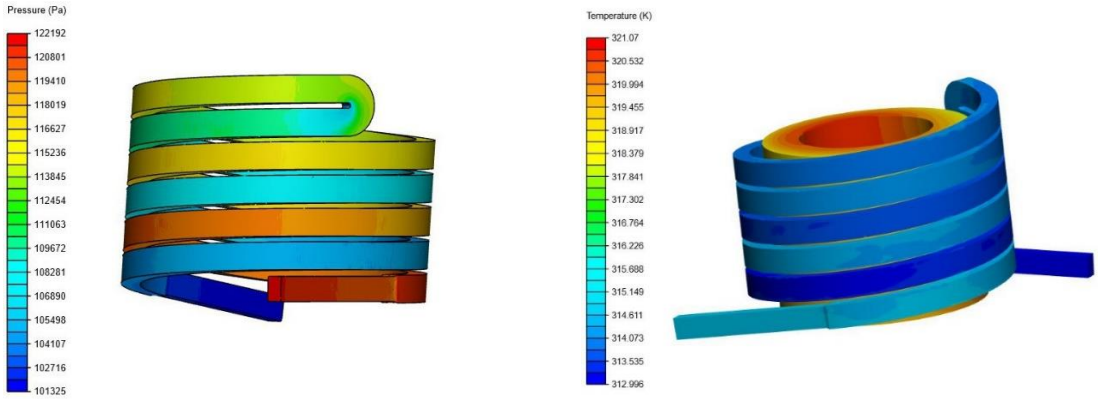


Fig. 80 – CFD simulation of the pressure drop and ΔT in the motor cooling circuit

5 Conclusions

The thesis illustrates the principal activities carried out along my 3 years long PhD course, focused on the understanding and developing methodologies to design and produce key components for HEV/BEV powertrains. Those powertrains are always composed by at least one battery pack, at least one electric motor each one controlled by its associated inverter.

The first component analysed is the battery pack. Advantages and limitations of various state of the art lithium polymer cells chemistries have been analysed to find a method to select the best cell for a given mission. Then the selected cell was tested and modelled to develop a complete powertrain model that was later used to validate design choices during the development of this component. Several design challenges have been studied and solved, especially regarding efficient and lightweight packaging to hold the cells in place. Laser welding method and fixtures has been designed yielding to easy and efficient assembly. A dedicated BMS that does not require wiring looms has been designed for this battery pack.

Regarding the inverter, several inverter designs have been prototyped. Two of them are using Gallium Nitride mosfets, a novel technology that aims to increase the switching frequency and then consequently reduce the size of the DC Bus capacitor, which is the most volume consuming component in conventional inverters. One prototype was designed for low voltage operation (up to 110V) while the other was designed for high voltage operation (500V). Both inverters, despite being in an early stage of prototyping, confirmed the feasibility and the advantages of an automotive inverter using GaN mosfets. The third inverter uses a novel topology capable to achieve Zero Voltage Switching in any operational situation and it uses Silicon mosfets. The prototype shown that is possible to minimize the switching losses of Si mosfets and then it becomes practical to drive them at considerable higher frequencies.

Finally, the mechanical design for a PMSM electric motor has been presented. The electrical part of this motor is provided by a specialized company that will build such motor around custom designed shaft and enclosure. Particular attention has been paid to the cooling circuit, directly machined on the outside of the enclosure assembly because of the strict cooling requirements of the electrical part of that motor.

6. References

[1] D. Doyle, G. Cunningham, G. Early e J. White, «Lap Time Simulation Tool for the Development of an Electric Formula Student Car,» *SAE Technical Paper 2019-01-0163,* 2019.

[2] G. Caramia, N. Cavina, S. Patassa e L. Solieri, «Predictive NOx emission control of a Diesel-HEV for CO2 and urea consumption reduction,» *74th ATI national congress, Modena,* 2019.

[3] N. Cavina, G. Caramia, S. Patassa e M. Caggiano, «Predictive Energy Management Strategies for Hybrid Electric Vehicles: Fuel Economy Improvement and Battery Capacity Sensitivity Analysis,» *SAE Technical Paper 2018-01-0998,* 2018.

[4] G. Caramia, N. Cavina, M. Caggiano, S. Patassa e D. Moro, «Battery state of charge management strategies for a real-time controller of a Plug-in Hybrid Electric Vehicle,» *Energy Procedia,Vol. 148,* pp. 258-265, 2018.

[5] H. Duane, Brushless permanent magnet motor design, Magna Physics Pub, 2006.

[6] M. M. Datasheet. [Online]. Available: https://sep.yimg.com/ty/cdn/yhst-129399866319704/ME1507MotorData.pdf.

[7] F. Saidani, F. Hutter, R.-G. Scurtu, W. Braunwarth e J. Burghartz, «Lithium-ion battery models: a comparative study and a model-based powerline communication,» *Advances in radio sciences 15, 83–91,* 2017.

[8] S. Madani, E. Schaltz e S. Knudsen Kær, «An Electrical Equivalent Circuit Model of a Lithium Titanate Oxide Battery».*Batteries 2019, 5, 31.*

[9] G. Caramia, N. Cavina, A. Capancioni, M. Caggiano e S. Patassa, «Combined Optimization of Energy and Battery Thermal Management Control for a Plug-in HEV,» *SAE Technical Paper 2019-24-0249,* 2019.

[10] F. Azidin, M. Hannan, M. Azah e A. G. Zamre, «Single and multi-sources energy sizing for electric vehicle: A case study.,» *Journal of Telecommunication, Electronic and Computer Engineering. 7,* pp. 117-122, 2015.

[11] Batteryuniversity.com, «BU-205: Types of Lithium-Ion,» 2016. [Online]. Available: https://batteryuniversity.com/learn/article/types_of_lithium_ion.

[12] X. Chen, W. Shen, T. T. Vo, Z. Cao e A. Kapoor, «An overview of lithium-ion batteries for electric vehicles,» *10th International Power & Energy Conference (IPEC),* pp. 230-235, 2012.

[13] Y. Miao, P. Hynan, A. von Jouanne e A. Yokochi, «Current Li-Ion Battery Technologies in Electric Vehicles and Opportunities for Advancements.,» *Energies 12, 1074,* 2019.

[14] N. Instruments, «CompactRIO Controller,» [Online]. Available: http://www.ni.com/it-it/shop/select/compactrio-controller.

[15] M. E. Foundation, «Motostudent Rules 2020,» [Online]. Available: http://www.motostudent.com/assets/files/MS1920_Regulations_V4_ENG.pdf.

[16] T. Solchenbach, P. Plapper e W. Cai, «Electrical Performance of Laser Braze-Welded Aluminum-Copper Interconnects,» *Journal of Manufacturing Processes, Volume 16, Issue 2,* pp. 183-189, 2014.

[17] A. Devices, «LTC6804 Datasheet,» [Online]. Available: https://www.analog.com/en/products/ltc6804-1.html.

[18] D. Andrea, Battery Management Systems for Large Lithium Ion Battery Packs, Artech House, 2010.

[19] «B-Foam Datasheet,» [Online]. Available: https://www.bcomp.it/wp-content/uploads/2014/10/schede_tecniche-IT.pdf.

[20] «SPAL Electric fans catalogue,» [Online]. Available: https://www.spalautomotive.it/it/elettroventilatori-assiali.

[21] B. Wu e M. Narimani, High-Power Converters and AC Drives, 2nd Edition, Wiley-IEEE Press, 2016.

[22] E. Gurpinar e A. Castellazzi, «Single-Phase T-Type Inverter Performance Benchmark Using Si IGBTs, SiC MOSFETs, and GaN HEMTs,» *IEEE Transactions on Power Electronics, vol. 31, no. 10,* pp. 7148-7160, 2016.

[23] S. Chowdhury, Z. Stum, Z. Da Li, K. Ueno e T. P. Chow, «Comparison of 600V Si, SiC and GaN Power Devices,» *Materials Science Forum, Vols. 778-780,* pp. 971-974, 2014.

[24] B. Ozpineci e L. M. Tolbert, «Comparison of wide-bandgap semiconductors for power electronics applications».*Oak Ridge National Laboratory.*

[25] N. Kaminski e O. Hilt, «SiC and GaN Devices - Competition or Coexistence?,» *7th International Conference on Integrated Power Electronics Systems (CIPS),* 2012 .

[26] J. Worman e Y. Ma, «Thermal Performance of EPC eGaN FETs,» *Efficient Power Conversion Corporation, Application Note,* 2011.

[27] J. Strydom, D. Reusch, S. Colino e A. Nakata, «Using Enhancement Mode GaN-on-Silicon Power FETs (eGaN® FETs)».*Efficient Power Conversion Application Note.*

[28] A. Lidow e M. De Rooij, «eGaN® FET Electrical Characteristics».*Efficient Power Conversion Application Note.*

[29] Infineon Application Note, «Some key facts about avalanche,» 2017.

[30] N. Massey, «Taking the heat and leads out of high power designs,» *EETimes,* May 2016.

[31] GaN Systems, «Thermal Design for GaN Systems' Top-side cooled GaNPX®-T packaged devices,» 2018.

[32] Sevcon, «Sevcon Gen4 Motor Controller Datasheet,» [Online]. Available: http://www.sevcon.com/products/low-voltage-controllers/gen4/.

[33] Efficient Power Conversion, «EPC2034 Datasheet,» [Online]. Available: https://epc-co.com/epc/Portals/0/epc/documents/datasheets/EPC2034_datasheet.pdf.

[34] D. Reusch, «Effectively Paralleling Gallium Nitride Transistors for High Current and High Frequency Applications,» Efficient Power Conversion application note, 2016.

[35] D. Reusch, «Optimizing PCB Layout,» Efficient Power Conversion application note, 2019.

[36] A. Lidow e J. Strydom, «eGaN® FET Drivers and Layout Considerations,» Efficient Power Conversion applicatio note, 2016.

[37] GaN Systems Application Guide, «Design with GaN Enhancement mode HEMT,» 2018.

[38] G. Systems, «GS66516T Datasheet,» [Online]. Available: https://gansystems.com/wp-content/uploads/2018/04/GS66516T-DS-Rev-180422.pdf.

[39] Infineon Technologies, «GaN EiceDRIVER™ product family Datasheet,» [Online].

[40] D. Sadik, L. Colmenares, G. Tolstoy, D. Peftitsis e M. Bakowski, «Short-circuit protection circuits for silicon-carbide power transistors,» *Transactions on Industrial Electronics, vol 63, no.4,* pp. 1995-2004, 2016.

[41] S. M. e B. J., «Selecting film bus link capacitors for high performance inverter applications,» *IEEE International Electric Machines and Drives Conference ,* 2009.

[42] K. Chao e C. Liaw, «Three-phase soft-switching inverter for induction motor drives,» *IEE Proceedings - Electric Power Applications, Vol.148, Issue 1,* 2001.

[43] FSG, «Formula Student Rules 2020,» [Online]. Available: https://www.formulastudent.de/fileadmin/user_upload/all/2020/rules/FS-Rules_2020_V1.0.pdf.

[44] M. Candeloro, Studio sperimentale sulla resistenza all'avanzamento di una vettura FSAE, Bologna, 2014.

[45] OptimumG, «OptimumLap - Vehicle simulation tool,» OptimumG, [Online]. Available: http://www.optimumg.com/software/optimumlap/.

[46] Fischer-Elektromotoren, «Torque motors inner rotor catalogue,» [Online]. Available: https://fischer-elektromotoren.eu/products/torque-motors-inner-rotor/.

[47] J. Simanek, J. Novak, O. Cerny e R. Dolecek, «FOC and flux weakening for traction drive with permanent magnet synchronous motor,» *IEEE International Symposium on Industrial Electronics,* 2008.

[48] M. A. Bevilaqua, A. Nied e J. d. Oliveira, «Labview FPGA FOC implementation for synchronous Permanent Magnet Motor Speed Control,» *11th IEEE/IAS International Conference on Industry Applications,* 2014.

[49] E. Jones, P. Wiliford e F. Wang, «A fast overcurrent protection scheme for GaN GITs,» *IEEE Wide Bandgap Power Devices and Applications,,* 2016.