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# RF Circuits and Systems Design and Technologies Enabling IoT Applications

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# Abstract

Internet of Things (IoT) is the paradigm used nowadays to summarize what is expected form the fourth industrial revolution (Industry 4.0) that is the connectivity of a huge number of "smart" objects disseminated in dissimilar scenarios. This concept is foreseen for practically any possible application domain: from home to transportation, from industry plants to health care, and for space monitoring. Long-term and self-sustainability of these smart thinks (people, objects, tools, etc.) becomes the most relevant aspect for the implementation of such a complex vision. In this framework, my PhD activities have been concentrated. The common goal is to investigate advanced solutions for energy-aware systems and circuits cooperating to enable the IoT paradigm. In particular, I have studied, designed and experimentally demonstrated quite a few novel solutions able to overcome some of the energy limitations existing in IoT.

The first project I have developed is an energy-autonomous power relay node at 2.45 GHz that is able to harvest energy from ambient-available or from dedicated RF sources and either use it for operating the node or for supplying power to other nodes. Both a hybrid and a monolithic implementation of the relay system has been implemented.

Then I was dedicated to the design of a system enabling Wake-Up Radio (WuR) operation at ultra-low power. The ambitious goal of WuR

radios is to reduce the communication power consumption in Wireless Sensor Networks (WSN) and IoT. With this scope in mind, I have proposed and implemented a multi-band WuR architecture. The flexibility of using frequency diversity in WuR enables a more reliable and robust communication channel. From the source side, analytical and experimental studies have been carried out to define the optimum Power Optimized Waveform (POW) excitation to push the WuR sensitivity down to power as low as -65 dBm.

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# Abbreviations

| | |
|---|---|
| **APRN** | Autonomous Power Relay Node |
| **CAD** | Computer-Aided Design |
| **CF** | Coupling Factor |
| **CW** | Continuous Wave |
| **EM** | Electro-Magnetic |
| **EH** | Energy Harvesting |
| **FET** | Field-Effect Transistor |
| **GaAs** | Gallium Arsenide |
| **GaN** | Gallium Nitride |
| **GSM** | Global System for Mobile Communication |
| **HB** | Harmonic Balance |
| **HEMT** | High Electron Mobility Transistor |
| **IC** | Integrated Circuit |
| **ICW** | Intermittent Continuous Wave |
| **InGaP** | Indium Gallium Phosphide |
| **IoT** | Internet of Things |
| **ISM** | Industrial Scientific and Medical |
| **MIC** | Microwave Integrated Circuit |
| **MIM** | Metal-Insulator-Metal |
| **MMIC** | Monolithic Microwave Integrated Circuit |
| **MoM** | Method of Moments |

| | |
|---|---|
| **NFC** | Near-Field Communication |
| **N-LOS** | Non-Line-of-Sight |
| **OOK** | On-Off Keying |
| **OW** | Optimized Waveform |
| **PAPR** | Peak-to-Average Power Ratio |
| **PIFA** | Planar Inverted-F Antennas |
| **PDA** | Personal Digital Assistant |
| **PDK** | Process Design Kit |
| **POW** | Power Optimized Waveform |
| **pHEMT** | pseudomorphic-HEMT |
| **RF** | Radio Frequency |
| **RFC** | Radio Frequency Choke |
| **RFID** | Radio-Frequency IDentification |
| **RMS** | Root Mean Square |
| **RX** | Receiving |
| **SMD** | Surface Mounting Device |
| **SPDT** | Single Pole Double Throw |
| **SWIPT** | Simultaneous Wireless Information and Power Transfer |
| **TaN** | Tantalum Nitride |
| **TiWSi** | Titanium-Tungsten -Silicon |
| **TRD** | Time-Reversal Duality |
| **TX** | Transmitting |
| **UHF** | Ultra High Frequency |
| **VNA** | Vector Network Analyzer |
| **WuR** | Wake-Up Radio |
| **WuRx** | Wake-Up Radio Receiver |
| **WPT** | wireless Power Transfer |
| **WSN** | Wireless Sensor Node |

# Chapter 1

# Introduction

Internet of Things (IoT) is an emerging concept which is receiving a lot of interest from industries and researchers. This concept describes a structure where physical objects, each one equipped with a unique and identifiable communication system, are connected to the Internet and they can exchange information everywhere and in anytime. In this scenario long-term and self-sustainability operation of the devices are crucial points and, to date, they still are open items which strongly limit the IoT applications. In order to enable IoT applications even in a pervasive way, new systems and technologies needs to be developed with the objective of obtaining energy-aware devices able to maximize the longevity of the energy source (i.e. battery), or even able to self-sustain their operations. This work is divided in two parts: one dedicated to the optimization of power consumption in IoT devices, and the second one dedicated to the wireless power transfer between objects.

## 1.1 Motivation

The IoT concept used in this work is constituted by an intelligent infrastructure of devices equipped with radio transceivers connected to the

Internet. This way, it is possible to realize a pervasive distribution of Internet [1, 2] to any kind of physical object and this can potentially affect and improve many aspects of user's quality of life. Numerous applications of such a concept can be found such as home automation [3], healthcare [4], surveillance [5], transportation [6] and smart environments [7] (as summarized in Fig. 1.1). Starting from these necessities, many technological solutions have been developed and already available in the market.

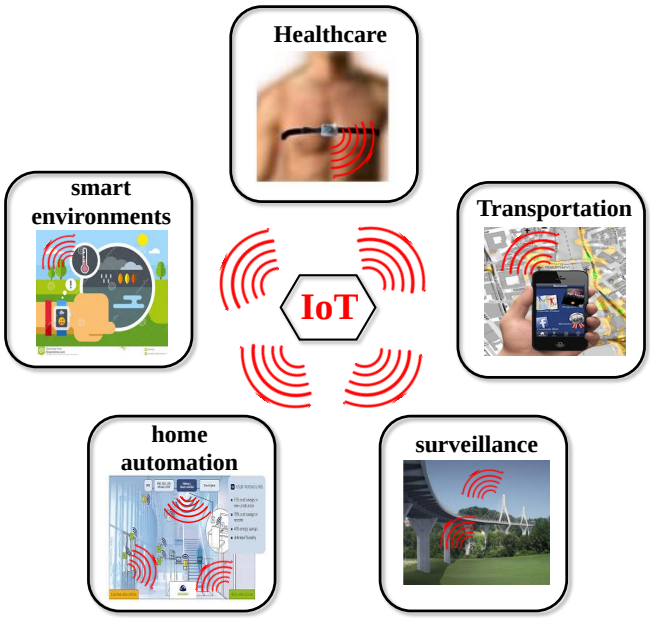


**Figure 1.1:** Examples of IoT applications.

Fig. 1.2 shows some example of these devices that are becoming more and more diffused in our everyday life such as Activity Trackers, Smart Watches and Smart Phones. A typical architecture of IoT devices includes sensors, radio receivers, digital processors and, last but not least, an energy source (i.e. lithium batteries). The major limited factor in making IoT strongly pervasive is associated to the difficulties in supplying adequate energy to the objects to operate within the IoT structure for long time (from few months to years) without compromising the de-

vice's quality of service. For this reason, it becomes very important to improve the efficiency of such devices and extending the node's lifespan connected to the IoT network.

To solve this problem and improve the efficiency, different approaches have been investigated in literature such as using efficient communication protocols [8], or designing optimized embedded batteries for long-term duration [9], and adopting low-power consumption radio transceivers [10]. However, all these solutions are still not enough to guarantee a continuous and long term operation of the devices. In addition, the adoption of batteries can limit the real diffusion of the IoT concept due to i) their dimension which dominates the devices size, and ii) their need of maintenance. Moreover, batteries can discourage the use of wearable devices for medical applications.


**Figure 1.2:** Examples of commercial IoT devices.

A recent technology trend able to provide a further energy source to the IoT nodes is the Energy Harvesting (EH) [11]. Practically, many energy sources are present in the environment such as Thermal, Solar, Vibration, and Radio Frequency. Scope of an energy harvesting system is to convert these sources into electric energy that can be used from the device itself (Fig. 1.3). The intensity of the aforementioned environmental sources depends on the presence of the corresponding energy source. As stated in [12], the more intense sources are solar (10–1000 $\mu W/cm^2$)

and thermal (20–1000 $\mu W/cm^2$). Less intense sources are the vibration and (50–250 $\mu W/cm^2$) and Radio Frequency (0.01–0.1 $\mu W/cm^2$). It can be noted the significant energy gap between RF sources with respect to the other ones .

Nevertheless, RF energy harvesting (RF-EH) is so far the most promising approach for the emerging IoT. In fact, RF-EH has a fundamental key property that other sources miss: it is wireless by definition. Thus, the energy is readily available in the form of electromagnetic (EM) waves and can be exploited everywhere and at any time.

Due to its importance, from some years researchers, and even the research group I am working with, are investigating solutions to develop intelligent and dedicated RF energy sources (also known as energy shower) able to provide on-demand the needed energy to the IoT nodes [13]. In this different application of the energy harvesting concept, the RF power is intentionally provided to the device and the available power levels are much higher than those stated in Fig. 2.3. A such approach is known as Wireless Power Transfer (WPT). The key benefit in using WPT systems is basically the knowledge of the source and receiver positions and their EM properties. This allows us to optimize the point-to-point link between a source and a receiver, maximizing the power that the node receives. As demonstrated in [14], intelligent beam-forming systems can be adopted to optimize the link in complex IoT scenarios. Of course, the transmissible power in WPT links is limited by the international regulations which defines the maximum transmitting power in standard communication systems.

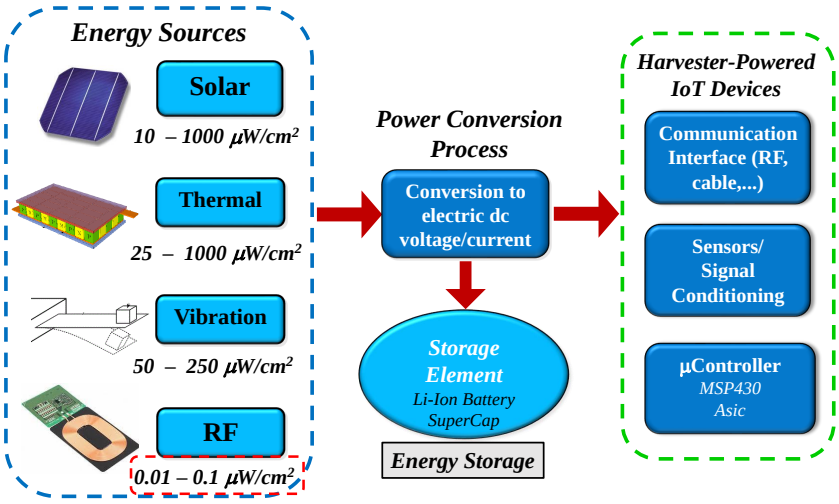


**Figure 1.3:** Schematic representation of a generic Energy Harvesting system.

In summary, we can divide the approaches helping to enabling IoT applications in two groups (Fig. 1.4):

1. **Optimize Power Efficiency**: Represents the set of techniques aimed to increase the on-board battery life by reducing the power consumption.

2. **Wireless Power Transfer**: Represents a further energy source for the device which can be requested on-demand and provided wirelessly.

Both these solutions can improve the longevity of the batteries. The first group belongs to some of the cited techniques [8, 9, 10]. However, an additional and promising approach is based on the Wake-up Radios (WuR). These radios are secondary radio transceiver (respect to the main radio, responsible for the data communications) implemented to monitor the channel condition so that the main radio can be turned off when there is no communication activity. This way, it is possible to strongly reduce the power consumption of the main radio, which, as well-known, represents the most power-hungry component in a communication node.

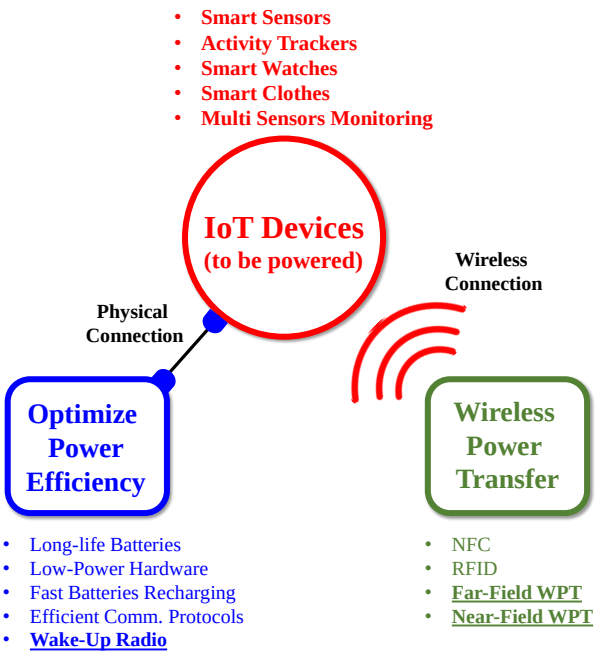


**Figure 1.4:** Techniques used to tackle the IoT energy limitations.

The second group provides a further approach to improve the system efficiency providing energy to the node. Potentially, such energy could also be enough to guarantee the self-sustainability of the device.

The possible implementations of wireless power transfer are Far-Field and Near-Field. The first one is based on electromagnetic wave and for this it is called radiative. The second one is based on inductive or capacitive coupling that can exist between closely-placed systems. In this case, a reactive magnetic or electric field is exploited for transferring the power and no radiation effects exist (non-radiative).

The aim of this work is to develop techniques, systems and circuits able to overcome the energy limitation in the IoT applications. The working areas of my PhD Thesis fall into the aforementioned groups depicted in Fig. 1.4. Specifically, the contributions to the IoT can be listed as follows:

- *Radiative Wireless Power Transfer*: Study and realization of a battery-less system able to accumulate and generate energy and operate as power relay node. Such a system allows passive devices to increase the operating range respect to the conventional approach.

- *Non-Radiative Wireless Power Transfer*: Realization of a WPT rechargeable system tailored for PDAs. In this work, the same antenna, designed for data communication purposes, is exploited for simultaneously realizing a WPT link.

- *Wake-Up Radio*: Development of techniques for increasing the flexibility and sensitivity of WuR radios. In particular, multi-band and Power Optimized Waveforms (POW) methods have been investigated for wake-up radios.

These points will be outlined in the next section where it will be described the scopes of the research activities made in this work.

Finally, this section concludes providing a summary of the main achievements obtained through three years in the Electromagnetic Group of the University of Bologna. As summarized in the section "achievements", during my activity I was able to present my work in a number of different scientific site, namely international conferences (*IEEE MTT-S International Microwave Symposium* and *Wireless Power Transfer Conference*) and journal (*IEEE Transaction on Microwave Theory* and *Techniques and Institute of Engineering and Technology*), resulting a total of 14 papers. As it will be described in the section dedicated to my PhD activities, I attended a number of international schools and student contests. In some of these contests, I also received awards. For instance, I was appointed as finalist in the student paper competition at *IMS 2015*, Phoenix. Then, I won the first prize in two student contests:

$5^{th}$ *Meeting of the EU-COST IC1301* (2015), and at *European School of Antennas* (ESoA), 2015.

Due to the quantity of materials published in this work, and considering the success that they have received, it has been decided to rework part of the available materials in writing this Ph.D. Thesis.

## 1.2 Research Objective

### 1.2.1 Radiative Wireless Power Transfer

In the radiative WPT field, this work concentrates on the investigation and development of a power relay node architecture. This relay node is a system which has the objective to receive and store energy from dedicated RF sources, and then using it either for specific operations of node itself or provide this energy to other devices closely-placed. The latter solution has the key benefit of overcoming the limitation due to the free space attenuation, such as the isotropic attenuation, multipath fading and non-line-of-sight (N-LOS) links.

This matter becomes even more important when passive systems operating at high frequency are involved. For instance, in RFID system, the most common tags operate at low frequency (868 MHz). At higher frequency (i.e. ISM bands: 2.45 GHz or 5.8 GHz), tags are at moment difficult to be diffused in the market because of the high attenuation. The aim of this work is to overcome such limitations introducing a power relay between reader and tags focusing on the 2.45 GHz band.

Two implementations of the relay node have been developed: the first based on a hybrid technology (MIC), and the second based on a monolithic technology (MMIC).

### 1.2.2 Non-Radiative Wireless Power Transfer

Considering the non-radiative WPT technology, this work aims to studying and implementing an architecture, embeddable in the common mobile phone, able to realize a bidirectional power transfer between mobile devices in order to realize an on-demand batteries recharging. This way, any device can be wirelessly recharged or be recharged, everywhere when it is requested. To this scope, a near-field WPT approach is used, and the innovative idea is to create the link by exploiting the existing antennas in the PDAs. Doing so, it is not requested to add further antennas into the system. Obviously, the antenna system is not primarily dedicated to WPT and this limits the maximum obtainable efficiency, but represents a solution to realize a WPT link without any additional antenna.

Of course, special attention must be given to the effects that the WPT link introduces in the far-field properties of the existing antennas, in order not to affect their normal operation.

### 1.2.3 Wake-Up Radio

The most energy-hungry part of IoT nodes is the radio transceiver due to its high power consumption. To enhance the communication efficiency, the main radio transceiver should be kept in sleep mode, most of the time, and be activated only when the related node is effectively interrogated. Among proposed energy-aware solutions, asynchronous-type transceivers with passive wake-up radio are very promising. Such RF systems have the role of continuously listening to the transmission medium and wake up the main radio upon detection of the incoming message. The aims of this work are:

**a)** Investigate solutions able to improve the robustness of the commu-

nication in WuR systems,

**b)** Improve the WuR sensitivity which determines the maximum communication distance.

## 1.3 Thesis Structure

To describe the different contributions introduced in the IoT field, this thesis is divided into two main parts. The first part will be dedicated to the systems developed in the WPT working area, and the second one will discuss the techniques introduced to improve the energy efficiency of the wireless sensor nodes (WSN). The thesis is organized as follows:

**Part I**: Wireless Power Transfer

- **Chapter 2:** First, it will be analyzed the power relay node architecture with the objective of demonstrating the advantages of this approach. The hybrid design and implementation of the relay node will be divided in sub-blocks and discussed. Then, it will be described the measurement set-up to experimentally validate the ability of the system to behave as a power relay node.

- **Chapter 3:** This chapter will demonstrate that a monolithic version of the relay node is attainable. After a brief overview about the adopted GaAs technology, the chapter will illustrate the entire general architecture of the MMIC and its sub-blocks. The design procedure of each sub-blocks will be deeply discussed. Finally, experimental results will be shown including the designed Test-Jig and measurement set-up.

- **Chapter 4:** It will be discussed the architecture of a WPT link established between two PDAs-like devices. Then, it will be illus-

trating the design procedure of the capacitive WPT link as well as the non-linear section. Finally, a detailed discussion on the measurement results will be provided.

**Part II**: Wake-Up Radio

- **Chapter 5:** This chapter shows the results obtained from our work in the WuR systems. First, it will be introduced the multi-band concept as a useful approach to obtain a frequency diversity. The designs procedure is then illustrated, and the experimental results shown. Thereafter, an approach based on power optimized waveforms (POW signals) is experimentally investigated to verify the effectiveness of such signals to improve the sensitivity of wake-up radios.

Finally, the thesis will conclude with a summary of the main results obtained during my PhD research.

# Chapter 2

# Autonomous Power Relay Node (APRN)

The work presented in this chapter was stimulated by a joint research issued by Prof. Alessandra Costanzo and Prof. Apostolos Georgiadis during a COST meeting. I was granted with a a Short Term Scientific Mission (STSM) from the COST Action IC1301 entitled "Wireless Power Transmission for Sustainable Electronics (WiPE)" to start the design of a circuit acting at the same time as a power harvesting and a power source module. The time spent abroad was 4 weeks from November $1^{th}$, 2014 to December $1^{th}$, 2014. The mission was carried out under the supervision of Prof. Apostolos Georgiadis and Ana Collado from Centre Tecnològic de Telecomunicacions de Catalunya (CTTC), in Barcelona, Spain.

The purpose of the mission was to develop an energy autonomous RFID system operating at 2.45 GHz (ISM band) based on a class-F oscillators/rectifier topology. Accordingly, this chapter will describe the development of a fully autonomous bi-directional circuit which starts in rectifying mode in order to harvest RF energy from intentional power

transmission, and after storing the necessary energy, is switched to oscillator mode to wirelessly power devices located in its proximity. The innovation of this works consists of an alternative approach for designing a 2.45 GHz class-F oscillator/rectifier, instead of a amplifier/rectifier approach, that in this way overcomes the need for external dc bias to operate, without degrading the performance of the two states (oscillator and rectifier). In fact, the circuit does not include a dedicated gate bias terminal, and thus eliminates the on-board batteries. This represents an important step with respect to solutions proposed in literature. In addition, the architecture developed and implemented in this chapter results to be a "true" autonomous bidirectional oscillator/rectifier system.
As far as the author knows, this is the only solution with these features available in literature.
The work done at CTTC was divided in tasks as follow:

- **Task 1**: Analysis and design of a class-F oscillator (1 week).
- **Task 2**: Optimization of the oscillator and rectifier as a unique system with high efficiency (2 weeks).
- **Task 3**: Test and debug of the system in both states to obtain the maximum efficiency (1 week).

This work was presented at the *International Microwave Symposium* (IMS) 2015 in Phoenix, Arizona [15]. On this occasion, the paper was also appointed as paper finalist in the framework of the Student context reaching a good score in the reviewer score. After this first version, a significantly extended work was published in the *IEEE Transactions on Microwave Theory and Techniques journal* [16]. In addition, from September $24^{th}$ to $25^{th}$ (2015), I attended at the *5th Meeting of the EU-COST IC1301* in Thessaloniki, Greece.

In such meeting, the relay node system was presented, and it won the first place of the student contest session as best poster.

This chapter is partially extracted by the published papers which contains a clear and complete base of the entire work. Thanks to the success of this project, the University of Bologna has decided to enroll myself in developing a monolithic version of the relay node by using a GaAs technology. Next chapter will be dedicated to give details on the MMIC version of the relay node.

The remainder of the chapter is organized as follows. Section 2.1 provides an overview of the system implementation and addresses the main issues to be solved for a successful autonomous power relay node operation. Section 2.2, 2.3 and 2.4 discuss the nonlinear design of the node: starting from the oscillator design, the rectifier topology is then derived; the two subsystem predicted performances are then experimentally validated. Section 2.5 describes the measurement set-up to validate experimentally the ability of the system to behave as an energy-autonomous power relay node. Section 2.6 drives the work conclusions.

## 2.1 System Overview

One of the issues in RF energy harvesting (RF-EH) solutions is the unknown and often variable RF link (rectenna location and polarization), which can threaten the effective use of energy-autonomous wireless systems. Several solutions have been pursued to reduce energy consumption [17, 18], and to enable high-efficiency harvesting capabilities that eliminate the need for battery replacement, thus reducing maintenance cost [19, 20]. In such scenarios, strategically located dedicated RF sources can help increase battery lifetime through wireless power delivery to sensors distributed in the source coverage area. A useful figure of merit

for far-filed wireless power transfer (WPT) links is the total RF-to-dc conversion efficiency, from the input of the transmitting antenna to the output of the receiver dc-dc converter [18]:

$$\eta_{TOT} = \eta_{RF-RF} \cdot \eta_{RF-DC} \cdot \eta_{DC-DC} = \frac{P_{RX}}{P_{TX}} \cdot \frac{P_{DC}}{P_{RX}} \cdot \frac{P_{ST}}{P_{DC}} \qquad (2.1)$$

This consists of the product of three power ratios, based on the RF power available at the transmitting antenna input port ($P_{TX}$), the RF power received by the rectenna ($P_{RX}$), the dc power converted by the rectenna ($P_{DC}$) and the dc power ($P_{ST}$) stored in a dc-dc converter emulating the rectenna optimum load. The transmit-to-receive RF efficiency RF-RF can be maximized by design of both transmit and receive parts of the WPT system only in the case when dedicated (intentional) RF sources are available.

For those devices that are located in areas where these sources would be less efficient, the proposed power relay node can act as an energy repeater. Such a node, capable of bidirectional operation, should be able to harvest sufficient power for its own operation, in addition to providing power to surrounding devices, as illustrated in Fig. 2.1. This figure represents the architecture studied and developed in this work with the objective to extend the powering range of passive tags.

The novelty of this chapter is the alternative circuit solution able to ensure a bidirectional functionality without the need for external batteries, by using the energy stored during the rectifier operation mode. As it will be illustrated, the same nonlinear circuit is used to perform the two operations, where two switches are simultaneously driven to position 1 for oscillator operation, and to position 2 for rectifier operation.

This represents the system developed in this work with the objective to extend the powering range of remote passive tags.

This chapter presents a novel circuit solution with bidirectional functionality and without the need for external batteries, by using the energy stored during the rectifier operation mode. The same nonlinear circuit is used to perform the two operations, where two switches are simultaneously driven to position 1 for oscillator operation, and to position 2 for rectifier operation (Fig. 2.1).
Other bidirectional systems have been proposed in the literature by exploiting the time reversal duality (TRD) [21]. In [22], a 2.4 GHz IMPATT diode based oscillating rectenna demonstrated 85% RF-to-dc efficiency as a rectifier and 1% dc-to-RF efficiency as an oscillator operating at 3 GHz. This publication highlights the challenges in maintaining a high efficiency in both operating modes as well as controlling the oscillation frequency and rectifier bandwidth. In [23], it is demonstrated that class-F RF power amplifiers exhibit comparable efficiencies and power levels when operated as self-synchronous rectifiers. In [24], this concept is extended to a 2.14 GHz 85% efficiency 10 W class-F-1 rectifier and a Fourier expansion-based theory for various classes of harmonically-terminated rectifiers (C, F, F-1) is developed. In [25] the concept is extended to 10 GHz in a GaN MMIC, and in [26] to a two-stage GaN MMIC. A reconfigurable mW-level class-E oscillator/rectifier in the UHF band is presented in [27]. Excellent conversion efficiencies (up to 75%) are obtained for both operating modes.

However, the limitation common to all these proposed solutions is that they are strictly dependent on the device bias conditions that need be supplied by external dc batteries. In addition, they have limited power operating range and sensitivity when they operates as rectifier.

This work aims to overcome all these limitations realizing a "true" efficient and autonomous bidirectional system.

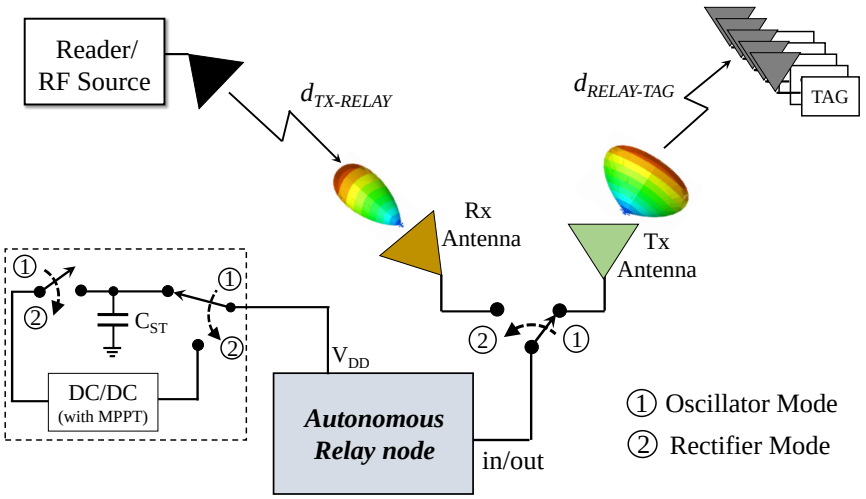


**Figure 2.1:** System representation of a bidirectional switchable energy autonomous power relay node: switch in state 1 corresponds to oscillator operating mode; switch in state 2 corresponds to rectifier operating mode.

Before to start with the system design, it is necessary to verify the effectiveness of the power relay node approach in a typical RFID scenario. A link budget analysis is presented considering two cases illustrated in Fig. 2.2:

**(a)** without relay node, as the conventional reader-tag scenario, and

**(b)** with relay node placed between reader and tag.

The link budget analysis of these two scenarios will allow us to confirm that thanks to the relay node presence an improvement in the reading range of tags can be attained. There are several factors that may impact the performance of a radio system such as available and permitted output power, available bandwidth, receiver sensitivity, antenna gains, and environmental conditions.

Due to the nature of the comparison that here we want to illustrate, the following link conditions are adopted:

- Frequency of operations 2.45 GHz.
- The reader in case **(a)** and **(b)** is the same (same antenna gain, output power, etc.).
- Directional antenna for the reader is adopted (6 dBi).
- Omnidirectional antennas are considered for the tags (2 dBi).
- The transmitting power is selected in order to respect the maximum power provided by international regulations (EIRP = 2 W).
- The propagation link is unobstructed and it operated with line-of-sight (LOS) conditions without fading effects.
- The sensitivity of he tags is selected equal to $-15$ dBm (typical for 2.45 GHz tags).

Similarly, specifications must be given for the relay node system. As it will be illustrated, the relay node proposed in this chapter features a receiver simulated sensitivity as low as $-8$ dBm, and a maximum transmitting power in oscillator mode of about $+14$ dBm. For this reason, in this link analysis we have adopted the following relay properties:

- Receiving relay antenna can be directive because the reader's position is well-know (10 dBi is assumed).
- Directional antenna is also assumed for the transmitting antenna of the relay (6 dBi, typical value for patch antennas).
- The receiver sensitivity of the relay node in receiver mode is assumed to be $-10$ dBi.
- The output power of the relay node is 25 mW.

Basically, the link budget consists in analyzing a RF link of the above defined cases by using the well-known Friis formula (note that, this formula is split in two paths for the relay node case):

- case (a)

$$P_{RX}(d) = P_{TX} \cdot G_{READER} \cdot G_{TAG} \cdot L_{PATH}(d) \tag{2.2}$$

- case (b)

$$P_{RX}(d_1, d_2) = \begin{cases} P_{TX} \cdot G_{READER} \cdot G_{RX-RELAY} \cdot L_{PATH}(d_1) \\ P_{TX} \cdot G_{TX-RELAY} \cdot G_{TAG} \cdot L_{PATH}(d_2) \end{cases} \tag{2.3}$$

Where:

- $P_{TX}$ =Reader transmitting power.
- $G_{READER}$ =Reader antenna Gain.
- $G_{TAG}$ =Tags antenna Gain.
- $G_{TX-RELAY}$ =Transmitting antenna Gain of the relay node.
- $G_{RX-RELAY}$ =Receiving antenna Gain of the of the relay node.
- $L_{PATH}$ =Propagation losses in function of the distance.
- $P_{RX}$ =Power received by the Tags.

Note that, the current analysis has the only objective of evaluating the activation distance of the tag. No considerations have been done in this work about the backscattering communication conditions.

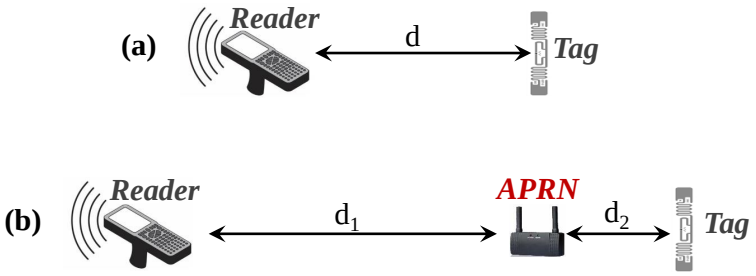


**Figure 2.2:** Link budget setup: (a) without relay node; (b) with relay node.

However, thanks to the high sensitivity of the available readers (–90 to –120 dBm), the limitation in the operating distance is only related to the tags activation rather than the backscattering communication. Fig. 2.3 shows the maximum reachable distances with and without relay node. According to the results, an improvement of 2 meters (about 50%) is achieved by using a battery-less relay node.

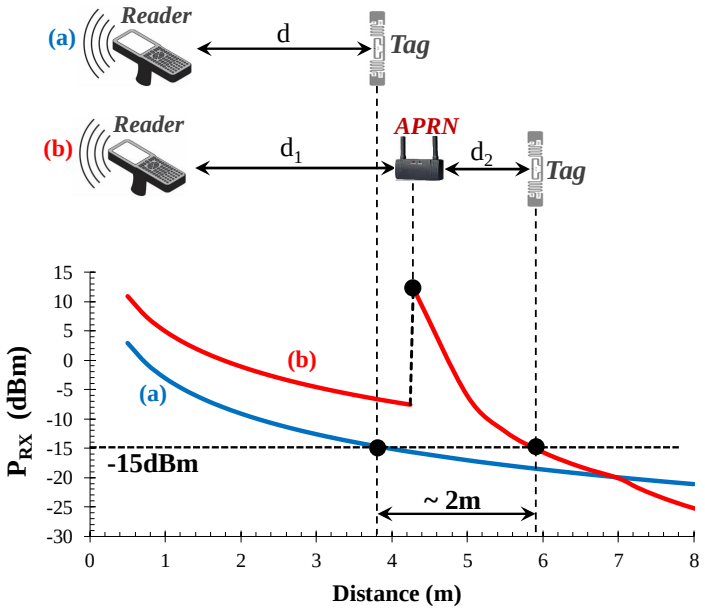


**Figure 2.3:** Power budget versus distance analyzed without (blue curve) and with (red curve) relay node.

This improvement is reached by taking advantage from the possibility of the relay node to optimize the point-to-point RF link between the

relay and the RF source, as well as the ability to regenerate a high-power CW tone at a distance far from the reader (about 4.3 meters in Fig. 2.3). Of course, in order to maximize the reading distance of the tags, the relay node position plays a crucial rule and it has to be carefully considered into the link optimization.

## 2.2 Oscillator Design and Results

As explained before, the key features of the relay node are the self-sustainability and bidirectionality. These are obtained through a sequence of two optimized operations: first the system is set in rectifying mode to harvest the dc voltage needed to bias the oscillator, and such power can be intentionally provided by well-known RF sources. For this purpose, some recent research has provided the design rules for transmitting ad-hoc RF signals that increase the RF-to-dc conversion efficiency of the receiver [28, 29]. The dc energy can be stored in a super-capacitor or managed for subsequent use. Secondly, the system can switch into transmitting mode using the harvested dc power to start oscillation. In this case, the generated power is intentionally radiated toward the interested area where are placed tags. In this context, the core component in a relay node system is the oscillator. This components must be efficient, robust to $V_{DD}$ variation and, as it will be illustrated, able to operate as rectifier without requiring complex biasing systems.

The main operating principle of the power relay node introduced in this work is the gate self-biasing of the MESFET [30]. By exploiting this feature, the oscillation start-up and rectifier operations can be accomplished with no need for dc biases. For this purpose, a medium power HEMT with weakly negative threshold voltage is chosen, which allow the device to start its operation from floating gate conditions in both

transmit and power-receive modes. This is done by using the same device and, most important, with the same conversion efficiency. In order to provide a clear description of the design procedure to be followed, it is introduced first the design of the self-biased oscillator, followed by the design of the self-biased rectifier obtained by using the time reversal duality (TRD) principle.

In order to understand the gate self-biasing mechanism, the HEMT transistor model is now analyzed. Fig. 2.4 shows the intrinsic GaAs FET models, including off-chip linear parasitic elements. It is a network composed of a voltage-controlled drain-source current source $I_{DS}\,(V_{GS}, V_{DS})$, a voltage-dependent gate-source capacitance $C_{SG}\,(V_{GS})$and a Schottky barrier diode gate-source current $I_{GS}\,(V_{GS})$.

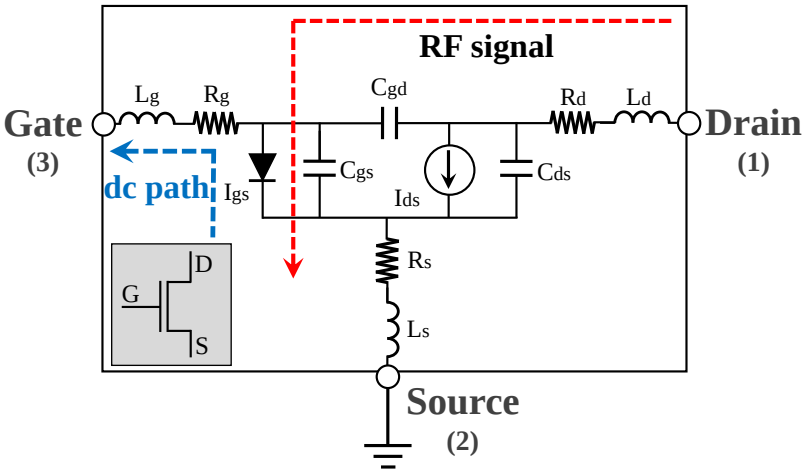


**Figure 2.4:** GaAs FET transistor model.

A source-grounded GaAs transistor with the gate terminal kept open in a dc manner (Fig. 2.4) can be self-biased without any external intervention. This can be explained with reference to the nonlinear FET model: as oscillation starts, the gate is floating and the RF signal flows into the gate-source junction through the feed-back drain-gate capacitance $C_{GD}$. Due to the Schottky-barrier rectifying property of the gate

junction, the RF gate-source voltage generates a dc gate current and the gate capacitance is charged to a negative voltage, thus obtaining a self-biased transistor. By using the self-bias mode operation, it is possible to build a GaAs oscillator, operable with a single positive dc bias voltage source. In addition, as it will be seen in the next section, the self-bias process is also valid in rectifier mode.

Once decided the biasing mechanism of the active device, an accurate study about the architecture of the oscillator has been done and Fig. 2.5 shows the final oscillator circuit topology (switches in State 1, which represents the oscillator configuration). The proposed architecture represents a 2.45 GHz Class-F oscillator with floating gate for the biasing. The architecture is composed of a Colpitts-like feedback, embedded in a linear sub-network that is optimized to ensure a class-F operation. In this work only the second harmonic has been terminated for obtaining a simple and compact network.

In order to maximize the dc-to-RF efficiency and to operate as oscillator, the drain impedance of the device must satisfy the Class-F harmonic termination condition at each harmonic [31], and simultaneously the feedback network must satisfy the oscillation conditions. For this reason, the HB optimization used in this work was envisioned to simultaneously meet the Barkhausen conditions and the maximum dc-to-RF oscillator conversion efficiency, in a suitable range of drain biases.

Ideally, the latter condition can be searched during the oscillator design by adding the following constraints to the ratio between the drain voltage and current harmonics to the design goals:

$$Z_h\left(V_{DDi}\right) = \frac{V_{DS,h}(V_{DDi})}{I_{DS,h}(V_{DDi})} = \begin{cases} < \varepsilon & if\ h\ is\ even \\ > M & if\ h\ is\ odd \end{cases} \tag{2.4}$$

$$V_{DDi} = V_{DD\,min}, ..., V_{DD\,max}$$

where $V_{DDi}$ is the drain bias spanning in the interval where oscillation condition is met, $V_{DS,h}$ and $I_{DS,h}$ are the drain voltage and current harmonic phasors, $\varepsilon$ and $M$ are low and high thresholds, respectively, h is the harmonic frequency index of the spectrum.

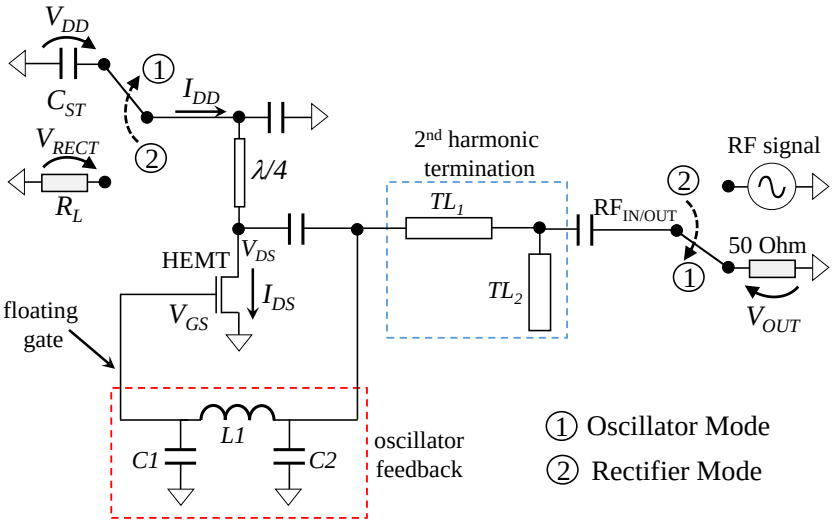


**Figure 2.5:** Circuit schematic of the bidirectional energy autonomous power relay node with $2^{nd}$ harmonic termination.

In the optimization, the dc component plus 64 harmonics are used, but condition (Eq. 2.4) has been applied only for $h = 2$. The active device is a JFET Renesas NE3509M04 with a negative threshold voltage of $-0.5$ V. As can be noted, the advantage of a negative threshold is two-fold:

1. the oscillation build-up is possible in the absence of a gate bias, that is, in floating-gate condition; and

2. the bias point for optimum conversion efficiency can be reached by gate self-biasing [30].

An analysis of the oscillator's transient has been carried out and the results of the oscillator start-up are summarized in Fig. 2.6. Initially, the drain and gate voltages are zero. During oscillation start-up, the self-bias mechanism drives the gate terminal to a negative voltage, the threshold voltage (or lower), thus allowing the oscillator to operate in a high-efficiency region with a reduced conduction angle.

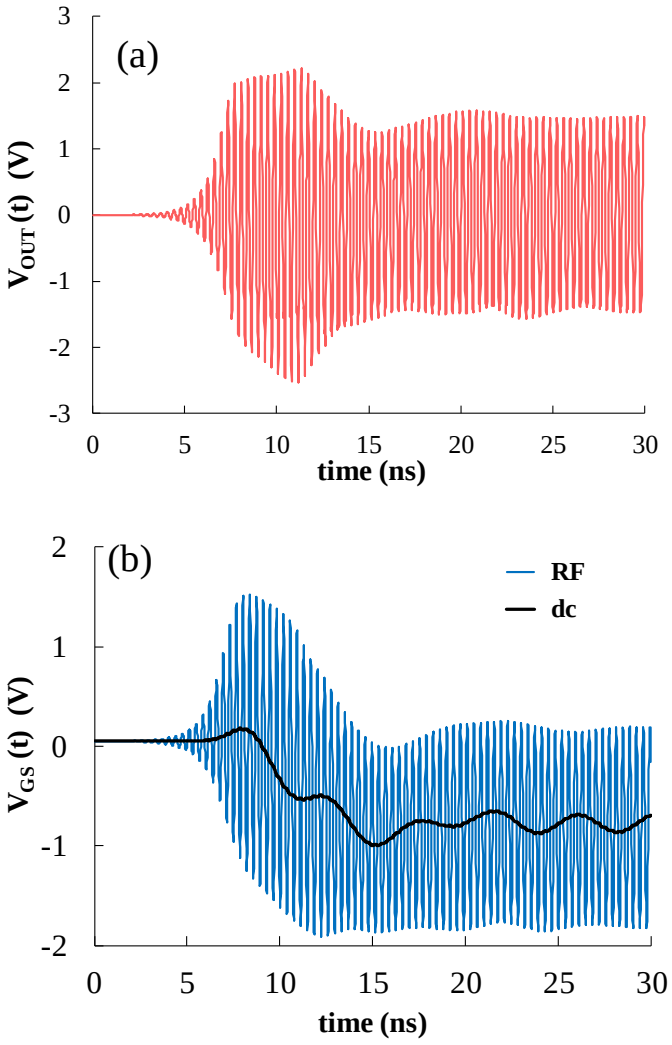


**Figure 2.6:** Simulated transient behavior of the oscillator: (a) oscillator output voltage waveform; (b) gate voltage waveforms.

This is highlighted in the same figure where the transient behavior

of the dc components of the gate-to-source voltage is superimposed with the time-variable waveform. The shorter the time needed to reach the oscillator class-F steady-state regime, the lower the power dissipated during the oscillator start-up, and the longer the oscillator steady-state operation. This is a critical aspect for energy autonomy of the system, since the energy stored during rectifier operation supports the oscillator steady-state regime.

Fig. 2.7 shows the transient behavior of the drain bias current $I_{DD}$, representing the transistor transition from a high-loss Class-A to a low-loss Class-F operation. In small-signal condition during start-up, the circuit requires a lot of drain current; after oscillations build-up, the gate terminal is negatively self-biased, and the dc drain current is thus minimized. The dc power consumed to extinguish the oscillator transient is minimized in the present design process and could be further reduced by using a device with shorter channel length.

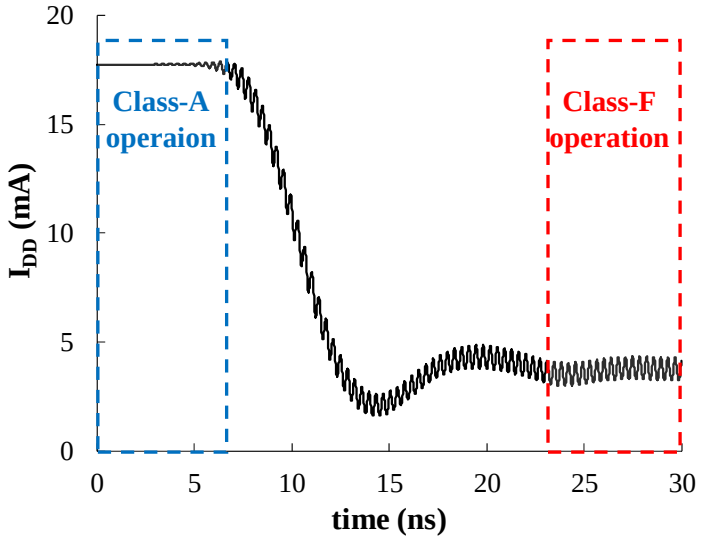


**Figure 2.7:** Simulated transient behavior of the oscillator bias current.

To verify by measurements the circuit in oscillator mode an external bias is used to provide drain polarization (switches of Fig. 2.5 are in

State 1). More details on the prototype physical dimensions will be given in the next sections. The oscillator efficiency is over 50% for the entire drain supply range starting from 2 V. The oscillator mode reaches a maximum dc-to-RF conversion efficiency of 52.5% at 4.2 V drain bias voltage and an output power of +14 dBm (Fig. 2.8). Note that, the dc-to-RF efficiency has a very flat behavior over drain voltage, highlighting the robustness of the proposed system.

Fig. 2.9 shows the oscillation frequency and gate voltage variations with the drain bias. A measured frequency shift of 60 MHz has been obtained over the entire $V_{DD}$ range. This is probably due to the inaccuracy of the FET model. In the measured dc-to-RF conversion efficiency and oscillator output power are compared to the simulated ones with varying drain supply voltage. The 15% overestimate in simulations is attributed to the HEMT nonlinear model accuracy.

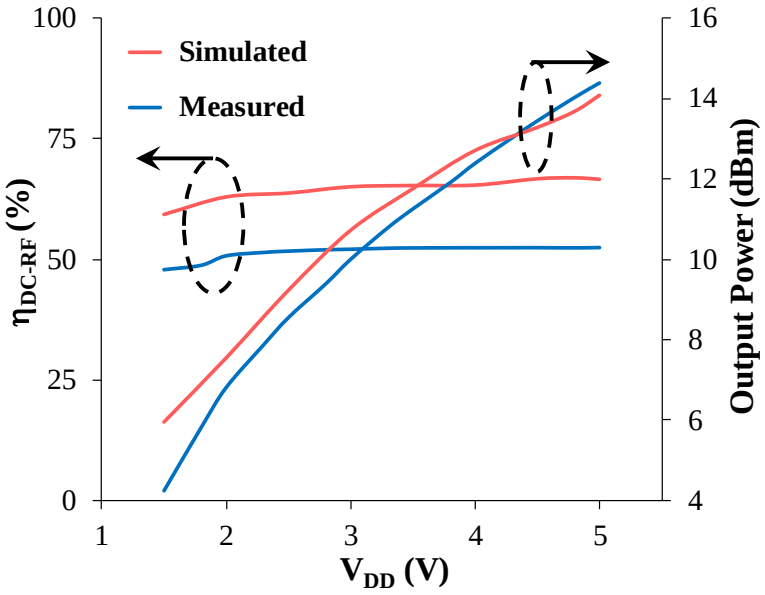


**Figure 2.8:** Measured and simulated oscillator dc-to-RF efficiency and output power with respect to drain bias.

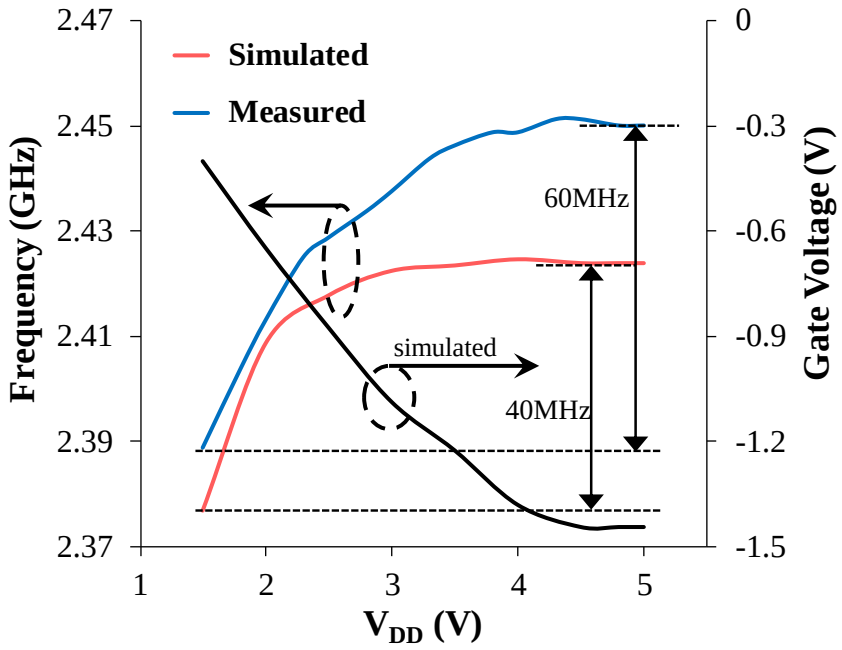


**Figure 2.9:** Measured and simulated oscillation frequency and simulated self-bias gate voltage as a function of the input RF power.

Fig. 2.10 shows the frequency spectrum of the oscillator, for a drain bias of 4.8 V. As expected, the second harmonic is about 50 dB below the other harmonics, confirming the class-F with second harmonic termination operation of the oscillator. The frequency spectrum is measured using an Agilent E4440A PSA spectrum analyzer with a resolution bandwidth of 3 MHz.

A further interesting measurement is the oscillator phase noise shown in Fig. 2.11. A phase noise of −80 dBc/Hz at about 100 kHz from the carrier is measured using the Agilent E4448A PSA vector signal analyzer with span 3 MHz and resolution bandwidth of 1 kHz: the instrument noise floors at frequency offsets of 10 kHz, 100 kHz, and 1 MHz are −116 dBc/Hz,−122 dBc/Hz, and −145 dBc/Hz, respectively. For the phase noise measurements, the circuit was biased with a4.5 V battery in order to eliminate supply noise.

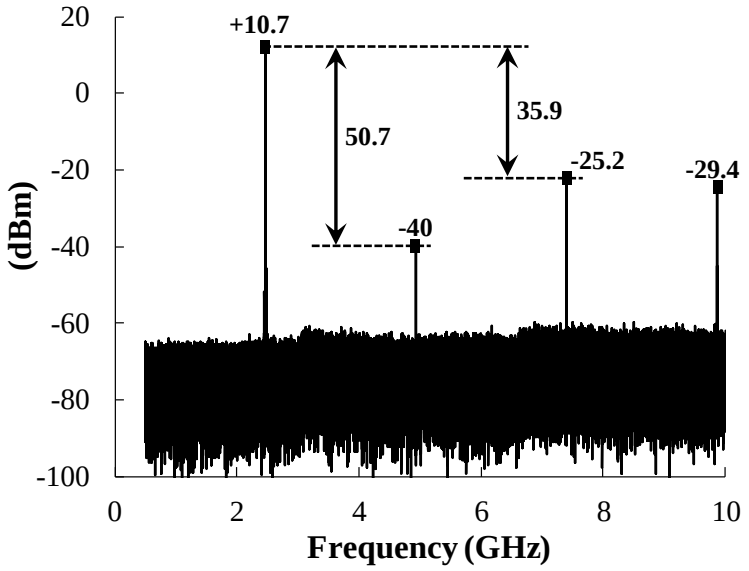


**Figure 2.10:** Measured oscillator output power spectrum.

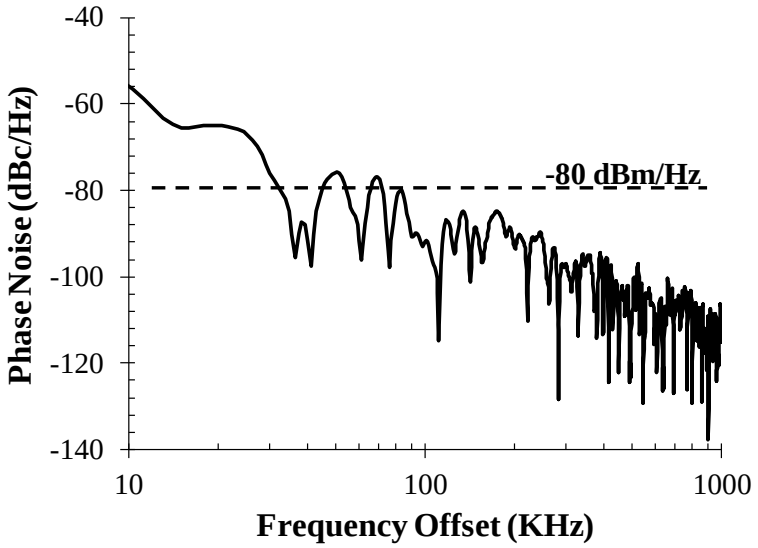


**Figure 2.11:** Measured phase noise of the oscillator circuit in oscillator mode.

## 2.3 Self-Bias Rectifier: Design and Validation

The goal of this section is to describe the design and the simulated performances of the oscillator used as rectifier. By means of the time reversal duality (TRD) principle [23], rectifiers with high RF-to-dc conversion efficiency can be derived in a straightforward manner from the design of high conversion efficiency amplifier [32] and oscillator [33]. In fact, in the TRD concept, the waveforms of one network are time reversed with respect to their counterparts in the dual network. This principle is widely applicable throughout power electronics for designing system able to reverse the power flow. Thanks to this theory, a general design method for amplifiers can also be applied for rectifier design preserving the system efficiency in both the operation modes. However, state-of-the-art solutions usually are not intended for fully autonomous systems and they require for external batteries, to adjust the gate bias in rectifier mode, or adopt a different RF gate termination for the rectifier operation [23].

Here we show a procedure that eliminates the battery and gate termination tuning. Fig. 2.5 shows the external port arrangement of the system of Fig. 2.1 for rectifier mode (switches in State 2). In this case, the drain is disconnected from the dc bias path and loaded by $R_L$, which is optimized during the rectifier nonlinear design. The oscillator output port is now fed by the incoming RF signal at 2.45 GHz. Ideally, by means of the TRD principle, according to which the waveforms of a nonlinear device are time reversed versions of their counterparts in the dual device, oscillator and rectifier drain voltage and current are related by equations:

$$\begin{cases} V_{DS}^{OSC}(t) = V_{DS}^{RECT}(-t) \\ I_{DS}^{OSC}(t) = I_{DS}^{RECT}(-t) \end{cases} \tag{2.5}$$

thus preserving the intrinsic class-F behavior of the transistor. Consequently, proper device polarization needs to be ensured to provide conversion efficiency in rectifier mode, similar to the one obtained in oscillator mode (Fig. 2.8). However, to pursue the goal of fully energy-autonomous system, thus getting rid of external batteries, two main issues still need be solved:

**i)** to reach self-synchronized conditions, between the gate and drain voltages, namely waveforms with opposite-phase;

**ii)** to properly select the nonlinear device operating points for several possible RF input power levels, by exploiting the FET self-bias mechanism only.

Indeed, synchronous operation has demonstrated to ensure best rectifier conversion efficiency [33]. In this way a truly seamless switching between the two modes of operation can be performed. Optimization of the rectifier operating modes is performed with HB simulations with optimization goals on the RF-to-dc conversion efficiency. In the present case, an efficiency better than 60% for the optimization is specified as the design goal.

However, an important aspect in time reversal duality systems, is the accuracy of the nonlinear simulation of the FET model. For the rectifier and oscillator analysis, a nonlinear model capable of predicting device behavior in the first and third quadrant of the IV curves is needed, as in [34, 35]. In particular, nonlinear models for gate-source, gate-drain and drain-source capacitances are required to satisfy energy constraints

over all drain-source and gate-source voltage variations; the gate-source and gate-drain diodes interchange roles in the two modes of operation. A nonlinear device model from the manufacturer is implemented in Keysight ADS. An acceptable physical consistency with respect to the above mechanisms was tested for the selected device: in Fig. 2.12 the dc characteristics are plotted, parameterized by $V_{GS}$ for $V_{DS} > 0$, and by $V_{GD}$ for $V_{DS} < 0$, showing that the model is able to describe the device symmetry [34]. The dynamic load lines for both the operating modes are given in the same figure: the importance of the third quadrant of the I-V characteristics is evident from the rectifier-mode load line behavior. In fact, a nonlinear device model with accuracy and physical consistencies in the first as well as in the third quadrant of the I-V characteristics is mandatory to simulate the rectifier mode operation of the transistor.

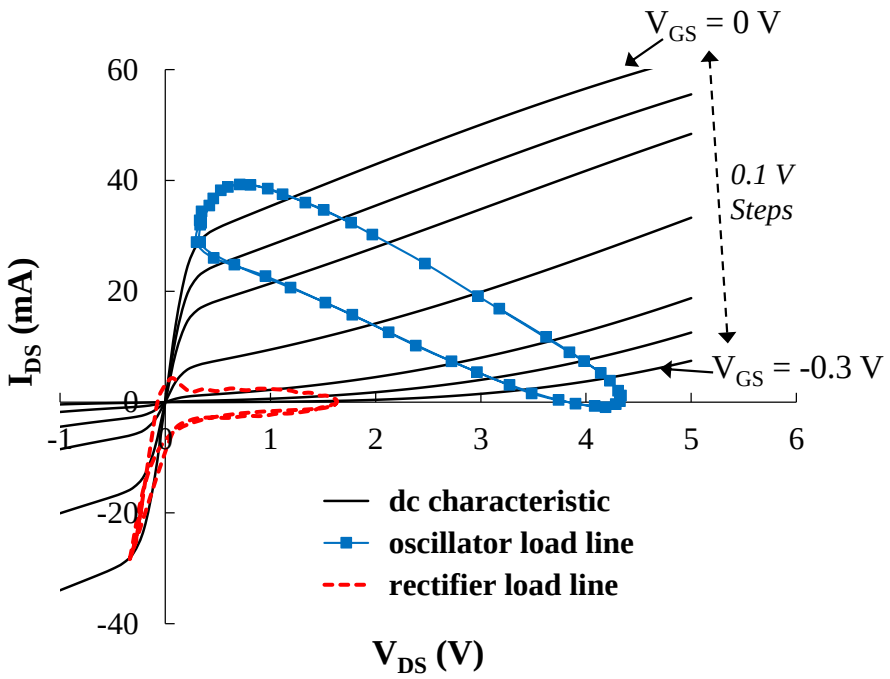


**Figure 2.12:** dc characteristics of the bilateral FET model, parameterized by $V_{GS}$ for $V_{DS} > 0$, and by $V_{GD}$ for $V_{DS} < 0$, and dynamic load lines in both operating modes.

Thus, to meet the self-synchronization conditions [24, 25] and maximize the efficiency, a nonlinear optimization of the same circuit topology for the concurrent maximization of the rectifier performance is carried out. Of course, the load resistance $R_L$, represents the optimization variable and plays a crucial role in achieving the best rectifier conversion efficiency. An optimum value of about 680 Ohm is obtained by the optimization. Fig. 2.13 and Fig. 2.14 summarize the results of the nonlinear system optimization for the rectifier operation mode.

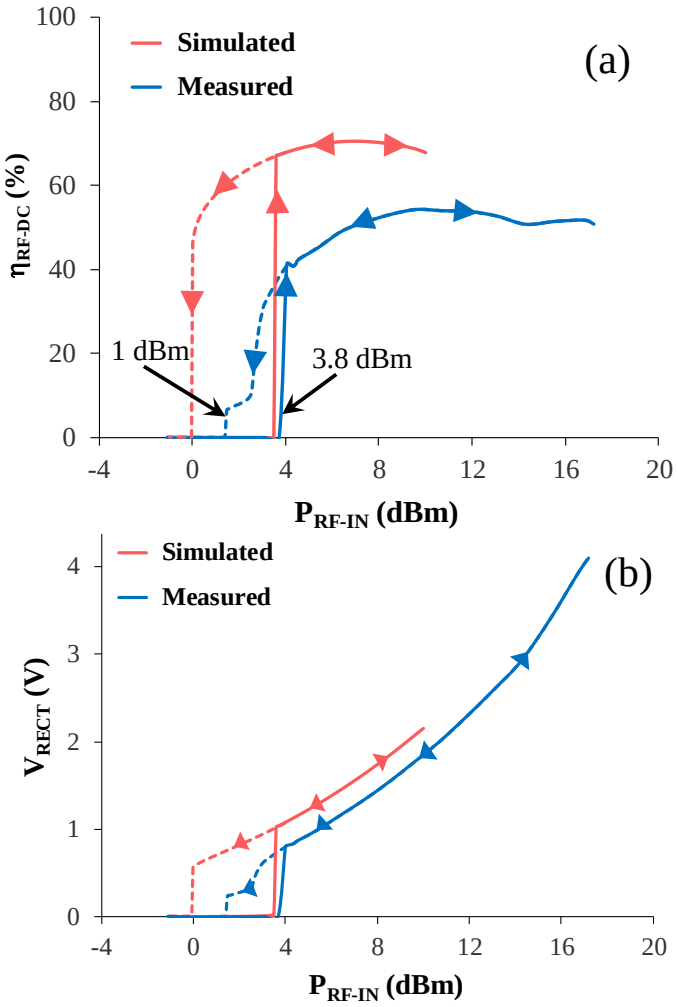


**Figure 2.13:** Measured and simulated RF-to-dc conversion efficiency (a) and output voltage (b) for the rectifier mode.

In Fig. 2.13(a) the simulated RF-to-dc efficiency is plotted. Fig. 2.13(b) shows the simulated output dc voltage, across the optimum dc load, resulting from the system nonlinear optimization. These plots predict that the circuit is able to operate with efficiency higher than 60% starting from about +3.8 dBm of input power. This performance is then preserved over a 12 dB RF input power range. From the same plot we get the corresponding dc voltage available at the rectifier output (up to 2 at 12 dBm).
The same figure shows the corresponding measured data: the circuit is able to operate with efficiency higher than 40% starting from input power as low as +4 dBm. This performance is preserved over a 14 dB range in input power. Starting from the floating gate condition ($V_{GS} \cong 0$).

Fig. 2.14 shows the evolution of the dc gate voltage versus input RF power using the self-bias mechanism. At the lower interval of RF power levels, $V_{GS}$ remains approximately zero; as the power increases, weak rectification is observed up to a selected value at which the dc gate voltage reaches a value lower than the transistor threshold voltage ($V_{TH}$). Increasing further the RF power drives the transistor more deeply in the depletion region, but this does not affect the efficiency performances of the rectifier.
Additionally, in Fig. 2.13 it is shown that the circuit operating in the rectifier mode exhibits hysteresis behavior versus input power. Starting from the minimum RF power levels (solid line), rectification is possible only over 4 dBm. For decreasing input power (dashed line), the measured rectifier operates down to +1.1 dBm. This further limit the input power ranges for which the circuit could rectify, since operating in the hysteresis zone between +1.1 dBm and +4 dBm is undesirable.
Of course, this limitation cannot be acceptable for a relay node system.

Thus, in this work we developed a different approach for increasing the sensitivity. Next section will show how we solve this problem by designing a network that acts as a bias-assisting loop in rectifier mode without affecting the oscillator mode.

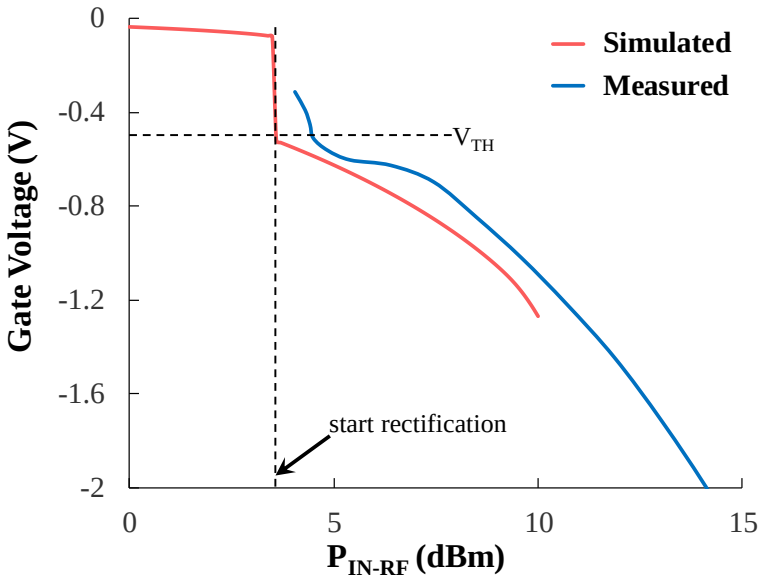


**Figure 2.14:** Measured and simulated self-bias gate voltage as a function of the input RF power.

## 2.4 Self-Bias Rectifier: Bias-Assisting Loop Approach

The major drawback of using the TRD principle to implement oscillator/rectifier circuits is that, depending on the transistor threshold voltage, a minimum RF input power is needed to start rectifier operation. To overcome this limitation, a simple network based on a matched low-power diode in shunt configuration, is included to bias the gate when the intrinsic transistor mechanism is not active yet. In this way the rectifier sensitivity is extended to lower input power levels with an acceptable RF-to-dc conversion efficiency. The bias assisting loop is optimized to

operate at low input power levels when the self-bias mechanism is not sufficient.

The loop is designed in such a way that it does not affect the oscillator mode of operation, while providing the minimum gate bias to start rectification. Fig. 2.15 shows the modified architecture of the oscillator/rectifier. The bias-assisting loop is connected to the rectifier input (oscillator output) by means of a microstrip coupler, which drives a sample of the incoming RF signal at 2.45 GHz to the diode through a suitably optimized stepped-impedance open-stub matching network.

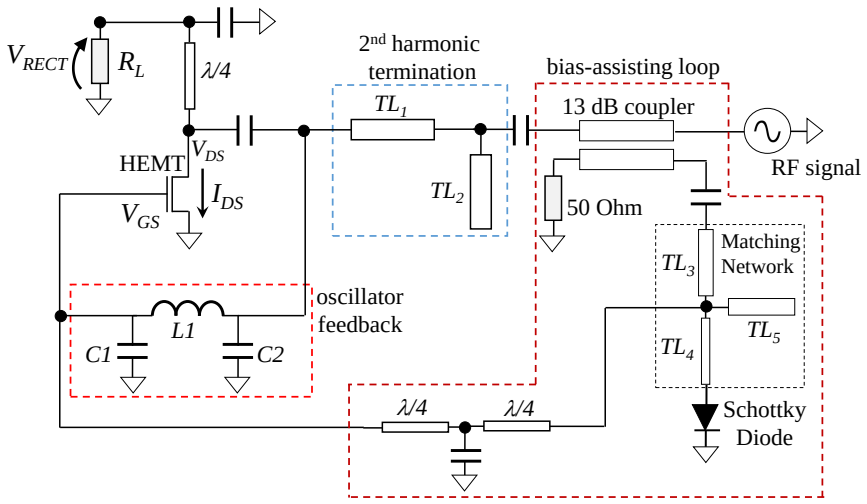


**Figure 2.15:** Oscillator/rectifier system schematic with bias assisting loop.

A Schottky diode (Skyworks SMS7630-079) is chosen and is arranged in shunt configuration providing a negative dc voltage at the transistor gate port. The two quarter-wave lines in the assisting loop play the role of RF blocks, thus ensuring isolation between the Class-F oscillator and the bias-assisting loop. In addition, they provide the dc path for the Schottky diode and the transistor gate. Coupling and isolation coefficients of the coupler are designed to reach the best compromise between high isolation between oscillator and bias assisting loop (demanding high

coupler directivity) and minimum power to activate the diode (demanding low coupler directivity).

For the present design, a 13 dB coupling coefficient is chosen, resulting in a directivity of 10 dB and an insertion loss of 0.8 dB at 2.45 GHz. Such insertion loss generates a 5% RF-to-dc efficiency degradation, but the oscillator performance is completely preserved.

Fig. 2.16 and Fig. 2.17 show the final optimization results for the system of Fig. 2.15. In Fig. 2.16 the dc component of the gate voltage is plotted against input RF power: the minimum activation voltage of $-0.3$ V is now available at RF input power of $-8$ dBm.

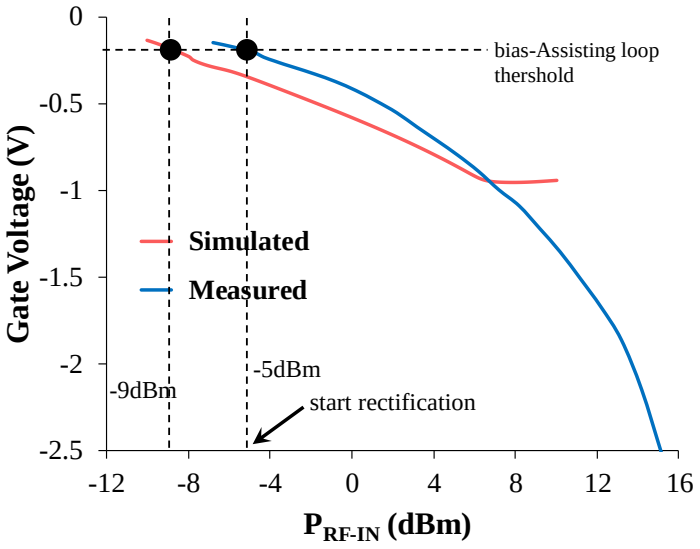


**Figure 2.16:** Measured and simulated self-bias gate voltage with bias-assisting loop as a function of the input power.

The corresponding simulated RF-to-dc conversion efficiency is shown in Fig. 2.17: an efficiency better than 60% is ensured for RF power levels ranging from $-4$ to $+10$ dBm. Note that, for simplicity the same load is used here for all input power levels. We expect possible improvement in efficiency when a proper dc-to-dc converter is designed to dynamically emulate the optimum load, for any possible RF input [20].

To experimentally characterize the circuit in rectifier mode, the drain bias is disconnected and an input RF signal at 2.45 GHz is fed into the RF port (switches in State 2, rectifier mode). The input power levels are varied from −6 dBm up to +18 dBm and the output dc voltage is measured across the output load $R_L$. Fig. 2.17 also shows the measured output voltage and RF-to-dc conversion efficiency as a function of input power. The same dc load, equal to the one obtained by circuit simulation, was used for these measurements.

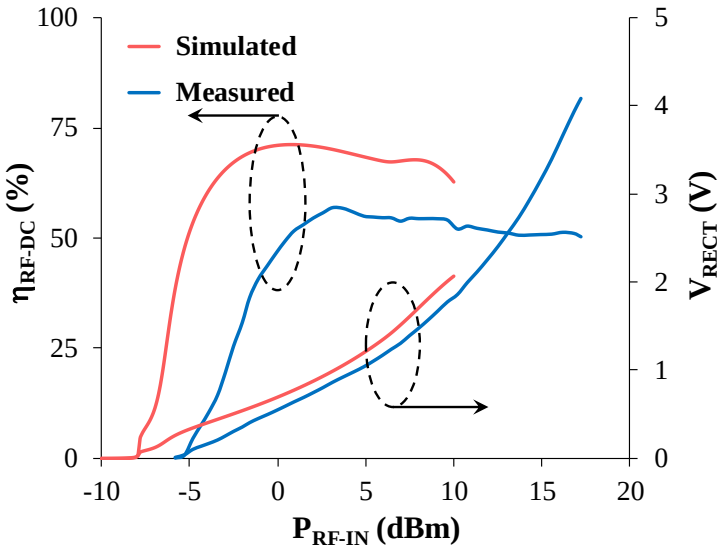


**Figure 2.17:** Measured and simulated RF-to-dc conversion efficiency and output voltage with bias-assisting loop as a function of the input power.

The measured plot shows that the circuit is able to start operating at −4 dBm, but with an efficiency of about 10%; whereas, for an input power of −2 dBm, the achieved efficiency is better than 40% and this performance is preserved over a 20 dB range in input power. Thus, it can be assumed that the rectifier sensitivity is around −4 dBm. Based on this measured performance, the power budget of the link between the RF source and the relay node can be obtained, assuming free-space propagation. Note that numerical convergence was difficult to be ob-

tained during nonlinear circuit simulation for the results of Figs. 2.13, 2.14, 2.16 e 2.17. Indeed, the circuit simulator was able to handle problems up to about +10 dBm of RF powers, while measurements could be carried out up to +18 dBm.

Finally, Fig. 2.18 demonstrates the key role of the bias-assisting loop in enhancing the system performance, by comparing the measured rectifier performance with and without the loop: in the absence of the loop the rectifier operates over a reduced input power range, approximately from +4 dBm to +18 dBm, with 45-50% of efficiency. With the bias-assisting loop, the minimum voltage required to start gate self-biasing is reached with input power levels as low as −4 dBm (8 dB improvement), and, by increasing the power, efficiency values similar to the no-loop case are achieved.

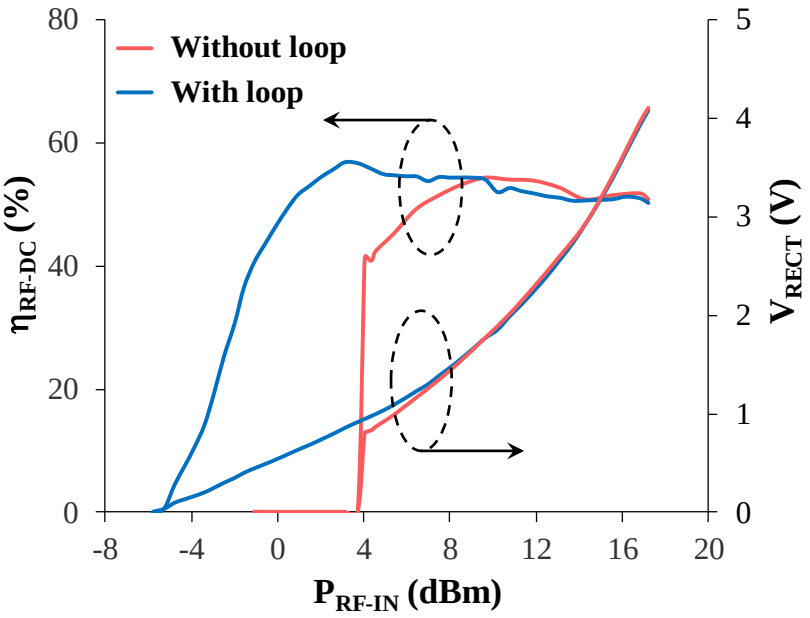


**Figure 2.18:** Measured RF-to-dc conversion efficiency and output voltage, with and without bias-assisting loop, as a function of the input power.

## 2.5 System Experimental Validation

This section will provide the final test done to verify the feasibility of the system. The final prototype is shown in Fig. 2.18. In particular, Fig. 2.19 (a) shows the resulting CAD model obtained by ADS Keysight tool, and Fig. 2.19(b) shows the photo of the final prototype. It is realized on a RF substrate named Arlon AN25N substrate ($\varepsilon_r = 3.38$; $tan(\delta) = 0.0025$; $thickness = 0.508$ mm).

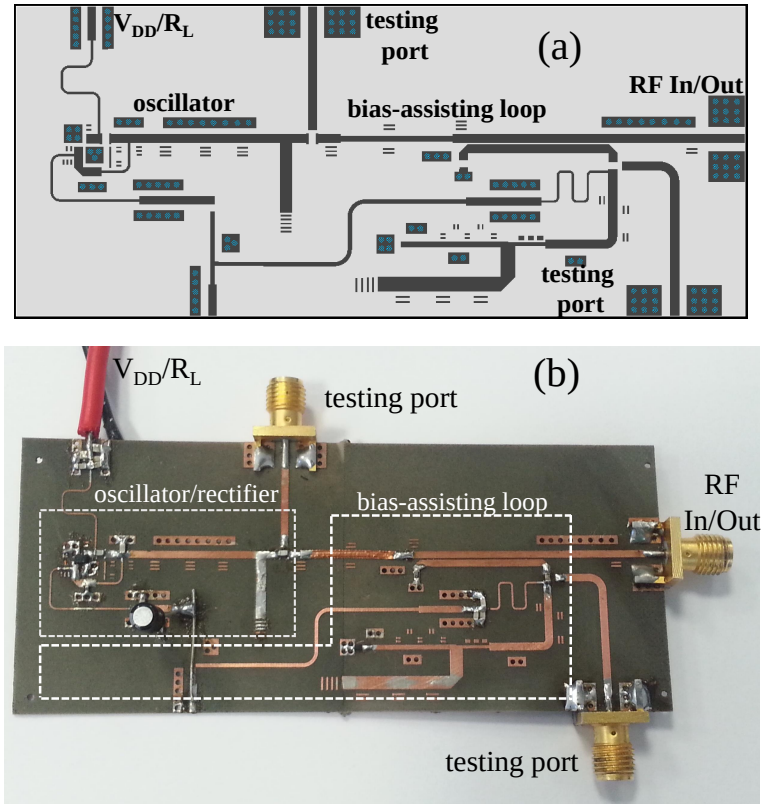


**Figure 2.19:** Photo of the fabricated prototype of the bidirectional system with bias-assisting feedback loop.

The PCB was built by using an in-house laser machine available at CTTC. As it can be seen, two testing ports are placed for measuring the directional coupler insertion loss and measuring and tuning the input matching of the bias-assisting loop. In addition, to understand the

lengths of the prototype, Fig. 2.20 shows the circuit layout with details on microstrip dimension (in mm). The adopted SMD components are capacitors from Murata (GRM1885). At the in/out port an RF switch can be used to connect the node to a directive receiving antenna or to a non-directive transmitting one.

To experimentally validate the feasibility of the energy-autonomous power relay node, measurements of the transient waveforms in both rectifying and power transmitting phases were carried out. The block diagram of the measurement set up is shown in Fig. 2.21; the in/out port of the prototype of Fig. 2.19 are alternatively connected to an RF signal generator (HP B3752A) or to an RF oscilloscope (Tektronix DPO72304DX) through a commercial switch (Skyworks SKY13350-385LF). Note that, at this stage no switch has been used to connect the antennas to the relay node. In the next chapter, it will be illustrating the limitation of commercial switches and how we overcome the problem by designing an ad-hoc switch implemented with GaAs technology.

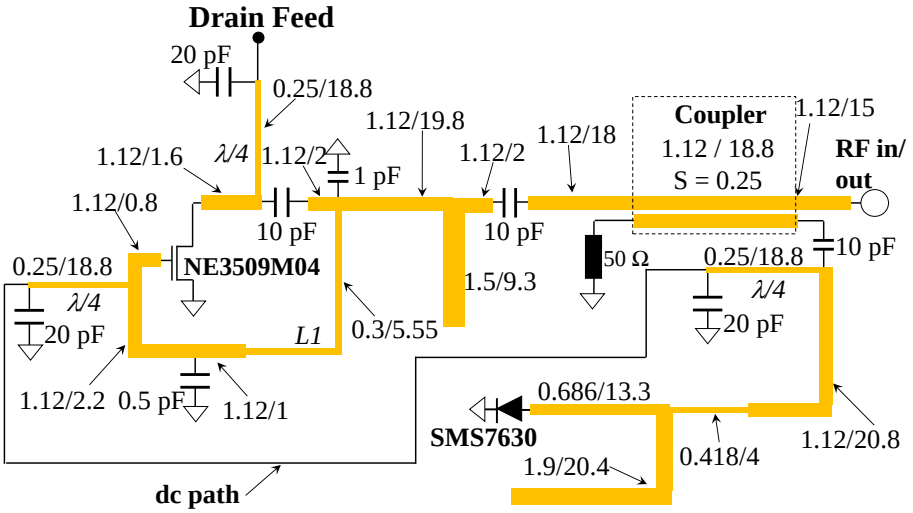


**Figure 2.20:** Measured waveform of the voltage ($V_{DD}$) on the storage capacitance ($C_{ST}$) with the system in rectifier mode.

The measurement procedure is carried out in two steps:

**i)** the switch is connected to port 2, the signal generator;

**ii)** the switch is commuted and is connected through port 3 to the scope.

In the first step the system acts as a rectifier and stores energy into the capacitor $C_{ST}$. The corresponding charging behavior is plotted in Fig. 2.22, where the measured time-evolution of $V_{DD}$ is shown. When a stable value of drain voltage is reached, the second step starts, and the system oscillation is captured by the scope. For this proof-of-concept demonstration, a storage capacitance of 50 μF is used: it can be substituted by a dynamic dc-to-dc converter, able to wake-up the system for low RF input power levels [20, 36]. For the present measurement set-up we simply make use of a higher input power of +8 dBm, resulting in a rectifier output open circuit voltage ($V_{DD}$) of about 2.4 V. This value corresponds to onset of oscillation as shown in the plots of Fig. 2.8.

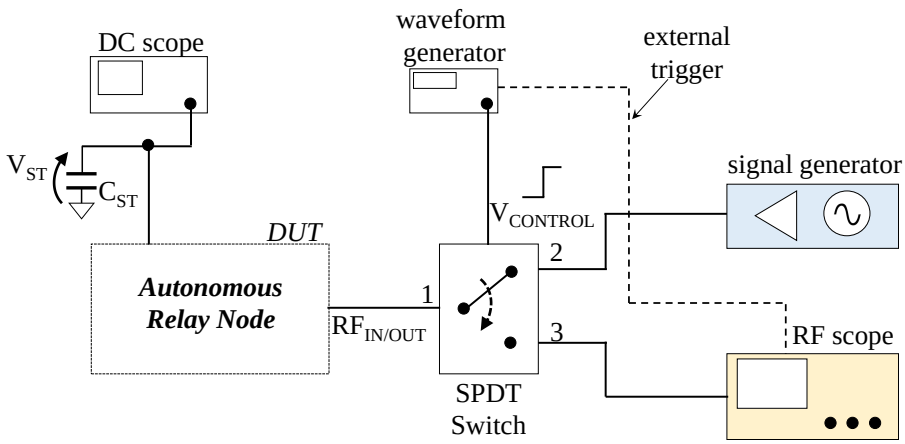


**Figure 2.21:** Block diagram of the measurement set-up.

Fig. 2.23 reports the measurements of the self-biased oscillator transient, with 2.4 V across the storage capacitor $C_{ST}$. Specifically, Fig. 2.23(a) shows the decreasing of $V_{DD}$ with respect to time, corresponding to the discharging behavior of $C_{ST}$. Fig. 2.23(b) shows the oscillator

RF output voltage evolution along the same time interval: as soon as the system is switched to the oscillator mode, it is loaded by a 50 Ohm termination with the drain bias of 2.4 V (voltage across $C_{ST}$).

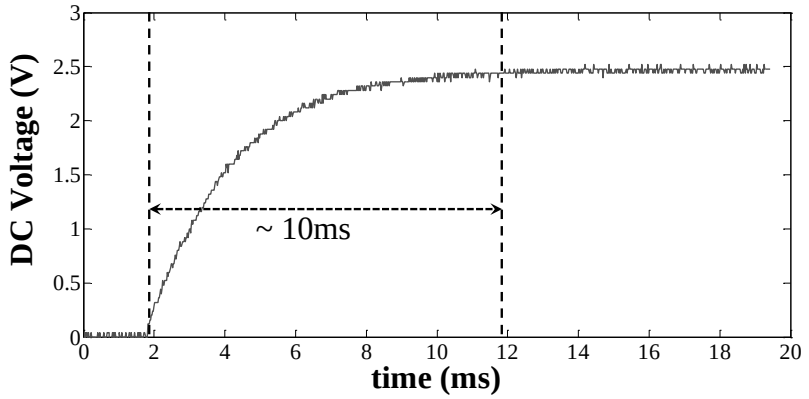


**Figure 2.22:** Measured waveform of the voltage ($V_{DD}$) on the storage capacitance ($C_{ST}$) with the system in rectifier mode.

In such conditions the oscillation build-up takes place. In Fig. 2.23 it can be observed that, after oscillation build-up, the RF output voltage decreases in the same time as the voltage in the storage capacitor. During this time-interval, the oscillator experiences different nonlinear regimes, as both $V_{DS}$ and $V_{GS}$ change continuously. As a consequence, RF output power, oscillation frequency and dc-to-RF efficiency change as well. This explains the different slopes observed in Fig. 2.23 during the transient.

For the present storage capacitance selection ($C_{ST}$ = 50 μF), the rectifier charging, and the oscillator transient time intervals are 10 ms and 28 ms, respectively. These different duration are due to the different nonlinear circuits that drive the charging/discharging operations of $C_{ST}$. It is worth noting that the discharging time (oscillator operation) is three times longer than the charging time, thus allowing a power transmission activity longer than the harvesting one. Of course, both these transient

intervals depend on the $C_{ST}$ value. In this case the 50 µF choice was adopted for measurement purposes to comply with the scope constraint in terms of available memory and sampling rate (12.5 GS/s). For example, for $C_{ST}$ = 1 mF and a reduced sampling rate, the measured oscillation is sustained for over half a second, which represents a feasible activation time in real applications [37].

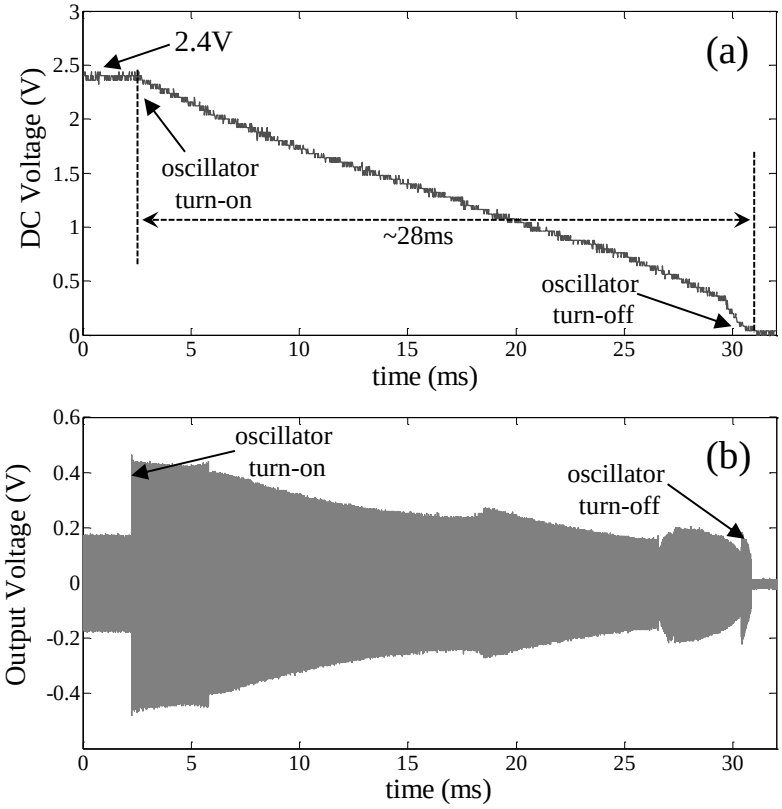


**Figure 2.23:** Measured waveform of the voltage ($V_{DD}$) on the storage capacitance ($C_{ST}$) with the system in oscillator mode (a), and transient oscillation waveform (b) of the prototype of Fig. 2.19(a).

## 2.6 Conclusion

In this chapter, is first demonstrated the effectiveness of using a relay node inside a RFID system communication. A 50% improvement, in terms of RF power needed to activate the node, with respect to the case without relay node has been calculated. Then, theoretical and experimental aspects for a true energy autonomous wireless power relay node are presented. The node can operate continuously without a battery, and demonstrates the same efficiency at 2.45 GHz in rectifier (power-receive) mode and oscillator (power-transmit) mode. The receiver starts operating at input power levels below 0 dBm and remains in a robust oscillatory regime over a wide range of drain supply voltages.

Based on the time-reversal property, a new oscillator design is developed using the MESFET floating-gate property for self-biasing. In the rectifier mode of operation, the gate self-bias is enhanced by a single short-circuited diode to extend the dynamic range of the relay. A commercial RF switch is included in the prototype to experimentally demonstrate first the energy reception and storage, and subsequently autonomous power generation.
Measured and simulated results for the 2.45 GHz hybrid prototype are in good agreement, and the circuit is amenable to monolithic integration. The entire measurements campaign has demonstrated the feasibility of proposed system both in term of bidirectional operation and in term of system efficiency.

We envision many application scenarios that could take advantage of the presented proof-of-concept: it can be integrated in next-generation sensors, or RFID-enabled sensor tags, for cooperative energy supplying, or it can be configured as a special node/tag, among many standard passive ones, precisely located to fully exploit the point-to-point con-

nection to an RF source. In the first case, randomly placed tags with non-directive antennas will receive or provide energy from/to neighboring nodes depending on their activities. In such situations, the relay capabilities will enable the extension of the nodes energy autonomy. In the second scenario, a highly efficient link can be established between the RF source and the node, while the rest of the (standard) battery-less tags can be randomly and dynamically located close to the node, taking advantage of its power generation capabilities.

# Chapter 3

# APRN: Monolithic Implementation

This chapter is dedicated to the design of the previously proposed power relay node by using a monolithic technology. This choice was taken considering that one of the biggest milestone in the modern manufacture is the ability of miniaturizing the product that they intend to sell as much as possible. This miniaturization involves electronic devices but not only, even mechanical, optical and thermal parts are interested in this important process. Examples include miniaturization of mobile phones, computers and vehicle engines. To this end, for years many technologies and processes have been investigated and developed. In the electronic market, Moore's law predicted that the number of transistors on an integrated circuit would double every 18 months [38].

This tendency has been mostly respected in the last years thanks to the huge investments done in such field. Many technologies have been developed tailored for RF, microwave and mm-Wave applications such as Gallium Arsenide (GaAs) and Gallium Nitride (GaN). GaAs can be used to implement various transistor type such as MESFET, HEMT and

JFET. All these structures work well at high frequency.

Table 3.1 summarize pros of using monolithic and hybrid approach [39, 40]. The first question that needs to be asked is: which of these processes is better in term of performances? The answer is simple, the hybrid MIC. In fact, MIC components are implemented using different material such as dielectric, semiconductor, etc. Such division allows designers to adopt the optimal technology for implementing the different parts of the system. Nevertheless, an hybrid circuit results to be large, less reliable due to the miscellaneous of technology, and frequency limited because of the existence of many parasitic effects.

**Table 3.1:** Microwave Processes pros Comparison.

| **MIC** | **MMIC** |
|---|---|
| Better performance (NF, Efficiency, P1dB) | Performances uniformity guaranteed over the entire production |
| Low unit Cost (small and big quantity) | Low unit Cost (only big quantity) |
| Fast development | Long time for development |
| Variety of dielectric Mmaterials | Very Small Size and Weight |
| Integration of Semiconductors: MESFETs, Bipolar, Pin Diodes, Digital | Very Broadband Performance due to few parasitic effects |

On the other hand, MMIC technology allows us to obtain highly miniaturized devices (order of $1 - 15$ mm$^2$). With this technology, no parasitic effect can exist because components are directly implemented on-chip and no bonding wires or transmission lines are needed. furthermore, it is much easier to design broadband circuits.

Finally, monolithic processes are truly reliable in terms of performances since all circuit elements are realized on the same piece of semiconductor (wafer). This approach strongly reduces the process variability and components defects. This way, consistent design can be accomplished

with higher production yield with respect to a hybrid implementation. The current chapter is dedicated to a novel MMIC implementation of the power relay node concept adopting the UMS PH10-10 GaAs technology. As for the hybrid version of the system, the same nonlinear device is exploited for the two operation modes, namely the RF-to-dc conversion (rectifier mode) and the dc-to-RF conversion (oscillator mode). In order to commute between the two modes a novel solution for an on-chip switch is introduced together with the implementation of an on-chip nonlinear coupler. Both these these choices were strategic to accomplish a fully autonomous relay node operation.

In addition, special care has been devoted to the optimization of the MMIC area, since it is well known that it is directly related the cost of each sample itself. Such area minimization has been obtained mainly obtained by two design choices:

**i)** multifunction Input/Output ports, and

**ii)** using of a compact FET-based coupler.

The first one allows to minimize the number of chip ports, which is an issue when the MMIC area is very small ($1 \times 1$ mm$^2$). Multifunction ports are designed in such a way that they are able to transfer the RF signal as well as the bias dc voltage and control signals. So, given the dual mode operation of the same active device, it is possible at the same time to bias the MMIC and use the RF signal generated by the oscillator. The second choice is important likewise, since distributed-elements couplers at frequencies of few GHz (our case 2.45 GHz) lead to a relevant occupied are on the chip, even with meandrization. In the following, it will be shown that adopting a FET-based coupler only requires an area of about 300 $\mu$m$^2$ with no compromise with its performances. Of course, meeting all the requirements while keeping a compact design of

the overall system was not an easy task, and a trade-off was needed. The present chapter is dedicated to the description of the MIMIC nonlinear design procedure and intentionally outlines the issues encountered and the countermeasures adopted to overcome them. The second part of the chapter is dedicated to the extensive experimental characterization of the MMIC prototype of the relay node mounted on a custom test-jig developed on purpose.

The chapter is organized as follows. Section 3.1 is dedicated to the description of the selected MMIC technology. Section 3.2 provides an overview of the power relay node operation in transmitter and receiver mode. Sections 3.3, 3.4 and 3.5 describe the MMIC subsystems design, namely the high-efficiency oscillator and its reverse mode of operation, the asymmetric RF switch, and the hybrid-approach bias-assisting loop. The MMIC simulated performances are then experimentally validated and Section 3.6 describes the measurement set-up to validate power relay node MMIC implementation. Section 3.7 drives the work conclusions and discusses possible application scenarios where the power relay node can be exploited.

## 3.1 Technology

The first step of the MMIC design is the technology and related foundry selection. For the present scientific work in order to obtain an easy and economical access to MMIC technologies, the European foundry United Monolithic Semiconductors (UMS) [41] has been chosen. With this foundry, shared project and multi-project wafer are possible allowing costs saving mandatory for research center and universities. According to the foundry rules, the lead time to manufacture the MMIC is about 16 weeks and it supplies 20 dicing dies already passivated and dc tested.

Fig. 3.1 shows an overview of the UMS available technologies. Two main materials based on the III-V group (GaN and GaAs) are used and different transistors are available such as HEMT, pHEMT and InGAP. Since the operating frequency of the relay node is relatively low (2.45 GHz ) and an output power over +15 dBm is sufficient to meet the relay node goals, a low-noise medium power technology as PH25 and PH15 were considered the appropriate one as a good trade-off between technology maturity and costs. Unfortunately, the time slots of these runs were not synchronized with our design time schedules and a technology for higher frequency was chosen, namely the UMS PH10-10 [42]. Indeed, the PH10-10 is a process tailored for millimeter wave applications ($40 - 70$ GHz [43]) but this was the unique choice compatible with my activity schedule.

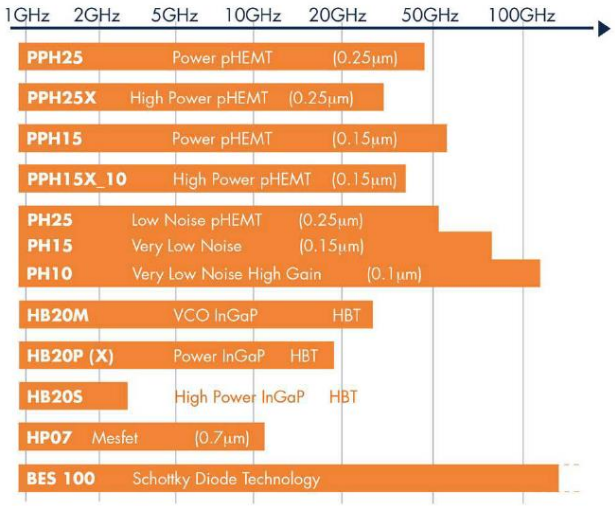


**Figure 3.1:** UMS Foundry GaAs processes (source: www.ums-gaas.com).

PH10-10 technology will be now deeper analyzed to understand its key features. One of the most important parameter of a GaAs technology is the channel length, also called gate length ($L_G$), which determines the cutoff frequency $f_T$. PH10-10 implements a 100 nm gate length

on a 70 μm substrate which is well suited for high gain and low-noise applications.

Fig. 3.2 shows a cross section of the selected technology and relative active and passive components. The pHEMT transistor has a T-shaped aluminum gate and it is passivated on top by silicon nitride to protect the die. To have access to the transistor, two gold ($Au$) metallization layers are used.

As already said, the active device is a pHEMT transistor with a typical pinch-off voltage $V_{th}$ of $-450$ mV. This transistor power performance can be optimized in terms of number of fingers ($N$) and fingers width ($W_u$) and it is able to provide a power density above 250 $mW/mm$ at 2.5 V and a typical noise figure of 2.3 dB @70 GHz.

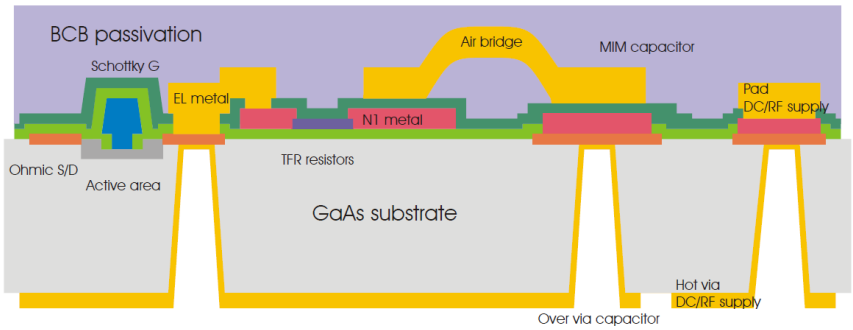


**Figure 3.2:** Cross section view of PH10 process (source: UMS PH10-10 Design Kit).

The second metallization layer is available for implementing air bridges in order to guarantee a good isolation for lumped spiral inductors. The available inductors are realized by adopting square planar spiral topology optimized to operate at high frequency. In addition, lumped capacitors are available as Metal-Insulator-Metal (MIM) structure implemented with silicon nitride. The described lumped elements, both inductors and capacitors, have value ranges from0.12 to 12.65 nH and 0.25 to 10 pF, respectively.

Other critical components in MMIC technology are the conductive vias that are used to pass through the substrate to connect the source contacts to the back side. PH10-10 provides two kinds of vias:

**i)** standard conductive vias and,

**ii)** vias placed below MIM capacitors over via (called *MIM over via*).

The first one, are via hole with an area of 50 × 50 m and provide an easy way to have access to the MMIC ground. The second one provides a special feature that is very useful to compact the design and to reduce the parasitic effects. In fact, by using this kind of capacitor, it is possible to use a shunt MIM capacitor with no need for an additional via-hole. PH10 also provides sheet resistors implemented by different materials: tantalum nitride ($TaN$), TiWSi and GaAs. The first one is used to build low-value (30 Ohm/sq) and accurate resistors, whereas TiWSi and GaAs resistors are used for higher values: 1000 Ohm/sq and 120 Ohm/sq, respectively.
All the components described above are modelled directly by the foundry and are made available in the process design kit (PDK). Such library contains the linear and non-linear models. All the simulation presented in this chapter are obtained by Keysight ADS tool.

Finally, it must be noted that no diodes are provided in the PH10-10 technology. This point is one of the limitation of the selected technology and, because of this, it was not possible to realize the bias-assisting loop completely on-chip. Indeed, a hybrid approach has been adopted as it will be explained in Section 3.5.

## 3.2 System Overview

The description of the Relay Node components, suitable for an MMIC realization, is the subject of the present chapter. A novel aspect of this implementation with respect to the MIC version is the integration of an interesting solution of the switch to select the transmitting and receiving antennas. According to the relay node facilities, the main MMIC sub-circuits are: the oscillator/rectifier, the switch and the bias-assisting loop. Unfortunately, due to the absence of diodes models in the PH-10 library, the bias-assisting loop has been implemented off-chip. Indeed, a hybrid combination of off-chip and on-chip sub-circuits has been chosen, to overcome the diode limitations.
The block diagram of the GaAs chip is shown in Fig. 3.3(a), with the main building blocks highlighted, while Fig. 3.3(b) illustrates the entire system, with the MMIC embedded among the off-chip components: the high-efficiency oscillator, the SPDT switch and the coupler have been realized monolithically, with the coupler being a portion of the bias assisting loop. The Schottky rectifier and its matching network are external and the connection between the MMIC and the off-chip rectifier is accomplished by using bonding wires.

The RF chokes (RFC1, RFC2 and RFC3) allows us to provide or extrapolate dc signals without affecting the RF performances. They are realized off-chip. By using these chokes, it is possible to efficiently separate the RF and dc signals (i.e. RF-IN/SW1).

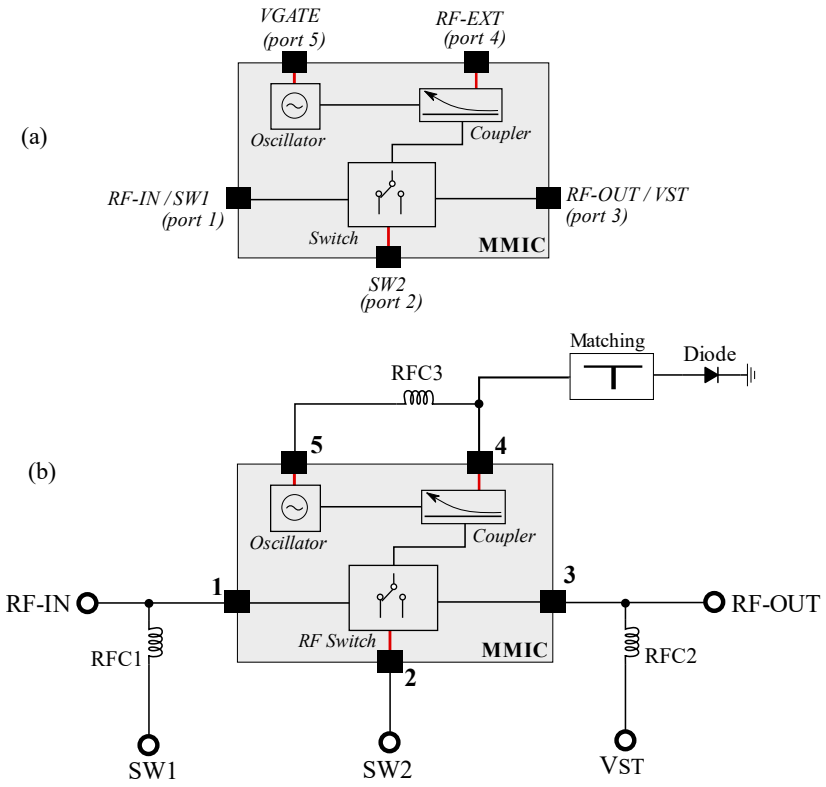


**Figure 3.3:** System Architecture: (a) MMIC architecture, (b) complete system configuration.

In order to drive the MIMIC in both the operating modes, a total of seven ports are used (Fig. 3.3(a)) that are listed below:

- **RF-IN**: RF input of the relay node.
- **RF-OUT**: RF output of the relay node.
- **SW1**: Logical control pin of the switch (in combination with SW2).
- **SW2**: Logical control pin of the switch (in combination with SW1).
- $\mathbf{V}_{ST}$: Storage node.
- **RF-EXT**: RF output of the internal coupler to feed the external rectifier.

- $\mathbf{V}_{GATE}$: Directly connected to the gate of the oscillator's transistor.

where RF-IN is the input port to be connected to the receiving antenna. SW1 and SW2 are the logical pin used to control the switch state. RF-OUT is the RF output port of the MMIC, where the transmitting antenna is connected. $V_{ST}$ is the most important port: it is used to extract the rectified voltage (relay node in receiving mode) or provide a dc voltage to the internal oscillator (relay node in transmitting mode). When the MMIC operates in rectifier mode, this port is loaded by the parallel connection of the storage capacitor and the optimum load. RF-EXT is the on-chip coupler output port, used to provide RF power to the external rectifier (bias assisting loop) in order to obtain the negative voltage for the gate biasing of the oscillator's transistor.

Finally, $V_{GATE}$ is the access port to the oscillator's gate, to provide the DC bias to the oscillator in reverse mode, that is when it operates in rectifier mode. Note that, ports RF-EXT and $V_{GATE}$ are needed for realizing the combined off-chip and on-chip bias loop of the oscillator. If the diode model were available in the technology library, the external rectifier could have been integrated in the chip, thus eliminating the external diode and the rectifier and the related ports.

Let us now discuss how the two possible operation modes of the rely node, namely receiving and then transmitting power, can be implemented with a MMIC technology.
In the first mode, it operates as rectifier and the incoming energy from the receiving antenna is rectified and stored on the external capacitor connected at port $V_{ST}$ in parallel with $R_{OPT}$. Fig. 3.4 shows the MMIC schematic signal and bias flows when the relay operates as rectifier. At the beginning, the storage voltage $V_{ST}$ is 0 V. In this state, the mono-

lithic switch is designed in such a way that it is connected to the RF-IN port (port-1). To do so, port SW1 is grounded and SW2 is connected to $R_{OPT}$. This will be explained in detail in Section 3.4.

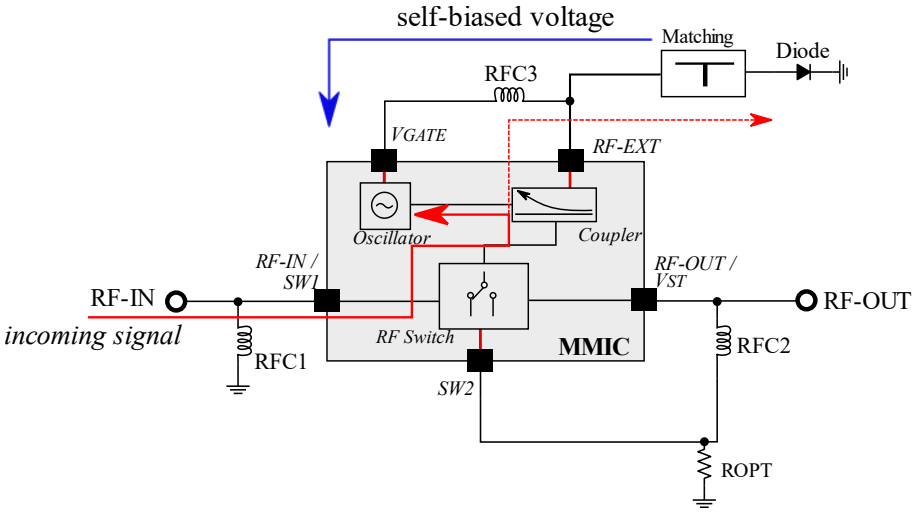


**Figure 3.4:** System behavior in receiver mode.

In this way the RF signal received at RF-IN, is transferred to oscillator drain port (Fig. 3.4, solid red arrow), that now operates as rectifier, by means of the duality principle.

To improve the sensitivity, in rectifier mode is used the bias-assisting loop as done in the previous version of this system. According to this, the on-chip coupler extracts a few powers from the incoming RF signal to feed, through port RF-EXT, the external rectifier port (Fig. 3.4, dotted red arrow) performing the bias assisting loop: it is a negative voltage which is feedback to the oscillator gate through the RF choke RFC3 and the $V_{GATE}$ port (Fig. 3.4, blue arrow).

Finally, the rectified dc voltage is extracted through the external RF choke RFC2 and it is available at the $V_{ST}$ port to charge the storage capacitance. Note that, the switch needs to be dc-coupled in order to permit a dc path from the oscillator to the output pin.

Once the output voltage $V_{ST}$ reaches a sufficient voltage to bias the oscillator (typically 2.5 V) the relay node can be configured in oscillator (transmit) mode. Fig. 3.5 shows the configuration of the MMIC in oscillator mode. Instead of the optimum load, a dc bias is now used, and it is directly provided to the oscillator (Fig. 3.5, blue arrow). The RF signal generated by the oscillator is available at the RF-OUT port (Fig. 3.5, red arrow) thanks to the switch configuration. Note that, to have the switch configured in transmit mode, SW1 is connected to $V_{DD}$ and SW2 is connected to ground as will be explained in 3.4.

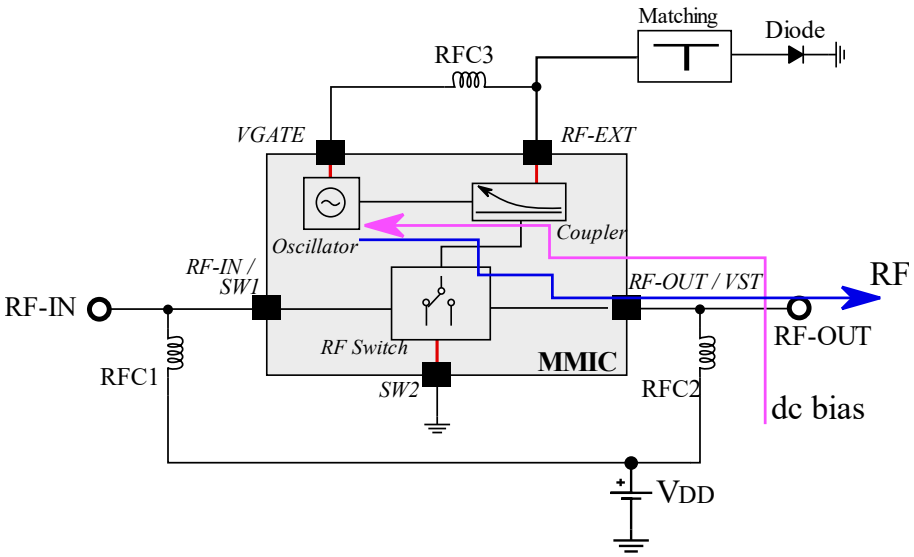


**Figure 3.5:** System behavior in transmitter mode.

In this phase, the coupler does not affect the oscillator performances due the high isolation that it offers.

As conclusion of this section, Fig. 3.6 shows the final circuital schematic of the MMIC, consisting of an oscillator, a switch and a FET-based coupler. The design of the oscillator is the subject of the next section (Section. 3.3). It describes the design and operation of the oscillator, including the dual rectifier process. Section. 3.4 discusses the design details of the RF switch and Section. 3.5 will explain the implementation

of the hybrid bias-assisting loop with special emphasis on the on-chip coupler. Finally, the final layout of the MMIC and relative test-jig board are presented in Section. 3.6, together with the experimental results.

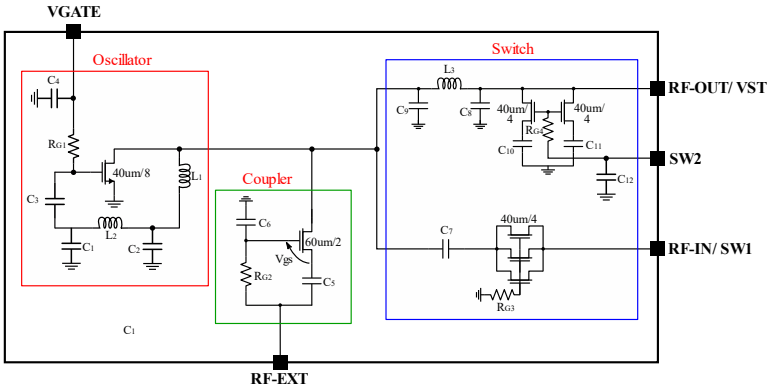


**Figure 3.6:** Final schematic of the MMIC relay node.

## 3.3 MMIC Oscillator/Rectifier Design

Obtaining a high efficiency oscillator is not an easy task. It generally requires switching architecture like Class-E and Class-F. However, the implementation of these architectures using a monolithic technology requires high-Q resonant load network [44, 45]. For instance, from simulations carried out at 2.4 GHz, the quality factors of the spiral inductor and MIM capacitor available from the PH10-10 process, are both lower than 8, thus limiting the maximum obtainable efficiency.

In order to design a high-efficiency oscillator, it was decided to implement a simple switching oscillator operating with a reduced circulation angle, between 180 to 360 degrees. Such type of operation is known as class-AB. This approach simplifies the design because it does not require a resonant loading network to obtain high efficiency. In addition, it is fully compatible with the floating gate solution, discussed in the previous chapter. The selected topology is the best compromise to cope with low Q-factor of the lumped elements. No better results could be

obtained using harmonic termination techniques.

As it will be shown, the oscillator efficiency is aligned with state-of-the-art solutions. Theoretically, the efficiency of class-AB device can vary from 50% (class-A) up to 80% (class-B). In practice, these values drop to 30% and 60%, respectively.

The schematic of the proposed 2.4 GHz oscillator is shown Fig. 3.7. it consists of a common-source FET and a double-stage LC feedback network. In the MMIC version has been used the gate floating approach in order to exploit the self-bias mechanism responsible for the transistor switching behavior: the higher is the negative voltage resulting from the self-biasing, the smaller the conduction angle and consequently the higher the efficiency.

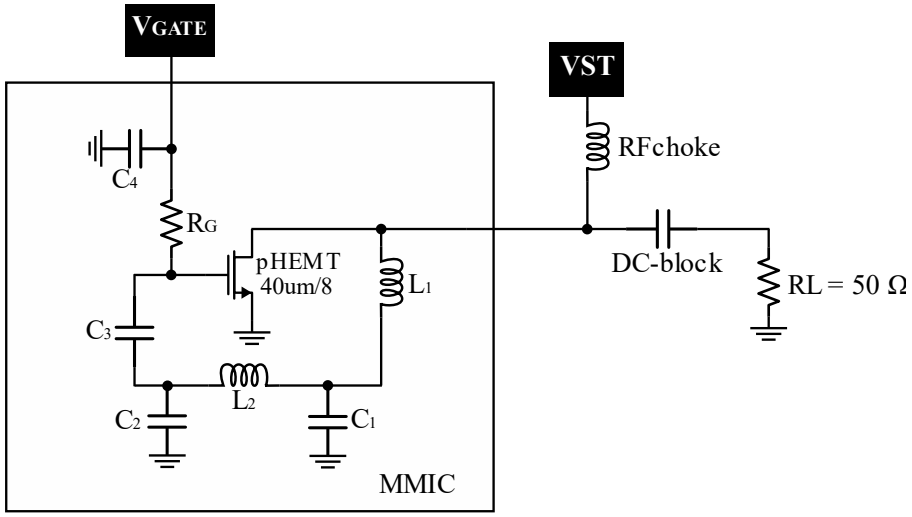


**Figure 3.7:** Oscillator architecture with external bias network.

From the UMS library, it is possible to vary the number of gate fingers ($N$) and the width of the gate fingers ($W_u$) to select the most appropriate device. Essentially, such parameters are used to increase the gate periphery and hence, the maximum output power of the device itself. A power density of 250 $mW/mm$ for a drain bias voltage of 2.5

V can be expected by the PH10-10 technology. According to this, we selected one $8 \times 40$ μm GaAs pHEMT with a resulting total periphery of 320 μm. This way, an output power of +19 dBm at 2.5 V drain bias should be guaranteed.

The feedback network is a dual-stage lumped element LC network. This structure has been optimized to accomplish two goals:

**i)** satisfy the oscillation condition, and

**ii)** to ensure the fundamental matching circuit.

To reach these specifications a cascade of two L-series and C-shunt elements have been used which resonate at the operating frequency $f_0$. The capacitor $C_3$ is simply a dc block for the dc bias $V_{DD}$, and the combination of $R_G$ and $C_4$ are used to eliminate any RF path towards the $V_{GATE}$ pad. This allows the external circuitry to bias the oscillator without disturbing its behavior. Finally, the bias network is not implemented inside the chip, but externally using a RF choke.

The optimization process of the oscillator was performed with harmonic balance (HB) simulation with optimization goals on the dc-to-RF oscillator efficiency and operating frequency $f_0$. Inductors $L_1$, $L_2$ and capacitors $C_1$, $C_2$ are optimization variables. In the present case, an efficiency better than 60% is specified as the design goal at the operating frequency of 2.4 GHz. Once the circuit optimization process is concluded and its results collected, to verify the layout correctness all the passive components such as microstrip lines, MIM capacitors, and spiral inductors, are all simulated with a 2.5D EM simulator available in Keysight ADS called Momentum. This EM simulator uses a frequency-domain Method of Moments (MoM) technology to accurately simulate complex EM effects including coupling and parasitic.

The final layout of the proposed 2.4 GHz oscillator is shown Fig. 3.8. It can be recognized the feedback network composed by the spiral inductors and the MIM capacitors.

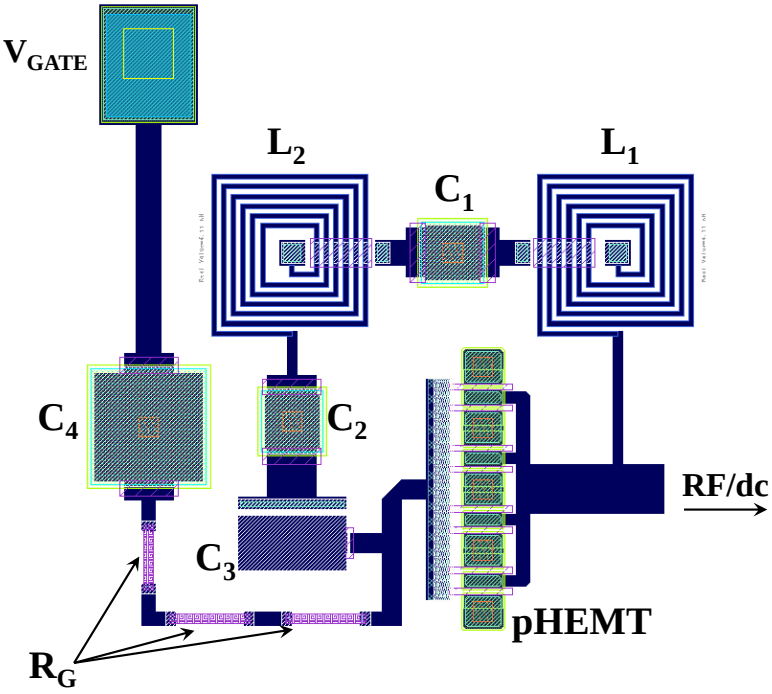


**Figure 3.8:** Oscillator layout arrangements.

Note that besides standard MIM capacitor, MIM capacitors over vias are used to reduce the occupied area. Capacitor $C_3$ is a standard MIM capacitor and is used to block the dc voltage $V_{DD}$. This capacitor must be properly selected to avoid any further filtering effect in the feedback loop: a 2 pF value has been chosen as the best trade-off between occupied area and filtering effect.

In Fig. 3.9 the simulated dc-to-RF conversion efficiency and output power of the oscillator are plotted versus the drain bias. The resulting oscillator efficiency is over 52% for the whole drain voltage range, from 0.8 to 2.8 V, the peak value is 55% for a drain bias of 1.4 V. In addition,

a peak output power of +18 dBm (Fig. 3.9) is obtained at 3.2 V. It is noteworthy the flat behavior of the dc-to-RF efficiency, over the $V_{DD}$ range from 0.8 to 2.8 V, with a variation lower than 5%.

In Fig. 3.10 the oscillation frequency and gate voltage variations with respect to the drain bias are plotted.

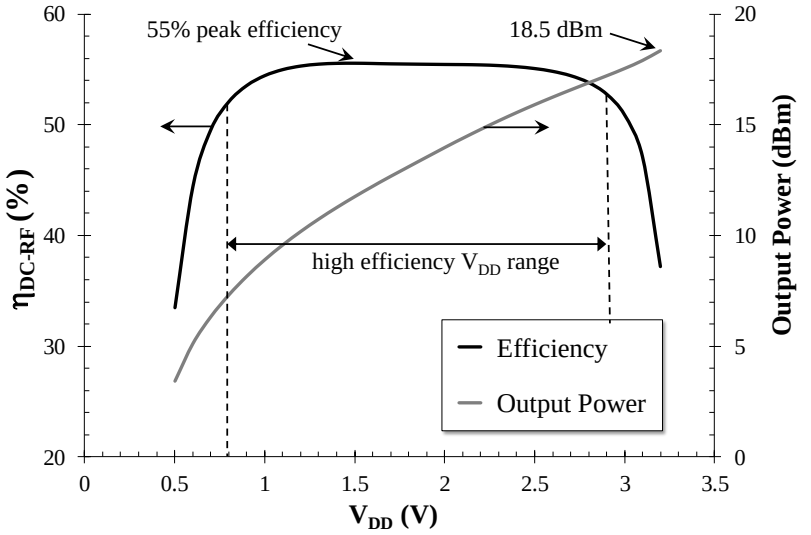


**Figure 3.9:** Simulated oscillator dc-to-RF efficiency and output power versus drain voltage.

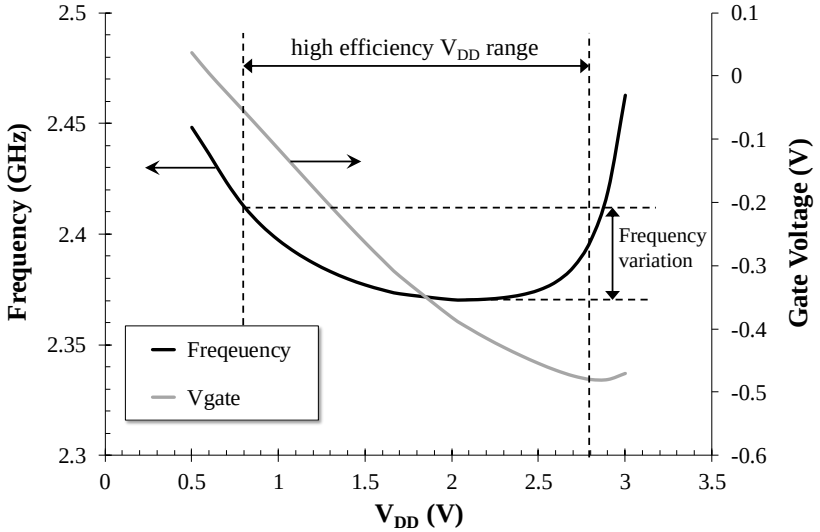


**Figure 3.10:** Simulated oscillator frequency and gate self-biased voltage versus drain voltage.

The oscillator presents a good frequency stability over $V_{DD}$, with a maximum deviation of 40 MHz well centered at 2.4 GHz.

Once again, it has to be recalled that, by means of the TRD principle, rectifiers with high RF-to-dc conversion efficiency can be derived in a straightforward manner from the design of high-efficiency oscillator. to obtain this second operating mode, the drain is disconnected from the dc bias path and loaded by $R_{OPT}$, which plays a crucial role in achieving the best rectifier conversion efficiency. From a dedicated HB optimization of the full system, an optimum value of about 80 Ohm is obtained. The oscillator output port is then fed by the incoming RF signal at 2.4 GHz.

Figs. 3.11 and 3.12 summarize the results of the nonlinear system optimization for the rectifier operation mode. In Fig. 3.11, the simulated RF-to-dc efficiency is plotted versus the input power (RF-IN), on the same graph the simulated output dc power, across the optimum dc load. These plots predict that the circuit is able to operate with efficiency higher than 50% (similar value to the dc-to-RF efficiency demonstrated for the transmitting mode) starting from about +1.1 dBm of input power. This performance is then preserved over a 6 dB RF input power range.

Fig. 3.12 shows the evolution of the dc gate voltage versus input RF power using the self-bias mechanism. At the lower interval of RF power levels, $V_{GS}$ remains approximately zero; as the power increases, weak rectification is observed up to a threshold input power value at which the dc gate voltage value approaches the transistor threshold voltage. At this stage, the rectification starts with a high efficiency. Increasing further the RF power drives the transistor more deeply in the depletion region, but this does not affect the efficiency performances of the rectifier.

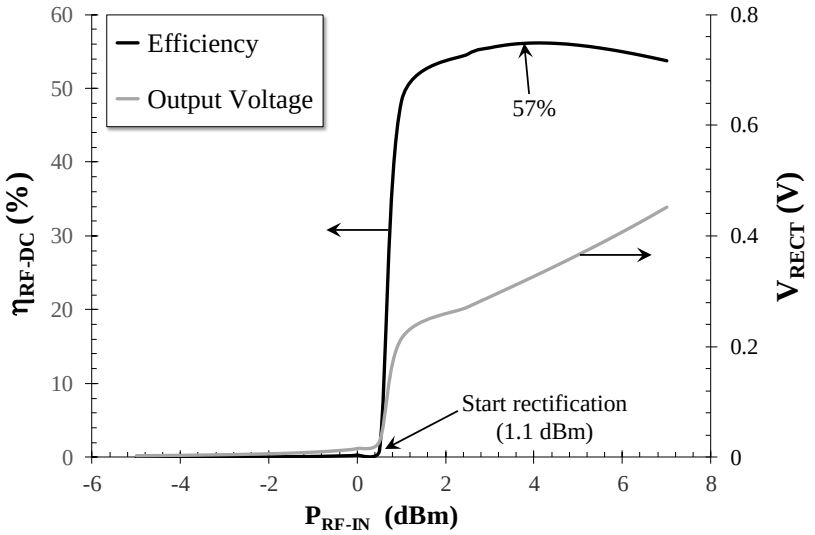


**Figure 3.11:** Simulated rectifier RF-to-dc efficiency and output rectified voltage.

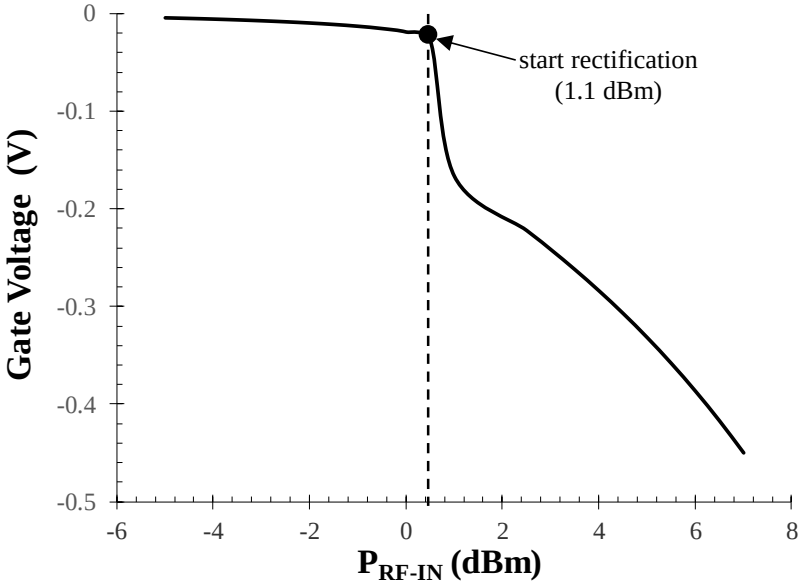


**Figure 3.12:** Simulated gate self-biased voltage in the rectifier phase.

## 3.4 SPDT Switch Design

Switches are essential elements for a number of applications requiring to selectively route a RF signal from a certain path to another. As explained in Section 3.2, the oscillator needs to be dynamically connected to two different antennas: the receiving and the transmitting ones. For this scope, a single-pole double-throw (SPDT) switch needs to be adopted. A possible implementation of solid-state switches is to use GaAs FET transistors.

A FET-based switch is used as three-terminal device, and the gate is properly biased to define the states of the switch. The most common configuration for SPDT switches is shown in Fig. 3.13 (a) [46]: it consists of two series and two shunt connected transistors which realize two symmetric arms "A" and "B" driven by two complementary control signals ($V_g$ and $\overline{V_g}$).

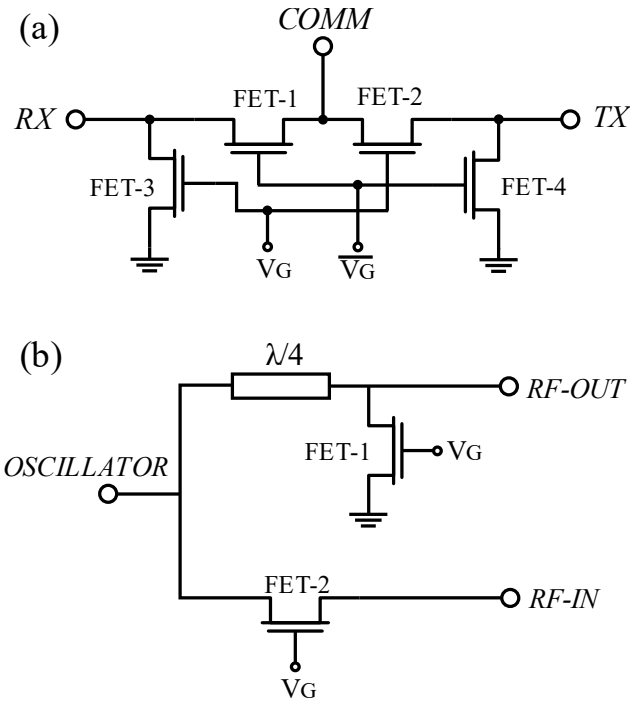


**Figure 3.13:** SPDT switch configurations: (a) standard approach (b) proposed approach.

It is simple to see that the switch connects COMM and RX ports when the series and shunt device in the arm "A" are in the low-impedance and high-impedance state, respectively; while as a consequence of the complementary control scheme, the series and shunt device in the arm "B" are in the high-impedance and low-impedance state, respectively. This way, the RF signal travels from the common port COMM to port RX, while good isolation with the TX port is guaranteed. Inversely, when COMM port needs to be connected to the TX port, the branch "A" must be set in high-impedance state and the branch "B" in low-impedance. This is accomplished by inverting the gate control signal $V_g$ and $\overline{V_g}$.

However, the presented switch architecture is not compatible with the relay node system when operates in rectifier mode. In fact, a compatible switch should be able to establish a port connection between RX and COMM ports even if no gate bias is applied (condition with $V_{ST} = 0$ V). This is not possible with the architecture in Fig. 3.13(a). In addition, another important requirement for the switch is that the gate control voltage must be single and positive.

To overcome the above-mentioned issues, a custom switch has been designed and it is illustrated in Fig. 3.13(b). It is a modified approach with respect to Fig. 3.13(a) and involves one series and one shunt FET as well as an impedance inverter ($\lambda/4$). Note that the resulting switch architecture is asymmetric. Such asymmetry allows us to reduce the control gate signals from two complementary voltages ($V_g$ and $\overline{V_g}$) to one voltage (single biasing) and, consequently, now it is possible to have a port connection even with $V_g = 0$ V.

Fig. 3.14(a) and Fig. 3.14(b) show the RF paths of the switch when the relay node is in transmitting and receiving mode, respectively. When

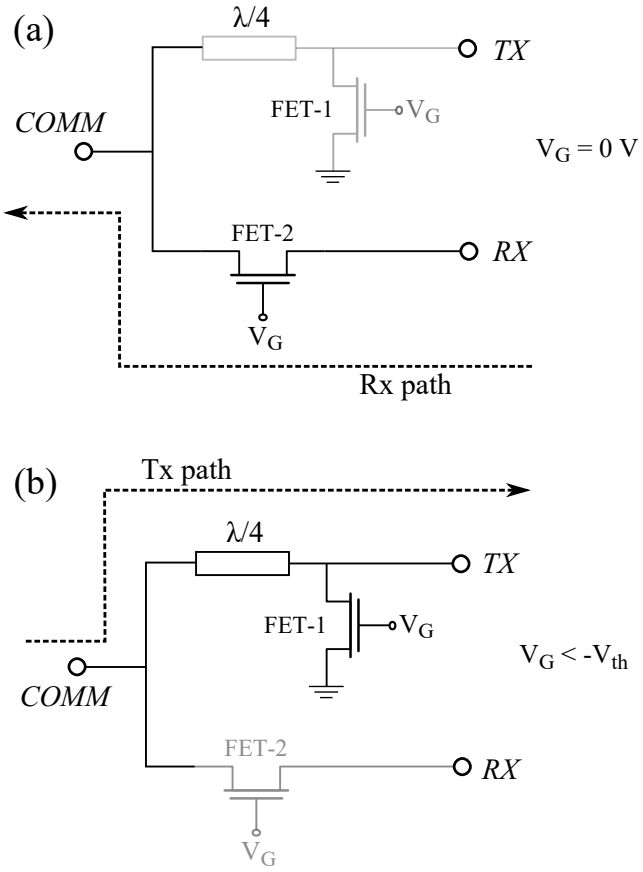


**Figure 3.14:** Proposed switch behavior: (a) RX mode, (b) TX mode.

the system operates in receiving mode, no energy is available from the storage elements and the gate-to-source voltage of each FETs is 0 V. Consequently, the receiving path presents a low insertion loss, whereas the transmit path results to be isolated because of the quarter-wave line. This transformer has the objective to transform the low-impedance value offered by the shunt transistor (FET-1) into a high-impedance value.

When the system is in transmitting mode, a non-zero $V_{ST}$ is available and the transistors can be driven (Fig. 3.14(b)). In this case, both the FETs are in OFF state offering a high channel impedance. Thus, the receive and transmit paths are now open and closed, respectively. In Fig. 3.14(b), the isolated path is highlighted in gray. Note that, the impedance transformer acts now as a standard transmission line with

characteristic impedance $Z_0$. However, the architecture in Fig. 3.14(b) still requires a negative voltage to drive the transistor ON/OFF.

To drive the transistors with a positive voltage an alternative bias scheme has been adopted namely source-floating approach [47, 48]. In this case, a positive voltage is applied at the source pin of the transistor instead of the gate, generating a negative differential gate-to-source voltage. The final schematic of the switch is shown in Fig. 3.15. It can be recognized the series and shunt configuration of the transistor with a proper re-arrangement to implement a positive biasing scheme. To minimize the insertion loss in the receive path, a three stacked FETs are adopted. Similarly, two shunt transistors in a stacked configuration are used in the transmit path to lowering the impedance when the devices are in ON-state. This way, a better isolation can be obtained when the relay node operates in rectifier mode.

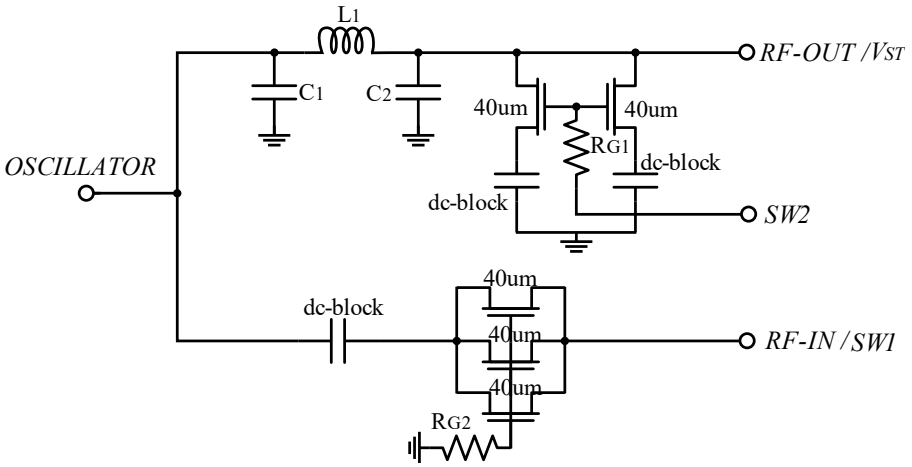


**Figure 3.15:** Final schematic of the proposed asymmetric switch.

Another important aspect is the impedance inverter implementation. At frequency of few GHz, distributed elements strongly impact on the occupied space and a lumped elements approach is preferred. In fact, at 2.45 GHz the transmission line λ/4-long on GaAs is approximately 10

mm, which results too space expensive for a monolithic realization.
A Lumped-element impedance inverter is implemented by using a - network with two shunted capacitors and a series inductor. The design of this component requires to define the frequency at which we have the inverted impedance (phase shift of 90°) and the characteristic impedance $Z_0$ (50 Ohm). The following equations have been used to have a first approximated design of $L_1$ and $C_1$, $C_2$:

$$L_1 = \frac{Z_0}{2\pi f_0} \tag{3.1}$$

$$C_1 = C_2 = \frac{1}{2\pi f_0 Z_0} \tag{3.2}$$

The final simulations of the inverter carried out by a 2D EM simulator (ADS Momentum) suggested slightly modified values with respect to those derived from Eq. 3.1 and Eq. 3.2, consequently adjusted.
Fig. 3.16 shows the final layout: first of all, it is noteworthy that the RF input and output ports are either RF and dc coupled. The common port of the switch, highlighted in the figure, is internally connected oscillator. To reduce the occupied area, the inverter capacitors ($C_1$ and $C_2$ ) are made directly over via. Transistors are designed by eliminating the grounding vias from the pHEMT cells. This is the first step to obtain a 3-terminal device. The second step is to create the source floating conditions for the positive biasing scheme. This is performed by means of the capacitors $C_3$, $C_4$, and $C_5$. In addition, stacked FETs are arranged in the transmit (two FETs) and receive (three FETs) paths.

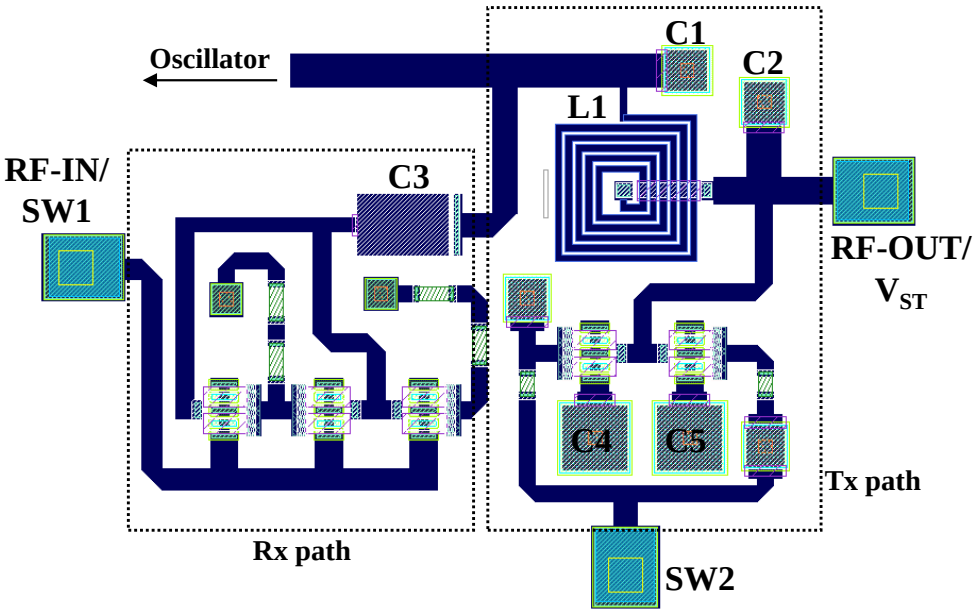


**Figure 3.16:** Final layout of the asymmetric SPDT switch.

Finally, it is possible to define the logic state table as detailed in Table 3.2.

**Table 3.2:** Logic state command of the switch

| State | SW1 | SW2 |
|---|---|---|
| Receive | 0 | $V_{ST}$ |
| Transmit | $V_{ST}$ | 0 |

Fig. 3.17 summarize the simulated insertion loss of the switch for both the receiver and transmit path. As it can be seen, the receiver path (gray line) has a flat response over frequency centered to 2.45 GHz. At this frequency, the insertion loss is 1 dB. For the transmit path, the response is less stable over frequency. However, considering an oscillating frequency of 2.45 GHz, the archived insertion loss is 1.4 dB. Of course, both in rectifier and in oscillating mode, the presence of these losses reduces the overall efficiency with respect to what has been shown in Section 3.1.

In Fig. 3.18 the simulated return loss at the three ports are plotted. A good return loss (less than −10 dB) is guaranteed up to 3 GHz for the RF-IN port and Oscillator internal port.

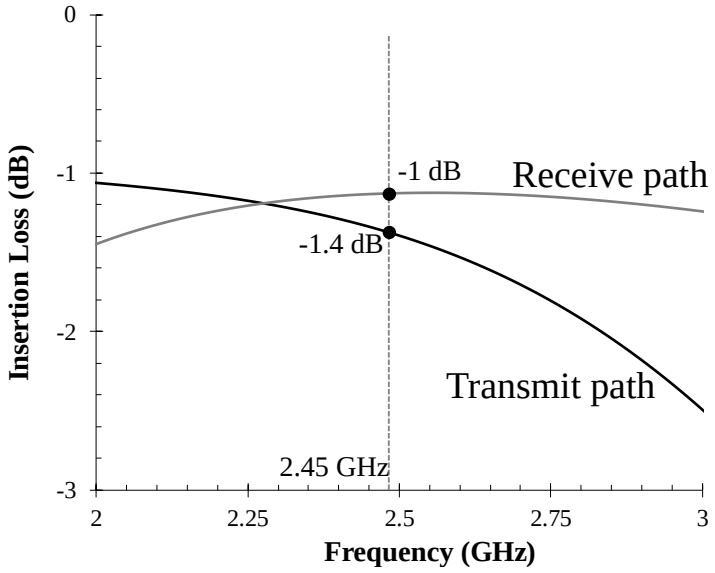


**Figure 3.17:** Simulated Insertion loss of the switch in RX and TX mode.

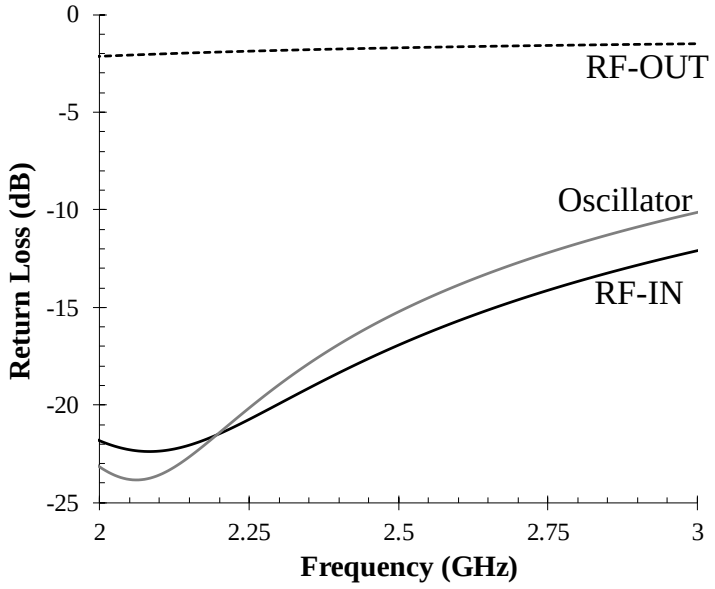


**Figure 3.18:** Simulated Return loss at all ports of the switch for the relay in RX mode.

Observe that, the proposed switch is reflective, which means that

the non-connected port has a very poor matching as can be observed in Fig. 3.18.

In Fig. 3.19 are plotted the simulated return losses when the relay operates in oscillating mode. A worse return loss is achieved in this state. In particular, at 2.45 GHz a $-8.5$ dB is obtained for the oscillator internal port and $-12$ dB for the RF-OUT port. Also in this case, the non-connected port has a very poor return loss which results higher than $-0.5$ dB over frequency.

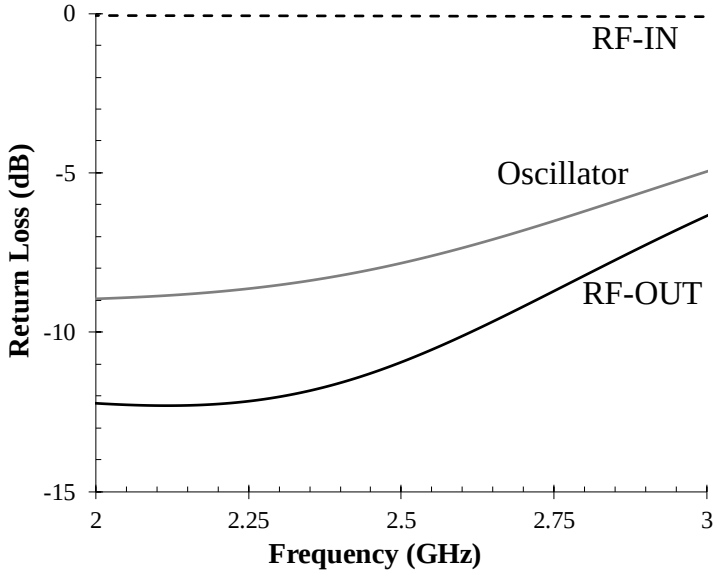


**Figure 3.19:** Simulated Return loss at all ports of the switch for the relay in TX mode.

## 3.5 Bias-Assisting Loop Design

The hybrid bias-assisting loop approach has been introduced and motivated in Section 3.2. As explained, due to the unavailability of optimized diodes in the PH10 technology, the best solution was to divide the bias-assisting loop in two sections (Fig. 3.20): the first one is the coupler and it is built on-chip, the second one is the gate rectifier externally implemented. With this approach, an optimum control of the rectification

process was obtained.

The first step of the design was the coupler of the bias-assisting loop. It is well known that directional couplers are difficult to realize in MMIC technology either with distributed or lumped elements. In fact, transmission lines require large areas especially at frequency of few GHz, while using lumped components, requires quite a few inductors, thus large area and losses.

In this work, we adopted a new scheme for implementing the coupler. Our goal was to design a non-linear coupler able to change its coupling factor (CF) with the power levels. Doing so, it is possible to improve the sensitivity of the relay node. The ideal coupler should behave as follows:

**a)** At low input power a low coupling factor is required (S13) to allow the available power to flow towards the external rectifier input port (P3 in Fig. 3.20). This generally means that the insertion loss on the main path is higher.

**b)** At higher power levels, the coupling factor could be higher because the available power to the rectifier is sufficient to generate the needed dc voltage. Increasing the coupling factor means reduce the insertion loss and thus increase the efficiency.

The starting topology of the coupler was a resistive power divider. Resistive power dividers are adopting two resistors, $R_1$ and $R_2$, to sample power from the primary path. In this work, an improved version of the resistive divider has been developed which is able to dynamically change its coupling factor as the input power varies.

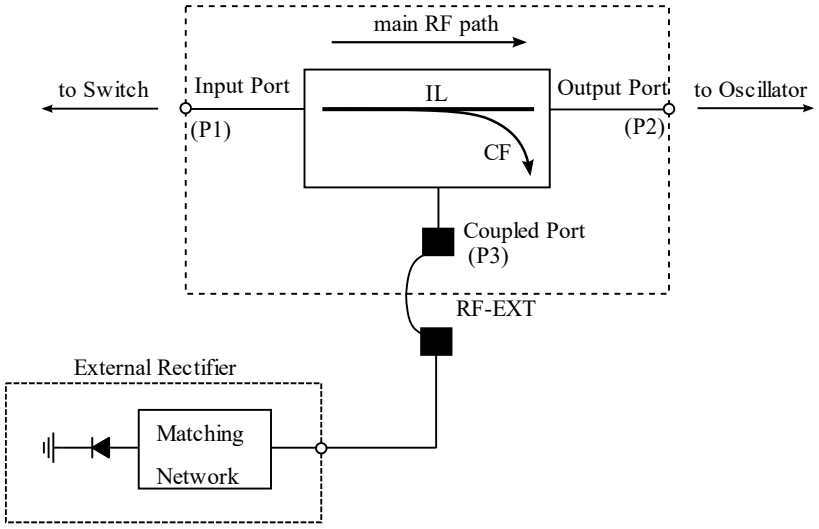


**Figure 3.20:** Hybrid approach for the bias-assisting loop implementation.

The proposed architecture is illustrated in Fig. 3.21 where the resistive element is implemented by using an active device (FET). Observe that, by tuning its gate-to-source voltage, it is possible to modulate the coupling factor (CF) of the coupler dynamically. The FET is connected to the external rectifier by means of a bonding wire technique. An important aspect to be underlined is that the gate of the transistor is now dc-coupled. This is done by choice, since it is the way the operating point of the FET is varied as the RF input power varies. In fact, the dc negative voltage generated by the external rectifier is feedback to the transistor's gate and in this way the coupling factor is modulated. In particular, when low power level is received, the gate-source voltage is going to zero. In this state, the FET channel resistance is low, and more power is provided to the rectifier, increasing the sensitivity. Of course, the insertion loss in this state is lower.

On the other hand, as the power level increases, a more negative voltage is generated by the external rectifier and the FET channel resistance is increased. As a result, the coupling factor and the insertion

loss decrease, and the relay node efficiency improves. Fig. 3.21 shows the bias assisting loop schematic. Note that, in order to improve the rectified voltage, instead of using a voltage multiplier, we adopted a configuration with two series diodes.

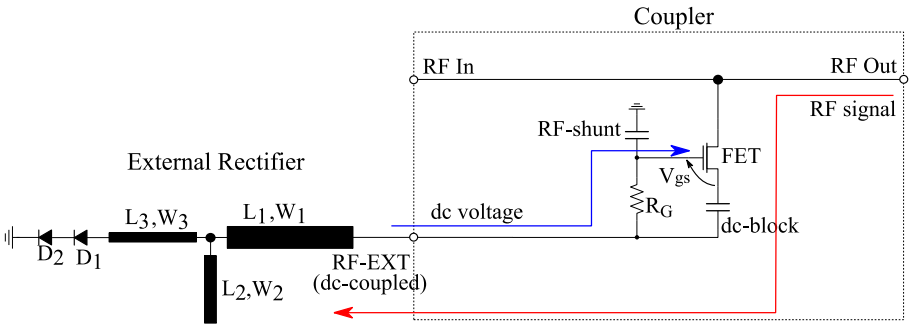


**Figure 3.21:** Final schematic of the proposed hybrid bias-assisting loop.

The optimization process of the external rectifier accounted for two aspects:

**i)** relay node sensitivity,

**ii)** relay node efficiency.

The final optimization involved the external rectifier only and the lengths $(L_i)$ and widths $(W_i), i = 1, \ldots, 3$ of the transmission lines were optimized. Of course, the bonding wire effect was considered during the process.The optimization goals were:

1. Maximize the dc output voltage for power as low as $-5$ dBm.
2. Insertion loss higher than $-1$ dB for RF input power higher than $-3$ dBm.
3. Guarantee a return loss better than $-10$ dB at the RF-IN port.

Fig. 3.22 shows the final layout arrangement of the coupler. The RF-EXT port of the coupler is highlighted in the figure. A 6-finger transistor

was used with finger width of 20 μm. The source floating is obtained by connecting the source to $C_1$, whereas capacitor $C_2$ and resistor $R_1$ and $R_2$ are used to create a RF choke at the transistor's gate.

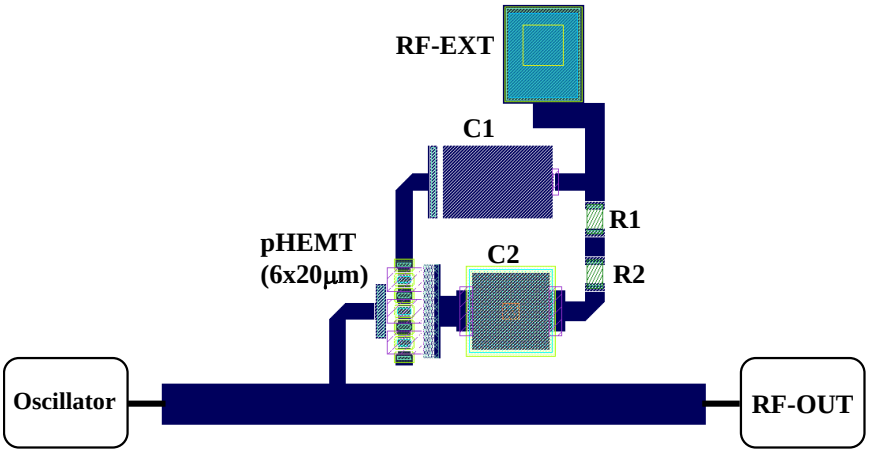


**Figure 3.22:** Final layout of the coupler.

Fig. 3.23 shows the simulated insertion loss and coupling factor behavior versus the input power level: the non-linear behavior of the coupling factor is clearly demonstrated. Specifically, at low power levels (i.e. $-10$ dBm) the coupling factor is$-6$ dB and the insertion loss is $-1.5$ dB. As it will be seen in the next section, this coupling is sufficient to guarantee the start-up of the relay node in rectifier mode. As the input power increases, the coupling factor increase, and the insertion loss reduces. The insertion loss become less than $-1$ dB when the input power is higher than $-7$ dBm.

Instead, Fig. 3.24 shows the simulated return loss against the RF input power. Less than 15 dB of return loss is guaranteed for input power levels higher than $-11$ dBm. This ensure that the oscillator and the switch will continue to operate properly even if the coupler is connected between these two subsystems.

Finally, Fig. 3.25 illustrate the simulated negative dc voltage. Note

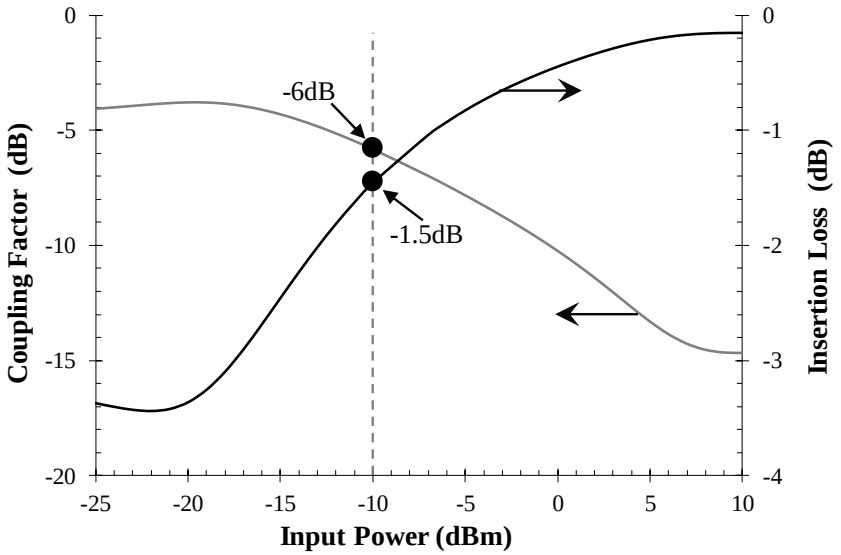


**Figure 3.23:** Simulated coupling factor at 2.45 GHz and insertion loss for the coupler in Fig. 3.21, against RF input power.

that, at $-10$ dBm the rectifier provides a $-220$ mV voltage, which results sufficient to start the rectification process of the oscillator.

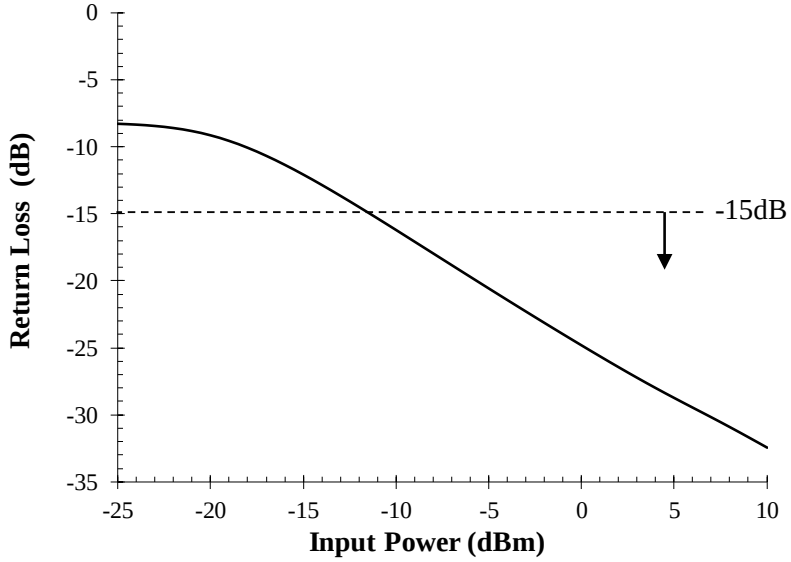


**Figure 3.24:** Simulated return loss of the bias-assisting loop at 2.45 GHz against RF input power.

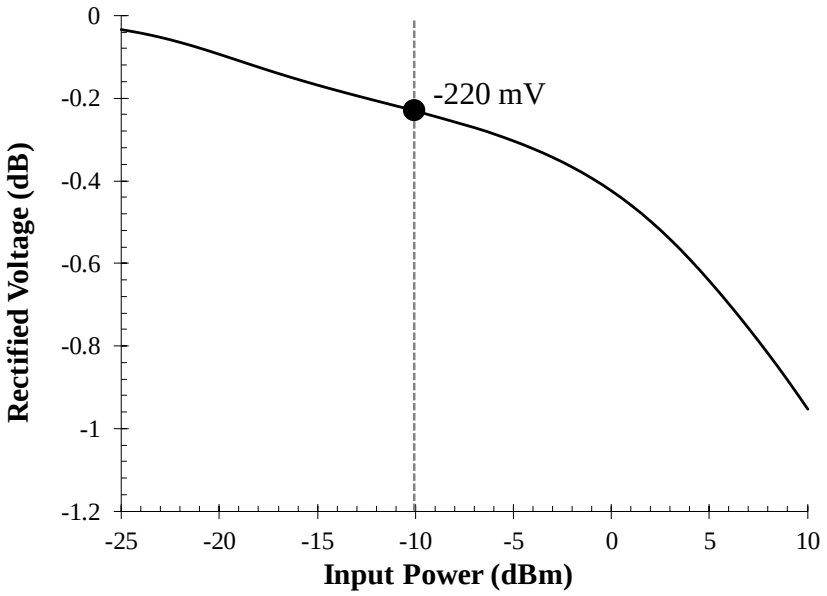


**Figure 3.25:** Simulated rectified dc-voltage by the external rectifier against input power.

## 3.6 Experimental Results

In the previous sections we have seen the topologies and related design procedures of the single sub-blocks of the monolithic system.

This section is dedicated to illustrate the final prototype and its experimental characterization. Fig. 3.26 shows the final schematic of the MMIC as anticipated in Section 2.1. It can be recognized the oscillator, the FET-based coupler and the SPDT switch as explained in previous sections.

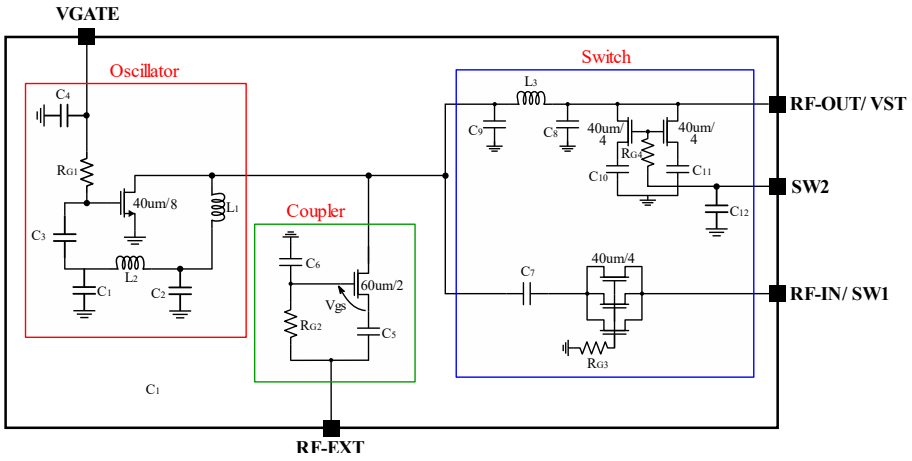


**Figure 3.26:** Final MMIC schematic.

The lumped elements values of the final version are listed in Table 3.3. Note that a slight modification with respect to the first version of the oscillator is obtained. This was necessary because of the actual oscillator load. In fact, the effective load network is now composed of switch and coupler, and thus the load impedance is now different from an ideal 50 Ohm (as the case in Section 2.2).

In order to convert the schematic of Fig. 3.26 into layout to be fabricated, a commercially available CAD software was used (ADS Keysight software). In general, a series of design rules must have followed during the design of a MMIC layout, such as orientation, device spacing,

probe and pad placement, etc. These design rules are provided from the foundry and they are strictly related to the technology process. By using CAD software, it is possible to run automatic analysis able to detect violations of the design rules.

**Table 3.3:** List of values of the lumped component used in the MMIC.

| Component | Function | Value |
|---|---|---|
| L1 | Oscillator | 4 nH |
| L2 | Oscillator | 4 nH |
| L3 | Switch | 4.2 nH |
| C1 | Oscillator | 1 pF |
| C2 | Oscillator | 1 pF |
| C3 | Oscillator | 2 pF |
| C4 | Oscillator | 4 pF |
| C5 | Coupler | 4 pF |
| C6 | Coupler | 4 pF |
| C7 | Switch | 4 pF |
| C8 | Switch | 1.1 pF |
| C9 | Switch | 1.1 pF |
| C10 | Switch | 4 pF |
| C11 | Switch | 2 pF |
| C12 | Switch | 4 pF |
| RG1 | Oscillator | 750 Ω |
| RG2 | Switch | 2 kΩ |
| RG3 | Switch | 4 kΩ |
| RG4 | Switch | 2 kΩ |

The first step in the layout design is the definitions of the master frame: which consists of defining the pads placement and the components adjustment according to the design rules. Fig. 3.27 shows the master frame of my MMIC, fully compatible with the UMS design rules. The master occupies an area of $1.4 \times 1.4$ mm$^2$ and includes five ports as seen in Fig. 3.26. Note that, according to the foundry design rules, the area usable to design the layout is reduced to $1 \times 1$ mm$^2$.

Once the master frame is defined, the layout has been designed and it is shown in Fig. 3.28(a). Observe that, It is a rearrangement of the already presented layout of the single sub-block described in the previous

sections: all the components are implemented inside the usable area defined by the master frame that is highlighted in the figure. This is an important recommendation from the foundry in order not to destroy components such as capacitors, inductors and FETs, during the bonding and dicing operations.

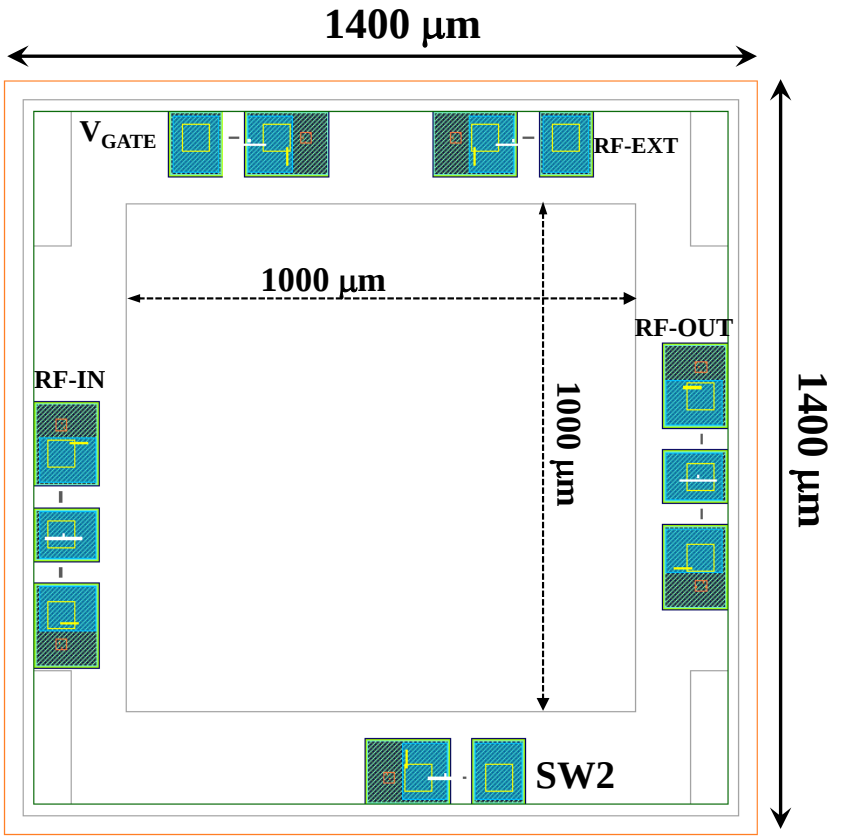


**Figure 3.27:** Master frame of the chip compatible with the UMS design rules.

Fig. 3.28(b) is a photo of the MMIC taken through the microscope. From this picture is possible to see the upper metallization layer as well as the air-bridge used to realize inductors. The final version of the layout was completed and the GDSII file delivered the to the UMS foundry on July $15^{th}$, 2016 . On October $25^{th}$, we received the dies from UMS inside a chip trays.

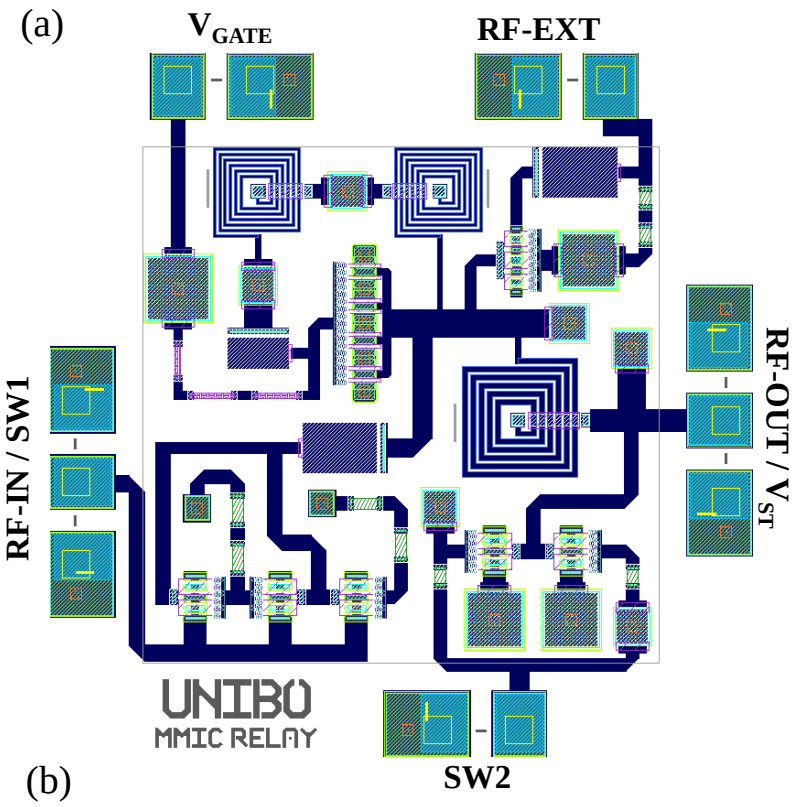


**Figure 3.28:** Final MMIC layout: (a) CAD layout, (b) microscope photo.

To test the realized MMIC, a test-jig carrier has been implemented. In a test-jig, chips and other circuitries are connected on the same carrier in order to make simple and fast measurements such as voltage/current tests, RF signal level measuring, resistance evaluation, etc. By following this approach, an inexpensive MMIC characterization was accomplished by using the chip-and-wire integration, in which the chip is attached directly on a microstrip substrate carrier (soft laminates in our case).

To attach the MMIC on the substrate an epoxy die attach method was used. This is the preferred attaching method in most monolithic applications, especially for low-power applications. There are several companies supplying die attach epoxies. For instance, Chemtronics manufactures a variety of die attach and microcircuit adhesives such as the CircuitWorks Conductive Epoxy (TDS # CW2400), which was used in this work.

Another important effect to be considered in the chip-and-wire approach is the parasitic inductance of the grounding pad. In fact, the MMIC is attached to a pad which is not at ground reference, but it is connected to the real ground by a series of via-holes. An inadequate number of vias or an erroneous positioning of them can result in a high inductance value for the MMIC RF grounding. This can lead to efficiency reduction of the oscillator as well as to a frequency detuning.

Fig. 3.29 shows the designed pad for the chip. Note that, the vias are all placed away from the MMIC ground. This is because it is necessary to have a very flat and clean surface of the pad in order to guarantee a good attaching process of the die. According to this, it has been designed a pad where the vias array is placed very close to the die but not onto its bottom side. The vias array is designed to minimize the parasitic ground inductance.

Other important issues, shown in Fig. 3.29, are the board-to-chip interconnections made via bonding wire technique. Of course, these wires introduce inductive effects associated to their length and height that need be accounted for especially when oscillator are concerned. The general rule is to make the connections as short as possible to reduce the inductive effect of the bond wire. The connections depend on the minimum lines spacing offered by the PCB manufacturer. In our case, an in-house fabrication has been made by using a commercial milling machine. According to the machine accuracy, a minimum spacing of 450 μm had to be respected. With this sapcing, the minimum attainable inductance is about 600 pH.

Due to the low operating frequency (up to 2.5 GHz), such value does not affect the RF behavior and the return loss and insertion loss was preserved. Different is the case of operating frequencies higher than 10 GHz where the parasitic inductances become comparable to the designed ones.

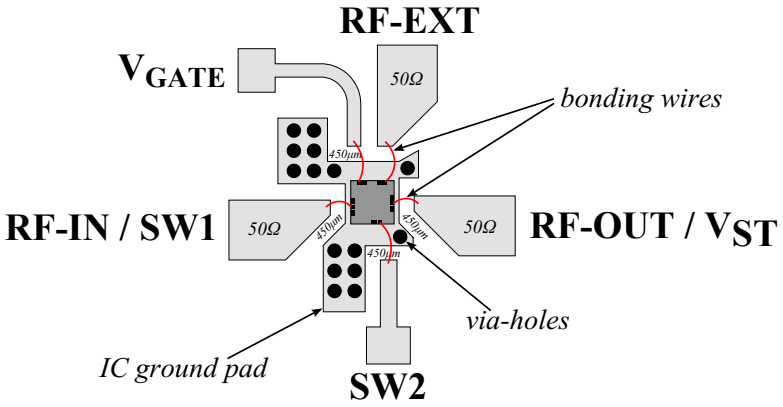


**Figure 3.29:** Adopted MMIC PAD with corresponding bonding wires.

The unpackaged MMIC relay node is soldered onto a carrier made on a 810 μm-thick RO4003 substrate from Rogers Inc. ($\varepsilon_r = 3.55$, $tan\,(\delta) = 0.0021$). Fig. 3.30 illustrates the schematic circuit of the test-jig board. The input and output ports of the board are directly connected to the

MMIC through dc-block capacitors. The external rectifier RF port is connected to the relay node, while its dc output is feedback to the gate pin of the MMIC. To control the RF switch, two ports are implemented on the board named SW1 and SW2.

The external rectifier implements a stepped-impedance open-stub matching network similar to that used in the MIC version of the relay node. Fig. 3.31illustrate the final prototype. A testing port is placed for tuning the matching of the external rectifier. The adopted SMD components are capacitors from Murata (GRM1885).

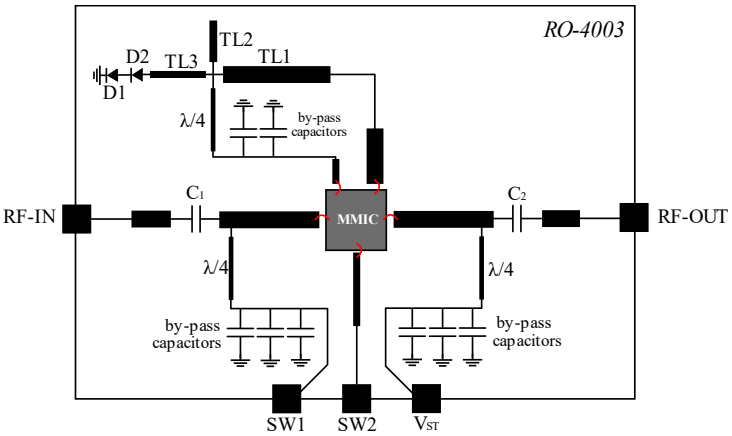


**Figure 3.30:** Schematic of the Test-Jig board.

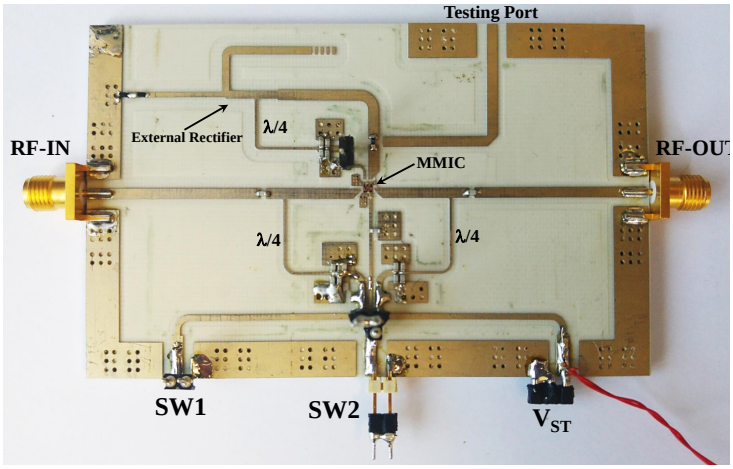


**Figure 3.31:** Picture of the Test-Jig board.

Finally, to experimentally validate the performance of the developed power relay node, measurements in both rectifying and power transmitting modes were carried out.

First, we started analyzing the system when it operates in rectifying mode.

The block diagram of the measurement set-up is shown in Fig. 3.32; the RF-IN port of the prototype is connected to the RF signal generator (HP B3752A), whereas the out port is connected to the RF Spectrum Analyzer (Agilent DPO72304DX).

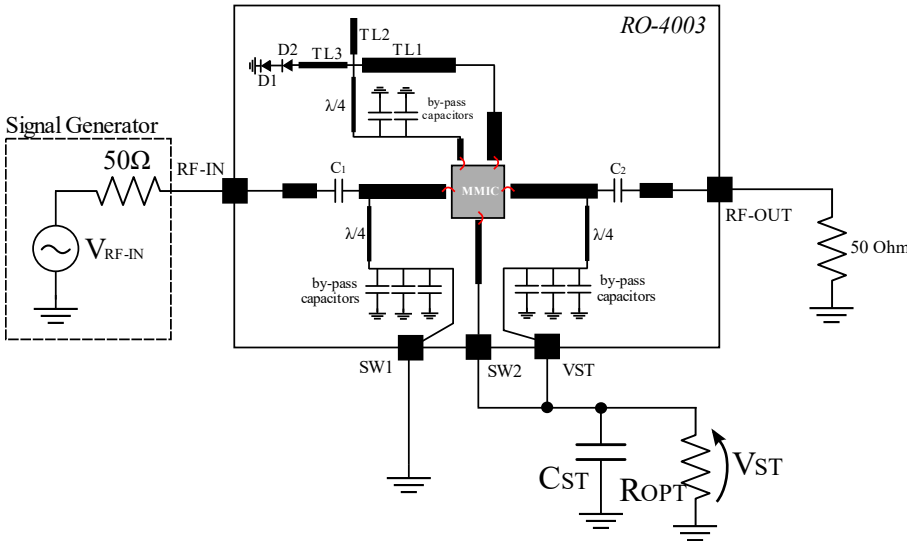


**Figure 3.32:** Set-up used for characterizing the MMIC relay node in RX mode.

The storage port ($V_{ST}$) is loaded with the optimum load (80 Ohm). As explained in 3.2, to configure the custom switch in receiving mode, port SW1 and SW2 must be connected to ground and to the storage node ($V_{ST}$), respectively. The selected storage capacitance $C_{ST}$ is 100 μF.

The measurement procedure is carried out in two steps:

**i)** adjust the RF power at the input ($RF - IN$),

**ii)** measure the rectified dc voltage across the optimum load $R_{OPT}$, and the dc voltage generated by the external rectifier.

The dc voltage measured is then used to derive the overall efficiency of the system. The input power has been swept from $-10$ dBm to $+10$ dBm. This represents the operating range of the designed relay node in receiving mode. Note that, for simplicity the same load is used here for all input power levels, while it slightly varies.

Figs. 3.33 and 3.34 show the final results for the set-up of Fig. 3.32. In Fig. 3.33 the dc gate voltage generated by the external rectifier is plotted against input RF power: the minimum activation voltage of$-0.22$ V is measured at RF input power of $-10$ dBm. However, the simulated activation power is $-8$ dBm, showing an improvements with respect to the simulation results. Moreover, a very good matching between simulation and measurement results are shown in Fig. 3.33.

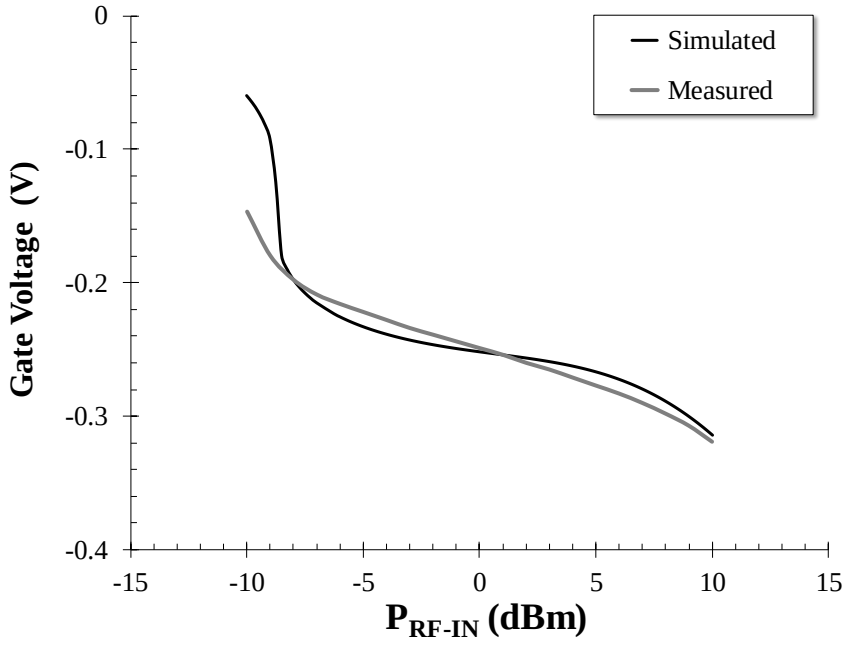


**Figure 3.33:** Gate self-bias voltage generated by the bias-assisting loop.

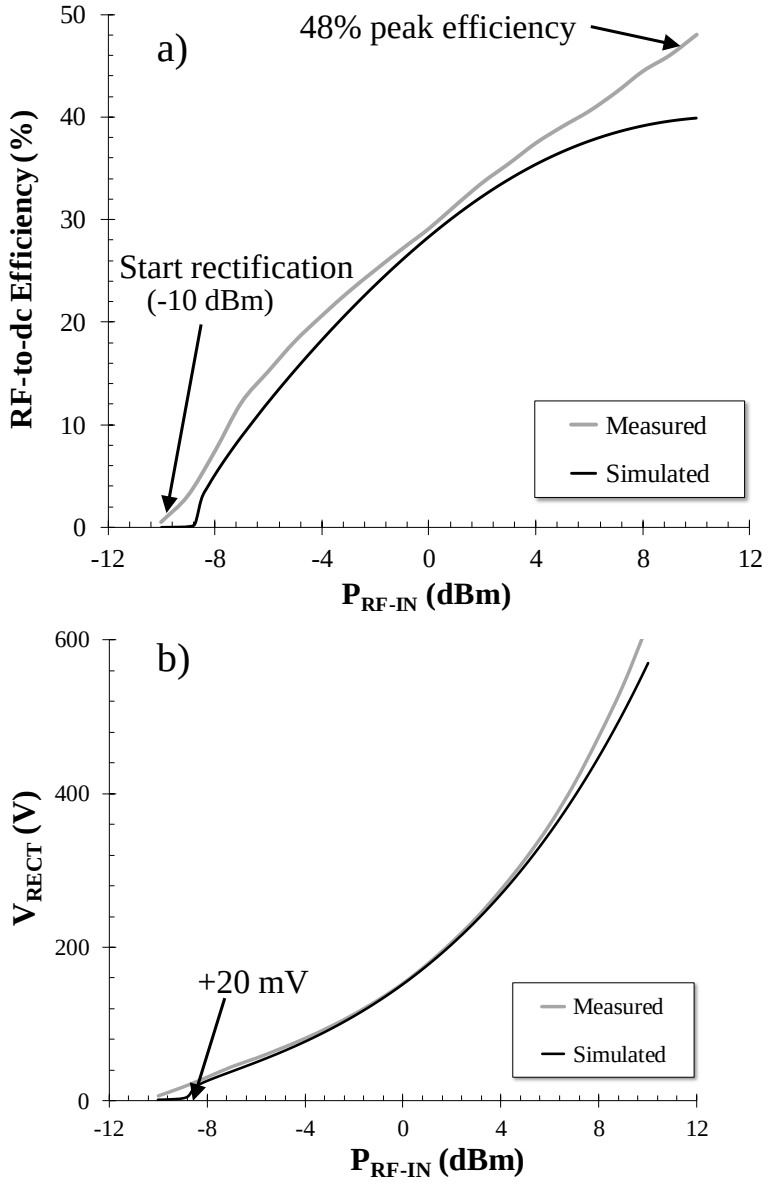


**Figure 3.34:** Measured and simulated RF-to-dc conversion efficiency (a) and output voltage (b) for the oscillator/rectifier circuit operating in rectifier mode.

The corresponding output dc voltage and RF-to-dc conversion efficiency are shown in Fig. 3.34. A measured efficiency better than 20% is obtained for RF power levels ranging from −4 to +10 dBm. A peak efficiency of 50% is reached at +10 dBm input power. It is noteworthy that, the presented efficiencies represent the performance of the entire

system considering oscillator, switches and coupler, and of course, they include all the losses of these sub-blocks. This means that the oscillator itself is running at higher conversion efficiency.
The rectified output voltage is about 20 mV when the input power is $-8$ dBm. This low value is associated to the low optimum resistance $R_{OPT}$ of the rectifier (80 Ohm), which results in a low output voltage even if the system efficiency is preserved.
Of course, due to these dc voltage levels of the relay node, dc-dc converters need to be used to step-up the voltage up to 2 or 3 V. In this work, I did not have time to realize this section that it will be arguments for future developments.

Finally, thanks to the bias-assisting loop, the minimum voltage required to start the rectification is reached with a RF input power as low as $-10$ dBm. Based on the previous measured performance, the power budget of the link between the RF source and the relay node can be obtained, assuming free-space propagation. For reader and relay node antenna gains of 7 dBi and 10 dBi, respectively, with 1 W transmitted power, the maximum distance to guarantee $-10$ dBm input power to the relay node is about 7 m. This represents with respect to the results shown in the previous chapter.

As last point of this chapter, to experimentally characterize the circuit in oscillator mode an external bias is used to provide drain polarization (due to the absence of a proper dc-dc converter). The output power levels are measured by using a spectrum analyzer connected to the RF-OUT port. The drain voltage is controlled by measuring the voltage across the storage capacitance $C_{ST}$. Fig. 3.35 shows the measurement set-up. Note that, the port SW1 and SW2 are now connected in a different manner with respect to the rectifier mode. Particularly,

SW1 is connected to the drain voltage and the is connected to a voltage divider ($R_1 = R_2 = 100$ kΩ).

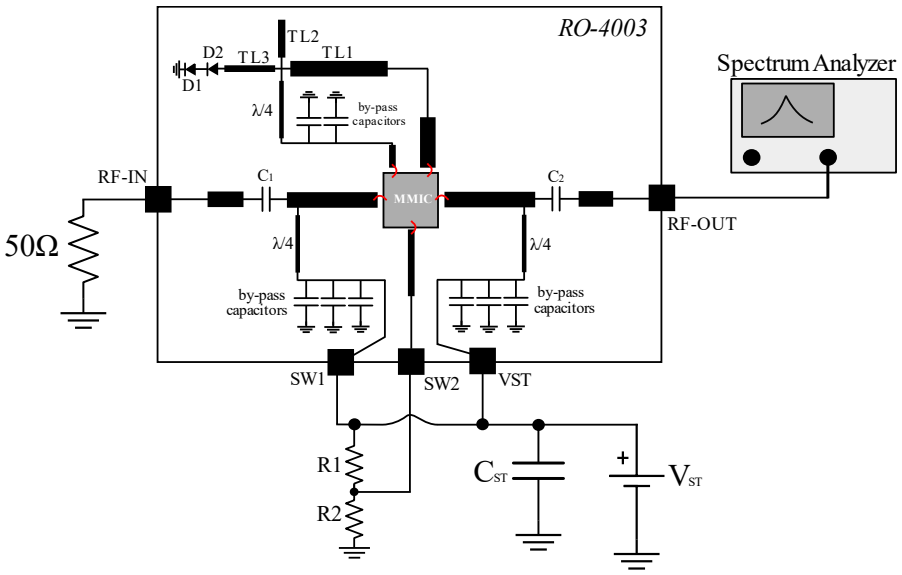


**Figure 3.35:** Set-up used for characterizing the MMIC relay node in TX mode.

In Fig. 3.36 the measured dc-to-RF conversion efficiency and oscillator output power are compared to the simulated ones with varying drain supply voltage. The overall efficiency is over 45% for the entire drain supply range starting from 0.8 V up to 3.2 V. The oscillator mode has a maximum dc-to-RF conversion efficiency of 47% at 2.4 V drain bias voltage and a maximum output power of 16 dBm (Fig. 3.36). As already explained, this efficiency represents the overall system performance. Thanks to the very good measured results, it can be supposed that the standalone oscillator is working with a simulated efficiency equal to what declared in Section 3.3 (about 55%).

Fig. 3.37 shows the oscillation frequency variations with the drain bias as the tuning variable. A variation of 100 MHz is observed over the $V_{DD}$ range. From the shown results, it has been demonstrated that the node can operate continuously without a battery, and it presents

the same efficiency at 2.4 GHz in rectifier (power-receive) mode and oscillator (power-transmit) mode. The receiver starts operating at input power levels as low as −10 dBm and remains in a robust oscillatory regime over a wide range of drain supply voltages.

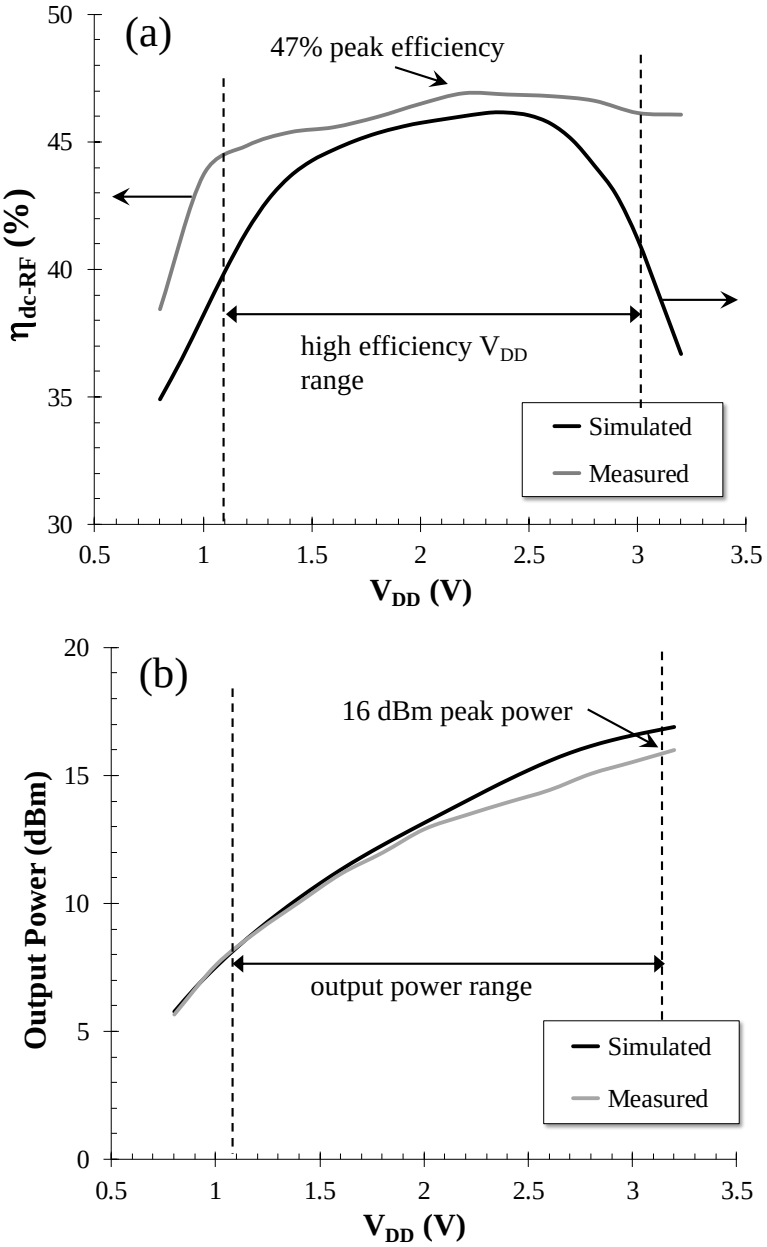


**Figure 3.36:** Measured and simulated dc-to-RF conversion efficiency (a) and output power (b) for the oscillator circuit operating in oscillator mode, as a function of the drain bias.

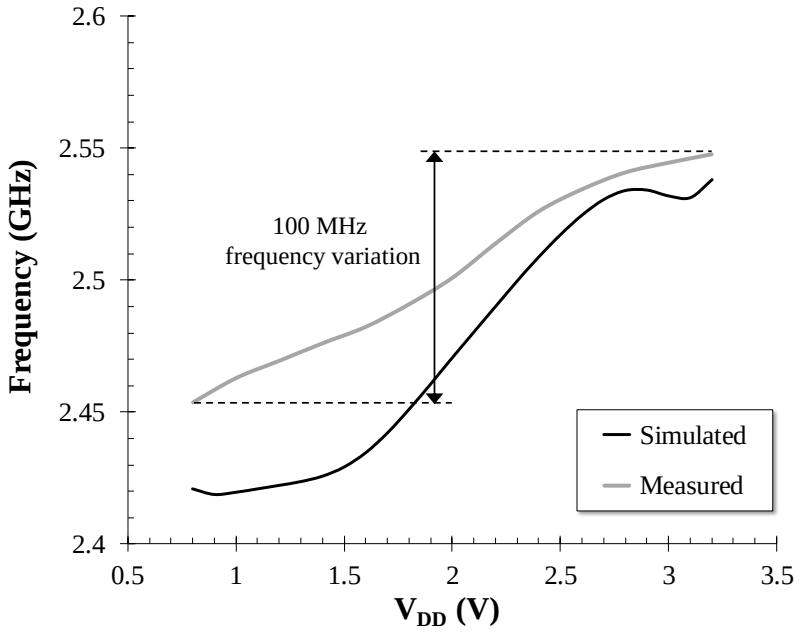


**Figure 3.37:** Simulated and Measured oscillator frequency variation versus drain voltage.

## 3.7 Conclusion

The aim of this chapter was to demonstrate the feasibility of using a GaAs monolithic technology in order to develop a 2.45 GHz MMIC relay node.

It has been first introduced the selected technology showing the main characteristic of the PH10-10 process. After that, an in-depth analysis has been done about the architecture of the system and the operation principle. it has been introduced the multiport and the hybrid bias assisting loop concepts.

Then, a theoretical design of the oscillator and related simulated results are discussed, demonstrating that a 55% dc-to-RF efficiency and a maximum output power of +18.5 dBm are archived exploiting a compact dual stage L-C feedback network for the oscillator. In this case, the efficiency of the oscillator is associated to the reduced angle of conduction, only. Such conduction angle is set by exploiting the gate self-bias mechanism. Based on the previously demonstrated time-reversal property, the corresponding rectifier is obtained and corresponding performances shown. An efficiency of 57% is reached, similar to that found for the oscillator, confirming once again, the TDR principle.

However, even in the MMIC implementation of the oscillator, the simulated rectification operation starts at relatively high power (+1.1 dBm). To overcome this problem has been adopted the bias-assisting loop. The proposed architecture of the bias-assisting loop includes an on-chip coupler realized with a FET transistor. The rectification is then performed by an external rectifier connected to the chip. The FET-based coupler permits to control the coupler factor (CF) by exploiting the negative voltage generated by the rectifier.

After this, an asymmetric SPDT switch is proposed and the design

procedure discussed. Thanks to the asymmetric architecture, the switch allowed us to have a default port connected even in absence of external voltages. This is a fundamental benefits for the relay node operations and it cannot be performed by using tradition SPDT architectures. In the designed switch, a maximum insertion loss of $-1.4$ dB is obtained for both TX an RX paths of the switch.

Finally, a MMIC prototype and the corresponding test-jig board are discussed. By using the test-jig a measurements campaign for characterizing the MMIC has been carried out. Measured and simulated results for the 2.45 GHz monolithic prototype are in very good agreement, demonstrating the feasibility of the device with GaAs processes. The entire measurements campaign has demonstrated the realizability of the proposed system both in term of bidirectional operation (transmit and receive) and in term of system efficiency.

# Chapter 4

# Simultaneous Wireless Information and Power Transfer (SWIPT)

The objective of this chapter is to describe a novel solution for portable devices to exploit their existing communication antennas for bi-directional near-field wireless re-charging, without compromising their far-field performances. To demonstrate this concept, the GSM 900/1800 MHz and the IMS 433 MHz bands are adopted for the far-field communication and for the near-field wireless recharging, respectively.

The contribution of this work is basically to validate the maximum reachable power transfer efficiency that can be obtained by using a typical personal digital assistant (PDA) antenna. The studied architecture is able to simultaneously ensure data communication at higher frequency bands and wireless re-charging at lower frequency band. As a proof-of-concept, a system prototype is built: the obtained RF-to-dc link efficiency measured. Such measurements demonstrate that wireless charging and communication can be exploited at the same time, without

limiting the respective communication capabilities.

This work was presented at the Wireless Power Transfer Conference (WPTC), Boulder, CO, 2015 [49]. A significantly extended version, including the experimental verification of a realized proof of concept, version of this work has also been produced and published at the IET Microwaves journal, Antennas & Propagation journal [50]. The current chapter is partially extracted by these papers.

The remaining of this chapter is organized as follows. Section 4.1 provides an overview of WPT link implemented by using antennas belonging to typical PDAs. Section 4.2 overviews the proposed architecture for portable devices. Section 4.3 and 4.4 discusses the co-design of the antenna and nonlinear system: starting from the antenna design, a diplexer and a WPT network topologies are then derived; Section 4.5 describes the measurement set-up and the final results. Section 4.6 drives the work conclusions.

## 4.1 Introduction

With the increase of wireless applications and communications technologies exploiting several frequency bands, portable devices are already equipped with complex antenna structures to comply with several wireless operations and there is an increasing interest in including near-field communication (NFC) capabilities and wireless power recharging [51]. An example of application that explains the basic idea is illustrated in Fig. 4.1. Two devices that, placed close to each other, can transfer power as they need.

This application poses the problem of minimizing interference among them [52] to ensure a safe simultaneous operations. To face this aspect, it is interesting to exploit the near-field operation of the antenna(s) al-

ready available in a PDA for wireless recharging or NFC.


**Figure 4.1:** Example of application of two near-field PDA devices for recharging operation (source: www.taptrack.com).

The use of reactive fields [53, 54, 55] reduce the electromagnetic interference and adds security to communications. However, the exploitation of the reactive fields (near-fields) must be complying with a number of challenges. In fact, they need to be simultaneously suitable for far-field (data communication) and near-field (power transfer) operations [56]. In the solution proposed in [57], wireless power transmission (WPT) by antennas coupled in the near-field is studied, and the power-transmission efficiency accounts for antenna dimensions and ohmic losses. Similarly, in [58], a 2.45 GHz monopole is considered for realizing near-field WPT to obtain high transfer efficiency, but the antenna is located in a dedicated docking support and no simultaneous near- and far-field activities are demonstrated.

Our contribution in this field is started from the preliminary studies provided in [59] which demonstrates the feasibility of simultaneous near-field and far-field exploitation of the same antenna in a PDA, without resorting to dedicated antenna design. Then, a demonstrator has been realized e tested to validate the system.

## 4.2 Antenna Feeding for Simultaneous Operations

Nowadays, PDAs and cell phones are overcrowded by several antennas to cover the GSM (900 MHz and 1800 MHz), UMTS (2150 MHz) and WiFi (2450 MHz) bands. Fig. 4.2 shows a typical antenna structure implemented in common mobile phones. This example shows the relevant level of integration present in mobile devices .

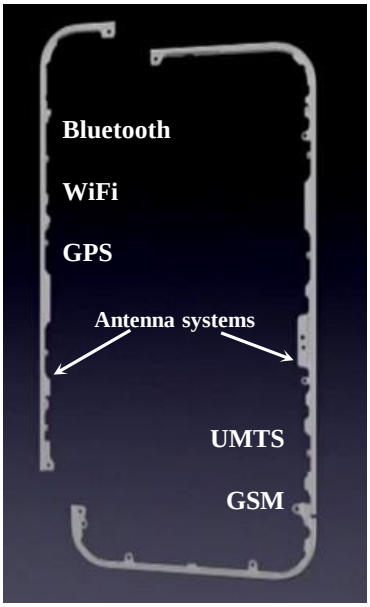


**Figure 4.2:** Example of embedded antenna in modern mobile phones (source: www.anandtech.com).

The basic idea introduced in this work is the exploitation of the available antennas in order to realize at lower frequencies a near-field link among different devices. This is very useful for re-charging or NFC purposes at the only condition that, of course, their far-field communication activities are not significantly affected.

This goal can be achieved by adjoining the antennas with suitable feeding network, to guarantee the co-existence of such different wireless operations (at the related operating frequencies).

A schematic block diagram of one side of the proposed solution is shown in Fig. 4.3: it represents a mobile handset, which can be placed in close proximity to another one (the other side), to enable a reactive near-field capacitive coupling for WPT. At each antenna side, a three-port lumped-element antenna feeding-network is designed as a suitable frequency diplexer, enabling near-field power transfer and far-field data communication in a seamless way. The frequency separation, between far- and near-field antenna operations, allows a reliable design of a frequency-division antenna feeding network, which consists of a three-port diplexer, with high isolation between the WPT and communication ports and high forward transmission between each of them and the matched antenna port. For each distance, a near-field coupling mechanism is derived by full-wave simulation of the same link.This way, a model of two-faced antennas was derived to design a proper embedded network that maximizes the power transfer efficiency, while preserving the data communication performance.

Once defined the diplexer network, the system is completed with the WPT network and UHF transceiver. The first includes the RF-to-dc conversion block, when the system operates as receiver, or the dc-to-RF conversion block, when it operates as transmitter. In a typical application, one of the two sides operates as transmitter, while the other side works as receiver.

The UHF transceiver simply represents the TX/RX chipset used in the handled device to manage the data communications. This can operate indiscriminately with GSM, UMTS or WiFi protocols. As it will be shown in the next sections, one-way recharging has been considered but the reverse direction can be taken valid for symmetry reasons.

Since the primary purpose of the system is not WPT, the obtained near-

field transfer efficiencies are not as high as in dedicated systems, but still significant, considering that wireless recharging of PDAs is enabled by simply embedding the existing antenna system in a frequency diplexer, without further crowding the wireless device.

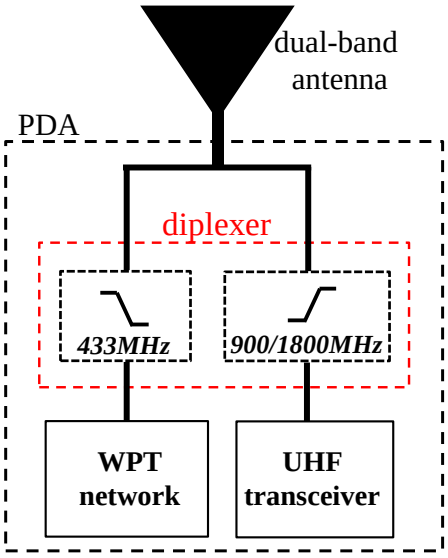


**Figure 4.3:** Schematic block diagram of the PDAs sub-system with the antenna for simultaneous far-field communication and near-field power transfer.

## 4.3 Dual-band Printed Antenna and Far-Field Performance

The first step is the antenna design. In this work we selected two dual-band monopole antennas, geometrically similar to those of modern mobile-phones, designed for covering the *GSM900* and *GSM1800* bands for communication and exploiting the 433 MHz ISM band for WPT purposes.

Printed antennas solutions are preferred for their light-weighted, compact size, ease of manufacturing, and ease of integration with the associated circuitry. Several topologies have been proposed to be compatible with the handsets shells, as multiband monopoles [60], PIFA [61] and

3D antennas [62].

In this work, a dual-band printed dipole layout similar to the one in [63] has been selected and it is shown in Fig. 4.4: it consists of a two-branch wire antenna, whose arms share the same 50 Ohm microstrip feeding line, and are printed on the ungrounded portion (light-blue in the figure) of a Taconic substrate RF-60A ($\varepsilon_r = 6.15$, $tan(\delta) = 0.0028$, $thickness = 0.635$ mm).

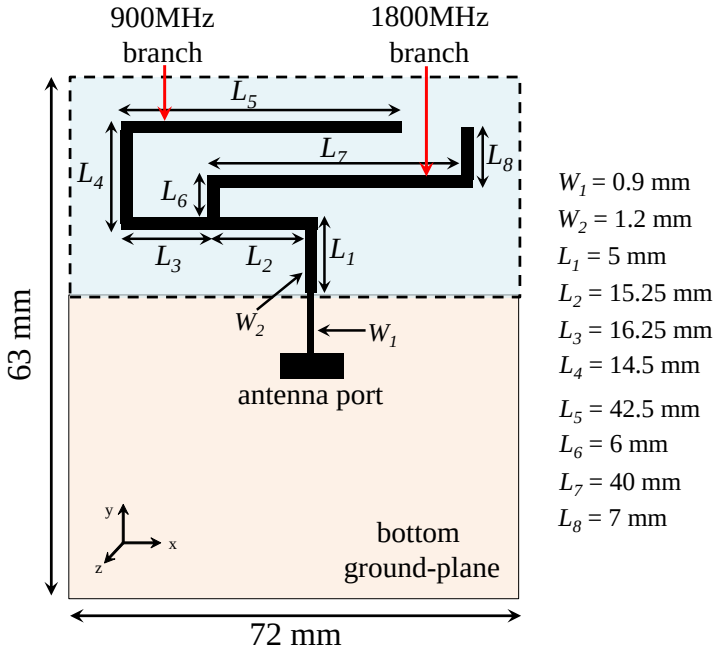


**Figure 4.4:** Layout of the printed dual-band dipole antenna and corresponding lengths.

Maximization of the radiation efficiency and minimization of port mismatching are simultaneously achieved by properly varying the design parameters. Low-directive behavior at both operating frequencies is searched during the design process, thus enabling antenna transmission/reception capability in a wide range of directions. No additional antenna optimization has been carried out for near-field operation at 433 MHz.

Note that, the chosen antenna topology is only one choice among a wide range of possibilities: this work aims to demonstrate the feasibility of the WPT operation exploiting strip-like antennas already available in modern PDAs.

A full–wave simulation of the standalone antenna in terms of input reflection coefficient and normalized radiation patterns are given in Figs. 4.5 and 4.6 by solid lines, while dashed lines represent measurements. Good agreement is observed in Fig. 4.5, with a reflection coefficient lower than −15 dB in the two bands: the slight frequency shift (100 MHz) in the upper band is probably due to mechanical tolerances in the prototype realization on the adopted thin and soft substrate. In fact, to build the prototype has been used a in-house milling machine not tailored for RF applications, and thus less accurate with soft laminates.

The comparison in terms of normalized E-field radiation patterns in the H- and E- planes is very satisfactory as well.

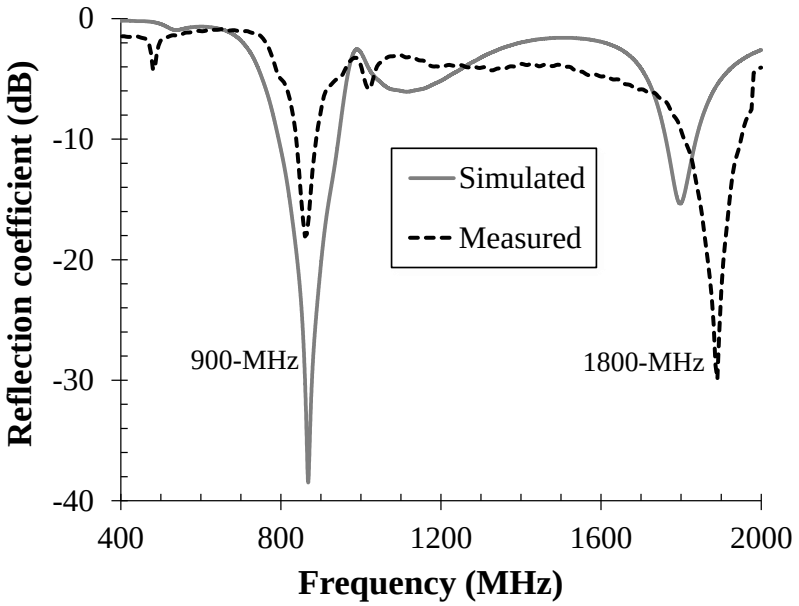


**Figure 4.5:** Simulated and measured reflection coefficient of the dual-band dipole antenna.

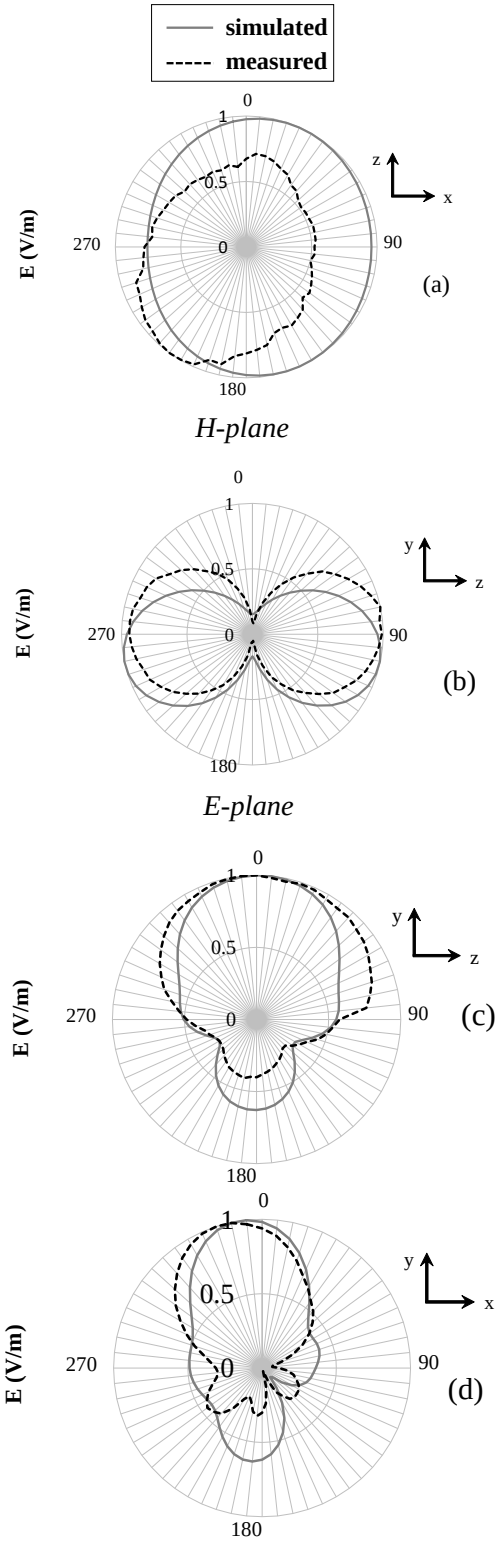


**Figure 4.6:** Simulated and measured normalized E-field radiation patterns in H-plane and E-plane of the standalone printed antenna at 900 MHz ((a) and (b)) and 1800 MHz ((c) and (d)) (linear scale).

From inspection of Fig. 4.6, the antenna radiation mechanism is easily retrieved: at 900 MHz the radiation pattern is almost omnidirectional in the H-plane (xz-plane), as expected from the y-aligned monopole behavior of the left antenna branch; a bit more directive pattern occurs at 1800 MHz because of the contribution of two x-aligned dipoles in a Yagi-Uda-like configuration.

## 4.4 Design of the Diplexer for Antenna Feeding

The circuit model of the proposed WPT system and of the antennas feeding are shown in Fig. 4.7. The link includes the transmitting and receiving antennas (connected with ports A1 and A2) fed by a three-port diplexer, as explained in the previous section. The architecture is conceived to simultaneously enable the dual-band communication at UHF, through ports 2 and 3, and wireless power transfer at 433 MHz, through ports 1 and 4.

The WPT path consists of a one-stage low-pass filter, and the communication path of a two-stage high-pass filter. The WPT branch also includes the proper network to resonate with the weak capacitive coupling (as that offered by the two small antennas of Fig. 4.4) to maximize the RF-to-RF power transfer efficiency ($\eta_{LINK}$), which is affected not only by the distance-dependent weakly-coupled link, but also by the Q-factor of the resonant networks. When a rectifier is connected to the receiving WPT port, the overall link conversion efficiency can be computed as:

$$\eta_{WPT-LINK} = \eta_{LINK} \cdot \eta_{RF-DC} = \frac{P_{OUT}^{WPT}}{P_{IN}^{WPT}} \cdot \frac{P_{DC}}{P_{OUT}^{WPT}} \tag{4.1}$$

where $\eta_{RF-DC}$ represents the efficiency of the rectifier, and $P_{IN}^{WPT}$,

$P_{OUT}^{WPT}$ are the RF powers at the input and output ports of the WPT path. Of course, $P_{DC}$is the rectified dc voltage. Thus $\eta_{WPT-LINK}$ depends on both the nonlinear behavior of the RF-to-dc converter and the achieved matching conditions of the resonant link.

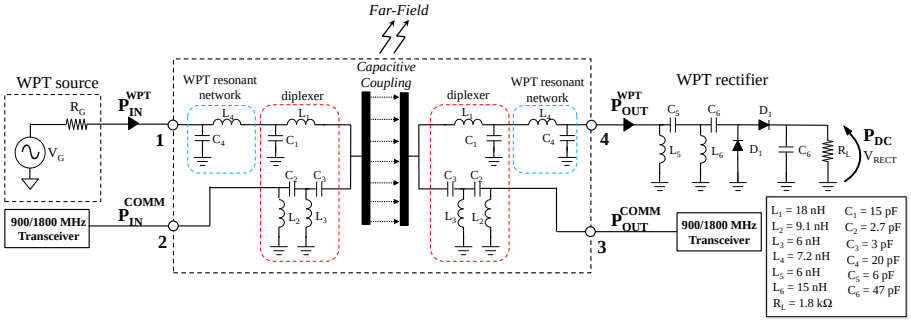


**Figure 4.7:** Circuit schematic of the entire dual-mode sub-system of two faced PDAs: the three-port diplexers, the components for a resonant capacitive WPT link, and the rectifier network at the receiving side are put into evidence.

The nonlinear circuit design of the link of Fig. 4.7 is carried out in two steps:

**i)** for all the considered distances, a unique resonant network is derived to maximize the power transfer efficiency (between ports 1 and 4) and to provide high isolation between the communication and WPT paths;

**ii)** a nonlinear optimization, simultaneously carried out at different power levels, defines the proper matching at 433 MHz between the full-wave rectifier and the input WPT port (port 1).

Power levels of the order of mW are considered for the present proof-of-concept design, in order to be able to validate it in our lab. However, the proposed design procedure can be straightforwardly scaled up to higher power levels by adopting the proper rectifying devices and matching networks.

A voltage-doubler topology, as in [64], has been chosen for the rectifier, to be matched to the resonant link by the lumped-element π-network of Fig. 4.7. Skyworks SMS7630-079 Schottky diodes have been used. The optimization is carried out in a 20 dB input power range (−10 dBm to +10 dBm) to properly model the power-dependent input impedance of the RF-to-dc converter, focusing on typical near-field WPT scenarios. All the lumped elements of the rectifier, including the load resistance $R_L$, are used as design variables.

It is noteworthy that, accurate modelling in the largest possible power range is mandatory since the rectifier input impedance is the resonant link load and it determines the overall efficiency (Eq. 4.1). For the same reason, accurate diode package parasitic models are needed, and those derived in [65, 66] are adopted in the present design.
Finally, the used SMD capacitors are Murata GRM1885 and the inductors are Coilcraft LD0402. The final circuit parameters are listed in Fig. 4.7.

## 4.5 Experimental Characterization

The two sides of the system of Fig. 4.7, including the dual-band printed antennas, have been fabricated on a Taconic RF-60A substrate ($\varepsilon_r$ = 6.15, *thickness* = 0.635 mm) and the photo of the prototype of one side of the link, with a separated rectifying section, is shown in Fig. 4.8.

A testing port has been added to measure the antenna performance in stand-alone configuration. First will be illustrated the results obtained using the WPT link. After that, it will be shown the performances from a far-field (UHF) point of view.

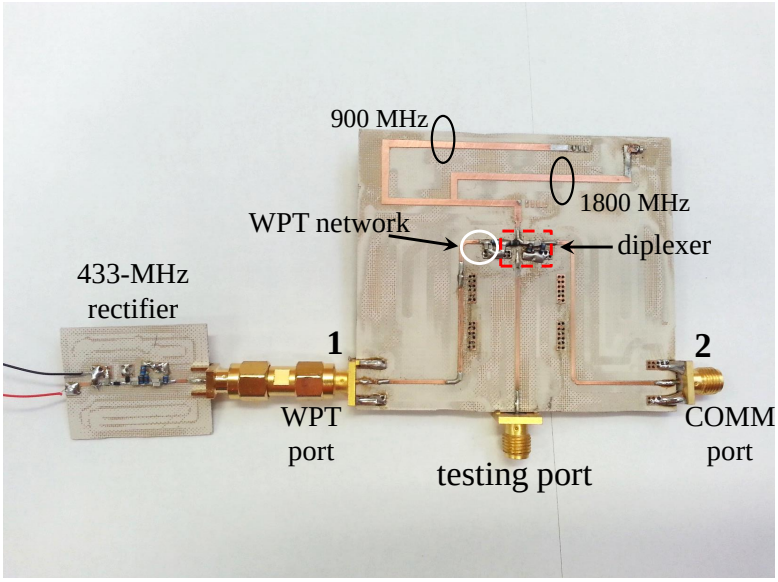


**Figure 4.8:** Prototype of the dual-band planar antenna system arranged for simultaneous data communication and energy transfer: the lumped-element diplexer, the resonant network and the rectifier are highlighted.

The results of the entire four-port network are shown in Figs. 4.9 and 4.10, in terms of scattering parameters.

In Fig. 4.9 the measured WPT to communication ports isolation (ports 1 - 2 or 3 - 4 of Fig. 4.7) is plotted versus frequency: at the communication frequencies isolation is better than 30 dB, whereas at the WPT frequency band it is better than 20 dB: this is not a concern

since the UHF transceiver of any PDAs is always equipped with a high-pass filter.

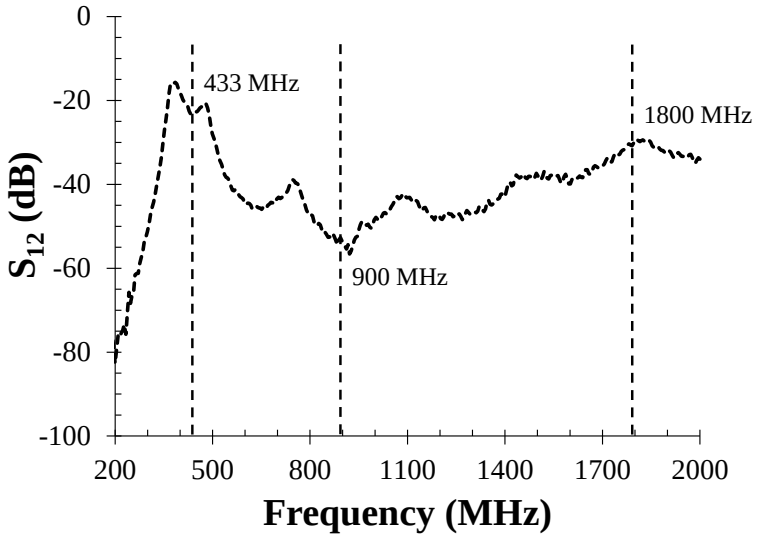


**Figure 4.9:** Measured isolation between ports 1 and 2 of Fig. 4.7 for the standalone antenna.

It can be concluded that simultaneous WPT at 433 MHz and communication at 900 and 1800 MHz, with the same antenna, can be accomplished by the proposed system configuration and a communication signal can be safely radiated by the antenna in the presence of the WPT path and vice versa.

Beyond these results, Figs. 4.10(a) and 4.10(b) shows the comparison between simulated and measured scattering parameters of the unique two-port WPT network (ports 1 - 4) for variable distances between the antennas: a good trade-off is obtained by the designed topology, the worst case being the 30 mm distance (S41 is only $-13$ dB). A 7% frequency shift between simulation and measurement is observed: it can be related to the average 5% tolerance of the commercial lumped element components and to the critical coupling capacitance which depends on the realized antenna pair geometry.

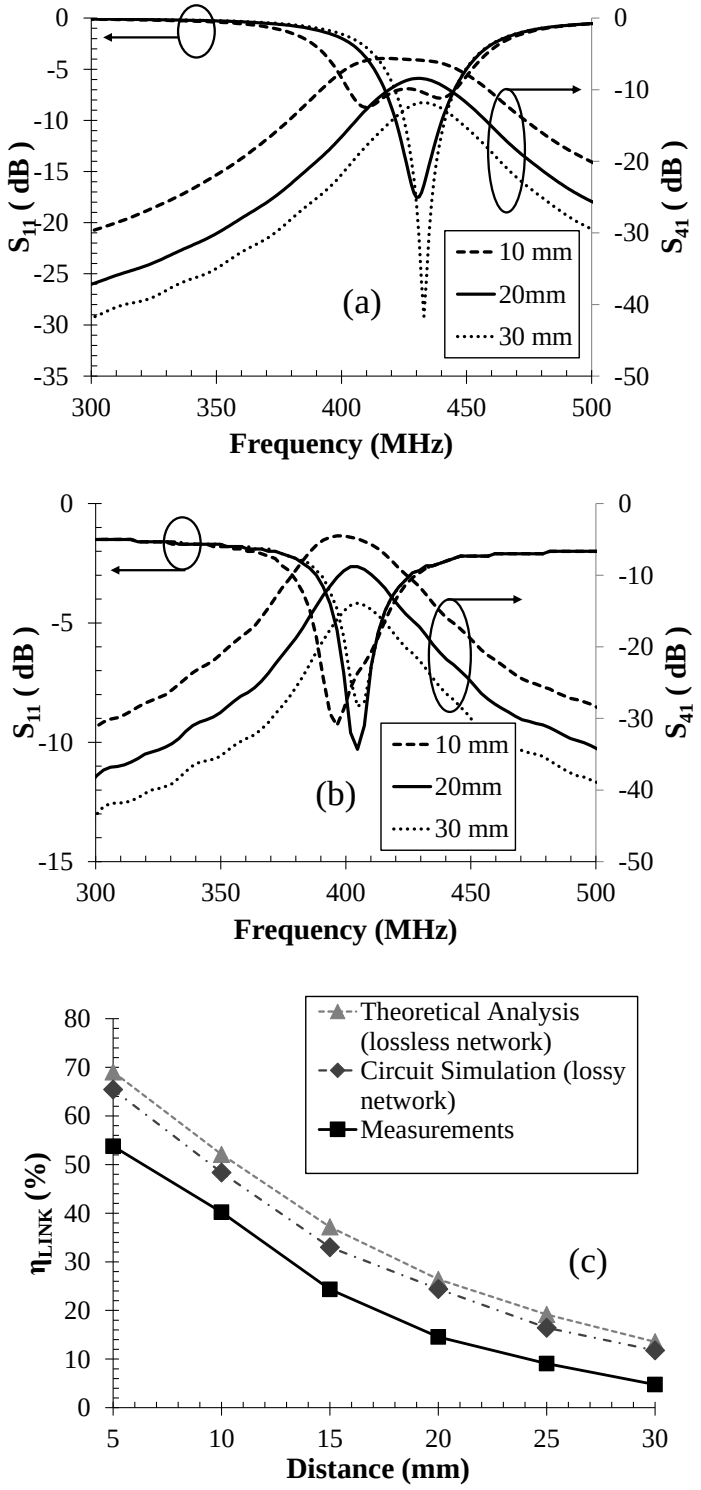


**Figure 4.10:** (a) simulated and (b) measured reflection and transmission coefficients for the two-faced antennas fed by the diplexer network (ports number as in Fig. 4.7). (c) predicted (with and without losses) and measured reactive link efficiencies for variable antenna distances, calculated through (Eq. 4.2).

In the Fig. 4.10(c) is shown the comparison of the link RF-to-RF transfer efficiency associated to the capacitive resonant link. This efficiency has been computed by using the measured and simulated four-port scattering parameters, by means of the following relation:

$$\eta_{LINK}(d) = \frac{|S_{41}(d)|^2}{1 - |S_{11}(d)|^2} \tag{4.2}$$

The ideal $\eta_{LINK}$, computed with lossless components and dedicated networks optimized for each antennas distance, is also superimposed in Fig. 4.10(c): an improvement of only 3 - 4% with respect to the simulated realistic situation is observed, which confirms that the proposed unique matching network can be effectively exploited.
Note that, the measured efficiency shows a 10% degradation, which is mainly due to the lower Q-factor of the adopted commercial components.

After analyzed the linear section of the link, let us now have a look to the non-linear performances. In Fig. 4.11(a) is shown the measured RF-to-dc conversion efficiency of the rectifier ($\eta_{LINK}$) as a function of the received RF power ($P_{OUT}^{WPT}$), while Figs. 4.11(b) and 4.11(c) report the measured $\eta_{WPT-LINK}$ and DC output power, respectively, as a function of the link input power ($P_{IN}^{WPT}$) with the antenna distance as a parameter: the shapes of these plots clearly show the nonlinear behavior of the rectifier.

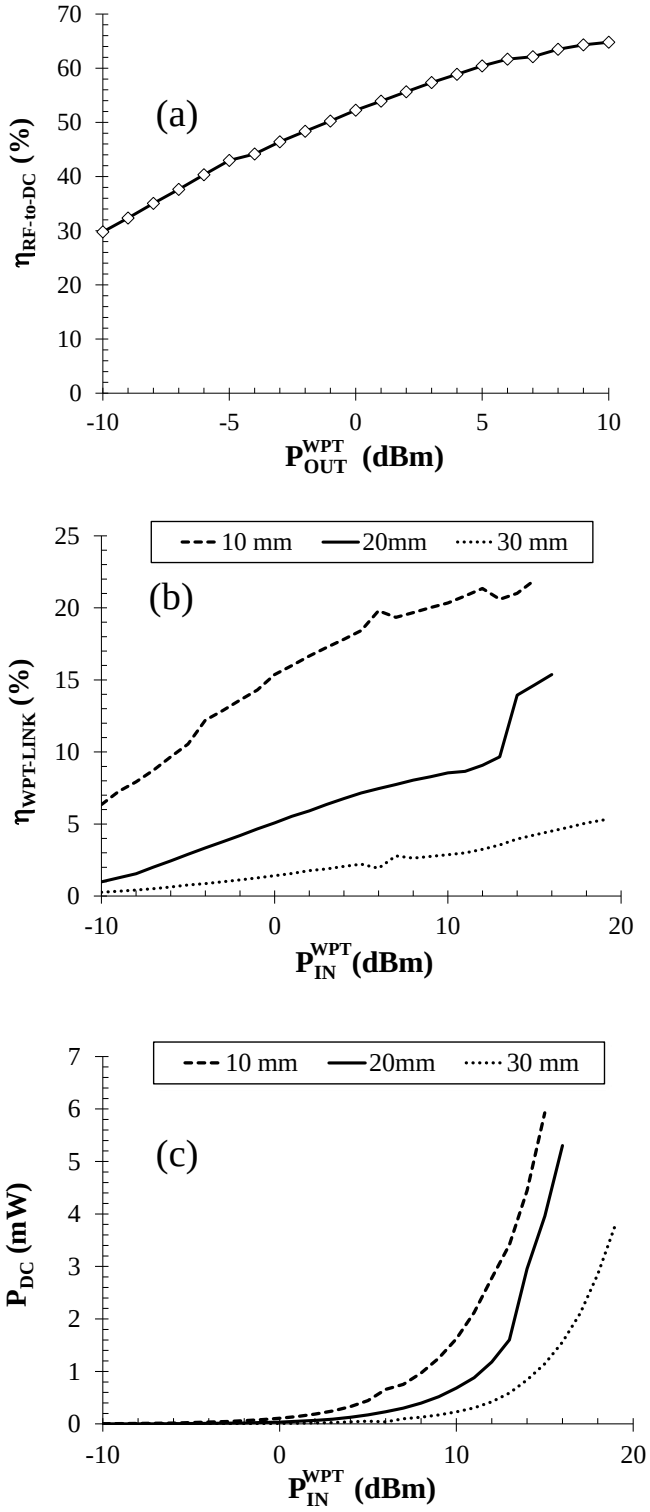


**Figure 4.11:** Measured RF-to-dc efficiency of the rectifier (a), overall system efficiency (b), and dc output power (c) for variable link distances.

When the portable devices are located 10 mm apart, the measured RF-to-dc link efficiency, from the link input power port to the rectifier dc output is better than 20%, for a transmitted power of only +10 dBm, while for greater distances it goes below 10%.

Of course, the use of strip-like antennas of different shape on each side of the link could bring to different performance: the effectiveness of this idea does not depend on the symmetry of the link, but on the creation of a weak reactive link between faced mobiles. In summary, so far we have validated the system and demonstrated that a considerable amount of power transfer efficiency can be obtained by exploiting existing and non-optimized antennas.

As last point, it is necessary to evaluate the effect that the WPT link has on the RF performances when the two PDAs are placed close. To evaluate this, first the antenna connected to the diplexer is characterized at UHF in standalone conditions. Then, the same antenna is faced to another one at the three distances: 10mm, 20mm, 30mm. Fig. 4.12 shows the measured reflection coefficient at the UHF port (port 2 in Fig. 4.7) and it confirms that the antenna matching is preserved. Note that, in this work a $-10$ dB return loss is considered suitable for the PDA operations.

Finally, the measured normalized radiation patterns are plotted in Fig. 4.13. They confirm that also the far-field properties are still guaranteed, even if even if they slightly worsen mainly for electromagnetic coupling reasons. This is also confirmed by the simulated antennas radiation efficiencies: from 98% and 96% at 900 MHz and 1800 MHz for the standalone antenna, to 45%, 52%, 59% and 54%, 61%, 73% in the two bands for the antennas faced at 10, 20, 30 mm, respectively.

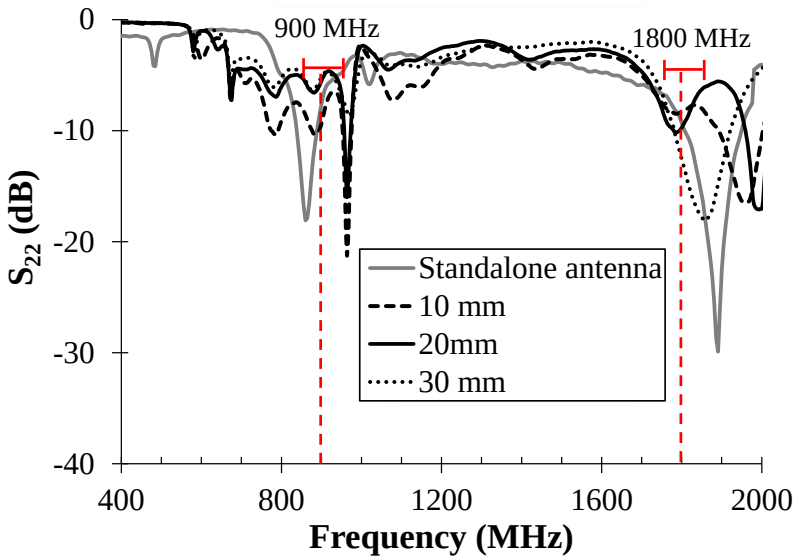


**Figure 4.12:** Input reflection coefficient at port 2 of Fig. 4.7, with standalone antenna and with a faced identical one, at different distances.

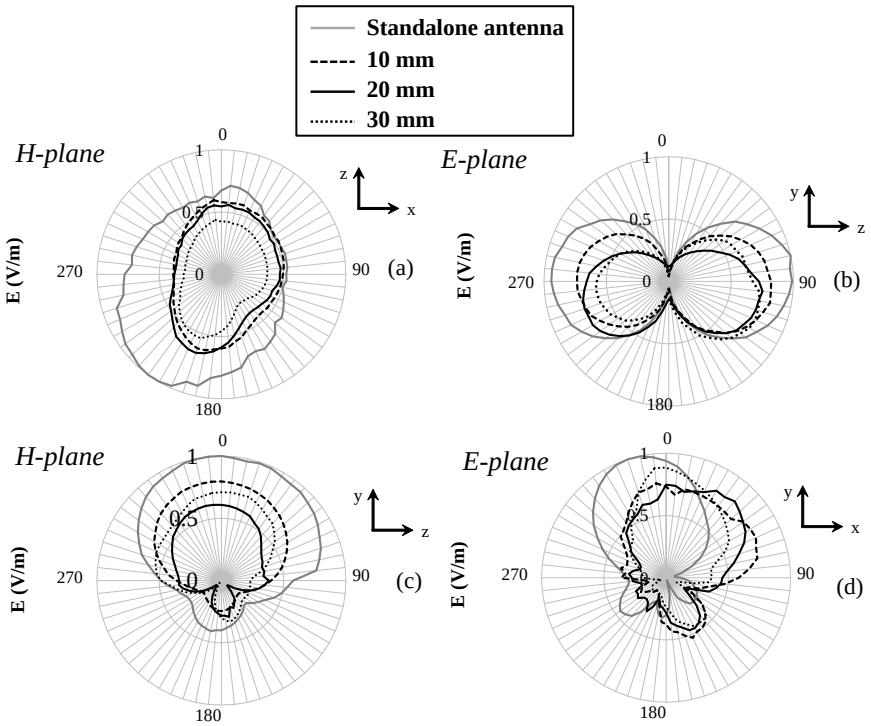


**Figure 4.13:** Antenna radiation patterns in H- and E- plane at 900 MHz ((a) and (b)) and 1800 MHz ((c) and (d)) (linear scale) for the standalone antenna and with a faced identical one, at different distances.

## 4.6 Conclusion

In this project I have proposed a seamless solution to exploit the available PDAs antennas for near-field wireless recharging, with no need for dedicated energy transfer antennas or charging stations. By choosing a suitable frequency (433 MHz), energy transfer between closely-located portable devices is possible by exploiting the coupling of their reactive field.

In particular, the proposed solution only needs to equip the portable antennas with a diplexer network, able to decouple the radiation and the power recharging paths. As a proof-of-concept, a full system prototype has been fabricated and the effective coexistence of the two concurrent activities experimentally demonstrated. Obviously, this architecture enables WPT with lower efficiency levels than state-of-the-art (with dedicated resonant reactive links), but sufficient to make the proposed idea a valid and extremely simple alternative.

The proposed theoretical and numerical approach can be further extended to the design of a new generation of mobile antenna system whose layout optimization addresses at the same time high frequency for far- and low-frequency near field performance.

# Chapter 5

# Wake-Up Radio

Wake-up radio (WuR) is an emerging technology for WSN consisting of an elementary, ultra-low power radio front-end, always ON, to be coupled with the main radio kept in sleeping mode and activated only when data exchange is required. This secondary radio has the role of listening to the channel and understand when its associated node is requested to be activated. This solution has the ambitious goal of reducing the communication power consumption in smart sensor networks and IoT. Indeed, wake-up radios, combined with existing radio transceiver and power management techniques, allow to reduce the overall communication power while maintaining the same communication performance. This reduction in power consumption is foreseen to enable a new generation of applications which could achieve a longer lifetime and energy autonomy.

In this context I have been dedicated to two main aspects. The first one consists of the design and implementation of a dual-band ultra-low power wake-up radio for WSN application. The dual-band radio is exploited to increase the flexibility of the WuR, allowing interoperability with the two most common frequencies used in WSN and IoT (868 and

2400 MHz). Such flexibility allows the radio to add frequency diversity which is a common technique for combating fading and co-channel interference and avoiding error bursts. In fact, since individual channels are subject to different levels of fading and interference, multiple versions of the same signal can be combined in the receiver to retrieve the message. The second contribution is focused on theoretical and experimental analysis of Power Optimized Waveform (POW) in order to define the optimum excitation able to improve the WuR sensitivity down to $-60$ dBm, thus to increase the node distance for communication purposes.
This work has been carried out in collaboration with the Department of Information Technology and Electrical Engineering ETH Zurich, Zurich, Switzerland. In particular, the collaboration was with group of Professor Luca Benini, that has the leadership in ultra-low power electronics for embedded systems.

During this activity, I have first developed a dual-band rectenna to be used as the source of the WuR radio and integrated with it. This system was presented at the 11th International Conference on Wireless and Mobile Computing, Networking and Communications (WiMob), 2015 in Abu Dhabi, UAE [67]. Then, an analysis of optimized excitations has been considered for the realized WuR system and the main results was presented to the International Microwave Symposium (IMS), 2016 in San Francisco, California [68]. After these, I was dedicated to the Proof-of-concept realization and validation of this idea. The main results have been demonstrated in a paper accepted from the Transactions on Microwave Theory and Techniques journal [69].

The remainder of the chapter is organized as follows. Section 5.1 provides an overview of wake-up radio system giving a broad summary of state-of-the-art. Section 5.2 discuss the design of the dual-band WuR,

both low-frequency analog and RF section. This section goes into the details of the various issues encountered and solved the antenna and the rectifier in a multi-band application. Sections 5.4,5.5 and 5.6 discuss the theoretical analysis and experimental results of POW signals applied to the realized WuR system: starting from an overview of the POW signals, the section proceeds with an analytical analysis. Then, an experimentally validation with a laboratory set-up as well as commercial off-the-shelf components will be illustrated. Section. 5.6drives the work conclusions.

## 5.1 Introduction to Wake-Up Radios

Recent advances in digital microelectronics are permitting the development of a large variety of cyber-physical systems. WSN and IoT [70] are one of most promising technologies exploiting these advances to provide a flexible distribution of low-cost and low-energy devices equipped with sensors which can communicate wirelessly. In particular, a sensor node has the ability to collect and process various information such as, temperature, quality of air with gas sensors, humidity, light intensity, pressure and many others, according to the sensor hosted on the device. Their computational capabilities can be used to process the sensor data directly on the node and only important information or actions are sent wirelessly to a remote host.

However, limited energy availability remains the crucial issue for sensor devices as usually they are supplied by non-infinite energy buffers (supercapacitors or batteries). This limitation reduces the lifetime not only of the single device but of the entire network, while emerging WSN applications demand ever longer system lifetimes [71]. Since the radio is, in general, the node's most power-hungry component, any reduction

in the communication power consumption can significantly improve the node's lifetime [72]. Thus, longer lifetimes can be achieved with aggressive duty cycling, turning the radio off ("power save mode") and on ("idle listening or transmitting mode") periodically to save energy. To reduce the power consumed in idle listening, three main schemes are possible, namely pure asynchronous, synchronous and pseudo synchronous. Asynchronous communication is, by far, considered to be the most energy efficient mechanism as can eliminate both the idle-listening and the transmission collisions reducing then the overall power consumption with an ultra-low latency [72]. Asynchronous communication can be achieved by using a wake-up radio receiver (WuRx) [73, 74, 75]. WuRx are able to detect short commands or wakeup signals on the communication channel, with a power consumption of only few microwatts or even nanowatts.

Fig. 5.1 shows the traditional WSN node operating with its main radio and the architecture with the adoption of the WuR receiver. The WuR radio is coupled to the main radio to provide a positive balance of power saved and used. To be effective, reducing the overall power consumption of the network and be compatible with a wireless sensor node, the WuRx has to be carefully designed providing a number of significant features [73]. The most important feature is the power consumption $P_{DISS}$. In fact, the WuR radio in this case represents extra hardware in the node, and for this must have much lower power dissipation than the main radio. Other significant features are the sensitivity, the latency and the robustness.

Finally, another critical feature which can reduce or increase the efficiency in a real deployment is the ability to listen the channel for messages at the operating frequency of the main radio or the radio which

is generating the wake-up message. This put into evidence a critical feature of WuRs, which is the capability to listen to the channel at various radio operating frequencies (as the case of our contribution). The most common frequencies in WSN and IoT are 868 MHz and 2.4 GHz frequency.

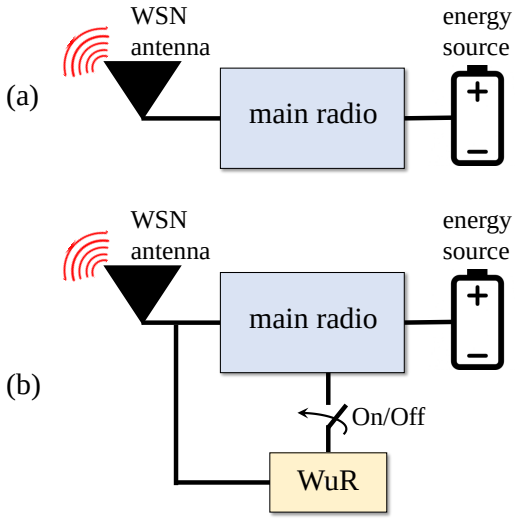


**Figure 5.1:** Comparison of the architecture of a traditional WSN system (a) and the WuR-based one (b).

Basically, wake-up receiver devices can be classified into two main groups: active WuR and passive WuR circuits. The active wake up receivers are the most common approach where the circuits are realized using a Schottky or MOSFET envelope detectors, for the radio front end and a simple logic (i.e. a comparator) to generate the wake-up interrupts or reconstruct the data. Many works present solutions with Schottky diodes as passive rectifier in combination with an ultra-low power comparator to achieve low power consumption [76, 77, 78, 79, 80]. For instance, the authors in [80] propose a very low-power solution with only 89 nW by adopting a custom CMOS rectifier to achieve a sensitivity of $-41$ dBm. Note that, in all these papers the reduction in energy consumption is achieved by eliminating the radio idle-listening activities,

exploiting a reduced duty-cycle approach.

On the other hand, in the passive WURs, the system is able to achieve a zero-power consumption in listening mode. In fact, the passive receiver circuit is used to extract the energy by exploiting the incoming messages received by the antenna. Although the passive capability is very attractive and significant for several applications, these receivers usually have a very limited operative range of a few meters or even centimeters. In fact, these circuits have a sensitivity of around $-30$ dBm or less, they are not suitable for the most typical WSN application. Examples of passive wake up radios with interrupt generators are presented in the literature [81, 82].
Within this scenario, our contribution is focused on improving the capability of WuR systems by introducing two concepts:

1. dual-band wake-up radio,

2. power optimized waveforms.

The first solution consists of a dual-band wake-up radio, able to receive data and wake-up signals in two WSN bands. This approach is similar to the one proposed in literature, however we present an ad-hoc dual antenna with a dual impedance matching to further increase the flexibility of the WuRx. Moreover, a standalone solution is proposed here to process the data received directly on board with an ultra-low power microcontroller to further increase the flexibility of the solution.
In addition, we introduce an analytical analysis of POW signals applied to the Wake-up Radios. At the time of this work, the idea to apply POW signals to WuR system was not proposed in literature yet.

## 5.2 Dual-Band Wake-Up Radio

The architecture of a dual-band wake-up radio receiver is detailed in Fig. 5.2. It is divided into two main sections:

**i)** the RF front-end consisting of a dual-band antenna and matching network, a passive envelope detector;

**ii)** the back-end composed of an interrupt/data generator and an ultra-low-power microcontroller for addressing and node interfacing.

The data are represented as absence (0) or presence (1) of a carrier frequency, the back-end is frequency-independent, operating with any type of RF front-end without any changing in the design.
On the other hand, the front-end needs to be frequency-dependent to guarantee the impedance matching of the back-end with the antenna. The antenna and its matching network have been designed to operate at the ISM bands 868 MHz and 2.45 GHz with the best trade-off between them.
The signals received at one of the two ISM bands in matching conditions, are provided to the demodulator input, which can be as simple as a passive envelope detector to guarantee the best trade-off between power consumption and sensitivity.

Once the signal is rectified, the received wake-up message needs to be reconstructed. An ultra-low power comparator with a small voltage offset is needed to detect the 0-bit and 1-bit. A passive filter is used after the comparator to filter false alarms, tuning the filter to detect a preamble with the specific sequence of bit-length. Thus, the preamble detector signals a wake-up interrupt to the on-board microcontroller which is in sleep mode.

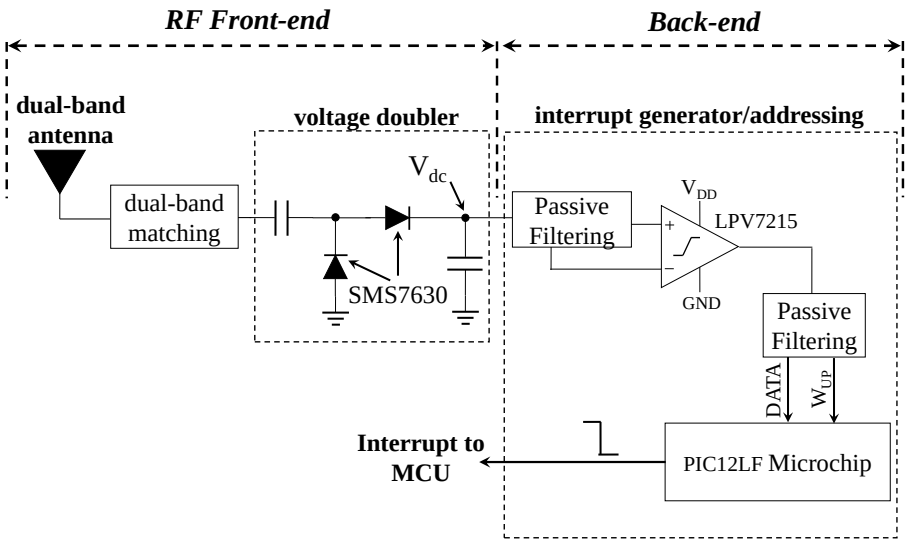


**Figure 5.2:** System Architecture of dual-band Wake-up receiver with addressing capability.

The first step of the implementation is the dual-band antenna design. Several antenna topologies have been proposed in the last few years to be compatible with the WSN cases [83]. The most common are monopoles external or printed on the same PCB of the sensor node. Recently several 3D antenna topologies have been proposed as multiband antenna for their compactness and reduced costs.

The picture of the realized WuR system is shown in Fig. 5.3. Focusing on the RF front-end, a PIFA-like, dual-band, low-profile antenna is adopted to simultaneously operate in the 868 and 2450 MHz bands. It is based on a 635 μm-thick RF-60A-Taconic substrate ($\varepsilon_r = 6.15$, $tan\,(\delta) = 0.0038$ at 10 GHz).

The antenna is a combination of two monopoles whose lengths are optimized to tune the antenna at the required resonant frequencies with the highest radiation efficiency and the monopole-like radiation pattern at the two operating frequencies.

The measured and simulated performances of the antenna, in terms of

input reflection coefficient, are shown in Fig. 5.4: very good agreement has been obtained with the full–wave simulation. An additional resonance is obtained at about 1.5 GHz due to the combined effect of the two branches, which does not affect the present design.

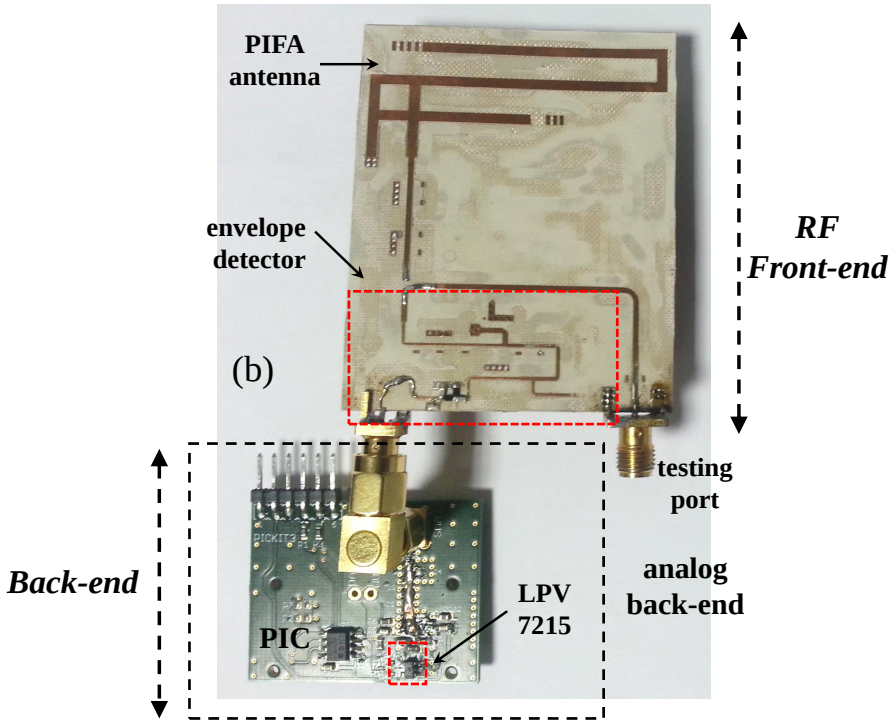


**Figure 5.3:** Picture of the implemented WuR system with illustrated the RF front-end and the analog back-end.

It is noteworthy that this RF section of the WuR is designed in such a way as to present end-to-end continuity between the antenna and the detector, thus allowing to minimize the matching network elements with the twofold advantage of reducing the overall node size and losses. The latter are small in absolute, although significant for the purposes of our work, given the ultra-low power involved.

The adopted detector is a single-stage full-wave Dickson voltage doubler rectifier. The diodes are selected based on their sensitivity, defined as the highest dc-voltage at a given (low) input RF power.

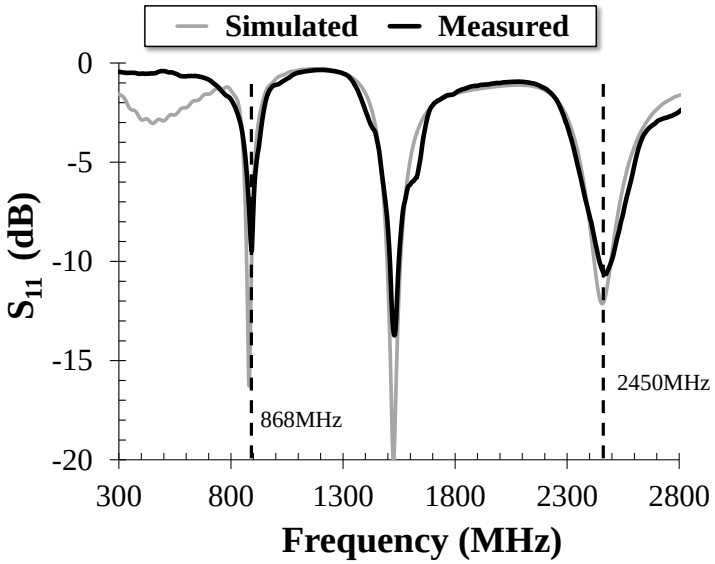


**Figure 5.4:** Simulated and measured antenna reflection coefficient versus frequency.

The SMS7630-079 (Skyworks Inc.) results to be the best compromise among sensitivity, losses and operating frequencies to be covered. This was obtained by simulating the performance of the SMS7630 diode and another commercial model (HSMS2852 from Avago Technology) optimized for operating at low frequency (up to 1.5 GHz). The results are plotted in Fig. 5.5.

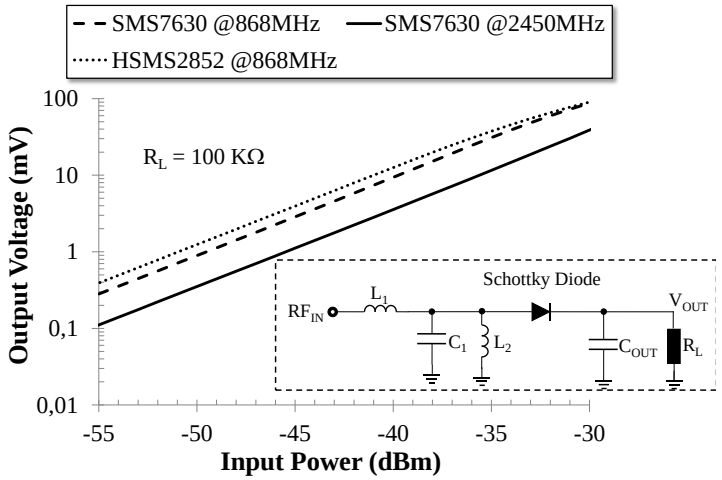


**Figure 5.5:** Sensitivity analysis of two commercial diode with corresponding circuit topology used for the simulations.

The circuit adopted for this comparison is plotted in the same figure. It can be noticed that, the diode sensitivity of the SMS7630 decreases with increasing frequency. This loss is, in any case, small (about 8%) with respect to the sensitivity of the HSMS2852 diode. As a result, to extend the wake-up receiver operation at two bands requires an acceptable sensitivity loss in the 868 MHz band.

Another challenging task of the detector design is the multi-band matching network which requires to account for the dispersive and non-linear behavior of the overall system affecting the power-dependent detector input impedance [80].
The chosen topology is illustrated in Fig. 5.3 and consists of two impedance steps and two stubs, the first shorted and the second open. Impedance steps are employed to guarantee a wideband matching between the detector and the antenna while the stubs tune the resonance of the system at 868 and 2450 MHz. For any operating frequency and incoming RF power, focusing on typical wake-up scenarios ($-55 \div -40$ dBm), the non-linear regime is optimized accounting for the dispersive behavior of the linear sub-network (antenna and matching networks), available from EM simulation, and the non-linear diode model including its package.

The HB-based optimization is aimed at enhancing the dc output voltage $V_{dc}$ in order to obtain the highest rectifier sensitivity defined as:

$$\gamma\left(P_{RF-IN}, f_0\right) = \frac{V_{dc}\left(P_{RF-IN}, f_0\right)}{P_{RF-IN}} \left[\frac{V}{W}\right] \tag{5.1}$$

where $f_0$ is the design frequency and $P_{RF-IN}$ is the input power of the RF front-end. It is noteworthy that by using a unique matching network and rectifier circuitry for both the operating frequency allows to enhance the sensitivity of the whole receiver.

The final performances of the system are summarized in Figs. 5.6 and 5.7. Fig. 5.6 shows the measured and simulated behavior of the output voltage with respect to input power ($P_{IN}$), for the two operating frequencies, in CW excitation conditions: at −56 dBm the system provides approximately 300 μV at 868 MHz, and to obtain the same dc-voltage at 2.45 GHz the required input power is −54 dBm.

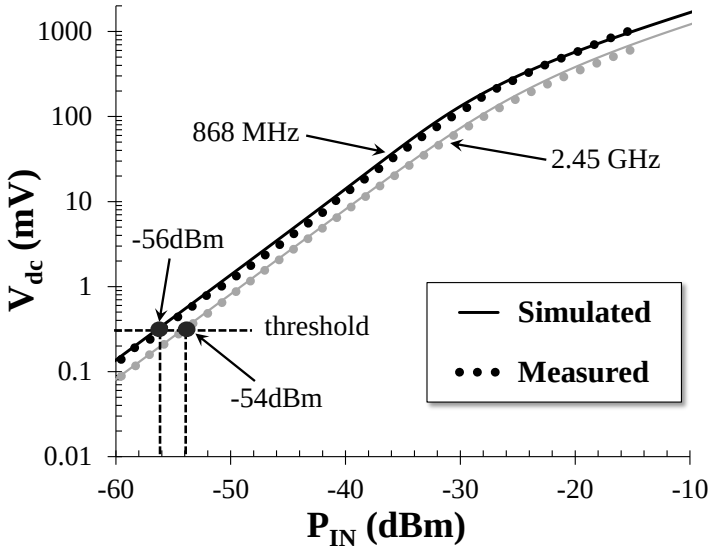


**Figure 5.6:** Simulated and measured WuR detector output voltage versus input power.

Note that 300 μV is the minimum voltage where the back-end comparator is able to detect the incoming signal. As a consequence, −56 dBm and −54 dBm can be defined as the system sensitivity for 868 and 2450 MHz bands, respectively.

Thus, only a 2 dB sensitivity reduction at the higher frequency is obtained. This can be explained by considering two effects: i) the lower diode sensitivity at higher frequencies; ii) the losses increase of the matching network at 2.45 GHz.

Nonetheless a good sensitivity is obtained, comparable with respect to state-of-the-art [81]. Fig. 5.7 shows the effect of frequency varia-

tions on the dc-voltage, for the two operating bands and for different power levels. A good agreement between simulations and measurements is again obtained. A slight frequency-shift is observed between the measured and simulated results, the highest measured performances in the two bands being at 860 MHz and 2.41 GHz, respectively.

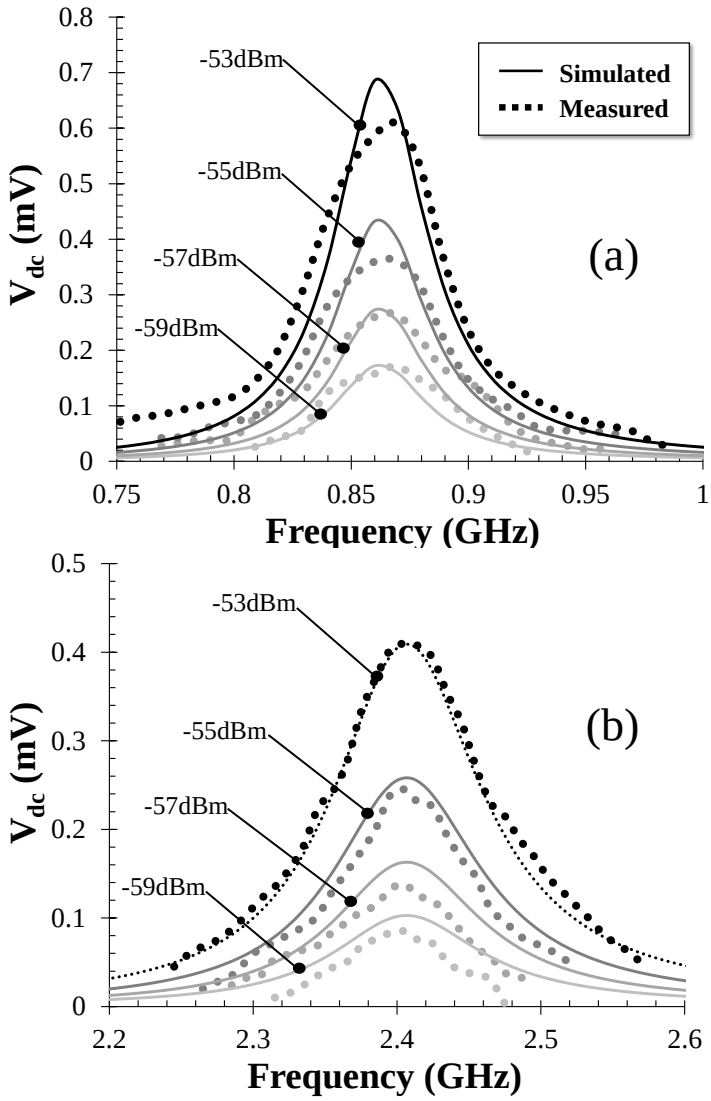


**Figure 5.7:** Predicted and measured dispersive behavior of the detector output voltage for the two operating bands: (a) 868 MHz and (b) 2.45 GHz.

So far, the RF front-end has been described illustrating the feasibility and main feature of the dual-band wake-up radio. However, the

good sensitivity shown is related to the RF section only. It is obvious that, the sensitivity depends on the analog back-end as well due to the fact that it is responsible for the data demodulation.
The back-end building blocks are still shown in Fig. 5.2 and the corresponding prototype shown Fig. 5.3, and they are:

**i)** the ultra-low power comparator, which generates the demodulated information by detecting the (ultra-low) variations at its differential input;

**ii)** the passive filter;

**iii)** the microcontroller used for demodulation and for the main radio activation.

To accomplish the comparator conversion and to overcome the noise effects, an adaptive low power threshold mechanism for the reference pin of the comparator is adopted, which is based on a simple passive band pass (RC) filter on the '-' pin of the comparator, while the output is directly connected to the '+' pin. Due to the filter, the comparator can detect the bit '1' by exploiting the differences of the incoming received powers, since the reference signals are based on the received signal level itself. Thus, an important parameter of the comparator is the voltage offset (minimal difference between V+ and V-) that determines the minimum sensitivity of the received message.
The adaptive mechanism is designed based on the output signal directly connected to the '+'. The back-end building blocks are: the LPV7215 comparator from Texas Instruments, having an extremely low voltage offset of 300 μV and consuming only 600 nA; PIC12LF microcontroller from Microchip with only 40 nW at 2 V, in sleep mode, and a fast wake-up time of only 250 μs at 1 MHz. The PIC enables the WuR to match

the address by reading the wake-up message.

Table 5.1 summarized the measured sensitivity obtained with the system in Fig. 5.2. The measurements were made considering more frequencies within the two bands. The maximum of sensitivity is obtained at the center frequency where the receiver is perfectly tuned. Note that, the power consumption is almost constant versus frequency.

**Table 5.1:** Measured sensitivity and power consumption for the WuR in Fig. 5.2.

| ***Frequency*** **[MHz]** | ***Sensitivity*** **[dBm]** | ***Consumption*** **[nW]** |
|---|---|---|
| 860 | −52.4 | 1242 |
| 868 | −55.7 | 1255 |
| 875 | −52.1 | 1221 |
| 2400 | −50.1 | 1210 |
| 2450 | −53.2 | 1225 |
| 500 | −49.7 | 1223 |

The base-band WuR sub-system is realized on a low-cost FR4 substrate and its size is $30 \times 40$ mm$^2$. The front-end part dimension of the WuR is $62.5 \times 51$ mm$^2$ . Thus, the overall dimension of the system is $102.5 \times 63$ mm$^2$ which is compatible with WSN module's dimensions, but can be significantly reduced by merging the RF and base-band sections, including the antenna, in a unique substrate.

In this section, it has been demonstrated the feasibility of a dual-band wake-up radio. Other works proposed in literature have a fixed frequency band in the range of MHz against the two bands typically used by WSNs in our solution. On the multi-band approaches only, few previous works are presented in literature. In [84] a dual band (2.4 GHz and 915 MHz) envelope detector-based wake-up receiver front-end is presented.

The proposed receiver consumes 51 μW and it is built with 80 mm CMOS achieving −69 dBm and +80 dBm sensitivity at 2.4 GHz and

915 MHz respectively. In [85] a 116 nW tri-band wake up radio with crystal reference, interference compensation, and base-band processing (selectable 31-bit code) is presented. The low power consumption of this solution is very impressive, but this affects the sensitivity which is around only $-40$ dBm for the three bands.
Compared with these two solutions, our solution can be placed in the middle on the trade-off between power consumption and sensitivity. In fact, the proposed solution compared to [84] consumes less power (about $1,2$ μW in our solution versus 51 μW) achieving a lower sensitivity ($-53$ dBm in our solution versus $-80$ dBm). Compared with [85] our solution consumes more ($1,2$ μW versus 116 nW) achieving better sensitivity ($-53$ dBm versus around $+40$ dBm). Another important feature is the addressing capability which is not present in the solution [84] and it is not programmable in the solution [85].

In the solution described in this chapter, the addressing and data parsing can be performed directly on board with an ultra low-power programmable microcontroller, which can reduce the overall power consumption due to false positive wake up when used during in-field applications. In addition, the proposed solution also has ad-hoc dual-band antenna and dual matching networks which are not considered by the authors in [84] and [85].

## 5.3 Power Optimized Waveform (POW)

Power Optimized Waveforms (POWs) have been successfully presented in the last few years to improve system performance in different applications: in [86, 87] they allow to enlarge RFIDs reading range, whereas in [34], [88] higher rectenna efficiencies are achieved in energy harvesting and wireless power transfer scenarios.

In [88] closed-form equations, theoretically justifying the convenience in utilizing high peak-to-average power ratio (PAPR) waveform, are provided; but a quite discrete matching with experimental data is observed. However, it is proved that such kind of waveforms improve the system performance in precise RF power ranges, that are much higher than those of interest for the WuR [86]. POWs have already been considered to enlarge RFIDs reading range [86] or to maximize the rectenna efficiency in energy harvesting system [34]. Such waveforms are effective only for selected RF low-power ranges [86], still much higher than those desirable for a WuR, and in high loading conditions, far from the optimum one.

In this chapter, we show that using intermittent signals [89] with reduced duty-cycles allows to exploit high power peaks, while the average RF power can be as low as $-64.5$ dBm. Basically, a POW is a multi-carrier waveform whose high peak-to-average power ratio (PAPR) is able to overcome the diode losses at low-input powers. A high PAPR generates a voltage spike when the signals which forms the waveform are combined in-phase.

Fig. 5.8 shows an example of CW and POW signals. Both these signals have the same average power $P_{AVG}$, but it is easy to recognize that the POW signal provides a higher peak able to overcome the turn-on threshold of the diode. Doing so, a higher dc voltage can be obtained with same $P_{AVG}$.

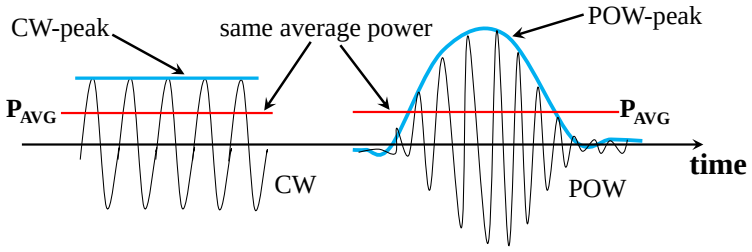


**Figure 5.8:** Example of continuous wave and POW signals.

The idea of boosting the operating region of RF/microwave detectors and rectifiers, with optimized non-continuous wave excitations, has been the subject of a large number of studies and experiments [86, 87, 90]. Indeed, non-CW excitations, such as those composed of multi-sine waveforms, closely spaced in frequency, with high peak-to-average power ratio enable diodes turn-on in sub-intervals of their period, where the CW wave, with the same average power, cannot.

It is noteworthy that this situation occurs in a precise range of average input power, depending on the specific diode adopted [86, 91]. The lowest power limit is the one enabling the diode turn-on, and the highest one is fixed by the decreasing of the maximum efficiency, due to the diode being driven in the breakdown region [88]. This has been proved for RF input power ranging from $-30$ dBm up to $-10$ dBm approximately, if using rectifier Schottky diodes such as SMS7630, HSMS-285B.
For energy harvesting (EH) purposes, the main goal of the detector design is to achieve the highest RF-to-dc efficiency, as well as the minimum dc power and voltage sufficient to bias the rectifier load (consisting of either a sensor or a dc-dc converter) [17]. For this purpose, the load is optimized, together with the rest of the entire system, by nonlinear circuit techniques, for the expected power range of interest [18].
Conversely, for WuR applications the detector load is fixed, and it is usually very high (of the order of few MOhm), being the comparator input impedance. Moreover, the WuR source is a simple modulated signal, usually adopting OOK modulation, which represents data with the presence or absence of the carrier. In this case the main goal is to achieve the maximum detectable dc-voltage, to correctly trigger the ultra-low-power comparator [92], rather than the highest conversion efficiency.

To select the optimum excitation for the WuR, the RF front-end

described in the previous section, is first analyzed in CW conditions, for a wide range of (low) input power, spanning from 0 dBm down to −70 dBm by means of HB analysis. The simulated dc-voltage output, $V_{dc}$, with respect to the input power $P_{IN}$ is plotted in Fig. 5.9 in logarithmic scale. The curve is well described by a piecewise linear function [93], satisfying the closed form relationship:

$$V_{dc}\left(P_{IN}\right) = V_{d0}\left(P_{IN}\right) \cdot \left[\sqrt[2]{P_{IN}}\right]^{\alpha(P_{IN})} \tag{5.2}$$

which in logarithmic form becomes:

$$V_{dc}\left(P_{IN}\right)|_{dBV} = 10 \cdot \log\left[V_{d0}\left(P_{IN}\right)\right] + \frac{\alpha\left(P_{IN}\right)}{2} \cdot 10 \cdot \log_{10}\left[P_{IN}\right] \tag{5.3}$$

where $V_{d0}$ (in dBV) is the intercept of the line at $P_{IN} = 0$ dBm, while $\alpha\left(P_{IN}\right)/2$ is its exponential coefficient. Three different regions for the linear approximation can be distinguished:

**i)** $\alpha = 2$ at the lower power interval;

**ii)** $\alpha = 1$ in the higher power interval, and

**iii)** a transition zone between the two of them.

For the present topology, the intercept at $P_{IN} = 0$ dBm is 4 and 68 for $\alpha = 2$ and $\alpha = 1$, respectively [93].

A suitable figure of merit, to be maximized for the optimum WuR excitation, is the ratio between the dc-voltage envelopes due to the optimized waveforms (OW) and to the CW excitations:

$$G_V\left(P_{IN}\right) = \frac{V_{dc|OW} \cdot P_{IN}}{V_{dc|CW} \cdot P_{IN}} \tag{5.4}$$

that can be called voltage gain and it is again a nonlinear function of the $P_{IN}$ through (Eq. 5.2).

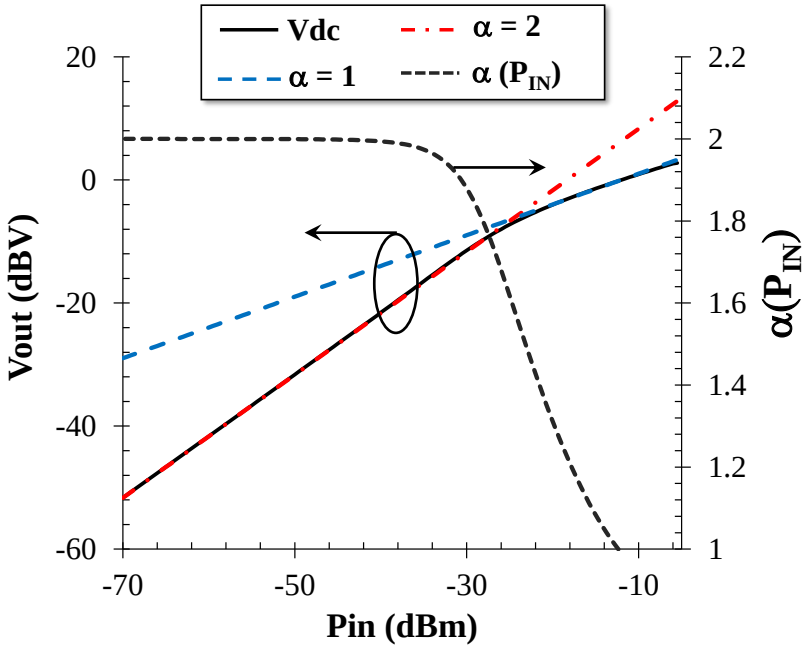


**Figure 5.9:** Simulated behavior of the detector output voltage over the wide power range of interest, and corresponding behavior of the exponential $\alpha\,(P_{IN})$: for power values from $-70$ dBm to $-35$ dBm a quadratic low is confirmed, then it starts decreasing and reaches the 1 value at about $-12$ dBm. The carrier frequency is 868 MHz.

$P_{IN}$ can be rigorously computed as the power received by the antenna by means of the equivalent Thevenin or Norton circuit representation presented in [18].

If the Thevenin equivalent is chosen, the CW voltage generator can be expressed as $V_{CW}\,(t) = V_{A0}\cos\,(\omega_0 t)$, and for the optimized waveforms as $V_{OW}\,(t) = V_A\,(t)\cos\,(\omega_0 t)$, where represents the carrier angular frequency and $V_A\,(t)$ represents the low-rate modulated law.

For this study we assume that the antenna is matched to the rectifier and that its impedance is purely real $(R_A)$. In addition, two families of excitations are considered:

**i) Multi-sine excitation**, generated by combining equally and closely spaced N-subcarriers. It can be observed that, for a fixed tone-spacing, peaks increase with the number of tones [74] and the bandwidth as well, while the signal period is fixed;

**ii) Intermittent excitation**, carrying the OOK WuR data, generated as square pulses modulating the RF carrier, and intermittently switched ON and OFF with different ON intervals ($T_{ON}$), within the bit period ($T_B$), to dynamically modify the duty cycle.

In order to compare the detector performance $G_V$, in terms of its highest output dc-voltage at the lowest average power, all the waveforms are designed to ensure the same average power over the bit period $T_B$, and $G_V$ is evaluated with respect to the same time interval, the ON bit period ($T_{ON}$), which is usually much longer than the multi-sine one.
Fig. 5.10(a) shows the time behavior of a set of multi-sine excitation, equally spaced, consisting of N-subcarriers with frequency shift $\Delta f =$ 500 kHz and 0°-phase-shifting among the carriers, as suggested in [34] for EH purposes; tests are carried out using 2, 4 and 8 tones.

For the present case, the signal period $T_{OW}$ is equal to 2 μs. For the ICW excitations a 1-kbit data rate is used, corresponding to $T_B = 1$ ms. $T_{ON}$ intervals reduced to 50% (500 μs), 25% (250 μs), 12.5% (125 μs) of $T_B$ are generated. Fig. 5.10(b) compares the corresponding modulated waveforms, within the same bit interval $T_B$.

To account for the worst case in terms of bandwidth increase, due to the reduced duty cycle, a periodic sequence of "1" and "0" bits is used. The analytical evaluation of $G_V$ can be obtained by computing the average dc output detector voltage in the same time interval $T_{ON}$ as a function of the CW and OW excitations using (Eq. 5.3). The following expressions are obtained:

$$V_{dc|CW} = \frac{1}{T_{ON}} \cdot \int_0^{T_{ON}} \left[ V_{d0}\left(P_{IN}\right) \cdot \sqrt{\frac{V_A^{\alpha(P_{IN})}}{8 \cdot R_A}} \right] dt \tag{5.5}$$

$$V_{dc|OW} = \frac{1}{T_{ON}} \cdot \int_0^{T_{ON}} \left[ V_{d0}\left(P_{IN}\right) \cdot \sqrt{\frac{V_A^{\alpha(P_{IN})}(t)}{8 \cdot R_A}} \right] dt \tag{5.6}$$

It is obvious that, for power levels belonging to the diode region where $\alpha = 2$ (see Fig. 5.9), it is not possible to increase $G_V$ adopting excitation waveforms having the same average power of the CW counterparts. This is because in this region the detector operates as power mete, measuring the average power and peaks does not affect the output voltage. The the power decreases, as in second region of Fig. 5.9, the peaks can affect the output voltage.

However, higher values of $G_V$ are obtained by enhancing the peaks in the ON interval ($T_{ON}$) of $T_B$, while ensuring the same average power over $T_B$. This phenomenon is explained by observing that, by intermitted signal excitations, the voltage envelope is forced to its highest value for a longer time interval than under multi-sine excitations.

This is confirmed by the simulated $G_V$ of the detector excited by the two families of excitations discussed above and loaded by the equivalent comparator impedance (1 MOhm) shown in Fig. 5.10 where $G_V$ is plotted in logarithmic scale. The envelope transient HB simulation technique [94] is used to derive these results. These plots show that, for the entire power interval to be exploited for enhancing the WuR sensitivity, higher values of $G_V$ can only be obtained by enhancing the peaks in the ON interval ($T_{ON}$) of $T_B$, while ensuring the same average power over $T_B$. Fig. 5.11 shows that $G_V$ further increases to 6 and 9 dB if the duty-cycle is reduced to 25% and 12.5%, respectively. These results

are experimentally confirmed in the next two sections by a lab-level experimental set-up and a more realistic set-up based on off-the-shelf components.

Note that, in order to fully exploit the POW approach, the control of the ICW spectrum is needed to comply with the available regulations. For example, in the RFID UHF band, a 500 kHz channel bandwidth is allowed by the FCC standard [95], and it is reduced to only 200 kHz by (ETSI) [96].

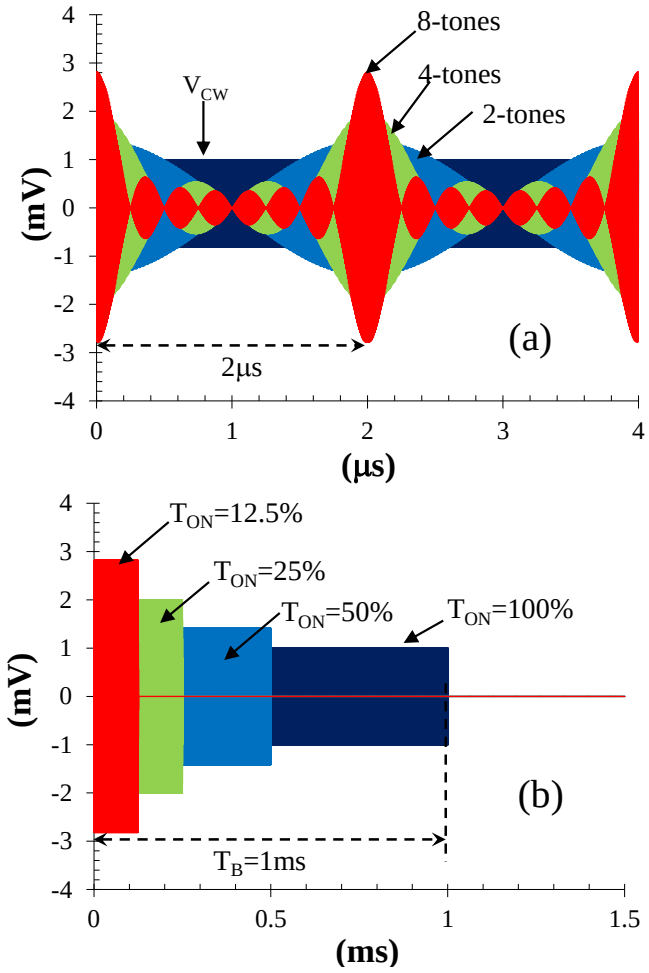


**Figure 5.10:** (a) Multi-sine waveforms with different number of tones, 500 kHz spaced, with a period of 2 μs, and (b) ICW excitations with different 'ON' intervals. To compute these excitations an average power per bit of −50 dBm and a WuR bit rate is 1 kHz are used.

This aspect is considered in Fig. 5.12, where the simulated spectra for the considered reduced duty-cycles are shown. In this figure, it can be observed that in the worst case ($T_{ON} = 12.5\%$) the occupied bandwidth is 140 kHz only, confirming that ICW are fully comply with the standards when a low bit rate is involved.

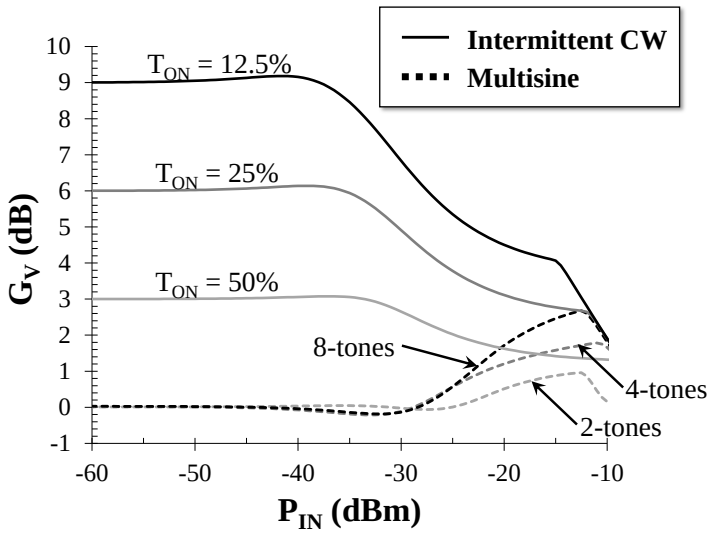


**Figure 5.11:** Simulated results of the voltage gain $G_V$ using muti-sine and ICW detector excitations.

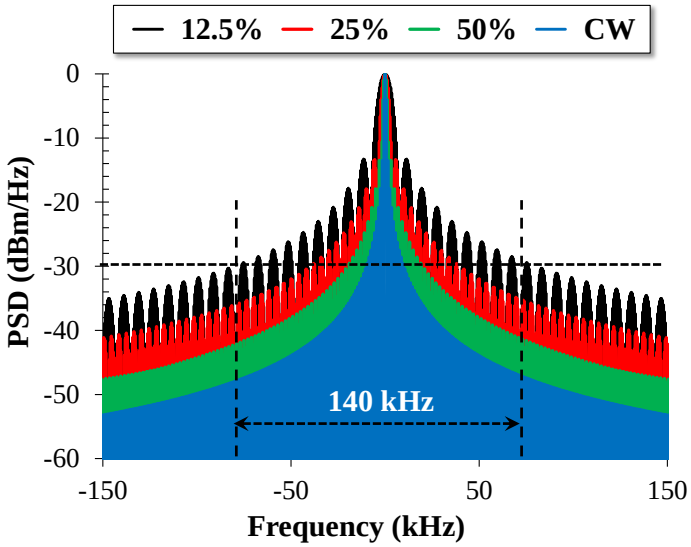


**Figure 5.12:** Simulated spectra of ICW signal with a periodic sequence of "1" and "0" bits with a bit period ($T_B$) of 1 ms and for different $T_{ON}$.

## 5.4 Power Optimized Waveforms: Experimental Validation

This section is dedicated to the dual-band experimental validation of the WuR by using the ICW excitations, which have been demonstrated to be the proper signals able to enhance the WuR sensitivity at the lowest power intervals. As a reference, an average RF power as low as $-56$ dBm is targeted.

Due to the low-level voltage and power of the signals involved in the POW measurements, special attention has been given to the experimental setup. The adopted setup is schematically depicted in Fig. 5.13.

First of all, to generate the designed optimized waveforms, the wide-band arbitrary waveform generator Tektronix AWG7122C is used. These optimized signals have been first implemented in Matlab and then loaded in the generator. The generator output is then connected to a 0.25 dB step digital attenuator (Minicircuit RUDAT-6000) in order to scale the average RF power of the waveforms and keep the same value over a bit interval while reducing the duty-cycle.

In order to double check such power values, the generator output signal is split in two ways: the first one is used to feed the RF section of the WuR and the second one is connected to a spectrum analyzer (Agilent N1996A), to measure the current average power in any attenuator state. This average power has been measured within a limited bandwidth in order to minimize the noise floor. In fact, to correctly measure the power levels as low as $-70$ dBm, the spectrum analyzer must be configured in a way that its noise floor does not affect the actual signal. For this scope, the allowed bandwidth has been reduced to 500 kHz and the pre-amplifier function of the spectrum analyzer is turned on. With this set-up, the noise floor drops to $-80$ dBm/Hz. Furthermore,

to precisely characterize the sensitivity, the detector is directly fed by the waveform generator through the testing port (see Fig. 5.2) and the antenna is disconnected.

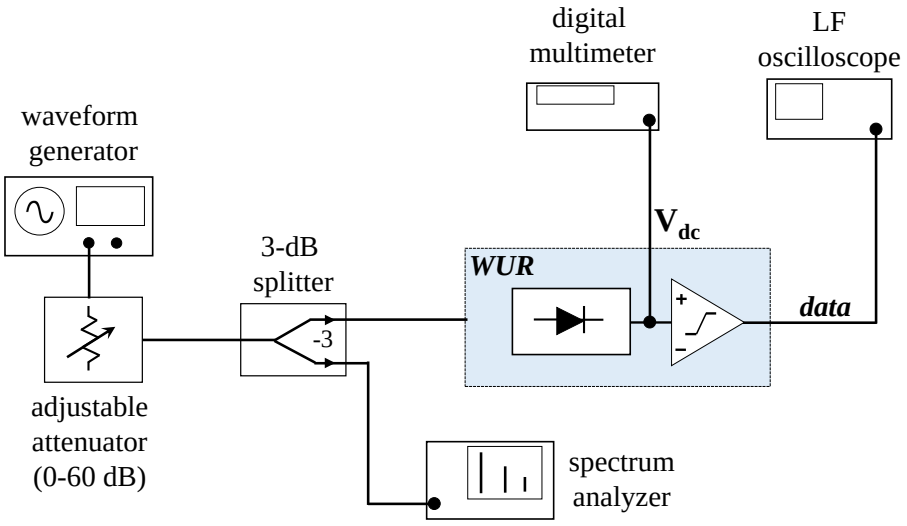


**Figure 5.13:** Block representation of the experimental set-up.

Another critical aspect is the voltage multimeter accuracy in order to precisely measure the detector output dc-voltage ($V_{dc}$), since values as low as 100 μV need to be distinguished. For this purpose, a high-sensitivity digital multimeter (Keithley 2015-THD) with an accuracy of 0.1 μV and typical RMS noise floor of 22 μV is used. However, during the tests a higher noise level of 50 μV has been observed.

Finally, a low-frequency oscilloscope (Agilent DSO X-3024) is used to monitor the comparator activation, as well as the correct reading of the digital data. In this case, the output voltage can be either the comparator bias ($V_{DD}$) or 0 V.

Each measurement procedure is carried out in two steps: in the first one, the averaged power is set ($P_{AVG}$) and verified by the spectrum analyzer; in the second one, the comparator output voltage is measured during the ON-state of the waveforms, when the signal peaks occur. For any

waveform under test, the average RF power is spanned from −68 to −15 dBm, with a 0.5 dB step.
The maximum power is limited by the maximum voltage swing of the generator. In fact, the waveforms are generated using a range from −1 V to 1 V. With this bound, when higher peaks signals (as the PAPRs) are used, the maximum available power decreases.

The WUR is tested under intermittent excitations that are generated as square pulses, modulating the RF carrier, and intermittently switched on and off with different timing, within the bit interval, to dynamically modify the duty cycle.
For the present experiment, square pulses with 50%, 25%, 12.5% duty-cycles are considered.
For the bit interval, we adopt the same symbol rate of 1 kbit/s ($T_B = 1$ ms) for any ICWs, which is typical of wake-up radio operation. With such a low bit-rate, for any optimized wake-up signal, no pulse shaping is performed to control the signal bandwidth. For the sake of simplicity, the performances are measured using a sequence of "1" and "0" bits, continuously repeated.

Fig. 5.14 and 5.15 report the results for the intermittent signals, versus the average RF power. Fig. 5.14 shows the dc output voltage resulting from different duty cycle at 868 MHz (Fig. 5.14(a)) and 2.45 GHz (Fig. 5.14(b)). These plots demonstrate that by decreasing the duty-cycle, the detector output voltage increases, and this is especially true at the lowest power levels. In particular, for the 868 MHz case, the system sensitivity is approximately −56 dBm in CW conditions ($T_{ON} = 100\%$) while it improves down to −65 dBm with a $T_{ON} = 12.5\%$).
Similar results can be observed at the second WuR operating frequency of 2.45 GHz: in CW conditions ($T_{ON} = 100\%$) the sensitivity is -54

dBm, while it improves down to−63 dBm with a $T_{ON} = 12.5\%$). In this way 9 dB of maximum gain with respect to the CW excitations is obtained.

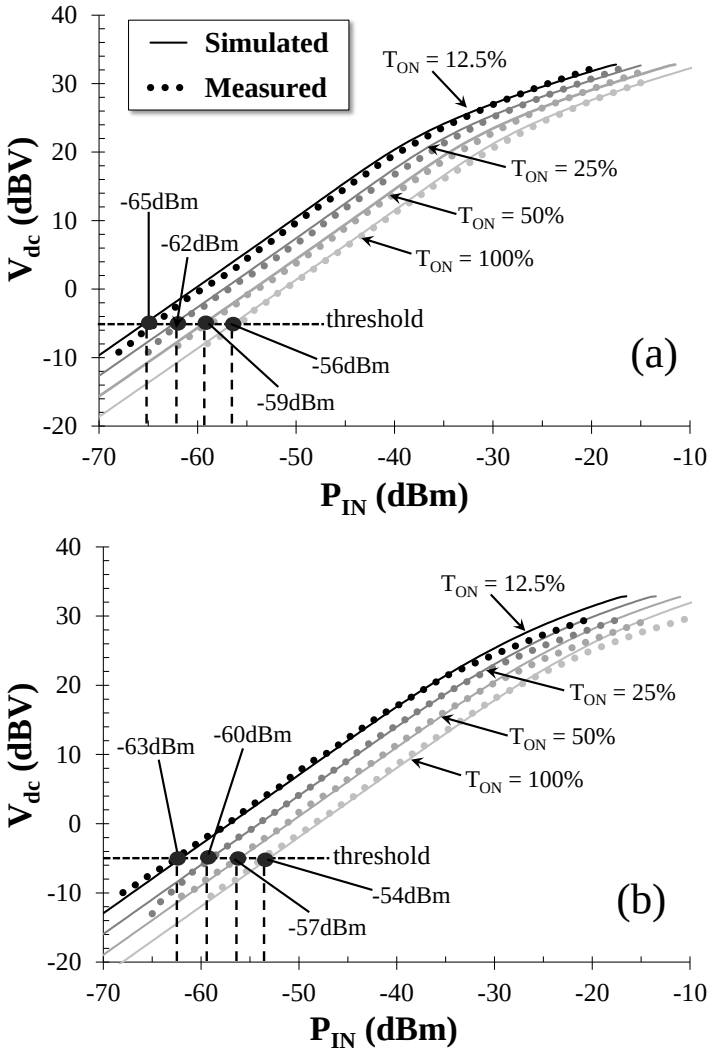


**Figure 5.14:** Dual-band measured and predicted performance of the RF subsystem, in terms of detector output voltage: (a) for a carrier frequency of 868 MHz, (b) for a carrier frequency of 2.45 GHz.

The measured results of the detector figure of merit $G_V$, previously defined are plotted in Figs. 5.15(a) and 5.15(b) for carriers at 868 MHz and 2.45 GHz, respectively, and are compared with the predicted ones: the chosen excitation waveforms demonstrate that a constant increase of

$G_V$ can be obtained over a large range of ultra-low power values, starting from −65 dBm, or −63 dBm, depending on the carrier frequency.

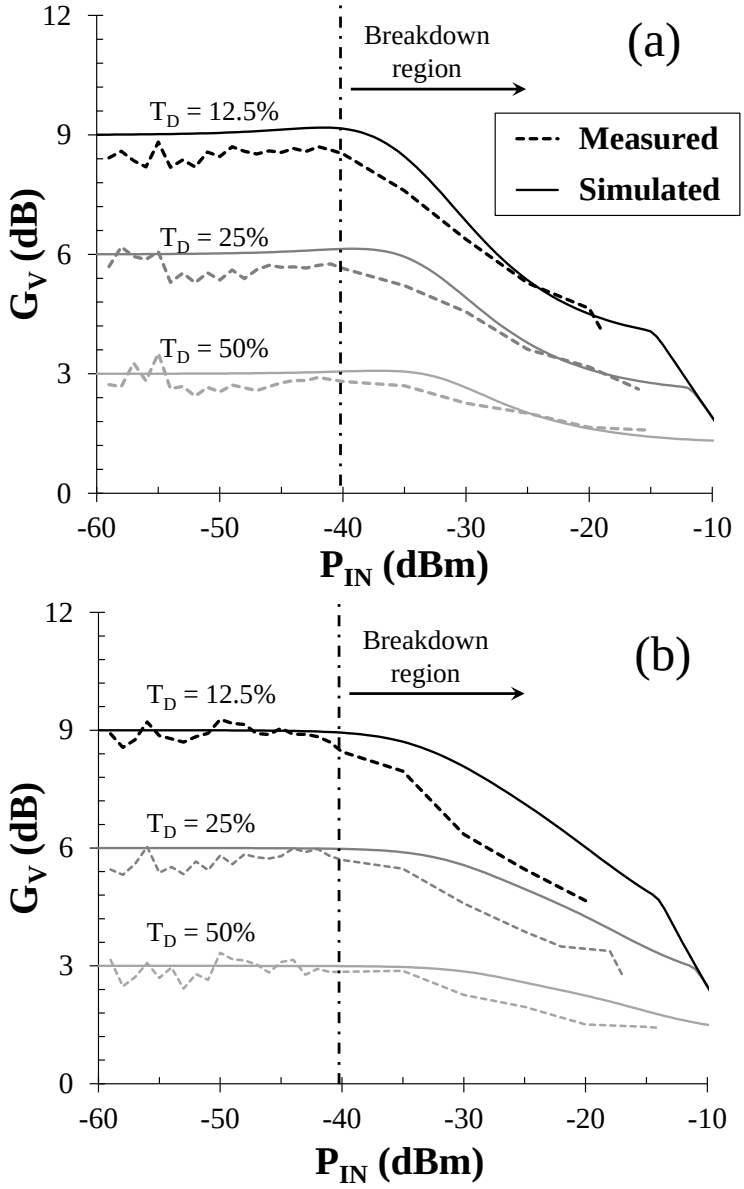


**Figure 5.15:** Dual-band measured and predicted results in terms of obtainable detector voltage gain for the selected WuR excitation waveforms: (a) for a carrier frequency of 868 MHz, (b) for a carrier frequency of 2.45 GHz.

For any chosen 'ON' interval ($T_{ON}$), the gain is almost constant and start decreasing at those levels where the diode saturation is explored. From inspection of Figs. 5.15(a) and 5.15(b) it can be observed that reducing

$T_{ON}$ results in a decreasing of the gain for lower power levels, due to the increasing of the excitation peaks. In addition, Fig. 5.15 show that a 3 dB gain with $T_{ON} = 50\%$ is obtained, approximately and increases to 6 and 9 dB if $T_{ON}$ is reduced to 25% and 12.5%, respectively.
Very good agreement of the measured behavior is observed with respect to the predicted ones.

## 5.5 WuR Validation by Off-the-Shelf Components

In the previous section, it has been experimentally validated, by using lab-level instrumentation and a rigorous measurement procedure, the effectiveness of using ICW waveform in WuR systems. In this section, we show that the proposed WuR excitation strategy can be fully implemented by using commercial off-the-shelf components to generate the optimized WuR excitations.

The developed test-bed is shown in Fig. 5.16: it consists of a demo board from TI, using the transmitter (EM430-F6137RF900), an attenuator and the described WuR as receiver; the attenuator is used to emulate the free space path-loss. The TI transmitter hosts a microcontroller with integrated radio (TI CC430F6137). Due to the considered transmitter only the 868 MHz band is considered.
The other WuR operating band (2.45 GHz) can be tested as well, with a different proper transmitter, without loss of generality. The chosen set-up allows to dynamically control all the parameters of interest for the purpose of this demonstration, such as data rate, transmitted power, and bit sequence to be sent.

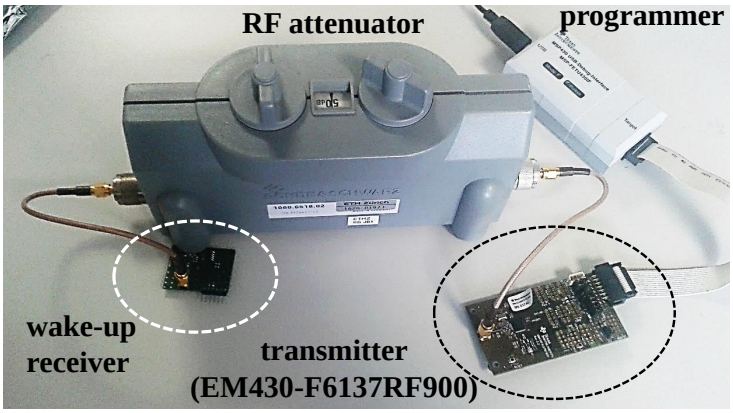


**Figure 5.16:** Picture of the experimental set-up.

Specifically, four different configurations have been set according to the $T_{ON}$ intervals considered for testing the WuR. The bit period used for these analyses was 10 ms (0.1 kHz). Thus, such configurations can be categorized by the ON period and the transmitter output power $P_{OUT}$, which is adjusted according to $T_{ON}$ changes, in order to keep the same average power for any configuration. Specifically, for the measurement conditions where:

**a)** $T_{ON} = 10$ ms, $P_{OUT} = 0$ dBm;

**b)** $T_{ON} = 5$ ms (0.2 kHz), $P_{OUT} = +2.5$ dBm;

**c)** $T_{ON} = 3.33$ ms, $P_{OUT} = +4.5$ dBm;

**d)** $T_{ON} = 1$ ms, $P_{OUT} = +10$ dBm.

These values have been selected considering the available settings of the demo-board. The address message to be detected at the WuR side was: "0xAA", corresponding to the 8-bit sequence "10101010".
For all the configurations under test, the minimum power enabling the correct data reception was registered and the results are summarized in Table 5.2: it is possible to notice that using the proposed optimized excitations, configuration d) allow a successful data transmission at an average power that is 8 dB lower than that needed by configuration a). This fully validates the results obtained by the laboratory setup.

Note that, such sensitivity can be reached only by using the methodology proposed in this chapter. In literature does not exist (to date) solutions able to be comparable with the results that we have shown in this chapter.

**Table 5.2:** Summary of the WuR sensitivity with off-the-shelf components.

| ***Setup*** | ***a)*** | ***b)*** | ***c)*** | ***d)*** |
|---|---|---|---|---|
| $P_{OUT}$(dBm) | 0 | 2.5 | 4.5 | 10 |
| *Bit rate* (kbps) | 0.1 | 0.2 | 0.3 | 1 |
| *Avarage Input Power* (dBm) | $\sim 0$ | $\sim 0$ | $\sim 0$ | $\sim 0$ |
| *Achieved Sensitivity* (dBm) | $-56$ | $-57.5$ | $-60.2$ | $-64$ |

## 5.6 Conclusion

In this chapter, I have developed a dual band low-power wake-up radio receiver with on board addressing capability. Simulations and experimental results demonstrate the high sensitivity and the low power consumption of the realized prototype. In particular, using a dual-band antenna and dual impedance matching has been demonstrated that is possible to achieve high sensitivity of $-55.7$ dBm and $-53.2$ dBm at 868 MHz and 2.45 GHz, respectively.

The dual-band solution has been exploited to increase the flexibility of the wake-up radio, allowing interoperability with the two most common frequencies used in WSN and IoT. The final prototype consumed only 1.2 μW of power during the listening mode. A prototype demonstrator of the entire system has been shown together with a complete set experimental validation.

Completed this first task, I used the designed WuR receiver as testing device for carrying out a measurements campaign on POW signals applied to WuR radios. Experimental results shown that POW signals, by intermitted signals rather than by multi-sine excitations, outperform the state-of-the-art minimum RF power for WURs, taking advantage of the duration of the voltage envelope peaks. It has been measured that the comparator is able to operate and drive the main radio at average

power levels as low as −65 dBm. A possible drawback of these excitation choices could be an increase of the overall received signal bandwidth, which can be kept under control by a further shaping of POW themselves. The correct addressing of the WuR is then demonstrated by a suitable commercial transceiver and a similar increment of the sensitivity was verified.

# Thesis Conclusion

In this thesis, I have reported the main researches and activities results in which I was involved during my PhD studies. Thanks to the numerous aspects faced in these works, I have maturated an important background on a variety of arguments such as RF energy harvesting systems, radiative and non-radiative WPT links, capacitive links and bidirectional autonomous nonlinear circuits (oscillator/rectifier), concluding with complex signal processing to implement a POW-WuR system.

In particular, I have proposed an alternative architecture for realizing a bi-directional Class-F oscillator, in order to implement a fully autonomous power relay node for future implementation in IoT nodes. This result was possible by introducing two key novel aspects in the system: the gate self-bias mechanism, and the bias-assisting loop network. A proof of concept prototype has been developed and measured. The obtained results validate the feasibility of the proposed system as autonomous power relay node.

After this success, myself and my advisor decided to investigate a more complex but fascinating field which was completely new for the group where I worked: the monolithic circuit implementation of the realy node for miniaturizing the developed facility. In particular, a GaAs MMIC has been developed with the objective to demonstrate the realizability of the relay node with monolithic circuit. Very good results have been

obtained making this project a great experience truly positive for me.

I have also proposed a new near-field WPT architecture able to exploit the available PDAs antennas in order to wirelessly recharging devices with no need for dedicated charging stations. The proposed solution is interesting since it makes use of the existing antennas available in any PDA, connected to an adjoin diplexer network, able to decouple the radiation and the power re-charging paths. As a proof-of-concept a capacitive coupling system has been developed and experimentally validated. Due to the non-optimized antenna layout, the WPT link operates with lower efficiency than those proposed in the state-of-the-art. However, this efficiency results to be sufficient to realize small power transfer system compatible with the simple application of the method itself.

Finally, in order to extend my knowledge on low-power solution that can exploit RF energy harvesting, I focused on WuR systems. In this context, I introduced two interesting contributions. The first one consists of a dual-band ultra-low power wake-up radio for WSN application. The dual-band radio was exploited to increase the flexibility of the WuR, allowing interoperability with the two most common frequencies used in WSN and IoT. The second contribution is an experimental analysis of Power Optimized Waveform (POW) in order to define the optimum modulation to be used as the excitation source able to increase the WuR sensitivity. Experimental results shown that POW signals, by intermitted signals rather than by multi-sine excitations, outperform the state-of-the-art of minimum RF power for WURs, especially when the power levels are ultra-low. We demonstrated WuR activation with an incoming power as low as $-65$ dBm.

# List of Achievements

## International Awards:

- Student Design Competition in Wireless Energy Harvesting - **First Place**

  Honor date: May 2016 - International Microwave Symposium, San Francisco, USA.

  Honor issuer: IEEE Microwave Theory and Techniques Society.

- Student Design Competition - **First Place**

  Honor date: November 2015 - European School of Antennas in Barcelona, Spain.

  Honor issuer: European School of Antennas (ESoA).

- Student Paper Competition - **First Place**

  Honor date and place: September 2015 - 5th Meeting in Thessaloniki, Greece.

  Honor issuer: COST IC1301 - Wireless Power Transmission for Sustainable Electronics (WIPE).

- IMS 2015 Student Paper Competition - **Appointed as Finalist**.

  Honor date: May 2015 - - International Microwave Symposium, Phoenix, USA.

  Honor issuer: IEEE Microwave Theory and Techniques Society.

## Education:

- Teaching assistant at the course of electrical engineering, 2014 - 2015. Aerospace Engineer, University of Bologna.
- Teaching assistant at the course of electrical engineering, 2015 - 2016. Aerospace Engineer, University of Bologna.

## Workshop:

- A. Costanzo, D. Masotti, F. Berra, **M. Del Prete**, "Antenna Systems Architectures for Simultaneous Far-Field Communication and Near-Field WPT", 2017 International Microwave Symposium (IMS), Honolulu (Hawaii), 9th June 2017.
- **M. Del Prete**, A. Costanzo, "Energy-autonomous Bi-directional Wireless Power transmission (WPT) and Energy Harvesting Circuit"; COST IC1301 $5^{th}$ Management Committee, Working Group and Workshop; Thessaloniki (Greece).

## Projects:

- D. Dardari, A. Costanzo, "LOST in SPACE": Localization of Objects in Space through RF Tags. European Space Agency (ESA).

# Acknowledgments

At the end of this PhD, I would like to express my gratitude to all the people who helped me to reach this important goal.

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Again, a special thanks to Mihai Banu for the great opportunity of working at Blue Danube System in New Jersey as Antenna Engineer Intern. Beyond the skills I gained, this abroad period was for me an important opportunity for a personal growth. Moreover, I want to thank all the people who helped me in such adventure in the United States: Victor, Lidia, Norma, Josh and James (who took me to work every day!), Giovanni, and Payam.

I would like to extend my thanks to the research group in Cesena and Bologna composed by Alex, Francesco, Marco, Giacomo. They worked with me in the UniBo EM-Lab and together we reached important goals, attended at exciting international events and won some prizes. However, most important thing, we had a lot of fun doing all these stuffs!

Last but obviously not less important, I wish to express my greatest thanks and appreciation to my family, my girlfriend Cristiana, and all my friends who supported and support me every day.

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