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Characterization and Modeling of Semiconductor Power Devices Reliability

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Thank you all,
Andrea

Abstract

With the increasing demand for renewable energy and smart mobile low-power applications, a compelling need arises for switching mode semiconductor power devices that are lightweight, compact and evermore efficient and reliable. This last feature represents one of the main issues for power devices because it forces a trade-off between long lifetime, high performance and low cost. For this reason, the power devices reliability represents a challenge for the research community, even more in the emerging technologies based on gallium nitride (GaN).

This thesis aims at studying, characterizing and modeling the trapping and de-trapping mechanisms occurring during the ON-state operation mode and leading to the degradation of semiconductor power devices. In this operating condition, the combined effect of moderate electric fields, high currents and temperatures due to self-heating effects can seriously affect the long-term reliability leading to device failure. Detailed analyses are performed on both silicon and gallium nitride based technologies by means of accelerated life test methods and electro-thermal simulations, aimed at understanding the physical origins of the degradation.

In particular, this thesis provides the following contributions:

- the role of the interface and oxide trapped charge induced by negative bias temperature instability (NBTI) stress in p-channel Si-based U-MOSFETs is investigated. The impact of relevant electrical and physical parameters, such as stress voltage, recovery voltage and temperature, is accounted for and proper models are also proposed.

In the field of innovative semiconductor power devices, this work focuses on the study of GaN-based devices. In particular, three different subtopics are considered:

- a thermal model, accounting for the temperature dependence of the thermal boundary resistance (TBR), is implemented in TCAD simulator in order to realistically model self-heating effects in GaN-based power devices;

- the degradation mechanisms induced by ON-state stress in GaN-based Schottky barrier diodes (SBDs) are proposed by analyzing their dependence on the device geometry;
- the trapping mechanisms underlying the time-dependent gate breakdown and their effects on the performance of GaN-based power HEMTs with p-type gate are investigated, and an original empirical model representing the relationship between gate leakage current and time to failure is proposed.

List of Publications

1. **A. N. Tallarico**, P. Magnone, E. Sangiorgi, and C. Fiegna, "NBTI in p-channel power U-MOSFETs – Understanding the degradation and the recovery mechanisms", *IEEE International Conference on Ultimate Integration on Silicon (ULIS)*, pp. 145-148, Stockholm, Apr. 2014.

2. **A. N. Tallarico**, P. Magnone, G. Barletta, A. Magrì, E. Sangiorgi, and C. Fiegna, "Negative Bias Temperature Stress Reliability in Trench-Gated P-Channel Power MOSFETs", *IEEE Transactions on Device and Materials Reliability*, Vol. 14, No. 2, pp. 657-663, Jun. 2014.

3. **A. N. Tallarico**, P. Magnone, E. Sangiorgi, and C. Fiegna, "Modeling Self-Heating Effects in AlGaN/GaN Electronic Devices during Static and Dynamic Operation Mode", *IEEE International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, pp. 233-236, Yokohama, Sept. 2014.

4. **A. N. Tallarico**, P. Magnone, G. Barletta, A. Magrì, E. Sangiorgi, and C. Fiegna, "Modeling Spatial and Energy Oxide Trap Distribution Responsible for NBTI in p-Channel Power U-MOSFETs", *IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, pp. 153-156, Hong Kong, May 2015.

5. **A. N. Tallarico**, P. Magnone, G. Barletta, A. Magrì, E. Sangiorgi, and C. Fiegna, "Influence of bias and temperature conditions on NBTI physical mechanisms in p-channel power U-MOSFETs", *Solid-State Electronics*, Vol. 108, pp. 42-46, Jun. 2015.

6. **A. N. Tallarico**, S. Stoffels, P. Magnone, J. Hu, S. Lenci, D. Marcon, E. Sangiorgi, C. Fiegna, and S. Decoutere, "Reliability of Au-free AlGaN/GaN-on-Silicon Schottky Barrier Diodes under ON-State Stress", *IEEE Transactions on Electron Devices*, Vol. 63, No. 2, pp. 723-730, Feb. 2016.

7. **A. N. Tallarico**, P. Magnone, S. Stoffels, J. Hu, S. Lenci, D. Marcon, E. Sangiorgi, S. Decoutere , and C. Fiegna, "Understanding the Degradation Sources Under ON-state Stress in AlGaN/GaN-on-Si SBD: Investigation

of the Anode-Cathode Spacing Length Dependence", *IEEE International Reliability Physics Symposium (IRPS)*, pp. 4A51-4A56, Pasadena, Apr. 2016.

8. **A. N. Tallarico**, P. Magnone, S. Stoffels, J. Hu, S. Lenci, D. Marcon, E. Sangiorgi, S. Decoutere , and C. Fiegna, "ON-State Degradation in AlGaN/GaN-on-Silicon Schottky Barrier Diodes: Investigation of the Geometry Dependence", *IEEE Transactions on Electron Devices*, Vol. 63, No. 9, pp. 3479-3486, Sept. 2016.

9. J. Hu, S. Stoffels, S. Lenci, B. De Jaeger, N. Ronchi, **A. N. Tallarico**, D. Wellekens, S. You, B. Bakeroot, G. Groeseneken, and S. Decoutere, "Statistical Analysis of the Impact of Anode Recess on the Electrical Characteristics of AlGaN/GaN Schottky Diodes with Gated Edge Termination", *IEEE Transactions on Electron Devices*, Vol. 63, No. 9, pp. 3451-3458, Sept. 2016.

10. **A. N. Tallarico**, S. Stoffels, P. Magnone, N. Posthuma, E. Sangiorgi, S. Decoutere , and C. Fiegna, "Investigation of the p-GaN Gate Breakdown in Forward-biased GaN-based Power HEMTs", *IEEE Electron Device Letters*, Vol. 38, No.1, pp. 99-102, Jan. 2017.

11. J. Hu, S. Stoffels, M. Zhao, **A. N. Tallarico**, I. Rossetto, M. Meneghini, X. Kang, B. Bakeroot, D. Marcon, B. Kaczer, S. Decoutere, and G. Groeseneken, "Time-Dependent Breakdown Mechanisms and Reliability Improvements in Edge Terminated AlGaN/GaN Schottky Diodes under HTRB Tests", *IEEE Electron Device Letters*, Vol. 38, No.3, pp. 371-374, Mar. 2017.

12. S. Stoffels, **A. N. Tallarico**, B. Bakeroot, T. L. Wu, D. Marcon, N. Posthuma, C. Fiegna, and S. Decoutere, "Failure Mode for p-GaN gates under forward gate stress with varying Mg concentration", *IEEE International Reliability Physics Symposium (IRPS)*, accepted, Monterey, Apr. 2017.

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Chapter 1

Introduction

1.1 Power Electronics and its Applications

Power electronics can be defined as a branch of electrical engineering aimed at converting and controlling electric power for a wide range of applications, using high-efficiency electronic converters based on switching mode semiconductor power devices. Today, there is a strong interest in power electronics because of its important role in energy saving and storage [1], renewable energy systems [2], electric/hybrid vehicles [3], etc. Therefore, it is evident that power electronics may contribute to alleviate climate change or global warming problems [2], which are of paramount importance.

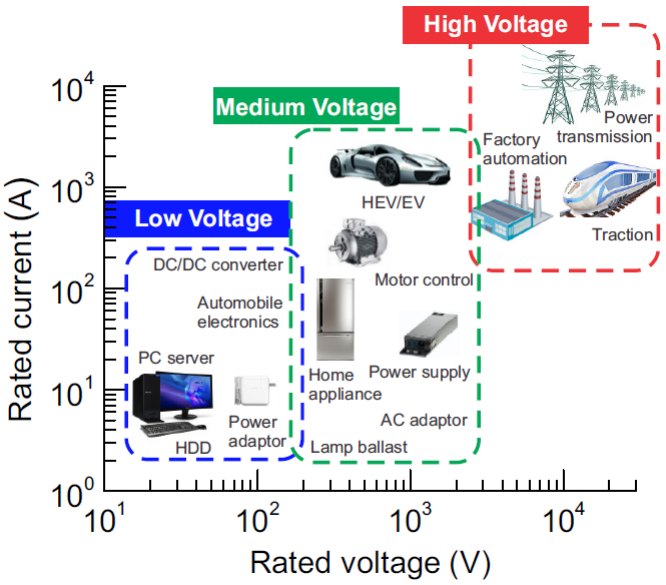

Figure 1.1: Fields of application as a function of different voltage and current ratings [4], [5].

Different voltage and current ratings are required to satisfy the vast range of power electronics applications. In particular, by mainly referring to the voltage rating, three macro areas (low, medium and high voltage) can be identified in Fig. 1.1. In this thesis, power semiconductor devices for application in the low voltage area ($\leq$ 200 V) are considered. In addition to voltage and current capabilities, the operating frequency is the other key factor that influences the choice of a specific device technology, allowing to minimize the size of passive components and hence to increase the overall power density.

1.2 Comparison of Semiconductor Technologies for Power Electronics

Fig. 1.2 shows the fields of application of silicon (Si), silicon carbide (SiC) and gallium nitride (GaN) based switching power devices as a function of the operating power and frequency. In particular, it is possible to notice that SiC-, GaN- and Si-based technologies are preferred for high power, high speed and low power low speed applications, respectively, according to the respective intrinsic material properties.

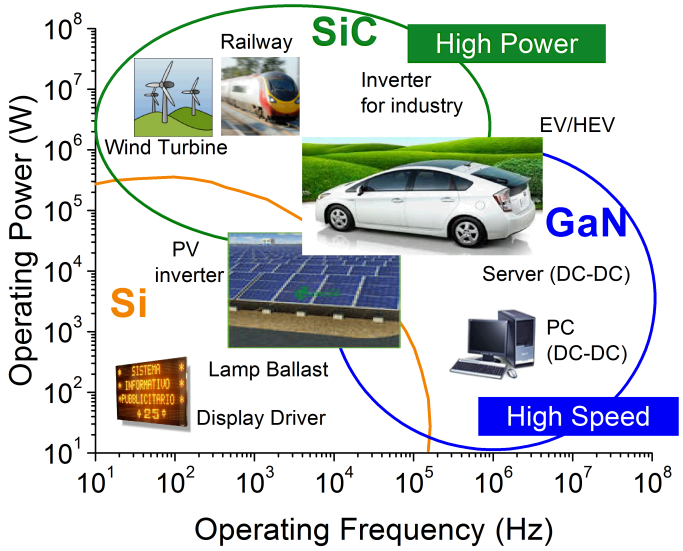

Figure 1.2: Fields of application as a function of operating power and frequency.

It is worth noting that SiC and GaN materials are compound semiconductors featuring much larger bandgap compared to silicon.

Fig. 1.3 compares the material properties for silicon, silicon carbide and gallium nitride, which have a high influence on the fundamental performance characteristics of the switching power devices [6], [7], because:

- a higher critical field, i.e. the field strength causing the onset of impact ionization and avalanche breakdown of the device, implies a larger breakdown voltage;
- a wider bandgap means lower intrinsic carrier concentration (n_i), which exponentially depends on the bandgap and temperature. Since leakage currents are proportional to n_i or n_i^2 [6], wider bandgap devices feature lower leakage currents;
- the higher the electron mobility, the lower the resistivity and the conduction losses in the device;
- according with the Johnson's FOM, i.e. the product of the charge carrier saturation velocity in the material and the electric breakdown field under same conditions, a higher carrier saturation velocity allows a higher frequency of switching [8]-[10];
- a higher thermal conductivity implies a more efficient heat conduction, therefore, larger power densities can be managed.

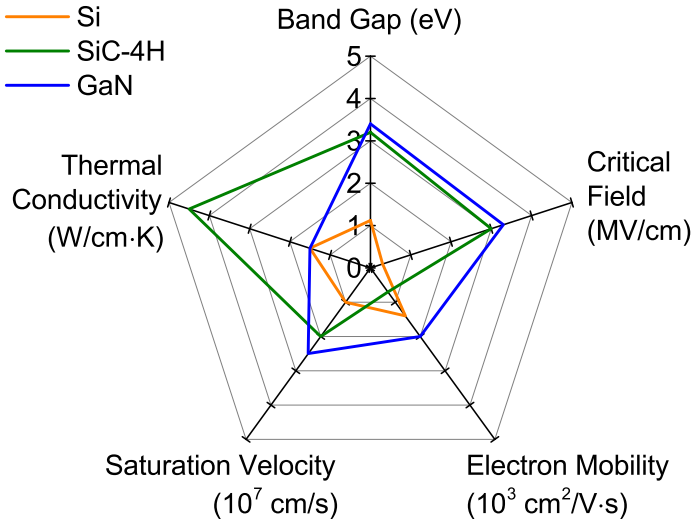

Figure 1.3: Impact of different physical parameters of semiconductor materials.

Consequently, as shown in Fig. 1.3, the higher electron mobility and saturation velocity identifies the GaN-based devices as the best solution for very high frequency power applications (high speed), whereas the higher thermal conductivity combined to high critical electric field and to wide bandgap establishes silicon carbide as one of the best materials for very high power operation. It is worth noting that at the device (transistor) level, the switching frequency is

mainly limited by the intrinsic capacitances of the device structure. However, as discussed in the next section, the better trade-off between breakdown voltage and ON-resistance allows a smaller GaN-based structure compared to Si-based one, having hence smaller capacitances. Finally, in the case of low power and low speed applications, Si-based devices are still preferred to SiC and GaN competitors because of the higher reliability and low cost due to technology maturity, discussed in the following chapters.

1.2.1 Theoretical limit of Si, SiC and GaN power FETs

An ideal power device should be characterized by a high switching frequency, good heat dissipation properties, a small ON-resistance and a large breakdown voltage. However, with reference to a conventional vertical power FET [11], while the switching speed and the thermal resistance are mainly dependent on the intrinsic capacitances of the structure, hence device dimensions and relative permittivity of the adopted materials, and by the thermal conductivity of the materials, respectively, in the case of ON-resistance and breakdown voltage a mutual dependence exists.

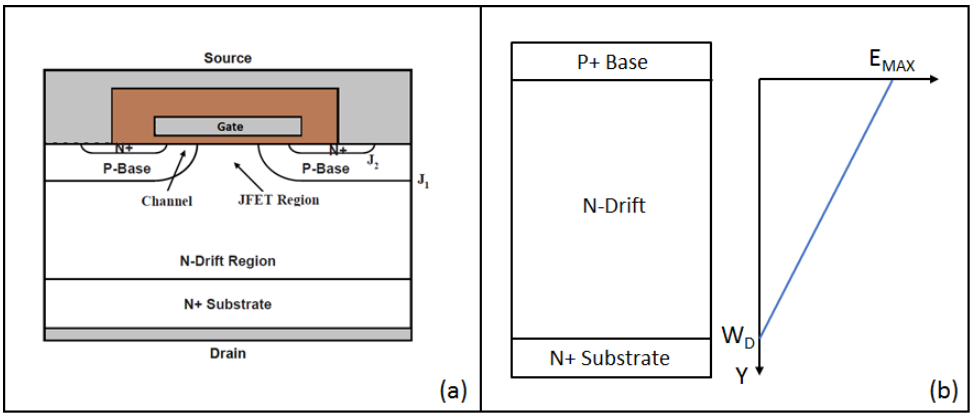

Figure 1.4: (a) Conventional vertical power MOSFET and (b) its electric field distribution in the drift region.

The maximum voltage (breakdown voltage) that a power device can support before the onset of a significant current flow is limited by the avalanche breakdown phenomenon caused by carrier multiplication by impact ionization. This latter occurs as the electron–hole pairs created by a carrier traversing the depletion layer and heated by a large electric field [11]. Consequently, the impact ionization and hence the breakdown voltage are strongly dependent on the magnitude of the electric field. The minimum value determining the avalanche breakdown phenomenon is named critical electric field (E_C) and is characteristics of each semiconductor material, as it is an increasing function

of bandgap.

The unipolar power devices, deeply discussed in the following sections, feature a drift region aimed at supporting the blocking voltage. Its properties can be analyzed by assuming an abrupt junction (P^+N) with high doping concentration on one side and a low uniform doping concentration on the other side as shown in Fig. 1.4. According to Poisson's equation, the maximum electric field (E_{max}) can be described as follows:

$$E_{max} = \frac{qN_D W_D}{\epsilon_0 \epsilon_r} \tag{1.1}$$

Breakdown occurs when $E_{max} = E_C$ and V_{DS} equals the breakdown voltage (BV). BV can be approximately evaluated as the voltage drop across the depletion region

$$BV = \frac{1}{2} E_C W_D = \frac{1}{2} \frac{qN_D W_D^2}{\epsilon_0 \epsilon_r} \tag{1.2}$$

where E_C, ϵ_0, ϵ_r, N_D, and W_D are the critical electric field, vacuum permittivity, relative permittivity of the semiconductor, doping concentration and maximum depletion width of the drift region, respectively. In the ON-state operation mode, the specific ON-resistance ($R_{ON,sp}$) associated to the drift region can be modeled as follows:

$$R_{ON,sp} = \rho W_D = \frac{W_D}{q\mu_n N_D} \tag{1.3}$$

where ρ and μ_n are the resistivity and the electron mobility, respectively. By replacing N_D and W_D by the expressions in Eq. 1.1 and 1.2, the so-called Baliga figure of merit (BFOM) [8] is attained:

$$\frac{R_{ON,sp}}{BV^2} = \frac{4}{\epsilon_0 \epsilon_r \mu_n E_C^3} \tag{1.4}$$

As shown in Eq. 1.4 the ratio of $R_{ON,sp}$ to BV^2 is fixed by the intrinsic properties of the material. As a result, by considering the material parameters reported in Table. 1.1 for silicon, silicon carbide and gallium nitride, the corresponding theoretical limits can be extracted as shown in Fig. 1.5 (lines).

$Material$	E_c (MV/cm)	μn (cm^2/Vs)	ϵ_r
Si	0.23	1350	11.8
SiC	2.2	950	9.7
GaN	3.3	1800	9

Table 1.1: Material properties of Si, SiC and GaN [12].

It is worth noting that real semiconductor devices (symbols) are generally far from ideal structures and so it is always a challenge to achieve the theoretical

limit. In particular, the channel mobility in real devices is lower than bulk (Si and SiC) mobility reported in Table 1.1 because of the surface scattering and/or high electric field related mechanisms, whereas the channel 2DEG mobility in GaN device is mainly reduced because of the process-related degradation under the gate area. Moreover, the theoretical limit is calculated by considering only the resistive contribution of the drift region whereas the real devices are affected by additional resistive effects contributing to the overall ON-resistance, especially in the low voltage field.

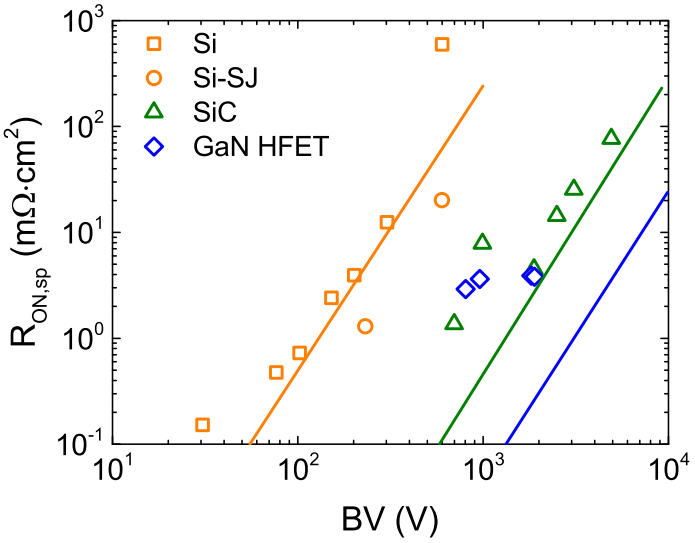

Figure 1.5: Specific ON-resistance per unit area as a function of the breakdown voltage for silicon, silicon carbide and gallium nitride. Theoretical limits (lines) and experimental data reported in [16] (symbols).

By observing Fig. 1.5 it is possible to notice that: i) the silicon FETs show more severe limitation compared to SiC and GaN counterparts. By increasing the voltage rating, Si-based devices provide less efficient electronics applications because of the higher resistance, hence higher conduction losses. As a result, for voltage range higher than about 200 V, GaN- and SiC-based devices seem to be preferable to silicon ones. Regarding the choice between SiC and GaN, as partially anticipated in Fig. 1.3, others factors like temperature handling, switching frequency and cost have a major impact; ii) by reducing the breakdown voltage, real devices (see Si-based devices in Fig. 1.5) show a larger resistance compared to its limit because, as previously anticipated and deepened later, additional resistive components start to give an important contribution to the overall R_{ON}; iii) GaN-on-Si devices are still far from own theoretical limit because the failure mechanisms are not due to avalanche breakdown occurring between drain and source but to vertical (buffer) breakdown occurring between

drain and substrate caused by the presence of defects due to lack of maturity process [13]-[15].

1.2.2 Si-based Power MOSFETs

The first commercially available power MOSFET was developed by using a vertical double-diffusion process. The vertical structure was necessary in order to withstand high voltages and currents required by a power circuit. Thanks to this approach drain and source are located on the opposite sides of the wafer allowing the use of thicker metal fingers (drain and source) compared to the lateral structure, where these latter must be interdigitated [11]. In addition, the electric field/potential distribution within the vertical structure is more appropriate for supporting high voltages.

The vertical-diffused (VD)-MOSFET structure is shown in Fig. 1.6. Without the application of a gate bias, a high positive voltage can be sustained between drain and source. In this case, junction J1 formed between the P-base and the N-drift region becomes reverse biased and the applied voltage is mainly supported by the lowly doped N-drift region.

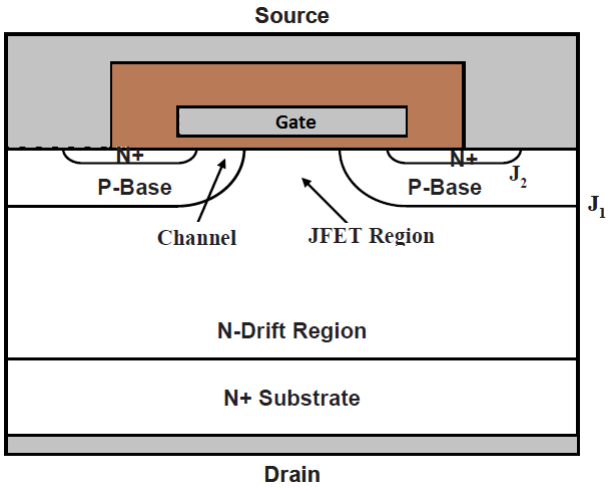

Figure 1.6: Vertical-diffused (VD)-MOSFET structure.

By applying a positive gate bias ($V_G > V_{TH}$) the channel is formed at the P-base/Oxide interface, providing a current path from the drain to the source when a positive drain voltage is applied. After drifting from the source region through the channel, the electrons are confined in a narrow JFET region located between the adjacent P-base regions within the VD-MOSFET structure. The higher is the applied drain voltage the thinner is the JFET region because of the wider depletion regions of the reverse biased junctions J1. As a result, this current confinement increases the internal resistance. Moreover, after being

transported through the JFET region, the current spreads from the narrow JFET region to the entire width of the N-drift section. This nonuniform current distribution increases the ON-resistance, making it larger than the ideal values of the drift region [11].

In order to reduce series resistance, an alternative device structure called trench-gate or U-MOSFET was developed by adopting a trench technology. As shown in Fig. 1.7 the trench extends from the upper surface of the structure to the N-drift region avoiding the JFET region. Consequently, the U-MOSFET structure offers the opportunity to reduce the internal resistance of the power MOSFET closer to the ideal value and to increase the cell density. Moreover, subsequent structure optimizations improved also the operating frequency for power MOSFETs up 1-MHz range [11].

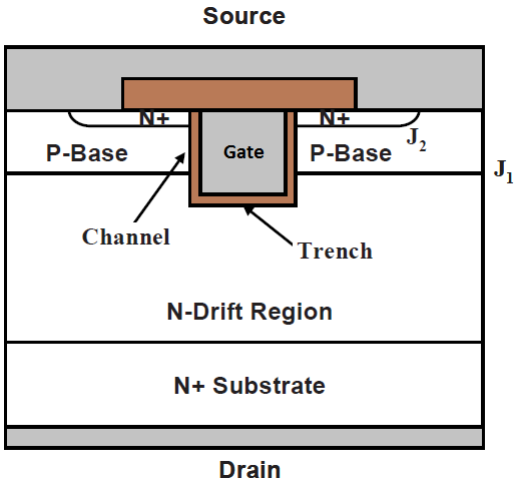

Figure 1.7: Trench-gate or U-MOSFET structure.

Taking into account the discussion of Section 1.2.1, it is evident that the higher is the breakdown voltage the higher and more dominant is the resistive contribution of the N-drift region. Consequently, this kind of structure are not inclined to very high voltages. On the other hand, by observing Figs. 1.6 or 1.7 it is possible to observe that by reducing the breakdown voltage, thus the N-drift resistance, other resistive components such as channel, accumulation, source/drain contacts, may become dominant avoiding to follow the theoretical limit (see Fig. 1.5).

In order to guarantee larger breakdown voltages with lower ON-resistances than a conventional power MOSFET, a new architecture named superjunction (SJ)-MOSFET has been implemented (Fig. 1.8).

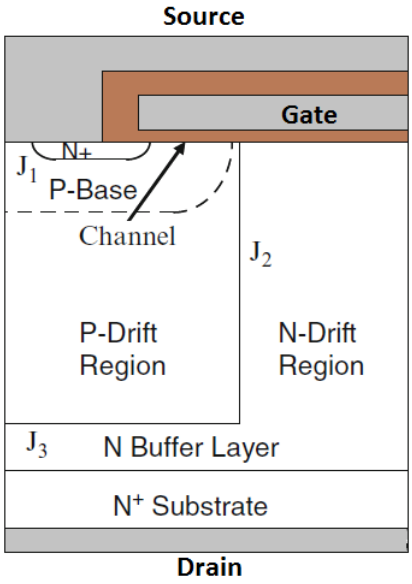

Figure 1.8: Superjunction (SJ)-MOSFET structure.

The principle behind the blocking voltage is different from that for the power MOSFET structures previously described. In this case, when a positive drain bias is forced in absence of an applied gate voltage, depletion regions are formed across the vertical junction J2 and the horizontal MOS interface creating the desired two-dimensional charge-coupling phenomenon [17], and the horizontal junction J3 creating the two-dimensional depletion phenomenon [17].

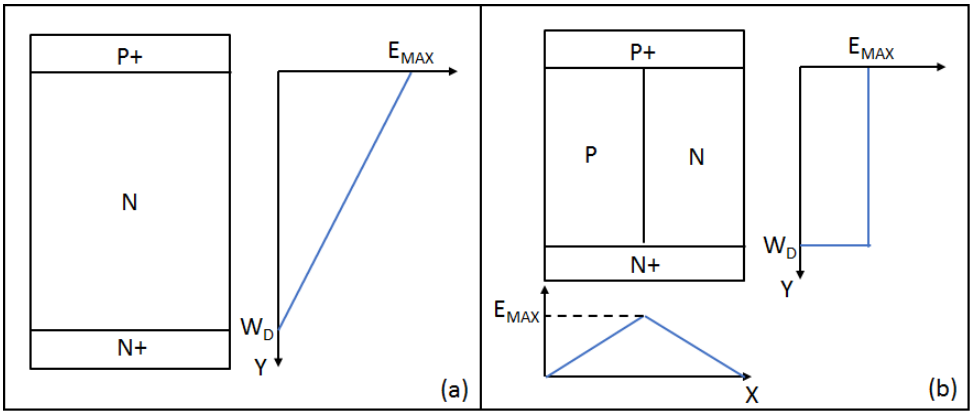

Figure 1.9: (a) The ideal drift region and its electric field distribution (conventional vertical power MOSFET), (b) basic charge coupled structure and its electric field distributions (SJ-MOSFET).

Consequently, the electric field distribution along the y-direction is altered from the triangular shape (Fig. 1.9a), observed in conventional junctions (VD- and U-MOSFET case), to a rectangular shape (Fig. 1.9b) (SJ-MOSFET) with a lower maximum field value for a given drain voltage. This allows to support a required blocking voltage over a shorter distance when compared with conventional power MOSFETs.

In addition, the doping concentration of the N-type drift region can be made much higher than that of a VD- or U-MOSFET, allowing a reduction of the specific ON-resistance below the ideal theoretical limit at any desired breakdown voltage (see Si-SJ in Fig. 1.4).

It is worth noting that, nowadays, in order to further increase the blocking (breakdown) voltage, similar structures are being proposed by simply replacing silicon with silicon carbide material [18], [19].

1.2.3 GaN-based High Electron Mobility Transistors (HEMTs)

High Electron Mobility Transistors (HEMTs) are based on an AlGaN/GaN heterostructure able to form a sheet of electrons with high density and mobility thanks to its intrinsic properties. In particular, because of a different electronegativity between gallium (Ga) and nitride (N), both AlGaN and GaN feature a spontaneous polarization as a bulk property. Moreover, the smaller lattice constant (aluminum concentration dependent) of the AlGaN induces a piezoelectric polarization due to mechanical stress (strain) occurring when the thin AlGaN layer is grown on the top of the GaN. Consequently, due to the charge compensation, a sheet of electrons is attracted at the AlGaN/GaN interface forming the so-called 2-dimensional electron gas (2DEG) [20], [21].

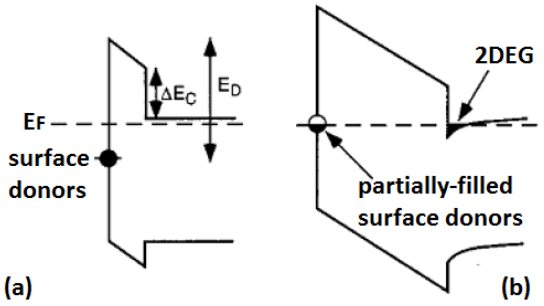

Figure 1.10: Band diagram showing the surface donor state in the case of undoped AlGaN barrier thickness (a) thinner than, and (b) thicker than the critical thickness for the formation of the 2DEG [22].

However, the origin of this negative charge is not so clear due to the absence of any intentional doped layer. The most accepted physical explanation consists in the presence of donor states at the AlGaN surface able to provide the source

of electrons for the 2DEG channel [21]. As a result, the thickness of the AlGaN layer play a fundamental role in the formation of the 2DEG. After a critical thickness, depending on the polarization contributions, the donor states cross the Fermi level (see Fig. 1.10b) and provide negative charge aimed at forming the 2DEG. More information on the physics of the 2DEG formation can be found in [20]-[22].

Due to the unavailability of large wafer size (above two inches) and high quality GaN bulk substrates, different solutions have been considered in order to grow the AlGaN/GaN heterostructure on top of foreign substrates. Today, many research groups have been fabricating GaN-based devices on large-area silicon substrates [23], [24] in order to guarantee a low-cost production.

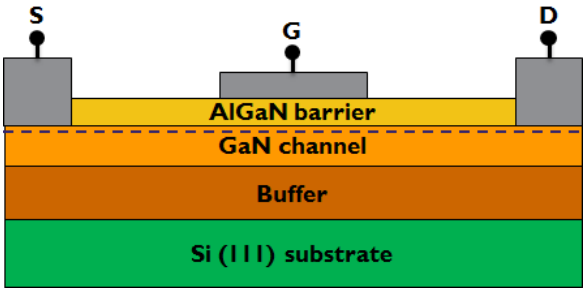

Figure 1.11: Conventional structure of a depletion-mode high electron mobility transistor (HEMT).

A typical structure of the GaN-based HEMT is shown in Fig. 1.11. Differently from Si-based MOSFETs, GaN HEMTs feature a lateral structure with two ohmic contacts (source and drain) connected to the 2DEG via a low-resistance path, and a Schottky gate contact on top of the AlGaN barrier able to modulate the 2DEG concentration by depleting or enhancing the charge density below the gate.

The huge difference in terms of thermal expansion coefficients and the large lattice mismatch occurring between GaN and silicon crystal, requires the epitaxial growth of an intermediated buffer ensuring a gradual variation of these properties along the stack aimed at avoiding the formation of cracks in the AlGaN/GaN heterostructure.

A relevant issue, limiting the adoption of GaN devices in power applications, is the negative threshold voltage (depletion-mode) due to the spontaneous formation of the electrons channel. On the other hand, power electronics applications require enhancement-mode devices for safety, power consumption and cost reasons [7].

To overcome this issue, several techniques have been developed to make normally-OFF GaN-based transistors. Interesting results come from HEMT structures in which a particular interlayer is placed between the heterostructure

and the gate contact, allowing to change the threshold voltage behavior and to enhance the positive swing of the gate terminal. In particular, MIS- and/or MOS-HEMTs, shown in Fig. 1.12a, are based on a deep barrier recess under the gate region [24], [25].With this solution the AlGaN barrier thickness is reduced below its critical thickness and, as previously discussed, the 2DEG formation is not allowed under the gate. Fig. 1.12b shows the structure of a p-gate HEMT. By introducing a p-type gate (pGaN or pAlGaN) the conduction band of the gallium nitride (GaN) in the channel is pulled up, opposing to the formation of the 2DEG [27]. However, these additional layers lead, as discussed in this thesis, to degradation mechanisms which need to be studied further.

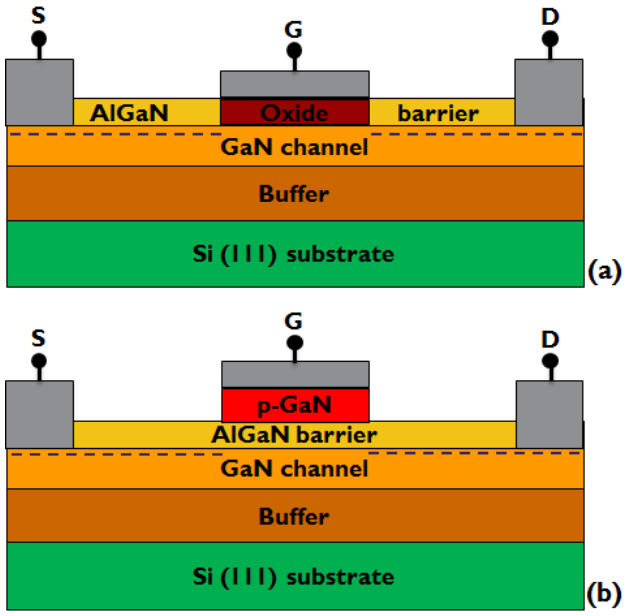

Figure 1.12: (a) Metal-oxide-semiconductor (MOS)-HEMT and (b) p-type gate HEMT structure.

1.3 Role of Switching Power Devices in Electronics Applications

By considering low voltage electronics applications ($\leq$ 200 V), an example of the most common and probably the simplest power stage topology, based on switching mode semiconductor power devices, is the DC-DC buck (step-down) converter [28] shown in Fig. 1.13. It is wort noting that this example is only aimed at introducing the role and the required features of the transistor and diode within a possible real electronics application and not at fully explaining the theory behind the DC-DC converter.

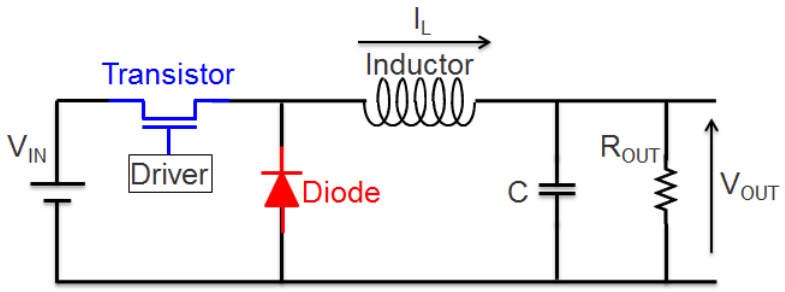

Figure 1.13: Circuit schematic of a simplified buck (step-down) converter which allows for the down-conversion of DC voltage.

Buck converter is a power supply which steps down voltage (while stepping up current) from its input (supply) to its output (load) with conversion efficiency close to 90 % [29]. The relationship between input and output voltage, under the hypothesis of continuous conduction mode operation, is given by Eq. 1.5:

$$V_{OUT} = V_{IN} \frac{t_{ON}}{T_S} = V_{IN} D \tag{1.5}$$

where t_{ON}, T_S and D are the transistor ON-time during each switching cycle, the switching period and the duty-cycle, respectively. It is worth noting that being D a number between 0 and 1 it is evident that V_{OUT} will be always lower or at least equal to V_{IN}.

Power electronics designers choose the buck converter because the output voltage has always the same polarity of the input voltage. Moreover, the output is not isolated from the input meaning that they can share a common ground reducing the circuit complexity, hence area and cost.

By referring to Fig. 1.13, the circuit includes a controlled power switch, which usually is an enhancement mode (normally-OFF) transistor for safety, power consumption and cost reasons [7], a so-called freewheeling Schottky diode, an inductor (L) and a capacitor (C) forming the output filter, and a resistor (R_{OUT}) representing the load. It is worth noting that a Schottky diode is preferred with respect to other kinds of diode due to its lower forward voltage leading to lower power dissipation during ON-state operation and because of the reduced reverse recovery current.

When the transistor switches ON the circuit is reduced to Fig. 1.14. The diode is reverse biased and the current through the inductor increases linearly according to Faraday's law. During this phase the supply provides energy, through the transistor, to the load and the inductor stores energy associated to a magnetic field.

When the transistor is turned OFF a large voltage up to V_{IN} is present at the drain-source port, the energy flow coming from the supply is stopped and the inductor starts to behave as a source thanks to the energy stored during

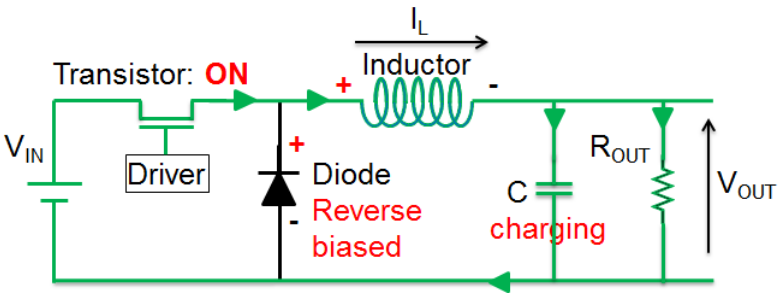

Figure 1.14: ON-state operation of buck converter. The transistor is in ON-state whereas the diode in OFF-state.

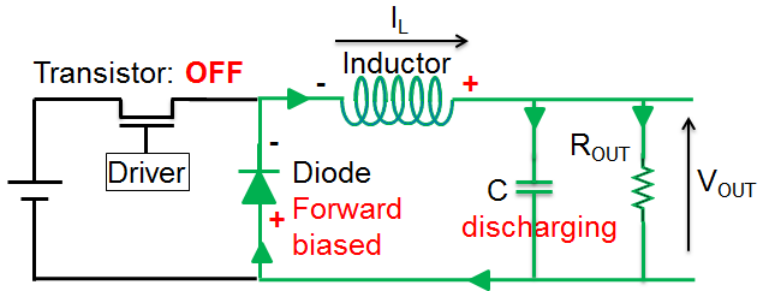

Figure 1.15: OFF-state operation of buck converter. The transistor is in OFF-state whereas the diode in ON-state.

the previous phase. At this time the voltage across the inductor reverts its polarity, thus forcing the diode in forward mode and supplying the current flow through the load as shown in Fig. 1.15.

The role of the freewheeling diode is crucial for the converter operation since it avoids an abrupt current variation on the inductor when the transistor is switched OFF. In fact, given the relationship between the inductor (L), the voltage (v(t)), and the current (i(t)):

$$v(t) = L\frac{\delta i(t)}{\delta t} \tag{1.6}$$

an abrupt change of the current can cause a huge voltage spike damaging the load or the other circuit components.

Based on the discussion on the roles played by switching mode semiconductor power devices (transistor and diode) in an example of DC-DC converter, the power losses might be analyzed in order to understand how the characteristics of each device impact the performance and the efficiency of a power electronics circuit.

The power loss of a switching circuit has two parts: static and dynamic power loss. The static power loss is mainly determined by the ON-resistance of

the transistor and Schottky diode during the conduction mode. The dynamic power loss occurs when the device (transistor and diode) switches from ON-state to OFF-state or vice versa. Consequently, devices with a fast switching capability and low recovery current are preferred to lower the dynamic power dissipation.

In addition, a faster switching frequency allows to reduce the size of the inductor (L) and of the capacitor (C), improving the power density of the circuit [30]. In order to understand this latter relationship, the output voltage ripple (ΔV_{OUT}) of the DC-DC buck converter may be considered. Under the hypothesis of continuous conduction mode operation, it can be calculated as:

$$\frac{\Delta V_{OUT}}{V_{OUT}} = \frac{1}{8}\frac{T_S^2(1-D)}{LC} = \frac{\pi^2}{2}(1-D)\Big(\frac{f_C}{f_S}\Big)^2 \tag{1.7}$$

with switching frequency $f_S = 1/T_S$ and corner frequency (f_C):

$$f_C = \frac{1}{2\pi\sqrt{LC}} \tag{1.8}$$

Equation 1.7 shows that the voltage ripple can be reduced by selecting a corner frequency (f_C) of the output filter (LC) such that $f_C << f_S$. For a given output voltage ripple (which is a key factor for DC-DC converters), the adoption of devices with a faster switching capability allows to use smaller passive components such as inductor and capacitor.

In conclusion, it seems obvious that wide bandgap devices could be potentially preferred to silicon ones. However, to win a place in the power electronics market, high performance is not enough since a low cost and a high level of reliability has to be guaranteed. In the next sections, the different technologies are compared in terms of costs and reliability.

1.4 Costs Comparison

Costs comparison between different technologies can be difficult since various elements of cost such as starting material, epitaxial growth, wafer fabrication and assembly [12] must be taken into account. Nowadays, it is well know that SiC-based devices feature a higher cost with respect to Si and GaN competitors due to the greater complexity of epitaxial growth and wafer fabrication [31], [32]. Therefore, the silicon technology is preferable, except for very high power electronics applications for which, as discussed in section 1.2, high thermal conductivity, critical field and wide bandgap are necessary.

Today, since GaN-based devices (transistors and Schottky diodes) with a voltage rating lower than about 600 V are mainly fabricated in thin (Al)GaN layers grown on 200 mm standard silicon substrate [33]-[35], there is not significant cost difference with power Si-MOSFETs produced on a wafer of

the same diameter. However, by considering that GaN transistors, thanks to intrinsic material properties, are able to withstand larger current densities compared to Si competitors, the cost per function is further reduced [12].

Unfortunately, the huge difference in terms of thermal expansion coefficients and the large lattice mismatch occurring between GaN and silicon crystal, requires the epitaxial growth of an intermediated buffer ensuring a gradual variation of these properties along the stack. This latter can be formed by multiple step-graded AlGaN buffers (Fig. 1.16a) with thickness up to few μm [36] or an AlN/GaN superlattice stack [37] (Fig. 1.15b) aimed at avoiding the formation of cracks in the GaN heterostructure. This is usually performed by means of metal-organic chemical vapor deposition (MOCVD) [38], which provides high quality buffer but at high costs due to the need of additional raw materials. Consequently, up to now GaN epitaxy on silicon is more expensive than Si epitaxy. However, assuming the strong interest in manufacturing GaN-on-Si devices, it is expected that the cost of GaN epitaxy will approach that of silicon [12].

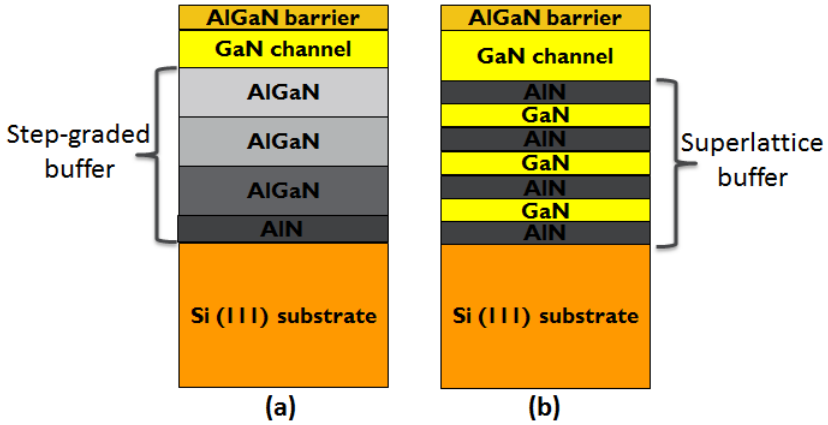

Figure 1.16: Example of a structure stack with (a) a multiple step-graded AlGaN and (b) an AlN/GaN superlattice buffer.

GaN-based devices are currently fabricated in high-productivity silicon CMOS facilities with processing temperatures similar to those of Si-competitors. Moreover, the GaN transistors structure is characterized by much fewer processing steps compared to silicon power MOSFETs [12]. As a result, the cost is reduced and it may become lower as the GaN transistor production volumes grow.

Finally, GaN-based devices can be packaged at a lower cost because of the lateral structure. In fact, they can be assembled in a wafer level chip-scale package (WLCSP) with terminals in a land grid array (LGA) [12] without compromising the electrical, thermal, or reliability characteristics. On the other hand, in the case of Si power MOSFETs, electrical package connections need

to be made to the top and bottom because of the vertical structure, increasing the package complexity and the cost.

In conclusions, by analyzing starting material, epitaxial growth, wafer fabrication and assembly costs it may be expected that GaN-based power devices can be fabricated at comparable or even, as expected for the future, lower costs compared to Si-based power transistors. However, it is worth noting that, nowadays, in order to increase the device voltage rating above 600 V other substrates such as SiC, AlN, etc. are required and still under investigation in terms of reliability and cost.

1.5 Reliability Issues

In the case of power devices, reliability is the most crucial and often the most challenging characteristic to be guaranteed in combination with high performance and low cost.

The Institute of Electrical and Electronics Engineers (IEEE) defines reliability as "the ability of a system or component to perform its required functions under stated conditions for a specified period of time" [39]. In the semiconductor power devices area the expected lifetime before failure usually ranges between 10 and 20 years.

Semiconductor device reliability may be related to different process aspects such as: i) undesired impurities due to many process steps adopted during fabrication phase; ii) thin layers deposition; iii) introduction of new material and processes; iv) assembly and environmental conditions, etc. Consequently, each of these factors can induce one or more failure mechanisms affecting the device reliability.

Before analyzing in detail the induced failure mechanisms it is really important to understand how and when the device reliability can be affected. By considering the buck DC-DC converter shown in Fig. 1.13 it is possible to summarize that:

- when the converter is in ON-state operation mode (Fig. 1.14) the transistor is in ON-state regime whereas the diode is reversely biased. In this phase, the transistor has to handle a moderate positive (normally-off technology) gate voltage aimed at allowing a high current flow between drain and source. As a result, the moderate gate bias, the high drain current and the high channel temperature due to self-heating effects may trigger degradation mechanisms, generally induced by charge trapping and/or electron migration phenomena [40], [41], affecting the transistor reliability. Concerning the diode, it must withstand a high reverse voltage inducing high electric fields degrading the device;

- when the converter is in OFF-state operation mode (Fig. 1.15) the transistor is switched-OFF whereas the diode is in forward regime. In

this case the transistor is subject to a high drain voltage (high electric field) promoting the creation or activation of defects degrading device performance [42]. On the other hand, the diode has to handle high forward currents; under this condition the combined effect of high current, moderate electric field and high junction temperature can affect the diode reliability;

- finally, a third operation condition, called semi-on-state, occurs during the switching transient. In this phase, the transistor operates with small output current and moderate drain bias. As a result, electrons present in the channel can be accelerated by the applied electric field becoming "hot electrons " and triggering trapping mechanisms [43].

Since the reliability analysis involves phenomena whose time-scale is in the order of many years, accelerated test methods have to be adopted in order to evaluate the device lifetime and to identify the involved degradation mechanisms in a reasonable time. Using temperature, voltage, current, and humidity as acceleration factors [44], failure can be induced earlier than usual and with the adoption of extrapolation methods the lifetime under nominal operation mode can be estimated. It is therefore evident the relevance of research on device reliability issues: without a correct investigation aimed at understanding the physical mechanisms inducing device degradation and failure, the reliability predictions are expected to become meaningless and the empirical estimations will be very inaccurately related to process modifications, device geometry, voltage and current ratings.

In this thesis, the experimental characterization of degradation mechanisms induced by ON-state stress and affecting the reliability of Si-based power U-MOSFETs, GaN-based Schottky diodes and transistors are investigated. Moreover, TCAD simulations aimed at understanding the sources of degradation are performed in combination to experimental tests.

1.6 Outline of the Thesis

This dissertation is organized as follows:

- Chapter 2 shows the results of an activity developed in collaboration with *STMicroelectronics* inside an European project named "E2SG Energy to smart grid". The purpose was the investigation of the degradation mechanisms induced by negative bias temperature instability (NBTI) in trench-gated p-channel power Si-MOSFETs (U-MOSFETs). Hence, various measurements techniques have been adopted in order to distinguish interface and bulk-oxide traps and a combined measurement/simulation method, aimed at estimating the spatial and energy oxide trap distribution, has been implemented;

- Chapter 3 is focused on the results obtained inside an European project named "E^2COGaN Energy Efficient Converters using GaN Power Devices". A physical model interface (PMI), accounting for the temperature dependence of the thermal boundary resistance (TBR) associated to the heterojunction transition layer, has been implemented by means of Sentaurus TCAD in order to realistically model self-heating effects. In particular, TBR associated to the nucleation layer between GaN and SiC- or Si-substrate was taken into account and the influence of the temperature on the surface charges trapping and de-trapping was investigated;

- Chapter 4 describes the results of an activity developed in collaboration with the *interuniversity microelectronics centre* (*imec*). A combined measurement/simulation analysis has been performed in order to understand the degradation mechanisms induced by ON-state stress in GaN-based Schottky barrier diodes (SBDs). In particular, by analyzing the geometry dependence, the physical mechanisms responsible for long-term degradation of SBDs have been identified;

- Chapter 5 reports the results of an experimental activity performed in collaboration with *imec*. The time-dependent breakdown, induced by forward gate stress in GaN-based power HEMTs with p-type gate, has been analyzed. In particular, the mechanisms underlying the gate breakdown and its effects on the device performance have been investigated by adopting different stress conditions, analyzing the influence of the temperature, and investigating the activation energy of the traps. In addition, an original empirical model, representing the relationship between gate leakage current and time to failure, has been proposed.

- Chapter 6 summarizes the main achievements of this PhD research project.

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Chapter 2

NBTI Reliability in Si-based Power U-MOSFETs

2.1 Introduction and State of the Art

Negative Bias Temperature Instability (NBTI) [1] is one of the main degradation mechanisms limiting the long-term reliability of power MOSFETs biased above threshold [2], [3]. The same effect is also referred to as Negative Bias Temperature Stress (NBTS) or High Temperature Gate Bias (HTGB) and is commonly observed in p-channel devices when stressed with negative gate voltages at elevated temperatures. In particular, when a large gate voltage combined with a high temperature is applied and the other terminals are short circuited to ground or held to the same potential, charge trapping and interface states generation mechanisms occur in the bulk gate oxide and at the semiconductor/oxide interface, respectively [4], [5]. These phenomena lead to a degradation of electrical parameters such as threshold voltage (V_{TH}), charge carrier mobility, ON-resistance, trans-conductance and sub-threshold slope [1], which are important figures of merit characterizing a power MOSFET.

The interface states (N_{it}) generation is usually ascribed to the breaking of SiH bonds at the SiO_2/Si interface by a combination of electric field, temperature and holes effects [4], whereas the build-up of positive oxide charge (N_{ot}), may be due to H^+ de-passivation [5] or hole trapping. However, the details how NBTI occurs and how it can be recoverable are not entirely clear.

Different models, by different groups, have been proposed on NBTI related physical mechanisms. A stress time linear-dependent SiO_2/Si interface traps generation has been suggested in [6]-[8] by means of a Reaction-Diffusion (R-D) model. In particular, hydrogen is released during reaction phase and then diffused from interface to oxide (diffusion phase) with a time dependence of $t^{0.25}$. Grasser et al. in [9] have proposed a four-energy-well model accounting for the coupled contribution of interface states and oxide traps. Instead, for [10] the NBTI phenomenon is ascribed to uncorrelated contribution of the

interface states and oxide traps, suggesting that only the oxide defects are involved in the recovery mechanism. Finally, on the other hand, a fast trapping and de-trapping mechanism of the oxide defects, with a slow recovery of the interface states, has been proposed by Mahapatra et al. [11].

Although many papers about NBTI reliability of CMOS technology have been published [12], [13], similar phenomenon affecting power MOSFETs received much less attention so far. However, as power devices are scaled down and large voltages are applied, NBTS together with the High Temperature Reverse Bias (HTRB), represent the main degradation mechanisms limiting the long-term power device reliability.

Limited studies have been performed on power VD-MOSFETs in order to understand [14] and to overcome [15] NBTI induced degradation. In particular, in [16] the oxide-trapped charge build-up is attributed to hole tunneling from the silicon valence band to oxygen vacancy defects, whereas the interface state generation is due to the electro-chemical reaction of the interface precursor with the charged oxide traps. Other studies, referred to as High Temperature Gate Bias (HTGB) but related to the same NBTI mechanisms, have been carried out on different structures of power MOSFETs. In particular, in [3] is reported a study of SiC power MOSFETs in which the V_{TH} shift is ascribed to the trapping and de-trapping of charge from the near interfacial oxide traps, whereas Aoki et al. [17] have treated a reliability study of trench gate power MOSFET with partially thick gate oxide film structure.

In this chapter, the NBTI degradation mechanisms in p-channel Si-trench power MOSFETs, also referred to as U-MOSFET, is extensively analyzed by investigating the impact of gate stress (voltage and temperature) on the main figures of merit, such as threshold voltage, trans-conductance and subthreshold slope.

First of all, different methods for evaluating NBTI stress-induced threshold voltage shift (ΔV_{TH}) are considered and discussed in order to highlight the fast-partial recovery phase occurring during the characterization phase. Then, besides the analysis of the degradation occurring during the stress phase, the recovery phase happening after the removal of the gate bias stress is also investigated. This analysis is performed at different recovery voltages and temperatures in order to understand how their contribution affects the recovery phase. Thanks to this approach, it is possible to ascribe the threshold voltage recovery, for the monitored time window, to the charge de-trapping from bulk oxide. Consequently, although various on-wafer techniques have been proposed for estimating the oxide trap distribution [18], [19], they cannot be easily applied in power U-MOSFETs, because of its vertical structure and because bulk and source terminals are often short-circuited. Therefore, in this work a method based on a combination of DC measurements and TCAD numerical simulations has been implemented. As a result, the oxide trap density, including its energy distribution and its distance from the Si interface,

has been calculated by evaluating the V_{TH} shift during the recovery phase.

2.2 Device Structure and Experimental Setup

Silicon-based p-channel power U-MOSFETs (Fig. 2.1), realized on-wafer by ST Microelectronics, are considered in this study. The gate stack is composed of $Polysilicon/SiO_2/Silicon$ layers, the channel length is 0.5 μm, the equivalent channel width is 69 cm and the oxide thickness is 40 nm. The device is composed by many fingers in parallel featuring of a maximum gate operation voltage of -16 V.

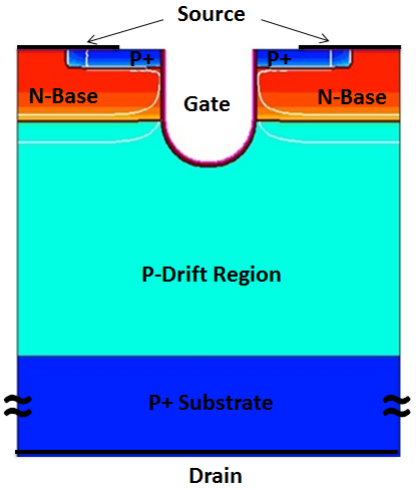

Figure 2.1: A Schematic of a p-channel trench-gate power MOSFET. It features a gate stack composed of $PolySi/SiO_2/Si$ layer, a channel length of 0.5 μm, an equivalent channel width of 69 cm and an oxide thickness of 40 nm. The U-shape of the gate allows the lowest ON-resistance (R_{ON}) among all MOS structure since JFET region is avoided.

This structural device architecture appears as the most suitable one for low to medium voltage power applications because of the opportunity to reduce the internal resistance closer to the ideal value [20], hence offering the lowest possible ON-resistance among all MOS devices [21], [22]. In particular, compared to conventional VD-MOSFET structure, the JFET region is avoided enabling a significant reduction of the overall specific ON-resistance. Moreover, the elimination of the JFET region allows a smaller cell pitch reducing the resistance contribution of channel, accumulation and drift regions [20].

On-wafer measurements were performed by means of a 200-mm Cascade probe station with an integrated Temptronic thermochuck able to warm up the wafer till temperatures of 150°C. Since the temperature is an acceleration

factor for the degradation induced by NBTI stress [23], the use of a high temperature allows to reach larger degradation in shorter times. In addition, Keithley System Measurement Units (SMUs) 26XX, controlled in a Lab-View environment, were used in order to force the bias stress/recovery and for IV measurements.

2.3 Measurements Techniques

Devices were stressed under NBTI, by applying a large gate voltage, and by grounding drain and source terminals in order to have a uniform degradation along the channel. After the stress a recovery phase was performed by forcing a gate bias equal or lower than threshold voltage. The temperature was kept constant during both stress and recovery phases. The drain bias during the measurement phases (both stress and recovery) was $V_{DS} = -25mV$ in order to enforce the linear operation.

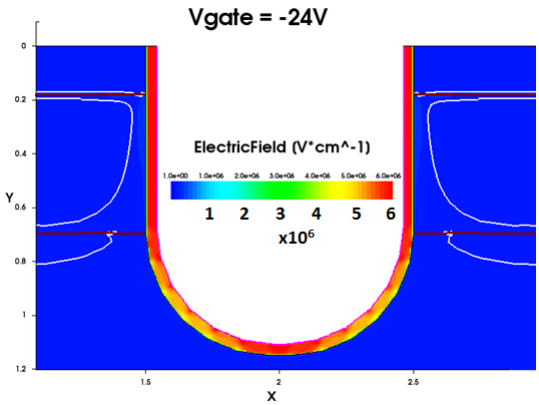

Figure 2.2: Electric field distribution along U-shape gate oxide in the case of the maximum stress condition V_G = -24V. The rounded shape prevents the creation of higher electric field in the proximity of corners.

The degradation due to NBTI was evaluated by mainly monitoring the threshold voltage shift. Different bias conditions are considered during the NBTI stress. In order to determine the gate voltage to apply, TCAD numerical simulations are performed, aiming at analyzing the electric field in the gate oxide. Because of the U-shape of the gate oxide, the uniformity of the electric field must be verified. In Fig. 2.2 a TCAD Sentaurus simulation [24] performed on a U-MOSFET structure is reported. In particular, by observing the electric field distribution in the gate oxide, it is possible to note as in the rounded region the maximum electric field is similar to the one in the channel region. Since NBTI degradation is generally performed for electric field values between 2 and 6 MV/cm [25], [26], having an oxide thickness of 40 nm, the following

gate voltages were adopted during the stress: -16, -20, and -24V.

As typically reported in [27] for CMOS technology, also in the case of U-MOSFETs the adopted method for evaluating the threshold voltage shift significantly affects the dynamics of the V_{TH} degradation. In fact, a partial recovery occurs because of the measurement delay, during which the gate-bias is removed or reduced at low voltage. To this purpose, three measurement techniques, namely I_DV_G-G_{MAX}, *Single Point* (SP), and *On The Fly* (OTF) were adopted in order to measure the threshold voltage. When these methods are used to estimate the V_{TH} shift during NBTI degradation, they differently affect the fast recovery mechanism occurring during the measurement phase.

It is worth noting that, during the discussions of the different methods, the word "*recovery*" is just referred to the fast recovery mechanism occurring during the I_D measurement phases when the gate stress is removed or reduced.

Besides the considered method, an I_DV_G measurement is required in fresh devices in order to estimate the trans-conductance (g_m) and the threshold voltage ($V_{TH-FRESH}$).

In the first method (I_DV_G-G_{MAX}), the threshold voltage was evaluated my means of maximum trans-conductance method [28]. NBTI was applied by biasing a constant gate voltage and the stress was periodically interrupted in order to monitor the threshold voltage shift by measuring a full I_DV_G transfer characteristic. The time delay, introduced by the measurement setup, occurring between the end of stress (removal gate bias) and the end of V_{TH} measurement, was about 3 seconds. This method is widely used because it gives the possibility to monitor the V_{TH}, R_{ON} (mobility) and the subthreshold slope degradations. On the other hand, the V_{TH} shift is estimated by considering the I_DV_G transfer characteristic at V_G values larger than V_{TH} and hence it may be affected by mobility degradation.

In *Single Point* method, during the periodic interruption of the stress, the gate bias was reduced to $V_G \approx V_{TH}$ in order to minimize the recovery process [29], [30]. The V_{TH} shift was estimated through the evaluation of ΔI_D for different stress times at $V_G \approx V_{TH}$ and $V_{DS} = -25mV$. The time delay in this case was 29 ms, since a single drain current value was measured. The benefit of this method is due to the non-total removal of the stress voltage, which allows to reduce the amount of recovery occurring during measurement phase, compared to the I_DV_G-G_{MAX} case. In addition, the shorter measurement time allows to evaluate the V_{TH} shift with lower recovery. On the other hand, it is not possible to monitor the degradations of other electrical parameters since a single drain current value is measured.

Finally, in OTF method, the stress was not suspended at all, in order to completely avoid the recovery process, and the drain current was periodically monitored for $V_G = V_{STRESS}$ [31]. Since the gate bias was not removed for monitoring ΔI_D, a series of repeated measurements were performed during the stress. As a result, the standard uncertainty of measurement was estimated.

By considering a Gaussian distribution, the error bar ($\pm$ 3 μ) guarantees a 99.7 % confidence interval. For the other methods, single measurements were considered since the repeated removal or reduction of the stress voltage would lead to a repeated fast recovery and hence to a non-correct evaluation of the NBTI induced degradation.

In the case of OTF method the V_{TH} shift was calculated as:

$$\Delta V_{TH} = -\frac{\Delta I_D}{g_m} \tag{2.1}$$

where g_m is the trans-conductance for V_G equal to the stress voltage in fresh device. The accuracy of this method is in general affected by the mobility/on-resistance degradation. In addition, the carrier mobility and subthreshold slope degradation cannot be evaluated.

The threshold voltages shift occurring during NBTI stress, evaluated according to the different measurement techniques are reported in Fig. 2.3.

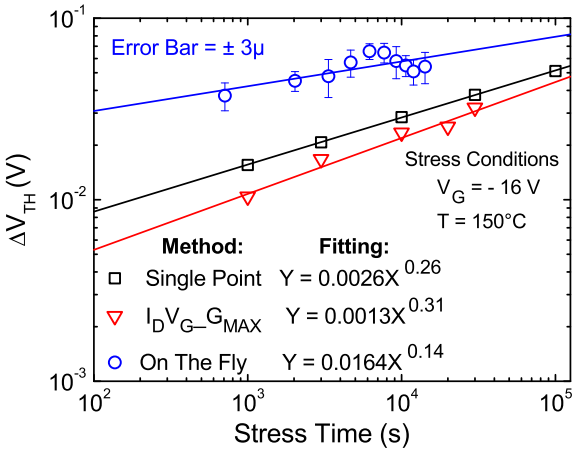

Figure 2.3: V_{TH} degradations, due to NBTI stress, evaluated with different techniques. The following stress conditions were considered: V_G = -16 V, V_{DS} = 0 V and T = 150 °C. During the measurement phases, V_{DS} = -25 mV was applied in order to guarantee the operation in linear region.

It is worth noting that for each stress condition a single device has been stressed. Therefore, the results reported from here on, are representative of a single device.

The observed degradation is function of the method adopted for the V_{TH} measurement, suggesting that when the gate-bias stress is suspended, a fast-partial degradation recovery occurs. In the case of OTF method, the gate-bias stress is not removed at all, hence no recovery occurs and the largest V_{TH} shift is observed. On the other hand, in the case of I_DV_G-G_{MAX} method, the gate voltage is reduced down to 0 during the measurement phase and a relatively

long time delay (about 3 seconds) is required. This leads to a higher recovery and thus to a lower V_{TH} shift. Intermediate values are observed in the case of *Single Point* method, since, during the V_{TH} measurement, the reduction of V_G to an intermediate value (close to V_{TH}) and an intermediate time delay (29 ms) is required. It may also notice that the results of the three methods tend to converge as the total stress time increases. The hypothesis of recovery during the V_{TH} measurement is supported by Fig. 2.4, in which the V_{TH} recovery is monitored for 2 s and is in qualitative agreement with the results reported in [32], [33] for p-CMOS technology. It is worth noting that a fast recovery of the threshold voltage happens for $t < 1s$. The delay of 29 ms, reported in Fig. 2.4, is due to the limited speed of the experimental setup. However, according to the large V_{TH} shift observed in Fig. 2.3 for the OTF method, a further V_{TH} increase could be expected in Fig. 2.4 for t < 29 ms.

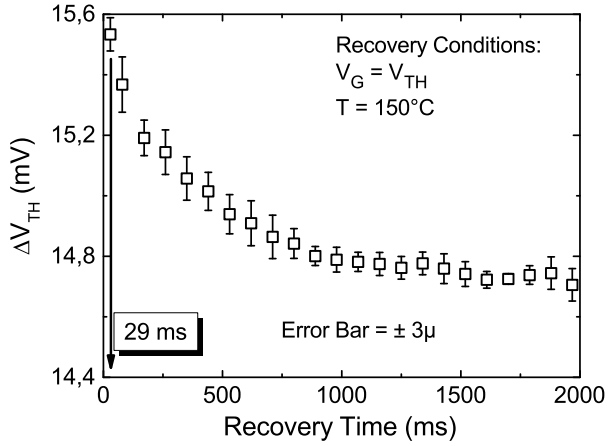

Figure 2.4: Threshold voltage recovery, evaluated by means of single point method, after 1000 s of stress with V_G = -16 V and T = 150 °C. During the recovery phase, the gate bias was chosen close to V_{TH}. The first measurement time (29 ms) is related to the limitations of the measurement setup. Other points are an average over a fixed time window, and μ is the uncertainty.

In the remainder of this chapter the analysis will be focused on I_DV_G-G_{MAX} method. Although a larger recovery occurs during V_{TH} measurement, the acquisition of a complete I_DV_G transfer characteristic allows to evaluate other relevant electrical quantities, such as trans-conductance and subthreshold slope. These further parameters can be useful in order to better understand the dynamics of interface states generation during the NBTI.

It is worth noting that from here on the word "recovery" will be considered as the recovery phenomenon occurring from the end of stress when no biases are applied on the device terminals.

2.4 Results and Discussion

In Fig. 2.5 the threshold voltage shifts for different stress conditions (V_{G_S}) are shown. By increasing the stress voltage, a translation of ΔV_{TH} curves is observed, whereas the time exponent seems to be not affected by the stress condition. This is in agreement with other studies reported in the literature, asserting that the time power-law slope (time exponent n) is technology dependent and typically ranges from 0.15 to 0.3 [26], [34]. Moreover, this wide range of n has been also attributed, by different groups, to measurement delay [30], [35], [36]. Indeed, in the previous section, it has been shown that adopting different techniques for threshold voltage evaluation, and thus reducing the measurement delay, the time power-law slope decreases from 0.31 to 0.14, confirming that higher measurement delay results in lower ΔV_{TH} and higher n.

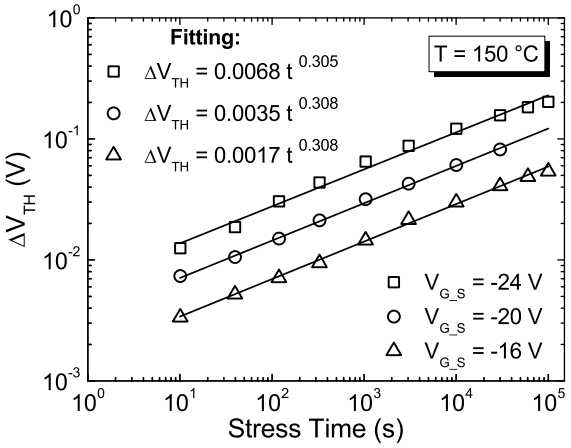

Figure 2.5: Threshold voltage shift versus NBTI stress time for different stress conditions.

However, by deeply analyzing the dependence of V_{TH} degradation on the gate-bias stress as reported by Fig. 2.6, it is possible to note the existence of different degradation dynamics of V_{TH}. For relatively large gate voltage (V_G = -24 V and $E_{OX} \approx 6$ MV/cm), see Fig. 2.6a, V_{TH} starts increasing rapidly and then the slope reduces at larger stress time, in qualitative agreement with the results reported in [37] for p-channel power VD-MOSFETs, where this reduction of slope is attributed to the time dependence of interface states generation. For V_G = -16 V ($E_{OX} \approx 4$ MV/cm), see Fig. 2.6b, a single slope is found for the whole range of stress time, likely because in this case bulk charge trapping represents the dominant degradation mechanism and thus the ΔN_{it} is negligible respect to ΔN_{OT}.

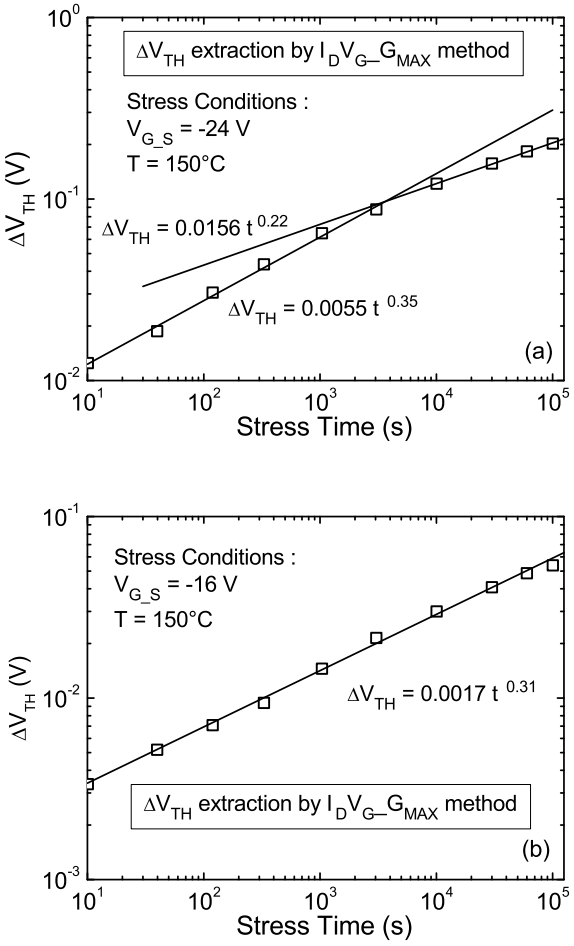

Figure 2.6: ΔV_{TH} vs. stress time due to NBTI degradation. Two different stress conditions are applied: V_G = -24 V (a) and V_G = -16 V (b). The threshold voltage is evaluated by means of $I_D V_G$-G_{MAX} method. Different stress dynamics, due to interface states generation, are observed. Dual slope is attributed to ΔN_{it}, which is dependent on the gate-bias stress.

In Fig. 2.7 the subthreshold slopes for different stress times are reported for the case V_{G_S} = -24 V. A faster increase of SS is observed in the initial stress time (from 0 s to 10^4 s of stress), with respect to the second phase (from 10^4 s to 10^5 s). This points out a higher N_{it} generation in early phase and it is in agreement with the results of Fig. 2.6a, hence confirming the previous observation regarding the dual slope over the stress time. As a matter of fact, in Fig. 2.8 it is possible to note the mobility degradation which is typically ascribed to the interface states generation as in the case of subthreshold slope increase.

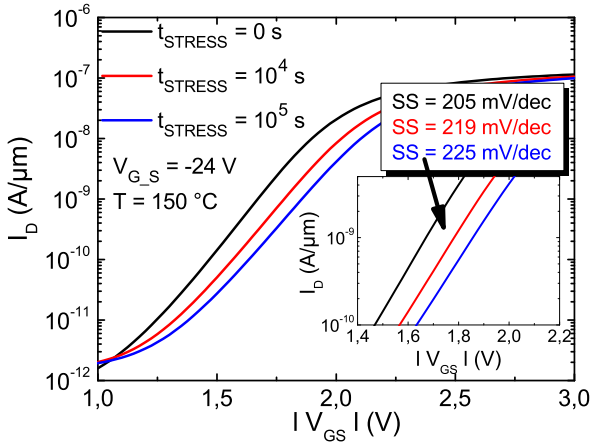

Figure 2.7: $I_D V_{GS}$ curves as a function of the stress time with V_G = -24 V and T = 150 °C. The subthreshold slope SS is reported in the inset. An increase of SS is observed after the stress.

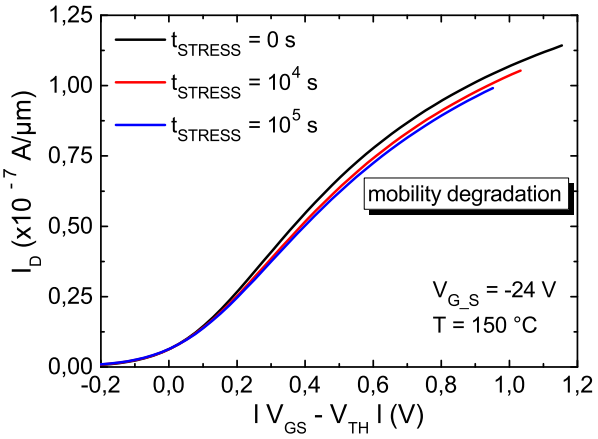

Figure 2.8: Drain current curves in fresh, during and after NBTI stress. A transconductance/mobility degradation linked to the interface trapping mechanisms is observed.

In Fig. 2.9a it is possible to observe a degradation of threshold voltage when the device is stressed at relatively low gate voltage (-16 V). It is believed that, for this specific stress condition, the observed degradation is mainly due to trapping/de-trapping of oxide charge (N_{OT}). As a matter of fact, in Fig. 2.9b there is not significant mobility degradation which is caused by the interface states generation. According to the results reported in Fig. 2.7, 2.8 and 2.9, the interface states generation mechanism seems to be strongly dependent on

gate-bias level during the stress.

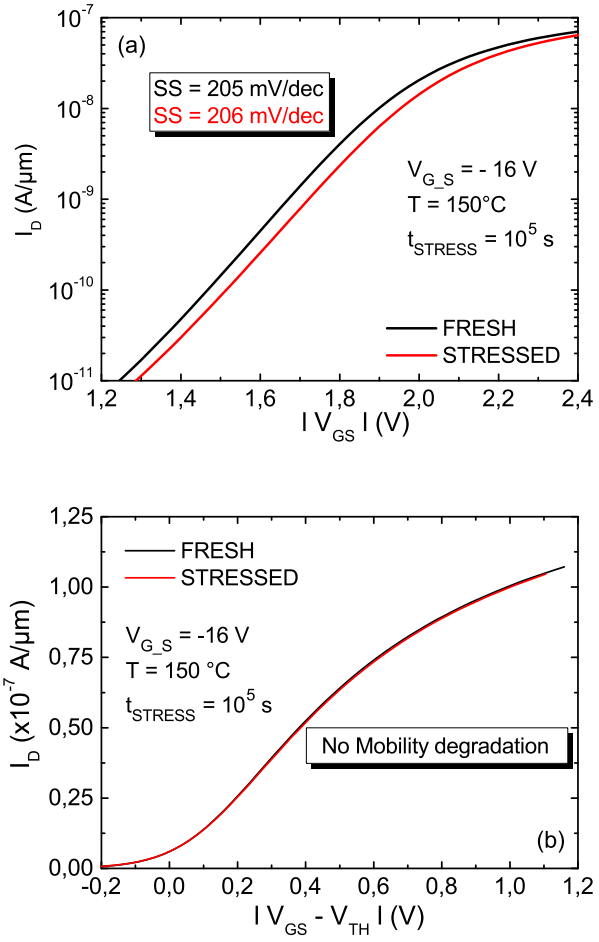

Figure 2.9: Drain current curves in fresh and stressed devices, in logarithmic (a) and linear scale (b). A degradation of V_{TH} is observed (a), whereas no mobility degradation (interface states generation) is shown (b).

Recovery phase, occurred after the stress with V_G = -24 V, is observable in Fig. 2.10. From this figure, it observed that: i) the shift detected during the stress phase (Fig. 2.6a) cannot be considered as a permanent degradation since after the removal of the gate voltage a recovery phase occurs (Fig. 2.10); ii) despite several hours of recovery ($\approx$ 22 hours at T = 150 °C) V_{TH} is not completely recovered, meaning that a very slow recovery mechanism is involved; iii) this recovery is mainly due to de-trapping of charge from the bulk oxide. The latter statement can be demonstrated by analyzing the interface trap density recovery, shown in Fig. 2.11, in the case of V_G = 0 V and temperature of 150 °C.

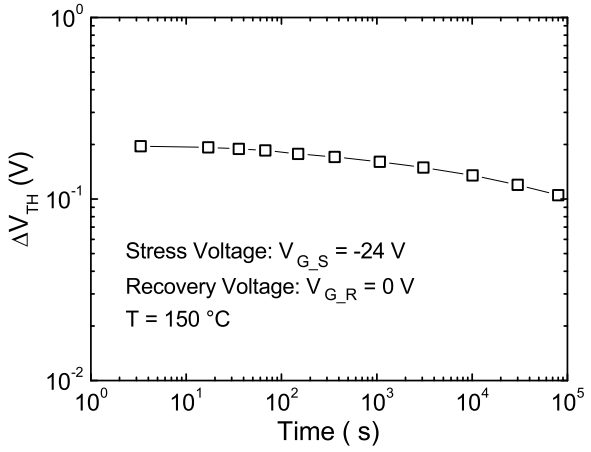

Figure 2.10: Threshold voltage shift during recovery after the stress with V_G = -24 V. A partial and slowly recovery mechanism is observed.

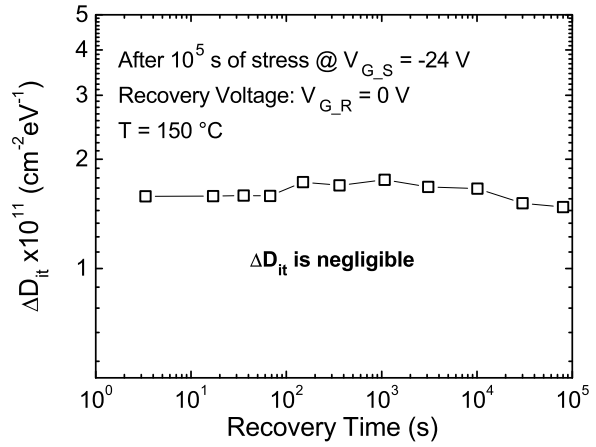

Figure 2.11: Interface trap density shift versus recovery time. The ΔD_{it}, extracted from sub-threshold slope shift, seems to be constant during the recovery phase. As a result, permanent interface states have been generated at the silicon/oxide interface.

The ΔD_{it} has been calculated with the following model proposed by Schroder in [28]:

$$\Delta D_{it} = \frac{C_{OX}(S_{after} - S_{before})}{ln(10)qkT} \tag{2.2}$$

where C_{OX} is the oxide capacitance per unit of area, S is the sub-threshold slope, q is the elementary electron charge, k is the Boltzmann constant and T is the temperature in kelvin. From Fig. 2.11, it is possible to observe that,

although a significant increase of interface state density is detected after the stress, there are not changes of ΔD_{it} during the recovery phase. Hence it is possible to conclude that: i) they contribute to a permanent component (defects not recovered for the considered recovery conditions); ii) the amount of recovery detectable from threshold voltage shift (Fig. 2.10) can be mainly ascribed to charge de-trapping from bulk oxide defects. These statements are strengthened by [13], [38], in which it has been asserted that interface traps contribute to a permanent component due to very small and slow re-passivation phenomenon.

The analysis of NBTI at different stress voltages allows to estimate the lifetime of the U-MOSFETs at the temperature of 150 °C, as reported in Fig. 2.12. Although such a large temperature represents an accelerated degradation condition, the operating temperature of power MOSFETs can be significantly high due to self-heating effects [39]. Considering as failure criterion the threshold voltage shift of 100 mV in a time of 1000 hours, the maximum applicable gate voltages, at the temperature of 150°C, is -16.1 V.

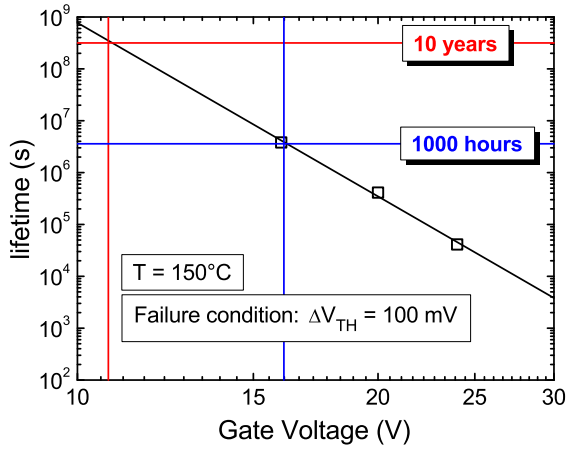

Figure 2.12: Lifetime extrapolation. The failure criterion is considered as the threshold voltage shift of 100 mV in 10 years or 1000 hours at the temperature of 150°C.

In addition to the performed analysis, the role of the temperature on NBTI degradation has been also investigated by stressing the devices at different temperatures. Fig. 2.13 shows the shift of the threshold voltage, monitored after $3 \cdot 10^4$ s of stress with a gate bias of -24 V, as a function of the temperature. The threshold voltage is estimated at the end of the stress in order to minimize the partial recovery occurring when the gate voltage is removed or reduced for the V_{TH} estimation. In Fig. 2.13 and 2.14 it is possible to observe as the V_{TH} degradation and the interface state generation increase with the temperature confirming that it is an accelerator factor for the NBTI mechanism [23].

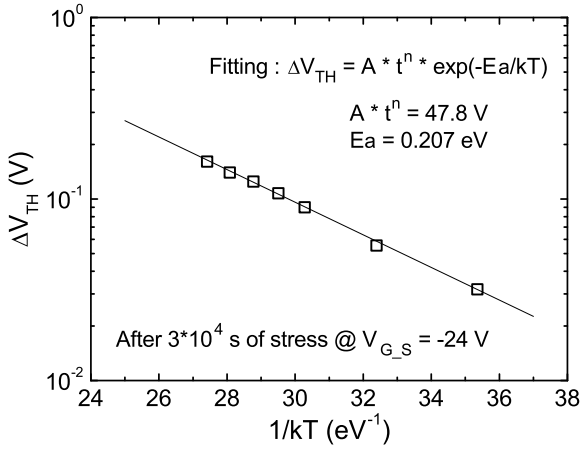

Figure 2.13: Arrhenius plot. The V_{TH} shift has been calculated by means of maximum trans-conductance method applied on an $I_D V_G$ transfer characteristic performed at the end of stress ($3 \cdot 10^4$ s).

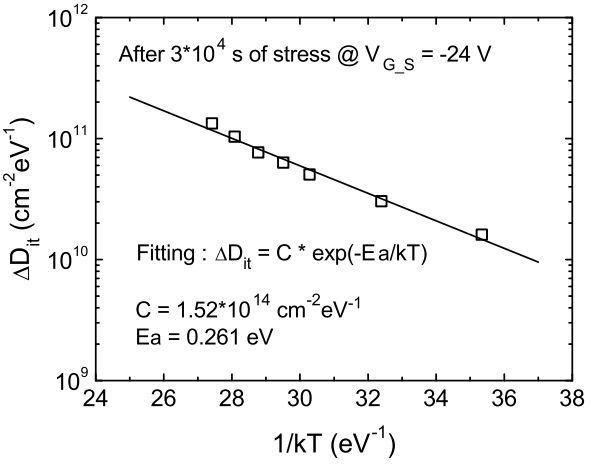

Figure 2.14: Arrhenius plot for interface trap density shift (ΔD_{it}) extracted at the end of NBTI. The activation energy differs from that in Fig. 2.13 since different physical mechanism occurs during NBTI stress.

In particular, by considering the Arrhenius plot of Fig. 2.13 and 2.14, an activation energy of 0.207 eV and 0.261 eV was estimated, respectively. It is worth noting that these values must be considered as effective values and are function of the considered stress conditions [13]. In particular, by considering the temperature of 150 °C and the stress time of $3 \cdot 10^4$ s, similar value of $\approx$ 0.2 eV is reported in [13] in the case of interface states. The difference between the activation energy, extracted in the case of V_{TH} and D_{it} Arrhenius plot, is ascribed to the different physical mechanisms affecting the two parameters

during NBTI stress [13]. Moreover, it is worth noting that the activation energy extracted from ΔV_{TH} is the result of the combined effect of oxide and interface trapped charge.

In Fig. 2.15, the threshold voltage recovery at different temperatures is shown. Since the stress and recovery phase are carried out at the same temperature, the initial value of ΔV_{TH} increases as long as the temperature rises (as already discussed in Fig. 2.13). Moreover, in Fig. 2.15 it can be observed that by increasing the temperature a faster recovery of V_{TH} occurs, meaning that, as reported also in the case of CMOS technology [40]-[42], the temperature is an acceleration factor also for the recovery mechanism.

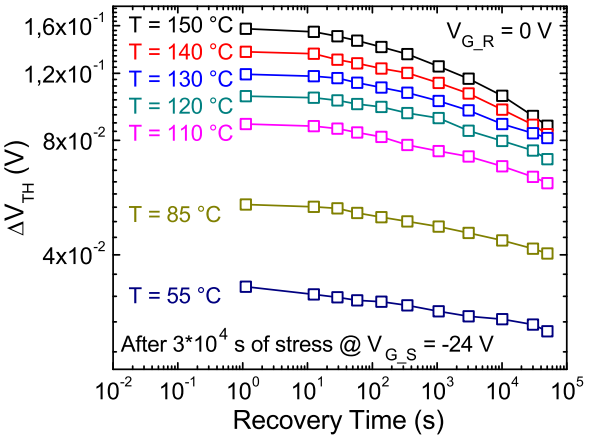

Figure 2.15: Threshold voltage recovery for different temperatures after $3 \cdot 10^4$ s of stress at V_G = -24 V. The same temperature is adopted during the stress and recovery phases. By increasing the temperature a faster recovery occurs, meaning that the temperature is an accelerator factor also for de-trapping mechanism.

Recovery dynamics, analyzed for different recovery gate voltages (V_{G_R}), are shown in Fig. 2.16. As it is possible to note, the recovery phase is V_{G_R} dependent. In particular, we observe that: i) in the case of V_{G_R} = -2.25 V ($V_{G\_R} \approx V_{TH}$ after stress) the V_{TH} recovery is negligible; ii) decreasing $|V_{G\_R}|$, hence moving from V_{TH} to the flat band voltage (V_{FB}), a larger recovery occurs; iii) for V_{G_R} ranging from -0.25 V to 0 V no additional recovery is observed. The gate voltage dependence is explained by the energy distribution of traps. In fact, traps having energy above the channel potential (Fermi level at SiO_2/Si interface) are filled with holes and are not discharged during recovery phase. On the other hand, traps below the channel potential are discharged, leading to a recovery of V_{TH}.

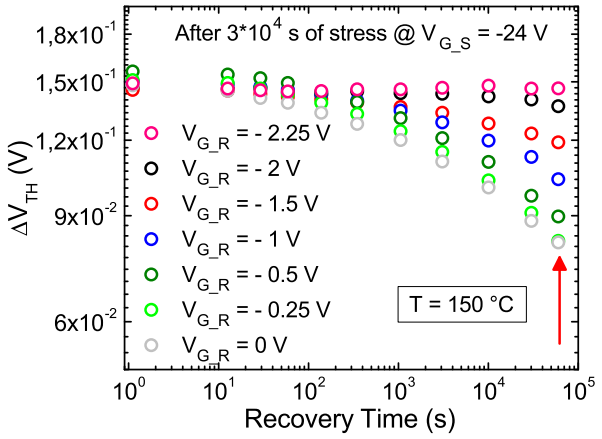

Figure 2.16: V_{TH} recovery for different recovery biases. With V_{G_R} = -2.25 V a negligible recovery is shown; moving the gate bias down to -0.25 V a larger recovery occurs. A further decrease of the gate voltage does not lead to additional recovery. Therefore, the traps involved in the recovery have an energy confined within the band-gap of the silicon.

Therefore, TCAD numerical simulations, aimed at evaluating the channel potential (Fermi level) and hence the oxide traps level, were implemented [24]. A calibration of the simulated structure was performed in order to reproduce the characteristics of the real device. The flat band voltage, due to gate doping and to the existing defects in fresh conditions, was taken into account by properly setting the work function difference between gate electrode and the semiconductor. Moreover, since the channel potential depends on the trapped charge density (ΔN_{OT}) after the stress phase, ΔN_{OT} was estimated by considering the experimental threshold voltage shift (ΔV_{TH}) as:

$$\Delta N_{OT} = \frac{C_{OX} \Delta V_{TH}}{q} \tag{2.3}$$

where C_{OX} and q are the oxide capacitance for unit of area and the elementary charge, respectively. Finally, the value calculated with Eq. 2.3 was accounted for in the simulation.

The calculated band diagrams corresponding to the border conditions, i.e. start and end of recovery phase with V_{G_R} = -2.25 V and -0.25 V, respectively, at T = 150 °C, are reported in Fig. 2.17 and 2.18, respectively. According to the discussion of Fig. 2.16, it can be asserted that the oxide traps involved in the recovery mechanism have an energy confined between 0.22 eV and 0.84 eV from silicon valence band.

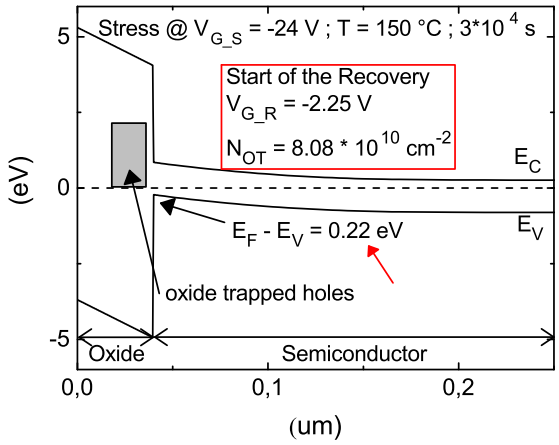

Figure 2.17: Band diagram at the start of recovery with an applied gate voltage of -2.25 V and a trap density, calculated with Eq. 2.3, of $8.08 \cdot 10^{10}$ cm^{-2}. With this gate bias all the charge, trapped during the stress, stays trapped into the oxide.

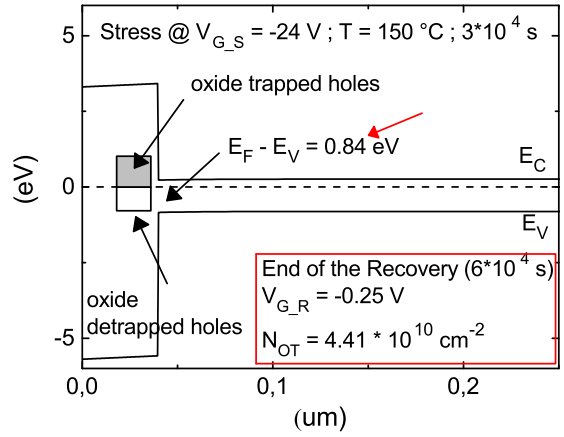

Figure 2.18: Band diagram at the end of recovery ($6 \cdot 10^4$ s) with an applied gate voltage of -0.25 V and a trap density, calculated with Eq. 2.3, of $4.41 \cdot 10^{10}$ cm^{-2}. Traps with an energy level between 0.22 and 0.84 eV from silicon valence band have been involved in the de-trapping process.

By combining the energy levels extracted with numerical simulations and the experimental ΔN_{OT} values calculated with Eq. 2.3, the energy distribution of the oxide charge de-trapping are reported in Fig. 2.19 and 2.20. Decreasing $|V_{G\_R}|$, hence moving from V_{TH} to V_{FB}, a higher number of filled oxide traps located down below the Fermi level and a larger de-trapping charge occurs till V_{G_R} reaches – 0.025 V ($E_F - E_V = 0.84eV$) (Fig. 2.19). Moreover, a large

part of these traps seems to be positioned close to conduction and valence band of the semiconductor at the Si/SiO_2 interface, since, from Fig. 2.20, it is possible to observe that the de-trapping charge concentration is higher compared to that occurring at the mid bandgap.

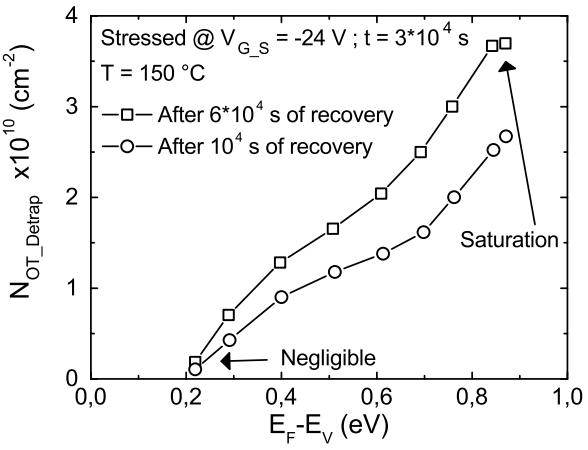

Figure 2.19: De-trapped oxide charge versus energy level after 10^4 s and at the end of the recovery phase. A saturation of the charge de-trapping at 0.84 eV from VB occurs, meaning that during the stress all the traps with higher energy have been filled.

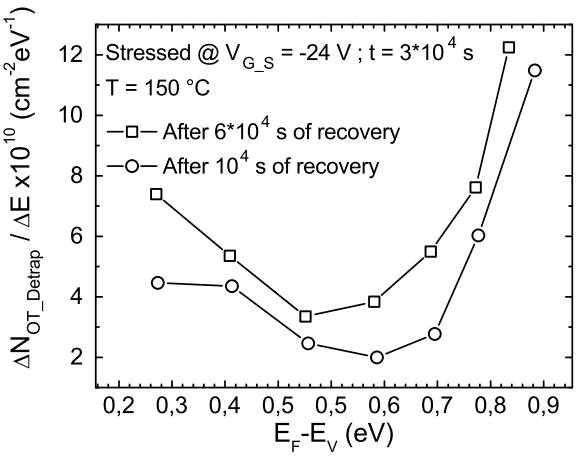

Figure 2.20: De-trapped oxide charge density variation versus energy level. Higher de-trapping charge variation occurs near the valence and conduction band with respect to mid-gap of the silicon.

The oxide trap depth was estimated by using the tunneling time constant model. By considering a small oxide field, oxide charge can escape via a

trapezoidal barrier tunneling and, by assuming a single trap energy (E_T), the de-trapping time is given by [43]-[46]

$$\tau = \tau_0 \cdot exp\left(2 \cdot \sqrt{\frac{2 \cdot m^* \cdot E_T}{\hbar^2}} \cdot x\right) \tag{2.4}$$

where τ_0, m^*, E_T, $\hbar^2$, and x are the time constant, charge tunneling effective mass, trap energy level from SiO_2 valence band, Dirac constant, and distance of the trap from the Si/SiO_2 interface, respectively.

In order to calculate the oxide trap distance (x) from SiO_2/Si interface, the experimental dynamics of V_{TH} recovery, shown in Fig. 2.21, has been modeled as the superposition of four first-order transients:

$$\Delta V_{TH} = A \cdot exp\left(-\frac{t}{\tau_1}\right) + B \cdot exp\left(-\frac{t}{\tau_2}\right) + C \cdot exp\left(-\frac{t}{\tau_3}\right) + D \cdot exp\left(-\frac{t}{\tau_4}\right) \tag{2.5}$$

with fitting parameters A, B, C, D = 8.09, 18.78, 25, 97.3 mV and τ_1, τ_2, τ_3, τ_4 = 18, 340, 6500, 320000 seconds, respectively.

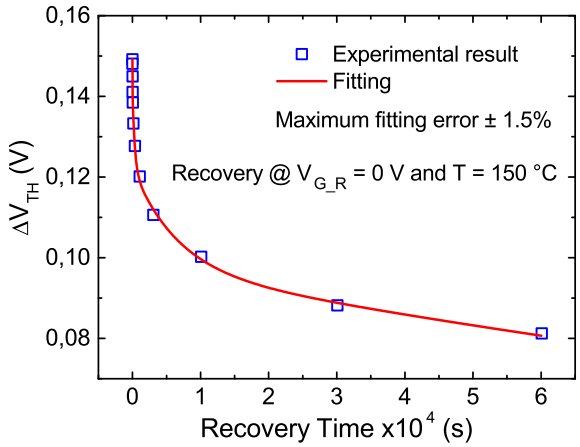

Figure 2.21: Experimental (markers) and modeled (line), with (3), threshold voltage shift versus recovery time for V_G = 0 V and T = 150 °C.

The different de-trapping time constants suggest different depths of the oxide traps. By considering the lowest and the highest time constant in the energy range of (0.22 - 0.84) eV, the possible physical locations of the traps, extracted with Eq. 2.4 are determined and reported in Fig. 2.22. As a result, we found a range of (2.24 - 3.04) nm distant from SiO_2/Si interface, which is in agreement with [47] asserting that oxide traps are located within 6 nm from SiO_2/Si interface.

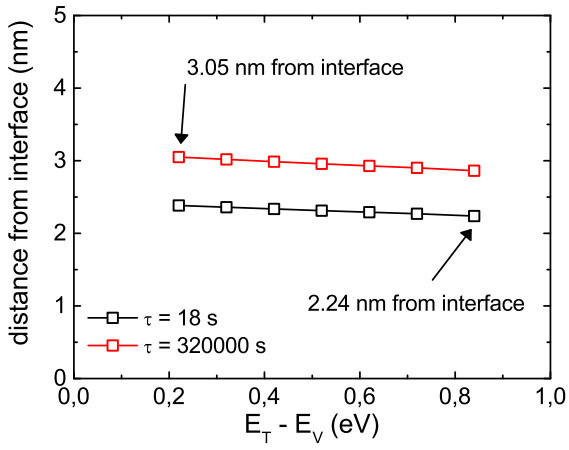

Figure 2.22: Distance of the oxide traps from silicon/oxide interface versus trap energy level. Considering the lowest and the highest de-trapping time constant a physical location between 2.24 and 3.05 nm has been estimated.

2.5 Conclusions

In this chapter the effects of degradation induced by Negative Bias Temperature Instability in p-channel Si-based power U-MOSFETs have been investigated.

In the experimental study, different methods for evaluating the threshold voltage shift have been adopted in order to underline the fast recovery occurring when gate-bias stress is reduced or removed. It has been shown that the adopted method significantly affects the dynamics of threshold voltage degradation, because of the different gate and time delay conditions implemented during the V_{TH} measurements.

A preliminary analysis, by means of TCAD simulator, has allowed to establish that, thanks to rounded shape of the gate, the electric field is rather uniform in the whole oxide structure, then both stress and recovery phases have been analyzed in order to understand which physical mechanism is responsible for the NBTI degradation.

Concerning the influence of gate voltage level during the stress, with V_G = -16 V an uniform dynamic of stress is found, since the V_{TH} shift is dominated by oxide charge trapping rather than interface states generation. On the other hand, for V_G = -24 V, both oxide charge trapping and interface state generation occur, causing a degradation of threshold voltage and sub-threshold slope. Moreover, the higher and faster interface states generation cause different dynamics of stress (change of slope).

Regarding the recovery mechanism, it is mainly dominated by charge de-trapping from bulk oxide defects, since the interface state recovery turns out to be negligible for the whole considered recovery time. Consequently,

a combined measurement/simulation methodology has been implemented in order to evaluate the spatial and energy oxide trap distribution.

In particular, by performing an experimental study on the recovery mechanisms at different bias conditions, it has been found that the oxide traps involved during NBTI stress have an energy confined in the silicon bandgap. Afterwards, by accounting for the experimental results in TCAD simulations, an oxide trap distribution with an energy level confined between 0.22 eV and 0.84 eV from silicon valence band has been estimated.

Finally, by adopting the tunneling constant model, it has been calculated that the distance of oxide traps from SiO_2/Si interface may range between 2.24 and 3.04 nm.

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Chapter 3

Modeling Self-Heating Effects in GaN-based HEMTs

3.1 Introduction and State of the Art

GaN-based transistors, as largely introduced in chapter 1, thanks to the intrinsic properties of the adopted materials, represent today a potential technology for switching power applications [1]-[3]. However, high performance is not enough, as a high level of reliability must be guaranteed under heavy-duty operation. For this reason, different works about heterostructures reliability have been focused on the charges trapping/de-trapping mechanisms [4]-[7].

However, since a power transistor is subject to high temperatures during its normal operation, self-heating effects play an important role in the understanding of the device performance limitations.

Several studies reported in the literature [8]-[13] have pointed out as the contribution of the thermal boundary resistance (TBR), introduced by the transition layer (or nucleation layer) between GaN-buffer and Si- or SiC-substrate in order to reduce the lattice constants mismatch, is fundamental for modeling the self-heating effects in the devices. Indeed, Sarua et al. [9] have experimentally proposed a model, based on GaN-on-SiC devices, able to describe the temperature dependence of the TBR emphasizing how its contribution becomes more and more important with the temperature increase. A similar study has been performed by Schwitter et al. [8] for AlGaN/GaN devices grown on silicon substrate.

In this chapter, a simulation study of self-heating effects has been performed in order to understand the performance limitations, under both static and dynamic operation modes. To this purpose, a physical model able to account for the realistic temperature dependence of the equivalent thermal boundary resistance ascribed to transition layer, has been implemented for both GaN-on-SiC and GaN-on-Si technologies.

3.2 Thermal Model Implementation

By considering for each material involved in the transition layer the simulator's default models for the thermal conductivity, the total transition layer thermal resistance results underestimated because its temperature-dependence and the interface impact between two different materials are not accounted for. In particular, in the case of Sentaurus TCAD the thermal conductivity of some materials, such as those AlN-based, is still reproduced as a temperature-independent constant [14]. Moreover, since materials with significant lattice mismatch and difference in thermal expansion coefficients are adopted, the impact of the interfacial thermal resistance could be dominant with respect to that of the bulk material or, at least, contributes to increase the total thermal resistance value.

Therefore, a specific Physical Model Interface (PMI) has been implemented, by means of C++ subroutines, in TCAD Sentaurus simulator in order to properly set the thermal boundary resistance (TBR) between GaN channel (layer) and substrate. This model is self-consistently solved with the Drift Diffusion model.

According to literature results based on an experimental characterization [8], [9], the implemented temperature-dependent thermal conductivity (k(T)) of the transition layer is modeled as:

$$k(T) = k_0 \cdot \left(\frac{T}{T_0}\right)^{\alpha} \tag{3.1}$$

where k_0 is the thermal conductivity at $T_0 = 300K$ and α is the power law coefficient. Both depend on the kind of substrate (Si or SiC in this work) and thus on the types of materials and their respective thickness adopted for the transition layer. Therefore, their values will be specified further in the following sections.

3.3 GaN-on-SiC Structure

3.3.1 Device Structure and Physical Models

Fig. 3.1 shows the simulated AlGaN/GaN structure. It was defined considering typical geometric characteristics and material parameters proposed in experimental works reported in the literature (e.g. [5]). The structure features a stack of $SiN/AlGaN/GaN/Oxide/SiC$ layers with thickness of $50nm/29nm/1.5\mu m/10nm/100\mu m$, respectively. The aluminum concentration in AlGaN barrier, which plays an important role in device operation through the piezoelectric charge induced by mechanical stress, is set to 35 %, representing a typical value for state-of-art devices [5]. Drain and source electrodes are modeled as ohmic contacts with length $L_S = L_D = 0.5\ \mu m$, whereas the 0.7

μm long gate electrode is modeled as a Schottky contact, with 1.1 eV barrier height, representing a typical measured value for realistic devices [15], [16]. The drain- and source-to channel access regions feature lengths of $L_{SG} = 0.7$ μm and $L_{GD} = 2$ μm, respectively. Finally, a device pitch (L_{DEV_PITCH}) of 4.4 μm was assumed.

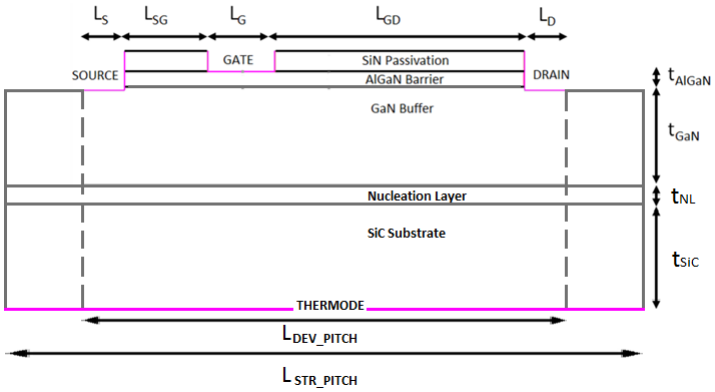

Figure 3.1: Simulated AlGaN/GaN HEMT structure. To allow a self-heating study, a thermode contact, fixed at the temperature of 300 K, is introduced at the bottom of the SiC substrate. Figure not in scale.

Donor-traps have been added at the SiN/AlGaN interface. Their introduction is important not only for studying the dispersion effects due to de-trapping/trapping phenomena, but also because the traps occupancy is required to set an adequate channel electrical conductivity, since the combined effect of the interface trapped- and polarization-charge is indispensable for filling the channel of electrons.

Moreover, since Meneghesso et al. [5] have shown that surface donor-traps are responsible for a drain current dispersion effect, a single trap energy level of 0.5 eV from valence band has been adopted in order to have a finite transient time, required by traps to respond to an external voltage signal, similar to that obtained in [5] during drain-lag measurements.

The device features an oxide nucleation layer that significantly affects self-heating effects due to motivations discussed in section 3.2. This effect has been modeled in [9] by defining an equivalent thermal boundary resistance (TBR) interposed between the GaN buffer and the SiC substrate. Sarua et al. [9] experimentally investigated the temperature dependence of the TBR in AlGaN/GaN devices proposing a model able to reproduce the experimental results. It is worth noting that, as discussed in section 1.4, the nucleation layer is not usually made of oxide. However, since the aim of this work was the study of its thermal behavior instead of the electrical one, the kind of the adopted material is not important once the thermal conductivity is properly calibrated.

In this study, Sarua's model has been implemented and included in the

simulation tool through the device simulator's model interface in order to realistically model self-heating effects. In particular, by referring to model reported in Eq. 3.1, $k_0 = 2.78$ W/m·K and $\alpha = -2.76$ have been adopted for modeling the temperature-dependent thermal conductivity of the overall transition/nucleation layer, whereas simulator's default models and parameters have been used for AlGaN, GaN and SiC layers [14].

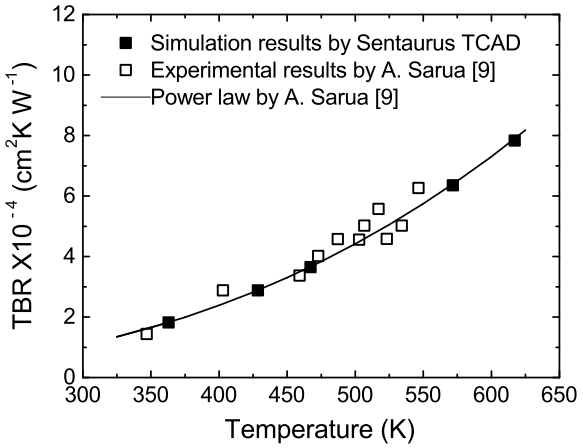

Figure 3.2: Calibration of the TBR by means of experimental results [9]. A PMI model has been implemented in the TCAD device simulator in order to account for the temperature dependence of the thermal conductivity.

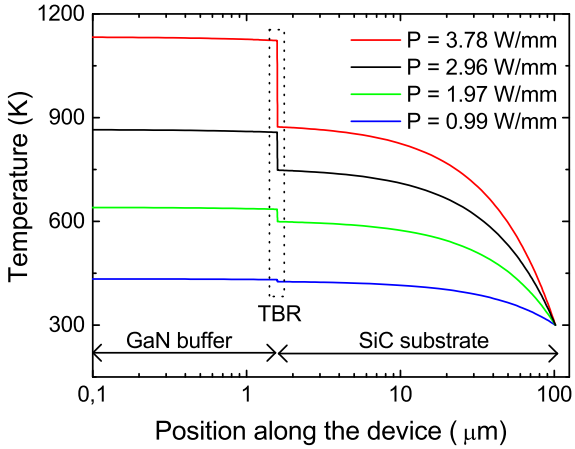

Figure 3.3: Thermal distribution along the device (vertical direction) for different electric powers. By increasing the temperature, the thermal boundary resistance (TBR) contribution plays an important role in the temperature behavior of device.

The implementation of the model for the thermal conductivity of the nucleation layer is validated in Fig. 3.2 by comparison with the experimental data for TBR reported by Sarua et al. in [9] and with the empirical power law proposed in the same paper. By considering Fig. 3.3, it is worth noting how the TBR becomes more and more important as the power dissipation increases, emphasizing the importance of the developed model for a realistic simulation.

3.3.2 Simulation Results and Discussion

In order to analyze the effect of mutual heating among adjacent devices, structures with different pitch (L_{STR_PITCH}) have been simulated.

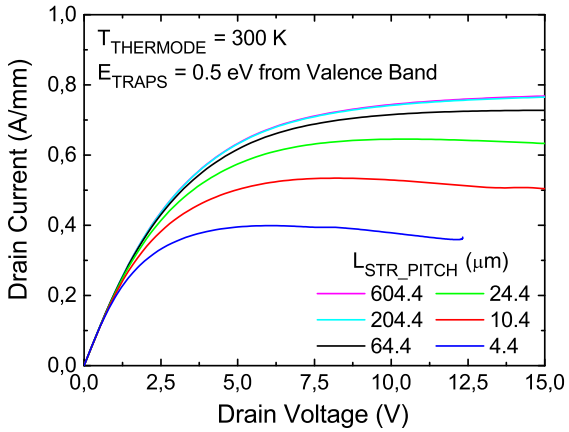

Figure 3.4: Simulated static I_DV_D characteristics evaluated on devices with different pitch. By increasing the pitch, the current increases because of the lower power density, leading to a reduction of the temperature in the channel and hence to an improvement of electron mobility.

Fig. 3.4 shows the simulated static I_DV_D characteristics for structures featuring different L_{STR_PITCH} values. By increasing L_{STR_PITCH}, the mutual heating effect is reduced and a lower power density is dissipated. As result a higher drain current is found.

In fact, according to Fig. 3.5, a channel temperature of 640 K and 335 K is found in the case of structure pitch of 4.4 μm and 604.4 μm, respectively, leading to a corresponding electron mobility, averaged along the channel, of 525 and 900 $cm^2V^{-1}s^{-1}$, respectively.

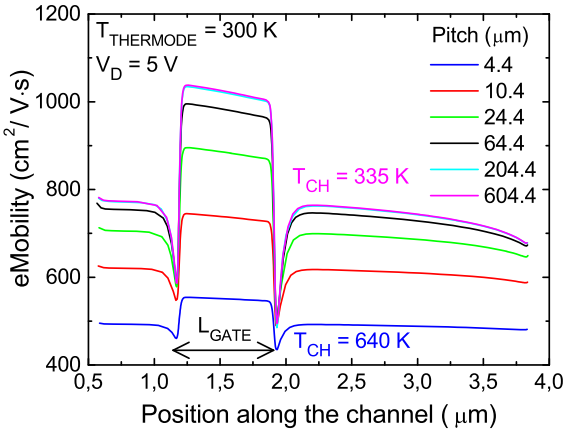

Figure 3.5: Electron mobility along the channel for structures featuring different pitch. By increasing the pitch, the electron mobility increases because of the lower channel temperature, leading to an increase of the drain current (Fig. 3.4).

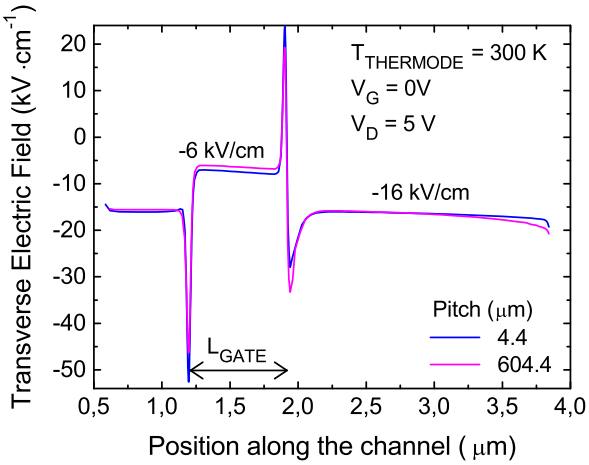

Figure 3.6: Transverse electric field distribution along the channel. The different electric field values are ascribed to absence of surface donor-like traps under the gate contact where the SiN passivation is absent. To this purpose, a different channel electron mobility is observed (Fig. 3.5).

The change of the electron mobility with respect to channel position is ascribed to the electric field variation. This can be attributed to the absence of surface donor-like traps under the gate contact where the SiN passivation is absent. Transverse electric field distribution is shown in Fig. 3.6 for structure pitch equal to 4.4 and 604 μm. It is possible to observe how it reaches about 6 kV/cm and 16 kV/cm in the region under the gate and in the drain-/source-to

channel access regions, respectively. These results are consistent with the significant decrease of electron mobility in AlGaN/GaN, for electric field larger than 5 kV/cm, reported in [17]. Therefore, the degradation of mobility along the channel can be ascribed to the large electric field values.

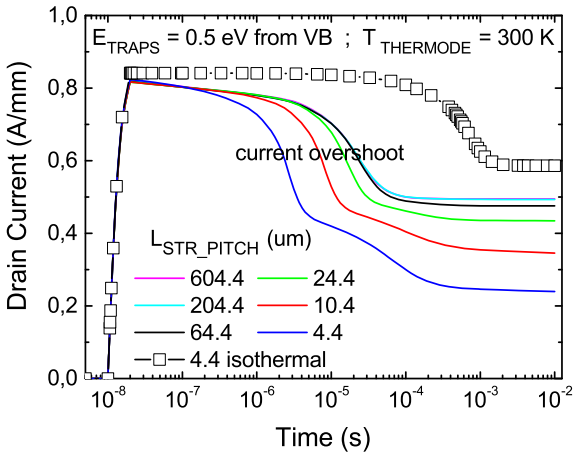

Figure 3.7: Drain-lag simulations for structures with different pitch. The current overshoot is linked to the transient of donor traps which is shorter but wider for higher temperatures.

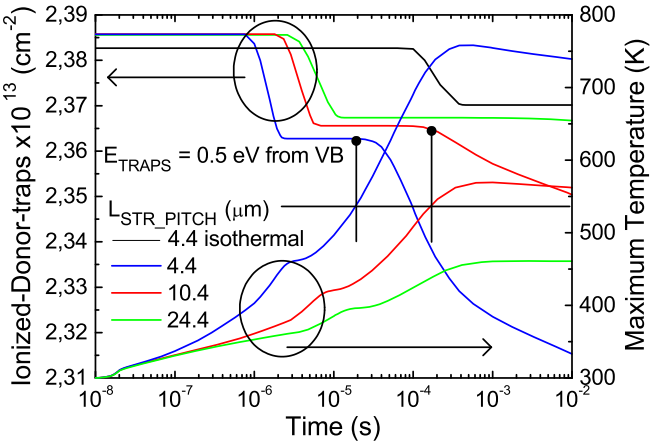

Figure 3.8: Ionized-donor-traps averaged over the whole SiN/AlGaN interface (left-axis), and maximum temperature in the channel (right-axis) as function of the time during drain-lag simulations (Fig. 3.7). While a single traps transient appears in the case of isothermal simulations, a second one is activated if, due to self-heating, the temperature exceeds approximately 540 K.

The dynamic behavior during drain-lag simulations for V_D switched between

0 and 10 V in 10 ns at $V_G = 0$ V is reported in Fig. 3.7 for structures with a different pitch. The amplitude of the drain voltage sweep has been chosen according with experimental and simulation works present in literature (e.g. [18]), whereas the ramp rate (1 V/ns) has been settled in order to have the trap transient starting after that drain voltage has reached the final level, allowing to monitor the whole traps transient. A drain current overshoot due to donor-traps transient is observable. Fig. 3.8 reports the time evolution of traps occupancy for devices with different pitch values. While a single transient appears in the case of isothermal simulations, a second one is activated if, due to self-heating, the temperature exceeds approximately 540 K. Indeed, for structure pitch larger than 10.4 μm the second transient does not occur (see also Fig. 3.7) since the increase of temperature, induced by self-heating, is limited. This suggests the presence of a trapping mechanism caused by two different source. The first one is electrical-related because noticeable also in the case of isothermal simulation (Fig. 3.7), whereas the second one is thermal-related (Fig. 3.8).

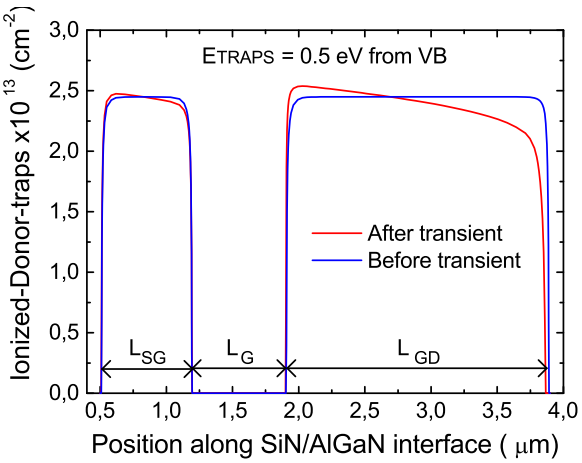

Figure 3.9: Traps occupancy along the SiN/AlGaN interface. Higher trapping/de-trapping phenomena are observed in the region close to the drain contact.

Finally, Fig. 3.9 reports the spatial dependence of trapping/de-trapping phenomena, suggesting that drain current dispersion effects, is mainly related to traps located in the region close to the drain contact. It is worth noting that the device structure does not have contact field-plates (see Fig. 3.1) and the surface donor-like traps under the gate contact are not considered since SiN passivation, in this region, is absent.

3.4 GaN-on-Si Structure

Similar analyses have been performed for GaN-on-Silicon devices. In particular, a 100 μm thick silicon substrate has been considered in order to model the self-heating effect during the transistor operation mode.

The device features a transition layer, composed of aluminum nitride (AlN) and different layers of AlGaN with different aluminum contents, significantly affecting the self-heating effects due to low thermal conductivity.

As in the case of GaN-on-SiC devices, this effect has been discussed and modeled, by means of experimental analysis reported in [8], in order to define an equivalent thermal boundary resistance (TBR) interposed between the GaN buffer and the Si substrate. As a result, the device simulator's model interface (PMI), implemented for devices with SiC substrate, has been optimized and calibrated for Si-substrate according to [8].

Unlike the case of GaN-on-SiC, where the PMI has been implemented only for the thermal resistance contribution of the transition layer, in the case of silicon substrate also the AlGaN barrier and GaN buffer contributions have been modeled by means of PMI because suggested in the experimental study of GaN-on-Si HEMT [8].

Model parameters for given temperature ranges are provided in Table 3.1.

$Material$	k_0 $(W/m \cdot K)$	α	$Temp.Range(K)$
GaN	150.0	-1.42	300-800
$AlGaN$	25.0	-1.44	300-500
TBR_{eff} $transition\ layer$	32.74	-2.09	300-500

Table 3.1: Thermal parameters adopted in GaN, AlGaN and transition layer. The considered model is reported in Eq. 3.1, while the calibration of the parameters have been done according to [8].

As already mentioned, the transition layer features, in the case of silicon substrate, a stack of different materials (1.6 $\mu m - Al_{21}Ga_{79}N/$ 0.5 $\mu m - Al_{40}Ga_{60}N/$ 0.5 $\mu m - Al_{76}Ga_{24}N/$ 150 $nm - AlN$). However, from thermal point of view, in the simulation, the transition layer is considered as a homogeneous material, in which all the layers have the same parameters (TBR_{eff} transition layer reported in the Table 3.1). Moreover, the simulator's default models for temperature-dependent thermal conductivity have been used for the silicon substrate.

By considering Fig. 3.10, it is worth noting how the TBR contribution, associated to the overall transition layer, plays an important role in the temperature behavior of device, emphasizing the importance of the developed model for a realistic simulation. In fact, by considering the temperature distribution of Fig. 3.10, it is possible to note that an underestimated channel temperature

is evaluated when default Sentaurus models are considered for the temperature dependence of the thermal conductivity related to the materials of the transition layer.

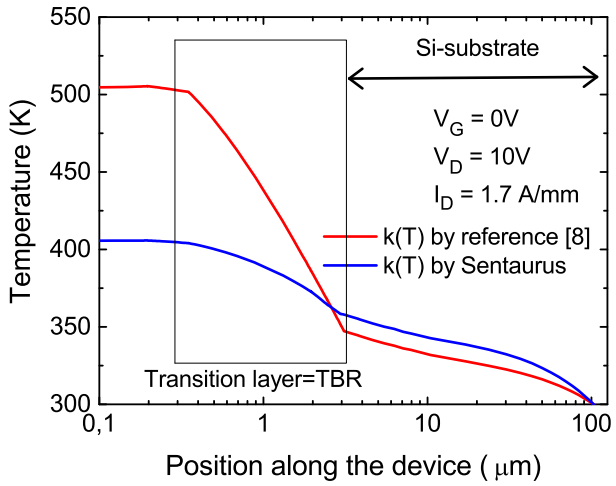

Figure 3.10: Thermal distribution along the device (vertical direction). The thermal boundary resistance (TBR) contribution, modeled by [8], plays an important role in the temperature behavior of device. Moreover, a relevant temperature distribution difference is observable with respect to the case of default Sentaurus models.

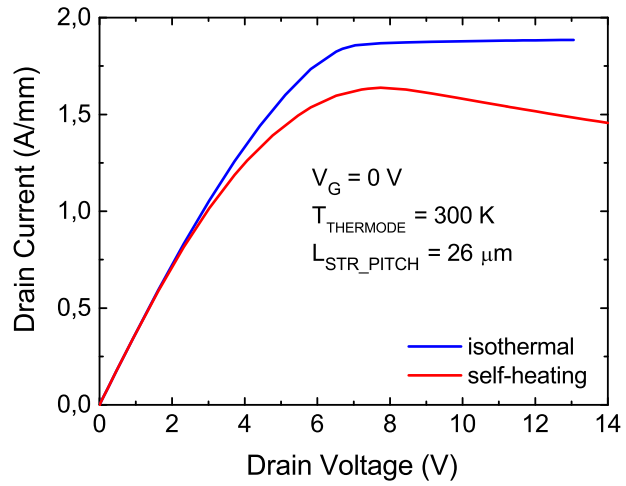

Figure 3.11: Simulated static $I_D V_D$ characteristics. By considering the self-heating effect, a lower drain current is observed with respect to isothermal case due to the higher channel temperature and hence to the mobility degradation.

Finally, the static output characteristics ($I_D V_D$) is shown in Fig. 3.11. By accounting for the self-heating effects in the simulations, higher temperatures occur in the device leading to a mobility degradation. As a result, a lower current density is observed.

3.5 Conclusions

A physical model interface (PMI) accounting for the impact of the transition layer on the self-heating in GaN-based power transistors with silicon and silicon carbide substrate has been implemented and applied to a simulation study of the static and dynamic operation mode. It has been shown that, non-considering the TBR contribution, the device channel/junction temperature can be underestimated up to 25/30 %. Consequently, different trapping related degradation mechanisms may be not fully exploited causing an inaccurate device lifetime prediction.

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Chapter 4

Reliability of GaN-on-Si Schottky Barrier Diodes under ON-State Stress

4.1 Introduction and State of the Art

With the increasing demand for renewable energy, smart and mobile low-power applications, there is an increasing need to fabricate power converters that are compact and evermore efficient and reliable. This evolution starts with improvements at the semiconductor level, and GaN-based power devices represent today one of the best choices due to good trade-off between performance and cost [1]-[4].

In particular, they feature a higher breakdown voltage and a lower ON-resistance with respect to silicon-based devices, because of the wider bandgap of the $III-N$ compounds and the formation of the two-dimensional electron gases (2DEG) at the AlGaN/GaN heterointerface, due to spontaneous and piezoelectric polarization [5], [6]. Moreover, GaN-based devices grown on a silicon substrate [7]-[10], have demonstrated the ability to be produced at a comparable cost than their aging silicon-based competitors [10]. As introduced in Section 1.4 a low-cost fabrication approach relies on the epitaxial growth of GaN over large diameter silicon (Si) substrates, by means of metal-organic chemical vapor deposition (MOCVD) [11]-[13]. Furthermore, this technology, being CMOS-compatible, can take advantage of a widely available and mature technological infrastructure.

Further strengthening the position of GaN-based devices in the power electronic market requires a further improvement of the device reliability. The reliability of GaN-based power devices is mainly limited by trapping and de-trapping phenomena occurring when transistors or diodes have to withstand large electric fields or current density during OFF- and ON-state operation mode, respectively.

Although many papers about trap-related phenomena in GaN high electron mobility transistors (HEMTs) [14]-[27] have been published, the reliability of the GaN-based power devices is still problematic and complex to analyze due to a large number of unknown degradation mechanisms. Moreover, in the case of SDBs, while a limited activity on the reliability to OFF-state stress has been performed [28]-[32], ON-state degradation mechanisms affecting power SBDs received much less attention so far. However, the SBDs, as the transistors, play an important role in various power electronic applications such as boost- [33] and buck-boost-converters [34], inverters [35], UPS systems [36], etc. [37]. As a consequence, an investigation followed by an improvement of the GaN-based Schottky barrier diodes reliability is strongly required.

Terano et al. investigated the relationship between the 2DEG density and the reverse leakage current in AlGaN/GaN SBDs, asserting that a leakage reduction of several orders of magnitude is achieved by slightly reducing the 2DEG density [38].

In [39], the temperature-dependence of the leakage current mechanisms affecting Schottky contacts, fabricated on AlGaN/GaN HFET, was investigated. The authors found out that at room temperature the reverse leakage is dominated by carrier transport via conductive dislocations, whereas at higher temperatures the Frenkel-Poole emission represents the main source of the reverse leakage.

The degradation mechanism and the influence of the anode recess on the electrical properties of the SBDs was analyzed in [28], highlighting that the anode recess process activates traps with relatively short capture and escape times, hence leading to a higher degradation of the I-V characteristics in short reverse stress experiments.

Finally, Hu et al. by combining experimental and simulation results have proposed the physical origin of the current collapse and ON-resistance degradation in Au-free AlGaN/GaN SBDs occurring when a negative bias is applied on the anode [29]. In particular, they have linked the gradual increase of the R_{ON} to those traps featuring an energy of 1 eV below the conduction band and located at $Si_3N_4/AlGaN$ interface. On the other hand, a sudden collapse of the ON-current has been related to the traps having an energy of 0.5 eV, positioned around the Schottky contact corner and playing a role only for the negative bias above a critical value (-175 V in that case).

In this chapter, the degradation mechanisms occurring when a large direct stress current (ON-state) is forced through Au-free AlGaN/GaN Schottky barrier diodes are extensively analyzed.

The impact of the stress on the main figures of merit, such as the turn-on voltage (V_{TON}), the forward voltage (V_F) and the ON-resistance (R_{ON}) are experimentally investigated. In particular, by performing stress and recovery experiments at different voltages and temperatures, it is possible to ascribe the V_{TON} and the R_{ON} degradation to different defects. On one hand defects

triggering V_{TON} degradation are located into the AlGaN barrier layer under the Schottky contact and probably due to nitrogen vacancies. On the other hand, traps causing R_{ON} degradation are located in the access region and probably due to nitrogen antisites in the GaN.

Finally, by combining experimental and simulation analyses, the device geometry dependence on the ON-state degradation is also investigated. Thanks to this approach, it is possible to further understand the degradation sources of the turn-on voltage (V_{TON}) and ON-resistance (R_{ON}). In particular, the vertical electric field occurring under the Schottky contact is responsible for the ΔV_{TON}, whereas the ΔR_{ON} is attributable to the longitudinal electric field in the GaN channel (between anode and cathode contacts).

4.2 Device Structure

Au-free AlGaN/GaN Schottky barrier diodes (SBDs), fabricated on silicon wafers by imec [9], with a nominal forward voltage (V_F) of $\approx$ 1.25 V, are considered in this study and shown in Fig. 4.1.

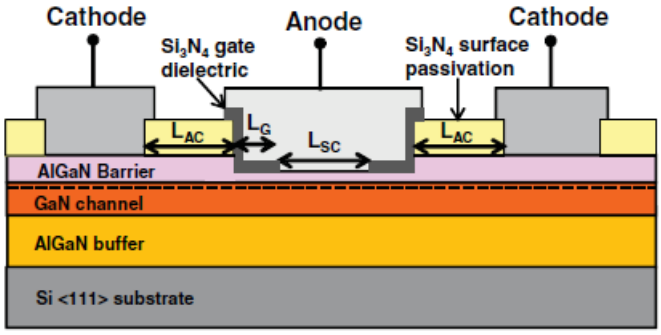

Figure 4.1: Schematic of the AlGaN/GaN-on-Si GET-SBDs (not in scale) [9]. The AlN spacer between the AlGaN barrier and the GaN channel, and the SiN cap between the AlGaN barrier and the Si_3N_4 surface passivation are not shown.

The epitaxial stack, grown on a 8-inch $< 111 >$ silicon substrate by means of MOCVD, features a 200 nm-thick AlN nucleation layer (on top of the Si substrate) followed by a 2800 nm-thick $AlGaN$ buffer, 150 nm-thick GaN channel, 0.5 nm-thick AlN spacer, 10 nm-thick $Al_{25}Ga_{75}N$ barrier, and 5 nm-thick SiN cap. Then the whole epitaxial stack is passivated with 140 nm of Si_3N_4 by rapid thermal chemical vapor deposition (RTCVD). Prior to the deposition of metal stack, the Si_3N_4 passivation layer is removed at the anode region by SF_6 dry etch and a 5 nm deep recess is opened in the AlGaN layer by atomic layer etching in order to improve the forward characteristics. It is worth noting that with the anode recess the forward characteristic is improved

by reducing the V_{TON} and the V_F with respect to the case of non-recessed devices. Moreover, the SBDs functionality not only as a stand-alone diode, but also in combination with MIS-HEMT process flow, was proved [9].

A further 25 nm-thick Si_3N_4 deposition with a subsequent etching in the central region of the anode (with length L_{SC}) is performed in order to make the gated edge terminations (GETs) (Fig. 4.1). Their role is mainly reducing the reverse leakage by splitting and attenuating the electric field peaks occurring at the anode corners.

Finally, Au-free anode and cathode contacts are realized. In particular, an Au-free metal stack, consisting of 20-nm TiN/20-nm Ti/250-nm Al/20-nm Ti/60-nm TiN, is deposited and etched to define the diode anode. A more detailed description of the diodes process is reported in [9].

The experimentally tested devices feature a central anode finger with two independently addressable cathode contacts. By referring to Fig. 1, devices with different Schottky diode lengths (L_{SC}), edge termination lengths (L_G) and anode to cathode spacing lengths (L_{AC}) have been analyzed. The dimensions of the diodes will be specified further in the chapter, where relevant.

4.3 Experimental Setup and Measurement Approach

On-wafer characterization has been performed by means of Keithley Source Measure Units 26XX. The devices degradation has been experimentally carried out by adopting the conventional measure/stress/measure (MSM) technique. During the stress phase a constant voltage (V_{AC_S}) was applied on the anode contact while short-circuiting the two cathodes with the substrate. The stress was periodically interrupted in order to monitor V_{TON}, V_F, and R_{ON} shift by measuring a full I-V characteristic from 0 V to 2.5 V in a time of about 2 s. The turn-on (V_{TON}) and forward (V_F) voltages were extrapolated at a current density of 1 mA/mm and 100 mA/mm, respectively, whereas the ON-resistance (R_{ON}) was evaluated by considering the slope in linear region, between 1.5 V and 2.5 V.

In some characterization (specified where relevant), at the end of the stress phase the reverse leakage current was evaluated by sweeping V_{AC} between 0 V and -6 V. Finally, the recovery was monitored by applying 0 V (V_{AC_R}) and periodically analyzing V_{TON}, V_F, and R_{ON}.

It is worth noting that, because of the process variability across the wafer, devices placed in different dies can show a different value of V_{TON} and/or R_{ON}. In fact, by characterizing all devices of the wafer with $L_{AC} = 3\ \mu m$ (50 devices), a V_{TON} and R_{ON} spread can be observed in the box chart of Fig. 4.2. As a result, an initial screening has been performed in order to guarantee the same current level during the stress phase. In particular, different devices featuring a similar fresh I-V characteristic, and hence a similar V_{TON} and R_{ON}, have been selected (Fig. 4.3) and adopted in this study. Moreover, for each

stress/recovery analysis different devices have been initially considered in order to verify the statistical dispersion of the measurements.

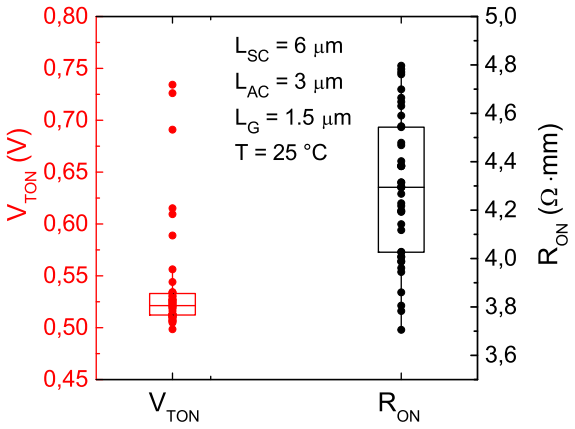

Figure 4.2: Box chart for V_{TON} and R_{ON} considering all device in the wafer with $L_{SC} = 6\ \mu m$, $L_G = 1.5\ \mu m$ and $L_{AC} = 3\ \mu m$ at T = 25 °C. Due to process variability across the wafer a V_{TON} and R_{ON} spread is shown. V_{TON} and R_{ON} were extrapolated at the current density of 1 mA/mm and at the anode cathode voltage of 2.5 V, respectively.

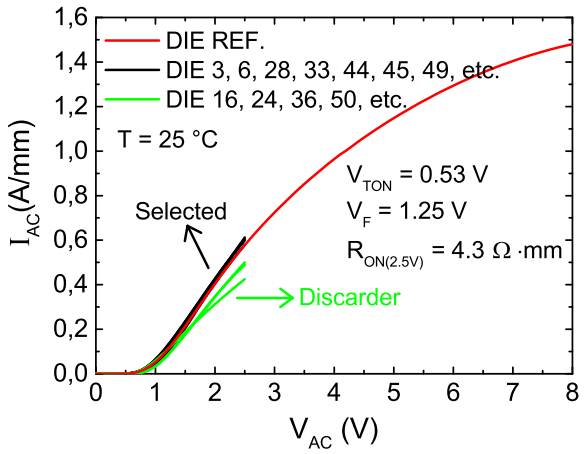

Figure 4.3: Forward characteristics of the GET-SBDs. Due to the variability of the process along the wafer, a screening of devices featuring similar I-V characteristics has been performed.

4.4 Simulation methodology

In order to evaluate the dependence of the ON-state degradation on diode geometry and to understand the degradation mechanisms affecting the devices parameters, experimental analyses combined with TCAD simulations, aimed at evaluating the electric fields distribution along the device, have been performed.

The simulated structure has been defined in Sentaurus TCAD simulator [40] considering the geometric characteristics and material properties of the devices under test (DUT). In particular, the Schottky barrier height, the ohmic contact resistance and the mobility degradation models have been properly set in order to attain the same turn-on voltage (V_{TON}) and comparable forward current levels of the real devices. Moreover, the effect of the traps on the electric field distribution is accounted for in the simulation by considering donor-like traps at the SiN/AlGaN interface (access and GET regions). As a result, a good agreement between experimental and simulated I-V characteristics has been obtained (Fig. 4.4).

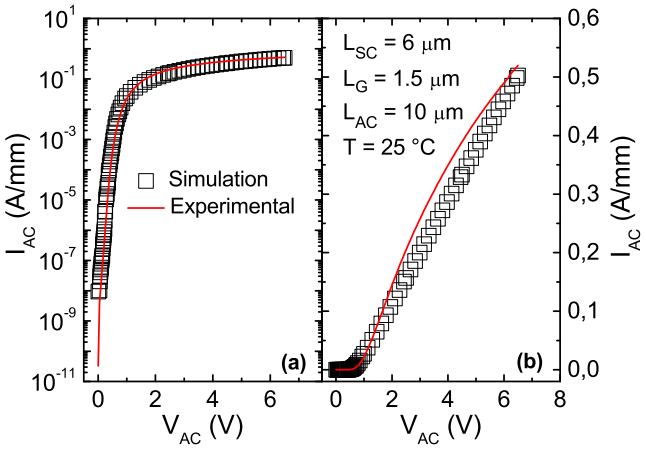

Figure 4.4: Comparison of the I-V characteristics in the case of simulated and experimental device in logarithmic (a) and linear (b) scale. The simulated structure has been calibrated in order to get comparable current level of the real device. As a result, an accurate electric field distribution can be evaluated.

4.5 Results and Discussion

4.5.1 Trapping/de-trapping mechanisms causing V_{TON} degradation

AlGaN/GaN Schottky barrier diodes with $L_{SC} = 9\ \mu m$, $L_G = 1.5\ \mu m$, $L_{AC} = 5\ \mu m$, and a finger width of 100 μm have been adopted for understanding the

trapping/de-trapping mechanisms underneath the V_{TON} degradation.

The turn-on voltage shift occurring during the ON-state stress and recovery is shown in Fig. 4.5. Four devices, positioned in different dies and selected as shown in Fig. 4.3, have been characterized under the same stress and recovery conditions in order to prove a good reproducibility of the V_{TON} degradation induced by trapping/de-trapping mechanisms. During the stress phase, electrons are trapped in the region under the anode (Schottky junction) causing an increase of the Schottky barrier height, and hence of the V_{TON}. Then, as the stress is removed (recovery phase) some defects are de-trapped and a partial V_{TON} recovery occurs.

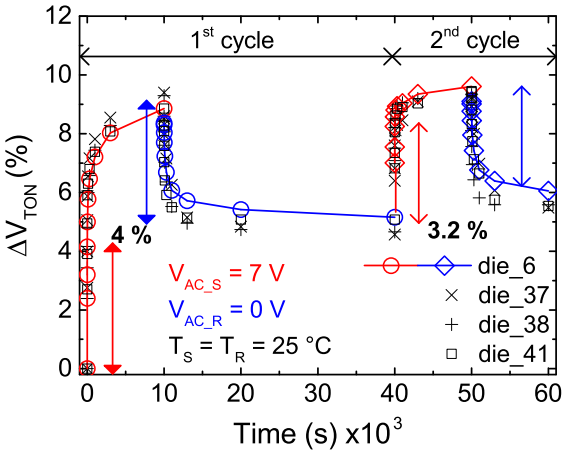

Figure 4.5: Turn-on voltage shift during two cycles of ON-state stress and recovery for four devices positioned in different dies. V_{TON} was extracted at the current density of 1 mA/mm and the following conditions were considered: V_{AC_S} = 7 V (during stress), V_{AC_R} = 0 V (during recovery), T = 25 °C (both phases). The four samples show similar V_{TON} degradation and recovery.

A second cycle of stress and recovery has been performed in order to understand which kind of trapping/de-trapping mechanism occurs, by comparing the two stress and recovery dynamics. It is worth noting that Fig. 4.6a and 4.6b are representative of the average of four samples (reported in Fig. 4.5). In order to account for the statistics dispersion, the error bars were calculated as $\pm 3\sigma$ (standard deviation).

From the evolution of V_{TON} reported in Fig. 4.6a, it is possible to distinguish two degradation phases characterized by different power slopes that may be associated to two different trapping mechanisms. For stress time up to 20 s, the build-up of charge in pre-existing defects appears to be the dominant mechanism causing the degradation, whereas afterwards, as discussed in subsection 4.5.3, the creation of new defects becomes the dominant one.

Based on Figs. 4.5, 4.6a, and 4.6b, it is possible to observe that: i) in both degradation cycles (Fig. 4.5) the relative degradation occurring during the first 10 s of stress is comparable to the amount of the corresponding subsequent recovery ($\approx$ 4 % and $\approx$ 3.2 % for the first and second cycle, respectively);

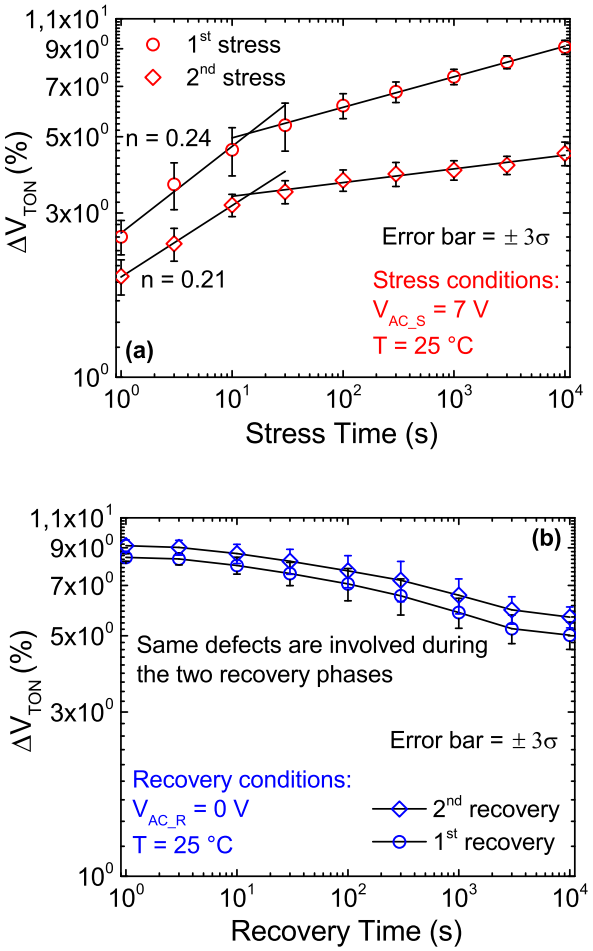

Figure 4.6: Stress and recovery phase related to Fig. 4.5. The dual slope shown in the stress phase (a) is probably attributed to two different mechanisms, build-up of charges and new trap creation, precisely. ΔV_{TON} degradation related to the second cycle is calculated with respect to the end of the first recovery phase. The two recovery phases show a similar dynamics (b), meaning that same defects are involved in the de-trapping mechanism.

ii) for short stress times ($\approx$ 10 s), the V_{TON} degradation features the same dynamics (same slope) in both cycles (Fig. 4.6a); iii) the two recovery phases exhibit the same trend (Fig. 4.6b). In conclusion, by considering together these aspects, it is possible to conclude that the shift of the turn-on voltage in the

first 10 s of stress and during the whole recovery phase, in both cycles, may be mainly ascribed to the trapping and de-trapping of the same pre-existing defects. In addition, these results suggest that pre-existing defects are the source of the recoverable degradation component, whereas the new created defects cause a quasi-permanent or slowly recoverable component.

Thanks to the adopted MSM technique the impact of degradation on reverse leakage during ON-state stress and recovery has been analyzed (Fig. 4.7). A slight non-recoverable reduction of the reverse leakage after the ON-state stress, due to electrons trapping, is shown in Fig. 4.7. By trapping negative charge in the AlGaN barrier layer or at $Si_3N_4/AlGaN$ interface, the 2DEG density in the channel is reduced; therefore, as observed in [32], a reverse leakage reduction may occur.

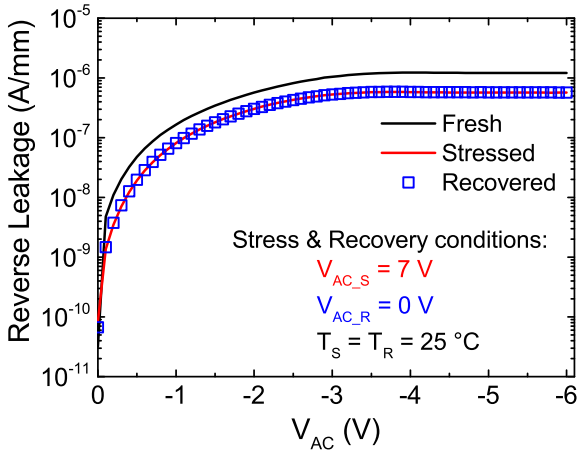

Figure 4.7: Reverse leakage measured in fresh condition, after 10^4 s of stress and after $3 \cdot 10^4$ s of recovery. The electrons trapping during the ON-state stress lead to a slight reduction of the reverse leakage.

4.5.2 Voltage-dependence

It is worth noting that from here on, the reverse leakage measurement has not been performed in order to avoid a possible alteration of the defects state due to negative voltage sweep. Moreover, given the limited statistical dispersion reported in Fig. 4.6, from here on (except where specified) a single device is used for each stress/recovery condition.

The V_{TON} degradation for different stress voltages is reported in Fig. 4.8. As already discussed with reference to Fig. 4.6a, two degradation phases are evident, and the first one may be attributed to pre-existing traps filling. Indeed, by increasing the stress voltage, the end of the first degradation phase (i.e. the change of the power slope) occurs for shorter stress time. This is expected when a fixed number of traps, with a fixed energy level, are present in the

fresh device. By applying a higher stress bias a faster charge trapping occurs, leading to a larger degradation and to a faster filling of the available traps.

Finally, as it is possible to observe in Fig. 4.9, the voltage-dependence of both turn-on and forward voltage degradations can be modeled by a power law.

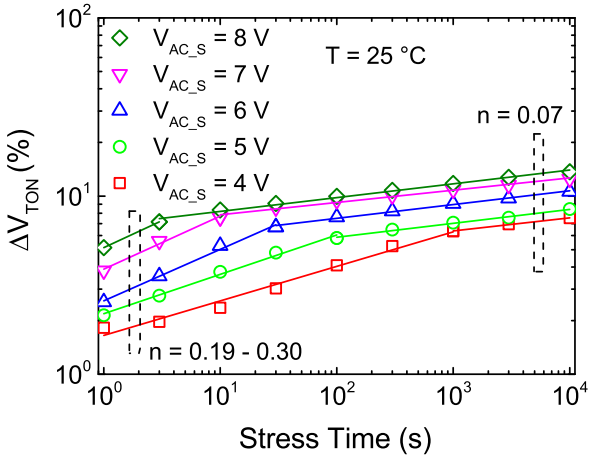

Figure 4.8: V_{TON} shift for different ON-state stress conditions. By stressing at higher voltage, the pre-existing traps filling is faster. As a result, the change of the logarithmic slope occurs for shorter stress time.

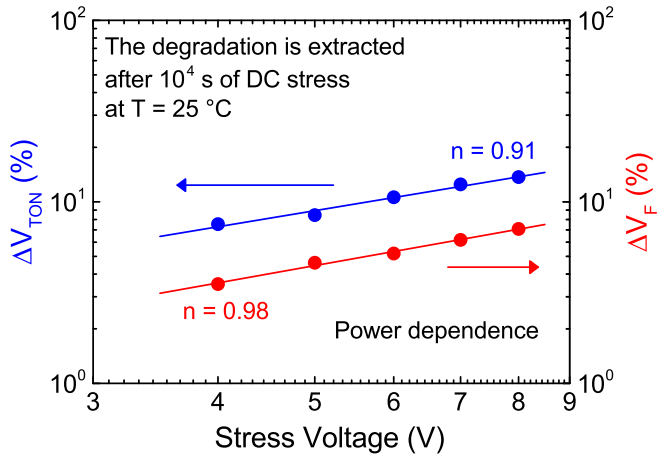

Figure 4.9: Turn-on and forward voltage degradation versus stress voltage. A power dependence is observed for both parameters.

On the other hand, the evolution of ΔR_{ON} and its dependence on stress bias are much more complex, and chaotic, compared to the case of turn-on voltage. Causes and reasons will be more deeply explored in subsection 4.5.4.

4.5.3 Temperature-dependence

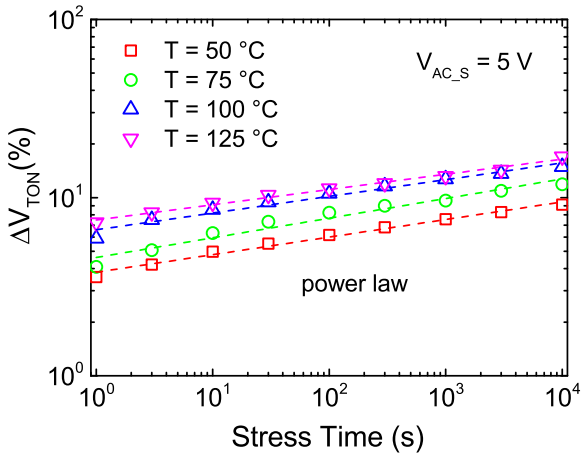

Figure 4.10: Turn-on voltage shift for different temperatures stress.

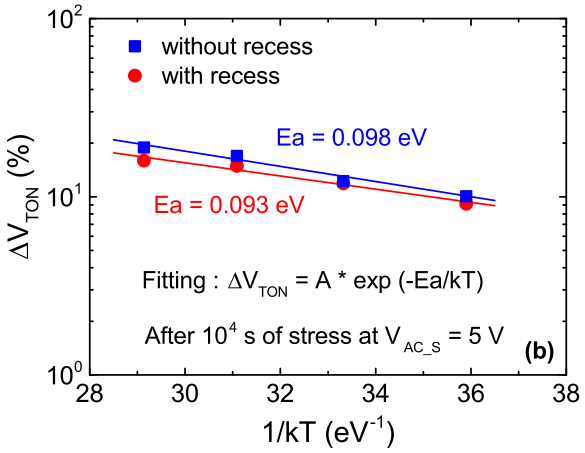

Figure 4.11: Arrhenius plot. The V_{TON} shift has been extracted at the end of the stress (10^4 s) in devices with (circle) and without (square) anode recess. By considering the database of the deep levels in GaN- and AlGaN-based devices [41], the activation energy of ≈ 0.09 eV is linked to the nitrogen vacancies.

The role of the temperature on the ON-state degradation has been investigated on the same devices analyzed in the two previous sections. Fig. 4.10 shows the shift of the turn-on voltage as a function of the temperature. It can be noticed that, by stressing at temperatures higher than 25 °C, the dual slope of the V_{TON} degradation is not clearly observed (Fig. 4.10), contrary to the case of room temperature (Fig. 4.8). As a matter of fact, by increasing the

temperature the process of filling of pre-existing traps, according to results, may be shorter than 1 s suggesting the presence of very shallow pre-existing traps. Moreover, curves at different temperatures feature a similar slope (0.08) that is similar to the second degradation phase of the room temperature case reported in Fig. 4.8.

By considering the Arrhenius plot of Fig. 4.11, an effective activation energy of 0.093 eV has been extracted from V_{TON} degradation. The database of the deep levels in GaN- and AlGaN-based devices (see [41]) suggests that traps having an activation energy of 0.09 eV can be ascribed to the nitrogen vacancies. A similar value has been found by Bisi et al. in AlGaN/GaN HEMT [41], by means of the current transient investigation at several temperature levels, linking these traps to the AlGaN barrier in the region under the gate.

In the case of diodes, the V_{TON} shift under forward stress is ascribed to an increase of Schottky barrier height and features a similar activation energy (0.093 eV). Hence, it can be assumed that traps, responsible for V_{TON} degradation, are located in the AlGaN barrier layer under the anode metal. An activation energy of 0.093 eV suggests that the traps are fairly shallow, and hence they should feature a short trapping/de-trapping time constant. On the contrary, in this case the activation energy is extracted after 10^4 s of stress. This observation confirms that the creation of new defects is the responsible mechanism causing the degradation.

In order to understand which is the cause of the nitrogen vacancies, a study of the temperature dependence of V_{TON} degradation has been performed also on devices without anode recess (Fig. 4.11). By considering the Arrhenius plot of Fig. 4.11, we can observe that: i) devices without recess show a comparable (or slightly higher) V_{TON} degradation; ii) the V_{TON} shift in both typologies of device is induced by the same kind of traps because of the similar activation energies. As a result, nitrogen vacancies are not caused by the recess process but probably are linked to crystal quality of the AlGaN barrier layer. By avoiding the anode recess, the AlGaN barrier under the anode metal is thicker; as a consequence, a larger number of bulk defects are present, leading to a slightly higher V_{TON} degradation.

Finally, the study of the R_{ON} degradation for different temperatures is shown in Fig. 4.12a. It seems from this figure that no R_{ON} degradation increase is observed for higher temperatures. On the other hand, from Fig. 4.12b, it is possible to observe a decrease of the ON-current during the stress and a huge recovery happening during each measurement phase. It is well known that by increasing the temperature, the de-trapping mechanism becomes faster, and hence the de-trapping time constant could be lower than the delay time introduced by measurement setup. As a result, the ON-resistance degrades during the stress but it is not possible to catch the real degradation with this technique. This suggests that R_{ON} and V_{TON} degradations are due to different defects, however, as previously anticipated, an in-depth investigation of R_{ON}

degradation will be shown in subsection 4.5.4.

It is worth noting that SBDs in actual application are forced to work with fixed ON-current, rather than with fixed V_{AC}. However, the change of the ON-current, during the stress (see Fig. 4.12b) at fixed voltage, is relatively low.

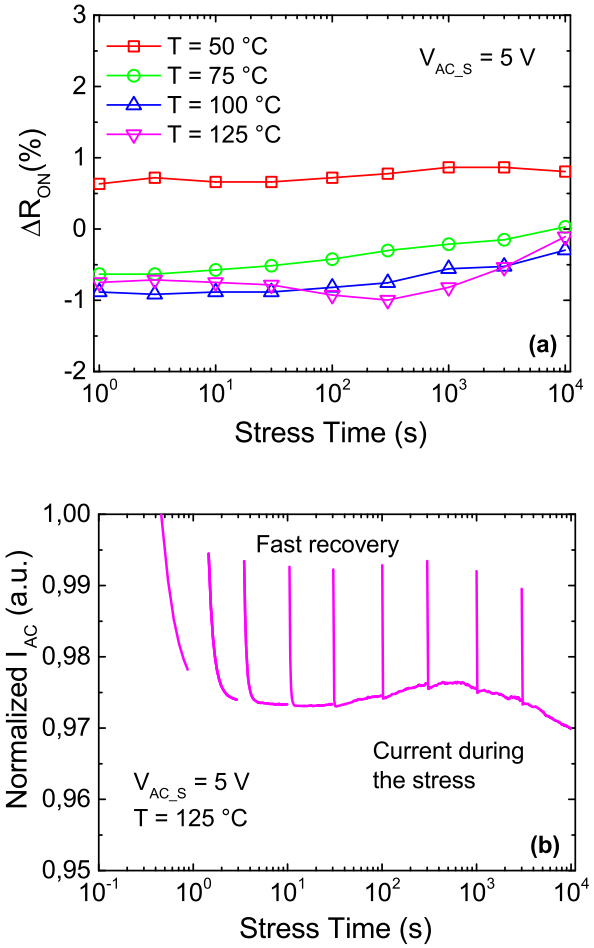

Figure 4.12: R_{ON} degradation at different temperatures (a). By increasing the temperature, as the stress voltage is removed in order to perform an IV characteristics, a fast recovery of the ON-current is observable (b). As a result, no R_{ON} degradation is shown (a).

4.5.4 Anode to cathode spacing length (L_{AC}) dependence

AlGaN/GaN Schottky barrier diodes with $L_{SC} = 6\ \mu m$, $L_G = 1.5\ \mu m$, different L_{AC} (3, 10 and 20 μm), and a finger width of 100 μm have been adopted for understanding the L_{AC} dependence on the ON-state degradation. By reducing L_{AC}, the devices show an improved ON-characteristic due to lower

ON-resistance (Fig. 4.13). On the other hand, for high stress voltages, the higher electric fields between anode and cathode accelerate the degradation mechanisms allowing to understand the causes underneath the device degradation.

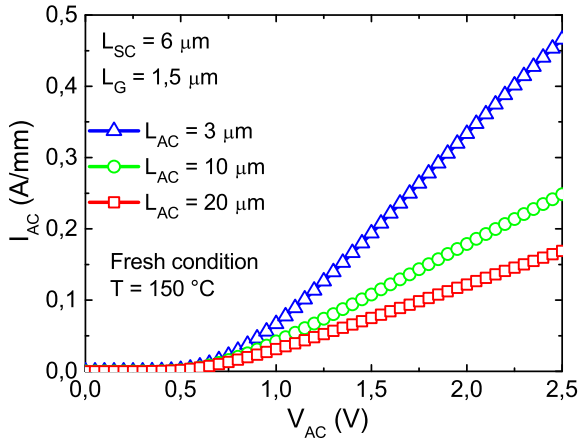

Figure 4.13: I-V characteristics of devices featuring different anode to cathode spacing lengths. By reducing L_{AC}, the devices show an improved ON-characteristic due to lower ON-resistance.

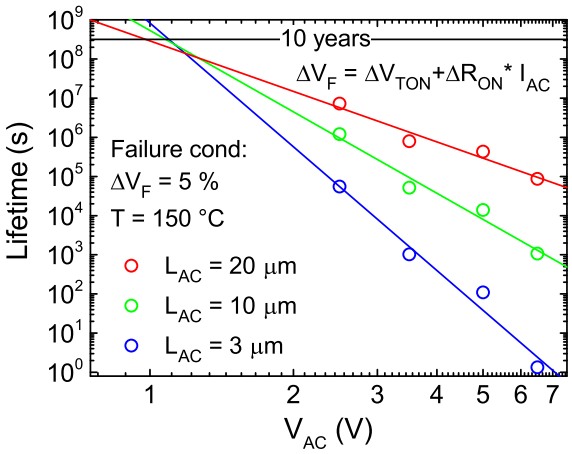

Figure 4.14: Lifetime estimation as function of anode-cathode spacing lengths (L_{AC}). The failure criterion is considered as 5 % shift of the forward voltage (ΔV_F) at the temperature of 150 °C. By increasing the anode to cathode stress voltage (V_{AC}), shorter devices show a higher V_F degradation.

The analysis of the ON-state degradation at different stress biases, by

means of constant voltage-stress method, allowed to estimate the lifetime of the AlGaN/GaN-on-Si GET-SBDs at the temperatures of 150 °C, as reported in Fig. 4.14. The lifetime has been extrapolated by considering the forward voltage degradation since it takes into account both V_{TON} and R_{ON} degradations by the following relationship:

$$\Delta V_F = \Delta V_{TON} + \Delta R_{ON} \cdot I_{AC} \tag{4.1}$$

In particular, a threshold ΔV_F value of the 5 % in 10 years has been selected. Four devices with a similar fresh I-V characteristic have been stressed for each L_{AC}. However, the reproducibility of the device degradation, due to ON-state stress, has been proven in section 4.5.1 by stressing different selected devices with the same stress conditions. By analyzing Fig. 4.14, for high stress voltages, short anode-cathode devices exhibit a significant larger degradation in the forward voltage (V_F), i.e. lower lifetime, with respect to wide anode-cathode devices. Intuitively, this can be ascribed to higher electric fields under the Schottky contact and/or in the anode to cathode access region. Interestingly, such a difference is not observed for low stress voltage and a crossing point is observed around V_{AC} = 1.2 V. Hence, the three analyzed L_{AC} lengths give rise to different power law fittings.

Since the ΔV_F is due to the combined effect of the turn-on voltage (V_{TON}) and on-resistance (R_{ON}) degradation by the relationship shown in Eq. 4.1, their contributions are separately evaluated in Fig. 4.15 and 4.16, respectively.

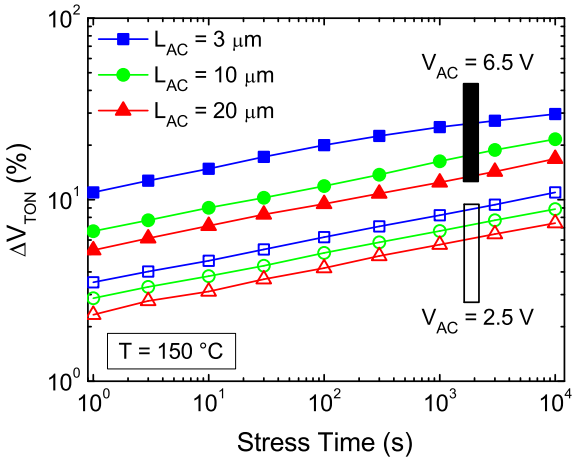

Figure 4.15: Turn-on voltage degradation, due to ON-state stress, evaluated for different L_{AC} at V_{AC} = 6.5 V (filled markers) and V_{AC} = 2.5 V (empty markers). V_{TON} was extrapolated at the current density of 1 mA/mm. As the stress voltage increases, a higher difference in V_{TON} degradation, between short and long device, is shown.

Although a significant V_{TON} degradation is observed with stress voltage- and L_{AC}-dependence (Fig. 4.15), in the case of the R_{ON} (Fig. 4.16), a sizable degradation is only observable for $V_{AC} = 6.5$ V and $L_{AC} = 3\ \mu m$. This suggests that different sources of degradation affect V_{TON} and R_{ON}.

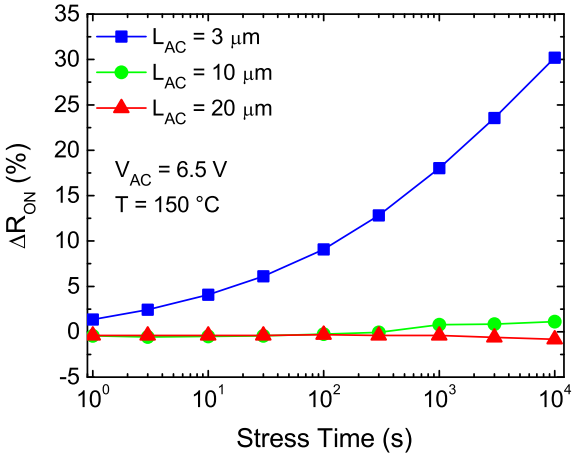

Figure 4.16: ON-resistance degradation evaluated for $V_{AC} = 6.5$ V and different L_{AC}, by considering the slope in linear region, between 1.5 V and 2.5 V. In spite of V_{TON} degradation (see Fig. 4.15), devices equal to or longer than 10 μm do not show R_{ON} shift. As a result, different mechanisms of degradation affect R_{ON} and V_{TON}.

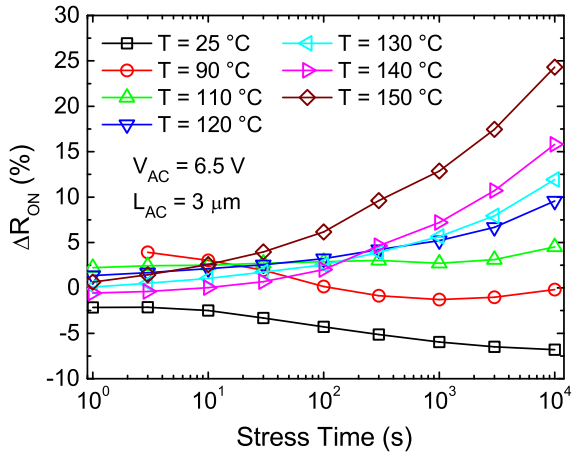

Figure 4.17: R_{ON} degradation evaluated at different temperatures. A significant temperature dependence is observed. Considerable R_{ON} degradation starts to occur only for T > 110 °C.

The important role of the temperature in the R_{ON} degradation is reported in Fig. 4.17. Despite the high voltage applied between anode and cathode, a significant ΔR_{ON} occurs only for temperatures higher than 110 °C. By considering the Arrhenius plots for R_{ON} shown in Fig. 4.18, an activation energy of 0.54 eV is estimated. According to results in the literature [41], the corresponding defects could be associated to nitrogen antisites in the gallium nitride (GaN).

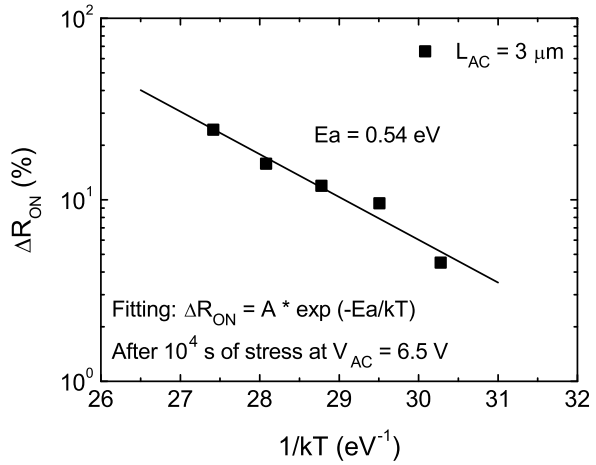

Figure 4.18: Arrhenius plot evaluated by considering the R_{ON} shift achieved at the end of the stress (10^4 s). By considering the database of the deep levels in GaN- and AlGaN-based devices [41], the activation energy of $\approx$ 0.54 eV is linked to the nitrogen antisites in the gallium nitride (GaN).

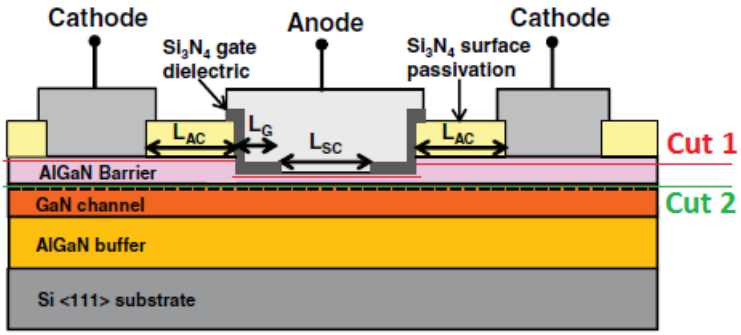

Figure 4.19: Cut1 and Cut2 represent the sections where the electric field is monitored by means of TCAD simulator.

It is worth noting that the activation energy for V_{TON} (0.09 eV) has been evaluated in section 4.5.3 proposing nitrogen vacancies, probably linked to

crystal quality of the AlGaN barrier, as defects responsible for the degradation of V_{TON}. However, it is again proved that R_{ON} and V_{TON} degradations are due to different kind of defects.

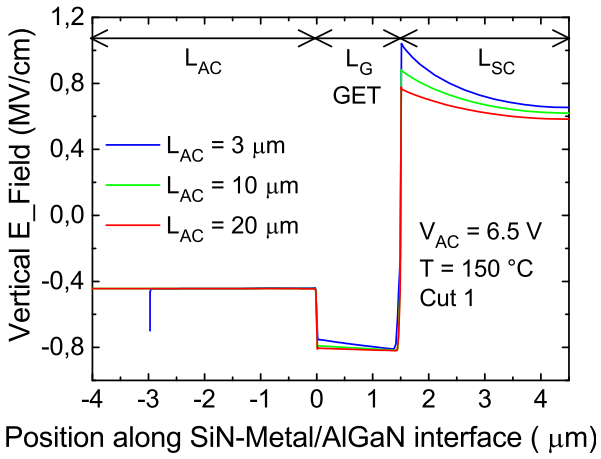

Figure 4.20: Vertical electric field profile in the AlGaN barrier close to interface with SiN and metal (cut 1 in Fig. 4.19) for high stress voltage. For high V_{AC} shorter devices show a larger electric field only in the region under the anode (Schottky) contact (L_{SC}) leading to a higher V_{TON} degradation (Fig. 4.15).

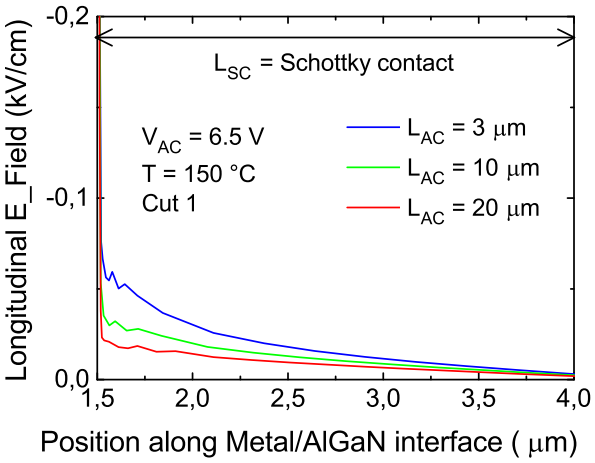

Figure 4.21: Longitudinal electric field profile in the AlGaN barrier close to interface with metal (cut 1 in Fig. 4.19). Despite the high anode voltage, low values of the longitudinal component of the electric field is noticeable, suggesting that it is irrelevant for the V_{TON} degradation.

In order to understand the sources triggering V_{TON} and R_{ON} degradation, TCAD simulations [40], aimed at evaluating the electric fields distributions

in the structure, have been performed. By considering the cut 1 of Fig. 4.19, the vertical component of the electric field at the SiN/AlGaN and at the metal/AlGaN (Schottky contact) interface, in the case of $V_{AC} = 6.5$ V for different L_{AC}, is shown in Fig. 4.20. By changing L_{AC}, the only difference is observed under the Schottky contact region near the edge termination (GET), where shorter devices exhibit a higher electric field and hence a higher V_{TON} degradation with respect to longer devices (Fig. 4.15). By observing Fig. 4.21, it is worth noting that in this region, the longitudinal component of the electric field is negligible, hence it is not able to contribute to the V_{TON} degradation.

The L_{AC} dependence of the R_{ON} degradation cannot be explained by the vertical component of the electric field since it is unchanged in the GET and anode-cathode spacing regions (Fig. 4.20) where the contribution to the overall on-resistance is dominant. Instead, by observing Fig. 4.22 it is possible to note a significant difference, between short and long device, for the electric field component longitudinal to current flow (cut 2 of Fig. 4.19). The link between longitudinal electric field and R_{ON} degradation is demonstrated in Fig. 4.23 and 4.24 by applying different stress voltages on devices with $L_{AC} = 5\ \mu m$. For electric fields higher than ≈ 6 kV/cm the R_{ON} starts to degrade. This dependence on the longitudinal electric field automatically implies a dependence on the current value because of their correlation. In particular, for an electric field of ≈ 6 kV/cm at T = 150 °C these devices feature an ON-state current density of ≈ 0.45 A/mm.

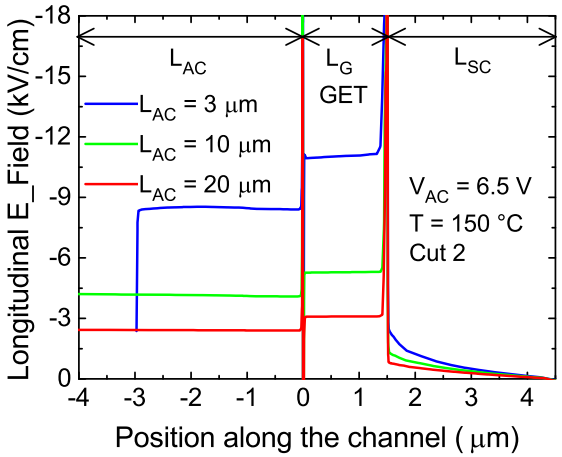

Figure 4.22: Longitudinal electric field profile in the GaN channel close to interface with AlGaN barrier (cut 2), for high stress voltage. By reducing L_{AC} a larger electric field difference, between short and long devices, is only shown in the L_G and L_{AC} regions. As a result, for high V_{AC}, larger ΔR_{ON} is shown for shorter devices.

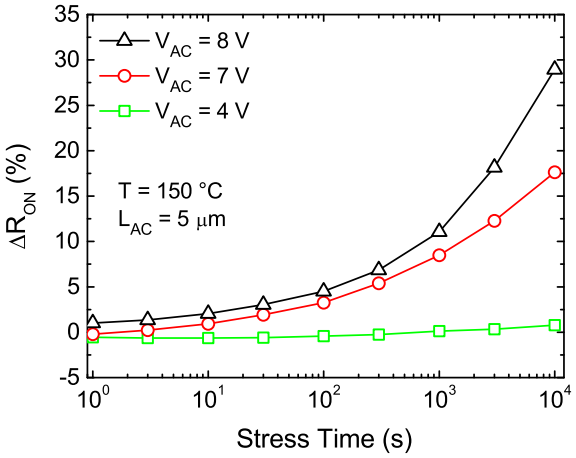

Figure 4.23: ΔR_{ON} evaluated with different anode bias stress on devices with $L_{AC} = 5\ \mu m$. The R_{ON} degradation is due to combined effect of temperature and longitudinal electric field (mainly under the L_G region).

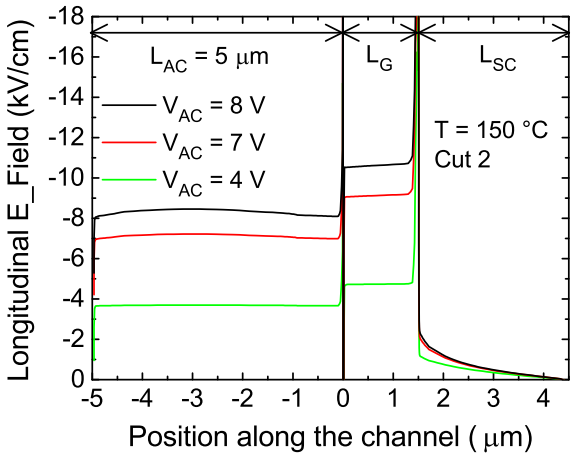

Figure 4.24: Longitudinal electric field profile (cut 2) related to the stress conditions of Fig. 4.23. A correlation between electric field and ΔR_{ON} is shown. Moreover, by comparing Fig. 4.23 and 4.16, despite the different L_{AC} and V_{AC}, a similar ΔR_{ON} ($\approx$ 30 %) is obtained under a similar electric field (Fig. 4.24 and 4.24, respectively).

The existence of a critical longitudinal electric field is in agreement with Fig. 4.22 and 4.16, where no degradation is observed for an electric field lower than $\approx$ 6 kV/cm. Moreover, devices with different L_{AC} (3 μm or 5 μm) featuring the same longitudinal electric field (11 kV/cm in Fig. 4.22 and 4.24), show a similar R_{ON} degradation ($\approx$ 30 %), as reported in Fig. 4.15 and 4.23. This confirms that the cause of the R_{ON} shift is due to combined effect of

longitudinal electric field (current level) and temperature.

The relation between longitudinal electric field in the GaN channel (cut 2) and the ON-resistance degradation is shown in Fig. 4.25 by adopting devices with $L_{AC} = 3\ \mu m$. In particular, the electric field component under the edge termination (L_G or GET) has been monitored since, in this region, it is maximized (Fig. 4.24). The corresponding applied anode to cathode voltage (V_{AC}) is reported on the top x-axis (Fig. 4.25).

By observing Fig. 4.25, the R_{ON} degradation on the electric field is well modeled by a power law. It is possible to note that, in order to have a significant R_{ON} degradation (i.e. larger than 5 % after $3 \cdot 10^4$ s of stress at the temperature of 150 °C) a longitudinal electric field higher than 7 kV/cm (density current higher than 0.52 A/mm) is required.

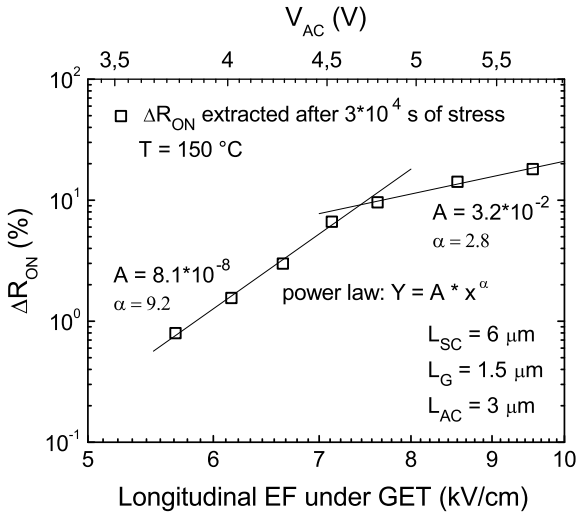

Figure 4.25: ON-resistance degradation versus the Longitudinal component of the electric field under the edge termination region (region where the highest value occurs (Fig. 4.24)) in the GaN channel (cut 2). A power dependence with a double slope is observed. Moreover, as long as the electric field is lower than 7 kV/cm, the R_{ON} degradation can be considered negligible.

Finally, Fig. 4.26 and 4.27 show the vertical and the longitudinal component of the electric field in the case of low stress voltage ($V_{AC} = 1$ V). The low electric field values shown in Fig. 4.26 and 4.27, do not introduce a significant difference in V_{TON} and R_{ON} degradations, respectively. In particular, in Fig. 4.27, the electric fields are lower than 1 kV/cm and hence lower than the critical longitudinal electric field. As a result, negligible V_{TON} and R_{ON} degradation is caused in both short and long devices and a comparable V_F degradation is observed for low anode to cathode voltages (Fig. 4.14).

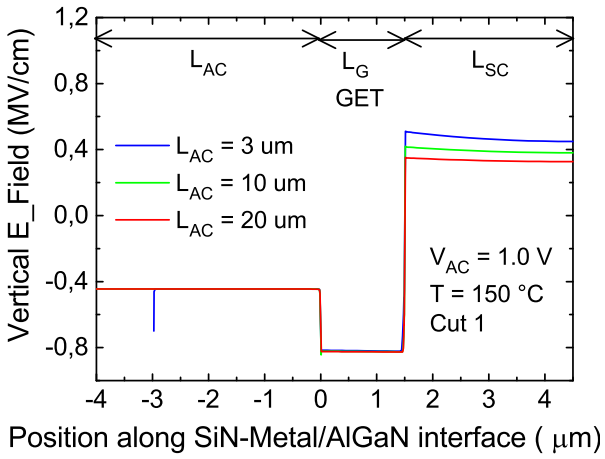

Figure 4.26: Vertical electric field profile in the AlGaN barrier close to interface with SiN and metal (cut 1 in Fig. 4.19), for low stress voltage. Differently to the high V_{AC} case (Fig. 4.20), for low V_{AC}, relatively low electric field values reduce the difference in V_{TON} degradation, between short and long devices (as observed in Fig. 4.15).

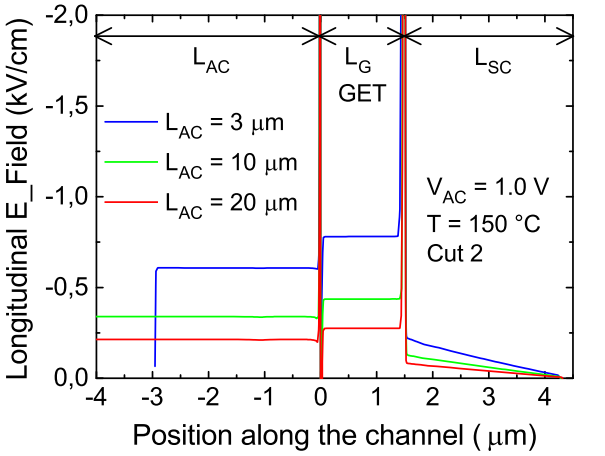

Figure 4.27: Longitudinal electric field profile in the GaN channel close to interface with AlGaN barrier (cut 2), for low stress voltage. Contrarily to high voltage case (Fig. 4.22), for low V_{AC} the small electric fields (smaller than a critical value) do not trigger R_{ON} degradation in both short and long devices.

4.5.5 Schottky contact length (L_{SC}) dependence

The influence of L_{SC} has been studied on devices featuring different Schottky contact lengths (6, 9, 12 and 15 μm), an edge termination length (L_G) of 1.5

μm, an anode to cathode spacing (L_{AC}) of 10 μm, and a finger width of 100 μm.

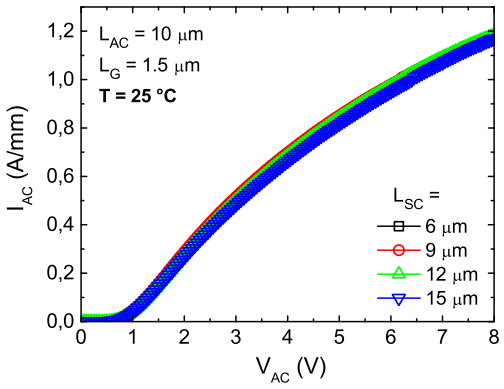

Figure 4.28: I-V characteristics of devices featuring different Schottky contact lengths. Due to the current crowding phenomenon occurring at the anode contact, the I-V curves are similar for different L_{SC}.

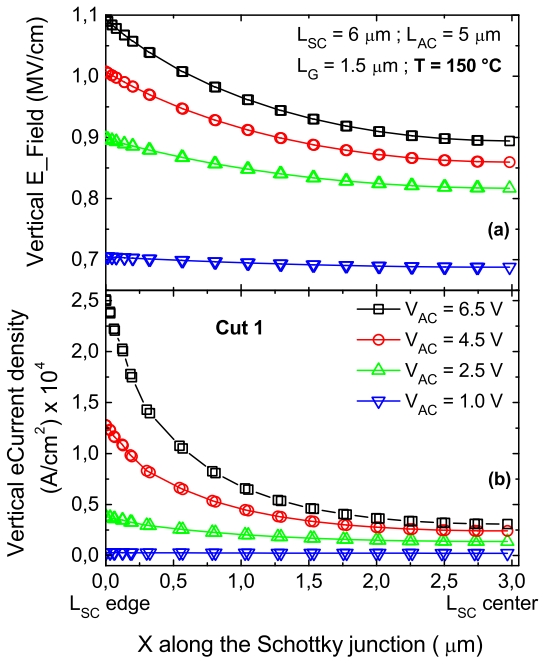

Figure 4.29: Simulated vertical electric field (a) and electron current density (b) under the Schottky contact close to the metal/AlGaN interface (cut 1 of Fig. 4.19). By increasing the anode to cathode bias (V_{AC}) a vertical current flow confinement is shown (b).

By observing Fig. 4.28, it is possible to note that same I-V characteristics are found for devices with different L_{SC}. This behavior is related to the electric field distribution, and hence to the current density distribution (Fig. 4.29b), under the anode contact.

In forward operation mode, by increasing the anode to cathode bias (V_{AC}), the electric field tends to be higher at the edge of Schottky contact, causing a current crowding at the contact edge (current transfer length) [42]. As a matter of fact, for V_{AC} higher than 2.5 V the anode current is limited by the contact resistance. Hence, the increase of L_{SC} does not lead to significant current improvement.

It is worth noting that, only half structure (hence half L_{SC}) has been considered in the simulations because of the device symmetry.

In order to understand how the Schottky contact length affects the diode reliability, a study of the degradation mechanisms has been performed for devices with different L_{SC}. The analysis of the ON-state degradation at different stress biases, by means of constant voltage-stress method, allows to estimate the lifetime of the AlGaN/GaN-on-Si GET-SBDs at the temperatures of 150 °C, as reported in Fig. 4.30. As in the previous section, the lifetime has been extrapolated by considering the 5 % of ΔV_F in 10 years, since it takes into account both V_{TON} and R_{ON} degradations.

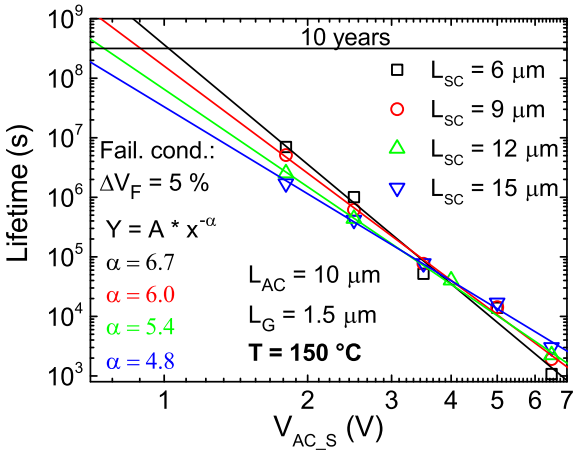

Figure 4.30: Lifetime estimation as a function of the Schottky contact lengths (L_{SC}). The failure criterion is considered as 5 % shift of the forward voltage (ΔV_F) at the temperature of 150 °C. By reducing the anode to cathode stress voltage (V_{AC_S}), shorter devices show a lower V_F degradation leading to a longer lifetime.

The typical operating bias for the devices under test corresponds to SBD forward voltage (V_F), i.e. around 1.2 V. However, in order to perform a study

of the ON-state degradation in reasonable times, accelerate stress conditions (high voltages and temperatures) have been adopted allowing to understand the sources of the degradation and to estimate the device reliability at the typical operating voltage through extrapolation from high-voltage and temperature conditions.

By observing Fig. 4.30, it is possible to note how the amount of V_F degradation depends on both anode stress voltage (V_{AC_S}) and Schottky contact length (L_{SC}). In fact, lifetime vs. V_{AC_S} plot has a power slope which is a function of L_{SC}: the larger L_{SC}, the lower the slope (α) in absolute value. The cross-point of the curves is around 3.5 V. As a result, shorter devices exhibit a longer lifetime or, in other words, can handle a higher anode voltage, during ON-state operation mode, guaranteeing the same lifetime (10 years).

Since the ΔV_F is due to the combined effect of the turn-on voltage and ON-resistance degradation, their contributions are separately evaluated in Fig. 4.31a and 4.31b, respectively, for low and high V_{AC_S}.

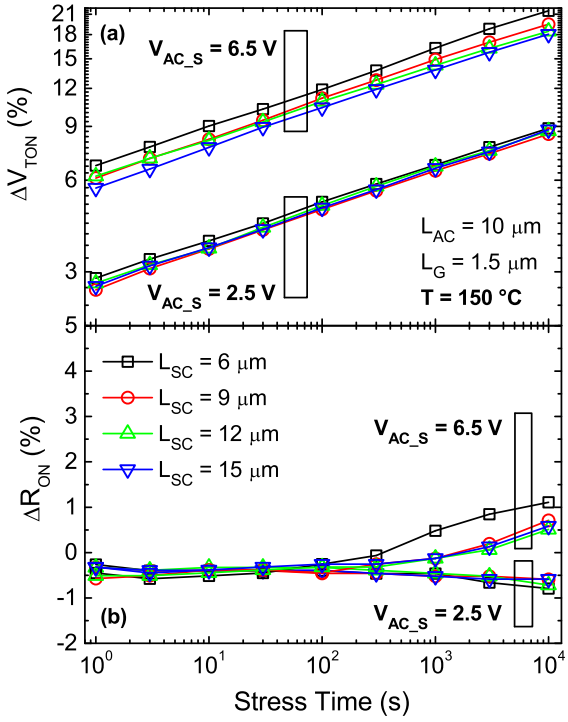

Figure 4.31: Turn-on voltage (a) and ON-resistance (b) degradations, due to ON-state stress, evaluated for different L_{SC} at V_{AC_S} = 6.5 V and V_{AC_S} = 1.8 V. The L_{SC}- and the stress voltage-dependencies of the ΔV_{TON} are explained by the vertical electric field under the anode contact (Fig. 4.32). No L_{SC} dependence is shown in the case of ON-resistance degradation (b).

By focusing on the ΔV_{TON} (Fig. 4.31a), a stress voltage- and a L_{SC}-dependence is shown. In particular, for V_{AC_S} = 6.5 V shorter devices show a larger V_{TON} degradation, whereas for V_{AC_S} = 1..8 V the L_{SC}-dependence of ΔV_{TON} is negligible and seems to reverse for lower stress voltages. This behavior is explained by the vertical component of the electric field in the region under the Schottky contact (Fig. 4.32). By applying 6.5 V on the anode contact, a high electric field peak occurs at the corner between edge termination and Schottky contact (origin in Fig. 4.32). Moreover, the peak is higher for shorter L_{SC}, leading to a larger V_{TON} degradation.

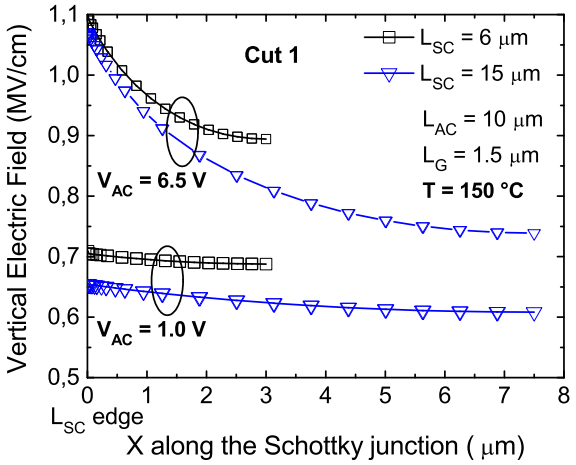

Figure 4.32: Vertical electric field profile in the AlGaN barrier close to interface with metal (cut 1 in Fig. 4.19), for high and low anode voltages. For high V_{AC} a higher electric field peak occurs in shorter devices leading to a larger V_{TON} degradation (Fig. 4.31a). On the other hand, for low V_{AC}, relatively low electric field values do not introduce a difference in V_{TON} degradation. On the contrary, due to uniform electric field distribution, longer devices may be affected by a larger ΔV_{TON}.

In the case of low anode bias, it is thought that the lower electric field values, found for both L_{SC} lengths, have a small impact on V_{TON} degradation. On the contrary, since the electric field distribution and the electron current density are approximately uniform along the Schottky junction (Fig. 4.32 V_{AC} = 1 V or Fig. 4.29 V_{AC} = 2.5 V and lower), a longer anode contact may lead to a larger V_{TON} degradation.

By focusing on the ON-resistance degradation (Fig. 4.31b), it is possible to note that, for both high (6.5 V) and low (1.8 V) stress voltages, the ΔR_{ON} is negligible (around $\pm$ 1 %) and no appreciable L_{SC} dependence is observed. This is in agreement with the results discussed in the previous section, where it has been shown that the source triggering R_{ON} degradation is the longitudinal

component of the electric field in the regions where the contribution to the overall ON-resistance is dominant, such as edge termination (GET) and anode to cathode access (L_{AC}) regions. Moreover, it has been shown that with a temperature operation of 150 °C, an electric field higher than ≈ 7 kV/cm is needed in order to achieve a significant R_{ON} degradation. Fig. 4.33 shows the longitudinal component of the electric fields related to the stress conditions of Fig. 4.31b. By applying a high stress voltage (6.5 V), the electric field, in particular under the GET region, is lower than 7 kV/cm and no L_{SC} dependence is shown.

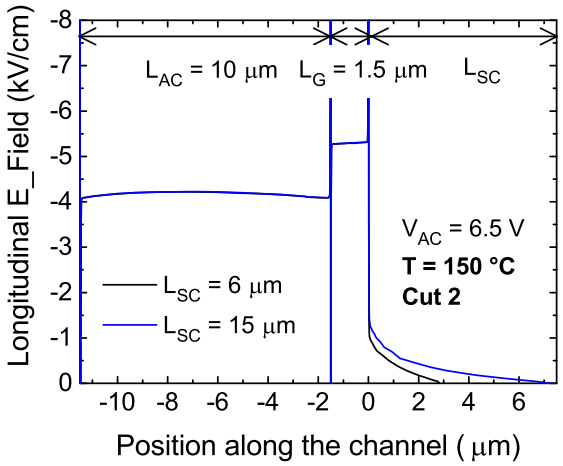

Figure 4.33: Longitudinal electric field profile (cut 2 in Fig. 4.19) with an anode bias of 6.5 V in the case of the shortest and longest device. By applying a high anode bias (6.5 V), the longitudinal electric field is lower than 7 kV/cm, hence negligible degradation is shown.

Overall, by changing the Schottky contact length only the turn-on voltage degradation is affected. In particular, by analyzing Fig. 4.29, 4.30 and 4.32, for $V_{AC} > 4$ V the vertical electric field is confined to the anode corner and a higher peak occurs in shorter devices, leading to a larger ΔV_{TON}. On the other hand, for $V_{AC} < 3$ V, the electric field and the current density (Fig. 4.29) tend to be uniform in the overall Schottky junction. As a result, longer diodes, featuring a larger Schottky contact area, may be subject to a larger V_{TON} degradation.

4.5.6 Edge termination length (L_G) dependence

AlGaN/GaN Schottky barrier diodes with $L_{SC} = 6$ μm, different L_G (1, 1.5, and 2 μm), $L_{AC} = 5$ μm, and a finger width of 100 μm have been adopted for understanding the L_G dependence on the ON-state degradation. The limited devices availability has dictated the choice to use diodes featuring a different

L_{AC} with respect to those investigated in section 4.5.5. However, in the case of $L_G = 1\ \mu m$ and $L_G = 2\ \mu m$, more devices (7 for each L_G), positioned in different dies but featuring a similar I-V characteristic in fresh condition, have been characterized under the same stress condition in order to verify the statistical dispersion of the measurements, and to prove a good reproducibility of the device degradation induced by trapping/de-trapping mechanisms.

In AlGaN/GaN-based devices, the main contribution to the overall ON-resistance comes from the two-dimensional electron gas (2DEG) in the access region. In the case of GET-SBDs, the R_{ON} is mainly attributable to the region between the anode and cathode contacts. Therefore, by reducing L_G, an improved forward characteristics, due to lower R_{ON}, is attained (Fig. 4.34).

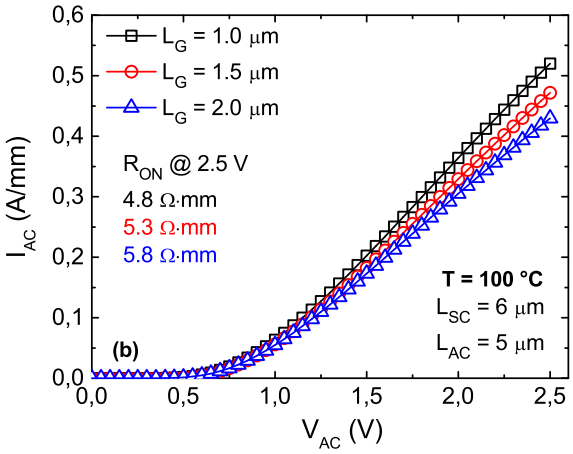

Figure 4.34: I-V characteristics of devices featuring different edge termination lengths. By reducing L_G, the devices show an improved ON-characteristic due to lower ON-resistance.

The turn-on voltage and the ON-resistance degradations, in the case of $V_{AC\_S} = 2.5$ V at T = 100 °C, are shown in Fig. 4.35a and Fig. 4.35b, respectively. It is worth noting that Fig. 4.35a and Fig. 4.35b are representative of the average of seven samples (except for the case $L_G = 1.5\ \mu m$). In order to account for the statistics dispersion, the error bars were calculated as $\pm\ 3\sigma$ (standard deviation).

A L_G dependence is only shown in the case of ΔV_{TON} (Fig. 4.35a) because of the increasing electric field in the region under the anode contact when L_G is reduced (Fig. 4.36a). Moreover, due to lower R_{ON}, devices with shorter L_G feature a higher current density (Fig. 4.36b). As a result, the combined effect of large field and current density may cause a larger V_{TON} degradation.

From the evolution of V_{TON} reported in Fig. 4.35a, it is possible to distinguish two degradation phases characterized by different power slopes. The

reasons for this phenomenon have been discussed in section 4.5.2. In particular, the first degradation phase has been linked to the build-up of charge in pre-existing defects, whereas new defects are created during the second one. Moreover, it has been shown that, the change of the power slope is stress voltage-dependent.

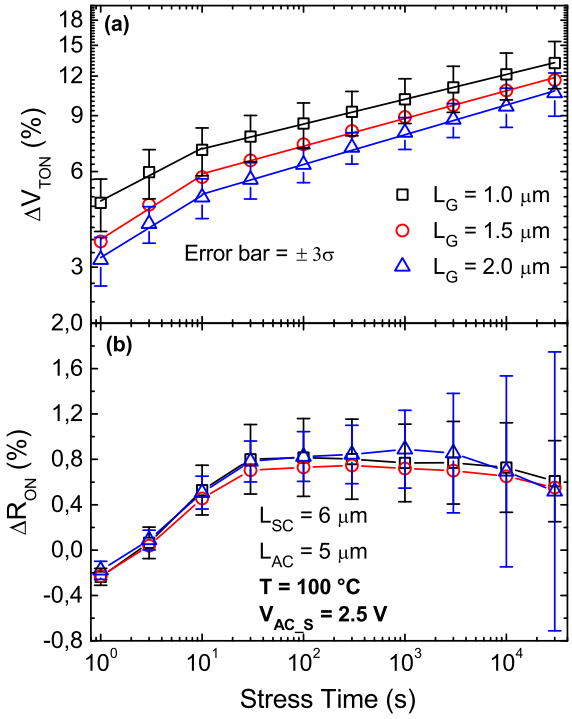

Figure 4.35: Turn-on voltage (a) and ON-resistance (b) degradations, due to ON-state stress, evaluated for different L_G at V_{AC_S} = 2.5 V and T = 100 °C. A L_G dependence is only shown in the case of ΔV_{TON}. In order to verify the statistical dispersion of the measurements, and to prove a good degradation reproducibility, seven devices for each L_G (except $L_G = 1.5\ \mu m$), have been characterized. The error bars represent the standard deviation ($\pm\ 3\sigma$).

By referring to Fig. 4.35b the R_{ON} degradation is limited (< 0.8 %) because, as in the case of L_{SC} dependence, the longitudinal component of the electric field (cut 2 in Fig. 4.19) is lower than 7 kV/cm since a low voltage is applied on the anode (V_{AC_S} = 2.5 V). Consequently, due to small R_{ON} shift, the amount of degradation can be affected by different sources of error possibly induced by experimental set-up, measurement technique, device variability, etc. In fact, by observing Fig. 4.35b, large error bars are shown compared to the measured expected value.

As a result, for the adopted stress conditions, the R_{ON} degradation is

not well reproducible and it is therefore impossible to identify the underlying physical mechanism. However, by deeply investigate the R_{ON} degradation, it has been shown in section 4.5.4 that: i) the ON-resistance degradation is linked to the longitudinal electric field occurring in the GaN channel (GET and access region); ii) this latter has to be higher than ≈ 7 kV/cm in order to achieve a significant ΔR_{ON} (≈ 5 % after $3 \cdot 10^4$ s of stress at T = 150 °C); iii) the corresponding defects could be associated to nitrogen antisites in the gallium nitride (GaN).

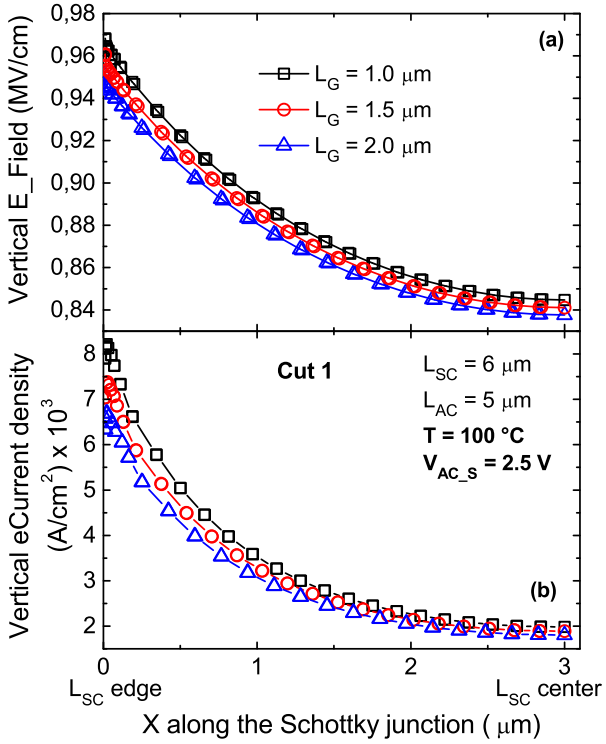

Figure 4.36: Vertical electric field (a) and electron current density (b) under the Schottky contact related to the stress condition of Fig. 4.35. The combined effect of higher electric field and current density, confirms the larger V_{TON} degradation in shorter devices, as reported in Fig. 4.35a.

In conclusion, the effects of the edge termination length have been investigated, highlighting its importance to get a good trade-off between performance and reliability to ON-state stress. In particular, diodes with longer L_G are more robust to ON-state degradation, mainly to V_{TON} shift; on the other hand, by increasing L_G lower ON-currents are obtained due to higher R_{ON}.

4.5.7 Conclusions

In this chapter, the degradation of the turn-on voltage, forward voltage and ON-resistance induced by ON-stress in AlGaN/GaN-on-Si GET-SBDs has been investigated.

By performing stress and recovery phases at different voltages and temperatures, it has been found that R_{ON} and V_{TON} degradations are triggered by different defects. In particular, thanks to combined experimental/simulation analyses, it has been reported that: i) the ΔV_{TON} is linked to the vertical electric field under the Schottky junction, possibly activating nitrogen vacancies defects in the AlGaN barrier; ii) the ΔR_{ON} is ascribed to longitudinal electric field occurring in the GaN channel, probably leading to the activation of nitrogen antisites defects; iii) the R_{ON} starts to significantly degrade only when a critical temperature-dependent (longitudinal) electric field is reached in the GaN channel.

In general, the vertical electric field is sensitive to all investigated geometry parameters; in fact, it increases with the reduction of L_{AC} and L_G leading to a larger V_{TON} degradation. Instead, in the case of L_{SC}, the anode stress bias plays an important role in the ΔV_{TON}. For stress voltages higher than about 4 V, the higher electric field peak occurring at the anode corner in the case of shorter devices, induces a larger turn-on voltage degradation. For stress biases lower than around 3 V, the vertical electric field under the anode contact and the current density tend to be uniform in the overall Schottky junction, causing a comparable or larger ΔV_{TON} in longer devices.

The role of the longitudinal electric field in R_{ON} degradation has been discussed with reference to the sensitivity to the length of the edge termination and to the anode-cathode spacing. In particular, by reducing L_G and L_{AC}, when the electric field is higher than about 7 kV/cm, a significant R_{ON} degradation occurs.

Finally, the irrelevant effect of the ON-state stress on the reverse leakage current has been shown. In particular, the trapping mechanisms occurring during forward stress do not contribute to reverse leakage degradation of the AlGaN/GaN-on-Si SBDs.

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Chapter 5

Gate Reliability of p-GaN power HEMTs

5.1 Introduction and State of the Art

Recently, GaN-based power transistors have received great attention in power electronics applications, due to the advantages of GaN over the conventional silicon [1] and to the possibility of manufacturing these devices at a comparable cost than their aging Si-based competitors [2]. In particular, the increasing demand for power switching applications, requiring normally-off devices for safety, power consumption and cost reasons [3], pushes the interest in developing and manufacturing enhancement-mode GaN-on-Si power transistors.

In the last years, different approaches, designed to fabricate normally-off high electron mobility transistors (HEMTs), have been proposed:

- MIS- and MOS-HEMTs based on a deep barrier recess under the gate region [4]-[10];
- fluorine plasma ion implantation into the AlGaN or GaN aimed at modulating the local potential under the gate, thus depleting the two dimensional electron gas (2DEG) in the channel [11], [12];
- introducing a p-type gate (p-GaN or p-AlGaN) able to pull the conduction band of the gallium nitride (GaN) in the channel up and, consequently, opposing to the formation of the 2DEG [13]-[16].

According to a recent comparison of different enhancement-mode architectures [17], the p-GaN solution seems to represent a promising technology because of the good trade-off between reliability and cost. In particular, by avoiding the deposition of an oxide/insulator layer (as in the case of MIS-/MOS-HEMT), the trapping-related degradation mechanisms (e.g. PBTI), caused by the defects at the GaN/insulator interface and/or in the bulk insulator, are strongly reduced [18]. Moreover, the adoption of standard silicon

manufacturing technology and facilities ensures a low process cost. However, relatively few data on trapping effects affecting the gate reliability of HEMTs with p-type gate are available in literature [19]-[21].

In [19] the breakdown phenomenon has been investigated and explained by avalanche multiplication in the space charge region of the Schottky metal/p-GaN junction, whereas in [20], the time dependence of the gate leakage current degradation was found to be consistent with a defect percolation process. Finally, Rossetto et al. [21], by combining experimental and simulation analyses, confirmed that the gate reliability of the p-GaN HEMTs is affected by the degradation originated from the high electric field within the p-GaN layer. Moreover, it is suggested, without providing a specific model, that the initial gate leakage current and, thus, the initial defectiveness of the fresh device influence the time to failure.

In this chapter, the degradation mechanisms underneath the time-dependent breakdown occurring when a forward constant voltage is applied on the p-type gate of the GaN-based transistor are extensively investigated. In particular, an original empirical relationship between gate leakage and time to failure that guides device optimization is identified by means of extensive statistical characterization on a few hundred devices. Moreover, thanks to this approach it has been found that:

- during the forward constant voltage stress a threshold voltage (V_{TH}) degradation occurs;
- after the breakdown event, in addition to an increase of the gate leakage (I_G), an improvement of the trans-conductance (g_m) is noticeable;
- the increase of I_G is ascribed to the creation of a percolation path in the depletion region of the p-GaN layer (close to the metal interface), and the possibly responsible defects are suggested;
- the V_{TH} degradation is ascribed to defects located in the AlGaN barrier layer;
- the g_m improvement is correlated to the gate leakage increase and ascribed to the channel conductivity modulation in the region under the gate.

5.2 Device Structure and Measurement Technique

P-GaN gate HEMTs (Fig. 5.1), fabricated at imec using an Au-free CMOS-compatible process flow [22], with a nominal threshold voltage of $\approx$ 2.1 V, are considered in this study. The epitaxial structure, is grown on 8-inch <111> silicon substrate by means of MOCVD and features a stack of: 200 nm-thick *AlN* nucleation layer on top of the Si substrate, followed by 3000 nm-thick

AlGaN buffer, 300 nm-thick *GaN* channel, 15 nm-thick $Al_{25}Ga_{75}N$ barrier, 70 nm-thick Mg-doped $p-GaN$, and 100 nm-thick TiN gate metal evaporated on top of the p-GaN in order to form a Schottky contact able to reduce the gate leakage current. A selective etch of the p-GaN layer is performed in the access regions stopping on the AlGaN layer and subsequently a SiN passivation layer is deposited. Finally, Au-free source and drain ohmic contacts are realized. The devices under test (DUT) feature a symmetric structure with a gate length (L_G) of 0.8 μm, gate-source/drain spacing length ($L_{GD} = L_{GS}$) of 0.85 μm, and gate width of 500 μm.

On-wafer characterization has been performed by means of Keithley 26xx Source Measure Units. During the stress phase a constant voltage (V_G) was applied on the gate contact while short-circuiting drain and source with the substrate. In this phase, the gate leakage current was continuously monitored until reaching 1 mA/mm, the current level chosen to identify the breakdown condition. Before and after the stress phase, a full I_DV_G transfer characteristic was measured in order to monitor the gate leakage (I_G), threshold voltage (V_{TH}), drain-source resistance (R_{DS}) and trans-conductance (g_m). Finally, the recovery was monitored by applying 0 V on all device contacts and periodically analyzing I_G, V_{TH}, R_{DS} and g_m.

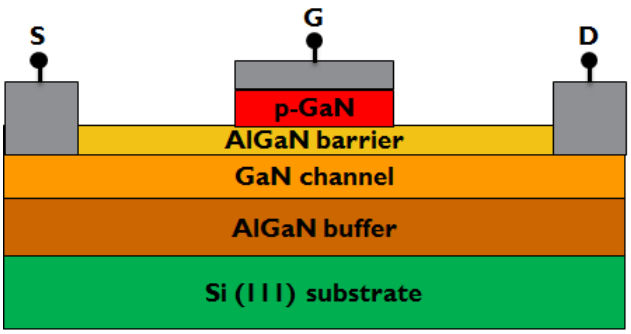

Figure 5.1: Schematic of the p-GaN/AlGaN/GaN-on-Si HEMTs (not in scale). The AlN nucleation layer between the AlGaN buffer and the Si substrate, and the SiN passivation layer are not shown.

5.3 Results and Discussion

Fig. 5.2 shows the gate current, monitored during the stress phase, of different devices biased with a gate voltage of 9.5 V at 25 °C. Two set of devices have been selected, characterized by different I_G levels. By observing Fig. 5.2, it is possible to note that: i) the higher the initial gate leakage current (I_G) (beginning of the stress), the shorter is the time to failure (TTF); ii) before the breakdown event, a noisy phase is only exhibited by the devices featuring a

lower I_G (set B in Fig. 5.2). In analogy to the case of CMOS FETs, this latter phenomenon may be ascribed to creation of defects forming a percolation path [23]-[26]. The higher initial gate leakage (set A in Fig. 5.2) can be related to a higher device defectiveness in fresh condition. As a result, with a higher number of pre-existing defects (higher initial gate leakage) the formation of the percolation path will only require the creation of a small number of additional defects and thus the noisy effect on the gate leakage is strongly reduced and TTF is significantly shorter. Larger defect creation, hence larger noisy behavior, occurs before breakdown in the case of devices featuring a low initial gate leakage (set B in Fig. 5.2).

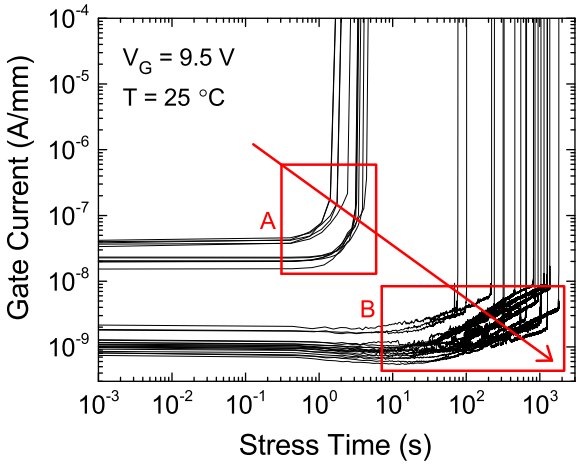

Figure 5.2: Gate current monitored during the constant stress at $V_G = 9.5$ V and T = 25 °C. It is possible to note a correlation between initial gate leakage current (I_G) and time to failure (TTF). The higher is I_G, the shorter is TTF.

The relationship between initial gate leakage (I_G), monitored at the start of the stress, and time to failure (TTF) is shown in in Fig. 5.3. It is worth noting that a statistical analysis has been performed in order to increase the accuracy of the analysis. In particular, for the case $V_G = 9.5$ V, more than 150 devices within a single wafer have been characterized at room temperature. While in [21] the stress gate voltage was modified in order to control gate current, in this case, in order to specifically highlight the link between TTF and I_G, the analysis has been performed at fixed applied voltage for devices featuring different levels of gate leakage.

The relationship between mean time to failure (MTTF) and initial I_G is well modeled by the exponential law reported in in Fig. 5.3. Moreover, this dependence has been confirmed for different stress voltages (8.5, 9.0, and 9.5 V). Thanks to this approach, the trade-off between safe operating gate voltage for a given lifetime and leakage current, can be estimated.

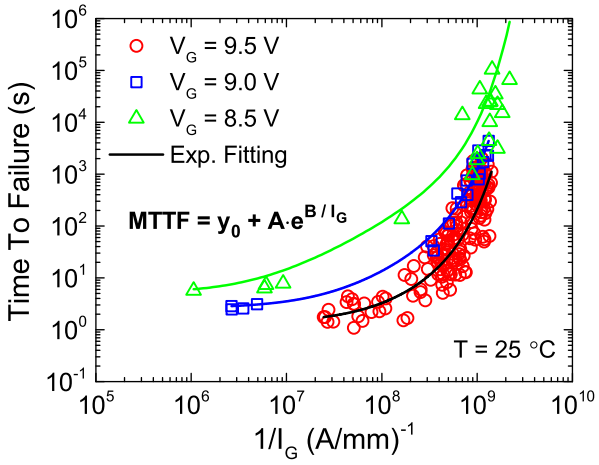

Figure 5.3: Correlation between the gate leakage current (I_G), monitored at the beginning of the stress, and the time to failure. An empirical model has been identified by means of a statistical analysis at room temperature and validated for three different stress conditions.

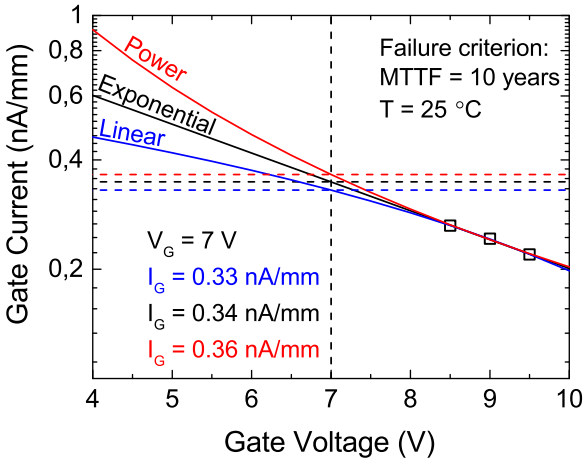

Figure 5.4: Relationship between gate voltage and initial gate leakage estimated by considering the empirical model of Fig. 5.3. In particular, by fixing the mean time to failure (10 years) and extrapolating the initial gate leakage at the corresponding gate voltage (Fig. 5.3), the maximum allowed initial I_G and operating voltage (V_G) enforcing the lifetime specification can be estimated.

Fig. 5.4 reports the initial gate current versus stress voltage as extrapolated from the exponential fits of the experimental data reported in in Fig. 5.3, by setting a 10 years' lifetime. In particular, based on the empirical model of in Fig. 5.3, the values of y_0, A and B parameters are extracted for each V_G condition. Then, the gate current (I_G) corresponding to the desired mean time

to failure (MTTF) (i.e. 10 years) is easily calculated for each V_G value.

Since only three data points (extrapolated from a statistical analysis) for initial I_G are reported in Fig. 5.4, different extrapolation laws could be suitable. However, considering that the desired maximum applicable gate voltage for p-GaN HEMT ranges around 7 V, it is possible to note as the uncertainty related to the choice of the fitting law is very small. As a result, by extrapolating such a dependence, it is estimated that in order to have a lifetime longer than 10 years at room temperature and a maximum applicable gate voltage of 7 V, the initial gate leakage current at $V_G = 7$ V has to be lower than approximately 0.3 nA/mm.

Additional tests show that the time to failure is Weibull distributed (Fig. 5.5) as commonly reported in the case of CMOS technology [27]-[29]. The main objective of these tests was the extrapolation of the lifetime. Therefore, three different stress biases at the temperature of 150 °C have been adopted. While previous papers, reported shape factors (β) below 1 [20], [21], in this case β is higher than 1.5. This suggests that extrinsic breakdown mechanisms related to presence of defects, are strongly reduced demonstrating a good process maturity and a good starting point for further device improvements.

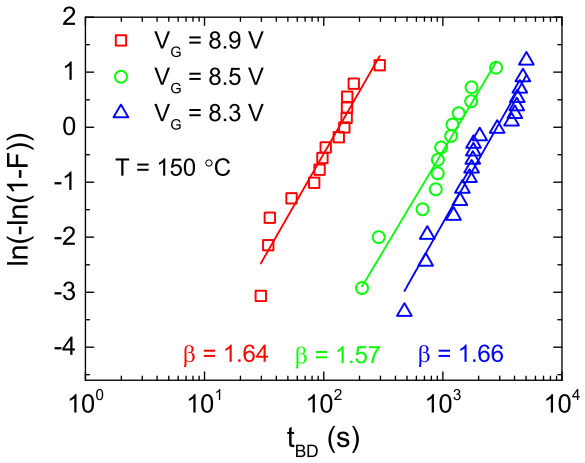

Figure 5.5: Weibull plot with different stress voltages at the temperature of 150 °C. The shape factor (β) higher than 1.5 suggests a reduced extrinsic breakdown, thus a good process maturity.

The analysis of the time to failure at different gate stress biases, performed by means of constant voltage-stress method, allowed to estimate the lifetime of the p-GaN/AlGaN/GaN HEMTs, as reported in in Fig. 5.6. By considering a lifetime of 10 years at a percentile of 1% and at a temperature of 150 °C, the maximum estimated applicable voltages is 5.6 V, which is a good achievement with respect to prior state of the art [20], [21]. However, further improvements

are needed in order to achieve this device reliability for large area devices.

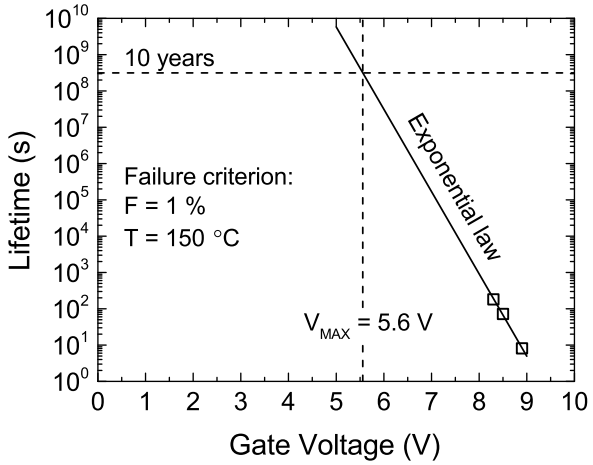

Figure 5.6: Lifetime extrapolation. By choosing the 1% of failure rate in 10 years at the temperature of 150 °C, the maximum applicable voltage, considering a device gate area of 400 μm^2, is 5.6 V. This is a good achievement considering the present state of the art. However, further improvements are required in order to have similar reliability for larger gate areas.

DC characterization has been performed before and after the gate failure aiming at monitoring and then at comparing the performance of the fresh and degraded samples. The transfer characteristics and the gate leakage current, in fresh and after the breakdown conditions, are reported in Fig. 5.7a and 5.7b, respectively. It is worth noting that Fig. 5.7 reports the results for a representative device. However, the same behavior has been observed for all tested devices.

By focusing on the curves measured after the breakdown and reported in Fig. 5.7 (red curves), it is possible to notice: i) an increase of the gate leakage current (b), ii) an improvement of the transconductance (g_m) (a); iii) a good correlation between the increase of g_m and I_G (a and b).

The gate leakage increase and hence the breakdown phenomenon may be related to the creation of a percolation path occurring in the depletion region of the p-GaN region of the Schottky junction, where the highest electric field occurs for positive gate bias. In order to confirm this hypothesis, the equivalent circuit of the p-GaN gate (Fig. 5.8a) may be considered. It consists of two back to back connected junctions. A Schottky diode formed by metal (TiN)/p-GaN (D1) and a PiN diode formed by p-GaN/AlGaN/GaN (D2). As a result, when a positive bias is applied on the gate, the diodes D1 and D2 are inversely and directly biased, respectively. Consequently, for high gate voltages the leakage current is limited by the Schottky diode (D1). This is supported by the voltage

drops across the diodes D1 and D2, evaluated analytically for a representative device by setting the reverse current of D1 and forward current of D2 equal to experimental gate leakage current [30], and reported in Fig. 5.8b.

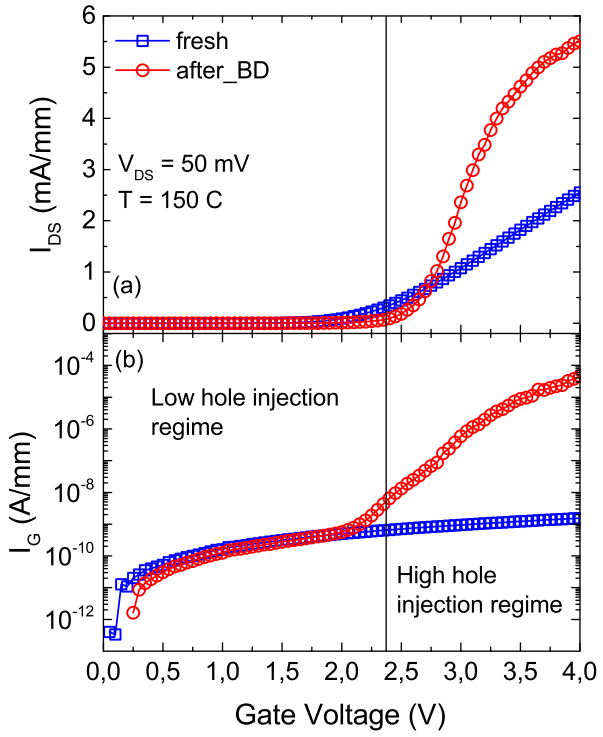

Figure 5.7: Transfer characteristics (a) and gate leakage currents (b) monitored in fresh devices and just after the breakdown event. After the failure it is possible to note an increase of I_G (b) due to creation of the percolation path in depletion region of the p-GaN layer and an improvement of g_m (a) linked to conductivity modulation mechanism triggered by high hole injection.

For V_G higher than $\approx$ 1.5 V the voltage drop across the AlGaN barrier (D2) is almost saturated and the whole additional applied gate voltage drops across the depletion region of the p-GaN layer (D1). As a result, defects induced by high fields form a percolation path in this latter region, leading to an increase of the gate leakage current (Fig. 5.7b).

By observing Fig. 5.7a, it is possible to note an improvement of the transconductance occurring after the breakdown event (circle/red curve). Moreover, a correlation with the increase of I_G (Fig. 5.7b) exists. According to [31], this can be ascribed to a conductivity modulation phenomenon. In [31] a GaN-based HEMT featuring a gate ohmic contact instead of a Schottky one is considered.

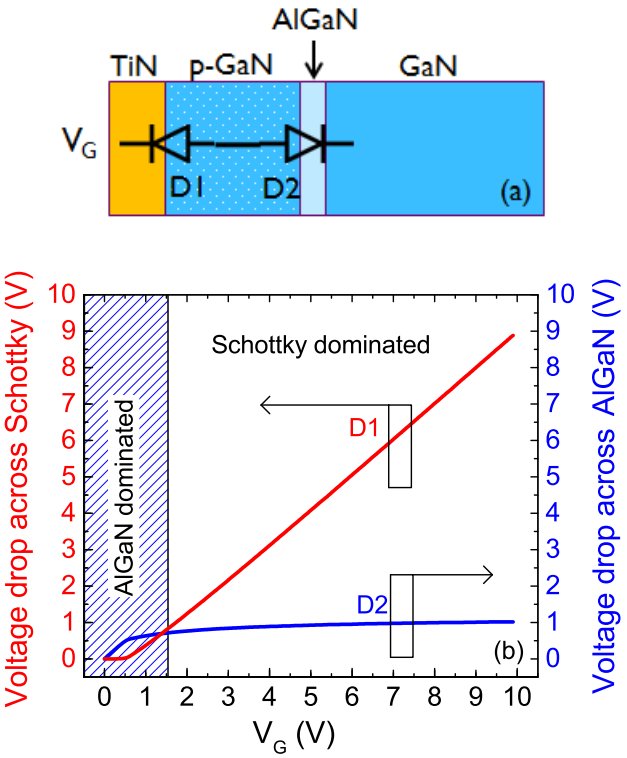

Figure 5.8: Schematic of the p-GaN gate (a) and evaluated diodes voltage drop (b). When a positive bias is applied on the gate, the diode D1 (Schottky) is in reversely biased, sustaining a high voltage and blocking reverse current, whereas the diode D2 (PiN) is in forward operation mode.

This new device principle utilizes hole-injection from the p-AlGaN to the AlGaN/GaN heterojunction, which simultaneously increases the electron density in the channel, resulting in a dramatic increase of the drain current owing to the associated conductivity modulation. In the case analyzed in this work, after the local Schottky barrier collapse caused by the opening of a percolation path, a similar mechanism occurs. In particular, it is thought that after the percolation path is activated, hole concentration increases in the AlGaN barrier. These holes can neutralize magnesium ions in the AlGaN barrier (Fig. 5.9b) increasing the 2DEG density in the channel. Notice that, the holes tunneling through or jumping above the AlGaN barrier, differently from electrons, are not confined at the AlGaN/GaN interface (Fig. 5.9b). The modulation of electron concentration by unconfined excess-hole tends to broaden the quantum well of the 2DEG, increasing its sheet concentration. As a result, the combined effect of neutralized magnesium ions into the AlGaN and the conductivity modulation induced by the holes injected in the channel reduces the channel resistance.

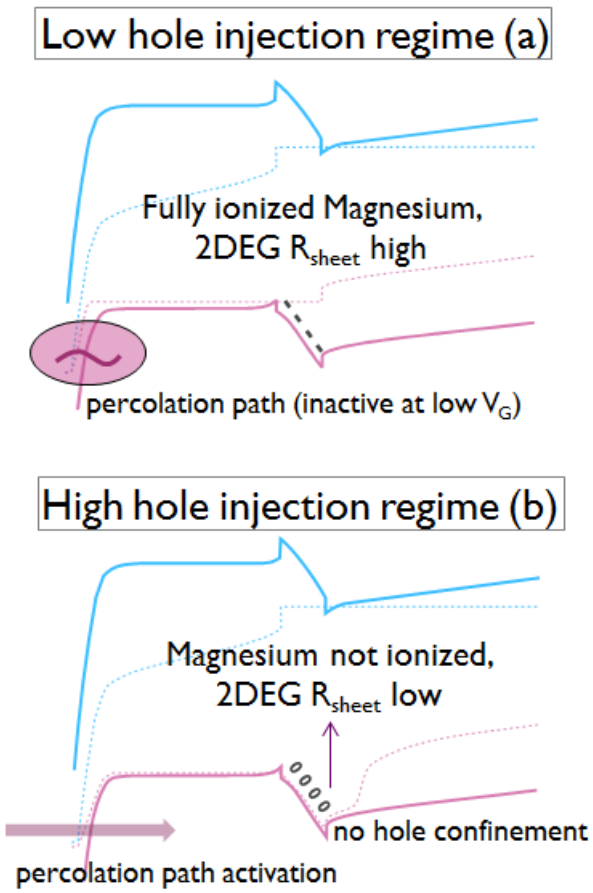

Figure 5.9: Band diagrams, considered under the gate region, in the case of low (a) (no percolation path) and high hole injection regime (b) (percolation path). The combined effect of magnesium ions neutralization in the AlGaN due to high hole injection, and the lack of hole confinement in the channel (b) can reduce the sheet resistance of the 2DEG improving g_m.

Additional understanding in the degradation physics was gained by implementing a percolation model in TCAD. The percolation path was implemented as a highly p-doped region, in accordance with the models which Uren et al. are using for their buffer simulations [32]. The simulation of the hole concentration with and without the percolation path are shown in Fig. 5.10. In the presence of a percolation path, a significant hole injection occurs into the channel where being unconfined causes a widening of the 2DEG quantum well, thus decreasing the 2DEG resistance. The depletion region below the 2DEG is indicated by a white line and is clearly extended towards the bottom for the case with percolation path. The simulated curves reported in Fig. 5.11 are qualitatively similar to the experimental curves of Fig. 5.7.

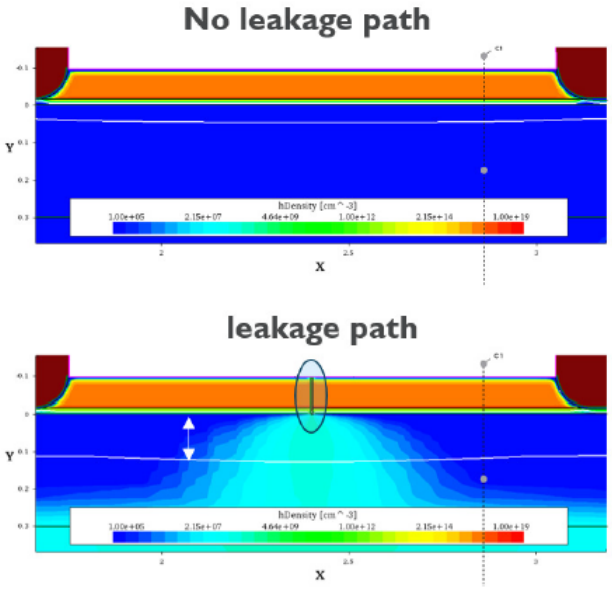

Figure 5.10: TCAD simulation of a p-GaN gate with and without p-type percolation path.

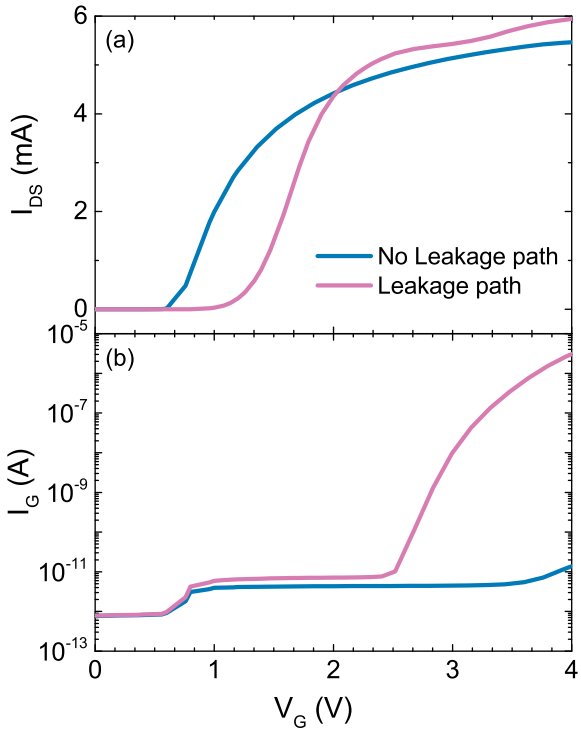

Figure 5.11: Simulated transfer characteristics (a) and gate leakage currents (b) monitored with and without p-type percolation path.

In order to further confirm the role played by trapping/detrapping mechanisms in the catastrophic gate failure, and the correlation between the gate leakage current and the transconductance, a recovery analysis has been performed and reported in Fig. 5.12. After the breakdown event, 0 V was applied on gate, source and drain at the temperature of 150 °C in order to allow a recovery phase. Gate leakage and transconductance were periodically monitored by measuring a full I_DV_G transfer characteristic from 0 V to 4 V with V_{DS} = 50 mV. By observing Fig. 5.12, the correlation between I_G and g_m is confirmed. It is thought that, during the recovery phase at T = 150 °C, some defect forming the percolation path are deactivated reducing the gate leakage (Fig. 5.12b). As a result, the smaller the hole injection, the smaller the conductivity modulation mechanism affecting the 2DEG resistance under the gate.

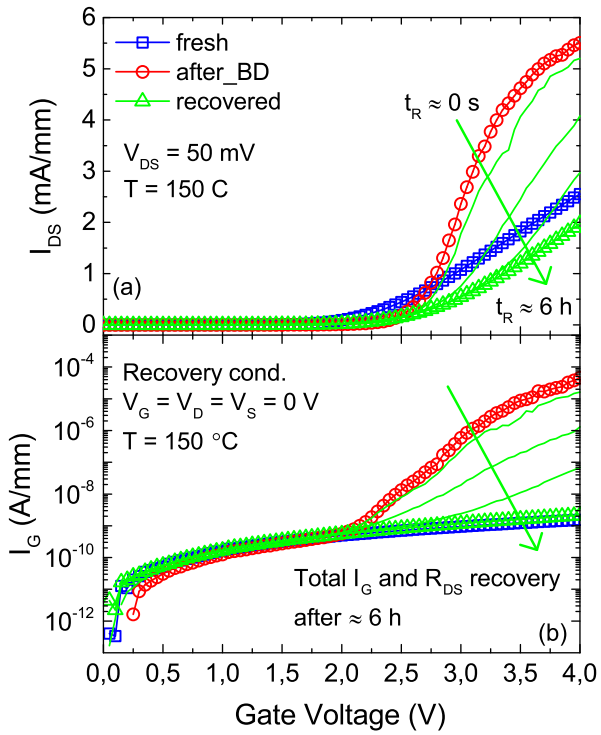

Figure 5.12: Transfer characteristics (a) and gate leakage currents (b) monitored in fresh condition, after the breakdown event, and during the recovery phase. In this latter, 0 V was applied on all device contacts at T = 150 °C. The correlation between g_m (a) and I_G (b) is further proved. It is worth noting that as in the case of Fig. 5.7 and 5.13, only a representative device is shown, but same behavior is reproducible for all tested devices.

However, although after ≈ 6 hours the gate leakage shows a complete

recovery for V_G up to 4 V, a permanent or slowly recoverable damage can be observed in Fig. 5.13. In particular, after a recovery of ≈ 22 hours at T = 150 °C, it is possible to note that the breakdown voltage of the recovered device (green) is lower than that of the fresh device (6 V and 10.5 V, respectively). As a result, part of the defects created during the stress and deactivated during the recovery can be easily re-activated when a high voltage is applied on the gate.

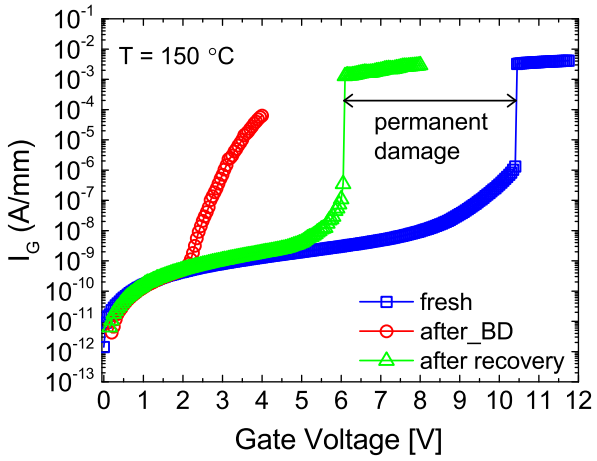

Figure 5.13: Device breakdown voltage characterized in fresh condition (blue), after the breakdown (red), and after 22 hours of recovery at T = 150 °C (green). Despite the full recovery shown for low voltage in Fig. 5.12, a permanent or slowly recoverable damage affects the device after the breakdown (V_{BD} recovered < V_{BD} fresh).

Finally, a temperature-dependent analysis aimed at understanding the possible kind of defects behind the trapping/detrapping mechanisms has been performed. In particular, by investigating the temperature dependence of the TTF, the nature of the defects located in the p-GaN layer can be identified. It is worth noting that each data reported in Fig. 5.14 is representative of the average of ≈ 20 samples stressed at a given temperature. In order to account for the statistics dispersion due to device variability, the error bars were calculated as ± 3σ (σ = standard deviation).

The temperature dependence of the time to failure is reported in Fig. 5.14. From the Arrhenius plot an activation energy of 0.44 eV is estimated. By considering the database of the deep levels in GaN- and AlGaN-based devices (see [33]), traps having an activation energy of 0.44 eV can be related to oxygen impurities in the gallium nitride [34], meaning that for our structure these defects would be present in the p-GaN gate.

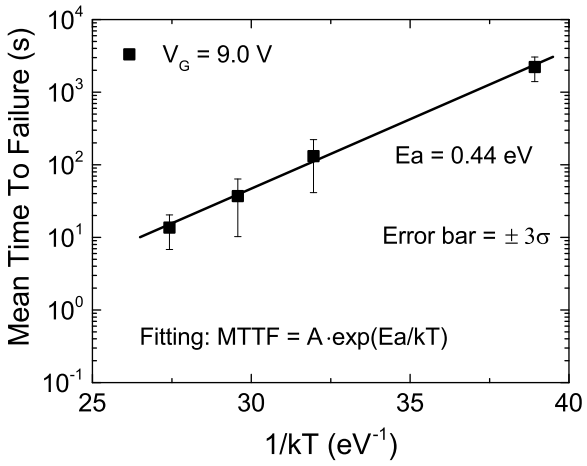

Figure 5.14: Arrhenius plot considering the mean time to failure (MTTF). The TTF has been extrapolated at the gate current of 1 mA/mm. By considering the database of the deep levels in GaN- and AlGaN-based devices [33, 34], the activation energy of ≈ 0.44 eV can be linked to the oxygen impurities in the gallium nitride.

5.4 Conclusions

In this chapter, the failure mechanisms induced by constant-voltage forward gate stress in GaN-on-Si power HEMTs with p-type gate have been investigated.

In particular, based on a statistical analysis, it has been found the following:

- the time to failure follows a Weibull distribution and it is function of the initial gate leakage. The higher is the gate leakage, the shorter is the time to failure. An empirical exponential model was proposed to take into account for this dependence;
- a maximum gate voltage of 5.6 V was estimated to ensure a 10 years' lifetime at a percentile of 1% and 150 °C;
- the breakdown mechanism is ascribed to the creation of the percolation path in the p-GaN layer (close the metal interface). When a high positive bias is applied on the gate, a large electric field (voltage drop) occurs in the depletion region of the p-GaN, creating defects with an activation energy of 0.44 eV;
- finally, the high hole injection occurring after the local Schottky barrier collapse, improves the transconductance due to a conductivity modulation phenomenon. In particular, the combined effect of the magnesium neutralization in the AlGaN barrier and the increase of hole concentration

in the channel, contribute to increase the 2DEG density and the mobility under the gate;

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Chapter 6

Conclusions

With the evolving of power electronics applications, there is an increasing need to fabricate switching mode semiconductor power devices that are compact, cheap and evermore efficient and reliable. This last feature is one of the main issues for power devices because it forces a trade-off between long lifetime, high performance and low cost. Consequently, extensive investigation and deep understanding of reliability issues are strongly required in order to keep up with the fast evolution of power electronics.

Chapter 1 presented the wide range of applications in which switching-mode power devices can be adopted, and analyzed the typical operating regimes representing the most critical conditions affecting the power device reliability, i.e. OFF-state, ON-state and SEMI ON-state.

This thesis aimed at studying, characterizing and modeling the trapping and de-trapping mechanisms, underneath the semiconductor power devices degradation, occurring during the ON-state operation mode. Although ON-state degradation received much less attention so far compared to OFF-state case, as demonstrated in this thesis, its impact on the power devices reliability is significant. This investigation has been carried out on technologies based on different semiconductors such as silicon and gallium nitride and different devices such as transistors and Schottky diodes, by means of accelerated life test methods combined with electro-thermal simulations, aimed at understanding the physical origins of the degradation.

The effects of degradation induced by Negative Bias Temperature Instability have been investigated in p-channel Si-based power U-MOSFETs, because this degradation mechanism appears as the most critical one occurring when transistor is in ON-state. Because of its vertical structure, moderate transverse electric fields and impact ionization related effects occur in the drift region. This latter, being far from the channel and hence from silicon/oxide interface, leads to negligible trapping mechanisms. On the other hand, the high/moderate gate bias required for ensuring a high drain current combined to a high temperature due to self-heating effects, causes thermally activated trapping mechanisms (i.e.

NBTI) in the gate region, affecting the device reliability. The contributions of the interface and bulk traps and their role on the degradation and recovery dynamics of the main figures of merit, have been analyzed and discussed. In particular, both oxide charge trapping and interface state generation occur during the stress, causing a degradation of threshold voltage and sub-threshold slope. On the other hand, the recovery mechanism is mainly dominated by charge de-trapping from bulk oxide defects featuring an energy confined in the silicon bandgap (between 0.22 eV and 0.84 eV from silicon valence band) and a distance from SiO_2/Si interface ranging between 2.24 and 3.04 nm.

Degradation mechanisms induced by ON-state stress have been also investigated in GaN-based Schottky barrier diodes (SBDs) and high electron mobility transistors (HEMTs). During ON-state stress, both devices are subject to high current levels, hence self-heating effects play an important role on the device performance and reliability limitations. Unfortunately, being GaN-based devices grown on foreign substrates with different thermal expansions coefficients and large lattice mismatch, an additional transition layer aimed at avoiding the formation of cracks in the GaN heterostructure is needed. This latter, in addition to structure vertical breakdown issues, implies a temperature increase due to the low thermal conductivity of the transition layer stack. In order to model this effect, a physical model accounting for the temperature dependence of the thermal boundary resistance (TBR) associated to the transition stack, has been implemented in the Sentaurus TCAD simulator in order to realistically model self-heating effects. In particular, it has been shown that, not including the TBR contributions, leads to an underestimation of the device channel/junction temperature by 25/30 %, resulting in an inaccurate estimation of the device performance and reliability.

A combined experimental/simulation analysis has been performed in order to understand the degradation induced in GaN-based Schottky barrier diodes (SBDs) by the combined effect of moderate electric fields and high temperature during ON-state stress. In particular, by analyzing the geometry dependence of the device degradation it has been reported that: the turn-on voltage degradation is linked to the vertical electric field under the Schottky junction, possibly activating nitrogen vacancies defects in the AlGaN barrier; the ON-resistance degradation is ascribed to longitudinal electric field occurring in the GaN channel, probably leading to the activation of nitrogen antisites defects; the R_{ON} starts to significantly degrade only when a critical temperature-dependent (longitudinal) electric field (or current level) is reached in the GaN channel.

Finally, the time-dependent breakdown, induced by forward gate stress in GaN-based power HEMTs with p-type gate, has been analyzed because the introduction of a p-type layer above the AlGaN barrier, aimed at realizing an enhancement-mode transistor, leads to undesired trapping mechanisms inducing a premature gate failure. The mechanisms underlying the gate breakdown

and its effects on the device performance have been investigated by adopting different stress conditions, analyzing the influence of the temperature, and investigating the activation energy of the traps. In particular, the breakdown mechanism has been ascribed to the creation of the percolation path in the p-GaN layer close the metal interface. When a high positive bias is applied on the gate, a large electric field (voltage drop) occurs in the depletion region of the p-GaN, creating defects with an activation energy of 0.44 eV. Moreover, an original empirical model, representing the relationship between gate leakage current and time to failure, has been proposed.