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NANO-POWER INTEGRATED CIRCUITS FOR ENERGY HARVESTING

Tesi di dottorato di
MICHELE DINI

Coordinatore Dottorato:

Prof. **CLAUDIO FIEGNA**

Relatori:

Prof. **ALDO ROMANI**
Prof. **MARCO TARTAGNI**

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Abstract

The energy harvesting research field has grown considerably in the last decade due to increasing interests in energy autonomous sensing systems, which require smart and efficient interfaces for extracting power from energy source and power management (PM) circuits. This thesis investigates the design trade-offs for minimizing the intrinsic power of PM circuits, in order to allow operation with very weak energy sources. For validation purposes, three different integrated power converter and PM circuits for energy harvesting applications are presented. They have been designed for nano-power operations and single-source converters can operate with input power lower than 1 μW.

The first IC is a buck-boost converter for piezoelectric transducers (PZ) implementing Synchronous Electrical Charge Extraction (SECE), a non-linear energy extraction technique. Moreover, Residual Charge Inversion technique is exploited for extracting energy from PZ with weak and irregular excitations (i.e. lower voltage), and the implemented PM policy, named Two-Way Energy Storage, considerably reduces the start-up time of the converter, improving the overall conversion efficiency.

The second proposed IC is a general-purpose buck-boost converter for low-voltage DC energy sources, up to 2.5 V. An ultra-low-power MPPT circuit has been designed in order to track variations of source power. Furthermore, a capacitive boost circuit has been included, allowing the converter start-up from a source voltage V_{DC0} = 223 mV. A nano-power programmable linear regulator is also included in order to provide a stable voltage to the load.

The third IC implements an heterogeneous multisource buck-boost converter. It provides up to 9 independent input channels, of which 5 are specific for PZ (with SECE) and 4 for DC energy sources with MPPT. The inductor is shared among channels and an arbiter, designed with asynchronous logic to reduce the energy consumption, avoids simultaneous access to the buck-boost core, with a dynamic schedule based on source priority.

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Chapter 1
Introduction

1.1 Energy Harvesting

In the last decade, the research interest in the energy harvesting field has grown considerably. Researches and industries are working on technologies able to supply micro-systems and sensing devices from environmental energy, thus enabling life extension of batteries. Another important aspect is the possibility of designing self-powered battery-less circuits, such for example the SSHI interface in [1] or the SECE circuit in [2], consuming only few μA and exploiting vibrational energy harvesting. This aim is particularly attracting, since replacing or recharging batteries is often problematic, if possible at all. The most frequently envisaged applications include monitoring of physiological parameters [3], long-term environmental sensing [4], structural health monitoring [5],[6], and industrial automation [7]. At the present time, most portable devices rely on electrochemical cells, and the potential of energy harvesting is still far from being fully deployed. One of the main hurdles is the difficulty of achieving a positive power budget on the energy harvesting interface, especially in size-constrained systems. Since energy transducers and materials deliver limited power densities down to few $\mu W/cm^2$ [8], the available power is reduced as system geometries shrink.

On the other hand, the baseline system consumption is set by the intrinsic consumption of the power converter and by the stand-by consumption of application circuits. In fact, in order to harvest as much energy as possible, the power converter should always be enabled. Disengaging from typical battery constraints (e.g. charging, leakage, temperature limitations, degradation over time, replacement) can be the starting point for self-powered pervasive sensing and monitoring applications. Electrical charge, and thus energy, is usually stored on low-leakage capacitors sized according to the application and the actual load requirements. In many targeted

applications of wireless sensor networks this constraint requires the use of supercapacitors [9], fostered by significant advances towards the reduction of geometries [10] and leakage currents [11]. On the other hand, the use of large capacitances in resonant power converters such as the previously mentioned ones, combined with the further constraint of designing micro-power control circuits with limited operating frequencies and bandwidths, may lead to low electrical quality factors, as it will be pointed out later on.

Recently, several integrated power converters for energy harvesting [12]–[15] have been proposed with power consumption in the order of hundreds of nW. Silicon implementation of converters allows, besides a smaller footprint and more complex and fully customizable architectures, a reduction of power of at least an order of magnitude with respect to optimized discrete components realizations [16]. Indeed, specific energy aware circuital design techniques, converter topology and silicon implementation allow the exploitation of ultra-low power sources with a positive output energy budget. The use of such sources, and of the associated power levels, would be prevented by a design using discrete components and the harvesting effectiveness is likely to be compromised.

A growing effort is also oriented to the miniaturization of transducers, key aspect for unobtrusive applications [17]. This means that energy harvesting systems and applications have to deal with very limited power levels, since optimized electro-mechanical designs with macro-scale transducers yield power densities as low as 10-100 μW/cm3 in many practical cases [8]. In addition, the current trend is to further shrink down transducers with MEMS fabrication processes [18], [19], with available power levels down to few μW. For this reason, a special care has to be put in designing efficient electrical interfaces for power conversion and energy storage with very low intrinsic consumption and power losses. Another possibility is offered by the use of microelectronic substrates: on-chip photovoltaic generation with integrated photodiodes [20][21]. In this case, a power converter circuit should manage source voltages as low as few hundreds mV and power levels up to tens of μW. A nanowire solar cells power battery charger with reconfigurable circuit power and clock speed has been presented in [22].

In order to go beyond the μW barrier, it becomes essential to exploit the modern microelectronic processes and their very low parasitics, along with the development of specific nano-power circuit design techniques. Many integrated power converters have been reported in literature which are tailored for different types of energy transducers. As an example, in [23][24] an integrated power management circuit for DC sources is reported to draw 330 nA with the ability of handling battery charging and cold start-up from input voltages down to 300 mV. Other reported solutions [25][26], with comparable power consumption, are able to deal with multiple types of transducers. In all the above cases, boost (or buck-boost) switching power conversion has been adopted, and FOCV MPPT was assumed to be a good compromise between converted and consumed power. An alternative buck switching converter with dynamic on-off time calibration and a regulated output voltage was reported to consume 217 nW [27].

However, differently from boost converters, buck topologies are not suitable for long-term energy accumulation. They are intrinsically limited in terms of voltage achievable on the output capacitor. Other types of power converter circuits based on inductor-less charge pumps [28] have also been proposed with comparable intrinsic consumption and activation voltages down to 150 mV [29]. On the other hand, the efficiency of charge pumps is typically lower than that of switching converters, and reaches values up to 72% in the latter case. The problem of activation voltage is of particular relevancy in thermoelectric energy harvesting, as the TEG voltage can be as low as some tens of mV. However, once the converter has started, e.g. with an application specific cold start circuit as in [23] or with the use of a charged battery as in [30], the input operating voltage can be considerably lowered as long as the power budget remains positive.

1.2 Energy Sources and Models

Several environmental energy sources have been widely investigated in the last decade as vibrations [31], light [32], heat [33] or electromagnetic radiation from communication equipment [34]. All these energy types can be successfully exploited

with appropriate transducers, e.g. piezoelectric transducers (PZs) for generating power from vibrations, photovoltaic (PV) cells for sunlight or artificial indoor light, thermoelectric generators (TEGs) for heat flows in wearable and industrial applications, rectifying antennas for incident electromagnetic waves (RF). The evaluated sources differs in their power density [35] and in their output characteristics. Two groups of sources have been identified, and each of them has its peculiar characteristics. Electrical models for such sources exist and are described in the following sections. For clarity, the sources have been divided into two categories: a) capacitive AC sources, e.g. a PZ, and b) DC sources, considering PV cells, RF rectennas, TEGs.

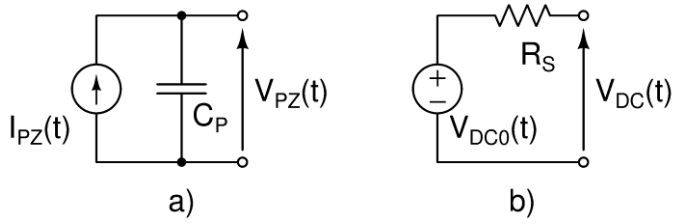

Fig. 1. Circuital model of a PZ (a) and of a DC source (b), e.g. a TEG.

The model used for a PZ is shown in Fig. 1 (a). It is a simplification of [36] in which the electro-mechanical circuit models direct and indirect piezoelectric effect. The model used in this thesis, shown Fig. 1 (a), does not account for indirect piezoelectric effect and thus the damping due to energy extraction is neglected. However, even if damping is neglected, it provides a simple and good representation of PZ. In case of single sinusoidal excitation of the PZ, the following equation holds, in which V_{P0} is the open circuit amplitude and f is the frequency of vibrations:

$$V_{PZ}(t) = V_{P0}\sin(2\pi f t). \tag{1.1}$$

$$P_{PZ,\max} = \frac{2}{T}\left(\frac{1}{2}C_P V_{P0}^2\right) = fC_P V_{P0}^2 \tag{1.2}$$

In order to provide a reference, input power $P_{PZ,max}$ available from the PZ, in case of sinusoidal excitation, can be expressed as the energy on C_P at each peak of V_{PZ} in a period T divided by T. The expression of $P_{PZ,max}$ is shown in (1.2).

The model used to represent a DC source is shown Fig. 1 (b). It is composed by a time variable DC voltage source V_{DC0} and a series resistance R_S. This model is suited for TEGs and, with some approximations, for RF rectennas [37]. The maximum power that can be extracted is expressed in (1.3) and the voltage V_{MPP} at maximum power point (MPP) is $V_{MPP} = V_{DC0}/2$. The model of PV cells is different but, as will be shown in the following chapters, they can be assimilated to DC sources. Even the MPP is different and (1.3) is not valid in this case.

$$P_{DC,\max} = \frac{1}{R_S}\left(\frac{V_{DC0}}{2}\right)^2 = \frac{V_{DC0}^2}{4R_S}. \tag{1.3}$$

1.3 Energy Harvesting Interfaces

1.3.1 Synchronous Electrical Charge Extraction

Several non-linear approaches have been developed for extracting energy from vibrations with piezoelectric transducers. Converters range from classical full wave rectifiers with an integrated boost converter [38] or with a switched capacitor converter [39] to complex waveform tracking algorithms [1], [14], [40]–[43]. Among the latter category, it is worth to mention synchronous electrical charge extraction (SECE) [16], [40]. The SECE converter is depicted in Fig. 2 (a), and is substantially a buck-boost converter exploiting non-linear techniques and resonant circuits. Among the advantages of SECE, it can be highlighted that: (a) the offset introduced by charge extraction increases the peak-to-peak voltage up to two times; (b) power conversion tracks, by definition, the input vibrations and generally outperforms passive interfaces, especially with irregular and weak vibrations; (c) differently from other approaches, such as passive interfaces [44], synchronized switch harvesting on inductor (SSHI) [1], active energy harvesting [43],[44] and single-supply pre-biasing

[47], the power source is kept disconnected from the load. This makes conversion efficiency quite constant in a wide range of conditions. The PZs have been modelled

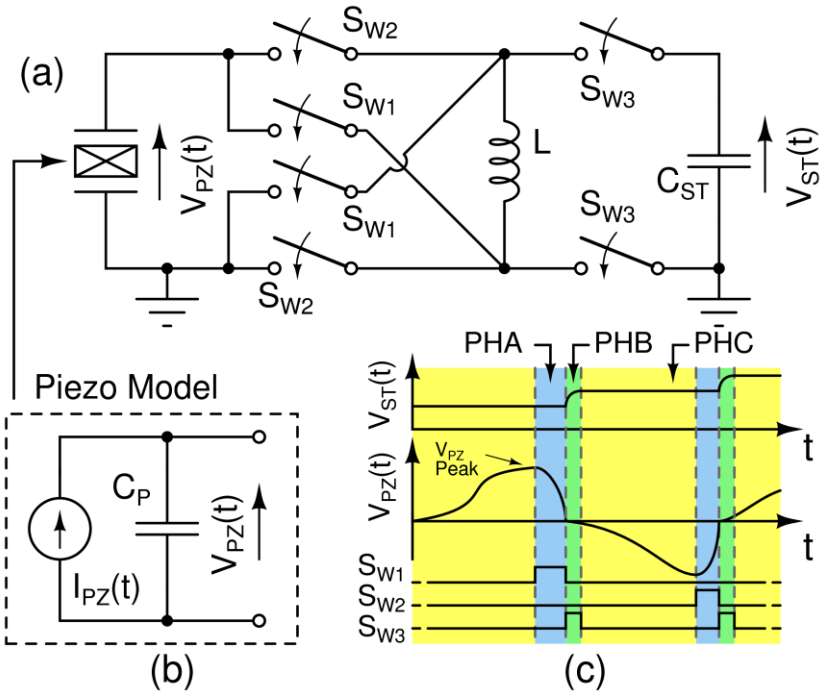

Fig. 2. (a) Circuit schematic for SECE from a PZ, (b) simplified PZ model valid for loosely coupled transducers, (c) sketch of typical waveforms, not to scale, in a SECE converter with energy extraction phases highlighted.

with the first-order capacitive model shown in Fig. 2 (b), which is a reasonable approximation in most applications. In general, when PZs have a high electro-mechanical coupling, a more complex representation of a PZ [2] should be adopted in order to account for the mechanical damping induced by the power converter. However, for the purposes of this work, the model of a PZ will be satisfactorily composed by the vibration driven current source $I_{PZ}(t)$ connected in parallel with the transducer capacitor C_P. With SECE, energy is extracted synchronously with each peak of $V_{PZ}(t)$ as shown in Fig. 2 (c). Three phases can be distinguished in an energy conversion cycle, namely PHA, PHB and PHC. The latter phase PHC, is an idle phase between two energy extraction cycles. In the first phase PHA, energy is transferred from C_P to the magnetic field in the inductor L. In the second phase PHB, energy is shifted from L into the storage capacitor C_{ST}. Since C_P is discharged at every activation, SECE applies a voltage offset on C_P at the beginning of each elongation.

This doubles the peak-to-peak voltage and boosts the available energy [16]. In addition, since the output node is never directly connected to the input PZ source, the SECE converter makes energy conversion efficiency from PZs independent from the values of V_{PZ} and V_{ST}. With respect to a bare passive diode interface, SECE requires an external inductor and an increase of design complexity. However, it will be shown that by exploiting IC technology, the impact of design complexity on the energy consumption of the control sub-system will be extremely weak.

1.3.2 DC-DC Converters

Many energy transducers have a DC output voltage, e.g. thermoelectric generators (TEGs), photovoltaic (PV) cells, RF rectennas. A maximum power point tracking (MPPT) circuit is mandatory in order to achieve a high conversion efficiency, which is essential when input power is very limited. Fig. 3 (a) depicts a buck-boost converter in an energy harvesting application storing energy in a capacitor C_{ST}, while Fig. 3 (b) shows a resistive model suitable to describe a generic DC source, in which R_S is the internal source resistance. Since the target applications have potentially extremely low input power levels, the buck-boost converter is expected to operate in discontinuous conduction mode. Although the accuracy of the MPPT circuit is important, the power required for the MPP computation should still be a negligible share of the available power, being the shortage of input energy one of the main constraints. In this manuscript, as will be shown in Chapter 4, a fractional open circuit voltage technique [23] (FOCV) has been chosen for MPPT. It is a trade-off between accuracy and power absorption, as the FOCV is an a priori technique not requiring on-the-fly computations. Accuracy relies on the assumption that the MPP is predictable and depends only on the open circuit voltage V_{DC0}, which is true for purely resistive sources as TEGs and an acceptable approximation for PV cells [48]–[50]. The MPP voltage is computed as $V_{MPP} = \beta V_{DC0}$, where β depends on the type of transducer: for TEGs and resistive DC sources $\beta = 0.5$, while for PV cells literature reports values ranging from 0.71 to 0.82 [48], [49], so that $\beta = 0.75$ was conservatively chosen in order to prevent operation of the PV cells in the region in which the output current is exponentially decreasing.

Fig. 3 (c) illustrates typical waveforms during energy extraction from a generic DC source. C_b is an energy buffer used to reduce the switching frequency of the converter as dynamic power consumption is proportional to switching frequency. V_{MPP} is kept as a reference and V_{DC} is kept into a $\pm\Delta V_{hystDC}$ range, which is the hysteresis of the comparator that detects the conditions for starting and stopping the energy extraction cycle. As in SECE conversion, three phases PHA, PHB and PHC can be distinguished: in PHA energy is transferred into L and V_{DC} then decreases; in PHB the energy is transferred from L to C_{ST}; PHC, which overlaps PHB, is an idle state in which the DC source charges C_b.

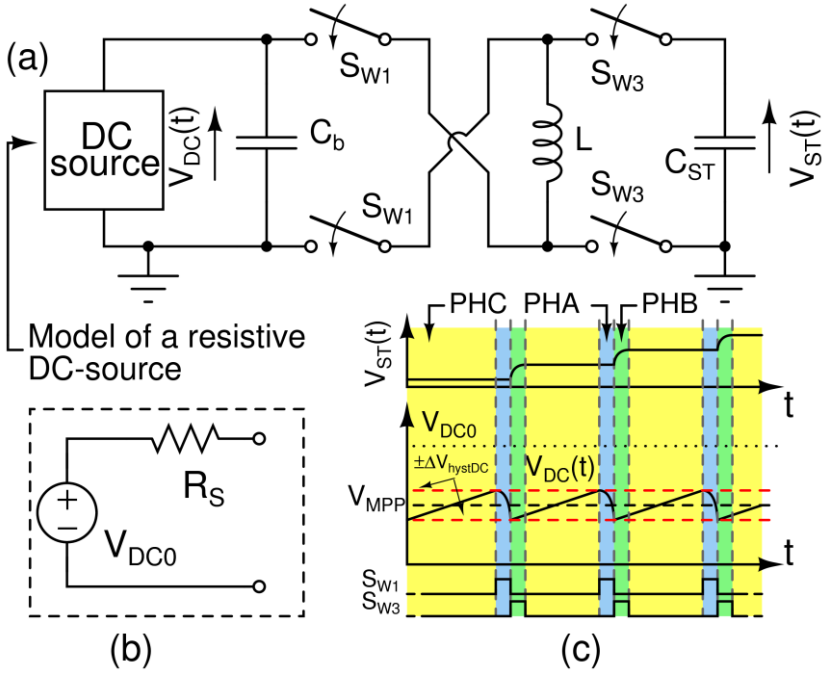

Fig. 3. (a) Circuit diagram for DC-source harvesting; (b) model of a generic resistive DC source; (c) sketch of typical waveforms, not to scale, in a DC harvesting converter, with energy extraction phases highlighted and MPPT references.

1.4 Multi-source Energy Harvesting

Typically, the available power in an energy harvesting scenario is in most cases constrained down to few μW or less [8], [51]. Hence, in order to achieve sufficient efficiency it is necessary to couple energy transducers with specific power conversion and management circuits [52]–[55], with very low power consumption. In this context, many energy conversion techniques and circuits have been developed in the last years with the main purpose of enabling autonomous wireless sensing applications.

One specific issue of energy harvesting, in addition to energy shortage, is the irregularity of energy flow. As an example, some energy sources are typically available only during specific parts of a day (e.g. sunlight) or undergo significant variations of intensity over time (e.g. vibrations from industrial machinery). When the involved power levels are very low and irregular, the combination of multiple energy sources of the same (e.g. only PZ) [16], [44], [56] or different types (e.g. TEGs and PV or other combinations) [57]–[60], is an effective solution for increasing the overall input power and the energetic reliability of the system. A multi-source multi-type approach for energy harvesting is also a typical scenario for wearable electronics applications [33], [51], [61] in which energy can be extracted from ambient light, body movements and heat, and RF energy from communication devices. Another area of interest for multi-source harvesting is the integration of both the converter and the transducer in the same package or on the same silicon die as shown in previous works with MEMS piezoelectric transducers [54], [62], micro fabricated thermoelectric devices [63] and solar cells [64].

Joining multiple energy flows is not a trivial task. The connection of N independent energy harvesters to a common output node V_{ST} through a unidirectional switch, e.g. a diode, is the simplest method [44], [57], [59], [60], also known as "power ORing" and illustrated in Fig. 4 (a). The main drawback of this topology is the "winner takes it all" nature: V_{ST} is generated by the energy harvester with the highest output voltage, excluding or limiting the contributes, in terms of power, from other harvesters. A more efficient method is to use a buck-boost converter to join N energy sources with their specific interface [16], [25] to the energy storage C_{ST} as in Fig. 4 (b). This approach allows each source, whatever its output voltage, to charge

C_{ST}. On the other hand, an additional interface circuit is needed to match the characteristics of both the source output and the converter input. Furthermore, a controller must ensure that no source can be ever connected with a low impedance path to any other source, wasting energy. The use of a single shared inductor in a multi-source converter for energy harvesting has been previously reported [16], [25], [56], [65]. The inductor can be time shared because the converter typically operates in discontinuous conduction mode (DCM) due to the very low involved power levels.

The low harvestable power requires converter circuitry to draw a small current for its operations for a matter of conversion efficiency. This is a non-trivial task with off-the-shelf ICs and discrete components due to their higher intrinsic parasitic capacitance and their higher power consumption with respect to an integrated optimized custom design. An integrated solution achieves at least a reduction of an order of magnitude in power consumption in comparison to advanced PCB implementations [16], [60] and achieves a considerable decrease of system size as well.

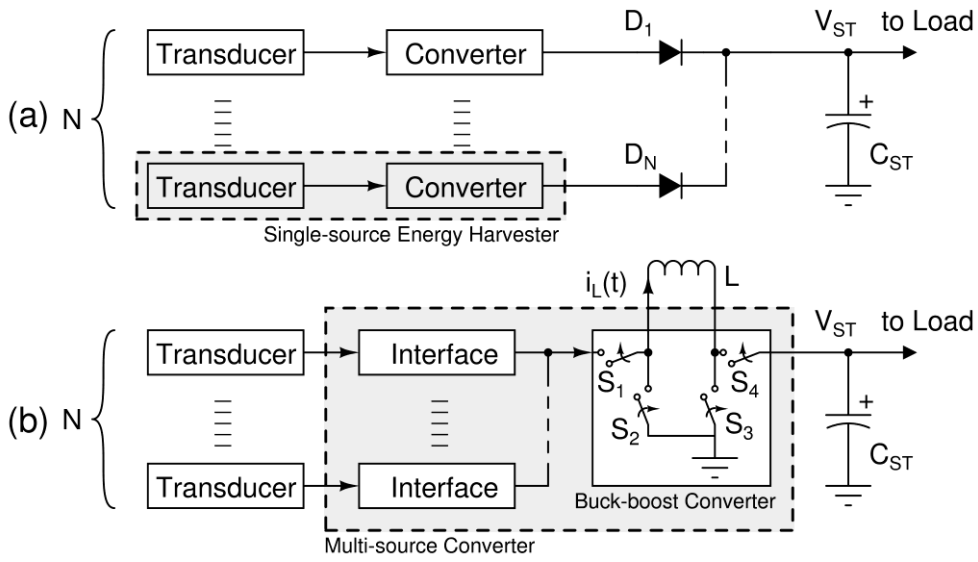

Fig. 4. (a) Basic method for combining energy harvesters output. (b) More efficient method for multi-source energy harvesting.

Differentiation allows to extract sufficient energy for system operation in a wider range of situations. As a first example, in [66] an airplane structural health monitoring system is powered by vibrations and thermal gradients, since batteries would not be allowed because of harsh environmental conditions. Such systems usually operate with a very low duty cycle [67], [68], with only some activations per hour or day while energy is slowly stored, for instance in low leakage super-capacitors. Another possibility for multi-source energy harvesting is the use of multiple differently sized piezoelectric transducers in order to exploit broadband vibrations [44] or different types of human movements [69]. Other attracting applications include environmental or structural monitoring [67], [68], wearable computing and sensing powered by human body [69] or electromagnetic waves [70], implantable bio-systems [71], [72], localization and positioning [73].

The design of a multisource power converter for energy harvesting, discussed in this thesis in Chapter 5, shows a set of circuital solutions and power reduction techniques which are suitable for ultra-low-power energy harvesting from multiple and heterogeneous sources. The focus is on the energy efficiency of the converter itself and on the achieved static consumption, which is considerably lower than in recent works on switching converters [21],[23] and active rectifiers [13], [15], [75]. Such value has been obtained with an energy aware design of each converter block. On the whole, such an optimized IC is suitable for applications in battery-less systems powered by weak and intermittent environmental power sources, which cannot individually sustain the electronic system under test.

1.5 Thesis Organization

As pointed in the previous sections, the design of efficient electrical interfaces for energy harvesting assumes a great importance as it is the basic block of an energy autonomous system. During the Ph. D. course, three different integrated converters has been designed and manufactured in a 0.32 μm BCD technology provided by STMicroelectronics. The design was aimed to improve the state-of-the-art of

converters for energy harvesting with a particular emphasis on circuital solutions addressed to the reduction of intrinsic consumption of the converter.

Chapter 2 presents the basic building blocks designed for the converters. Each of them has been designed in order reduce the static current into the tens of nA while preserving functionality and solve some of the problems associated to battery-less systems without a fixed and stable available voltage.

The first designed converter is presented in Chapter 3. It is a power converter for PZ which performs SECE, a non-linear energy extraction technique, with Two-Way Energy Storage (TWS) which allows for a faster start-up phase in comparison with standard power routing.. In addition, RCI is performed in order to improve the available input power and exploit weak vibrations (i.e. providing low voltage)

In Chapter 4 a converter for low voltage DC energy sources is described. The IC embeds a self-supplied buck-boost converter with peak efficiency of 77.1% and the same TWS policy presented in Chapter 3. Moreover, a dedicated start-up circuit in introduces in order to allow the start-up from source voltage as low as 223 mV and a low drop-out (LDO) regulator to provide a stable voltage to the load..

Finally, Chapter 5 describes the design and the experimental validation of a buck-boost converter for energy harvesting applications from multiple and heterogeneous energy sources. The converter features 9 independent channels and can handle from 1 up to 9 energy sources. The inductor is time-multiplexed among the active channels. Access conflicts are prevented by a logic arbiter which handles the requests and creates a queue in case of simultaneous requests. The static current is 431 nA, less than 48 nA per source, with a measured peak efficiency of 89.6%.

Chapter 2
Energy Aware Circuital Blocks

The typical input power available from energy sources is limited and ranges from some μW to some tens of μW. The electronic interface should provide an high conversion efficiency and a very low static consumption. Both this aspects are important and related each other. In case of irregular or intermittent energy sources, the static consumption minimization, in the range of tens of nA or less, is important. It prevents the waste of a consistent part of the previously harvested energy only for the interface quiescence.

For this reason, a set of energy aware circuital blocks has been developed as the building blocks of the proposed converters. The aim is the reduction of the static consumption of each block, compatibly with the requirement of the system in which they are used. In case the static consumption could not be limited to acceptable value, a dynamic power management policy has been adopted and energy hungry block are activated only for the minimum required time.

2.1 Bias generation and Under-Voltage Lock-Out

The generation of a stable nano-current reference is crucial for operations in the μW range. The left part of Fig. 5 shows the designed circuit diagram for the generation of I_{ref}, set to 16 nA. It is based on a classic supply independent current reference [76] but it is biased in the sub-threshold region and a cascode current mirror (M_{B1}, M_{B2}) has been added in order to increase the independence of I_{ref} with respect to the supply voltage V_{DD}. Current I_0 and I_{ref} are set by the resistor R_{BS} and their value can be expressed as follows:

$$I_{ref} = I_0 = \ln(\rho)\frac{V_T}{R_{BS}}, \tag{2.1}$$

where ρ is the ratio between the shape factors of M_{Br} and M_{B0} and V_T is the thermal voltage and can be obtained by equating the sub-threshold current expression of M_{Br} and M_{B0}. In this design R_{BS}=687 kΩ is an on-chip polysilicon resistor. The bias generator circuit outputs the voltage references V_{biasP} and V_{biasN} which are used by all analog sub-circuit in the IC. Distributing reference voltage instead of reference currents for biasing allows the reduction of quiescent current required by biasing circuits down to 48 nA.

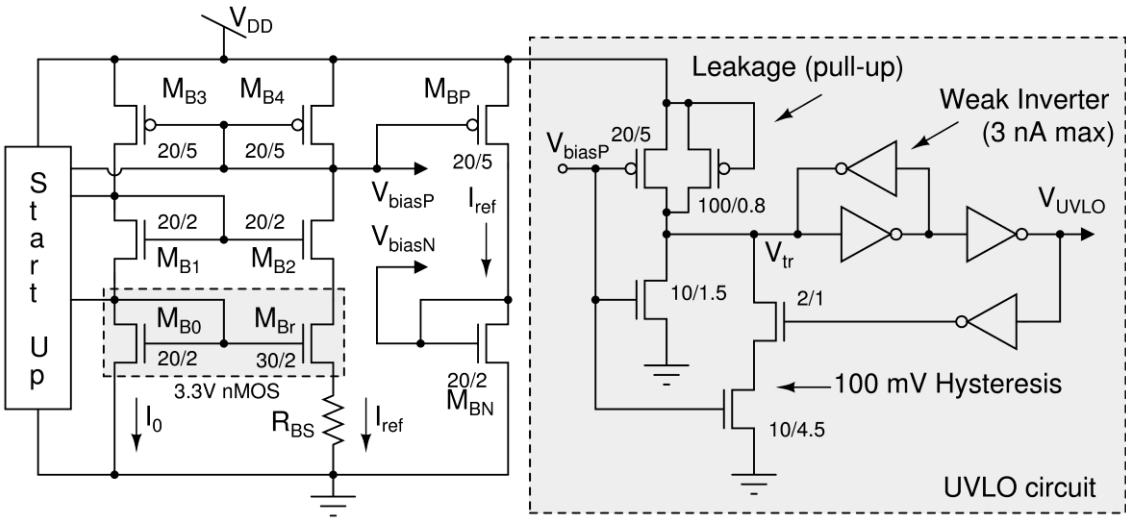

Fig. 5. Circuit diagram of the designed bias generation circuit (left) and of the UVLO circuit (right). The start-up block is used to prevent the undesired condition $I_0 = I_{ref} = 0$ A when V_{DD} rises. The start-up circuit does not draw any static current.

The UVLO circuit diagram is shown on the right of Fig. 5. An hysteresis of about 100 mV is provided in order to prevent switching around V_{DDmin} value. The UVLO circuit draws 16 nA. By changing the size of the two n-channel MOSFET with the gate connected to V_{biasP}, (for triggering at V_{DD} = 1.4 V the sizing is shown in Fig. 5) it is possible to change the value of V_{DD} at which the UVLO triggers. In the next chapters, different UVLO circuits will be shown. They keep the same basic structure as shown in Fig. 5, and only the sizing of the first stage is modified in order to change the triggering level (i.e. not at V_{DD} = 1.4 V).

2.2 Comparators

Four different nano-power comparators (circuit diagram shown in Fig. 6) with built-in hysteresis have been designed. They are all driven with the same tail current I_{bias}=I_{ref}=16 nA and they differ for the input common-mode V_{CM} voltage they can properly sense. Differently from other realizations [41], [74], [76], the inputs of comparators are placed on transistor gates in order to show a high impedance on the sensed nodes. Comparators (a) and (b) have nominal hysteresis V_{hyst} = 15 mV and (a) has been designed for sensing voltages up to the positive rail (V_{DD} +0.3 V, n-channel MOSFET input pair) whereas (b) can sense down to the negative rail (GND -0.3 V, p-channel MOSFET input pair). The same applies for comparators (c) and (d), used in DC interface circuits, which have hysteresis V_{hystDC} = 28 mV; furthermore, their tail current can be temporarily increased through a boost input signal (BoostC or $\overline{\text{BoostD}}$) of about 100 nA (exact values are shown in Table I) for reducing their propagation delay only when required.

$$V_{hyst} = nV_T \ln\left(\frac{W_{P3a}}{L_{P3a}}\frac{L_{P1a}}{W_{P1a}}\right) \tag{2.2}$$

The hysteresis amount, V_{hyst} or V_{hystDC}, can be obtained by solving (2.2), in which (W_{P3a}, L_{P3a}) and (W_{P1a}, L_{P1a}) are the width and the length of the transistors transistor M_{P3a} and M_{P1a} respectively (considering comparator (a) in Fig. 6). Moreover, V_T is the thermal voltage and n is the subthreshold slope parameter. Equation (2.2) has been derived in a similar fashion as shown in [77] and is valid for the MOSFETs biased in the sub-threshold region and not in strong inversion as in [77].

The comparators (a) and (b) do not have a dedicated boost input. They are used in the buck-boost converter core where a bias boost is provided at an higher level by directly increasing I_{bias} = I_{ref} = 16 nA to I_{bias} = 16I_{ref} = 256 nA.

The hysteresis voltage V_{hyst} is the input voltage difference necessary to balance, in comparator (a), the drain currents of M_{N1}a and M_{N2a}. Propagation delays obtained from simulations are reported in Table I for different bias conditions.

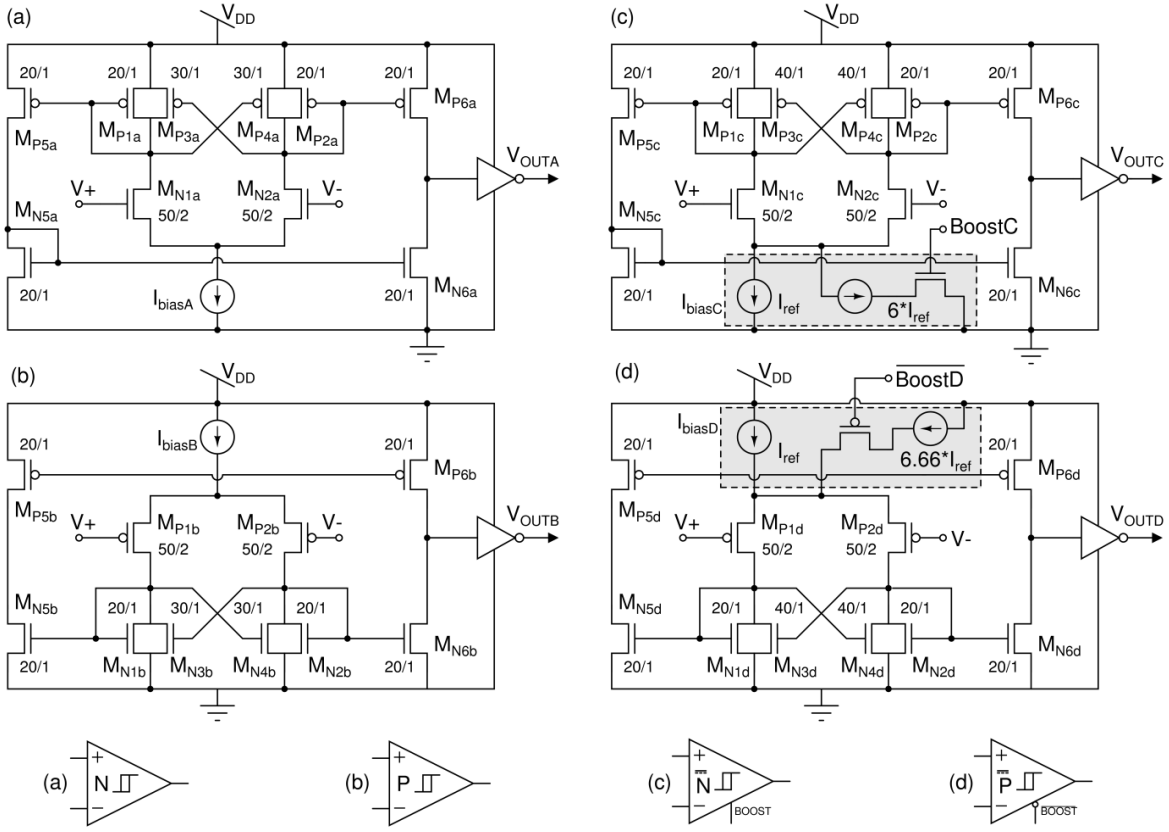

Fig. 6. Circuit diagram of the four designed comparators. (a) and (b) have V_{hyst} = 15 mV and allow signals up to V_{DD} and ground, respectively. (c) and (d) have V_{hystDC} = 28 mV, allow signals up to V_{DD} and ground, respectively, and have an actively tail current boost for t_{PD} reduction.

TABLE I. PROPAGATION DELAYS OBTAINED FROM SIMULATION[1] OF DESIGNED COMPARATORS WITH DIFFERENT BIASING CONDITIONS.

Comparator	t_{pdLH} **[µs]**	t_{pdHL} **[µs]**	**Biasing**
Standard N (a)	9.44	11.46	$I_{biasA}=I_{ref}$
Standard N (a)	0.74	0.76	$I_{biasA}=16*I_{ref}$
Standard P (b)	12.97	9.98	$I_{biasB}=I_{ref}$
Standard P (b)	0.86	0.78	$I_{biasA}=16*I_{ref}$
DC version N (c)	10.40	12.74	$I_{biasC}=I_{ref}$
DC version N (c)	1.34	2.02	$I_{biasC}=7*I_{ref}$
DC version P (d)	14.26	10.86	$I_{biasD}=I_{ref}$
DC version P (d)	1.59	1.19	$I_{biasD}=7.66*I_{ref}$

[1]Including parasitic capacitances, with T = 27 °C, V_{DD} =3 V, V_{CM} = V_{DD}/2, C_{load} = 500 f

2.3 Enhanced Negative Voltage Converter

The output voltage of a PZ is generally an AC signal with null average value requiring rectification. Negative voltage converters (NVC) have been already employed in this type of applications [43],[53] thanks to their low-drop out, which is due only to the on-resistance of MOSFETs. However, alike standard rectifiers, they have a minimum input voltage (i.e. roughly corresponding to $V_{GS,th}$), thus it is impossible to extract the whole charge on C_P. Moreover, an NVC is not able to force a current direction and cannot simply substitute a diode bridge. Fig. 7 shows the circuit diagram of the enhanced NVC (eNVC) circuit designed to overcome such limitation. Along a standard NVC core (M_{V0}-M_{V3}), four actively controlled switches (M_{Ve0}-M_{Ve3}) have been added. They are activated in pairs (by V_{AON} or V_{BON}) only

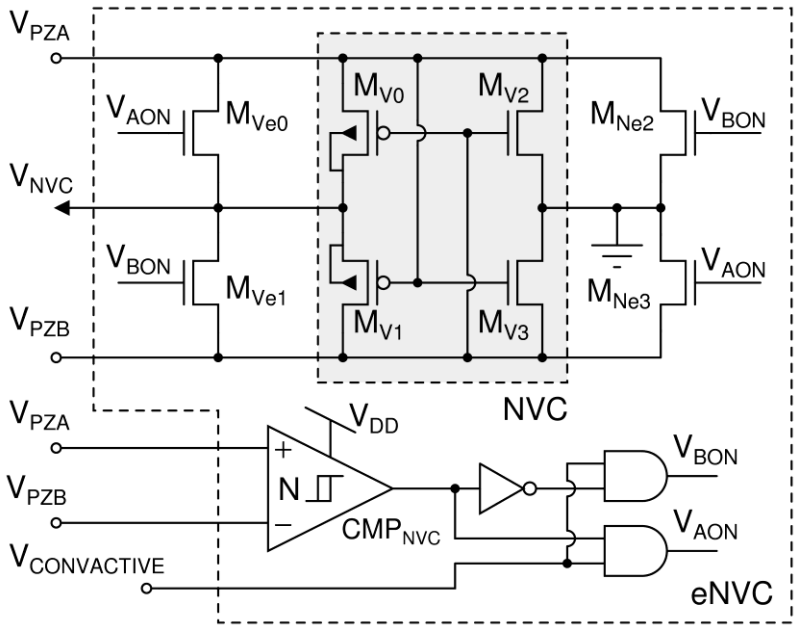

Fig. 7. Enhanced NVC circuit diagram.

during energy extraction phases ($V_{CONVACTIVE}$ signal is high) and allow the whole charge on C_P to be extracted (i.e. until V_{PZ}=0 V). The comparator CMP_{NVC} select which pair must be switched on by reading the polarity of V_{PZ} (V_{PZA} and V_{PZB}). The eNVC circuit draws 32 nA or 16 nA, depending on the output state of comparator

CMP_{NVC} and thus, as the AC voltage of a PZ has as many positive half-waves as negative ones, an average of 24 nA can be considered in a realistic scenario.

2.4 Higher Supply

As an autonomous system, the converter relies only on harvested energy. Then, no stable and regulated voltage is available. However, since the IC manages many sources with different voltage levels, several circuit blocks including the gate drivers of MOSFETs require to be supplied or driven with the highest possible voltage in order to operate properly. Thus, a very frequently used block is the Higher Supply (HS) circuit, depicted in Fig. 8. The output V_{HH} is selected as the higher voltage among V_{HA}, V_{HB} and, with a limited current of $12I_{ref}$, V_{DD}. Transistors M_{h1} and M_{h2} form a standard bulk-regulation circuit, whereas $M_{h3...5}$ (which are low V_{GSth} transistors) and the current generator have been added to improve the output voltage level for very similar input voltages.

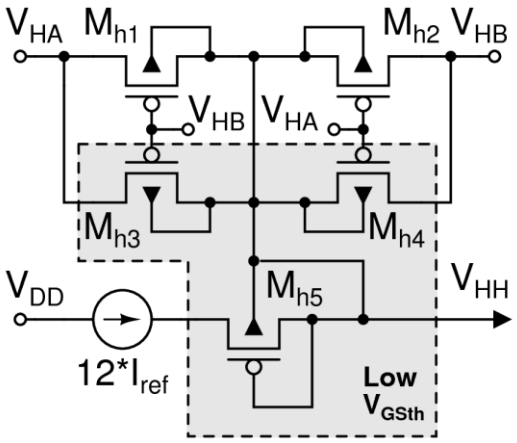

Fig. 8. Higher Supply circuit diagram.

Transistors M_{h3} and M_{h4}, which have a higher leakage current, have been sized with a trade-off between performance (i.e. V_{HH} voltage drop with respect to V_{HA} or V_{HB}) and leakage current in order to limit static current between V_{HA} and V_{HB} to few

nA in worst bias conditions. Fig. 9 shows the improvement brought by the added circuitry in the limitation of the voltage drop on V_{HH} for crossing inputs. Transistors M_{h5} and the current generator are mainly useful for analog circuitry requiring low current (i.e. comparators) on slowly variable signals (e.g. PZ voltage).

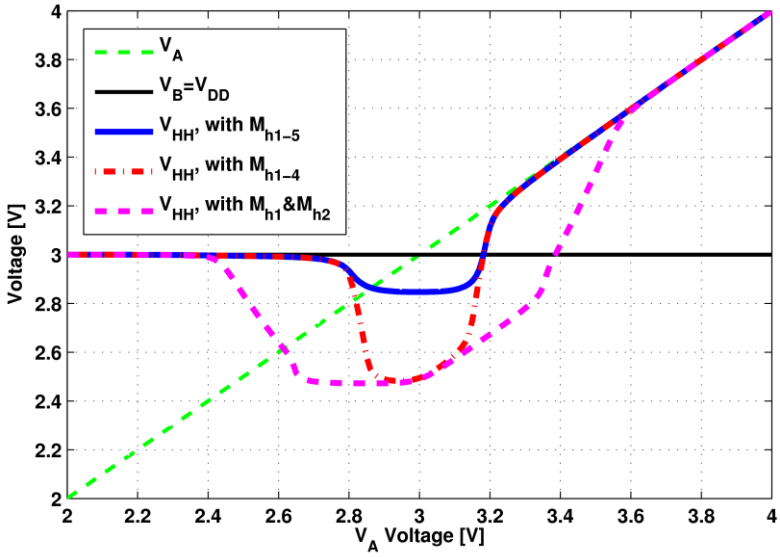

Fig. 9. Simulated output voltage V_{HH} of an HS circuit for V_A sweeping and $V_B = V_{DD} = 3$ V for several configurations.

2.5 Peak Detector

The SECE converter requires the tracking of $V_{PZ}(t)$ and the detection of maxima and minima in order to trigger energy extraction cycles. Fig. 10 shows the circuit diagram of the peak detector included in each PZ interface circuit. A design issue is the PZ voltage which can reach values significantly higher than V_{DD}. To overcome this issue, the supply voltage V_{HH} is selected as the highest between V_{NVC} and V_{DD} as described above. The first stage is composed by three diode connected transistors which produce V_{NVCds}, a down-shifted version of the input voltage V_{NVC} (i.e. the rectified version of V_{PZ}), and force it to be in the allowed common mode range (i.e. V_{HH}+0.3 V) of both the input pair M_{k1}-M_{k2} and the input pair of comparator $\mathrm{CMP_K}$.

The second stage generates V_{track} as a copy of V_{NVCds}. C_{track} can only be charged by M_{k6} and thus allows the comparator to detect a voltage maximum (peak) as soon as $V_{track}>V_{NVCds}+V_{hyst}$. The built-in comparator hysteresis increases the noise margin and prevents false triggering. The quiescent current drawn by the peak detector is 32 nA. Measurements showed that the circuit is able to track input signals up to 1 kHz which is a quite high frequency for macro-scale PZ and for typical vibrations in industrial or transportation environments [79]. In addition, it offers improved performance with respect to other discrete [16] and integrated implementations [80].

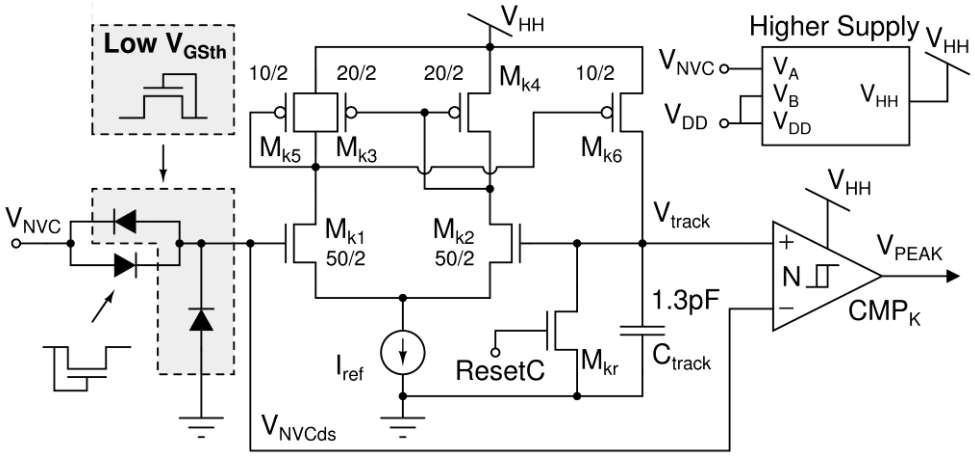

Fig. 10. Peak detector schematic circuit.

Chapter 3
Piezoelectric Energy Harvesting

The first presented interface is a power converter for piezoelectric energy harvesting. It implements a self-supplied nano-power SECE converter. Moreover, two major improvements with respect to standard SECE have been included. The first is Residual Charge Inversion (RCI) and is presented in Chapter 3.1. The RCI allows the increment of the available energy on the transducer capacitance by inverting the residual charge on C_P, which is due to the minimum operating voltage of the employed rectifier (i.e. a NVC in this case), after an energy extraction cycle. The second improvement is the use of a dual power routing topology. Of the two energy storage capacitors, one is for supplying the converter itself, and the second for the bulk energy storage (i.e. for providing power to the load). This power management policy has been named Two-Way Energy Storage (TWS) and is discussed in Chapter 3.2. The benefit of this policy is a reduction of the time spent by the converter in passive mode (i.e. a faster start-up time). As the converter is brought in active mode, SECE is performed, which is a far more efficient energy conversion process. In Chapter 3.3 the converter architecture is analysed, with particular emphasis on the power reduction strategies, and in Chapter 3.4 the experimental results on manufactured devices are presented and discussed in relation with the analysis performed in the previous sections of the chapter.

3.1 Residual Charge Injection

A careful design of the input interface is mandatory in order to achieve high efficiencies while extracting charge from piezoelectric transducers, especially when low voltages are involved. The more efficient this process is, the higher the duty cycle of operation of the final application, e.g. data acquisition and wireless transmissions, will be. In energy harvesting systems, energy should be collected as long as it is available from the environmental sources. For this reason, a buck-boost

topology is a suitable candidate as input stage. In fact, in passive rectifiers and step-down converters the output voltage cannot exceed that on the input whereas it is likely required to extract energy in the opposite situation. Among buck-boost topologies, piezoelectric transducers subject to weak and irregular vibrations are efficiently handled with SECE, which is also compatible with micro-power control circuits [2]. In self-powered implementations of SECE, since piezoelectric voltages often switch from negative to positive voltages, the difficulty of generating dual voltage supplies is usually overcome by using input rectifier stages, whose voltage drops, however, limit efficiency in case of low input voltages. Energy conversion, as mentioned in Section I and shown in Fig. 1, is activated on local maxima of the rectified voltage. Energy is first extracted from the piezoelectric capacitance C_P with a switched inductor L_I forming a L_I-C_P resonant circuit. Then, energy is transferred from L_I into a storage capacitor C_O by forming a second L_I-C_O resonant circuit. Since the L_I-C_O resonant circuit is never connected to the piezoelectric transducer, a measure of the capability of a SECE interface to extract power is given by the energy stored in the inductor at the end of the first phase.

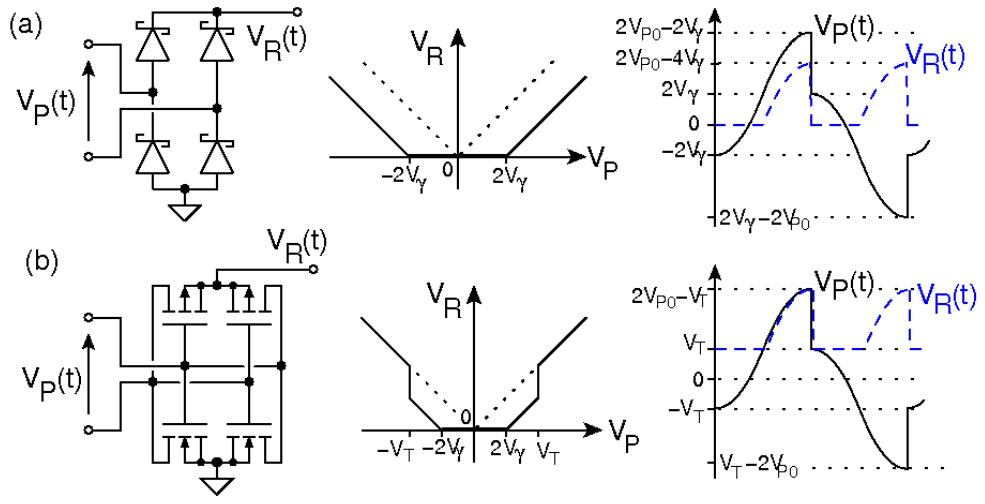

Fig. 11. Schematic, voltage transfer characteristic and transient behavior during SECE with: (a) BR; (b) NVC.

Let us suppose that $V_P(t) = V_{P0}\sin(2\pi ft)$ is the voltage generated across the transducer in open circuit, where f is the vibration frequency. If a full-wave bridge rectifier (BR) is adopted (Fig. 11a) as input interface, in case of conduction the rectified voltage is $V_R(t) = |V_P(t)| - 2V_\gamma$, where V_γ is the threshold voltage of a single diode and $V_R(t) \geq 0$. When SECE is activated on a voltage peak, the transducer is discharged through the rectifier and the inductor until $V_R(t) = 0$. Then, the rectifier turns off and a residual voltage $\pm 2V_\gamma$ is left on $V_P(t)$. From this condition, since a peak-to-peak elongation produces a voltage variation $2V_{P0}$ on the transducer, a maximum voltage $2(V_{P0} - V_\gamma)$ can be reached on $V_P(t)$.

If γ is defined as $\gamma = V_\gamma/V_{P0}$, with $0 < \gamma < 0.5$, the energy stored in L_1 at the end of the first phase can be computed by solving the differential equations of the L_1-C_P circuit, as demonstrated in [16]:

$$E_L^{(BR)} = 2C_P V_{P0}^2 (1-2\gamma)^2 e^{-\pi/(\omega_{01}\tau)}, \tag{3.1}$$

where $\tau = 2L_1/R_1$, with R_1 assumed to be the resistance of switches, inductor and transducer of L-C_P, and $\omega_{01} \cong \frac{1}{\sqrt{L_1 C_P}}$.

In case a NVC is used (Fig. 11b), $V_R(t) = V_P(t)$ as long as $|V_P(t)| > V_T$, where V_T is the absolute value of the highest MOSFET threshold voltage. With respect to diodes, MOSFETs offer negligible voltage drops and energy losses. However, on the activation of SECE, during the discharge of $V_P(t)$, the NVC turns off when $|V_P(t)| = V_T$. For lower voltages, conduction may still occur through the FET body diodes, which would introduce significant losses, so that energy extraction should safely stop at V_T. Then, at the end of the subsequent elongation, a maximum absolute voltage $2V_{P0} - V_T$ will be reached on $V_P(t)$.

Defining $\delta = V_T/V_{P0}$, with $0 < \delta < 1$, the energy stored in L_1 after the transducer has discharged from $2V_{P0} - V_T$ to V_T can be determined:

$$E_L^{(NVC)} = 2C_P V_{P0}^2 (1-\delta) e^{\frac{-2\arccos\left(\frac{\delta}{2-\delta}\right)}{\omega_{01}\tau}} \tag{3.2}$$

In the above two cases no power is harvested for absolute input voltages lower than the minimum conduction thresholds of $2V_\gamma$ and V_T, and residual charges $|Q_{BR}| = 2C_P V_\gamma$ and $|Q_{NVC}| = C_P V_T$ are left at the end of every conversion. Such residual charge has to be first canceled during the subsequent peak-to-peak elongation before the sign of $V_P(t)$ changes.

As a term of comparison, a lossless SECE with an ideal rectifier with $V_\gamma = 0$ (IR) would leave no residual charge and store in L_1 the following energy for a single activation:

$$E_L^{(IR)} = 2C_P V_{P0}^2 e^{-\pi/(\omega_{01}\tau)}. \tag{3.3}$$

In this section an input interface based on a NVC with residual charge inversion (RCI) is proposed and it is shown in Fig. 12. This allows to reduce energy losses through the MOSFET bridge and to remove all the charge $Q_{PP} = 2C_P V_{P0}$ generated in a peak-to-peak elongation. The inversion of residual charge applies a more favorable voltage offset for the next peak-to-peak elongation. Other types of pre-biasing techniques, in which the offset charge is drawn from the output, were introduced in [47] and showed to significantly increase the performance. However, in case of low output voltages, e.g. when high load currents are applied, the advantages of the pre-bias are reduced. Differently, the inverted residual charge is exploited as a bias, which otherwise would impact negatively output power. This approach improves the performance especially in case of low vibrations, when the input voltage is comparable to the conduction threshold and the losses would otherwise be significant. The inversion of residual charge is also performed in other synchronized switch techniques, such as for example SSHI, in which charge inversion is mostly required for keeping a rectifier bridge in a conducting state for most of the time. However, the conversion efficiency is still bias dependent. Differently, besides producing significantly higher piezoelectric voltages, performing RCI with SECE also introduces a bias independent energy conversion efficiency, because the transducer is never directly connected to the output node.

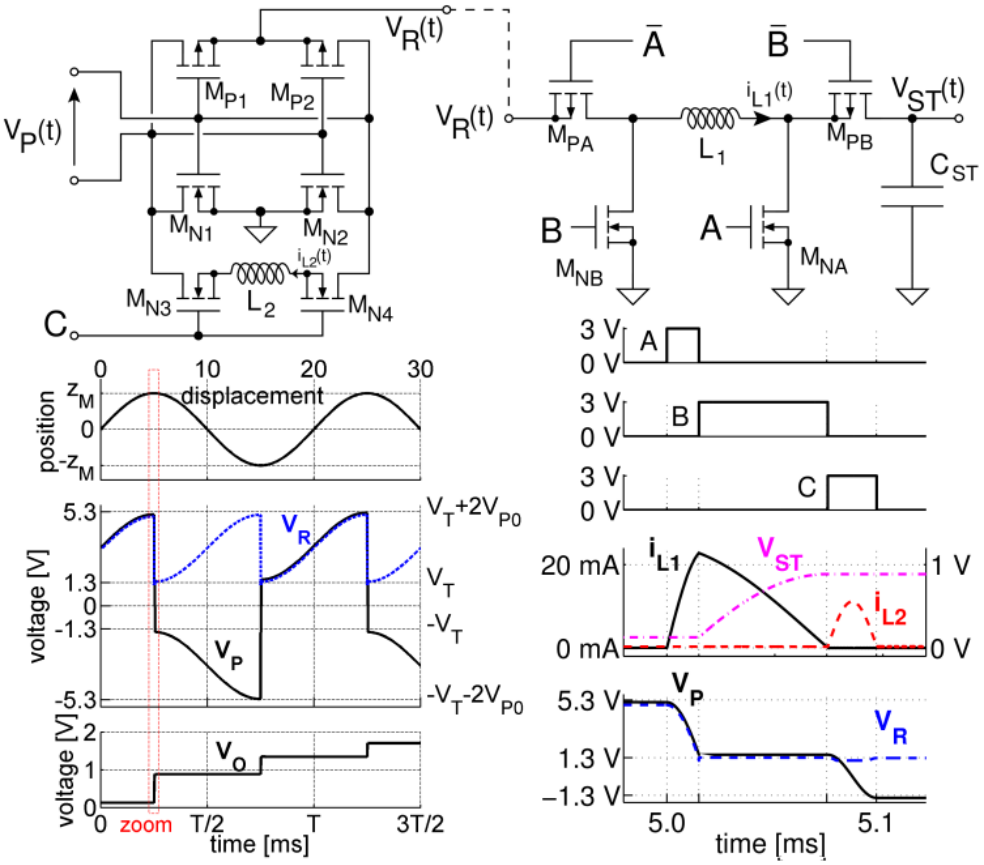

Fig. 12. Schematic and circuit simulations of a SECE circuit based on a NVC with the proposed RCI. Circuit simulations were performed with V_{P0} = 2 V, f = 50 Hz, L_1 = 10 mH, L_2 = 2.5 mH, C_O = 1 µF. $M_{N1..4}$ and $M_{P1,2}$ are standard MOSFETs with $|V_T|$ = 1.3 V A zoomed view of an individual energy conversion is also shown.

As shown in Fig. 12, with respect to SECE, an inductor L_2 and two switches M_{N3}, M_{N4} are introduced. An additional signal C is activated for inverting the residual charge left on the transducer. This is accomplished by letting the resonant circuit C_P-L_2 oscillate for a half period π/ω_{02}, where $\omega_{02} \cong 1/\sqrt{L_2 C_P}$ is its resonance frequency. This new initial offset would ideally allow to reach a higher maximum voltage $2V_{P0} + kV_T$ on $V_P(t)$, where k=exp($-\pi$ /($\omega_{02}\tau_2$)), τ_2=$2L_2/R_{2eq}$ and R_{2eq} is the series resistance of L_2 and of the RCI switches (M_{N3} and M_{N4} in Fig. 12). It can be found that the energy stored in L_1 after the transducer has discharged from $2V_{P0} + kV_T$ to V_T is:

$$E_L^{(RCI)} = 2C_P V_{P0}{}^2 \left(1 + k\delta + \frac{k^2-1}{4}\delta^2\right) e^{\frac{-2\arccos\left(\frac{\delta}{2+k\delta}\right)}{\omega_{01}\tau}} \tag{3.4}$$

Typical values for the components that have been considered for analytical evaluations are $V_\gamma \cong 0.35$ V for low threshold Schottky diodes, e.g. BAT754, and $V_T \cong 1.3$ V for discrete MOSFETs with low gate charge and compatible with piezoelectric voltages of up to 20 V, e.g. BSS138PW and NTR1P02T1, and $V_T \cong 0.7$ for integrated MOSFETs available in standard 0.35 µm CMOS technologies. Hence, in practical cases, it roughly holds that $\delta/\rho \cong 2 \ldots 3$.

The corresponding energy ratios of (3.1), (3.2), (3.3) and (3.4) normalized to $2C_P V_{P0}{}^2$, i.e. E_0, are functions of δ and ρ for a given set of circuit parameters. A comparison plot is shown in Fig. 13. As it can be noticed, Schottky rectifiers underperform with respect to NVC whereas RCI is the best option, especially for low input voltages. However, this holds for an integrated circuit perspective. For a discrete components design, Schottky rectifiers perform better than NVC for low input voltage due to typical higher V_T of MOSFET unless RCI is employed.

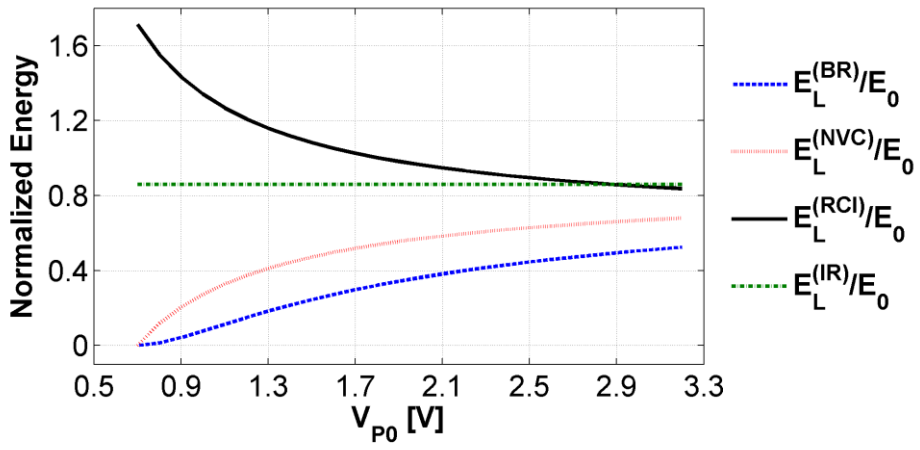

Fig. 13. Normalized energy ($E_0 = 2C_P V_{P0}{}^2$) extracted from C_P and stored in L_1 at the end of the first phase of SECE with different types of the input interface: full-wave bridge rectifier (BR), NVC, NVC with RCI enabled (RCI), and ideal rectifier (IR). The parameters used for the generation of the figure are: $V_T = 0.7$ V (corresponding to a generic 0.35 µm integrated process), $V_\gamma = 0.35$ V, $C_P = 52$ nF, $L_1 = L_2 = 560$ µH, $R_1 = 10$ Ω, $R_{2eq} = 5$ Ω.

The OSECE topology [81] is an interesting improvement of classic SECE topology. Differently from the latter, it exploits three coupled inductors and diodes. OSECE has a lower circuit complexity (switches and their controllers) and is surely more suitable than SECE for an implementation with off-the-shelf components, although some works implementing SECE converters have been reported [16]. However, in order to improve efficiency, reduce size and costs on large volumes, an integrated solution is advisable. Several works [12], [15], [82] use active rectifiers for diodes replacement as they have lower losses and lower inverse leakage current than diodes. The command energy required for the MOSFET and its driver is very small for integrated circuits compared to PCB circuits with discrete components and, furthermore, it can be tailored on application requirements (i. e. switching frequency, turn-on delay and on-resistance). In such a perspective, an integrated version of OSECE with active rectifiers might offer better performance than the PCB solution and even outperform an integrated SECE. A drawback of active switches and rectifiers is their inability to operate without a supply and therefore a start-up mechanism is required (e.g. a secondary passive rectifier in parallel with the active one).

However, a significant difference between SECE with RCI and OSECE lie in the amount of inverted charge on the piezoelectric transducer. With SECE-RCI such amount of charge is independent from both the load and the input parameters and depends only on the characteristics of the MOSFETs employed in the NVC (i.e. their $V_{GS,th}$). Differently, in OSECE the amount of inverted charge strongly depends on the output voltage (i.e. load), transformer turns ratio and diodes characteristics. With high turns-ratio of the transformer, the inverted charge might be very low and provide a less favorable offset than SECE-RCI.

3.2 Two-Way Energy Storage Policy

A typical issue of self-powered harvesting systems exploiting active converters (i.e. not a bare BR) is the start-up time required for transition from passive to active harvesting mode. Systems with a single energy storage element [21,22,28-30] rely on

such energy reservoir both for supplying both the converter supply and the load. Since application requirements, e.g. for sustaining a wireless sensor node transmission, require a minimum amount of stored energy and a minimum voltage to enable operation, usually large capacitors or supercapacitors are used. As a consequence, a considerable amount of time ranging from seconds to hours [12], [68] may be required for switching from a passive harvesting interface to an active power conversion interface, which also require a minimum operating voltage. During this period, the efficiency of energy extraction is negatively affected. A second issue is the inability of the load to consume all the energy in the storage element without compromising the operations of the converter by bringing it back into passive mode. This limits the energy available to the load because a considerable amount of energy is locked in the storage capacitor just for keeping the output voltage high enough for enabling the power converter and without the possibility of being used by the load. In systems with a huge energy storage, e.g. a tens of mF supercapacitor, such amount of wasted energy is intolerable, especially if a second buck-boost regulator is placed between the harvester and the load with the task of generating a stable and regulated supply voltage

The proposed power management policy is similar to that introduced in [83]–[86] and makes use of two different capacitors, as shown in Fig. 14: the converter power supply is provided by C_{DD} whereas the load is powered from C_{ST}. Furthermore, this scheme, which will be referred to in this paper as two-way energy storage (TWS), allows the load to completely drain C_{ST} without affecting the operation of the active power converter. In [84]–[86], C_{DD} is charged initially through a passive path to start the active converter and, when the voltage on C_{ST} is sufficient, the two capacitors are shorted or connected through a diode so that the incoming power sustains both the converter and the load. In the presented architecture, during the start-up phase C_{DD} is passively charged trough a secondary passive rectifier, implemented with a NVC with a diode in series (NVCD), until the minimum voltage V_{DDmin} required for properly powering the active conversion process. This phase is expected to be much shorter than in single storage systems because of the significantly lower value of C_{DD} with respect to C_{ST} for sustaining the power converter. Then, as soon as SECE is started, the energy flow is directed towards C_{DD} until it is recharged at least to a higher

voltage $V_{DDact,max}$ in order to keep the converter supply in the required operating range, which is a priority task as it will be shown in the next paragraph. $V_{DDact,max}$ is not the maximum allowed supply voltage, but it is the higher threshold voltage of an hysteretic level comparator used for routing energy alternatively to C_{ST} and C_{DD} (i.e. for activation of S_{ST} or S_{DD} in Fig. 14). Then, the energy flow is diverted to C_{ST} as long as V_{DD} remains above a second threshold voltage $V_{DDact,min}$ chosen for preserving a high conversion efficiency. Below this voltage, energy is diverted to C_{DD} again to keep the power converter functional. It holds that $V_{DDmin} < V_{DDact,min} < V_{DDact,max}$.

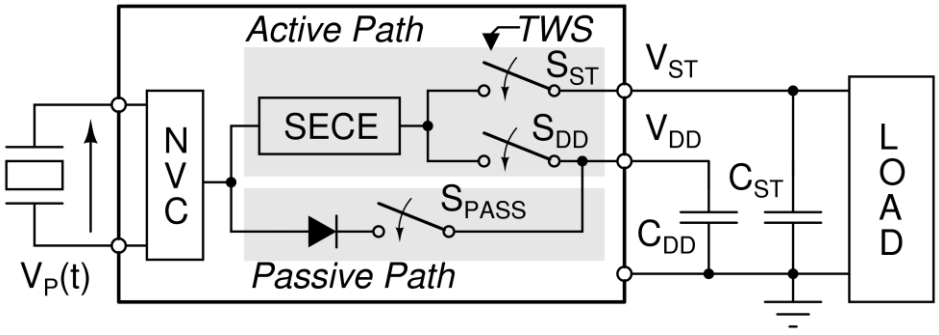

Fig. 14. Block diagram showing the active and passive charging paths in the converter and TWS for the active path.

In order to assess the advantages of TWS, it is useful to compare the energy extracted by the NVCD passive interface, i.e. when the minimum baseline voltage is still not reached in a single storage system with a large capacitor, with the energy extracted by SECE. The output energy in passive operation (i.e. when SECE is not activated) $E_{P,BR}$ per half-wave can be evaluated by integrating the current through the diode in the passive path in Fig. 14 with a fixed output V_{DD}, assumed to be constant in the half-period (e.g. with a large capacitor or a supercapacitor) and the resulting expression for $E_{P,BR}$ is the following:

$$E_{P,BR} = 2C_P V_{DD}\left(V_{P0} - V_{DD} - V_\gamma\right) \tag{3.5}$$

The SECE process has an intrinsic efficiency value η_S, defined as the energy transferred to the output divided by the energy removed from the transducer in a

single charge extraction, which is also dependent on circuit parameters and components. In an ideal case it holds that $\eta_S = 1$. In order to evaluate the performances of TWS, the effectiveness of SECE with NVC and BR are compared using the ratio $\eta_P = E_{P,BR} / E_L^{(NVC)}$. The ratio η_P accounts for the efficiency of SECE with NVC and, approximating to unity the exponential term in $E_L^{(NVC)}$, it can be written as:

$$\eta_P = \frac{1}{\eta_S} \frac{V_{DD}}{V_{P0} - V_T} \left(1 - \frac{V_{DD} + V_\gamma}{V_{P0}} \right) . \tag{3.6}$$

The numerical evaluation of (3.6) is illustrated in Fig. 15 for some values of V_{P0} and it is clearly shown that the theoretical efficiency of the ideal SECE ($\eta_S = 1$) is higher than the BR in any case (as $\eta_P < 1$). This also holds with a non-ideal SECE with a sub-optimal efficiency $\eta_S = 0.5$. Therefore, it is advisable to use SECE with respect to a passive rectifier in any configuration, as soon as it is possible. In addition, if a supercapacitor (from mF to the F range) is required, the use of a single

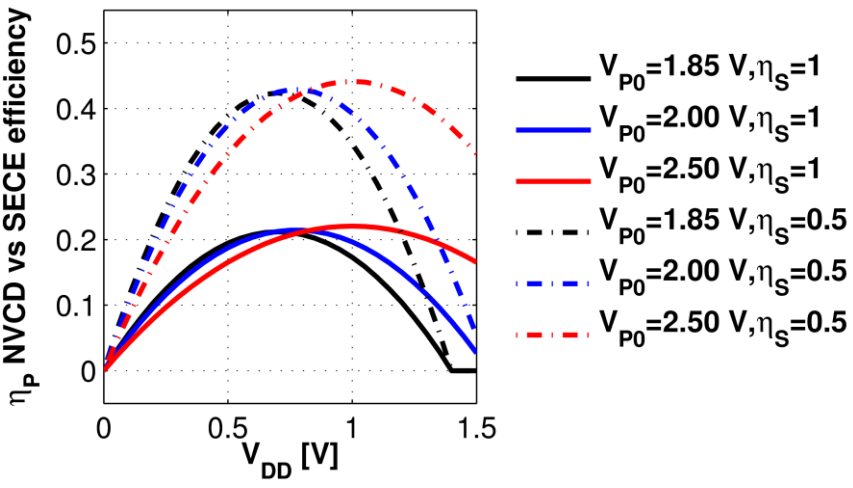

Fig. 15. Efficiency of passive charging of storage element (NVC+Diode) for start-up with respect to SECE. As can be pointed out, the efficiency is less than 50% even for SECE with a low conversion efficiency (η_S=0.5). The values used for the evaluation are V_T=0.7 V for generic MOSFETs and Vγ=0.35 V for diodes.

energy storage element for supplying both the converter and the load is not optimal for the start-up phase, i.e. from 0 V to V_{DDmin}, because this phase relies on a passive rectifier for energy harvesting. In the above considerations, RCI was not considered.

Anyway, enabling also RCI reinforces the above conclusions, as it will be shown experimentally in Chapter 3.4.

3.3 Architecture of Single Source SECE Converter

The architecture of the proposed converter implementing a self-starting SECE with RCI and TWS, which has been designed in a 0.32 μm BCD technology from STMicroelectronics, is depicted in Fig. 7.

The converter requires two external capacitors C_{DD} and C_{ST}, two inductors L_1 and L_2 and a variable resistor R_{RCI}, which is used for setting the duration of RCI. In a future version of the converter, a single inductor can be utilized rather than L_1 and L_2 as the utilization factor of each inductor is very low. In fact, the use of a second inductor L_2 for the RCI circuit is not mandatory and only L_1 might be used for both the buck-boost converter and the RCI circuit, as the RCI phase can be executed immediately after a full cycle of the buck-boost converter. Since the main purpose of this work was to assess the effectiveness of RCI, two separate inductors were used in this design for ease of implementation.

Once the converter has started active operations (i.e. SECE) the transducer is always kept in open circuit by the switch S_S, which is normally open. As the converter operates as a buck-boost converter, there is never a direct conduction path from the transducer to V_{ST} or V_{DD}. Moreover, RCI is performed directly on the transducer nodes and thus RCI is not affected by the load and by V_{ST} or V_{DD}. RCI depends only on the rectifier characteristics, hence on the threshold voltage $V_{GS,th}$ of the MOSFETs in the NVC, and on the series resistance of the associated L_2-C_P circuit.

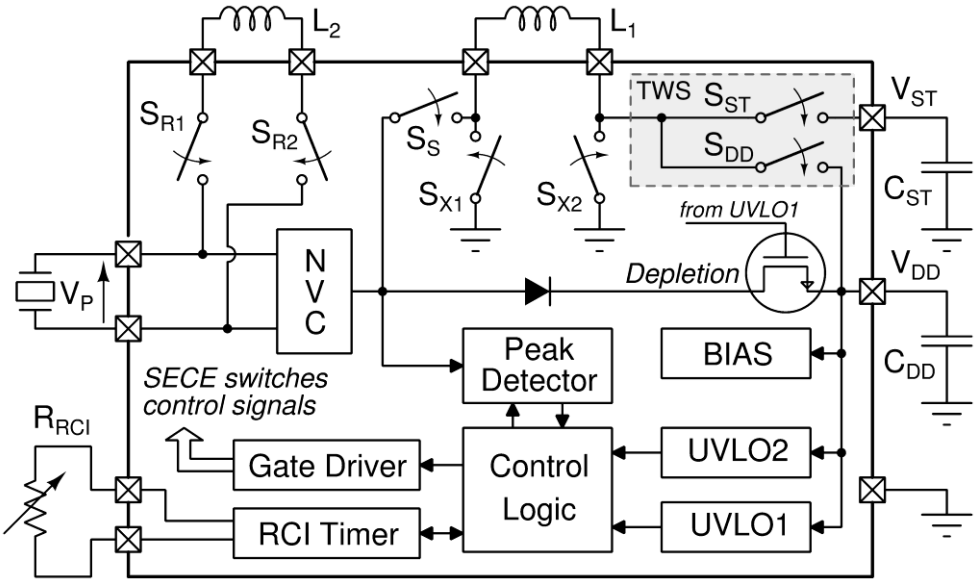

Fig. 16. Block diagram of the designed integrated converter for a single piezoelectric transducer.

The converter draws nominally a quiescent current I_{DDq} equal to 160 nA when no energy extraction cycles are preformed (i.e. in idle state) at V_{DD}=2.7 V. The current drawn from each sub-circuit, obtained by simulations, is listed in Table II.

TABLE II SIMULATED QUIESCENT CURRENT DRAWN BY EACH SUB-CIRCUIT OF THE CONVERTER.

Sub-circuit	**Current [nA]**
Bias	48
UVLO1	16
UVLO2	16
Peak Detector	32
Bias (in Buck-boost converter)	16
Other[1]	32

[1]This current is drawn by a comparator detecting whether V_{ST} is greater than an externally applied voltage reference. Such function is not used by the converter but its consumption has been considered in the evaluation of the quiescent current as well as in the experimental results.

The section of the circuit related to the passive start-up is shown in Fig. 17. The piezoelectric transducer is firstly connected to an NVC which outputs the rectified version V_R of the input voltage V_P (i.e. during the negative half-waves the sign is

inverted). At start-up from a discharged state, a pMOS diode M_{PD} and a depletion nMOS M_{Nd} (i.e. a normally-closed switch) connect V_R to V_{DD} allowing the latter to be passively charged. The converter starts to operate actively (i.e. SECE is activated) as soon as $V_{DD} \geq V_{DDmin} = 1.4$ V. At that voltage, an under-voltage lock-out (UVLO1) circuit triggers and M_{Nd} is turned off blocking the passive charging path towards C_{DD} and then the buck-boost converter is activated and SECE is performed. An hysteresis of about 100 mV is added to the UVLO in order to prevent undesired on-off switching due to noise and small variations on V_{DD}.

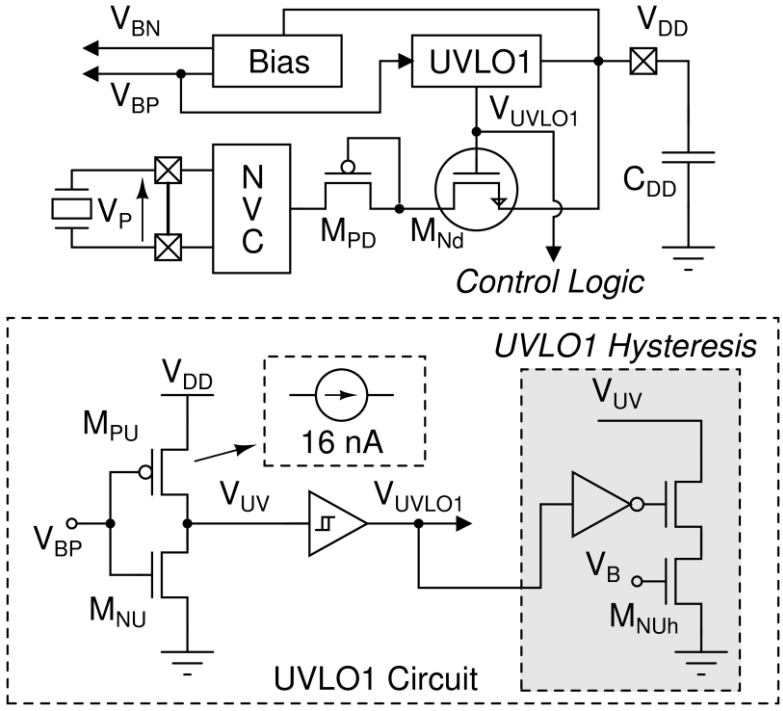

Fig. 17. Passive start-up circuit and details of UVLO1 circuit diagram.

Actually, the minimum required input voltage amplitude for a successful start-up operation is V_{P0}=1.8 V. However, as C_{DD} is usually comparable with the output capacitance of the piezoelectric transducer (in this work $C_{DD} \cong$ 200-470 nF), it only takes a few oscillation periods in order to charge C_{DD} up to V_{DDmin} and start SECE. Once SECE and RCI are started, the converter can successfully extract energy with input voltages down to 0.7 V. The passive start-up block draws 64 nA nominally and embeds a supply-independent bias circuit which generates a reference current of

16 nA and outputs the reference voltages V_{BP} and V_{BN} which are used as inputs for biasing all the analog circuitry of the IC.

The NVC output V_R is tracked by an ultra-low power peak detector and an energy extraction cycle is performed on each maximum of V_R. The circuit diagram of the interface for the piezoelectric transducer is shown in Fig. 18. It is composed by an NVC for signal rectification, a switch for the connection to the main inductance L_1, a peak detector and the switches for RCI. The first stage of the peak detector is an input signal conditioning block and such stage is required in order to filter the input signals lower than the minimum value of V_{Pmin} = 700 mV. It also includes an RC filter (R_f and C_f) with a -3dB cut-off frequency of 5.3 kHz in order to smooth the spikes generated during RCI and prevent false peak detections. M_{F1} and M_{F3} are low threshold nMOS transistors . The next stage is composed of a voltage tracking circuit and a hysteretic comparator with hysteresis V_h = ±15 mV.

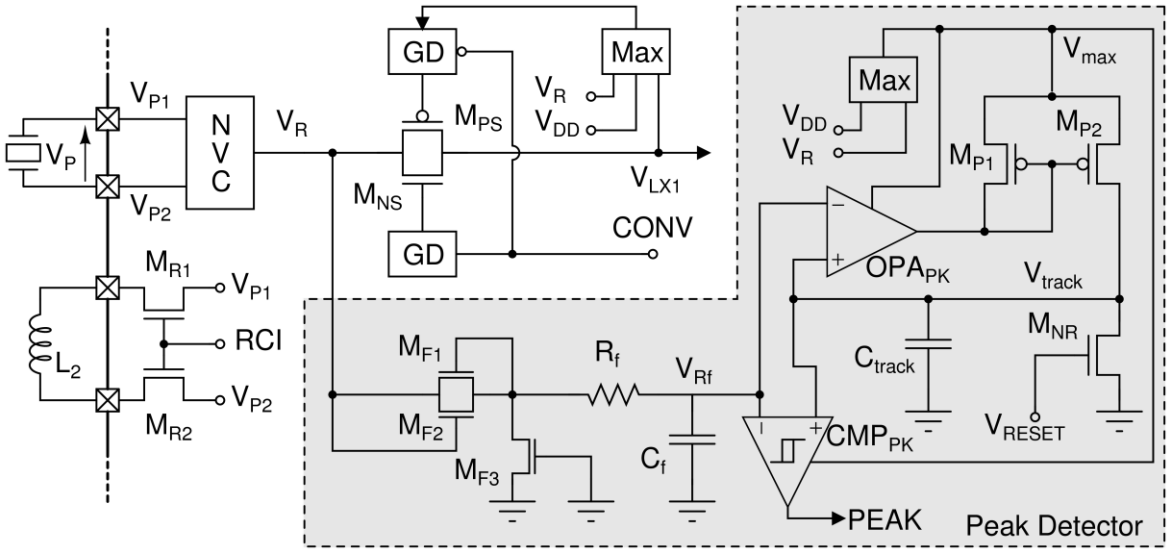

Fig. 18. Circuit diagram of the interface for the piezoelectric transducer.

The static current drawn by the peak detector is as low as 32 nA, equally divided between the voltage tracking block (OPA_{PK}) and the hysteretic comparator (CMP_{PK}). The voltage tracking block charges C_{track} with M_{P2} in order to keep $V_{track} = V_{Rf}$. As charge on C_{track} can only be added by M_{P2}, a maximum is detected by the comparator

when $V_{Rf} \leq (V_{track}\text{-}V_h)$ and, in this case, the PEAK signal is set to V_{DD}. At the end of an energy extraction cycle C_{track} is reset by M_{Nr} in order to rightly track the next half-wave on V_{Rf} and detect the following maximum; V_{RESET} is generated by the logic controller on the falling edge of CONV signal, which is activated by the control logic only during energy extractions. As V_P (and thus V_R) can exceed V_{DD}, the amplifier OPA_{PK}, the current mirror M_{P1}-M_{P2} and the comparator CMP_{PK} are supplied by the highest voltage between V_{DD} and V_R by a dedicated bulk regulator circuit.

The switch connecting V_R and V_{LX1} is composed by both a nMOS and a pMOS and both gates are driven by a gate driver (GD) which, for the case of M_{PS}, is constantly supplied by the highest voltage between V_{DD}, V_{LX1} and V_R in order to completely turn off M_{PS}.

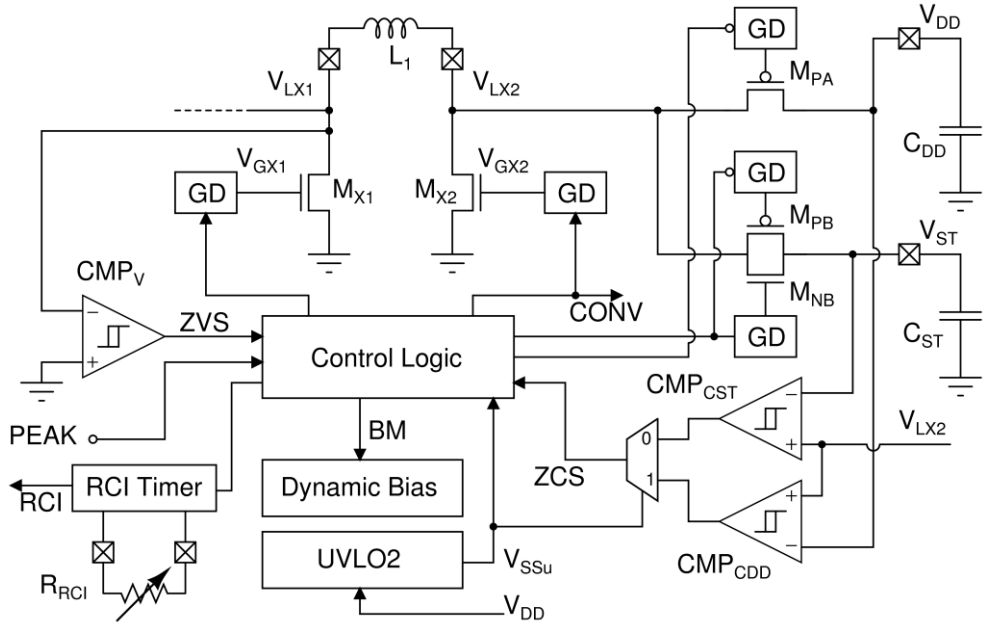

Fig. 19. Circuit diagram of the SECE converter

The RCI circuit is made of two nMOS switches M_{R1} and M_{R2}, which connect V_{P1} and V_{P2} to the inductor L_2. The RCI phase is started by the logic controller as soon as the energy on C_P has been extracted. In this implementation, the length of the RCI phase is set by the value of a resistor R_{RCI} which alters the RC constant in a pulse

generator (RCI Timer shown in Fig. 16). The timing of RCI is deeply analysed and illustrated in the next section, together with buck-boost converter operation.

The buck-boost converter (circuit diagram shown in Fig. 19 is managed by a clock-less logic controller which implements an asynchronous finite state machine (FSM). When a maximum is detected PEAK is set to V_{DD} and the FSM is activated from idle state. The end of each phase of the energy extraction process (energy transfer from C_P to L_X and from L_X to C_{ST} or C_{DD}) is dynamically determined by means of zero-voltage switching (ZVS) and zero-current switching (ZCS) detectors, This grants many degrees of freedom in the choice of the piezoelectric transducer, C_{DD}, C_{ST}, L_X, input power level and output voltage, because conversion timings are not hard-coded in the control circuits. While the converter is performing the second phase of the energy extraction process (i.e. energy transfer from L_X to C_{ST} or C_{DD}), the RCI is activated in order to invert the residual charge on C_P. The signals of the FSM, the input voltage V_P, and V_{LX2} are shown in Fig. 20. The extraction process starts as soon as the PEAK signal rises. The analog circuitry is normally turned off in idle state in order to minimize static current (down to 16 nA). When the extraction process starts, the dynamic bias block is turned on (BM=0, active low) and, as it is the first phase of the energy extraction process, signals are set as follows: $V_{GX2} = V_{DD}$ (which is the same signal as CONV in Fig. 18) and $V_{GX1} = 0$ V. The end of the first phase is notified by the rising edge of ZVS signal. The second phase of the energy extraction is the transfer of energy from L_1 to C_{ST} (or C_{DD}) with $V_{GX1} = V_{DD}$ and $V_{GX2} = 0$ V; V_{LX2} is clamped to V_{ST} in Fig. 20 which was forced, in this case, to 2 V. Simultaneously, the RCI is performed on the piezoelectric transducer (RCI control signal high and voltage inversion on V_P shown in the traces of Fig. 20). The second phase ends as all energy is moved to C_{ST} (or C_{DD}) and this is notified by a falling edge of ZCS. The inputs of the FSM are normally masked and are enabled only during the FSM state in which they are relevant in order to prevent incorrect operations. ZCS is achieved by monitoring the voltage on M_{PA} (or M_{PB}) due to its on-resistance and ZCS is effectively detected when V_{ST}-$V_{LX2} \leq$ -15 mV (or V_{DD}-$V_{LX2} \leq$ -15 mV). Such scheme allows flexibility and adaptability at the cost of a lower efficiency for values of V_{ST} approaching 5 V because di_{L1}/dt increases and the

discharge time of L_1 becomes comparable with the propagation delay of the comparator CMP_{CST} (or CMP_{CDD}) which is about 800 ns.

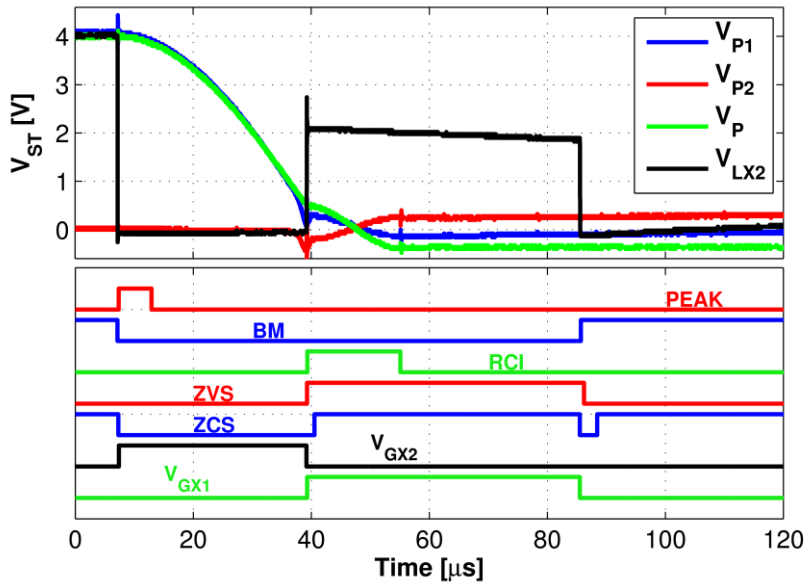

Fig. 20. Waveforms acquired from a sample device measurement during an energy extraction cycle. Both SECE and RCI are shown together with internal control signals (on bottom). In such acquisition, the energy was directed towards C_{ST}.

The UVLO2 circuit in Fig. 19 is similar to UVLO1 in Fig. 5 but it has different thresholds which determine $V_{DDact,min}$ and $V_{DDactmax}$. UVLO2 switches it state when V_{DD} rises above 2.6 V and when it drops below 2 V. Its output V_{SSu} notifies the control logic whether to charge C_{ST} or to start a C_{DD} charging sequence in order to provide energy to the converter itself. This process is illustrated on the top of Fig. 21 and it can be seen that C_{DD} is periodically recharged. On the bottom of Fig. 21, TWS operation on a measurement with a sample of manufactured devices is illustrated and the V_{SSu} signal, brought out of the chip with a test structure, is highlighted. The high state of the signal (about 1 V) means that the UVLO2 circuit has detected that V_{DD} is below the minimum value and thus the converter is forced to direct energy towards C_{DD} instead of C_{ST}.

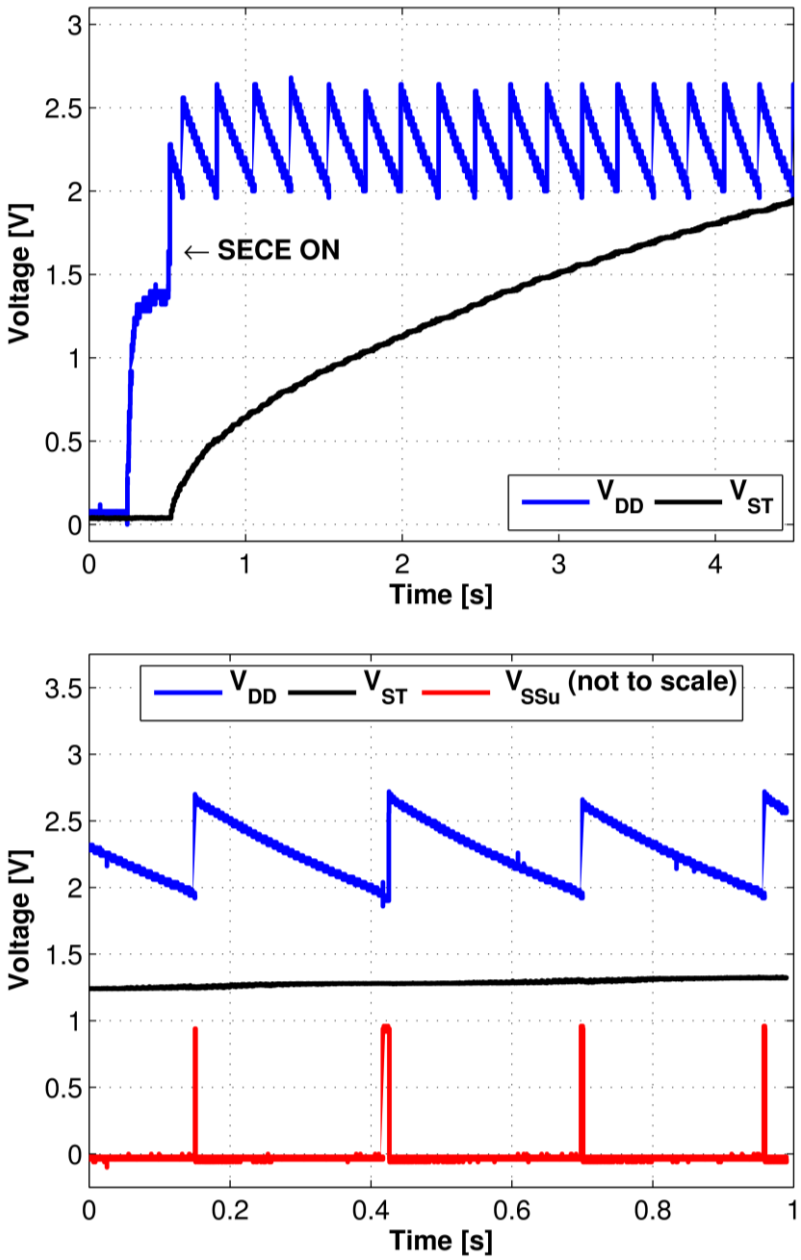

Fig. 21. (top) Waveforms acquired from a sample device measurement showing the TWS operating principle. C_{ST} is slowly charged while V_{DD} is charged only when its value is below a certain threshold, for keeping the active converter enabled. The experimental conditions were: V_{P0} = 2 V, C_P = 47.4 nF, f = 60 Hz, C_{ST} = 66 µF, C_{DD} = 200 nF, L_1 = 10 mH, L_2 = 560 µH. (bottom) Detail of the TWS operations with the slow discharge of V_{DD} due to self-consumption. V_{SSu} (amplitude not to scale, as it has been acquired from a test structure externally supplied) is the output of UVLO2 circuit and goes high when C_{DD} needs a re-charge sequence.

3.4 Experimental Results

The power converter has been manufactured in a 0.32 µm BCD technology from STMicroelectronics in an active area of 0.95 mm^2. The converter is placed in a 4.6 mm^2 die, whose micrograph is shown on the left of Fig. 22. The setup used in the performed measurements is depicted on the right of Fig. 22 and the values of the used external components are shown in Table III The chosen piezoelectric transducer is a Q220-A4-303YB from Piezo Systems which has a nominal output capacitance C_P=52 nF. Since the focus of the paper is on the converter design and the use of RCI and TWS, a first series of measurements has been performed with a real piezoelectric transducer in order to prove the functionalities of the proposed approach. Then, other experiments, whose aim was to quantitatively characterize the performance of the circuit from an electric point of view, have been performed by emulating the transducer with laboratory equipment for higher accuracy and precision in the electrical quantities. The emulation was performed with an Agilent 33120A function generator setting the open-circuit voltage V_{P0} and a series-connected metallized polypropylene capacitor of 47.4 nF.

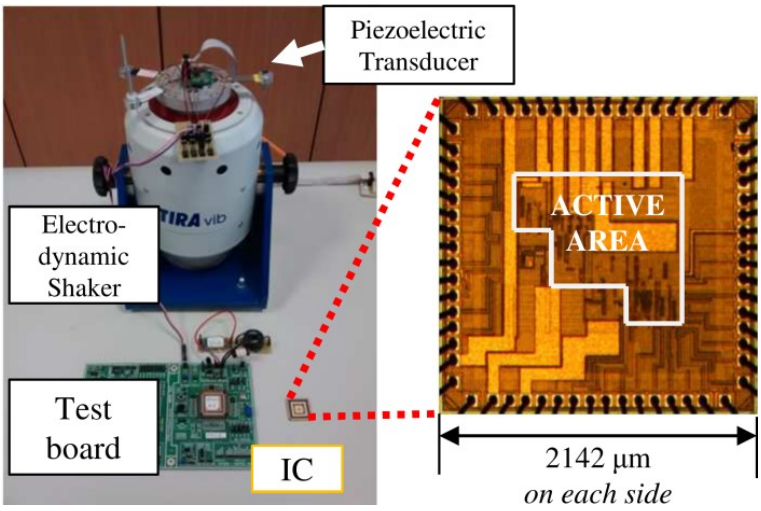

Fig. 22. Experimental setup used for measurements, based on the IC, a test board and a piezoelectric transducer stimulated by an electrodynamic shaker (left). Die micrograph with active area highlighted. (right).

TABLE III VALUES OF EXTERNAL COMPONENT USED IN ALL EXPERIMENTS.

Component	Value	DC Series Resistance
L_1	10 mH	4.4 Ω
L_2	560 µH	0.36 Ω
R_{RCI}	1…5 MΩ*	-
C_P	47.4 nF	-
C_{DD}	470 nF	-
C_{ST}	10 mF	-

* The value of R_{RCI} must be tuned to set the duration of RCI to $\pi/\sqrt{L_2 C_P}$ in order to obtain maximum RCI performance.

Firstly, as mentioned above, the IC has been tested with the piezoelectric transducer, as shown in Fig. 22. The load was emulated with a Keithley 2601 SMU forcing a load current of 8.25 µA in order to obtain V_{ST} = 2.5 V, which is a typical supply voltage for low power electronics. The piezoelectric transducer was excited with an electro-dynamic shaker vibrating at f_P=50 Hz and with an acceleration a_{RMS}=0.1 g. With RCI enabled, the energy conversion efficiency, evaluated as the ratio between output power and available input energy times the energy extraction frequency (i.e. $f_P C_P V_{Pmax}^2$ where V_{Pmax} is the transducer peak voltage generated by the non-linear energy extraction process), has been experimentally determined at 72.2%, with an extracted power from the transducer of 28.57 µW. However, it s be noticed that in the above experiment the IC was self-supplied with the harvested power and the reported efficiency value also includes the contribution of the IC intrinsic (ultra-low) power consumption. For this reason, the overall efficiency of the bare power conversion is higher than this value.

3.4.1 Intrinsic energy consumption

The second experiment is the measurement of the quiescent current of the IC with a Keithley 2601 SMU forcing V_{DD} and measuring the drawn current while it is not performing any energy extraction and with an external bias on V_P of 1 V. The results are shown in Fig. 23. The IC draws about 160 nA in its typical operating voltage (V_{DD} from 2 V to 3 V) and this is very important for energy-limited scenarios. Then, by forcing V_{DD}=2.7 V externally with the same SMU and filtering its output with an

RC filter (with R=1 MΩ, C= 4.7 μF) the average current drawn from V_{DD} by the converter has been measured, sweeping the input signal frequency from 20 to 100 Hz with V_{P0}=1.5 V and C_P=47.4 nF. The obtained results for the total current drawn I_{DD} are show on the left of Fig. 24 whereas the dynamic energy required per energy extraction cycle is shown on the right of Fig. 24 and it is calculated from the difference between I_{DD} and the measured I_{DDq} of 166 nA (at V_{DD}=2.7 V). The average value of the dynamic energy per conversion is 2.2 nJ, and is small, typically less than 3%, with respect to the available energy on a piezoelectric transducer ($0.5C_PV_{Pmax}^2$) with C_P in the order of some tens of nF.

In order to estimate the minimum input power required by the converter, a third experiment has been performed starting from an operating condition (with RCI enabled) and decreasing the input power down to 296 nW (f_P=7 Hz V_{P0}=500 mV, C_P=47.4 nF). In such conditions the converter stops to provide energy to C_{ST} but it is able to sustain itself and to continue performing SECE with RCI at V_{DD}=1.54 V.

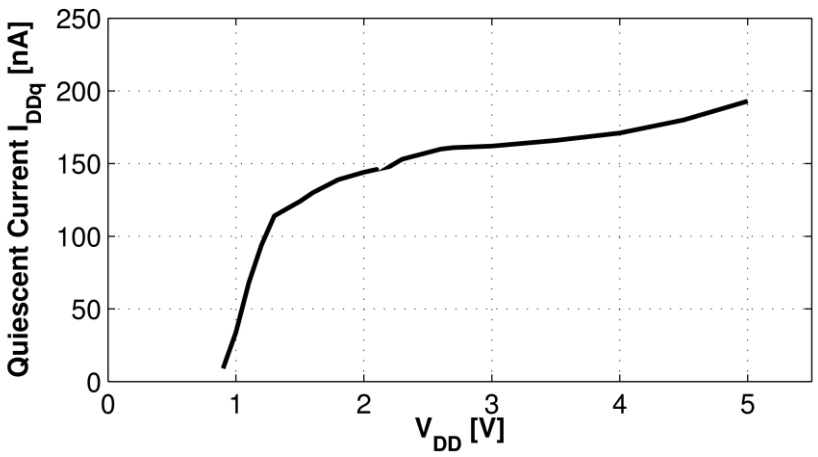

Fig. 23. Quiescent current drawn by the converter in stand-by state (no energy extractions are performed) for several V_{DD} values.

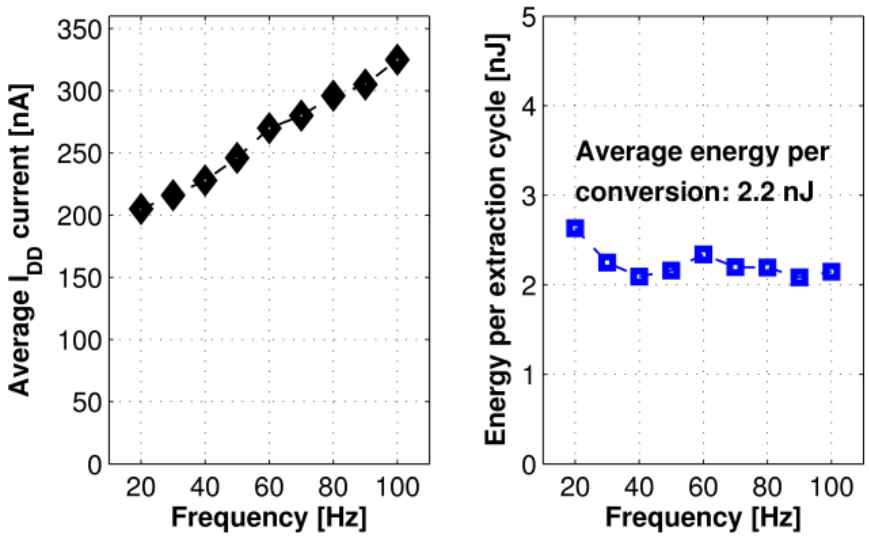

Fig. 24. (left) Measured average current I_{DD} drawn from V_{DD} for several input signal frequencies. (right). Energy required for a single energy extraction, calculated from the measured I_{DD} when SECE-RCI is enabled.

3.4.2 TWS performance improvement

The TWS has been validated through a fourth experiment: firstly, V_{DD} and V_{ST} have been connected together in order to emulate a classic single way storage (SWS) system; in a second time, the TWS technique has been enabled (i.e. V_{ST} and V_{DD} are independent). As previously discussed, in the start-up phase SECE and RCI can only be performed in the TWS system. The output voltage V_{ST} has been acquired with a Tektronix MSO2024 digital oscilloscope in both cases and the results are shown in Fig. 25. TWS, together with SECE and RCI, is considerably improving the energy extraction process with an increase of more than 6.5 times of the harvested energy after 1000 s with respect to SWS (which, further, does not benefit from SECE and RCI) under the same input conditions (piezoelectric transducer emulated with $V_P = 2$ V, $f = 60$ Hz, $C_P = 47.4$ nF). The gain of TWS over SWS is present only when $V_{ST} < 1.4$ V, because above this value SECE is activated also for SWS. However, this power management policy allows a quicker charging of the output from discharged states during start-up than with SWS, which becomes quite evident when C_{ST} is a large capacitor, e.g. a supercapacitor in the mF range. In the latter case the start-up phase of a SWS can take up to several minutes or hours [12], [68] with

supercapacitors and weak and irregular vibrations. In this latter case, activating SECE in the initial phases significantly boost efficiency. In addition, the efficiency of SECE is quite independent from the output load condition [16], [41], which results in an almost constant efficiency throughout the whole charging process.

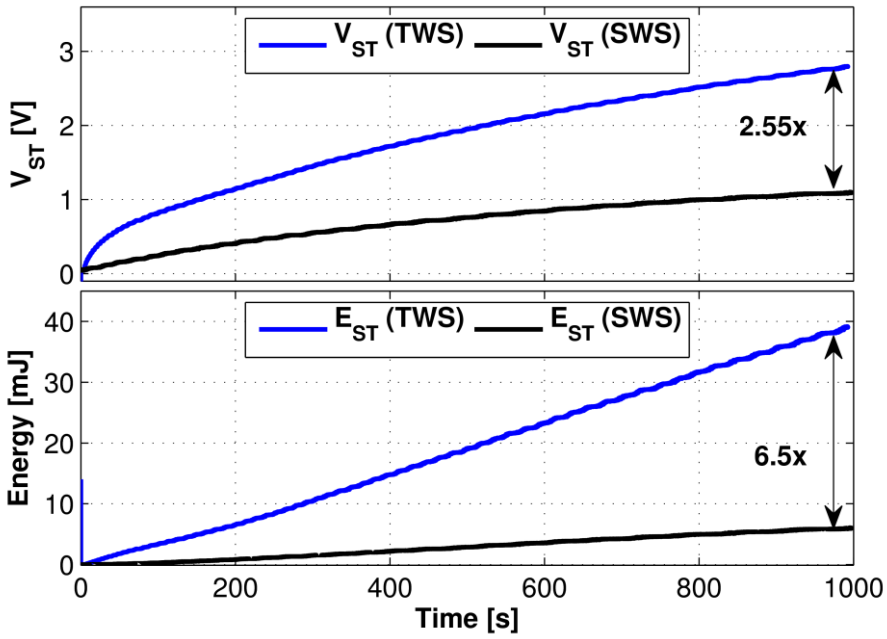

Fig. 25. Comparison of acquired V_{ST} voltage with C_{ST}=10 mF in two configurations (SWS and TWS) with the same input excitation: piezoelectric transducer emulated with V_{P0}=2 V, f=60 Hz, C_P=47.4 nF.

3.4.3 Conversion efficiency

In a fifth experiment, the efficiency of the energy transfer from C_P to C_{ST} has been measured and Fig. 26 shows the results for several values of V_P spanning into the allowed range of operation of the IC. In this experiment C_{ST} = 66 µF and a Keithley 2601 SMU was used as a constant current load. The measured peak efficiency is 85.3% for V_P = 2.35 V. However, except for V_{P0} = 1 V, the efficiency is quite similar. The efficiency loss with V_{P0}=1 V is mainly due to incorrect ZCS timing: the time for energy transfer from L_1 to C_{ST} is approximately proportional to the V_P/V_{ST} ratio and,

as charging progresses, it becomes comparable with the delay of the ZCS comparator and with the time required for detecting a negative (i.e. discharging C_{ST}) current on L_1. However, this is a necessary trade-off for reducing the intrinsic power consumption for operating with very low input power levels.

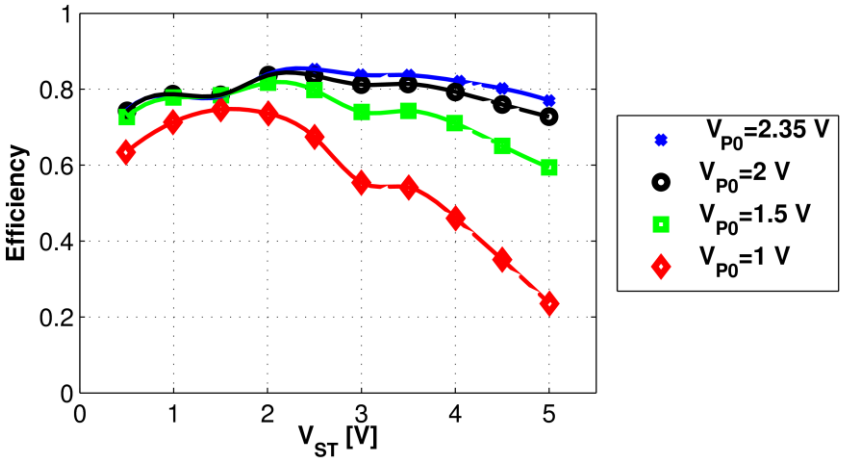

Fig. 26. Energy conversion efficiency for several values of V_{P0} at a frequency of 60 Hz with V_{DD}=2.7 V externally supplied. Component values in Table II.

The output power dependence from the equivalent load resistor is shown in Fig. 27. Data are obtained from the fifth experiment. The equivalent load resistance is evaluated by dividing the voltage V_{ST} by the current forced by SMU. The SMU current was chosen in order to obtain V_{ST} ranging from 500 mV (points on the left of Fig. 27) to 5 V (points on the right of Fig. 27), with steps of 500 mV. The dependency of output power from the load resistance is low, as expected from a SECE converter. In addition, two main effects can be observed. The first affects the output power (i.e. the energy transfer efficiency) for low value of load resistance and is caused by the increase of damping on the inductor L_1 current. This is due to the longer time needed for transferring the energy from L_1 to C_{ST} and to the smaller V_{GS} that turns on the M_{PB} p-channel MOSFET in Fig. 16 (part of switch S_{ST} in Fig. 16). On the other side, for higher load resistance (and thus V_{ST}) the main issue is due to the delay between the detection of the zero crossing of the inductor L_1 current and the turn-off of S_{ST}.

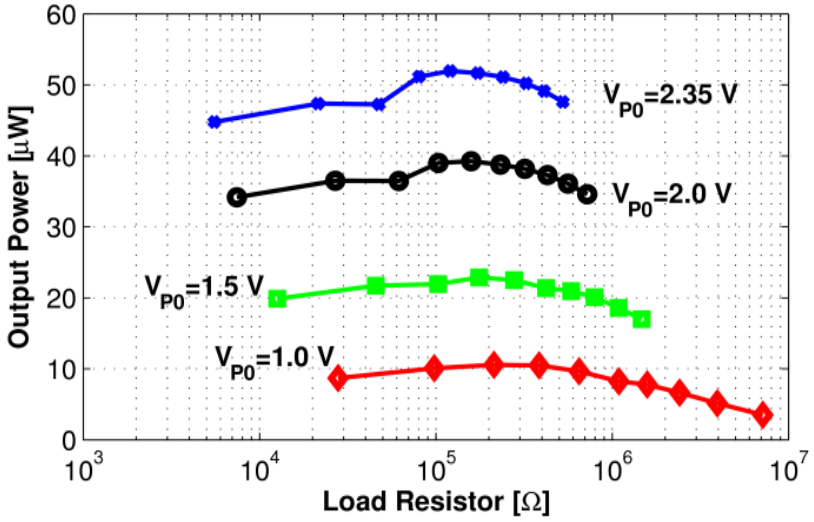

Fig. 27. Output power dependence on equivalent load resistance for different input voltage levels covering the allowed operating regions of the chip.

3.4.4 RCI

A sixth experiment has been used for the evaluation of the effectiveness of RCI and a comparison has been made with RCI enabled and disabled. After setting an operating point with V_{ST}=1 V and then with V_{ST}=2 V, the output power of the converter has been measured with RCI enabled and, at a later stage, with RCI disabled and for different values of piezoelectric open-circuit voltage V_{P0}. The output power has been measured with the same methodology as the efficiency in the previous paragraph. The ratios between output power with and without RCI are illustrated in Fig. 28 in which the theoretic value, computed as the ratio of (4) over (2) is also shown. As it can be seen, the output power increases up to three times and there is a satisfactory agreement with analytical values (red line) and measured points. The mismatch in this case is mainly due to the resistive losses on the RCI switches which do not allow to perform a full voltage inversion.

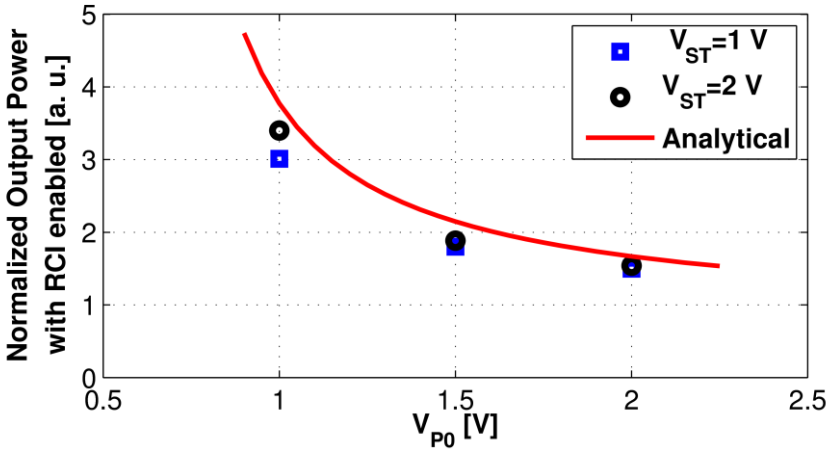

Fig. 28. Analytical performance improvement in output power of RCI and comparison with measured data on manufactured devices. For the analytical evaluation, V_T=0.6 V and the other component values are listed in Table II.

A comparison of the experimental results obtained on the designed converter with other recent works on SECE converters is shown in Table IV.

TABLE IV. COMPARISON OF INTEGRATED SECE IMPLEMENTATION.

Parameter	[41]	[84]	**IC presented in Chapter 3**
Technology	0.35 µm CMOS	0.35 µm CMOS and off-chip MOSFETs	0.32 µm BCD
Year	2012	2013	2014
Quiescent current	1.76 µA[1]	330 nA[2]	160 nA
Maximum input voltage	20 V	>70 V	5 V
Maximum output voltage	5 V	3.3 V	5 V
Features	PSCE	MS-SECE, TWS	RCI, TWS
Peak Efficiency	85%	61%	85.3% at V_P = 4.63 V

[1] Equivalent current estimated from reported power losses. [2] Equivalent current estimated from reported power consumptions.

Chapter 4
Low Voltage DC Energy Harvesting

The second presented interface is a power management IC for energy harvesting from low voltage transducers such as TEGs, PV cells. and the overall architecture is discussed in Chapter 4.1. It includes a self-supplied nano-power buck-boost converter with configurable FOCV MPPT, and its design is extensively portrayed in Chapter 4.2. As previously described for the converter in Chapter 3, the TWS has also been implemented. Moreover, a capacitive dc-dc boost converter has been designed in order to allow the start-up of the buck-boost converter from energy sources with output voltage as low as 223 mV. Such start-up unit (SU) is presented in Chapter 4.3. Finally, a linear regulator with low drop-out (LDO) has been included in order to provide a stable voltage to the load. The LDO design is illustrated in Chapter 4.4. The last part of the chapter shows the results of the experimental measurements performed on the manufactured samples and a discussion of such results is provided.

4.1 Architecture of Single Source Low Voltage DC Converter

The overall system architecture is shown in Fig. 1. The converter is composed of three main blocks: the start-up (SU) circuit, the main DC/DC buck-boost converter (MC) and a low drop-out regulator (LDO) in order to provide a stable voltage to the load. The IC requires an external inductor L_1 for the MC and four capacitors. The IC operates with two storage capacitors C_{DD} and C_{ST}, as in [83], [86]. The power conversion and management circuits are supplied by C_{DD} (IC supply), while C_{ST} provides the bulk energy storage (e.g. a supercapacitor) for the application circuits. This choice allows the use of a small capacitor for C_{DD}, which ensures faster activation times and independency from the energy stored on C_{ST}. The capacitor C_{buf} is employed as an energy buffer for MPPT, and C_{REG} provides LDO loop stability compensation and filtering. With the exception of C_{ST}, which is sized upon user application constraints, the other external capacitors have a small footprint and tiny

SMD components can be used. The inductor L_1 used by the MC should have a sufficient inductance value, and the chosen one is 10 mH. The reason of such value is the necessity of operating in discontinuous conduction mode (DCM) as energy is transferred from the energy source (ES) and from C_{buf} to C_{ST} or C_{DD} by exploiting resonant LC circuits. Low inductance values would lead to very fast switching periods, in the order of the hundreds of ns, which are not compatible with ultra-low power circuit consumptions.

As the minimum operating voltage of the MC is $V_{DDmin} = 1.36$ V, while the ESs considered in the thesis typically output $V_{DC} \leq 1$ V, a voltage booster circuit is required for initial start-up. The SU circuit is a fully integrated charge pump and has the purpose of charging C_{DD} from 0 V up to V_{DDmin}, where the MC can be started. At this point, the MC disables the SU circuit. In this phase, the power consumed by the SU is only due to leakage currents.

The IC has been designed in a STMicroelectronics 0.32 µm BCD technology, although only CMOS modules have been utilized in the design

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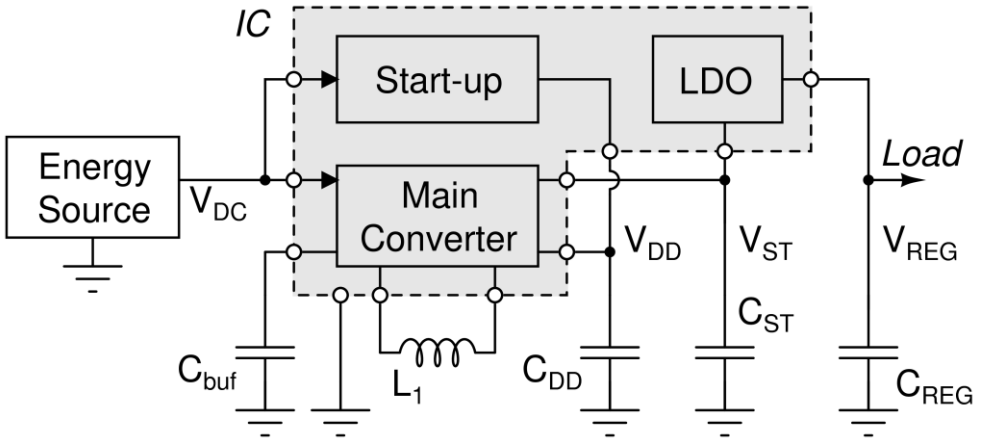

Fig. 29. Architecture of the low voltage converter.

4.2 Main Converter

The MC is basically a buck-boost converter and its circuit diagram is shown in Fig. 30. This topology was chosen in order to keep the ES disconnected from the energy storage, and to allow operation at MPP. It has been designed in order to draw a nominal quiescent current $I_{DDq} = 96$ nA at $V_{DD} = 1.4$ V. The reference current $I_{ref} = 16$ nA is generated by the bias block in Fig. 30. Such current is then mirrored and used as tail current in comparators, delay generators and under-voltage lock-out circuit (UVLO).

The MC is kept disabled by an UVLO circuit that triggers when V_{DD} rises above V_{DDmin} and enables the MC, which performs efficient energy extractions at MPPT. The UVLO provides an output $V_{UVLO} = V_{DD}$ when $V_{DD} < V_{DDmin}$, and $V_{UVLO} = 0$ V otherwise.

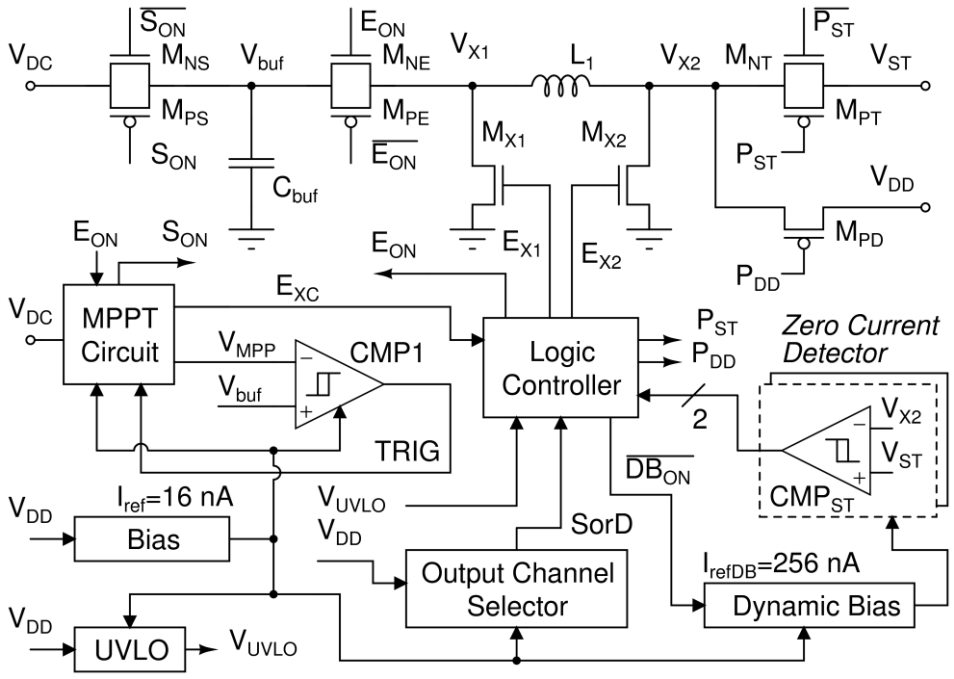

Fig. 30. Circuit diagram of the MC.

4.2.1 Two-way Energy Storage Policy

The MC has two possible output channels for the extracted energy stored in inductor: V_{DD} and V_{ST}. This power management policy has been named Two-Way Energy Storage. When the MC is active, C_{DD} gets progressively discharged. As long as the power budget is positive, the priority of the control logic of the MC is to keep V_{DD} over 2 V in order to remain in active mode. While the supply voltage V_{DD} is greater than 2 V, the extracted energy is directed towards C_{ST}. As V_{DD} drops below this value, the extracted energy is directed towards C_{DD} until it is recharged to 2.5 V. This mechanism, operated by the Output Channel Selector block in Fig. 2, allows a faster start-up as the SU needs to charge only C_{DD} to V_{DDmin}. The value used for C_{DD} is 200 nF and can be increased up to some µF, whereas C_{ST} is usually much larger due to applications constraints. Higher values of C_{DD} would increase the start-up time with no benefits on converter performance.

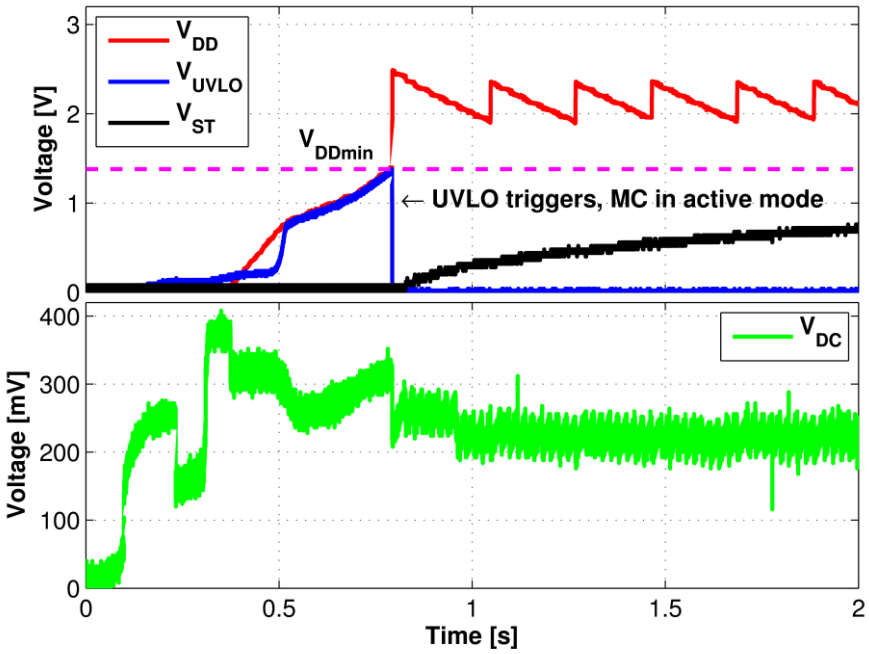

Fig. 31. Acquired waveforms of V_{DC}, V_{DD}, V_{ST}, and V_{UVLO} from an IC sample showing the start-up phase and the behavior of the two-way energy storage. The ES used is a tiny BPW34 photodiode under a table lamp, operated at the estimated MPP after the MC switches to active mode (V_{UVLO} falling to ground).

Moreover, the dual output channel topology allows C_{ST} to be completely drained if the LDO is replaced with a boost converter regulator. Other two-path architectures have been recently presented [84], where the supply voltage of the converter is directly linked to the voltage of the storage capacitor. Differently, the idea in the IC design of this chapter is to keep V_{DD} and V_{ST} independent, so that the intrinsic power does not increase with V_{ST}. The behaviour of this policy is shown in Fig. 31, where the acquired waveforms on an IC sample are reported. The benefit of a small value of C_{DD} is noticeable: V_{DD} rises quickly into its operative range while V_{ST} (C_{ST} = 33 μF) increases slowly.

4.2.2 Maximum Power Point Tracking

The chosen technique for MPPT is FOCV because it requires a very limited amount of energy for processing with respect to other techniques as it is based on intrinsic characteristics of the ES. The drawback is a limitation on the tracking accuracy. However, it allows saving power on the control circuit, so that the overall effect is advantageous. The selectable fractions of V_{DC0} are 75% for PV cells, 50% for resistive source and, additionally, 40% for non-linear rectennas, as observed experimentally in [34],[37].

The circuit diagram of the MPPT circuit is shown in Fig. 32. The open circuit voltage of the source V_{DC0} is sampled on C_S for the first time when the MC is activated (i.e. when V_{DD} rises above V_{DDmin}, as shown in Fig. 31). Then, the reference voltage V_{MPP} is generated by sharing the charge $Q_S = C_S V_{DC0}$ on the combination of appropriate capacitors chosen among C_{75}, C_{50} and C_{40}. The capacitor C_{75} is always used for V_{MPP} generation, whereas C_{50} is used only for MPPT at 50% and 40% of V_{DC0} and C_{40} is used only for MPPT at 40%: this approach allows to save silicon area. The capacitor values have been chosen in order to scale V_{DC0} to the appropriate value, according to the MPPT configuration. From then on, V_{MPP} is refreshed every 8 energy extraction cycles, in order to track voltage fluctuations, as shown in Fig. 33.

During normal operation S_{ON} and E_{ON} are low, so that $V_{DC} = V_{buf}$, and V_{buf} is compared with V_{MPP} (Fig. 2). An energy extraction cycle is started when the E_{XC} signal (i.e. the TRIG signal, disabled during the V_{DC0} sampling phase in order to

avoid undesired energy extractions, as shown in Fig. 3) goes high, i. e. when $V_{DC} = V_{MPP} + V_H$, where $V_H = 28$ mV is the hysteresis of comparator CMP1 in Fig. 30. The energy extraction from the ES (and C_{buf}) ends when $V_{DC} = V_{MPP} - V_H$. The ES voltage is kept in a window of size V_H centered in its approximated MPP. The maximum input voltage at MPP $V_{DC,max}$ is limited by the internal p-channel differential pair of comparator CMP1 [26]. The limit is due to the threshold voltage of the p-channel MOSFETs. This means that the limit on the open circuit voltage $V_{DC0,max}$ is $V_{DC0,max} = 2.5$ V with the MPPT circuit configured to operate at 50% of V_{DC0} and $V_{DC0,max} = 1.7$ V for MPPT at 75% of V_{DC0}.

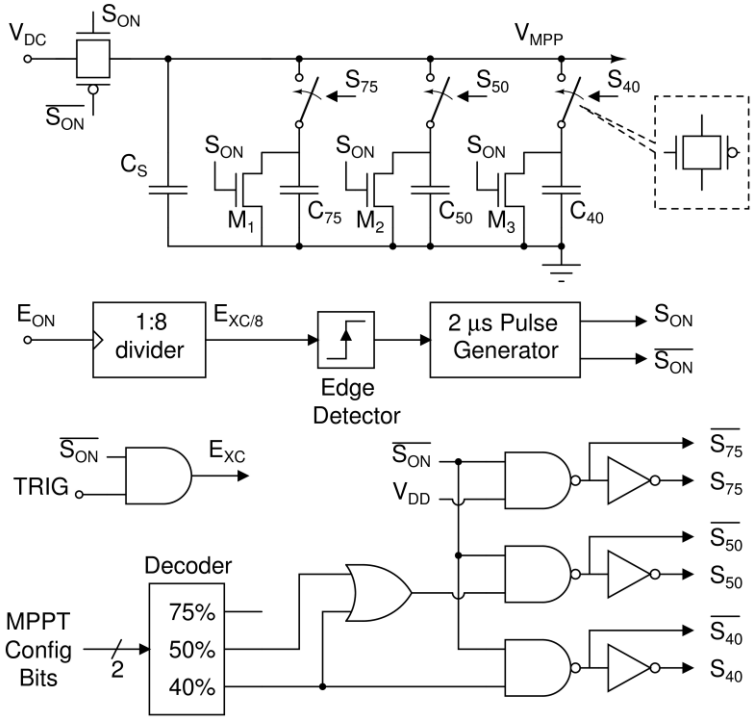

Fig. 32. Circuit diagram of the MPPT block that generates the reference voltage V_{MPP}. The diagram has been simplified and does not show the level shifters required for properly driving the p-channel MOSFETs of the CMOS switches.

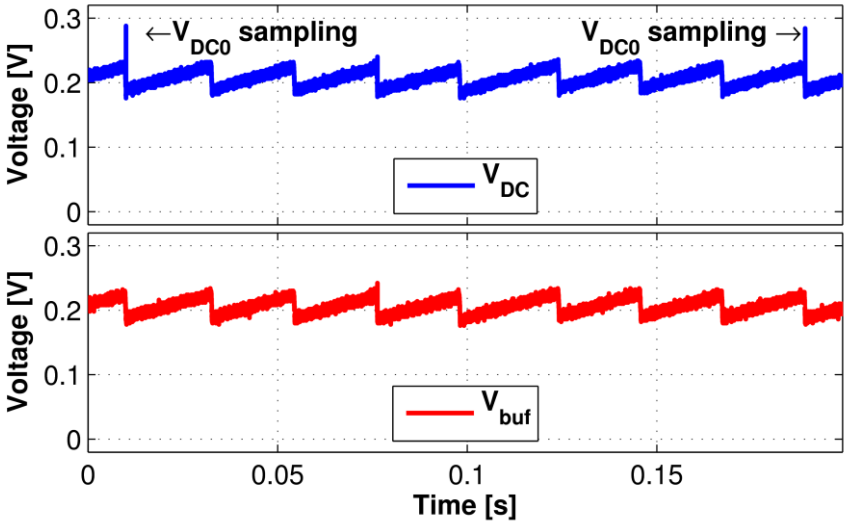

Fig. 33. Acquired waveforms of V_{DC} and V_{buf} from an IC sample showing the MPP being refreshed every 8 energy extraction cycles. The ES is a BPW 34 photodiode under the light of a table-lamp with a 50 W halogen lamp, half-power, at a distance of 45 cm. The noise on the waveforms is due to the oscilloscope (Tektronix MSO2024, no filter or bandwidth limitation).

4.2.3 Energy Extraction Cycle

During the first phase P1 (i.e. the corresponding of PHA in Chapter 3) of the energy extraction cycle, shown in Fig. 34, energy is transferred from C_{buf} and from the ES to the inductor L_1 by turning M_{X2} on and M_{X1} off. M_{NE} and M_{PE} are also turned on (E_{ON} signal high). In the second phase P2 (i.e. the corresponding of PHB in Chapter 3) of the cycle, M_{X2} is turned off and M_{X1} is turned on, so that energy flows from L_1 to the selected output capacitor, either C_{ST} or C_{DD}, while M_{NE} and M_{PE} are turned off. The process ends when the zero current switching is detected on M_{PT} or M_{PD}, depending on the selected power path. The output channel is selected with the signal SorD, which makes the logic controller choose the correct Zero Current Detector (ZCD, which is the same as the ZCS circuit in Chapter 3) with the signals P_{ST} and P_{DD}. Fig. 34 shows waveforms of V_{X1}, V_{X2}, V_{DD} and V_{buf} acquired during the energy extraction cycle after the UVLO has triggered (V_{DD} is shown to rise from 1.4 V). Phases P1 and P2 are highlighted along with the status of E_{ON}, M_{X1} and M_{X2}.

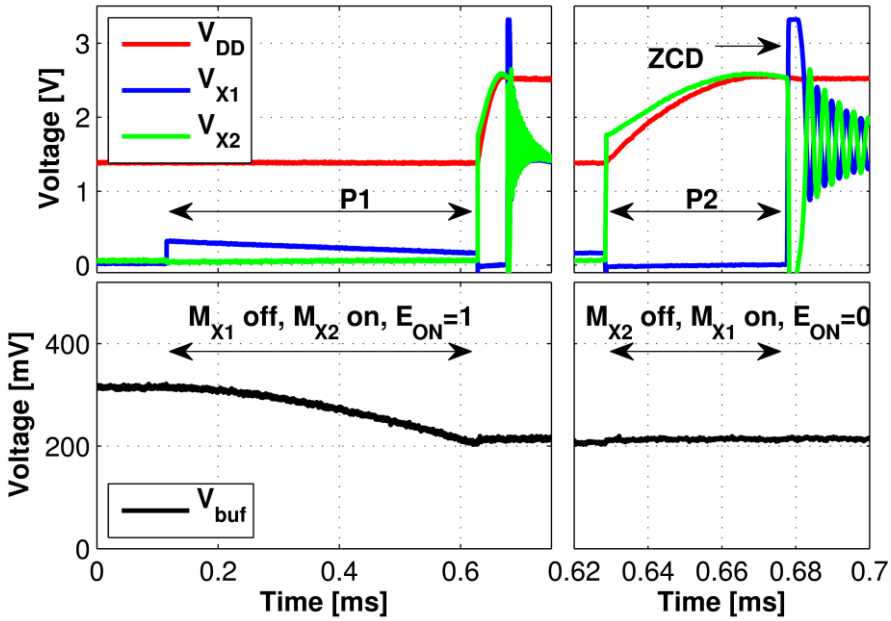

Fig. 34. Acquired waveforms of V_{DD}, V_{X1}, V_{X2} and V_{buf} during an energy extraction cycle. A zoomed view of the ZCD is illustrated on the right part of the figure. As it is the first energy extraction after the MC has switched to active mode, V_{ST} = 0 V.

The ZCDs are normally turned off and their static current is negligible, since they are biased by the Dynamic Bias block, which is activated only during energy extraction cycles by the Logic Controller (LC). However, in order to increase the comparator speed, the Dynamic Bias is set to provide a boosted bias current $I_{refDB} = 16I_{ref}$ (i.e. I_{refDB} = 256 nA) to ZCDs, in order to reduce their propagation delay.

4.2.4 Logic controller

A simplified circuit diagram of the LC is shown in Fig. 35. The LC implements a finite state machine that controls the energy extraction phases (represented by the state of P1 and P2 signals) and has been designed as a fully asynchronous logic block. This choice allows to spare the energy consumption due to clock generation and to minimize the delay between an event and the corresponding response. The. The LC also implements specific gate drivers (GD) circuits that provide a proper voltage for driving the p-channel FETs of the CMOS switches, either 0 V or the maximum

voltage available in the circuit. The RESET signal is generated from the high to low transition of V_{UVLO} and it used to clear all memory elements during the transition between passive and active mode in order to ensure the correct state of the circuit.

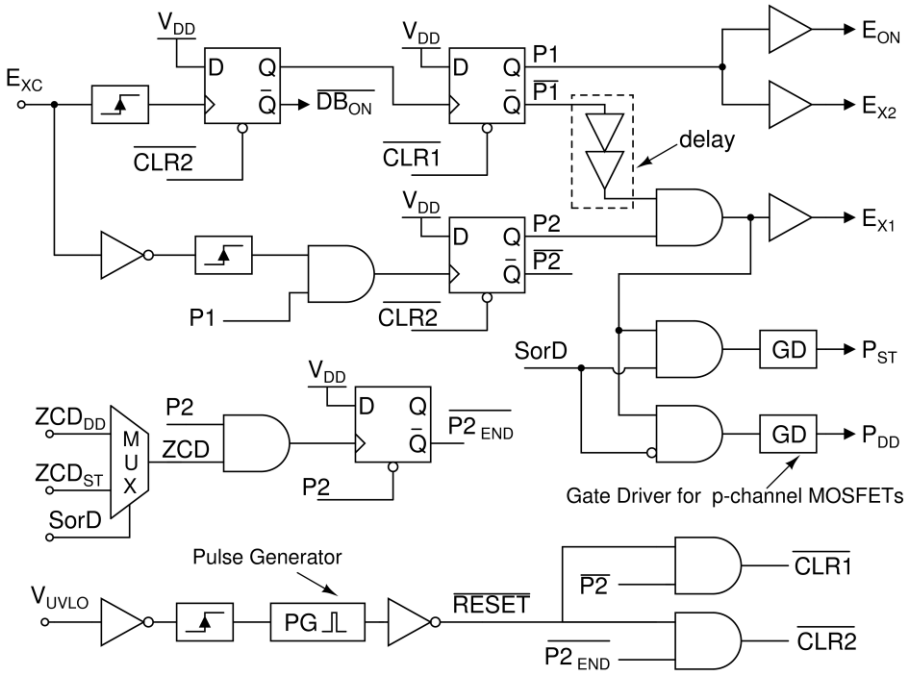

Fig. 35. Simplified circuit diagram of the LC.

4.3 Low Voltage Start-up

The SU is required in order to initially charge C_{DD} up to V_{DDmin}. It is a 16-stage charge pump based on [87] and its circuit diagram is shown in Fig. 36. The SU is supplied directly by the ES through the V_{SUin} pin. The output of the charge pump V_{SUout} is connected to V_{DD}. Low threshold MOSFETs have been used in the SU, in order to reduce down to about 200 mV the minimum value of V_{SUin} that allows $V_{SUout} \geq V_{DDmin}$. The number of stages has been evaluated from simulations in order to provide an output impedance lower than 14 MΩ at V_{SUin} = 0.25 V, which is the value of the input impedance of the MC seen from its power supply input port (V_{DD} and GND).

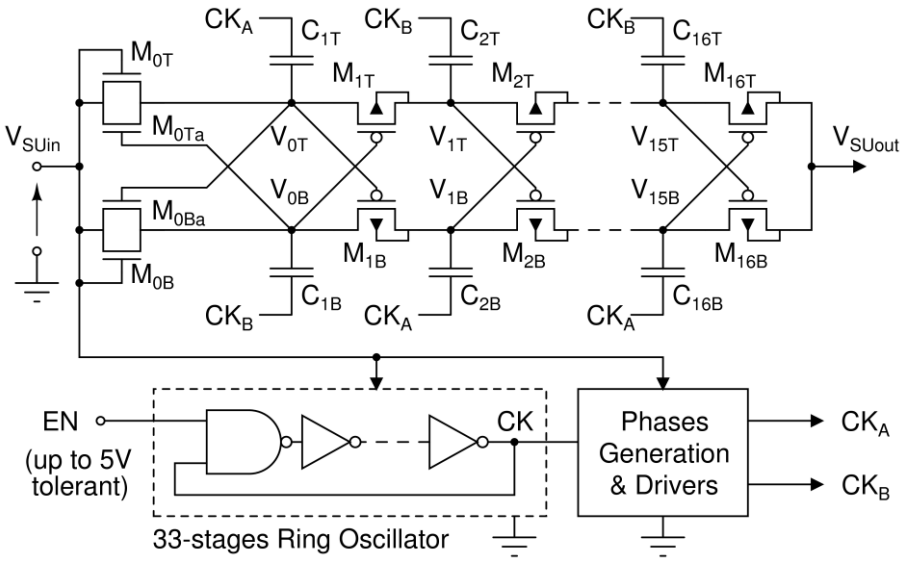

Fig. 36. Circuit diagram of the SU.

A 33-stage ring oscillator generates the clock signal *CK,* which is then used to generate the two phases required by the charge pump branches. The generated frequency f_{CK} depends on V_{SUin}. According to simulations, f_{CK} = 770 kHz at V_{SUin} = 250 mV. The ring oscillator can be disabled by driving the *EN* input to 0 V.

The active area of the SU is 0.192 mm^2. The 32 flying capacitors $C_{1T,}...C_{16B}$ are 2.52 pF each and occupy the 62% of the overall area of the SU. The remaining area is occupied by the buffers driving the CK_A and CK_B clock signals, and by empty space required to separate the n-wells of $M_{1T},\ldots,M_{15B}$ since each one of them is at a different potential.

The connection of the SU with the MC is shown in Fig. 37. The EN signal is connected to the ES through a resistor R_{ENS} = 44 MΩ, and to the V_{UVLO} signal through R_{ENU} = 0 Ω. The resistor R_{ENU} can be substituted with a short-circuit because, at start-up, the inverter driving V_{UVLO} is in a high-impedance state until $V_{DD} \approx 0.6$ V. As V_{DD} rises above this value, V_{UVLO} follows V_{DD}, keeping the SU active. When the UVLO triggers, V_{UVLO} = 0 V and also EN gets close to 0 V as R_{ENU} is far less resistive than R_{ENS}. In this implementation, for testing purposes, R_{ENU} and R_{ENS} are external resistors. The high resistance of R_{ENS} is necessary in order to cause only negligible perturbations on the ES, since the typical current drawn is less than 12 nA at

V_{DC0} = 0.5 V. However, they might be integrated, reducing the external components count, with an estimated area utilization of a fraction of mm^2.

Fig. 38 shows the waveforms acquired in a realistic case, where a start-up from V_{DC} = 0 V (V_{DC0} = 383 mV after the ES is illuminated) and V_{DD} = 0 V (V_{buf} and V_{UVLO} are 0 V by consequence) is performed. The ES is a 7.5 mm^2 BPW34 photodiode exposed at indoor light at time t = 0.1 s. In the initial phase the ES charges the parasitic capacitance, which is mainly due to the probe in this case, on the EN pin (i.e. the V_{UVLO} signal as R_{ENU} = 0 Ω) and, subsequently, the SU is then activated. C_{DD} and C_{buf} are charged. As V_{DD} = V_{DDmin}, the V_{UVLO} signal falls to 0 V and the MC is activated.

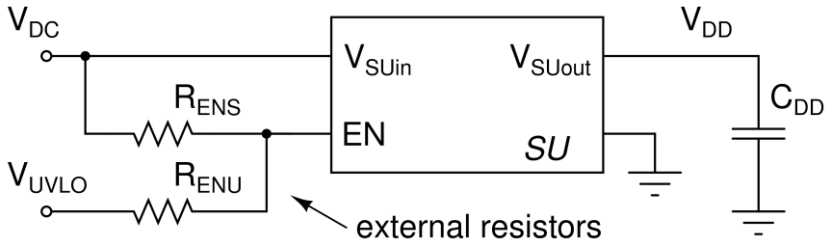

Fig. 37. Schematic of the connections of the SU block with the MC.

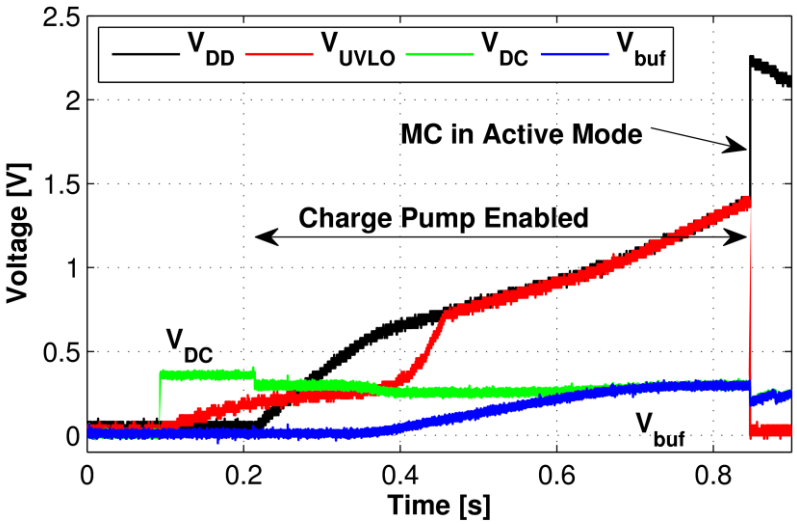

Fig. 38. Acquired waveforms of V_{DC}, V_{UVLO}, V_{buf} and V_{DD} during the start-up phase with a BPW 34 photodiode as ES. After the MC switches in active mode, the operation at MPP (set to 75% of V_{DC0}) is observable. External components values are: C_{DD} = 200 nF, C_{buf} = 22 µF, and C_{ST} = 33 µF.

4.4 Output Regulation

A low quiescent current LDO has been integrated in order to provide a regulated voltage to the load. The circuit diagram of the LDO is shown in Fig. 39. The circuit has been designed as an independent block and thus some of the bias circuitry of the MC has been replicated. The LDO draws a nominal static current of 251 nA. However, in a future version of the IC, sharing the bias block with the MC would reduce the static current to 203 nA. The LDO active area is 0.147 mm^2. Differently from existing nano-current commercial solutions [88], which use arrays of floating gate transistors programmed during manufacturing to precisely set the desired output voltage, the designed LDO uses standard CMOS. A single external capacitor with minimum value C_{REG} = 10 µF is required for ensuring stability.

The LDO has an external enable input (EN_{LDO} signal in Fig. 39). Moreover, the LDO features an internal UVLO that forces the transistor M_{PR} to be turned-off (i.e. V_{GR} is driven to V_{IN}) and thus forces, at steady-state, V_{REG} = 0 V. In a similar fashion to the MC, the UVLO disables the LDO if $V_{IN} \leq V_{DDmin}$. A second UVLO circuit, shown in Fig. 39, disables the LDO if there is not a sufficient input voltage, i.e. if $V_{IN} \leq V_{REG} + V_{SAFE}$, where the voltage V_{SAFE} is a safety margin set to about 350 mV. This feature, which can be externally disabled, has a positive effect on the energy budget of the system as it limits the static and leakage currents of both the load and the LDO when the input voltage V_{IN} is lower than required for operations.

The output voltage divider is fully integrated and is composed of a fixed resistor R_1 = 2.4 MΩ and a second resistor R_2, which is programmed by the configuration logic in order to provide the desired output voltage V_{REG}. The possible options for V_{REG} are 1.8 V, 2.5 V, 3.0 V and 3.3 V. The different values of R_2 generate the same current I_{fb} = 230 nA in each configuration. The overall nominal static current of the LDO is 481 nA. The LDO is stable in a no external load condition. A short-circuit protection with a current limit of 50 mA has also been implemented.

The generation of the reference voltage V_{REF} is based on the threshold voltage of the n-channel MOSFETs. V_{REF} is obtained from the voltage drop on two identical series connected transistors. The first one is diode-connected, with its drain and gate connected to V_{REF}. The second is used as a source degeneration with the gate

connected to V_{REF} in order to improve the independence of V_{REF} with respect to V_{DD}. The circuit is simple and effective in case a very high precise output voltage is not necessary. Results of Montecarlo simulations showed a standard deviation of 1.1% of mean value of V_{REF} at room temperature and V_{IN} = 2.5 V. This tolerance does account for the generation of V_{REF} and I_{ref} from the bias circuitry. However, it does not account for amplifier input offset, typically 7 mV, and for mismatch of R_1 and R_2, which can, however, be neglected.

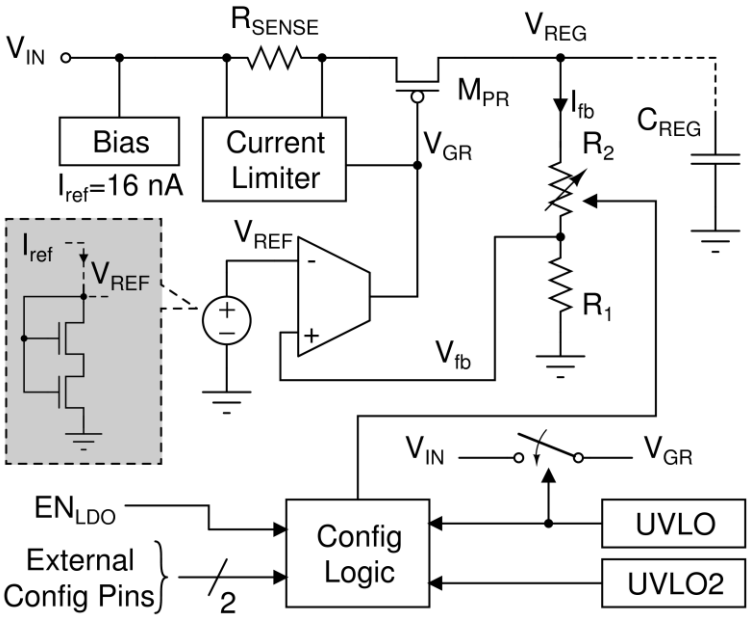

Fig. 39. Architecture of the low drop-out regulator.

4.5 Experimental Results

The experimental measurements in this section have been performed on samples of manufactured devices. A photograph of a manufactured die and of a packaged sample (CLCC68 package) is shown in Fig. 40 together with a BPW34 photodiode with 7.5 mm^2 of active area that was used for functional testing. The die area, a substantial part of which is taken by the pad ring, is 4.58 mm^2 while the active areas are respectively 0.588 mm^2 for the MC, 0.192 mm^2 for the SU, and 0.147 mm^2 for the LDO. The total active area is 0.93 mm^2.

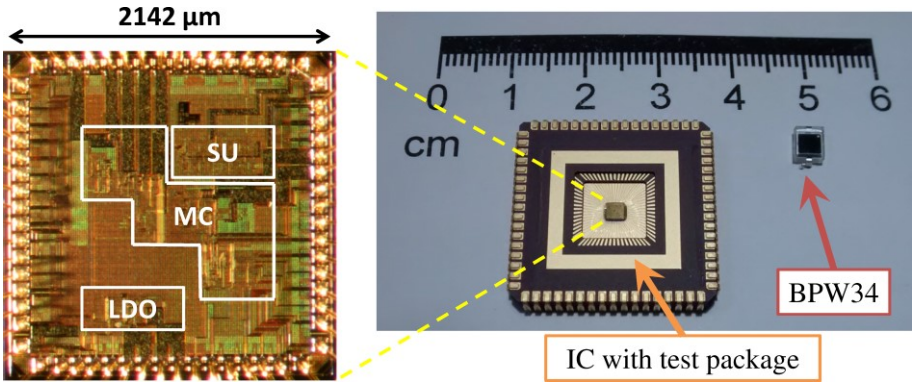

Fig. 40. Die micrograph and photograph of a packaged IC sample and of a BPW34 photodiode used as ES.

4.5.1 Functional tests

Functional tests has been performed with a BPW34 photodiode as ES, which was illuminated by a 50 W halogen lamp placed over the photodiode at a distance of 45 cm. The maximum output power of the ES at 75% of V_{DC0} = 373 mV was 14.8 µW (measured with a Keithley 2601A SMU). The external components of the circuit are C_{DD} = 200 nF, C_{ST} = 33 µF, C_{buf} = 32 µF, L_1 = 10 mH.

Fig. 38 shows the acquired waveforms of V_{DD}, V_{ST}, V_{DC} and V_{UVLO} with the aforementioned setup: the two-way energy storage policy can be clearly seen as V_{DD} quickly enters in its operative range after the start-up phase while V_{ST} raises slowly as $C_{ST} >> C_{DD}$. Fig. 38 shows the same process, acquired in a second time, with the focus on the operations of the SU and the subsequent energy extraction at MPP after the UVLO trigger. In a third test, the waveforms associated to the MPPT circuit have been recorded, in order to show the periodic refresh of the open circuit voltage V_{DC0} (depicted in Fig. 33) and the waveforms of inductor nodes V_{X1} and V_{X2} during an energy extraction cycle of the MC (depicted in Fig. 34).

4.5.2 Quiescent current

Firstly, the characterization of the MC is presented. The first measurements is the converter quiescent current and it has been measured with a Keithley 2601A SMU forcing V_{DD} and is I_{DDq} = 121 nA at V_{DD} = 2.0 V, while I_{DDq} = 101 nA at V_{DD} = 1.4 V

(i.e. slightly above V_{DDmin}, when the MC is in active mode). The equivalent input resistance R_{MC} of the MC seen from its power supply input and corresponding to its intrinsic current consumption, is useful for validating the SU, as it allows to estimate whether the SU can sustain the MC during the start-up phase. In order to characterize R_{MC}, the quiescent current I_{DDq} has been measured in a range of V_{DD} values closely centered on V_{DDmin}. Fig. 41 shows the measured values of R_{MC} and its minimum value is R_{MCmin} = 10.28 MΩ at V_{DD} = 1.36 V.

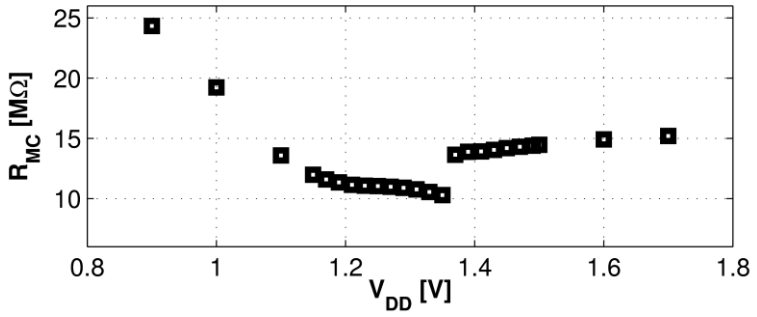

Fig. 41. Measured input resistance R_{MC} of the MC. The abrupt variation of R_{MC} at V_{DD} = 1.36 V (i.e. V_{DDmin}) is due to the change of state of the UVLO circuit.

4.5.3 Efficiency

In a second experiment the converter efficiency has been also investigated at different input power levels and voltages V_{DC0}. For this purpose, a constant current was sunk from V_{ST} with a SMU in order to set the output voltage at a desired value. The efficiency was assessed as the ratio between the output power flowing from the V_{ST} node and the maximum theoretical input power (i.e. $V_{DC0}^2/4R_S$). Five input configurations are shown in Fig. 42. In order to better control source characteristics, in these measurements the ES has been emulated with a voltage source with a series resistance and with the FOCV MPPT circuit configured at 50% of V_{DC0}. The MC has been tested with five different input configurations with input power ranging from 10.5 µW to 437 µW, with several values for V_{DC0} (from 248 mV up to 1.6 V) and R_S (from 267 Ω up to 4.607 kΩ). The parameters of the ES used in each measurement are shown in the legend Fig. 42. The chosen value of R_S are comparable with the resistance of several low-voltage transducers (e.g. BPW34, Micropelt MPGD751,

[34], [37]). The measured peak efficiency is 77.1% when the MC is self-supplied, i.e. the system is fully autonomous, whereas it reaches 79.3% if V_{DD} is provided externally (V_{DD} = 2.4 V). This results highlights, as discussed beforehand, the efforts made in order to reduce the power consumption of the MC, mainly the static one. The converter efficiency has a strong dependency on the input voltage V_{DC}. However, this can be mitigated, in a future version, by increasing the conductivity (i.e. the size) of the switches M_{NE} and M_{PE} at the cost of a slight increase of dynamic switching consumption. Another aspect that influences the MC efficiency is the relationship between the amount of energy E_{CYC} extracted per cycle and the ZCD delay: such delay has a noticeable effect on efficiency when $V_{ST} \geq 3.5$ V as it becomes comparable with the duration of phase P2 and, if the operations at $V_{ST} \geq 3.5$ V are prevalent, an improved ZCD circuit should be used. This effect is more evident when the A simple solution would be an increase of I_{ref} in order to reduce the propagation delay of comparator CMP_{ST}. However, in micro-power applications this does not represent a significant limitation because external circuits can operate at lower supply voltages.

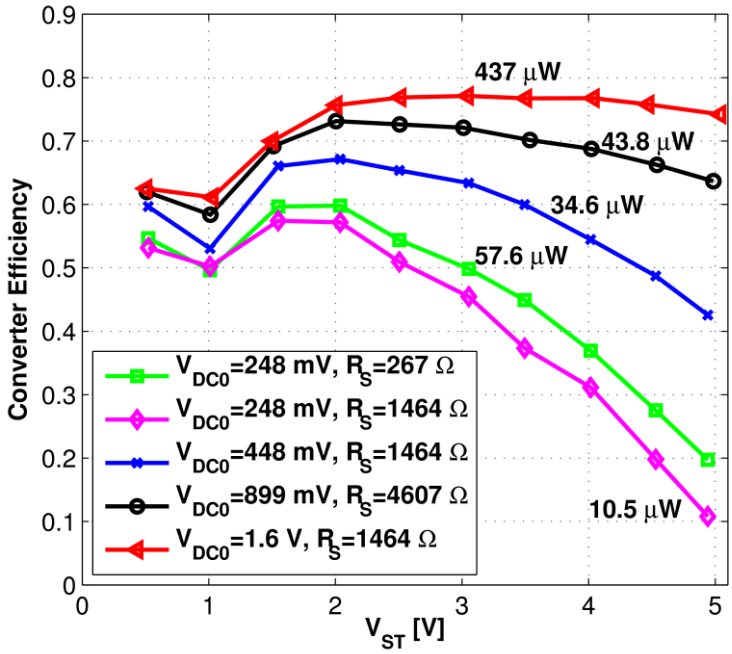

Fig. 42. Measured efficiency of the MC for different power levels (input voltage V_{DC0} and series resistance R_S). The reported efficiency is related to the self-supplied MC.

4.5.4 Energy per conversion cycle

In a third experiment, the energy E_C drawn by the MC during an energy extraction cycle has also been measured. In order to evaluate the MC dynamic consumption, the MC has been externally supplied (V_{DD} = 2.4 V) and the average current drawn I_{avg} has been measured with an Agilent E34401A multimeter as the drop voltage on a 6.8 kΩ sense resistor. The frequency f_e of energy extractions was also measured with a digital oscilloscope. The dynamic current I_{dyn} drawn by the MC is then obtained by subtracting I_{DDq}. E_C can be evaluated from measurements as:

$$E_C = V_{DD}\left(I_{avg} - I_{DDq}\right) f_c^{-1} = V_{DD} I_{dyn} f_c^{-1}, \tag{4.1}$$

The MC uses E_C = 6 nJ (at V_{DD} = 2.4 V and V_{ST} = 1 V) to perform a complete energy extraction cycle while supplying the LC, the analog circuits, and the switch drivers. However, when V_{ST} rises above 2.5 V, some energy is subtracted also from C_{ST}, mainly for activation of the switches. This may reduce the energy drawn from C_{DD}, but also increases the overall energy consumption. However, E_C also depends on the choice of external components as C_{buf} and L, on the series resistance R_S, and on the open-circuit voltage V_{DC0} of the ES.

4.5.5 Minimum and maximum input power

The minimum input power, required for sustaining active operation of the MC, once the MC has started, has been investigated in a fourth experiment. The source was emulated with R_S = 1464 Ω and a decreasing V_{DC0} until the circuit ceased operating. A minimum input power of 935 nW, computed as $V_{DC0}^2/(4R_S)$, was found at V_{DC0} = 74 mV. In this case, no power was delivered to C_{ST}. However, such a low V_{DC0} voltage does not allow the MPPT circuit to work efficiently as the voltage swing required for conversion is comparable with V_{DC0}. The swing of V_{buf} (and hence V_{DC}) has been measured as 42.5 mV, which is the 57.4% of the open circuit voltage V_{DC0}. Data elaboration from acquired waveforms showed that the average input power from the ES was, in the experiment, about 838 nW, with a drop of 10% with respect to theoretical maximum.

The maximum input power that can be handled by the MC has been experimentally evaluated in a fifth experiment. An ES was emulated with R_S = 267 Ω and an increasing V_{DC0} until the circuit ceased operating. A maximum input power of 4.95 mW was found at V_{DC0} = 2.3 V, R_S = 267 Ω, and with C_{DD} = 200 nF, C_{ST} = 33 µF, C_{buf} = 32 µF, MPPT at 50%. The voltage on V_{ST} settled at 3.15 V with a load resistor of 3227 Ω connected to V_{ST}. The MC was self-supplied and the net output power has been measured as 3.07 mW, with an efficiency of 62%. However, an optimum output load was not used. This power limit is mainly due to the time required for energy extraction (energy transfer between RLC circuits) and can be increased by reducing the inductance value of L_1: the drawback is a decrease of efficiency, especially for V_{ST} > 3 V, due to ZCD delay as shown in Fig. 42.

The maximum input voltage $V_{DC0,max}$ allowed by the converter has been investigated in a sixth experiment and the MC operates correctly up to V_{DC0} = 2.5 V, with R_S = 4.7 kΩ and the MPPT configured at 50%.

4.5.6 Start-up Circuit

Fig. 43 shows the steady-state output voltage of the SU for several values of V_{SUin} with a load R_{SUL} = 10 MΩ on V_{SUout}. The load R_{SUL} was imposed by the Agilent E34401A multimeter used in the tests, and is suitable to emulate the MC (R_{MCmin} = 10.28 MΩ). The minimum measured voltage required by the SU to reach $V_{SUout} \geq V_{DDmin}$ is 223 mV for R_S = 1.46 kΩ. In order to verify the ability of the SU to supply the MC, the output resistance R_{SUout} of the SU, which can be modelled as a voltage source with a series resistance R_{SUou}, has been evaluated from two different sets of measurements. The first set was obtained with R_{SUL} = 10 MΩ, whereas the second set in open circuit with R_{SUL} > 10 GΩ, corresponding to an additional setting of the multimeter. The obtained results are illustrated in Fig. 44. The minimum value of R_{MC} (i.e. R_{MCmin}) is highlighted in the graphs and shows that R_{SUout} is always lower than R_{MC} in the useful input voltage range (V_{SUin} > 223 mV), especially when $V_{DD} \leq$ 1 V, hence the designed SU is suitable as start-up block for the MC.

The efficiency of the SU, evaluated in a further experiment as the measured output power on a 10 MΩ load divided by the measured input power, has also been

investigated and the results are depicted in Fig. 45. However, the low efficiency of this block is not an issue as the SU is not the main energy path from the ES to C_{ST}. It must only provide the conditions (i.e. $V_{DD} = V_{SUout} \geq V_{DDmin}$) for the start of the MC, whenever the system falls in a fully discharged state.

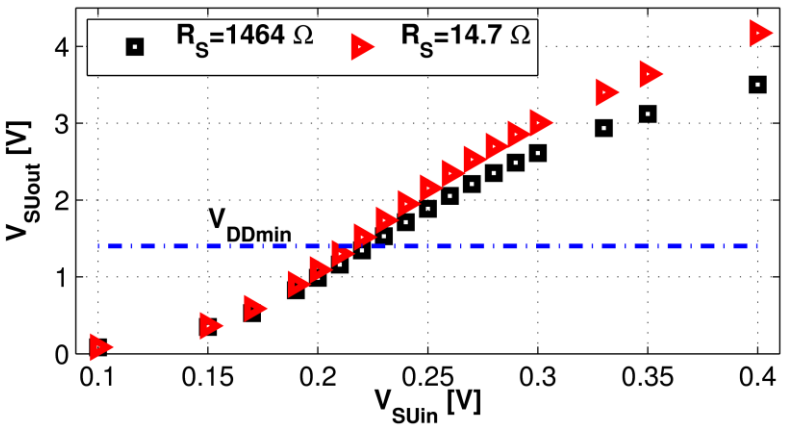

Fig. 43. Measured V_{SUout} with a load of 10 MΩ as a function of V_{SUin} and source resistance R_S.

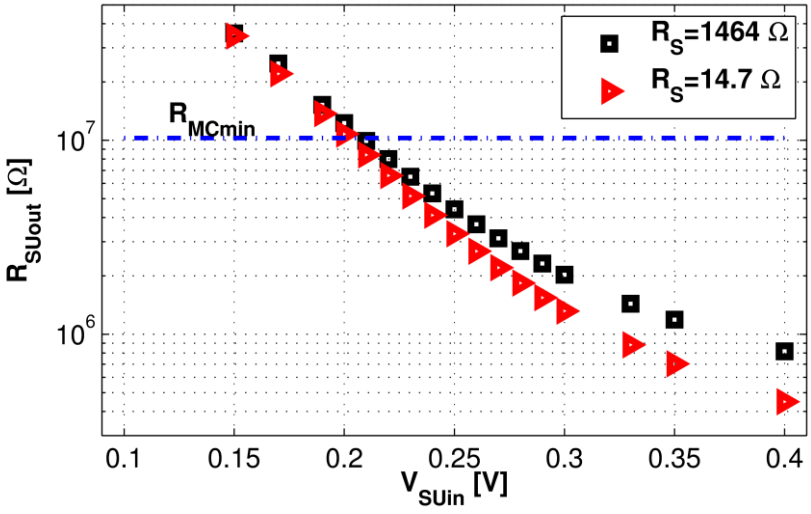

Fig. 44. Measured output resistance R_{SUout} of the SU in different input conditions.

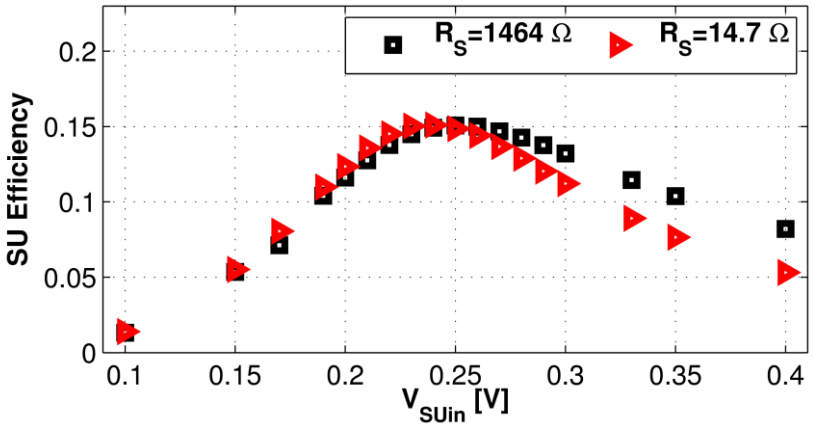

Fig. 45. SU power conversion efficiency

4.5.7 Low Drop-out Regulator

The performance of the LDO has been tested. Fig. 46 shows the measured quiescent current of the LDO for each output voltage. The graph clearly illustrates the operation of the UVLO that disables the LDO output and limits its quiescent current to the expected value (i.e. 251 nA). However, the LDO quiescent current graph discloses a dependency on V_{IN} much stronger than expected from simulations.

Another set of experimental measurements has been performed on 12 samples of the IC in order to verify the output voltage spread with respect to the nominal value. The measured average output voltage is about 7.2% lower than in simulations for each configuration. The standard deviation is 1.9% of the nominal V_{REG} value. Hence, the circuit is suitable for applications that do not require a high precision. However, since the standard deviation is quite low, as highlighted in Fig. 47, the normalized output values are quite close to the average value with low dispersion.

The line regulation of the LDO is less than 10 mV/V with a load current of 1.17 mA and V_{REG} set to 1.8 V. The measured load regulation, with the same set-up, has been measured to be 5.31 mV/mA, with a load current variation from 1.17 mA to 115 µA.

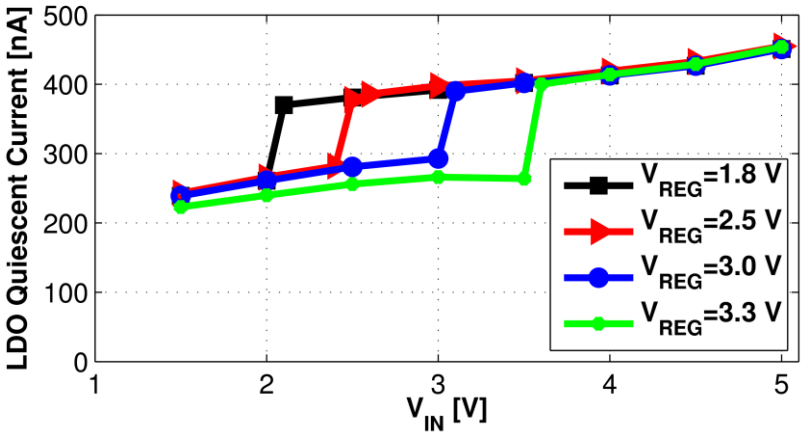

Fig. 46. LDO quiescent current for each output voltage configuration.

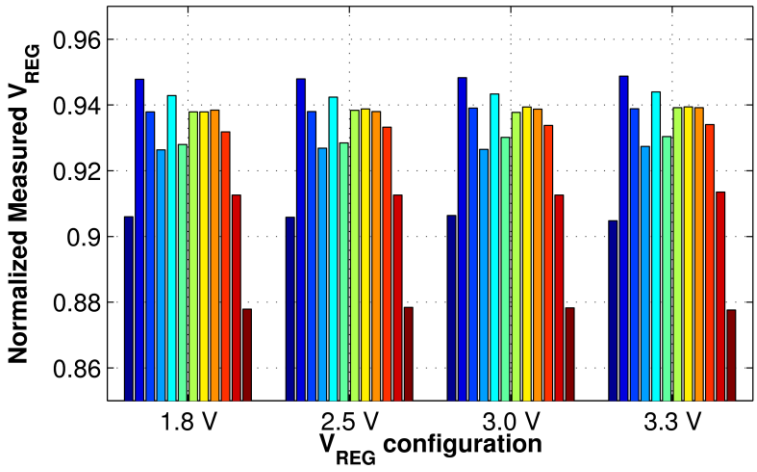

Fig. 47. Measured V_{REG} with a 10 MΩ load in each configuration (1.8 V, 2.5 V, 3.0 V, 3.3 V) normalized to the nominal V_{REG} value from simulations.

4.5.8 Results Discussion

A comparison of the experimental results obtained on the designed converter with other recent works on converters for energy harvesting is shown in Table V.

The obtained results from experimental measurements show that custom and tailored circuits for energy harvesting allow to achieve a high conversion efficiency even with very limited input power levels (tens of µW). A future work for the IC

performances improvement may consider the optimization of switches sizing in order to reduce their on-resistance, at the cost of a larger die area. Moreover, an optimization of the ZCD scheme can help to mitigate its effect on efficiency for $V_{ST} > 3.5$ V, the range in which the efficiency is deteriorated as shown in Fig. 42.

TABLE V. RECENT NANO-POWER ICS FOR ENERGY HARVESTING APPLICATIONS

Work	Source	Type of converter	Additional features	Quiescent current/power and P_{MIN}	Efficiency	Input voltage range
[27]	RF	Buck	MPPT with on-off time regulation, V_{OUT} regulated with APL comparator	181 nA, P_{MIN} = n.a.	< 95%	1.2-2.5 V
[29]	DC	Charge pump	Dynamic body bias, adaptive dead time	< 0.5 μW, P_{MIN} = n.a.	34%/72% at 0.18V/0.45V	> 0.15 V
[23]	DC	Boost	FOCV MPPT, battery charger, cold start-up	330 nA, P_{MIN} = 5 μW	38%/>80% at 0.1 V/5 V	80 mV – 3 V (330 mV startup)
[30]	TEG	Boost	Variation-tolerant FOCV MPPT, no output voltage regulation, battery required	n.a., P_{MIN} = n.a.	72%	70-600 mV
[20]	PV	Boost	On-chip PV cell, double-boost converter	n.a., P_{MIN} = 1 μW	65 %	> 0.5 V
[22]	PV	Battery Charger	Reconfigurable circuit power and speed	390 nW, P_{MIN} = n.a.	90 %	0.9-2 V
[26]	TEG, PV, PZ	Boost converter	Single shared inductor with asynchronous arbiter logic	431 nA (9 sources), P_{MIN} = 3 μW	89.6 %	< 5.5 V (1.4 V startup)
This work	DC	Boost converter	Asynchronous control logic, fast battery-less startup, nanopower LDO	121 nA, P_{MIN} = 935 nW	77.1 %	74 mV-2.5 V (223 mV startup)

n.a. No data available.

Chapter 5
Heterogeneous Multisource Energy Harvesting

The last chapter describes the third designed converter and the results of experimental measurements are discussed. The integrated power converter is an energy harvesting buck-boost for multiple and heterogeneous energy sources [26]. The architecture of the converter is analysed and a description at system and circuital level is provided of each channel type (i.e. either AC and DC channel are implemented) in the first five sections. Then, the maximum power capabilities of the IC are analysed and discussed. The sixth and last section of the chapter illustrated the experimental measurements performed on manufactured samples, providing a comparison with the state-of-the-art of multisource power converter for energy harvesting and insight on converter efficiency, static consumption and dynamic energy required for a single energy extraction.

5.1 Architecture

The block diagram of the proposed buck-boost converter IC is shown in Fig. 48. It features nine input channels, five of which are dedicated to PZ and the remaining four to DC sources. Among the DC input channels, two of them are dedicated to high voltage (HV) sources with $1\ V \leq V_{DC0} \leq 5\ V$, while the remaining two are optimized for low voltage (LV) sources, typically with $100\ mV \leq V_{DC0} \leq 1\ V$. Energy can be extracted simultaneously from up to 9 sources and transferred into the energy storage device (e.g. a supercapacitor). A high number of channels was deployed in order to demonstrate the high scalability of the proposed approach and the negligible impact on intrinsic consumption of the power converter. However, unused channels can be disabled. Multiple input channels allow simultaneous energy extraction from multiple and heterogeneous transducers such as PZ, TEGs, RF harvesters and PV cells, in

order to guarantee energy coverage with intermittent sources. A specific feature is the buck-boost converter core shared among all the channels, in order to limit die area and energy absorption; moreover, this allows the use of a single external inductor. The inductor value is critical: low values, e.g. tens of µH, require a high reactivity of the switching circuits leading to high power consumptions, while high values, e.g. some mH, translate into a bulky inductor, not suitable for extreme miniaturisation.

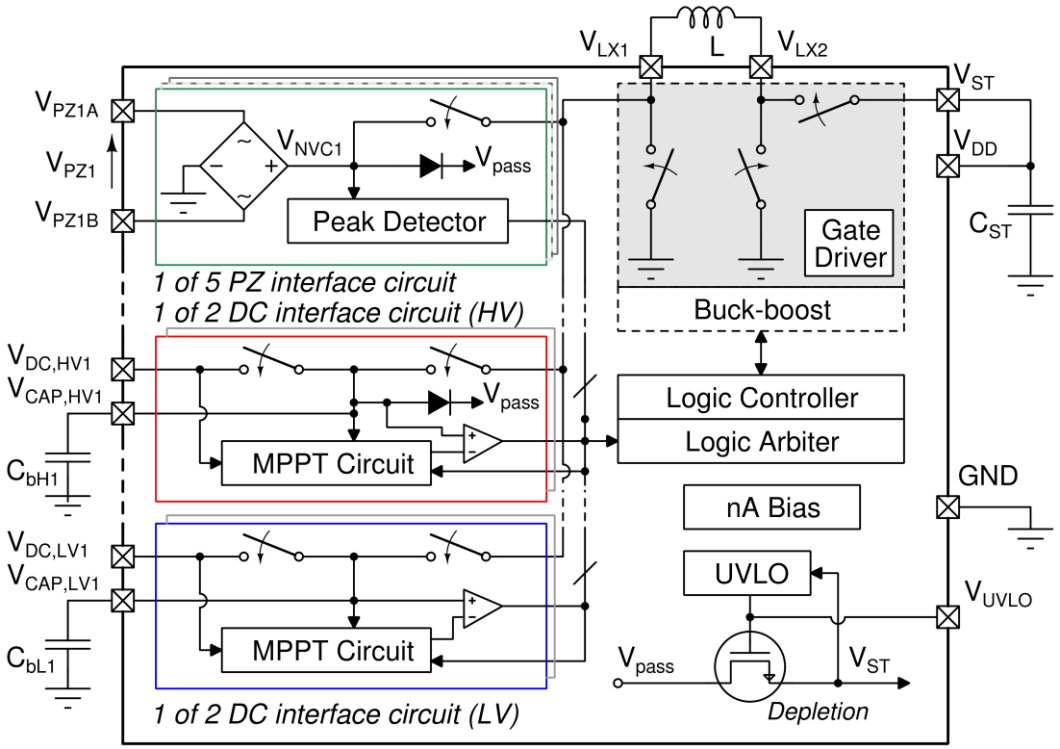

Fig. 48. Block diagram of the proposed heterogeneous multi-source converter.

The supply voltage V_{DD} of the converter and the energy storage output V_{ST} are shorted in order for the converter to supply itself with the harvested energy, leading to a fully autonomous solution. The energy stored in C_{ST} is also available to an external load such as a low dropout regulator (LDO) supplying a WSN node. In a more complex design like a system-on-chip (SoC), the LDO can be directly integrated within the same chip together with all application circuits. In the following sections of the paper, V_{ST} will be referred to as the energy storage voltage, whereas V_{DD} as the supply voltage of the converter. Moreover, where not specified, the bulk terminal of

MOSFETs has to be considered connected to V_{DD} or GND for p-channel and n-channel MOSFET respectively.

The IC, as the ones described in Chapter 3 and Chapter 4, has been designed in a 0.32 µm BCD technology from STMicroelectronics. All the transistors in the schematics should be assumed to be 5V MOSFET except otherwise noted. In addition to standard 5V CMOS devices, low threshold CMOS and n-channel depletion MOSFET have been used. The IC has been designed as a general-purpose building block for ultra-low-power systems, compatible with both integrated and discrete electronics. It can also fit into a SoC design as the harvesting core of the IC is based on standard MOS transistors. In case a depletion-mode MOSFET is not available in the chosen technology, it can be replaced by a standard n-channel MOSFET. However, a secondary DC/DC such as a charge-pump would be required in order to provide a sufficient gate voltage to make it conductive initially at the expense of increased complexity, silicon area and leakage current.

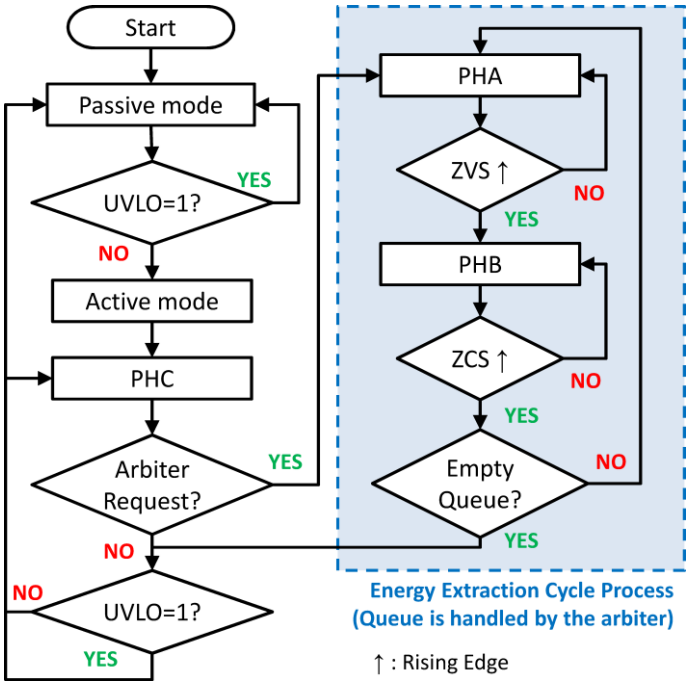

Fig. 49. Control flow-chart of the system.

The converter starts to operate in passive mode, in which V_{ST} and V_{pass} are shorted by a depletion n-channel MOSFET which acts as a normally-closed switch (Fig. 48). All the PZ and HV DC sources are connected to V_{pass} through a diode, so that in discharged states current may flow to C_{ST} through the depletion-mode MOSFET. As V_{ST} rises, the output of an under-voltage lock-out (UVLO) circuit starts following V_{ST}, in order to keep the depletion-mode MOSFET conductive. Such path is then cut off by driving the gate of the depletion MOSFET to 0 V as soon as the UVLO triggers (V_{UVLO} is high during start-up in passive mode), nominally at $V_{DD} \geq V_{DDmin}$ (V_{DDmin} = 1.38 V nominal), as this ensures that the supply voltage is high enough for every circuit block to start active operation.. The control flow-chart of the system is depicted in Fig. 49 where the phases of an energy extraction cycle are illustrated, together with the transitions between passive and active state.

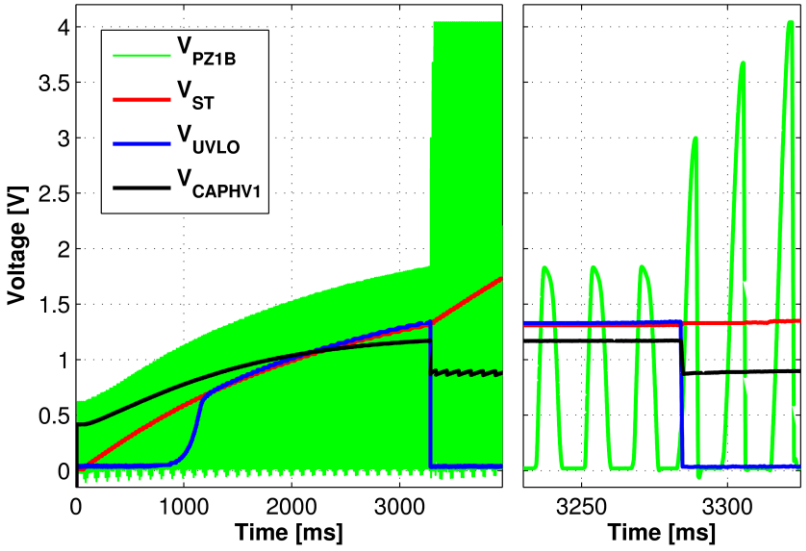

Fig. 50. (left) Start-up of the proposed converter from a zero energy state (V_{ST}=0 V) showing passive and active operating regimes and (right) close up during the transition. Waveforms are acquired from real transducers and a sample of the manufactured IC.

Fig. 50 depicts a real-world scenario with the initial start-up of the converter described in this paper and measured with stimulated devices: a Q220-A4-303YB PZ (acceleration $a_{RMS} = 0.164g$, $V_{PZ}(t) = 4.1\sin(128\pi t)$ V, $C_P = 52$ nF) from Piezo

Systems and an Ixys KXOB22-01X8 PV module (indoor laboratory light, $V_{DC0} = 1.2$ V) contribute to charge $C_{ST} = 33$ µF. Energy is at first passively harvested and active operations start as soon as $V_{ST} \approx 1.38$ V, i.e. on the UVLO signal V_{UVLO} falling edge. The latter phase can be easily recognized in the left part of Fig. 50 by the clipped sinusoids on PZ trace that extend their amplitude once SECE is started.

5.2 PZ Channels Interfaces

Fig. 51 shows the schematic of the interface for PZ. This block is replicated for each PZ input channel (i.e. five times). The depletion-mode n-channel MOSFET driven by V_{pass} ensures the previously introduced battery-less start-up from discharged states. The first stage of the circuit interface is the enhanced NVC (eNVC) of Fig. 7. The PZ voltage is tracked by the peak detector (Fig. 10) which identifies the local maxima of $V_{NVC}(t)$, i.e. the peaks of $V_{PZ}(t)$, and feeds the control logic, which activates energy extraction on the involved channel by activating $V_{CONVACTIVE}$. In case of simultaneous requests of energy extraction cycles, the delay of the conversions due to the queuing introduced by the control logic has no significant impact on the amount of extracted energy because the duration of each charge extraction is normally significantly shorter (i.e. less than 0.1%) than the PZ oscillation frequency.

When a conversion is started, phase PHA is applied (Fig. 2) by closing the M_{SP}-M_{SN} switch, so that C_P is discharged through L. The gate of M_{SP} requires a specific gate driver which performs a level shift on its digital control input, driven by the logic controller, from V_{DD} to the highest possible voltage among V_{DD}, V_{NVC} and V_{LX1}, in order to ensure that M_{SP} is completely turned off between energy extractions (phase PHC), so that no charge is transferred among sources. This is of utmost importance because the inductor terminal V_{LX1} is shared among all input channels. The gate of M_{SN} is driven at V_{DD} supply voltage level as M_{SN} carries most of the current when V_{NVC} is less than about 1 V.

One of the main challenges in the design of the converter was related to the huge number of variable voltage supplies for each channel and their sub-block, in particular regarding the gate drivers of the p-channel MOSFET switches. A

remarkable care has been used in order to prevent activation of bulk diodes caused by variations of voltage supplies. Similarly, ESD protection devices on pad-ring have been connected to an internal floating rail with protections instead to V_{DD} (or V_{ST}). In this way the voltage of PZ and HV DC sources is allowed to swing at a voltage higher than V_{DD} (or V_{ST}) and preventing charge to flow to V_{DD}. Otherwise, efficiency (for PZ) and correct operations (for HV DC sources) would be compromised.

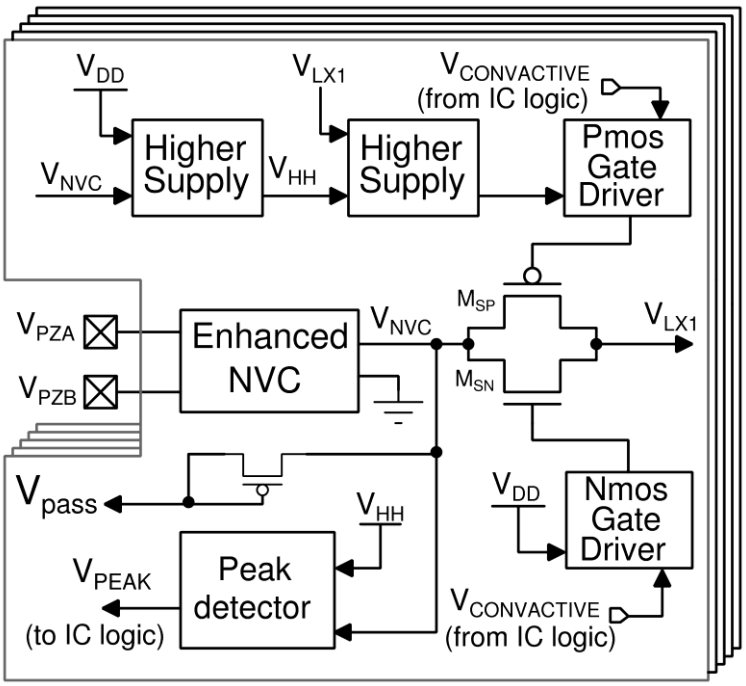

Fig. 51. PZ channel interface circuit diagram.

5.3 DC Channels Interfaces

The main task of the interface circuit for a DC channel is the control of energy extraction from the transducer performing MPPT. The FOCV MPP technique requires a voltage reference $V_{FOCVref}$ obtained as a particular fraction of V_{DC} at open circuit (i.e. V_{DC0}). An external pin $V_{MPPconf}$ is tied to V_{DD} or ground in order to select a

fraction of 50% or 75%. A sample and hold circuit has been designed for this purpose and is depicted in Fig. 52. V_{DC0} is sampled on C_S by closing S_{SAMP} for 2 µs. Then, the charge of C_S is shared with C_{H75} (or C_{H50} depending on $V_{MPPconf}$) by closing the switch S_{H75} (or S_{H50}) in order to set $V_{FOCVref}$ to the desired value. The value of C_S=3 pF has been chosen as a trade-off between charging time, in order to allow compatibility with high impedance sources, and both noise immunity and leakage, in order to reduce $V_{FOCVref}$ drift over time while maintaining an high MPPT accuracy. After C_S, the values C_{H75} = 1 pF and C_{H50} = 2 pF were chosen. $V_{FOCVref}$ is refreshed every eight energy extraction cycles in order to quickly track fluctuations on V_{DC0} and, at each refresh, C_{H50} and C_{H75} are discharged. The quiescent current of the reference circuit is only due to the leakage of transistors in the order of some pA. Differently from other MPPT schemes which can draw as much as 5 µW [25], [32], the implemented MPPT scheme offers a negligible power loss at the cost of a slightly lower accuracy on the MPP, resulting in an convenient trade-off for sources in the µW range.

The schematic of the interface circuit for a DC channel is depicted in Fig. 52 and is composed of a MPPT circuit for the generation of $V_{FOCVref}$, a comparator CMP_{DC} (which is, referring to Fig. 6, of type (d) for LV channels and of type (c) for HV channels), and an HS circuit (only for HV channels).The switches S_{CAP} and S_{CONV} are built exactly alike the switch connecting V_{NVC} and V_{LX1} (M_{SN} and M_{SP}) in Fig. 51. S_{CAP} is always closed except during the refresh operation of the threshold $V_{FOCVref}$. This allows the converter not to stop during the update of $V_{FOCVref}$. S_{CONV} is a normally open switch which is closed only during the phase PHA of an energy extraction cycle. Whenever V_{CAP} exceeds $V_{FOCVref}+\Delta V_{hystDC}$, CMP_{DC} activates power conversion (phase PHA), which is stopped when V_{CAP} drops below $V_{FOCVref}-\Delta V_{hystDC}$ (phase PHC). In order to reduce intrinsic consumption, only in phase PHA the associated CMP_{DC} tail current is boosted according to the comparator type by the control logic, increasing temporarily the speed of the comparator itself.

Like in the PZ interface circuit, the gate of p-channel MOSFET in the switches requires to be driven with the highest available voltage for an effective cut off, then HS circuits are implemented between V_{LX1}, V_{ST} and V_{CAP}.

The acquired waveforms from a LV DC source depicted in Fig. 53 show the periodic refresh of $V_{FOCVref}$ every 8 energy extractions and the amplitude of hysteresis ΔV_{hystDC}.

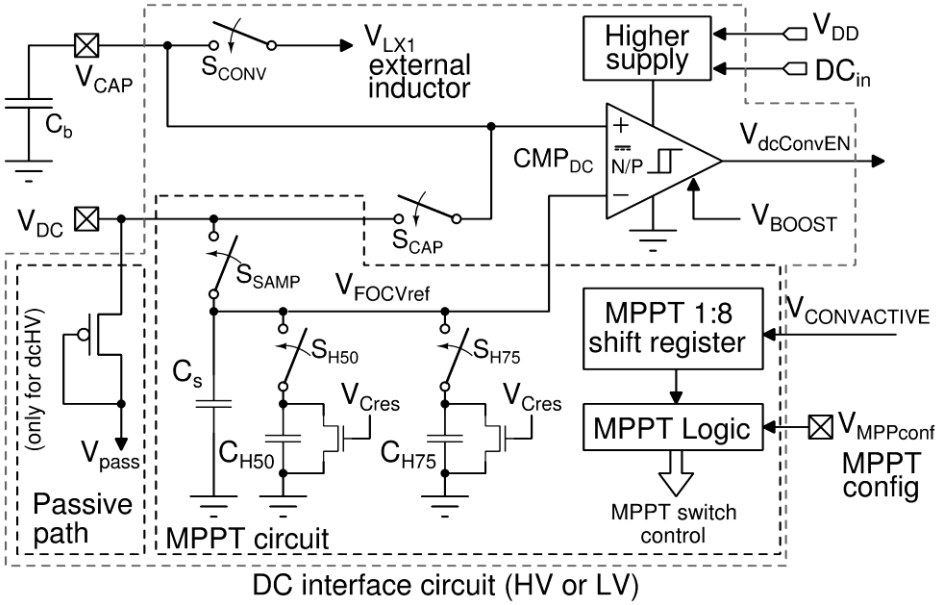

Fig. 52. MPP threshold generator circuit diagram.

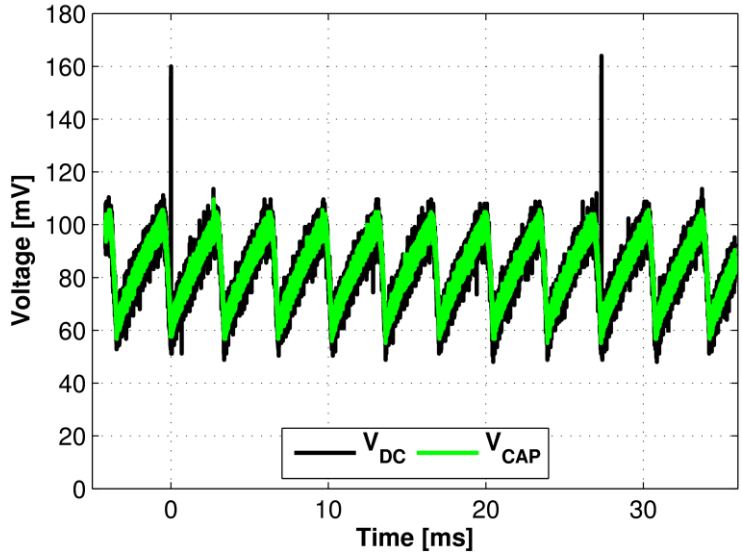

Fig. 53. Acquired waveforms on a LV-DC channel from a Micropelt MPG-D751 TEG chip heated with a fingertip at room temperature (V_{DC0}= 160 mV, C_{bLI}=22 µF) showing MPP tracking and the refresh of the MPP threshold $V_{FOCVref}$ every 8 energy extractions.

5.4 Buck-boost Converter

The buck-boost converter core (Fig. 54) has been carefully designed in order to minimize energy consumption per operation and to guarantee a robust system. The buck-boost core is shared with all the input channels and is mainly composed of an analog section, the switches with their respective drivers, and a logic controller implemented as a finite state machine (FSM). The three MOSFET switches of the buck-boost converter (M_{X1}, M_{X2}, M_{XA}) are sized to achieve a trade-off between dynamic power consumption and on-resistance, which affects conversion efficiency. Such switches are driven by the output signal of the FSM which marks the correct timings of each phase (PHC, PHA and PHB). The transition from state PHC to state PHA is determined by a start signal generated by the arbiter when an energy extraction cycle is requested by one of the sources. The analog section consists of two comparators (CMP_V, CMP_I) and a bias generator to dynamically increase the bias current of CMP_V, CMP_I in order to reduce their propagation delay. The bias generator has a full shutdown feature: no current is drawn by the buck-boost circuits when the converter is in idle (V_{biasON} signal high) state whereas the bias is set to 16Iref during PHA and PHB (V_{biasON} signal low). This dynamic biasing policy offers on one hand a very low quiescent current and on the other hand a fast response time only when needed. In fact the propagation delay t_{pd} of CMP_V and CMP_I decreases, according to simulations, down to 0.74 µs and 0.78 µs respectively (Table I). The analog section of the buck-boost core draws no current during PHC and draws 1.2 µA during PHA and PHB. However, PHC typically last longer than PHA and PHB and the system remains in idle state (PHC) whenever there is no energy to harvest.

The converter detects at run-time the end of both PHA and PHB, therefore the system is self-adapting to arbitrary energy transducers (i.e. C_P for PZ and R_S for DC), to the value of the chosen passive components (C_{ST}, L and all four buffer capacitors C_b of DC sources), and to the value of V_{ST} which affects the duration of PHB. The start of PHA is requested by individual input channel interfaces and granted by the control logic (according to the $V_{CONVactive}$ signal). The end of PHA and the contextual start of PHB happen on the zero-crossing of V_{LXI} by CMP_V (signal ZVS, Zero Voltage Switching) whereas the end of PHB is detected by CMP_I (signal ZCS, Zero Current

Switching) when drain-source voltage of M_{XA} (V_{ST}-V_{LX2}), which is used as a current sense resistor, becomes lower than -V_{hyst} (i.e. current is flowing from C_{ST} to GND trough the inductor L). Zero voltage and current detection implemented on custom microelectronic circuits grant a significant degree of flexibility at the expense of few tens nW. This represents a clear advantage over existing solutions where timings are statically determined [16].

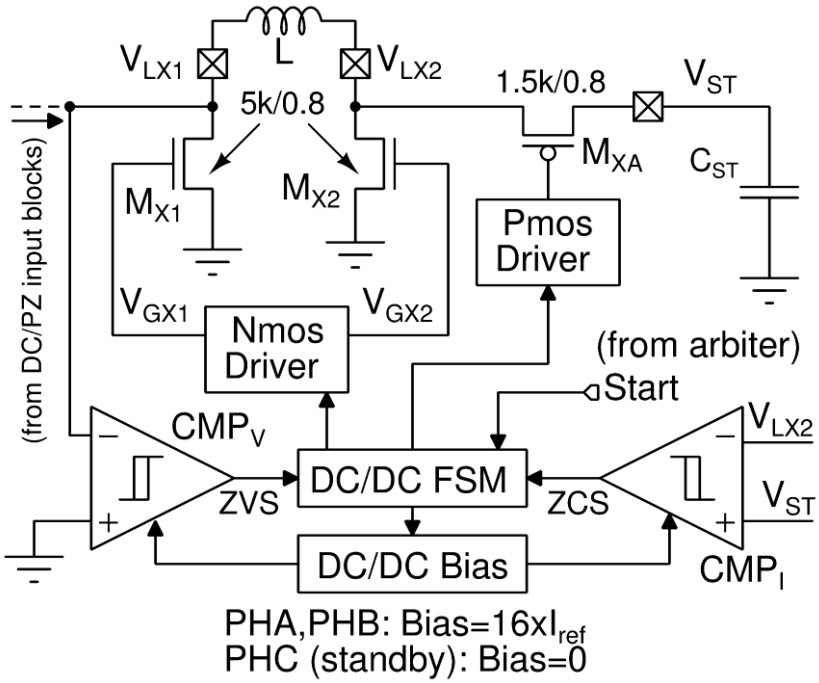

Fig. 54. Buck-boost core circuit diagram.

The inductor L is kept shorted to ground in idle state for preventing false triggering of CMP_V and CMP_I, for dissipating possible unwanted residual energy on L without producing ringing on V_{LX1} and V_{LX2}, and for easing correct state detection on CMP_V and CMP_I for a new energy extraction. The switch M_{XA} is closed (i.e. the gate is driven to V_{ST}) directly from the logic controller through the set input of a D-type flip-flop. The output of CMP_I is used only for the detection of the opening condition and operates directly on the clear input of such flip-flop. Such designed control methodology prevents oscillation and multiple switchings of M_{XA} at the end of PHB which may lead to unstable operations and a worthless switching activity increasing

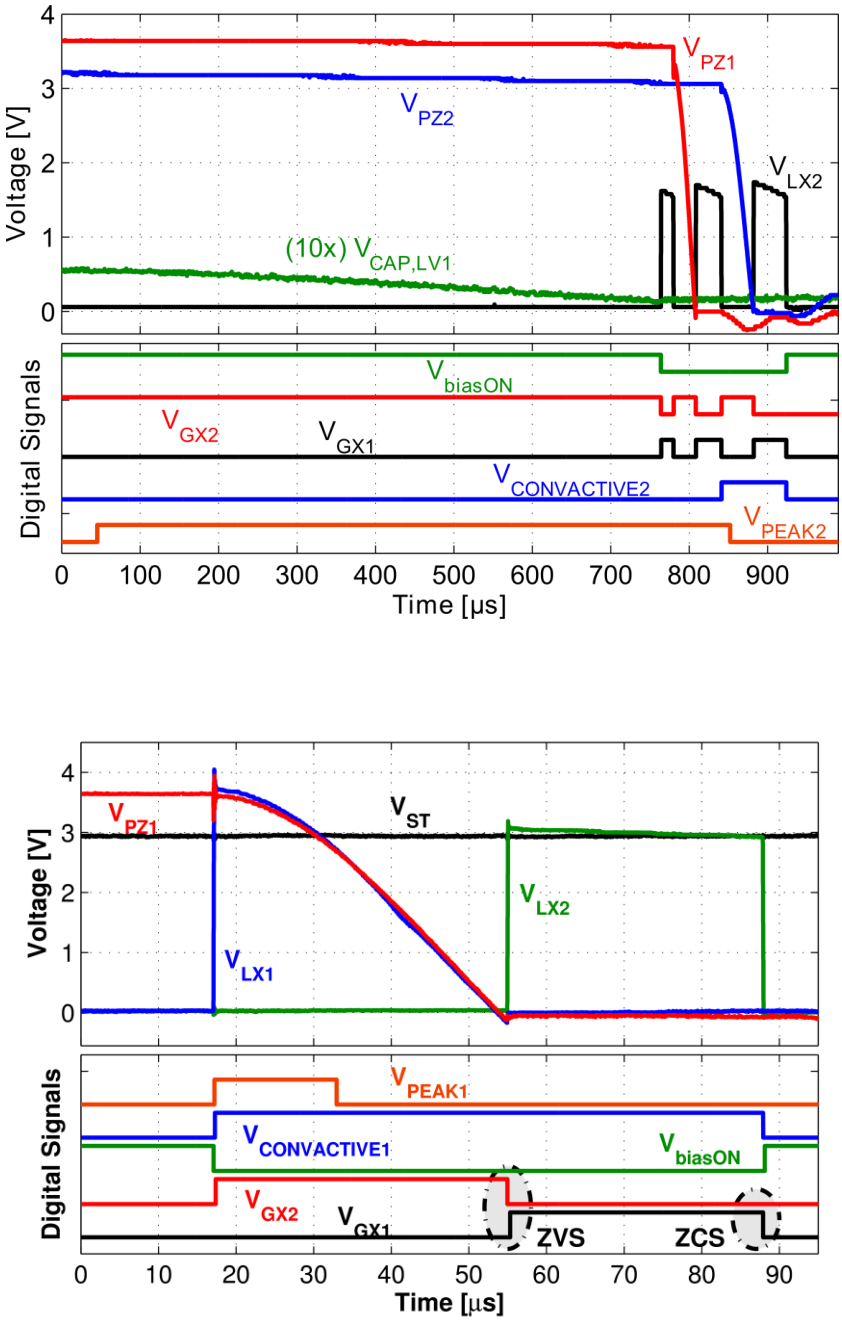

Fig. 55. (top) Example of acquired signals during simultaneous requests of energy extraction from a LV-DC channel and two PZ channels obtained from real transducers. (bottom) Waveforms and internal signals acquired during an energy extraction cycle from a PZ. ZVC and ZCS signals are not directly shown and their effect on the buck-boost converter is highlighted in gray ellipses (transitions from PHA to PHB due to ZVS and transition from PHB to PHC due to ZCS).

dynamic power. A typical scenario for simultaneous energy extraction cycles is shown on the left of Fig. 55 where two PZ (Q220-A4-303YB from Piezo Systems with about 7 g tip mass, f=60 Hz and a_{RMS}=0.164g) have been stimulated through an electrodynamic shaker while a Micropelt MPG-D751 was heated with a fingertip (cold plate at room temperature). Waveforms were acquired with a digital oscilloscope. An additional measurement with a single PZ (with the same parameters from the previous measurement) has been performed in order to show waveforms and signals of the buck-boost core and the acquired data are shown on the right of Fig. 55.

5.5 Arbitering of Multiple Sources

An important block of the system is the logic arbiter. It manages all nine channels and serializes the accesses to the buck-boost converter core. In case two or more sources concurrently request the execution of an energy extraction cycle, the arbiter chooses the one with the highest priority and creates a priority-based queue for the remaining requests. The priority has been selected at design stage with the PZ channels having higher priority over DC channels. Moreover, PZ on channel 1 has the highest priority over PZ, followed by channel 2, channel 3, and so on. A simplified diagram of the arbiter circuit is shown in Fig. 56.

The arbiter is composed of sub-arbiters which grant priority in this order: first the A channel, then B, and at last C. Sub-arbiters are sequential circuits with their internal memory (i.e. edge-triggered flip-flops) used to generate and store the queue. A combinational logic (i.e. chains of and gates) processes the state and the requests in order to select the most priority channel. The outputs of the sub-arbiters A_{out}, B_{out} and C_{out} are all ‘0’ or mutually exclusive (e.g. if A_{out} is ‘1’, B_{out} and C_{out} are ‘0’) with the output corresponding to the chosen active channel set to ‘1’. If new requests arrive when another output is active, the sub-arbiter waits for the current selection to be completed before changing its state. Looking at the top-level arbiter, the structure of priorities is highlighted. Then, priority is wired in the circuit. The sub-arbiters communicates among them with a start-stop signaling.

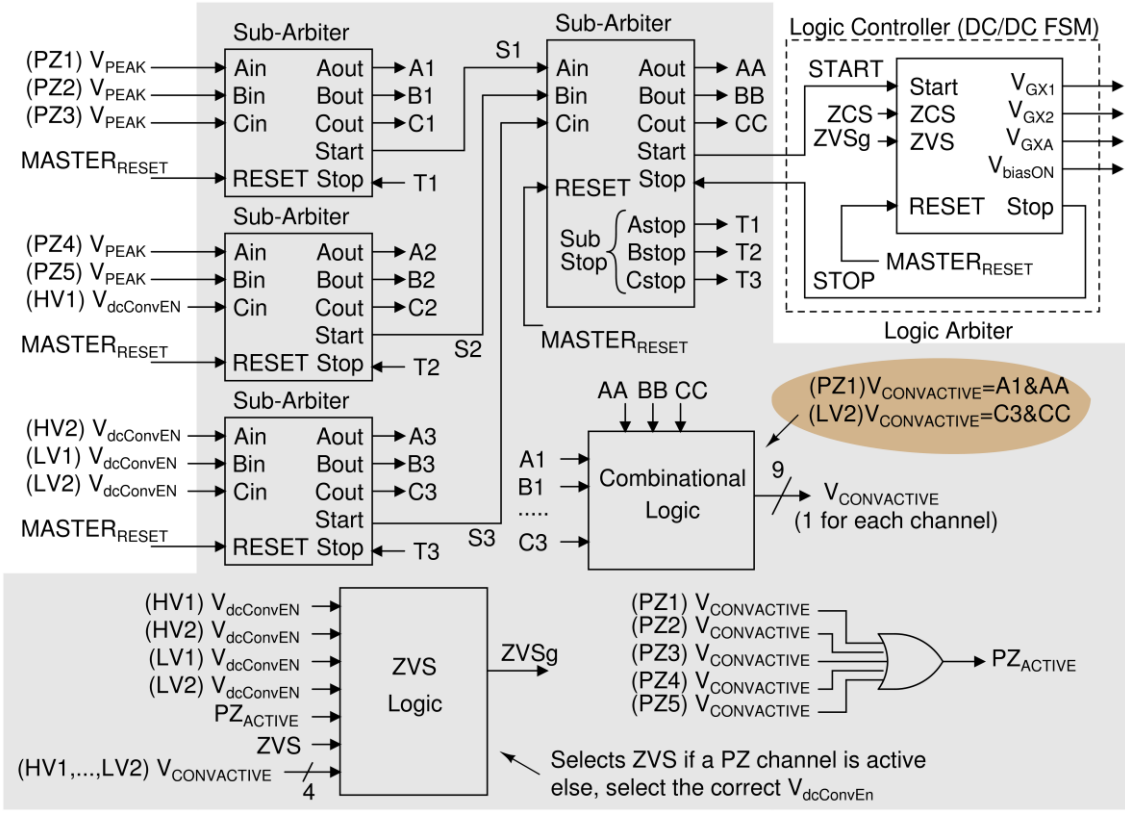

Fig. 56. Simplified schematic of the logic arbiter and logic controller (DC/DC FSM). For the sake of simplicity, the generation of $V_{CONVACTIVE}$ has been exemplified for two cases. The operations of the ZVS combinational logic is explained in the note.

Asynchronous logic is exploited in order to minimize energy consumption in both logic arbiter and logic controller, implementing a finite state machine (FSM) which handles the phases PHA, PHB and PHC. The global reset signal $MASTER_{RESET}$ (Fig. 56) is used to reset all the logic at the transition between passive and active mode in order to avoid false triggering of energy extractions.

Clock-less digital circuits can exploit their maximum speed without the energy overhead necessary for clock signal generation and distribution, which can easily be quantified in some µW for a clock frequency of 125 kHz at a supply voltage of 3 V, corresponding to a low consumption scenario. An additional drawback of a clocked circuit would be the discretization of the converter switching times: low clock frequencies would consume less power but would lead to a loss of conversion efficiency because of timing inaccuracies.

The implemented logic does not provide information on the power levels of each source to external devices such as a microcontroller unit (MCU). However, for DC sources this could be implemented by: (i) providing the MPP voltage to an ADC of the MCU and (ii) by placing a counter for each channel and by incrementing it at every energy extraction. Then, through a communication interface, a MCU may read such values and their variations over time.

5.6 Analysis of Maximum Input Power

The converter has been designed for energy harvesting applications with input power ranging from tens to hundreds of μW. Furthermore, the converter is designed to operate only in discontinuous conduction mode. However, the converter can work with higher power levels if some rules are respected.

The first and main limitation is the utilization factor D_L of the inductor defined in (1) as the fraction of time during which the inductor is in use:

$$D_L = \sum_{i=1}^{9} f_i \left(t_{PHA,i} + t_{PHB,i} \right) \leq 1 \quad , \; i = 1,2,...,9 \tag{5.1}$$

In the above equation, $t_{PHA,i}$ and $t_{PHB,i}$ are the durations of phases PHA and PHB for the i-th source, and f_i is the number of energy extraction cycles per second. In a multi-source scenario, D_L must be evaluated in order to safely satisfy (5.1). In the following derivation, (5.2) and (5.3) assess t_{PHA} for PZ and DC sources respectively. Equation (5.4) determines t_{PHB} with the assumption that the inductor current is approximated to a ramp and no losses occur while transferring an energy packet E_{CY} from the inductor to the capacitor. A more accurate analytical analysis for SECE with PZ is provided in [40].

$$t_{PHA,PZ} = \frac{\pi}{2} \sqrt{C_P L} \tag{5.2}$$

$$t_{PHA,DC} = \sqrt{L}\frac{\sqrt{2E_{CY}}}{\beta V_{DC0}} = \sqrt{L}\frac{\sqrt{2E_{CY}}}{V_{MPP}} \tag{5.3}$$

$$t_{PHB} = \sqrt{L}\frac{\sqrt{2E_{CY}}}{V_{ST}} \tag{5.4}$$

The PZ maximum input power is easily expressed by (5.5), where f_{PZ} is the vibration frequency and V_{PZ}=5 V is a circuit constraint. The resulting inductor duty cycle is shown in (5.6) in which t_{PHA} is given by (5.2).

$$P_{PZ\max} = 2f_{PZ}\overbrace{\frac{1}{2}C_P V_{PZ}^2}^{energy\ per\ cycle} \tag{5.5}$$

$$D_{L,PZ} = f_{PZ}\left(t_{PHA,PZ} + t_{PHB}\right) = f_{PZ}\left(\frac{\pi}{2} + \frac{V_{PZ}}{V_{ST}}\right)\sqrt{C_P L} \tag{5.6}$$

The same is applied to DC sources and results are shown in (5.7) and (5.8), in which f_{DC} is the switching frequency (i.e. the number of energy extraction per second, which depends on input power).

$$P_{DC\max} = f_{DC}\overbrace{2C_b V_{MPP}\Delta V_{hystDC}}^{energy\ per\ cycle} \tag{5.7}$$

$$D_{L,DC} = 2f_{DC}\frac{V_{ST}+V_{MPP}}{V_{ST}V_{MPP}}\sqrt{V_{MPP}\Delta V_{hystDC}}\sqrt{C_b L} \tag{5.8}$$

From the above equations, a graph showing the maximum input power for a single source is provided in Fig. 57 for the chosen 10 mH inductor (Murata 1410604) in several configurations: (a) PZ with C_P=52 nF with V_{PZ}=5 V; (b) LV source with $V_{MPP}= 0.75V_{DC0}$, V_{DC0}=1 V and C_b=150 µF; (c) LV source with $V_{MPP}= 0.50V_{DC0}$, V_{DC0}=1 V and C_b=120 µF; (d) HV source with $V_{MPP}= 0.75V_{DC0}$, V_{DC0}=5 V and C_b=180

μF; (e) HV source with V_{MPP}= 0.50V_{DC0}, V_{DC0}=5 V and C_b=180 μF. All the above configurations have D_L=0.9.

However, the internal switches (with the exclusion of M_{X1} and M_{X2} in Fig. 54 with R_{DSon}=0.8 Ω) have not been sized for currents of hundreds of mA. Then, because of their resistance, the maximum input power is limited to about 5 mW. This limitation descends from the S_{CONV} switch in Fig. 52. For DC input power above 5 mW, the current in the resonant circuit L-C_b would lead transistors in S_{CONV} to saturation, preventing correct energy transfer and, in the end, the functionality of the converter. The intrinsic efficiency of converter remains almost the same in the μW to mW range because the energy transfers are performed with resonant circuits with a constant quality factor. In addition, an increased input power in the mW range makes the IC consumption even more negligible and therefore an increase of efficiency is expected. Furthermore, the heat generated by losses on switches is not an issue for input power of some mW, even if the package has a very high thermal resistance.

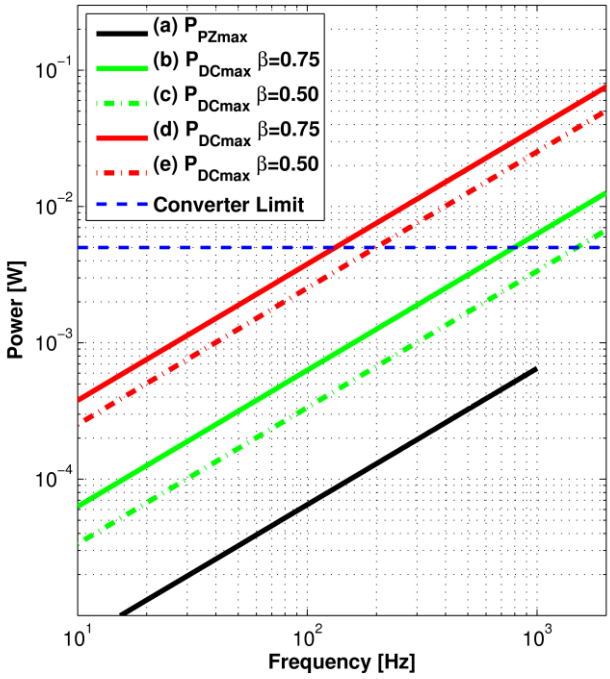

Fig. 57. Graph showing the theoretical maximum input power that can be handled by the converter operating with a single source.

5.7 Experimental Results

The proposed heterogeneous multi-source converter has been designed and fabricated in a 0.32 µm BCD technology from STMicroelectronics. A micrograph is shown in Fig. 58, and the die measures 2142 µm on each side with an overall area of about 4.6 mm^2.

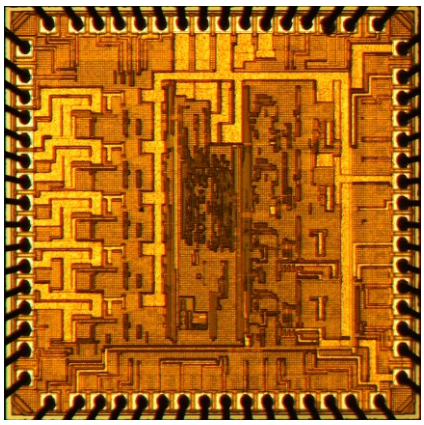

Fig. 58. Die micrograph of the IC. Each side, including the 64-pad padring, measures 2142 µm.

A functional test setup with the converter test board, two Q220-A4-303YB transducers from Piezo Systems with 7 g tip masses, an Ixys KXOB22-01X8 PV cell and a Micropelt MPG-D751 TEG is shown on the left of Fig. 59. On the right of Fig. 59, waveforms of acquired input voltages are shown with a forced external load consuming 40.5 µW (13.4 µA at V_{ST}=3 V) with the following input conditions applied: a fingertip heating the TEG at room temperature, typical indoor office illumination and the PZ driven with an acceleration with $a_{RMS} = 0.2g$ at 60 Hz.

5.7.1 Static consumption

An additional performed measurement is the quiescent current I_{DDq} of the converter. The IC was supplied with an external voltage provided by a Keithley 2601 SMU, which also measured the corresponding drawn current. Two cases have been

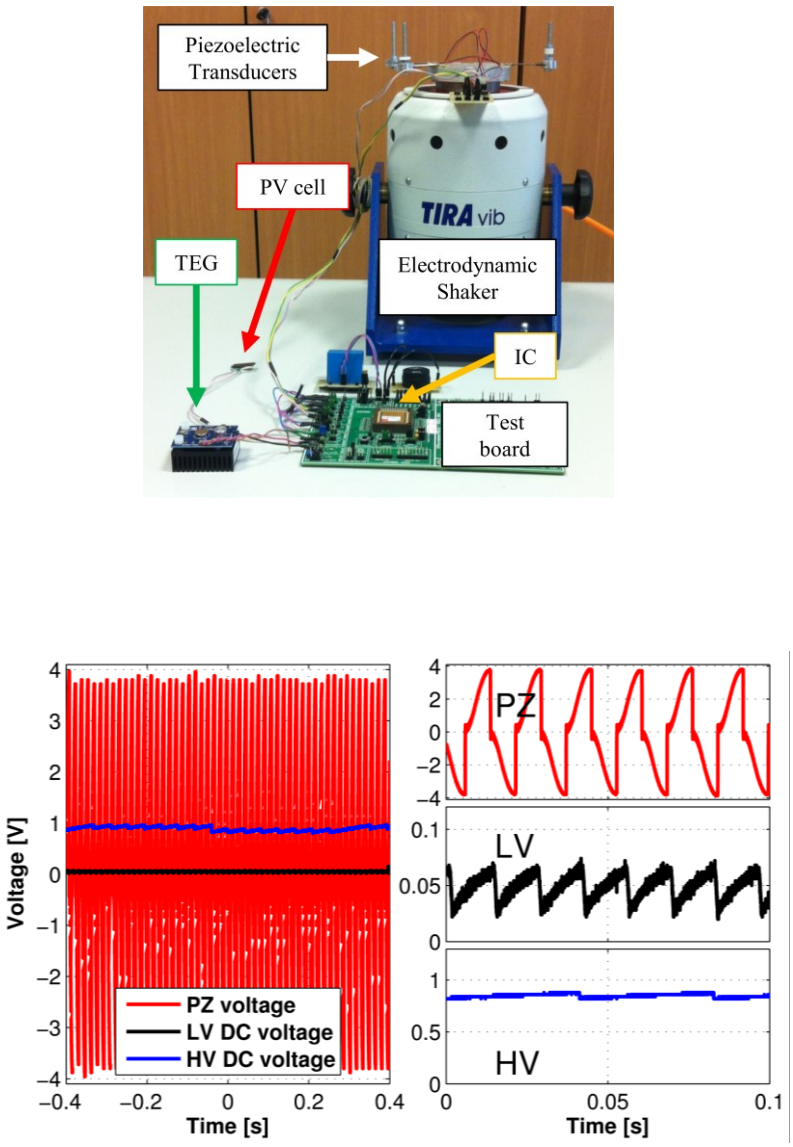

Fig. 59. (top) Setup for functional tests and (bottom) acquired waveforms showing: MPPT on the DC HV and LV channels and the sliced sinusoid resulting from SECE from a PZ.

evaluated in order to account for the different possible sign of PZ voltage V_{PZ}, which has been forced as $V_{PZ} = \pm 1$ V externally and $V_{DC} = 1$ V for HV DC inputs while $V_{DC} = 1$ V for LV DC inputs. The results, obtained on a fabricated device, are shown on top of Fig. 60 and point out an overall value of 431 nA, at V_{DD}=V_{ST}=3 V, corresponding to an average value of 47.9 nA per source. This remarkable result of

143.7 nW of static power per source is of vital importance in self-supplied energy-limited applications and is considerably lower with respect to other ICs for harvesting [41], [89]which have a static consumption for a single source of about 1.5 µW. The generated I_{ref} is inferred from obtained data and is compared with simulations on bottom of Fig. 60, in which a satisfactory matching is observed. However, I_{ref} exhibits a stronger dependence on V_{DD} than expected.

The converter is able to operate without a pre-charged energy reservoir as illustrated in Fig. 50 and therefore is suitable for battery-less applications. The minimum V_{ST} for active operation is V_{ST}≥1.38 V. Hence, because of the internal diodes at least one of the PZ and HV sources should provide a voltage higher than 1.65 V. Once the system switches to active operation such value is decreased down to about 0.7 V for PZ and 1 V for HV DC sources, while the lower limit for LV sources is about 60 mV, mainly due to the intrinsic ±28 mV hysteresis of the comparator in their interface circuit.

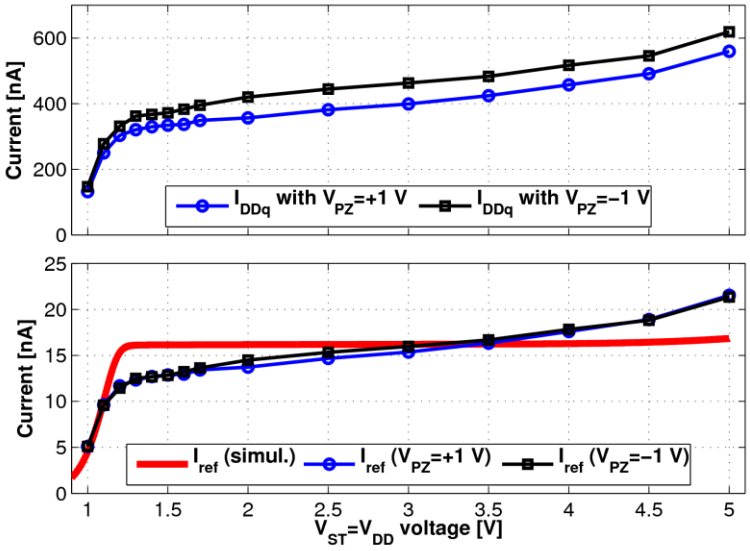

Fig. 60. (top) Quiescent current I_{DDq} drawn by the IC in an idle state (no conversions are performed) with PZ inputs polarized with +1 V or -1V and V_{DC} = 1 V for HV DC inputs while V_{DC} = 1 V for LV DC inputs (bottom) Comparison between inferred and

5.7.2 Conversion efficiency

A third experiment has been performed in order to assess converter efficiency η as the ratio between the power output on V_{ST} pin (i.e. power drawn from load, emulated with a Keithley 2601 SMU, and self-consumption from V_{DD} pin) and analytical input power. Fig. 61 shows the obtained efficiency for single source operation. The PZ was emulated with a $V_{PZ} = 4.42$ V peak voltage sinusoid on a $C_P = 47.7$ nF at $f_{PZ} = 64$ Hz, corresponding to a Q220-A4-303YB with a 7 g tip mass stimulated at 64 Hz with $a_{RMS} = 0.164g$. The HV-DC source has been emulated with $V_{DC0} = 2.7$ V and $R_S = 32.9$ kΩ to imitate a Sanyo AM1407 solar cell in standard laboratory light (about 300 lux), whereas the LV-DC source has been emulated with $V_{DC0} = 330$ mV and $R_S = 264$ Ω to simulate a Micropelt MPG-D751 TEG chip at room temperature with a thermal gradient of approximately 3 °C. Input power has been calculated with (5) and (7) as 59 µW for PZ, 55 µW for HV-DC, and 101 µW for LV-DC. The external components used in the setup are: $C_{ST} = 66$ µF, $L = 10$ mH, $C_{bHV1} = 2.7$ µF and $C_{bLV} = 22$ µF. The leakage of C_{ST} was found to be < 1 nA and therefore has not been considered.

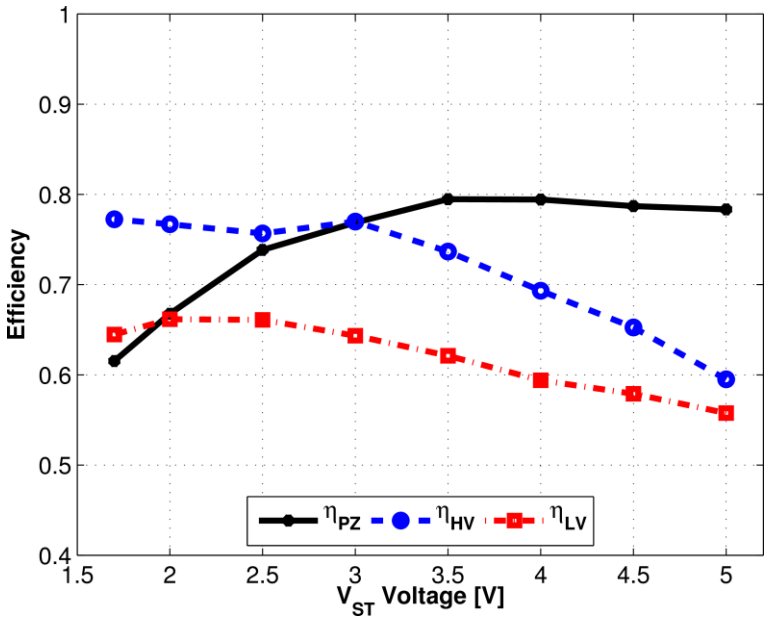

Fig. 61. Efficiency of the converter for each input channel type.

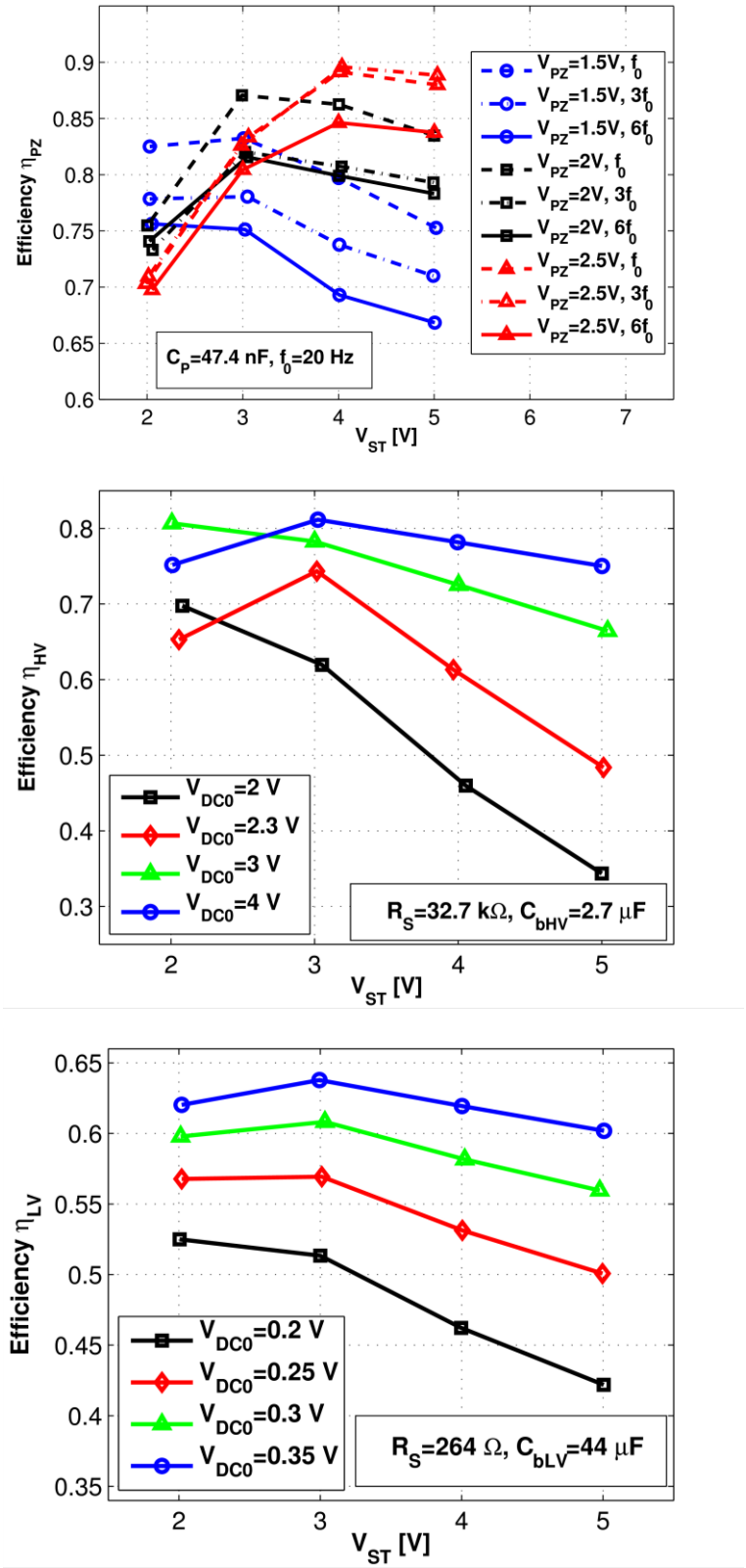

Fig. 62. Measured efficiency and current absorbed for different input configurations: (top) single PZ, (middle) single HV DC, (bottom) single LV DC.

The efficiency of the converter and its energy consumption have been investigated for other input configurations. Fig. 62 shows the obtained efficiency results for the converter operating with a single channel, PZ, DC HV and DC LV respectively and for the converter consumption during such measures. The used set-up is the same used in previous experiments with emulated sources and parameters and external components are listed in Fig. 62. The graphs show that the efficiency is in substantial agreement with Fig. 61 and variations are mainly due to variations of source characteristics (input power, frequency). The peak efficiency for PZ is 89.6% with input power ranging from 6.9 μW to 111 μW, 81% for HV DC channels with input power ranging from 30 μW to 122 μW, and 63.8% for LV DC channels with input power ranging from 21 μW to 116 μW.

5.7.3 Dynamic consumption

The energy absorbed by the IC in the aforementioned conditions has been measured by connecting a shunt resistor on the V_{DD} pin and by subtracting I_{DDq} from the resulting average current. The corresponding power was divided by the conversion frequency. The resulting energy consumption E_{cycle} per energy extraction is illustrated in Fig. 63 for each channel. The data show that the energy spent for an energy extraction cycle is only a small part of the available energy. In particular, in the tested scenario and in the worst condition ($V_{DD} = V_{ST} = 5$ V) the IC uses only the 2.36%, 2.75% and 2.48% of the energy per extraction cycle available respectively from PZ, HV-DC and LV-DC. Moreover, the energy usage follows a quadratic law, and then the amount of energy consumed at $V_{DD} = V_{ST} = 3$ V is even lower: 0.38%, 0.78% and 0.58% respectively. A comparison of energy consumption, losses and usable harvested energy is illustrated in Fig. 64.

The measurements on dynamic power absorbed by the converter are consistent for all the configurations. For example the energy used by the converter for a single energy extraction from a PZ agrees with data in Fig. 63 ($E_{cycle} \cong 12$ nJ at $V_{ST} = 5$ V, and $E_{cycle} \cong 5$ nJ at $V_{ST} = 5$ V). The same holds for DC channels (for example in LV channels $E_{cycle} \cong 4.5$ nJ at V_{ST}=5 V, and $E_{cycle} \cong 2$ nJ at $V_{ST} = 4$ V).

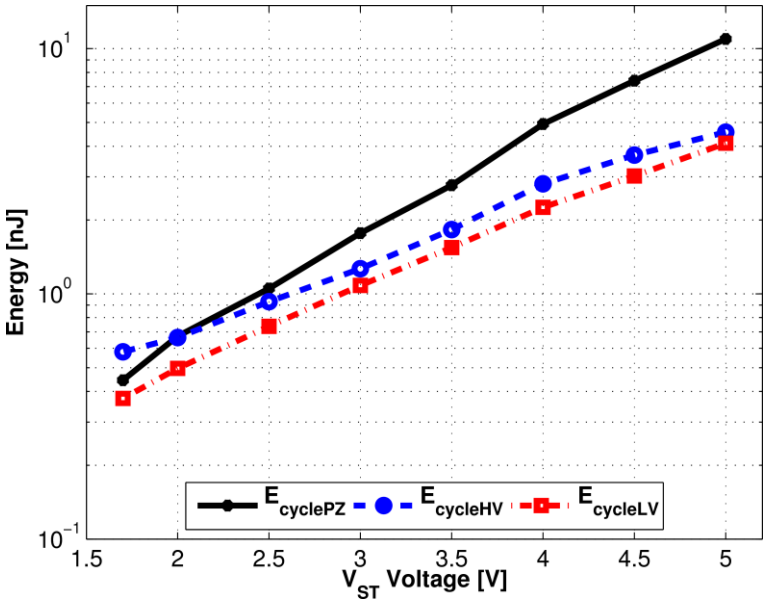

Fig. 63. Energy consumed during a single energy conversion.

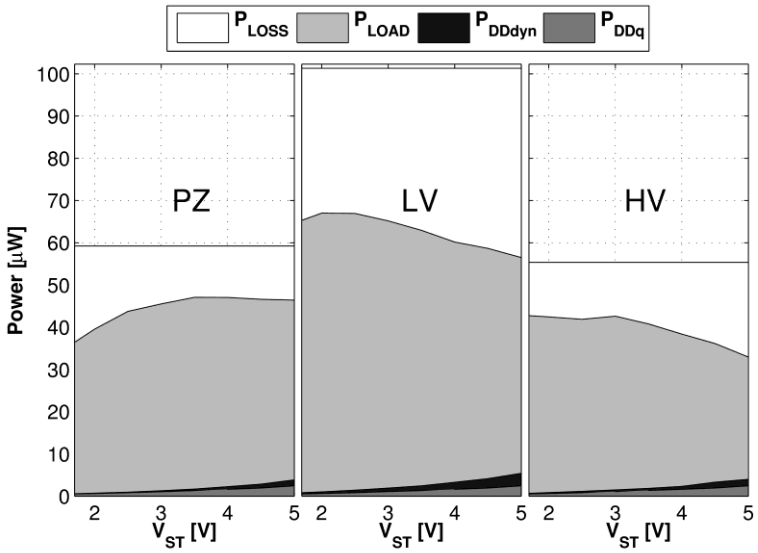

Fig. 64. Break-down of all contributions of the power conversion process for PZ, HV and LV DC sources. P_{DDq} is the static power of the converter due to I_{DDq}, P_{DDdyn} is the dynamic power associated to energy extraction cycles, P_{LOAD} is the net output power, and PLOSS is the power lost in the conversion process.

5.7.4 Input power boundaries

The nano-power design of the IC allows very weak source to supply and keep fully-functional the converter. The minimum required power, once the converter has switched to active-mode, was found to be about 3 μW with the above mentioned transducers. In a non-optimal case the converter can be supplied by a single PZ (Q220-A4-303YB PZ from Piezo Systems) driven at 60 Hz with an acceleration a_{rms}=0.04g with a 7g tip mass or, similarly, with a Micropelt MPG-D751 TEG chip with less than 1 K between its plates (generating V_{DC0}=60 mV). In an further measurement, a stable working condition at V_{ST} = 1.5 V, using the previously reported external components (C_{bLV}=22 μF, C_{ST}=33 μF, L=10 mH), was achieved with a drawn power of 0.77 μW by emulating a LV DC source with V_{DC0}=400 mV and R_S=52 kΩ which represents the minimum input power for a single source to keep the converter active.

The maximum power capabilities of the IC have also been investigated experimentally. By emulating a LV DC source with V_{DC0} = 850 mV and R_S = 55.1 Ω, which results in an input power of 3.275 mW, the converter was able to output 2.124 mW at V_{ST}=3 V with a 64.8% efficiency. The obtained efficiency agrees with the values in Fig. 61. The measurement was carried out with C_b=69 μF, the frequency of energy extraction was 1540 Hz and the duty-cycle D_L of the inductor was about 93%.

5.7.5 Summary

The obtained results from experimental measurements highlight two main causes for energy losses: resistivity (of switches, mainly) and back-current in the inductor due to inaccuracies in ZCS.

The first issue depends on the resistance of the inductor L (which is related to inductor size) and on the sizing of all the integrated switches in the IC, for which a die area constraint applies.

The second issue is due to delays in detecting the zero current condition in L (i.e. the end of phase PHB) and could be partially mitigated by increasing the tail current of comparator CMP_I in the buck-boost core.

The obtained results are summarized in Table VI, and they are compared to the other realizations of integrated power converters for energy harvesting applications with multi-source capabilities. Future work may consider the optimization of switch sizing in order to reduce their on-resistance at the cost of a larger die area.

TABLE VI. COMPARISON OF MULTI-SOURCE INTEGRATED CONVERTER FOR ENERGY HARVESTING.

Parameter	[66]	[25]	This work
Technology	0.35 µm HV CMOS 0.8 µm SOI	0.35 µm CMOS	0.32 µm BCD
Input channels	2	3	9
Type of sources	PZ, TEG	Piezoelectric, TEG, PV	Piezoelectric, TEG, PV, RF
Voltage Range	≥4 V	PZ: 1.5-5 V TEG: 0.02-0.16 V PV: 0.15-0.75 V	PZ: 0.7-5 V LV: 0.1-1 V HV: 1-5 V
Converter type	Rectifier + LDO	Switching	Switching
Peak Efficiency	66 %	83 %	89.6 %
Quiescent current	300 nA	1.5 µA (5µW at 3.3 V)	431 nA
MPPT type	n.a.	Hill-Climbing	FOCV (DC), SECE (PZ)
Maximum Output Voltage	> 4 V (2.4 V regulated)	3.3 V	5 V
Maximum Output Power	n.a.	2.5 mW	2.12 mW

Conclusions

The work leading to this thesis has been focused on the design on nano-power converters and power management circuits tailored for energy harvesting applications. The requirements and intrinsic limitations of the available energy sources led to the design and manufacturing of three ICs:

- a converter for vibrational energy harvesting implementing SECE and introducing RCI and TWS;
- a power management circuit for low voltage DC energy harvesting which includes a low voltage buck-boost converter with TWS, an inductor-less start-up circuit and a linear output regulator;
- a buck-boost converter for multiple and heterogeneous energy sources with a single shared inductor able to extract energy from up to 9 independent transducers.

The results obtained from experimental validations showed that the ICs advance the actual state-of-the-art in the research field of integrated converters for energy harvesting. The conversion efficiency is kept at an high value (over 70%) even with very low intrinsic consumptions, below the μW. Sub μW operation has been demonstrated for both vibrational energy harvesting and DC energy harvesting.

Due to extreme power limitations, and in order to achieve very low intrinsic consumptions, several aspects have been taken into account at the design stage. Any sub-circuit has been designed to strictly meet the requirements of its macro-function, avoiding general-purpose designs with oversized performances. Moreover, silicon integration easily allows the dynamic variation of the bias current of circuits. Such variation has also been taken to the extreme, with the complete turn-off of a sub-circuit when it is not in use. The drawback of this techniques is a more complex design and, in wider terms, the reduction of energy consumption in this ultra-low-power applications reflects into further efforts at the design stage.

Self-supplied and battery-less systems exhibit a further degree of complexity. A stable power supply is missing in such systems and each sub-circuit has to deal with

several variable voltages, and moreover the highest voltage is unknown and may continuously change (e.g. the PZ voltage has a wide swing at each oscillation period). Hence, providing the correct supply voltage to each block is essential for correct operation of both analog circuits and drivers of power switches. Furthermore, the choice of the correct supply voltage is critical as errors may originate the turn-on of parasitic devices, deteriorating efficiency and even stopping converter operation.

The static current (i.e. leakage) of CMOS digital circuits is not an issue for the small digital blocks used in the designed converter, in the order of some hundreds of gates. At those levels, the main source of energy consumption is the clock generation (and distribution). Furthermore, the clock frequency should be dynamically changed to comply with timing variations of the different phases (i.e. PHA, PHB and PHC) of the energy extraction process. The design of asynchronous controllers and FSMs prevents such issues and allows a significant reduction of intrinsic consumptions of logic circuits. One more time, the adoption of asynchronous logic circuits introduces further complexity at the design stage.

A trade-off among efficiency, power consumption and inductor size is mandatory. The working principle of the designed converters is based on the energy transfer between two LCR circuits. Inductors with a small footprint have typically a low inductance value (tens of μH) which are not compatible with ultra-low-power applications. With smaller inductors (i.e. $L < 10$ mH) the time required for energy transfer is reduced, and hence the bias current of analog circuitry managing the energy extraction phases (ZVS and ZCS circuits) must be boosted, increasing the power consumption of the converter. In case of input power over the mW, smaller inductors can be used, leading to an increase of efficiency and also of energy consumption. However, the overall power budget is positive. In ultra-low-power scenarios (i.e. input power of some μW), large inductors are required as the benefit on conversion efficiency given by a smaller inductor would not balance the increment of intrinsic consumptions, leading to a negative power budget.

The use of a more recent silicon technology (e.g. 0.18 μm) would improve the performances of the converters, especially in the case of energy harvesting from low voltage DC sources. The converter performances would benefit from lower switch on-resistance, lower parasitic, lower transistor MOSFET threshold voltage (i.e. lower

operative voltage, and hence power consumption). On the other hand, the maximum voltage allowed by technologies is reduced as the geometries shrink, and thus a more recent process is best suited for energy harvesting from low voltage energy sources (e.g. single PV cells or TEGs). Since the voltage of a PZ under stress can easily reach 5 V (up to tens of V), recent silicon technologies are not recommended as they are designed to work at 1.8 V or 3.3 V.

Future works may include further optimizations at the circuital level, with two main key aspects:

- reduction of the on-resistance of the switches in power path, at the cost of more silicon usage and an increase of dynamic power;
- improvement of the ZCS circuit, responsible for efficiency degradation for $V_{ST} > 3.5$ V.

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