Alma Mater Studiorum – Università di Bologna

DOTTORATO DI RICERCA IN

Ingegneria Elettrotecnica

Ciclo XXVII

Settore Concorsuale di afferenza: 09/E2

Settore Scientifico disciplinare: ING-IND/32

POWER CONVERTERS AND ELECTRIC DRIVES FOR SMART GRID APPLICATIONS

Presentata da: **Marco Bonavoglia**

Coordinatore Dottorato **Relatore**

Prof. Domenico Casadei **Prof. Angelo Tani**

Esame finale anno 2015

“Li miei compagni fec’io sì aguti,
con questa orazion picciola, al cammino,
che a pena poscia li avrei ritenuti;
e volta nostra poppa nel mattino,
de’remi facemmo ali al folle volo,
sempre acquistando dal lato mancino.”
“Inferno · Canto XXVI”

“Facesti come quei che va di notte,
che porta il lume dietro e sé non giova,
ma dopo sé fa le persone dotte.”
“Purgatorio · Canto XXII”

“Poca favilla gran fiamma seconda:
forse di retro a me con miglior voci
si pregherà perché Cirra risponda.”
“Paradiso · Canto I”

“Per aspera sic itur ad astra”

Table of contents

1 Smart Grid

1.1 Introduction

In recent years there has been an increasing growth of the number of power plants for electric generation from renewable sources connected at different points of the grind or directly with the distribution network. In fact, at the moment, the problem of sustainable development is central and this led to cleaner fuels usage, investments and incentives in the renewable energy sector.
Distributed generation nodes created by these new retail power makers are added to load nodes, often customers are also producers, and since it is expected a further substantial development of renewable energy in the near future, it is required an increasing "active" use of distribution networks with the fundamental capability of bidirectional power flow.
Besides, from the users point of view, there has been a continuing increase of power electronic loads, with the resulting problem of "Power Quality" and the situation is prone to a further modification due to the diffusion of electric mobility.
Since the electricity production from renewable energy is intermittent, the theme of '"Energy storage" and its interfacing with the network storage systems is of great importance. In this context, the electric mobility could play a crucial role.
For these reasons, it is fundamental an evolution of the grid and of the distribution networks - designed only for a "passive" usage where the power flow is unidirectional from centralized sources to distributed users - into "Smart Grids".
The architecture of the electricity networks was in fact originally designed for a situation where the energy production was assigned to large production nodes supplied by fossil and nuclear fuels often located at relevant distances from the user areas, the grid subsequently had a passive role.
Nowadays the situation is different. Due to the reasons already introduced the required behavior of the network is considerably changed. In particular it is necessary an active utilization of the electrical distribution network.
To this end, a coordinated control is required that, through a continuous monitoring of the state of the grid, can manage in an integrated way all its resources to optimize production and improve service to customers in the most convenient way from an economical point of view.

In this scenario it will be necessary to integrate two different structures:

- Microgrids: low voltage networks which are a small-scale version of centralized electricity system with distributed sources, accumulation devices and load control. They have capacities ranging from a few hundred of kW to several MW. Microgrids can operate connected with the distribution network, but are also able to be automatically configured in island operation. The microgrid is therefore a controlled entity that can generate, distribute, and regulate the flow of electricity to consumers in response to instructions that could be for example of economic nature.

- Virtual Power Plant (VPP): a cluster of distributed generation installation, conventional or renewable, connected to the network even in areas geographically larger, which, thanks to information technology, are collectively run by a central control entity and act as a single aggregate.

Actually the main characteristic should be that both VPP and retail power makers can be coordinated by the control system of the network, to produce the electricity required and provide auxiliary services like regulation and reserves of active and reactive power.
An example of Smart grid project is shown in Figure 1-1 where the distribution network, both in low and medium voltage, should be designed to operate in a flexible way and also with the possibility to work in stand-alone configuration.

Figure 1-1 – Smart Grid.

1.2 Desired characteristics

What is the desired behavior of the Smart Grid? Which tasks it should achieve?

First of all the grid should be fully integrated, i.e. fully interoperable with existing systems and with the capacity to incorporate a diverse set of energy sources. It should satisfy the different load requests not only in steady state but also in transient conditions to guarantee a good quality of the service supply.
In particular, one of the characteristic that could be requested to the control system is to give priority to renewable power generators. Another important aspect could be the economic management of the grid.
A smart grid should also guarantee a good power quality in the system. To achieve this it can operate with the available degrees of freedom (e.g. by using the reserve capability of power converters for interconnection of the renewable power generators). Moreover it can use active power filters and active UPS filters present in the grid.
The grid should be able to work in a stand-alone configuration or connected to the distribution grid that can be seen as the slack node. In this case the grid should participate to the regulations.
To integrate and enhance these structures, it's needed the development of systems that, through appropriate architectures of control, operate autonomously from the public distribution network or, if connected, able to work both in parallel to the public grid and in island mode.
The grid should guarantee the safety of the system and should be automatized to quickly operate and reconfigure when there are faults or problems.
Then it should control the energy storage system in the grid. If there are electric vehicles they can be seen as storage system as well.

1.3 Elements of Smart Grid

To evolve into "smart" as shown in Figure 1-1 a normal grid requires the following characteristics:

- Observability: it is necessary to continuously monitor the system state. All the variables needed to control the grid should be measured and visualized. By employing PMUs (Phasor Measurement Units) to know the voltages in different location of the grid it is possible to visualize the related phasors.

- Communication: information technology has a key role into smart grids. In fact it is necessary to transmit all the data collected in the singles nodes to the control system and vice versa. Communications infrastructure should enable the timely, secure and adaptable information flow needed to provide the service in the most reliable and economic way. Different solutions for the communication infrastructure have been proposed in literature. Among them optical fiber, wireless and powerline emerge. They have different characteristics in terms of bandwidth, cost, reliability that should be taken into account.

- Control: the system should be manipulated and automated. This can be done with tools such as the Distribution Management System (DMS) i.e. centralized management systems of portions of electrical distribution networks that can use the greater amount of information available, are capable of solving optimization problems, to control the power flows, the voltage and supply of ancillary services from distributed generation and load. The control system should also provide monitoring and real-time control of the distribution network by deciding the set point of the regulators, opening and closing breakers, monitoring alarms and collecting measurements from the field.

- Actuators and power conditioning: there are different instruments to operate on the network as required by the control system. Of course the switches could be controlled and used in emergency case to guarantee the security of the grid. For the normal operation of the network existing power converters could be used to control the active and reactive power flow. Inverters that interconnect renewable power sources, active power filters, or inverters that interface the storage systems or electric vehicles with the grid could be used for this purpose. Obviously, in this scenario the different converters should be equipped by a suitable control and communication system. The possibility to help in the regulation should be properly contractualised.

1.4 Research topic

The power involved in this sector is high, the research project aims to explore the problems and potential of new types of converters with particular emphasis on multi-level and matrix converter architectures. The advantages of such structures are discussed widely in the recently international scientific literature.

The multilevel technology allows, with same power and current, to split the voltage on different static switches while improving the quality of the voltage produced.
The matrix converter has no intermediate dc link capacitors, due to this reason it is easy to develop a reliable structure with space and weight saving. Even in this architecture the output voltage is multilevel. Moreover this architecture has different advantages that could be interesting for Smart Grids and for Power Quality requests. The input current is an high quality current, the power flow is totally bidirectional and the converter offers the possibility to control the input power factor (i.e. possibility to participate to active and reactive power regulations).

1.5 Thesis outline

This thesis is organized into six chapters, the outline of the thesis is described below.

Chapter one is the introduction of the thesis. This chapter describes the Smart Grid concept and what are its main features and key components. The future developments and the technologies that can be integrated into the Smart Grid are highlighted.

Chapter two presents an introduction to multilevel inverters. It provides an analysis of the modulation techniques for this type of inverters. In particular SVM and PWM approach are compared with particular emphasis on the degrees of freedom available.

Chapter three presents the first multilevel architecture, Diode Clamped topology. Simulation results of different configurations are shown. The DC capacitors voltage analysis and its correlation with the state of the inverter is performed.

Chapter four presents the second multilevel architecture, Cascaded topology. Its advantages and drawbacks are discussed and simulation results of different configurations are shown.

Chapter five proposes different control techniques for a new topology of multilevel inverter, the modular multilevel converter (MMC). The study of the single leg configuration, the three phase configuration and the back to back configuration is conducted. Simulation results and experimental results of the different configurations are shown.

Chapter six presents the Matrix converter topology. The analysis of fault detection strategies and diagnostic methods are analyzed in detail. Experimental results of the realized control system are shown.

Chapter seven concludes the thesis.

2 Multilevel inverters

2.1 Introduction

This chapter has the purpose to introduce to the general concept of multilevel architecture.
In general, inverters are static power converters implemented to generate a desired voltage or current, with the possibility to freely control amplitude and frequency.
VSI (Voltage Source Inverter) inverters, with a fixed DC voltage source will be analyzed. Traditional VSI inverters are commonly called ”two level”, due to the fact that each leg has two voltage levels available. In Figure 2-1 the two voltage levels for each phase in a traditional inverter are represented. The semiconductor switches could be substituted with an ideal switch. The voltage output can assume only two values: *0* or V_d.

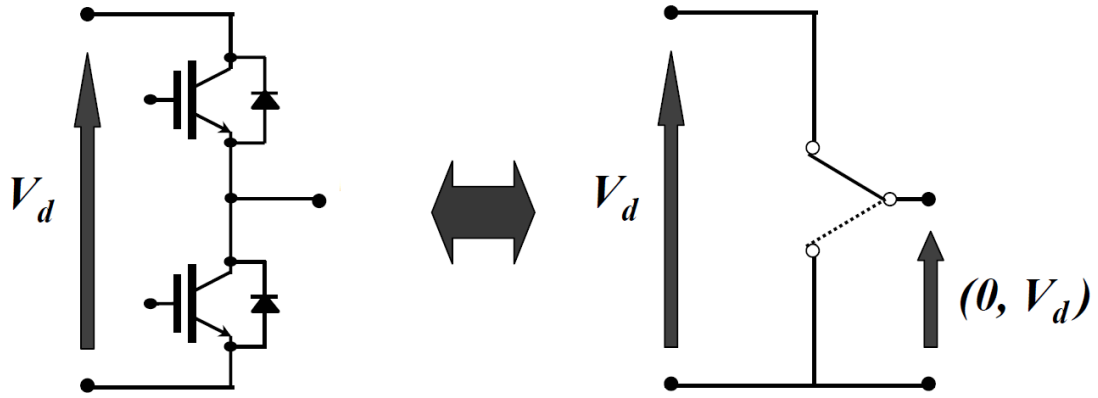


Figure 2-1 – Scheme of a two-level inverter leg.

It is possible to proceed with the generalization of the scheme with an higher number of levels, for example five as shown in Figure 2-2. Even in this scheme, the semiconductor switches have been substituted with an ideal switch that can provide n different voltage levels to the output.
It is easy to notice that the voltage output of this type of inverter can assume five values: *0*, $V_d/4$, $V_d/2$, $3V_d/2$, V_d.
In this short analysis some simplifications have been introduced. In particular, it is considered that all the DC voltage sources have the same value and are connected in series. In real application there are not such constraints, consequently the voltage levels can be different. This introduces a degree of freedom and also a further element that is necessary to monitor and control, as it will be shown in the following.

In general a three-phase inverter composed by n-level legs will be considered for the analysis. Obviously the number of phase-to-neutral voltage (i.e. pole voltage) output levels is n. The number *k* of the line-to-line voltage levels is given by equation (2-1).

$$k = 2n - 1 \tag{2-1}$$

Considering a star connected load, the number *p* of phase voltage levels is given by equation (2-2).

$$p = 2k - 1 \tag{2-2}$$

For example, considering a 5-level inverter leg, it is possible to obtain 9 line-to-line voltage level (3 negative levels, 3 positive levels and 0) and 17 phase voltage levels.

Higher is the number of levels better is the quality of the generated output voltage, in fact with the increase in the number of steps it is possible to better approximate the sinusoidal waveform. For this reason, the increase of the number of the levels brings to a benefit to the THD (Total Harmonic Distortion) of the applied output voltage, but the control system became more complex than the traditional 2-level architecture.

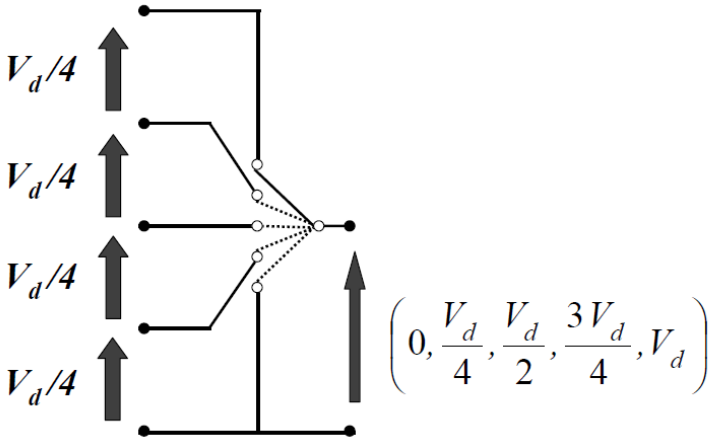


Figure 2-2 – Scheme of a five-level inverter leg.

2.2 Multilevel inverter features

The limit of traditional two-level three-phase inverters is connected to the maximum power which can be supplied to the load, that depends to maximum voltage and current of the power switches and capacitors.

Moreover, it is verified in general that the higher is the power of a switch and the lower is its switching frequency. A possible solution to avoid this limit is to connect more semiconductor devices in series or in parallel. The series connection of two or more electronic switches is not

viable due to the impossibility to synchronize their commutations. In fact, if one device switches off quicker than the others it will explode because it will be affected by the entire voltage drop designed for the whole series. On the other hand, parallel connection is a little less problematic due to the property of MOSFETs and more latest IGBTs to increase their internal resistance with the increment of the junction temperature.
When a device switches on quicker than the others, it will conduct a greater current than the one it was designed for. Consequently the power switch increases its junction temperature and its resistance, so it limits the current which is circulating on it. This behavior allows to overcome the troubles coming from a delay among gate signals or from differences among real turn on time of the components. Nevertheless, the parallel connection of power electronic switches involves a really precise design of the P.C.B. (Printed Circuit Board).

Multilevel inverters are a possible solution to increase the power with a relatively low stress on the components and with a relatively simple control system. Moreover, this type of architecture presents several other benefits. First of all, multilevel inverters generate better output waveforms with a lower dv/dt than standard two-level inverters. For this reason, a multilevel inverter can increase the power quality due to the great number of steps of the output voltage: this way, the filter on AC side can be reduced or removed, decreasing the costs and increasing the efficiency. Besides, multilevel inverters can operate with a lower switching frequency than 2-level inverters, so they can generate reduced electromagnetic emissions, making it easier to respect the standards. Finally, multilevel inverters can be directly connected to high voltage grids without the need of transformers (e.g. interconnection of offshore wind farms with the grid); this brings to a reduction of the costs and to an easier implementation and maintenance.

The main advantages of multilevel inverters in comparison with standard two level inverters can be summarized as follow:

- Output voltage with low THD.
- Low dv/dt that brings to a less solicitation of the system.
- Power switches are subjected to a reduced voltage, this means that the multilevel inverter can reach an higher DC voltage.
- Possibility to reach higher switching frequency.

2.3 Modulation strategies

In this section PWM (Pulse Width Modulation) technique and SVM (Space Vector Modulation) technique for three-level three-phase inverters will be analyzed and compared. The study can be extended to an inverter with a generic number of levels.

The configuration (state) of the inverter can be always described by three state functions s_A, s_B, s_C (one for each phase A, B and C) that can assume three values: *-1*, *0*, *+1* (one for each of the three levels). The three pole voltages v_A, v_B, v_C can be expressed as:

$$v_{A0} = \frac{V_d}{2} s_A \tag{2-3}$$

$$v_{B0} = \frac{V_d}{2} s_B \tag{2-4}$$

$$v_{C0} = \frac{V_d}{2} s_C \tag{2-5}$$

In general the space vector of the load phase voltages is equal to the space vector of the pole voltages and can be expressed as:

$$\bar{v}_C = V_d \frac{1}{3}\left(s_A + s_B\bar{\alpha} + s_C\bar{\alpha}^2\right) \tag{2-6}$$

There are 27 possible configurations, 24 of them are active voltage configurations whereas 3 of them are null voltage configurations.

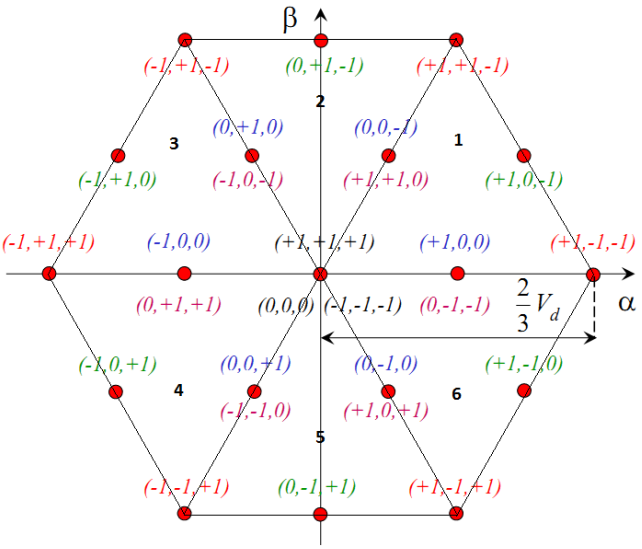


Figure 2-3 – Switching configurations in α-β plane of three-level three-phase inverter.

In Figure 2-3 all the switching configurations in α-β plane of a three-level three-phase inverter are shown.

2.3.1 SVM

In SVM modulation approach the reference space vector of the load phase voltages $\bar{v}_{C,ref}$ is an average combination of the nearest three space vectors during a switching period T_C.

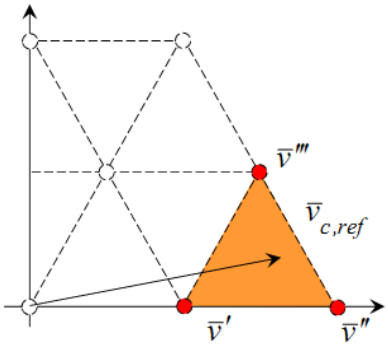


Figure 2-4 – SVM modulation strategy.

Referring to Figure 2-4 where a generic area (triangle) is considered and $\bar{v}'$, $\bar{v}''$, $\bar{v}'''$ are his vertex (nearest three space vectors), the equation that allows to calculate the reference voltage space vector is:

$$\bar{v}_{C,ref} = \frac{\bar{v}'T'+\bar{v}''T''+\bar{v}'''T'''}{T_C} = \bar{v}'\delta'+\bar{v}''\delta''+\bar{v}'''\delta''' \tag{2-7}$$

where T', T'', T''' are the application times of the three vectors, their sum is equal to T_C. δ', δ'', δ''' are the duty-cycles of the three vectors.

Of course it is necessary to recall that the duty cycles must satisfy the following constraint:

$$\delta'+\delta''+\delta'''=1 \tag{2-8}$$

Combining equation (2-7) and equation (2-8) it is possible to find the unique expressions for the three duty cycles.

To obtain the switching pattern two more conditions are required:

1- Specular symmetry of the pattern.
2- One commutation for each state change.

In general, the pattern is constituted by 7 intervals (i.e. 7 switching configurations). According to Figure 2-3 it is possible to notice that there is still a degree of freedom for vectors that can be

expressed with more than one combination of the three state-functions (i.e. vectors that can be applied with different switching configurations). In fact, there is the possibility to distribute in a different way the application times of the switching configurations of the vectors with redundancies.
For example as a particular case it is possible to obtain a symmetrical 7 intervals pattern or 5 intervals pattern (type A or type B).

2.3.2 PWM

In PWM modulation approach if the reference load phase voltage space vector is known it is consequently possible to know also the reference pole voltage space vector:

$$\bar{v}_{P,ref} = \bar{v}_{C,ref} \tag{2-9}$$

Using inverse-transformation relations it is possible to find the reference pole voltages for each phase:

$$v_{Ao,ref} = \frac{v_{po}}{2} + \bar{v}_{C,ref} \cdot 1 \tag{2-10}$$

$$v_{Bo,ref} = \frac{v_{po}}{2} + \bar{v}_{C,ref} \cdot \bar{\alpha} \tag{2-11}$$

$$v_{Co,ref} = \frac{v_{po}}{2} + \bar{v}_{C,ref} \cdot \bar{\alpha}^2 \tag{2-12}$$

Then the relations of the modulating signals for each phase can be found:

$$m_A = m_o + \frac{2}{V_d} v_{AN,ref} \tag{2-13}$$

$$m_B = m_o + \frac{2}{V_d} v_{BN,ref} \tag{2-14}$$

$$m_C = m_o + \frac{2}{V_d} v_{CN,ref} \tag{2-15}$$

Finally it is possible to calculate the switching pattern with the comparison of the modulating signals with two carrier signals: one between *-1* and *0* and the other one between *0* and *1* (level shift multicarrier approach).

m_o is the zero-sequence of the modulating signals and is equal to:

$$m_o = \frac{v_{po}}{V_d} \tag{2-16}$$

where v_{po} is the zero-sequence of the pole voltages.
m_o is a degree of freedom of the modulation and represents a rigid translation of the three modulating signals.

2.3.3 SVM and PWM comparison

It is possible to demonstrate that, under the previous assumptions, the SVM and PWM techniques are equivalent. The order and the distance between the three modulating signals in PWM correspond to a specific sector in SVM approach. The shift of the three modulating signals according to the value of m_o corresponds to different choices of the switching configuration for vectors that have multiplicity.

It is possible to divide the α-β plane into six sectors (triangles) according to Figure 2-3. Each sector corresponds to a different order of the modulating signals like in two level inverters as shown in Table 2-1.

$m_A > m_B > m_C$	Sector 1
$m_B > m_A > m_C$	Sector 2
$m_B > m_C > m_A$	Sector 3
$m_C > m_B > m_A$	Sector 4
$m_C > m_A > m_B$	Sector 5
$m_A > m_C > m_B$	Sector 6

Table 2-1 – Equivalence between modulating signals order and SVM sectors.

In this chapter it will be analyzed sector 1, the approach is equivalent for the other sectors, only the modulation indexes order changes.
Sector 1 can be divided into four sub-sectors I, II, III, IV according to Figure 2-5, that will be descripted into the following four sections.

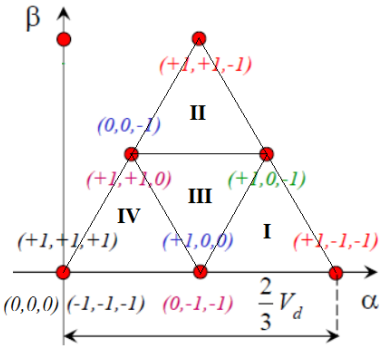


Figure 2-5 – Sector 1.

2.3.3.1 Sub-sector I

A situation where the voltage space vector is in sub-sector I is considered in Figure 2-6.

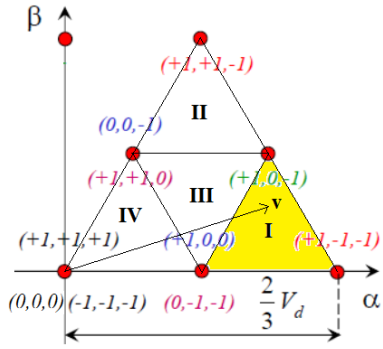


Figure 2-6 – Sub-sector I in α–β plane.

This situation corresponds in PWM approach to a case where the following relations between modulating signals are verified:

$$m_A > m_B + 1 \tag{2-17}$$

$$m_A > m_C + 1 \tag{2-18}$$

In Figure 2-7 it is shown an example of this situation. The switching pattern obtained with PWM is the same that is possible to calculate with SVM technique described in this chapter.

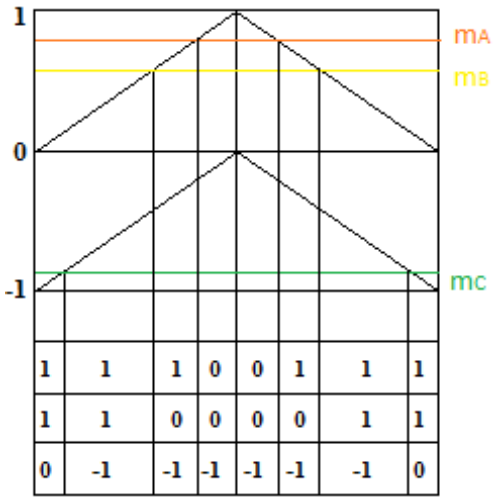


Figure 2-7 – Modulating signals disposition and switching pattern in sub-sector I.

As already seen, one of the vertex (vector) has two possible combinations that represent a degree of freedom. In SVM, different application times of these two combinations correspond to a shift of the three modulating signals in PWM.

2.3.3.2 Sub-sector II

A situation where the voltage space vector is in sub-sector II is considered in Figure 2-8.

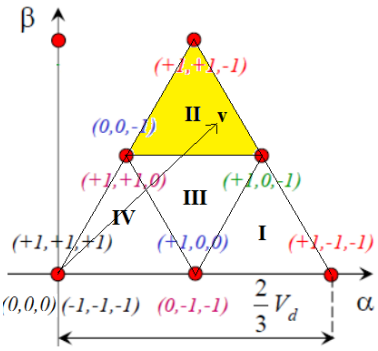


Figure 2-8 – Sub-sector II in α–β plane.

This situation is similar to the previous one and corresponds in PWM approach to a case where the following relations between modulating signals are verified:

$$m_A > m_C + 1 \tag{2-19}$$

$$m_B > m_C + 1 \tag{2-20}$$

In Figure 2-9 it is shown an example of this situation. The switching pattern obtained with PWM is the same that is possible to calculate with SVM technique.

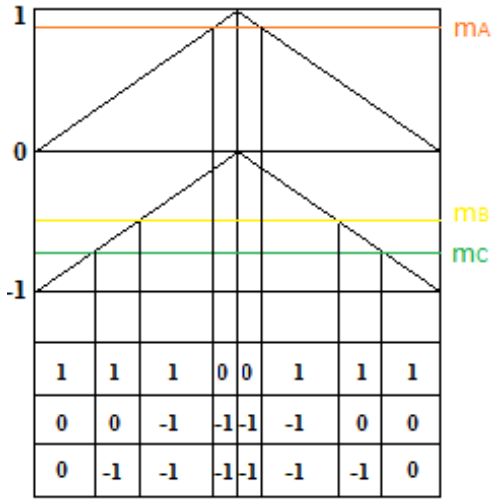


Figure 2-9 – Modulating signals disposition and switching pattern in sub-sector II.

2.3.3.3 Sub-sector III

A situation where the voltage space vector is in sub-sector III is considered in Figure 2-10.

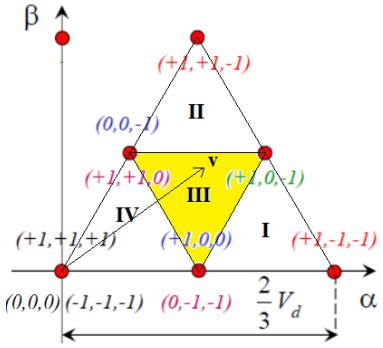


Figure 2-10 – Sub-sector III in α–β plane.

This situation corresponds in PWM approach to a case where the following relations between modulating signals are verified:

$$m_A > m_C + 1 \tag{2-21}$$

$$m_A < m_B + 1 \tag{2-22}$$

$$m_B < m_C + 1 \tag{2-23}$$

This case is slightly different from the previous two. In fact, there are two vertexes that have a double multiplicity. Consequently, there are two possible combinations in SVM approach that respect the required constraints. It's probably easier to analyze these combinations with PWM approach. It is possible to obtain one combination from the other with a different choice of m_o (i.e. rigid translation of the modulating signals).

In particular, if the choice of m_o brings to condition (2-24) the related PWM scheme and switching pattern is shown in Figure 2-11.

$$m_B > 0 \tag{2-24}$$

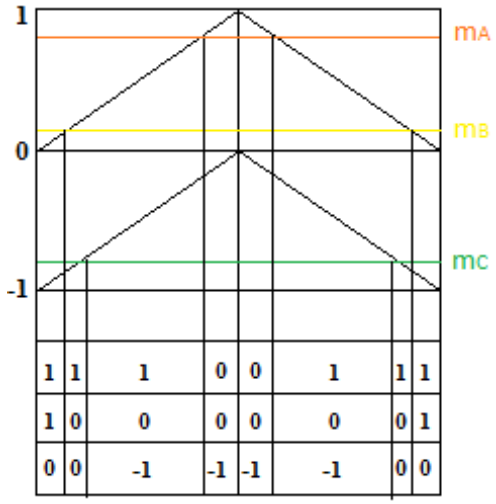


Figure 2-11 – Modulating signals disposition and switching pattern in sub-sector III – First case.

On the other hand, if the choice of m_o brings to condition (2-25) the related PWM scheme and switching pattern is shown in Figure 2-12.

$$m_B < 0 \tag{2-25}$$

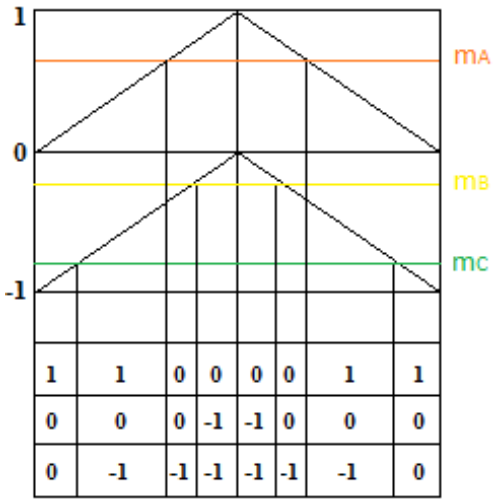


Figure 2-12 – Modulating signals disposition and switching pattern in sub-sector III –Second case.

It's worth to notice that, provided that one of the two conditions is verified (i.e. one of the two switching patterns is chosen), there is still a degree of freedom in the repartition of the application times of the configuration with multiplicities as usual.

2.3.3.4 Sub-sector IV

Finally, a situation where the voltage space vector is in sub-sector IV is considered in Figure 2-13.

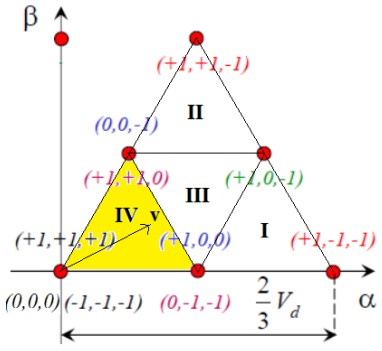


Figure 2-13 – Sub-sector IV in α–β plane.

This situation corresponds in PWM approach to a case where the following relation between modulating signals is verified:

$$m_A < m_C + 1 \qquad (2\text{-}26)$$

This is the most complex case. In fact, there are two vertexes that have a double multiplicity and one with triple multiplicity (the zero voltage vector). There are four possible combinations in SVM approach that respect the required constraints. It's probably easier to analyze this combinations with PWM approach. It is possible to obtain one combination from another one with a different choice of m_o (rigid translation of the modulating signals).

In particular, if the choice of m_o brings to conditions (2-27), (2-28) and (2-29) the related PWM scheme and switching pattern is shown in Figure 2-14.

$$m_A > 0 \tag{2-27}$$

$$m_B > 0 \tag{2-28}$$

$$m_C > 0 \tag{2-29}$$

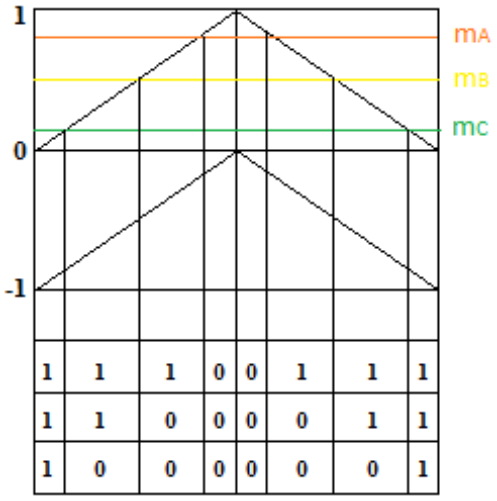


Figure 2-14 – Modulating signals disposition and switching pattern in sub-sector IV – First case.

If the choice of m_o brings to conditions (2-30), (2-31) and (2-32) the related PWM scheme and switching pattern is shown in Figure 2-15.

$$m_A > 0 \tag{2-30}$$

$$m_B > 0 \tag{2-31}$$

$$m_C < 0 \tag{2-32}$$

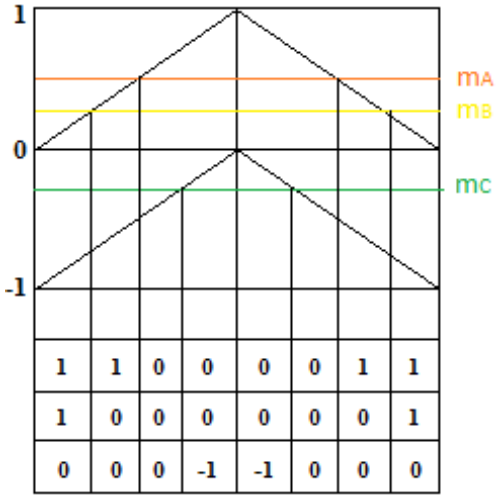


Figure 2-15 – Modulating signals disposition and switching pattern in sub-sector IV – Second case.

If the choice of m_o brings to conditions (2-33), (2-34) and (2-35) the related PWM scheme and switching pattern is shown in Figure 2-16.

$$m_A > 0 \tag{2-33}$$

$$m_B < 0 \tag{2-34}$$

$$m_C < 0 \tag{2-35}$$

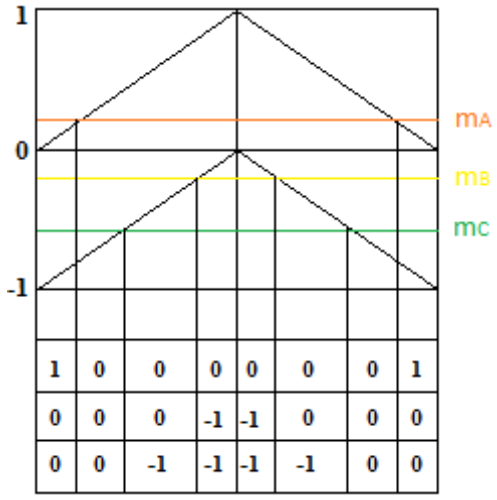


Figure 2-16 – Modulating signals disposition and switching pattern in sub-sector IV – Third case.

Finally if the choice of m_o brings to conditions (2-36), (2-37) and (2-38) the related PWM scheme and switching pattern is shown in Figure 2-17.

$$m_A < 0 \tag{2-36}$$

$$m_B < 0 \tag{2-37}$$

$$m_C < 0 \tag{2-38}$$

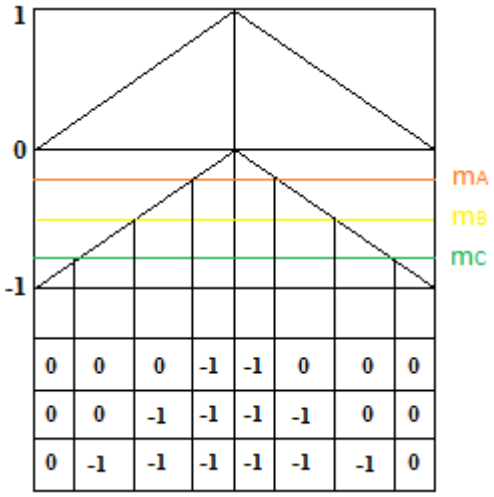


Figure 2-17 – Modulating signals disposition and switching pattern in sub-sector IV – Fourth case.

Even for the last sector it is interesting to notice that, provided that one of the four conditions is verified (i.e. one of the four switching patterns is chosen), there is still a degree of freedom in the repartition of the application times of the configuration with multiplicities as usual.

3 Diode Clamped (NPC – Neutral Point Clamped) Multilevel Inverter

3.1 Introduction

The first multilevel topology, analyzed in this chapter, is the Diode Clamped. A single leg of three-level Diode Clamped inverter architecture is shown in Figure 3-1. A five-level architecture of the same topology is shown in Figure 3-2.

It is possible to understand that by increasing the number of levels the architecture became more complex due to the typical non-modular structure of this type of inverter. In industrial applications usually three or more phases are needed. For example in Figure 3-3 is shown a three-phase three-level configuration.

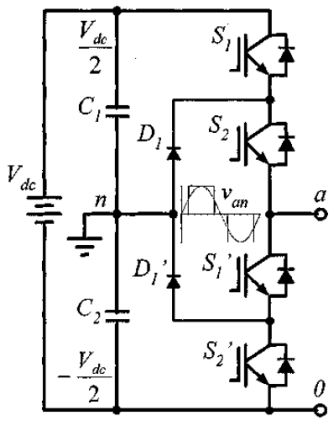


Figure 3-1 – Three-level Diode Clamped inverter leg.

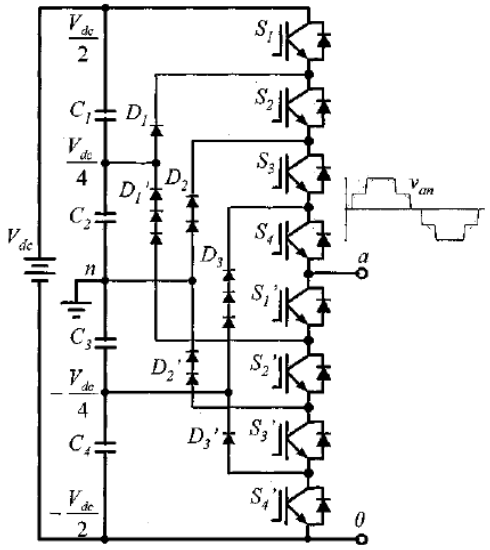


Figure 3-2 – Five-level Diode Clamped inverter leg.

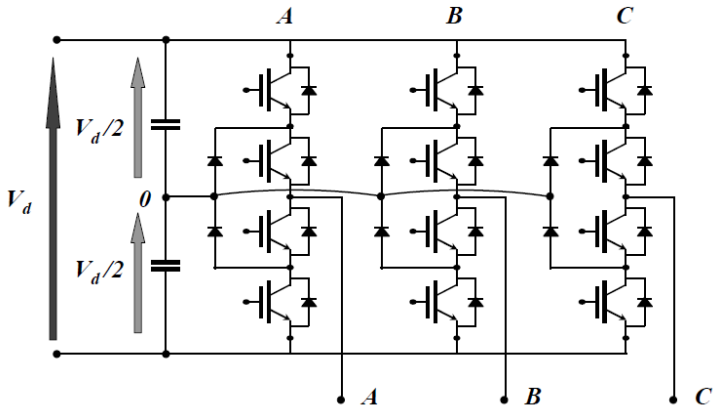


Figure 3-3 – Three-level three phase Diode Clamped inverter.

This structure is not flexible because it's not possible to reconfigure the inverter if more levels are needed for a certain application but a completely new design is necessary. Furthermore, it's not possible to increase the voltage and consequently the power over a certain level because the inverter becomes too difficult to realize.

Another critical aspect of this inverter is the presence of the capacitors that are subject to voltage oscillations, depending on the current that flows through the components.

So during normal operation the voltages across the capacitors are not constant and it's crucial to control the amplitude of the oscillation, to avoid critical over-voltages on the electronic devices.

Where this structure is compatible with the application, there is the advantage to have a single DC source directly applied to the series of the capacitors.

3.2 DC capacitors voltage analysis

In this type of inverter the study of the DC voltage capacitors behavior is essential, in fact it is necessary to keep the system operating in the correct way avoiding failures. The capacitors must be kept at the right voltage average level, and the amplitude of the oscillations must be controlled.

In Figure 3-4 it is shown a single leg of Diode Clamped inverter.

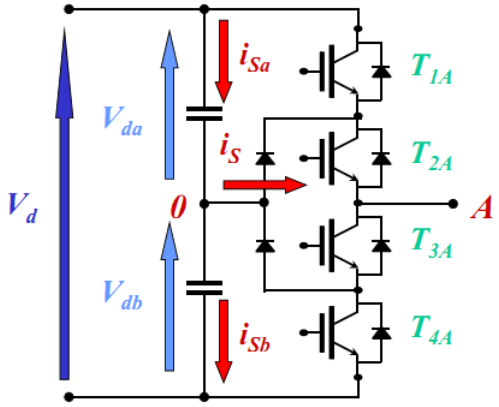


Figure 3-4 –Single leg Diode Clamped inverter.

The sum of the voltage drops across the upper and lower capacitors are equal to the DC voltage:

$$V_d = v_{da} + v_{db} \tag{3-1}$$

The DC voltage is impressed and constant so:

$$\frac{dV_d}{dt} = 0 \tag{3-2}$$

The equations of the upper and lower capacitors are:

$$\frac{dv_{da}}{dt} = \frac{i_{Sa}}{C} \tag{3-3}$$

$$\frac{dv_{db}}{dt} = \frac{i_{Sb}}{C} \tag{3-4}$$

Substituting equation (3-1) into equation (3-2) and considering equations (3-3) and (3-4) it is possible to obtain:

$$i_{Sa} = -i_{Sb} \tag{3-5}$$

The Kirchhoff's current law in node 0 is:

$$i_S = i_{Sa} - i_{Sb} \tag{3-6}$$

Combining equations (3-5) and (3-6) it is possible to find:

$$i_{Sa} = \frac{i_S}{2} \tag{3-7}$$

$$i_{Sb} = -\frac{i_S}{2} \tag{3-8}$$

Finally if equations (3-7) and (3-8) are substituted in equations (3-3) and (3-4) it is possible to obtain:

$$\frac{dv_{da}}{dt} = \frac{i_S}{2C} \tag{3-9}$$

$$\frac{dv_{db}}{dt} = -\frac{i_S}{2C} \tag{3-10}$$

Current i_S tends to change the potential of the 0 point and tends to unbalance the system, due to the variation of the voltages across the capacitors.

In three phase configuration the 0 point can still be subjected to a current i_S depending from the state of the three phases.
According to Figure 3-5, where sector 1 in shown, it is possible to notice that only the intermediate vectors V_{10}, V_{20}, V_{12}, lead to a system unbalance, in fact only when these vectors are applied the current i_S is not equal to zero.

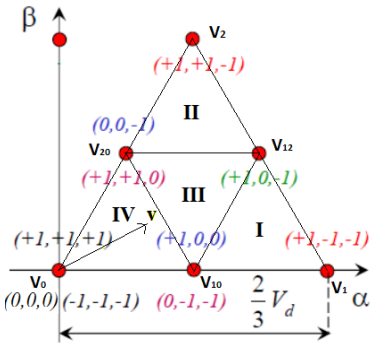


Figure 3-5 –Sector 1 in α–β plane.

In Table 3-1 the values of i_S, when these vectors are applied, are shown.

It is possible to understand that when vectors V_{10} or V_{20} are applied there's the possibility to balance the system alternating the two configurations that have contrary effects. The worst case is when vector V_{12} is applied. In fact there's only one configuration available and the current i_S is not controllable and depends only from the load requests.

In general the output voltage space vector is a rotating space vector (steady state operation). In this situation, the voltages across the capacitors will be subjected to oscillations, due to the symmetry of the required configurations, but the average value of the voltages will be constant. The amplitude of the oscillations increases with the reduction of the value of the capacitors and with the reduction of the frequency of the load space vector.

If the frequency is zero (i.e. the load space vector is constant), the average value can possibly be not constant if i_S is not zero.

Still referring to Figure 3-5 it is possible to study what happens in each sub-sector.

Configuration	$\boldsymbol{i_S}$
V_{12} *(+1,0,-1)*	i_B
V_{10} *(+1,0,0)*	i_A
V_{10} *(0,-1,-1)*	$-i_A$
V_{20} *(+1,+1,0)*	i_C
V_{20} *(0,0,-1)*	$-i_C$

Table 3-1 – Value of the current i_S with different configurations.

3.2.1 Sub-sector I

If the voltage space vector is in this triangle then in half of the switching period T_C there are four configurations applied for a certain period of time as already studied. In particular each of the four configurations has an effect on the i_S current for its application time:

$$i_S = i_A\delta_{10} + i_B\delta_{12} + 0\delta_1 - i_A\delta_{10}' \tag{3-11}$$

Obviously the choice of the configuration of space vector v_{10} is a degree of freedom and must be chosen in this case to keep the average value of i_S over $T_C/2$ equal to zero. Not in all situations it is possible to respect this constraint but only if the following condition is verified:

$$|i_A|\delta_{10} \geq |i_B|\delta_{12} \tag{3-12}$$

If it's not possible to keep balanced the capacitors because equation (3-12) is not satisfied for a certain position of the voltage space vector and the assigned load currents, then it's not possible to modulate using only the nearest three vectors (triangle vertexes).

Even in this case, where the voltage space vector is constant or the frequency is too low and there are unacceptable oscillations, it's always possible to keep balanced the capacitors using external

vectors but of course this means that not all the available levels are used. Moreover it should be considered that, using external vectors, the number of commutations increases.

3.2.2 Sub-sector II

This area is similar to the previous one. The expression that allows to calculate the current i_S over half a period starting from the four contributes is:

$$i_S = i_C\delta_{20} + 0\delta_2 + i_B\delta_{12} - i_C\delta_{20}' \tag{3-13}$$

In this case to keep the average value of i_S over half a period equal to zero the following condition must be satisfied:

$$|i_C|\delta_{20} \geq |i_B|\delta_{12} \tag{3-14}$$

Also in this case if it's not possible to keep balanced the capacitors, because equation (3-14) is not satisfied due to the position of the voltage space vector and the assigned load currents, then it's not possible to modulate using only the three nearest vectors (triangle vertexes). The same considerations of the previous case are valid.

3.2.3 Sub-sector III

In this triangle there are two possible switching patterns that imply two different expressions of the current i_S over half a period starting from the four contributes:

$$i_S = i_C\delta_{20} + i_A\delta_{10} + i_B\delta_{12} - i_C\delta_{20}' \tag{3-15}$$

$$i_S = i_A\delta_{10} + i_B\delta_{12} - i_C\delta_{20} - i_A\delta_{10}' \tag{3-16}$$

In the first equation the choice of the configuration of vector v_{20} and in the second equation the choice of the configuration of vector v_{10} are degrees of freedom and must be chosen to keep i_S equal to zero over $T_C/2$. To do this it is necessary to satisfy respectively these two constraints:

$$|i_C|\delta_{20} \geq |i_A\delta_{10} + i_B\delta_{12}| \tag{3-17}$$

$$|i_A|\delta_{10} \geq |i_C\delta_{20} + i_B\delta_{12}| \tag{3-18}$$

It is necessary to recall that is always possible to shift from one switching pattern to the other, to choose the less restrictive constraint.

If it's still not possible to keep balanced the capacitors, the same considerations made for the other sectors are valid.

3.2.4 Sub-sector IV

In this last area vector V_{12} is not involved. Remembering that the vectors V_{10} and V_{20} have two possible configurations with opposite effects and that the choice of the configurations is totally free, it is always possible to keep the average value of i_S over $T_C/2$ equal to zero and consequently the capacitors balanced.

3.3 Simulation model of three-phase three-level Diode Clamped inverter

In this section a three-phase three-level inverter will be analyzed. To simulate the inverter and the control system the software Matlab-Simulink will be used.
In Figure 3-6 the general model realized in Simulink is shown. It is constituted by the inverter, the R-L load and the control system.
The Diode Clamped inverter is generated by using the Sim Power System library and it's shown in Figure 3-7 while in Figure 3-8 it is possible to see the control system.

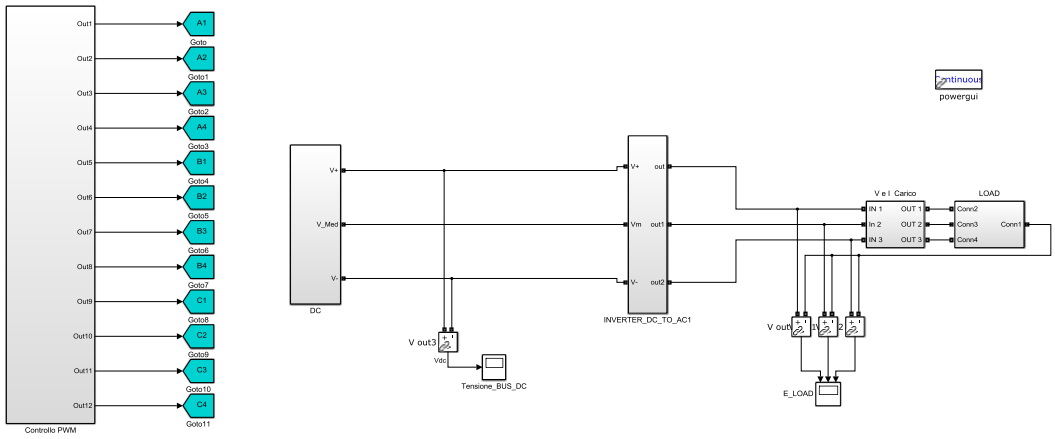


Figure 3-6 – Simulink general model of three-phase three-level Diode Clamped inverter.

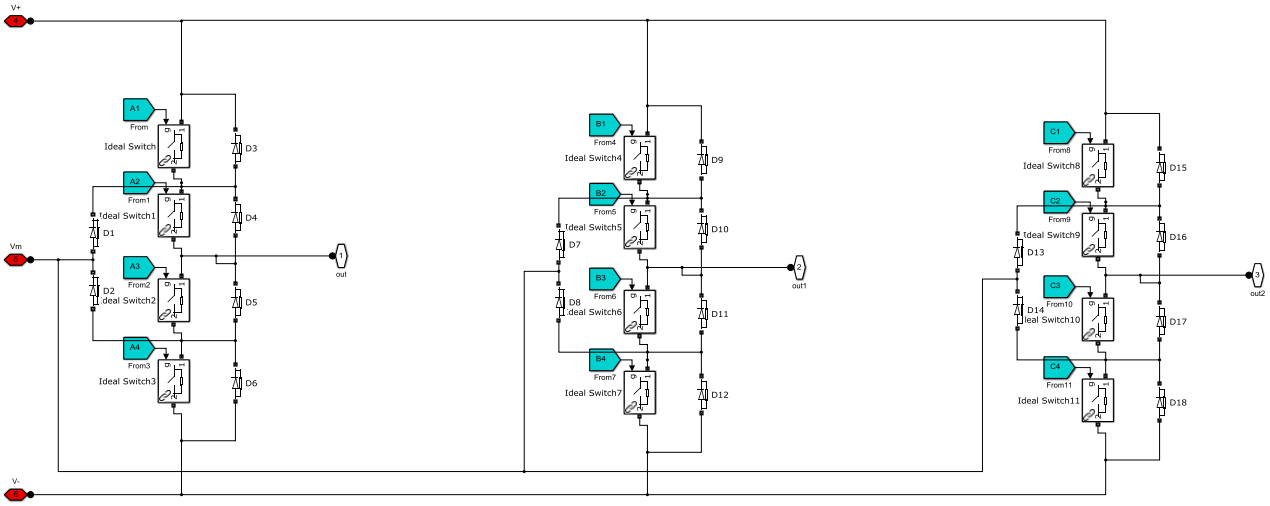


Figure 3-7 – Three-phase three-level Diode Clamped inverter.

Two carrier signals, one between *-1* and *0* and the other one between *0* and *1*, are compared with the modulating signals to generate the switching pattern. There are four gate signals for each one of the three phases.

The simulation parameters are listed in Table 3-2.

Frequency	50 [Hz]
DC voltage	100 [V]
Load resistance	2.22 [Ω]
Load inductance	5.3e-3 [H]
DC capacitors	170e-5 [F]

Table 3-2 – Simulation parameters.

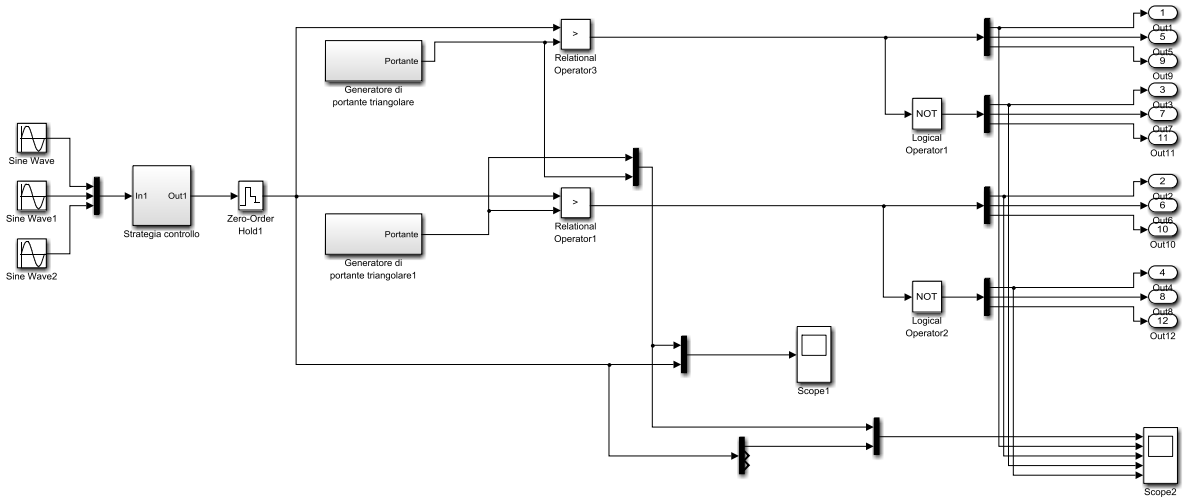


Figure 3-8 –Control system of three-phase three-level Diode Clamped inverter.

3.4 Simulation results of three-phase three-level Diode Clamped inverter

In this section the simulation results of the described configuration will be shown and analyzed.
First of all in Figure 3-9 the line-to-line voltages are displayed. As already seen, if there are three levels in the pole voltages, the line-to-line voltages are composed by five levels. The equation that allows this calculation is recalled:

$$k = 2n - 1 \tag{3-19}$$

where n is the number of levels in the pole voltages and k is the number of levels in line-to-line voltages.
In Figure 3-10 the phase voltages are shown. As already discussed if there are five levels in the line-to-line voltages the phase voltages are composed by nine levels. The equation that allows this calculation is recalled too:

$$p = 2k - 1 \tag{3-20}$$

where k is the number of levels in the line-to-line voltages and p is the number of levels in phase voltages.
The output currents of the three phases are shown in Figure 3-11.

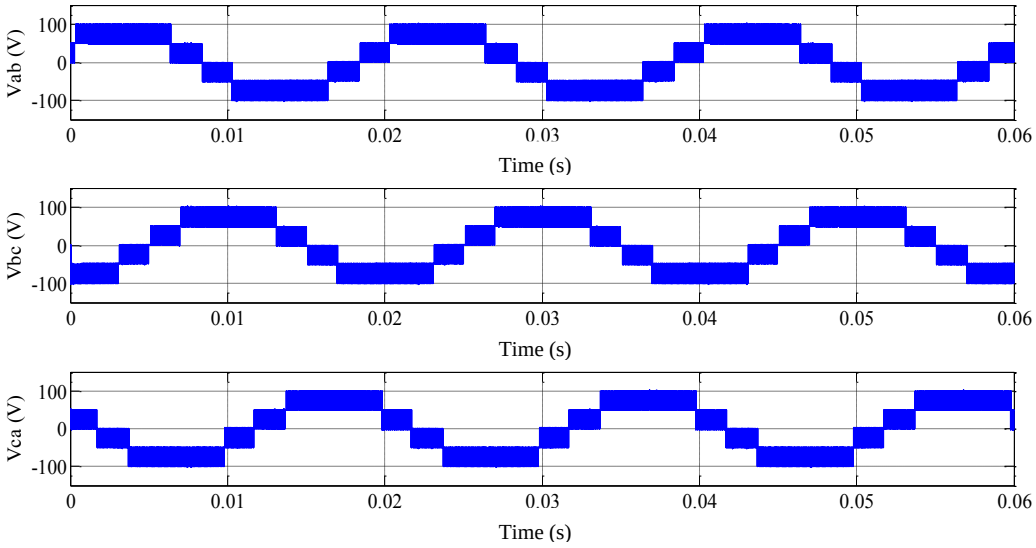


Figure 3-9 – Line-to-line voltages.

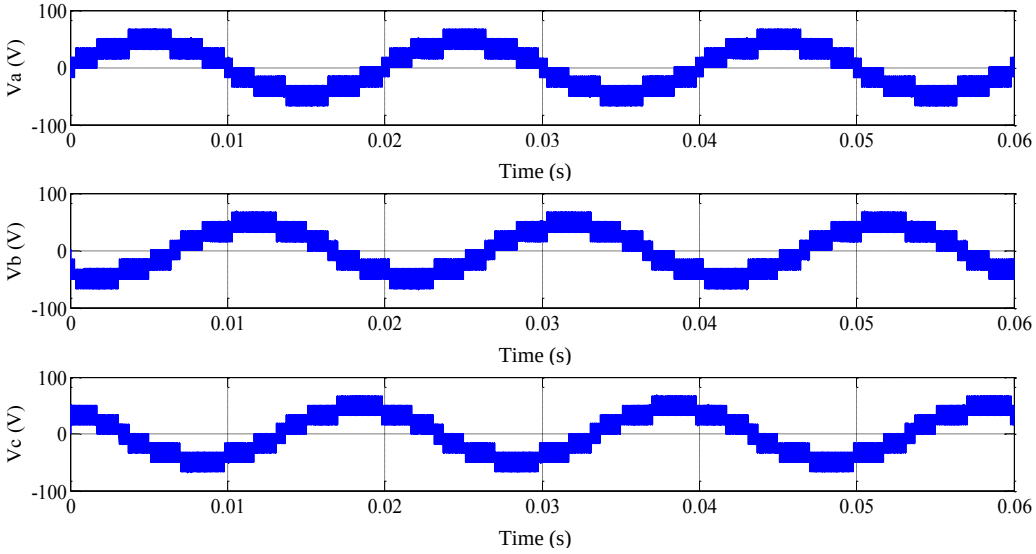


Figure 3-10 – Phase voltages.

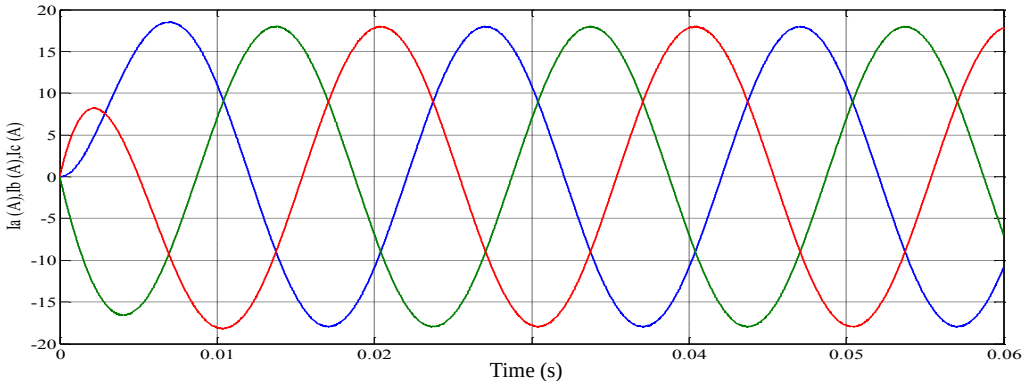


Figure 3-11 – Phase currents.

In Figure 3-12 the voltage oscillations on the upper and lower DC capacitors are shown.

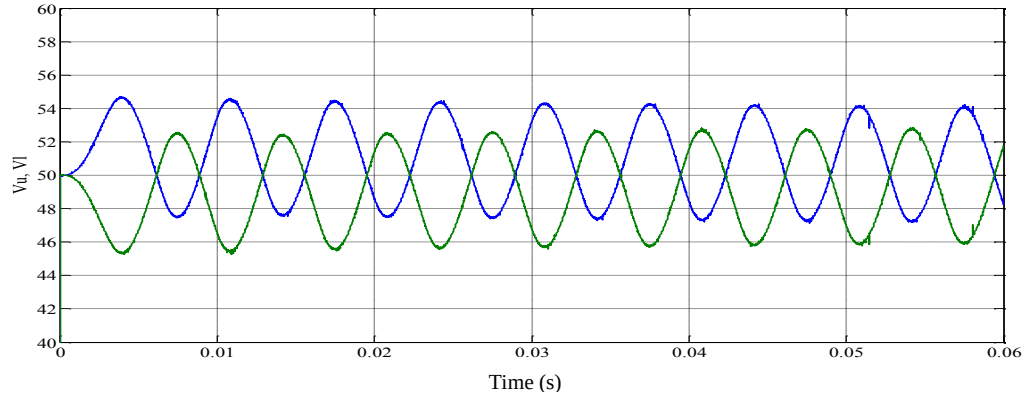


Figure 3-12 – DC capacitor voltage oscillations.

In Figure 3-13 the three modulating signals are displayed with the two carrier signals. The modulation strategy used is PWM symmetrical as it is possible to understand observing their shape.

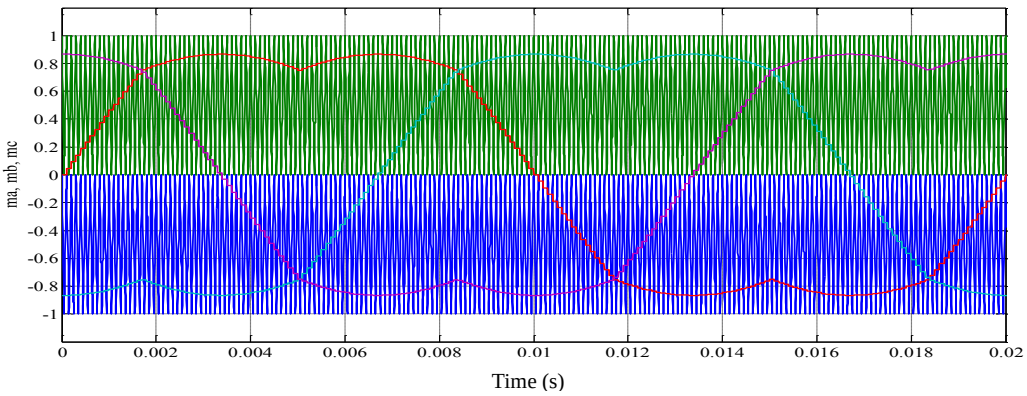


Figure 3-13 – Modulating signals and carrier signals.

In Figure 3-14 the modulating signals are shown in detail.

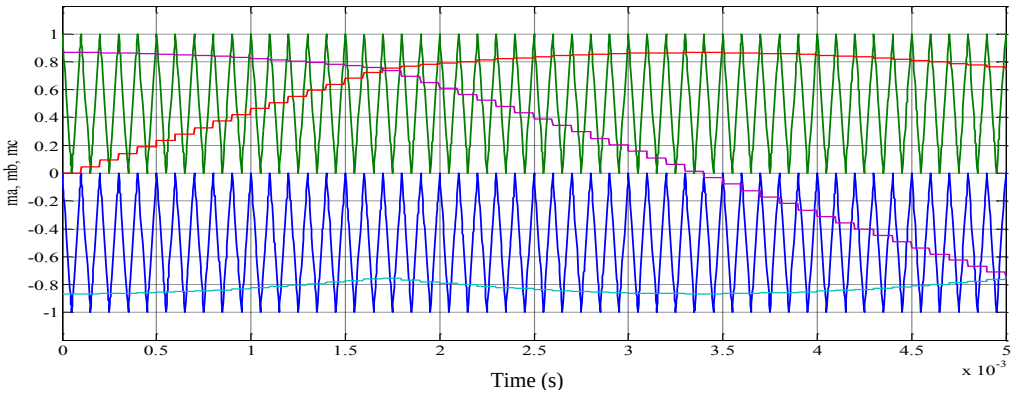


Figure 3-14 – Modulating signals and carrier signals detail.

Finally in Figure 3-15 it is possible to see the gate signals (i.e. state functions) obtained by the comparison between the modulating signal of one phase and the carrier signals. The gate signals are four, one for each of the four power switches that constitute the module.

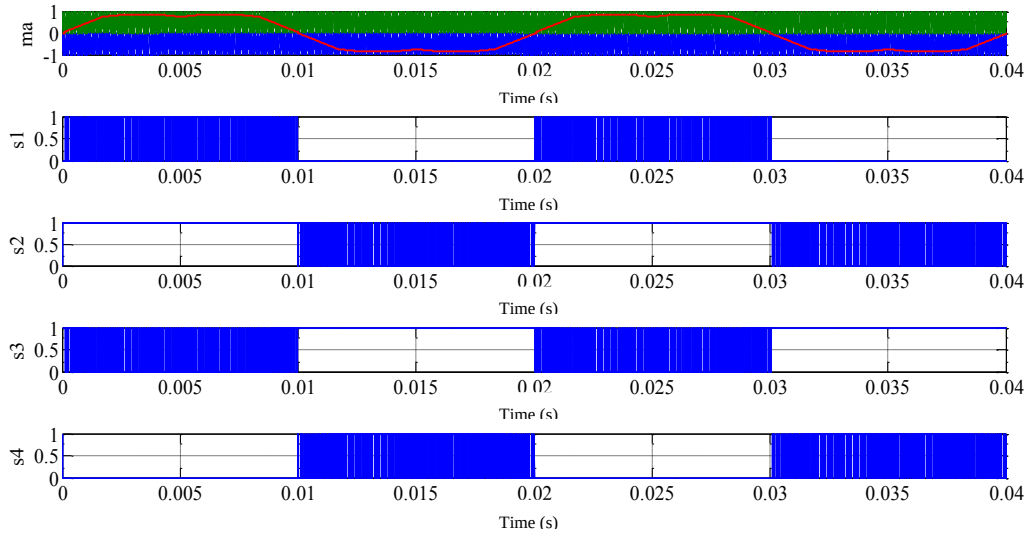


Figure 3-15 – Modulating signal and gate signals of phase A.

3.5 Simulation model of three-phase five-level Diode Clamped inverter

In this section a three-phase five-level inverter will be analyzed. To simulate the inverter and the control system the software Matlab-Simulink will be used.

In Figure 3-16 the general model realized in Simulink is shown. It is composed by the inverter, the R-L load and the control system.

The Diode Clamped inverter is generated by using the Sim Power System library and it's shown in Figure 3-17 while in Figure 3-18 it is possible to see the control system.

In this case, to generate five levels, four carrier signals are needed, varying between [*-1*;*-0.5*], [*-0.5*;*0*], [*0*;*0.5*] and [*0.5*;*1*]. There are eight gate signals for each one of the three phases.

The simulation parameters are listed in Table 3-3.

Frequency	50 [Hz]
DC voltage	565 [V]
Load resistance	2.22 [Ω]
Load inductance	5.3e-3 [H]
DC capacitors	170e-5 [F]

Table 3-3 – Simulation parameters.

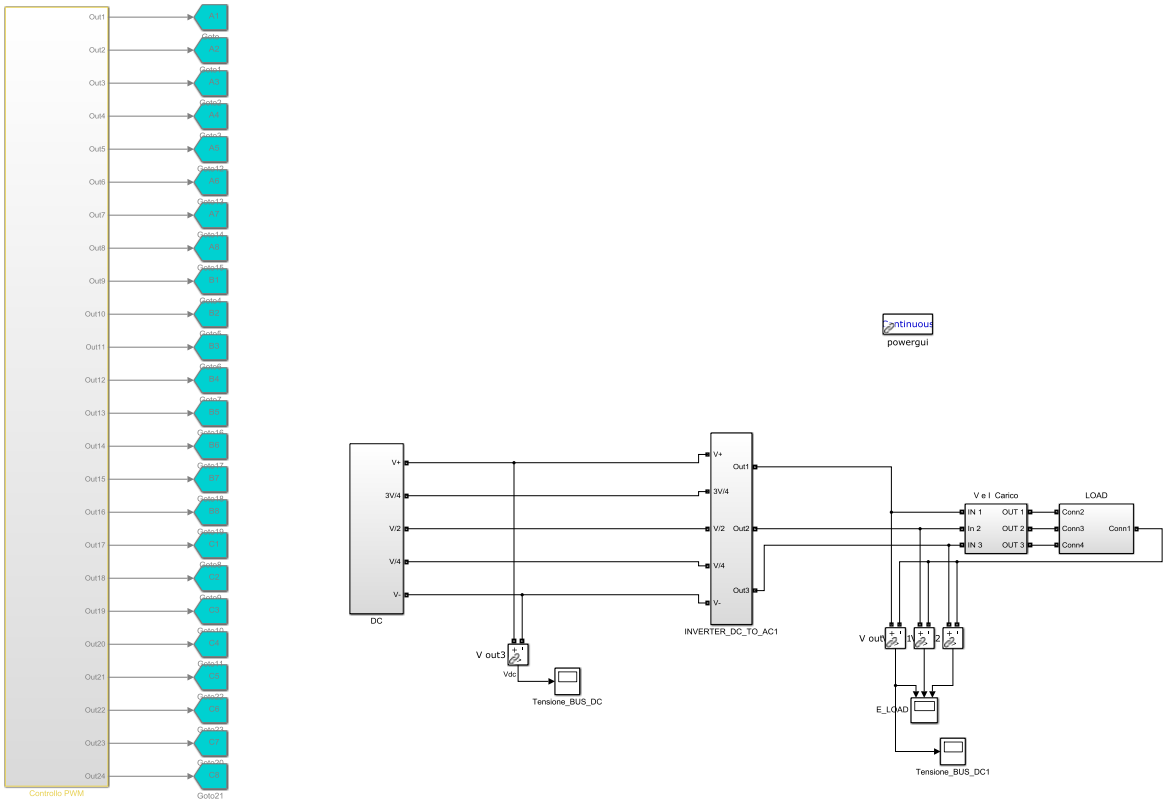


Figure 3-16 – Simulink general model of three-phase five-level Diode Clamped inverter.

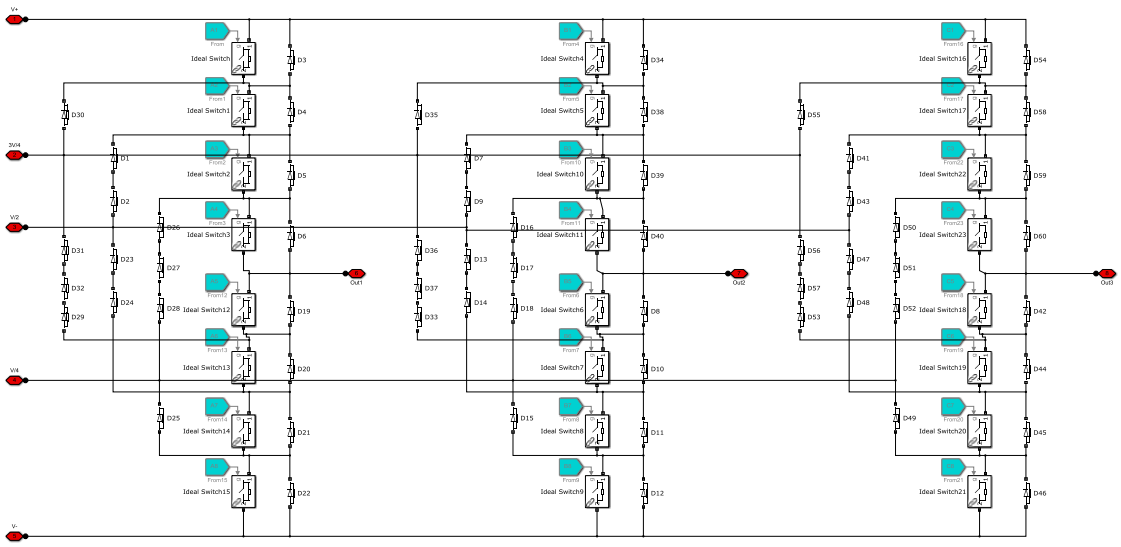


Figure 3-17 – Three-phase five-level Diode Clamped inverter.

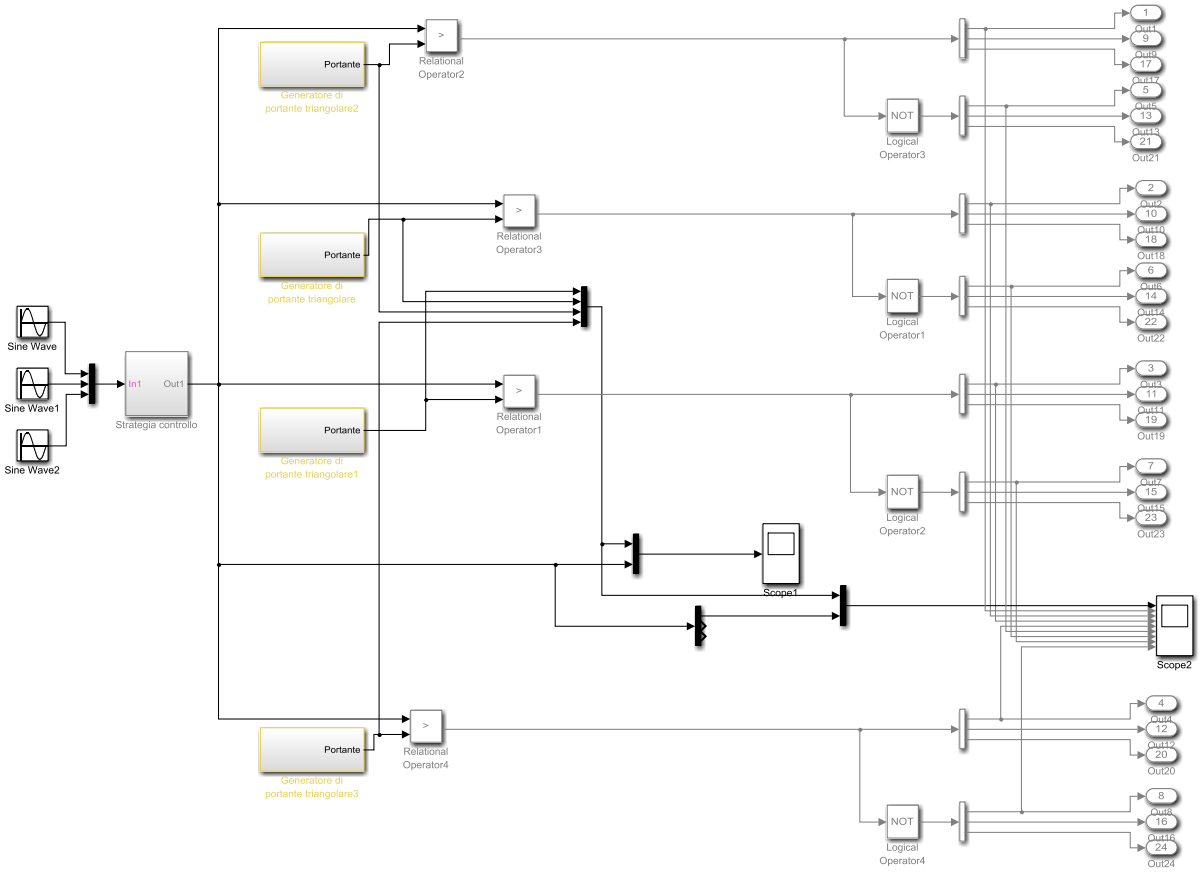


Figure 3-18 – Control system of three-phase five-level Diode Clamped inverter.

3.6 Simulation results of three-phase five-level Diode Clamped inverter

In this section the simulation results of the described configuration will be shown and analyzed.

First of all, in Figure 3-19 the line-to-line voltages are shown. Using equation (3-19) it is possible to calculate that if there are five levels in the pole voltages the line-to-line voltages are composed by nine levels.

In Figure 3-20 the phase voltages are displayed. Using equation (3-20) it is possible to calculate that if there are nine levels in the line-to-line voltages the phase voltages are composed by seventeen levels.

The output currents of the three phases are shown in Figure 3-21.

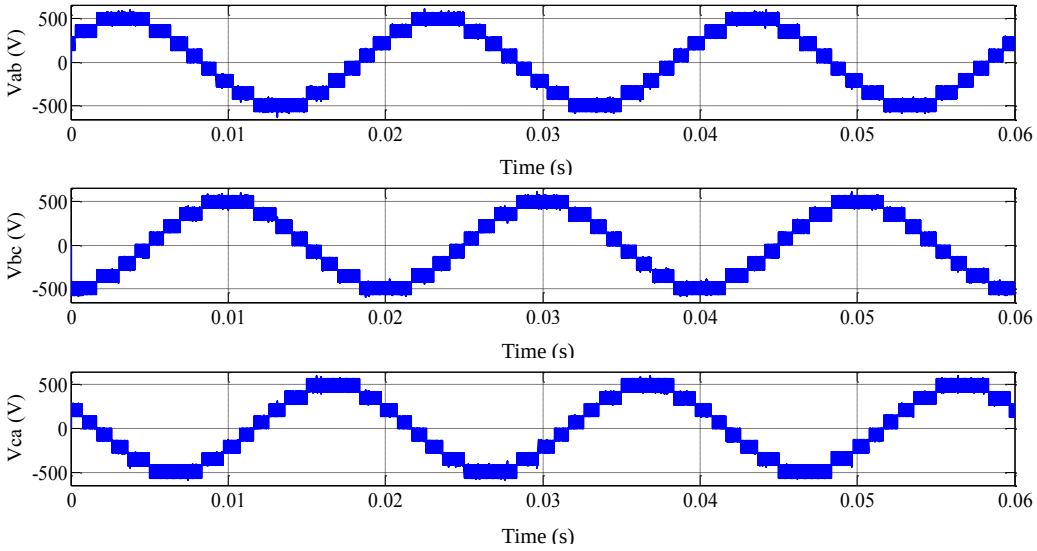


Figure 3-19 – Line-to-line voltages.

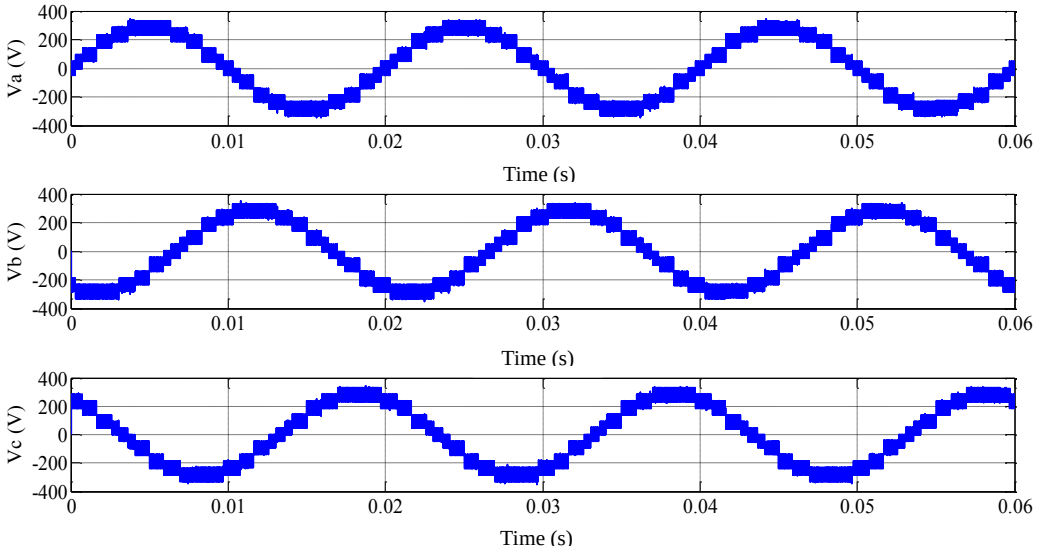


Figure 3-20 – Phase voltages.

In Figure 3-22 the voltage oscillations on the two upper and the two lower DC capacitors are shown.

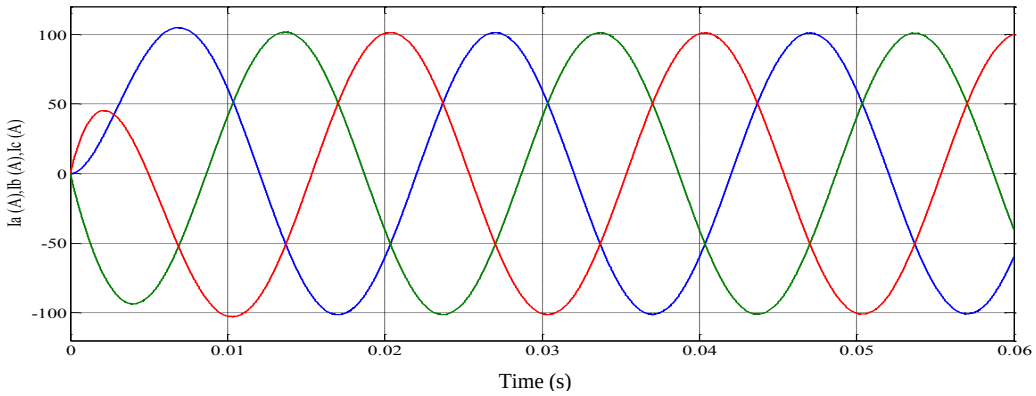


Figure 3-21 – Phase currents.

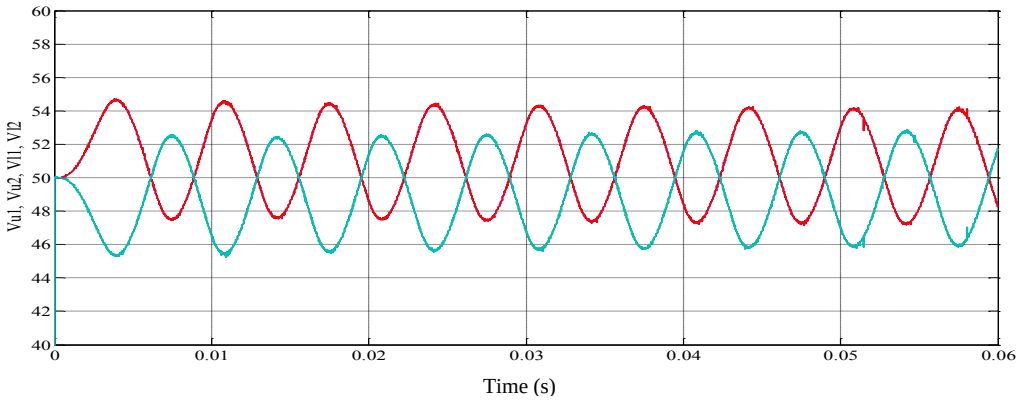


Figure 3-22 – DC capacitor voltage oscillations.

In Figure 3-23 the three modulating signals (one for each phase) are shown with the four carrier signals. The modulation strategy used is PWM symmetrical as it is possible to understand observing the shape of the modulating signals. In Figure 3-24 the modulating signals are displayed in detail.

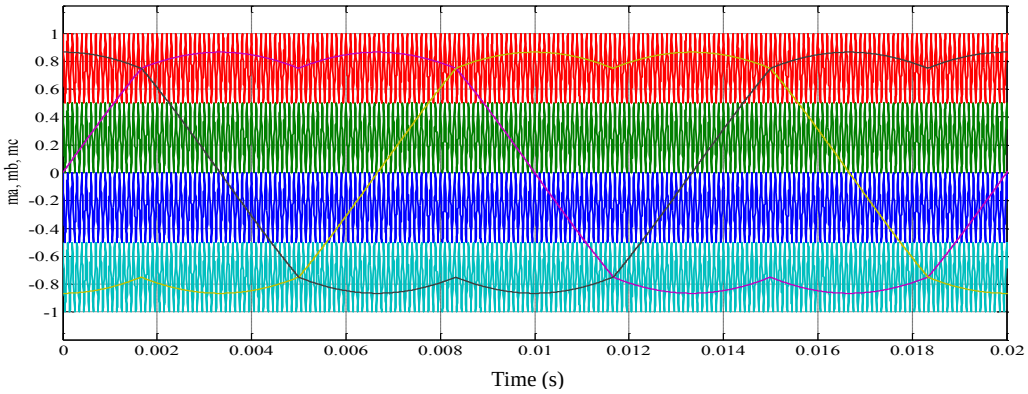


Figure 3-23 – Modulating signals and carrier signals.

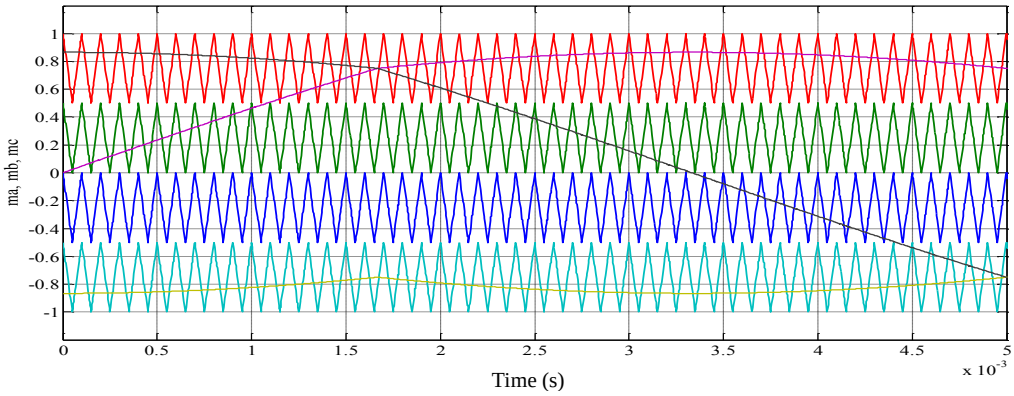


Figure 3-24 – Modulating signals and carrier signals detail.

Finally, in Figure 3-25 it is possible to see the gate signals (i.e. state functions) obtained by the comparison between the modulating signal of one phase and the carrier signals. The gate signals are eight, one for each of the eight power switches that constitute the module.

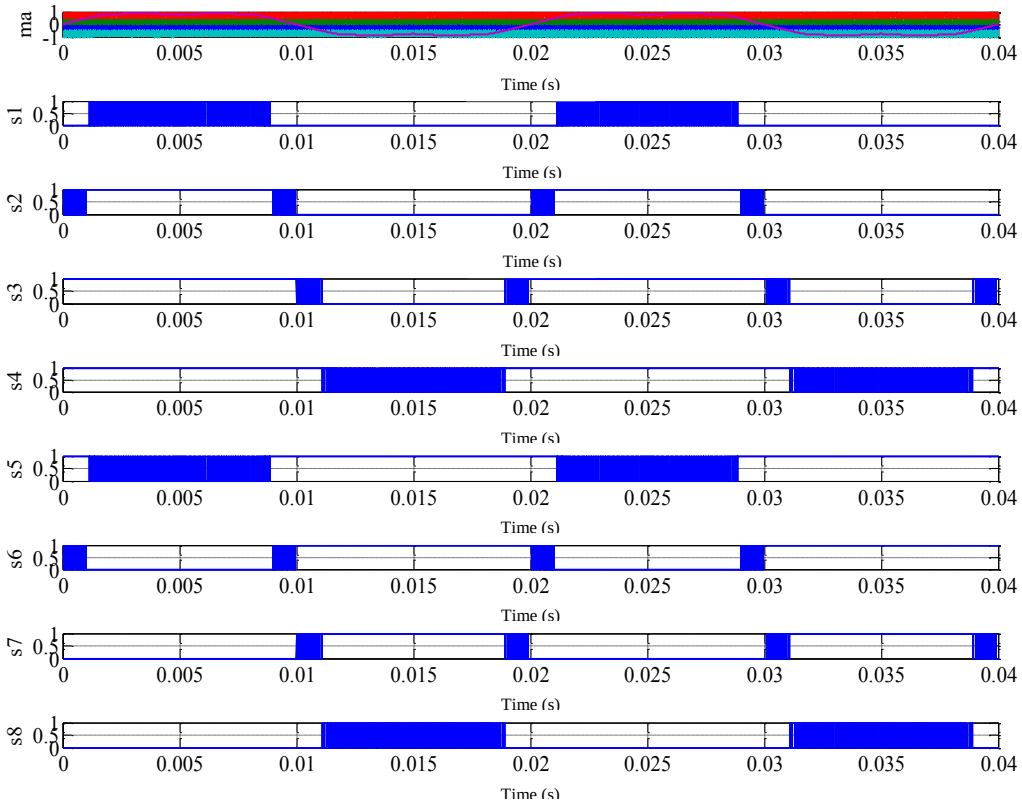


Figure 3-25 – Modulating signal and gate signals of phase A.

4 Cascaded H-bridge Multilevel Inverter

4.1 Introduction

In this chapter a second topology of multilevel inverter will be analyzed. The multilevel Cascaded inverter has a modular architecture. One of the modules that constitute the inverter (i.e. H-bridge) is shown in Figure 4-1.

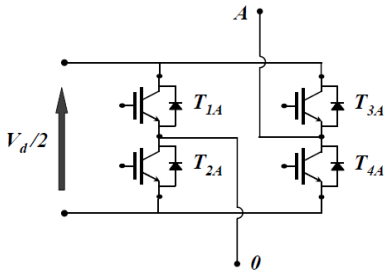


Figure 4-1 – Single module of Cascaded inverter.

It is possible to notice that, in three-level configuration, unlike Diode Clamped topology, only half of the DC voltage is needed.

To reach the required number of levels in the output voltage it is needed a series connection of several modules. If, for example, nine levels are requested it is necessary to connect in series four modules. A single leg is shown in Figure 4-2.

Additionally, it is possible to connect in parallel a different number of legs to reach the desired number of phases. This architecture has a great advantage if compared to Diode Clamped inverter, in fact no DC capacitors are required. This allows to completely overcome the problem to keep under control the voltages across the capacitors. So the control is simpler and there are no limitation in the operation of the inverter.

On the other hand, the relevant limitation in the use of this topology is that, to avoid short circuits, insulated DC sources for each module are necessary needed. But it's also worth to notice that there are some applications that have, by their nature, separated DC sources, for example photovoltaic power stations. Another application that could possibly be well combined with Cascaded inverter is constituted by electric vehicles due to the fact that the DC source is made by separate cells.

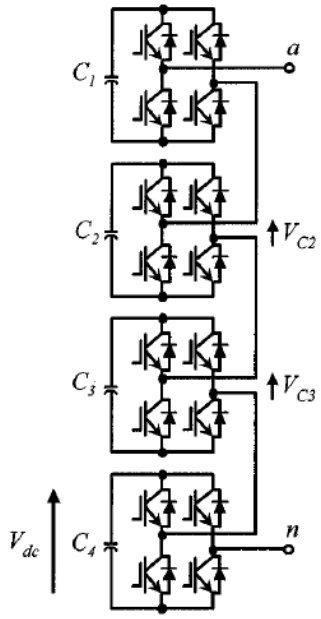


Figure 4-2 – Single phase of nine-level Cascaded inverter.

4.2 Simulation model of three-phase three-level Cascaded inverter

In this section, a three-phase three-level inverter will be analyzed. To simulate the inverter and the control system the software Matlab-Simulink will be used.

In Figure 4-3 the general model realized in Simulink is shown. It is composed by the inverter, the R-L load and the control system.

The Cascaded inverter is generated by using the Sim Power System library and it's shown in Figure 4-4 while in Figure 4-5 it is possible to see the control system.

Two carrier signals, one between *-1* and *0* and the other one between *0* and *1*, are compared with the modulating signals to generate the switching pattern. There are four gate signals for each one of the three phases.

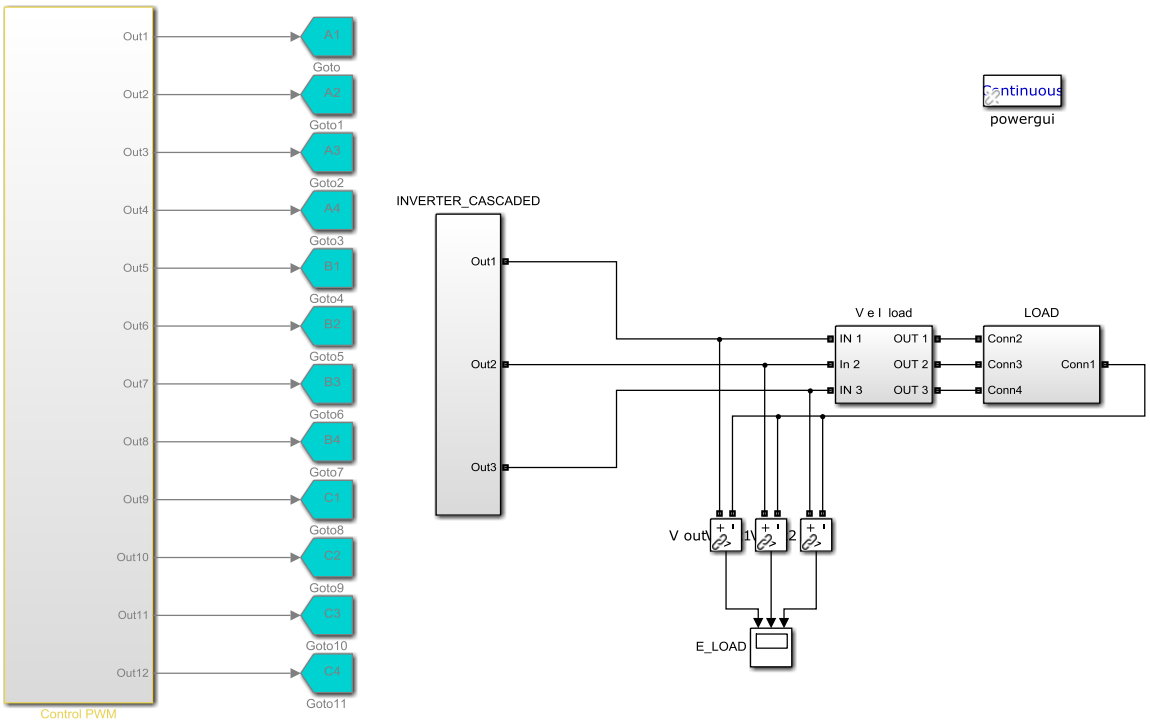


Figure 4-3 – Simulink general model of three-phase three-level Cascaded inverter.

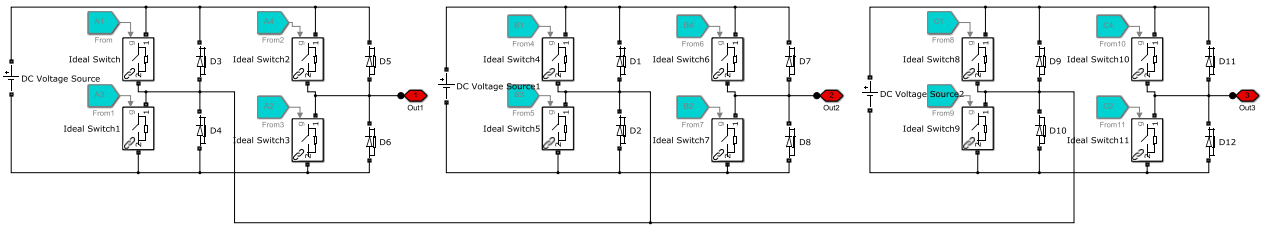


Figure 4-4 – Three-phase three-level Cascaded inverter.

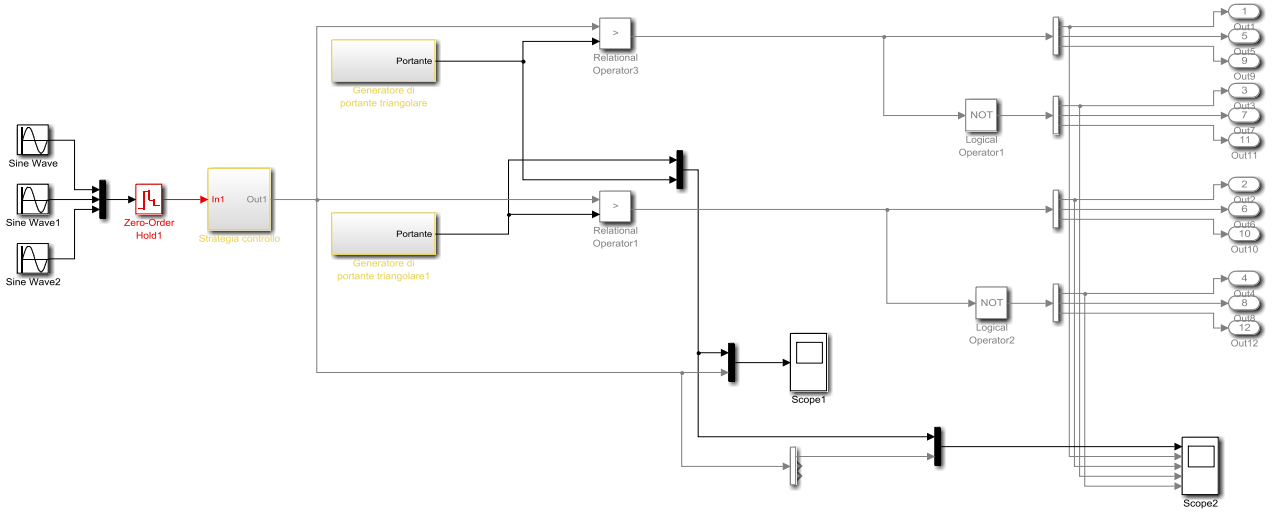


Figure 4-5 – Control system of three-phase three-level Cascaded inverter.

The simulation parameters are listed in Table 4-1.

Frequency	50 [Hz]
DC voltage (single H bridge)	100 [V]
Load resistance	2.22 [Ω]
Load inductance	5.3e-3 [H]

Table 4-1 – Simulation parameters.

4.3 Simulation results of three-phase three-level Cascaded inverter

In this section, the simulation results of the described configuration will be shown and analyzed. First of all in Figure 4-6 the line-to-line voltages are displayed. As already seen if there are three levels in the pole voltages the line-to-line voltages are composed by five levels. The equation that allows this calculation is recalled:

$$k = 2n - 1 \tag{4-1}$$

where n is the number of levels in the pole voltages and k is the number of levels in line-to-line voltages.

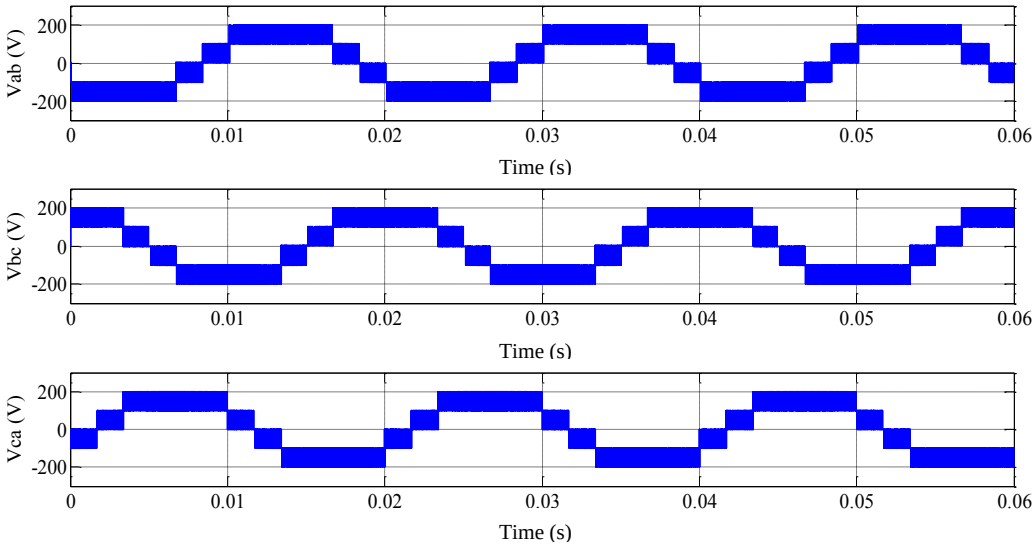


Figure 4-6 – Line-to-line voltages.

In Figure 4-7 the phase voltages are shown.

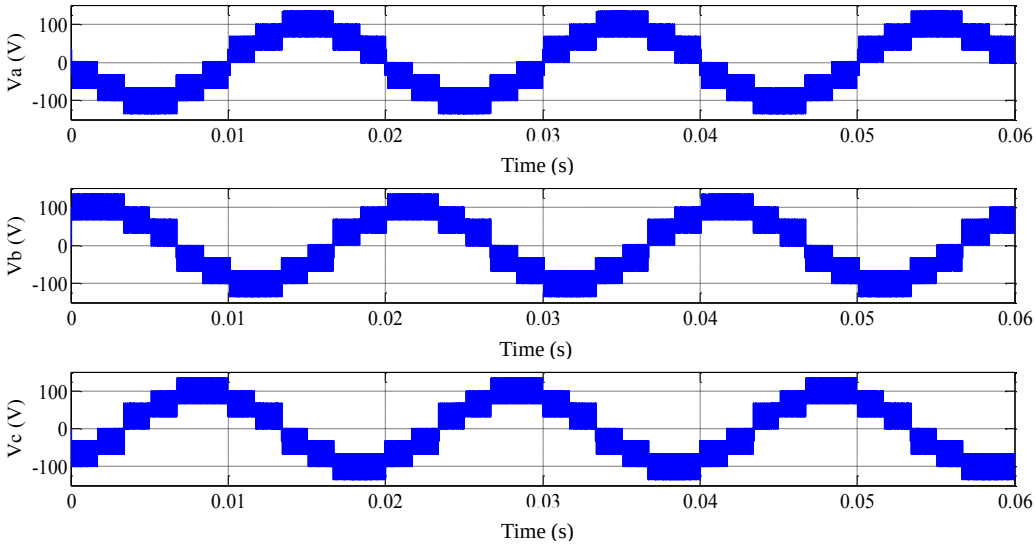


Figure 4-7 – Phase voltages.

As already seen, if there are five levels in the line-to-line voltages the phase voltages are composed by nine levels. The equation that allows this calculation is recalled:

$$p = 2k - 1 \tag{4-2}$$

where k is the number of levels in the line-to-line voltages and p is the number of levels in phase voltages.

The output currents of the three phases are shown in Figure 4-8.

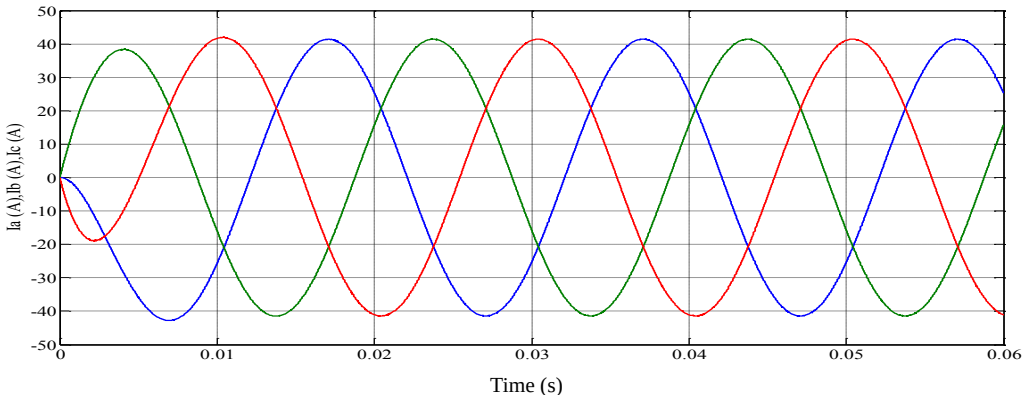


Figure 4-8 – Phase currents.

In Figure 4-9 the three modulating signals (one for each phase) are shown with the two carrier signals. The modulation strategy used is PWM symmetrical as it is possible to understand observing the shape of the modulating signals. In Figure 4-10 the modulating signals are shown in detail.

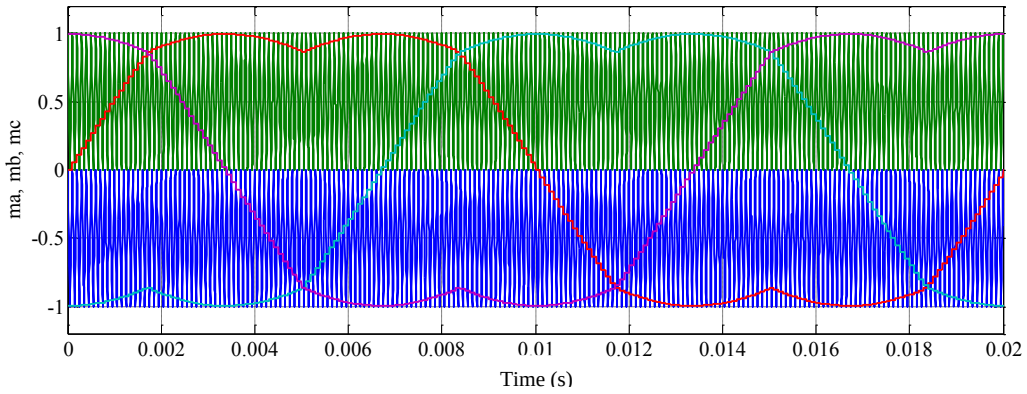


Figure 4-9 – Modulating signals and carrier signals.

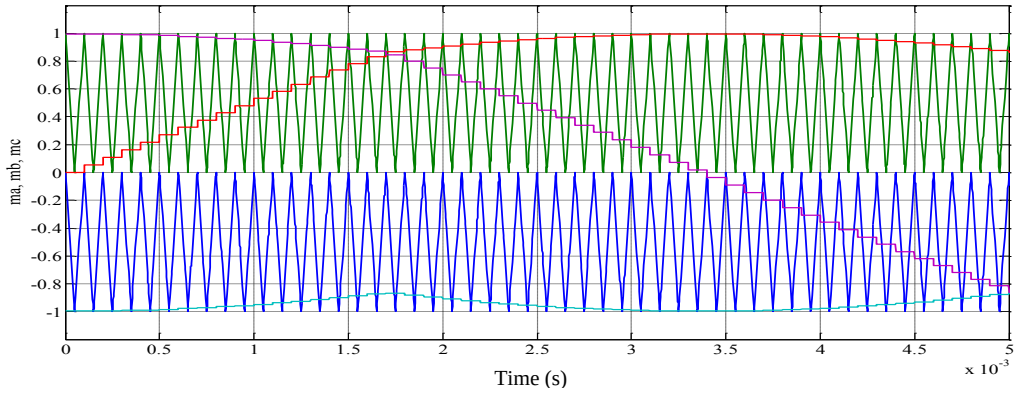


Figure 4-10 – Modulating signals and carrier signals detail.

Finally in Figure 4-11 it is possible to see the gate signals (i.e. state functions) obtained by the comparison between the modulating signal of one phase and the carrier signals. The gate signals are four, one for each of the four power switches that constitute the module.

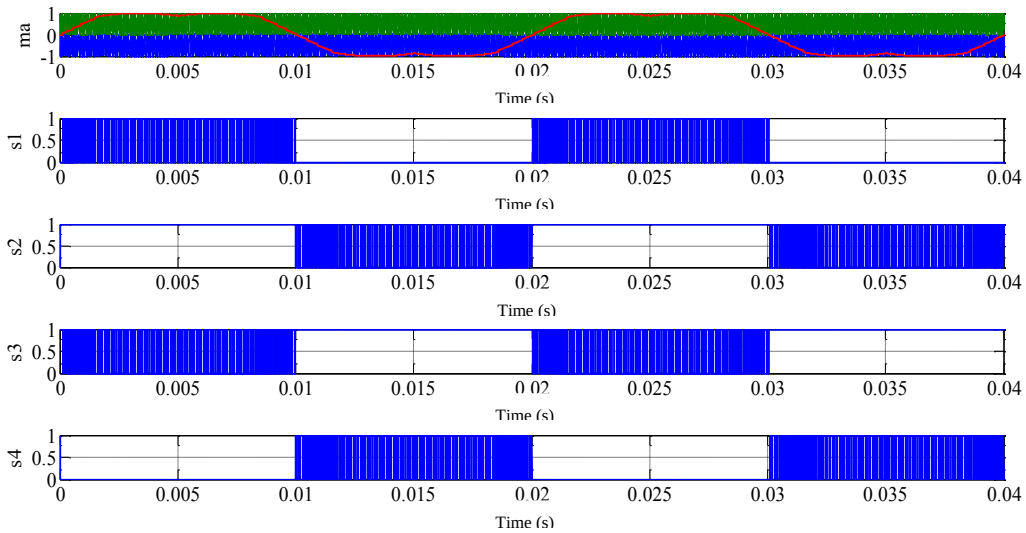


Figure 4-11 – Modulating signal and gate signals of phase A.

4.4 Simulation model of three-phase five-level Cascaded inverter

In this section a three-phase five-level inverter will be analyzed. To simulate the inverter and the control system the software Matlab-Simulink will be used.

In Figure 4-12 the general model realized in Simulink is shown. It is composed by the inverter, the R-L load and the control system.

The Cascaded inverter is generated by using Sim Power System library and it's shown in Figure 4-13 while in Figure 4-14 it is possible to see the control system.

In this case, to generate five levels, four carrier signals are needed, varying between [*-1*;*-0.5*], [*-0.5*;*0*], [*0*;*0.5*] and [*0.5*;*1*]. There are eight gate signals for each one of the three phases.

The simulation parameters are listed in Table 4-2.

Frequency	50 [Hz]
DC voltage (single H bridge)	100 [V]
Load resistance	2.22 [Ω]
Load inductance	5.3e-3 [H]

Table 4-2 – Simulation parameters.

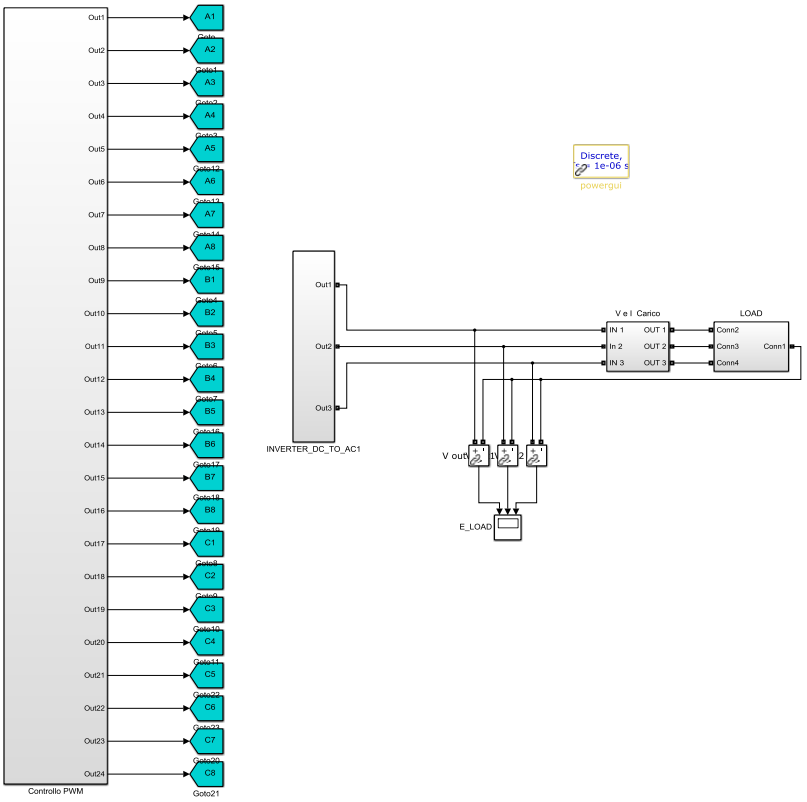


Figure 4-12 – Simulink general model of three-phase five-level Cascaded inverter.

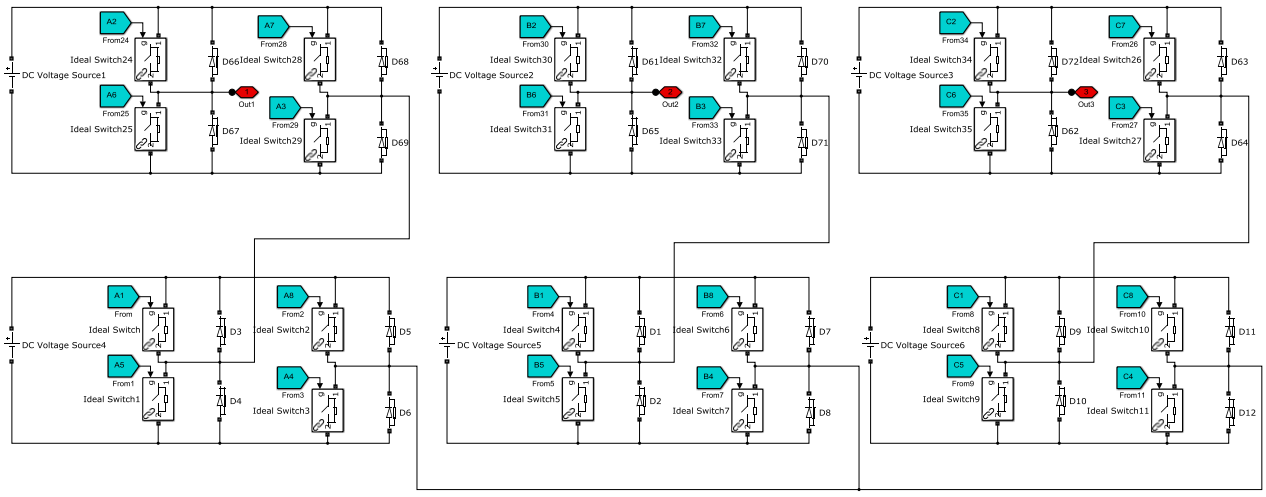


Figure 4-13 – Three-phase five-level Cascaded inverter.

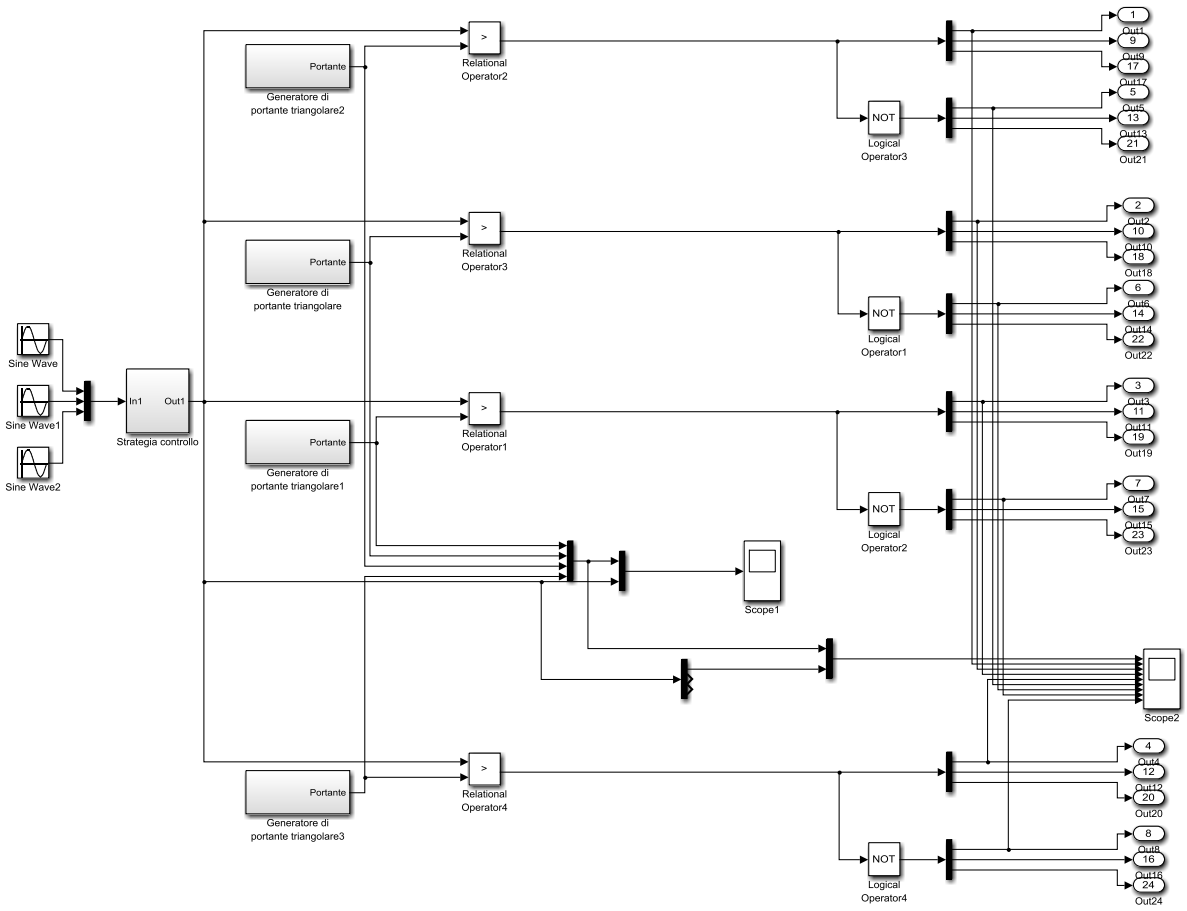


Figure 4-14 – Control system of three-phase five-level Cascaded inverter.

4.5 Simulation results of three-phase five-level Cascaded inverter

In this section the simulation results of the described configuration will be shown and analyzed.

First of all in Figure 4-15 the line-to-line voltages are displayed. Using equation (4-1) it is possible to calculate that if there are five levels in the pole voltages the line-to-line voltages are composed by nine levels.

In Figure 4-16 the phase voltages are shown. Using equation (4-2) it is possible to calculate that if there are nine levels in the line-to-line voltages the phase voltages are composed by seventeen levels.

The output currents of the three phases are shown in Figure 4-17.

In Figure 4-18 the three modulating signals (one for each phase) are shown with the four carrier signals. The modulation strategy used is PWM symmetrical as it is possible to understand observing the shape of the modulating signals. In Figure 4-19 the modulating signals are shown in detail.

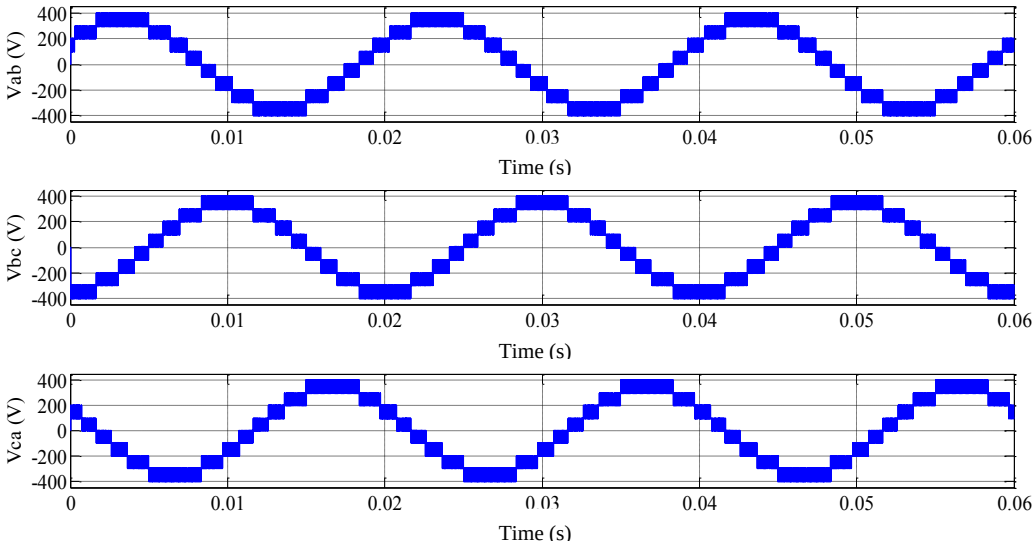


Figure 4-15 – Line-to-line voltages.

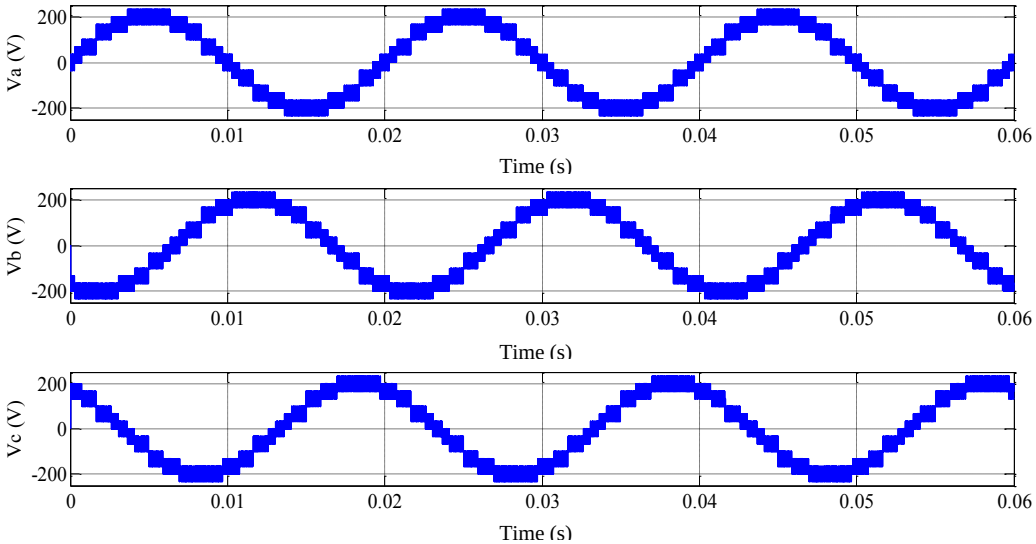


Figure 4-16 – Phase voltages.

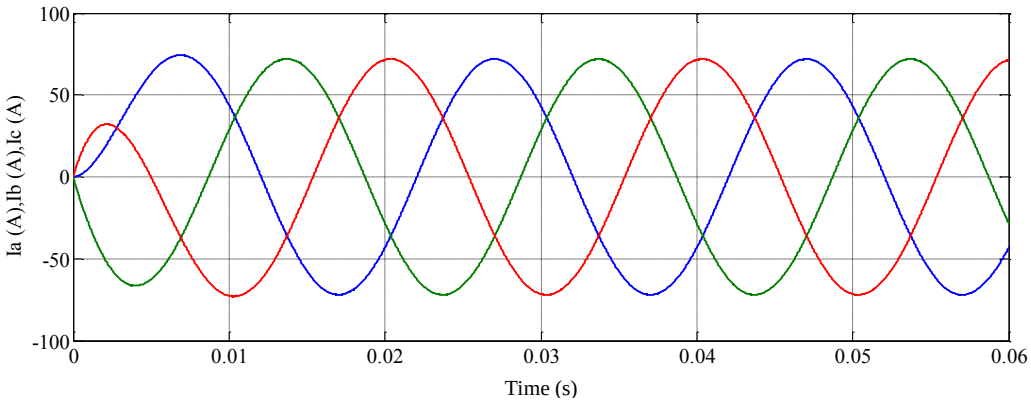


Figure 4-17 – Phase currents.

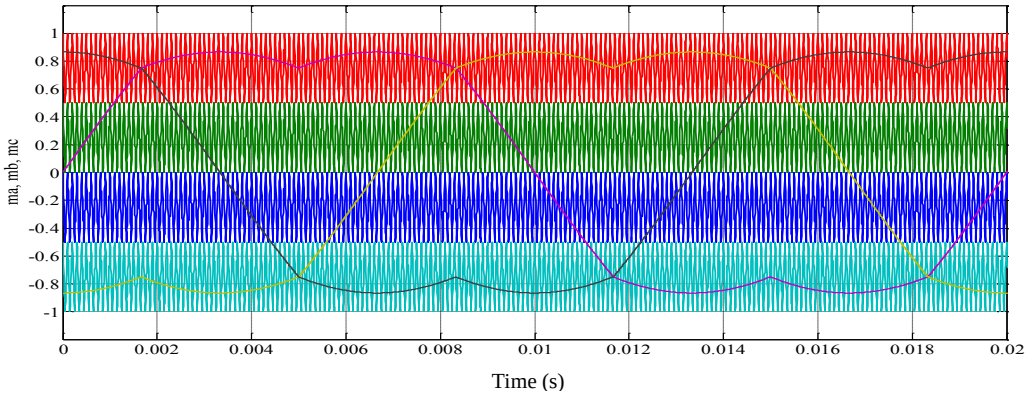


Figure 4-18 – Modulating signals and carrier signals.

Finally in Figure 4-20 it is possible to see the gate signals (i.e. state functions) obtained by the comparison between the modulating signal of one phase and the carrier signals. The gate signals are eight, one for each of the eight power switches that constitute the module.

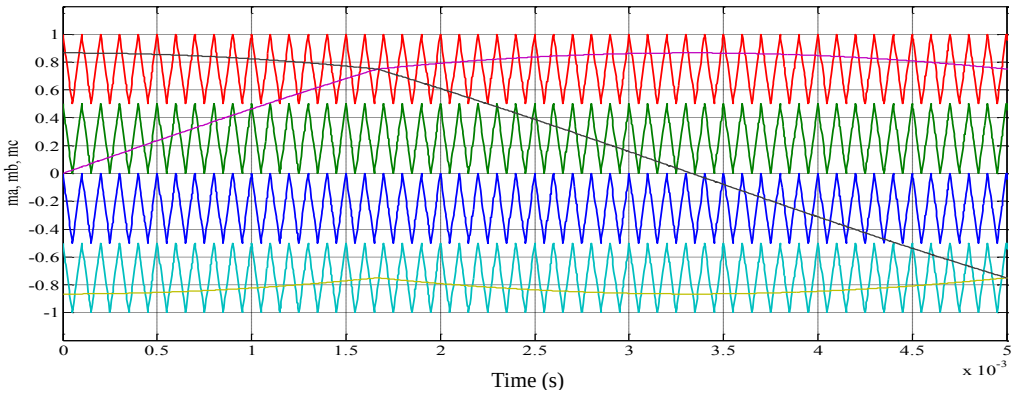


Figure 4-19 – Modulating signals and carrier signals detail.

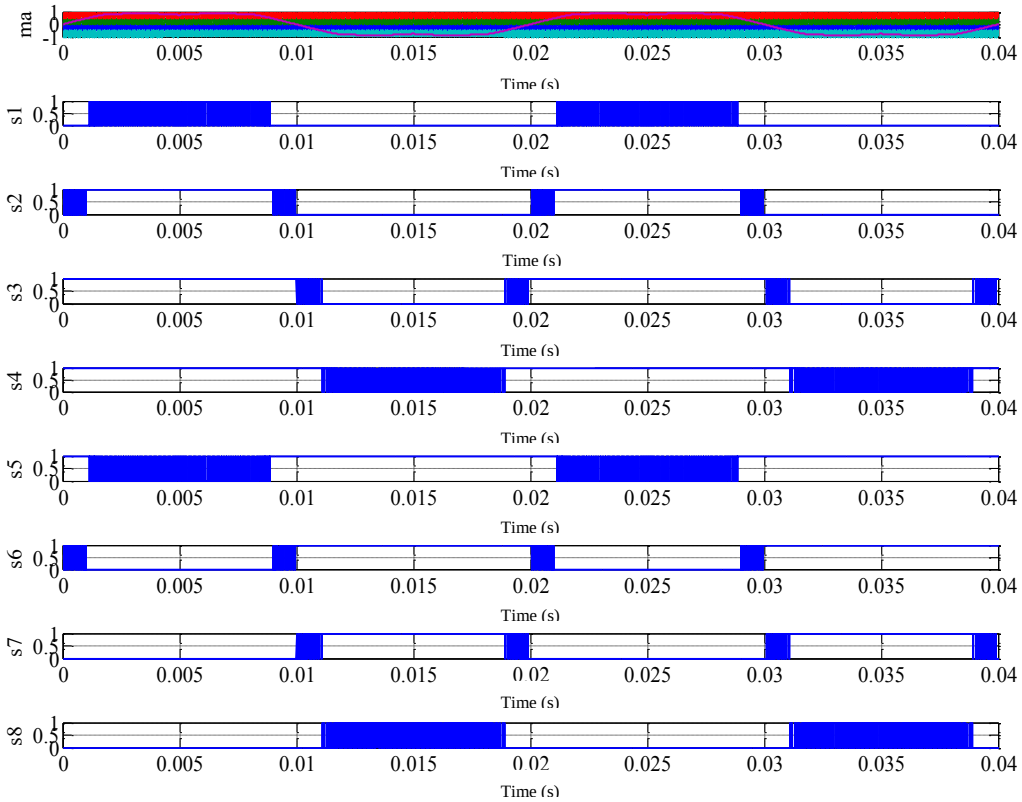


Figure 4-20 – Modulating signal and gate signals of phase A.

5 MMC – Modular Multilevel Converter

5.1 Introduction

Modular multilevel converter (MMC) is an emerging multilevel topology for high-voltage applications that has been developed in recent years. Voltage Source Converter (VSC) technology is becoming common in high-voltage direct current (HVDC) transmission systems for renewable energies (e.g., transmission of offshore wind power, among others).

The possible advantages of choosing HVDC instead of AC to transmit power are the possibilities of lower losses over long distances and lower cost. One of the most important advantages of HVDC over conventional AC systems is related with the capability to accurately control the active power transmitted without incurring in network instability. Many multi-level inverter topologies have been investigated in recent years, but their structure for very high voltages can become unpractical. In fact, conventional inverters do not meet easily the requirements of HVDC transmission in terms of voltage level, quality and power level.

A viable solution to these problems is represented by the modular multilevel converter. Compared to conventional VSC technology, the modular multilevel topology offers advantages such as higher voltage levels, modular structure, longer maintenance intervals and improved reliability. The multilevel approach ensures a reduction in the harmonics of the output voltages and nearly sinusoidal output currents. Consequently, the grid filters become negligible, thus leading to a reduction in the cost and in the complexity of the system.

This topology seems very promising for high power applications in the near future, particularly for HVDC links, and has been investigated extensively. The literature is mainly focused on the analysis of simplified circuit models and proposes some control schemes to achieve a reliable and stable operation of the inverter. Since the voltages of the multiple sub-modules in each arm have to be balanced and, similarly, the energies of the upper and lower arms have to be equalized, the control of the voltages in the upper arm and in the lower arm is a crucial point as it determines the overall performance of the inverter.

In Figure 5-1 a typical HVDC application with a back to back MMC inverter is shown.

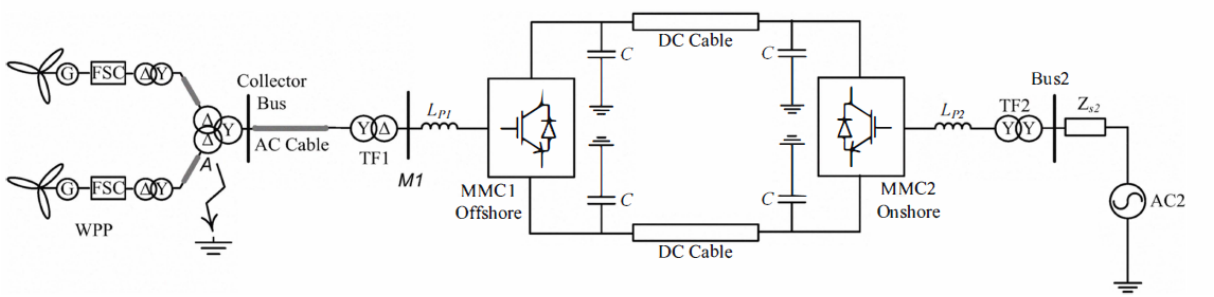


Figure 5-1 – HVDC application with back to back MMC inverter.

5.2 Single leg MMC

Figure 5-2 shows a single leg of the MMC architecture with *n* sub-modules connected in series for each one of two arms that constitute the leg.

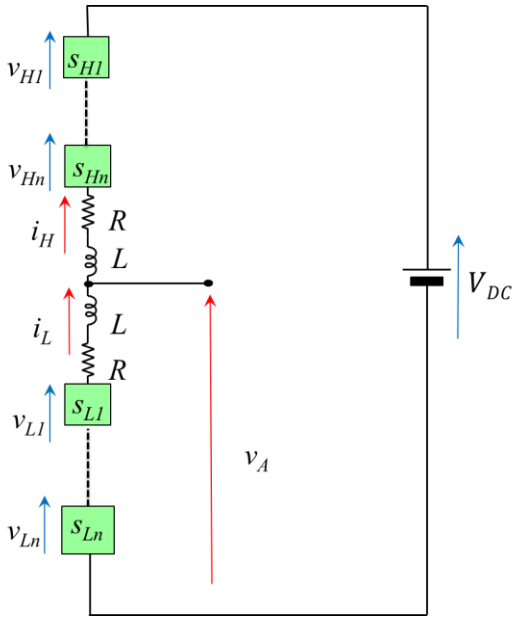


Figure 5-2 – Scheme of a single leg MMC with *n* sub-modules for each arm.

Figure 5-3 shows a detailed rapresentation of the generic module. As it is possible to see there are two IGBTs with the reverse recovery diode connected in series and a capacitor connected in parallel to them.

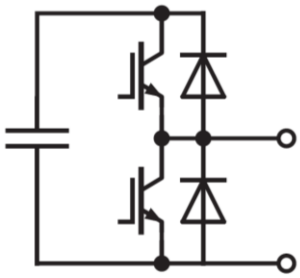


Figure 5-3 – Generic MMC module.

In this chapter the constitutive equations for the single generic module will be written. It will be rigorously analyzed how it is possible to simplify a leg having a generic number of modules, with an equivalent leg having one single module in the upper arm and one single module in the lower arm.

Given this leg with the equivalent modules, the equations are processed to obtain a suitable form to design a control technique.

The expressions of the capacitors stored energy are considered to design and compare different techniques based on the control of such energies.

5.2.1 Model equations

Figure 5-4 shows an MMC leg with one equivalent module for each one of the two arms. In paragraph 5.2.18 it will be demonstrated that a series of *n* sub-modules could be represented with one equivalent module under appropriate assumptions.

A generic R-L-E load is connected between the central point of the phase and the neutral point.

First of all it is necessary to write the two equations of the upper and lower modules:

$$v_H = s_H v_{CH} \tag{5-1}$$

$$v_L = s_L v_{CL} \tag{5-2}$$

where s_H and s_L are the modulation indexes of the upper and lower modules whereas v_{CH} and v_{CL} are the voltages of the upper and lower capacitors. The quantities v_H and v_L are the output voltages of the upper and lower modules.

When the module is inserted the arm current is exactly equal to the capacitor current, while when the module is bypassed the capacitor current is zero.

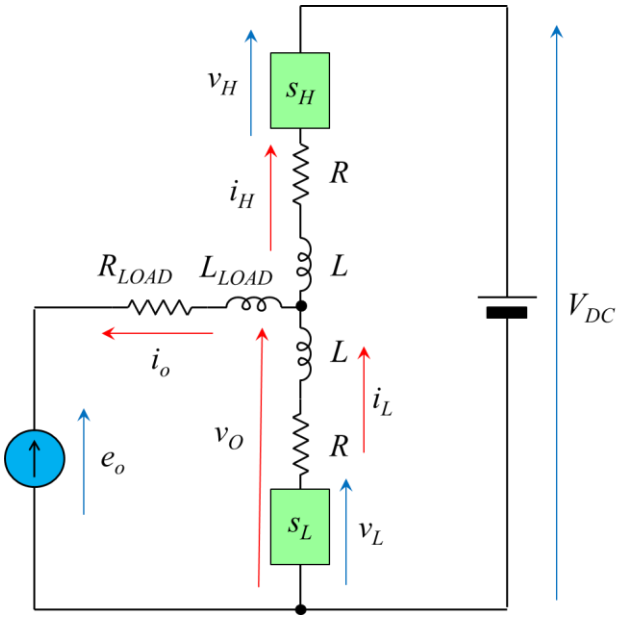


Figure 5-4 – Scheme of a single leg MMC.

So the equations of the currents of the upper and lower modules are:

$$i_{CH} = s_H i_H \tag{5-3}$$

$$i_{CL} = s_L i_L \tag{5-4}$$

where i_{CH} and i_{CL} are the currents on the upper and lower capacitors and i_H and i_L are the currents of the upper and lower arms.

The equations of the upper and lower capacitors of the modules are:

$$\frac{dv_{CH}}{dt} = -\frac{i_{CH}}{C} \tag{5-5}$$

$$\frac{dv_{CL}}{dt} = -\frac{i_{CL}}{C} \tag{5-6}$$

where C is the equivalent total capacitance of the SMs in the lower and upper arms.

The output current i_o can be expressed as the sum of the currents of the upper arm and lower arm as follows (i.e. Kirchhoff's current law):

$$i_0 = i_L - i_H \tag{5-7}$$

Some Authors have proposed to introduce the concept of differential or circulating current i_d which is a combination of the arm currents. The definition of the circulating current is not unique. From now on it will be defined as the half of the difference between the current flowing in the upper arm

and the current flowing in the lower arm. The current i_d flows through the whole leg and goes to the DC source without affecting the grid:

$$i_d = \frac{i_L + i_H}{2} \tag{5-8}$$

Starting from equations (5-7) and (5-8) the currents i_H and i_L can be expressed as functions of i_o and i_d as follows:

$$i_H = i_d - \frac{i_0}{2} \tag{5-9}$$

$$i_L = i_d + \frac{i_0}{2} \tag{5-10}$$

With reference to the scheme of Figure 5-4, it is possible to write the equations of the upper and lower arms of the MMC and the equation of the load. These are as follows:

$$V_c - v_H + Ri_H + L\frac{di_H}{dt} - v_0 = 0 \tag{5-11}$$

$$v_L - Ri_L - L\frac{di_L}{dt} - v_0 = 0 \tag{5-12}$$

$$v_0 - e_0 - R_{LOAD}i_0 - L_{LOAD}\frac{di_0}{dt} = 0 \tag{5-13}$$

where, as already seen, i_H and i_L are the upper and lower arm currents, v_H and v_L are the upper and lower sub-modules output voltages, whereas L and R are the arm inductance and resistance, V_c is the dc voltage, and v_o is the output voltage applied by the inverter to the load.

By adding and subtracting equations (5-11) and (5-12) it is possible to obtain the following relations:

$$\frac{v_L - v_H}{2} = v_0 - \frac{V_c}{2} + \frac{R}{2}(i_L - i_H) + \frac{L}{2}\frac{d}{dt}(i_L - i_H) \tag{5-14}$$

$$\frac{v_L + v_H}{2} = \frac{V_c}{2} + R\frac{(i_L + i_H)}{2} + L\frac{d}{dt}\frac{(i_L + i_H)}{2} \tag{5-15}$$

At this stage it's convenient to introduce the definition of differential voltage between the lower and upper modules v_d and the average voltage between the two modules v_{int}. These voltages are the combination of the voltages v_H and v_L and it's not possible to directly measure them. They are defined as follow:

$$v_{\text{int}} = \frac{v_L - v_H}{2} \tag{5-16}$$

$$v_d = \frac{v_L + v_H}{2} \tag{5-17}$$

The inverse transformations are:

$$v_H = v_d - v_{\text{int}} \tag{5-18}$$

$$v_L = v_d + v_{\text{int}} \tag{5-19}$$

By substituting the definitions (5-9), (5-10) and (5-18), (5-19) into equations (5-14) and (5-15), it is possible to obtain:

$$v_{\text{int}} = e_0 - \frac{V_c}{2} + R_{eq} i_0 + L_{eq} \frac{di_0}{dt} \tag{5-20}$$

$$v_d = \frac{V_c}{2} + R i_d + L \frac{di_d}{dt} \tag{5-21}$$

where the definitions of the equivalent resistance and the equivalent inductance are:

$$R_{eq} = \frac{R}{2} + R_{LOAD} \tag{5-22}$$

$$L_{eq} = \frac{L}{2} + L_{LOAD} \tag{5-23}$$

The equations (5-20) and (5-21) show a direct correlation between the voltage v_{int} and the load current i_o and between the voltage v_d and the differential current i_d and can be implemented in the control system if the parameters of the system are known.

5.2.2 Energy equations

To control the capacitor voltages, which are directly correlated to the stability and the performances of the system, it is useful to calculate the electromagnetic energies W_{CH} and W_{CL} stored in the upper and lower capacitors as follows:

$$\frac{dW_{CH}}{dt} = \frac{1}{2} C v_{CH}^2 = v_{CH} C \frac{dv_{CH}}{dt} = -v_{CH} i_{CH} = -v_H i_H \tag{5-24}$$

$$\frac{dW_{CL}}{dt} = \frac{1}{2} C v_{CL}^2 = v_{CL} C \frac{dv_{CL}}{dt} = -v_{CL} i_{CL} = -v_L i_L \tag{5-25}$$

These last expressions are obtained considering equations (5-1)-(5-6).

It is then possible to substitute equation (5-9) and (5-18) into (5-24) and equation (5-10) and (5-19) into (5-25) obtaining:

$$\frac{dW_{CH}}{dt} = -(v_d - v_{\text{int}})(i_d - \frac{i_0}{2}) \tag{5-26}$$

$$\frac{dW_{CL}}{dt} = -(v_d + v_{\text{int}})(i_d + \frac{i_0}{2}) \tag{5-27}$$

From the previous relations it is possible to understand that the differential current is the only degree of freedom that can be used to balance the energies of the capacitors. With one variable it's necessary to manage two quantities, for this reason it is not possible to control the instantaneous value of both the energies. What can be achieved, is the control of the average values of the capacitor voltages, but they will be still affected by voltage oscillations and how to construct the reference signal for the differential current is not a trivial task.

It is interesting to use the relations (5-26) and (5-27) to introduce the definitions of total energy W_{CT} and differential energy $W_{C\Delta}$ of the capacitors of the leg as follows:

$$\frac{dW_{CT}}{dt} = \frac{d(W_{CH} + W_{CL})}{dt} = -2 v_d i_d - v_{\text{int}} i_0 \tag{5-28}$$

$$\frac{dW_{C\Delta}}{dt} = \frac{d(W_{CH} - W_{CL})}{dt} = v_d i_0 + 2 v_{\text{int}} i_d \tag{5-29}$$

5.2.3 Steady state solution

To understand how it is possible to implement equations (5-28) and (5-29) first of all it is interesting to find a steady state solution.

The emf of the load is the sum of a constant contribute and a sinusoidal contribute. The constant part must be equal to half of the DC voltage due to the choice of the load connection.

$$e_0 = E_0 + \Re\{\overline{E}_0 e^{j\omega t}\}; E_0 = \frac{V_c}{2} \tag{5-30}$$

In general the load current can be constituted by a constant contribute and a sinusoidal contribute.

$$i_0 = I_{00} + \Re\{\bar{I}_0 e^{j\omega t}\} \tag{5-31}$$

The differential current in general can be constructed with an infinite number of sinusoidal contributes as shown in the following equation:

$$i_d = \sum_{k=0}^{\infty} \Re\{\bar{I}_{dk} e^{jk\omega t}\} \tag{5-32}$$

By substituting (5-30), (5-31) and (5-32) into equation (5-20) and (5-21) it is possible to obtain:

$$v_{\text{int}} = R_{eq} I_{00} + \Re\{[(j\omega L_{eq} + R_{eq})\bar{I}_0 + \bar{E}_0] e^{jk\omega t}\} \tag{5-33}$$

$$v_d = \frac{V_c}{2} + \sum_{k=0}^{\infty} \Re\{(jk\omega L + R)\bar{I}_{dk} e^{jk\omega t}\} \tag{5-34}$$

It's convenient to introduce the following definitions:

$$\bar{V}_0 = [(j\omega L_{eq} + R_{eq})\bar{I}_0 + \bar{E}_0] \tag{5-35}$$

$$\bar{Z}_{dk} = (jk\omega L + R) \tag{5-36}$$

So equation (5-33) and (5-34) become:

$$v_{\text{int}} = R_{eq} I_{00} + \Re\{\bar{V}_0 e^{jk\omega t}\} \tag{5-37}$$

$$v_d = \frac{V_c}{2} + \sum_{k=0}^{\infty} \Re\{\bar{Z}_{dk} \bar{I}_{dk} e^{jk\omega t}\} \tag{5-38}$$

Finally if the previous definitions are introduced into equations (5-28) and (5-29) it is possible to obtain the relations for total energy and differential energy:

$$\frac{dW_{CT}}{dt} = -2\left(\frac{V_c}{2} + \sum_{k=0}^{\infty} \Re\{\bar{Z}_{dk} \bar{I}_{dk} e^{jk\omega t}\}\right)\left(\sum_{k=0}^{\infty} \Re\{\bar{I}_{dk} e^{jk\omega t}\}\right) - (R_{eq} I_{00} - \Re\{\bar{V}_0 e^{jk\omega t}\})(I_{00} + \Re\{\bar{I}_0 e^{j\omega t}\}) \tag{5-39}$$

$$\frac{dW_{C\Delta}}{dt} = \left(\frac{V_c}{2} + \sum_{k=0}^{\infty} \Re\{\bar{Z}_{dk} \bar{I}_{dk} e^{jk\omega t}\}\right)(I_{00} + \Re\{\bar{I}_0 e^{j\omega t}\}) + 2(R_{eq} I_{00} + \Re\{\bar{V}_0 e^{jk\omega t}\})\left(\sum_{k=0}^{\infty} \Re\{\bar{I}_{dk} e^{jk\omega t}\}\right) \tag{5-40}$$

Developing all the products:

$$\begin{aligned} \frac{dW_{CT}}{dt} = & -\sum_{k=0}^{\infty}\sum_{h=0}^{\infty} (\Re\{\bar{Z}_{dk} \bar{I}_{dk} \bar{I}_{dh} e^{j(k+h)\omega t}\} + \Re\{\bar{Z}_{dk} \bar{I}_{dk} \bar{I}_{dh}^{*} e^{j(k-h)\omega t}\}) - V_c \sum_{k=0}^{\infty} \Re\{\bar{I}_{dk} e^{jk\omega t}\} - \\ & - R_{eq} I_{00} \Re\{\bar{I}_0 e^{j\omega t}\} - R_{eq} I_{00}^2 - I_{00} \Re\{\bar{V}_0 e^{j\omega t}\} - \frac{1}{2}\Re\{\bar{I}_0 \bar{V}_0 e^{j2\omega t}\} - \frac{1}{2}\Re\{\bar{I}_0 \bar{V}_0^{*}\} \end{aligned} \tag{5-41}$$

$$\frac{dW_{C\Delta}}{dt} = \frac{V_c}{2} I_{00} + \frac{1}{2}\sum_{k=0}^{\infty} \Re\{\bar{Z}_{dk}\bar{I}_0\bar{I}_{dk}e^{j(k+1)\omega t}\} + \frac{1}{2}\sum_{k=0}^{\infty} \Re\{\bar{Z}_{dk}\bar{I}_{dk}\bar{I}_0^* e^{j(k-1)\omega t}\} + I_{00}\sum_{k=0}^{\infty} \Re\{\bar{Z}_{dk}\bar{I}_{dk}e^{jk\omega t}\} +$$
$$+ \frac{V_c}{2}\Re\{\bar{I}_0 e^{j\omega t}\} + 2R_{eq}I_{00}\sum_{k=0}^{\infty}\Re\{\bar{I}_{dk}e^{jk\omega t}\} + \sum_{k=0}^{\infty}\Re\{\bar{V}_0\bar{I}_{dk}e^{j(k+1)\omega t}\} + \sum_{k=0}^{\infty}\Re\{\bar{V}_0^*\bar{I}_{dk}e^{j(k-1)\omega t)}\} \quad (5\text{-}42)$$

In the two equations there are a dc term and an infinite number of sinusoidal terms in steady state conditions. A dc component in equation (5-41), total energy, means the capacitors endure to charge or discharge indefinitely depending on the sign. A dc component in equation (5-42), differential energy, brings to unbalance between the upper and lower capacitor. So it's necessary to keep these two dc components under control in order to achieve a correct behavior of the inverter.

The sinusoidal terms bring an average contribute equal to zero if integrated into a period, that is the fundamental period of the load current.

So if only the dc components are considered the equations became:

$$\frac{dW_{CT}}{dt}(dc) = \Re\{\bar{Z}_{d0}\bar{I}_{d0}^2\} - \sum_{\gamma=0}^{\infty}\Re\{\bar{Z}_{d\gamma}\bar{I}_{d\gamma}\bar{I}_{d\gamma}^*\} - V_c\Re\{\bar{I}_{d0}\} - R_{eq}I_{00}^2 - \frac{1}{2}\Re\{\bar{I}_0\bar{V}_0^*\} \quad (5\text{-}43)$$

$$\frac{dW_{C\Delta}}{dt}(dc) = \frac{V_c}{2}I_{00} + \frac{1}{2}\Re\{\bar{Z}_{d1}\bar{I}_{d1}\bar{I}_0^*\} + I_{00}\Re\{\bar{Z}_{d0}\bar{I}_{d0}\} + 2R_{eq}I_{00}\Re\{\bar{I}_{d0}\} + \Re\{\bar{V}_0^*\bar{I}_{d1}\} \quad (5\text{-}44)$$

To simplify the analysis it's possible to erase the terms where there is the resistance of the arm because its value is negligible. The equations become:

$$\frac{dW_{CT}}{dt}(dc) = \Re\{\bar{Z}_{d1}\bar{I}_{d1}\bar{I}_{d1}^*\} - V_c\Re\{\bar{I}_{d0}\} - \frac{1}{2}\Re\{\bar{I}_0\bar{V}_0^*\} \quad (5\text{-}45)$$

$$\frac{dW_{C\Delta}}{dt}(dc) = \frac{1}{2}\Re\{\bar{Z}_{d1}\bar{I}_{d1}\bar{I}_0^*\} + \Re\{\bar{V}_0^*\bar{I}_{d1}\} \quad (5\text{-}46)$$

Starting from the second equation it's clear that the only way to control the differential energy is to control the first harmonic of the differential current (in amplitude and phase). In the equation of the total energy when the value of the first harmonic of the differential current is provided the only degree of freedom available for control purposes is the dc component of the differential current.

From this analysis it's clear that is possible to control only the dc value of the two energies and not the instantaneous value. In particular with a differential current that is composed only by zero and first harmonic (which are both necessary for the stability of the system) the two energies will be affected by oscillations of the same frequency of the fundamental frequency and oscillations at double frequency of the fundamental.

Of course it is possible to use other harmonics in the differential current apart from the zero and first component to erase some of the oscillating contributes and improve the overall performances of the control.

5.2.4 Alternative connection of the load

In practical applications when only a single MMC leg is involved often it's not convenient to implement the connection of the load discussed in previous section, due to the need of a DC voltage offset in the load. A more suitable connection could be the one shown in Figure 5-5 where, instead of connecting the load in parallel with the lower arm, it is connected between the central point of the two modules and the central point of the bus DC. In this paragraph the equations of this type of connection will be described.

Of course this type of connection is possible only if the central point of the bus DC is available. This type of configuration is implemented in the experimental setup so it's important to show the differences between the two configurations. This analysis is not important with two legs where the load is connected between the two central points of the phases or with three legs where the load is connected with the three central point of the three legs.

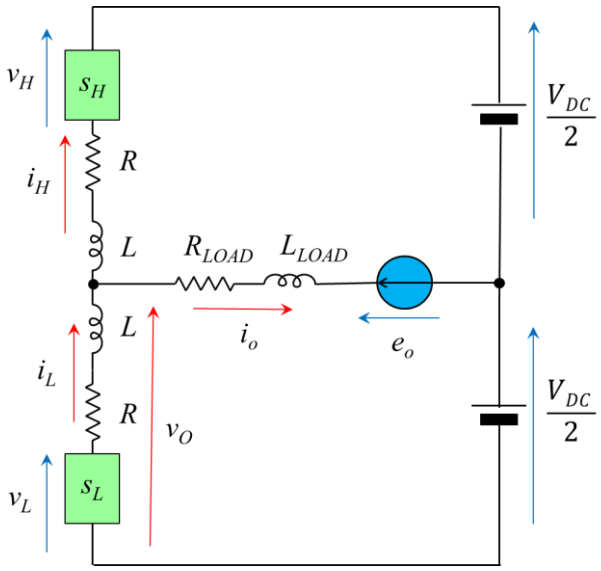


Figure 5-5 – Scheme of a single leg MMC with alternative connection of the load.

Applying Kirchhoff's voltage law on the external loop, on the lower loop and on the load loop it is possible to obtain:

$$V_c - v_H + Ri_H + L\frac{di_H}{dt} - v_0 = 0 \tag{5-47}$$

$$v_L - Ri_L - L\frac{di_L}{dt} - v_0 = 0 \tag{5-48}$$

$$v_0 - e_0 - R_{LOAD}i_0 - L_{LOAD}\frac{di_0}{dt} = 0 \tag{5-49}$$

By substituting equation (5-49) into (5-47) and (5-48) it's possible to find:

$$V_c - v_H + Ri_H + L\frac{di_H}{dt} - e_0 - \frac{V_c}{2} - R_{LOAD}i_0 - L_{LOAD}\frac{di_0}{dt} = 0 \tag{5-50}$$

$$v_L - Ri_L - L\frac{di_L}{dt} - e_0 - \frac{V_c}{2} - R_{LOAD}i_0 - L_{LOAD}\frac{di_0}{dt} = 0 \tag{5-51}$$

Separating v_H and v_L in the previous equations:

$$v_H = \frac{V_c}{2} + Ri_H + L\frac{di_H}{dt} - e_0 - R_{LOAD}i_0 - L_{LOAD}\frac{di_0}{dt} \tag{5-52}$$

$$v_L = \frac{V_c}{2} + Ri_L + L\frac{di_L}{dt} + e_0 + R_{LOAD}i_0 + L_{LOAD}\frac{di_0}{dt} \tag{5-53}$$

By adding and subtracting equations (5-52) and (5-53) and introducing the definitions of internal voltage, differential voltage, load current and differential current it is possible to find:

$$v_{\text{int}} = e_0 + R_{eq}i_0 + L_{eq}\frac{di_0}{dt} \tag{5-54}$$

$$v_d = \frac{V_c}{2} + Ri_d + L\frac{di_d}{dt} \tag{5-55}$$

In this case, changing the connection of the load, the second equation, with the differential voltage, remains the same, whereas in the first equation there is no more the contribute $V_C/2$. Apart from this, the two systems are totally equivalent and will be considered indifferently in the following.

5.2.5 Control of single leg MMC – Constrained approach

In general there are two variables that is possible to control in MMC inverters, the modulating signals of the upper and lower modules. A first simple control approach impose a constraint

between these two modulating signals. This way the control system should only calculate one control signal instead of two, because they are directly correlated.

In this section this type of control that can be named "constrained control" will be discussed and analyzed.

A single leg MMC will be taken into account, with one equivalent module for the upper arm, and one equivalent module for the lower arm, as usual. The output signals of the control system are two, the modulating signals of the upper and lower arms, and constitute the input of the PWM modulator. The outputs of the PWM modulator are the state functions, that are directly applied to the IGBTs of the inverter. As already discussed, if a constraint is imposed between the two modulating signals, even if the outputs of the control system are two, the control system have to calculate only one reference signal. It is possible to impose the constraint on the modulating signals, in this case it is valid every switching period, or directly on the switching functions.

The equation (5-20), (5-21) and (5-24), (5-25) of the MMC leg, discussed in this chapter, can be rewritten in terms of switching functions:

$$v_{CL}s_L - v_{CH}s_H + V_c - 2e_0 = 2R_{eq}i_0 + 2L_{eq}\frac{di_0}{dt} \tag{5-56}$$

$$v_{CL}s_L + v_{CH}s_H - V_c = 2Ri_d + 2L\frac{di_d}{dt} \tag{5-57}$$

$$\frac{dv_{CH}}{dt} = -\frac{1}{C}\left(i_d - \frac{i_0}{2}\right)s_H \tag{5-58}$$

$$\frac{dv_{CL}}{dt} = -\frac{1}{C}\left(i_d + \frac{i_0}{2}\right)s_L \tag{5-59}$$

The values assumed by the electrical quantities appearing in the equations, strongly depend on the values assumed by the switching functions.

During the design of the control strategy it is fundamental to correlate the behavior of the quantities that is necessary to control with the variables s_H and s_L.

The first equation expresses the correlation between the switching functions and the load current, while the second equation expresses the correlation between the switching functions and the differential current. The last two equations express the oscillations across the capacitors depending on the load current, the differential current and the switching functions.

Imposing the constraint between the switching functions it is possible to control only the load current, ignoring the differential current that is not controllable anymore. In fact, this way, it is possible to use the only control variable to obtain the desired load current.

For example, what can be done, is to impose a complementary behavior of the two equivalent upper and lower modules. This way each instant only one of the two modules is switched on while the other one is bypassed. The constraint that is necessary to impose to achieve this condition can be expressed as follows:

$$\begin{cases} s_H + s_L = 1 \\ s_H, s_L = [0;1] \\ s = s_H - s_L = \pm 1 \end{cases} \tag{5-60}$$

The variables s_H and s_L identify the state of the modules, while the variable s identifies the state of the leg. The absolute value of this variable is always equal to one and it's positive if the upper module is on and negative if the lower module is on.

The two switching functions s_H and s_L can be expressed as function of s as follows:

$$s_H = \frac{1+s}{2} \tag{5-61}$$

$$s_L = \frac{1-s}{2} \tag{5-62}$$

It is possible to substitute the variable s in place of the variables s_H and s_L reducing the input variables to one:

$$\frac{di_0}{dt} = \frac{1}{2L_{eq}}\left[V_c - v_{CH}\left(\frac{1+s}{2}\right) + v_{CL}\left(\frac{1-s}{2}\right) - 2R_{eq}i_0 - 2e_0\right] \tag{5-63}$$

$$\frac{di_d}{dt} = \frac{1}{2L}\left[-V_c + v_{CH}\left(\frac{1+s}{2}\right) + v_{CL}\left(\frac{1-s}{2}\right) - 2Ri_d\right] \tag{5-64}$$

$$\frac{dv_{CH}}{dt} = -\frac{1}{C}\left(i_d - \frac{i_0}{2}\right)\left(\frac{1+s}{2}\right) \tag{5-65}$$

$$\frac{dv_{CL}}{dt} = -\frac{1}{C}\left(i_d + \frac{i_0}{2}\right)\left(\frac{1-s}{2}\right) \tag{5-66}$$

It is possible to rewrite the first two equations highlighting the sum and the difference of the voltages on the capacitors as shown:

$$\frac{di_0}{dt} = \frac{1}{2L_{eq}}\left[V_c + \frac{v_{CL} - v_{CH}}{2} - s\frac{v_{CL} + v_{CH}}{2} - 2R_{eq}i_0 - 2e_0\right] \tag{5-67}$$

$$\frac{di_d}{dt} = \frac{1}{2L}\left[-V_c + \frac{v_{CH} + v_{CL}}{2} + s\frac{v_{CH} - v_{CL}}{2} - 2Ri_d\right] \tag{5-68}$$

It is useful, at this stage, to define two new variables starting from the capacitors voltages:

$$v_C^+ = \frac{v_{CH} + v_{CL}}{2} \tag{5-69}$$

$$v_C^- = \frac{v_{CL} - v_{CH}}{2} \tag{5-70}$$

The variable $v_C{}^+$ is correlated to the electrostatic energy stored in the modules, while the variable $v_C{}^-$ is correlated to the voltage unbalance between the two capacitors. The capacitors voltages can be expressed starting from the variables introduced with the following expressions:

$$v_{CH} = v_C^+ - v_C^- \tag{5-71}$$

$$v_{CL} = v_C^+ + v_C^- \tag{5-72}$$

The system is balanced if the capacitors of the upper and lower arms have the same voltages and consequently the same electrostatic energy is stored. This way $v_C{}^+$ is equal to the sum of the voltages of the two capacitors and $v_C{}^-$ is zero.

Substituting the new variables introduced into equations (5-67), (5-68) and (5-65), (5-66) leads to:

$$\frac{di_0}{dt} = \frac{1}{2L_{eq}}\left[V_c + v_C^- - sv_C^+ - 2R_{eq}i_0 - 2e_0\right] \tag{5-73}$$

$$\frac{di_d}{dt} = \frac{1}{2L}\left[-V_c + v_C^+ + sv_C^- - 2Ri_d\right] \tag{5-74}$$

$$\frac{dv_C^+}{dt} = -\frac{1}{2C}\left(i_d - \frac{si_0}{2}\right) \tag{5-75}$$

$$\frac{dv_C^-}{dt} = -\frac{1}{2C}\left(-si_d + \frac{i_0}{2}\right) \tag{5-76}$$

The third and the fourth equations are obtained considering that the voltages on the capacitors are continuous functions and the derivative is linear so the super position effect is valid.

The system of four equations written allows to calculate in each instant the voltages and the currents that characterize the inverter.

5.2.6 Simulation model of single leg MMC – Constrained approach

Starting on the analysis of the previuos section it is possible to syntetize a control alghoritm. First of all it is possible to realize a closed loop control system. This type of control is theoretically correct and it is possible to correctly simulate it. Unfurtantely, even a slight error in the measures of the capacitor voltages bring instability to the system, in fact the upper and the lower capacitors are not balanced and they are at a voltage level that is different from the required reference value. This is correlated to the fact that, with this type of control, it is not possible to control the differential current. In pratical applications measurement errors are not avoidable and so the close loop control is not achievable.

For this reason, a simple open loop control that allows to control the voltage applyed to the load was developed.

To this end it can be designed a control system that direclty imposes the desired modulating signal, avoiding any type of feedback.

The system realized in simulation with the software Matlab/Simulink is shown in Figure 5-6.

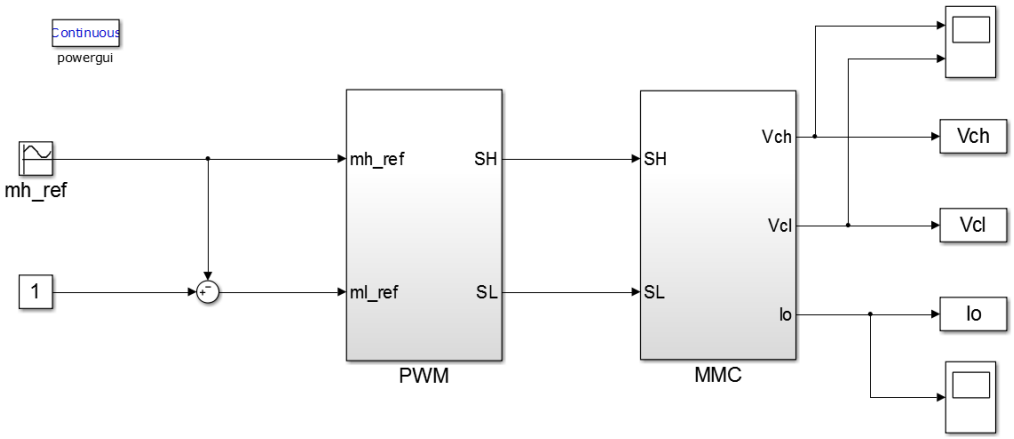


Figure 5-6 – Simulink general model of single leg MMC with open loop control.

In general the single leg MMC inverter can be simulated with a mathematical model, based on equations, directly with Simulink blocks, or by using the Sim Power System library.

Both the models were realized, the first approach, based on equations, is shown in Figure 5-7, while the second approach based on Sim Power System library is shown in Figure 5-8.

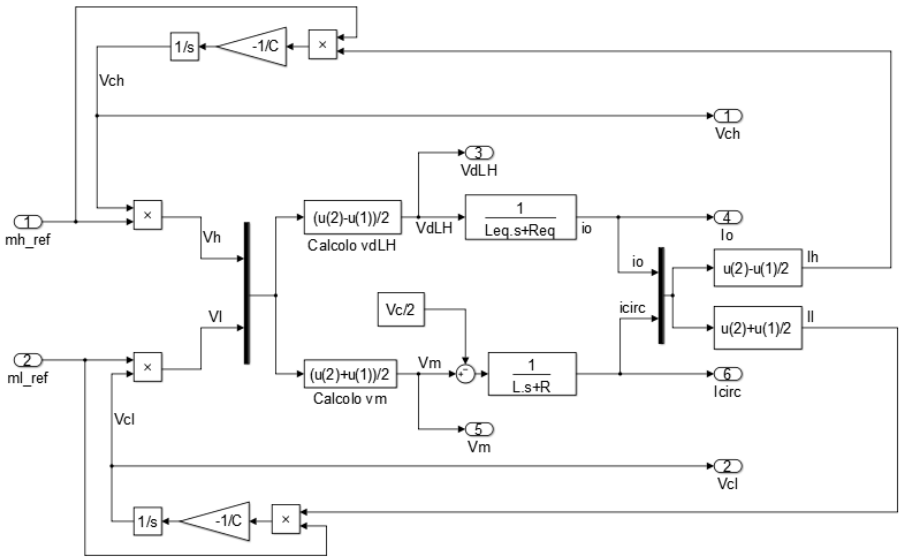


Figure 5-7 – Simulink equation based model of single leg MMC.

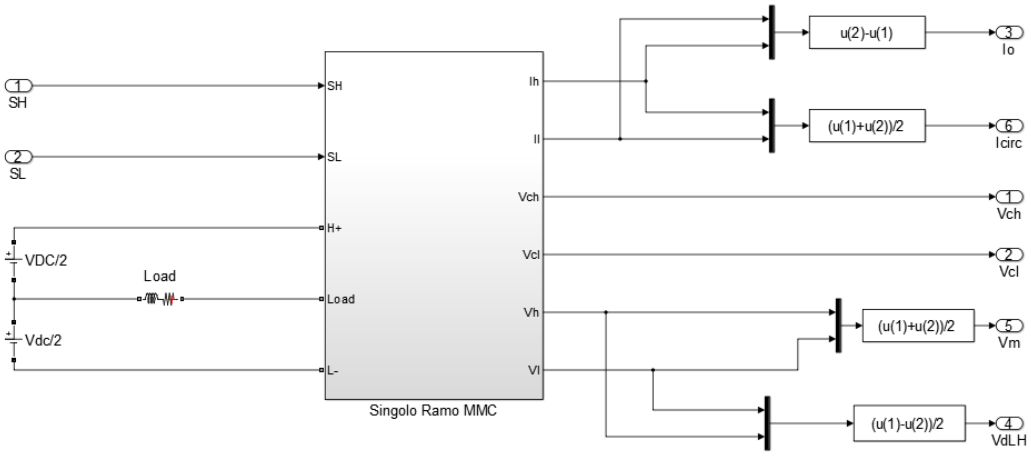


Figure 5-8 – Sim Power System model of single leg MMC, DC link and load.

Figure 5-9 shows the model of the single leg of the MMC realized with Sim Power System, while Figure 5-10 shows the model of the single module of the MMC.

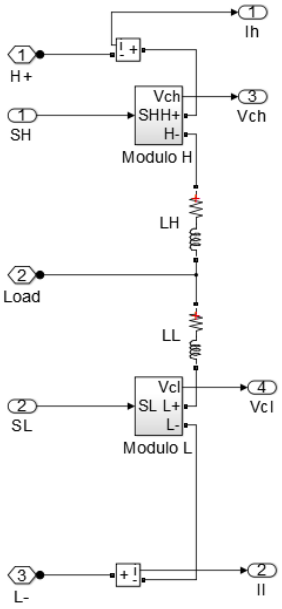


Figure 5-9 – Sim Power System model of single leg MMC.

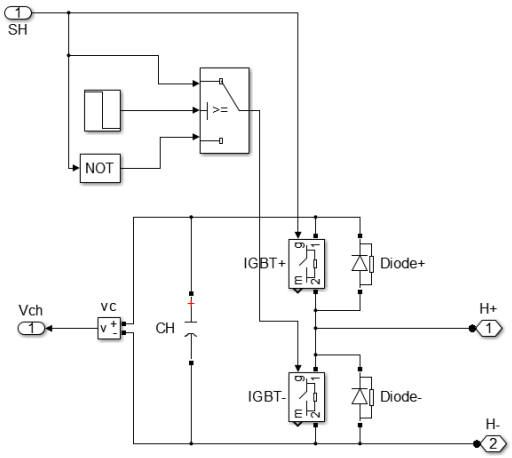


Figure 5-10 – Sim Power System model of single MMC module.

Both the models can be used for the analysis. In general the equation based model allows fast calculations and consequently fast simulations, and it is also possible, in first approximation, to avoid the PWM modulators, when the ripple caused by the modulation can be neglected.

The models of PWM modulators are shown in Figure 5-11. It is necessary to saturate the modulating signals between *0* and *1* to avoid overmodulation.

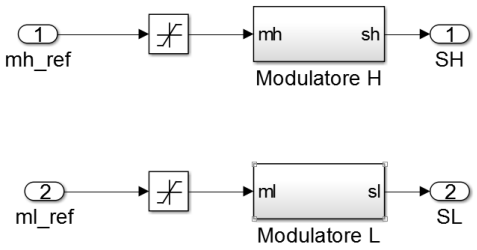


Figure 5-11 – PWM modulators.

The simulation parameters are listed in table Table 5-1.

DC voltage	24 [V]
Capacitors	880 [μF]
Arm inductance	1.18 [mH]
Arm resistance	0.4 [Ω]
Load inductance	0.5 [mH]
Load resistance	1 [Ω]
Frequency	50 [Hz]

Table 5-1 – Simulation parameters.

As it is possible to notice, there is only one input to the system which is the modulating signal required. What is imposed is the complementarity of the two modulating signals and not the complementary of the switching functions.

5.2.7 Simulation results of single leg MMC – Constrained approach

Imposing a modulating signal m_H of amplitude *0.2* and frequency *50 Hz*, with the average value of *0.5* it is possible to obtain the load current shown in Figure 5-12. The modulating signal m_L is correlated to m_H in such a way that their sum is equal *1* in each instant.

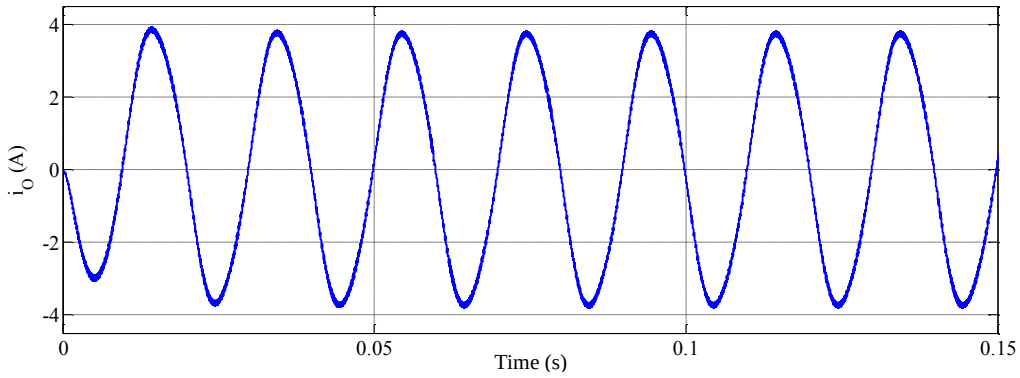


Figure 5-12 – Load current with low amplitude modulating signal.

It is possible to notice that load current is affected by distortion, due to the fact that the sinusoidal modulating signals are not applied to constant voltages, but to the oscillating voltages of the capacitors. In a closed loop control the voltage oscillations are taken into account for the calculation of the reference currents to obtain the correct input signals. In the open loop control instead, there is no such possibility to operate on modulating signals to compensate the oscillations.

The voltages on the capacitors are shown in Figure 5-13 and in Figure 5-14.

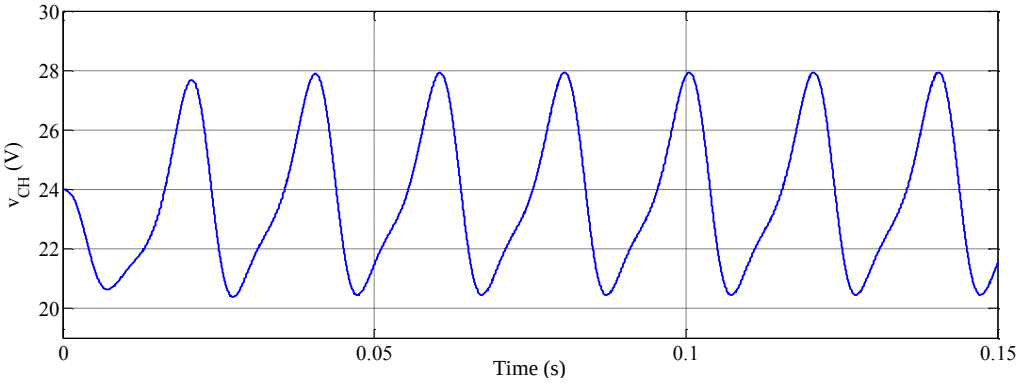


Figure 5-13 – Upper capacitor voltage with low amplitude modulating signal.

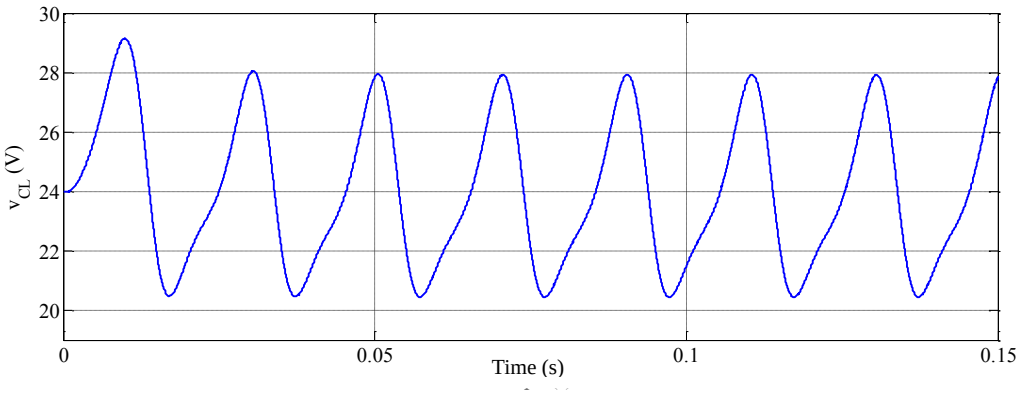


Figure 5-14 – Lower capacitor voltage with low amplitude modulating signal.

The voltages of both the capacitors have an average value of 24 V, and oscillate with an amplitude of 2 V and 50 Hz frequency.

If the amplitude of the reference modulating signal is 0.4 the distortion of the load current increases. In fact the increase of the modulating signals amplitude causes the increase of the load current and consequently the increase of the voltage ripple on the capacitors.

Applying sinusoidal modulating signals to even more distorted voltages origins an even more distorted output quantity. Load current and capacitor voltages obtained with an amplitude of 0.4 of m_H are represented in Figure 5-15, Figure 5-16 and Figure 5-17.

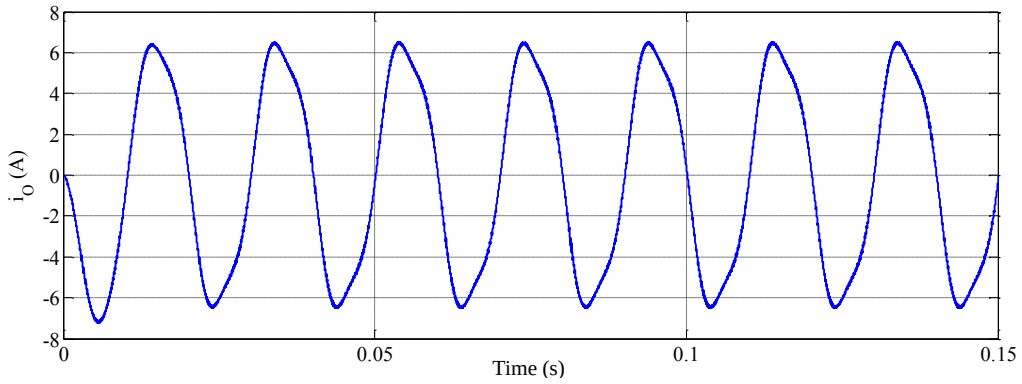


Figure 5-15 – Load current with double amplitude modulating signal.

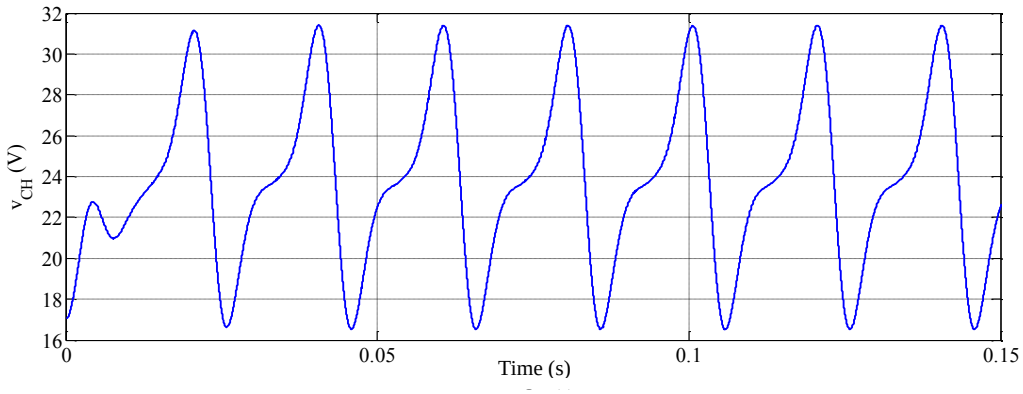


Figure 5-16 – Upper capacitor voltage with double amplitude modulating signal.

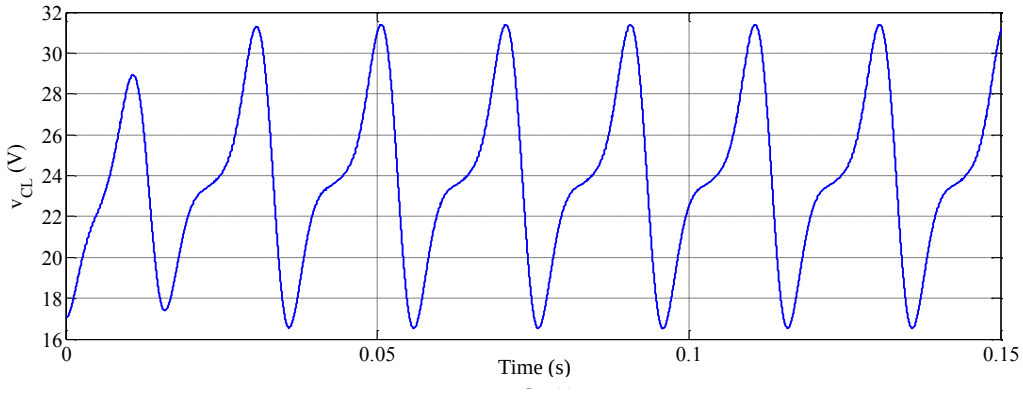


Figure 5-17 – Lower capacitor voltage with double amplitude modulating signal.

This time the voltages of both the capacitors oscillates across the average value of 24 V with an amplitude of about 4 V and 50 Hz frequency.

To compensate the oscillations of the voltages across the capacitors it is necessary to increase as much as possible the value of the capacitors.

5.2.8 Experimental setup of single leg MMC

An experimental setup to test all the control strategies developed on a single leg MMC was realized at LEMAD laboratory. From now on all the experimental results in this chapter are related to this setup.

The parameters of the setup are generally the same used in simulation and are listed in Table 5-2.

The DC voltage is realized with two batteries connected in series.

The measurement probes allow to read voltages and currents with the oscilloscope, the scales of the probes used for measurement purposes are:

- Current probe: 1 A → 100 mV
- Voltage probe: 20 V → 1 V

DC voltage	24 [V]
Capacitors	880 [μF]
Arm inductance	1.18 [mH]
Arm resistance	0.4 [Ω]
Load inductance	0.5 [mH]
Load resistance	1 [Ω]
Frequency	50 [Hz]

Table 5-2 – Experimental setup parameters.

Figure 5-18 shows a general view of the experimental setup.

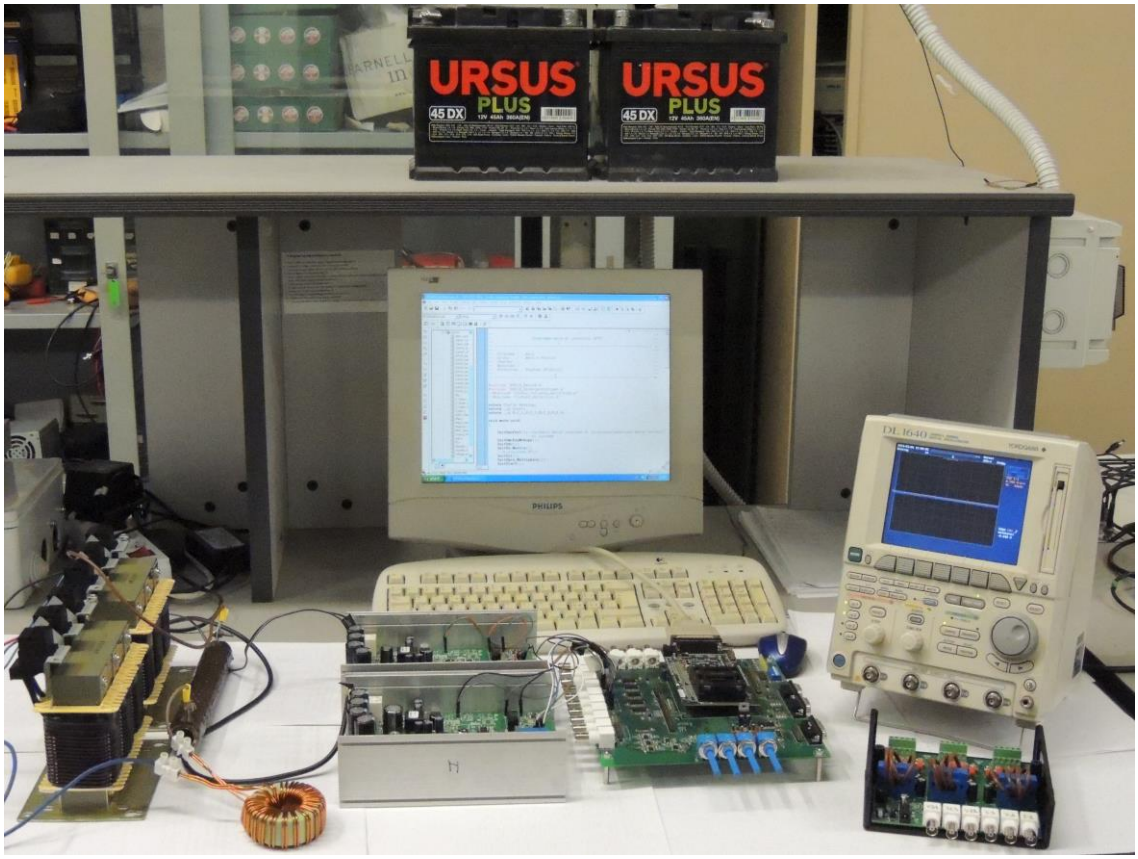


Figure 5-18 – General view of the experimental setup.

The single module of the MMC was designed with the software Altium Designer. The 3-D view of the designed module is shown in Figure 5-19.

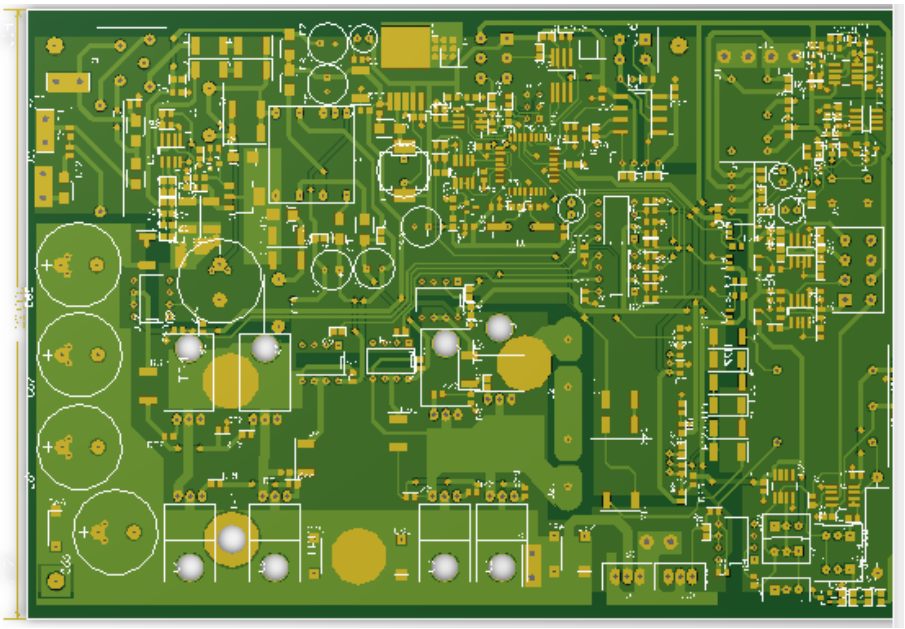


Figure 5-19 – 3-D view of the single MMC module.

One of the MMC realized module is shown in Figure 5-20 with the heatsink and the main signal connections.

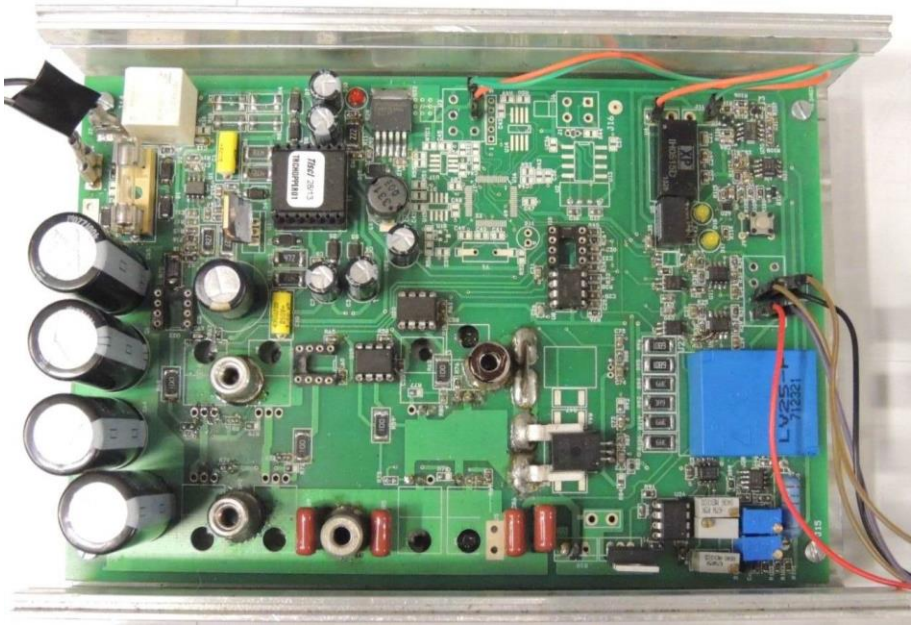


Figure 5-20 – Single MMC module.

Finally, Figure 5-21 shows the leg composed by the two hardware modules and the DSP used to control the system that is a Texas Instrument TMS320F2812.

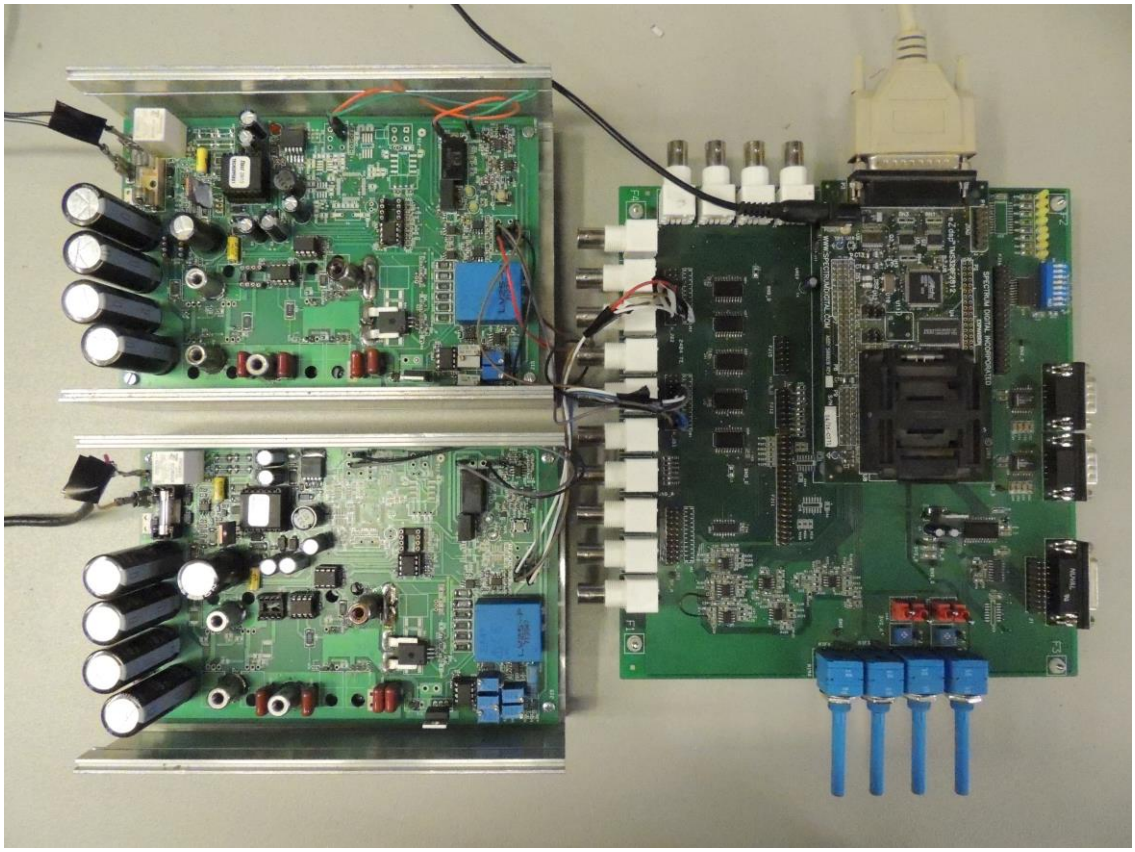


Figure 5-21 – Single MMC leg with DSP controller.

5.2.9 Experimental results of single leg MMC – Constrained approach

For the reasons explained in the last section it is not possible to implement a close loop control when the two modulating signals are constrained. For this reason in the experimental setup was not possible to realize a stable close loop control due to the unavoidable measurement errors of voltages and currents.
The experimental results obtained with the open loop control are reported in this section.

By requesting two oscillating modulating signals with an amplitude of about 0.15 and 50 Hz frequency, and average value of 0.5, the load current obtained is shown in Figure 5-22.
The period of the showed quantities is 20 ms, due to the requested frequency of 50 Hz. The modulating signals are measured by two signals sent by the DSP to the oscilloscope. The current amplitude is 2 A and the distortion is due to the presence of other harmonics as seen.

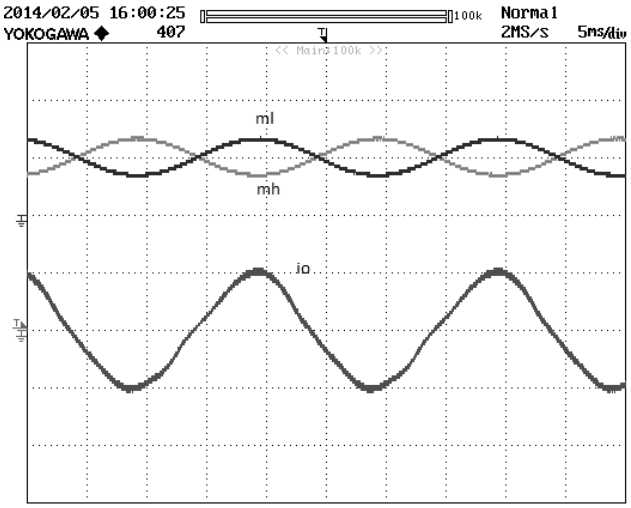


Figure 5-22 – Reference modulating signals (0.5 /div) and load current (2 A/div) with open loop control - (5 ms/div).

The measured currents in the upper and lower arms are shown in Figure 5-23.

The difference between i_L e i_H is equal to the load current, while the current i_H with the opposite sign corresponds to the input current of DC link.

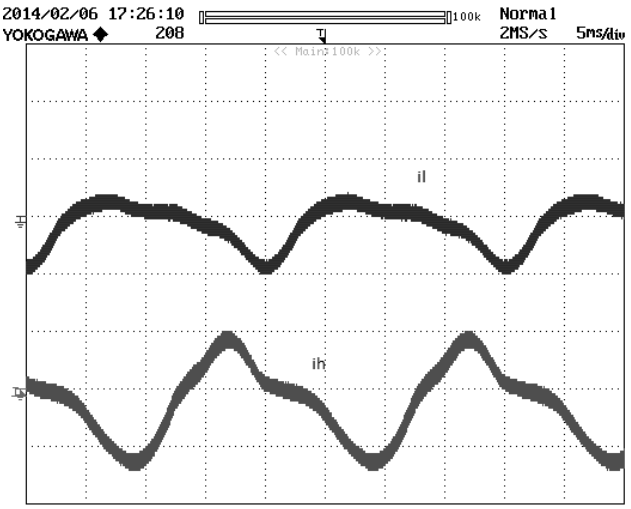


Figure 5-23 – Upper and lower arm currents (2 A/div) with open loop control - (5 ms/div).

Figure 5-24 shows the capacitors voltages, the load current and the input DC link current. The modulating signals are imposed such a way that the load current has still an amplitude of 2 A and frequency 50 Hz.

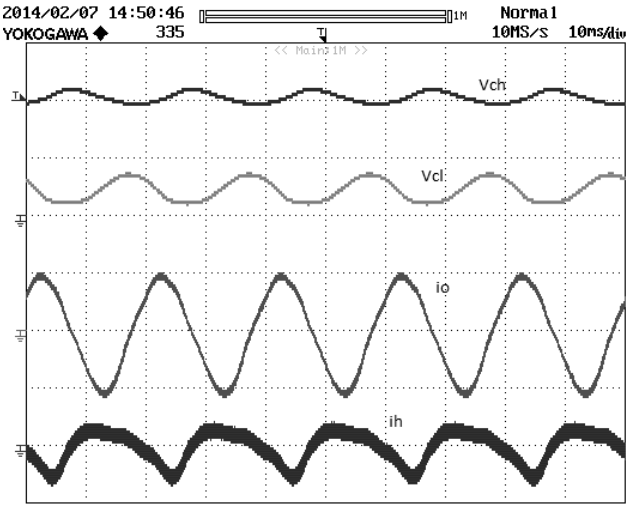


Figure 5-24 – Capacitor voltages (10 V/div) of the upper and lower modules with open loop control – (10 ms/div).

v_{CH} oscillates across 21 V, while v_{CL} oscillates across 24 V. Oscillations have a major amplitude for v_{CL}.

The oscillations of the capacitor voltages decrease if the amplitude of the load current decreases.

By reducing the amplitude of the modulating signal such a way that the amplitude of the load current is reduced from 2 A to 0.5 A it is possible to obtain a strong reduction of voltage fluctuations, as shown in Figure 5-25.

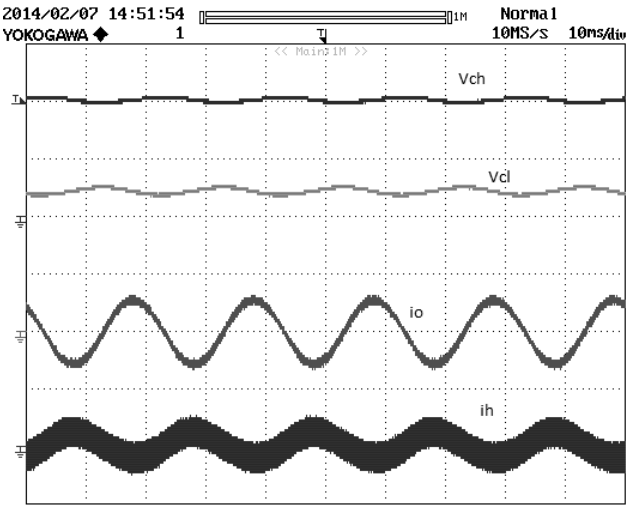


Figure 5-25 – Capacitor voltages (10 V/div) of the upper and lower modules with open loop control with reduced load current (1 A/div) – (10 ms/div).

It can be noted that the current is less distorted, due to the decrease of the voltage oscillations across the capacitors.

Figure 5-26 and in Figure 5-27 show the waveforms to evaluate the distortion of the load current if the frequency varies, with equal amplitude.

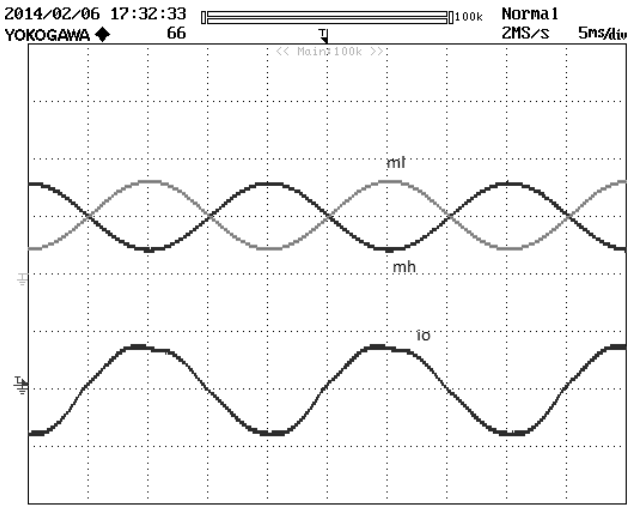


Figure 5-26 – Load current (5 A/div) with frequency 50 Hz – (5 ms/div).

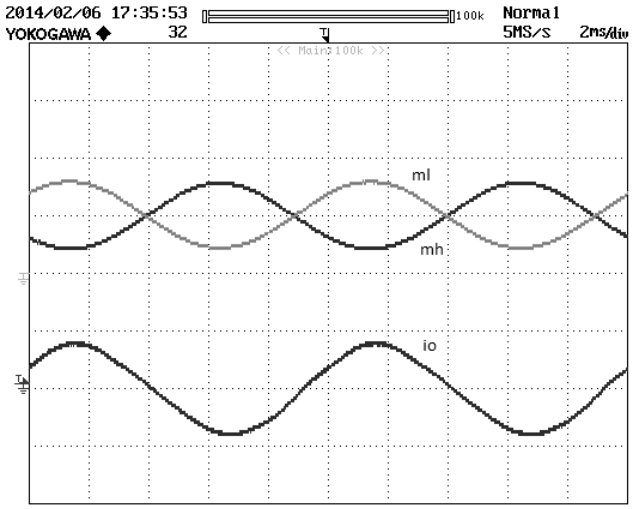


Figure 5-27 – Load current (5 A/div) with frequency 100 Hz – (2 ms/div).

In particular, the modulating signal amplitude is set such a way to obtain an amplitude of the load current of 4 A and a measure at 50 Hz is compared with a measure at 100 Hz. It is clear that the distortion decreases as the frequency increases. The factors that cause this reduction are the increase

of the filtering effect of inductive reactance on the current and the increase of the filtering effect of capacitive reactance on the voltage.

5.2.10 Control of single leg MMC – Unconstrained approach

In practical applications the control system has two goals. The first one is to ensure that the load current i_0 follows a sinusoidal reference signal $i_{0,ref}$. In particular if the inverter is connected to the grid, the output voltage v_0 is sinusoidal too. The second task of the control system is to keep the capacitor voltages v_{CH} and v_{CL} in the upper and lower arms almost constant and below a suitable safety threshold. How to achieve these three goals is not trivial, since, as already discussed, the control system can rely only on two control variables, i.e., the modulation indexes m_H and m_L. The control system can control the currents i_0 and i_{diff} by choosing suitable values of the voltages v_{int} and v_{diff}. While the reference signal for i_0 is given, the one for i_{diff} must be chosen. The next section shows how it is possible to manage the current i_{diff} to control the total energy of the capacitors and the unbalance between the energy stored in the upper and lower capacitors.

5.2.10.1 Total energy and differential energy

The total energy is equal to the sum of the energies stored in the upper and lower capacitors, while differential energy is equal to the difference of the energy stored into the upper and lower capacitors. If during the operation the derivatives of these energies are equal to zero than these energies are constant. The value of the total energy should be equal to the reference value of the total energy stored into the capacitors, while the differential energy must be zero.
The equations of total and differential energy of the capacitors are useful to implement a closed loop control system.
First of all it is necessary to integrate equations (5-28) and (5-29) over a period of the load current:

$$\Delta W_{CT} = -\int_0^T 2v_d i_d dt - \int_0^T v_{\text{int}} i_0 dt \tag{5-77}$$

$$\Delta W_{C\Delta} = \int_0^T v_d i_0 dt + \int_0^T 2v_{\text{int}} i_d dt \tag{5-78}$$

In general the product of two sinusoids with the same frequency, and a certain phase shift, results into a continuous contribute and a sinusoidal contribute with a frequency that is the double of the frequency of the multiplied sinusoids, that depends from the phase shift.

The integral of the product of two sinusoids, with the same frequency and a phase shift, over a period results into a non-zero value depending from the amplitudes of the sinusoids and from their displacement.
In particular this value is equal to half of the product of the amplitudes multiplied for the cosine of the displacement angle. Usually for electrical quantities rms values are considered.
It is imposed a sinusoidal waveform for the load current i_O and the internal voltage v_{int} is sinusoidal too.
The second integral of the total energy has a certain value that depends from the internal voltage and the load current. The first integral has two contributes, the differential current is constituted by at least a continuous contribute and a sinusoidal contribute with the same frequency of the load current. Since it's not possible to use the second term to control the total energy, in fact the load current is already decided by the load, it is possible to use the first term to achieve this task.
The first term in the differential energy equation depends from the load current and the differential voltage, and is dependent from the load, the second integral instead has a value that depends on the internal voltage and the differential current. The sinusoidal contribute of the differential current with the same frequency of the internal voltage multiplied by the internal voltage gives a continuous contribute that can control the differential energy, while the continuous contribute of the differential current has no effects if integrated over a period.
In synthesis what is done with this control strategy is to use the continuous component of the differential current to control the total energy while the sinusoidal component is used to control the differential energy.

Thanks to these considerations it is possible to design a control scheme that has the task to follow the average value of the total energy and to keep equal to zero the average value of the differential energy.
It is possible to synthetize the control technique developed using the following representation:

$$v_{INT} \rightarrow i_0 \tag{5-79}$$

$$v_d \rightarrow i_d \rightarrow \begin{pmatrix} W_T \\ W_\Delta \end{pmatrix} \tag{5-80}$$

Basically, the internal voltage is related and controls the load current, while the differential voltage controls the differential current. This current, if is realized with a continuous and a sinusoidal component, can control the total and differential energy of the capacitors of the leg.

5.2.10.2 Control scheme

In Figure 5-28 the two internal control loops of the load current and the differential current are shown. In particular the two systems are characterized by a low pass filter. The control system pre-compensates the other terms and uses a PI controller to track the current error between the reference signal and the measured signal. In this case resonant PI controllers are used due to the necessity to follow sinusoidal reference values. It should be noted that there is at least another pole at high frequency that represents the inverter commutation and is not shown in figure.

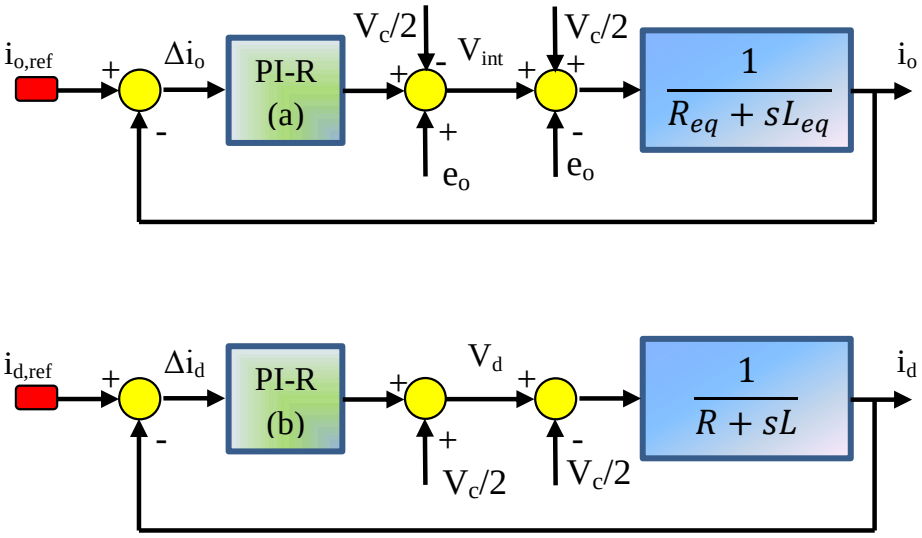


Figure 5-28 – Current control scheme in the unconstrained approach.

The tuning of PI controllers can be done with a pole-zero cancellation and by imposing a phase margin of about 75 degree to achieve the better dynamic performances and avoid overshoot in the response.

With these considerations the two control loops can be simplified to low pass filters as shown in Figure 5-29, where ω_C is the cutoff frequency of the closed loop systems.

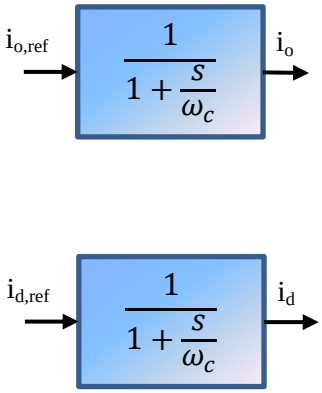


Figure 5-29 – Reduced current control schemes in the unconstrained approach.

Figure 5-30 shows the control scheme of the total energy and differential energy loops. In the total energy loop there is a low pass filter to reduce disturbances effects at high frequency. The zero of the PI controller is put one decade before the critical frequency of the differential current loop.

In the differential energy loop the signal is multiplied by a sinusoidal signal that has the same frequency and phase of the internal voltage. Since there is already an integrator in the transfer function a simple P controller was implemented.

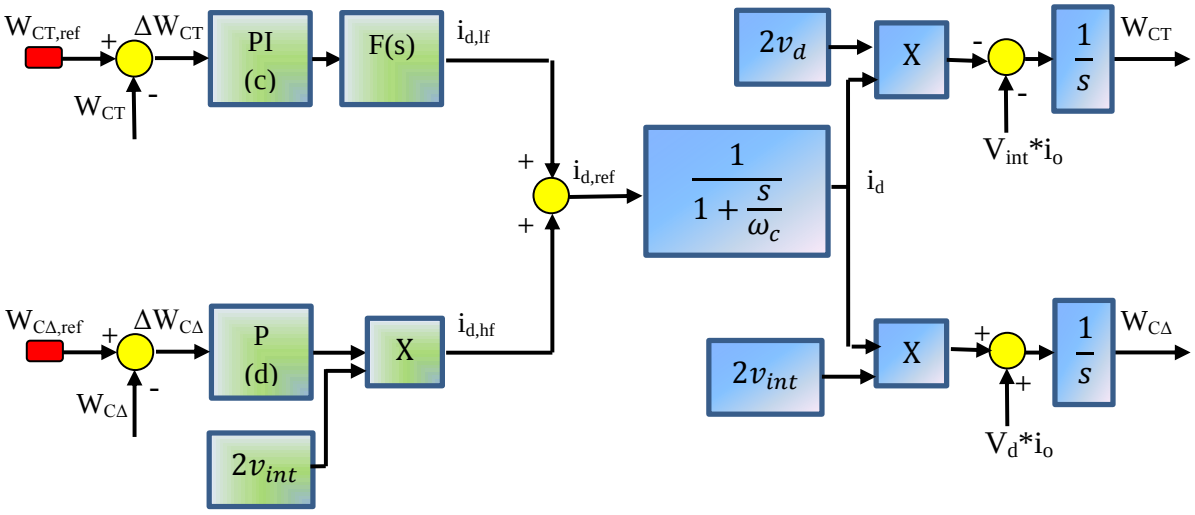


Figure 5-30 – Energy control schemes in the unconstrained approach.

5.2.11 Simulation model of single leg MMC – Unconstrained approach

Figure 5-31 shows a model of the control system with the unconstrained approach, based on the considerations made and the equations written in the previous sections. The model is realized in

Matlab/Simulink and the details of the control schemes are shown in Figure 5-32 (total and differential energy loops) and in Figure 5-33 (load and differential current loops).

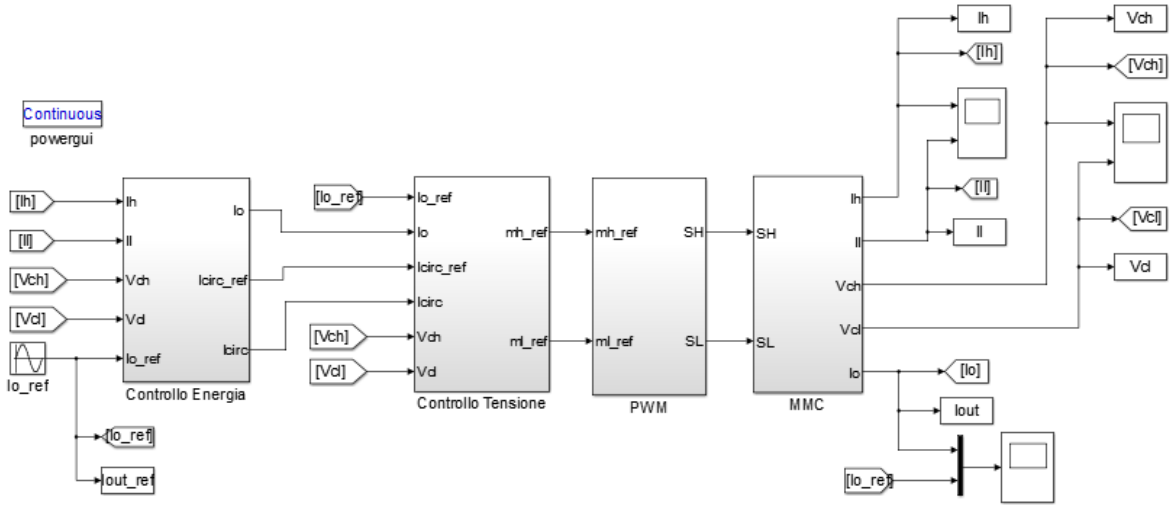


Figure 5-31 – Simulink general model of single leg MMC with unconstrained control.

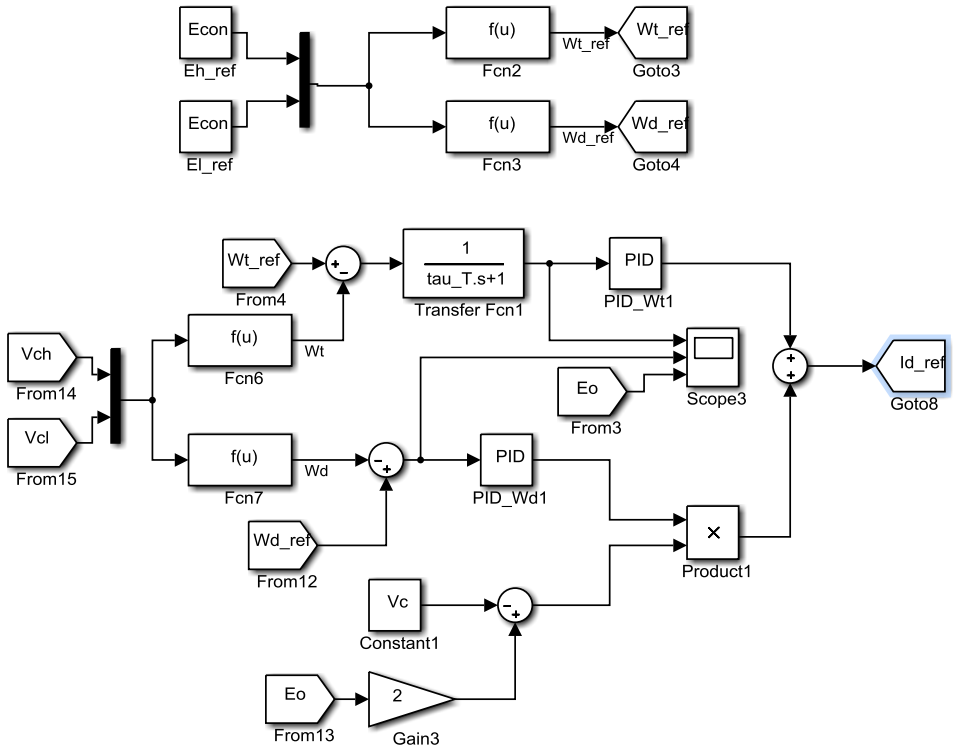


Figure 5-32 – Control system energy loop of single leg MMC.

The upper part of the energy control loop imposes the references for total and differential energies whereas the lower part calculates the reference signal of the differential current based on the energy errors.

The control voltage is based on the errors of the load current and the differential current, calculated by the difference between the reference signals and the measured currents. When the internal and differential voltages are determined, the upper and lower voltage reference signals are calculated and according to the voltages measured across the capacitors, the modulating signals are sent to the PWM modulators. The models of the PWM modulators and of the single leg MMC are the same of the previous control.

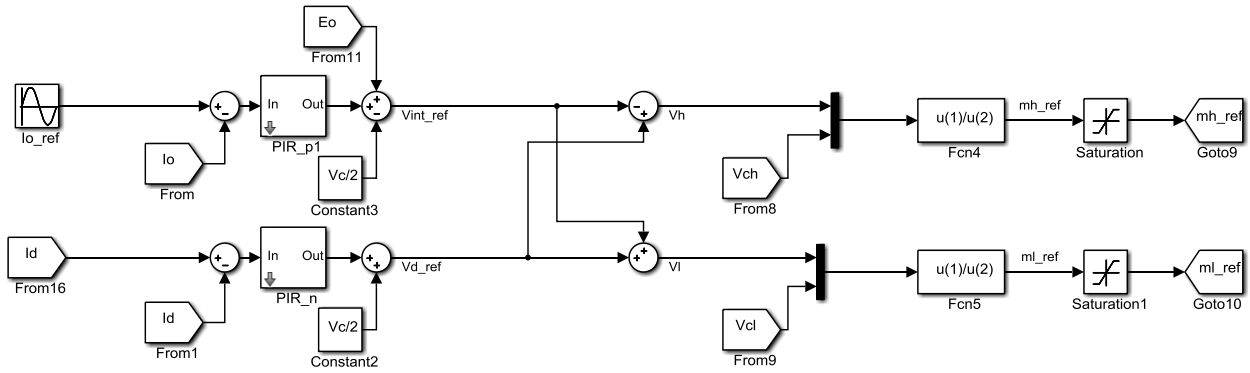


Figure 5-33 – Control system current loop of single leg MMC.

The simulation parameters are shown in Table 5-3.

DC voltage	24 [V]
Capacitors	880 [μF]
Capacitors reference voltage	24 [V]
Arm inductance	1.18 [mH]
Arm resistance	0.4 [Ω]
Load inductance	0.5 [mH]
Load resistance	1 [Ω]
Load current	2 [A]
Frequency	50 [Hz]

Table 5-3 – Simulation parameters.

5.2.12 Simulation results of single leg MMC – Unconstrained approach

At first, no measurement errors are considered in the simulation.

In Figure 5-34 it can be observed that the load current is at the correct reference value and that the dynamic performances are adequate. In Figure 5-35 and in Figure 5-36 it can be observed that the voltages of the capacitors oscillate around the average reference value of 24 V with an amplitude of the oscillations of 2 V, after an initial transient of about 300 ms.

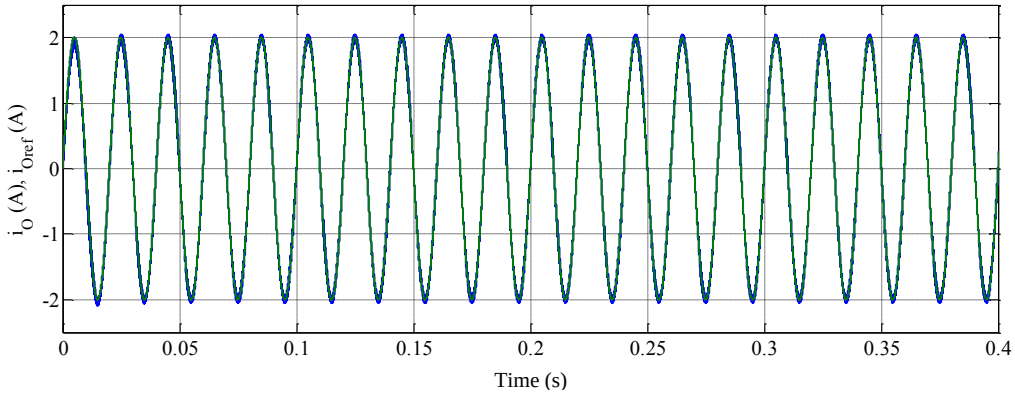


Figure 5-34 – Load current.

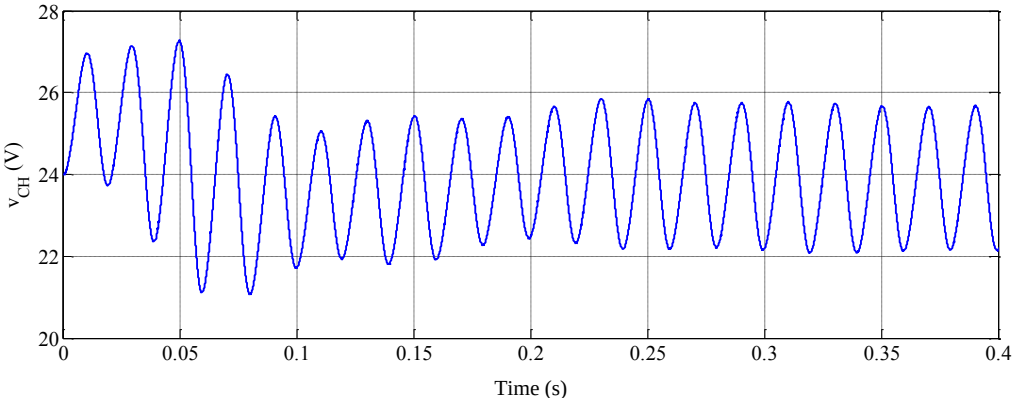


Figure 5-35 – Upper capacitor voltage.

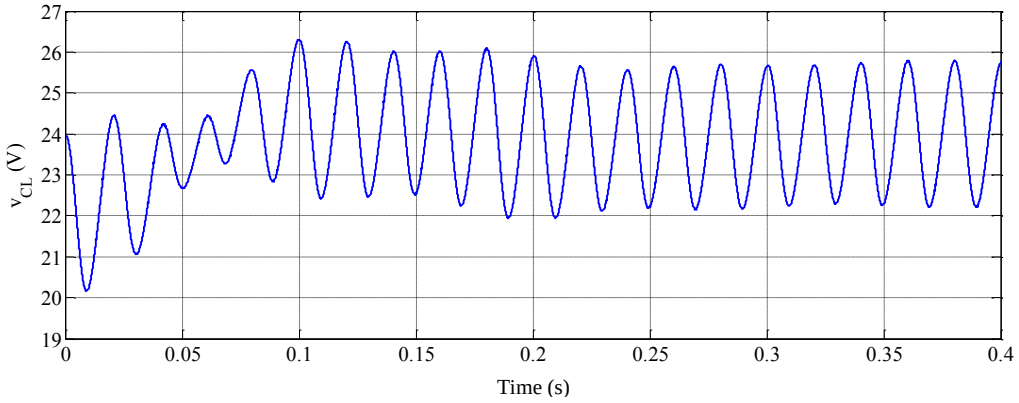


Figure 5-36 – Lower capacitor voltage.

In Figure 5-37 the modulating signals corresponding to the required operating condition, are shown. It can be observed that they oscillate around the average value of 0.5, and have opposite phases.

The circulating current follows its reference signal, as shown in Figure 5-38. Its average value is approximately - 0.2 A.

The reference signals of total energy and differential energy are followed in a satisfactory way, as shown in Figure 5-39 and Figure 5-40.

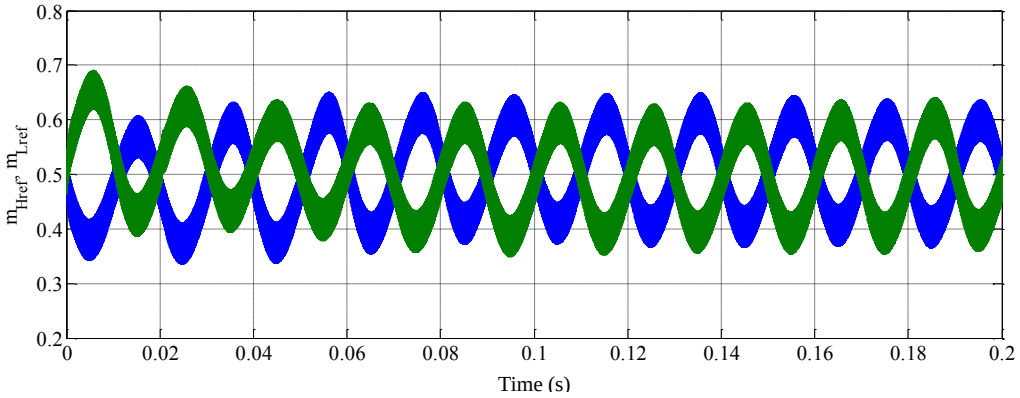


Figure 5-37 – Modulating signals of the upper and lower module.

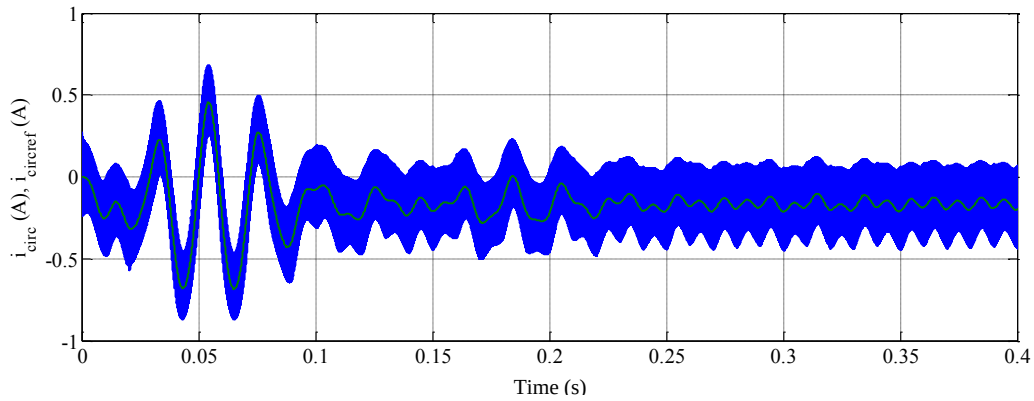


Figure 5-38 – Differential current.

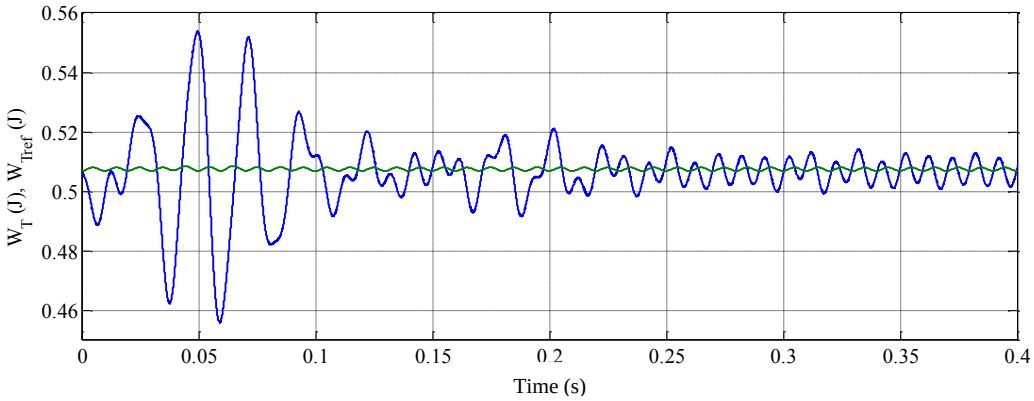


Figure 5-39 – Total energy.

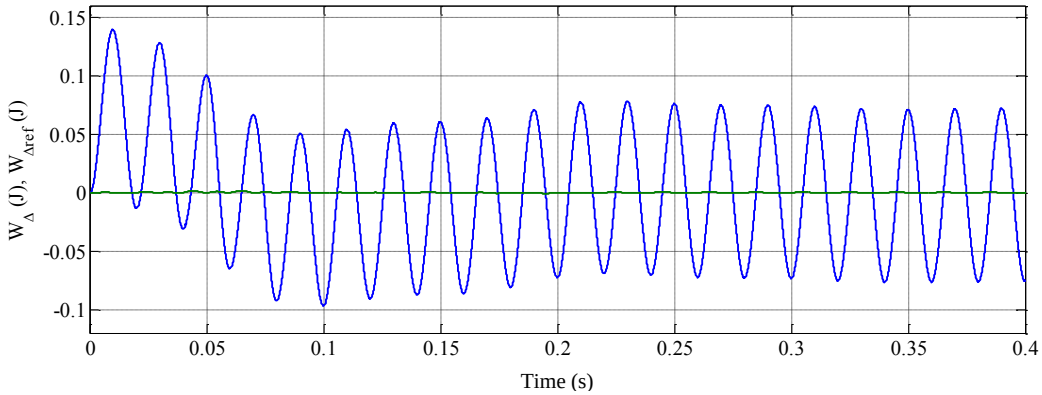


Figure 5-40 – Differential energy.

In the following a simulation with the same parameters as previous case but in presence of measurement errors will be showed, to investigate the robustness of the control system.

In particular, an error of 0.5 A is considered on the current i_L and an error of 3 V is considered on voltage V_{CH} .

In Figure 5-41 it can be observed that the load current follows the reference and is slightly shifted downwards, due to the fact that the system measures in the feedback a current higher than the actual value.

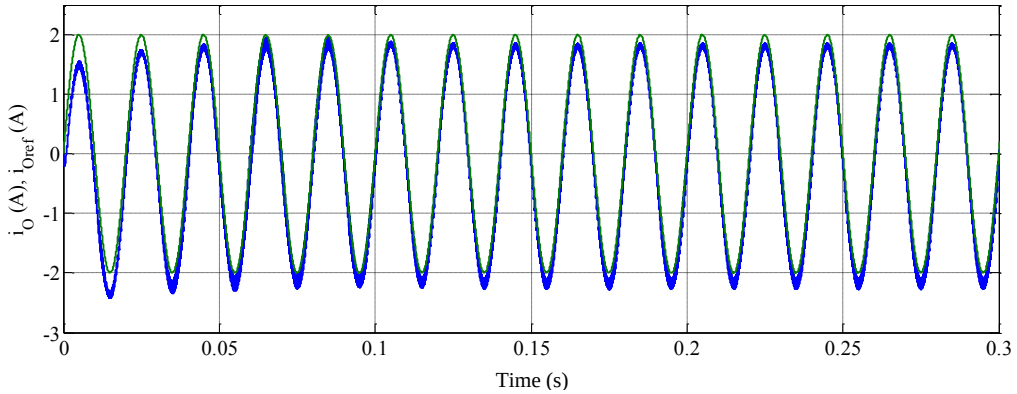


Figure 5-41 – Load current with measurement errors.

In Figure 5-42 and in Figure 5-43 it is possible to see that the capacitor voltages are not balanced at the beginning, but after a transient of about 2 seconds the voltages are stabilized. In particular, V_{CH} oscillates around 21 V, with an amplitude of the oscillations of 0.5 V, while V_{CL} oscillates around 24 V, with an amplitude of the oscillations of 3 V. The fact that V_{CH} oscillates around a value that is lower than 24 V is coherent with the fact that the system feedback measures a voltage higher than the actual value.

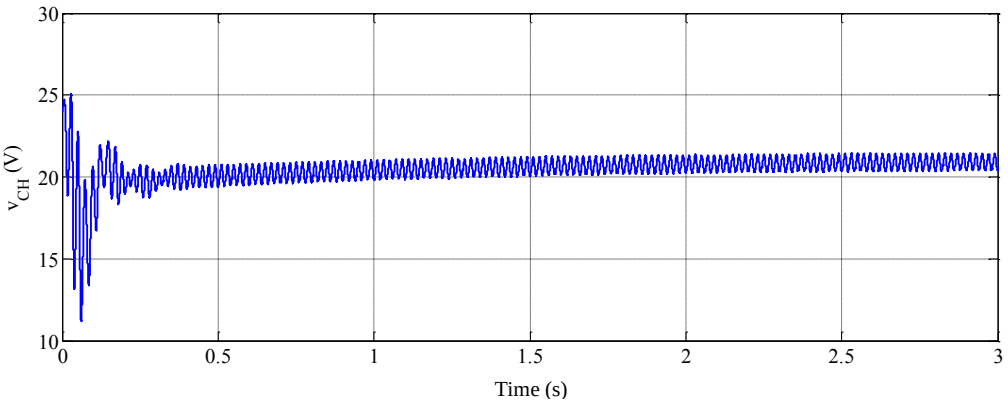


Figure 5-42 – Upper capacitor voltage with measurement errors.

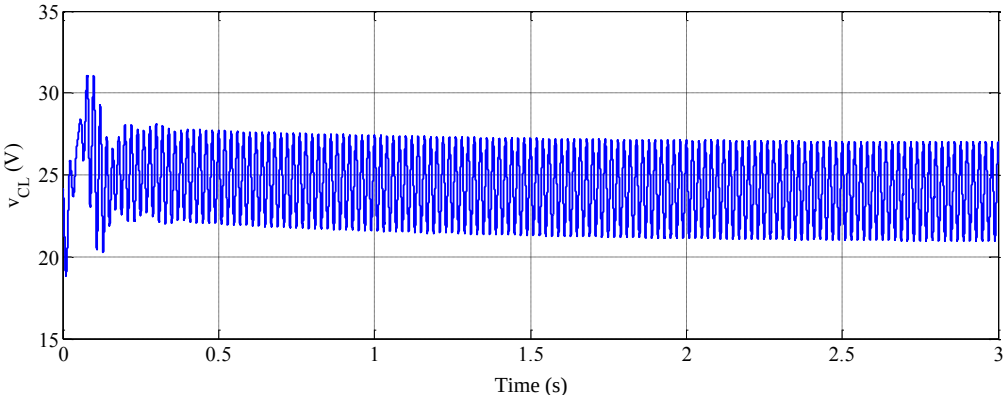


Figure 5-43 – Lower capacitor voltage with measurement errors.

The currents of the upper and lower arms assume different amplitudes and are shown in Figure 5-44 and in Figure 5-45. In particular, the amplitude of the current of the lower branch is higher than the amplitude of the current in the upper branch.

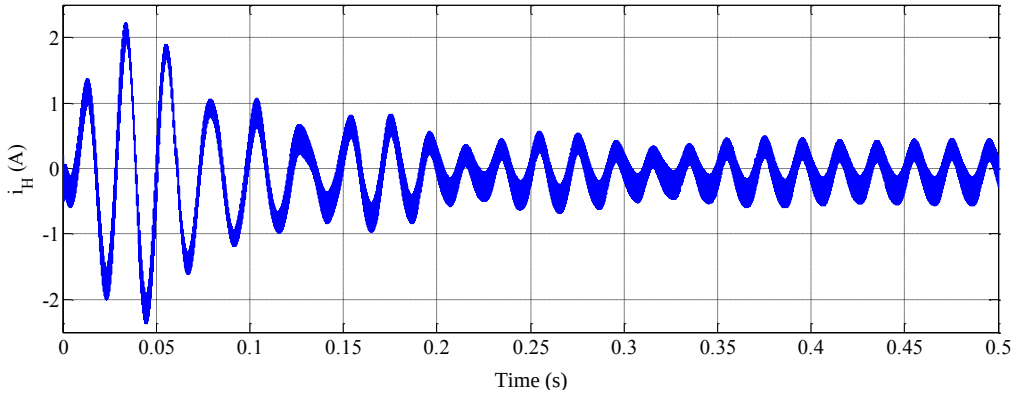


Figure 5-44 – Upper arm current with measurement errors.

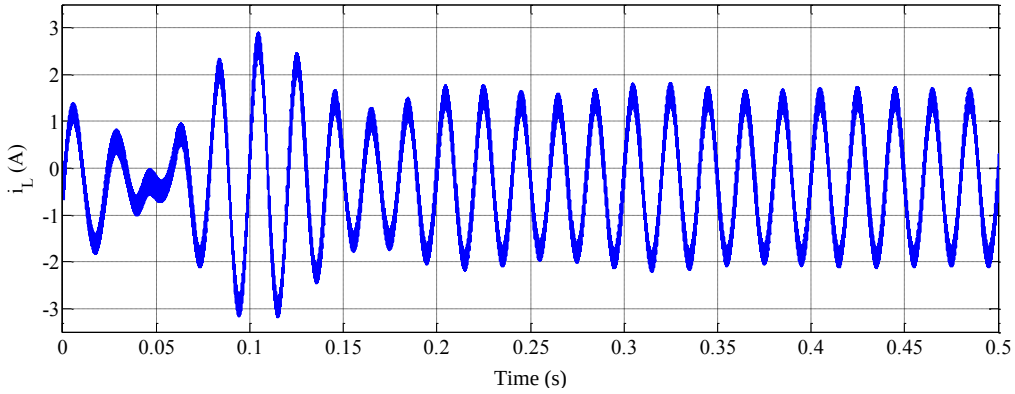


Figure 5-45 – Lower arm current with measurement errors.

The modulating signals in this simulation still present a phase opposition and have a different mean value in steady state conditions as shown in Figure 5-46.

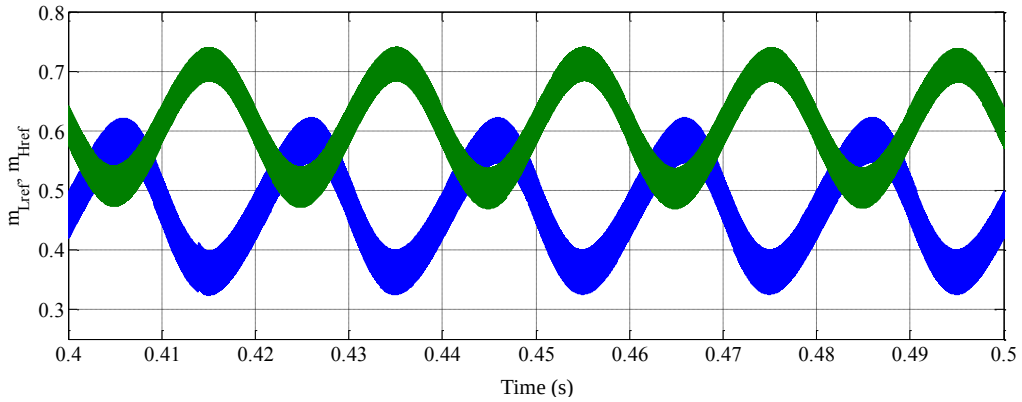


Figure 5-46 – Modulating signals with measurement errors.

5.2.13 Experimental results of single leg MMC – Unconstrained approach

The unconstrained approach is robust in presence of measurement errors of voltages and currents, due to its control of total and differential energy, and this allows operation in closed loop. It is required a sinusoidal reference signal for the load current, of amplitude 2 A and frequency 50 Hz. In Figure 5-47 it is possible to compare the reference load current with the real load current and it is possible to see the currents in the upper and in the lower arm.

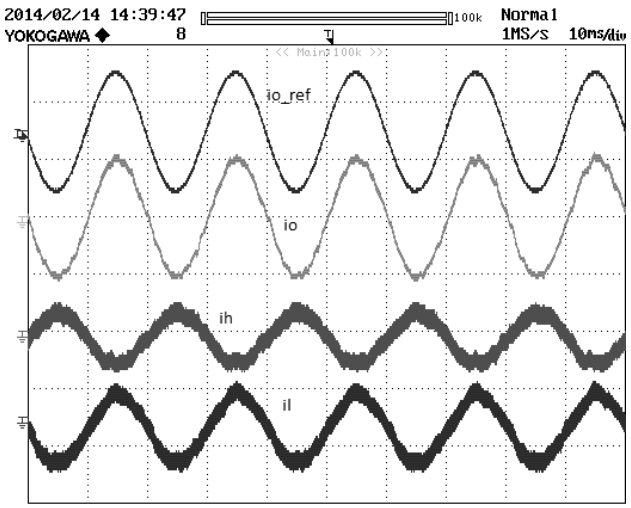


Figure 5-47 – Load current (2 A/div) and arm currents (2 A/div) - (10 ms/div).

The displayed quantities have a frequency of 50 Hz and the load current has an amplitude of 2 A, like the reference signal.

In Figure 5-48 the reference load current, the measured load current, and the currents in the two branches in transient conditions are displayed.

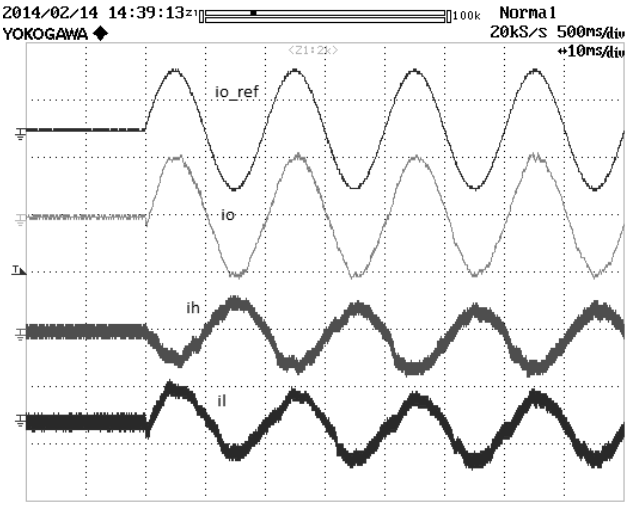


Figure 5-48 – Transient of load current (2 A/div) and arm currents (2 A/div) - (10 ms/div).

The time and amplitudes scales are the same. It can be observed that the load current follows correctly its reference and has good dynamic performances in fact it follows the reference from the first moment.

In Figure 5-49 it is possible to compare the reference current and the real load current. In addition the capacitor voltages of the two modules are shown. The configuration is the same. The voltages across the capacitors oscillate around 24 V with an amplitude of about 2 V and frequency of 50 Hz.

In Figure 5-50 the transients of the reference current, the measured load current, in addition to the voltages across the capacitors of the two branches, are displayed. The offset between the reference voltages is zero, then the oscillations of the capacitor voltages are shown together. It may be noted that the transient of the capacitor voltages has a duration of about 60 ms.

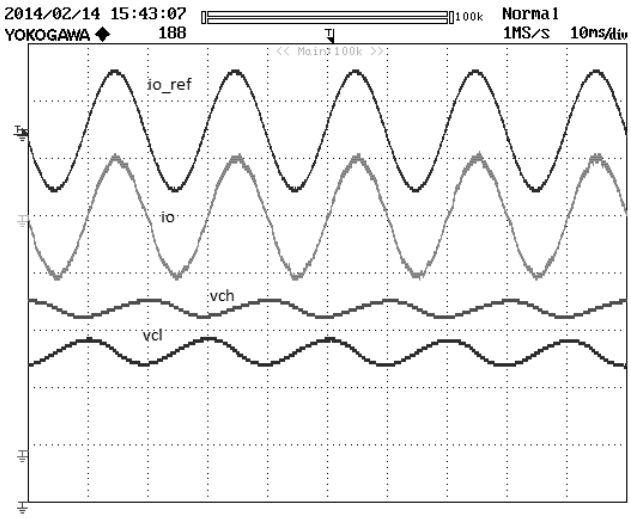


Figure 5-49 – Load current (2 A/div) and capacitor voltages (10 V/div) – (10 ms/div).

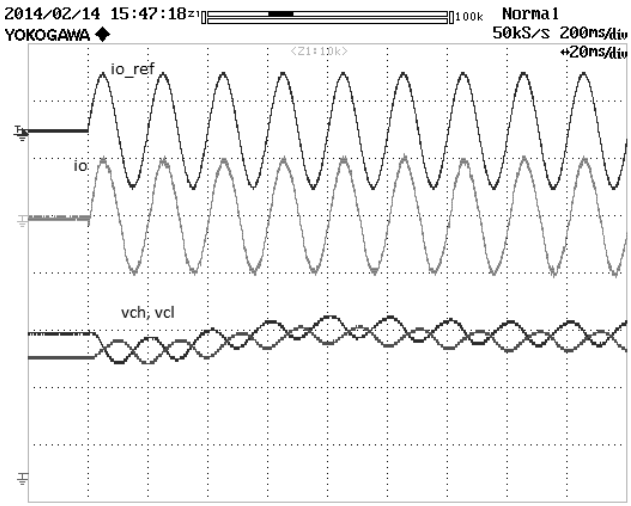


Figure 5-50 – Transient of load current (2 A/div) and capacitor voltages (10 V/div) – (20 ms/div).

In Figure 5-51 the reference and measured load current, the total energy and the differential energy are represented. The total energy has a value slightly exceeding 0.5 J and is practically constant, while the differential energy oscillates with an amplitude of about 0.1 J around zero.

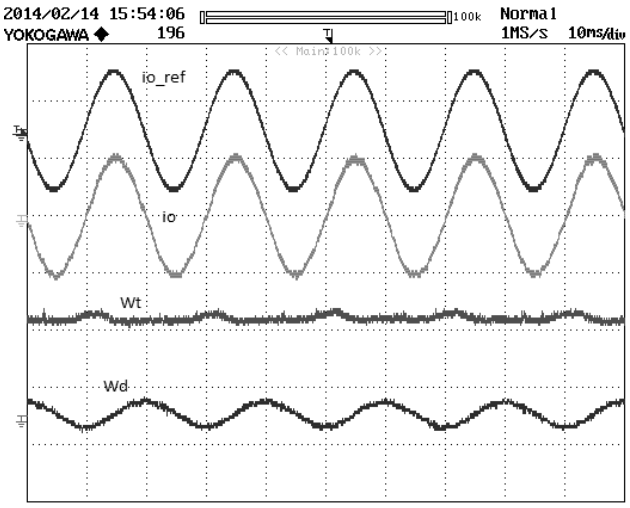


Figure 5-51 – Load current (2 A/div), total and differential energies (0.5 J/div) - (10 ms/div).

In Figure 5-52 the transient of the reference and real load current, in addition to the transient of total energy and differential energy, are shown.

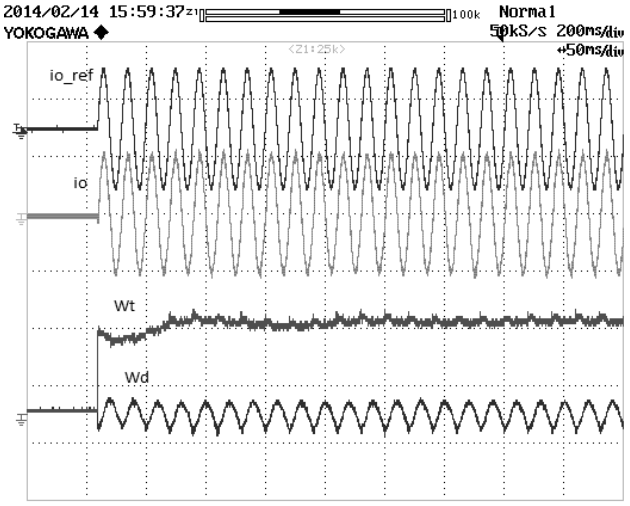


Figure 5-52 – Transient of load current (2 A/div), total and differential energies (0.5 J/div) - (50 ms/div).

Since the system is the same, the transient still has the same duration of 60 ms.

In Figure 5-53 the reference and real load currents are compared with the modulating signals of the upper and lower arms.

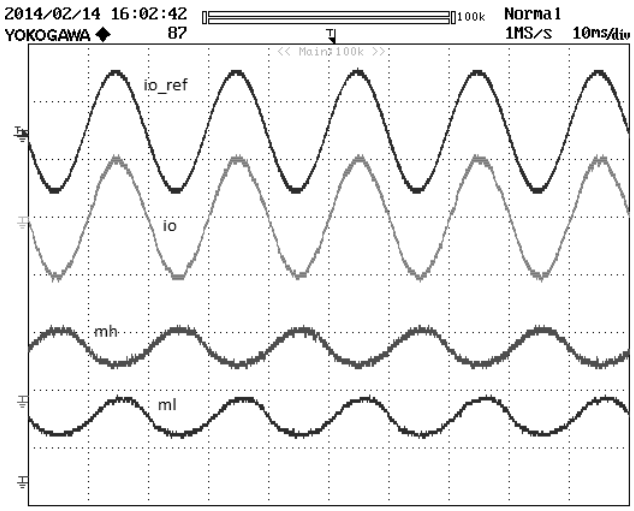


Figure 5-53 – Load current (2 A/div) and modulating signals (0.5 /div) – (10 ms/div).

The modulating signals are sent from the DSP to the oscilloscope, they oscillate around the average value of 0.5 with an amplitude of 0.15 and a frequency of 50 Hz. Their shape is not sinusoidal, in fact to achieve a sinusoidal waveform for the load current it is needed to consider the voltage oscillations across the capacitors to calculate the modulating signals. In Figure 5-54 the capacitor voltages of the two modules, the total energy and the differential energy are shown, in the steady state operation. It can be noted that the oscillation of V_{CL} around the mean value is slightly wider than the oscillation of V_{CH}.

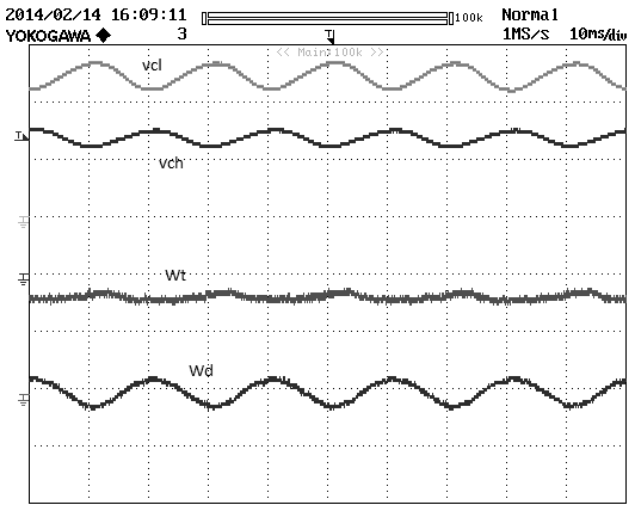


Figure 5-54 – Upper and lower capacitor voltages (10 V/div), total and differential energies (0.5 V/div) - (10 ms/div).

Figure 5-55 represents the transient of the capacitor voltages of the two modules and the total and differential energy. The duration is 60 ms.

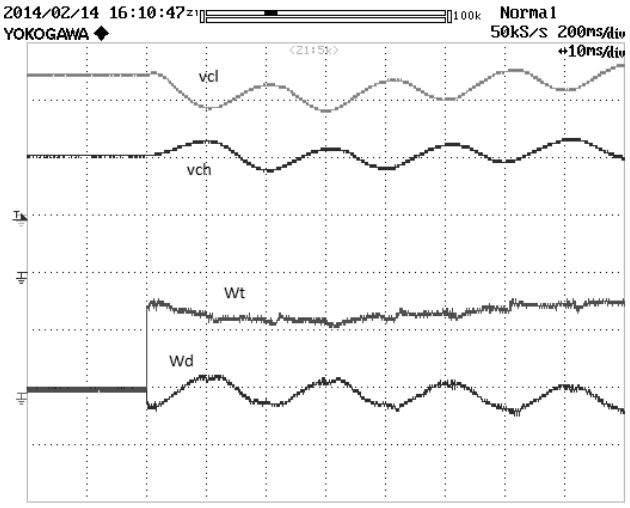


Figure 5-55 – Transient of upper and lower capacitor voltages (10 V/div), total and differential energies (0.5 V/div) - (10 ms/div).

In Figure 5-56 the differential current is represented, in addition to the load current, the total energy and the differential energy. The waveform is acquired with the DSP, the measure is subject to errors due to low resolution. Taking into account the amplification factor, the average value of the differential current is - 0.2 A, which is the same value obtained in simulation.

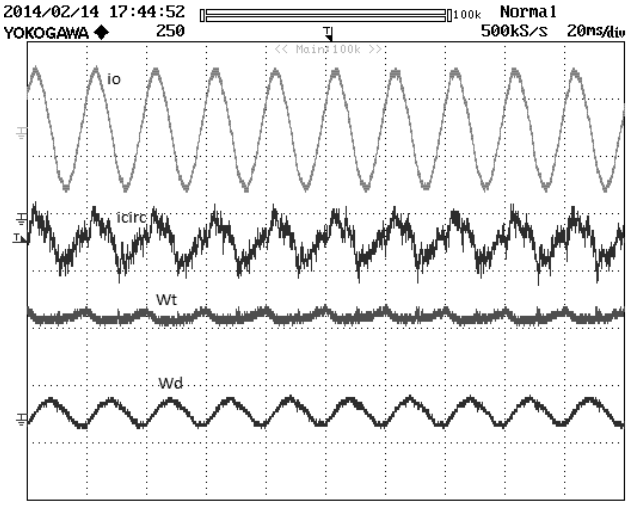


Figure 5-56 – Load and differential currents (5 A/div), total and differential energies (0.5 V/div) – (20 ms/div).

5.2.14 Control of single leg MMC – Orthogonal functions and two-time scale analysis approach

In this section a novel theoretical approach for the control of MMC is described.
As already seen, it is well-known that the capacitor voltages show unavoidable oscillations around their average value. These oscillations are caused by the intrinsic structure of the inverter, which leads to non-linear equations with periodic inputs. The so called "multiple-scale analysis" can be used to find an approximate model of the MMC in which the periodic oscillations of the capacitor voltages are deleted from the average trend. This is done by introducing two different time variables, i.e. a fast-scale time variable and a slow-scale time variable, which are treated as if they are independent.
The second part of the analysis shows that this approximate model can be very useful to synthesize a reference signal for the circulating current. This signal can be written as a linear combination of fast time-scale orthogonal functions with slow time-scale coefficients (it is useful to recall that, by definition, two functions are orthogonal if their inner product is zero). As a consequence, each term of the resulting signal can affect only a group of capacitors, but not the others, thus naturally leading to the decoupling of the control variables.

5.2.14.1 Two Time-Scale Analysis

It is possible to rewrite equations (5-26) and (5-27) as:

$$\frac{dW_{CH}}{dt} = v_H \frac{i_0}{2} - v_H i_d \tag{5-81}$$

$$\frac{dW_{CL}}{dt} = -v_L \frac{i_0}{2} - v_L i_d \tag{5-82}$$

Initially, let focus only on the energy of the upper arm, W_{CH}. Since v_0 and i_0 are sinusoidal signals with angular frequency ω, (5-81) shows that W_{CH} cannot be constant. It is necessarily affected by oscillations at frequency multiple of ω (the product between v_H and i_0 produces power harmonics at angular frequency ω and 2ω).
According to the method of multiple scale analysis, it is possible to assume that W_{CH} is the combination of a slow-varying part and a fast-varying part. An equivalent formulation of this concept is that W_{CH} is a function of two state variables, θ and τ, having different time scales.

Let us suppose that the frequency band of the slow-varying part of W_{CH} is [0, ω_c], where $\omega_c << \omega$. Then, θ and τ can be defined as follows:

$$\theta = \omega t = \frac{\omega_C}{\varepsilon} t \tag{5-83}$$

$$\tau = \omega_C t \tag{5-84}$$

where ε is the ratio between ω_c and ω ($\varepsilon << 1$).

Equations (5-83) and (5-84) state that the variation rate of θ is $1/\varepsilon$ times that of τ. Hence, θ is a fast-scale variable compared to τ, which is a slow-scale variable. In conclusion, the energy W_{CH} can be written as follows:

$$W_{CH} = W_{CH}(\theta, \tau, \varepsilon) \tag{5-85}$$

Finally, W_{CH} is assumed to be a periodic function with respect to θ:

$$W_{CH}(\theta + 2\pi, \tau, \varepsilon) = W_{CH}(\theta, \tau, \varepsilon) \tag{5-86}$$

Figure 5-57 graphically shows the meaning of the variables θ and τ.

Substituting (5-85) in (5-81) and multiplying both sides by ε leads to the following partial differential equation:

$$\frac{\partial W_{CH}}{\partial \theta} \omega_C + \frac{\partial W_{CH}}{\partial \tau} \varepsilon \omega_C = \varepsilon (v_H \frac{i_0}{2} - v_H i_d) \tag{5-87}$$

When ε tends to zero, W_{CH} can be expanded into a power series with respect to ε:

$$W_{CH} = W_{CH0}(\theta, \tau) + W_{CH1}(\theta, \tau)\varepsilon \tag{5-88}$$

where W_{CH0} is the slow-varying term of the energy (the period of the fast oscillations is negligible in comparison to the period of the slow changes), and W_{CH1} is the energy contribution due to the interaction between the oscillation modes. Substituting (5-88) in (5-87), collecting the powers of ε with the same degree, and equating to zero the resulting coefficients (second-degree terms are neglected) gives the following set of decoupled equations:

$$\frac{\partial W_{CH0}}{\partial \theta} = 0 \tag{5-89}$$

$$\frac{\partial W_{CH0}}{\partial \tau} \omega_C + \frac{\partial W_{CH1}}{\partial \theta} \omega_C = v_H \frac{i_0}{2} - v_H i_d \tag{5-90}$$

Equation (5-89) means that W_{CH0} is not a function of θ. Consequently, integrating both sides of (5-90) with respect to θ over the interval [0, 2π], recalling that W_{CH1} is periodic due to (5-86), and using (5-84), it is possible to come to the following result:

$$\frac{\partial W_{CH0}}{\partial t} = \frac{1}{2\pi}\int_0^{2\pi} v_H \frac{i_0}{2} d\theta - \frac{1}{2\pi}\int_0^{2\pi} v_H i_d d\theta \tag{5-91}$$

The methodology used to find (5-91) can be applied to W_{CL}, thus obtaining:

$$\frac{\partial W_{CL0}}{\partial t} = -\frac{1}{2\pi}\int_0^{2\pi} v_L \frac{i_0}{2} d\theta - \frac{1}{2\pi}\int_0^{2\pi} v_L i_d d\theta \tag{5-92}$$

The meaning of (5-91) and (5-92) becomes clearer when the change of variable (5-83) is used to express the integral terms:

$$\frac{\partial W_{CH0}}{\partial t} = \frac{1}{T}\int_0^{T} v_H \frac{i_0}{2} dt - \frac{1}{T}\int_0^{T} v_H i_d dt \tag{5-93}$$

$$\frac{\partial W_{CL0}}{\partial t} = -\frac{1}{T}\int_0^{T} v_L \frac{i_0}{2} dt - \frac{1}{T}\int_0^{T} v_L i_d dt \tag{5-94}$$

where T is $2\pi/\omega$.

Equations (5-93) and (5-94) show that the derivatives of the slow-varying energy components depend on the average value of the powers exchanged by the SMs over a period T.

Equations (5-93) and (5-94) can be used instead of (5-81)-(5-82) for the synthesis of a stable control system.

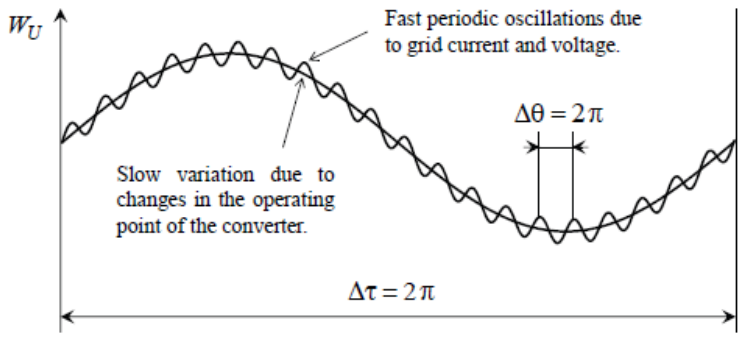


Figure 5-57 – Meaning of the fast and slow scale variables θ and τ.

5.2.14.2 Orthogonal Functions

Two functions *f* and *g* are called orthogonal if their inner product is zero. The definition of inner product is not unique. The average operator:

$$< f, g >= \frac{1}{2\pi}\int_0^{2\pi} f(\theta)g(\theta)d\theta \tag{5-95}$$

that appears in (5-91) and (5-92) is a well-defined inner product for real periodic functions in the interval [0, 2π]. Consequently, (5-91) and (5-92) can be rewritten in terms of the inner product (5-95):

$$\frac{\partial W_{CH0}}{\partial t} =< v_H, \frac{i_0}{2} > - < v_H, i_d > \tag{5-96}$$

$$\frac{\partial W_{CL0}}{\partial t} = - < v_L, \frac{i_0}{2} > - < v_L, i_d > \tag{5-97}$$

In the right-hand side of (5-96)-(5-97) only the terms depending on i_d can be used to control the average capacitor energies. However, the solution of this control problem is not simple, because i_d appears simultaneously in both equations. To decouple (5-96) and (5-97), it is useful to express i_d as a linear combination of two functions w_1 and w_2,

$$i_d = \lambda_1(\tau)w_1(\theta,\tau) + \lambda_2(\tau)w_2(\theta,\tau) \tag{5-98}$$

where the coefficients λ_1 and λ_2 are functions of the slow-scale time variable τ and are measured in [Ω^{-1}], while w_1 and w_2 are measured in [V]. If v_H is called v_1 and v_L is called v_2 the functions w_1 and w_2 are chosen so that they are mutually orthogonal to v_1 and v_2, according to the following rule:

$$< v_h, w_k >= \begin{cases} V_C^2 \ if \ h = k \\ 0 \ \ if \ h \neq k \end{cases} \quad h,k = 1,2 \tag{5-99}$$

Substituting (5-98) in (5-96)-(5-97) and considering (5-99) gives the following decoupled equations for the energy of the upper and lower arms:

$$\frac{\partial W_{CH0}}{\partial t} =< v_H, \frac{i_0}{2} > -\lambda_1 V_C^2 \tag{5-100}$$

$$\frac{\partial W_{CL0}}{\partial t} = - < v_L, \frac{i_0}{2} > -\lambda_2 V_C^2 \tag{5-101}$$

The set of functions w_1 and w_2 is said to be reciprocal to the set of functions v_1 and v_2, while the variables λ_1 and λ_1 are referred to as covariant components of i_d.

To determine explicitly w_1 and w_2, it is sufficient to assume that each of them can be expressed as a combination of v_1 and v_2, as follows:

$$w_k = \mu_{k,1} v_1 + \mu_{k,2} v_2 \tag{5-102}$$

where the coefficients $\mu_{k,h}$ (h=1,2) are usually known as contravariant components of w_k.

By replacing (5-102) in (5-99), it turns out that the coefficients $\mu_{k,h}$ can be found by solving the following matrix equation:

$$\begin{bmatrix} \mu_{1,1} & \mu_{1,2} \\ \mu_{2,1} & \mu_{2,2} \end{bmatrix} = \begin{bmatrix} < v_1, v_1 > & < v_1, v_2 > \\ < v_2, v_1 > & < v_2, v_2 > \end{bmatrix} = V_C^2 \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \tag{5-103}$$

The explicit solution of (5-103) is

$$\begin{bmatrix} \mu_{1,1} & \mu_{1,2} \\ \mu_{2,1} & \mu_{2,2} \end{bmatrix} = V_C^2 \begin{bmatrix} < v_1, v_1 > & < v_1, v_2 > \\ < v_2, v_1 > & < v_2, v_2 > \end{bmatrix}^{-1} \tag{5-104}$$

It is necessary to consider the expressions of v_L and v_H

$$v_H = \frac{V_C}{2} + R i_d - v_{\text{int}} - L \frac{di_d}{dt} \cong \frac{V_C}{2} - v_{\text{int}} \tag{5-105}$$

$$v_L = \frac{V_C}{2} + R i_d + v_{\text{int}} + L \frac{di_d}{dt} \cong \frac{V_C}{2} + v_{\text{int}} \tag{5-106}$$

where the resistance is negligible, and the terms with the inductance is equal to zero in steady state operation if the control is working correctly.

The four different inner products are:

$$< v_H, v_H >= \frac{1}{2\pi} \int_0^{2\pi} v_H^2 d\theta = \frac{1}{2\pi} \int_0^{2\pi} (\frac{V_C}{2} - v_{\text{int}})^2 d\theta = \frac{1}{2\pi} \int_0^{2\pi} (\frac{V_C^2}{4} + v_{\text{int}}^2) d\theta = \frac{V_C^2}{4} + V_{\text{int,}RMS}^2 \tag{5-107}$$

$$< v_L, v_L >= \frac{1}{2\pi} \int_0^{2\pi} v_L^2 d\theta = \frac{1}{2\pi} \int_0^{2\pi} (\frac{V_C}{4} + v_{\text{int}})^2 d\theta = \frac{1}{2\pi} \int_0^{2\pi} (\frac{V_C^2}{4} + v_{\text{int}}^2) d\theta = \frac{V_C^2}{4} + V_{\text{int,}RMS}^2 \tag{5-108}$$

$$< v_H, v_L >= \frac{1}{2\pi} \int_0^{2\pi} v_H v_L d\theta = \frac{1}{2\pi} \int_0^{2\pi} (\frac{V_C^2}{4} - v_{\text{int}}^2) d\theta = \frac{V_C^2}{4} - V_{\text{int,}RMS}^2 \tag{5-109}$$

$$< v_L, v_H >= \frac{1}{2\pi} \int_0^{2\pi} v_L v_H d\theta = \frac{1}{2\pi} \int_0^{2\pi} (\frac{V_C^2}{4} - v_{\text{int}}^2) d\theta = \frac{V_C^2}{4} - V_{\text{int,}RMS}^2 \tag{5-110}$$

It is possible to calculate the explicit expression of the coefficients $\mu_{k,h}$:

$$\mu_{1,1} = \mu_{2,2} = \left(1 + \frac{V_C^2}{4V_{\text{int},RMS}^2}\right) \tag{5-111}$$

$$\mu_{1,2} = \mu_{2,1} = \left(1 - \frac{V_C^2}{4V_{\text{int},RMS}^2}\right) \tag{5-112}$$

where $V_{int,RMS}$ is the root mean square value of the internal voltage.

The expressions of w_1 and w_2 resulting from (5-81)-(5-82), (5-102) and (5-111)-(5-112) are

$$w_1 = V_C\left(1 - \frac{V_C}{2}\frac{v_{\text{int}}}{V_{\text{int},RMS}^2}\right) \tag{5-113}$$

$$w_2 = V_C\left(1 + \frac{V_C}{2}\frac{v_{\text{int}}}{V_{\text{int},RMS}^2}\right) \tag{5-114}$$

According to (5-100)-(5-101), the values of λ_1 and λ_2 can be separately chosen to control the average value of the arm energies. Finally, the reference value for i_d, can be found on the basis of (5-98), (5-113) and (5-114).

5.2.14.3 Control Scheme

A control scheme for MMC based on (5-100)-(5-101) is shown in Figure 5-58. As can be seen, according to the proposed solution, the structure of the control scheme is rather simple. The main idea is to decouple the control of the currents i_0 and i_d.

The internal loops are the same of the previous control, two controllers have the task to track the reference currents $i_{0,ref}$ and $i_{d,ref}$. Since these references are not constant, it is necessary to adopt controllers that are suitable to reduce the steady-state error, such as high-gain PI regulators, deadbeat controller or resonant PI controllers.

The voltages v_{int} and v_d are the output signals of the current controllers. Once they are known, the output voltages of the SMs, and consequently the duty-cycles, can be found and s_H and s_L are:

$$s_H = \frac{v_H}{v_{CH}} = \frac{v_d - v_{\text{int}}}{v_{CH}} \tag{5-115}$$

$$s_L = \frac{v_L}{v_{CL}} = \frac{v_d + v_{\text{int}}}{v_{CL}} \tag{5-116}$$

The reference signal $i_{d,ref}$ is determined according to (5-98) as a linear combination of the orthogonal functions w_1, w_2 and the components λ_1 and λ_2.

Equations (5-100)-(5-101) show that the average values of W_{CH} and W_{CL} can be controlled separately by changing λ_1 and λ_2. Two PI controller, (c) and (d), ensure the tracking of the arm energy references, while the low pass filters are designed in such a way to cut out the energy oscillations. The reference signals of the arm energies are calculated by means of (5-24)-(5-25), where the dc voltage v_H and v_L are equal to the desired reference values $v_{H,ref}$ and $v_{L,ref}$.

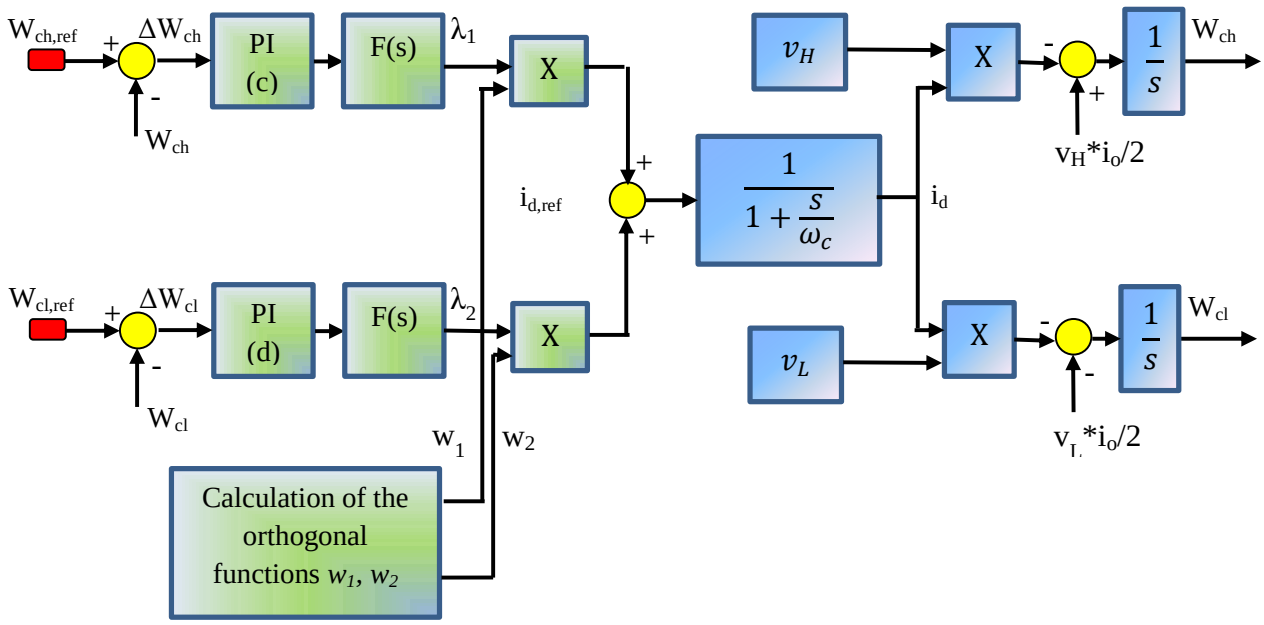


Figure 5-58 – Control scheme energy loop, orthogonal function and two-time scale analysis approach.

5.2.15 Simulation model of single leg MMC – Orthogonal functions and two-time scale analysis approach

Figure 5-59 shows the general model realized in Matlab/Simulink of the single leg MMC controlled with orthogonal functions and two time scale analysis approach. The model of the single leg MMC, the DC link and the load is shown in Figure 5-60. The MMC is realized with elements of the Sim Power System library as shown for the unconstrained control.

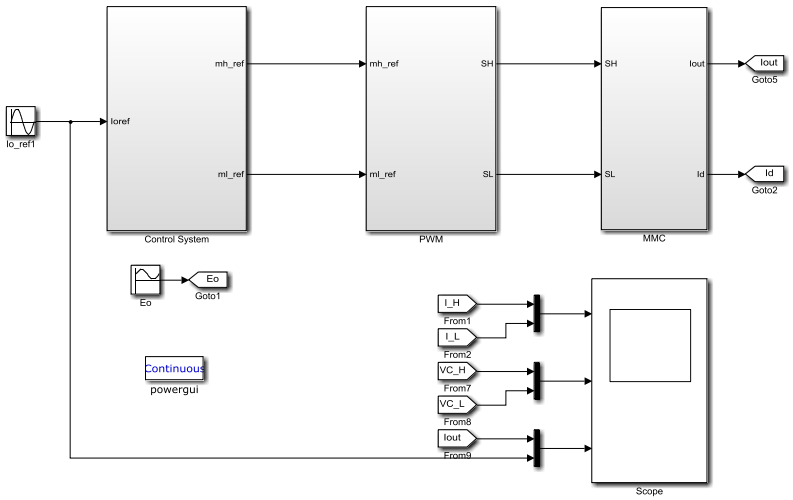


Figure 5-59 – Simulink general model of single leg MMC.

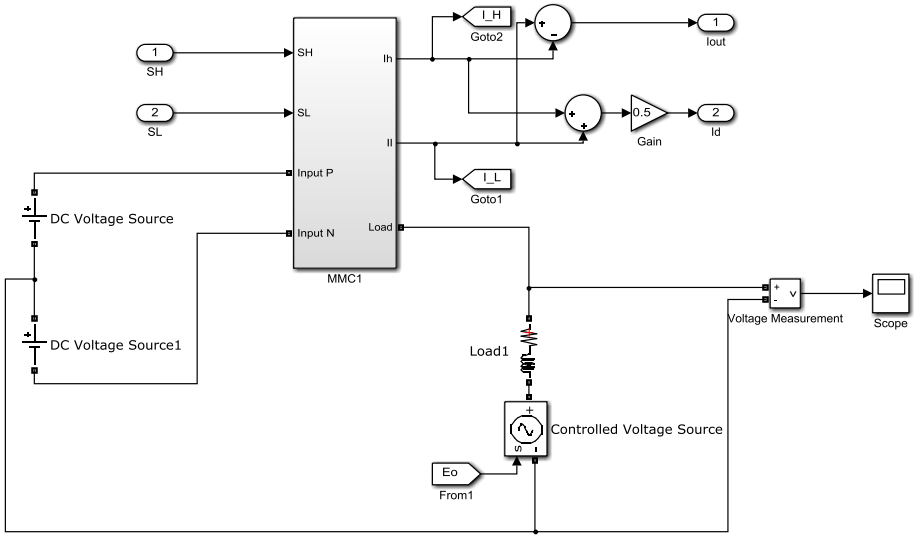


Figure 5-60 – Simulink model of single leg MMC, DC link and load.

In Figure 5-61 it is possible to see in the upper part the energy control loop, and in the lower part the calculation of the functions w_1 and w_2. The current internal loop is the same of the unconstrained control as already discussed.

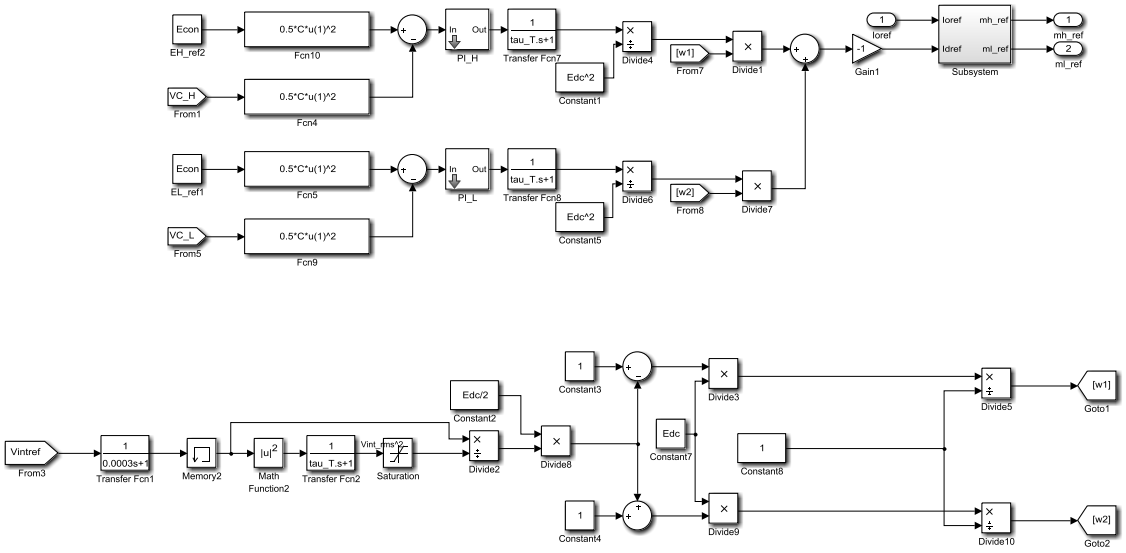


Figure 5-61 – Control system of the single leg MMC.

In Table 5-4 the simulation parameters are listed.

DC voltage	24 [V]
Capacitors	880 [μF]
Capacitors reference voltage	30 [V]
Arm inductance	1.18 [mH]
Arm resistance	0.4 [Ω]
Load inductance	0.5 [mH]
Load resistence	1 [Ω]
Load current	2 [A]
Frequency	50 [Hz]

Table 5-4 – Simulation parameters.

5.2.16 Simulation results of single leg MMC – Orthogonal functions and two-time scale analysis approach

In Figure 5-62 the load current is shown. As it is possible to notice, it follows the reference signal with satisfying dynamic performances.

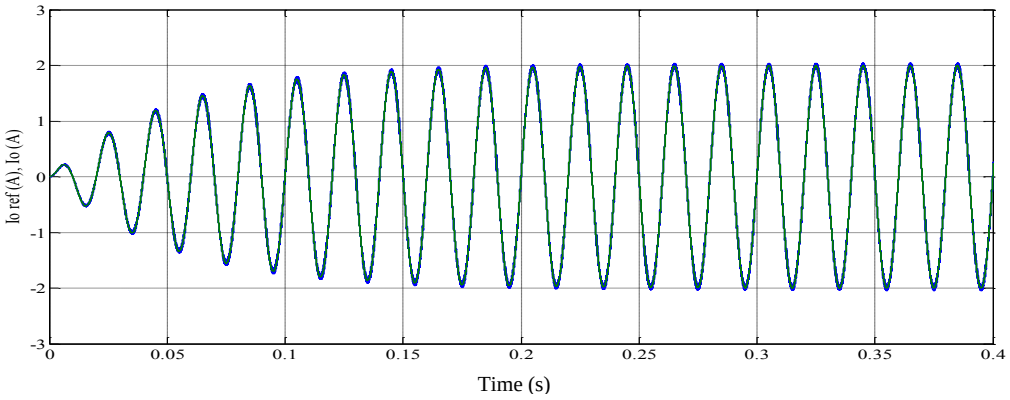


Figure 5-62 – Load current.

Figure 5-63 shows the differential current that has the same form of the other controls with a mean value of - 0.2 A. In Figure 5-64 the arm currents are shown.

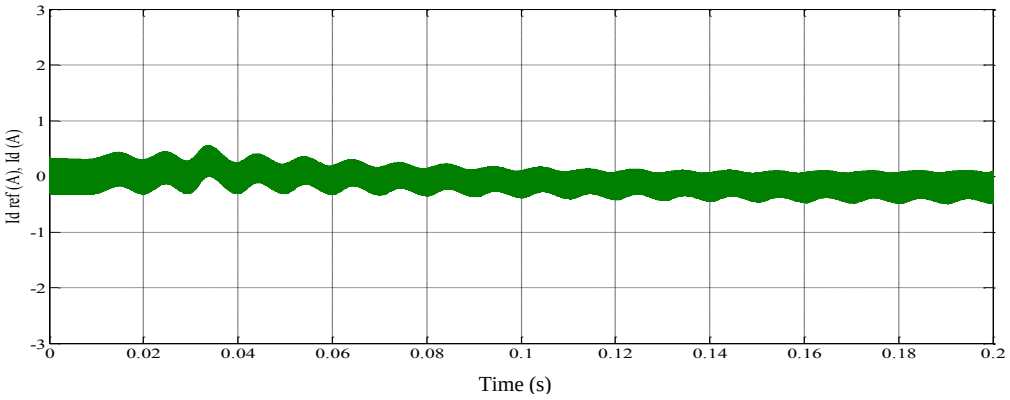


Figure 5-63 – Differential current.

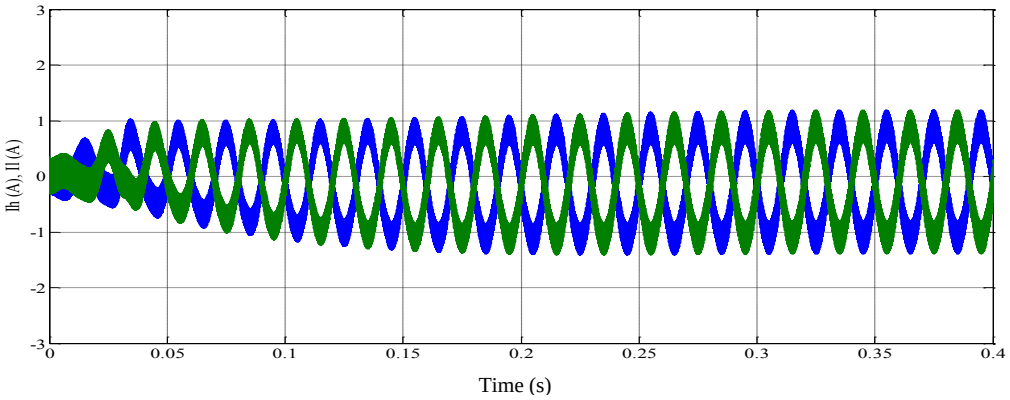


Figure 5-64 – Upper and lower arm currents.

The modulating signals, corresponding to the required operating condition are shown in Figure 5-65. It can be observed that, after a transient, they oscillate around the average value of 0.5, and have opposite phases, as for the other controls.

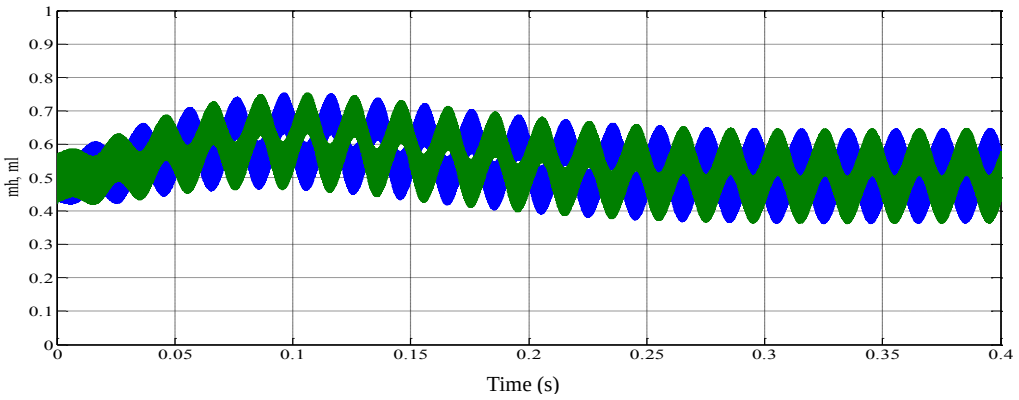


Figure 5-65 – Modulating signals.

In Figure 5-66 the voltages of the upper and lower capacitors are shown. It is possible to see that after a transient the average value in steady state corresponds to the reference value. The amplitude of the oscillations is about 1.5 V. In Figure 5-67 the waveform of the functions w_1 and w_2 are shown.

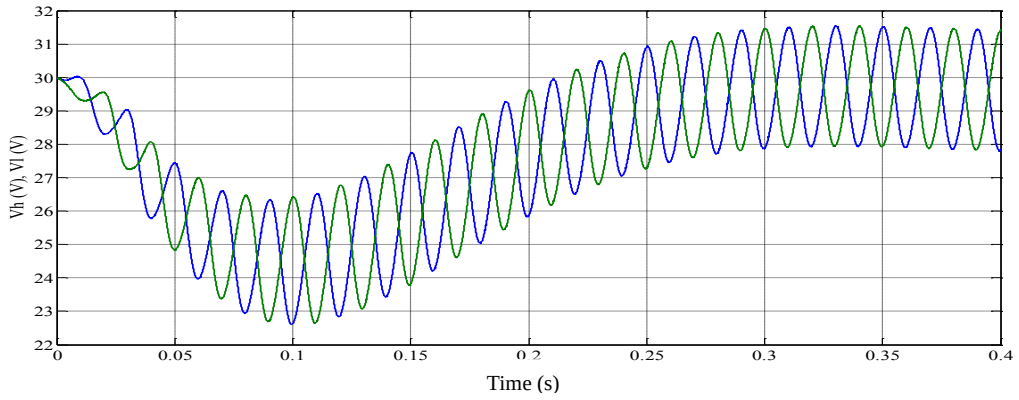


Figure 5-66 – Upper and lower capacitor voltages.

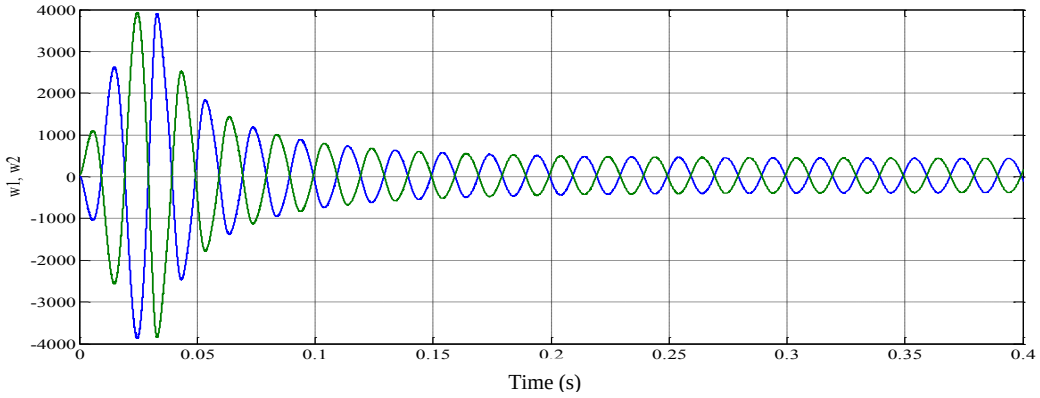


Figure 5-67 – Functions w_1 and w_2.

In Figure 5-68 the internal voltage and the differential voltage are displayed. The average value of the differential voltage is equal to half of the DC voltage while the internal voltage has an average value equal to zero and an amplitude that depends on the load requests.

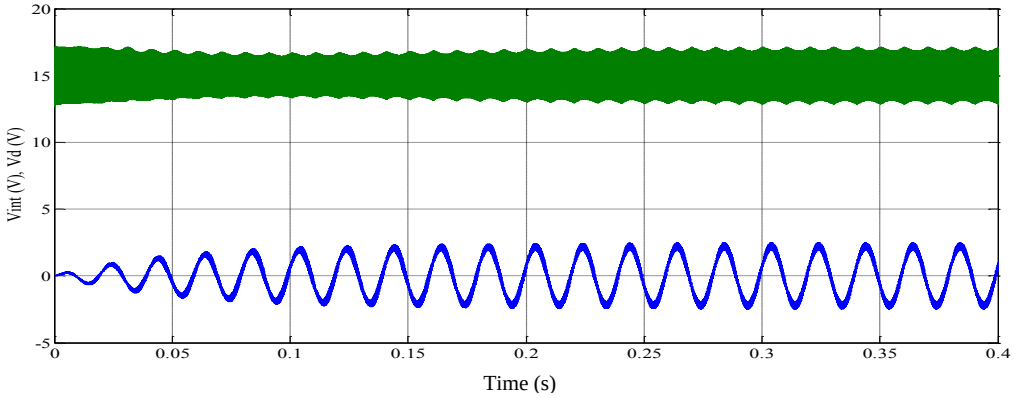


Figure 5-68 – Internal voltage and differential voltage.

In Figure 5-69 the output voltage is shown. It is possible to see that it is affected by the effect of commutations in fact the load is a generic R-L-E load and not the grid that can impose its sinusoidal voltage.

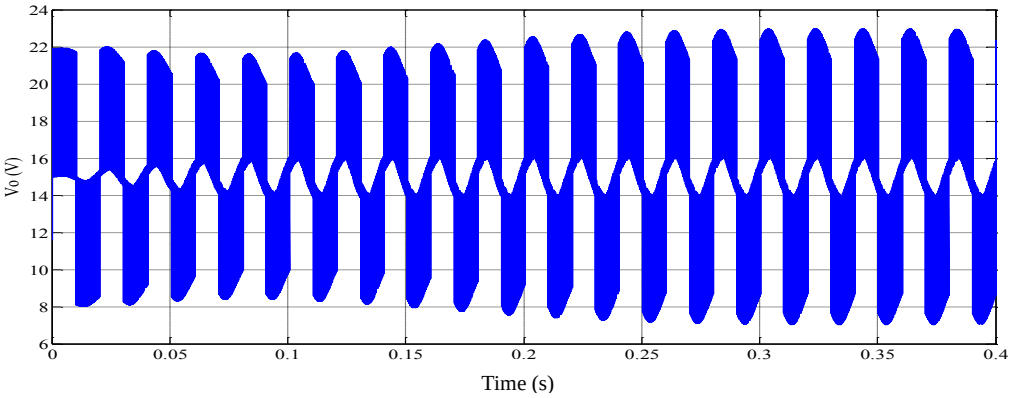


Figure 5-69 – Output voltage.

It is interesting to verify what happens if the two capacitors starts with a voltage that is 20% lower than the reference value. If the controls works correctly it should follow the reference load current and recharge the two capacitors with the energy controllers. In Figure 5-70 it is possible to see that the load currents follows the reference value.

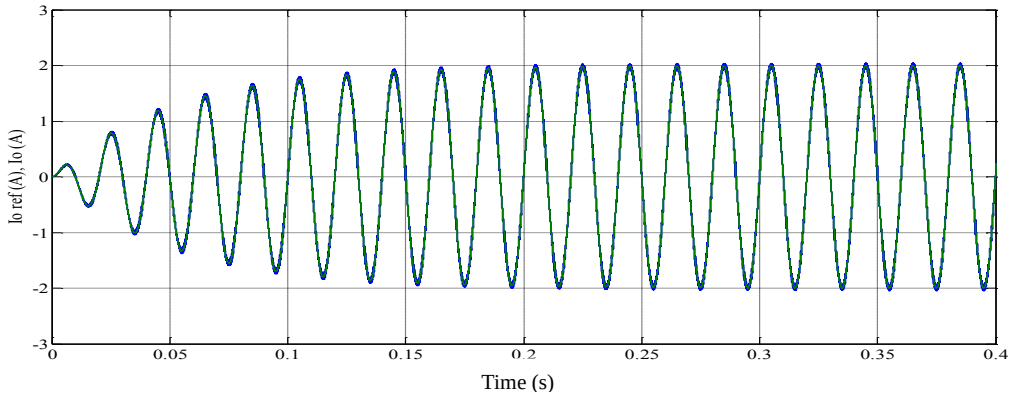


Figure 5-70 – Load current with discharged capacitors.

In Figure 5-71 it is possible to observe the differential current. Finally it is possible to see that the two capacitors that start in a discharged state after a transient are at the right reference value in Figure 5-72.

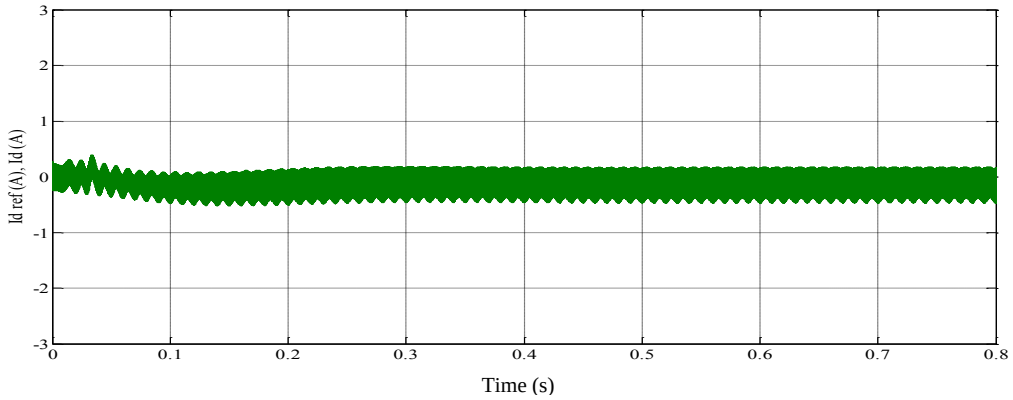


Figure 5-71 – Differential current with discharged capacitors.

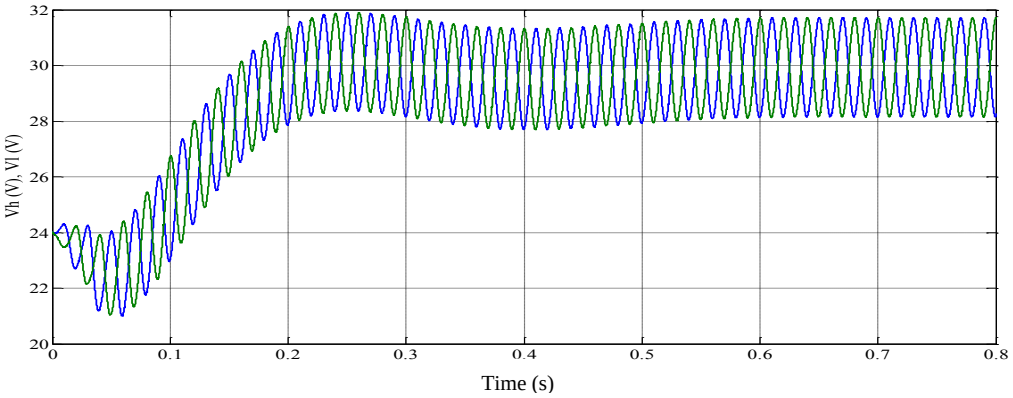


Figure 5-72 – Upper and lower capacitor voltages with discharged capacitor.

The other condition that the control system should properly manage, is the unbalance between the upper and the lower capacitors. In particular if the upper one starts with a voltage that is +20% the reference value and the lower one -20% the reference value it is possible to see in Figure 5-73 the load current is still at the correct value.

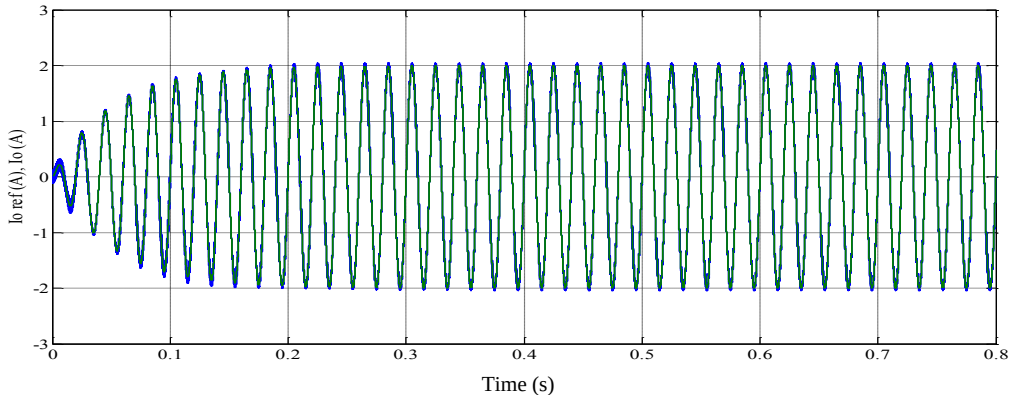


Figure 5-73 – Load current with unbalanced capacitor voltages.

The differential current is shown in Figure 5-74 while in Figure 5-75 the voltage capacitors are displayed and they are still at the right reference value after a transient.

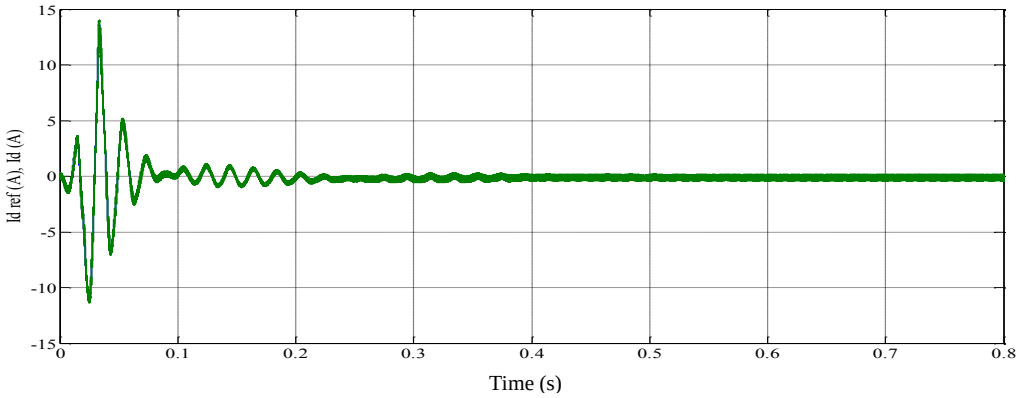


Figure 5-74 – Differential current with unbalanced capacitor voltages.

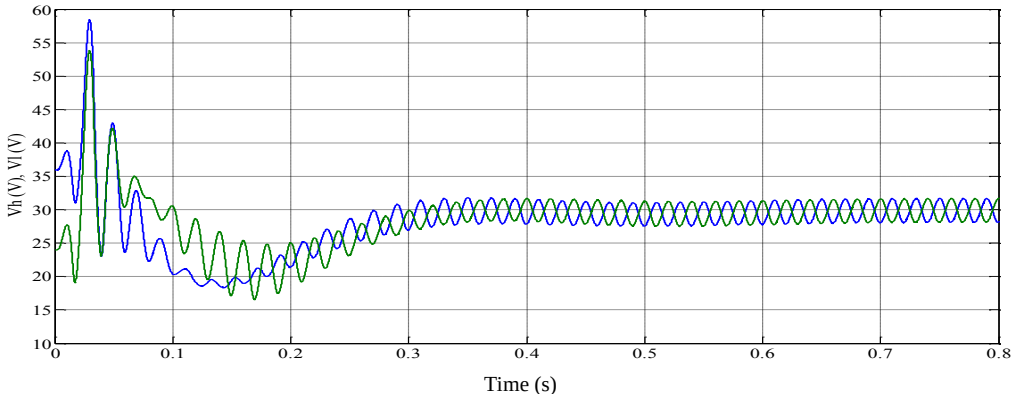


Figure 5-75 – Upper and lower capacitor voltages with unbalanced capacitor voltages.

5.2.17 Experimental results of single leg MMC – Orthogonal functions and two-time scale analysis approach

A sinusoidal reference signal for the load current, of amplitude 4 A and frequency 50 Hz is required. In Figure 5-76 it is possible to compare the reference load current with the real load current. The displayed quantities have a frequency of 50 Hz and the load current has an amplitude of 4 A, like the reference signal.

In Figure 5-77 the reference load current and the measured load current are shown in detail. In Figure 5-78 it is shown the initial transient of the load current. It is possible to notice that, the

tuning of the regulators implemented, allows to obtain a good dynamic response as displayed in detail in Figure 5-79.

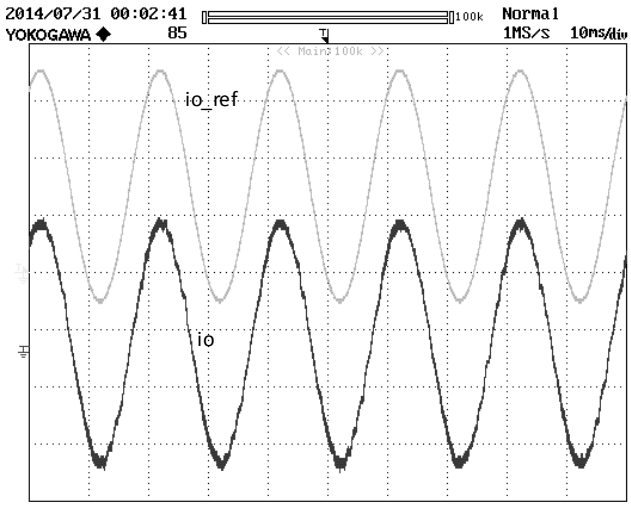


Figure 5-76 – Load current (2 A/div) - (10 ms/div).

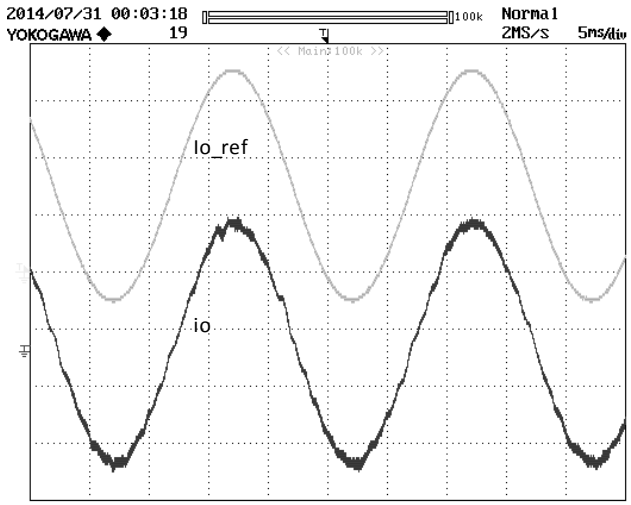


Figure 5-77 – Load current (2 A/div) detail - (5 ms/div).

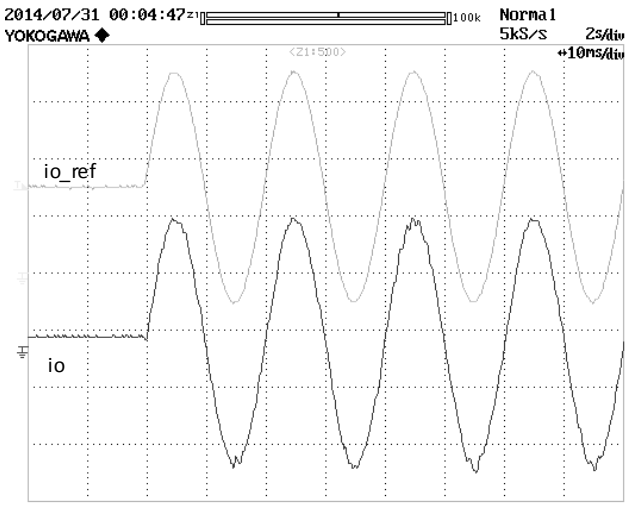


Figure 5-78 – Transient of load current (2 A/div) - (10 ms/div).

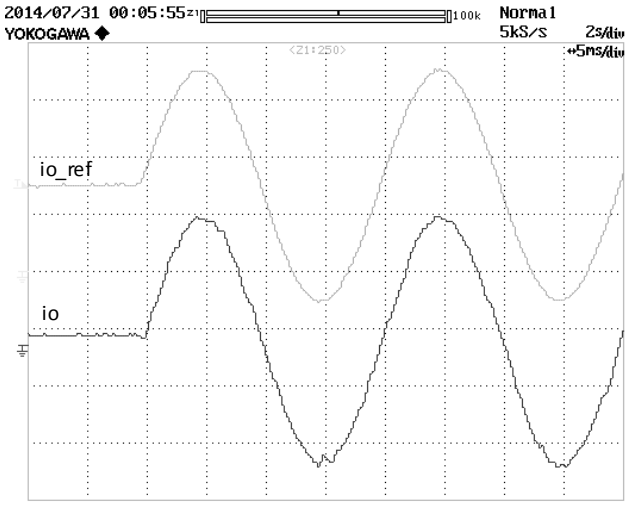


Figure 5-79 – Transient of load current (2 A/div) detail - (5 ms/div).

In Figure 5-80 the currents of the upper and lower arms are. In Figure 5-81 the same currents are shown in detail.

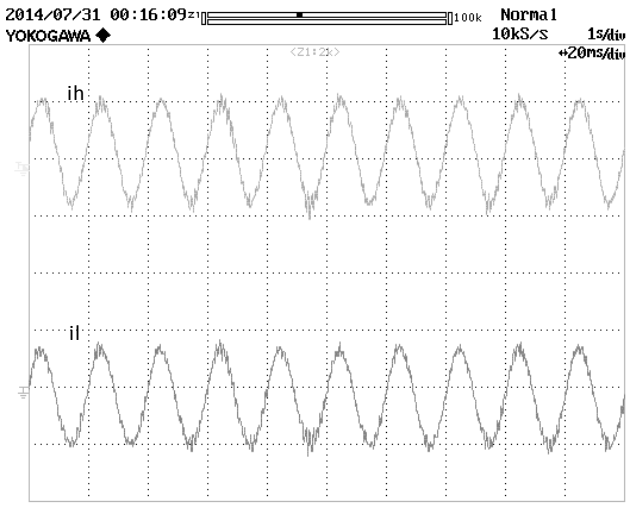


Figure 5-80 – Upper and lower arm currents (2 A/div) - (20 ms/div).

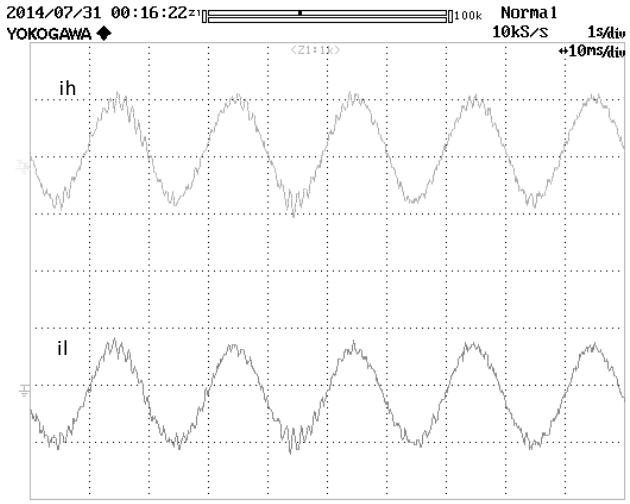


Figure 5-81 – Upper and lower arm currents (2 A/div) detail - (10 ms/div).

The transient of the arm currents is shown in Figure 5-82 and in Figure 5-83 with different time scales.

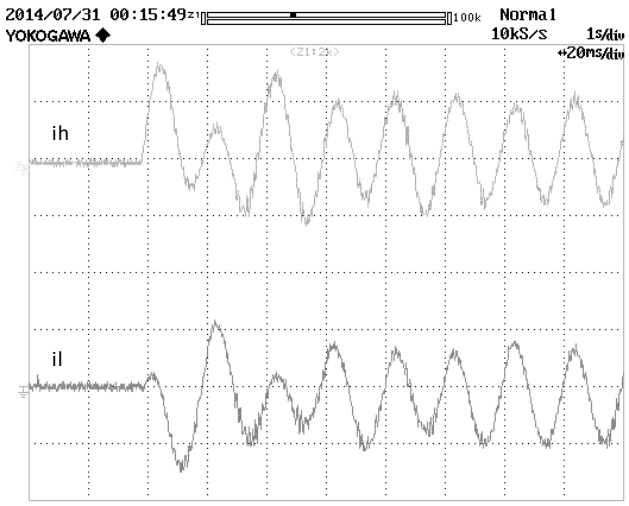


Figure 5-82 – Transient of upper and lower arm currents (2 A/div) - (20 ms/div).

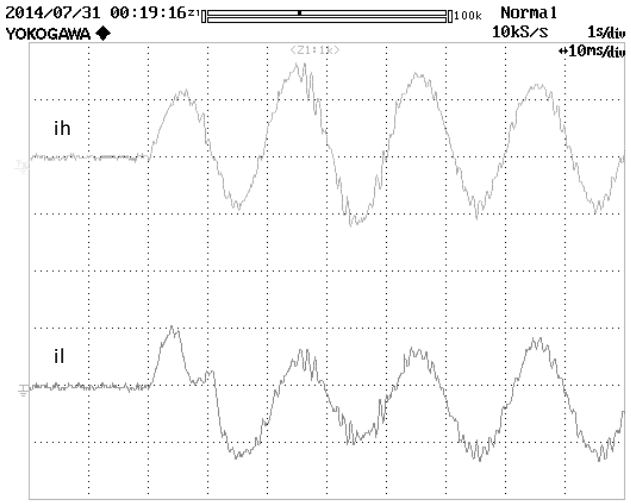


Figure 5-83 – Transient of upper and lower arm currents (2 A/div) detail - (10 ms/div).

In Figure 5-84 it is possible to compare the load current and the differential current. In Figure 5-85 these two currents are shown in detail. In both figures it is possible to observe the initial transient of the differential current.

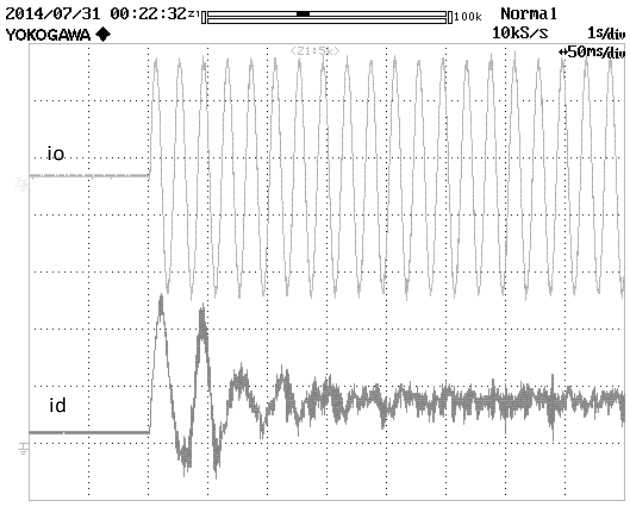


Figure 5-84 – Transient of load and differential currents (2 A/div) - (50 ms/div).

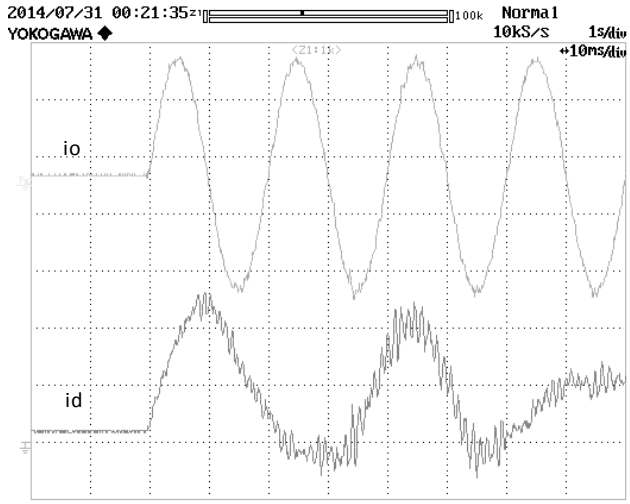


Figure 5-85 – Transient of load and differential currents (2 A/div) detail - (10 ms/div).

The capacitor voltages of the two modules are shown in Figure 5-86. The voltages across the capacitors oscillate around 30 V with an amplitude of about 4 V and frequency of 50 Hz. In Figure 5-87 the transient of the voltages is shown.

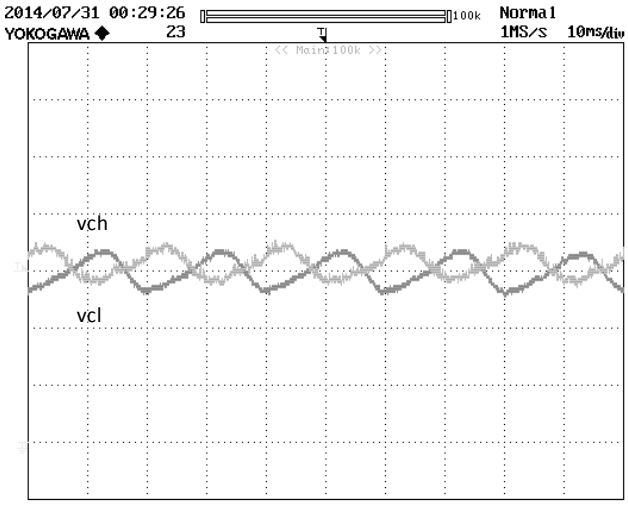


Figure 5-86 – Upper and lower capacitor voltages (10 V/div) - (10 ms/div).

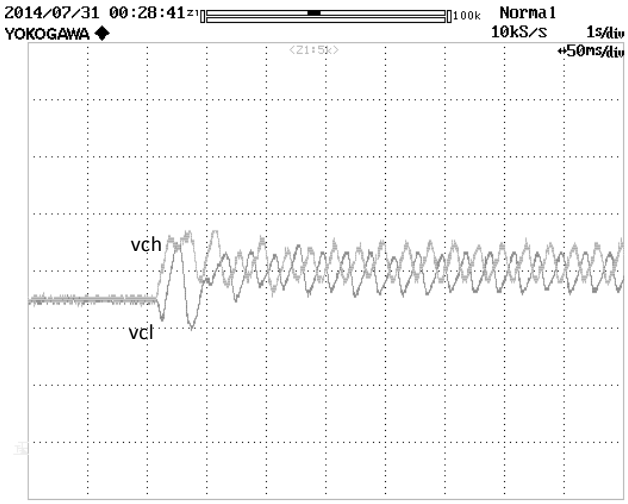


Figure 5-87 – Transient of upper and lower capacitor voltages (10 V/div) - (50 ms/div).

In Figure 5-88 the function w_1 and w_2 are shown. The same functions are displayed in detail in Figure 5-89.

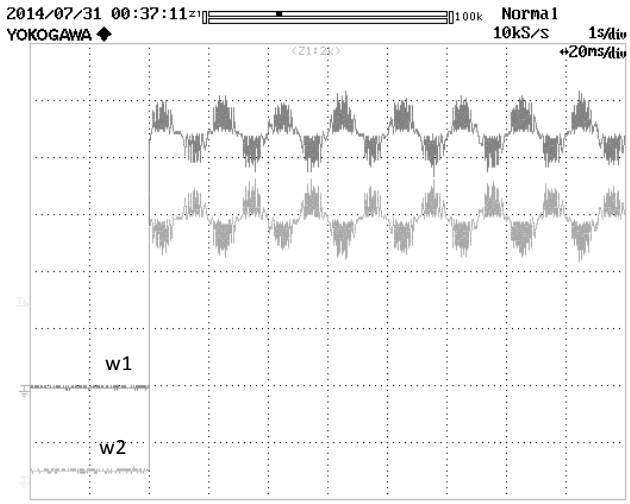


Figure 5-88 – Transient of functions w_1 and w_2 (20 V/div) - (20 ms/div).

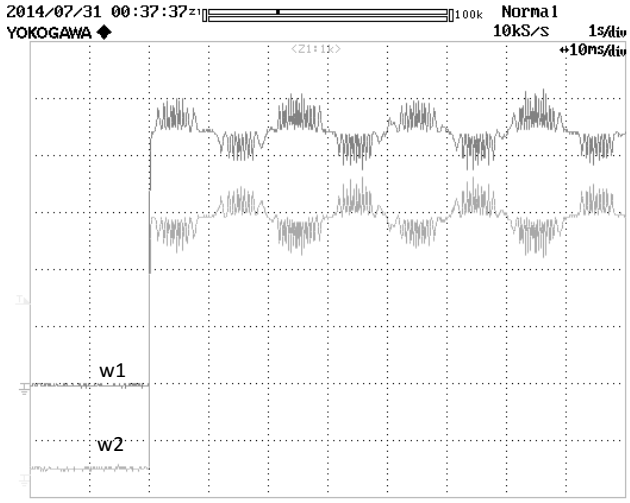


Figure 5-89 – Transient of functions w_1 and w_2 (20 V/div) detail - (10 ms/div).

In Figure 5-90 the output voltages of the upper and lower modules of the leg are shown. In Figure 5-91 the initial transient is shown.

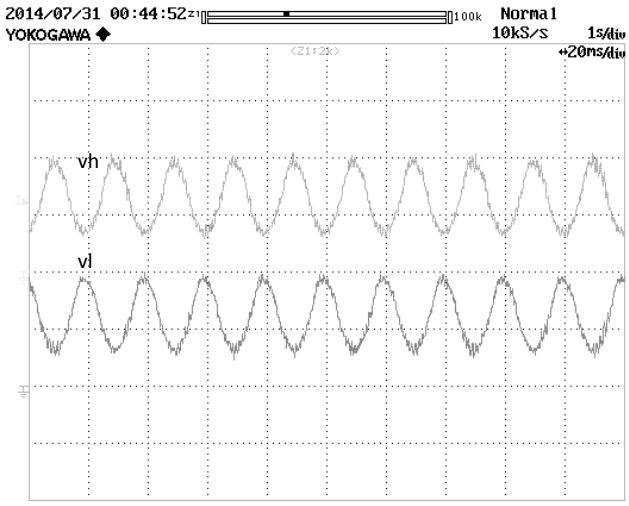


Figure 5-90 – Upper and lower module voltages (10 V/div) - (20 ms/div).

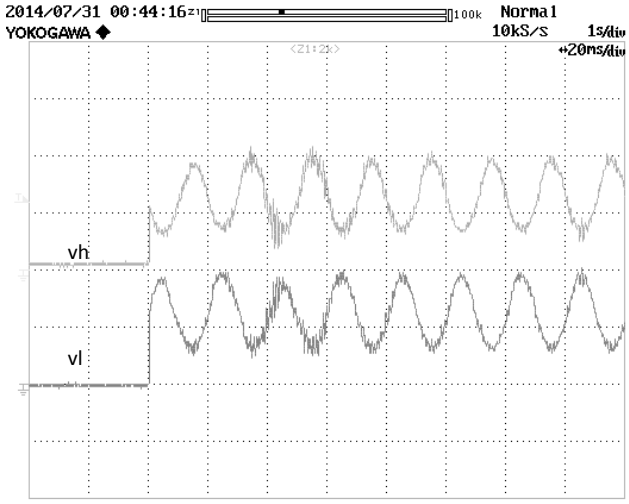


Figure 5-91 – Transient of upper and lower module voltages (10 V/div) - (20 ms/div).

In Figure 5-92 the internal voltage and the differential voltage are shown. In Figure 5-93 the initial transients of the same voltages are displayed.

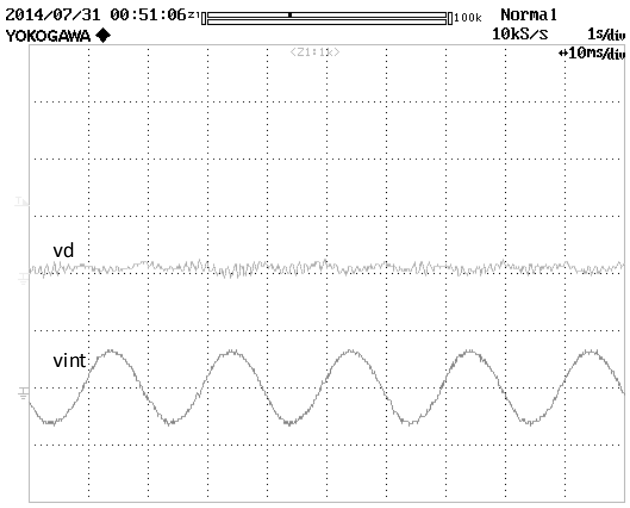


Figure 5-92 – Internal and differential voltages (10 V/div) - (10 ms/div).

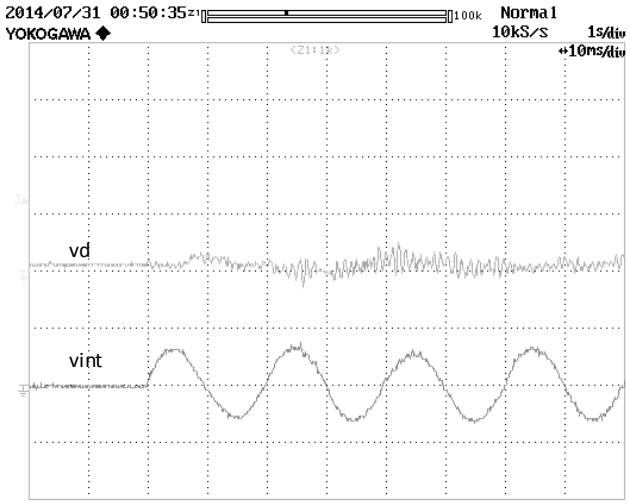


Figure 5-93 – Transient of internal and differential voltages (10 V/div) - (10 ms/div).

5.2.18 Equivalence between a series of *n* modules and an equivalent single module

In general a single leg of MMC can be constituted by a series of *n* sub-modules. In this section it will be demonstrated the equivalence of this series with a three-level MMC inverter with only a single equivalent module for the upper arm and one for the lower arm. To this end it is necessary to report the series of a generic number of sub-modules to the equivalent one.

As already discussed the single module is constituted by a capacitor connected in parallel with a series of two IGBTs with the reverse recovery diode.

If the upper arm is taken into account and is constituted by *n* sub-modules, the equations for all the *n* modules are:

$$\begin{cases} v_{H1} = s_{H1} v_{CH1} \\ v_{H2} = s_{H2} v_{CH2} \\ \quad \dots \\ v_{Hj} = s_{Hj} v_{CHj} \\ \quad \dots \\ v_{Hn} = s_{Hn} v_{CHn} \end{cases} \quad \begin{cases} i_{CH1} = s_{H1} i_H \\ i_{CH2} = s_{H2} i_H \\ \quad \dots \\ i_{CHj} = s_{Hj} i_H \\ \quad \dots \\ i_{CHn} = s_{Hn} i_H \end{cases} \quad \begin{cases} \dfrac{dv_{CH1}}{dt} = -\dfrac{i_{CH1}}{C_1} \\ \dfrac{dv_{CH2}}{dt} = -\dfrac{i_{CH2}}{C_2} \\ \quad \dots \\ \dfrac{dv_{CHj}}{dt} = -\dfrac{i_{CHj}}{C_j} \\ \quad \dots \\ \dfrac{dv_{CHn}}{dt} = -\dfrac{i_{CHn}}{C_n} \end{cases} \tag{5-117}$$

For the lower arm, it is possible to find similar equations substituting *H* with *L*:

$$\begin{cases} v_{L1} = s_{L1} v_{CL1} \\ v_{L2} = s_{L2} v_{CL2} \\ \quad \dots \\ v_{Lj} = s_{Lj} v_{CLj} \\ \quad \dots \\ v_{Ln} = s_{Ln} v_{CLn} \end{cases} \quad \begin{cases} i_{CL1} = s_{L1} i_L \\ i_{CL2} = s_{L2} i_L \\ \quad \dots \\ i_{CLj} = s_{Lj} i_L \\ \quad \dots \\ i_{CLn} = s_{Ln} i_L \end{cases} \quad \begin{cases} \dfrac{dv_{CL1}}{dt} = -\dfrac{i_{CL1}}{C_1} \\ \dfrac{dv_{CL2}}{dt} = -\dfrac{i_{CL2}}{C_2} \\ \quad \dots \\ \dfrac{dv_{CLj}}{dt} = -\dfrac{i_{CLj}}{C_j} \\ \quad \dots \\ \dfrac{dv_{CLn}}{dt} = -\dfrac{i_{CLn}}{C_n} \end{cases} \tag{5-118}$$

where s_{Hj} and s_{Lj} are the switching functions of the upper and lower module *j* respectively, v_{CHj} and v_{CLj} are the voltages of the capacitor *j* in the upper and lower arm respectively and v_{Hj} and v_{Lj} the output voltages of the module *j* in the upper and lower arm respectively. The currents i_{CHj} and i_{CLj} are the currents for the capacitor *j* of the upper and lower arm respectively, while i_H and i_L are the currents of the upper and lower arm.

At first, the upper module will be considered then the results will be extended to the lower one.
The voltage of the series of the modules can be obtained by summing the voltages of the sub-modules, as follows:

$$v_H = v_{H1} + v_{H2} + \dots + v_{Hj} + \dots + v_{Hn} = \sum_{j=1}^{n} v_{Hj} \tag{5-119}$$

$$v_H = s_{H1} v_{CH1} + s_{H2} v_{CH2} + \dots + s_{Hj} v_{CHj} + \dots + s_{Hn} v_{CHn} \tag{5-120}$$

It is supposed that the voltages across the capacitors are equal, it is true if the average value over a period is considered:

$$v_{CH1} = v_{CH2} = ... = v_{CHj} = ... = v_{CHn} = v'_{CH} \tag{5-121}$$

The voltage of the equivalent capacitor is defined as follow:

$$v_{CH} = nv'_{CH} \tag{5-122}$$

$$v_H = \sum_{j=1}^{n} s_{Hj} v'_{CH} = v'_{CH} \sum_{j=1}^{n} s_{Hj} = \frac{v_{CH}}{n} \sum_{j=1}^{n} s_{Hj} \tag{5-123}$$

The equivalent switching function is defined as follow:

$$s_H = \frac{1}{n} \sum_{j=1}^{n} s_{Hj} \Rightarrow v_H = s_H v_{CH} \tag{5-124}$$

This way the structure of the voltage equation for the equivalent module is equal to the voltage equation of the generic module.

The inverter is designed so that the capacitors has the same value for all the sub-modules.

$$C_1 = C_2 = ... = C_j = ... = C_n = C' \tag{5-125}$$

The equivalent capacitance is obtained by dividing the capacitance of the single module by *n*:

$$C = \frac{C'}{n} \tag{5-126}$$

Introducing the current equation it is possible to obtain:

$$\sum_{j=1}^{n} i_{CHj} = \sum_{j=1}^{n} s_{Hj} i_H = i_H \sum_{j=1}^{n} s_{Hj} = i_H n s_H \tag{5-127}$$

Defining the equivalent current for the capacitor and using the definition of the equivalent switching function it is possible to obtain:

$$i_{CH} = \frac{1}{n} \sum_{j=1}^{n} i_{CHj} \Rightarrow i_{CH} = s_H i_H \tag{5-128}$$

This way the equation for the equivalent current of the module has the same structure of the equation of the generic module.

By adding all the derivatives of the voltage drops across the capacitors and introducing equation (5-22):

$$\sum_{j=1}^{n}\frac{dv_{CHj}}{dt}=\frac{d}{dt}\sum_{j=1}^{n}v_{CHj}=\frac{d}{dt}(nv_{CH}^{'})=\frac{d}{dt}v_{CH} \tag{5-129}$$

It is possible to see that, the sum of the derivatives of the voltages is equal to the derivative of the sum of the voltages on the assumption that the voltages are free of discontinuities in time. This assumption is always verified because the electrostatic energy stored by a capacitor depends on the square of the voltage and if the voltage is discontinuous than the capacitor would exchange an infinite power with the outside, which is absurd from a physical point of view. The principle described above is known as the principle of continuity of the voltage on the capacitors.

Adding all the second members of capacitors equations in (5-117) and using the definition of the capacitor current:

$$\sum_{j=1}^{n}\frac{i_{CHj}}{C_j}=\sum_{j=1}^{n}\frac{i_{CHj}}{C^{'}}=\frac{1}{C^{'}}\sum_{j=1}^{n}i_{CHj}=\frac{ni_{CH}}{C^{'}}=\frac{i_{CH}}{C} \tag{5-130}$$

Equating the sum of the first members with the sum of the second members it is possible to find an equation for the equivalent capacitor module entirely analogous to that of the capacitor of the generic module:

$$\frac{dv_{CH}}{dt}=-\frac{i_{CH}}{C} \tag{5-131}$$

Of course, it's possible to make a reasoning entirely analogous for the lower arm defining the voltage of the equivalent capacitor, the switching function and the equivalent current of the equivalent capacitor. The equivalent capacity is considered equal for upper and lower arms. For the lower arm, in summary:

$$\begin{cases} v_{CL}=nv_{CL}^{'} \\ s_L=\dfrac{1}{n}\displaystyle\sum_{j=1}^{n}s_{Lj} \\ i_{CL}=\dfrac{1}{n}\displaystyle\sum_{j=1}^{n}i_{CLj} \end{cases} \Rightarrow \begin{cases} v_L=s_Lv_{CL} \\ i_{CL}=s_Li_L \\ \dfrac{dv_{CL}}{dt}=-\dfrac{i_{CL}}{C} \end{cases} \tag{5-132}$$

Consequently, the simple case of a single module for the upper arm and a single module for the lower arm can be considered, aware that the discussion can be generalized in any moment to any number of modules, through the definitions introduced. The equations are valid instant by instant,

and the switching functions of the upper and lower modules are considered coinciding with the switching functions of the respective arms in the simple case of a single module for each arm. If the average values in the generic switching period are considered than, the modulating signals instead of the switching functions should be taken into account.

5.2.19 Simulation model of the internal control loop for the management of the capacitors voltage levels

When the number of modules per arm is greater than one is necessary to choose, based on the value of the reference voltages, which modules to activate. The choice can be based on the direction of the currents of the arms and on the values of the capacitor voltages of the modules. An arm having two upper modules and two lower modules with a control system with unconstrained approach was simulated, by placing a block named CVB (Capacitor Voltage Balancing), between the block of the unconstrained control, and the PWM modulator. The overall block diagram is shown in Figure 5-94. The block containing the unconstrained control system incorporates both the energy control and the current control, as seen for the simulation of single leg control with only one module per arm, and provides at its output the reference voltages of the upper and lower arms.
The task of block CVB, shown in Figure 5-95 (where the block in the right part is internal to the block in the left part), is therefore the calculation of the modulating signals of the four modules.

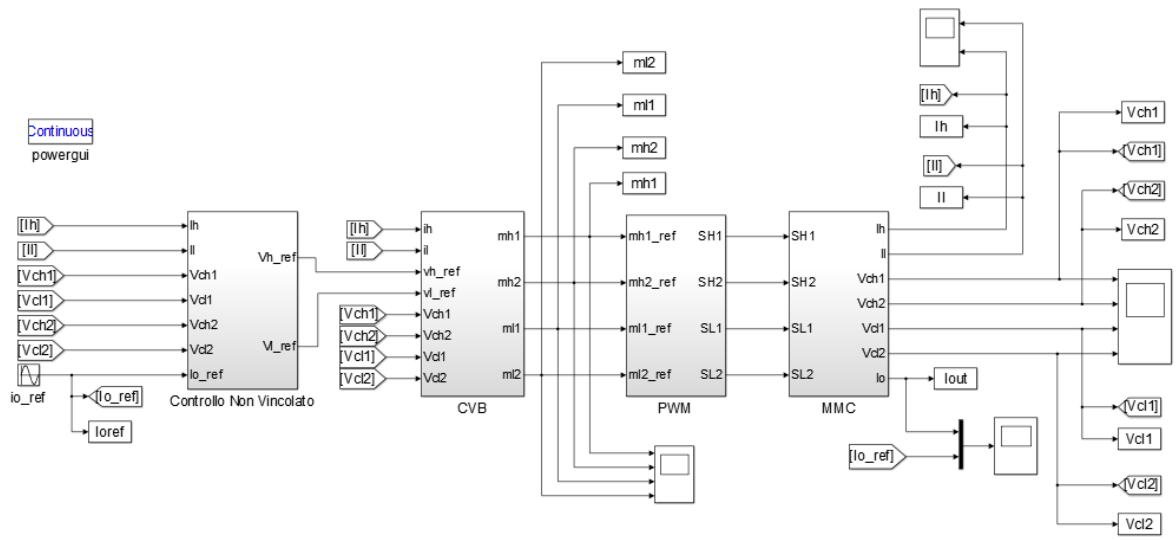


Figure 5-94 – Simulink general scheme of single leg MMC with two modules per arm.

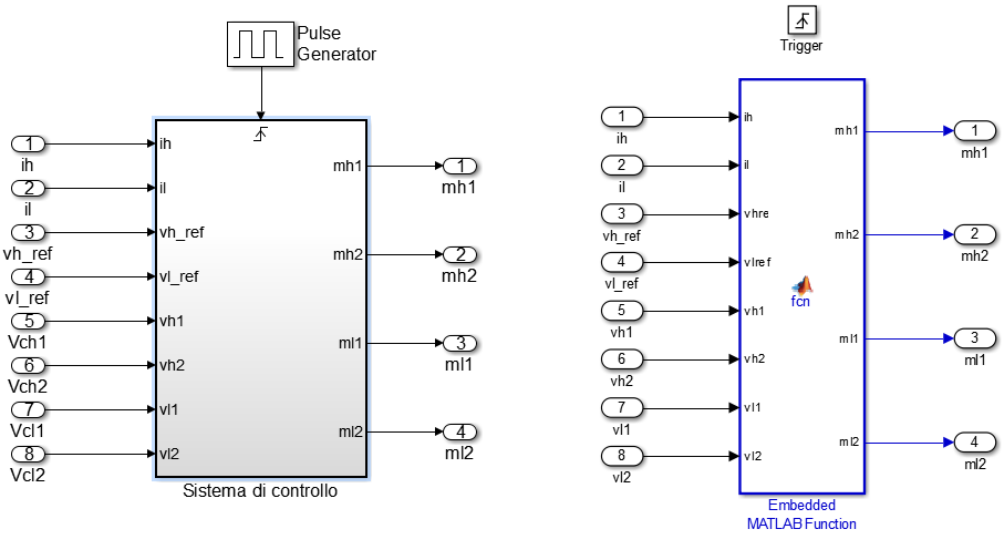


Figure 5-95 – Control scheme of single leg MMC with two modules per arm.

The "Matlab function" contained in the block of the right part of Figure 5-95 is shown below.

```
function [mh1,mh2,ml1,ml2] = fcn(ih,il,vhref,vlref,vh1,vh2,vl1,vl2)

%   Calcolo delle modulanti
% Ramo superiore

if (ih>0); %I condensatori superiori si scaricheranno
    if (vh1>vh2); %Si deve scaricare h1
        if (vh1>vhref);
            mh1=vhref/vh1;
            mh2=0;
        else;
            mh1=1;
            mh2=(vhref-vh1)/vh2;
        end;
    else;
        if (vh2>vhref);
            mh2=vhref/vh2;
            mh1=0;
        else;
            mh2=1;
            mh1=(vhref-vh2)/vh1;
        end;
    end;
```

```
else; %I condensatori superiori si caricheranno
    if (vh1>vh2); %Si deve caricare h2
        if (vh2>vhref);
            mh2=vhref/vh2;
            mh1=0;
        else;
            mh2=1;
            mh1=(vhref-vh2)/vh1;
        end;
    else;
        if (vh1>vhref);
            mh1=vhref/vh1;
            mh2=0;
        else
            mh1=1;
            mh2=(vhref-vh1)/vh2;
        end
    end
end

% Ramo inferiore

if (il>0); %I condensatori inferiori si scaricheranno
    if (vl1>vl2); %Si deve scaricare l1
        if (vl1>vlref);
            ml1=vlref/vl1;
            ml2=0;
        else;
            ml1=1;
            ml2=(vlref-vl1)/vl2;
        end;
    else;
        if (vl2>vlref);
            ml2=vlref/vl2;
            ml1=0;
        else;
            ml2=1;
            ml1=(vlref-vl2)/vl1;
        end;
    end;
```

```
else; %I condensatori inferiori si caricheranno
    if (vl1>vl2); %Si deve caricare l2
        if (vl2>vlref);
            ml2=vlref/vl2;
            ml1=0;
        else;
            ml2=1;
            ml1=(vlref-vl2)/vl1;
        end;
    else;
        if (vl1>vlref);
            ml1=vlref/vl1;
            ml2=0;
        else
            ml1=1;
            ml2=(vlref-vl1)/vl2;
        end
    end
end
```

The PWM modulator consists of four modulators, one for each module.

The block of the single arm with two upper modules and two lower modules is shown in Figure 5-96, where the right part is contained in the left part. The individual modules are made with elements of the Sim Power Systems library.

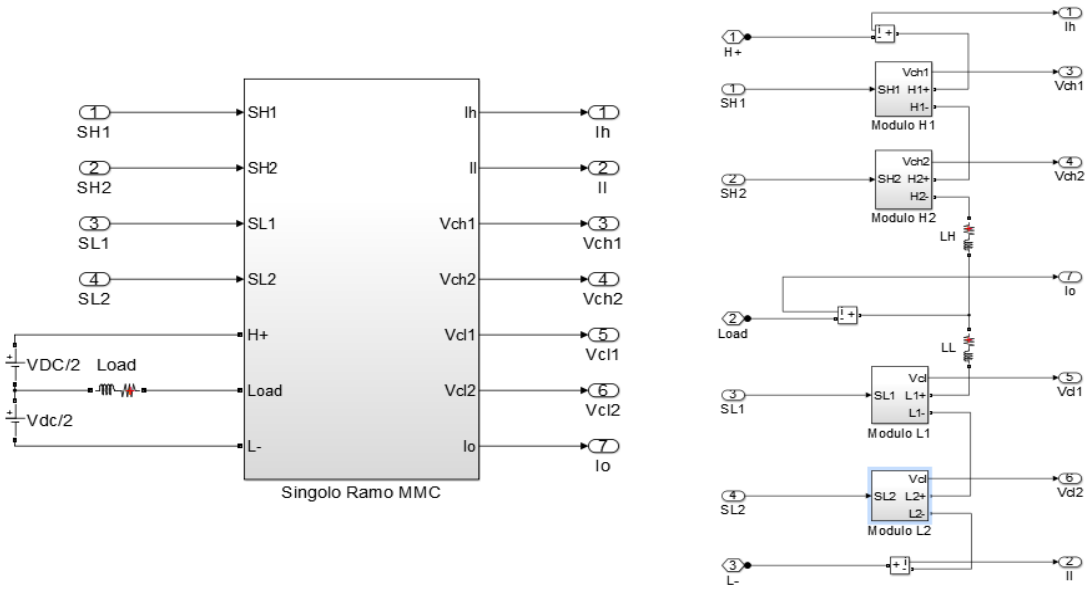


Figure 5-96 – Sim power system model of single leg MMC with two modules per arm.

The simulation was performed with the same parameters of the simulation of the unconstrained control with one module per arm as shown in Table 5-5.

DC voltage	24 [V]
Capacitors	880 [μF]
Capacitors reference voltage	24 [V]
Arm inductance	1.18 [mH]
Arm resistance	0.4 [Ω]
Load inductance	0.5 [mH]
Load resistence	1 [Ω]
Load current	2 [A]
Frequency	50 [Hz]

Table 5-5 – Simulation parameters.

5.2.20 Simulation results of the internal control loop for the management of the capacitors voltage levels

The current reference is properly followed from the very beginning, as can be seen in Figure 5-97.

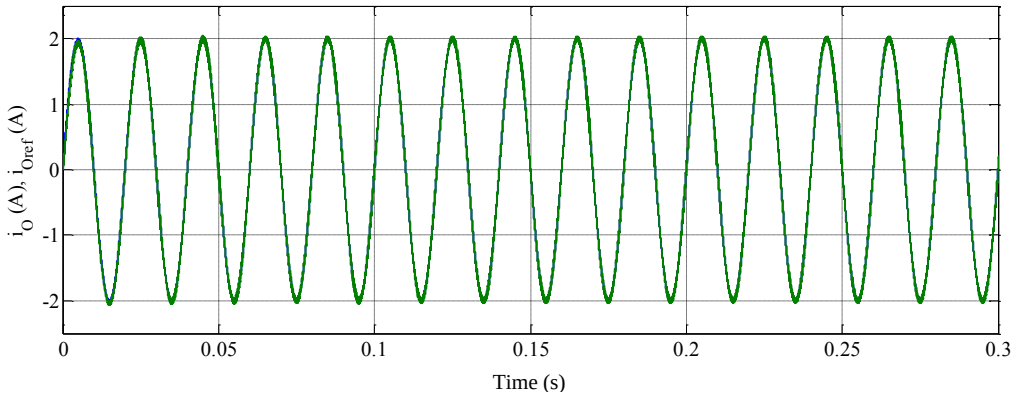


Figure 5-97 – Load current.

The voltages of the two capacitors in the upper arm present the same waveform, shown in Figure 5-98, and also the voltages of the capacitors of the lower arm have the same trend, shown in Figure 5-99. The voltage at the initial instant for each capacitor was set at 12 V.

After the initial transient operation, the average value of the voltage of all capacitors is 12 V and they oscillate around the mean value with an amplitude of 2 V.

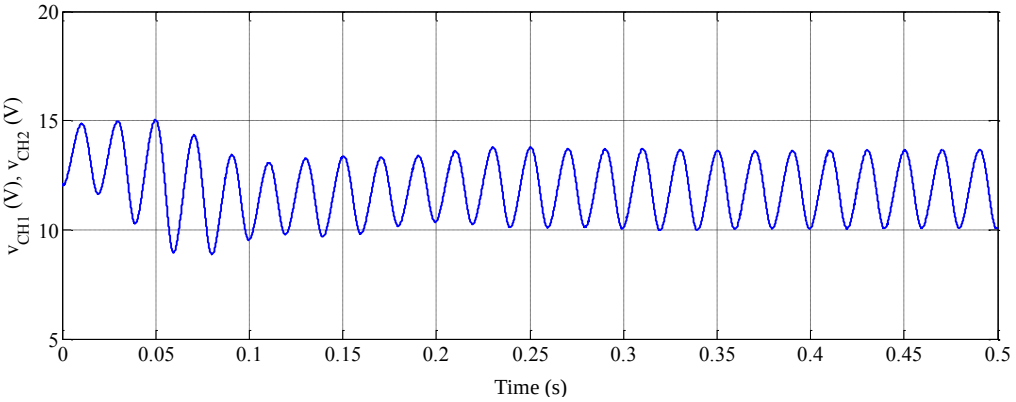


Figure 5-98 – Upper capacitors voltages.

The currents of the upper arm and the lower arm are shown respectively in Figure 5-100 and Figure 5-101. After a transient of about 250 ms the currents oscillate in phase opposition with an amplitude of 1 A, a frequency of 50 Hz and average value of - 0.1 A.

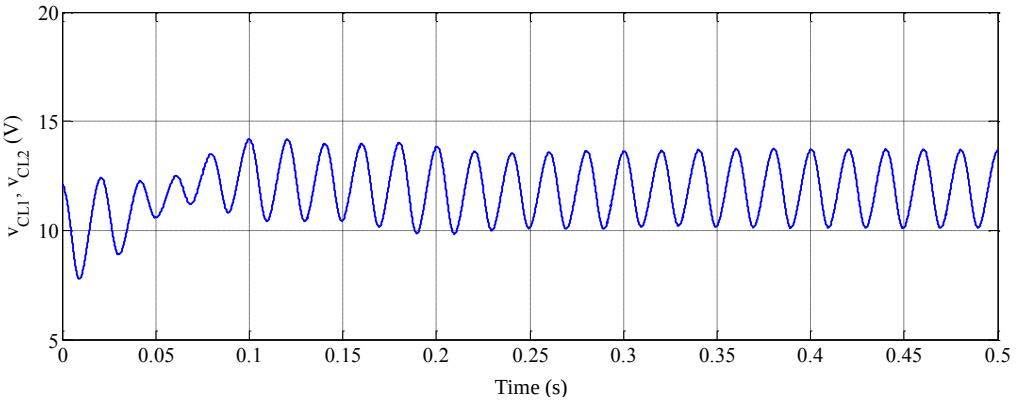


Figure 5-99 – Lower capacitors voltages.

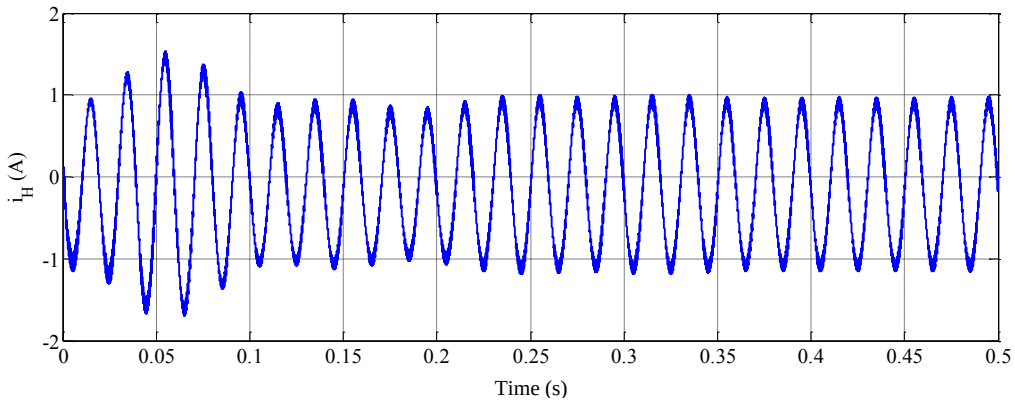


Figure 5-100 – Upper arm current.

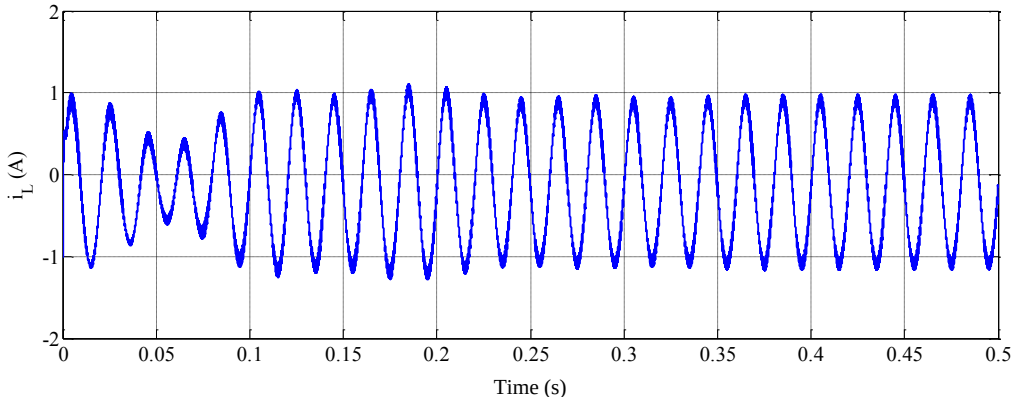


Figure 5-101 – Lower arm current.

The differential current has the trend displayed in Figure 5-102. After the initial transient assumes the average value of - 0.1 A.

The tracking of the total energy and the differential energy is correct and is shown respectively in Figure 5-103 and Figure 5-104. The reference total energy is approximately 0.25 J, the half of the case of a single equivalent module for each arm. In general, if *n* modules per arm are connected in series with capacitors having the same capacity and it is required that all modules have the same voltage, i.e. V_C/n, the total energy is the ratio between the energy of the case with one single equivalent module and *n*. So it is necessary to pay attention to properly modify the reference energy in the block of the unconstrained control, in order to obtain the desired average voltage for each capacitor.

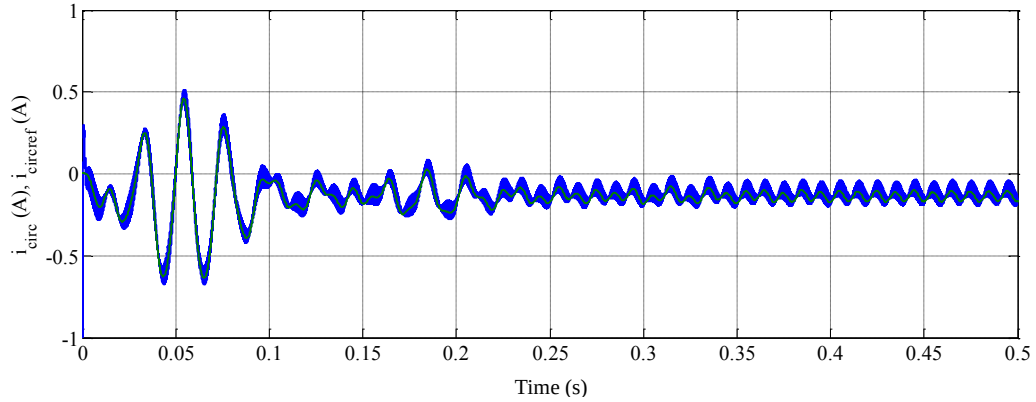


Figure 5-102 – Differential current.

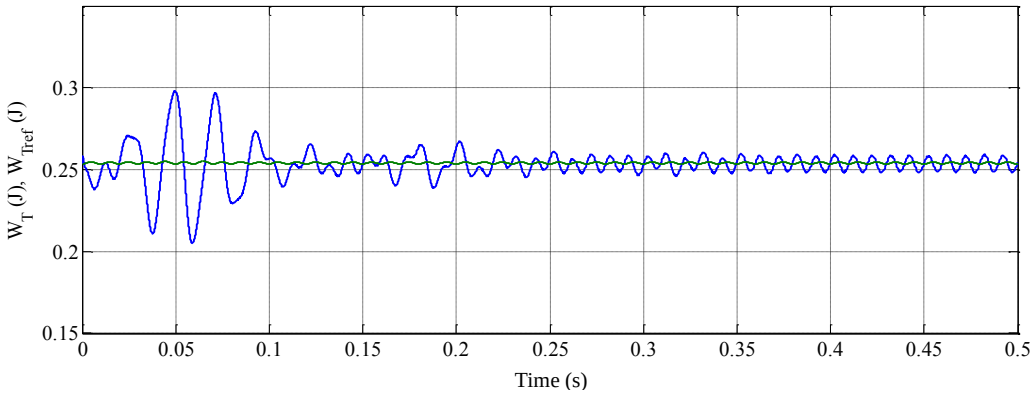


Figure 5-103 – Total energy.

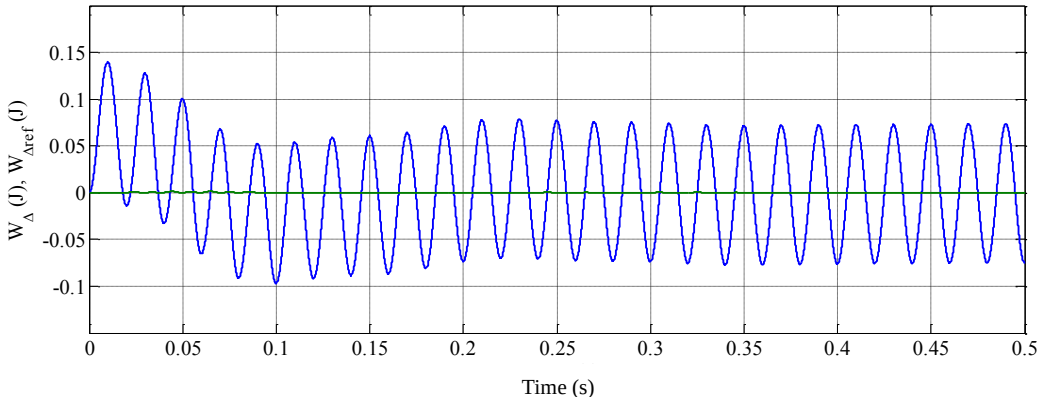


Figure 5-104 – Differential energy.

In Figure 5-105 and Figure 5-106 the waveforms of the modulating signals of the first upper module, called H_1, and the second upper module, called H_2 are represented. Comparing the two figures it can be seen that the balancing algorithm alternates in correspondence of almost all the

switching activation of the modules. When a module remains active for longer than a switching period, the other module remains inactive for the same periods.

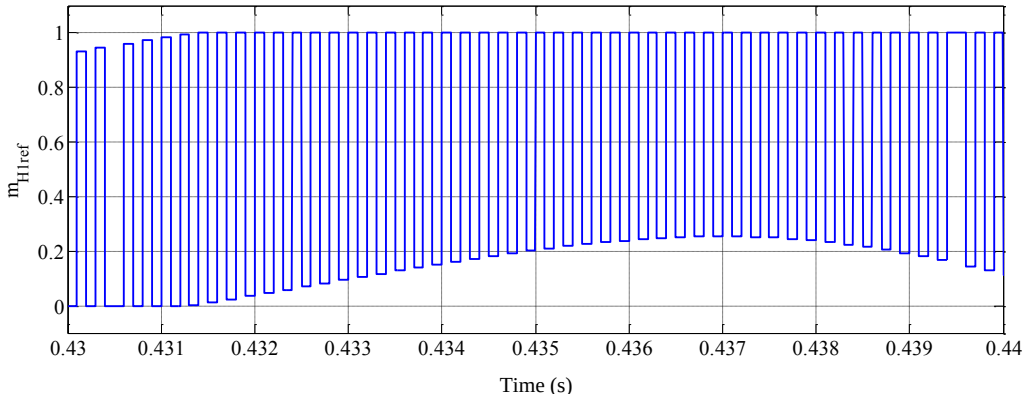


Figure 5-105 – Upper modulating signal.

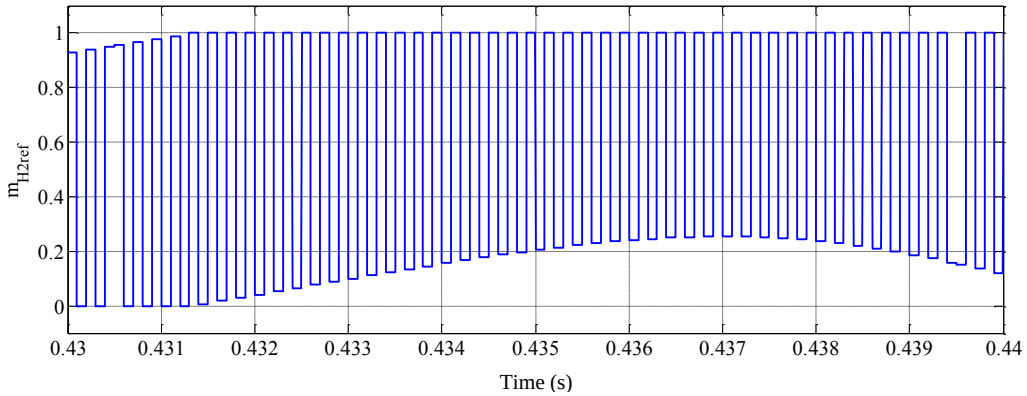


Figure 5-106 – Lower modulating signal.

5.3 Three Phase MMC

In this chapter the analysis on single leg MMC, performed in this chapter, will be extended to three-phase configuration.

In this section, the modelling and the control of MMC are restated in terms of space vectors, which may allow a deeper understanding of the inverter behavior. As a result, a control scheme for three-phase MMC based on the previous theoretical analysis is presented. In particular, this model allows identifying the main control variables that can be used to ensure the system stability. As a result, the control scheme of the three phase inverter is not the mere replication of three single-phase control schemes. On the contrary, the analysis of the inverter as a whole allows separating the different dynamics of the system. Numerical simulations are used to test the control scheme feasibility.

5.3.1 General description

The typical structure of a three-phase MMC is shown in Figure 5-107. Every leg of the inverter has two arms, each one consisting of *n* sub-modules. The typical configuration of a SM, as already discussed, is a simple dc/dc cell composed of two IGBT switches, two anti-parallel diodes and a capacitor. In each arm there is also a small inductor to compensate for the voltage difference between the upper and the lower arms produced when a SM is switched in or out.

The output voltage of each leg can be generated by combining the partial voltages of a suitable number of SMs. In general, there are several possible switching configurations that can be selected to obtain the desired output voltage, but among them only the ones that tend to keep the capacitor voltages balanced should be selected.

Equal voltage sharing among the capacitors of each arm can be achieved by the algorithm seen in previous section that selects the SMs to be inserted or bypassed during each sampling period of the control system.

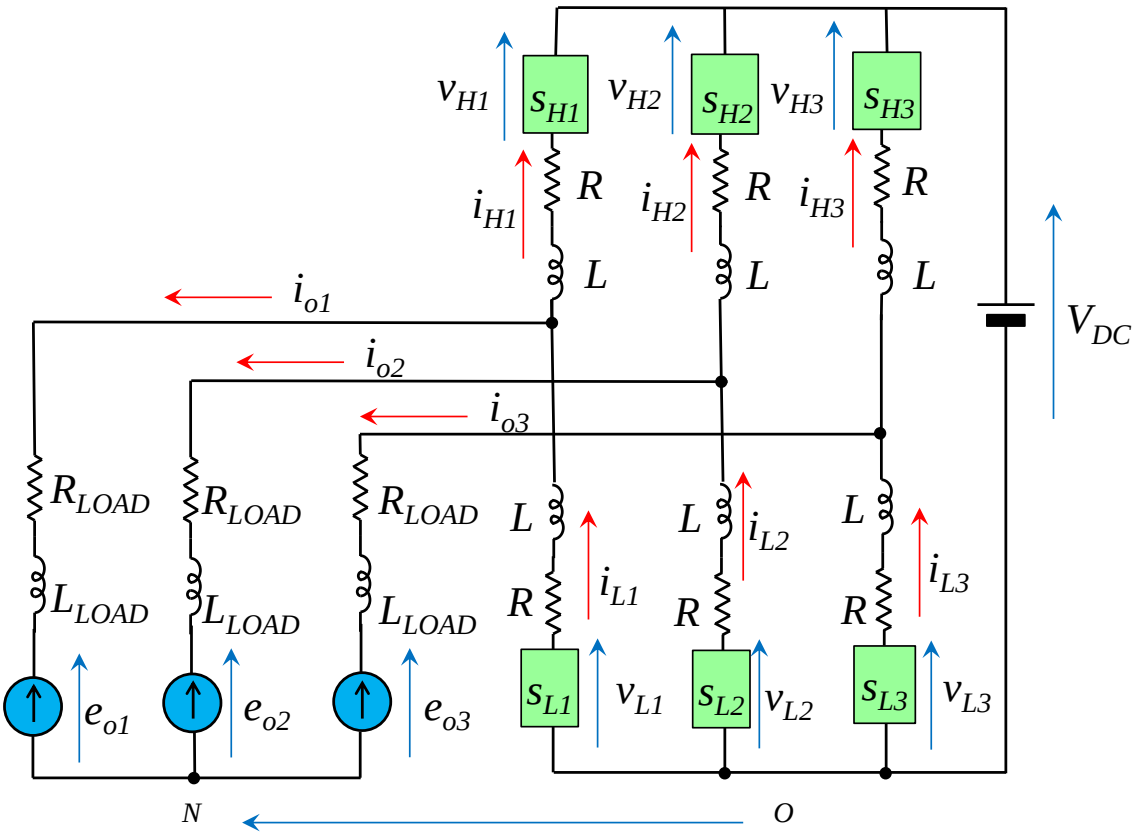


Figure 5-107 – Three-phase MMC

Although it is possible to consider the full representation of the MMC inverter, including the operation of each sub-module, this approach is complex and it is not simple to use the resulting model as a starting point for the development of more complex control schemes, in particular in three-phase case. If the lower level control ensures that all capacitors of the SMs of the same arm are equally charged then, it is possible to simplify, as usual, the scheme of an MMC, substituting all the SMs with two equivalent SMs.
The analysis is carried out under the hypothesis that the switching frequency is much higher than the frequency of the output voltages and currents, and that the resolution of the output voltage is very small compared to its amplitude owing to the high number of sub-modules.

5.3.2 Space Vector Transformation

Given three real quantities x_1, x_2 and x_3, the space vector transformation produces a space vector $\bar{x}$ and a zero-sequence component x_0, defined as follows:

$$\bar{x} = \frac{2}{3}\sum_{k=1}^{3} x_k e^{j\frac{2\pi}{3}(k-1)} \tag{5-133}$$

$$x_0 = \frac{1}{3}\sum_{k=1}^{3} x_k \tag{5-134}$$

The space vector transformation is invertible. In other words, the real quantities x_1, x_2 and x_3 can be determined by using the following relationships:

$$x_k = x_0 + \bar{x} \cdot e^{j\frac{2\pi}{3}(k-1)} \tag{5-135}$$

where "·" is the dot product, defined as the real part of the product of the first operand multiplied by the complex conjugate of the second.

5.3.3 Three-phase MMC equations

The output voltages of the modules are equal to the product between the capacitor voltage and the state of the module as follow:

$$v_{Hk} = s_{Hk} v_{Hk} \tag{5-136}$$

$$v_{Lk} = s_{Lk} v_{Lk} \tag{5-137}$$

where $k=1,2,3$ indicates the generic leg, s_{Hk} and s_{Lk} are the duty-cycles of the upper and lower arms and v_{Hk} and v_{Lk} are the capacitor voltages.
It is straightforward to verify that the capacitor voltages depend on the arm currents as follows:

$$C\frac{dv_{Hk}}{dt} = -s_{Hk}i_{Hk} \tag{5-138}$$

$$C\frac{dv_{Lk}}{dt} = -s_{Lk}i_{Lk} \tag{5-139}$$

With reference to the simplified circuit in Figure 5-107, by applying Kirchhoff's voltage law, as seen for the single leg MMC, it is possible to obtain the following equations:

$$V_c - v_{Hk} + L\frac{di_{Hk}}{dt} + Ri_{Hk} - v_{0k} = 0 \tag{5-140}$$

$$v_{Lk} - L\frac{di_{Lk}}{dt} - Ri_{Lk} - v_{0k} = 0 \tag{5-141}$$

$$v_{0k} - v_{N0} = e_{0k} + R_{LOAD}i_{0k} + L_{LOAD}\frac{di_{0k}}{dt} \tag{5-142}$$

where v_{ok} are the output voltages.
Introducing the definition of the internal voltage and the differential voltage and combining relations (5-140) and (5-141) it is possible to find the expressions for the leg k of three-phase MMC:

$$v_{\mathrm{int}k} = v_{0k} - \frac{V_c}{2} + \frac{R}{2}i_{0k} + \frac{L}{2}\frac{d}{dt}i_{0k} \tag{5-143}$$

$$v_{dk} = \frac{V_c}{2} + Ri_{dk} + L\frac{d}{dt}i_{dk} \tag{5-144}$$

Introducing relation (5-142) into (5-143):

$$v_{\mathrm{int}k} = e_{0k} - v_{N0} - \frac{V_c}{2} + R_{eq}i_{0k} + L_{eq}\frac{d}{dt}i_{0k} \tag{5-145}$$

By applying the transformation (5-133) and (5-134), and introducing (5-136) and (5-137) it is possible to calculate the space vectors and the zero-sequence components corresponding to the arm voltages v_{Hk} and v_{Lk}:

$$\bar{v}_H = \frac{2}{3}\sum_{k=1}^{3} v_{Hk}e^{j\frac{2\pi}{3}(k-1)} = \frac{2}{3}\sum_{k=1}^{3} s_{Hk}v_{CHk}e^{j\frac{2\pi}{3}(k-1)} \tag{5-146}$$

$$v_{H0} = \frac{1}{3}\sum_{k=1}^{3} v_{Hk} = \frac{1}{3}\sum_{k=1}^{3} s_{Hk} v_{CHk} \tag{5-147}$$

$$\bar{v}_L = \frac{2}{3}\sum_{k=1}^{3} v_{Lk} e^{j\frac{2\pi}{3}(k-1)} = \frac{2}{3}\sum_{k=1}^{3} s_{Lk} v_{CLk} e^{j\frac{2\pi}{3}(k-1)} \tag{5-148}$$

$$v_{L0} = \frac{1}{3}\sum_{k=1}^{3} v_{Lk} = \frac{1}{3}\sum_{k=1}^{3} s_{Lk} v_{CLk} \tag{5-149}$$

It is possible to combine (5-146) and (5-148) to find the expressions of the internal voltage space vector and differential voltage space vector:

$$\bar{v}_{\text{int}} = \frac{\bar{v}_L - \bar{v}_H}{2} \tag{5-150}$$

$$\bar{v}_d = \frac{\bar{v}_L + \bar{v}_H}{2} \tag{5-151}$$

The output currents can be written as sums of the upper and lower arm currents. The corresponding space-vector equations are as follows:

$$\bar{i}_0 = \bar{i}_L - \bar{i}_H \tag{5-152}$$

$$\bar{i}_d = \frac{\bar{i}_L + \bar{i}_H}{2} \tag{5-153}$$

where $\bar{i}_0$ and $\bar{i}_d$ are the space vectors of the arm currents i_{0k} and i_{dk}.

By applying the same transformations to equations (5-145) and (5-144) and considering the previous definitions it is possible to find:

$$\bar{v}_{\text{int}} = \bar{e}_0 + R_{eq}\bar{i}_0 + L_{eq}\frac{d\bar{i}_0}{dt} \tag{5-154}$$

$$\bar{v}_d = R\bar{i}_d + L\frac{d\bar{i}_d}{dt} \tag{5-155}$$

The same analysis can be done for the zero sequence to find the zero sequences of internal voltage and differential voltage:

$$v_{\text{int}0} = \frac{v_{L0} - v_{H0}}{2} \tag{5-156}$$

$$v_{d0} = \frac{v_{L0} + v_{H0}}{2} \tag{5-157}$$

The zero sequences for the load current and for the differential current are:

$$i_{00} = i_{L0} - i_{H0} = 0 \Rightarrow i_{L0} = i_{H0} \tag{5-158}$$

$$i_{d0} = \frac{i_{L0} + i_{H0}}{2} \Rightarrow i_{d0} = i_{L0} = i_{H0} \tag{5-159}$$

where i_{00} is equal to zero due to the star connection of the load

The zero sequences for equations (5-145) and (5-144) are:

$$v_{\text{int}0} = v_{N0} + e_{00} - \frac{V_C}{2} \tag{5-160}$$

$$v_{d0} = \frac{V_C}{2} + Ri_{d0} + L\frac{di_{d0}}{dt} \tag{5-161}$$

$\bar{v}_{INT}$, $\bar{v}_0$, $v_{int,0}$ and v_{d0} are key variables to control the load currents and differential currents.

The dc-link current i_{DC} can be written as sum of the arm currents:

$$i_{DC} = \sum_{k=1}^{3} i_{Hk} = \sum_{k=1}^{3} i_{Lk} \tag{5-162}$$

and consequently the zero-sequence currents i_{H0} and i_{L0} in (5-159) are proportional to i_{DC}:

$$i_{H0} = \frac{1}{3} i_{DC} \tag{5-163}$$

$$i_{L0} = \frac{1}{3} i_{DC} \tag{5-164}$$

Considering equation (5-159) it is possible to substitute the DC current expression finding the following equation for the dc-link current:

$$\frac{1}{3} Ri_{DC} + \frac{1}{3} L\frac{di_{DC}}{dt} = v_{d0} - V_C \tag{5-165}$$

Equation (5-165) shows that the zero-sequence component of the differential voltage plays a fundamental role in controlling the input DC current.

5.3.4 Control of three-phase MMC – Unconstrained approach

In practical applications, the aim of the control system is to ensure that the load current vector $\bar{i}_O$ tracks a circular trajectory $\bar{i}_{O,ref}$. Another task of the control system is to keep the voltages of the capacitors of the upper and lower arms almost constant and below a suitable safety threshold.
The solution to achieve these three goals is not trivial, since the control system has at disposal only the modulation indexes m_{Hk} and m_{Lk} (k=1,2,3) as control variables.
If the reference values for $\bar{i}_d$ and i_{d0} are known, it is possible to calculate the reference values of $\bar{i}_H$, $\bar{i}_L$, i_{H0} and i_{L0}.
However, the choice of the current set-points $\bar{i}_{d,ref}$ and $i_{d0,ref}$ is not straightforward. A well-known method is based on the calculation of the energies in the upper and lower arms, W_{CHk} and W_{CLk}.

$$W_{CHk} = \frac{1}{2} C v_{Hk}^2 \tag{5-166}$$

$$W_{CLk} = \frac{1}{2} C v_{Lk}^2 \tag{5-167}$$

By adding equations (5-166) and (5-167) for each phase it is possible to find the expression of the total energy stored into the capacitors of the leg:

$$\frac{dW_{CT1}}{dt} = -2v_{d1}i_{d1} - v_{\text{int}1}i_{01} \tag{5-168}$$

$$\frac{dW_{CT2}}{dt} = -2v_{d2}i_{d2} - v_{\text{int}2}i_{02} \tag{5-169}$$

$$\frac{dW_{CT3}}{dt} = -2v_{d3}i_{d3} - v_{\text{int}3}i_{03} \tag{5-170}$$

By subtracting equations (5-166) and (5-167) it is possible to find for each phase the expression of the differential energy stored into the capacitors of the leg:

$$\frac{dW_{C\Delta1}}{dt} = v_{d1}i_{01} + 2v_{\text{int}1}i_{d1} \tag{5-171}$$

$$\frac{dW_{C\Delta2}}{dt} = v_{d2}i_{02} + 2v_{\text{int}2}i_{d2} \tag{5-172}$$

$$\frac{dW_{C\Delta 3}}{dt} = v_{d3} i_{03} + 2v_{\text{int}3} i_{d3} \tag{5-173}$$

By applying the space vector transformation to W_{CHk} and W_{CLk}, it is possible to define the space vector of the upper arm energies, $\overline{W}_{CH}$, and of the lower arm energies, $\overline{W}_{CL}$, and the corresponding zero-sequence components, W_{CH0} and W_{CL0}. It is worth noting that the zero-sequence components represent the mean total energy stored in the upper or in the lower capacitors.

Then, the total and unbalance energy space vectors $\overline{W}_{CT}$, $\overline{W}_{C\Delta}$ and the zero-sequence components W_{CT0}, $W_{C\Delta 0}$ can be defined as follows:

$$\overline{W}_{CT} = \overline{W}_{CH} + \overline{W}_{CL} \tag{5-174}$$

$$W_{CT0} = W_{CH0} + W_{CL0} \tag{5-175}$$

$$\overline{W}_{C\Delta} = \overline{W}_{CH} - \overline{W}_{CL} \tag{5-176}$$

$$W_{C\Delta 0} = W_{CH0} - W_{CL0} \tag{5-177}$$

It can be verified that W_{CT0} represents the total energy stored into the capacitors of the inverter, whereas $W_{C\Delta 0}$ represents the energy unbalance between the upper and the lower arm capacitors.

It is possible to calculate the following time derivatives:

$$\frac{d\overline{W}_{CT}}{dt} = -2v_{d0}\bar{i}_d - 2\bar{v}_d i_{d0} - \bar{v}_d^* \bar{i}_d^* - v_{\text{int}0}\bar{i}_0 - \bar{v}_{\text{int}} i_{00} - \frac{1}{2}\bar{v}_{\text{int}}^* \bar{i}_0^* \tag{5-178}$$

$$\frac{dW_{CT0}}{dt} = -\bar{v}_d \cdot \bar{i}_d - 2v_{d0} i_{d0} - \frac{1}{2}\bar{v}_{\text{int}} \cdot \bar{i}_0 - v_{\text{int}0} i_{00} \tag{5-179}$$

$$\frac{d\overline{W}_{C\Delta}}{dt} = v_{d0}\bar{i}_0 + \bar{v}_d i_{00} + \frac{1}{2}\bar{v}_d^* \bar{i}_0^* + 2v_{\text{int}0}\bar{i}_d + 2\bar{v}_{\text{int}} i_{d0} + \bar{v}_{\text{int}}^* \bar{i}_d^* \tag{5-180}$$

$$\frac{dW_{C\Delta 0}}{dt} = \frac{1}{2}\bar{v}_d \cdot \bar{i}_0 + v_{d0} i_{00} + \bar{v}_{\text{int}} \cdot \bar{i}_d + 2v_{\text{int}0} i_{d0} \tag{5-181}$$

On the basis of (5-178), (5-179), (5-180) and (5-181) it is possible to define a stable control strategy for three-phase MMC. First of all, it is supposed that v_{int0} is controlled in such a way that it is equal to *0* (as it is possible to understand in equation (5-160)), while the zero component of the load current is *0* due to the star connection of the load. For these reasons the terms in the previous equations that are proportional to these two quantities vanish:

$$\frac{d\overline{W}_{CT}}{dt} = -2v_{d0}\bar{i}_d - 2\bar{v}_d i_{d0} - \bar{v}_d^*\bar{i}_d^* - \frac{1}{2}\bar{v}_{\text{int}}^*\bar{i}_0^* \tag{5-182}$$

$$\frac{dW_{CT0}}{dt} = -\bar{v}_d \cdot \bar{i}_d - 2v_{d0}i_{d0} - \frac{1}{2}\bar{v}_{\text{int}} \cdot \bar{i}_0 \tag{5-183}$$

$$\frac{d\overline{W}_{C\Delta}}{dt} = v_{d0}\bar{i}_0 + \frac{1}{2}\bar{v}_d^*\bar{i}_0^* + 2\bar{v}_{\text{int}}i_{d0} + \bar{v}_{\text{int}}^*\bar{i}_d^* \tag{5-184}$$

$$\frac{dW_{C\Delta 0}}{dt} = \frac{1}{2}\bar{v}_d \cdot \bar{i}_0 + \bar{v}_{\text{int}} \cdot \bar{i}_d \tag{5-185}$$

Let's assume that $\bar{i}_d$ and i_{d0} can be written as the sum of a low frequency component, whose bandwidth is much lower than the output angular frequency ω, and a component at frequency ω:

$$\bar{i}_d = \bar{i}_d^{LF} + \bar{I}_d^{HF}e^{j\omega t} \tag{5-186}$$

$$i_{d0} = i_{d0}^{LF} + \text{Re}\left[\bar{I}_{d0}^{HF}e^{-j\omega t}\right] \tag{5-187}$$

As in single leg analysis it is convenient to integrate equations (5-182)-(5-185) over a period of the output voltage. The variations of the inverter energies between the end and the beginning of a period of the output voltage can be approximately written as follows:

$$\begin{aligned}\Delta\overline{W}_{CT} = &-2\int v_{d0}^{LF}\bar{i}_d^{LF}dt - \int \overline{V}_{d0}^{HF}\bar{I}_d^{HF}dt - 2\int \bar{v}_d^{LF}i_{d0}^{LF}dt - \int \overline{V}_d^{HF}\bar{I}_{d0}^{HF}dt - \int \bar{v}_d^{*LF}\bar{i}_d^{*LF}dt - \\ &- \frac{1}{2}\int \bar{v}_{\text{int}}^{*LF}\bar{i}_0^{*LF}dt\end{aligned} \tag{5-188}$$

$$\begin{aligned}\Delta W_{CT0} = &-\int \bar{v}_d^{LF} \cdot \bar{i}_d^{LF}dt - \int \Re\{\overline{V}_d^{HF}\bar{I}_d^{*HF}\}dt - 2\int v_{d0}^{LF}i_{d0}^{LF}dt - \int \Re\{\overline{V}_{d0}^{HF}\bar{I}_{d0}^{*HF}\}dt - \\ &- \frac{1}{2}\int \bar{v}_{\text{int}}^{LF} \cdot \bar{i}_0^{LF}dt - \frac{1}{2}\int \Re\{\overline{V}_{\text{int}}^{HF}\bar{I}_0^{*HF}\}dt\end{aligned} \tag{5-189}$$

$$\begin{aligned}\Delta\overline{W}_{C\Delta} = &\int v_{d0}^{LF}\bar{i}_0^{LF}dt + \frac{1}{2}\int \overline{V}_{d0}^{HF}\bar{I}_0^{HF}dt + \frac{1}{2}\int \bar{v}_d^{*LF}\bar{i}_0^{*LF}dt + 2\int \bar{v}_{\text{int}}^{LF}i_{d0}^{LF}dt + \\ &+ \int \overline{V}_{\text{int}}^{HF}\bar{I}_{d0}^{HF}dt + \int \bar{v}_{\text{int}}^{*LF}\bar{i}_d^{*LF}dt\end{aligned} \tag{5-190}$$

$$\Delta W_{C\Delta 0} = \frac{1}{2}\int \bar{v}_d^{LF} \cdot \bar{i}_0^{LF}dt + \frac{1}{2}\int \Re\{\overline{V}_d^{HF}\bar{I}_0^{*HF}\}dt + \int \bar{v}_{\text{int}}^{LF} \cdot \bar{i}_d^{LF}dt + \int \Re\{\overline{V}_{\text{int}}^{HF}\bar{I}_d^{*HF}\}dt \tag{5-191}$$

Equations (5-188)-(5-191) show that the variations of energy variables can be controlled independently of each other by adjusting the low-frequency and high-frequency components of the

currents $\bar{i}_d$ and i_{d0}. In particular, it can be noted that the low-frequency components of $\bar{i}_d$ and i_{d0} can be used to control the mean value of the total energies $\overline{W}_{CT}$ and W_{T0}, whereas the harmonic component of $\bar{i}_d$ at the output frequency can be used to control the energy unbalance $W_{\Delta 0}$. The harmonic component of i_{d0} can be used to control the space vector of the differential energy $\Delta\overline{W}_{C\Delta}$. These results can be summarized as follows:

$$\bar{i}_d^{LF} \rightarrow \overline{W}_{CT} \tag{5-192}$$

$$i_{do}^{LF} \rightarrow W_{CT0} \tag{5-193}$$

$$\bar{I}_{do}^{HF} \rightarrow \overline{W}_{C\Delta} \tag{5-194}$$

$$\bar{I}_d^{HF} \rightarrow W_{C\Delta 0} \tag{5-195}$$

Equations (5-192)-(5-195) highlight the correlation between the energies that is necessary to control to keep balanced the system capacitors and the variables that the control can modify to this purpose. All the other contributes in equations (5-188)-(5-191) are not controllable and can be considered as disturbance effects. To reduce their influence it is possible to tune the regulators with a sufficient gain or to pre-compensate them.

5.3.5 Simulation model of three-phase MMC – Unconstrained approach

To control a three-phase MMC with unconstrained approach it is necessary to create a reference load current space vector by transforming three reference currents with a phase displacement of $2\pi/3$.

There are six capacitors in the three legs of the inverter, that should be controlled. The total energy and the differential energy of the three individual legs can be transformed with the space vector approach seen in previous section instead of being controlled independently one from the each other. This way there are four quantities to control, two of them are vectors and can be decoupled into two orthogonal axis. This way there are six energy regulators in total.

For the voltages a similar approach can be followed. It is possible to realize a control by space vectors that requires five regulators, given that if the load is star connected, the zero-sequence component of the load current is zero and there is no need to control it with an additional regulator.

The overall block diagram of the control, is represented in Figure 5-108. The three phases are named with numbers *1*, *2* and *3*.

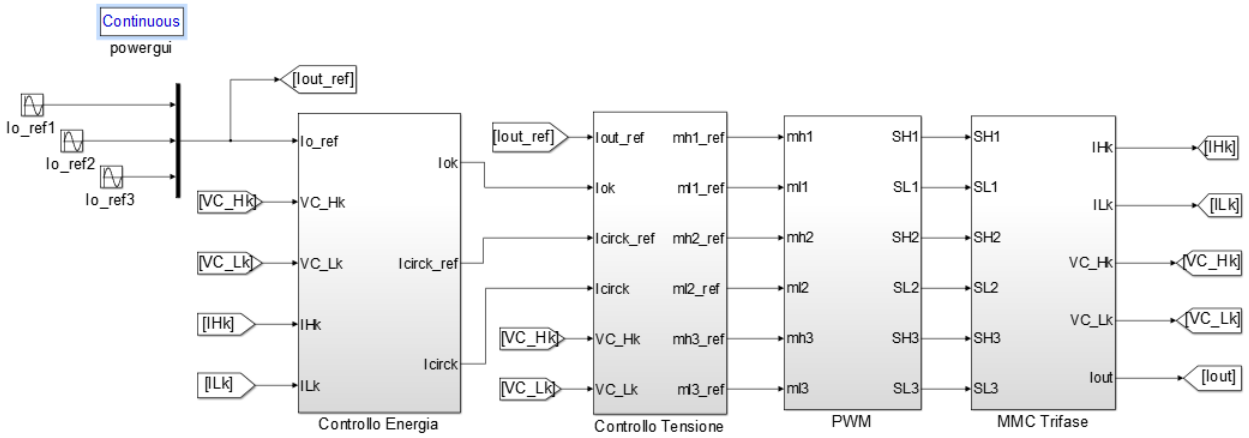


Figure 5-108 – Simulink general model of three-phase MMC.

The block that controls the energy of the legs and generates the references of the circulating currents is presented in Figure 5-109. The control blocks of the space vectors and zero sequences of the total and differential energies are shown.

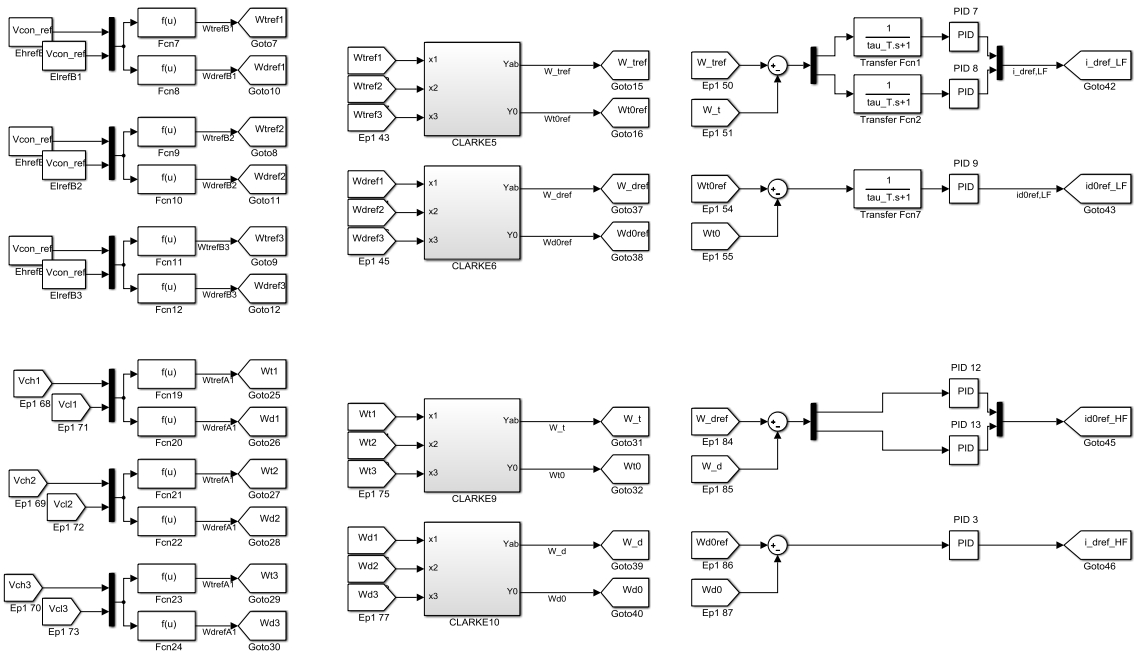


Figure 5-109 – Control scheme energy loop of the three-phase MMC.

The control block of the current loops are shown in Figure 5-110. It is realized, as already discussed, via space vectors. The internal blocks generate the reference modulating signals based on the load and differential current errors.

The block of the control voltage is based on the transformations between phase variables and space vectors written in previous section and realized in simulation as shown in Figure 5-111. The block of inverse transformation is shown in Figure 5-112 instead.

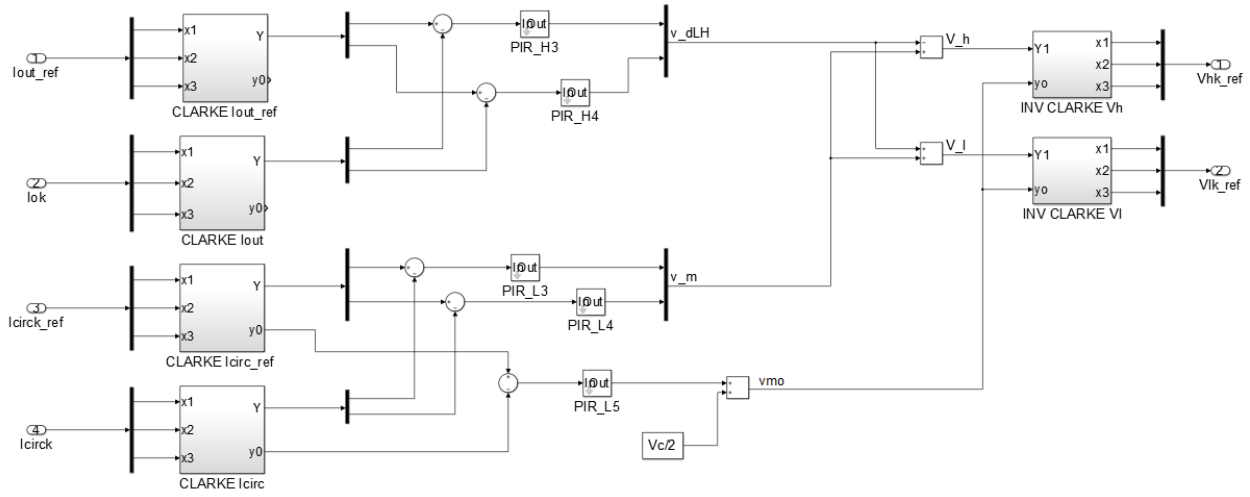


Figure 5-110 – Control scheme current loop of the three-phase MMC.

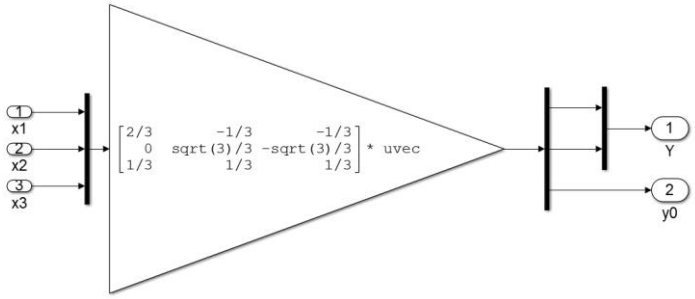


Figure 5-111 – Clarke transformation.

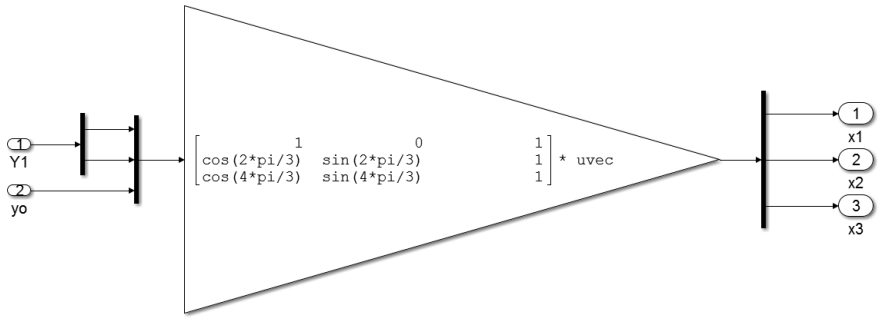


Figure 5-112 – Clarke anti-transformation.

The block that contains the model of the inverter can be realized with library components Sim Power Systems, as shown in Figure 5-113. The three legs are equal to each other and coincide with the model seen in the single leg MMC.

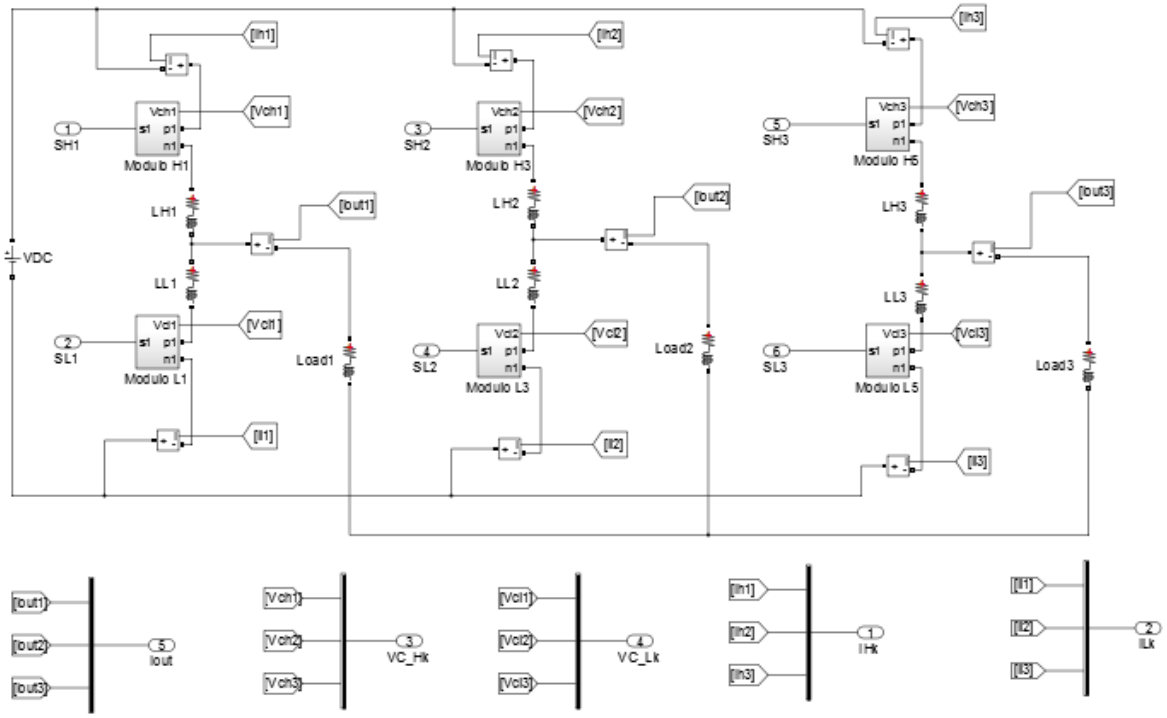


Figure 5-113 – Sim power system model of three-phase MMC.

In Table 5-6 the simulation parameters are listed. It is possible to see that the parameters are the same of the single phase case.

DC voltage	24 [V]
Capacitors	880 [μF]
Capacitors reference voltage	24 [V]
Arm inductance	1.18 [mH]
Arm resistance	0.4 [Ω]
Load inductance	0.5 [mH]
Load resistence	1 [Ω]
Load current	2 [A]
Frequency	50 [Hz]

Table 5-6 – Simulation parameters.

5.3.6 Simulation results of three-phase MMC – Unconstrained approach

The amplitude of the reference current load is the same for the three phases and the three currents have a phase displacement of 2π/3. The references are tracked correctly right from the start, as shown in Figure 5-114.

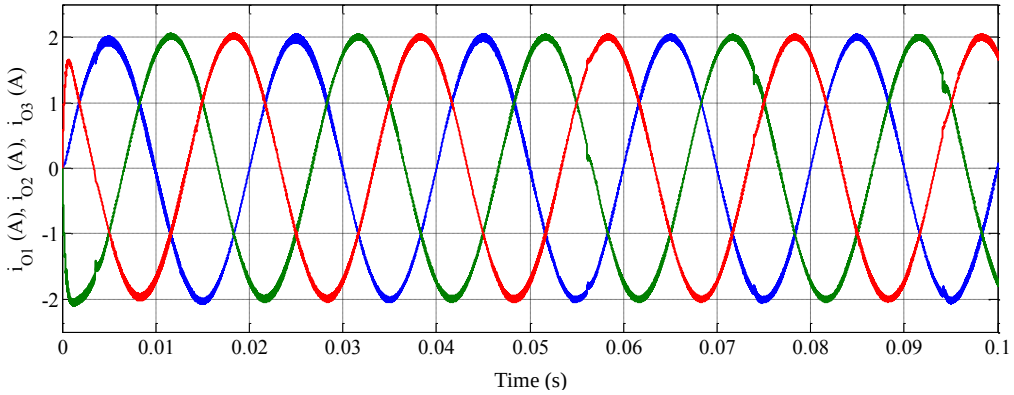


Figure 5-114 – Load currents.

The tracking can also be evaluated in terms of space vectors, as shown in Figure 5-115. In this figure, the curve starts from the origin, performs the initial transient and tracks a circumference in steady state, while the thickness of the circumference coincides with the ripple.

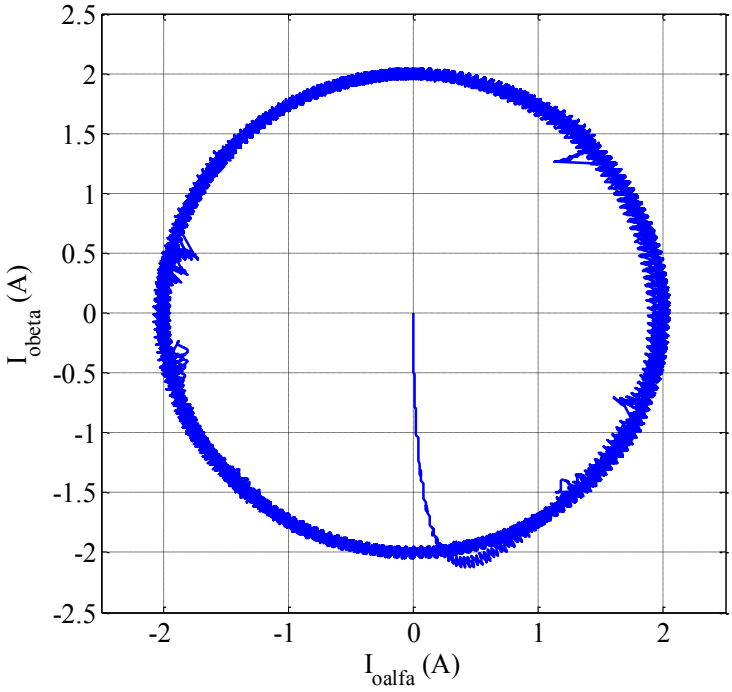


Figure 5-115 – Load currents space vector.

The capacitor voltages of the upper and lower modules respectively are shown in Figure 5-116 and Figure 5-117. All waveforms take about 250 ms to go in steady state. Considering only the capacitors of the upper modules, or only those of the lower modules, it is possible to observe a phase displacement of $2\pi/3$ between the waveforms of voltage. In steady state operation all the voltages oscillate around 24 V, with an amplitude of 2 V.

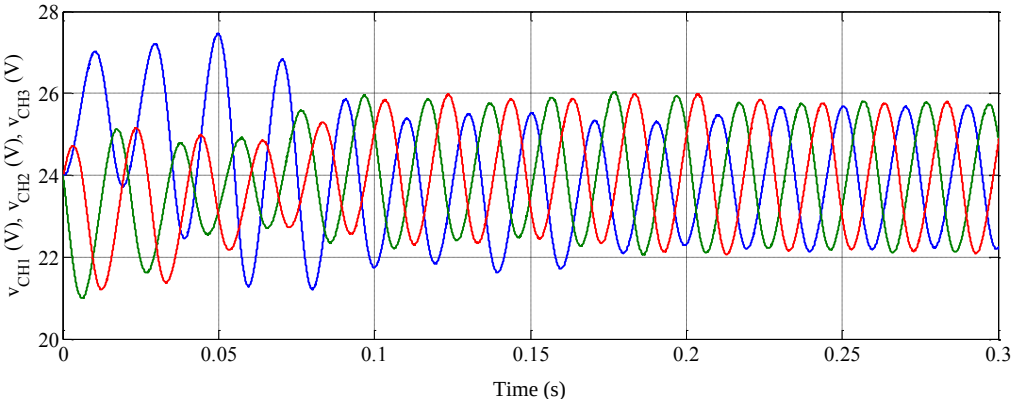


Figure 5-116 – Upper capacitor voltages.

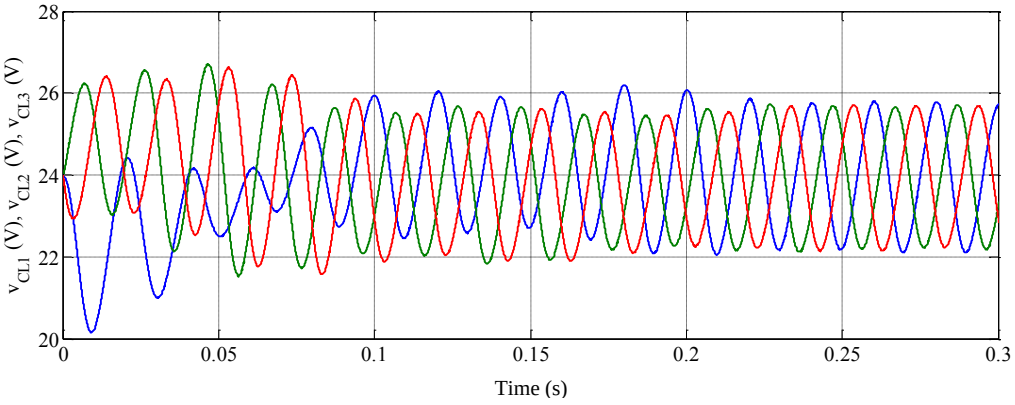


Figure 5-117 – Lower capacitor voltages.

The currents of the upper and lower branches are represented respectively in Figure 5-118 and Figure 5-119. As for the voltages of the capacitors, there is a phase displacement of $2\pi/3$ and they take 250 ms to reach steady state condition. When they are in steady state the amplitude is 1 A and the frequency 50 Hz.

The differential current has the same trend in the three phases and each one has a mean value of -0.1 A. In Figure 5-120 it is shown as example the current in the first phase.

The reference signals of total and differential energy, are tracked correctly in all the three phases and in Figure 5-121 and Figure 5-122 are shown as example the waveforms of phase 1.

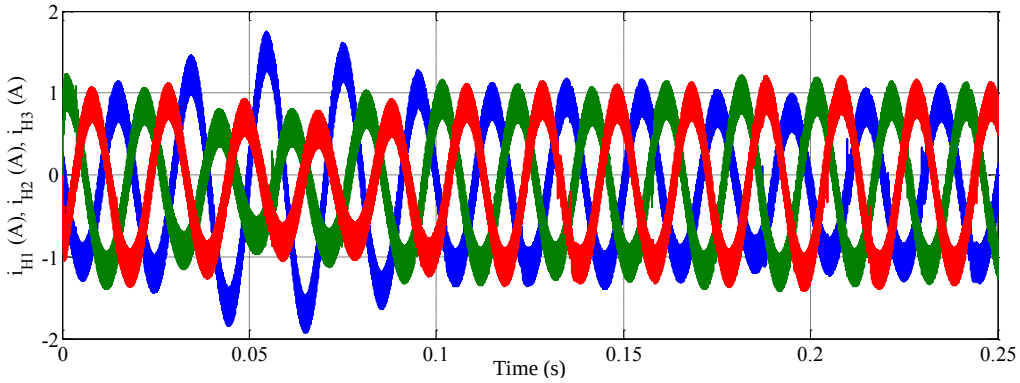


Figure 5-118 – Upper arm currents.

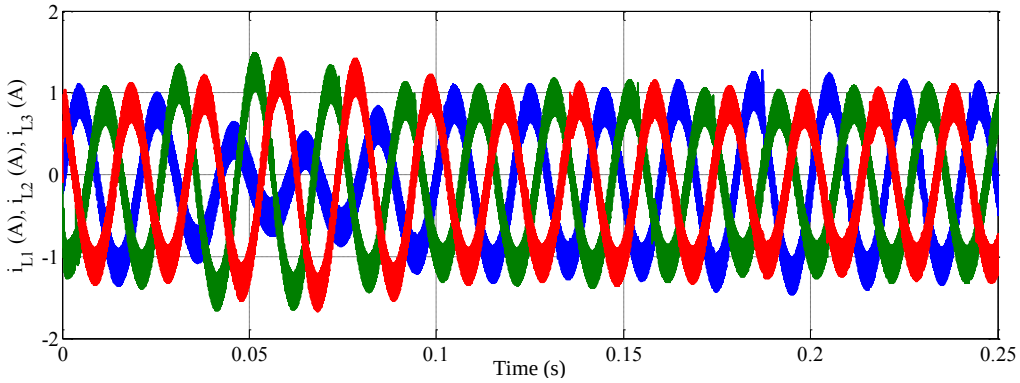


Figure 5-119 – Lower arm currents.

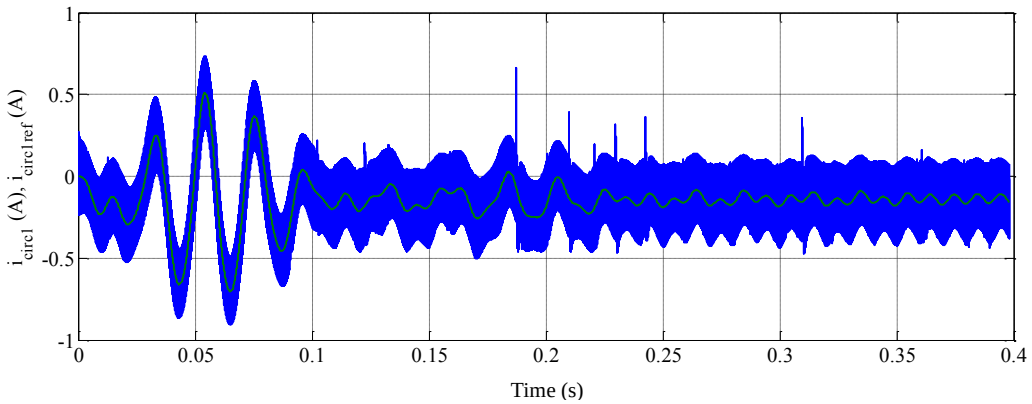


Figure 5-120 – Differential current of one leg.

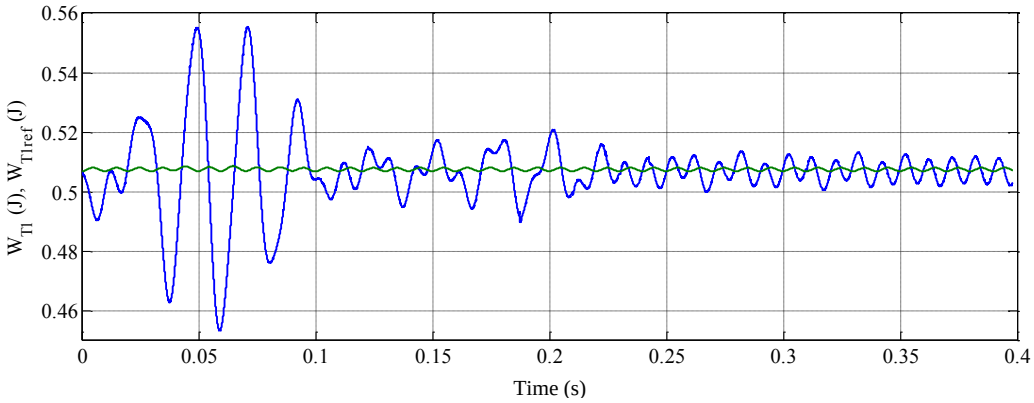


Figure 5-121 – Total energy of one leg.

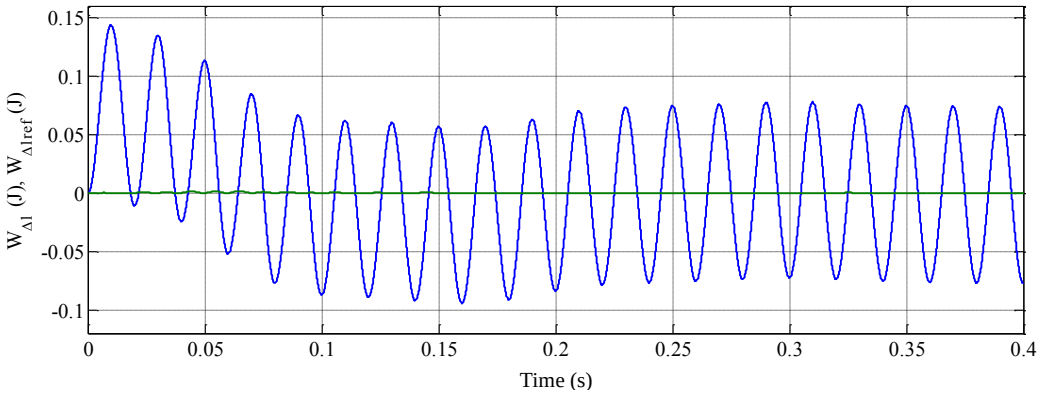


Figure 5-122 – Differential energy of one leg.

5.4 Back to back MMC

The structure and the control of the back to back MMC configuration is analyzed in this section.Figure 5-123As shown in Figure 5-123, the two inverters connect two different three-phase AC systems with different voltage and frequency, for example a generic R-L-E load can be connected to inverter B, while inverter A is connected to the grid. One of the main application of this configuration, and in general for the MMC, is HVDC for offshore wind farms.

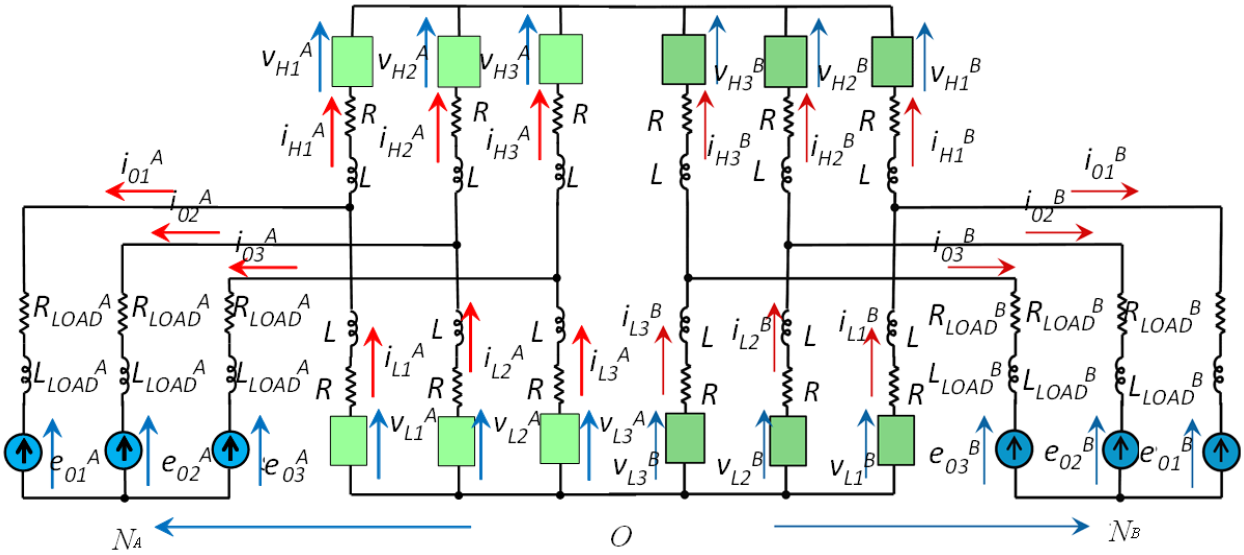


Figure 5-123 –Back to Back MMC.

5.4.1 Control of back to back MMC

As seen in the previous section, considering inverter A and applying the space vector transformations, it is possible to obtain four equations:

$$\bar{v}_{\text{int}}^{A} = \bar{e}_{0}^{A} + R_{eq}\bar{i}_{0}^{A} + L_{eq}\frac{d\bar{i}_{0}^{A}}{dt} \tag{5-196}$$

$$v_{\text{int}0}^{A} = v_{N0}^{A} + e_{00}^{A} - \frac{v_{dc}}{2} \tag{5-197}$$

$$\bar{v}_{d}^{A} = R\bar{i}_{d}^{A} + L\frac{d\bar{i}_{d}^{A}}{dt} \tag{5-198}$$

$$v_{d0}^{A} = \frac{v_{dc}}{2} + Ri_{d0}^{A} + L\frac{di_{d0}^{A}}{dt} \tag{5-199}$$

It is possible to see that the zero sequence of the load current is zero due to the star connection of the load.

The total and differential energy relations for inverter A, in terms of space vectors and zero sequence, are:

$$\frac{d\overline{W}_{CT}^{A}}{dt} = -2v_{d0}^{A}\bar{i}_{d}^{A} - 2\bar{v}_{d}^{A}i_{d0}^{A} - \bar{v}_{d}^{*A}\bar{i}_{d}^{*A} - \frac{1}{2}\bar{v}_{\text{int}}^{*A}\bar{i}_{0}^{*A} \tag{5-200}$$

$$\frac{dW_{CT0}^{A}}{dt} = -\bar{v}_{d}^{A} \cdot \bar{i}_{d}^{A} - 2v_{d0}^{A} i_{d0}^{A} - \frac{1}{2}\bar{v}_{\text{int}}^{A} \cdot \bar{i}_{0}^{A} \tag{5-201}$$

$$\frac{d\overline{W}_{C\Delta}^{A}}{dt} = v_{do}^{A}\bar{i}_{0}^{A} + \frac{1}{2}\bar{v}_{d}^{*A}\bar{i}_{0}^{*A} + 2\bar{v}_{\text{int}}^{A} i_{d0}^{A} + \bar{v}_{\text{int}}^{*A}\bar{i}_{d}^{*A} \tag{5-202}$$

$$\frac{dW_{\Delta 0}^{A}}{dt} = \frac{1}{2}\bar{v}_{d}^{A} \cdot \bar{i}_{0}^{A} + \bar{v}_{\text{int}}^{A} \cdot \bar{i}_{d}^{A} \tag{5-203}$$

For inverter B similar equations can be written:

$$\bar{v}_{\text{int}}^{B} = \bar{e}_{0}^{B} + R_{eq}\bar{i}_{0}^{B} + L_{eq}\frac{d\bar{i}_{0}^{B}}{dt} \tag{5-204}$$

$$v_{\text{int},o}^{B} = v_{N0}^{B} + e_{00}^{B} - \frac{v_{dc}}{2} \tag{5-205}$$

$$\bar{v}_{d}^{B} = R\bar{i}_{d}^{B} + L\frac{d\bar{i}_{d}^{B}}{dt} \tag{5-206}$$

$$v_{d0}^{B} = \frac{v_{dc}}{2} + Ri_{d0}^{B} + L\frac{di_{d0}^{B}}{dt} \tag{5-207}$$

The energy relations for inverter B are:

$$\frac{d\overline{W}_{CT}^{B}}{dt} = -2v_{d0}^{B}\bar{i}_{d}^{B} - 2\bar{v}_{d}^{B} i_{d0}^{B} - \bar{v}_{d}^{*B}\bar{i}_{d}^{*B} - \frac{1}{2}\bar{v}_{\text{int}}^{*B}\bar{i}_{0}^{*B} \tag{5-208}$$

$$\frac{dW_{CT0}^{B}}{dt} = -\bar{v}_{d}^{B} \cdot \bar{i}_{d}^{B} - 2v_{d0}^{B} i_{d0}^{B} - \frac{1}{2}\bar{v}_{\text{int}}^{B} \cdot \bar{i}_{0}^{B} \tag{5-209}$$

$$\frac{d\overline{W}_{C\Delta}^{B}}{dt} = v_{d0}^{B}\bar{i}_{0}^{B} + \frac{1}{2}\bar{v}_{d}^{*B}\bar{i}_{0}^{*B} + 2\bar{v}_{\text{int}}^{B} i_{d0}^{B} + \bar{v}_{\text{int}}^{*B}\bar{i}_{d}^{*B} \tag{5-210}$$

$$\frac{dW_{\Delta 0}^{B}}{dt} = \frac{1}{2}\bar{v}_{d}^{B} \cdot \bar{i}_{0}^{B} + \bar{v}_{\text{int}}^{B} \cdot \bar{i}_{d}^{B} \tag{5-211}$$

It is worth to notice that because the DC links are directly connected there is an additional constraints on DC current (i.e. on the zero sequence of differential current):

$$i_{DC} = i_{DC}^{B} = -i_{DC}^{A} \tag{5-212}$$

$$i_{d0} = i_{d0}^{B} = -i_{d0}^{A} \tag{5-213}$$

So equation (5-199) and equation (5-207) could be rewritten as:

$$v_{d0}^{A} = \frac{v_{dc}}{2} - Ri_{d0} - L\frac{di_{d0}}{dt} \tag{5-214}$$

$$v_{d0}^{B} = \frac{v_{dc}}{2} + Ri_{d0} + L\frac{di_{d0}}{dt} \tag{5-215}$$

By adding and subtracting the previous equations it is possible to obtain:

$$v_{dc} = v_{d0}^{A} + v_{d0}^{B} \tag{5-216}$$

$$v_{d0}^{B} - v_{d0}^{A} = 2Ri_{d0} + 2L\frac{di_{d0}}{dt} \tag{5-217}$$

Equations (5-216) and (5-217) show how controlling the zero sequence of differential voltages of inverter A and B it is possible to independently control DC-link voltage and zero sequence of differential current (that is of course directly related to the value of the DC current).

The value of the space vector of the load current for inverter B is generally defined by the load.

So it is necessary to keep the capacitors at the desired voltage level satisfying the constraint conditions expressed by the energy relations (5-208)-(5-211) with the remaining degrees of freedom that are the space vector and the zero sequence of differential current of inverter B.

The differential current could be analyzed in the same way of the previous section:

$$\bar{i}_{d}^{B} = \bar{i}_{d}^{B,LF} + \bar{I}_{d}^{B,HF} e^{j\omega^{B}t} \tag{5-218}$$

$$i_{d0} = i_{d0}^{LF} + \mathrm{Re}\left[\bar{I}_{d0}^{HF} e^{-j\omega^{B}t}\right] \tag{5-219}$$

It can be noted that, even in this case, the low-frequency components of $\bar{i}_{d}^{B}$ and i_{d0} can be used to control the mean value of the total energies $\overline{W}_{CT}^{B}$ and W_{CT0}^{B}, whereas the harmonic component of $\bar{i}_{d}^{B}$ and i_{do} at the output frequency ω_B can be used to control the energy unbalance $W_{C\Delta 0}^{B}$ and $\overline{W}_{C\Delta}^{B}$. These relations can be summarized as follows:

$$\bar{i}_{d}^{B,LF} \rightarrow \overline{W}_{CT}^{B} \tag{5-220}$$

$$i_{do}^{LF} \rightarrow W_{CT0}^{B} \tag{5-221}$$

$$\bar{I}_{do}^{HF} \rightarrow \overline{W}_{C\Delta}^{B} \tag{5-222}$$

$$\bar{I}_{d}^{B,HF} \rightarrow W_{C\Delta 0}^{B} \tag{5-223}$$

For inverter A instead, it is not possible to choose the zero sequence of the differential current because it is proportional to the DC current and it is imposed by inverter B as seen:

$$i_{d0} = i_{d0}^{LF} + \mathrm{Re}\left[\bar{I}_{d0}^{HF} e^{-j\omega^{B}t}\right] \tag{5-224}$$

It is important to note that the high frequency component of zero sequence of differential current has the same frequency of system B.

The space vector of the differential current of inverter A can be expressed in a similar way as:

$$\bar{i}_{d}^{A} = \bar{i}_{d}^{A,LF} + \bar{I}_{d}^{A,HF} e^{j\omega^{A}t} \tag{5-225}$$

The last variable that is possible to use to control inverter A is the space vector of the load (the zero sequence is zero due to the connection of the load):

$$\bar{i}_{0}^{A} = \bar{i}_{0}^{A,LF} + \bar{I}_{0}^{A,HF} e^{j\omega^{A}t} \tag{5-226}$$

The energy relations (5-200)-(5-203) can be rewritten taking into account equation (5-213) as follows:

$$\frac{d\overline{W}_{CT}^{A}}{dt} = -2v_{d0}^{A}\bar{i}_{d}^{A} + 2\bar{v}_{d}^{A}i_{d0} - \bar{v}_{d}^{*A}\bar{i}_{d}^{*A} - \frac{1}{2}\bar{v}_{\mathrm{int}}^{*A}\bar{i}_{0}^{*A} \tag{5-227}$$

$$\frac{dW_{CT0}^{A}}{dt} = -\bar{v}_{d}^{A}\cdot\bar{i}_{d}^{A} + 2v_{d0}^{A}i_{d0} - \frac{1}{2}\bar{v}_{\mathrm{int}}^{A}\cdot\bar{i}_{0}^{A} \tag{5-228}$$

$$\frac{d\overline{W}_{C\Delta}^{A}}{dt} = v_{d0}^{A}\bar{i}_{0}^{A} + \frac{1}{2}\bar{v}_{d}^{*A}\bar{i}_{0}^{*A} - 2\bar{v}_{\mathrm{int}}^{A}i_{d0} + \bar{v}_{\mathrm{int}}^{*A}\bar{i}_{d}^{*A} \tag{5-229}$$

$$\frac{dW_{\Delta 0}^{A}}{dt} = \frac{1}{2}\bar{v}_{d}^{A}\cdot\bar{i}_{0}^{A} + \bar{v}_{\mathrm{int}}^{A}\cdot\bar{i}_{d}^{A} \tag{5-230}$$

By using the space vectors of the load current and differential current of inverter A it is possible to control the mean values of the energy obtained by integrating equations (5-227)-(5-230) over a period:

$$\Delta\overline{W}_{CT}^{A} = -2\int v_{d0}^{A,LF}\bar{i}_{d}^{A,LF}dt - \int \overline{V}_{d0}^{A,HF}\bar{I}_{d}^{A,HF}dt + 2\int \bar{v}_{d}^{A,LF}i_{d0}^{LF}dt - \int \bar{v}_{d}^{*A,LF}\bar{i}_{d}^{*A,LF}dt - \\ -\frac{1}{2}\int \bar{v}_{\text{int}}^{*A,LF}\bar{i}_{0}^{*A,LF}dt \tag{5-231}$$

$$\Delta W_{CT0} = -\int \bar{v}_{d}^{A,LF}\cdot\bar{i}_{d}^{A,LF}dt - \int \Re\{\overline{V}_{d}^{A,HF}\bar{I}_{d}^{*A,HF}\}dt + 2\int v_{d0}^{A,LF}i_{d0}^{LF}dt - \frac{1}{2}\int \bar{v}_{\text{int}}^{A,LF}\cdot\bar{i}_{0}^{A,LF}dt - \\ -\frac{1}{2}\int \Re\{\overline{V}_{\text{int}}^{A,HF}\bar{I}_{0}^{*A,HF}\}dt \tag{5-232}$$

$$\Delta\overline{W}_{C\Delta}^{A} = \int v_{do}^{A,LF}\bar{i}_{0}^{A,LF}dt + \frac{1}{2}\int \overline{V}_{do}^{A,HF}\bar{I}_{0}^{A,HF}dt + \frac{1}{2}\int \bar{v}_{d}^{*A,LF}\bar{i}_{0}^{*A,LF}dt - 2\int \bar{v}_{\text{int}}^{A,LF}i_{d0}^{LF}dt + \\ +\int \bar{v}_{\text{int}}^{*A,LF}\bar{i}_{d}^{*A,LF}dt \tag{5-233}$$

$$\Delta W_{C\Delta0}^{A} = \frac{1}{2}\int \bar{v}_{d}^{A,LF}\cdot\bar{i}_{0}^{A,LF}dt + \frac{1}{2}\int \Re\{\overline{V}_{d}^{A,HF}\bar{I}_{0}^{*A,HF}\}dt + \int \bar{v}_{\text{int}}^{A,LF}\cdot\bar{i}_{d}^{A,LF}dt + \int \Re\{\overline{V}_{\text{int}}^{A,HF}\bar{I}_{d}^{*A,HF}\}dt \tag{5-234}$$

In some terms of relations (5-227)-(5-230) there is a product between the zero sequence component of differential current at the frequency of inverter B and a quantity at the frequency of inverter A. These products generate two contributes that oscillates at different frequencies and have a null mean value when integrated into their own period.

The correlations between the energies that should be kept balanced and the control variables can be summarized as follows:

$$\bar{i}_{d}^{A,LF} \rightarrow \overline{W}_{CT}^{A} \tag{5-235}$$

$$\bar{I}_{0}^{A,HF} \rightarrow W_{CT0}^{A} \tag{5-236}$$

$$\bar{i}_{0}^{A,LF} \rightarrow \overline{W}_{C\Delta}^{A} \tag{5-237}$$

$$\bar{I}_{d}^{A,HF} \rightarrow W_{C\Delta0}^{A} \tag{5-238}$$

The inverse transformation of the space vector and zero sequence of the differential current of inverter A leads to:

$$i_{d1}^{A} = \frac{i_{d0}}{2} + \bar{i}_{d}^{A}\cdot 1 = \frac{i_{d0}^{LF} + \bar{i}_{d}^{A,LF}\cdot 1}{2} + \frac{\text{Re}\left[\bar{I}_{d0}^{HF}e^{-j\omega^{B}t}\right]}{2} + \bar{I}_{d}^{A,HF}e^{j\omega^{A}t}\cdot 1 \tag{5-239}$$

$$i_{d2}^{A} = \frac{i_{d0}}{2} + \bar{i}_{d}^{A}\cdot\overline{\alpha} = \frac{i_{d0}^{LF} + \bar{i}_{d}^{A,LF}\cdot\overline{\alpha}}{2} + \frac{\text{Re}\left[\bar{I}_{d0}^{HF}e^{-j\omega^{B}t}\right]}{2} + \bar{I}_{d}^{A,HF}e^{j\omega^{A}t}\cdot\overline{\alpha} \tag{5-240}$$

$$i_{d3}^{A} = \frac{i_{d0}}{2} + \bar{i}_{d}^{A} \cdot \bar{\alpha}^{2} = \frac{i_{d0}^{LF} + \bar{i}_{d}^{A,LF} \cdot \bar{\alpha}^{2}}{2} + \frac{\mathrm{Re}\left[\bar{I}_{d0}^{HF} e^{-j\omega^{B}t}\right]}{2} + \bar{I}_{d}^{A,HF} e^{j\omega^{A}t} \cdot \bar{\alpha}^{2} \tag{5-241}$$

It is interesting to notice that the three currents have a dc component and two AC components one with the same frequency of system B and one with the same frequency of system A. It leads to two different oscillation of the energy on the capacitor of inverter A depending on the frequency.

It is also interesting to consider that when there is no unbalance between the upper and lower capacitors the AC components are equal to zero.

5.4.2 Simulation model of back to back MMC inverter

The overall simulation model realized with the software Matlab/Simulink is shown in Figure 5-124. In the following the blocks that are related to inverter A, which is connect to the grid, are colored in magenta. The blocks related to inverter B, which is connect to the load, are colored in green. The block that are in common, related to DC link, are colored in yellow. The three legs of both the inverters are named with numbers *1*, *2*, *3*.

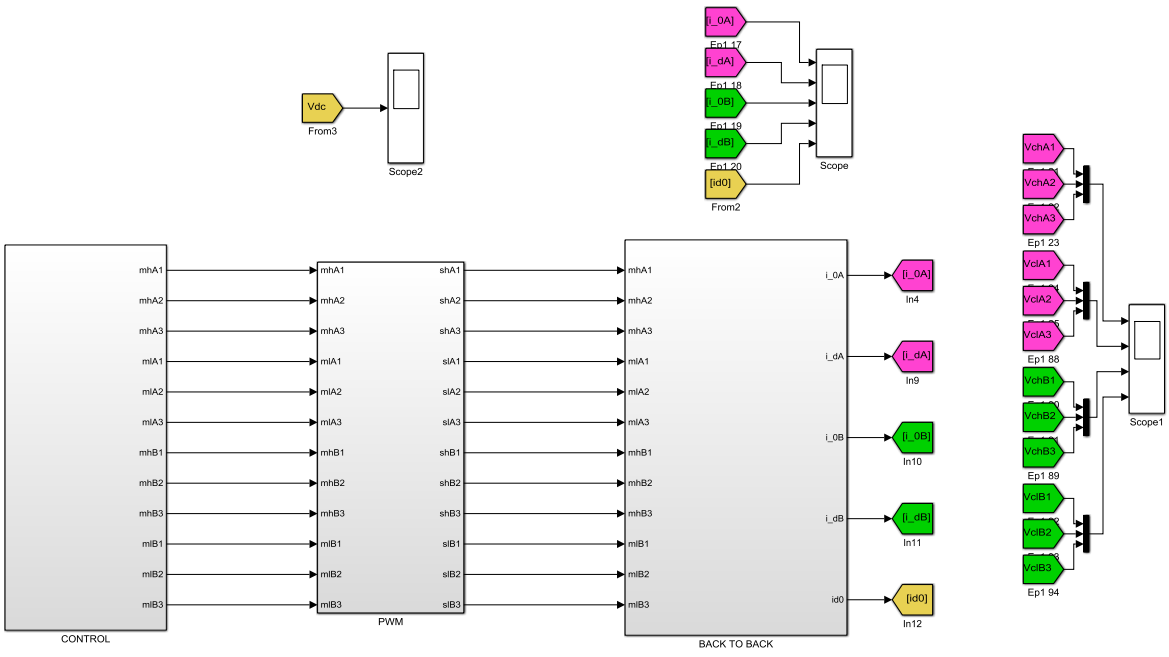


Figure 5-124 – Simulink general model of back to back MMC inverter.

Figure 5-125 shows the model of the back to back MMC based on space vector equations. Figure 5-126 shows the model realized with Sim Power System library.

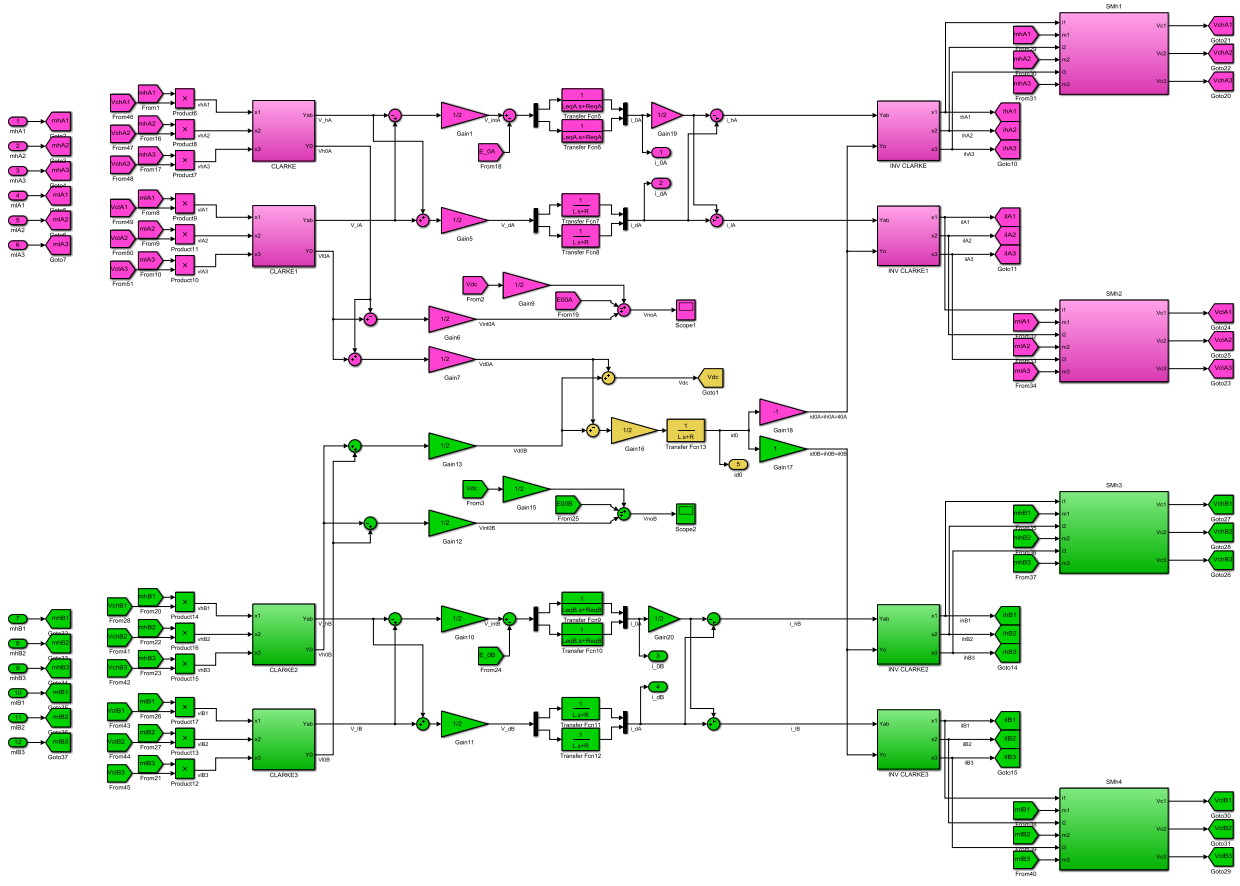


Figure 5-125 – Simulink equation based model of back to back MMC inverter.

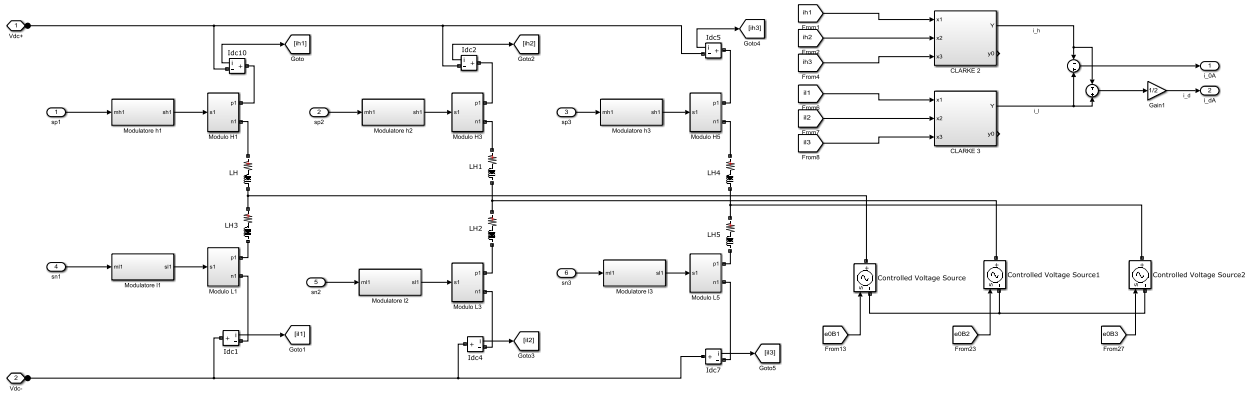


Figure 5-126 – Sim power system model of back to back MMC inverter.

The current loops are shown in Figure 5-127, while in Figure 5-128 the energy loops are shown.

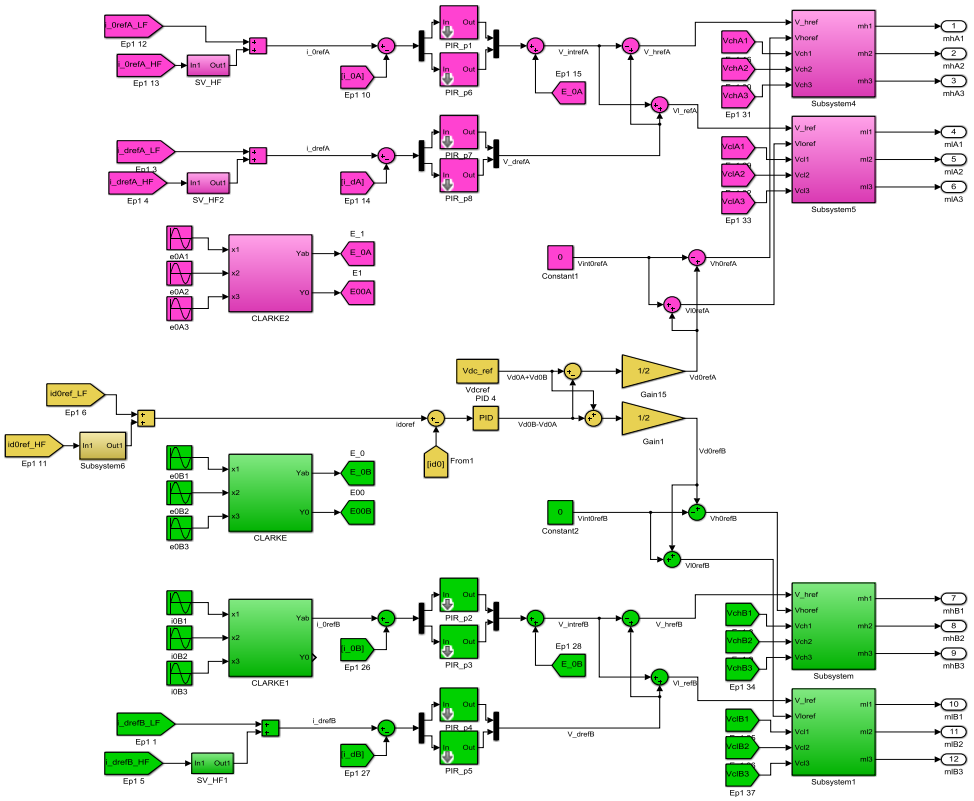


Figure 5-127 – Control scheme current loops of the back to back MMC inverter.

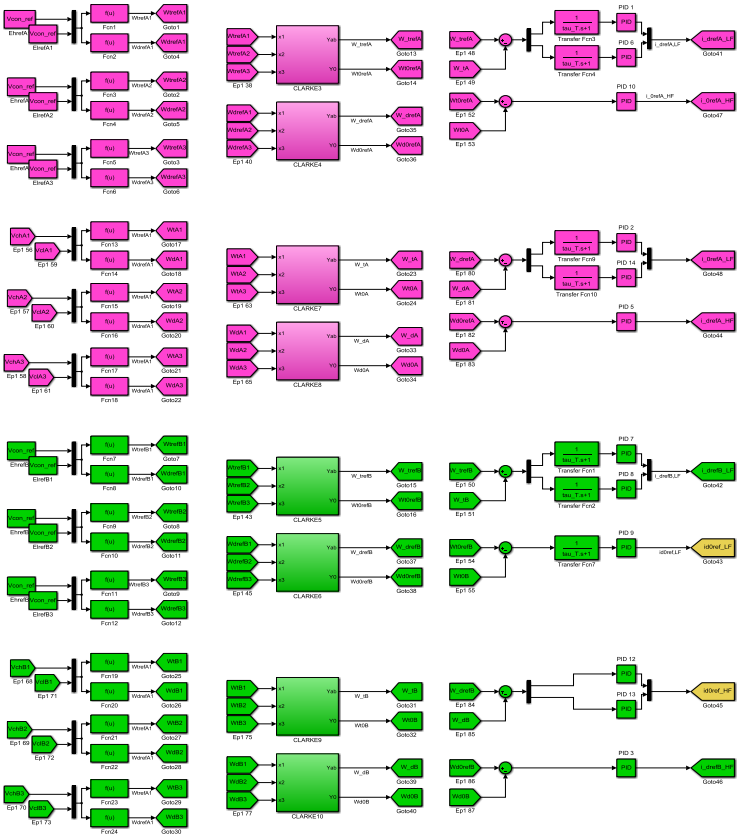


Figure 5-128 – Control scheme energy loops of the back to back MMC inverter.

In Table 5-7 the simulation parameters are listed.

Reference DC voltage	20000 [V]
Capacitors	0.05 [F]
Capacitors reference voltage	20000 [V]
Arm inductance	3.3 [mH]
Arm resistance	0.001 [Ω]
INVERTER A - GRID	
Grid voltage	10000 [V]
Grid frequency	50 [Hz]
INVERTER B - LOAD	
Load voltage	2000
Load frequency	60 [Hz]
Reference load current	1000 [A]

Table 5-7 – Simulation parameters.

5.4.3 Simulation results of back to back MMC inverter

In Figure 5-129 the load side currents are shown in steady state. In Figure 5-130 the grid side currents are shown. It is possible to see that the control system requires a current space vector necessary to keep the energy balance into the system.

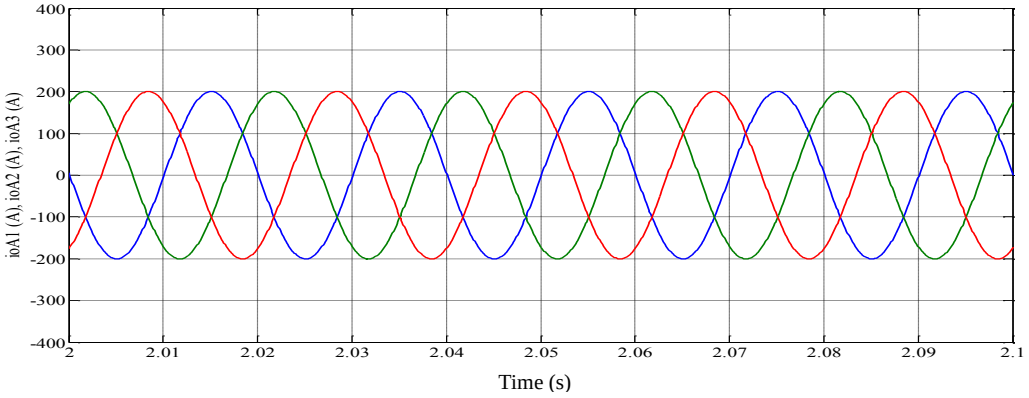


Figure 5-129 – Load side currents.

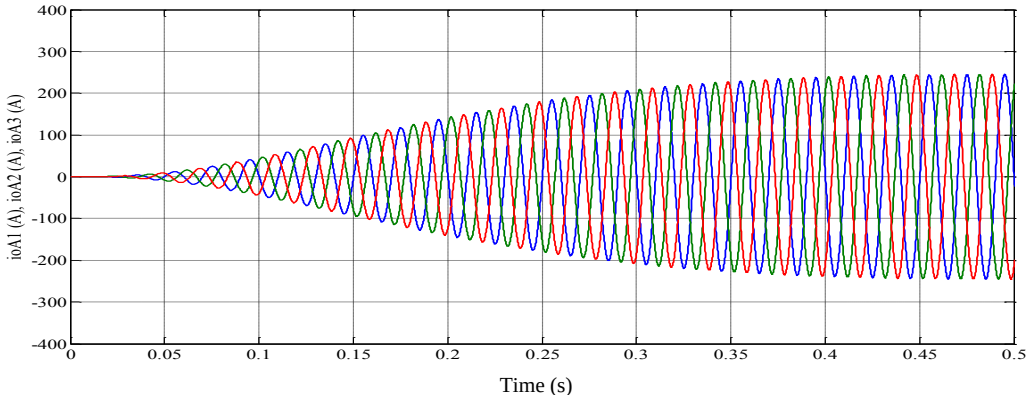


Figure 5-130 – Grid side currents.

In Figure 5-131 the current of the DC link is shown. It is directly correlated with the zero sequence of the differential current. In Figure 5-132 and Figure 5-133 the differential currents space vectors of both inverters are shown. It is possible to see that the regulators keep them to zero due to the fact that in this operation the capacitors are at the right voltage level and the system is balanced.

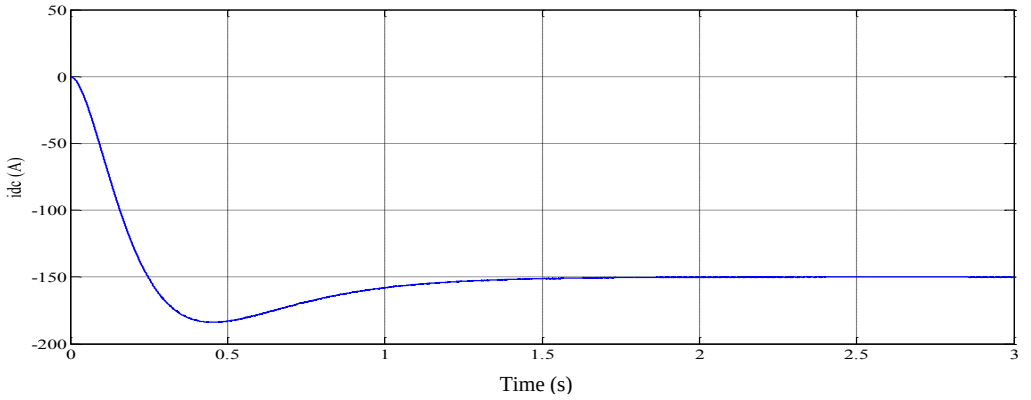


Figure 5-131 – DC current.

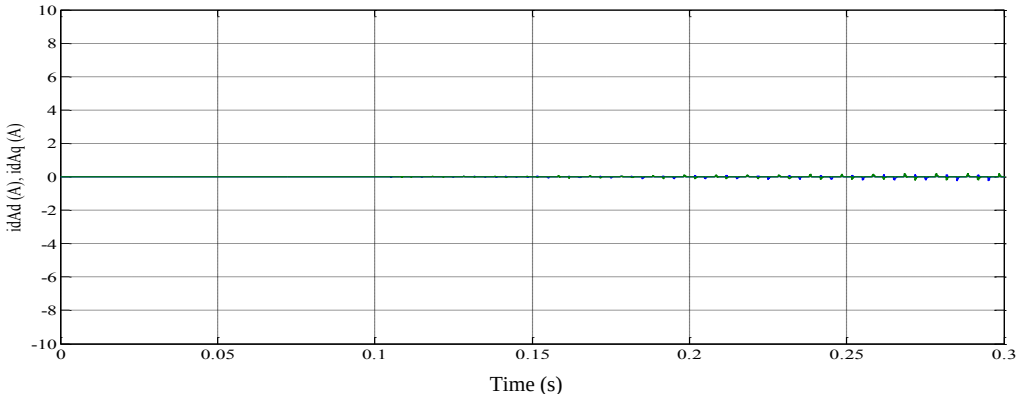


Figure 5-132 – d-q components of grid side differential currents space vector.

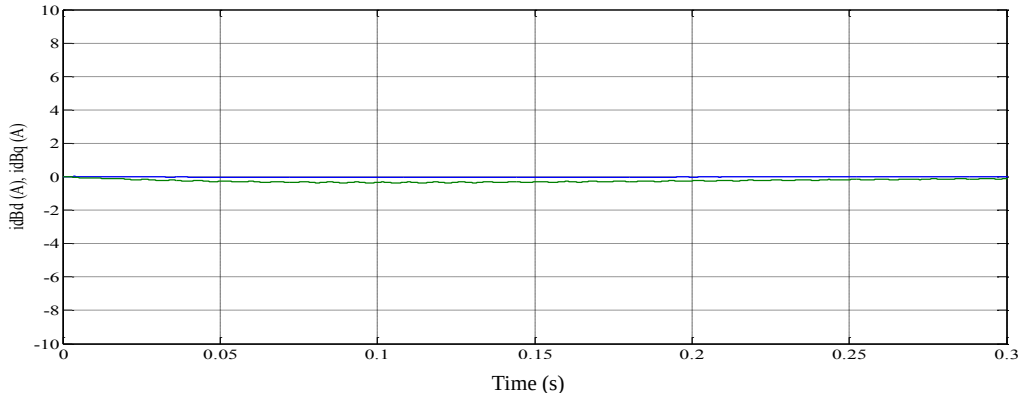


Figure 5-133 – d-q components of load side differential currents space vector.

In Figure 5-134 the differential currents of the three phases of inverter B are shown.

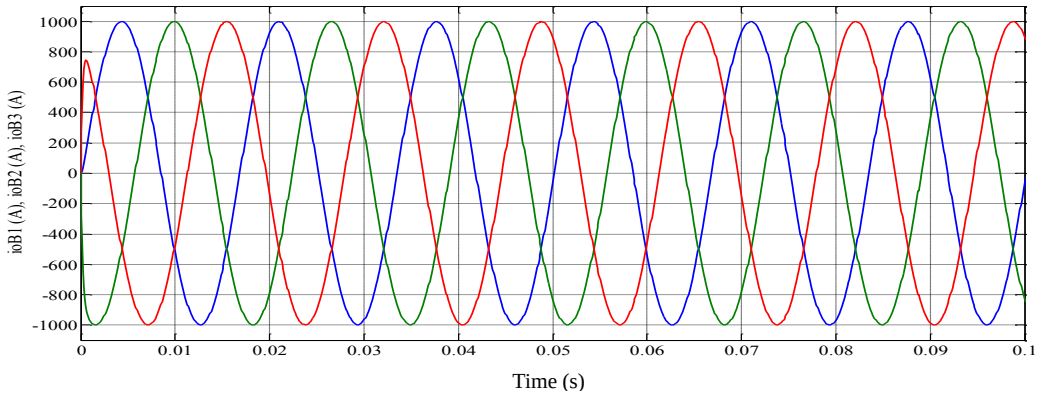


Figure 5-134 – Load side differential currents.

Figure 5-135 and Figure 5-136 show respectively the upper and lower modulating signals of inverter A.

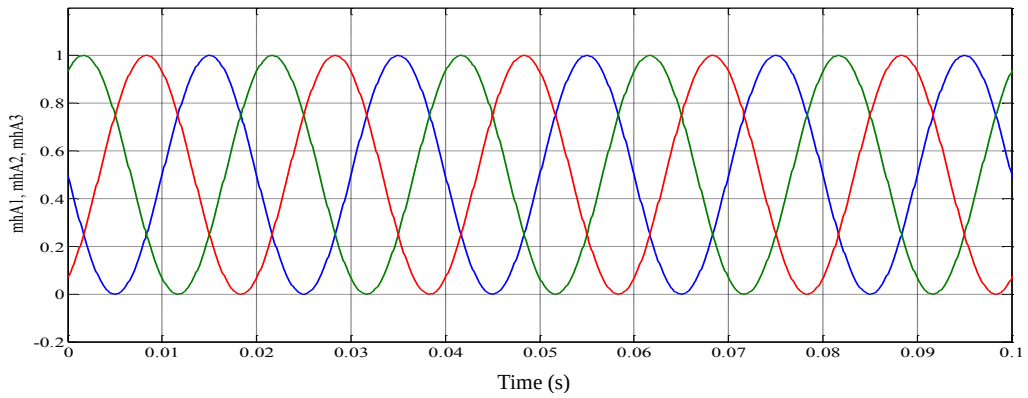


Figure 5-135 – Grid side upper modulating signals.

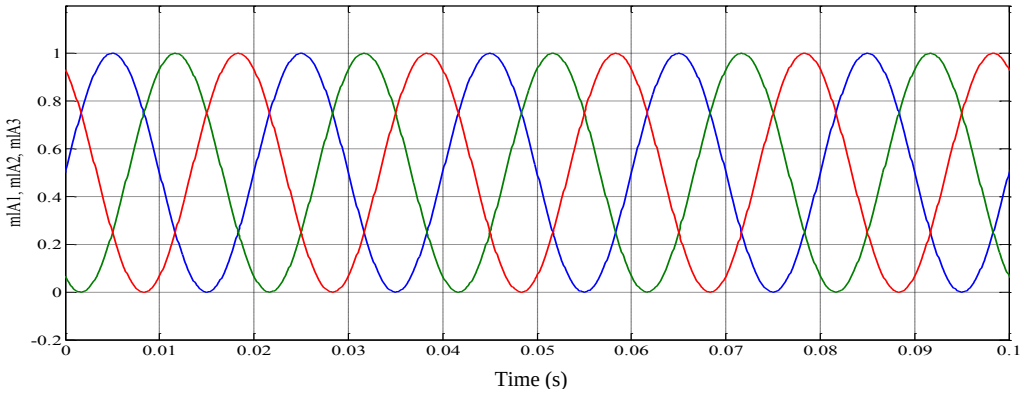


Figure 5-136 – Grid side lower modulating signals.

Figure 5-137 and Figure 5-138 show respectively the upper and lower modulating signals of inverter B.

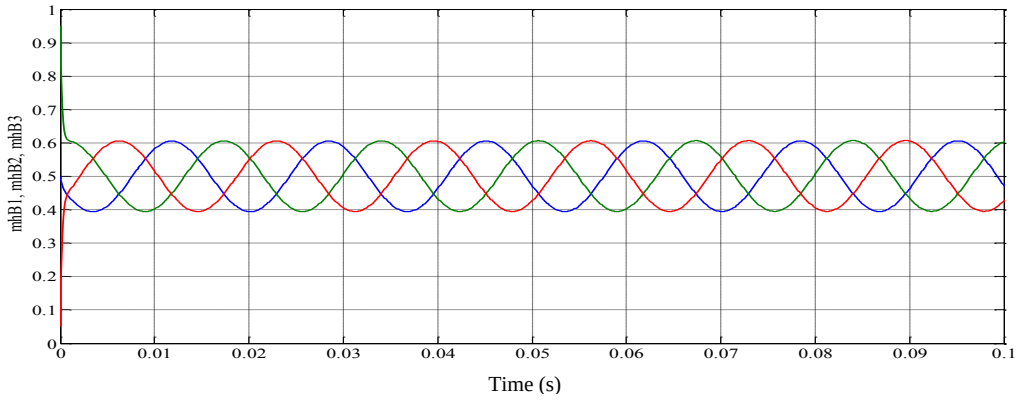


Figure 5-137 – Load side upper modulating signals.

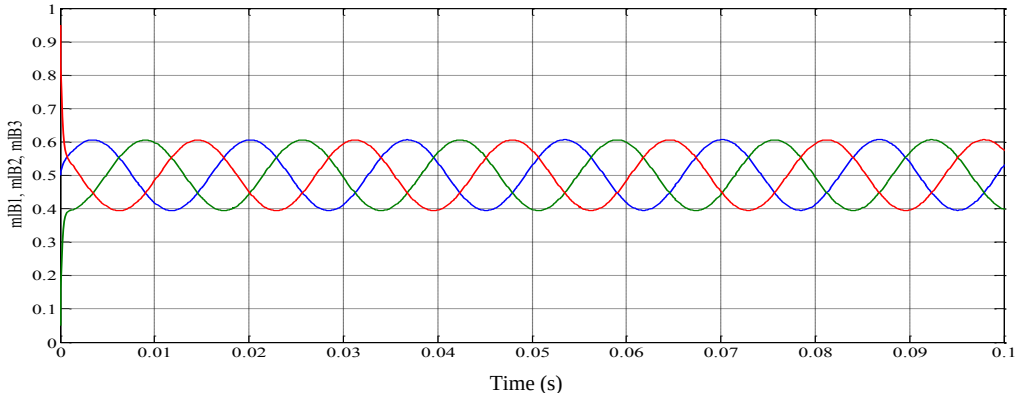


Figure 5-138 – Load side lower modulating signals.

In Figure 5-139 and in Figure 5-140 the upper and lower capacitor voltages of inverter A are shown respectively.

Figure 5-141 and Figure 5-142 show respectively the upper and lower capacitor voltages of inverter A.

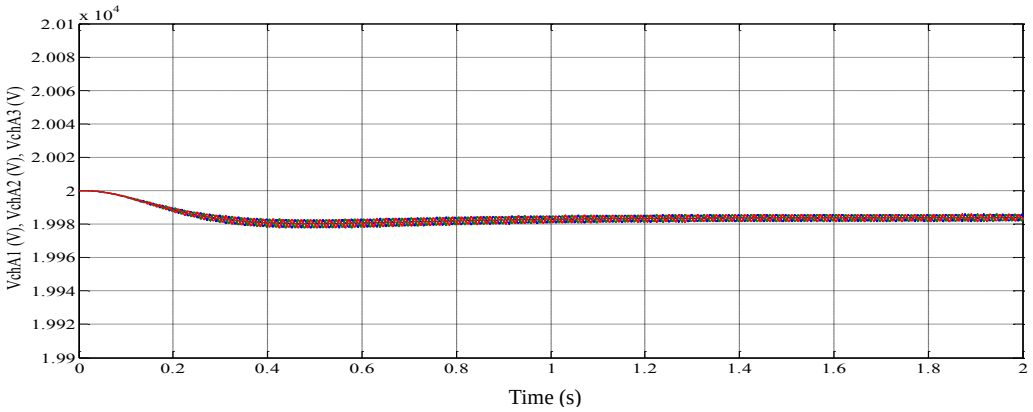


Figure 5-139 – Grid side upper capacitor voltages.

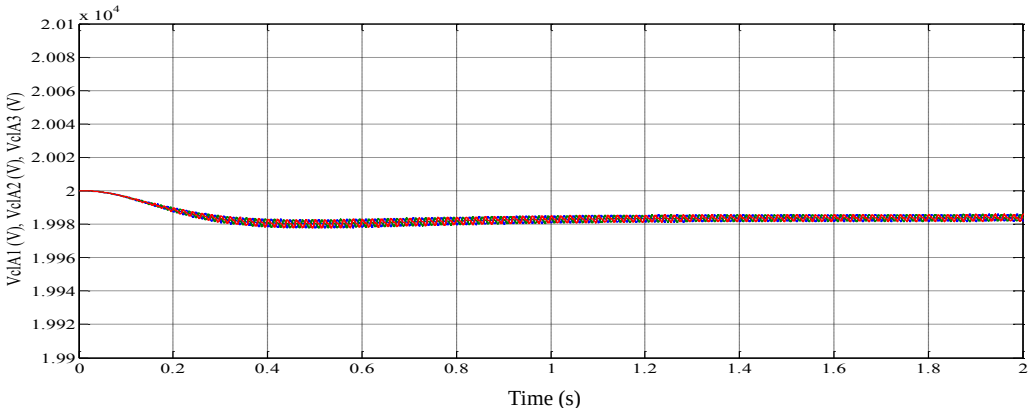


Figure 5-140 – Grid side lower capacitor voltages.

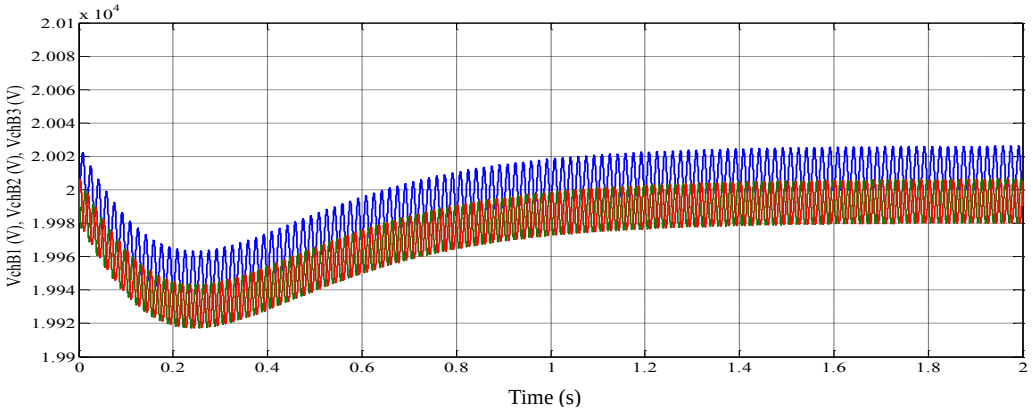


Figure 5-141 – Load side upper capacitor voltages.

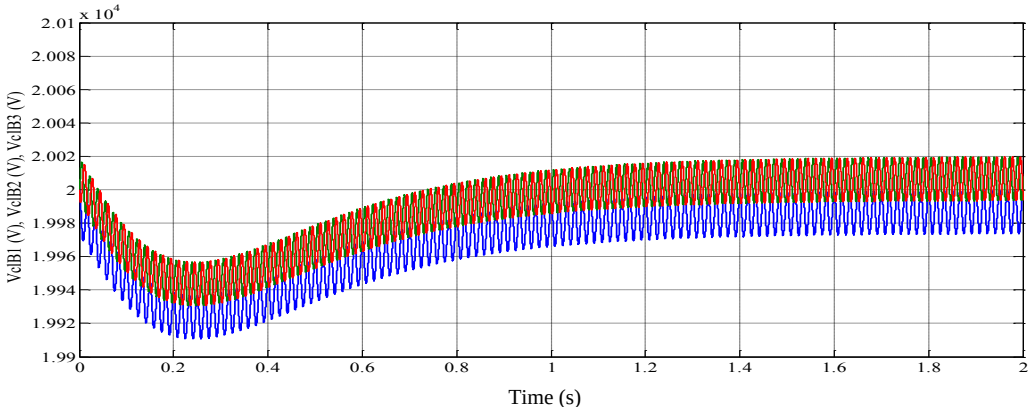


Figure 5-142 – Load side lower capacitor voltages.

In Figure 5-143 the DC voltage is shown. The high frequencies component caused by the PWM commutation is filtered, because it can affect control sensitivity.

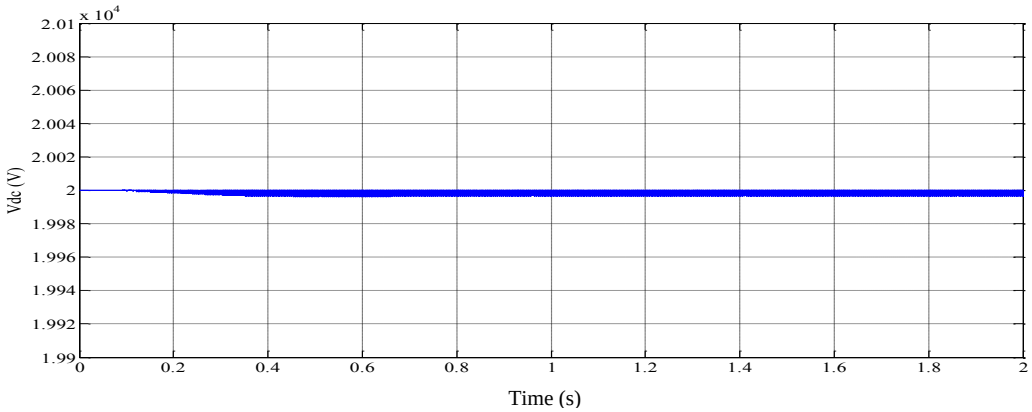


Figure 5-143 – DC voltage.

It is necessary to verify that the control system of grid side inverter is capable to keep balanced the system if one or more of the twelve capacitors of the system are not at the right voltage level.

As example a situation in which all the capacitors of both inverters are charged at 80% of their reference value is shown.

In Figure 5-144, Figure 5-145, Figure 5-146 and Figure 5-147 it is possible to observe that after a transient all the capacitors are at right voltage level.

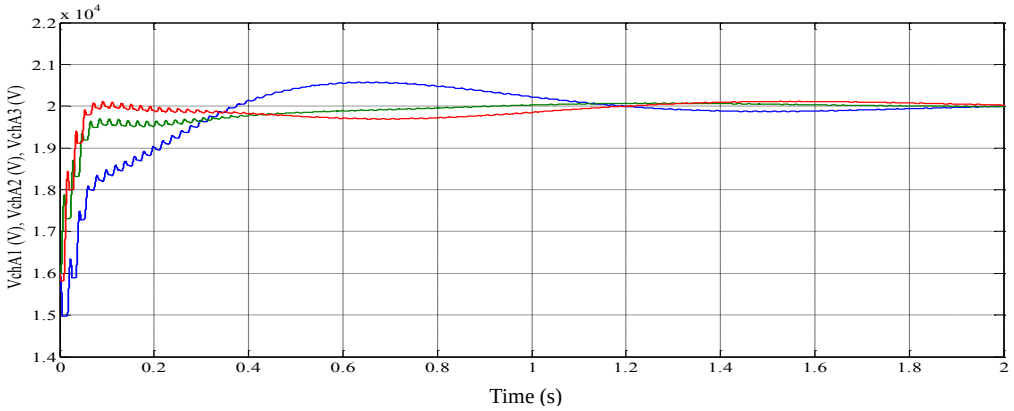


Figure 5-144 – Grid side upper capacitor voltages with discharged capacitors.

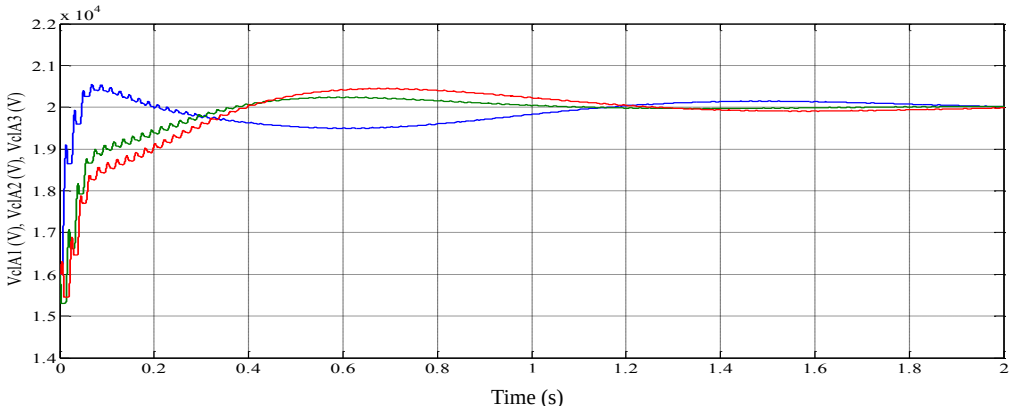


Figure 5-145 – Grid side lower capacitor voltages with discharged capacitors.

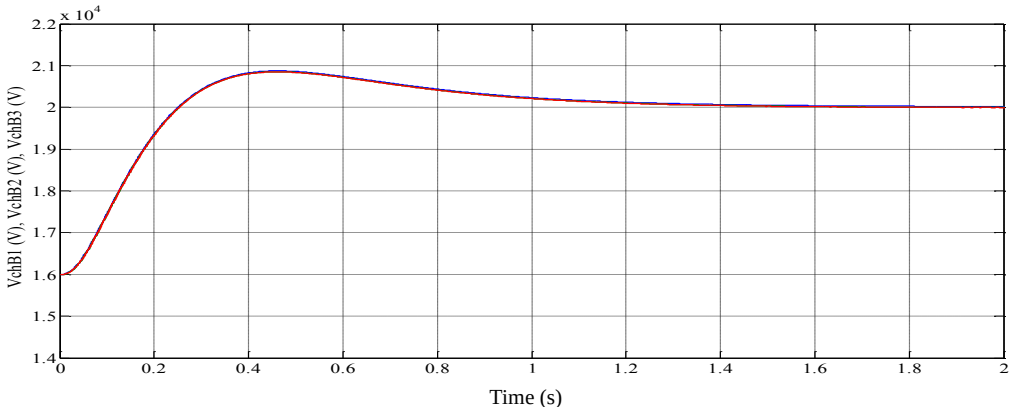


Figure 5-146 – Load side upper capacitor voltages with discharged capacitors.

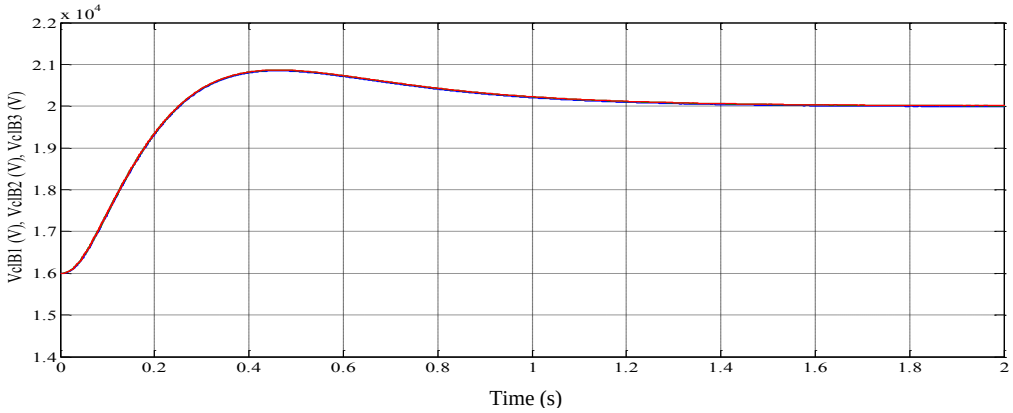


Figure 5-147 – Load side lower capacitor voltages with discharged capacitors.

In the second situation the upper capacitor in phase 1 of inverter A is charged at the 60% of its reference value. The lower capacitors in phases 2 and 3 of inverter B are charged at 80% of their reference value. In Figure 5-148, Figure 5-149, Figure 5-150 and Figure 5-151 it is possible to observe that after a transient all the capacitors are at right voltage level.

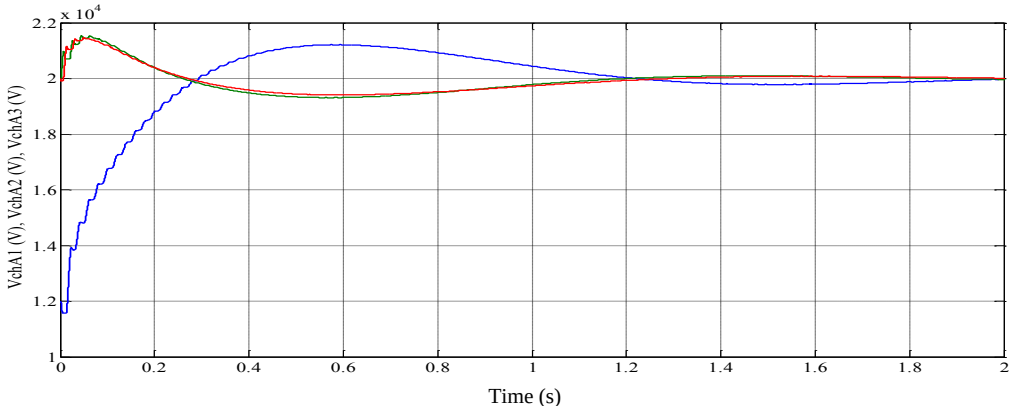


Figure 5-148 – Grid side upper capacitor voltages with unbalanced capacitors.

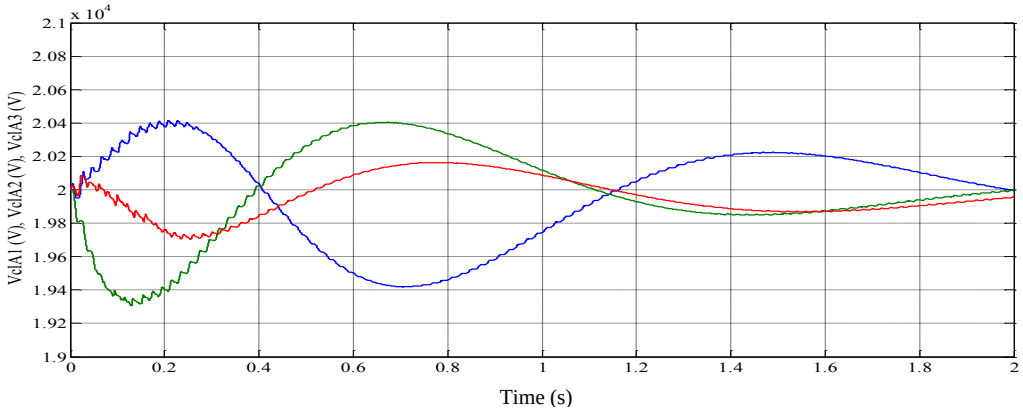


Figure 5-149 – Grid side lower capacitor voltages with unbalanced capacitors.

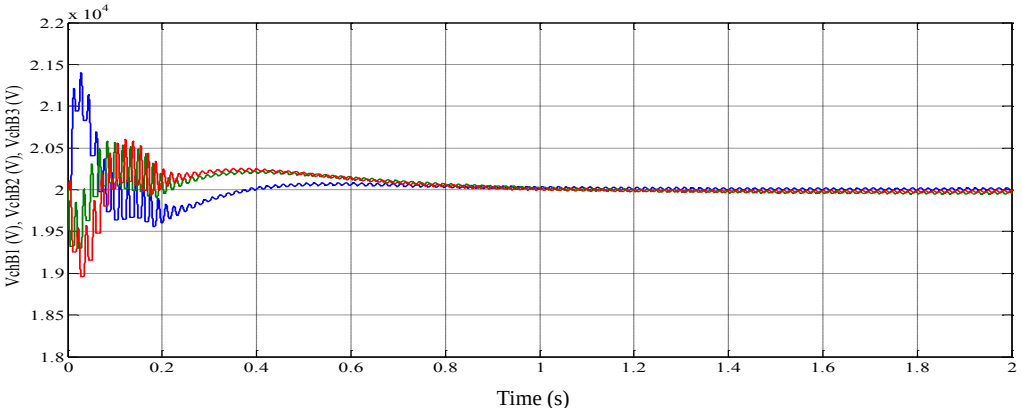


Figure 5-150 – Load side upper capacitor voltages with unbalanced capacitors.

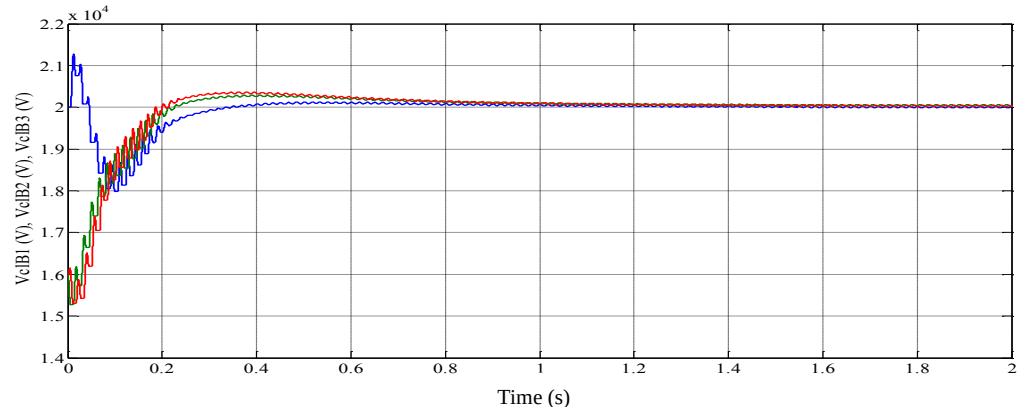


Figure 5-151 – Load side lower capacitor voltages with unbalanced capacitors.

6 Matrix converter

6.1 Introduction

A matrix converter is an array of controlled semiconductor switches that directly connect each input phase to each output phase as shown in Figure 6-1.

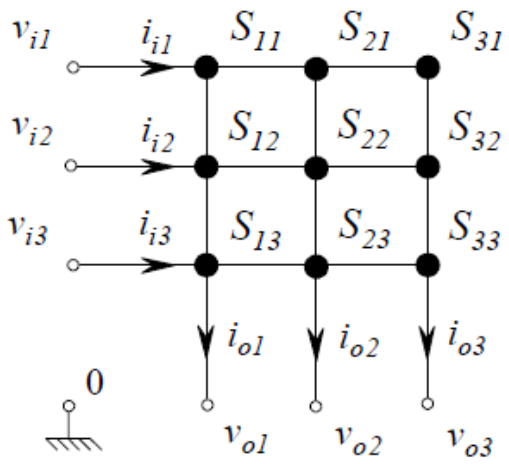


Figure 6-1 – Basic scheme of a three-phase to three-phase matrix converter.

The input-output relationships are shown in equations (6-1) and (6-2).

$$\begin{bmatrix} v_{o1} \\ v_{o2} \\ v_{o3} \end{bmatrix} = \begin{bmatrix} m_{11} & m_{12} & m_{13} \\ m_{21} & m_{22} & m_{23} \\ m_{31} & m_{32} & m_{33} \end{bmatrix} \begin{bmatrix} v_{i1} \\ v_{i2} \\ v_{i3} \end{bmatrix} \tag{6-1}$$

$$\begin{bmatrix} i_{i1} \\ i_{i2} \\ i_{i3} \end{bmatrix} = \begin{bmatrix} m_{11} & m_{21} & m_{31} \\ m_{12} & m_{22} & m_{32} \\ m_{13} & m_{23} & m_{33} \end{bmatrix} \begin{bmatrix} i_{o1} \\ i_{o2} \\ i_{o3} \end{bmatrix} \tag{6-2}$$

where the variables m_{hk} are the duty-cycles of the nine switches S_{hk}. Each duty-cycle must be contained within *0* and *1*.

To avoid short circuits on the input side and ensure uninterrupted load current flow on the output side, the duty-cycles must satisfy the three following constraint conditions:

$$m_{11} + m_{12} + m_{13} = 1 \tag{6-3}$$

$$m_{21} + m_{22} + m_{23} = 1 \tag{6-4}$$

$$m_{31} + m_{32} + m_{33} = 1 \tag{6-5}$$

This converter was originally implemented in aerospace and military applications and recently it is attracting interest for electric vehicles and smart grid applications. One of the main characteristics of this architecture is the absence of intermediate dc link capacitors, which are subject to ageing, and reduce system reliability. Due to this reason it is easy to develop a compact structure with space and weight saving. It is important to have a fault-tolerant system, in all possible applications and in particular where it's fundamental to avoid device unavailability, performance de-rating, and the safety concerns are a priority.

In addition, this structure has different advantages that could be interesting for Smart Grid. The power flow is totally bidirectional and the converter offers the possibility to control the input power factor (i.e. possibility to participate to active and reactive power regulations).

The input current is an high quality current, and the output voltage is multilevel, so the converter is compatible with Power Quality requests.

6.2 Modulation strategy

It is required to determine a modulation strategy that allows, in each cycle period, to calculate the duty-cycles that satisfy the input-output voltage relationships (6-1), the instantaneous required power factor, and the constraint conditions (6-3)-(6-5).

The duty-cycle space vector approach will be followed.

First of all the input and output voltage and current space vectors will be defined:

$$\bar{v}_i = v_i e^{j\alpha_i} \tag{6-6}$$

$$\bar{v}_o = v_o e^{j\alpha_o} \tag{6-7}$$

$$\bar{i}_i = i_i e^{j\beta_i} \tag{6-8}$$

$$\bar{i}_o = i_o e^{j\beta_o} \tag{6-9}$$

The three duty-cycles m_{11}, m_{11}, m_{11} in the first row of the modulation duty-cycle matrix (equation (6-1)) can be represented by the duty-cycle space vector $\bar{m}_1$ defined by the following transformation equation:

$$\overline{m}_1 = \frac{2}{3}\left(m_{11} + m_{12}e^{j\frac{2}{3}\pi} + m_{13}e^{j\frac{4}{3}\pi} \right) \tag{6-10}$$

Taking into account the constraint condition (6-3), the inverse transformations are:

$$m_{11} = \frac{1}{3} + \overline{m}_1 \cdot e^{j0} \tag{6-11}$$

$$m_{12} = \frac{1}{3} + \overline{m}_1 \cdot e^{j\frac{2}{3}\pi} \tag{6-12}$$

$$m_{13} = \frac{1}{3} + \overline{m}_1 \cdot e^{j\frac{4}{3}\pi} \tag{6-13}$$

For the second and third rows, two similar transformations can be introduced:

$$\overline{m}_2 = \frac{2}{3}\left(m_{21} + m_{22}e^{j\frac{2}{3}\pi} + m_{23}e^{j\frac{4}{3}\pi} \right) \tag{6-14}$$

$$\overline{m}_3 = \frac{2}{3}\left(m_{31} + m_{32}e^{j\frac{2}{3}\pi} + m_{33}e^{j\frac{4}{3}\pi} \right) \tag{6-15}$$

Taking into account the constraint condition (6-4), the inverse transformations for $\overline{m}_2$ are:

$$m_{21} = \frac{1}{3} + \overline{m}_2 \cdot e^{j0} \tag{6-16}$$

$$m_{22} = \frac{1}{3} + \overline{m}_2 \cdot e^{j\frac{2}{3}\pi} \tag{6-17}$$

$$m_{23} = \frac{1}{3} + \overline{m}_2 \cdot e^{j\frac{4}{3}\pi} \tag{6-18}$$

Taking into account the constraint condition (6-5), the inverse transformations for $\overline{m}_3$ are:

$$m_{31} = \frac{1}{3} + \overline{m}_3 \cdot e^{j0} \tag{6-19}$$

$$m_{32} = \frac{1}{3} + \overline{m}_3 \cdot e^{j\frac{2}{3}\pi} \tag{6-20}$$

$$m_{33} = \frac{1}{3} + \overline{m}_3 \cdot e^{j\frac{4}{3}\pi} \tag{6-21}$$

To understand the meaning of this duty-cycle space-vector approach, the geometrical representation of $\overline{m}_1$ in *d-q* plane is considered.

Considering that these duty cycles can vary from *0* to *1*, it is possible to comprehend that all the acceptable values for $\overline{m}_1$ are inside the area shown in Figure 6-2 by the equilateral triangle ABC.

m_{11} can assume values inside the plane delimited by two vertical parallel lines obtained by solving equation (6-11) when m_{11} is equal to *0* and *1*, respectively. Likewise, other two areas delimited by two parallel lines can be defined also with reference to m_{12} and m_{13}. The intersection among all the three regions generates the triangular domain ABC of Figure 6-2, which includes all the possible values that $\overline{m}_1$ can assume, and then any possible combination of duty-cycles m_{11}, m_{12} and m_{13}.

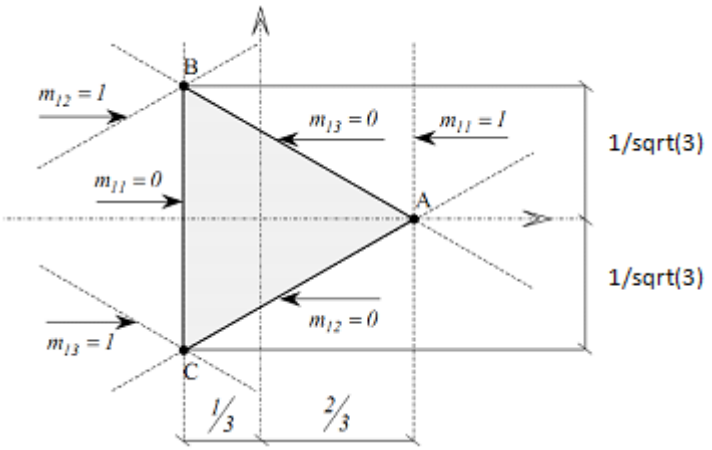


Figure 6-2 – Geometrical representation of the validity domain for $\overline{m}_1$.

It is worth to notice that the distances between the duty-cycle space vector and the sides of the triangle are equal to the values of the three duty-cycles in that particular situation.

Moreover, the position of the space vector $\overline{m}_1$ inside the triangle determines the number of switch commutations of S_{11}, S_{12} and S_{13} in a cycle period.

If the space vector is inside the triangle the switching pattern is constituted by four commutations. If the space vector lies on a triangle side the switching pattern has only two commutations, with one switch always off. In fact, each triangle side is defined by a null value of one of the duty cycles.

Finally, if the space vector corresponds with one of the vertex than the switching pattern has no commutations, two switches are always off and one always on.

It should be noted that, using this notation, the three constraint conditions (6-3)-(6-5) are intrinsically satisfied.

It is possible to rewrite the input-output relationships (6-1) and (6-2) as follows:

$$\bar{v}_o = \frac{\bar{v}_i}{2}\left(\overline{m}_1^* + \overline{m}_2^* e^{j\frac{2}{3}\pi} + \overline{m}_3^* e^{j\frac{4}{3}\pi}\right) + \frac{\bar{v}_i^*}{2}\left(\overline{m}_1 + \overline{m}_2 e^{j\frac{2}{3}\pi} + \overline{m}_3 e^{j\frac{4}{3}\pi}\right) \tag{6-22}$$

$$\bar{i}_i = \frac{\bar{i}_o}{2}\left(\overline{m}_1 + \overline{m}_2 e^{j\frac{4}{3}\pi} + \overline{m}_3 e^{j\frac{2}{3}\pi}\right) + \frac{\bar{i}_o^*}{2}\left(\overline{m}_1 + \overline{m}_2 e^{j\frac{2}{3}\pi} + \overline{m}_3 e^{j\frac{4}{3}\pi}\right) \tag{6-23}$$

Starting from the previous equations it is possible to define three new variables $\overline{m}_d$, $\overline{m}_i$ and $\overline{m}_0$ that are functions of $\overline{m}_1$, $\overline{m}_2$ and $\overline{m}_3$ as follows:

$$\overline{m}_d = \frac{1}{3}\left(\overline{m}_1 + \overline{m}_2 e^{j\frac{2}{3}\pi} + \overline{m}_3 e^{j\frac{4}{3}\pi}\right) \tag{6-24}$$

$$\overline{m}_i = \frac{1}{3}\left(\overline{m}_1 + \overline{m}_2 e^{j\frac{4}{3}\pi} + \overline{m}_3 e^{j\frac{2}{3}\pi}\right) \tag{6-25}$$

$$\overline{m}_0 = \overline{m}_1 + \overline{m}_2 + \overline{m}_3 \tag{6-26}$$

These three new quantities can be considered as direct, inverse and zero component of the three duty-cycle space vectors $\overline{m}_1$, $\overline{m}_2$ and $\overline{m}_3$.

The inverse transformation equations are:

$$\overline{m}_1 = \overline{m}_d + \overline{m}_i + \overline{m}_0 \tag{6-27}$$

$$\overline{m}_2 = \overline{m}_d e^{j\frac{4}{3}\pi} + \overline{m}_i e^{j\frac{2}{3}\pi} + \overline{m}_0 \tag{6-28}$$

$$\overline{m}_3 = \overline{m}_d e^{j\frac{2}{3}\pi} + \overline{m}_i e^{j\frac{4}{3}\pi} + \overline{m}_0 \tag{6-29}$$

Substituting equations (6-27) - (6-29) into (6-22) and (6-23) yields:

$$\bar{v}_o = \frac{3}{2}\bar{v}_i \overline{m}_i^* + \frac{3}{2}\bar{v}_i^* \overline{m}_d \tag{6-30}$$

$$\bar{i}_i = \frac{3}{2}\bar{i}_o \overline{m}_i + \frac{3}{2}\bar{i}_o^* \overline{m}_d \tag{6-31}$$

Equations (6-30) and (6-31) represent in a compact form the input-output relationships of three-phase matrix converter.

To require the desired input power factor it is necessary starting from equation (6-31) imposing the following condition:

$$\left(\bar{i}_o \overline{m}_i + \bar{i}_o^* \overline{m}_d\right) \cdot j\overline{\psi} = 0 \tag{6-32}$$

where $\overline{\psi}$ has the desired phase angle for the input current space vector and amplitude equal to 1:

$$\overline{\psi} = e^{\beta_i} \tag{6-33}$$

Equation (6-32) alongside whit equation (6-30), that express the output voltage control requirement, allows to determine a modulation strategy.

The quantity $\overline{m}_0$ does not appear in these two equations so it can assume any arbitrarily chosen value, without affecting the average value of the reference quantities.

The general solution of the system of equations (6-30) and (6-32), valid for any value of the parameter λ, is:

$$\overline{m}_d = \frac{\bar{v}_o \overline{\psi}}{3(\bar{v}_i \cdot \overline{\psi})} + \frac{\lambda}{\bar{v}_i^* \bar{i}_o^*} \tag{6-34}$$

$$\overline{m}_i = \frac{\bar{v}_o^* \overline{\psi}}{3(\bar{v}_i \cdot \overline{\psi})} - \frac{\lambda}{\bar{v}_i^* \bar{i}_o} \tag{6-35}$$

There are three degrees of freedom: the parameter λ and $\overline{m}_0$. The parameter λ can be utilized only if the phase angle of the output current space vector is known in each cycle period. If it is set to zero equation (6-34) and (6-35) can be rewritten as:

$$\overline{m}_d = \frac{q}{3\cos\varphi_i} e^{j\alpha_o} e^{j\beta_i} \tag{6-36}$$

$$\overline{m}_i = \frac{q}{3\cos\varphi_i} e^{-j\alpha_o} e^{j\beta_i} \tag{6-37}$$

where q is the voltage transfer ratio:

$$q = \frac{v_o}{v_i} \tag{6-38}$$

Taking into account (6-27) - (6-29), equations (6-36) and (6-37) lead to:

$$\overline{m}_l = \frac{2}{3} q \frac{\cos\left[\alpha_o - (l-1)\frac{2\pi}{3}\right]}{\cos\varphi_i} e^{j\beta_i} + \overline{m}_0 \tag{6-39}$$

where *l=1,2,3*.

Equation (6-39) allows the calculation, in each cycle period, of the values of the three duty-cycle space vectors $\overline{m}_1$, $\overline{m}_2$ and $\overline{m}_3$ as a function of the voltage transfer ratio *q*, the output phase angle α_o, the input current phase angle β_i, and the input power factor $\cos\varphi_i$.

These equations can be analyzed using their geometrical representation in the *d-q* plane. If λ is not equal to zero, then the three quantities $\overline{m}_1$, $\overline{m}_2$ and $\overline{m}_3$ in general are the vertexes of a scalene triangle. If $\lambda=0$, the three quantities $\overline{m}_1$, $\overline{m}_2$ and $\overline{m}_3$ lie on a segment of variable length, as shown in Figure 6-3, rotating and translating within the triangular domain as function of time.

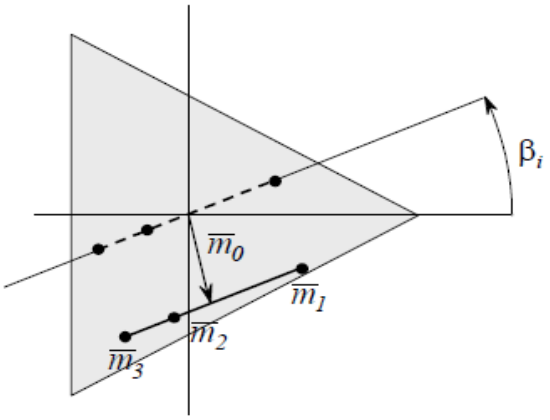


Figure 6-3 – Geometrical representation of the segment connecting $\overline{m}_1$, $\overline{m}_2$ and $\overline{m}_3$.

The position of any segment connecting the three duty-cycle space vectors can be arbitrarily changed by means of $\overline{m}_0$, within the condition that it has to remain completely inside the triangular region. The choice of $\overline{m}_0$ provides two degrees of freedom, affecting the modulation features in terms of maximum voltage transfer ratio, number of switch commutations, and ripple of the input/output quantities.

For given values of α_o, β_i and φ_i, the maximum achievable value for the voltage transfer ratio depends on how long the segment can be without crossing the triangle boundary. It is interesting to notice that, if the control of the power factor is required to participate to reactive power regulation (e.g. into Smart Grid), than the maximum transfer ratio is not always achievable. It is possible to compensate for this controlling the other degree of freedom λ.

Finally, it is possible to find the modulation law for matrix converters, determining the nine duty-cycles of equation (6-1) with the anti-transformation relations.

6.3 Diagnosis and fault detection strategy

The research activity at "The University of Nottingham" was focused on the evaluation of Matrix converter performances and the analysis of fault condition behavior.

6.3.1 Output current and process model method

The first method proposed in this section is a process model based method. In Figure 6-4 a block diagram of this detection system is shown. The real system is constituted by the matrix converter and the R-L load. The process model block describes both the matrix converter and the R-L load. The estimated output currents are the outputs of this block. The error between the estimated and the measured output currents is the input of fault detection and diagnosis block.

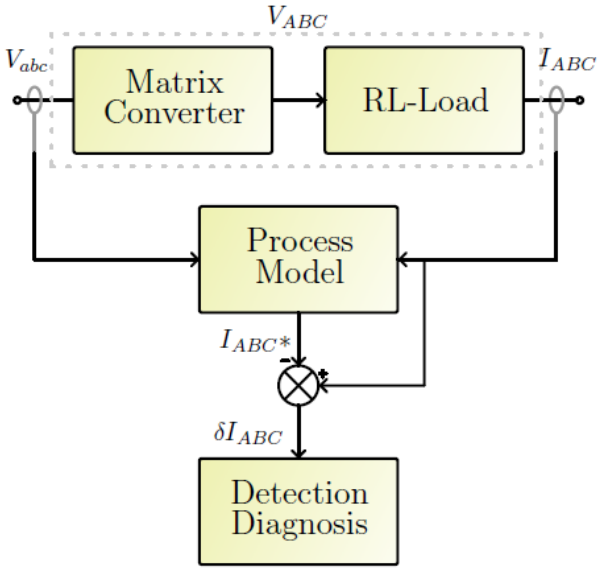


Figure 6-4 – Diagnosis system block diagram of the analytical method.

The matrix converter is simulated with a low frequency modulation matrix model and the R-L load is simulated with a state-space model. The low frequency modulation matrix produces the matrix converter average output voltages in each modulation period starting from the control demands and input voltages. These output voltages are then fed into a load observer whose states are the estimated load currents. The observer normally runs in a closed loop until a fault is detected and

then the loop is left open-circuit as the systems model has changed. The output current error signal is then generated and fed into an inference system, which detects and diagnoses the fault.

6.3.2 Direct output current fault detection and diagnosis method

The second method places the current sensors between the output phases of the converter and the clamp voltages as shown in Figure 6-5.

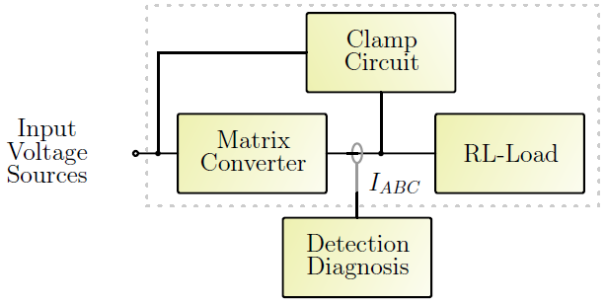


Figure 6-5 – Diagnosis system block diagram of the direct method.

By using the common mode current measurement of the matrix converter it is possible to construct a current similar in nature to that which flows through the clam circuit midpoint (i.e. the fault current) without additional sensors.
In the scheme, the converter output currents are used for fault detection and diagnosis. The detection and diagnosis inference system uses expert knowledge about the converter current during a fault together with knowledge about the converter switching pattern.

In the implementation, the output currents are sampled six times per modulation period, during the six zero-vectors that are present in the symmetrical SVM modulation pattern. The zero-vectors were chosen as the sample point because the switches in each phase are in the same states and every switch in a phase is used at least once in the zero-vectors regardless of input-output sector combination. This makes the detection system more modular because a detection scheme developed for one phase is universal. Information is taken directly from the modulator of the matrix converter and used to strategically sample the output currents during a modulation period. These samples are then used to detect and diagnose the fault by checking for differences in the currents flowing through the matrix converter during the zero-vectors.

6.3.3 Combined output current detection method

This method is essentially a hybrid between the process model and direct method, this is done to produce an optimal fault detection and diagnosis solution. The direct method only works when there is significant load current and the process model method only works well when there is no load current. Also by combining the two methods, the duplication of the system model is removed and the direct methods speed can be improved by comparing each sample directly to the model. In doing this the direct method can detect the fault as soon as the first zero-vector that uses the faulty device is sampled, assuming the load current is non zero.

A simplified block diagram for this method is shown in Figure 6-6. The detection and diagnosis system is now more complex, and must evaluate two inference systems to detect and diagnose the switch fault.

The process model method and the direct method complement each other, so by using both methods in conjunction it is possible to detect and diagnose matrix converter faults at any operating point and in any input-output sector combination.

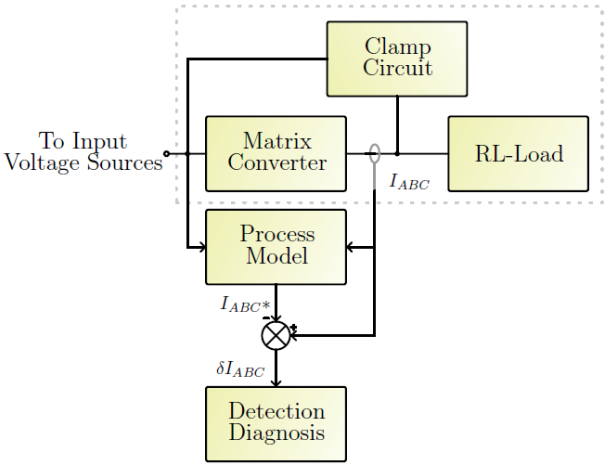


Figure 6-6 – Combined fault detection and diagnosis system block diagram.

6.4 Control and diagnosis experimental setup

The control platform, where the control and the different fault tolerant algorithms were implemented, consists of an high-speed Digital Signal Processor (DSP) and a couple of high-speed Field-Programmable Gate Array (FPGA) in parallel. An Infineon Tricore TC1797 floating point DSP shown in Figure 6-7 and an Actel ProASIC3 FPGA were used.

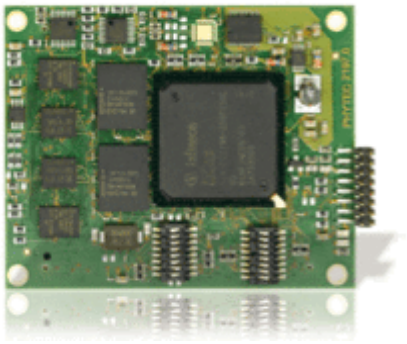


Figure 6-7 – Infineon Tricore TC1797.

The HighTec Platform (Eclipse based I.D.E. - Integrated Design Engine) is shown in Figure 6-8.

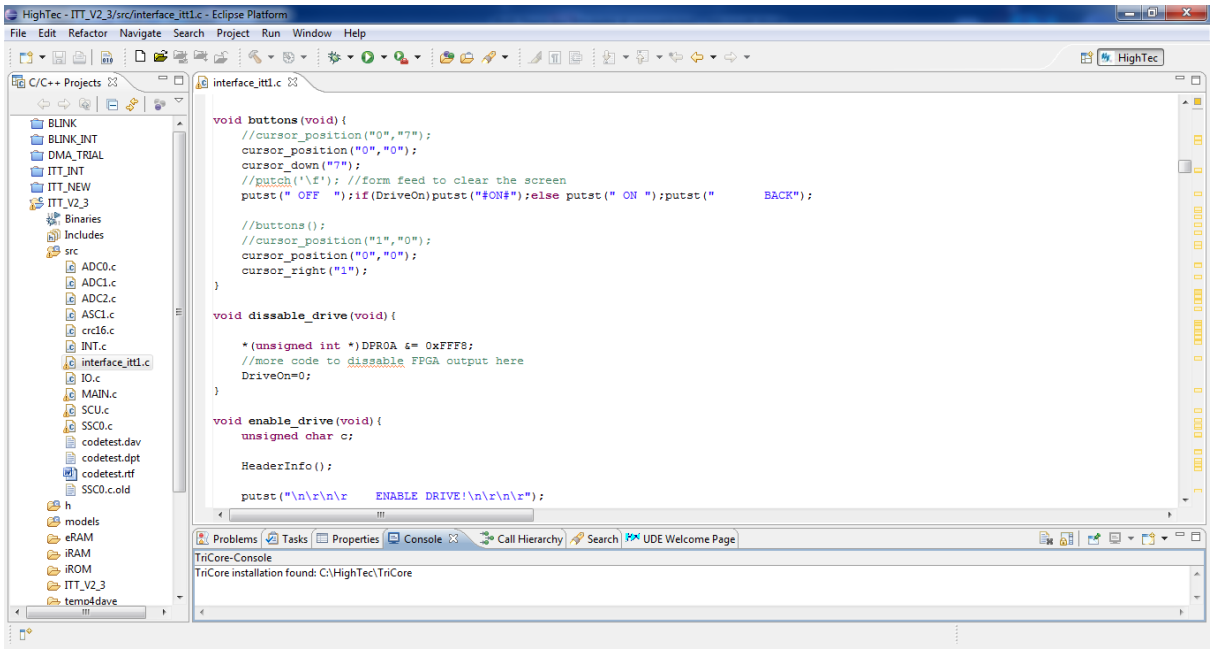


Figure 6-8 – HighTec Platform.

One of the main objectives during the code implementation was the optimization of the controller resources due to the need of extensive computing capability required to control the matrix converter and in particular for the fault detection algorithms. The code implementation of two fundamental parts of the code will be explained in the following sections.

6.4.1 Interface

An interface for the control and data-acquisition through serial communication was developed to control the drives for all the necessary tests. The interface is needed to set all the values of the

parameters for the desired setup, the type of the control and the relative tuning, and when is necessary to start the acquisition of a required number of samples of the specified variables. It is possible, through the fast monitoring of the wide range of information necessary, to operate the system in both healthy and faulty conditions.

To realize the interface it was necessary to avoid any type of polling algorithms apart from the infinite main loop. A polling algorithm is a process where the microcontroller checks the status of a peripheral as a synchronous activity waiting for its readiness. In particular in this case it can check if the user sends a character to the microcontroller to select a required option or to insert a value. A polling cycle is the time in which each element is monitored once. The limit of this type of algorithm is that, in every cycle, computation resources are required even if no action is necessary and that's why a different strategy was chosen for this application. The alternative of polling is the interrupt. Interrupt is a signal to the microcontroller indicating an event that needs attention. An interrupt notifies that an high-priority condition requires the interruption of the current code the processor is executing. So when the user enters a character the relative function is activated.

The management of an interface with many different levels of sub-menus is not a trivial task. In fact each time the character is sent a relative menu is activated and executes a particular function. Than the program has to exit all the functions and restore the previous context; the controller is ready again for the next interrupt trigger. Of course, to know which sub-menu should be entered each time and what are the correct values of the stored parameters the micro-controller have to know some information.

To this end a state machine was realized. When a character is entered by the user's interface then the interrupt is triggered and the relative function is entered. Basically in this function it is only implemented the state machine, that is shown in the following.

```
void ASC1_viRx(void)
{
      globalC = getch(0);

      switch(context)
      {
            case 0:
                  menu0();
                  break;
            case 1:
                  menu1();
                  break;
            case 2:
                  menu2();
                  break;
            case 3:
```

```
                menu3();
                break;
            case 4:
                menu4();
                break;
            case 5:
                menu5();
                break;
            case 6:
                menu6();
                break;
            case 7:
                menu7();
                break;
            case 8:
                menuF2();
                break;
            case 31:
                menu31();
                break;
            case 32:
                menu32();
                break;
            case 51:
                menu51();
                break;
            case 52:
                menu52();
                break;
            case 53:
                menu53();
                break;
            case 6162:
                menu6162();
                break;
            case 63:
                menu63();
                break;
            case 64:
                menu64();
                break;
            case 9991:
                getintMenu();
                break;
            case 9992:
                getyesnoMenu();
                break;
            case 9993:
                dummy54();
                break;
            case 9994:
                getfloatMenu();
                break;
        }

} //  End of function ASC1_viRx
```

It is possible to see that its only purpose is to enter the right sub-menu depending on the number case. Then, all the other tasks are demanded to the sub-menu. Of course, before exiting the sub-

menu function it is necessary to set the right value of the number case depending of what should be opened at the next trigger.

Many state variables (i.e. global variables) and flags (i.e. static local variables) are used to memorize the correct state in the sub-menu.

The result of the implemented interface is shown in Figure 6-9 and in Figure 6-10.

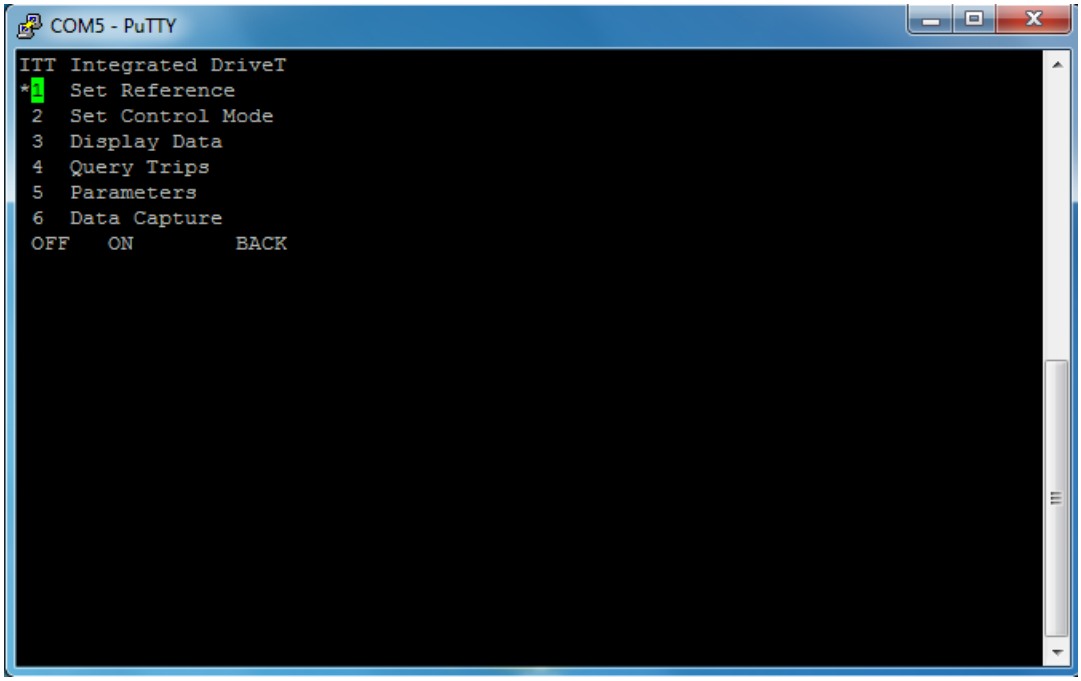


Figure 6-9 – Interface menu.

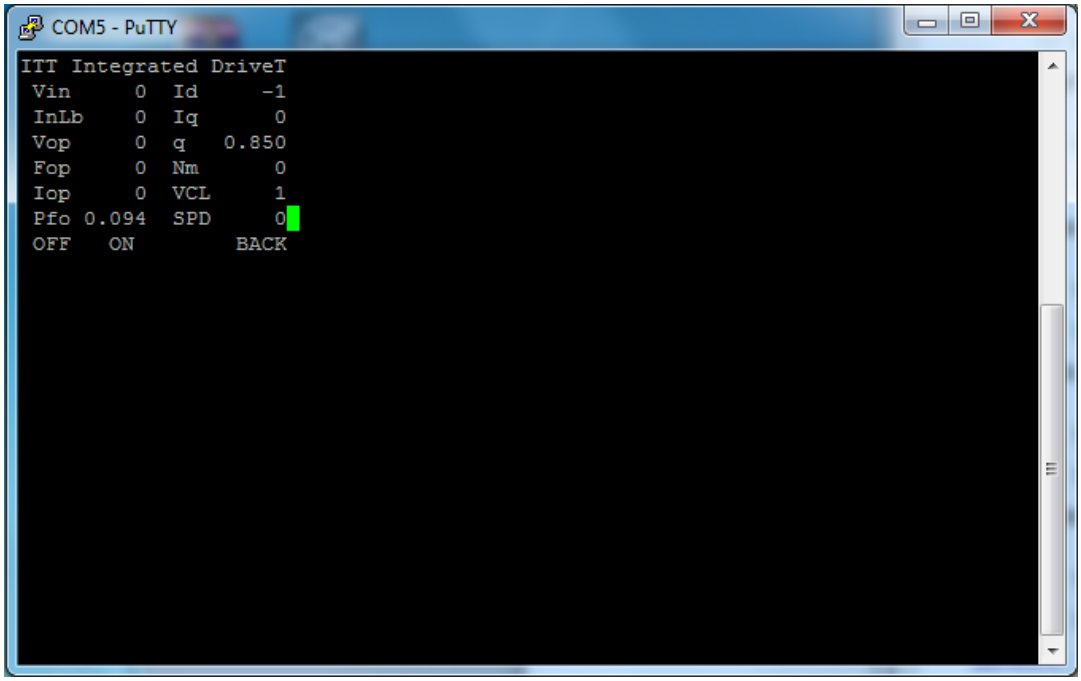


Figure 6-10 – Interface Parameters submenu.

6.4.2 High speed acquisition

Like any type of electrical drive, to control an electrical drive based on matrix converter, it is necessary to measure, during each switching period, a set of variables depending on the type of control. In general, for control purpose, it is needed to acquire one (or few) samples, for each of the variables, every switching period.

In addition to this "low speed" sampling it was required for this project to have the possibility to perform an "high speed" sampling for a certain set of desired variables. All this stored variables can be used to study the behavior of the electrical drive with the current setup, to implement fault detection algorithms, and to develop fault tolerant strategies.

In this case to store the necessary samples for the variables of interest a massive amount of computational resources are needed. In fact using a switching period of 125 us (carrier frequency 8 kHz) it is required to sample 50 points for each of the chosen variables resulting in a 2.5 us for each sample. The samples, stored into a circular buffer (that are overwritten the next period), should be transferred each switching period.

It is worthy to notice that, during the switching period - even if the ADC sampling and the PWM management are demanded directly to FPGAs - the microcontroller still have to import from FPGAs the "low speed" sampled variables necessary for the control, execute all the calculations needed to control the drive, implement the modulation routine, communicate the desired duty-cycles to the FPGAs and manage the interface when required.

The microcontroller has not enough calculation resources to add the "high speed" sampling task in the switching period.

For example, it can be interesting, for diagnostic purposes, to sample the three output currents, the three input voltages and the voltage of the clamp circuit. To avoid interrupting the main routine (that cannot be halted for the correct behavior of the system), this acquisition was implemented into a second core available into the platform TC1797, called PCP (Peripheral Control Processor), that is shown in Figure 6-11.

This way the "high speed" sampling operation does not affect the primary DSP. The PCP basically is a second microcontroller with its own RAM and flash memories that is seen as a peripheral from the primary DSP. It can only executes interrupts and has not a main function. Basically all the interrupt available on the board can be routed on this secondary microcontroller setting a bit into the relative peripheral interrupt register.

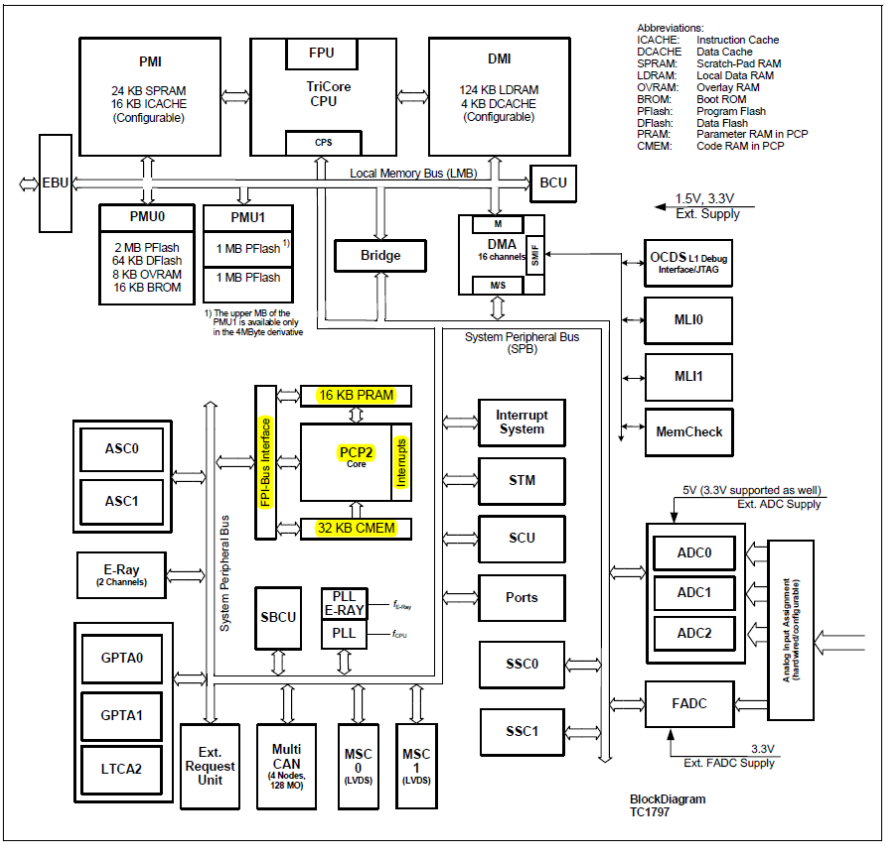


Figure 6-11 – TC1797 Block Diagram.

What was implemented into an interrupt was a function that simply stores all the samples into an array that is memorized, then the array is overwritten from the new samples the next cycle period. Part of the code relative to the variables is shown:

```
while(*(unsigned int *)DPR0B &0x00000008);
dpr1B = *(unsigned int *)DPR1B;
dpr2B = *(unsigned int *)DPR2B;
dpr3B = *(unsigned int *)DPR3B;
dpr4B = *(unsigned int *)DPR4B;
dpr5B = *(unsigned int *)DPR5B;
dpr6B = *(unsigned int *)DPR6B;
dpr7B = *(unsigned int *)DPR7B;

adc0 = (0x00003fff & dpr1B);
adc1 = (0x00003fff & dpr2B);
adc2 = (0x00003fff & dpr3B);
adc3 = (0x00003fff & dpr4B);
adc4 = (0x00003fff & dpr5B);
adc5 = (0x00003fff & dpr6B);
adc6 = (0x00003fff & dpr7B);

ia=(float)(adc0-offset0)*IgainA;
ib=(float)(adc1-offset1)*IgainB;
ic=(float)(adc2-offset2)*IgainC;
VA=(float)(adc3-offset3)*VgainA;
VB=(float)(adc4-offset4)*VgainB;
```

```
VC=(float)(adc5-offset5)*VgainC;
VCLAMP=(float)(adc6-offset6)*VgainClamp;
VLcommon=(VA+VB+VC)/3;
```

After several periods, the acquired samples can be exported directly into Matlab to allow the manipulation and graphical reapresentation of the data. The Matlab interface used is shown into Figure 6-12.

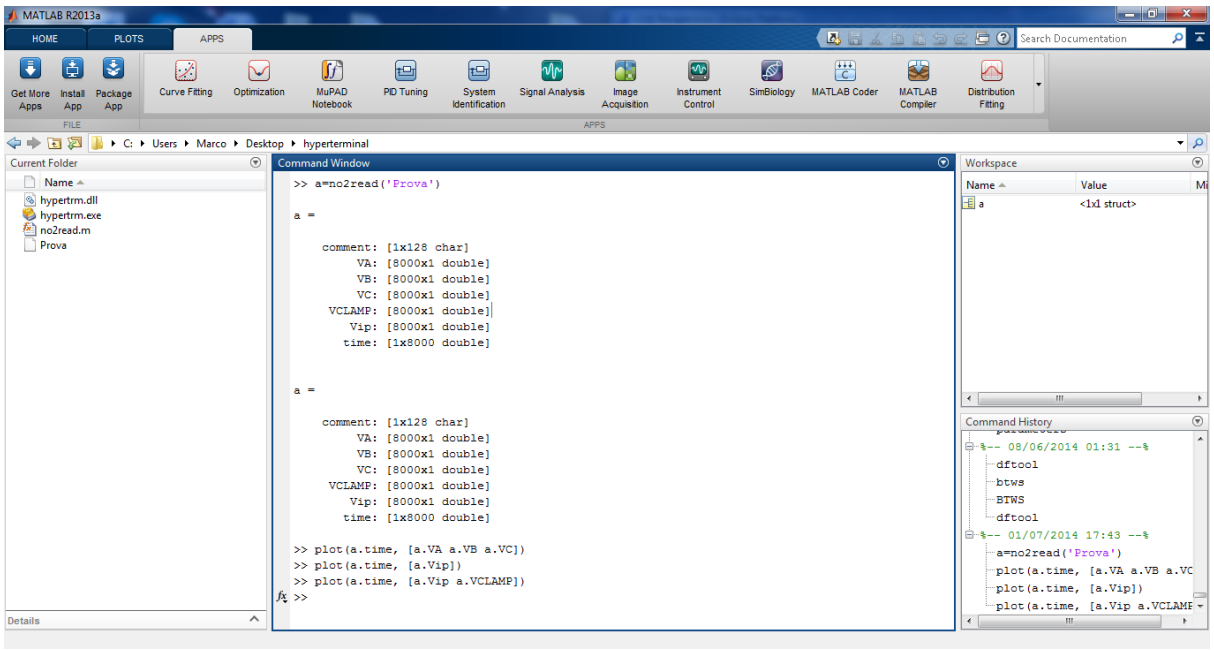


Figure 6-12 – Matlab interface used for data manipulation.

6.5 Experimental results

At "The University of Nottingham" a Matrix converter of 70 kW was available as experimental setup to test the code and try different controls and fault detection algorithms. The matrix converter is shown in Figure 6-13.

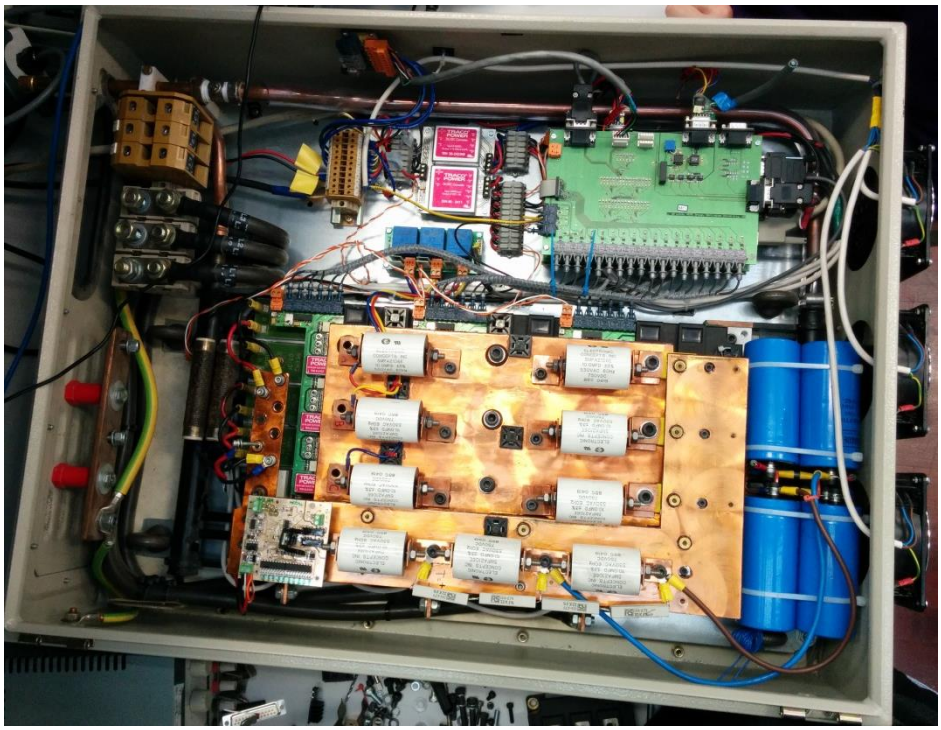


Figure 6-13 – Matrix converter prototype.

First of all, to correctly run the system it was necessary the measure and the accurate compensation of all the disturbance effects, for example the voltage drop across all the power switches. This operation is important also for the diagnostic purpose due to the need, of some of the fault detection methods, of high reliability measures. Then the correct behavior of the circuit clamp was verified.
In Figure 6-14 is shown the voltage of the circuit clamp, that is the green trace. The red trace is the filtered voltage of the clamp circuit. The blue trace represents the voltage threshold of the clamp.

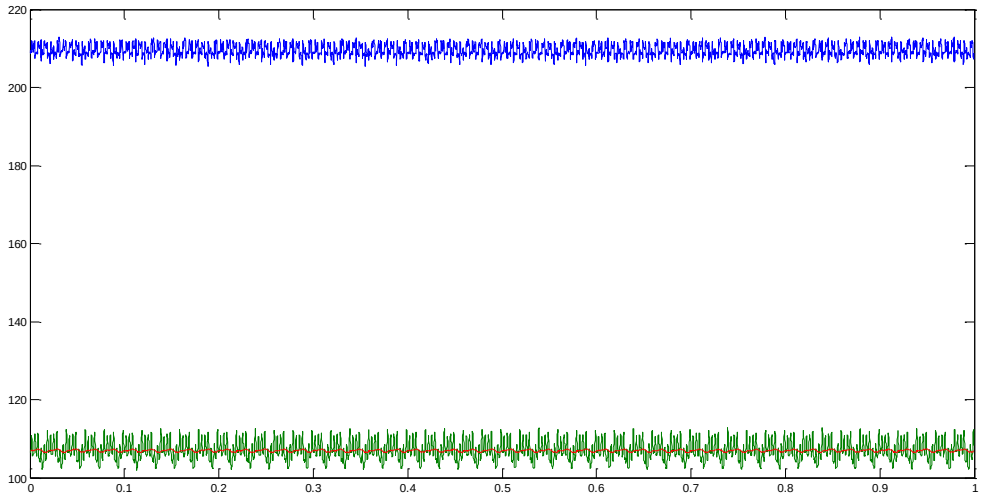


Figure 6-14 – Voltage clamp and voltage limit.

The experimental setup was constituted by an induction motor. Its rated parameters are listed in Table 6-1. The motor is shown in Figure 6-15.

Power	30 [kW]
Rotating speed	1470 [g/min]
Voltage	380-415 [V] - Δ
Current	57-52 [A]
Frequency	50 [Hz]
Duty	S1
Power factor	0.87

Table 6-1 – Induction motor parameters.

Figure 6-15 – Induction machine.

The first experimental setup consist in *V/f = constant* control of the induction motor.
The frequency is 20 Hz, and the output rated voltage is 70 V.
First of all in Figure 6-16 the oscilloscope acquisition of the three output currents and one of the filtered output voltages is shown. From now on the results obtained with the DSP acquisition and Matlab manipulation will be shown.

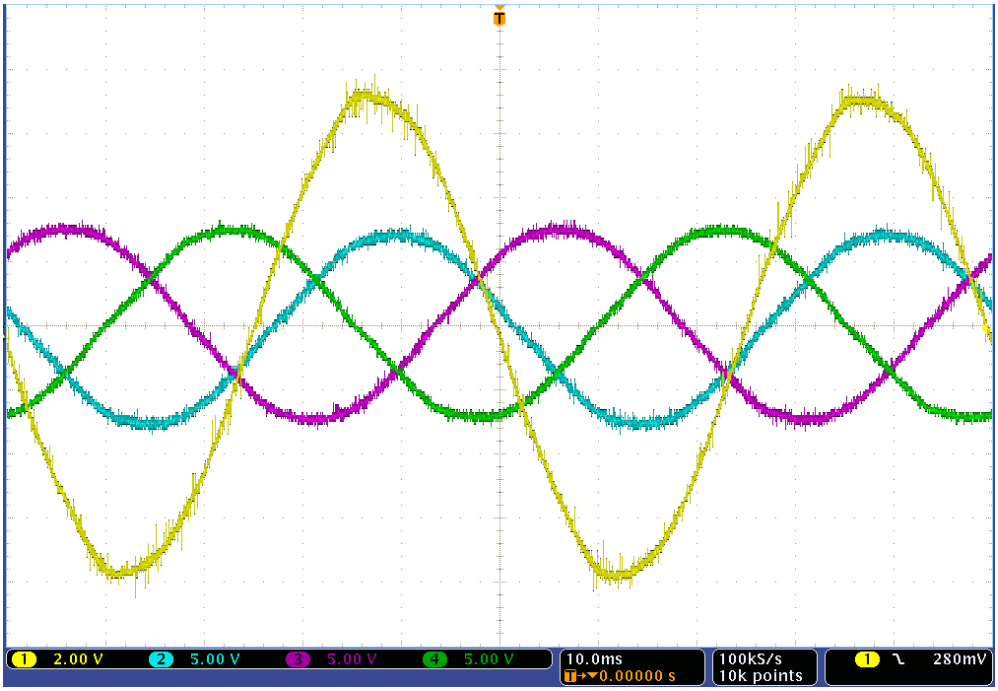


Figure 6-16 – Output currents and input voltage, frequency 20 Hz, Vrated 70 V.

In Figure 6-17 the output phase currents with this setup are shown. In Figure 6-18 are shown the input voltages. These quantities were acquired with "slow speed" sampling.

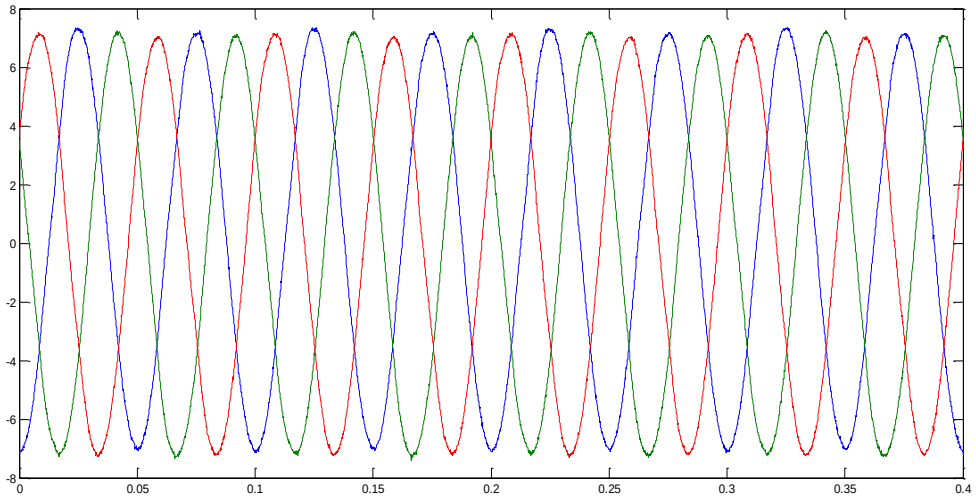


Figure 6-17 – Output currents, frequency 20 Hz, Vrated 70 V.

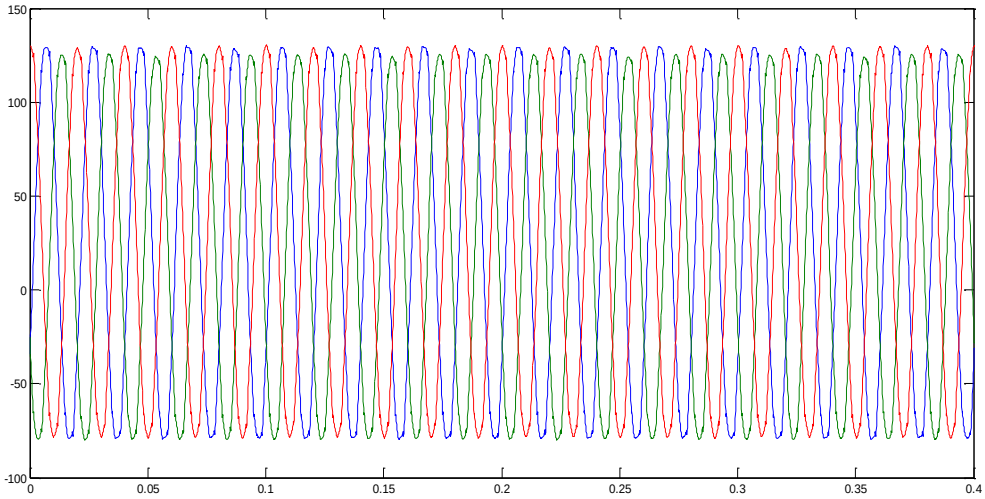


Figure 6-18 – Input voltages, frequency 20 Hz, Vrated 70 V.

In Figure 6-19 it is shown the result of "high speed" sampling of the output currents. It is also possible to see the Fourier analysis realized in Matlab.

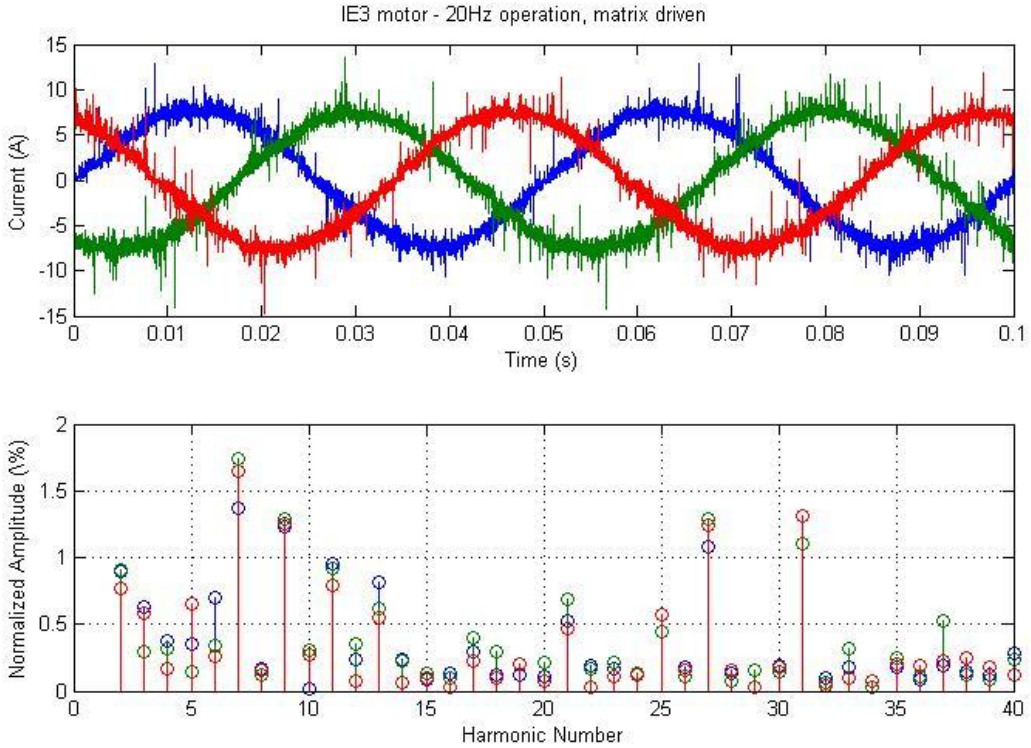


Figure 6-19 – Fourier analysis, output currents frequency 20 Hz, Vrated 70 V.

The second experimental setup consists in the same control with the same frequency. The rated output voltage is 28 V.

In Figure 6-20 the " slow speed" acquisition of the output currents is shown. In Figure 6-21 the "high speed" sampling with relative Fourier analysis is shown.

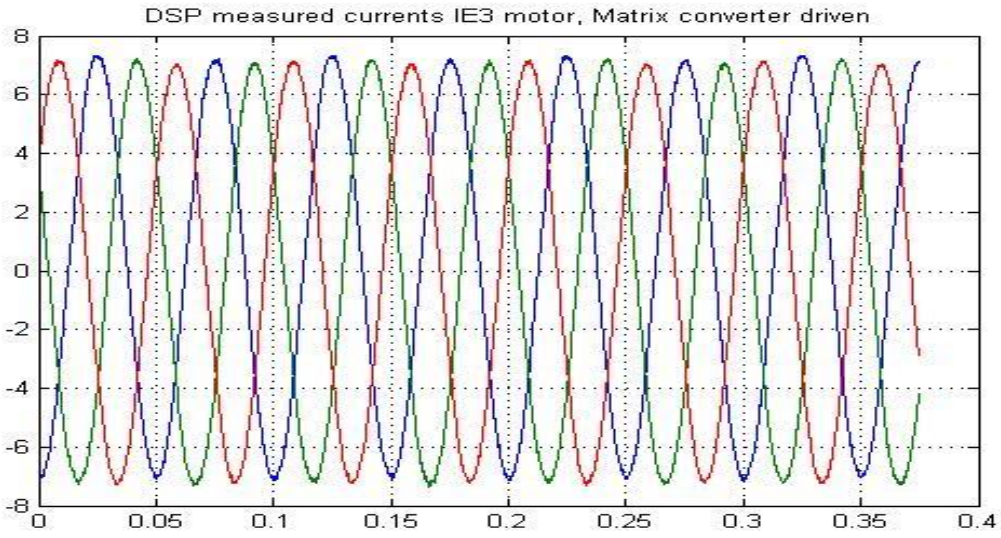


Figure 6-20 – Output currents, frequency 20 Hz, Vrated 28 V.

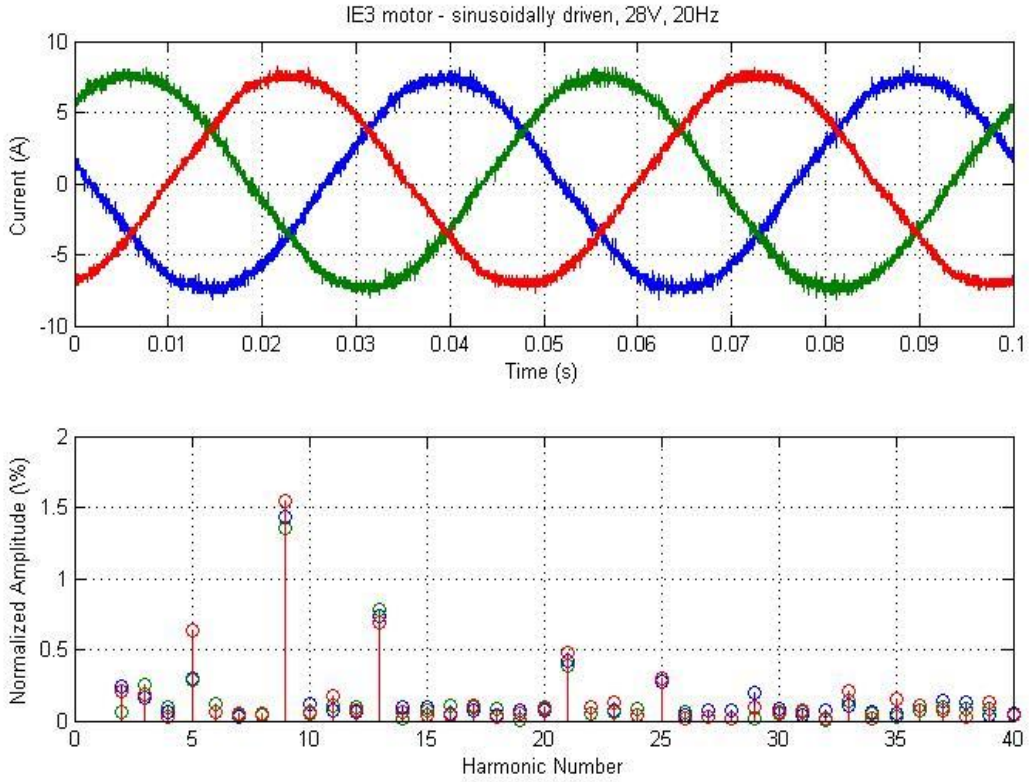


Figure 6-21 – Fourier analysis, output currents frequency 20 Hz, Vrated 28 V.

The Fourier analysis of the two discussed experimental setups were studied to make a slot harmonic investigation on the induction machine. It is possible to observe that the THD improves with the reduction of the requested output voltage.

7 Conclusion

In this thesis, power converters and electric drives for Smart Grid applications were studied. Nowadays the electricity networks, whose architecture was designed for passive use only, have the necessity of bidirectional power flow capability because generation nodes are distributed all over the network. In particular, the renewable energy power generators are intermittent and the energy needs to be stored, possibly also with the use of the available electric vehicles. To operate this networks, alongside with coordinated control, information technology and measurement equipment, the power conditioning plays a crucial role for control purposes and power flow management. Inverters that interface the renewable energy generators or electric vehicles or storage systems or active power filters can be used to this end. The power involved in this sector can be high, for example in Virtual Power Plants.

The research project aims to explore the problems and perspectives of different architectures of converters whose characteristics can be particularly promising for Smart Grid, with particular emphasis on multi-level and matrix converter topology.

In fact the multilevel technology allows, with same power and current, to split the voltage on different static switches while improving the quality of the voltage produced.

The matrix converter has no intermediate dc link capacitors, due to this reason it is easy to develop a reliable structure with space and weight saving. Even in this architecture, the output voltage is multilevel. Moreover the input current is an high quality current, the power flow is totally bidirectional and the converter offers the possibility to control the input power factor (i.e. possibility to participate to active and reactive power regulations).

A general analysis of multilevel inverters was conducted with particular attention to modulation strategies. It was demonstrated that, the SVM and PWM techniques are equivalent. The order and the distance between the three modulating signals in PWM correspond to a specific sector in SVM approach. The shift of the three modulating signals corresponds to different choices of the switching configuration for vectors that have multiplicity. The different configurations were analyzed in detail.

The Diode Clamped Inverter was studied. Its structure is not modular, and for this reason an increase of the levels over a certain number is not feasible. One of the main task of the control system is to keep balanced the DC capacitors and avoid unacceptable oscillations. The analysis was validated through simulations models.

Cascaded Inverter was the second topology analyzed. Its structure is totally modular but each module needs an insulated DC source. This is not compatible with all applications, but can be used,

for example, with photovoltaic generators and electric vehicles. The study was assessed with simulations results as well.

An innovative multi-level architecture, called MMC (Modular Multilevel Converter) was analyzed in detail. The inverter structure is modular, this results in design flexibility, allows to reach high voltages and guarantees system reliability. First of all, a mathematical model for the single leg was developed and the equations were manipulated to obtain a suitable control form. Then, different control systems were developed and validated trough simulation results. The control system has the objective to track the reference current and keep balanced the upper and lower capacitors.

It was realized an experimental setup of the single leg MMC at LEMAD laboratory. The experimental results obtained with the different control system were presented and discussed.

It was then studied the three-phase configuration. A control system based on space vector and zero sequence transformation was developed and validated trough simulation models.

Finally the back to back MMC configuration was analyzed. This configuration is suitable for HVDC lines and offshore wind power generation. A control system was developed and validated trough simulation models, as well.

The last part of the thesis is focused on the research activity conducted at “The University of Nottingham” on Matrix converters. In particular, fault detection algorithms and diagnostic methods were analyzed and compared. A control system was implemented with particular attention to fast data acquisition and diagnostic capability. Experimental results of the realized control system, obtained with the equipment available in Nottingham laboratory, were shown.

Bibliography

[1] N. Hatziargyriou, H. Asano, R. Iravani, C. Marnay, "Microgrids," IEEE Power & Energy Magazine, July/August 2007 The Smart Grid: An introduction, publication sponsored by US DOE's Office of Electricity Delivery and Energy Reliability, 2009.

[2] Jinquan Zhao, Wenying Huang, Zhaoxiong Fang, Feng Chen, Kewen Li and Yong Deng, "On-Line Voltage Stability Monitoring and Control (VSMC) System in Fujian Power Grid," in Proc. Power Engineering Society General Meeting, 2007.

[3] W. Kempton and J. Tomic, "Vehicle-to-Grid Power Fundamentals: Calculating Capacity and Net Revenue," J. Power Sources, vol. 144, no. 1, pp. 268–279, Jun. 2005.

[4] N. J. Gil and J. A. P. Lopes, "Hierarchical Frequency Control Scheme for Islanded Multi-Microgrids Operation," in Proc. IEEE Lausanne Power Tech., Lausanne, Switzerland, Jul. 2007, pp. 473–478.

[5] J. A. P. Lopes, P. M. R. Almeida, and F. J. Soares, "Using Vehicle-to-Grid to Maximize the Integration of Intermittent Renewable Energy Resources in Islanded Electric Grids," in Proc. Int. Conf. Clean Electr. Power Renewable Energy Resources Impact, Capri, Italy, pp. 290–295, Jun. 2009.

[6] J. A. P. Lopes, C. L. Moreira, and F. O. Resende, "Microgrids Black Start and Islanded Operation," in Proc. 15th Power Syst. Comput. Conf., Liege, Belgium, pp. 1–7, Aug. 22–26, 2005.

[7] Sanmin Wei, "A General SVPWM Control Algorithm for Multilevel Inverters," IEEE, 2003(3): pp. 24-30.

[8] Sun Chi, Bi Zengjun, Wei Guanghui, "Modeling and Simulation of a Three-Phase Four-Leg Inverter Based on a Novel Decoupled Control Technique[J]," in Proc. CSEE, 2004, 24(1): pp. 124-130.

[9] Li Zhi-min, Zhang Yu-jie. Synchronous Motor Variable Speed System [M]. Beijing: Mechanism Industry Press, 1996.

[10] J. S. Lai and F. Z. Peng, "Multilevel Converters - A New Breed of Power Converters," IEEE Trans. on Ind. Applicat., vol. 32, pp. 509 -517 1996.

[11] L. Tolbert, F.-Z. Peng, and T. Habetler, "Multilevel Converters for Large Electric Drives," IEEE Trans. on Ind. Applicat., vol. 35, pp. 36 -44 1999.

[12] R. Teodorescu, F. Beaabjerg, J. K. Pedersen, E. Cengelci, S. Sulistijo, B. Woo, and P. Enjeti, "Multilevel Converters - A Survey," in Proc. European Power Electronics Conf. (EPE',99), 1999.

[13] A. Nabae, I. Takahashi, and H. Akagi, "A New Neutral-Point Clamped PWM Inverter," IEEE Trans. on Ind. Applicat., vol. IA-17, pp.518 -523, 1981.

[14] T. A. Meynard and H. Foch, "Multi-Level Choppers for High Voltage Applications," in Eur. Power Electron. Drives J., vol. 2, no. 1, pp. 45-50 1992.

[15] C. Hochgraf, R. Lasseter, D. Divan, and T. A. Lipo, "Comparison of Multilevel Inverters for Static Var Compensation," in Conf. Rec. IEEE-IAS Annu. Meeting, pp.921 -928, 1994.

[16] P. Hammond, "A New Approach to Enhance Power Quality for Medium Voltage Ac Drives", IEEE Trans. on Ind. Applicat., vol. 33, pp.202 -208, 1997.

[17] E. Cengelci, S. U. Sulistijo, B. O. Woom, P. Enjeti, R. Teodorescu, and F. Blaabjerge, "A New Medium Voltage PWM Inverter Topology for Adjustable Speed Drives," in Conf. Rec. IEEE-IAS Annu. Meeting, pp.1416 -1423, 1998.

[18] J. Rodriguez, J. S. Lai, F. Z. Peng, "Multilevel Inverters: A Survey of Topologies, Controls, and Applications," IEEE Trans. on Ind. Electronics, vol. 49, no. 4, pp. 724-738, August 2002.

[19] T. A. Meynard, H. Foch, P. Thomas, J. Courault, R. Jakob, and M. Nahrstaedt, "Multicell Converters: Basic Concepts and Industry Applications," IEEE Trans. on Ind. Electron., vol. 49, no. 5, pp. 955–964, Oct. 2002.

[20] Lesnicar, R. Marquardt, "A New Modular Voltage Source Inverter Topology," in Proc. EPE 2003, Toulouse, France, September 2-4, 2003, pp. 1-10.

[21] H. Akagi, "Classification, Terminology, and Application of the Modular Multilevel Cascade Converter (MMCC)," IEEE Trans. on Power Electronics, vol. 26, no.11, pp. 3119 - 3130, Nov. 2011.

[22] M. Glinka, R. Marquardt, "A New AC/AC Multilevel Converter Family," IEEE Transactions on Industrial Electronics, vol. 52, no. 3, June 2005, pp. 662-669.

[23] B. Gemmel, J. Dorn, D. Retzmann, and D. Soerangr, "Prospects of Multilevel VSC Technologies for Power Transmission," in Conf. Rec. IEEE-TDCE 2008, pp. 1-16.

[24] M. Hagiwara, H. Akagi "Control and Experiment of Pulse Width Modulated Modular Multilevel Converters," IEEE Trans. on Power Electronics, Vol. 24, No. 7, July 2009, pp. 1737-1746.

[25] Antonopoulos, L. Angquist, and H.-P. Nee, "On Dynamics and Voltage Control of the Modular Multilevel Converter," in Proc. of EPE'09, Barcelona, Spain, September 8-10, 2009, pp. 1-10.

[26] G. Bergna, M. Boyra, J. H. Vivas, “Evaluation and Proposal of MMC HVDC Control Strategies Under Transient and Steady State Conditions,” in Proc. of EPE'11, Birmingham, UK, Sept. 2011, pp. 1-10.

[27] P. Munch, S. Liu, M. Dommaschk, “Modeling and Current Control of Modular Multilevel Converters Considering Actuator and Sensor Delays,” in Proc. IECON 2009, Porto, Portugal, Nov. 3-5, 2009, pp. 1633-1638.

[28] L. Ängquist, A. Antonopoulos, D. Siemaszko, K. Ilves, M. Vasiladiotis, H. P. Nee, “Open-Loop Control of Modular Multilevel Converters Using Estimation of Stored Energy,” IEEE Trans. on Ind. Appl., vol. 47, no. 6, Nov./Dec. 2011, pp. 2516-2524.

[29] S. Rohner, J. Weber, S. Bernet “Continuous Model of Modular Multilevel Converter with Experimental Verification,” in ECCE 2011, Phoenix, USA, Sept. 2011, pp. 4021-4028.

[30] M. Hagiwara, R. Maeda, H. Akagi, “Control And Analysis of the Modular Multilevel Cascade Converter Based on Double-Star Chopper-Cells (MMCC-DSCC),” IEEE Trans. on Power Electronics, Vol. 26, No. 6, June 2011, pp. 1649-1658.

[31] L. Harnefors, A. Antonopoulos, S. Norrga, L. Ängquist, Hans-Peter Nee, “Dynamic Analysis of Modular Multilevel Converters,” IEEE Trans. on Industrial Electronics, Vol. 60, No. 7, July 2013, pp. 2526- 2537.

[32] G. Bergna, E. Berne, P. Egrot, P. Lefranc, A. Arzandé, J. C. Vannier, M. Molinas, “An Energy-Based Controller for HVDC Modular Multilevel Converter in Decoupled Double Synchronous Reference Frame for Voltage Oscillation Reduction, ” IEEE Trans. on Industrial Electronics, Vol. 60, No. 6, June 2013, pp. 2360-2371.

[33] S. Norrga, L. Ängquist, K. Ilves, L. Harnefors and H.-P. Nee, “Decoupled Steady-State Model of the Modular Multilevel Converter with Half-Bridge Cells,” in PEMD 2012, Bristol, UK, 27-29 Mar. 2012, pp. 1-6.

[34] R. Teodorescu, F. Blaabjerg, M. Liserre, P.C. Loh, “Proportional Resonant Controllers and Filters for Grid-Connected Voltage-Source Converters,” IEE Electric Power Applications, Vol. 156, No. 5, Sept. 2006, pp. 750-762.

[35] S. V. Garcia Oliveira and Y. R. de Novaes, L. M Cunico, G. L.ambert, Rodrigo P. Dacol, “Parameters Design for Modular Multilevel Converter (MMC),” 2013 in Brazilian Power Electronics Conference (COBEP), Gramado, Brasil, 27-31 Oct. 2013, pp. 264 – 270.

[36] L. Xu, B.R. Andersen and P. Cartwright, “Multilevel Converter Based VSC Transmission Operating Under Fault AC Conditions,” in Proc IEE Gener Transm. and Distr., Vol. 152, No. 2, Mar. 2005.

[37] N. Flourentzou, V.G. Agelidis and G.D. Demetriades, "VSC-Based HVDC Transmission Systems: an Overview," IEEE Trans. on Power Electron., vol. 24, No. 3, Mar. 2009, pp. 592-602.

[38] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L.G. Franquelo, B. Wu, J. Rodriguez, M.A. Perez, J.I. Leon. "Recent Advances and Industrial Applications of Multilevel Converters," IEEE Trans. on Ind. Elect., 2010, vol. 57, No. 8, pp. 2553-2580.

[39] Yazdani, R. Iravani, "A Unified Model and Control for the Voltage Source Converter Under Unbalanced Grid Conditions," IEEE Trans. on Power Delivery, Vol. 21, No. 3, July 2006, pp. 1620-1629.

[40] M. Saeedifard and R. Iravani, "Dynamic Performance of a Modular Multilevel Back-To-Back HVDC System," IEEE Trans. on Power Delivery, vol. 25, pp. 2903-2912, 2010.

[41] Lesnicar and R. Marquardt, "An Innovative Modular Multilevel Converter Topology Suitable for a Wide Power Range," in Proc. of IEEE PowerTech Conf., 2003, pp. 6.

[42] M. Glinka, "Prototype of Multiphase Modular-Multilevel-Converter with 2 MW Power Rating and 17-Level-Output-Voltage," in IEEE PESC 2004, pp. 2572-2576.

[43] S. Allebrod, R. Hamerski, R. Marquardt, "New Transformerless, Scalable Modular Multilevel Converters for HVDC Transmission," in Proc. of IEEE Power Electron. Spec. Conf., PESC, 2008, pp. 174-179.

[44] G.S. Konstantinou, V. G. Agelidis "Performance Evaluation of Halfbridge Cascaded Multilevel Converters Operated with Multicarrier Sinusoidal PWM Techniques," in IEEE ICIEA 2009, pp. 3399-3404.

[45] S. Rohner, S. Bernet, M. Hiller and R. Sommer "Modulation, Losses and Semiconductor Requirements of Modular Multilevel Converters," IEEE Trans. on Ind. Electr., 2010, Vol. 57, No. 8, pp.2633-2642.

[46] U. N. Gnanarathna, A. M. Gole, and R. P. Jayasinghe, "Efficient Modeling of Modular Multilevel HVDC Converters (MMC) on Electromagnetic Transient Simulation Programs," IEEE Trans. on Power Delivery, vol. 26, pp. 316-324, 2011.

[47] G. Konstantinou, M. Ciobotaru and V.G. Agelidis, "Operation of a Modular Multilevel Converter with Selective Harmonic Elimination PWM," in ICPE&ECCE Asia, Jeju, Korea, May 2011, pp. 999–1004.

[48] K. Ilves, A. Antonopoulos, S. Norrga, and H-P. Nee, "A New Modulation Method for the Modular Multilevel Converter Allowing Fundamental Switching Frequency," in ICPE&ECCE Asia, Jeju, Korea, May 2011, pp. 991–998.

[49] L. Angquist, A. Antonopoulos, D. Siemaszko, K. Ilves, M. Vasiladiotis and H.P. Nee “Inner Control of Modular Multilevel Converters - An Approach Using Open-Loop Estimation of Stored Energy,” in IEEE Int. Power Electronics Conference IPEC, 2010, 1579-1585.

[50] Q. Tu and Z. Xu, ”Impact Of Sampling Frequency On Harmonic Distortion For Modular Multilevel Converter,” IEEE Trans. on Power Delivery, vol. 26, pp. 298-306, 2011.

[51] Q. Tu, Z. Xu and L. Xu ”Reduced Switching-Frequency Modulation and Circulating Current Suppression for Modular Multilevel Converters,” IEEE Trans. on Power Delivery, Early access.

[52] J. Qin and M. Saeedifard "Predictive Control of a Modular Multilevel Converter for a Back-To-Back HVDC System", IEEE Trans. on Power Del., vol. 27, no. 3, pp.1538 -1547, 2012.

[53] S. P. Engel and R. W. D. Doncker "Control of the Modular Multi-Level Converter for Minimized Cell Capacitance," in Proc. Eur. Conf. Power Electron. Appl., pp.1 -10 2011.

[54] Alesina and M. Venturini, “Solid-State Power Conversion: A Fourier Analysis Approach to Generalized Transformer Synthesis,” IEEE Trans. on Circuits Syst., vol. CAS-28, pp. 319–330, Apr. 1981.

[55] M. J. Maytum and D. Colman, “The Implementation and Future Potential of the Venturini Converter,” in Proc. Drives, Motors Controls, 1983, pp.108–117.

[56] Alesina and M. G. B. Venturini, “Analysis and Design of Optimum Amplitude Nine-Switch Direct AC–AC Converters,” IEEE Trans on Power Electron., vol. 4, pp. 101–112, Jan. 1989.

[57] G. Roy and G. E. April, “Cycloconverter Operation Under A New Scalar Control Algorithm,” in Proc. IEEE PESC’89, Milwaukee, WI, 1989, pp. 368–375.

[58] P. D. Ziogas, S. I. Khan, and M. H. Rashid, “Analysis and Design of Forced Commutated Cycloconverter Structures with Improved Transfer Characteristics,” IEEE Trans. on Ind. Electron., vol. 1E-33, pp. 271–280, Aug. 1986.

[59] L. Huber and D. Borojevic, “Space Vector Modulator for Forced Commutated Cycloconverters,” in Conf. Rec. IEEE-IAS Annual Meeting, vol. 1, 1989, pp. 871–876.

[60] L. Huber and D. Borojevic, “Space Vector Modulation with Unity Input Power Factor for Forced Commutated Cycloconverters,” in Conf. Rec. IEEE-IAS Annual Meeting, 1991, pp. 1032–1041.

[61] D. Casadei, G. Grandi, G. Serra, and A. Tani, “Space Vector Control of Matrix Converters with Unity Input Power Factor and Sinusoidal Input/Output Waveforms,” in Proc. EPE Conf., vol. 7, Brighton, U.K., Sept. 13–16, 1993, pp. 170–175.

[62] D. Casadei, G. Serra, and A. Tani, “Reduction of the Input Current Harmonic Content in Matrix Converters Under Input/Output Unbalance,” IEEE Trans. on Ind. Electron., vol. 45, pp. 401–411, June 1998.

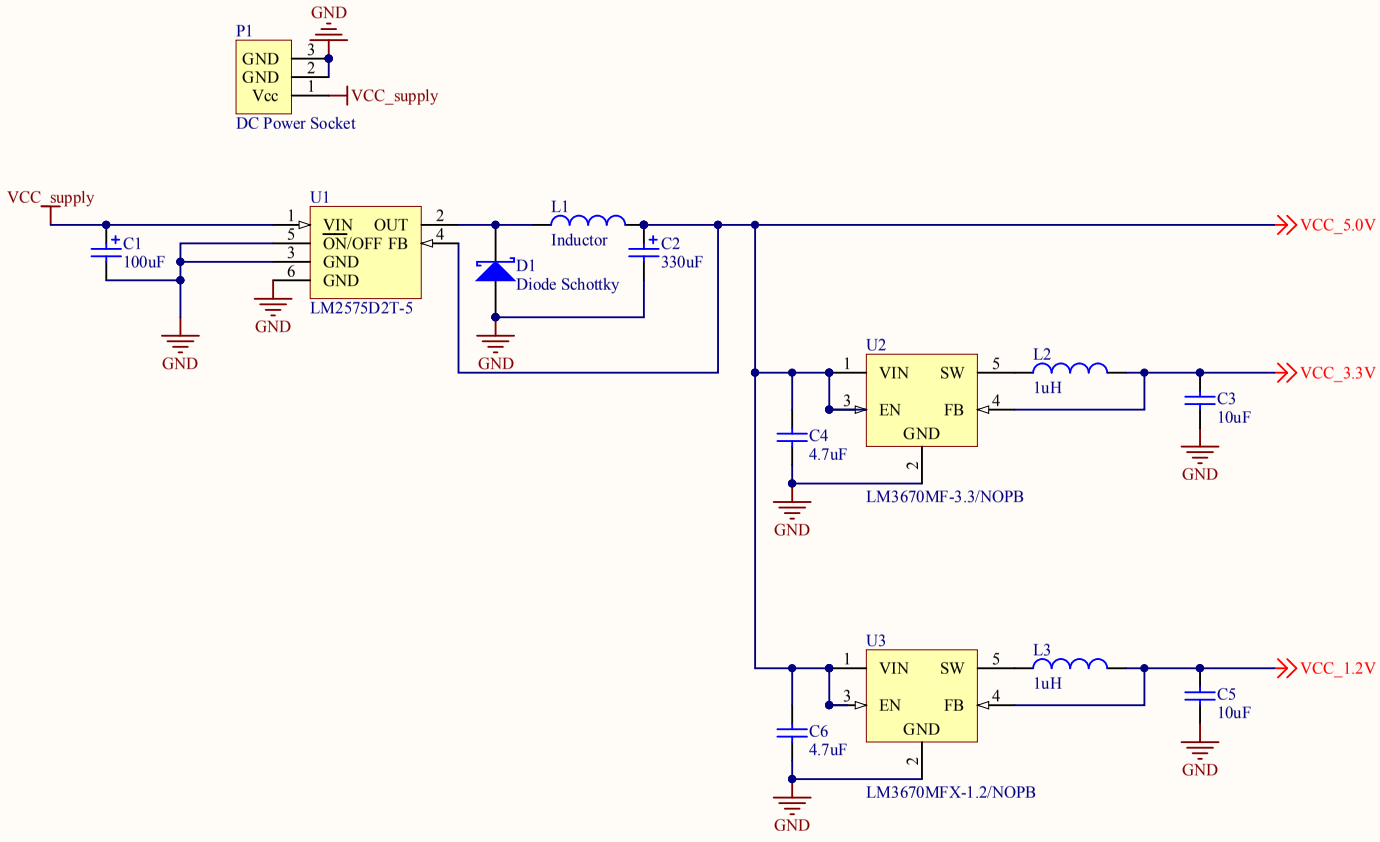
[63] O. Simon and M. Braun, “Theory of Vector Modulation for Matrix Converters,” in Proc. EPE Conf., Graz, Austria, Aug. 27–29, 2001.

[64] S. Khwan-on , L. de Lillo , L. Empringham and P. Wheeler "Fault-Tolerant Matrix Converter Motor Drives with Fault Detection of Open Switch Faults," IEEE Trans. on Ind. Electron., vol. 59, no. 1, pp.257 -268, 2012.

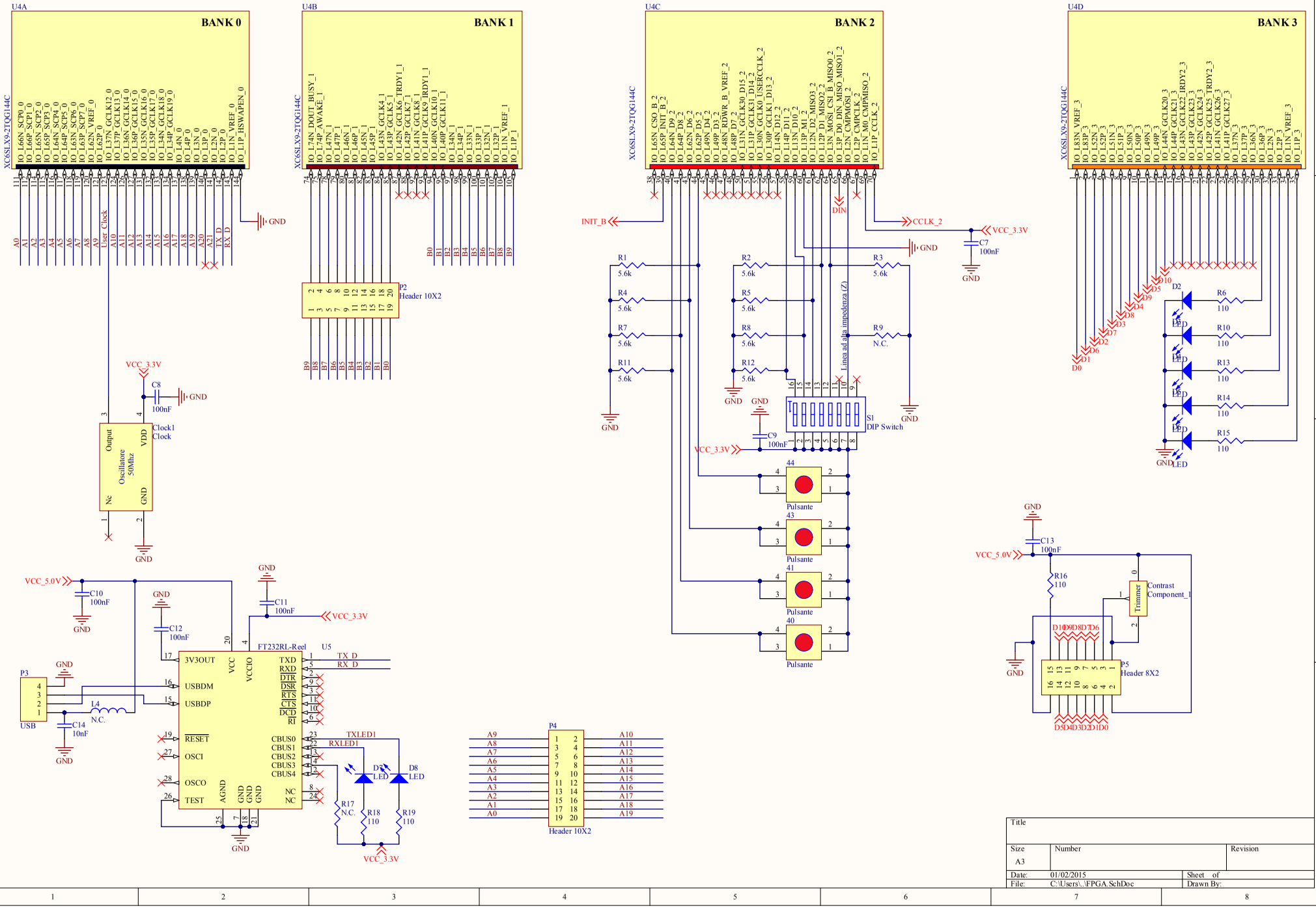
[65] P. W. Wheeler , J. Rodriguez , J. C. Clare and L. Empringham "Matrix Converter: A Technology Review," IEEE Trans. on Ind. Electron., vol. 49, no. 2, pp.276 -288, 2002.

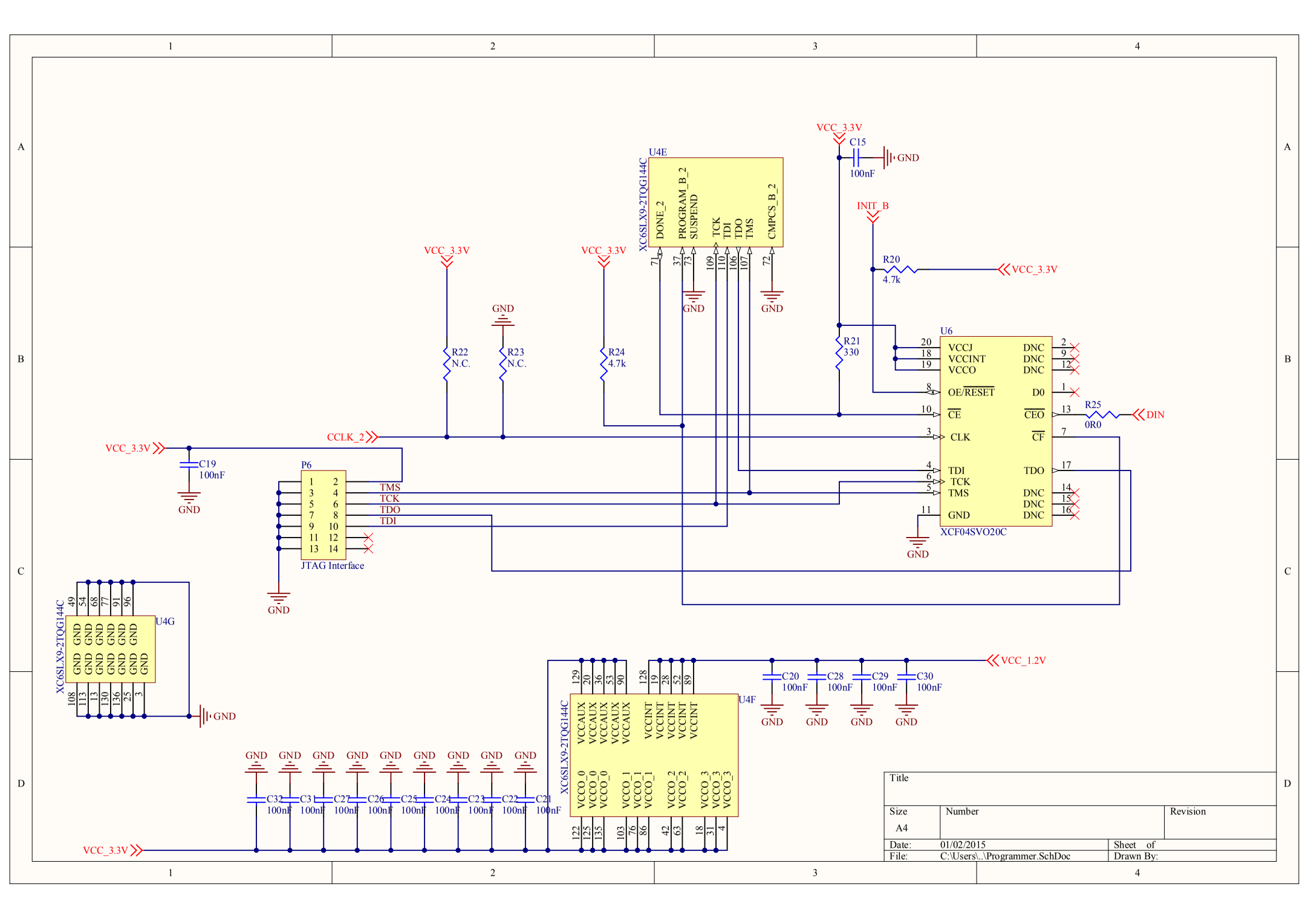
[66] S. Kwak and H. A. Toliyat "An Approach to Fault-Tolerant Three-Phase Matrix Converter Drives," IEEE Trans. on Energy Convers., vol. 22, no. 4, pp.855 -863 2007.

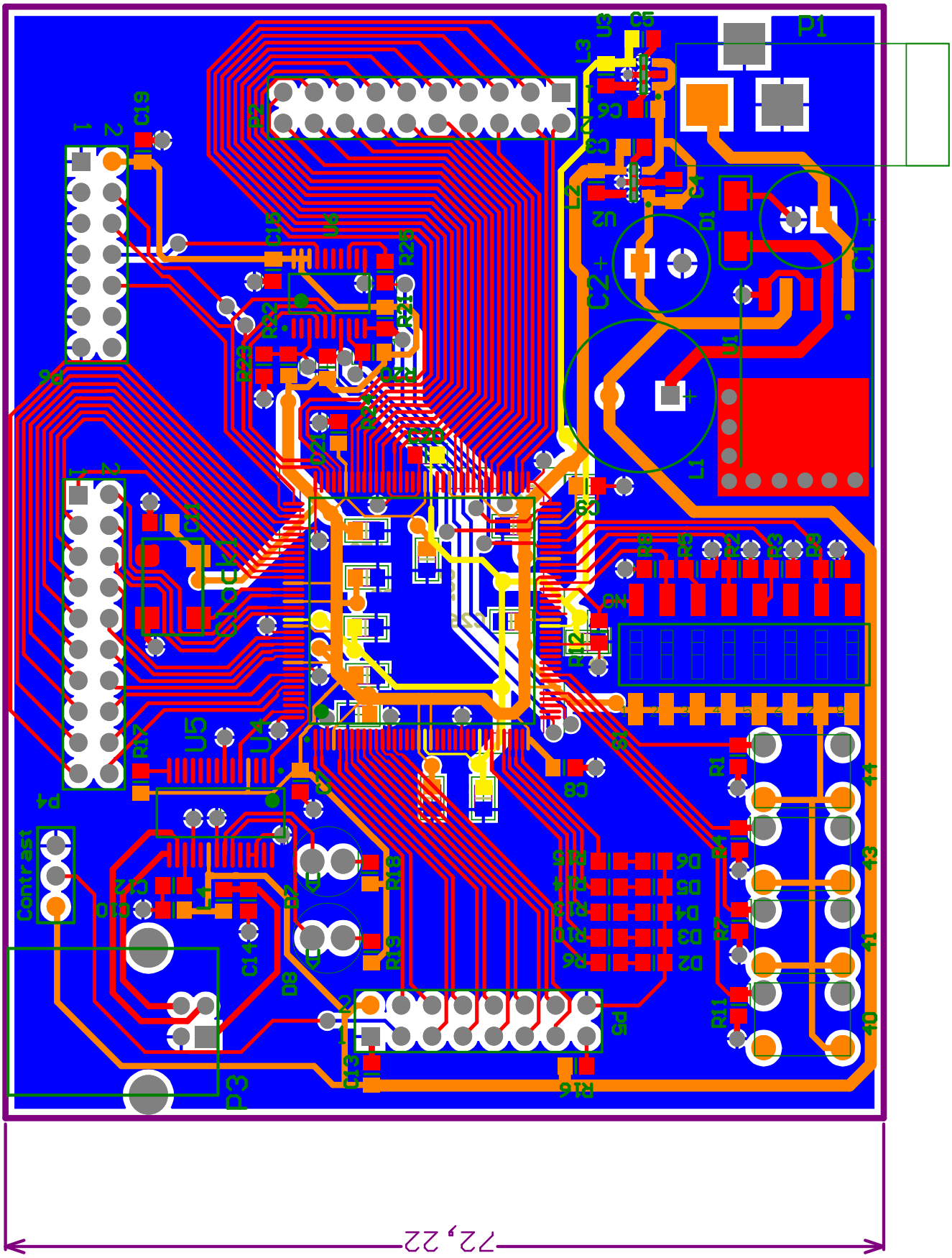
Appendix I – Hardware

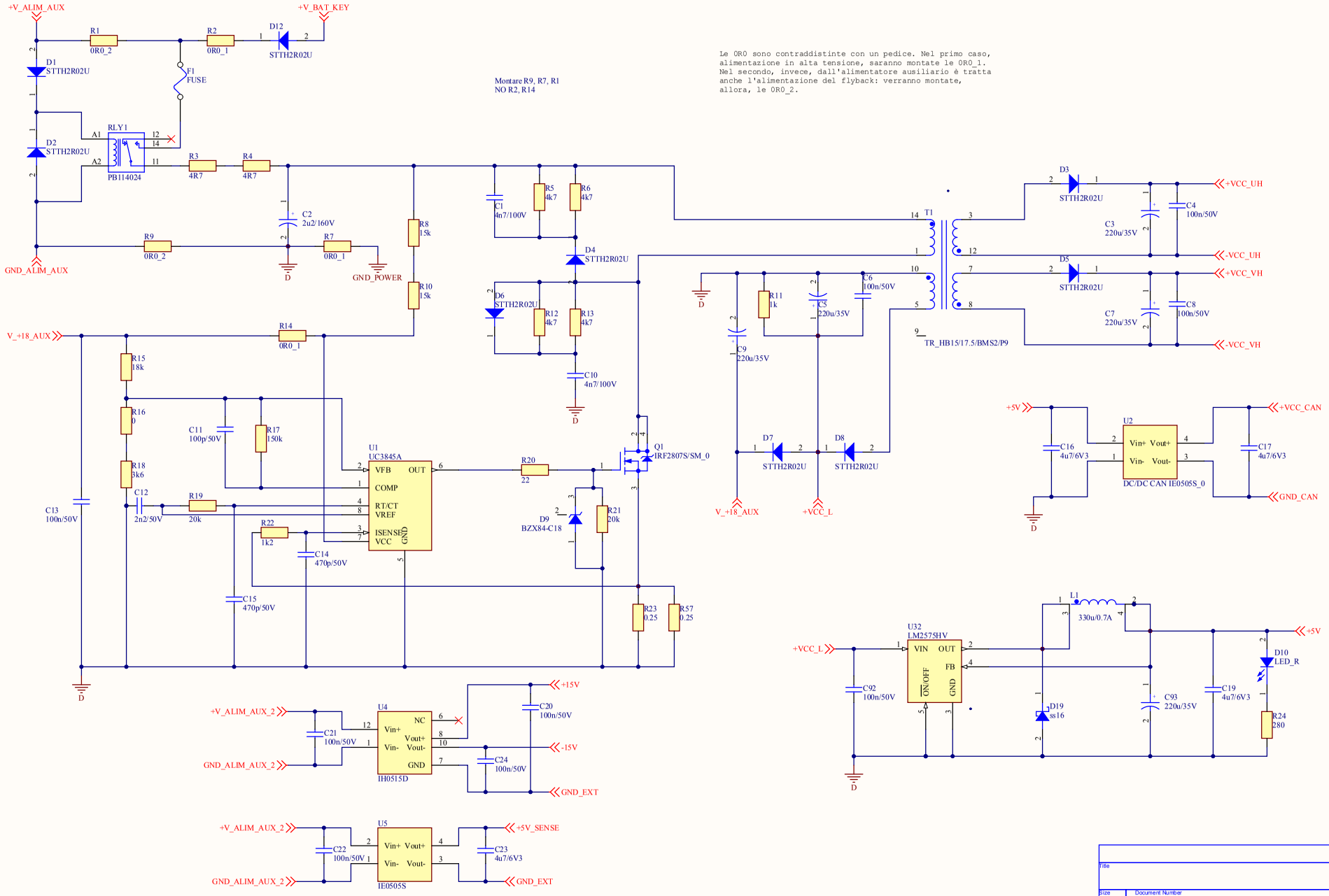


Title		
Size: A4	Number	Revision
Date: 01/02/2015		Sheet of
File: C:\Users\..\Alimentazione.SchDoc		Drawn By:

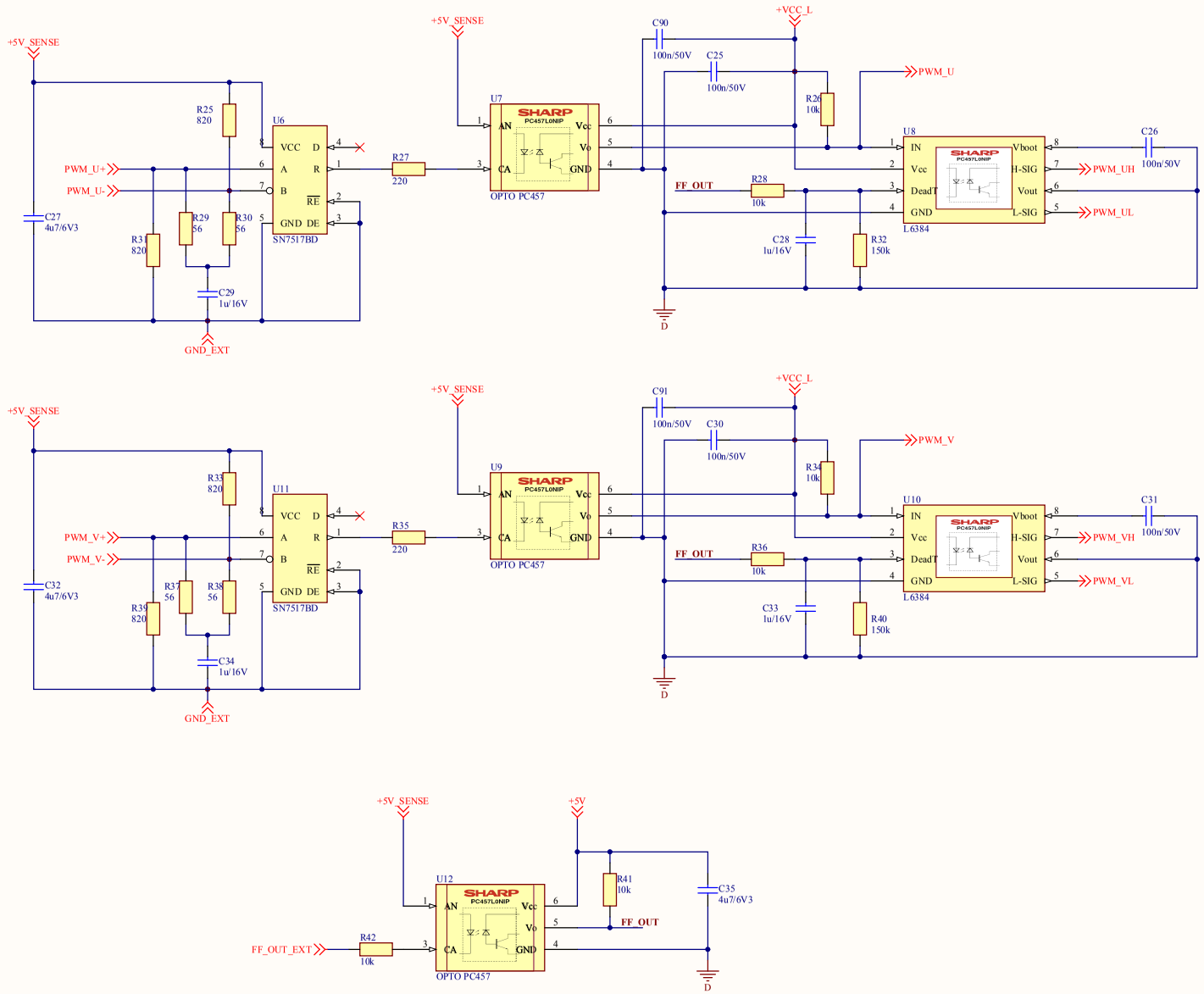

U4A
BANK 0
XC6SLX9-2TQG144C
IO_L66N_SCP0_0
IO_L66P_SCP1_0
IO_L65N_SCP2_0
IO_L65P_SCP3_0
IO_L64N_SCP4_0
IO_L64P_SCP5_0
IO_L63N_SCP6_0
IO_L63P_SCP7_0
IO_L62P_0
IO_L62N_VREF_0
IO_L37N_GCLK12_0
IO_L37P_GCLK13_0
IO_L36N_GCLK14_0
IO_L36P_GCLK15_0
IO_L35N_GCLK16_0
IO_L35P_GCLK17_0
IO_L34N_GCLK18_0
IO_L34P_GCLK19_0
IO_L4N_0
IO_L4P_0
IO_L3N_0
IO_L3P_0
IO_L2N_0
IO_L2P_0
IO_L1N_VREF_0
IO_L1P_HSWAPEN_0
A0
A1
A2
A3
A4
A5
A6
A7
A8
User Clock
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
A20
A21
TX_D
RX_D
GND
U4B
BANK 1
XC6SLX9-2TQG144C
IO_L74N_DOUT_BUSY_1
IO_L74P_AWAKE_1
IO_L47N_1
IO_L47P_1
IO_L46N_1
IO_L46P_1
IO_L45N_1
IO_L45P_1
IO_L43N_GCLK4_1
IO_L43P_GCLK5_1
IO_L42N_GCLK6_TRDY1_1
IO_L42P_GCLK7_1
IO_L41N_GCLK8_1
IO_L41P_GCLK9_IRDY1_1
IO_L40N_GCLK10_1
IO_L40P_GCLK11_1
IO_L34N_1
IO_L34P_1
IO_L33N_1
IO_L33P_1
IO_L32N_1
IO_L32P_1
IO_L1N_VREF_1
IO_L1P_1
B0
B1
B2
B3
B4
B5
B6
B7
B8
B9
P2
Header 10X2
U4C
BANK 2
XC6SLX9-2TQG144C
IO_L65N_CSO_B_2
IO_L65P_INIT_B_2
IO_L64N_D9_2
IO_L64P_D8_2
IO_L62N_D6_2
IO_L62P_D5_2
IO_L49N_D4_2
IO_L49P_D3_2
IO_L48N_RDWR_B_VREF_2
IO_L48P_D7_2
IO_L31N_GCLK30_D15_2
IO_L31P_GCLK31_D14_2
IO_L30N_GCLK0_USERCCLK_2
IO_L30P_GCLK1_D13_2
IO_L14N_D12_2
IO_L14P_D11_2
IO_L13N_D10_2
IO_L13P_M1_2
IO_L12N_D2_MISO3_2
IO_L12P_D1_MISO2_2
IO_L3N_MOSI_CSI_B_MISO0_2
IO_L3P_D0_DIN_MISO_MISO1_2
IO_L2N_CMPMOSI_2
IO_L2P_CMPCLK_2
IO_L1N_M0_CMPMISO_2
IO_L1P_CCLK_2
INIT_B
DIN
CCLK_2
VCC_3.3V
GND
C7
100nF
R1
R2
R3
R4
R5
R6
R7
R8
R9
R11
R12
5.6k
N.C.
Linea ad alta impedenza (Z)
S1
DIP Switch
C9
100nF
Pulsante
44
43
41
40
U4D
BANK 3
XC6SLX9-2TQG144C
IO_L83N_VREF_3
IO_L83P_3
IO_L52N_3
IO_L52P_3
IO_L51N_3
IO_L51P_3
IO_L50N_3
IO_L50P_3
IO_L49N_3
IO_L49P_3
IO_L44N_GCLK20_3
IO_L44P_GCLK21_3
IO_L43N_GCLK22_IRDY2_3
IO_L43P_GCLK23_3
IO_L42N_GCLK24_3
IO_L42P_GCLK25_TRDY2_3
IO_L41N_GCLK26_3
IO_L41P_GCLK27_3
IO_L37N_3
IO_L37P_3
IO_L36N_3
IO_L36P_3
IO_L2N_3
IO_L2P_3
IO_L1N_VREF_3
IO_L1P_3
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
LED
R10
R13
R14
R15
110
GND_LED
C8
100nF
Clock1
Clock
Output
Oscillatore
50Mhz
VDD
Nc
C10
100nF
C11
100nF
C12
100nF
C13
100nF
VCC_5.0V
FT232RL-Reel
U5
3V3OUT
VCC
VCCIO
TXD
RXD
DTR
DSR
RTS
CTS
DCD
RI
TX_D
RX_D
USBDM
USBDP
RESET
OSCI
OSCO
TEST
AGND
CBUS0
CBUS1
CBUS2
CBUS3
CBUS4
NC
TXLED1
RXLED1
P3
USB
L4
N.C.
C14
10nF
D7
D8
R17
R18
R19
110
P4
Header 10X2
R16
Trimmer
Contrast
Component_1
P5
Header 8X2
Title
Size
A3
Number
Revision
Date:
01/02/2015
File:
C:\Users\..\FPGA.SchDoc
Sheet of
Drawn By:


U4E
XC6SLX9-2TQG144C
DONE_2
PROGRAM_B_2
SUSPEND
TCK
TDI
TDO
TMS
CMPCS_B_2
VCC_3.3V
C15
100nF
GND
INIT_B
R20
4.7k
R21
330
R22
N.C.
R23
N.C.
R24
4.7k
U6
XCF04SVO20C
VCCJ
VCCINT
VCCO
OE/RESET
CE
CLK
TDI
TCK
TMS
GND
D0
CEO
CF
TDO
DNC
R25
0R0
DIN
CCLK_2
C19
100nF
P6
JTAG Interface
TMS
TCK
TDO
TDI
U4G
U4F
VCCAUX
VCCINT
VCCO_0
VCCO_1
VCCO_2
VCCO_3
C20
C28
C29
C30
100nF
VCC_1.2V
C32
C3
C27
C26
C25
C24
C23
C22
C21
Title
Size
A4
Number
Revision
Date:
01/02/2015
Sheet of
File:
C:\Users\..\Programmer.SchDoc
Drawn By:

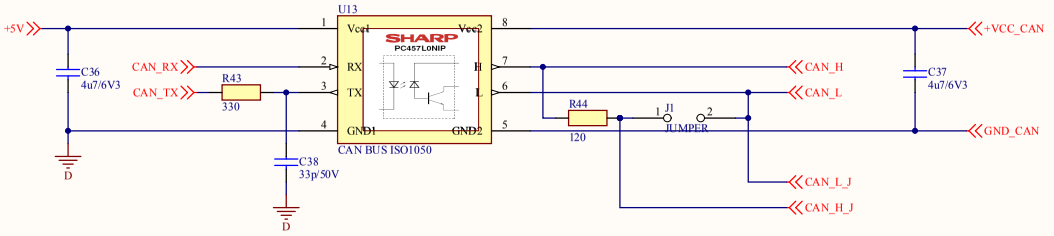

72,22



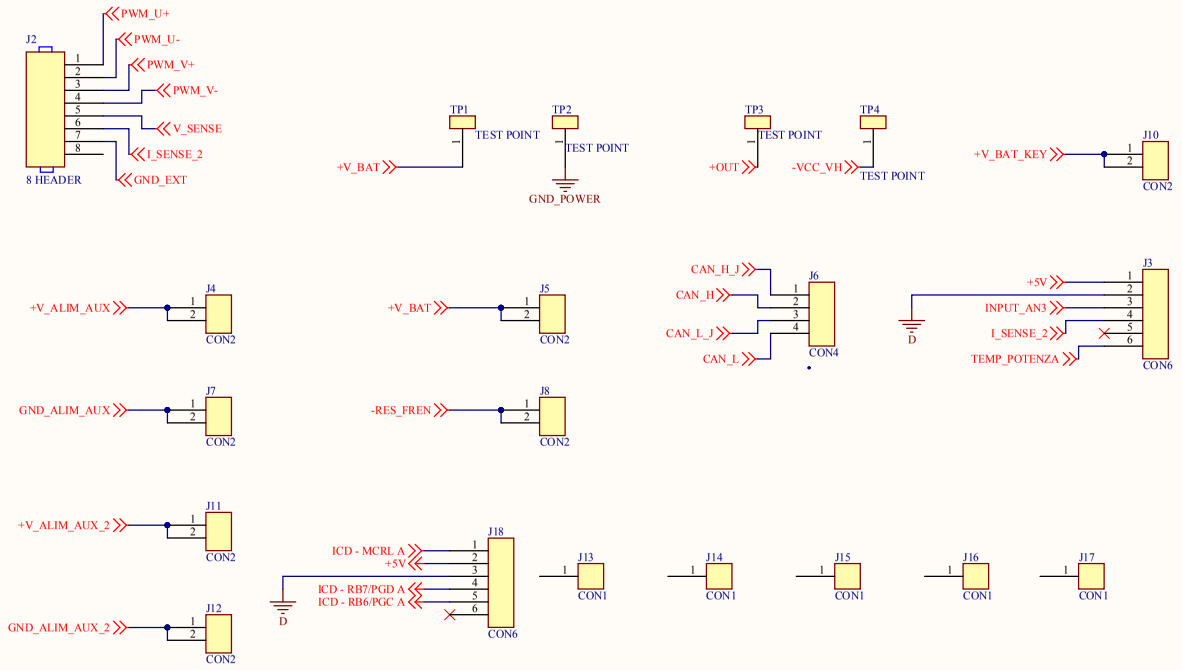
Title			
Size	Document Number		Rev
Date:		Sheet 6 of	



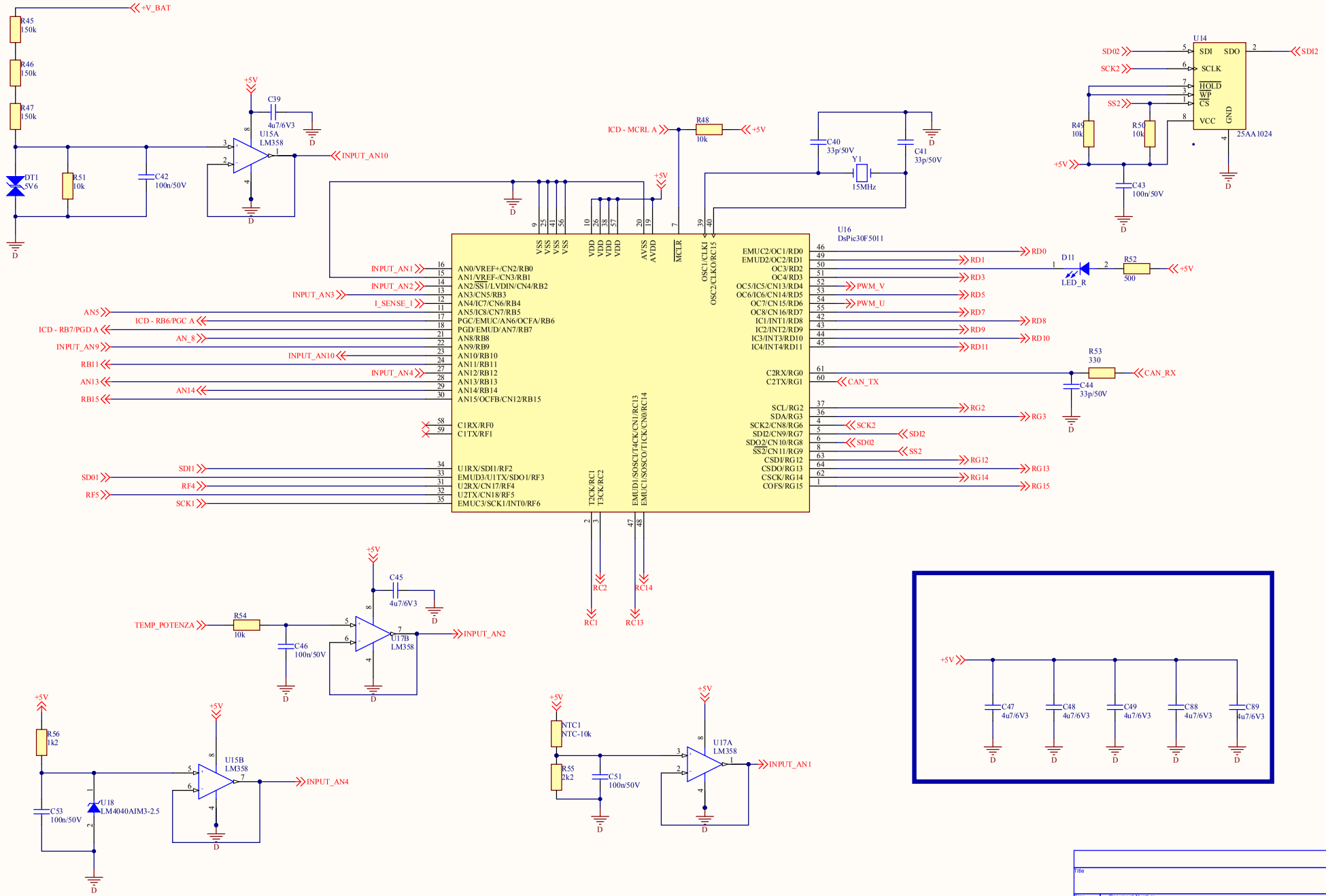
Title	
Size	Document Number
Rev	•
Date: •	Sheet 6 of 48

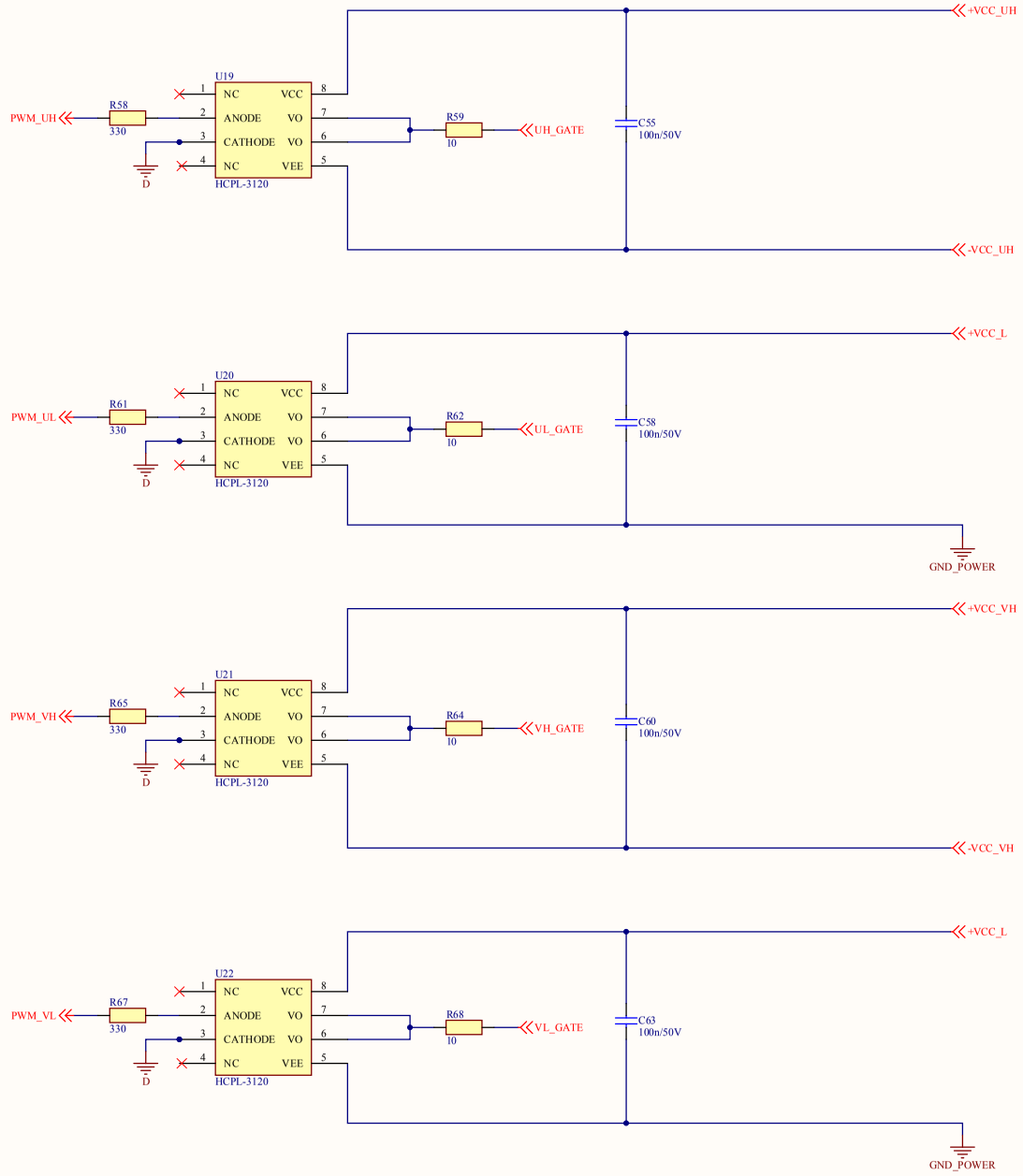


Title		
Size	Document Number	Rev
Date:	Sheet 6 of	

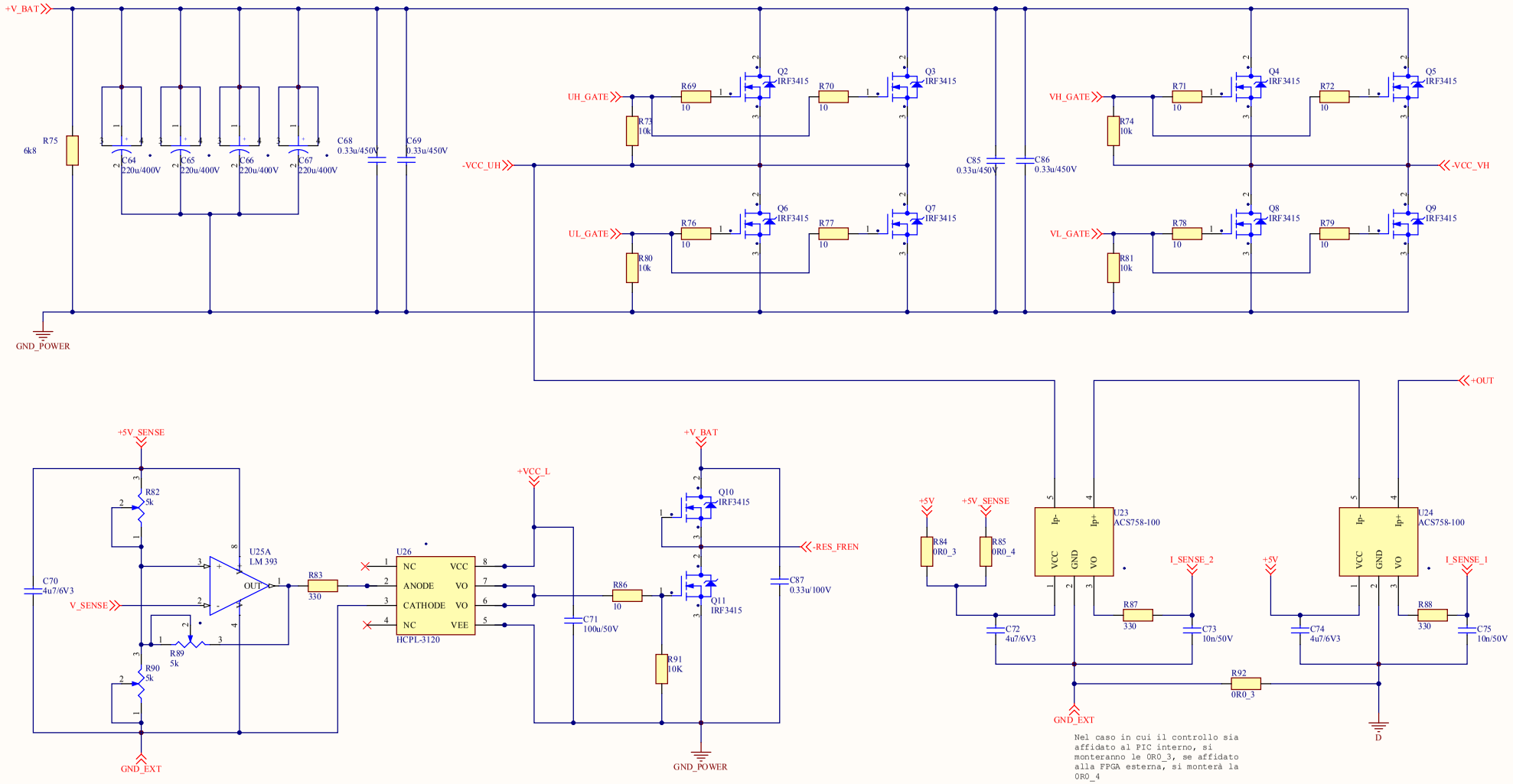


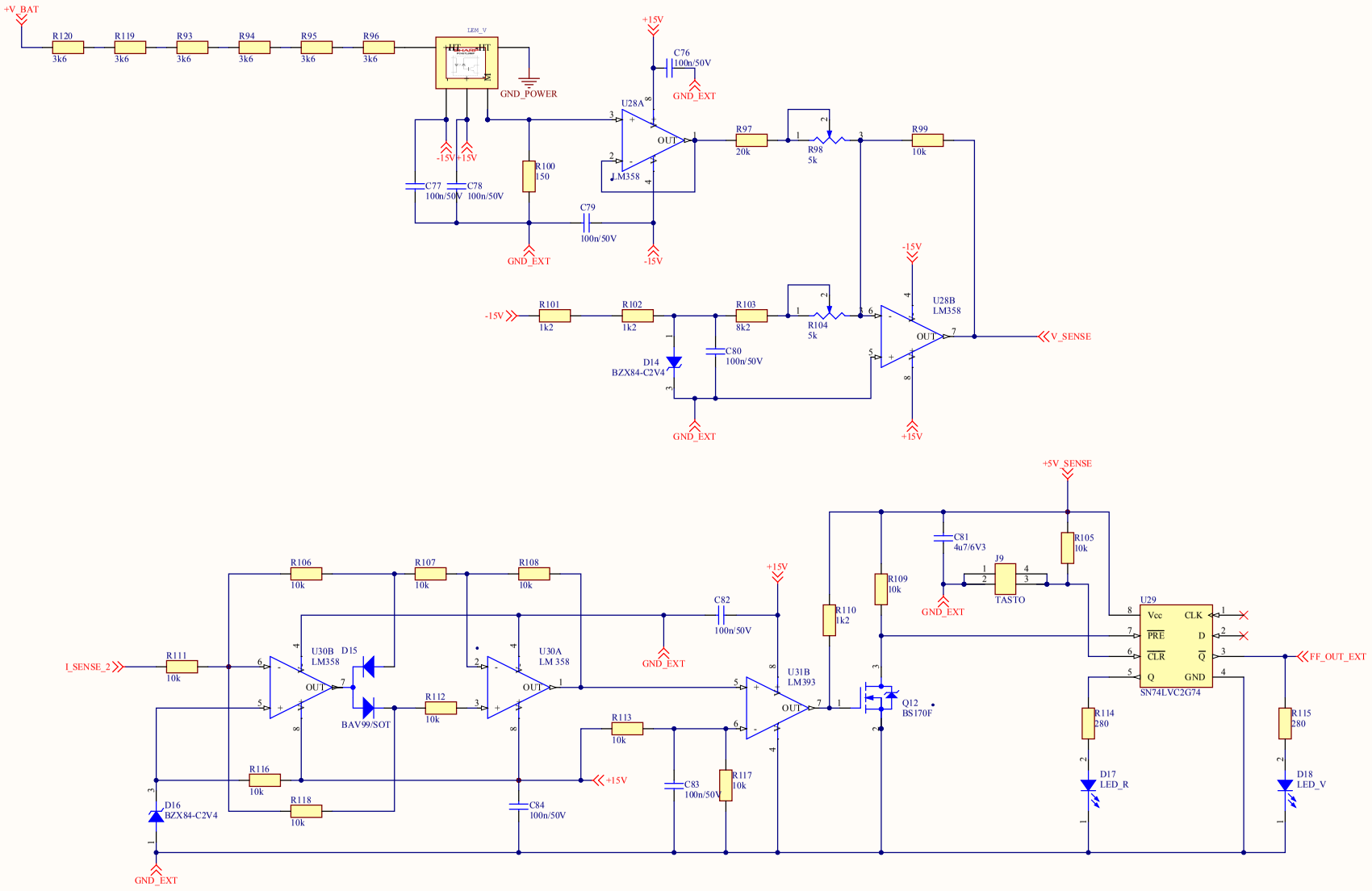
Title		
Size	Document Number	Rev
Date:	Sheet 6 of	


+V_BAT
R45 150k
R46 150k
R47 150k
DT1 5V6
R51 10k
C42 100n/50V
C39 4u7/6V3
U15A LM358
INPUT_AN10
U16 DsPic30F5011
INPUT_AN1
INPUT_AN2
INPUT_AN3
I_SENSE_1
AN5
ICD - RB6/PGC A
ICD - RB7/PGD A
AN_8
INPUT_AN9
INPUT_AN10
RB11
INPUT_AN4
AN13
AN14
RB15
SDI1
SD01
RF4
RF5
SCK1
C1RX/RF0
C1TX/RF1
U1RX/SDI1/RF2
EMUD3/U1TX/SDO1/RF3
U2RX/CN17/RF4
U2TX/CN18/RF5
EMUC3/SCK1/INT0/RF6
T2CK/RC1
T3CK/RC2
EMUD1/SOSCI/T4CK/CN1/RC13
EMUC1/SOSCO/T1CK/CN0/RC14
RC2
RC1
RC14
RC13
MCLR
OSC1/CLKI
OSC2/CLKO/RC15
ICD - MCRL A
R48 10k
C40 33p/50V
C41 33p/50V
Y1 15MHz
EMUC2/OC1/RD0
EMUD2/OC2/RD1
OC3/RD2
OC4/RD3
OC5/IC5/CN13/RD4
OC6/IC6/CN14/RD5
OC7/CN15/RD6
OC8/CN16/RD7
IC1/INT1/RD8
IC2/INT2/RD9
IC3/INT3/RD10
IC4/INT4/RD11
RD0
RD1
RD3
PWM_V
PWM_U
RD5
RD7
RD8
RD9
RD10
RD11
D11 LED_R
R52 500
C2RX/RG0
C2TX/RG1
CAN_TX
CAN_RX
R53 330
C44 33p/50V
SCL/RG2
SDA/RG3
SCK2/CN8/RG6
SDI2/CN9/RG7
SDO2/CN10/RG8
SS2/CN11/RG9
CSDI/RG12
CSDO/RG13
CSCK/RG14
COFS/RG15
RG2
RG3
SCK2
SDI2
SD02
SS2
RG12
RG13
RG14
RG15
U14 25AA1024
SDI
SDO
SCLK
HOLD
WP
CS
VCC
GND
R49 10k
R50 10k
C43 100n/50V
TEMP_POTENZA
R54 10k
C45 4u7/6V3
C46 100n/50V
U17B LM358
R56 1k2
U15B LM358
U18 LM4040AIM3-2.5
C53 100n/50V
NTC1 NTC-10k
R55 2k2
C51 100n/50V
U17A LM358
C47 4u7/6V3
C48 4u7/6V3
C49 4u7/6V3
C88 4u7/6V3
C89 4u7/6V3
+5V
D

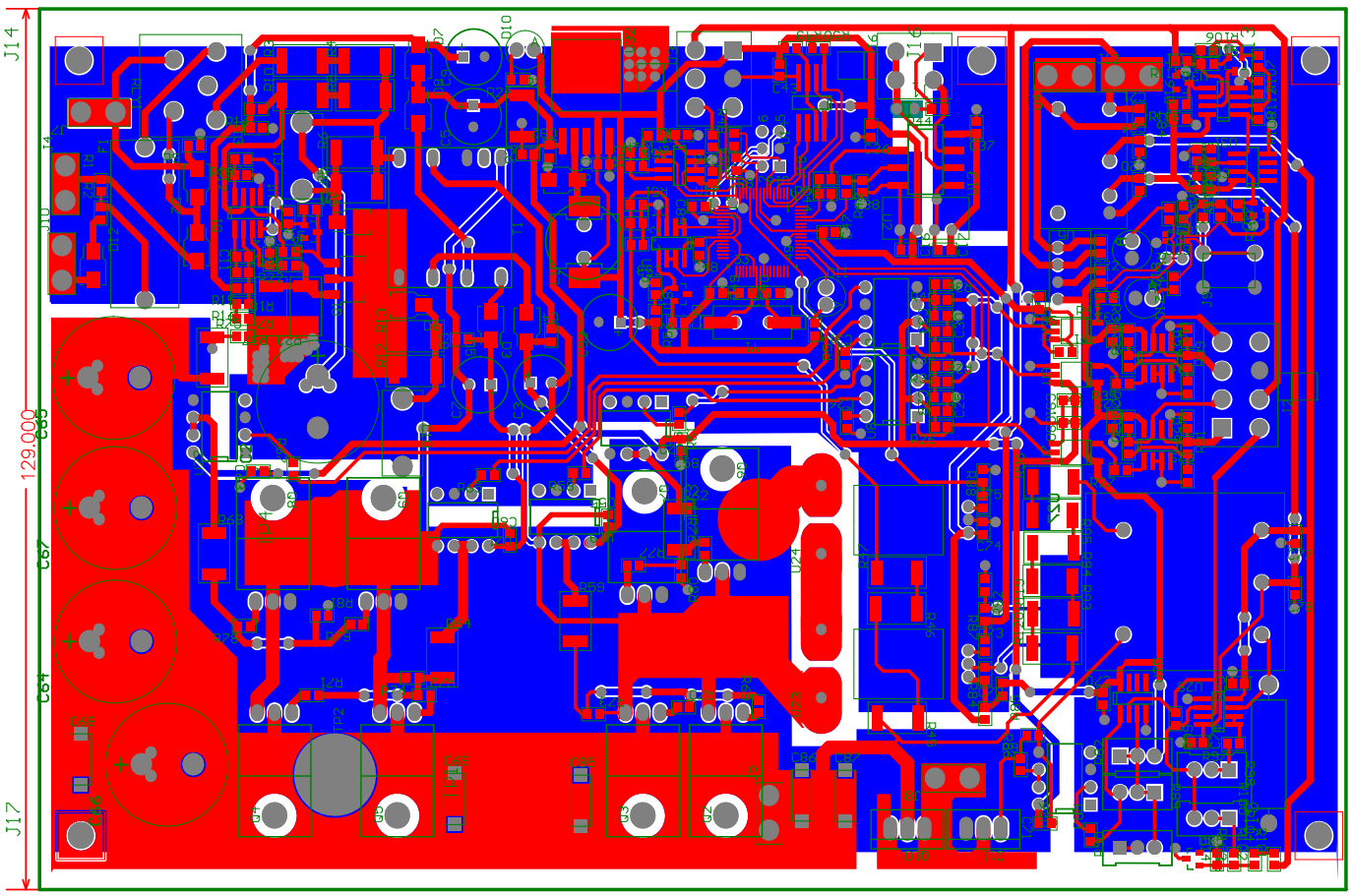


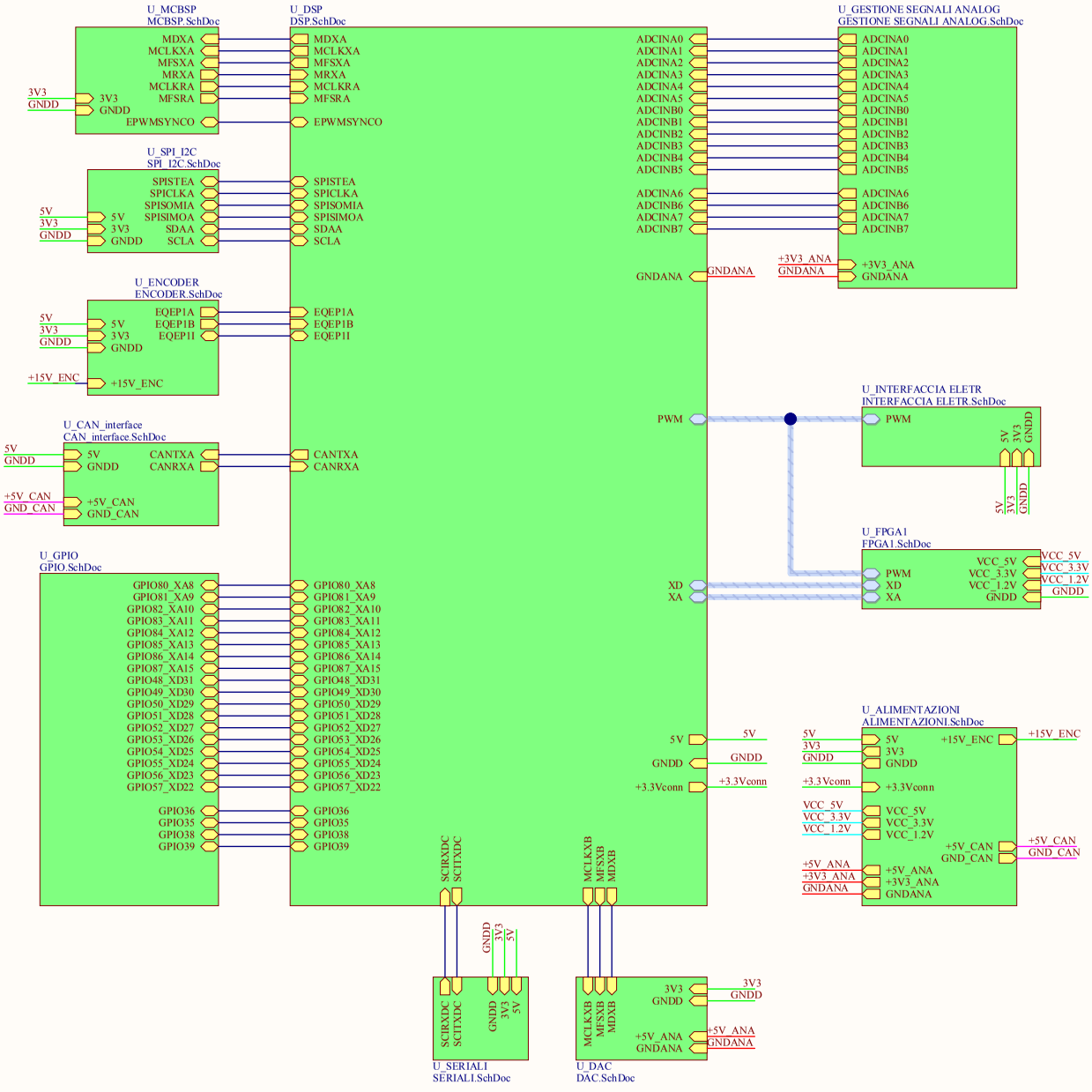
Title		
Size	Document Number	Rev
Date:	Sheet 6 of	


+V_BAT
R75
6k8
C64
220u/400V
C65
220u/400V
C66
220u/400V
C67
220u/400V
C68
0.33u/450V
C69
0.33u/450V
GND_POWER
-VCC_UH
UH_GATE
R69
10
R70
10
R73
10k
Q2
IRF3415
Q3
IRF3415
UL_GATE
R76
10
R77
10
R80
10k
Q6
IRF3415
Q7
IRF3415
C85
0.33u/450V
C86
0.33u/450V
VH_GATE
R71
10
R72
10
R74
10k
Q4
IRF3415
Q5
IRF3415
-VCC_VH
VL_GATE
R78
10
R79
10
R81
10k
Q8
IRF3415
Q9
IRF3415
+5V_SENSE
R82
5k
R89
5k
R90
5k
C70
4u7/6V3
V_SENSE
U25A
LM 393
R83
330
GND_EXT
U26
NC
ANODE
CATHODE
NC
VCC
VO
VO
VEE
HCPL-3120
+VCC_L
C71
100u/50V
R86
10
R91
10K
+V_BAT
Q10
IRF3415
Q11
IRF3415
-RES_FREN
C87
0.33u/100V
GND_POWER
+5V
+5V_SENSE
R84
0R0_3
R85
0R0_4
U23
ACS758-100
Ip-
Ip+
VCC
GND
VO
I_SENSE_2
R87
330
C72
4u7/6V3
C73
10n/50V
GND_EXT
+OUT
U24
ACS758-100
I_SENSE_1
R88
330
C74
4u7/6V3
C75
10n/50V
R92
0R0_3
Nel caso in cui il controllo sia affidato al PIC interno, si monteranno le 0R0_3, se affidato alla FPGA esterna, si monterà la 0R0_4
Title
Size
Document Number
Rev
Date:
Sheet 6 of

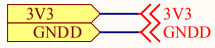


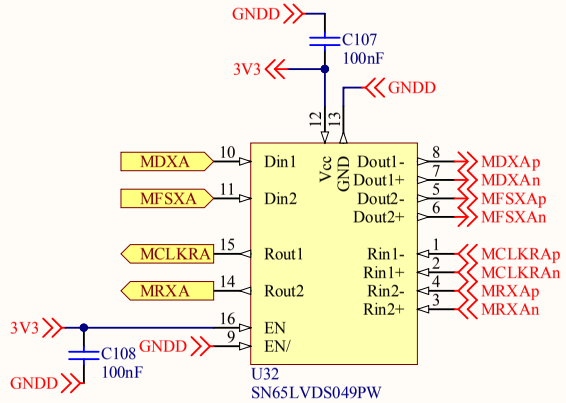
Title		
Size	Document Number	Rev
Date:	Sheet 6 of	

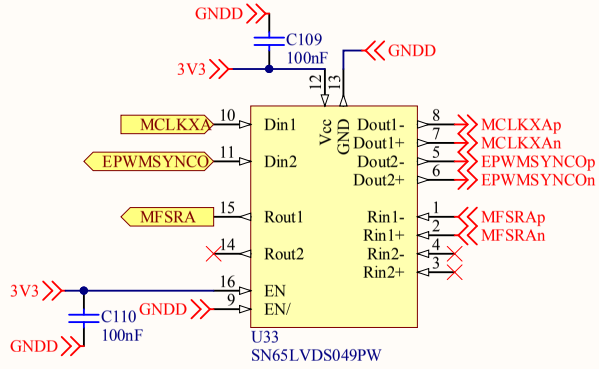

J14
129.000
J17

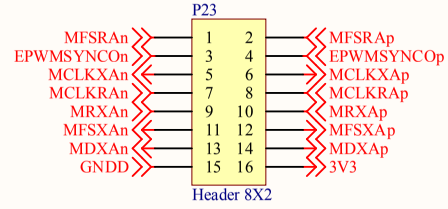


Title		
Size A3	Number	Revision
Date: 01/02/2015	Sheet of	
File: C:\Users\...\SCHEDA_CONTROLLO.SchDoc	Drawn By:	

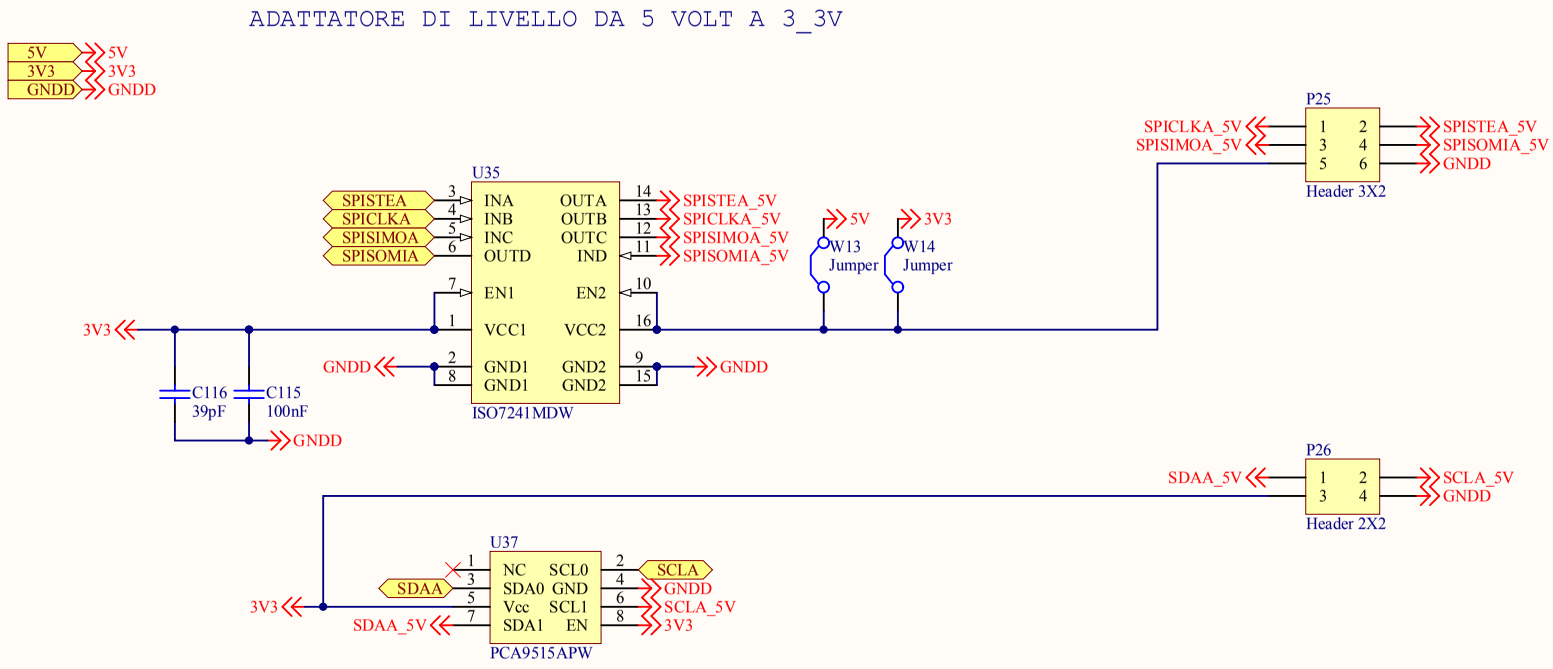




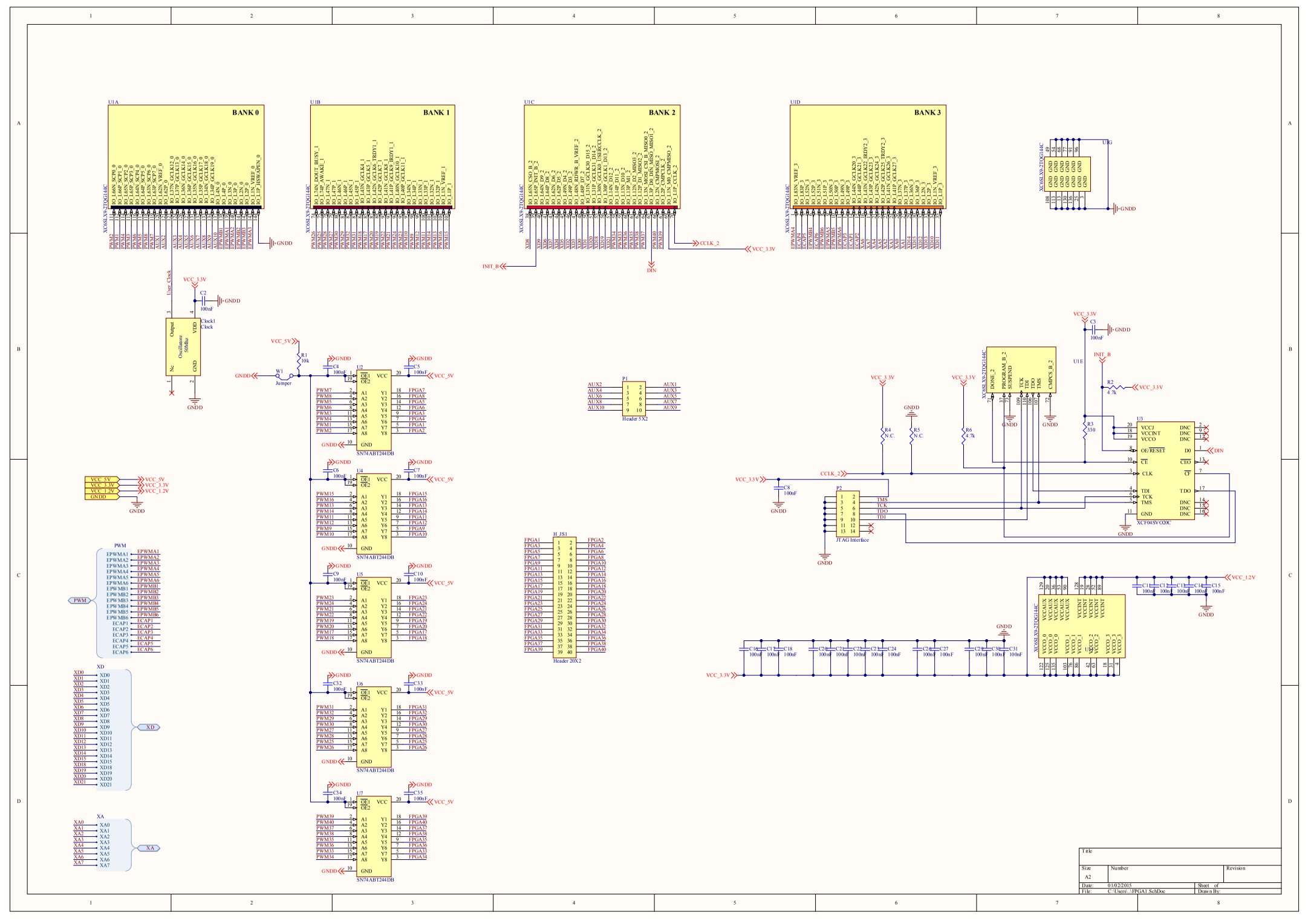




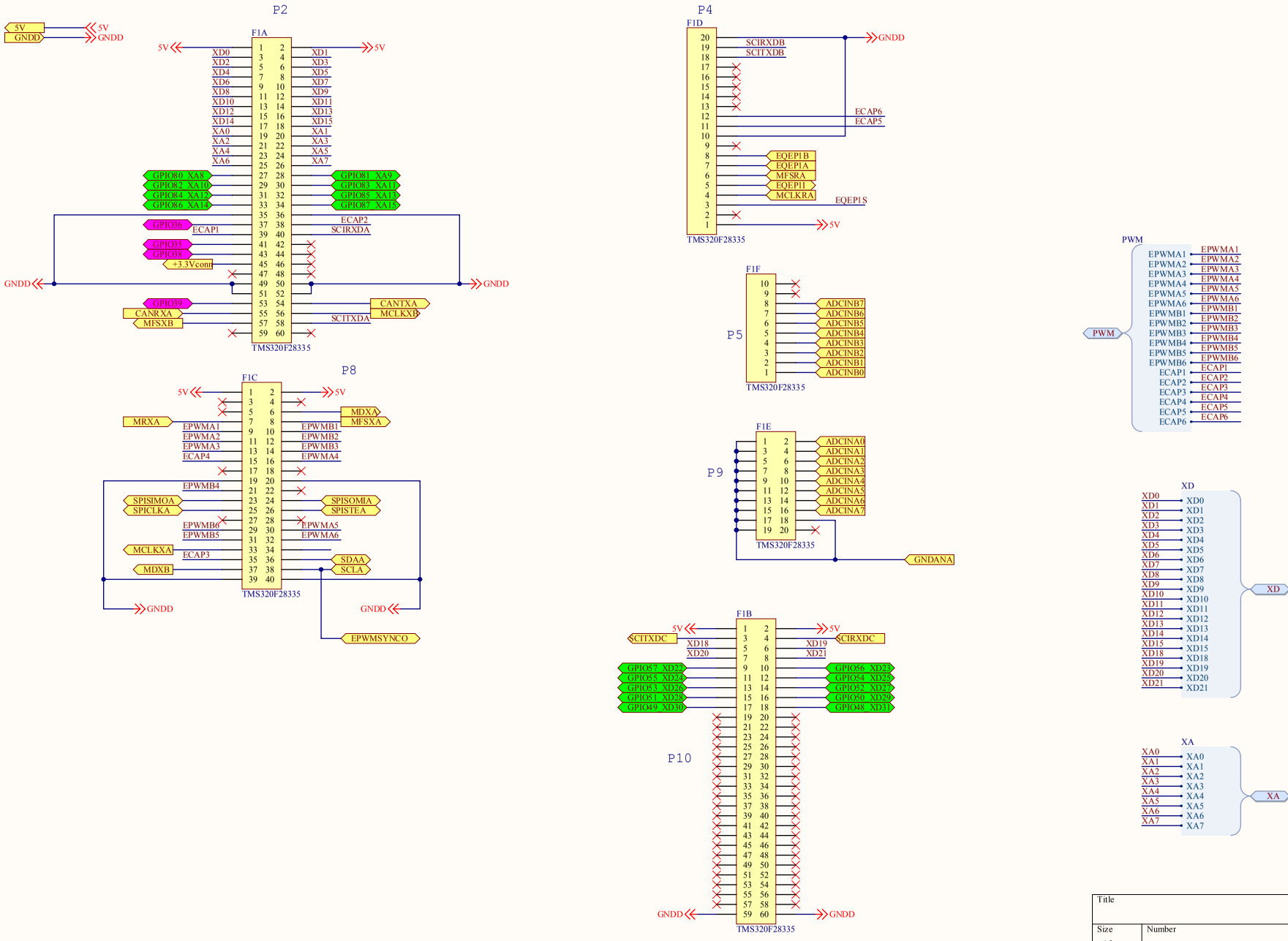
Title		
Size A4	Number	Revision
Date: 01/02/2015		Sheet of
File: C:\Users\..\MCBSP.SchDoc		Drawn By:



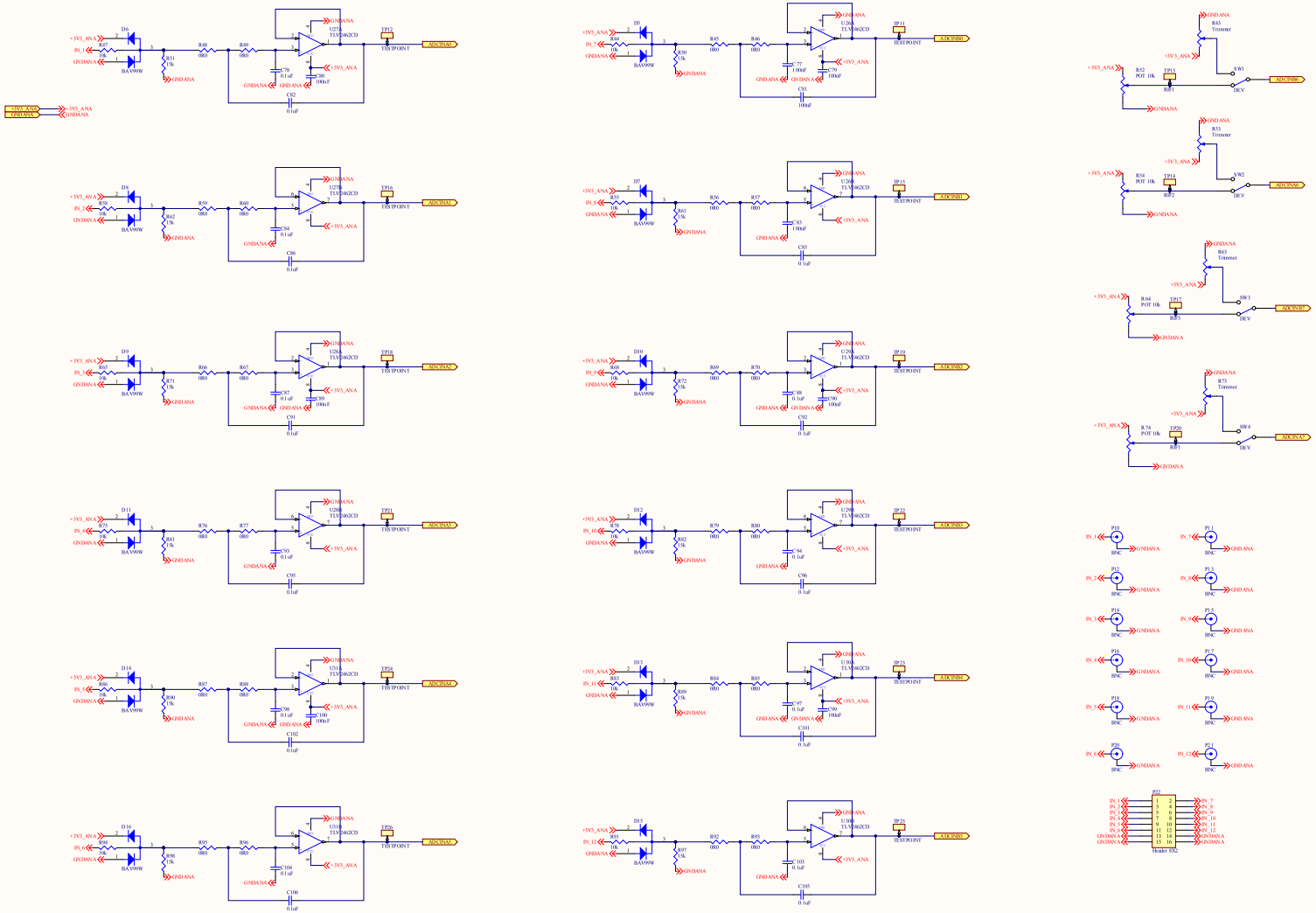
Title		
Size: A4	Number	Revision
Date: 01/02/2015	Sheet of	
File: C:\Users\..\SPI_I2C.SchDoc	Drawn By:	



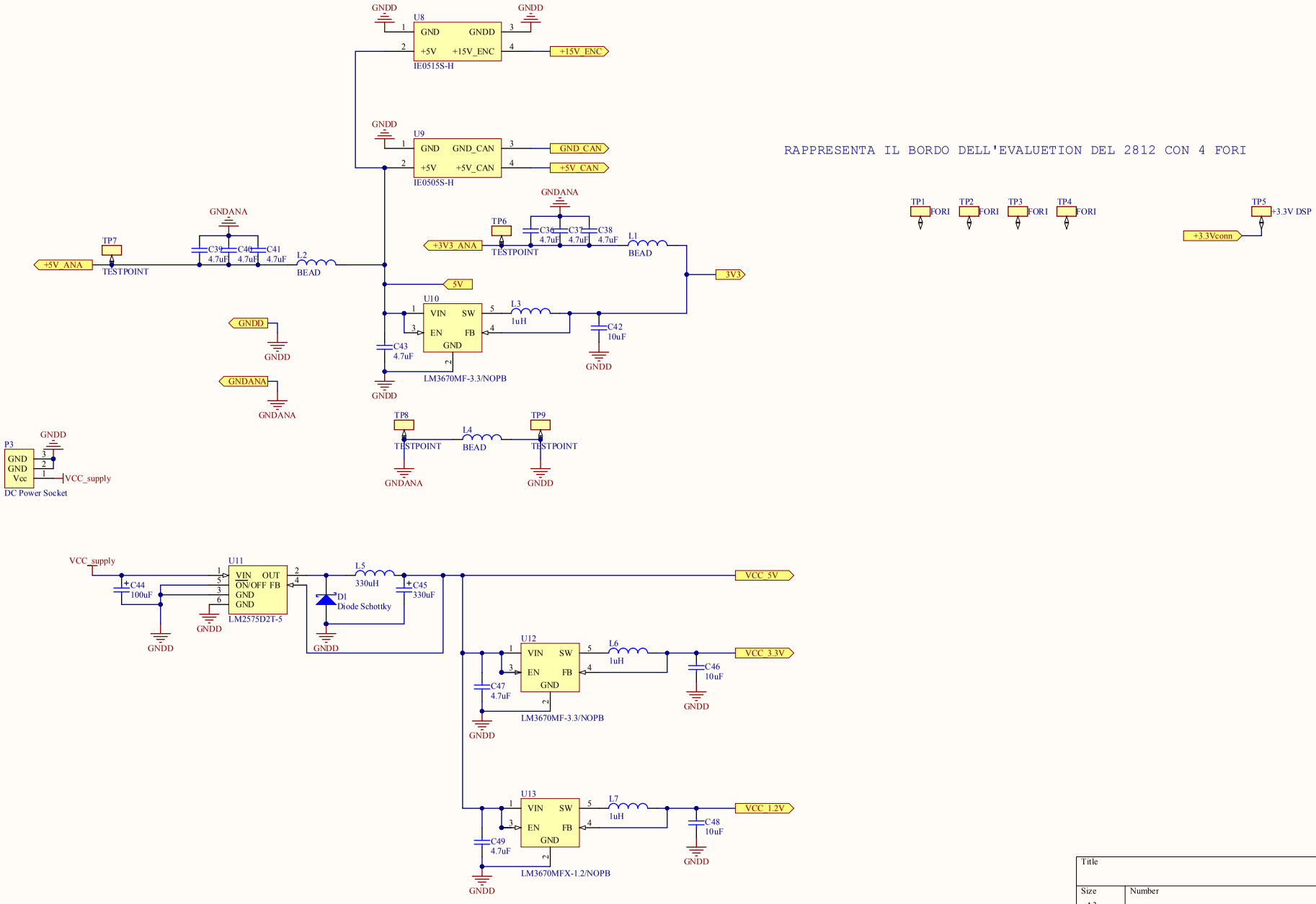
Title			
Size	Number		Revision
A2			
Date:	01/02/2015	Sheet of	
File:	C:\Users\...\FPGA1 SchDoc	Drawn By:	



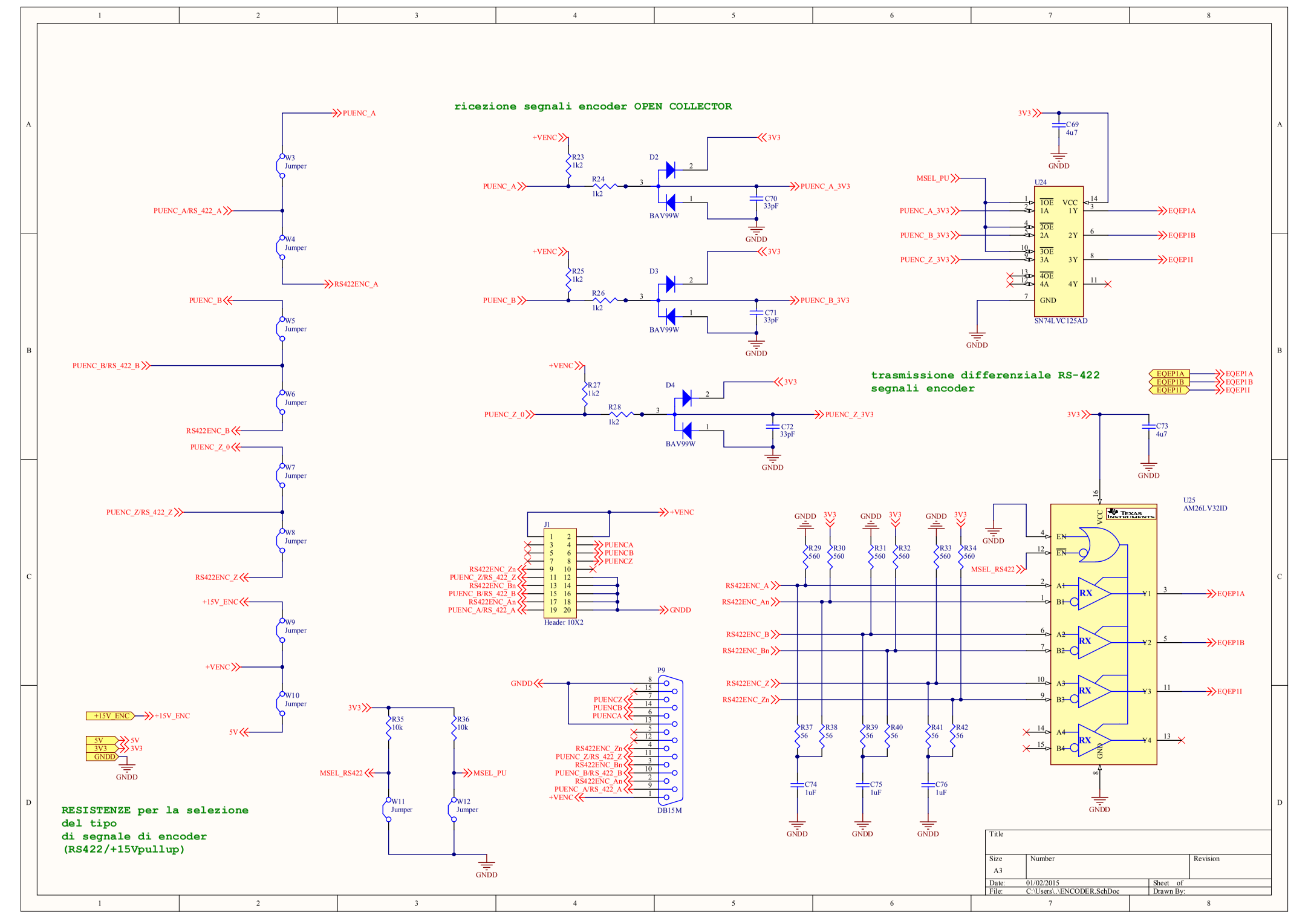
Title			
Size A3	Number		Revision
Date: 01/02/2015		Sheet of	
File: C:\Users\..\DSP.SchDoc		Drawn By:	

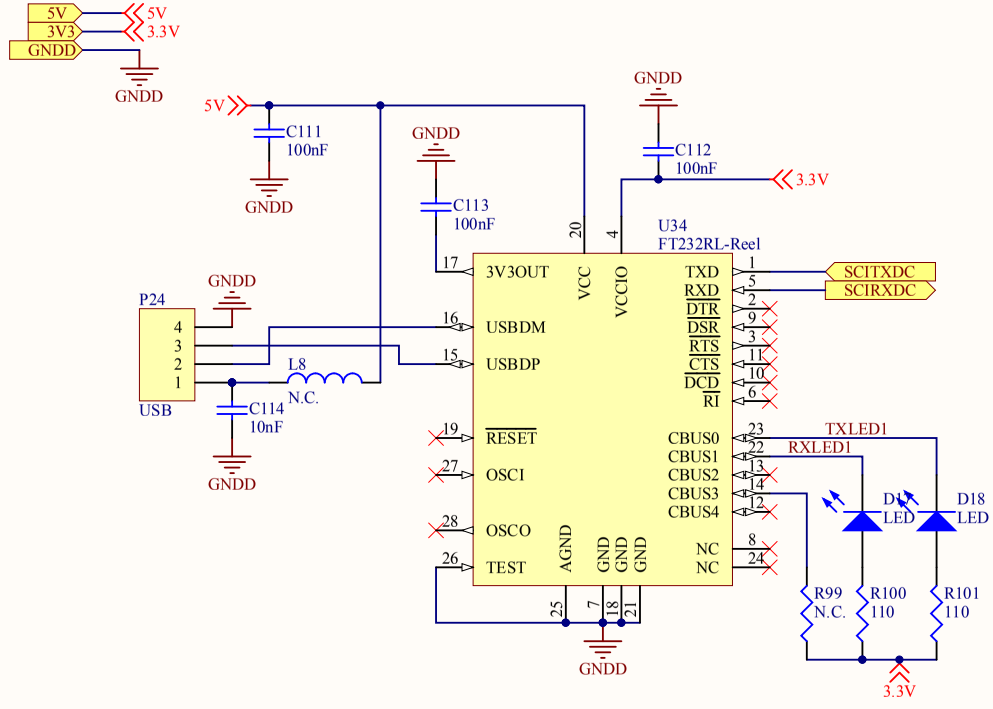


Title		
Size: A1	Number: 1	Revision:
Date: 01/02/2017	Sheet 1 of 1	
File: C:\Users\...\ANALOG_SIGNALS_ANA.SchDoc		

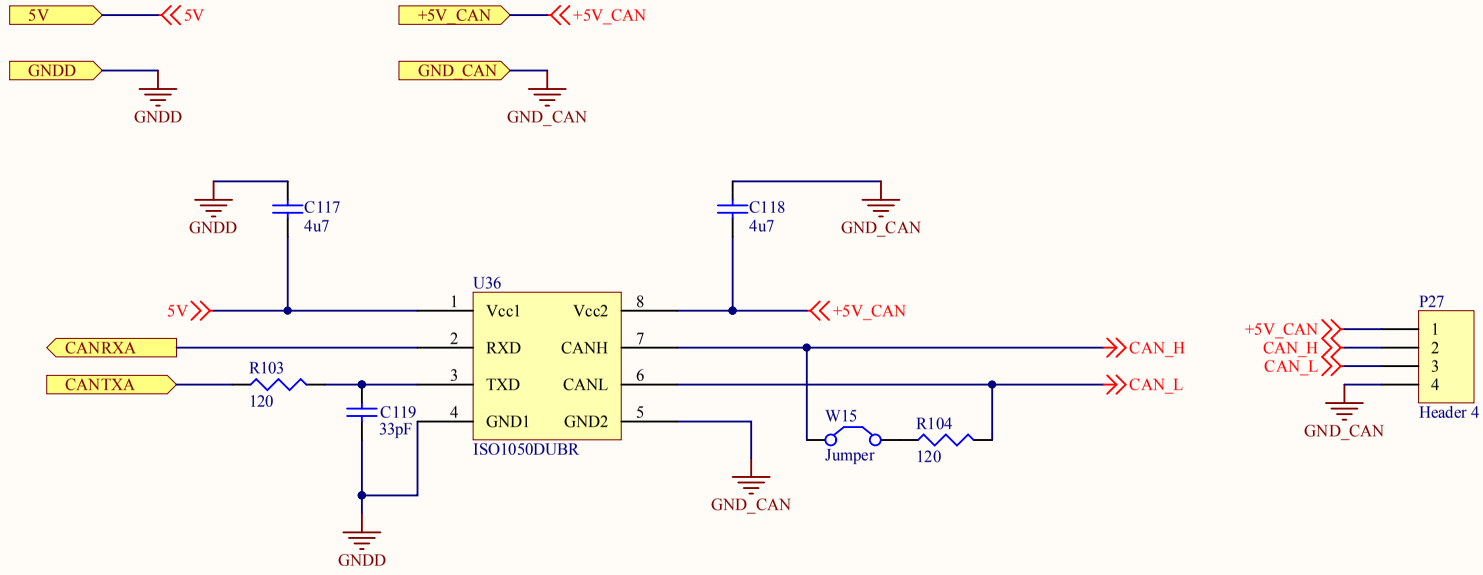


Title		
Size A3	Number	Revision
Date: 01/02/2015		Sheet of
File: C:\Users\..\ALIMENTAZIONI.SchDoc		Drawn By:

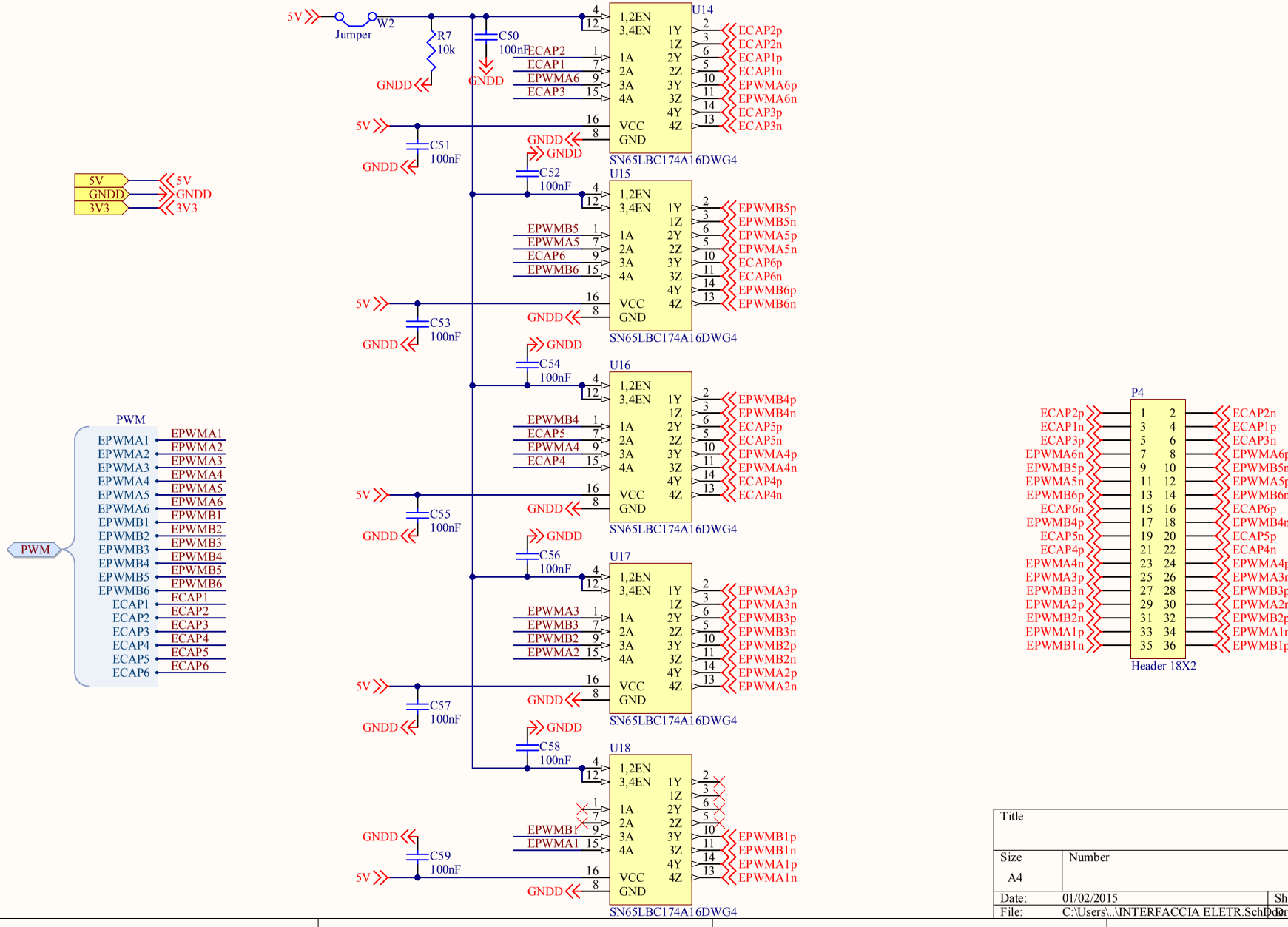

ricezione segnali encoder OPEN COLLECTOR
trasmissione differenziale RS-422
segnali encoder
RESISTENZE per la selezione
del tipo
di segnale di encoder
(RS422/+15Vpullup)
PUENC_A
PUENC_A/RS_422_A
RS422ENC_A
PUENC_B
PUENC_B/RS_422_B
RS422ENC_B
PUENC_Z_0
PUENC_Z/RS_422_Z
RS422ENC_Z
+15V_ENC
+VENC
5V
3V3
GNDD
W3 Jumper
W4 Jumper
W5 Jumper
W6 Jumper
W7 Jumper
W8 Jumper
W9 Jumper
W10 Jumper
R23 1k2
R24 1k2
R25 1k2
R26 1k2
R27 1k2
R28 1k2
D2
D3
D4
BAV99W
C70 33pF
C71 33pF
C72 33pF
PUENC_A_3V3
PUENC_B_3V3
PUENC_Z_3V3
C69 4u7
C73 4u7
U24
SN74LVC125AD
MSEL_PU
EQEP1A
EQEP1B
EQEP1I
J1
Header 10X2
RS422ENC_Zn
PUENC_Z/RS_422_Z
RS422ENC_Bn
PUENC_B/RS_422_B
RS422ENC_An
PUENC_A/RS_422_A
PUENCA
PUENCB
PUENCZ
P9
DB15M
U25
AM26LV32ID
MSEL_RS422
R29 560
R30 560
R31 560
R32 560
R33 560
R34 560
R35 10k
R36 10k
R37 56
R38 56
R39 56
R40 56
R41 56
R42 56
C74 1uF
C75 1uF
C76 1uF
W11 Jumper
W12 Jumper
Title
Size A3
Number
Revision
Date: 01/02/2015
File: C:\Users\..\ENCODER.SchDoc
Sheet of
Drawn By:

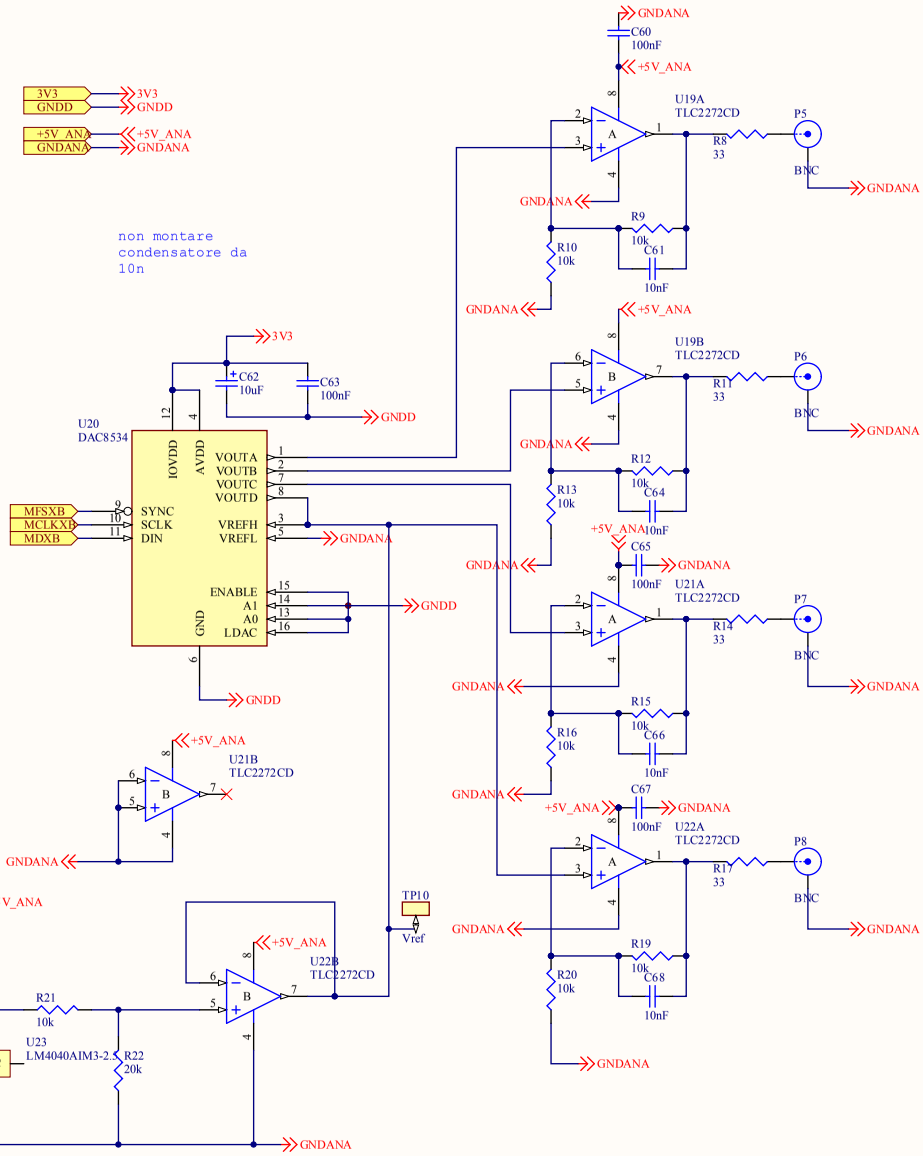


Title			
Size A4	Number		Revision
Date:	01/02/2015	Sheet of	
File:	C:\Users\..\SERIALI.SchDoc	Drawn By:	

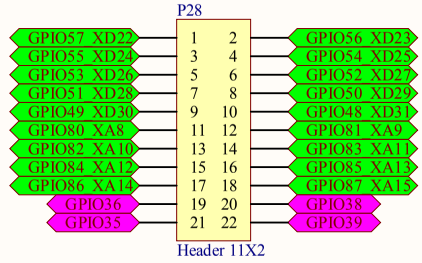


Title		
Size: A4	Number	Revision
Date: 01/02/2015		Sheet of
File: C:\Users\..\CAN_interface.SchDoc		Drawn By:

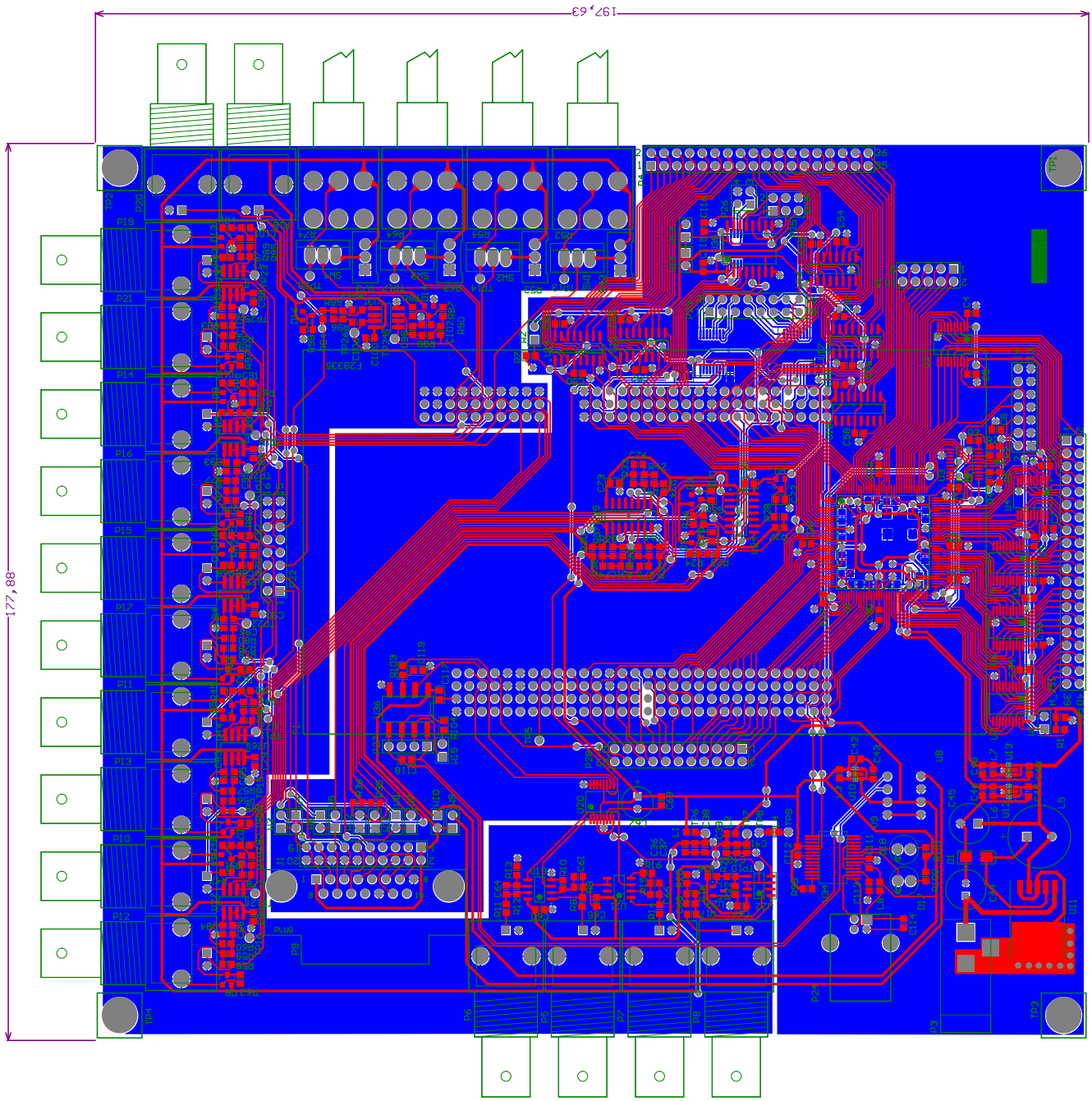

5V
GNDD
3V3
PWM
EPWMA1
EPWMA2
EPWMA3
EPWMA4
EPWMA5
EPWMA6
EPWMB1
EPWMB2
EPWMB3
EPWMB4
EPWMB5
EPWMB6
ECAP1
ECAP2
ECAP3
ECAP4
ECAP5
ECAP6
W2
Jumper
R7
10k
C50
100nF
U14
U15
U16
U17
U18
1,2EN
3,4EN
1A
2A
3A
4A
1Y
1Z
2Y
2Z
3Y
3Z
4Y
4Z
VCC
GND
SN65LBC174A16DWG4
C51
C52
C53
C54
C55
C56
C57
C58
C59
100nF
P4
Header 18X2
Title
Size
A4
Number
Revision
Date:
01/02/2015
Sheet of
File:
C:\Users\..\INTERFACCIA ELETR.SchDoc
Drawn By:



Title		
Size: A3	Number	Revision
Date: 01/02/2015		Sheet of
File: C:\Users\..\DAC.SchDoc		Drawn By:



Title		
Size A4	Number	Revision
Date: 01/02/2015		Sheet of
File: C:\Users\..\GPIO.SchDoc		Drawn By:


197,63
177,88

Acknowledgments

Desidero ringraziare per questi bellissimi ed indimenticabili anni del Dottorato e per il lavoro che ho potuto svolgere il mio Tutor Prof. Angelo Tani.

Un grazie particolare anche al Prof. Giovanni Serra e al Prof. Domenico Casadei.
Un vivo senso di gratitudine esprimo nei confronti dei Professori Luca Zarri, Michele Mengoni e Claudio Rossi e di tutti i Colleghi ed Amici del Gruppo di Convertitori, Macchine ed Azionamenti Elettrici del Dipartimento DEI dell'Università di Bologna.

Ringrazio anche il Prof. Pericle Zanchetta dell'Università di Nottingham e tutto il Suo Gruppo di Ricerca, in particolare i Ricercatori Liliana De Lillo e Lee Empringham per la stretta vicinanza nel lavoro di ricerca svolto in Inghilterra.

Ringrazio infine la mia famiglia che sempre mi sostiene.