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Nonlinear Characterization and Modelling of GaN HEMTs for Microwave Power Amplifier Applications

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Contents

Nomenclature

Acronyms

AFG Arbitrary Function Generator

CAD Computer Aided Design

DC Direct Current

DSO Digital Storage Oscilloscope

DUT Device Under Test

FET Field Effect Transistor

FFT Fast Fourier Transform

GaAs Gallium Arsenide

GaN Gallium Nitride

HB Harmonic Balance

HEMT High Electron Mobility Transistor

IFFT Inverse Fast Fourier Transform

ISS Impedance Standard Substrate

LDMOS Laterally Diffused Metal Oxide Semiconductor

LSNA Large Signal Network Analyzer

LUT Look Up Table

$NVNA$ Nonlinear Vector Network Analyzer

$OFDM$ Orthogonal Frequency-Division Multiplexing

PA Power Amplifier

$PAPR$ Peak-to-Average Power Ratio

$pHEMT$ Pseudomorphic HEMT

RF Radio Frequency

$SOLT$ Short Open Load Thru

VNA Vector Network Analyzer

WBG Wide Band-Gap

Introduction

Semiconductors technologies are rapidly evolving driven by the need for higher performance demanded by applications. Thanks to the numerous advantages that it offers, gallium nitride (GaN) is quickly becoming the technology of reference in the field of power amplification at high frequency. The RF power density of AlGaN/GaN HEMTs (High Electron Mobility Transistor) is an order of magnitude higher than the one of gallium arsenide (GaAs) transistors. The first demonstration of GaN devices dates back only to 1993. Although over the past few years some commercial products have started to be available, the development of a new technology is a long process. The technology of AlGaN/GaN HEMT is not yet fully mature, some issues related to dispersive phenomena and also to reliability are still present. Dispersive phenomena, also referred as long-term memory effects, have a detrimental impact on RF performances and are due both to the presence of traps in the device structure and to self-heating effects. A better understanding of these problems is needed to further improve the obtainable performances. Moreover, new models of devices that take into consideration these effects are necessary for accurate circuit designs. New characterization techniques are thus needed both to gain insight into these problems and improve the technology and to develop more accurate device models.

This thesis presents the research conducted on the development of new characterization and modelling methodologies for GaN-based devices and on the use of this technology for high frequency power amplifier applications.

The thesis is organized as follows. The properties of gallium nitride, the fundamental working principles of HEMTs and the advantages that these offer are introduced in Chapter 1. A review and some examples of the effects related to traps and self-heating are also presented. In Chapter 2, to show the big potential of

the technology also compared to GaAs, the design of some GaN-based Monolithic Microwave Integrated Circuits (MMIC) high power amplifiers is presented with some considerations on thermal issues. A method for the characterization of the thermal resistance of devices is explained in Chapter 3. The method involves only multi-bias small-signal S-parameter and DC I/V measurements at different base plate temperatures. In Chapter 4, a new pulsed characterization setup is presented. The post-processing of measurements and the specifically developed calibration procedure are explained in detail. Results of the pulsed characterization of GaAs and GaN HEMTs are presented. A different measurement setup developed to characterize the effects of traps trough transient current measurements is presented in Chapter 5. Different devices are measured and compared trough the extraction of a model of the transient. Finally, some results of a pulsed RF characterization are presented, showing how traps can be an added source of distortion for modulated signals.

Chapter 1

GaN Technology

The development of new semiconductors technologies for power applications at high frequency has been made necessary by the demand of a continuous increase in performance of the final stage of power amplifiers. Modern wireless communication systems, microwave and satellite links, defence and scientific radar and electronic warfare systems are demanding: high power with high efficiency and linearity at low cost. These are requirements that are in conflict with each other.

The pervasive deployment of technologies such as WiFi, GSM, UMTS, etc. with the radio spectrum more and more crowded is in contrast with the need to have increasingly high throughput. This is driving the definition of new standards and technologies like LTE and WiMax that in order to ensure a high spectral efficiency in terms of Bit/sec/Hz use complex modulations based on OFDM. These modulations that have a high PAPR require a high linearity of the power amplification stage to avoid distortion (measured in terms of EVM) and spectral regrowth or spreading (i.e. ACPR) but maintaining a reasonable level of output power. At the same time energy efficiency is becoming more and more important. The power amplifier is often the subsystem with the highest power consumption and its efficiency has a direct impact on battery life in mobile end user terminals and on the operating cost of base stations.

In the field of very high power at microwave frequency, vacuum tube devices like Traveling-wave tubes (TWT), Klystron and Magnetron are often still the only possibility. Replacing these with solid-state devices in applications like geostationary communication satellites or Radars would bring great advantages of size and weight.

Although a lot of work is being done on the development of new circuit topologies and techniques for power amplifiers like Dohertry, Envelope Tracking, Load modulation, advanced operation classes, digital predistortion, etc. ,current semiconductors technologies like GaAs, SiGe and LDMOS are reaching their limits and begin to no longer be able to fulfil all the requirements [1].

For a significant step forward a new technology was needed. The requirement of high power and frequency requires transistors based on semiconductor materials with both large breakdown voltages and high electron velocity. For this, research has been focused on wide band-gap materials like GaN and SiC [2]. GaN has a high electron saturation velocity which allows high frequency operation and the ability to form heterojunctions that can be used to fabricate High Electron Mobility Transistors (HEMT). The wide band-gap results in high breakdown fields and in general in more rugged devices. These properties combined allow to obtain high electron mobility and carrier concentration with high fields which results in higher power densities and efficiency at high frequency [3]. Since the first demonstration in the early nineties of AlGaN/GaN HEMT devices [4], the technology has seen a continuous improvement in performance that has led in the last five years to the availability of several commercial products and MMIC processes. Today GaN HEMTs are a very promising candidate for high power and efficiency microwave applications from L band of cellular base stations up to K band for satellite communications and radars but the research trend is to extend the application of GaN to higher millimeter-wave and even terahertz frequencies [5].

The technology however is not yet fully mature and some specific problems are still to be resolved and better understood.

Because of the high RF power density that can be in the order of 10 W/mm and despite the higher obtainable efficiency, the thermal management is becoming an important issue. In fact in many cases GaN technology is limited by the difficulty in heat dissipation rather than by electrical limitations. Reliability of devices is directly correlated with the operating junction temperature and despite power densities up to 41 W per millimetre of gate periphery have been demonstrated [6] today commercial devices and processes are optimized for densities of the order of 5 to 8 W/mm.

The characterization of the thermal resistance and the inclusion of thermal

effects in compact models is much more important for GaN based devices than it was for GaAs. Moreover, heating and cooling are not instantaneous phenomena and this could be a source of long-term memory effects and thus distortion that have to be taken into account.

Another issue that is still affecting the technology is the presence of trap states. These are due to imperfections in materials and to lattice mismatches at interfaces of different layers of the device causing defects in the crystal structure. Traps can capture and emit mobile charge carriers causing in general a degradation of performances. Similarly to self-heating, trapping and de-trapping are dynamic processes that can be an added source of distortion for modulated signals. Different traps can be located in different positions in the device structure with different effects on performances. In early stages of the development of the technology it was discovered that adding a passivation on the surface of devices greatly reduces surface traps. The problem is however not resolved because other traps are present and their location and effects are not yet fully understood.

Both thermal and trapping phenomena can introduce memory effects and are considered slow phenomena because the associated time constants are usually much longer than the period of applied RF signals. Because of this, their effects are called *long-term memory effects*. In the frequency domain the consequence of these phenomena can be seen as the change of some device parameters (i.e.transconductance) versus frequency. Effects of thermal and trapping phenomena are thus also called *dispersive effects*.

1.1 GaN properties

Gallium nitride is a wide band-gap (WBG) semiconductor with an energy gap between valence and conduction band of $E_g = 3.4\,\mathrm{eV}$ that allows to operate with very high electric fields. The breakdown field can be higher than $3\,\mathrm{MV/cm}$ [3]. As a consequence, GaN-based devices can be biased at high drain voltages, usually in the order of $30\,\mathrm{V}$, without incurring in breakdown. The breakdown voltage depends on the particular device structure but it is higher than $100\,\mathrm{V}$. Moreover, the high thermal conductivity of $1.3\,\mathrm{W/(K\,cm)}$, allows to operate at higher temperatures compared to other semiconductors. Another advantage of GaN is to have a high carrier saturation velocity ($2.5 \times 10^7\,\mathrm{cm/s}$) which contributes

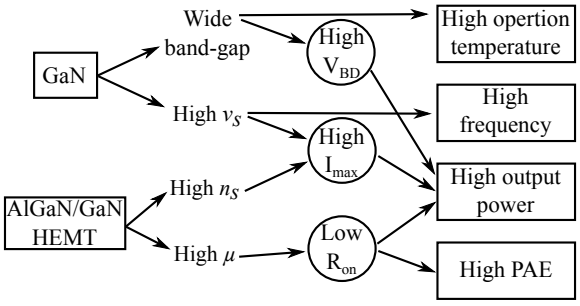

Figure 1.1: Relations between GaN and HEMT properties and advantages for applications.

to high current densities. The maximum current I_{max} is indeed proportional to qn_sv_s where q is the electron charge, n_s is the carrier density and v_s the electron saturation velocity. The high v_s allows also a high operation frequency being f_t (current gain cut-off frequency) and f_{max} (maximum power gain cut-off frequency) proportional to it. Of fundamental importance is the possibility to realize an AlGaN/GaN heterostructure which forms a two dimensional electron gas (2DEG) at the interface. This was first discovered in 1992 by Khan [7]. The 2DEG, which forms the channel of HEMT devices, has a high carrier density ($n_s \approx 1 \times 10^{13}/\mathrm{cm}^2$) and a high electron mobility ($\mu \approx 1500 - 2000\,\mathrm{cm}^2/(\mathrm{V\,s})$) [8] that also allow a high I_{max} current. The channel on-resistance, being inversely proportional to the electron mobility, is small with consequent advantages in terms of efficiency. As a consequence of all these physical properties, AlGaN/GaN HEMTs have high breakdown voltages, current density, and can work at microwave frequencies with a good efficiency. Power densities up to 41 W/mm [6] and f_t up to 350 GHz [9] have been demonstrated to date. A discrete AlGaN/GaN HEMT with an output power of 800 W in pulsed operation at S-band has been reported [10] while commercial discrete devices rated up to 380 W are available [11]. A schematic representation of relations between physical and technological properties and advantages for applications is shown in Fig. 1.1.

In Table 1.1 are reported the most important material properties of GaN and of competing semiconductors [2]. Gallium nitride is better in almost all parameters. The low band-gap of GaAs limits the maximum drain voltage to less than 10 V. At the same output power, a lower voltage means a higher current and being the dissipated power proportional to RI^2 the overall system efficiency is lower.

Material	Energy gap (eV)	Electron mobility ($cm^2/(V\,s)$)	Breakdown field (MV/cm)	Dielectric constant	Thermal conductivity (W/(K cm))
Si	1.1	1350	0.3	11.8	1.5
GaAs	1.4	5000	0.4	12.5	0.5
SiC	3	400	3	10	3.5
GaN	3.4	1500	3	9	1.3

Table 1.1: Material properties of microwave semiconductors.

A higher dissipated power means also higher costs and dimensions for cooling systems. Furthermore, being the drain voltage higher and the current lower, the optimal load impedance for maximum output power for GaN HEMTs is an order of magnitude higher than for GaAs devices [12]. The maximum RF power density of GaAs pHEMTs is in the order of 1 W/mm [13] while for GaN it is in the range from 5 to 10 W/mm [1]. This means that for same RF output power a GaN transistor is much smaller with smaller parasitic capacitances. The optimum impedance is thus easier to match to the system 50 Ω with great advantages in terms of bandwidth and matching networks losses. In general, all WBG materials have also a higher resistance to radiation and are well suited for harsh environment like space [14, 15].

An issue of GaN is the difficulty in realizing high quality bulk single crystal GaN substrates. This problem was overcome in the late 1990s and early 2000s when it became possible to grow high quality Silicon Carbide (SiC) substrates on top of which is then growth the GaN epi-layer [1]. The SiC substrate has a very high thermal conductivity ($\sim 350\,W/(m\,K)$) that helps in heat dissipation and allows a lower junction temperature than the one which would result with other substrate technologies. Moreover, SiC has a lower lattice mismatch to GaN that helps in reducing dislocation density in the epy-layer. The GaN on SiC technology is well suited to realize both discrete devices and Monolithic Microwave Integrated Circuits (MMIC).

Compared to silicon and LDMOS FET devices, which are currently the technology of choice for the cellular base station industry, gallium nitride has better performances and allows high-power operation at much higher frequency. The big advantages of Si are the lower raw cost and the high maturity of the technology. However, the market share of GaN is increasing and with bigger volumes the cost should go down becoming competitive. Moreover, in comparing the cost of different technologies, it should be considered the full advantages that GaN

brings at system level. In fact it can be shown [16] that for MMIC high power density applications, GaN is already advantageous with respect to GaAs also in terms of cost. To reduce cost it is also possible to realize AlGaN/GaN devices on Si substrates with some penalties in maximum performances [17]. Si has a lower thermal conductivity and also a lower electrical resistivity than SiC. A high substrate resistivity is important to minimize losses in MMIC. The cost advantage of GaN-on-Si technology is also due to the possibility of realizing 300 mm wafers while SiC wafers are currently limited to 100 mm. At least one commercial vendor is already offering GaN-on-Si technology with others moving in this direction.

GaN is not only very good for high power applications. In recent years several GaN-based low noise amplifiers (LNA) have been reported with noises figures around 1 dB and covering frequencies from L to X-band [18, 19]. Also other components like SPDT switches and resistive mixers have been demonstrated [20]. This opens the possibility of realizing fully integrated front-ends in GaN [21, 22]. This is especially attractive for Radar applications like Synthetic Aperture Radars (SAR) where a high number of Transmit/Receive modules is employed [17].

In Chapter 2 some MMIC power amplifiers, developed as part of the research activity, will be presented to demonstrate the performances obtainable with the AlGaN/GaN technology, also compared to GaAs.

1.2 Fundamentals of High Electron Mobility Transistors

Many technologies are available for the realization of high-frequency power amplifiers. In GaAs it is possible to realize Heterojunction Bipolar Transistors (HBT), Metal Semiconductor Field Effect Transistor (MESFET), HEMTs and pseudomorphic-HEMTs (pHEMT). In Si we have bipolar junction transistors (Si BJT), Silicon Metal Oxide Semiconductor Field Effect Transistor (Si MOSFET), Silicon Laterally Diffused Metal Oxide Semiconductor FET (LDMOS) and SiGe HBT. Indium Phosphide (InP) HEMTs are used in very high frequency applications. With GaN it is possible to realize HEMT and HBT. The alternatives are many. Every technology has advantages and disadvantages that need to be assessed in relation to specifications both in terms of performance and cost. For many years the main devices used in microwave power applications have been

GaAs MESFET, today HEMTs offer superior performance. HEMTs are sometimes also known as MODFET (Modulation-Doped FET).

The HEMT is a FET transistor based on a heterostructure formed by two semiconductors with different band-gap. The heterojunction forms a quantum well in the conduction band which allows a high electron mobility. HEMTs are usually depletion mode devices where the channel is normally-on and a negative gate voltage is needed to turn it off. Although less common, enhancement mode HEMTs are also possible [23].

For GaAs HEMTs, the two semiconductors are usually intrinsic GaAs and n-doped AlGaAs. In GaN HEMTs the most common heterojunction is formed by intrinsic GaN and undoped AlGaN. A simplified structure of AlGaAs/GaAs HEMT is shown in Fig. 1.2 with the corresponding energy band diagram. The doped AlGaAs has a bigger band-gap and is in contact with the undoped GaAs which has a smaller energy gap. At the interface the conduction band of GaAs is lower than the Fermi energy level forming a quantum well with a high carrier density. Free electrons in the n-doped AlGaAs layer drops into the well forming the 2DEG. Electrons in the 2DEG move in the undoped GaAs without colliding with any impurities allowing a high carrier mobility, generally much greater than can be obtained in bulk semiconductor material. The 2DEG is the channel of the device and its carrier density depends on the applied gate-source field. Many optimisations of the heterojunction are possible and adding other layers more advanced devices like pHEMT and mHEMT are realized.

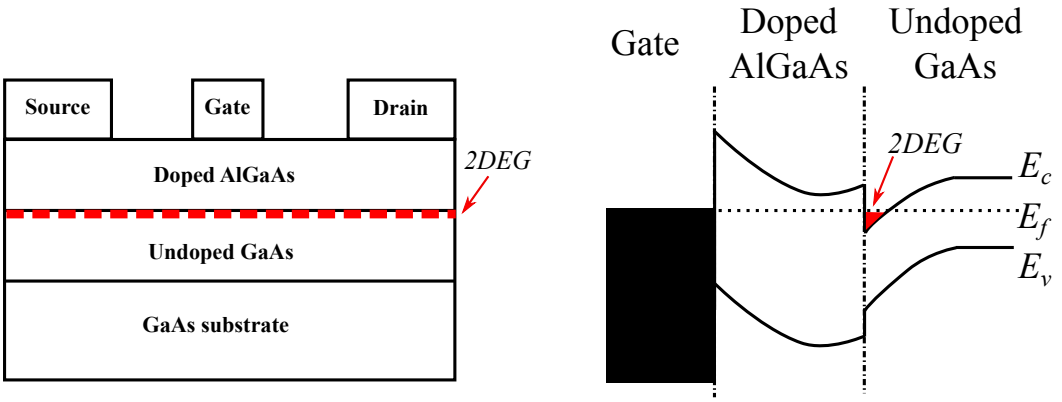

Figure 1.2: Basic AlGaAs/GaAs HEMT structure (left) and band diagram (right).

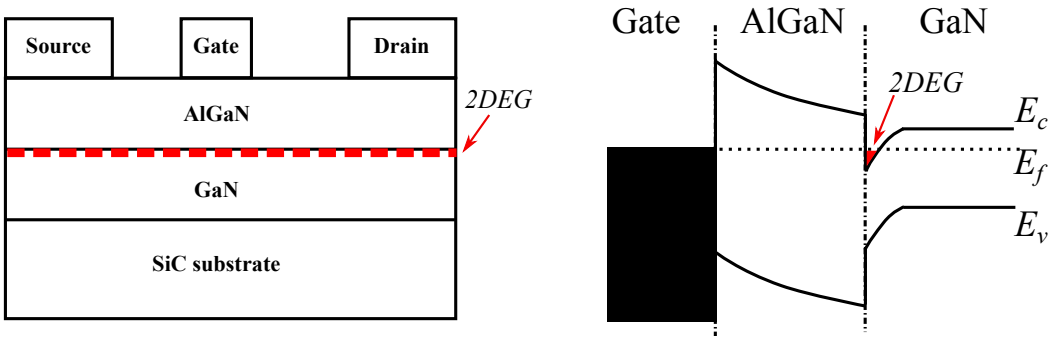

Figure 1.3: Basic AlGaN/GaN HEMT structure (left) and band diagram (right).

AlGaN/GaN HEMTs are realized in a similar way and a simplified structure is shown in Fig. 1.3 An important difference is that in this case it is possible to have a 2DEG even when the AlGaN layer is undoped [24]. Moreover, when the AlGaN layer is doped, the 2DEG carrier density is not proportional to the doping but to the Al concentration. In AlGaN/GaN HEMTs the origin of the 2DEG is thus different. It has been shown [25] that electrons that form the 2DEG can result from loosely bond surface electrons and from impurities in the AlGaN layer. As a consequence of the polar and piezoelectric nature of the AlGaN layer, during its growth an intense electric field is created with the negative side of the dipole facing the surface and the positive side facing the interface with GaN. The high electric field ($E \sim 10^6\,\mathrm{V\,cm^{-1}}$) causes electrons to drift towards the heterointerface and to the quantum well forming the 2DEG. As electrons move, the electric field is reduced until an equilibrium condition is reached. The Al concentration influences the stress at the AlGaN/GaN interface due to the lattice mismatch. The polarization and piezoelectric charge density and thus the electric field in the AlGaN are altered.

In reality, the structure of a GaN HEMT device is often more complex with additional layers [1]. A resistive AlN nucleation layer is often added between the SiC substrate and the GaN buffer. The use of another thin AlN interlayer between the AlGaN barrier and the GaN channel has been demonstrated to reduce the sheet resistance by increasing the mobility and electron density in the 2DEG. The growth of epitaxial layers on the substrate can be performed both by Metal

Organic Chemical Vapour Deposition (MOCVD) and Molecular Beam Epitaxy (MBE) techniques.

The metal electrode contacts are formed directly on the top AlGaN layer. For the drain and the source are used ohmic contacts as in MESFET. The gate contact is instead realized with a metal-semiconductor Schottky junction. High quality contacts with low resistance are important for high frequency and efficiency operation. A wide variety of combinations of metals and implanting technique have been studied. Ti/Al/Ni/Au alloys are often employed [12]. Gate contacts are often realized with a T-shape in order to realize short gate length with low parasitic resistance [26].

In an AlGaN/GaN HEMT, for $V_{gs} = 0$ and $V_{ds} = 0$, the band diagram is similar to the one in Fig. 1.3. The 2DEG has a high carrier concentration and the channel is on. For small value of the V_{ds} drain-source potential, a current starts to flow between the drain and source ohmic contacts through the 2DEG. Initially the current is proportional to V_{ds} but as the field increases the saturation electron velocity is reached with a consequent saturation of I_{ds}. The V_{gs} potential controls the 2DEG carrier density: as the gate-source voltage goes negative the electron density decreases with a reduction of I_{ds}. When the negative pinch-off voltage is reached the channel is fully depleted and the drain current is zero.

1.3 Trapping and dispersive effects

Despite the excellent performances already demonstrated at microwave frequencies and the tremendous potential in a variety of applications, the GaN technology still presents some issues that are not yet fully understood and need more investigation. In particular, the performances of GaN HEMTs can be limited by dispersion effects related to the presence of traps. Traps are also involved in the reliability of devices.

The AlGaN/GaN processing technology is not yet fully mature and the quality of materials is not perfect. The presence of crystallographic defects or dislocations and electronic states on the surface of the device, can act as charge trapping centres that limit the device performance [27]. The parasitic charge, moving in and out of trap energy states, affects the density of the 2DEG. Trapped carriers are maintained in these levels during an important lapse of time and cannot take

part in the conduction with a direct reduction of the carrier density in the 2DEG. What is probably more important is that trapped charges, forming a quasi-static charge distribution on the surface or inside the device, can change the electric field distribution altering the electric behaviour of the transistor.

Traps can be located at different position in the AlGaN/GaN HEMT structure: on the surface, in the AlGaN layer, at the heterostructure interface or in the GaN buffer layer [28,29]. Moreover, some trapping mechanisms are activated only under certain circumstances, for instance with high fields or after thermal stress. Traps can thus evolve during the operation of the device [30,31]. Hot-electron induced by high electric fields can generate new traps or lattice defects whit negative impact on the reliability of the device [27,32].

Different traps can have different effects on performances and on measured characteristics of devices. These effects include small-signal (i.e. transconductance and output conductance) frequency dispersion, anomalous IV characteristics (i.e. kink effect), gate- and drain-lag transients and limited RF output power [28]. For instance, in the early stage of the development of the technology, many AlGaN/GaN HEMTs showed a much lower RF output power density than expected from static IV characteristics [33]. This is referred to as *DC to RF dispersion* or *current collapse* and is a trap related phenomenon where both surface and bulk traps can contribute [3].

In general, traps lead to dynamic IV characteristics that are different from static one. The capture and emission of charge from trap centres are not instantaneous phenomena. Time constants associated with different trapping and de-trapping mechanisms can range widely from nanosecond to minutes [31,34,35]. These time constants are in any case longer than the period of RF signals. The state of traps is highly dependent on applied voltages and in general with higher fields more carriers can be trapped. However, being these slow phenomena compared to RF signals, trapped electrons cannot follow instantaneously the high frequency signal . Trapping phenomena are thus referred as *long-term effects* or, viewed in the frequency domain, as *low frequency dispersion*.

One form of current collapse due to traps which is commonly observed on measured static IV characteristics of devices, is the so called *kink effect*. An example of this effect will be discussed in Section 1.3.1.

Many characterization techniques have been developed over the years to study

traps and their influences on performances and reliability. Because of the dynamic behaviour of traps, many methods are based on some sort of pulsed or transient measurement. Other techniques are based for instance on low-frequency noise measurements [31, 36] or on electroluminescence (EL) measurements [37].

A widely adopted method to assess the extent of trapping in a device and to compare different devices or processes is based on a pulsed characterization [36–39]. The device is biased at a quiescent bias point defined by gate and drain bias voltages (V_{GB},V_{DB}). Gate and drain voltages are then synchronously pulsed to different amplitudes ($\hat{V}_G$,$\hat{V}_D$). For each ($\hat{V}_G$,$\hat{V}_D$) combination the resulting drain current is measured inside the pulses obtaining a pulsed output characteristic of the device:

$$I_D^P = I_D^P(V_{GB}, V_{DB}, V_G, V_D) \tag{1.1}$$

Because of the presence of traps and also due to self heating phenomena, pulsed IV characteristics performed starting from different bias points are in general different. Indeed, the state of all the traps is dependent on the starting static field distribution inside the device. To evaluate the amount of trapping and to rule out self heating effects, three pulsed characteristics are measured for three starting bias points, each whit a 0 W dissipated power:

A) $(V_{GB}, V_{DB}) = (0, 0)$: in this case, with no fields inside the device traps can be considered empty.

B) $(V_{GB}, V_{DB}) = (V_{Gpo}, 0)$: the gate is biased at pinch-off and the G-D and the G-S junctions are equally reverse biased.

C) $(V_{GB}, V_{DB}) = (V_{Gpo}, V_{Dsat})$: the gate is biased at pinch-off and the drain in the saturation region (i.e. $V_{Dsat} = 15\,\text{V}$). The field in the G-D region is high being $V_{GD} = V_{GS} - V_{DS}$.

An example of this type of characterization is schematically shown in Fig. 1.4. As can be seen, the three characteristics are quite different. For case A, with almost no trapping in the starting condition, the drain current is the highest. The reduction of drain current in case B is often attributed to the presence of traps below the gate. Finally, in case C, due to the high G-D field, electrons can tunnel from the gate metal and get trapped at the surface between the gate and the drain

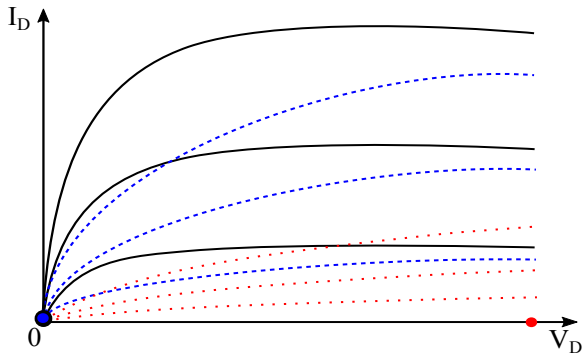

Figure 1.4: Schematic representation of pulsed characteristics of a dispersive device measured pulsing from three starting bias points $(V_{GB}, V_{DB}) = \ : A\ (0,0)$ (black), $B\ (V_{Gpo}, 0)$ (blue) and $C\ (V_{Gpo}, V_{Dsat})$ (red).

causing a significant reduction of the maximum drain current and an increase of the channel resistance [30, 34]. This charge distribution on the surface can alter the intrinsic controlling gate-to-source field. The effective V_{GS} is thus reduced compared to the externally applied one. This effect is referred to as *virtual gate* or *backgating*. To quantify the effect of traps and to compare different devices and technologies, it is possible to use a current collapse parameter defined as the ratio between the drain current measured in case A and the one measured in case B or C for the same $(\hat{V}_G, \hat{V}_D)$. This parameter is referred to as *slump ratio* [32]. In general, the discrepancy between case A and B has been put into relation with traps located below the gate and in part with traps on the surface between the gate and the drain. The discrepancy between A and C is instead strongly correlated with traps on the surface and with traps in the GaN buffer layer.

One assumption of this kind of pulsed characterization is that the used voltage pulses are shorter than traps and thermal time constants. The state of traps (and the internal temperature) is thus only defined by the starting bias point and does not change during the application of pulsed voltages. This assumption might not be correct as will be shown in Chapter 4. Commonly used pulse lengths are in the order of hundreds of nanoseconds or few microseconds. Thanks to the development of a new type of measurement setup for pulsed characterization, we show that in some circumstances even 50 ns are not short enough to consider the state of traps defined only by the starting bias point. This is important also because, pulsed IV characteristics, that are assumed to be *dispersion-free*, are also widely used as the

basis of some device modelling approaches.

The presence of the current collapse has severely limited the microwave output power of GaN HEMTs. Fortunately it was discovered that with the adoption of a SiN surface passivation the current collapse can be effectively reduced [40]. In fact, for SiN passivated devices, the discrepancy between the pulsed characteristics in the three cases is also strongly reduced [37]. The passivation helps in limiting the accumulation of charge on the surface and thus also the backgating effect. The adoption of field plates, which has been introduced to limit the high field between the gate and the drain, has been shown to also help in the reduction of current collapse [3]. These innovations allowed to obtain the outstanding performances presented in Section 1.1. However, the problem of traps is not yet resolved. As will be shown in Chapter 4 and Chapter 5, fast traps can alter the dynamic behaviour of the device, possibly becoming a source of distortion for modulated RF signals. Moreover, it has been shown that even if a virgin device presents little current collapse, after device degradation the trapping effect increases and plays thus a key role in reliability [41].

Other techniques that are commonly employed to evaluate trapping are the *gate-lag* and *drain-lag* measurements [29]. Gate (drain) lag can be defined as the response of the drain current to a step gate (drain) voltage variation. The current does not respond instantaneously to the voltage change and presents instead a slow transient that can be attributed to the presence of traps [42]. Gate-lag measurements are performed starting from a bias point similar to case *C*. A step gate voltage is applied (i.e. $V_G = 0$) and the drain current is measured. Drain lag is measured in similar way starting from a case *A* bias point and changing only the drain voltage. Various variants of these methods have been proposed and used to study traps in GaN HEMTs [28, 34, 35, 42].

In spite of this, a detailed understanding of traps is still lacking today. While all trapping effects result in some sort of degradation of performances, the dominant trapping mechanism could vary in devices grown by different methods or different processing procedures. A wide variety of phenomena have been observed by different groups with different methods and on different technologies and explanations are not always consistent. More research effort is needed to better understand trapping phenomena.

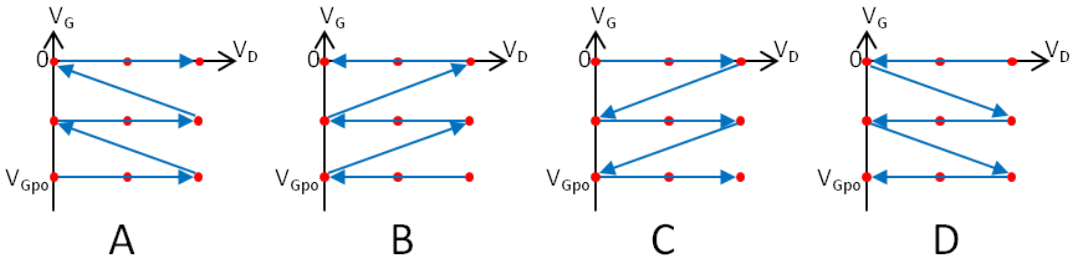

Figure 1.5: Schematic representation of sweep sequences for the four static characterizations.

1.3.1 Kink effect

To show how dispersive phenomena due to traps can affect static IV characteristics, in this Section an experiment conducted on an AlGaN/GaN HEMT device is presented. By means of an HP4156 Precision Semiconductor Parameter Analyzer, static IV characteristics are measured changing the way in which voltages are swept.

The common way of measuring static IV characteristics of FET-like devices is to sweep the gate voltage starting from below pinch-off (V_{po}) up to $V_G = 0\,\mathrm{V}$ or possibly up to a slightly positive gate voltage until the gate-source diode starts to conduct. For each gate voltage the drain voltage is swept from 0 V up to a safe maximum voltage V_{Dmax} and the drain current I_D is measured at every (V_G^i, V_D^i). In theory changing the order and direction in which voltages are swept should not have any influence on the obtained $I_D(V_G, V_D)$ characteristic.

We consider here four cases of the infinite possible (see also Fig. 1.5):

A) Common way:
sweep V_G from V_{po} up to 0 V
$\forall V_G$, sweep V_D form 0 V up to V_{Dmax}.

B) Reverse V_D:
sweep V_G from V_{po} up to 0 V
$\forall V_G$, sweep V_D form V_{Dmax} down to 0 V.

C) Reverse V_G:
sweep V_G from 0 V down to V_{po}
$\forall V_G$, sweep V_D form 0 V up to V_{Dmax}.

D) Reverse V_G and V_D:
sweep V_G from 0 V down to V_{po}
$\forall V_G$, sweep V_D form V_{Dmax} down to 0 V.

An AlGaN/GaN device with gate length of 0.25 µm and width of 400 µm (8×50) has been characterized in these four ways at room temperature. In all cases same voltages were used: $V_{Gmin} = -4$ V, $V_{Gmax} = 0$ V, in steps of 0.2 V; $V_{Dmin} = 0$ V, $V_{Dmax} = 30$ V, in steps of 0.5 V.

The static IV characteristic obtained in the common way A is shown in Fig. 1.6. What is referred to as *kink effect* or *current collapse* [33] is clearly observed in the knee region for drain voltages around 4 V to 7 V with an abrupt increase in drain current and output conductance. Kink effect in GaN is linked to charge carrier trapping in deep levels located in the epitaxial layer [43],in the GaN buffer layer below the gate [44] or in the upper band gap region of the AlGaN barrier [45]. This effect is not eliminated with SiN surface passivation (as in the case of the measured device) suggesting that surface traps are not involved. These traps have long time constants associated and the effect is a strong function of the maximum drain voltage. When carriers are trapped create a negative charge below the gate which act reducing the effective intrinsic gate to source controlling field and as a consequence the drain current. This is in fact a backgating effect.

Observing case B, where the drain voltage is swept from high to low voltages, carriers are trapped at maximum drain voltage but during the sweep to lower voltages carriers have enough time to be gradually emitted back and the kink effect is not present. In the A case instead, for a fixed V_G, traps are filled sweeping to higher drain voltages. When V_G is then changed and a new sweep in V_D begins, traps are still filled and this is evident in the reduction of the drain current in the knee region. When a critical drain voltage is reached (e.g. 4 V to 7 V) traps are then released with an increase of the drain current. This long-term memory behaviour is even more evident from the characterization in the C case in Fig. 1.6. The first characteristic for $V_G = 0$ V presents no kink because starting from ($V_G = 0, V_D = 0$) traps are empty. The second curve, for $V_G = -0.2$ V present instead an evident kink. This is due to the fact that traps were charged by the high V_D reached at the end of the previous sweep for $V_G = 0$ leading to a reduction of the intrinsic G-S controlling field. Finally, the D case is almost identical to case B showing that the direction in which the gate voltage is swept

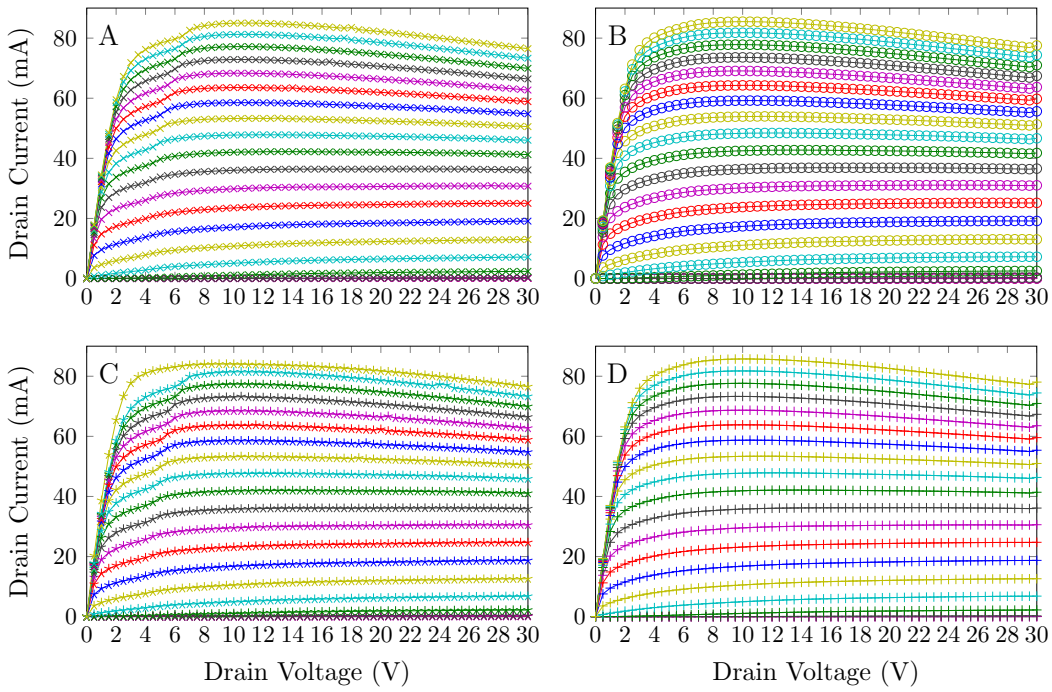

Figure 1.6: Static IV characteristics of the same device carried out in the four different ways.

has not influence when the drain is swept from high to low voltages.

In case A the amount of kink depends also on the maximum drain voltage reached during the characterization. In Fig. 1.7 are shown two static characteristics of same device, in one case without any maximum DC power compliance and in the other with a compliance of 1 W. The drain voltage at which the kink occurs (V_{Dkink}) can be defined as the V_D where a peak in the output conductance g_d occurs. The position of the kink in the two cases is compared in Fig. 1.8 while in Fig. 1.8 is shown the calculated g_d at V_{Dkink} versus gate voltage. With a higher $g_d(V_{Dkink})$ is associated a more evident kink in the static characteristic. When lower maximum V_D are reached during the characterization the kink is less pronounced and is shifted to lower voltages.

The amount and position of the kink is also dependent on the speed of the voltage sweep. The HP4156 instrument allows to set the sweeping speed in terms of the time to wait for every imposed (V_G,V_D) before taking the current measurement. Previous measurements in this Section have been carried out with a 50 ms delay. Case A has been repeated with two different settings for this delay: 0 s and 1 s. For the slower sweep more carriers are trapped and this reflects in a higher output

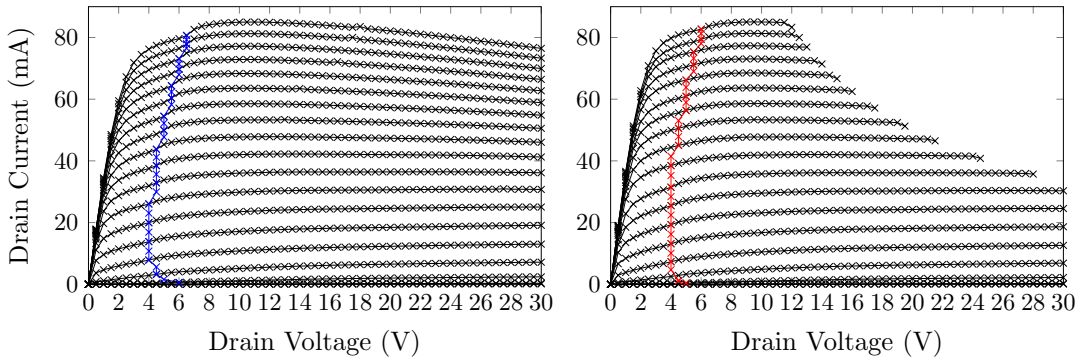

Figure 1.7: Static IV characteristics of the same device without (left) and with a 1 W DC power compliance (right). In evidence the V_{Dkink} voltage.

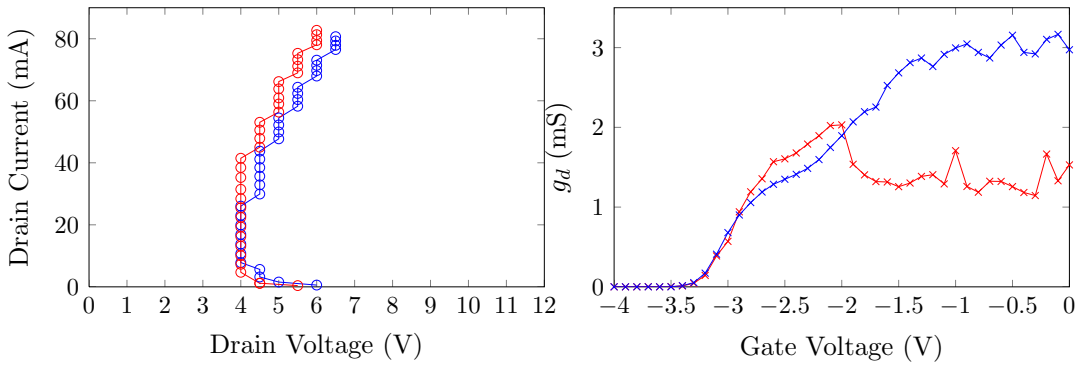

Figure 1.8: Comparison of V_{Dkink} (as seen in Fig. 1.7) (left) and output conductance g_d at V_{Dkink} (right), for no DC power compliance (blue) and 1 W compliance (red).

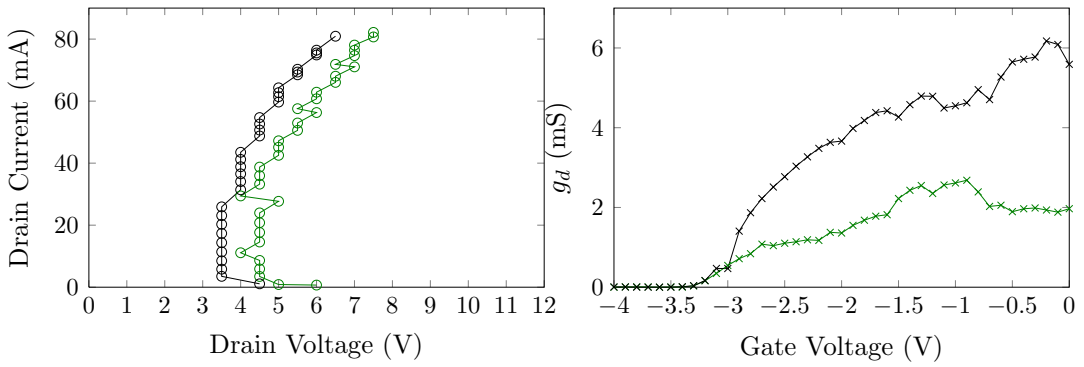

Figure 1.9: Comparison of V_{Dkink} (left) and output conductance g_d at V_{Dkink} (right), for no delay (green) and with 1 s delay (black). No power compliance in both cases.

conductance at the kink voltage V_{Dkink} that is also shifted to lower V_D as shown in Fig. 1.9. In fact, whit a pulsed characterization the kink is rarely observed demonstrating how for this effect slow trapping and detrapping phenomena are involved.

This proves further how long-term memory effects are affecting also the shape of DC output characteristics of devices. These traps are strongly dependent on the peak drain voltage or on the peak drain-source electric field. The static characteristic of a GaN device it thus dependent on the way it is measured. This has to be considered carefully if DCIV are used in the extraction of devices models, in particular the knee region can change significantly.

1.3.2 Thermal effects

Despite GaN allows to operate with higher channel temperatures, the performance of the device is still dependent on the thermal state. Even with a good efficiency, a high RF power density means also a high dissipated power. The increase of channel temperature due to the dissipated power inside the device leads to lower carrier mobility and saturation velocity with a consequent reduction of the drain current and thus of the output power [46, 47]. The junction temperature depends on the ambient temperature, the dissipated power and on the thermal resistance

of the device, i.e.:

$$T_j = T_A + R_\theta P_{DISS} \tag{1.2}$$

The SiC substrate has a low thermal resistance and helps in limiting the channel temperature. In some applications this could not be enough and Diamond substrates are also evaluated despite the higher cost [48]. A method for the characterization of the thermal resistance will be presented in Chapter 3.

Moreover, like traps, the change of the internal device temperature is not instantaneous and has one or more associated time constants. Self-heating/cooling effects are much slower than the fast varying RF signal, therefore are also considered *dispersive* or *long-term-memory effects*.

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Chapter 2

C-band AlGaN-GaN MMIC HPAs for SAR

The advantages offered by GaN-on-SiC technology in terms of high power density and efficiency at microwave frequency are becoming attractive, not also for commercial applications, but even for strategic fields like communication infrastructures, military and space. To give evidence of obtainable performances, also compared to GaAs technology, in this Section some GaN MMIC high power amplifiers designed and realized as part of the research activity are described. This work has been developed in the framework of a project funded by the Italian Space Agency (ASI) to make an assessment of the performance of GaN technology for future satellite Synthetic Aperture Radar (SAR) systems. In SAR and in active electronically scanned array (AESA) antennas, hundreds or thousands of transmit/receive (T/R) modules are employed. Each module includes at least HPA, LNA, phase shifter and switches or circulator. A modern T/R module may require more than ten MMICs integrated on a substrate with other discrete components. There is a big interest in reducing cost and size of T/R modules and GaN is a very promising candidate for this type of application [1–3]. The technology allows to realize compact HPA but also linear and robust LNAs and mixers whit big advantages. For instance, the circulator and/or the limiter, that is usually necessary whit GaAs MMIC, could be avoided and more circuits can be integrated on a single MMIC [4–6].

C-Band MMIC HPAs have been designed exploiting a 0.25 µm gate length HEMT GaN process on SiC substrate. The HPAs are designed for future SAR

antenna applications. A first single-stage HPA delivers 10 W of output power at 5.8 GHz with a 50 % Power Added Efficiency (PAE). A double-stage HPA delivers 16 W output power with PAE over 38 % at 6 dB gain compression within a 900 MHz bandwidth around 5.75 GHz. Up to 20 W output power and 40 % PAE are obtained at higher gain compression. A comparison with another amplifier, differing only for the layout of the devices in the final stage, points out that the transistor thermal conditions represent the main limitation for this high power density technology.

2.1 Technology and device characterization

The selected technology is a 0.25 µm gate length HEMT AlGaN-GaN process on SiC from United Monolithic Semiconductors foundry. The process characteristics are described in [7], where also long-term reliability data are provided. Static and pulsed I/V characteristics, S-parameters and load pull measurements were carried out on device samples in order to select the best device periphery for the application: an 8 fingers by 125 µm cell was chosen as the best compromise in terms of output power, PAE, gain and source/load impedances: indeed, larger peripheries were discarded since they showed a decrease of the PAE. The selected quiescent bias point is at class AB with $V_D = 30$ V and $I_D = 80$ mA/mm (about $I_{DSS}/6$). In Fig. 2.1 the measured (CW) load-pull contours and optima for maximum output power and PAE are shown. The optimum output impedances for power (Z_P) and PAE (Z_E) are close to each other, which is useful for the design. The measured performance of the 1 mm cell, loaded with Z_P and Z_E, are also shown in Fig. 2.1. The drain currents at maximum output power are 326 mA and 285 mA respectively. The small signal gain, almost unchanged for the two loads, is about 18.5 dB, while maximum power is obtained at 3.4 dB compression. Performance differences between Z_P and Z_E are limited and the two loads are quite similar: hence a good power/PAE compromise has been possible by choosing an intermediate load between Z_P and Z_E.

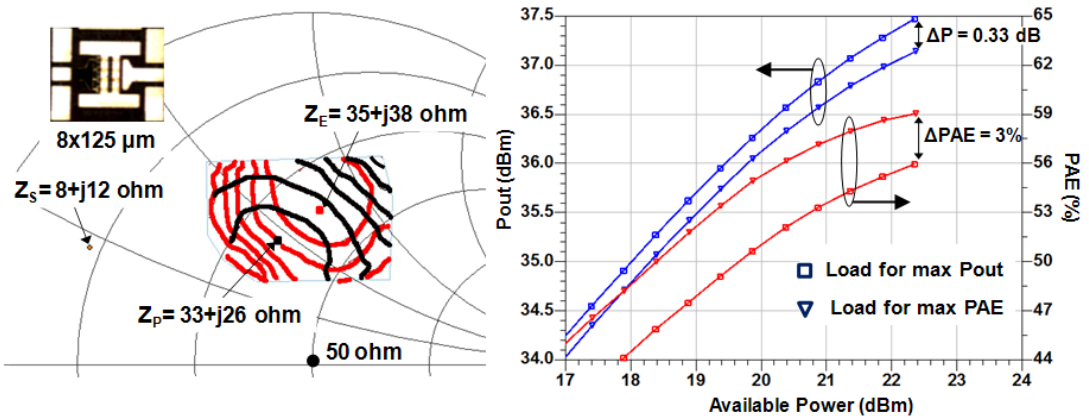
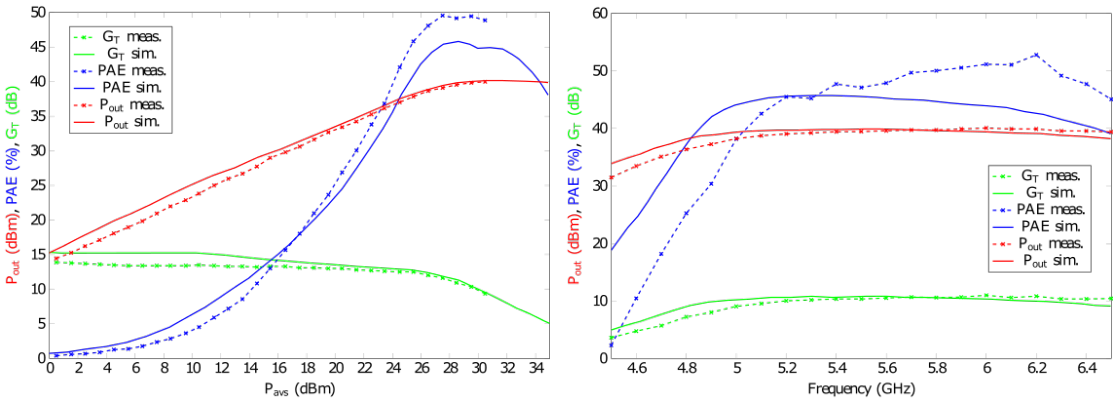


Figure 2.1: Measured load-pull contours for the $8 \times 125\,\mu m$ cell and CW performance for the cell loaded with Z_P and Z_E.



(a) (b)

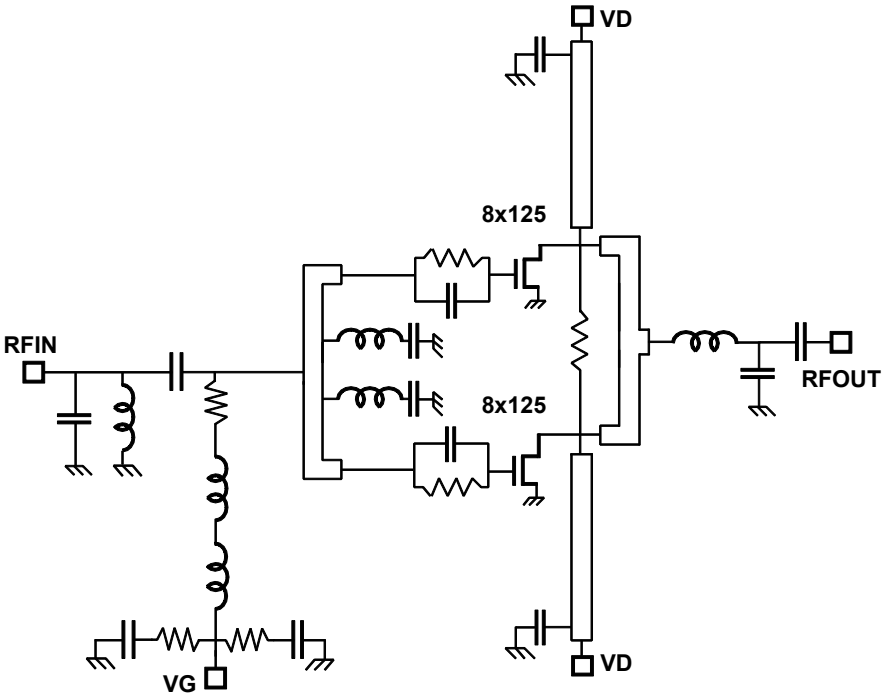
Figure 2.2: Single-stage HPA measured and simulated performances. Compression characteristic at 5.8 GHz (a) and performance along the bandwidth at 3.5 dB gain compression (b).

2.2 Single-stage HPA

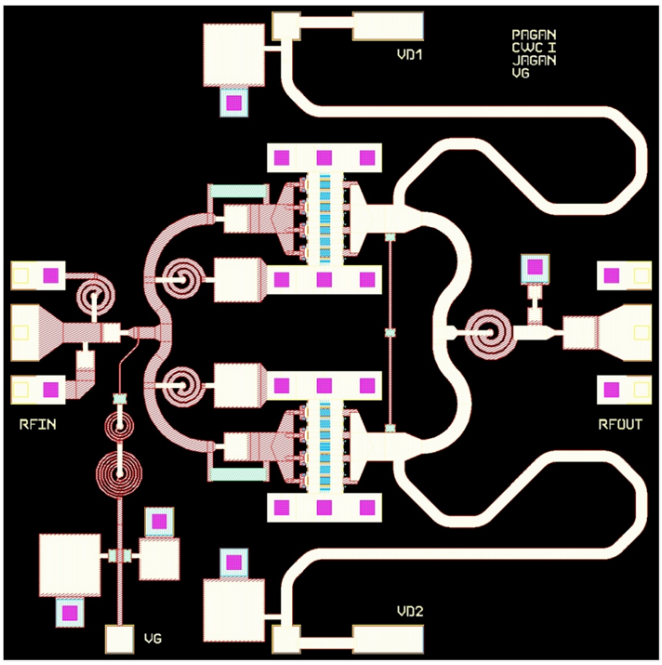
For a first foundry run a single-stage class AB HPA was designed. The purpose of this design was to explore the capabilities of the technology and the accuracy of available models. For this, a simple topology with two devices in parallel was selected. The schematic and the layout of the HPA are shown in Fig. 2.3. The two devices used in the circuit are $8 \times 125\,\mu m$ cells that are separated allowing a better thermal dissipation and limiting self-heating. The single devices are made unconditionally stable from 300 MHz upwards by a parallel RC stabilization network directly in series to the gate port. The input and output matching is realized with lumped components and by the distributed input and output coupling networks. The two short-circuited stubs are also part of the output matching and allow to bias the drain of devices. A resistor is added between drain outputs to suppress eventual differential oscillations.

The MMIC realized by the foundry was mounted on a metallic carrier and bias pad were bonded to a test jig. The HPA was then characterized in CW conditions with baseplate at ambient temperature. The measured and simulated performances versus input power at 5.8 GHz are shown in Fig. 2.2a. The peak output power is 40 dBm (10 W) with 50 % PAE and 10.5 dB associated gain at about 3.5 dB gain compression. This performance corresponds to 5 W/mm of RF power per device periphery at C-band. The measured PAE is higher than the simulated one. This was expected also from load-pull measurements. The used foundry model [7] tend to overestimate the DC drain current and thus a lower $PAE = (P_{OUT} - P_{IN})/(V_{D0}I_{D0})$ is obtained in simulation. The dynamic drain current under large-signal operation and in particular its DC component is strongly affected by the presence of dispersive phenomena due to both thermal effects (e.g. self-heating) and charge trapping phenomena [8]. Models that take into account these phenomena are needed for an accurate prediction of the PAE [9, 10]. The small error (≤ 1 dB) in gain at low source available power was also expected being the model optimized for large-signal design. In the graph of Fig. 2.2b the HPA measured performance along the bandwidth with fixed available input power of 29 dBm are given (about 3.5 dB gain compression). Output power exceeds 39 dBm from 5.2 GHz to at least 6.5 GHz, with an associated gain of 10 dB. In the same bandwidth the PAE is higher than 45 %.

In Table 2.1 these performances, obtained with GaN HEMTs, are compared



(a)



(b)

Figure 2.3: Schematic (a) and layout (b) of the single-stage C-band HPA. Circuit dimensions are $2 \times 2\,\mathrm{mm}$.

Ref.	Tech.	Freq. (GHz)	P_{OUT} (dBm)	PAE (%)	Gain (dB)	Area (mm^2)	Power density (W/mm)
This work	GaN	5.2–6.5	40	52	10.5	4	5
[11]	GaAs	3.5–4	39	35	16.5	13.4	0.53

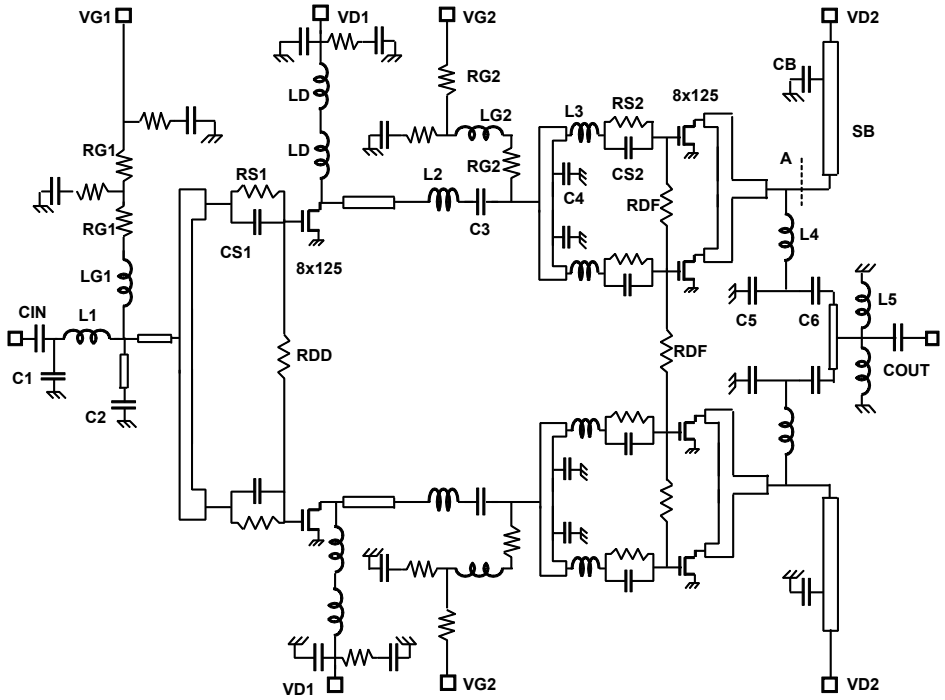
Table 2.1: GaN and GaAs C-band MMIC HPAs comparison.

with a GaAs 8 W, S/C-band MMIC HPA found in literature and presented in [11]. The advantages of GaN technology are evident. In Table 2.1 are reported the peak P_{OUT}, PAE and Gain over the bandwidth. The presented HPA has higher performances over wider bandwidth. The power density is calculated as the peak output power divided by the total periphery of transistors of the power stage. The GaAs HPA has indeed two stages and this explain also its higher gain. With GaN is obtained an order of magnitude higher power density with much better efficiency and bandwidth.

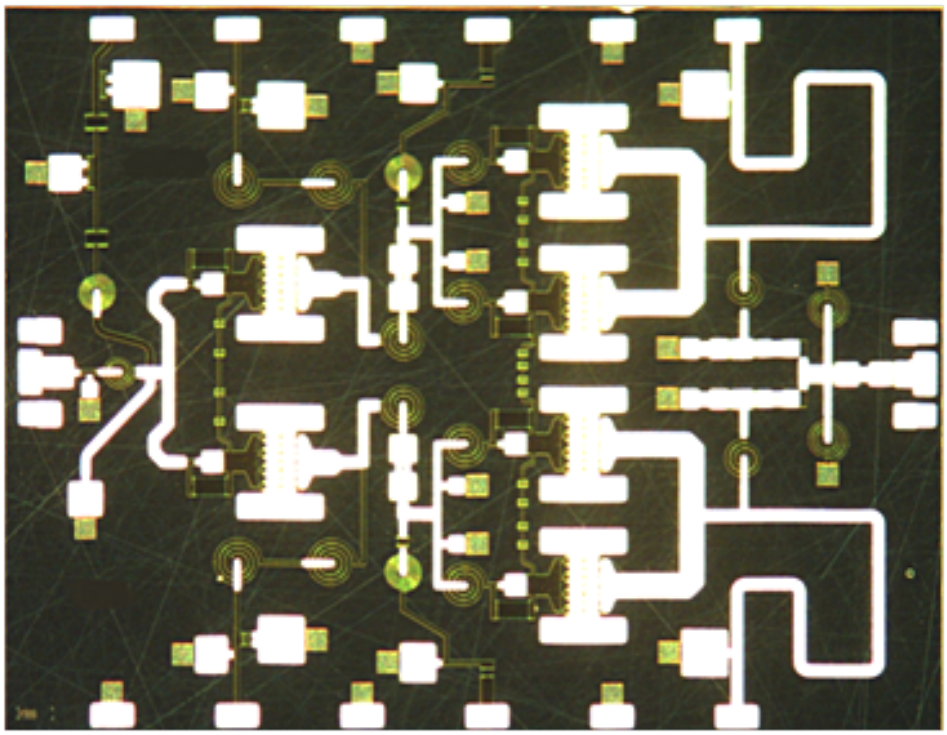
2.3 Double-stage HPA

The schematic and a picture of a double-stage HPA are shown in Fig. 2.4. All the devices used in the circuit are 8×125 µm cells. The transistors were made unconditionally stable from 300 MHz upwards, by synthesizing an RC stabilization network (RS, CS) directly at the gate port. An extensive use of lumped passive components was necessary in the matching and bias networks, due to the relative low operative frequency of approximately 5.5 GHz. RF chokes in the bias networks are mainly implemented with spiral inductors (LG1,LG2,LD). The exceptions are the second stage drain bias networks: in this case the use of spiral inductors was not viable, because of the high current levels. It was also impossible to use $\lambda/4$ lines, which is too bulky for this frequency (5.5 mm on SiC substrate). Hence short-circuited stubs (SB in Fig. 2.4a) were used to feed the bias current: these stubs are short-circuited near the DC pads with a large MIM capacitor (CB) connected to ground. At their connection point to the output combining network (A in Fig. 2.4a), the stubs synthesize a selected impedance, which is part of the device matching.

For its characterization the HPA was mounted on a test jig as shown in Fig. 2.5.



(a)



(b)

Figure 2.4: Schematic (a) and picture (b) of the C-band HPA. Circuit dimensions are $4.5 \times 3.5\,\mathrm{mm}$.

To manage the power dissipation and to control the base plate temperature the test jig is then mounted on a Peltier cell. The drain voltage was pulsed from

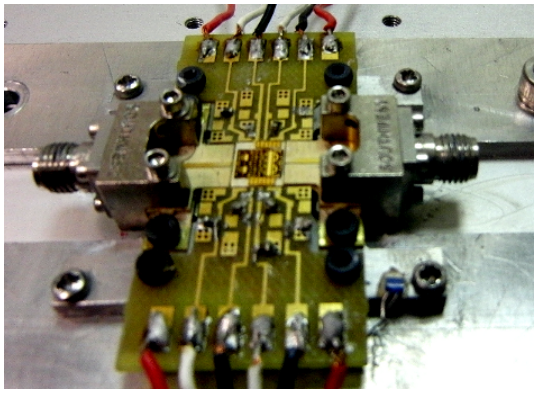


Figure 2.5: MMIC HPA mounted on test jig for characterization.

0 V to 30 V, with fixed gate bias voltage. The pulse width is 100 µs, with a duty cycle of 30 %. These values represent very long pulses and duty cycle for radar applications, hence they are severe operating conditions. Shorter pulse width and duty cycle would reduce the device channel temperature, improving performances. The HPA pulsed S-parameters are shown in Fig. 2.6 at 30 °C base plate.

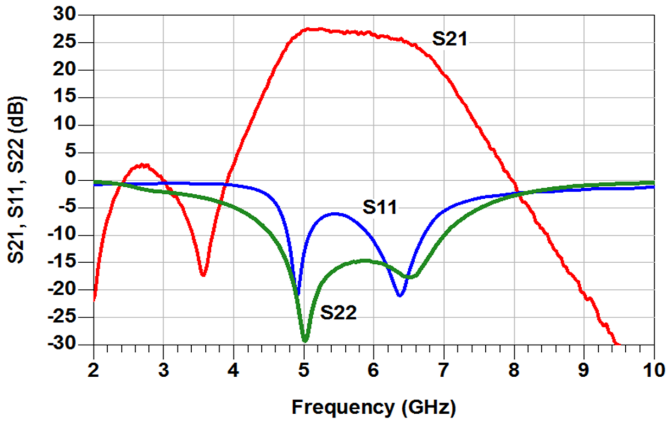
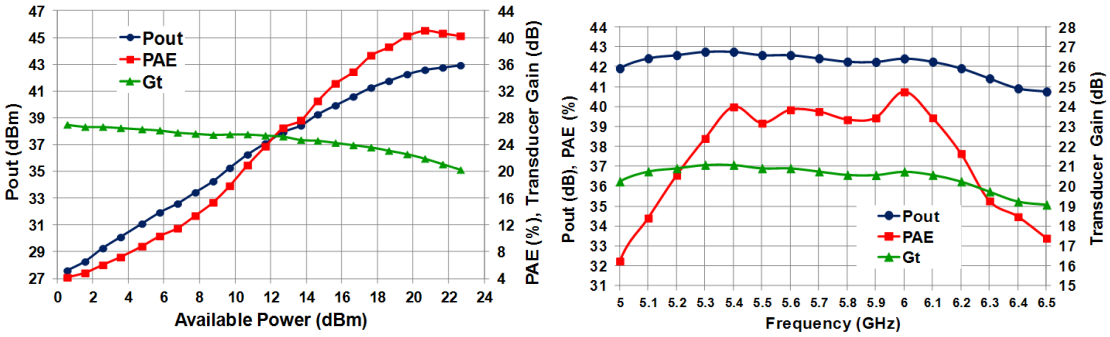


Figure 2.6: Pulsed S-parameter of the HPA at 30 °C base plate.

The HPA linear gain exceeds 25 dB in a 1.6 GHz bandwidth; in that bandwidth $|S_{11}| \leq 7$ dB and $|S_{22}| \leq 15$ dB. In Fig. 2.7a the large signal characteristic of the amplifier is shown at 5.4 GHz at 30 °C: in this condition the device channel temperature is below 80 °C. The peak power is 20 W with 40 % PAE and 20 dB



(a) (b)

Figure 2.7: Double-stage HPA compression characteristic at 5.4 GHz (a) and performance along the bandwidth at 6 dB gain compression (b).

associated gain at about 6 dB gain compression. This peak performance corresponds to 5 W/mm of RF power per device periphery at circuit level. The HPA operates in class AB, with drain current of the HPA during the pulse of 1.65 A (480 mA bias). In the graph of Fig. 2.7b the circuit measured performance along the bandwidth with fixed available input power of 21.5 dBm are given (about 6 dB gain compression). Output power exceeds 42.05 dBm (16 W) from 5 GHz to 6.2 GHz, with an associated gain over 20 dB. PAE is bigger than 37 % from 5.2 GHz to 6.2 GHz.

To the authors knowledge these performances represent the state of the art for GaN MMIC HPA for this application. Indeed, while several examples of C-band GaN hybrid HPAs are described in the literature, it was not possible to find information about published C-Band MMIC HPA for T/R module space SAR application. On the contrary, some example of GaN MMIC HPAs can be found at present for X-band SAR application. A few examples of GaN MMIC HPAs covering C band are the ones in [12,13] and [14], but these circuits address different applications with broader bandwidth, making a direct comparison unfeasible. The obtained performances of the double-stage HPA are compared in Table 2.2 with published C-band MMIC HPAs for this type of application. The different GaAs based technologies representing up to now the typical solution for this application were considered. The proposed GaN design features clear advantages in terms of power density and physical dimensions. It is worth to notice that also the pulse width and duty cycle conditions are important parameters to be taken into account when comparing the different circuits.

Ref.	Technology	Freq. (GHz)	P_{OUT} (dBm)	PAE (%)	Gain (dB)	Area (mm^2)	Power density (W/mm)	Pulse/duty (µs/%)
This work	GaN HEMT	5.2–6.2	42.1–43	37–41	20	15.75	5	100/30
[15]	GaAs HBT	4.7–6	41.8–42.4	31–41	18	60	2.17	100/10
[16]	GaAs pHEMT	4.9–6.1	44.3–44.9	30–35	16.5	27.23	1.29	20/2
[17]	GaAs pHEMT	5.2–5.6	42–42.2	45–50	21	25.3	0.67	25/10
[18]	GaAs pHMET	5–6	38.5–39	35	18	15.23	0.75	10/25
[19]	GaAs HBT	5–6	39–40	45–50	21	37.34	2.6	CW

Table 2.2: C-band MMIC HPAs for Radar Applications

2.4 Thermal issues with power-bar approach

A second version of the double-stage HPA was designed (namely HPA2, while the first version will be referred to as HPA1) in order to explore the performance and issues of a more compact topology solution. HPA2 is totally similar to HPA1, but it employs a power-bar topology in the final stage. The difference is visible in Fig. 2.8: in the power-bar the devices are packed together in a smaller area (0.73 mm^2 vs 1.03 mm^2), sharing the via holes connecting their sources to ground. This space saving (−29 %) would be necessary in the design of an HPA with eight HEMTs in the final stage for higher output power. Small differences in the combining networks of the two HPAs do not compromise the following comparisons, since their losses are practically identical. Performances of the HPAs at peak output power are listed in Table 2.3.

The devices of HPA1 have more chip area to dissipate power, leading to a lower operating temperature. For this reason HPA1 delivers more power with better PAE. These thermal effects prove to be particularly critical when dealing with GaN on SiC, due to the nonlinear thermal behaviour versus the dissipated power as observed for example in [20]. Measured DC power consumptions of driver stages P_{DCD} are almost identical (HPA1: 7.83 W, HPA2: 7.97 W) indicating that the drivers operate in very similar conditions. Measured DC power consumption

	P_{OUT} (W)	PAE (%)	Gain (dB)	P_{DCFS} (W)	P_{DFS} (W)	P_{DD} (W/mm)	P_{DA} (W/mm^2)	P_{DCD} (W)
HPA1	20	40	20.2	40.02	18.22	4.56	17.7	7.83
HPA2	17.5	34	16.3	42.49	22.09	5.52	30.26	7.97

Table 2.3: HPA Pulsed performances at Peak Output Power.

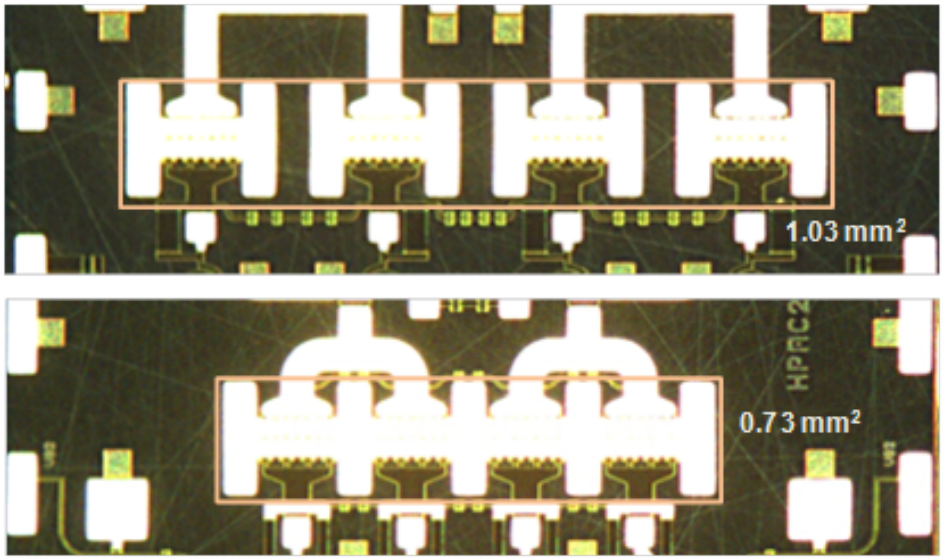


Figure 2.8: Final stage configuration and occupied area: HPA1 spaced devices (top), HPA2 power-bar topology (bottom).

P_{DCFS} and estimated dissipated power P_{DFS} of transistors in the final stage are also shown in Table 2.2. In particular, the latter is calculated as:

$$P_{DFS} = P_{DCFS} + P_{INFS} - (P_{OUT} + P_{LOSS}) \tag{2.1}$$

where P_{INFS} (RF power at the input of the final stage) and P_{LOSS} (losses in the output combiner) are simulated values. Simulations of P_{LOSS} are supported by measurements on separate cut-out passive structures and P_{INFS} is simulated very similar for the two HPAs. As shown in Table 2.3, lower peak output power is obtained from HPA2 ($-12.5\,\%$) at higher DC power consumption (lower PAE). Thus the topology of HPA2 leads to higher power dissipated per mm of active periphery P_{DD} ($+21\,\%$) as well as higher power dissipated per mm^2 of chip area P_{DA} ($+71\,\%$), which is a really noticeable result. According to our analysis, such a large difference in P_{DA} is mainly due to nonlinearity effects of the thermal resistance R_θ with the dissipated power [20], causing a detrimental thermal feedback in the compact topology. A verification of the proposed analysis was performed by measuring the HPAs with 1 µs pulse width and 1 % duty cycle: in those conditions, where the thermal effect is negligible, the difference in the HPAs output power falls to $-1\,\%$, validating the proposed considerations. These results confirm the

influence of thermal budgeting in the exploitation of the GaN technology and they remind the need of nonlinear models for the accurate R_θ prediction to optimize the circuit performance at design level, while keeping reliable channel temperature operation. In this work the electrical models provided by the foundry [7] have been used for the determination of the device large-signal operating point, while in-house thermal impedance measurements [21] were exploited for the computation of the operating channel temperature.

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Chapter 3

Nonlinear thermal resistance characterization

3.1 Introduction

GaN-based technology nowadays offers interesting features for the implementation of microwave integrated circuits in terms of high power densities, high temperature operation, energetic efficiency and ease of matching network design as shown in Chapter 2. However, thermal management at transistor, circuit and system level is one of the most important issues, which still require reliable solutions. Full electrothermal models of transistor are needed in this context. They should be able to provide accurate predictions of the electrical device behaviour depending on the base plate temperature and the instantaneous dissipated power in the device active area, also in order to guarantee thermally safe operating conditions for the device. To this aim suitable methods for the numerical computation or empirical characterization of the device thermal resistance (or, more in general, impedance, when pulsed operation is involved like in radars) are needed. Some approaches (e.g. [1, 2]) are based on channel temperature measurements using different direct sensing techniques, which however require special equipment and, in many cases, can be applied only with special-purpose, thermal-analysis-oriented device structures and geometries. Other techniques are based on more conventional electrical measurement techniques like, for instance, using the intrinsic temperature dependence of the on-state gate junction I-V characteristic as a built-in temperature sensor (e.g. [3]). These have the advantage of not requiring

special-purpose measurement equipment or device structures and have already been used for GaAs FET thermal characterization. These methods, however, have not yet been fully validated in the case of GaN HEMTs, where some problems may arise, owing to specific features of GaN technology (e.g. particular gate junction characteristics, strong influence of the temperature dependence of the source/drain parasitic resistors).

In this Chapter a different approach for the characterization of the nonlinear (i.e. temperature/power dependent) thermal resistance of GaN devices is presented. This method only requires conventional static drain current measurements at different base plate temperatures and small-signal S-parameter measurements, carried out at a frequency well above the upper cut-off of low- frequency dispersion over a set of different biases in the current saturated region. This approach consists of using the low-frequency dispersive effect on the drain current due to self-heating phenomena as the sensing parameter of the channel temperature changes deriving from dissipated power variations.

Since GaN FETs are also affected by charge-trapping (which are additional dispersive phenomena), in order to correctly extract the thermal resistance parameters by best-fitting the measured data, the thermal resistance description is embedded in a full electro-thermal model, where also low-frequency drain current dispersion due to traps is taken into account. This does not only allow for the correct identification of the self-heating dispersion and consequently of the thermal resistance, but has also the advantage of leading to an intrinsically coherent, compact electro-thermal model. As GaN devices are capable of operating at relatively high temperatures with high power densities, non-linearity of heat-conduction phenomena is taken into account by considering in our thermal model a second-order dependence of the channel temperature on the dissipated power.

3.2 Nonlinear electrothermal modelling

We consider now the problem of characterizing the nonlinear electrothermal behaviour of an on-wafer device sample. In particular, the following description of the thermal resistance is assumed:

$$R_\theta[P, \theta_B] = R_{\theta 0} + R_{\theta P} P + R_{\theta B}(\theta_B - \theta_B^*) \tag{3.1}$$

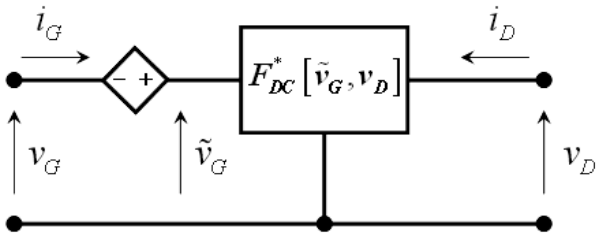


Figure 3.1: Intrinsic device description used for thermal resistance extraction.

where P is the dissipated power within the device; $theta_B$ is the base plate temperature; θ^*_B is a reference base plate temperature; $R_{\theta 0}$ is the thermal resistance value at θ^*_B and ideally zero dissipated power, while $R_{\theta P}$ and $R_{\theta B}$ are the thermal resistance sensitivities with respect to power and base plate temperature variations.

The proposed method allows to characterize the three coefficients $R_{\theta 0}$, $R_{\theta P}$ and $R_{\theta B}$ on the basis of small-signal parameters and static I/V characteristics at two different base plate temperatures. To this aim, we consider the model sketched in Fig. 3.1. Extrinsic parasitic elements are thought as already de-embedded and displacement current contributions are not considered here. Indeed, the model is intended for describing only the purely resistive part of the dynamic device behaviour, since displacement currents can be separately taken into account by means of a parallel capacitive 2-port network.

The dynamic drain current is described here by means of:

$$i_D(t) = F^*_{DC}[v_G(t) + \Delta v_G(t), v_D(t)] \tag{3.2}$$

where $F^*_{DC}[\,]$ is the static I/V characteristic measured by keeping constant the base plate temperature at the reference value θ^*_B. This characteristic is controlled by an equivalent intrinsic gate voltage: $\tilde{v}_G = v_G + \Delta v_G$ and the intrinsic drain voltage v_D. The equivalent gate voltage deviation Δv_G is defined by:

$$\Delta v_G = \alpha_G(v_G(t) - V_{G0}) + \alpha_D(v_D(t) - V_{D0}) + \alpha_\theta[v_G](\theta_0 - \theta^*_S(t)) \tag{3.3}$$

where α_G, α_D are model parameters; $\alpha_\theta[\,]$ is a model function; V_{G0}, V_{D0} are the average values of the instantaneous gate and drain voltages v_G, v_D ; θ_0 is the actual channel temperature in dynamic operation (thought as averaged along the channel) and θ^*_S at the generic time t is the channel temperature that would be

observed under stationary operation in the presence of $V_G = v_G(t)$, $V_D = v_D(t)$ and with the base plate temperature at the reference value θ_B^*.

The three terms introduced in the gate voltage deviation (3.3) explain the differences between the actual dynamic current $i_D(t)$ and $F_{DC}^*[v_G(t), v_D(t)]$ in terms of different statuses of traps (two terms corresponding to gate and drain lag effects) and different channel temperatures. Gate and drain lags are here treated in a simplified way as linearly dependent on the gate and drain purely-alternate voltage components $v_G(t) - V_{G0}$ and $v_D(t) - V_{D0}$ through the two scalar coefficients α_G and α_D [4]. This has been considered sufficient for the purpose of thermal resistance characterization and for a simplified electrothermal modelling approach within the scope of this work.

The third term in (3.3) refers to a thermal correction. It can be further developed by considering that:

$$\theta_0 = \theta_B + R_\theta[P_0, \theta_B]P_0 \tag{3.4}$$

$$\theta_S^*(t) = \theta_B^* + R_\theta[p_S^*(t), \theta_B^*]p_S^*(t) \tag{3.5}$$

where P_0 represents the averaged dissipated power in a generic dynamic regime and $p_S^*(t)$ is the power that would be dissipated under stationary operation in the presence of $V_G = v_G(t)$, $V_D = v_D(t)$ and with $\theta_B = \theta_B^*$:

$$p_S^*(t) = v_D(t)F_{DC}^*[v_G(t), v_D(t)] \tag{3.6}$$

3.3 Nonlinear thermal resistance identification

The electrothermal model (3.2)-(3.6) is used in this section for the identification of the nonlinear thermal resistance (3.1) of a GaN HEMT with $L = 0.25\,\mu\text{m}$ and a total periphery of $600\,\mu\text{m}$.

The static I/V characteristic $F_{DC}^*[\,]$ is measured on-wafer at the reference base plate temperature $\theta_B^* = 36\,^\circ\text{C}$ and is shown in Fig. 3.2.

The thermal resistance identification procedure consists of two steps.

In the first step, the base plate temperature is held at the reference value θ_B^* and multi-bias S-parameters are measured at a frequency low enough to neglect

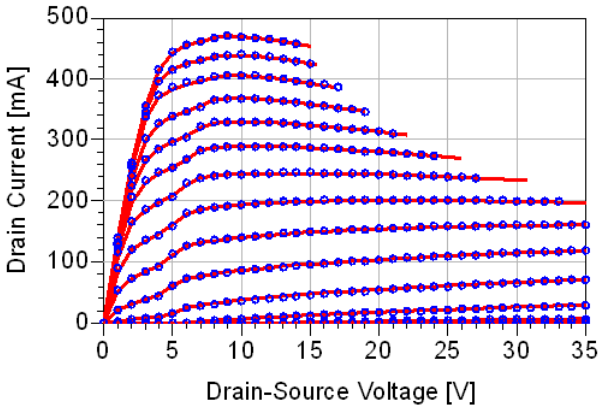


Figure 3.2: GaN HEMT ($L = 0.25\,\mu m$, $W = 600\,\mu m$): static I/V characteristic at the reference base plate temperature $\theta_B^* = 36\,°C$; $-3.5\,V < V_G < 0.5\,V$ (step $0.25\,V$). Model predictions (red lines) coincide with measurements (circles) at $\theta_B = \theta_B^*$ since $\Delta v_G = 0$ under static operation.

reactive effects in the transistor, but high enough to be greater than the upper cut-off frequency of dispersive phenomena due to traps and thermal effects. In our experiment a frequency about hundreds of MHz has been chosen, in a range where the trans- and output conductance of the transistor (i.e. the real parts of admittance parameters Y_{21} and Y_{22}) are almost independent of frequency.

The S-parameters are measured at the same base plate temperature used for the static characterization: $\theta_B = \theta_B^*$. In this small signal condition the dissipated power is defined by the bias point ($P_0 = V_{D0} \times I_{D0}$) and is obviously the same dissipated power of the reference static I/V in the same bias point:

$$P_0 = P_0^* = V_{D0} F_{DC}^*[V_{G0}, V_{D0}] \tag{3.7}$$

In this condition the term $\theta_0 - \theta_S^*(t)$ of (3.3) can be rewritten using (3.4) and (3.5) as:

$$\begin{aligned} \theta_0 - \theta_S^*(t) =& \theta_B + R_\theta[P_0, \theta_B]P_0 - \theta_B^* - R_\theta[p_S^*(t), \theta_B^*]p_S^*(t) \\ =& \theta_B^* + R_\theta[P_0^*, \theta_B^*]P_0^* - \theta_B^* - R_\theta[p_S^*(t), \theta_B^*]p_S^*(t) \\ =& R_\theta[P_0^*, \theta_B^*]P_0^* - R_\theta[p_S^*(t), \theta_B^*]p_S^*(t) \end{aligned} \tag{3.8}$$

$p_S^*(t)$, the power that would be dissipated instant by instant under stationary operation in the presence of $V_G = v_G(t)$, $V_D = v_D(t)$, can be further decomposed

in a time independent and in a time dependent term:

$$p_S^*(t) = P_0^* + p_{Sa}^*(t) \tag{3.9}$$

Continuing from equation (3.8) and using (3.9) and the definition of R_θ (3.1) we can write

$$\begin{aligned}\theta_0 - \theta_S^*(t) = \\ &= (R_{\theta 0} + R_{\theta P} P_0^*) P_0^* - [R_{\theta 0} + R_{\theta P}(P_0^* + p_{Sa}^*(t))](P_0^* + p_{Sa}^*(t)) \\ &= -R_{\theta 0} p_{Sa}^*(t) - 2R_{\theta P} P_0^* p_{Sa}^*(t) - R_{\theta P}(p_{Sa}^*(t))^2 \end{aligned} \tag{3.10}$$

In the small signal condition considered here, the quantity $(p_{Sa}^*(t))^2$ is infinitesimal and the last term of (3.10) can be neglected leading to:

$$\begin{aligned}\theta_0 - \theta_S^*(t) &= -(R_{\theta 0} p_{Sa}^*(t) + 2R_{\theta P} P_0^* p_{Sa}^*(t)) \\ &= (R_{\theta 0} + 2R_{\theta P} P_0^*)(P_0^* - p_S^*(t)) \end{aligned} \tag{3.11}$$

Consequently, in this case, the last term of the equivalent gate voltage deviation (3.3) becomes

$$\alpha_\theta[v_G](R_{\theta 0} + 2R_{\theta P} P_0^*)(P_0^* - p_S^*(t)) \tag{3.12}$$

The model function $\alpha_\theta[v_G]$ can be expanded in series around the bias gate voltage V_{G0}:

$$\alpha_\theta[v_G] = \alpha_\theta[V_{G0}] + \left.\frac{d\alpha_\theta}{dv_G}\right|_{V_{G0}} (v_G - V_{G0}) + \left.\frac{d^2\alpha_\theta}{d^2 v_G}\right|_{V_{G0}} (v_G - V_{G0})^2 + \cdots \tag{3.13}$$

and in substituting (3.13) into (3.12) all terms apart the first one can be neglected being infinitesimal quantities that multiply the infinitesimal quantity $(P_0^* - p_S^*(t))$.

Eventually the gate voltage deviation (3.3) can be rewritten as:

$$\begin{aligned}\Delta v_G = &\alpha_G(v_G(t) - V_{G0}) + \\ &\alpha_D(v_D(t) - V_{D0}) + \\ &\alpha_P[V_{G0}, P_0^*](P_0^* - p_S^*(t)) \end{aligned} \tag{3.14}$$

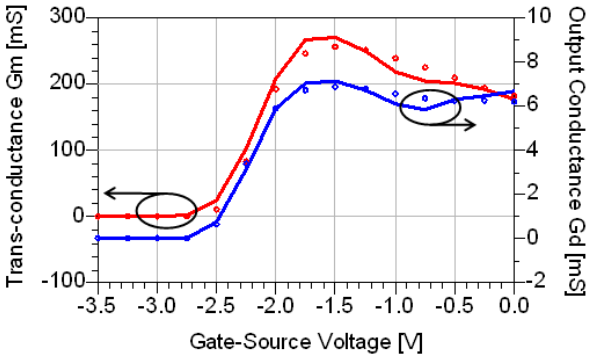


Figure 3.3: GaN HEMT ($L = 0.25\,\mu\text{m}$, $W = 600\,\mu\text{m}$): measurements (circles) and predictions (line) of the intrinsic trans- and output conductance versus V_{G0} at $V_{D0} = 14\,\text{V}$ and 250 MHz.

where

$$\alpha_P[V_{G0}, P_0^*] = \alpha_\theta[V_{G0}](R_{\theta 0} + 2R_{\theta P}P_0^*) \tag{3.15}$$

By assuming for $\alpha_\theta[V_{G0}]$ a linear approximation versus V_{G0} of the form

$$\alpha_\theta[V_{G0}] = \alpha_{\theta 0} + \alpha_{\theta 1}V_{G0} \tag{3.16}$$

equation (3.15) can be expressed as

$$\begin{aligned}\alpha_P[V_{G0}, P_0^*] &= (\alpha_{\theta 0}R_{\theta 0}) + (2\alpha_{\theta 0}R_{\theta P})P_0^* + (\alpha_{\theta 1}R_{\theta 0})V_{G0} + (2\alpha_{\theta 1}R_{\theta P})P_0^*V_{G0} \\ &= \alpha_{P0} + \alpha_{P1}P_0^* + \alpha_{P2}V_{G0} + \alpha_{P3}P_0^*V_{G0}\end{aligned} \tag{3.17}$$

where α_{P0}, α_{P1}, α_{P2} and α_{P3} are four coefficients to be identified in addition to α_G and α_D. These are determined by fitting the measured trans-conductance and output conductance in a bias range within the saturation region of the transistor ($10\,\text{V} < V_{D0} < 18\,\text{V}$, $I_{DSS}/8 < I_{D0} < I_{DSS}$) with the model defined by (3.2), (3.14) and (3.17). The good approximation obtained for the multi-bias intrinsic trans- and output conductances is shown in Fig. 3.3.

The second step of the procedure consists in changing the base plate temperature to a different value (we used $\theta_B = 90\,°\text{C}$ in our experiment) and measuring the static I/V characteristic $F_{DC}[V_{G0}, V_{D0}]$ in this new thermal condition. The difference between this static DC characteristic and the reference $F_{DC}^*[\,]$ is point

by point only due to a different thermal state. Being the purely-alternate voltage components equal to zero, under DC operation at $\theta_B \neq \theta_B^*$ to reproduce the new characteristic from the reference one, the gate voltage deviation (3.3) reduces to:

$$\Delta V_G = \alpha_\theta[V_{G0}]\big(\theta_0 - \theta_S^*(t)\big) \tag{3.18}$$

by substituting the definition of θ_0 (3.4), $\theta_S^*(t)$ (3.5) and then of R_θ (3.1) and by noting that in static conditions $\theta_S^*(t) = P_0^* = V_{D0}F_{DC}^*[V_{G0}, V_{D0}]$ (3.9) we obtain:

$$\begin{aligned}\Delta V_G = \alpha_\theta[V_{G0}] \Big[&\Big(\theta_B + \big(R_{\theta 0} + R_{\theta P}P_0 + R_{\theta B}(\theta_B - \theta_B^*)\big)P_0\Big) \\ &- \Big(\theta_B^* + \big(R_{\theta 0} + R_{\theta P}P_0^*\big)P_0^*\Big)\Big] \\ = \alpha_\theta[V_{G0}](1 + R_{\theta B}P_0)(\theta_B - \theta_B^*) \\ &+ \alpha_\theta[V_{G0}]\big(R_{\theta 0} + R_{\theta P}(P_0 + P_0^*)\big)(P_0 - P_0^*)\end{aligned} \tag{3.19}$$

where $P_0 = V_{D0}F_{DC}[V_{G0}, V_{D0}]$. By defining now $\Delta P = P_0^* - P_0$ which is the dissipated power variation due to the change of the base plate temperature, the second term of (3.19) can be written as:

$$\alpha_\theta[V_{G0}]\big(R_{\theta 0} + 2R_{\theta P}P_0^* + R_{\theta P}\Delta P\big)\Delta P \tag{3.20}$$

where we can neglect the second order infinitesimal term ΔP^2.

The gate voltage variation (3.18) can thus be written as:

$$\begin{aligned}\Delta V_G = &\alpha_\theta[V_{G0}](1 + R_{\theta B}P_0)(\theta_B - \theta_B^*) \\ &+ \alpha_P[V_{G0}, P_0^*](P_0 - P_0^*)\end{aligned} \tag{3.21}$$

where the function $\alpha_P[V_{G0}, P_0^*]$ is still defined as in (3.15) and must coincide with it since, in spite of the different operative regimes considered, it describes the same self-heating phenomenon. Since $\alpha_P[\,]$ has been already determined during the first step, the second term in (3.21) is completely known at each choice of V_{G0}, V_{D0}. Thus (3.21) can be effectively used in order to distinguish the effects due to the base plate temperature change from self-heating on the corresponding total change in the internal channel temperature. In particular, we consider a set of biases sharing a single value of the gate voltage V_{G0} giving a wide open channel operation (for instance operation at about I_{DSS}) and different drain voltages V_{D0}

$R_{\theta 0}$ ($^\circ$C W^{-1})	$R_{\theta P}$ ($^\circ$C W^{-2})	$R_{\theta B}$ (W^{-1})
14.3	1.10	0.12

Table 3.1: GaN HEMT ($L = 0.25\,\mu$m, $W = 600\,\mu$m): extracted thermal coefficients.

(corresponding to different dissipated powers P_0 and P_0^*). Fitting the static current $F_{DC}[V_{G0}, V_{D0}]$ on this set of bias conditions easily lead to the determination of the $\alpha_\theta[V_{G0}]$ value and of the thermal resistance sensitivity $R_{\theta B}$ to base plate temperature variations.

Finally, by taking (3.15) and (3.17) into account we obtain an estimation of the remaining coefficients defining the nonlinear thermal resistance in (3.1), namely $R_{\theta 0}$ and the sensitivity $R_{\theta P}$ to dissipated power variations:

$$R_{\theta 0} = \frac{\alpha_{P0} + \alpha_{P2} V_{G0}}{\alpha_\theta[V_{G0}]} \tag{3.22}$$

$$R_{\theta P} = \frac{\alpha_{P1} + \alpha_{P3} V_{G0}}{2\alpha_\theta[V_{G0}]} \tag{3.23}$$

In order to obtain maximally consistent parameters, the DC current fitting can be possibly repeated at different values of V_{G0} and the $R_{\theta 0}$, $R_{\theta B}$, $R_{\theta P}$ coefficients chosen after solving an over-determined set of equations. Extracted values are reported in Table 3.1.

The corresponding thermal resistance versus dissipated power is also plotted in Fig. 3.4, for different base plate temperatures.

3.4 Validation

As a validation example, the analytical method proposed in [5–7] for the extraction of a constant thermal resistance has been applied to the case of the GaN HEMT under investigation. Thermal resistance predictions according to [5] versus typical values of the thermal conductivity of the SiC substrate (which is a temperature dependent quantity) are shown in Fig. 3.5. These values are substantially in agreement with those obtained with the coefficients in Table 3.1 for typical powers

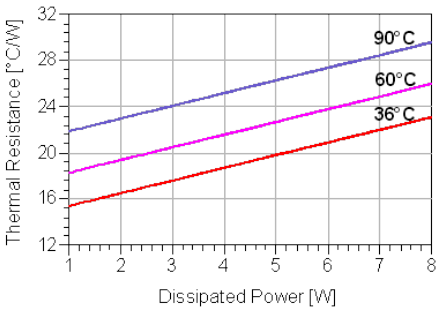


Figure 3.4: GaN HEMT ($L = 0.25\,\mu m$, $W = 600\,\mu m$): thermal resistance $R_\theta[P, \theta_B]$ versus dissipated power P at three different base plate temperatures θ_B.

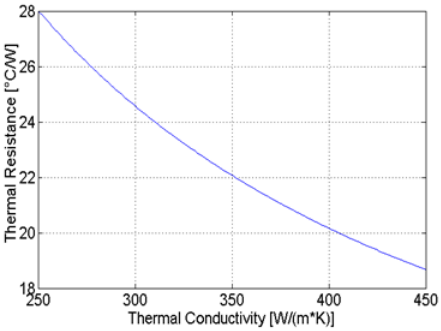
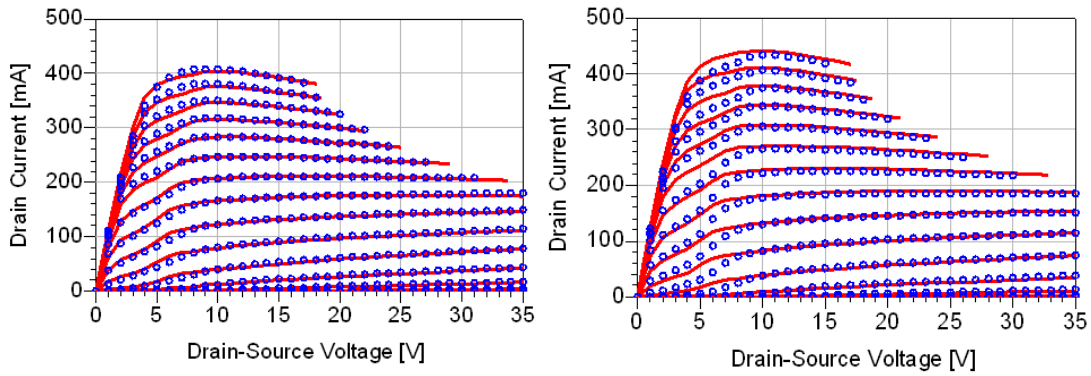


Figure 3.5: Thermal resistance simulated through the analytical method proposed in [5].

and base plate temperatures.

As far as the two thermal resistance sensitivities $R_{\theta B}$, $R_{\theta P}$ are concerned, these also seem in a reasonable agreement with literature data. For instance, data reported in [8] for thermal resistance sensitivities of GaN HEMTs over SiC substrates are comparable with those reported in Table 3.1. In fact, evaluation from graphics shown in [8], after appropriate scaling of the device periphery, leads to about $0.8\,°\mathrm{C\,W^{-2}}$ for $R_{\theta P}$ and $0.08\,\mathrm{W^{-1}}$ for $R_{\theta B}$.

In order to complete the electrothermal model identification, the $\alpha_\theta[\,]$ function has to be identified over the whole set of gate voltages. To this aim, after the determination of the thermal resistance, further fitting of the static I/V characteristic $F_{DC}[V_{G0}, V_{D0}]$ at $\theta_B \neq \theta_B^*$ in the saturation region through (3.21), leads to the complete identification of the $\alpha_\theta[\,]$ function. Prediction of the static I/V characteristic at 60 °C (along with the static I/V at 90 °C used for identification) is shown in Fig. 3.6, confirming the accuracy of the thermal resistance extraction.



(a) (b)

Figure 3.6: GaN HEMT ($L = 0.25\,\mu\mathrm{m}$, $W = 600\,\mu\mathrm{m}$): predicted static I/V characteristic (red lines) compared with measurements (circles) at two base plate temperatures: 90 °C (used for the thermal resistance identification - a) and 60 °C (b); $-3.5\,\mathrm{V} < V_G < 0.5\,\mathrm{V}$ (step 0.25 V).

An interesting possibility offered by the proposed electro-thermal model is to provide a simple way to simulate isothermal static characteristics, possibly useful in other device modelling approaches (e.g. [9]). This can be easily carried out by simulating the DC characteristics with the model (3.2)-(3.3), where the channel temperature θ_0 is held constant. For instance, the iso-thermal I/V characteristic at

$\theta_0 = 136\,°C$ (corresponding to $\theta_B = \theta_B^* = 36\,°C$ and the self-heating at $V_{D0} = 30\,V$ and $I_D = I_{DSS}/2$) is shown in Fig. 3.7.

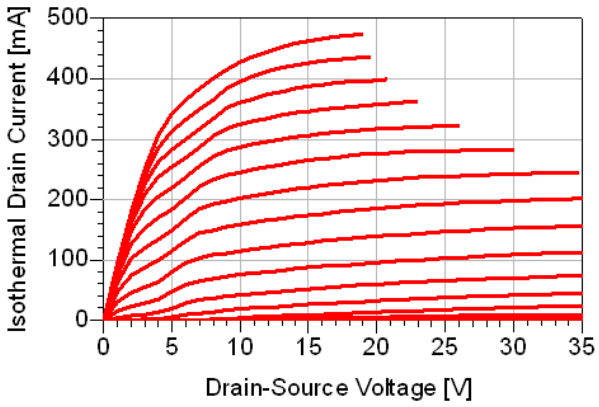
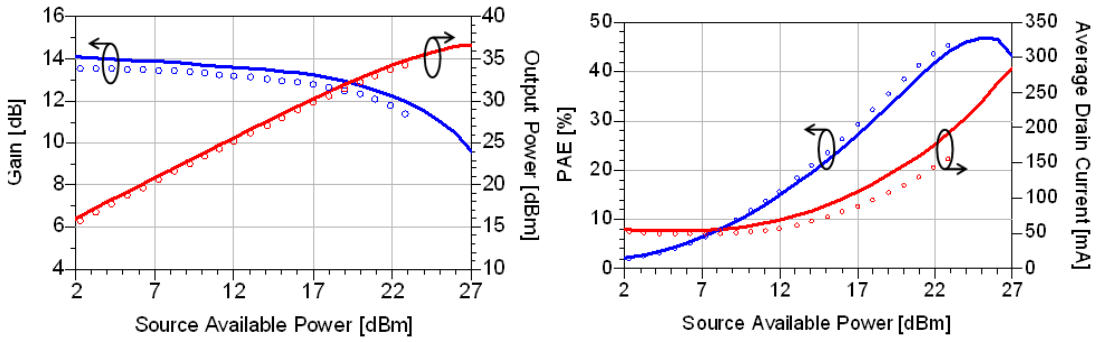


Figure 3.7: GaN HEMT ($L = 0.25\,\mu m$, $W = 600\,\mu m$): isothermal static I/V characteristic provided by the proposed model at channel temperature $\theta_0 = 136\,°C$ ($\theta_B = \theta_B^* = 36\,°C$ and dissipated power about 5 W); $-3.5\,V < V_G < 0.5\,V$ (step 0.25 V).

Experimental large signal validation of the whole electrothermal modelling approach is provided in Fig. 3.8, where the main device performance under class-AB, X-band (10 GHz) operation is shown. To this aim, a purely quasi-static model of the displacement current components [9] has been added in parallel to the circuit schematic shown in Fig. 3.1. The measurements on the GaN HEMT are carried out with a load-pull setup with source and load impedances for maximum output power.

3.5 Conclusions

In this Chapter, a non-invasive method for compact electrothermal modeling and nonlinear thermal resistance extraction of AlGaN/GaN FETs has been proposed. The method involves only multi-bias small-signal S-parameter and DC I/V measurements at different base plate temperatures and it does neither require special-purpose device geometries/structures nor measurements in the conduction region of the gate junction. The extracted values compare well with measured electrothermal data and analogous parameters obtained with other methods taken from the literature. Large-signal validation in X-band has been also provided



(a) (b)

Figure 3.8: GaN HEMT ($L = 0.25\,\mu m$, $W = 600\,\mu m$): transducer gain, output power (a), PAE and average drain current (b), measured with load-pull setup (circles) and predicted by the electro-thermal model (lines) at 10 GHz. Power amplifier operation in class-AB ($I_D = I_{DSS}/6$, $V_{D0} = 35\,V$) with source and load impedances for maximum output power.

after embedding the proposed thermal resistance description into an RF nonlinear device model.

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Chapter 4

A new pulsed characterization setup

4.1 Introduction

Many approaches have been presented in the scientific literature dealing with compact models of FETs based on pulsed drain current versus voltage (pulsed IV) characteristics (e.g. [1–5]). This kind of curves is obtained through low-duty-cycle narrow-width pulsed periodic gate and drain excitations, so that every measured IV curve sample ideally corresponds to a fixed channel temperature operation and to a frozen-like state of trapped charges (e.g. [6–14]). Although this kind of characterization seems to work well in association with GaAs technologies, some doubts have raised when considering GaN based transistors, due to specific properties of charge trapping dynamics in GaN on SiC devices [15, 16]. Due to this reason, some nonlinear models have been proposed, which avoid the use of pulsed I/V curves but nevertheless take into account dispersive phenomena (e.g.: [17]). Low-frequency source/load-pull methods represent another viable alternative [18]. However, pulsed characterization is undoubtedly suited for I/V curve tracing also due to its dynamic isothermal nature. For this reason, it is worth to further investigate how and if the associated limitations can be overcome.

In order to obtain a iso-dynamic IV device characteristic it is important to use pulses that are shorter than the time constants associated with dispersive phenomena. Conventional setups [6–9] which essentially are based on pulsed voltage generators with an ideally zero output impedance are limited to a pulse length

of about 200 ns. To overcome these limitations here is proposed and described in detail a new pulsed characterization setup that relies on 50 Ω pulser and a digital storage oscilloscope (DSO). Furthermore, it is possible to fully calibrate the setup in order to obtain devices characteristic directly at the DUT ports. Another advantage is the possibility to obtain the complete time domain waveform of the pulsed voltages and currents while with commercial systems only the final output IV characteristic is obtained. This hides many details that could be relevant and important for the understanding of long term memory phenomena. This setup, first introduced in [19], is specifically dedicated to the characterization of dispersive phenomena related to thermal and charge trappings in III-V compound semiconductor FETs, but it can be more generally used also in different contexts (e.g. other semiconductors testing). Specific requirements for the pulsed periodic excitation are reviewed and the impact on pulsed IVs are discussed also in relation to the specific hardware solutions adopted. In addition, some interesting differences between GaAs and GaN technologies are explored and highlighted with experimental data. Critical issues in performing pulsed characterization of GaN based-devices are discussed.

This Chapter is organized as follows. In Section 4.2 the new pulsed measurement system is described and then in Section 4.3 main advantages of the hardware configuration are highlighted. More details on measurement data post-processing are given in Section 4.4 while the calibration error model and procedure is described in Section 4.5 where also some validation measurements are presented. The setup is then used for the on-wafer characterization of a GaAs pHEMT. Experimental results are presented in Section 4.6, where pulsed IV slopes are compared to measurements taken with standard VNA. Pulsed IV characteristics are also used for the implementation of a simple nonlinear model of the GaAs device. Large-signal high-frequency experimental validation at 2.5 GHz is also presented in this Section. In the last Section 4.7, a GaN on SiC FET is characterized on-wafer and experimental results are presented. Critical differences are highlighted with respect to GaAs devices in relation to charge trapping effects.

4.2 Setup description

The measurement system is schematically presented in Fig. 4.1. Its components consist of standard instrumentation, usually available in most laboratories oriented to the characterization of circuit/devices for low-frequency applications. In particular, periodic pulsed waveforms having 20 V peak to peak maximum amplitudes on 50 Ω loads and programmable rise/fall times from 2.5 ns upwards are obtained through a two-channel arbitrary function generator (AFG). Additional power amplification can be added in the case of need for higher pulse amplitudes and currents on the drain side. For instance, this could be the case when dealing with large periphery GaN devices. A 10 kHz to 250 MHz, 25 W power amplifier has been used for the measurements on GaN devices presented in Section 4.7. The internal impedance of the two AFG channels is set to 50 Ω. The generator outputs are connected through 50 Ω cables to wide-band matched dual directional couplers (10 kHz to 1000 MHz), while two bias-tee (max. current: 400 mA, bandwidth: 200 kHz to 12 GHz) provide direct and alternate current path separation. The four output of the couplers feed the input of a suitably fast time-domain sampling system. A standard 8 bit oscilloscope can be effectively used (with some limitation in the sensitivity) or a more sophisticated data acquisition system based on higher-resolution A/D boards can be adopted. All the results presented are obtained through a standard four-channel 8 bit, 1.5 GHz bandwidth sampling oscilloscope,

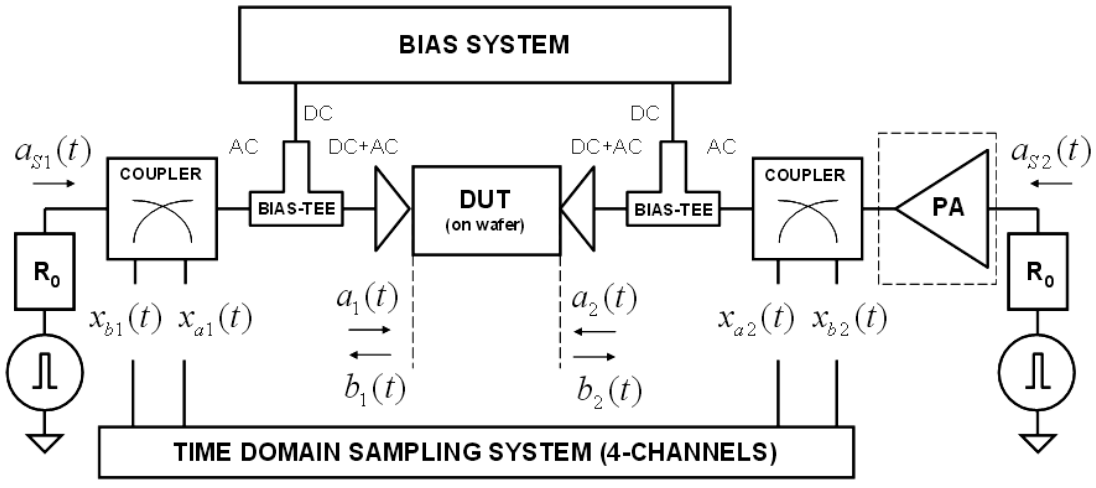


Figure 4.1: Schematic of the pulsed measurement setup.

Instrument	Model
Arbitrary Function Generator	Agilent 81150
Digital Storage Oscilloscope	Agilent 54845A
Bias System	HP 4142
Directional Couplers	Amplifier Research DC3010
Power Amplifier	Amplifier Research 25A250A
Bias Tees	AEROFLEX 8810
Bias Tees	Minicircuit ZFBT-6GW+
Thermal Chuck	Temptronic TP03215A

Table 4.1: Used components and instruments.

externally triggered by the TRIG OUT signal of the waveform generator. On wafer measurements have been carried out by means of a thermally- controlled probe-station with Ground-Signal-Ground access to the DUT electrodes. In Table 4.1 are summarized the used instruments.

The measurement system is fully automated through a remote controlling software, specifically developed in the MATLAB programming environment. The controlling interface allows the shaping of the periodic pulsed waveforms, the setting of the bias voltages, of the sweep parameters of the pulse amplitudes, the acquisition averaging and the base-plate temperature.

A SOLT-like on-wafer calibration technique has been specifically developed. This is based on the wideband characterization under sinusoidal excitation of the measurement setup after replacement of the actual DUT with a set of calibration standards, i.e. Short, Open, 50 Ω Load and a Thru. Absolute calibration of the pulse amplitudes is also taken into account. More detail on the calibration are given in Section 4.5. Let $x_{a1}(t)$, $x_{b1}(t)$, $x_{a2}(t)$ and $x_{b2}(t)$ be the time-domain waveforms sampled at the four channels of the oscilloscope. After the calibration corrections are applied, the four incident and reflected waveforms at the DUT ports (or equivalently the waveforms of the voltages and currents) are completely known. Subsequently, in the post-processing phase, the pulsed I/V characteristic can be extracted from the amplitude of the reconstructed time domain voltage and current waveforms.

It is worth noting that the working principle of the pulsed setup presented here is very similar to the one used in other measurement systems for the linear and non-linear characterization of electron devices (i.e. VNAs, high-frequency [20] and

low-frequency load-pull [18], LSNAs and NVNAs [21]). However, this is to our knowledge the first system for pulsed I/V device characterization fully based on measurements in the wave-variable domain with a full calibration procedure.

4.3 Advantages of the new setup

The main feature of the proposed measurement system consists in generating pulses in a 50 Ω environment. Equivalently, the DUT can be thought as excited by incident pulsed waves $a_1(t)$, $a_2(t)$ instead of pulsed voltages. Generation of pulses in a 50 Ω environment offers great and fundamental advantages.

First, resistive terminations seen by the DUT usually guarantee its stability. Most of conventional setups, which use voltage instead of wave pulses, may in some case force the user to introduce extra resistive components for maintaining stability [13]. This is not necessary in the actual setup since the bias networks used and the two-channel pulse generator provide wide-band 50 Ω terminations from the very low frequency of 100 kHz up to some hundreds of megahertz (in the bandwidth of the AFG, see Fig. 4.2). At higher frequencies, although not perfectly 50 Ω, the terminations provided by the setup are dissipative (in the order of 200 Ω max.) up to several gigahertz minimizing the likelihood of instabilities. In any case better 50 Ω terminations can be obtained by using attenuators along the input and output paths. In the author experience this has never been needed.

Secondly, reflections due to mismatches of cables and setup components are

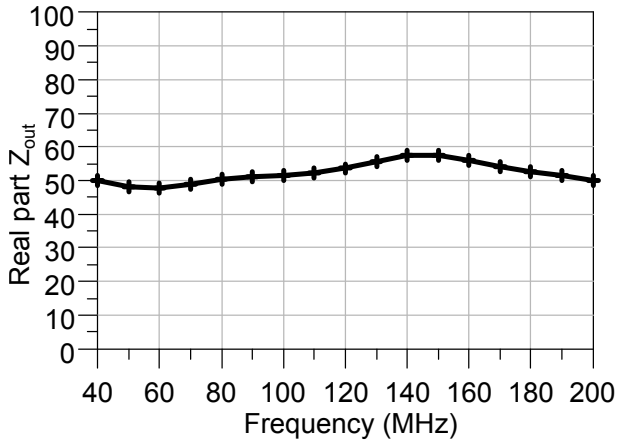


Figure 4.2: Real part of measured output impedance of the Agilent 81150 AFG.

reduced to a minimum. This leads to:

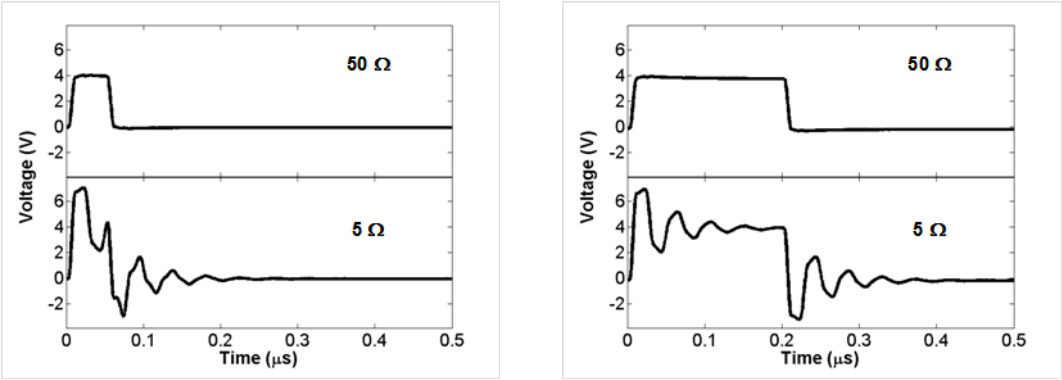
1. ability to operate with pulse widths down to 50 ns (compared to typical 200 ns of other pulsed systems [6–8]);

2. simplified on-wafer calibration procedures, since the incident wave pulses are almost undistorted and calibration mostly involve attenuation corrections and phase shifts due to the setup components;

3. more freedom in the choice of cable lengths, since they are 50 Ω.

A simple experiment demonstrating this advantage was executed. The input port of the DUT (almost equivalent to an open circuit up to frequencies of some hundreds of megahertz) was replaced with the high-impedance input port of an oscilloscope. The voltage waveform measured at the instrument input (this reading being proportional to the incident wave at the input of the DUT) is shown in Fig. 4.3 for two different internal impedances of the pulse generator: 5 Ω (similar to a voltage pulse excitation) and 50 Ω (actual wave-pulse excitation). As it can be seen, the 50 Ω case corresponds to the expected almost ideal case, while undesired strong oscillations originate in the 5 Ω case due to the presence of mismatches along the pulse travelling path. It is worth noting that standard voltage pulse measurement systems apply pulses through the DC path of the bias network, thus adopting quite a different electrical scheme. However, analogously to what happens in our experiment, the voltage pulse travels through a 50 Ω matched cable and a 50 Ω probe tip before reaching the DUT and for this reason mismatches across the pulse travelling path are necessarily involved.

A third important characteristic of the proposed measurement setup consists in direct and alternate current path separation through bias networks. The pulsed excitation (50 Ω internal impedance) feeds the AC port, while the bias system feeds the DC port exactly as in standard power amplifier circuit schematics. Special attention must be paid to the bias network frequency response in relation to the choice of pulse width and duty cycle adopted, so as to avoid excitation distortion. Wide-band bias tees (200 kHz to 12 GHz) have been chosen in the proposed setup. A more common solution consists of using bias networks with relatively high cut-off frequency of the DC path (in the order of hundreds of megahertz) and in injecting both bias and pulse waveforms into the DC port (provided that the whole spectrum of the pulses lays below the cut-off frequency of the low-pass DC



(a) (b)

Figure 4.3: Instrument voltage reading proportional to the input incident wave when the DUT input is replaced by an open circuit (similar to the gate input of a FET). Pulse generator internal impedance set to 50 Ω and 5 Ω. Pulse width: 50 ns (a) and 200 ns (b).

feed inductor). Moreover, the AC port of the bias-tees is usually closed on 50 Ω terminations for limiting risks of device instability at high frequency, e.g.: [6–8] (risks still exist however at lower frequencies through the DC path and the voltage pulse generation circuitry).

In order to highlight other advantages of the proposed setup it is worthwhile to analyse the repetitive pulse waveform. Let $V(t) = V_0 + v(t)$ be the voltage at the generic device port, where V_0 is the average value and $v(t)$ is the purely-ac voltage component. By assuming $\delta = \tau/T$ (τ : pulse width, T : time period) as the duty cycle, an ideal repetitive pulse voltage waveform $v(t)$ (with positive amplitude A) at the device terminals looks like in Fig. 4.4, with $V_{base} = -\delta A$ and $\hat{V} = (1-\delta)A$. In addition, by expanding the pulsed waveform $v(t)$ in Fourier series, we obtain:

$$v(t) = \sum_{\substack{n=-\infty \\ n\neq 0}}^{+\infty} A_n \cos\left(\frac{n2\pi t}{T}\right) \tag{4.1}$$

with

$$A_n = \delta A \frac{\sin(\pi n\delta)}{\pi n\delta} = \delta A \,\mathrm{sinc}(n\delta) \tag{4.2}$$

or equivalently

$$A_n = \delta A \frac{\sin(\pi \tau f_n)}{\pi \tau f_n} = \delta A \,\mathrm{sinc}(\tau f_n) \tag{4.3}$$

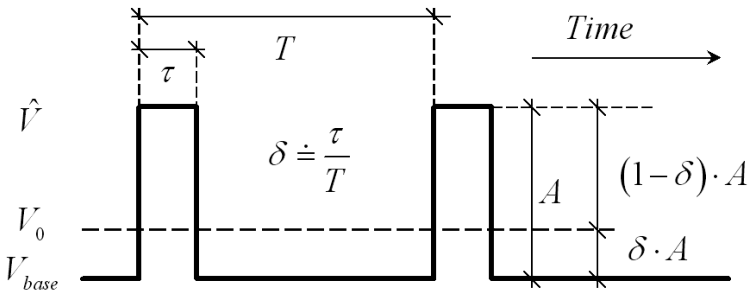


Figure 4.4: Due to the DC and AC current path separation provided by the bias networks, the bias system fixes the average value of the pulse. Positive pulse case is shown in the figure.

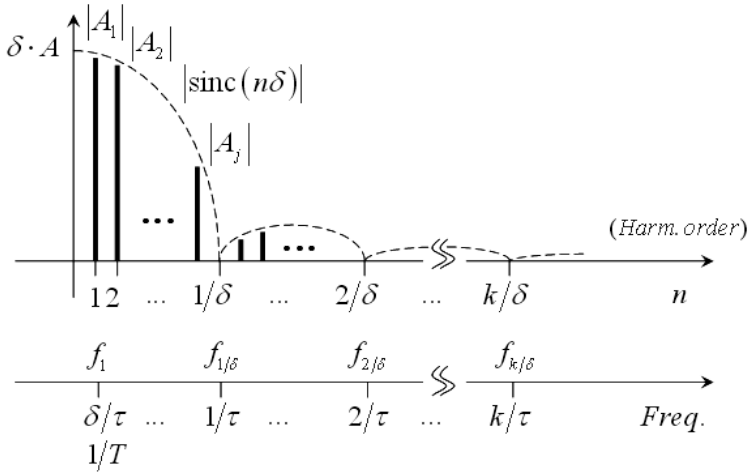


Figure 4.5: Discrete amplitude spectrum of the pulsed waveform (plotted here for $n \geq 1$ only).

The corresponding amplitude spectrum is shown in Fig. 4.5.

Direct and alternate current path separation through bias networks, as in the present setup, leads to a couple of other important advantages.

First, the bias system sets and maintains the average voltage value V_0 at the gate and drain terminals (strictly corresponding to the selected bias) independently of the duty cycle adopted during the repetitive wave pulse excitation and regardless of the pulse amplitudes. This issue is interesting when dealing with the purpose of characterizing the dispersion due to charge trappings in FETs. In fact, provided that all the spectral components A_n of the repetitive pulse excitation waveform

lay at frequencies above the upper cut-off of dispersive phenomena (i.e. $f_t > f_{cutoff}$),the current deviation due to charge trapping between static and pulsed I/V curves can be considered (for a wide range of devices such as GaAs HEMTs) as a function of the average gate and drain voltages only, as a first order of approximation [22]. The charge trapping state is thus well defined through the proposed pulsed setup. Instead, when considering pulsed systems where DC and AC components of voltages and currents share the same electrical path, the quiescent (baseline) voltage value V_{base} is not coincident with the average voltage V_0 since: $V_0 = V_{base} + \delta A$. In this case, it is clear that the duty cycle has to be chosen small enough to guarantee that the baseline voltage practically coincides with the average value. This has to be carefully considered especially when dealing with the characterization of wide-bandgap devices (such as GaN-based transistor), which operate at very large drain-source signal amplitudes. With this respect, the choice of duty cycle could be slightly relaxed in the actual case and the pulse spectrum first harmonic component A_1 at $f_t = 1/T = \delta/\tau$ could be more easily shifted towards and above the dispersion frequency cut-off (the pulse width τ is usually chosen as the minimum value allowed by the instrumentation setup). However, it is worth noting that excessively high duty cycle should be avoided in any case. In fact, this might result in: 1) variations of the thermal state during the pulsed characterization, which is related to the rms value of the voltage waveforms ($V_{rms}^2 = \delta(1-\delta)A^2$); 2) spurious variations of the dynamic drain current due to a second-order dependency of the trap state on the rms values of the applied voltages (mainly observed in GaN transistors [15]). Duty cycles in the order of a few percent are usually adopted.

A second advantage of having AC and DC current paths separation consists in the ability of monitoring the average drain current during the pulsed characterization. This leads to a better understanding of the dispersion mechanisms. In fact, the average drain current observed under above-cut-off repetitive pulse voltage excitations can be expressed as [15]:

$$I_{D0} = F\{V_{G0}, V_{D0}, \tilde{X}, \vartheta_0\} \tag{4.4}$$

where V_{G0} and V_{D0} are the average gate and drain voltages, $\tilde{X}$ is a vector of variables denoting a particular (frozen) state of charged traps and ϑ_0 is the channel temperature corresponding to the power dissipated at the average voltage

conditions and at a default baseplate temperature (36 °C in our experiments). The frozen state of traps $\tilde{X}$ has been often considered a function of the average gate and drain voltages only and this assumption is verified later in this work in the experimental validation Section 4.6 dedicated to GaAs transistor characterization. In fact, it will be shown that the average current under pulsed operation remains constant at the quiescent value for different gate and drain pulse amplitudes, as expected. Things change instead when considering GaN transistors. Some Authors, e.g.: [15, 16] suggest that the $\tilde{X}$ variables might be also dependent on other quantities (such as rms values of voltages under an almost sinusoidal regime [15] or dependent on peak values of voltages [16]). This is confirmed in the following Section 4.7 dedicated to GaN transistors.

4.4 Post-processing of measured data

During the measurement, for each combination of gate and drain pulse amplitudes, a whole period T of the four waveforms (x_{a1}, x_{b1}, x_{a2}, x_{b2}) is acquired with the scope. The mean voltages and currents (V_{G0}, V_{D0}, I_{G0}, I_{D0}) are measured with the bias system (e.g. HP 4142). The outputs of the pulsed measurement are therefore basically two:

- the waves measurement matrix $\underline{S}_P$ of dimension

$$4 \times N_G \times N_D \times N_p \tag{4.5}$$

  where N_G and N_D are the number of gate and drain amplitudes and

$$N_p = SrT \tag{4.6}$$

  is the number of points in time acquired at the sampling rate Sr.

- the DC measurement matrix $\underline{S}_{DC}$ of dimension

$$4 \times N_G \times N_D \tag{4.7}$$

To obtain the pulsed I/V characteristic $I_d = F_p\{V_{G0}, V_{D0}, V_G, V_D\}$ from these two matrices five basic post-processing steps are necessary:

1. Calibration correction, which leads to calibrated incident and reflected waves at the DUT ports;
2. Transformation from incident/reflected waves to voltage/currents;
3. Addition of DC voltages and currents;
4. Peak values extraction;
5. Interpolation (and optional extrapolation) of voltage/currents on a rectangular voltage domain at the DUT ports.

Post-processing of data is carried out off-line after the user-programmed acquisitions have been completed. However, real-time post-processing represents a feasible alternative. In the following Sections these steps are described in more detail.

4.4.1 Application of calibration correction

The calibration is performed in the frequency domain and its implementation will be addressed in Section 4.5. In order to apply the calibration to the measurements more steps are necessary:

1. Decimation of all time-domain measurements in $\underline{S}_P$ to reduce the maximum frequency of acquired data;
2. Transformation to the frequency domain by means of Fast Fourier Transform (FFT);
3. Application of calibration (see Section 4.5);
4. Transformation of corrected waves back to the time domain by means of Inverse FFT (IFFT);

Time domain waves are sampled with sampling rate S_r , in our setup this could be as high as 8 GS/s. The frequency resolution of the FFT or the spacing between frequency components is

$$\Delta_f = \frac{S_r}{N_{sampl}} \tag{4.8}$$

where N_{sampl} is the number of time domain sample to be processed. The spectrum of the periodic waveform has instead components at integer multiples of $1/T$. Therefore, for a correct application of the FFT the following relation has to be verified

$$\frac{S_r}{N_{sampl}} = \frac{1}{T} \tag{4.9}$$

or, in other words, the period should be an integer multiple of the sampling interval t_s:

$$N_{sampl} = S_r T = \frac{T}{t_s} \tag{4.10}$$

This is ensured by always setting the scope in order to acquire the right number of time-domain points at the selected sampling rate.

The highest frequency component in the FFT output is the Nyquist frequency $f_{Ny} = S_r/2$. The calibration instead is performed on a frequency grid up to a maximum frequency f^C_{max} that usually is lower:

$$f^C_{max} < f_{Ny} \tag{4.11}$$

It is thus necessary to decimate the time domain waveform in order to reduce the highest frequency from f_{Ny} to $f'_{Ny} = f^C_{max}$. This is done by first low-pass filtering the signal with a high order FIR filter and then by downsampling by a factor of

$$D = \frac{f_{Ny}}{f^C_{max}} \tag{4.12}$$

This effectively reduces the sampling rate and the number of points maintaining the correct Δ_f. The filter is needed to avoid aliasing and has the added benefit of reducing the noise on the signal. A maximum frequency for the calibration f^C_{max} of 100 MHz has been used for the measurements presented in the following Sections. This bandwidth is enough also for short pulses with fast rise and fall time. While the ideal periodic pulse repetition has in theory an infinite bandwidth and that the pulse width sets the nulling frequency $(1/\tau)$ of the first lobe of the spectrum, as a first approximation the relevant bandwidth of a real pulse can be estimated from its 10 % to 90 % rise or fall-time t_r [23, 24] with

$$BW_{puls} \approx \frac{0.5}{t_r} \tag{4.13}$$

For a bandwidth of 100 MHz the minimum rise time is thus approximately 5 ns.

The calibration correction is then performed for every complex harmonic component of the spectrum as explained in Section 4.5.

As the final step, the corrected waveforms in the frequency domain are transformed back to the time domain by means of an Inverse Fast Fourier Transform.

4.4.2 Transformation to voltages/currents

The transformation from incident/reflected waves to voltages/currents time domain waveforms at the DUT ports is then readily performed with

$$v(t) = \big(a(t) + b(t)\big)\sqrt{R_0} \tag{4.14}$$

$$i(t) = \frac{a(t) - b(t)}{\sqrt{R_0}} \tag{4.15}$$

where the following formalism for incident and reflected waves definition is adopted [25]:

$$a = \frac{1}{2\sqrt{|\Re\{Z_{ref}\}|}}(v + Z_{ref} i) \tag{4.16}$$

$$b = \frac{1}{2\sqrt{|\Re\{Z_{ref}\}|}}(v - Z^*_{ref} i) \tag{4.17}$$

Z_{ref} is the reference impedance associated with the formalism and in our case is chosen to be equal to the real input impedance of the sampling instrument, i.e. $Z_{ref} = R_0 = 50\,\Omega$. Follows:

$$a = \frac{1}{2\sqrt{R_0}}(v + R_0 i) \tag{4.18}$$

$$b = \frac{1}{2\sqrt{R_0}}(v - R_0 i) \tag{4.19}$$

The measured DC values from matrix $\underline{S}_{DC}$ are then added:

$$V(t) = V_0 + v(t) \tag{4.20}$$

$$I(t) = I_0 + i(t) \tag{4.21}$$

From the time-domain current and voltage pulsed waveforms at the DUT ports is then possible to extract the peak values to obtain the pulsed I/V characteristic. This can be done either automatically or manually selecting on a plot of all waveforms a suitable range inside the pulse width. This has the advantage to allow to visually inspect the quality of pulses and to avoid to select time ranges where some ringing could be present.

It has to be stressed here that at this point the entire period of the pulsed voltages and currents is available. This allows for instance to observe and study any long term transient response if present.

As already explained, thanks to the DC and AC path separation, it is also possible to work separately on the DC and AC characteristics. As will be shown in Section 4.7 in some circumstances this gives new insight into the effects of dispersive phenomena on the pulsed characteristic.

4.4.3 Interpolation

Ohmic voltage drops across 50 Ω resistors make the organization of acquired data slightly more complicated to deal with in comparison to the case where more conventional voltage pulses are applied. A rectangular bi-dimensional grid of waves applied at the generator ports turn out into a non-rectangular grid of voltages at the device ports due to the current-dependent voltage drops across 50 Ω resistors, as will be shown in Section 4.6. Suitable bi-dimensional post-processing of data is executed in order to achieve a full reconstruction of the dynamic drain current characteristics over a rectangular domain of voltages at the device ports. In particular, the measured data can be seen as samples of the two functions:

$$x_{b1} = F_1\left[x_{a1}, x_{a2}\right] \tag{4.22}$$

$$x_{b2} = F_2\left[x_{a1}, x_{a2}\right] \tag{4.23}$$

Bi-dimensional interpolation algorithms on non-rectangular grids available in

commercial mathematical processing tools [26] can be exploited to this aim. Alternatively, special purpose routines can be developed in order to avoid interpolation on non-rectangular grids.

4.5 Calibration

The time domain voltage and current pulsed waveforms at the DUT ports are obtained from the incident and reflected waves. These are not measured directly at the DUT ports but are sampled in the time domain by the oscilloscope at the coupled ports of the two dual directional couplers. A calibration procedure is thus necessary to reconstruct the waves, and consequently voltages and currents, at the reference plane. In general a calibration procedure is defined by an error model that describes how the wanted quantities are linked to the actual measurements (or that, in other words, describes systematic measurement errors) and by a procedure that describes a way to determine the coefficients of the error model [27]. This usually involves the measurement with the instrument to be calibrated of known (and sometimes unknown) standards. The calibration procedure presented here and implemented for the first time for a pulsed I/V measurement setup is based on calibrations employed in LSNA and NVNA systems [28–31].

The two dashed boxes, on the input and on the output, in Fig. 4.6 can be considered as two linear 4-port networks. These include the directional couplers but also bias tees, probes and 50 Ω connection cables.

Taking into consideration only the input box, ports 3 and 4 are closed on the oscilloscope 50 Ω input impedance and thus the reflected waves at these ports can be considered to be equal to zero

$$b_3 = 0$$
$$b_4 = 0$$

Port 2 represents the DUT reference plane where we want to determine the a_2 and b_2 incident and reflected waves. As a consequence of the limited directivity of the dual directional coupler and to the presence of the bias tee, that particularly at low frequency could present a not perfect match, a portion of the wave that

travels toward the DUT is reflected back and contribute to the wave measured at port 4. In a similar way, a portion of the wave that is reflected back from the DUT goes also to port 3 where in an ideal case we would like to sample only the incident wave.

We can thus write the waves at the DUT, a_2 and b_2, as a linear combination of both the measured waves a_3 and a_4[1]

$$b_2 = \hat{k}a_3 + \hat{p}a_4 \tag{4.24}$$

$$a_2 = \hat{q}a_3 + \hat{r}a_4 \tag{4.25}$$

This defines a linear error model for the input port with parameters $\hat{k}$, $\hat{p}$, $\hat{q}$ and $\hat{r}$. For a single frequency the waves are effectively sinusoidal and can be represented by a single complex phasor. The error model is thus defined by four complex parameters or equivalently by eight real quantities and puts into relation the sinusoidal waves, measured with the scope, with the incident and reflected sinusoidal waves at the DUT plane.

Redefining the waves names in relation to the DUT as shown in Fig. 4.7 and assuming that the input and output box are isolated we can write the complete

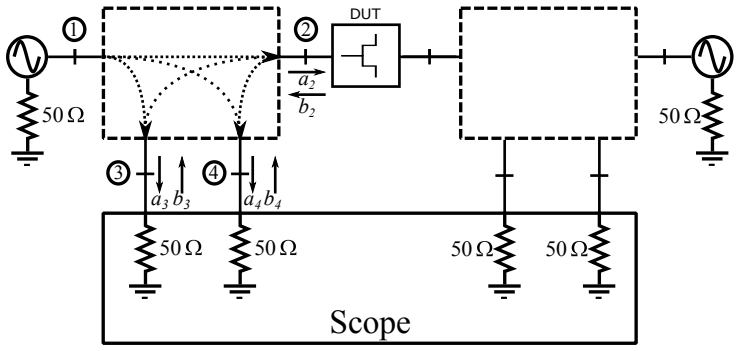


Figure 4.6: Schematic of the pulsed measurement setup.

[1]Note that the linear combination of sinusoidal waves of same frequency but different phases is still sinusoidal with the same frequency but different phase and amplitude.

error model

$$a_{D1} = \hat{k}a_{R1} + \hat{p}b_{R1} \tag{4.26}$$

$$b_{D1} = \hat{q}a_{R1} + \hat{r}b_{R1} \tag{4.27}$$

$$a_{D2} = \hat{s}a_{R2} + \hat{t}b_{R2} \tag{4.28}$$

$$b_{D2} = \hat{u}a_{R2} + \hat{v}b_{R2} \tag{4.29}$$

where the subscript D stand for DUT and R for Reading. 1 and 2 now refer respectively to the input and output part of the setup. In matrix form this can be written as

$$\begin{bmatrix} a_{D1} \\ b_{D1} \\ a_{D2} \\ b_{D2} \end{bmatrix} = M \begin{bmatrix} a_{R1} \\ b_{R1} \\ a_{R2} \\ b_{R2} \end{bmatrix} \tag{4.30}$$

where M is the complex calibration matrix

$$M = \begin{bmatrix} \hat{k} & \hat{p} & 0 & 0 \\ \hat{q} & \hat{r} & 0 & 0 \\ 0 & 0 & \hat{s} & \hat{t} \\ 0 & 0 & \hat{u} & \hat{v} \end{bmatrix} \tag{4.31}$$

The coupling factors of the couplers and attenuations and phase relations

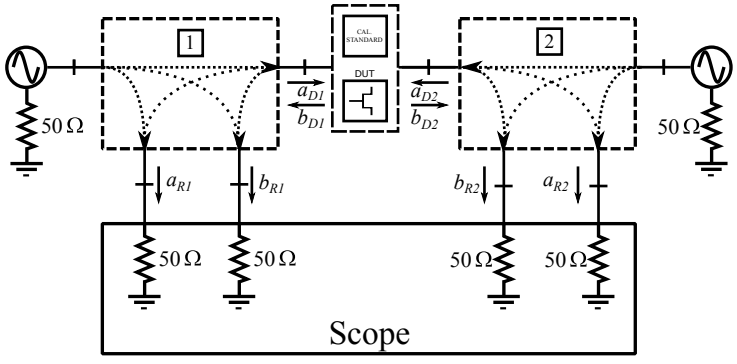


Figure 4.7: Schematic of the pulsed measurement setup.

between ports are not perfectly constant within the operational bandwidth and this has to be taken into account. Being the system linear the calibration can still be applied but it has to be performed for different frequencies. In our case of periodic pulsed waveforms that can be expanded in Fourier series (see Eq. (4.1)) the calibration is repeated for the harmonic frequencies from the fundamental ($f_0 = 1/T$) up to a maximum frequency f_{max}^C.

Being N the number of harmonics to be considered, the total number of real parameters to be determined with the calibration procedure is thus $8 \times N$. The calibration matrix M and its coefficients are therefore a function of frequency or of the harmonic index n, i.e. M^n, $\hat{k}^n$, $\hat{p}^n$, $\hat{q}^n$, $\hat{r}^n$, etc.. In the following this will be omitted for clarity of notation.

Normalizing now the calibration matrix M to its first element $\hat{k}$ it can be rewritten as

$$M = \hat{k}\overline{M} = \mathbf{k}e^{j\phi_k} \begin{bmatrix} 1 & p & 0 & 0 \\ q & r & 0 & 0 \\ 0 & 0 & s & t \\ 0 & 0 & u & v \end{bmatrix} \tag{4.32}$$

where $\hat{k}$ has been expanded in its phasor form and where $p = \frac{\hat{p}}{\hat{k}}$, $q = \frac{\hat{q}}{\hat{k}}$ and so on.

The calibration procedure can now be divided in two parts. In a first step a common Short, Open, Load and Thru (SOLT) calibration is used in order to determine the coefficients of the matrix $\overline{M}$. This is the same calibration that is performed with VNAs and allows to correct systematic errors in the measurement of the ratio of incident, reflected and transmitted waves at the DUT ports. To obtain also the correct amplitude and phase for all the four waves a second calibration step is necessary to determine also the complex coefficient $\hat{k}$.

4.5.1 Relative calibration

The SOLT calibration is based on the measurement of known standards. In our case of a low working frequency, standards can be considered as ideal but in a more general case an appropriate model could be used. The relation between incident and reflected waves at the DUT plane is thus defined by the standard that is being measured. For on-wafer measurements the calibration reference plane is defined at the probe tips and a calibration substrate must therefore be used. In

this work a Cascade Microtech Impedance Standard Substrate (ISS) 101-190 has been used.

From (4.30) and (4.32) follows

$$a_{D1} = \mathbf{k}e^{j\phi_k}[a_{R1} + pb_{R1}] \tag{4.33}$$

$$b_{D1} = \mathbf{k}e^{j\phi_k}[qa_{R1} + rb_{R1}] \tag{4.34}$$

$$a_{D2} = \mathbf{k}e^{j\phi_k}[sa_{R2} + tb_{R2}] \tag{4.35}$$

$$b_{D2} = \mathbf{k}e^{j\phi_k}[ua_{R2} + vb_{R2}] \tag{4.36}$$

For now we can consider only the input section of the setup in Fig. 4.7. A calibration standard is connected at the DUT port reference plane and the AFG is setted up to generate a sinusoidal signal at an appropriate frequency. The a_{R1}^X and b_{R1}^X waves are acquired by the scope, where the superscript indicates the standard.

For the Short we have $b_{D1} = -a_{D1}$ and from (4.33) follows

$$a_{R1}^S + qa_{R1}^S + rb_{R1}^S + qb_{R1}^S = 0 \tag{4.37}$$

For the Open $b_{D1} = a_{D1}$ and thus

$$(q-1)a_{R1}^O + (r-p)b_{R1}^O = 0 \tag{4.38}$$

For the Load $b_{D1} = 0$ leading to the equation

$$qa_{R1}^L + rb_{R1}^L = 0 \tag{4.39}$$

This gives a system of three equations that can be solved for the three unknown coefficients q, r and p. In matrix form:

$$\begin{bmatrix} a_{R1}^S & b_{R1}^S & b_{R1}^S \\ a_{R1}^O & b_{R1}^O & -b_{R1}^O \\ a_{R1}^L & b_{R1}^L & 0 \end{bmatrix} \times \begin{bmatrix} q \\ r \\ p \end{bmatrix} = \begin{bmatrix} -a_{R1}^S \\ a_{R1}^O \\ 0 \end{bmatrix} \tag{4.40}$$

In a similar way for the output section of the setup and for the Short, Open and Load standards it is possible to write the equations

$$ua^S_{R2} + vb^S_{R2} + sa^S_{R2} + tb^S_{R2} = 0 \tag{4.41}$$
$$ua^O_{R2} + vb^O_{R2} - sa^O_{R2} - tb^O_{R2} = 0 \tag{4.42}$$
$$ua^L_{R2} + vb^L_{R2} + sa^L_{R2} = 0 \tag{4.43}$$

In the case of the Thru standard the two ports at the DUT are directly connected an thus $a_{D2} = b_{D1}$. From (4.33) follows

$$sa^T_{R2} + tb^T_{R2} = qa^T_{R1} + rb^T_{R1} \tag{4.44}$$

In the second term of (4.44) q and r are already known from (4.40) and thus defining

$$K^T = qa^T_{R1} + rb^T_{R1} \tag{4.45}$$

it is possible to write the system of four equations to be solved for the four unknown coefficients u, v, s and t :

$$\begin{bmatrix} a^S_{R2} & b^S_{R2} & a^S_{R2} & b^S_{R2} \\ a^O_{R2} & b^O_{R2} & -a^O_{R2} & -b^O_{R2} \\ a^L_{R2} & b^L_{R2} & 0 & 0 \\ 0 & 0 & a^T_{R2} & b^T_{R2} \end{bmatrix} \times \begin{bmatrix} u \\ v \\ s \\ t \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ K^T \end{bmatrix} \tag{4.46}$$

At this point the matrix $\overline{M}$ in (4.32) is fully known. In order to know the full calibration matrix M another calibration step is necessary to determine also the coefficient $\hat{k}$.

4.5.2 Absolute calibration

Theoretically the determination of $\hat{k}$ can be performed in two equivalent ways. From (4.33) we can write

$$\hat{k} = \frac{a_{D1}}{a_{R1} + pb_{R1}} \tag{4.47}$$

or

$$\hat{k} = \frac{a_{D2}}{sa_{R2} + tb_{R2}} \tag{4.48}$$

Taking into consideration (4.47), the function generator is connected at the input of the section 1 in Fig. 4.7. In this case is needed the direct measurement of the a_{D1} wave at the DUT port and therefore the inputs of the oscilloscope are connected in order to sample at the same time the three waves. In general, for an on-wafer calibration, where the reference plane is at the probe tips, this poses a problem because it is not possible to directly connect the scope there. The more rigorous way to address this is to use the principle of reciprocity and an additional calibration step like the one presented in [30, 32]. In our case, due to the low working frequency, it has been verified that is otherwise possible to neglect the effects of probes without introducing relevant errors. It is thus possible to skip this last extra calibration step.

With the determination of $\hat{k}$ the whole calibration matrix M is known and is thus possible to obtain the four incident and reflected waves at the DUT ports from the four waves measured, at the same time, with the scope.

In Figures from 4.8 to 4.13 are shown the magnitude and phase of the eight complex coefficients of M plotted versus frequency for a typical calibration of the setup. The calibration has been performed on a frequency grid uniformly spaced from 100 kHz to 20 MHz in steps of 100 kHz and logarithmically spaced from 20 MHz up to 100 MHz.

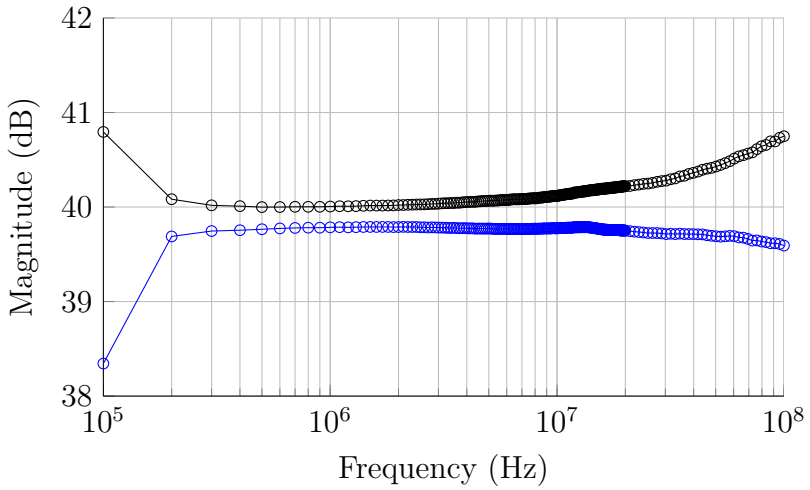


Figure 4.8: Magnitude of coefficients $\hat{k}$ (blue) and $\hat{r}$ (black) -Port 1- of calibration matrix M versus frequency for typical setup configuration.

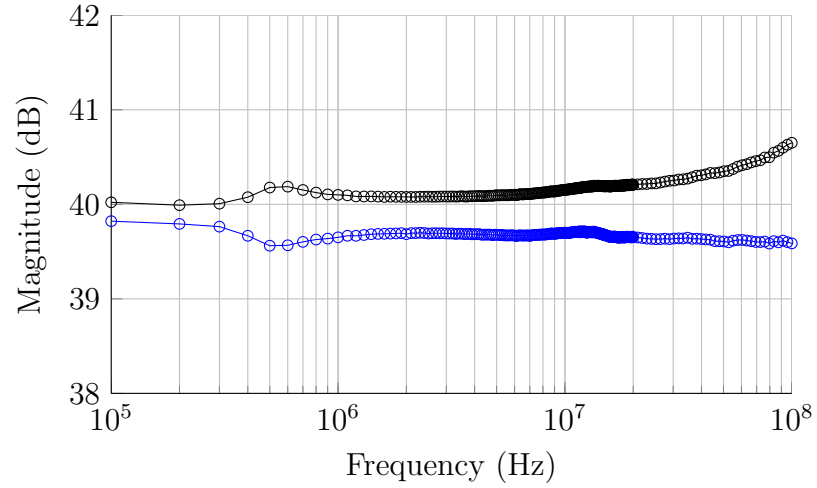


Figure 4.9: Magnitude of coefficients $\hat{s}$ (blue) and $\hat{v}$ (black) -Port 2- of calibration matrix M versus frequency for typical setup configuration.

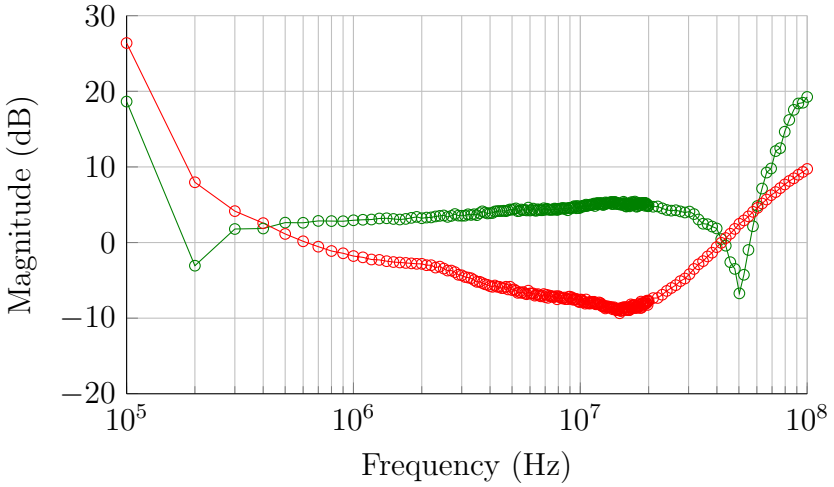


Figure 4.10: Magnitude of coefficients $\hat{p}$ (green) and $\hat{q}$ (red) -Port 1- of calibration matrix M versus frequency for typical setup configuration.

4.5.3 Practical considerations

It is important to point out that all the elements of the calibration matrix M are complex coefficients and each wave measured with the scope has to be described by a complex phasor.

At the oscilloscope port, from waves definitions (4.18)-(4.19) and being the

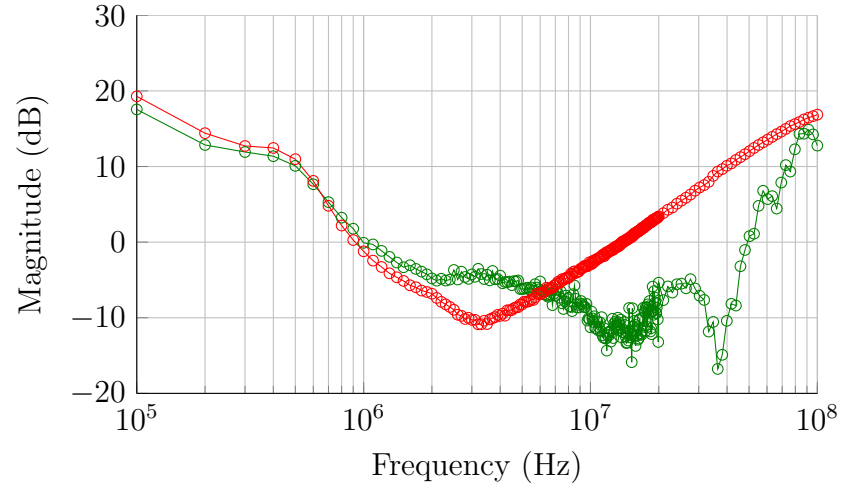


Figure 4.11: Magnitude of coefficients $\hat{t}$ (green) and $\hat{u}$ (red) -Port 2- of calibration matrix M versus frequency for typical setup configuration.

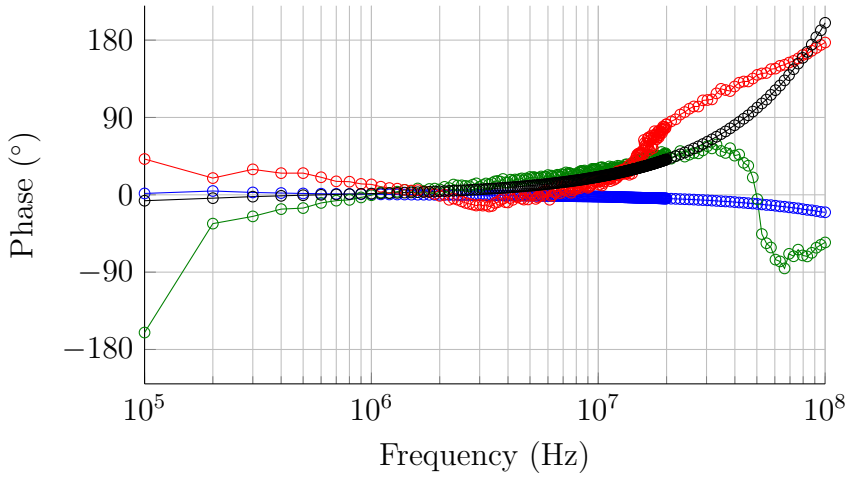


Figure 4.12: Phase of coefficients $\hat{k}$ (blue), $\hat{r}$ (black), $\hat{p}$ (green) and $\hat{q}$ (red) -Port 1- of calibration matrix M versus frequency for typical setup configuration.

reference impedance equal to $50\,\Omega$ as the input impedance follows

$$a = \frac{V}{\sqrt{R_0}} \tag{4.49}$$

$$b = 0 \tag{4.50}$$

For every wave to be measured during the calibration the module is thus determined by a measurement, directly on the scope, of the peak-to-peak amplitude of the

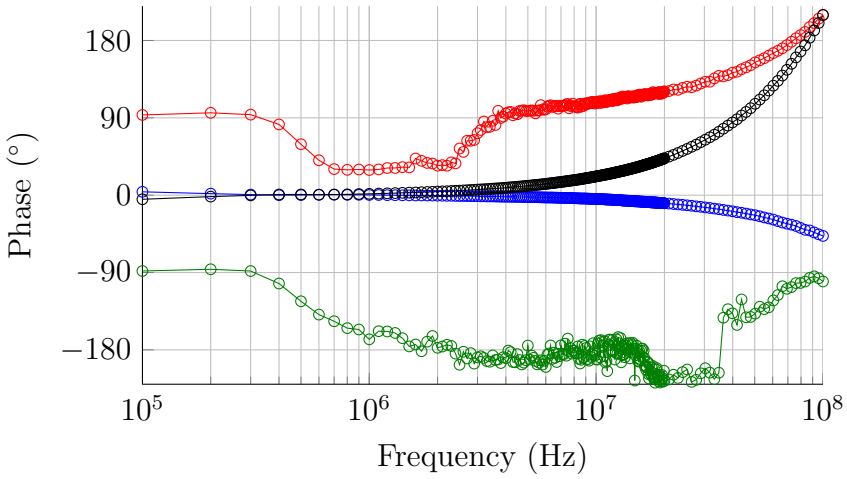


Figure 4.13: Phase of coefficients $\hat{s}$ (blue), $\hat{v}$ (black), $\hat{t}$ (green) and $\hat{u}$ (red) -Port 2- of calibration matrix M versus frequency for typical setup configuration.

sinusoidal voltage waveform. The phase is determine by measuring the delay τ from the trigger instant t_0 to the first positive crossing of the mean value of the sinusoidal voltage waveform and can be calculated as

$$\phi = 2\pi f \tau \tag{4.51}$$

where f is the used frequency.
The complex phasor of the wave a becomes

$$a = \frac{V_{pp}}{2\sqrt{50}} e^{-j\phi} \tag{4.52}$$

The measurement of the peak-to-peak amplitude and considering the mean value of the sine allow to minimize the effect of any DC offset error introduced by the scope[1].

The trigger signal comes from the AFG and is always synchronised with the beginning of the period of the generated signal (the sinusoidal waveform in the case of the calibration) on the main output channel. Besides starting the scope acquisition, the trigger therefore defines also the time instant of reference t_0 against which all the phases of the measured signals are calculated.

[1]Oscilloscope's DC offset accuracy is usually worse than the AC gain accuracy.

As already stated the scope has a limited vertical resolution. In order to maximise the accuracy of all measurements is thus important to use always the smallest allowed vertical range that guarantees not to clip the signal. For the Load standard for instance the reflected wave could be very small while for the Open almost all the incident wave is reflected. An optimized autoscale algorithm has thus been implemented to set in the best way possible the vertical range of the individual channels.

In order to improve the precision of the measurement and to reduce the effect of noise it is also possible to set in the software the number Na of waveforms to be acquired and averaged. Assuming that the noise is random with a uniform Gaussian distribution and that it is uncorrelated with the signal, the theoretical improvement in terms of extra bit of vertical resolution is

$$Nb = \frac{1}{2}\log_2(Na) \tag{4.53}$$

It has to be considered that increasing the number of averages increases the time required for the measurement. A good compromise is obtained with $Na = 128$ and this value has been used for measurements presented here.

Also the horizontal temporal resolution is limited and depends mainly on the used sampling rate Sr being the sampling period inversely proportional to it. For instance, in the case of the Agilent 54845A scope used in this work, the time delay measurement accuracy is specified [33] as

$$\pm\left[(0.007\%)\Delta t + \frac{0.2}{Sr}\right] \tag{4.54}$$

Note that this accuracy is better than $1/Sr$ due to the use of $\sin(x)/x$ interpolation and that there is also a small dependency on the measured time difference Δt. To improve the time measurement accuracy is thus desirable to maximize the sampling rate. On the other hand, for a correct phase determination, it is necessary to acquire at least a complete period T of the calibration sine wave. The number of points required is

$$Np = TSr \tag{4.55}$$

At low frequency this could be a problem due to limited memory resources of the scope. Therefore, for every harmonic frequency, the highest sampling rate that

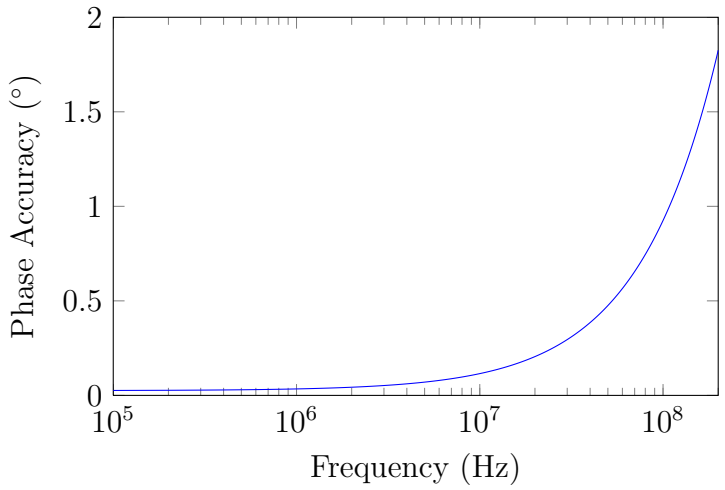


Figure 4.14: Theoretical phase accuracy versus frequency with Agilent 54845A DSO for a sampling rate of 8 GS/s.

guarantees to be able to acquire a whole period is selected.

As a consequence of (4.54) and (4.51), considering a constant sampling rate for all the harmonics, the accuracy of the phase determination worsens with increasing frequency. As an example, in Fig. 4.14 is reported the theoretical phase accuracy in degrees versus frequency for a 8 GS/s sampling rate. Periodic pulse waveforms used in this work have an amplitude spectrum that is decreasing with frequency and most of the energy is well below 20 MHz. The phase error introduced in our case is therefore not relevant. However, in trying to adopt this approach for higher frequency, the phase accuracy could quickly become the limiting factor.

4.5.4 Calibration verification

In order to verify the measurement and calibration procedure, different experiments were conducted. A full two port calibration of the setup has been performed as explained in previous Sections using a frequency grid uniformly spaced from 100 kHz to 20 MHz in steps of 100 kHz and logarithmically spaced from 20 MHz up to 120 MHz with 50 points per decade. A scope channel setted to 1 MΩ input impedance has then been connected in place of the DUT on the input (1) section of the setup (see Fig. 4.7). Outputs a_{R1} and b_{R1} from the coupler are connected to other two 50 Ω channels. The function generator is setted to generate 50 ns pulses with a period of 5 µs ($f_0 = 200$ kHz). The three channels are acquired at

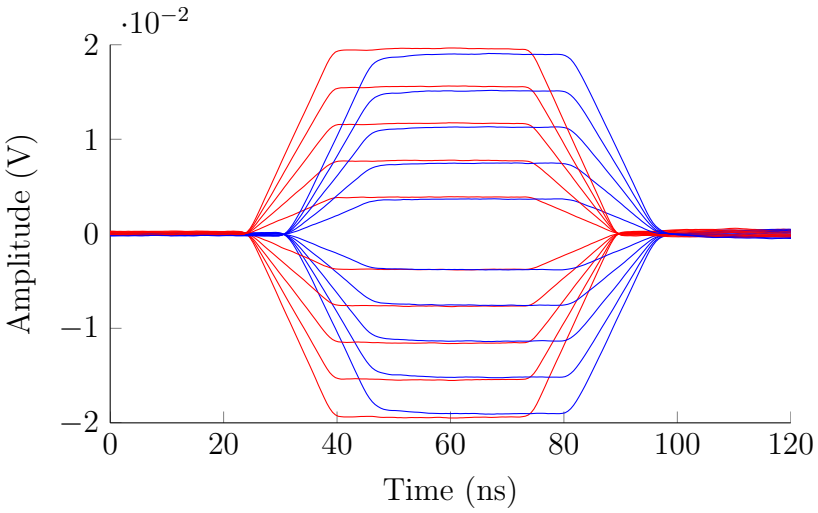


Figure 4.15: Raw a_{R1} (red) and b_{R1} (blue) measurements for different pulses amplitudes with 1 MΩ load.

the same time and voltage pulses reconstructed applying the calibration to a_{R1} and b_{R1} are compared with the pulses directly measured on the 1 MΩ channel.

In Fig. 4.15 are shown measured a_{R1} and b_{R1} waves for different amplitudes. Reconstructed voltage waveforms at the reference plane obtained by applying the calibration are shown in Fig. 4.16a along whit voltage pulses directly measured by the scope as a comparison. From the figure it is possible to see how waveforms are correctly aligned in time compared also to the raw acquisition of a_{R1} and b_{R1} of Fig. 4.15.

The relative amplitude error calculated for every time instant t_k as

$$Err_{rel}(t_k) = 100 \times \left| \frac{V_{meas}(t_k) - V_{rec}(t_k)}{V_{meas}(t_k)} \right| \tag{4.56}$$

is plotted in Fig. 4.17a for all pulses amplitudes. For smaller pulses the relative error is around 2 % but it is important to note that the relative error gets better as the amplitude increases.

The same verification experiment has been conducted for the output section (2), in this case also with the power amplifier connected between the output of the function generator and the coupler (see Fig. 4.1). As shown in Figures 4.16b and 4.17b similar results were obtained.

Other verification measurements where conducted changing pulses parameters

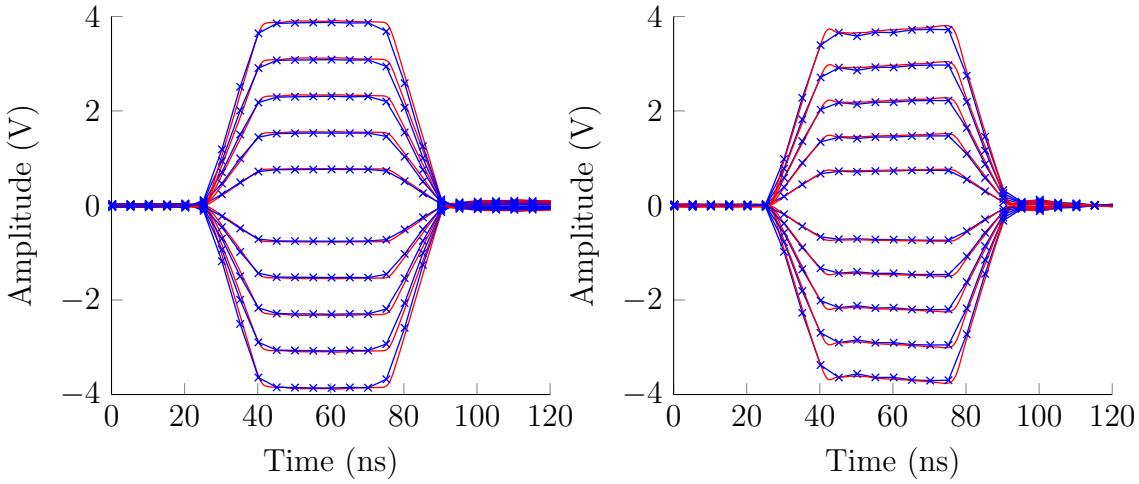


Figure 4.16: Reconstructed voltage waveforms at the reference plane for different amplitudes (blue) and directly measured waveforms (red) for input (a) and output (b) section of setup.

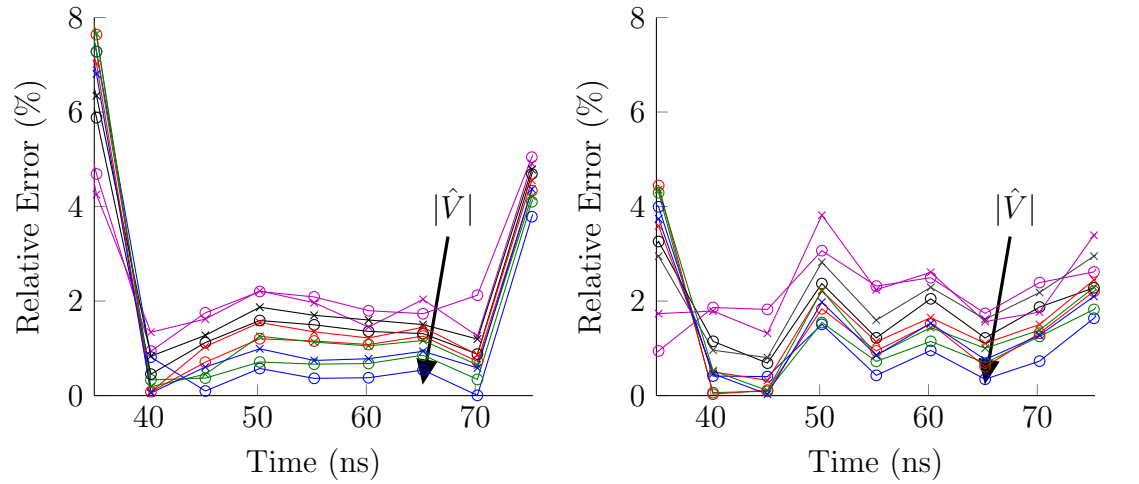


Figure 4.17: Relative error for voltage pulses of Fig. 4.16a for input (a) and Fig. 4.16b for output section of setup (b). The error decreases as the pulse amplitude increases.

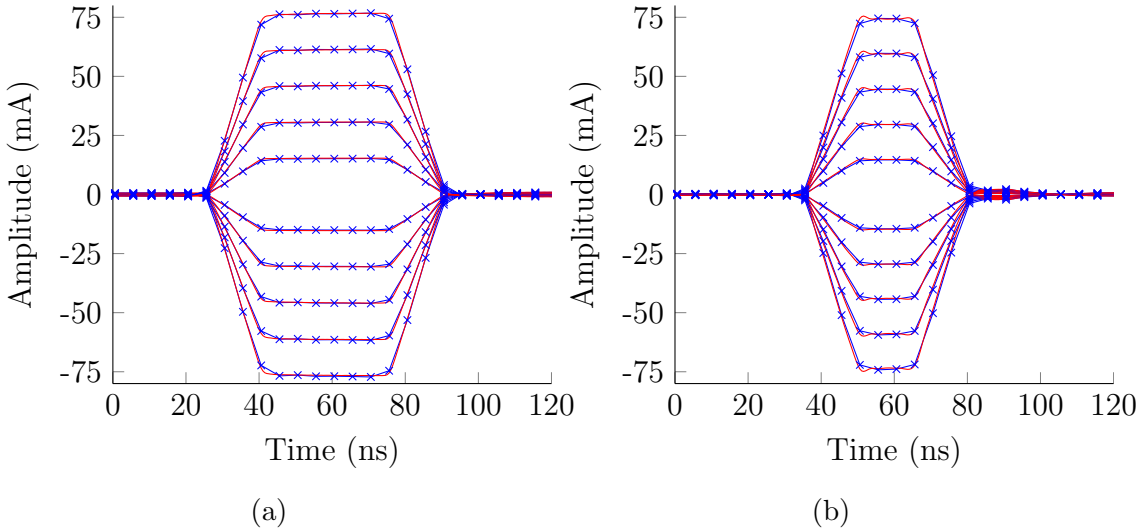


Figure 4.18: Reconstructed *current* waveforms at the reference plane for different amplitudes (blue) and measured waveforms (red) for input (a) and output (b) section of setup.

and with slightly different setup configurations obtaining always similar results in terms of relative error.

For instance, to verify also current accuracy, outputs of section (1) and (2) have been connected this time to scope 50 Ω channels. In Fig. 4.18a are shown the reconstructed current pulses and the pulses obtained from the direct voltage measurement divided by the nominal 50 Ω input impedance. Also in this case the calibration guarantee a good accuracy (Fig. 4.19a). Similar results for section (2) are shown in Fig. 4.18b and 4.19b. Note how in this case a pulse length of only 20 ns has been used.

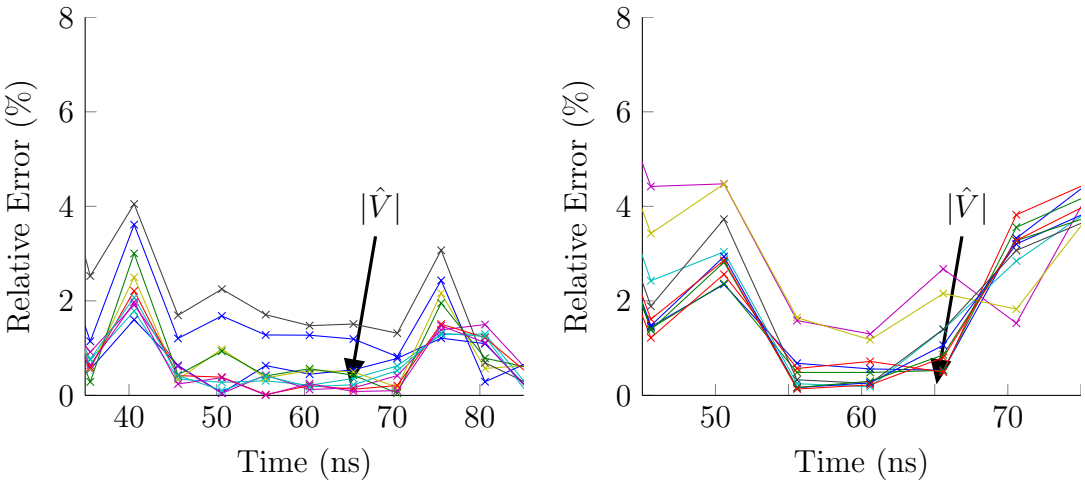


Figure 4.19: Relative error for *current* pulses of Fig. 4.18a for input (a) and Fig. 4.18b for output section of setup (b). The error decreases as the pulse amplitude increases.

4.5.5 DC calibration

As already explained, the setup guarantees AC and DC path separation and in previous Sections the procedure for the AC path calibration has been presented. For the DC path it has to be considered that a parasitic resistance from the DC source/monitor to probe tips is present. This series resistance is in part due to cables and in part due to bias tees and usually is of the order of 1–2 Ω. For instance, for a GaN device biased at 20 V on the drain and with a drain current of 500 mA, a parasitic resistance of 1.5 Ω means an error of 1 V, or 5 %, on the actual bias point. For the pulsed characterization it is important to set and to know the correct bias point because, as explained, dispersive effects are strongly dependent on the DC polarization starting condition.

The DC calibration is performed as an added step during the Short measurement step of the relative calibration explained in Section 4.5.1. With the DC source/monitor, a small DC current is sweep from −10 mA to 10 mA in steps of 1 mA while the voltage is measured. Resistances R_g and R_d, of the gate and drain DC paths, are calculated from the slope of the linear least square fitting of measurements. Imposing the current and measuring the voltage guarantees always a safe current on the Short standard.

During the biasing of the device, before the pulsed measurement, R_g and R_d are then used in an iterative procedure for setting the correct biasing point.

4.6 Characterization of GaAs HEMTs

The measurement setup and the corresponding calibration technique have been first validated through GaAs HEMTs. The Power Amplifier shown at the drain side in Fig. 4.1 was not needed in this case. Small-signal trans-conductance and output-conductance of a GaAs pHEMT ($L = 0.25\,\mu m$, $W = 300\,\mu m$) have been obtained from S-parameters measured on-wafer at different biases and at 250 MHz. At this frequency the displacement contribution to the drain current is negligible and the admittance parameters are almost real quantities.

Provided that the upper frequency cut-off of the dispersive phenomena (thermal and charge trapping effects) lays below the lower spectral component f_1 of the pulsed periodic excitation waveform, so called above cut-off conditions are met. In this case, the slopes of the measured pulsed IV curves in their quiescent points should be coherent with the differential parameters obtained from standard VNAs.

Sets of pulsed drain current measurements have been carried out by choosing different couples of gate and drain voltage bias conditions. Constant gate voltage has been kept during these measurements and pulses have been initially applied to the drain terminal only. Then, the slopes versus the drain voltage of the pulsed IV curves in the bias points have been evaluated and compared with output conductance data from VNA measurements.

Pulse width and duty cycle have been initially chosen equal to 200 ns (20 ns rise time) and 10 %, respectively. Good agreement on output conductance has been verified (also taking into account that rather small absolute quantities are being considered), as shown in Table 4.2.

In order to test the amount of dispersion mainly due to charge trapping in the device, the pulsed IV characteristics have been compared to corresponding static IV curves. Two sets of curves, at $V_{G0} = -0.4\,V$, $V_{D0} = 5\,V$ and $V_{G0} = -0.5\,V$, $V_{D0} = 5\,V$ are for instance shown in Fig. 4.20. Quite critical differences of slopes are observed between the static and the pulsed curves (static output conductance is about 2 mS in $V_{G0} = -0.4\,V$, $V_{D0} = 5\,V$, so the dispersion leads to a variation from the static value of about 70 %).

Bias		Output Conductance from S-par. at 250 MHz (mS)	Output Conductance from pulsed I/V (mS)	Relative Difference (%)
V_{G0} (V)	V_{D0} (V)			
−0.4	1.5	6.56	6.51	−0.76
−0.4	5	3.40	3.11	−8.5
−0.5	1.5	6.35	6.74	6.14
−0.5	5	3.34	3.21	3.89
−0.6	5	3.22	3.18	−1.2

Table 4.2: GaAs pHEMT ($L = 0.25\,\mu m$, $W = 300\,\mu m$): Small-Signal Output Conductance

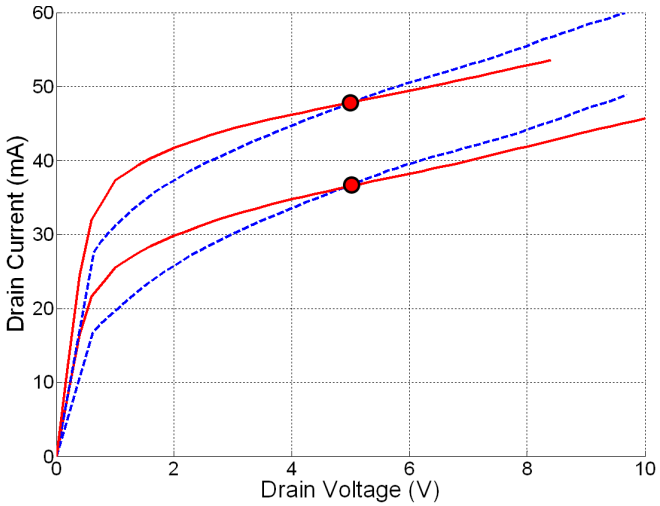


Figure 4.20: GaAs pHEMT - Measured Static (continuous lines) and pulsed (slashed) drain current sets from $V_{G0} = -0.5\,V$, $V_{D0} = 5\,V$ and $V_{G0} = -0.4\,V$, $V_{D0} = 5\,V$. Biases of the two sets are outlined in red. Drain pulses only.

Another test was carried out by biasing the device in $V_{G0} = -0.5\,V$, $V_{D0} = 5\,V$ and by applying gate pulses only. Obtained pulsed trans-characteristic data are shown in Fig. 4.21. No compensation of the $50\,\Omega$ load-line was carried out during this test. The slope of the curve in the quiescent condition corresponds to 95.43 mS. This value is in good agreement with 92.14 mS obtained by using S-parameters in

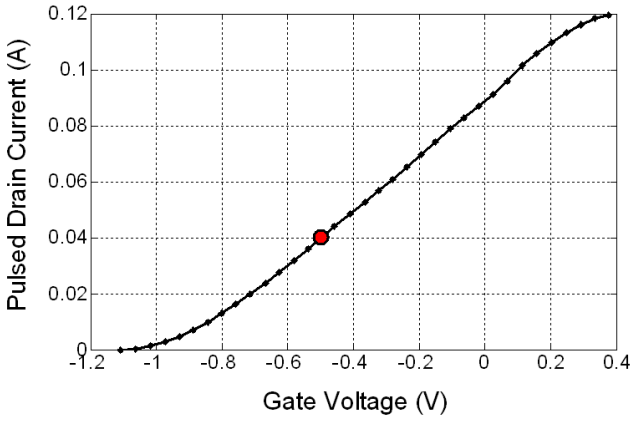


Figure 4.21: GaAs pHEMT - Pulsed Drain Current from $V_{G0} = -0.5\,\mathrm{V}$, $V_{D0} = 5\,\mathrm{V}$. Bias condition is outlined in red. Gate pulses, $50\,\Omega$ load.

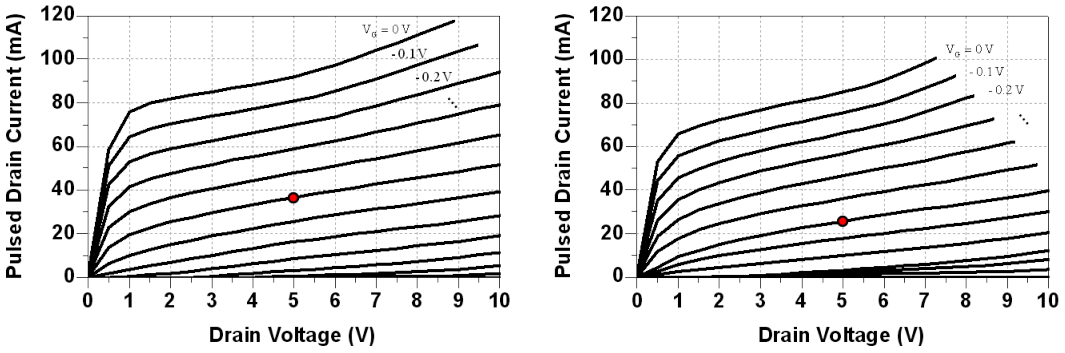
the same bias (3.57 % error) and taking into account the $50\,\Omega$ termination:

$$g_m = \Re\left\{\frac{Y_{21}}{1 + R_0 Y_{22}}\right\} \tag{4.57}$$

In order to test the pulsed setup in full operative mode, by also taking into account the measurement data post-processing procedures, a full characterization of the GaAs pHEMT was carried out through the application of simultaneous pulses from both gate and drain ports, by adopting waveforms with 50 ns pulse width and 1 % duty cycle. The post-processing compensate the effects of the $50\,\Omega$ terminations and leads to look-up-tables functions defined on a rectangular grid of voltages at the device ports. An example of measured pulsed-IV characteristics is shown in Fig. 4.22, where all the data shown have been obtained without extrapolation.

A new test of coherence between pulsed IV slopes versus gate (G_m) and drain (G_d) voltages and admittance parameters obtained from S-parameters ($\Re\{Y_{21}\}$, $\Re\{Y_{22}\}$) has been carried out on these data. Corresponding results are presented in Table 4.3.

In order to show the effects of the $50\,\Omega$ pulse wave sources on the resulting voltages at the DUT ports, a set of gate and drain voltage pairs corresponding to a uniform grid of incident excitation waves is presented in Fig. 4.23a (circles). As it can be seen, all the voltage pairs corresponding to a given gate pulse-wave

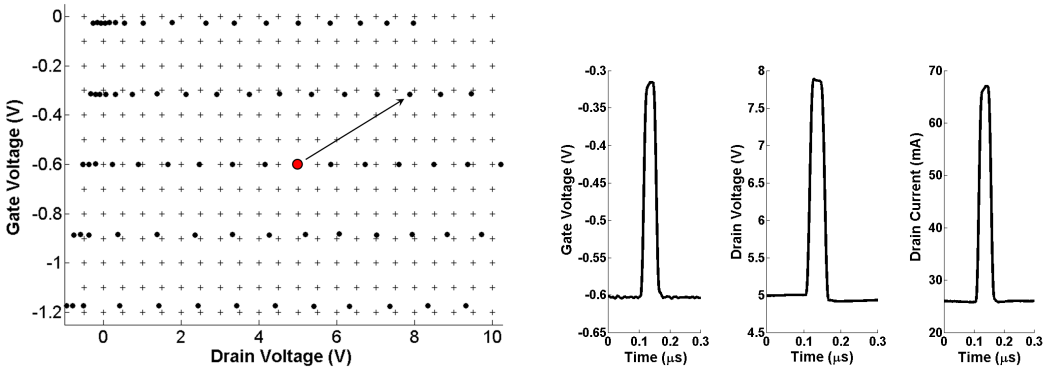


(a) (b)

Figure 4.22: GaAs pHEMT ($L = 0.25\,\mu m$, $W = 300\,\mu m$): Pulsed IV Characteristics measured (pulse width: 50 ns, duty cycle: 1 %) with the new setup from $V_{G0} = -0.5\,V$, $V_{D0} = 5\,V$ (a), $V_{G0} = -0.6\,V$, $V_{D0} = 5\,V$ (b).

Bias			Y-par (50 MHz)		Pulsed I/V		Relative Diff.	
V_{G0} (V)	V_{D0} (V)	I_{D0} (mA)	$\Re\{Y_{21}\}$ (mS)	$\Re\{Y_{22}\}$ (mS)	G_m (mS)	G_d (mS)	G_m %	G_d %
−0.8	5	9.4	69.2	2.4	65.0	2.3	−6.1	−1.3
−0.6	3	22.4	101.8	4.0	88.5	3.9	−13.1	−1.5
−0.6	5	25.6	102.5	3.2	91.2	3.1	−11.1	−4.0
−0.3	5	57.8	104.0	3.4	100.0	3.4	−3.9	0.6

Table 4.3: GaAs pHEMT ($L = 0.25\,\mu m$, $W = 300\,\mu m$): Pulsed IV Slopes Coherence Test.



(a) (b)

Figure 4.23: a) Gate and Drain voltage pairs at the DUT ports corresponding to incident and reflected wave acquisitions (•) and to reconstructed points on a uniform grid (+); b) Example of pulse waveforms of gate/drain voltages and drain current obtained from measured incident and reflected waves.

excitation lay on a straight line, due to the almost open circuit condition at the DUT input. Post-processing of measured data leads to reconstruct the pulsed drain I/V characteristics on a uniform grid of voltages (see for instance the plus-symbols grid in the same figure). Time-domain waveform examples of the gate and drain voltages and of the drain current obtained after post-processing of data is reported in Fig. 4.23b (pulse highlighted in Fig. 4.23a).

The pulsed drain current characteristics have been eventually used for the extraction of a compact quasi-static high-frequency model of the GaAs pHEMT as shown in Fig. 4.24. This was implemented into Agilent Advanced Design System (ADS) CAD. Lumped extrinsic parasitic components, according to the circuit topology shown in the figure, have been identified by fitting RF small-signal differential-parameters under Cold FET [34] and off-state channel gate bias. The obtained values are reported in Fig. 4.24. Parasitic effects have been de-embedded from the pulsed drain characteristics and the intrinsic current versus voltage description has been stored into a look-up-table (LUT).

A purely capacitive-like quasi-static description of the displacement gate and drain current contributions have been extracted from multi-bias Y-parameters at low frequencies (in the range between some hundreds of megahertz and a few gigahertz where the device almost exhibits a purely quasi-static behaviour). The non linear capacitance matrix (as a function of gate and drain voltages) has been also de-embedded from parasitics and the four capacitances stored

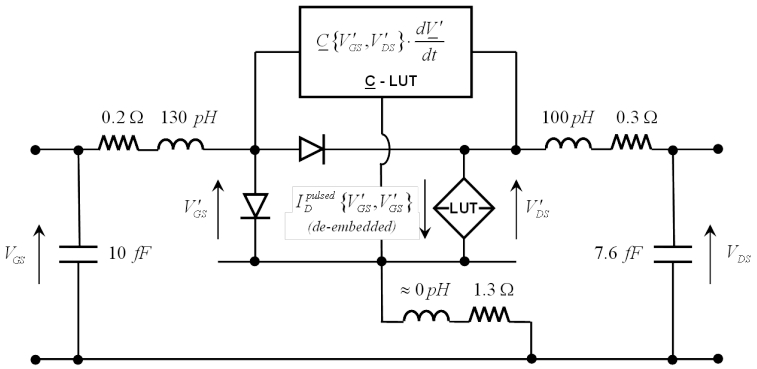


Figure 4.24: Equivalent Circuit Model used for large-signal HB simulations of an S-band single stage Power Amplifier.

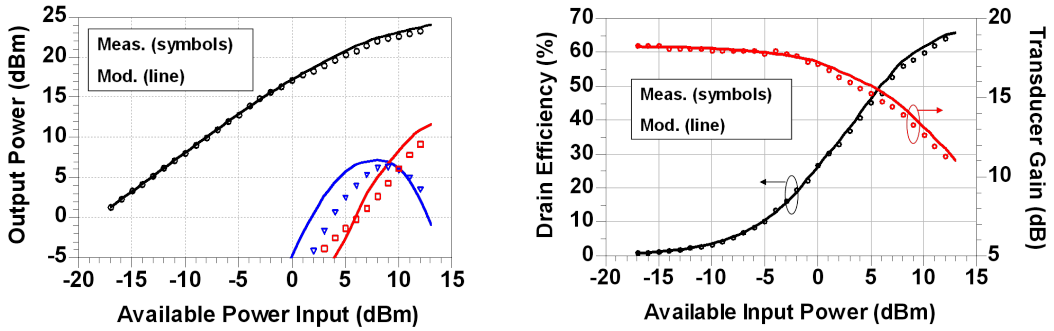


Figure 4.25: GaAs pHEMT ($L = 0.25\,\mu m$, $W = 300\,\mu m$): Large Signal test. Single stage Power Amplifier ($50\,\Omega$ terminations) at $f_0 = 2.5\,GHz$. Output power (1^{st}, 2^{nd},3^{rd} Harmonics) (left), Transducer Gain and Drain Efficiency (right). Bias: $V_{G0} = -0.5\,V$, $V_{D0} = 5\,V$ ($I_{D0} = 37\,mA$).

into LUTs. Displacement currents are implemented into the CAD environment through Symbolically Defined Devices. Finally, gate-source and gate-drain diodes were identified from Gummel-Plots under forward bias of the gate junction, de-embedded from parasitics and implemented into schematic.

The model has been used for the large-signal simulation of a single-stage PA working at 2.5 GHz in two bias conditions. Gate and drain terminations were set at $50\,\Omega$. Experimental validation results (on-wafer) are shown in Fig. 4.25 in terms of 1^{st}, 2^{nd} and 3^{rd} harmonic output power, Transducer Gain and Drain Efficiency. It must be emphasized that little thermal self- heating takes place into these devices when measured on-wafer. Otherwise, thermal corrections should have been taken into account, especially at very high level of input power.

Bias			Y-par. (50 MHz)		Pulsed I/V		Relative Diff.	
V_{G0} (V)	V_{D0} (V)	I_{D0} (mA)	$\Re\{Y_{21}\}$ (mS)	$\Re\{Y_{22}\}$ (mS)	G_m (mS)	G_d (mS)	G_m %	G_d %
−2.0	15	48.4	169.2	4.9	189.6	4.9	12.1	−1.0
−2.1	20	47.8	149.9	3.9	153.2	3.8	2.2	−3.8
−1.6	25	145.1	186.6	3.8	203.6	3.5	9.1	−8.8
−0.6	25	284.9	153.2	3.3	162.3	2.9	6.0	−11.3

Table 4.4: GaN HEMT ($L = 0.25\,\mu m$, $W = 600\,\mu m$): Small-Signal Output Conductance

4.7 Characterization of GaN HEMTs

An AlGaN/GaN FET on SiC ($L = 0.25\,\mu m$, $W = 300\,\mu m$, $I_{DSS} = 450\,mA$) has been characterized on-wafer under gate and drain pulsed excitations ($\tau = 50\,ns$, $\delta = 1\,\%$). As in the previous case, pulsed IV slopes around the quiescent conditions, both versus drain and gate voltage variations, have been compared to the real parts of small-signal admittance parameters obtained from low-frequency VNA data. The results are presented in Table 4.4 for different bias conditions. The relative differences observed are comparable with those obtained with the GaAs based device.

Instead, a different behaviour is observed when considering the large-signal pulsed behaviour. Drain-pulsed-only IV characteristics at constant gate voltage were first measured. The experiment has been repeated twice, by choosing $V_{D0} = 15\,V$ and $V_{D0} = 25\,V$. The obtained IV-plots are shown in Fig. 4.26a and Fig. 4.26b respectively (continuous lines), while the corresponding average drain currents appear in Fig. 4.26c and Fig. 4.26d.

A slope change in the pulsed drain IV curves at each of the two gate voltages considered is well observed. This change always occurs at the drain voltage corresponding to the selected bias condition. Changing the bias condition leads to a corresponding shift in the position of the slope-change. Dramatic drop in the average current is observed in the presence of positive drain pulses ($\hat{V}_D > V_{D0}$), while almost constant average values are monitored in the presence of negative drain pulses ($\hat{V}_D < V_{D0}$). Since thermal phenomena are generally characterized by slow time constants, we assume that they do not play a role in the pulsed

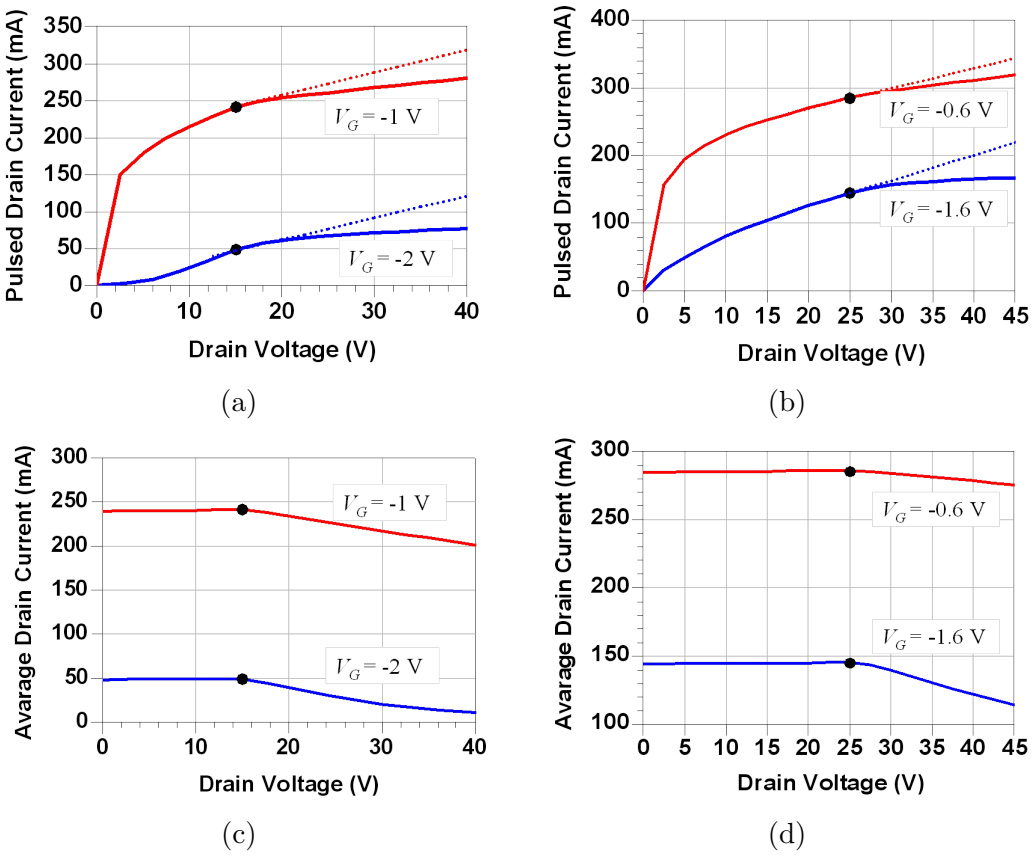


Figure 4.26: GaN HEMT ($L = 0.25\,\mu m$, $W = 600\,\mu m$): Drain-Pulsed I/V curves at constant Gate voltages. Drain pulses from $V_{D0} = 15\,V$ (a) and $V_{D0} = 25\,V$ (b). Corresponding average drain currents (c), (d). Slashed lines in (a) and (b) correspond to what it would be observed, if the average drain current is kept constant at the bias value.

experiment considered (i.e. constant internal temperature Θ_0 at all the pulsed IV points). Thus, according to

$$I_{D0} = F\{V_{G0}, V_{D0}, \tilde{X}, \vartheta_0\} \tag{4.58}$$

the observed behaviour of the average drain current suggests that the set of variables $\tilde{X}$ representing the state of traps could depend on peak values of drain voltages in the case of positive pulses, i.e.:

$$\tilde{X} = f(V_{G0}, V_{D0}, \hat{V}_D) \tag{4.59}$$

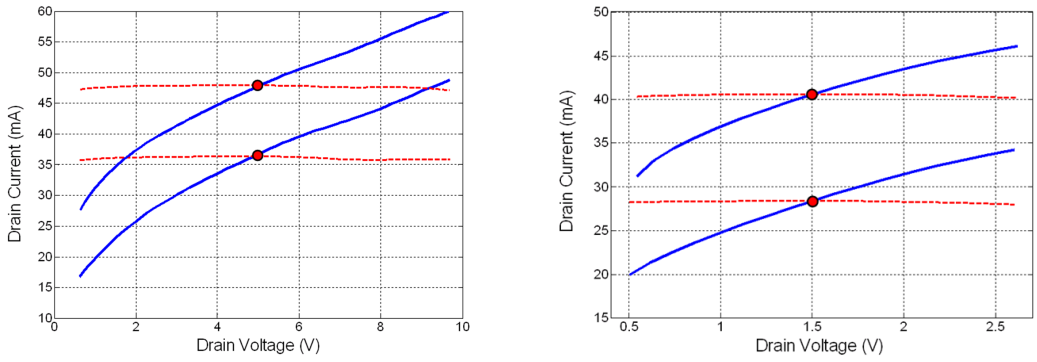
while a simple dependence on the average drain voltage can be accepted in the case of negative pulses, i.e.:

$$\tilde{X} = f(V_{G0}, V_{D0}) \tag{4.60}$$

This behaviour is in agreement with Jardel et al. [16]. Charge capture time constants are smaller than the actual pulse width (50 ns), so that traps change their state during the positive pulses. This leads to observe in Figures 4.26a and 4.26b an almost iso-thermal-DC IV characteristic for each $\hat{V}_D > V_{D0}$ (with decrease in the output IV slope). The same does not apply when negative drain pulses ($\hat{V}_D < V_{D0}$) are considered, because charge emission time constants are sensibly longer than pulse width. This leads to observe an almost ideal iso-thermal and traps- frozen IV characteristic for each $V_D < V_{D0}$.

For the sake of comparison, the same kind of experiment has been carried out with the GaAs pHEMT already introduced in the previous Section. Pulsed and average drain currents at two constant gate voltages are plotted in Figures 4.27a and 4.27b. Neither critical slope-changes in the pulsed IV curve nor variations in the average drain current are observed when considering both negative and positive pulses. This could possibly suggest that capture and emission time constants are in these GaAs devices both long enough to satisfy above cut-off pulsed operation.

The testing of the pulsed IV behaviour with respect to gate-only pulses was not such as straightforward. In fact, due to the 50 Ω load-line, a gate pulse always also leads to an associated drain pulse. Thus, IV characteristics were measured by simultaneously pulsing from the gate and drain ports and the IV data were



(a) (b)

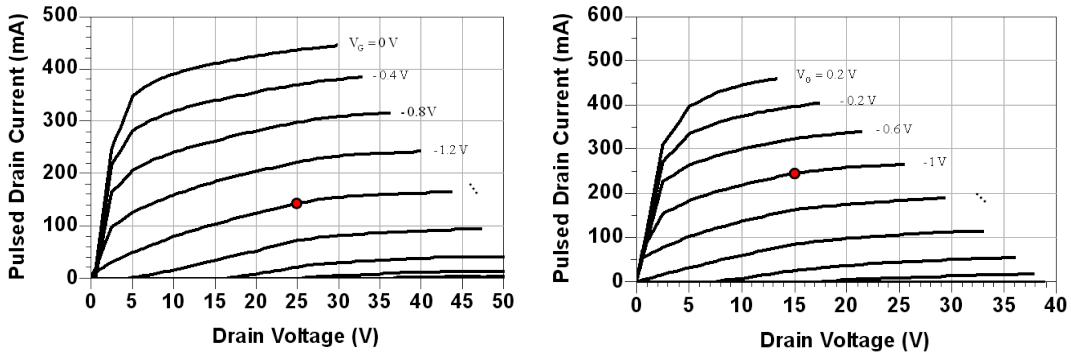
Figure 4.27: GaAs pHEMT : Pulsed (continuous) and average (slashed) Drain Current at $V_{G0} = -0.5\,\mathrm{V}$ and $V_{G0} = -0.4\,\mathrm{V}$. Drain pulses only at $V_{D0} = 5\,\mathrm{V}$ (a) and $V_{D0} = 1.5\,\mathrm{V}$ (b).

interpolated on a rectangular grid of voltages at the device ports. For instance, the pulsed IV characteristics obtained from $V_{G0} = -1.6\,\mathrm{V}$, $V_{D0} = 25\,\mathrm{V}$ and from $V_{G0} = -1\,\mathrm{V}$, $V_{D0} = 15\,\mathrm{V}$ are shown in Figures 4.28a and 4.28b, respectively. Moreover, the pulsed trans-characteristics corresponding to $V_{D0} = 25\,\mathrm{V}$ and $V_{D0} = 15\,\mathrm{V}$ are shown in Figures 4.29a and 4.29b. In the same figures the average current values are superimposed. Almost constant average current values are observed versus gate voltage variations.

Finally, the average currents observed in the presence of both gate and drain pulses are presented in Figures 4.30a and 4.30b. As it can be seen, in the presence of positive drain pulses, the peak of the gate pulse also plays a role in the definition of the trap states.

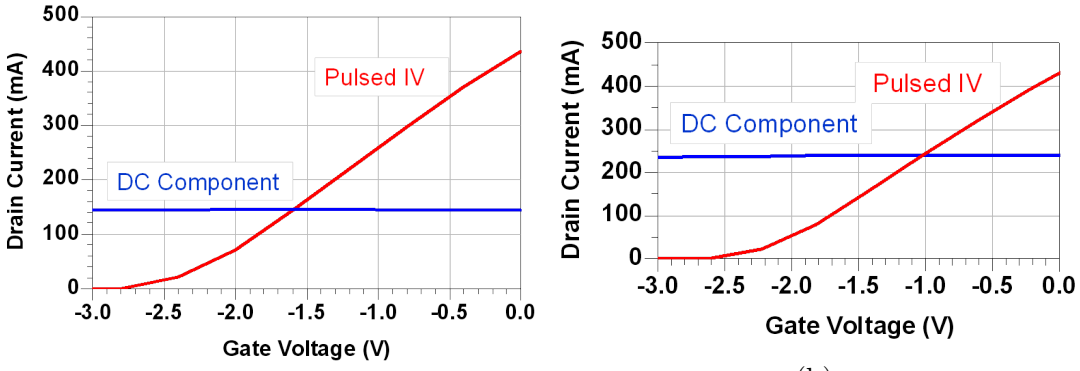
4.8 Conclusions

In this Chapter a new measurement setup for the pulsed characterization of devices has been presented. This system has many advantages compared to conventional setup and in particular allows to generate and measure shorter pulses. Moreover, a full calibration procedure has been implemented and validated. The setup has then been used to characterize GaAs and GaN on SiC Field Effect Transistors. Critical differences in the behaviour of the charge trapping phenomena taking place into these devices have been highlighted through the interpretation of the average



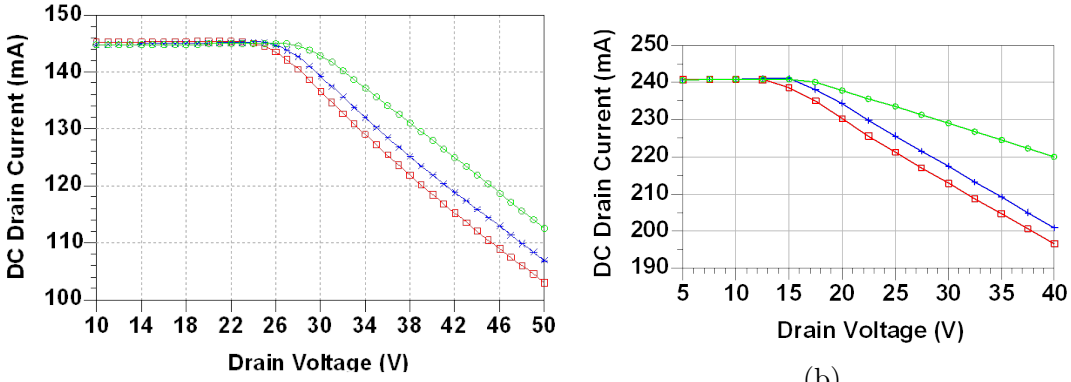
(a) (b)

Figure 4.28: GaN HEMT ($L = 0.25\,\mu m$, $W = 600\,\mu m$) : Pulsed Drain current characteristics from $V_{G0} = -1.6\,V$, $V_{D0} = 25\,V$ (a) and $V_{G0} = -1\,V$, $V_{D0} = 15\,V$ (b).



(a) (b)

Figure 4.29: GaN HEMT ($L = 0.25\,\mu m$, $W = 600\,\mu m$) : Pulsed trans-characteristics from $V_{G0} = -1.6\,V$, $V_{D0} = 25\,V$ (a) and $V_{G0} = -1\,V$, $V_{D0} = 15\,V$ (b).Curves are plotted for the drain voltage corresponding to the quiescent condition. Direct current components are also plotted in the figures.



(a) (b)

Figure 4.30: GaN HEMT ($L = 0.25\,\mu m$, $W = 600\,\mu m$) : Average drain current measured during a gate and drain pulsed IV acquisition: $\hat{V}_G = -1.6\,V$ (blue-crosses), $\hat{V}_G = -2.4\,V$ (red-squares), $\hat{V}_G = -0.8\,V$ (green-circles). Pulses from $V_{G0} = -1.6\,V$, $V_{D0} = 25\,V$ (a); $\hat{V}_G = -1\,V$ (blue-crosses), $\hat{V}_G = -2.2\,V$ (red-squares), $\hat{V}_G = -0.2\,V$ (green-circles). Pulses from $V_{G0} = -1\,V$, $V_{D0} = 15\,V$ (b).

drain currents measured during the pulsed characterization. This allows to observe that, in some circumstances, even a pulse length of 50 ns is not short enough to consider the state of traps as only determined by the bias point. The presented results prove that the trapping and detrapping behaviour in GaN HEMTs is highly asymmetric. Time constant associated with traps capture are really fast while the emission is a slow process. The proposed setup represents in our opinion a valuable characterization instrument, which will allow further investigations of the complex charge trapping phenomena in GaN FETs and the development of pulsed measurement procedures to be used for nonlinear model extractions and circuit design.

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Chapter 5

Transient response characterization

5.1 Introduction

One of the aims of the pulsed characterization setup presented in Chapter 4 was to generate pulses short enough to be faster than the time constants associated with thermal and trapping dispersive phenomena in order to obtain iso-dynamic pulsed I/V characteristics. In other words, we wanted to characterize devices above the cut-off frequency of dispersive phenomena. It has been shown for instance that with GaN HEMTs this requirement can be met when pulsing from a drain voltage bias to lower voltages while, pulsing to higher voltages, a change in the mean value of the drain current is observed indicating a change in the state of traps.

Otherwise, in practical applications, devices could be driven or controlled by signals that have a dynamic behaviour that is slower than dispersive phenomena. In the frequency domain this means that real signals could have a significant energy content below the cut-off frequency.

Let's consider for example the case of a microwave power amplifier to be used in a 4G base station. New communication standards such as LTE are almost all based on OFDM modulations. This kind of modulations, which allows to obtain a high spectral efficiency in terms of (bit/s)/Hz, have a high peak-to-average power ratio (PAPR). As a consequence, a LTE modulated signal viewed in the time domain resembles a irregularly pulsed RF signal. Even if in theory the signal has

energy only in a bandwidth around the RF carrier frequency, due to inevitably non-linearities in the PA, the device is stimulated also by the baseband replica of the modulated signal which corresponds to its envelop. This could have a significant energy content also below the cut-off frequency of dispersive phenomena leading to added distortion by long-term memory effects.

In this Chapter, the measurement of the dynamic drain current response of GaN devices under pulsed voltage excitation is therefore exploited to study the behaviour below the cut-off frequency of dispersive phenomena.

This is relevant because it allows, for instance, to compare different technologies or different processing techniques and materials. Moreover, a pulsed bias voltages characterization represents in a realistic way the working condition for many applications. This is the case for Radars but also for communication standards where a time domain duplexing of the uplink and downlink channels is adopted (i.e. LTE-TDD). Here the PA in the transceiver is switched on and off, or to a low power consumption state, following the TDD timing defined in the standard.

To improve the efficiency of PAs, techniques like Envelope Tracking are being explored [1]. Also in this case the power supply to the devices in the PA is dynamically changed with a potential excitation of memory effects [2, 3].

The transient response of the drain current gives also some indication on the time constants involved. This kind of information is useful in the development and optimization of behavioural models [4–6] that are used for instance in the linearisation of power amplifiers.

Moreover, results of pulsed characterization are well suited to be used in the calibration of parameters of TCAD physic-based models of devices.

The setup developed for the transient current characterization with pulsed voltage excitation is described in Section 5.2 and some verification measurements on resistor and LDMOS transistor are presented in Section 5.3. Results obtained pulsing in different ways an AlGaN/GaN device are then analyzed in Section 5.4. In Section 5.5, it is shown how it is possible to model the current transient response by means of exponential decay functions. The technique is then used in Section 5.6 to compare different devices. Finally, in Section 5.7 are presented some results of a pulsed RF characterization that shows how long term memory effects can affect

also RF performances with a dynamic behaviour similar to the one measured on the drain current with pulsed drain voltage excitation.

This work was carried out at Chalmers University of Technology during my stay as a visiting Ph.D. student.

5.2 Setup description

The block diagram of the measurement setup used in this work is shown in Fig. 5.1. Although the configuration is similar to the one used in conventional pulsed characterization setups, the ability to fine control all the details of the measurement and the use of the digital sampling oscilloscope allows to explore new characterization methods. With commercial setups [7] for instance only the final pulsed IV characteristic is obtained while with this setup it is otherwise possible to study the whole time domain response of the drain current and not only the peak current inside pulses.

An HP85120A K43 pulser module is used for the generation of drain voltage pulses. This instrument has a low output impedance and is able to generate voltage pulses up to 40 V, both positive and negative with respect to a base

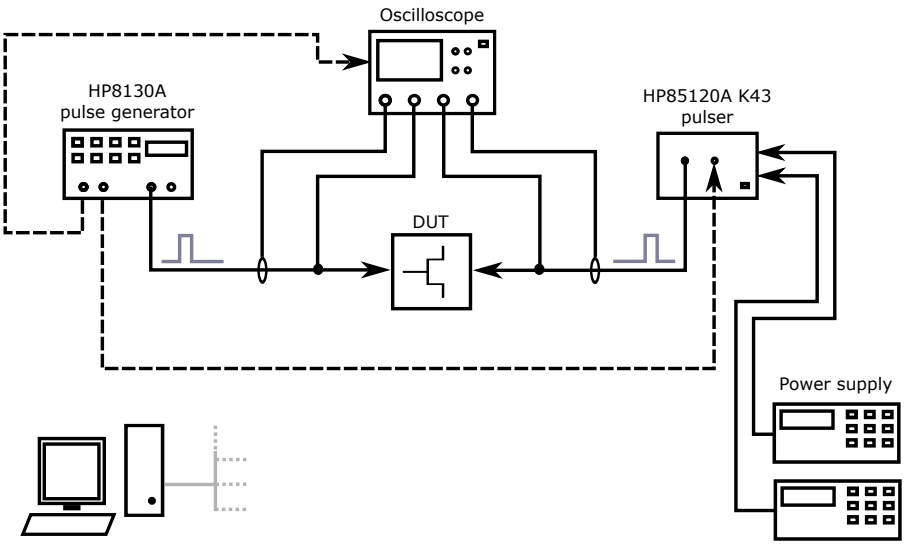


Figure 5.1: Block diagram of pulsed measurement setup.

voltage. Low and high pulses voltage levels are provided by two programmable DC power supplies (Agilent 6625A DC) which are also used to directly bias the gate of the DUT when only drain voltage pulses are applied.

One output channel of a HP8130A pulse generator is used as a master trigger for the HP85120A K43 while the second output channel can be used for pulsing directly the gate voltage when needed.

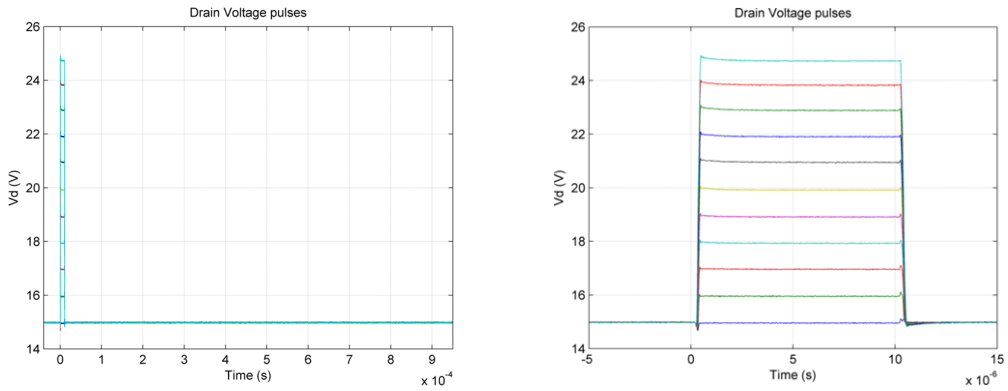
The drain current is measured with a Tektronix TCP202 current probe. This wideband probe is able to measure the current from DC up to 50 MHz. On the gate side is connected also a Tektronix CT-2 Current Transformer. This allows only the measurement of AC currents and has a high-pass frequency response with a lower cut-off frequency of 1.2 kHz. This probe is thus only used to monitor any eventual abnormal behaviour of the device. For instance, if the transistor under test has a high gate leakage current it will be clear from this monitoring.

A Tektronix TDS7104 Oscilloscope, with a maximum sampling rate of 10 GS/s, is used as the acquisition system and is triggered directly by the HP8130A. Current probes and high impedance voltage probes, used to monitor the applied voltage pulses, are thus connected to the four input channels of the scope.

All the instruments are controlled and synchronized by a Matlab program which allows also to set all the measurement parameters like the starting bias point, pulses lengths and period, number of averages, etc..

Before selecting the HP85120A K43 other pulser were also evaluated. In fact the quality of generated pulses varies greatly from instrument to instrument. Different pulser were compared doing a campaign of test measurements on resistors. Voltage pulses generated by the HP85120A K43 have almost no ringing both inside and after pulses. As will be shown, the absence of ringing after pulses is important to be able to correctly interpret the current transient. An example of generated drain voltage pulses of different amplitudes is shown in Fig. 5.2a and 5.2b.

The rise time of the pulses generated by the HP85120A K43 has been measured to be around 100 ns. Almost all the energy of pulses is thus well below 20 MHz (see Eq.(4.13)) which has been setted as the input bandwidth of the scope channels. In fact it has been verified with measurements on resistors that reducing the acquisition bandwidth to 20 MHz does not affect pulses waveforms compared to measurement made with the scope full analog bandwidth of 1 GHz. Instead,



(a) (b)

Figure 5.2: Example of drain voltage pulses of different amplitudes from a 15 V base voltage. Period 1 ms, pulse length 10 µs, duty cycle 1 % (a); Zoom in same pulses (b).

reducing the system bandwidth gives the advantage of considerably reducing the measurement noise.

With this setup the whole current ($I(t) = I_0 + i(t)$) and voltage ($V(t) = V_0 + v(t)$) waveforms are measured. As already explained, scopes have a limited DC accuracy and could present a small DC offset error. Moreover, also the current probe could have a small and constant offset. To compensate for this, before the actual pulsed measurement, the DC amplitude on the four channels is acquired while a DC 0 V is applied. After the measurement all the data is corrected by subtracting this offset.

Another important aspect to consider is the synchronization of gate and drain pulses. For this the output of gate and drain pulser are directly connected to the scope input channels and from the controlling software is then possible to adjust the relative delay between the two signals until a correct alignment is verified on the scope.

5.3 Verification measurements

As a first test to verify the setup, the measurement procedure and data post-processing, some experiments were conducted applying voltage pulses on resistors. The parameters of the measurement like the base voltage, pulse width, pulse period, etc. are the same that are used later for the characterization of GaN

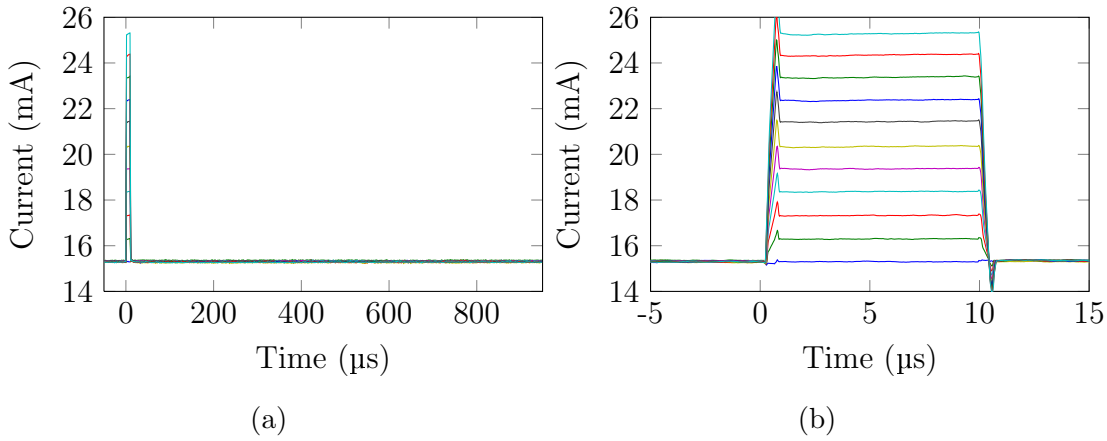


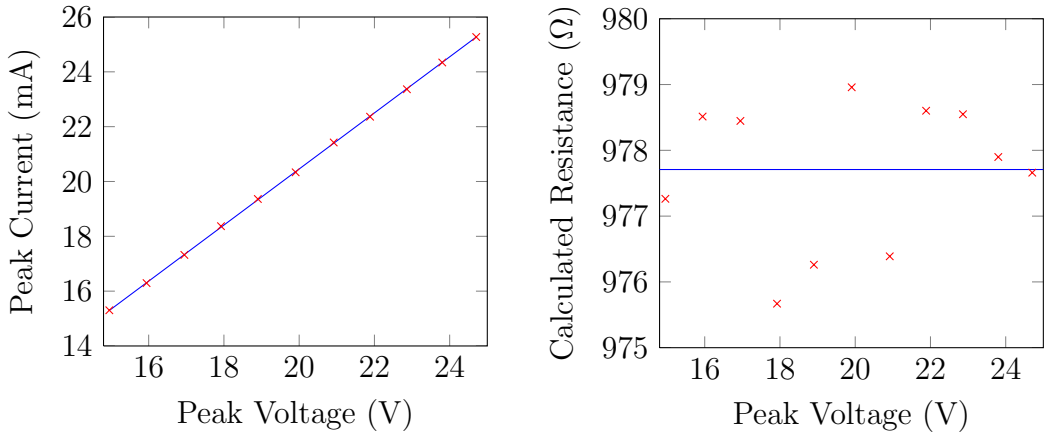
Figure 5.3: Measured current on resistor for different amplitudes of voltage pulses. Pulse width 10 µs, period 1 ms (a); Zoom in same pulses (b).

devices.

As an example in Fig. 5.3 is shown the acquired pulsed current on a resistor (this has been measured by means of a high precision Keytley 2400 SMU). The voltage pulses are the same shown in Fig. 5.2 with a base voltage of 15 V and maximum amplitudes from 16 V up to 25 V in steps of 1 V. The current presents some ringing at the beginning and ending of the pulse due to multiple reflections between the load and the pulser. This limits the minimum pulse width that is possible to use with this setup to approximately 500 ns. This is comparable to the capabilities of commonly available commercial systems but with the important advantage of being able to acquire the whole time-domain waveforms.

In Fig. 5.4a is shown the extracted pulsed IV characteristic of the resistor with a linear least square fitting of the measured data and in Fig. 5.4b the calculated resistance for every amplitude compared to the fitted value.

Other tests were conducted comparing the pulsed IV output characteristic obtained with the setup to the static IV measured by means of an Agilent 4156 Precision Semiconductor Parameter Analyzer. In Fig. 5.5 are shown the time-domain drain current responses of a Laterally Diffused Metal Oxide Semiconductor (LDMOS) transistor with a periphery of 3×100 µm pulsing the drain voltage down to 0 V (blue) and up to 25 V (red) from a bias point of $V_{G0} = 3.7$ V, $V_{D0} = 15$ V ($I_{D0} = 12$ mA). The output pulsed IV characteristic extracted from these measurements is shown in Fig. 5.6 superimposed on the corresponding static IV demonstrating a good agreement. LDMOS technology presents almost no



(a) Resistor pulsed IV characteristic with least square fitting.

(b) Calculated resistance for every peak voltage and least square fitting.

trapping phenomena and due to the low dissipated power the pulsed and static characteristics are coincident. As a consequence of the low output conductance of this device, the pulsed current amplitude for small voltages variations from the bias point in Fig. 5.5 is small.

5.4 Device characterization

In this work, instead to try to extract a complete pulsed IV characteristic, the aim is to study the effects that dispersive phenomena could have in a working condition similar to the one found in typical power amplifier applications and to compare different devices and technologies.

For this, it has been decided to characterize devices along a hypothetical load-line similar to the one that could be used in a Class-AB power amplifier. As shown schematically in Fig. 5.7 devices are therefore biased with a DC drain current of approximately 10 % to 20 % of the I_{DSS} maximum current determined from the static IV characteristic for $V_G = 0\,\mathrm{V}$ at the knee. From the bias condition appropriate gate and drain voltage pulses are then applied in order to follow the load-line. Considering for instance Gallium Nitride HEMTs, is thus necessary to simultaneously apply positive gate voltage pulses and negative drain voltage pulses with respect to the bias to reach the knee region, i.e. $\hat{V}_G > V_{G0}$, $\hat{V}_D < V_{D0}$. Instead, the opposite is true to reach the pinch-off region at high drain voltages: $\hat{V}_G < V_{G0}$, $\hat{V}_D > V_{D0}$.

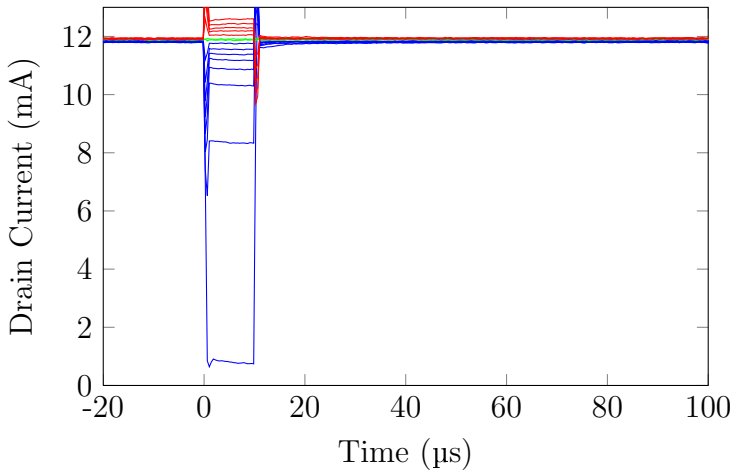


Figure 5.5: LDMOS ($W = 300\,\mu m$): time-domain drain pulsed current responses at $V_{G0} = 3.7\,V$ for lower (blue) and higher (red) amplitudes of drain voltage pulses from $V_{D0} = 15\,V$. Pulse width $10\,\mu s$, period $1\,ms$.

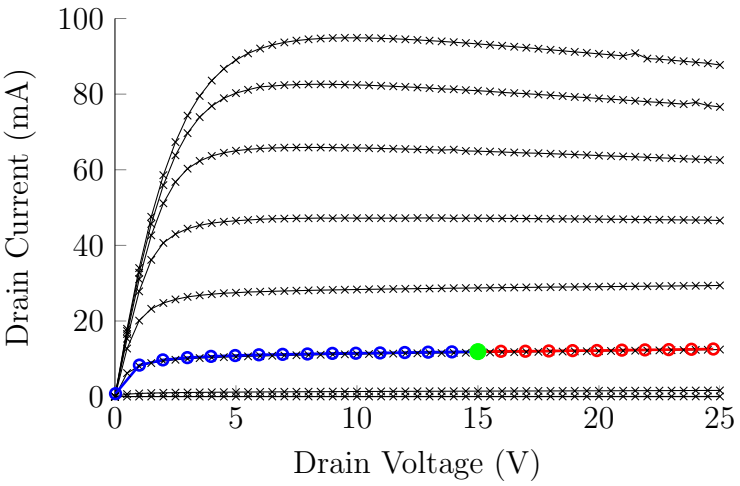


Figure 5.6: LDMOS ($W = 300\,\mu m$): output DC-IV characteristic for V_G from $2.5\,V$ to $6.7\,V$ in steps of $0.6\,V$. Superimposed extracted pulsed characteristic at $V_{G0} = 3.7\,V$ for lower (blue) and higher (red) drain voltages than bias (green).

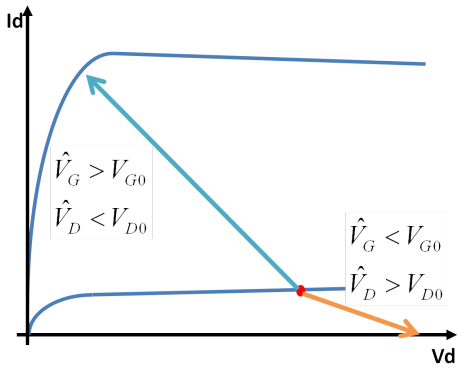


Figure 5.7: Class AB load-line.

As shown in Chapter 4 the state of traps is dependent on both gate and drain voltages although the drain has a bigger influence. To separate the two effects is therefore also interesting to study the drain current transient response with a fixed gate voltage and pulsing only the drain voltage to lower and higher levels with respect to the bias, i.e. $V_G = V_{G0}$, $\hat{V}_D < V_{D0}$ and $\hat{V}_D > V_{D0}$.

The results of this experiment on a AlGaN/GaN HEMT with a gate length of 0.25 µm and a periphery of 2×50 µm are shown[1] in Figures 5.8 and 5.9. The device is biased at $V_{G0} = -2.8\,\text{V}$, $V_{D0} = 15\,\text{V}$ with a corresponding $I_{D0} = 14.5\,\text{mA}$ ($\approx 18\,\%$ of I_{DSS}) and is mounted on a metal carrier to guarantee good thermal conduction. Drain voltage pulses have a period of 1 ms and a width of 10 µs. Comparing the drain current responses for voltage pulses with peak amplitudes from 14 V to 0 V in steps of 1 V in Fig. 5.8 with the current responses for voltage pulses with peak amplitudes from 16 V to 25 V in Fig. 5.9 it is evident how the two behaviour are quite different. No particular transient is observed pulsing to lower voltages while pulsing to higher $\hat{V}_D$ the current has a deep reduction after the pulse with a long recovery transient. This reduction gets bigger as the reached peak voltage increases and at the same time the mean value of the current calculated on the period decreases. This asymmetric behaviour is in agreement with the results presented in Chapter 4 obtained with a different measurement setup and for other AlGaN/GaN devices. In this case, however, longer pulses

[1] In following Figures it has been chosen to always show all (and the same) period to make it easier to visually compare and appreciate the difference of the transient response between different experiments/devices.

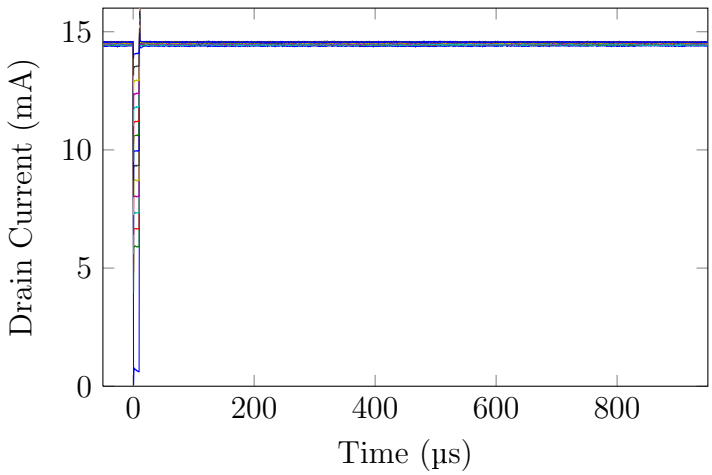


Figure 5.8: GaN HEMT ($W = 2 \times 50\,\mu m$): drain current for drain only voltage pulses with peak amplitudes from 14 V to 0 V in steps of 1 V starting from $V_{G0} = -2.8\,V$, $V_{D0} = 15\,V$. Pulse width 10 µs, period 1 ms.

and periods are used with a stronger excitation of dispersive phenomena which manifest clearly the effect on the drain current. It has also to be noted how this behaviour is totally absent in the case of the LDMOS transistor shown in Fig. 5.5 (red lines) whit similar current and voltage levels.

The asymmetry is explainable supposing again that capture and emission time constants of trap states are very different [8]. Capturing time constants τ_C are very short, probably shorter than ns because, as shown in Chap. 4, even with pulses of the order of 50 ns it is possible to measure a change in the mean value of the drain current. Emission is otherwise much slower with time constants τ_E in the order of tens of µs or even longer as we will see. When a positive drain voltage pulse is applied, the free carriers in the device are captured almost instantaneously; when the pulse excitation is then removed the carriers captured by trap states are emitted back with long time constant as is evident from Fig. 5.9. When otherwise the voltage pulse is negative with respect to the bias, already captured carriers don't have enough time to be emitted. After the pulse, the state of traps is thus the same as the bias state, with no change in the drain current.

The current reduction that is observed inside pulses of Fig. 5.11 can be attributed to self heating. The pulse length of 10 µs could be enough to cause a slight increase of the channel temperature. A similar but opposite behaviour is

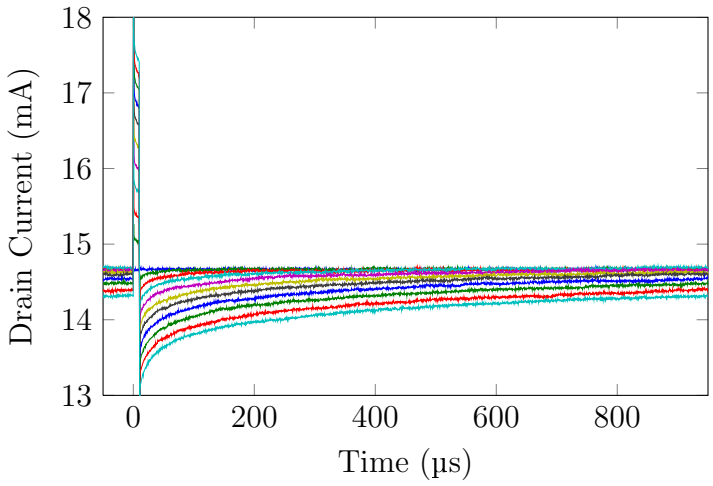


Figure 5.9: GaN HEMT ($W = 2 \times 50\,\mu m$): drain current for drain only voltage pulses with peak amplitudes from 16 V to 25 V in steps of 1 V starting from $V_{G0} = -2.8\,V$, $V_{D0} = 15\,V$. Pulse width 10 µs, period 1 ms.

seen in Fig. 5.10, with a slight increase of the current. In fact, in the pulses of Fig. 5.11 for $\hat{V}_D > V_{D0}$, both the effects of self heating and carriers capture by trap states could be present. The transient current response after pulses is otherwise not explainable by means of thermal effects. These should have a symmetric effect, with a similar but opposite behaviour in the cases of self heating (pulsing to higher voltages) and cooling (pulsing to lower voltages).

To verify further the influence of the drain voltage and to reach also the extremes of the hypothetical class AB load line, other experiments were conducted on the same device. Results obtained starting from the same bias point as before but pulsing simultaneously the gate to 0 V (channel fully open) and the drain to peak amplitudes from 14 V to 0 V are shown in Fig. 5.12: no transient is present after pulses. Pulsing otherwise the gate down to −5.5 V (pinch off) and the drain to peak amplitudes from 16 V to 25 V, the current response presents again a long transient as shown in Fig. 5.13. This proves further how this behaviour is a strong function of the increase in the drain voltage with respect to the bias and how this is not a thermal effect.

The extracted pulsed characteristic for $V_{G0} = -2.8\,V$ is shown in Fig. 5.14 superimposed to the static IV. Dashed lines were added to show the change of slope of the pulsed characteristic on the left and on the right of the bias point. In the same figure is reported also the extracted pulsed characteristic when $\hat{V}_G = 0\,V$

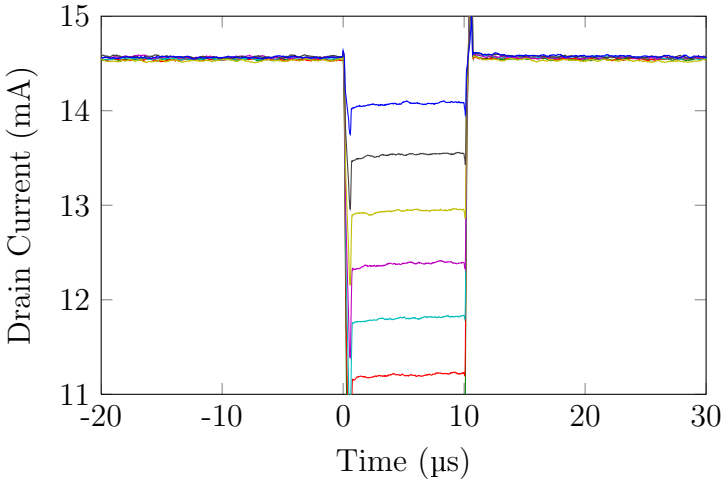


Figure 5.10: GaN HEMT ($W = 2 \times 50\,\mu m$): drain current for drain only voltage pulses with peak amplitudes from 14 V to 9 V in steps of 1 V starting from $V_{G0} = -2.8\,V$, $V_{D0} = 15\,V$. Pulse width 10 µs, period 1 ms. Detail of current response inside pulses.

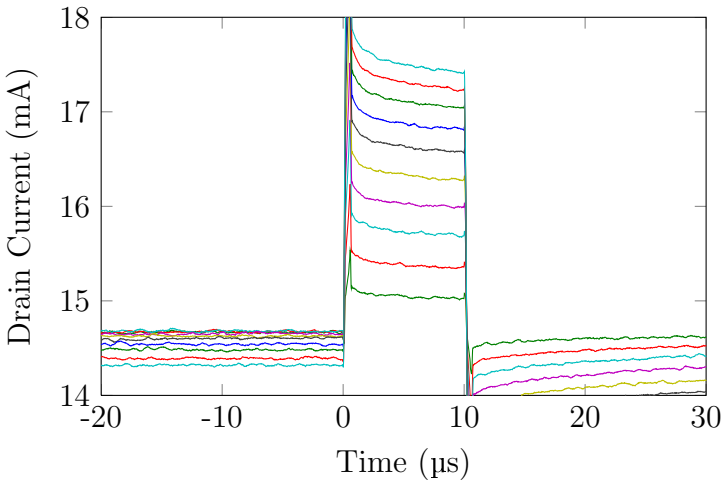


Figure 5.11: GaN HEMT ($W = 2 \times 50\,\mu m$): drain current for drain only voltage pulses with peak amplitudes from 16 V to 25 V in steps of 1 V starting from $V_{G0} = -2.8\,V$, $V_{D0} = 15\,V$. Pulse width 10 µs, period 1 ms. Detail of current response inside pulses.

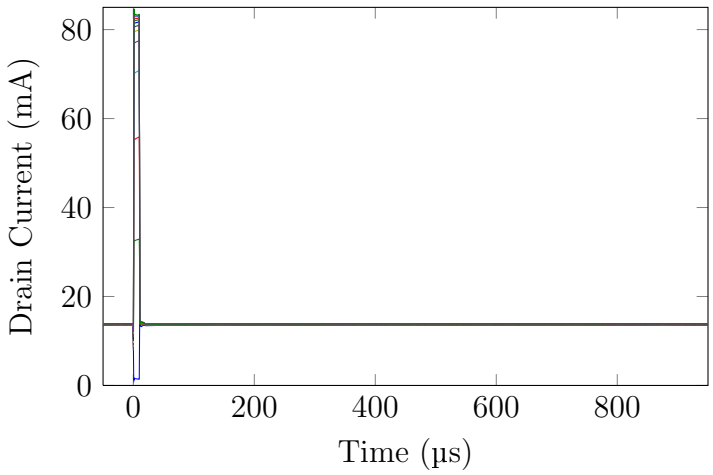


Figure 5.12: GaN HEMT ($W = 2 \times 50\,\mu m$): drain current for gate voltage pulsed to 0 V and drain peak amplitudes from 14 V to 0 V in steps of 1 V starting from $V_{G0} = -2.8\,V$, $V_{D0} = 15\,V$. Pulse width 10 µs, period 1 ms.

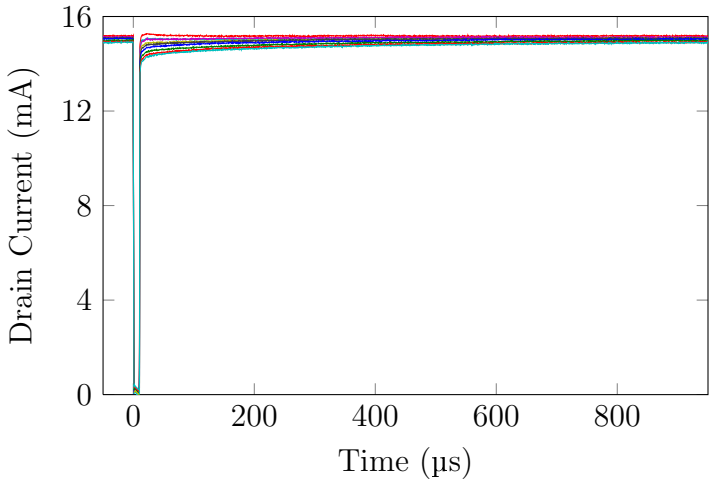


Figure 5.13: GaN HEMT ($W = 2 \times 50\,\mu m$): drain current for gate voltage pulsed to −5.5 V (pinch-off) and drain peak amplitudes from 16 V to 25 V in steps of 1 V starting from $V_{G0} = -2.8\,V$, $V_{D0} = 15\,V$. Pulse width 10 µs, period 1 ms.

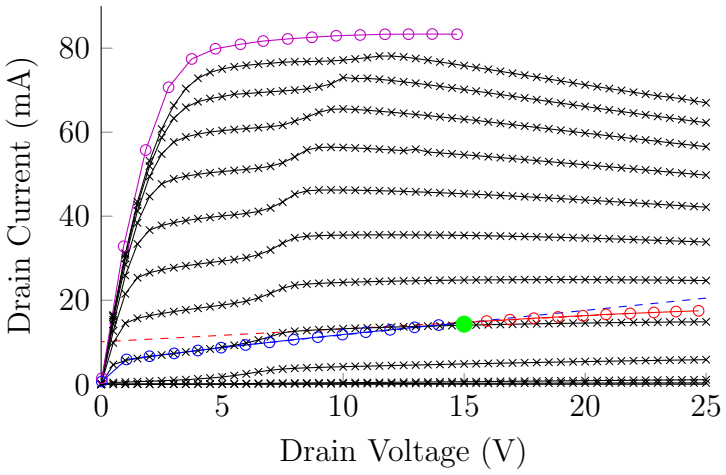


Figure 5.14: GaN HEMT ($W = 2 \times 50\,\mu m$): static DC-IV output characteristic for V_G from 0 V to −4 V in steps of 0.4 V (black lines). Superimposed extracted pulsed characteristic for $V_{G0} = -2.8\,V$: $\hat{V}_D < V_{D0}$ (blue) and $\hat{V}_D > V_{D0}$ (red). Dashed lines to put into evidence change of slope around bias point. Extracted pulsed characteristic for $\hat{V}_G = 0\,V$ and $\hat{V}_D < V_{D0}$ (purple). Bias point $V_{G0} = -2.8\,V$, $V_{D0} = 15\,V$ (green).

and $\hat{V}_D < V_{D0}$ (same measurements shown in Fig. 5.12) and as expected it is higher than the static DC-IV characteristic.

5.5 Transient modelling

In theory more than one time constant, each associated with different trap states, could be present in the current recovery transient after voltage pulses when $V_G = V_{G0}$, $\hat{V}_D > V_{D0}$. However, as a first approximation, the transient can be modelled with a single time constant exponential decay function of the form:

$$I(t) = B - S\,e^{-\frac{t}{\tau}} \tag{5.1}$$

$$= A + S(1 - e^{-\frac{t}{\tau}}) \tag{5.2}$$

where τ is the time constant, B is the final value of the transient (or equivalently the *base* value before the next pulse), S is the *step* in current after the pulse and A is the starting value of the transient ($B = A + S$). Parameters are schematically represented in Fig. 5.15.

An example of measured and fitted transient for different pulses amplitudes

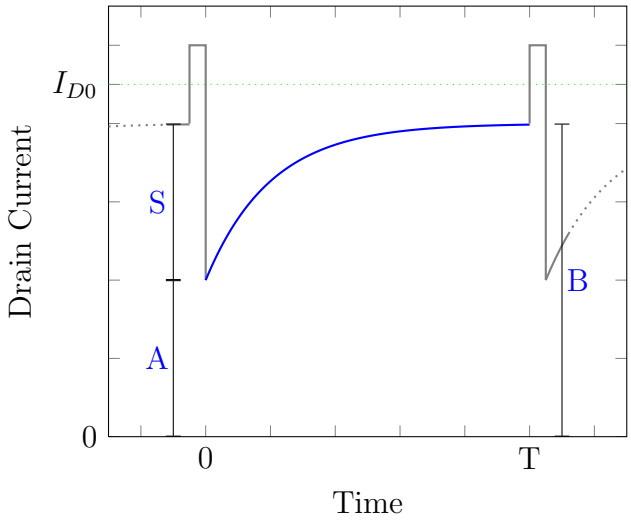


Figure 5.15: Schematic representation of transient current response with fitting parameters.

is reported in Fig. 5.16 for an AlGaN/GaN $2 \times 50\,\mu m$ device. Parameters of equation (5.1) have been extracted through nonlinear least-squares curve fitting optimization. These parameters are a function of the peak voltage amplitude as shown in Fig. 5.17 and the relations seems to be almost linear. In particular, in Fig. 5.17b is shown the percentage change of S in relation to the *base* B current as a function of the peak voltage, this can be approximated as

$$\left.\frac{S}{B}\right|_{\%} = k_{SB}(\hat{V}_D - V_{D0}) \tag{5.3}$$

As the peak voltage amplitude increases, there is a reduction both in the mean value and in the *base* value of the current compared to the bias current I_{D0} without pulses, as shown in Fig. 5.9 and Fig. 5.11. The percentage reduction (Fig. 5.17a) can be approximated as a linear function of the peak voltage:

$$\left.\frac{B}{I_{D0}}\right|_{\%} = 100 + k_{BB}(\hat{V}_D - V_{D0}) \tag{5.4}$$

Also the extracted time constant τ changes in a linear way, as shown in Fig. 5.17c and again can be approximated linearly as

$$\tau = k_{\tau}(\hat{V}_D - V_{D0}) \tag{5.5}$$

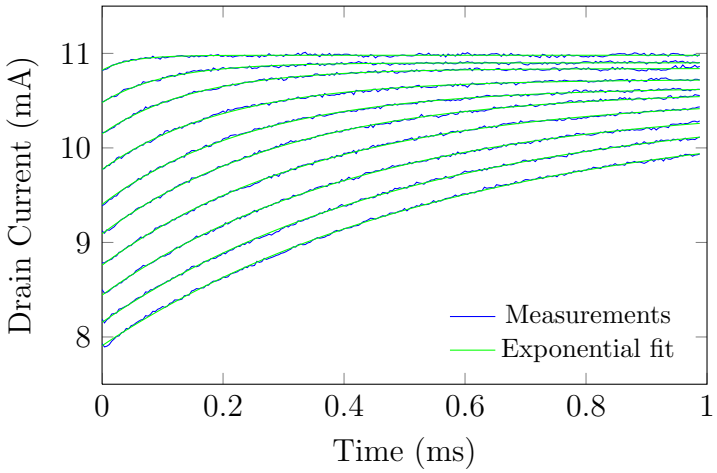


Figure 5.16: commercial GaN device C1 ($4 \times 50\,\mu s$): time-domain current for peak drain voltage amplitudes from 16 V to 25 V in steps of 1 V. Drain bias voltage 15 V. Pulse width 10 µs, period 1 ms.

Parameters k_{BB}, k_{SB} and k_τ, extracted by linear least square fit, are reported in Table 5.1 and the corresponding linear approximations are shown in Fig. 5.17.

k_{BB} (%/V)	k_{SB} (%/V)	k_τ (µs/V)
−0.60	2.43	56.53

Table 5.1: Extracted parameters for linear approximation of peak drain voltage dependence of exponential fitting parameters.

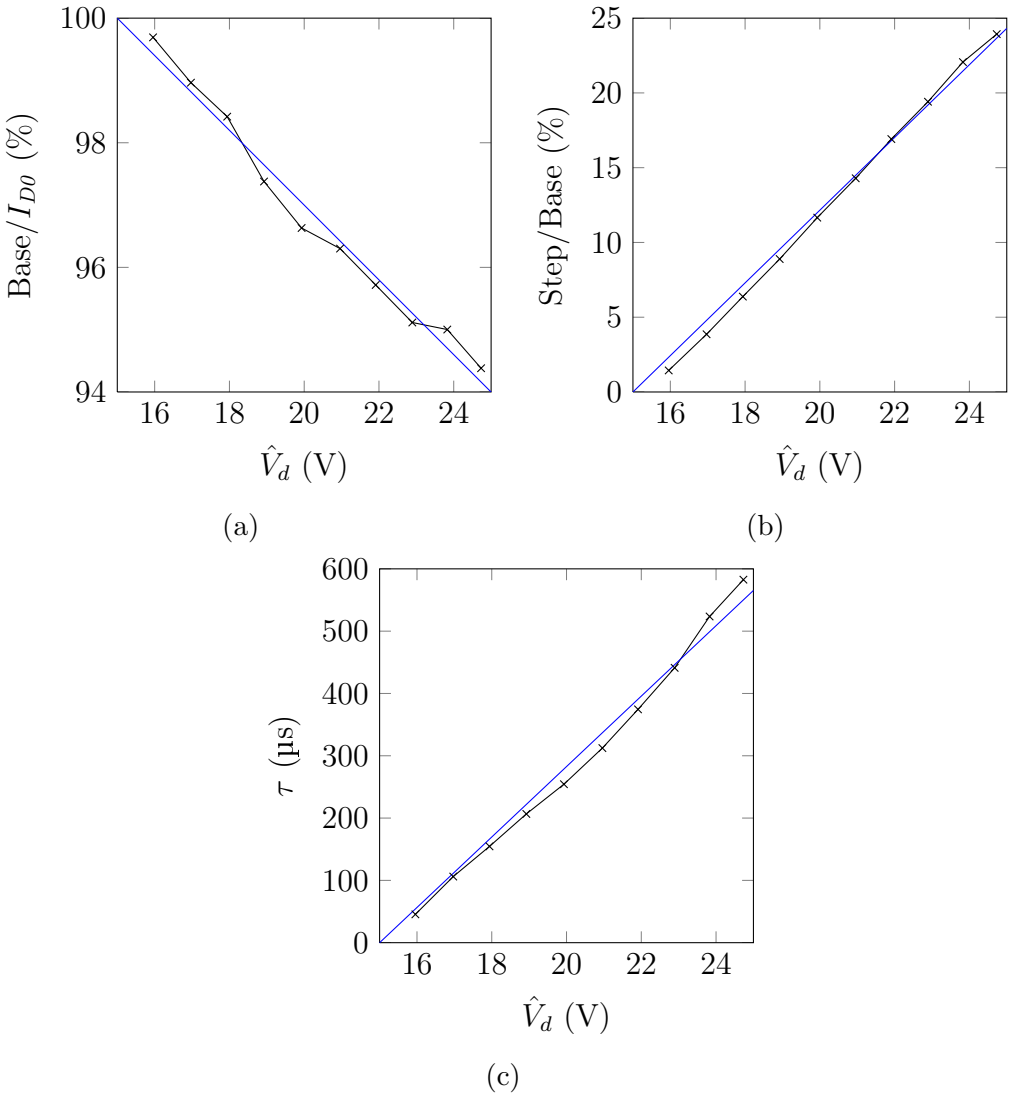


Figure 5.17: Extracted parameters

5.6 Devices comparison

Transient current responses similar to the ones shown in the previous Section have been verified on many different GaN devices. In this Section, the results of a comparison of six AlGaN/GaN HEMT devices of same gate length (0.25 µm) and periphery (2×50 µm) is presented. All the transistors are from the Chalmers University foundry [9] but are from different generations and therefore there is some difference in used materials and processing steps. All the devices are passivated. The time-domain current responses of the six devices are shown in Fig. 5.18 for peak drain voltage amplitudes from 16 V up to 25 V, starting from a 15 V drain bias voltage. Gate voltage is setted in order to have $I_{D0} \approx 15\,\%$ of I_{DSS}. Devices characteristics and bias points are reported in Table 5.2.

With this characterization it is possible to extract many informations. For instance, looking at the amplitude inside pulses it is possible to infer that device D1 has a higher output conductance.

The same experiment has also been repeated for an AlGaN/GaN HEMT device (0.25 µm, 4×50 µm) from a commercial vendor and results are shown in Fig. 5.19. The current reduction after the pulse is even bigger in this case with a slower recovery of the current.

To compare devices, the transient of the current after pulses has been fitted with an exponential decay function for all peak drain voltage amplitudes as described in Section 5.5. Extracted parameters as a function of the drain voltage are shown in Fig. 5.20. Devices D1, D2, D3, D4 and D5 have similar time constants while

Device	Peif.(µm)	I_{DSS}(mA)	$V_{p.off}$(V)	V_{G0}(V)	V_{D0}(V)	I_{D0}(mA)	$\%I_{DSS}$
D1	2×50	80	−3.4	−2.8	15	14.8	18
D2	2×50	85	−3.8	−3.2	15	11.8	14
D3	2×50	78	−2.8	−2.0	15	10.0	13
D4	2×50	66	−3.0	−2.3	15	8.5	13
D5	2×50	43	−2.2	−1.6	15	5.8	13
D6	2×50	85	−3.4	−2.8	15	11.1	13
C1	4×50	210	−4.0	−3.2	15	30.0	14

Table 5.2: GaN devices comparison: characteristics and starting bias points for pulsed characterization.

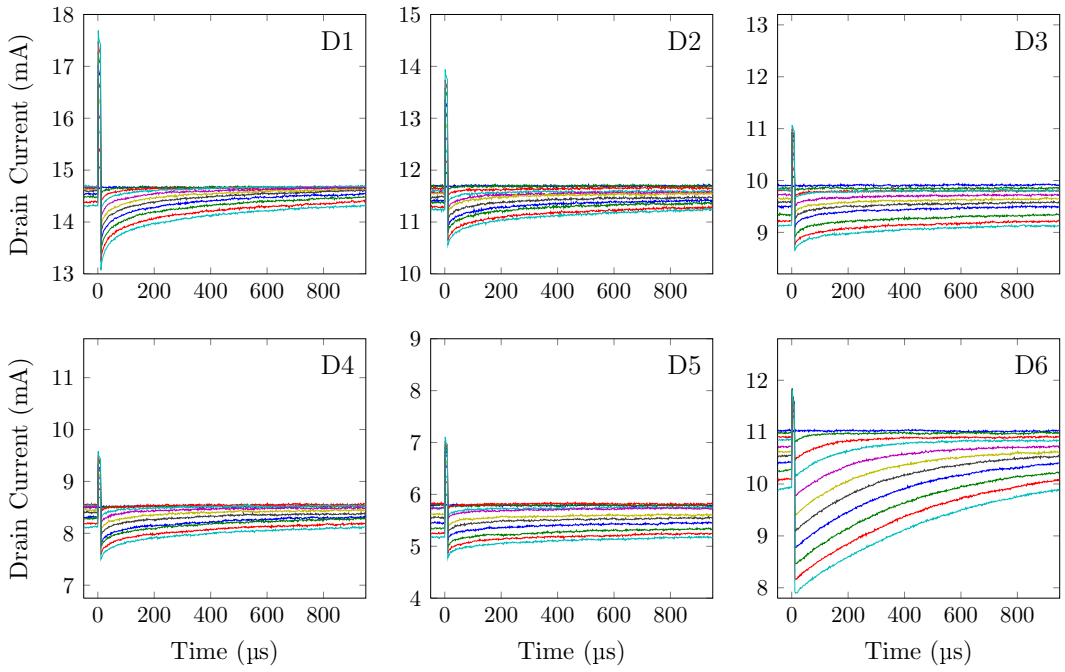


Figure 5.18: GaN devices (D1 to D6) comparison: time-domain current for peak drain voltage amplitudes from 16 V to 25 V in steps of 1 V. Drain bias voltage 15 V. Pulse width 10 µs, period 1 ms.

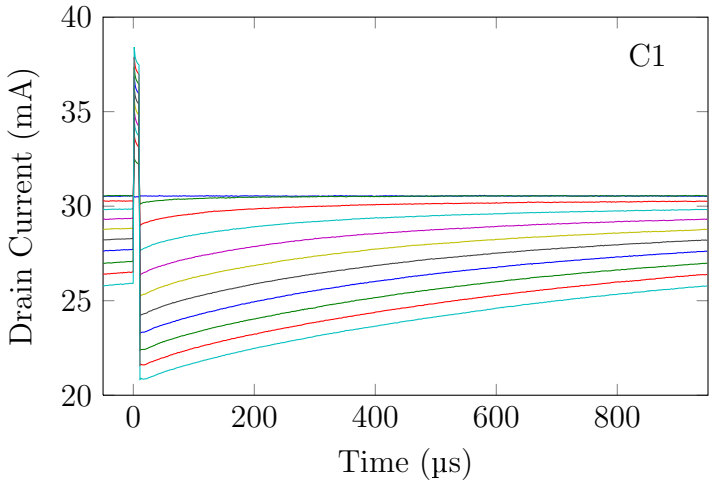


Figure 5.19: commercial GaN device C1 (4×50 µs): time-domain current for peak drain voltage amplitudes from 16 V to 25 V in steps of 1 V. Drain bias voltage 15 V. Pulse width 10 µs, period 1 ms.

D6 and C1 present clearly much longer time constants. Analogous considerations can be made for the step reduction of the current after voltage pulses. In this case devices C1 and D6 show a considerable reduction, up to 25 % of the drain current. This could be explained by a higher density of trap states. Instead, it has been verified that the reduction of the *base* current compared to the static DC bias value (Fig. 5.20a) is mainly influenced by the period of the pulsed voltage excitation used. This has been done comparing results of experiments conducted on the same device but with different temporal parameters for drain voltage pulses. In fact, if the period is long enough, the current can recover almost completely to the bias value. This, however, shows how in addition to a dynamic variation, also a shift on the current, that depends on the dynamics of applied signals, is present.

It has also to be noted that for some devices a single time constant function is not enough to model accurately the transient. In these cases could be interesting to try to adopt more advanced methods and algorithms for the fitting of multiple time constants exponential decay functions [10]. In principle by applying inverse Laplace transform methods, similarly to what is done in some Deep Level Transient Spectroscopy techniques [11], could also be possible to extract a continuous spectrum of time constants.

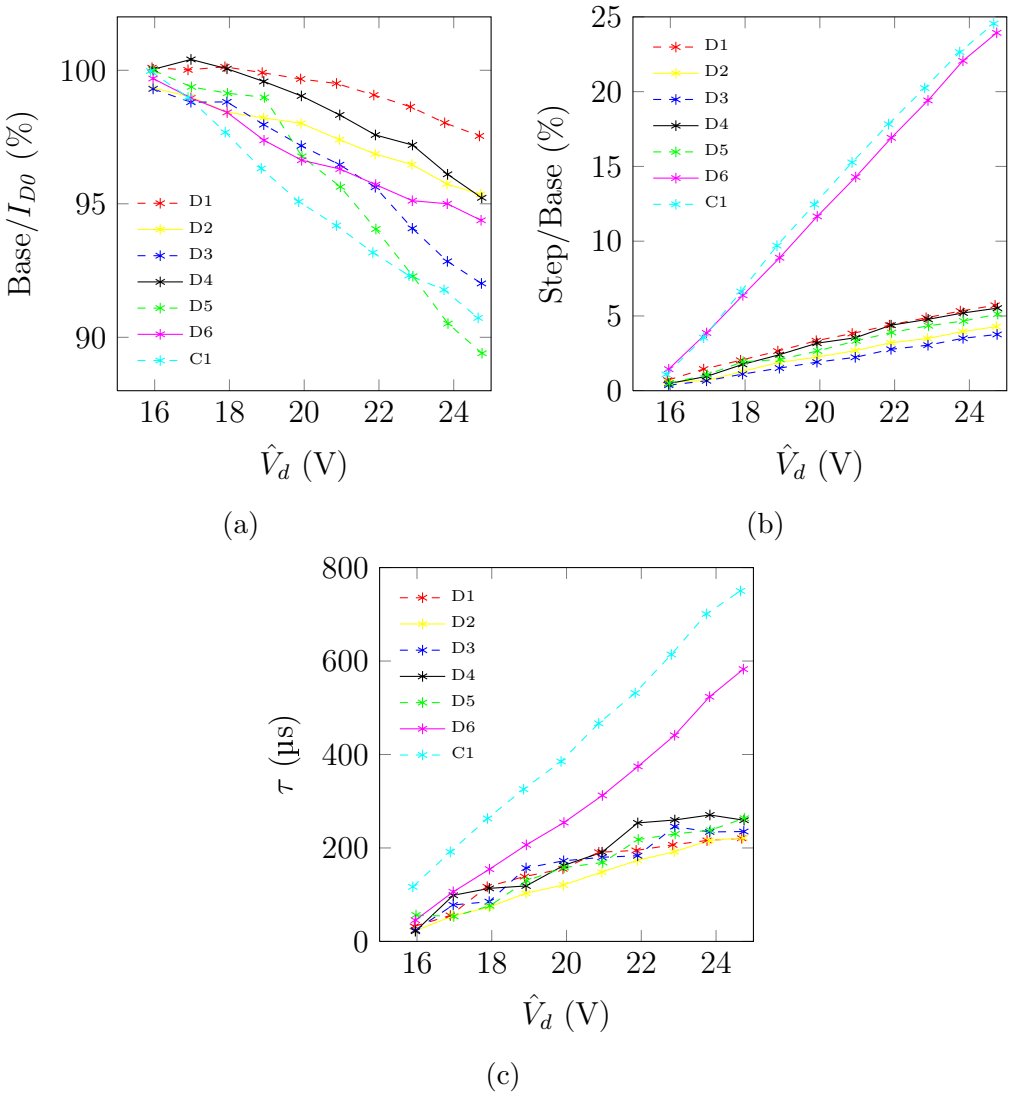


Figure 5.20: GaN devices (D1-D6,C1) comparison: extracted parameters as a function of the peak drain voltage.

5.7 Pulsed RF characterization

The long term memory effects measured on the drain current, as shown in previous Sections, are affecting also RF performances. To demonstrate this a pulsed RF characterization has been carried out by means of a large signal measurement setup developed at Chalmers University of Technology [12]. The idea is to apply at the input of the device a pulsed modulated RF signal with temporal parameters (i.e. T and τ) similar to the ones used for the pulsed IV characterization and to measure the time-domain gain and output power. This allows to verify if also these present some memory effect.

The schematic of the setup, that is based on a MT4463 Maury Microwave/NMDG Large Signal Network Analyzer (LSNA), is shown in Fig. 5.21. The LSNA allows to measure harmonics of incident and reflected waves at the DUT reference plane, from 600 MHz up to 50 GHz. Thanks to the calibration both the absolute amplitude and phase relation of waves are known [13]. When used in modulation mode, the LSNA is also capable of measuring modulated signals with a periodic modulation. Depending on the instrument settings a number of sideband frequencies are measured around each harmonic of the fundamental which corresponds to the carrier frequency of the test signal. From incident and reflected waves is then possible to directly calculate the input and output power and thus the gain in the time domain for the whole length of a modulation period.

The amplitude of the source RF carrier is modulated by a vector modulator which is synchronized with the LSNA sampler [12] and is controlled in similar way

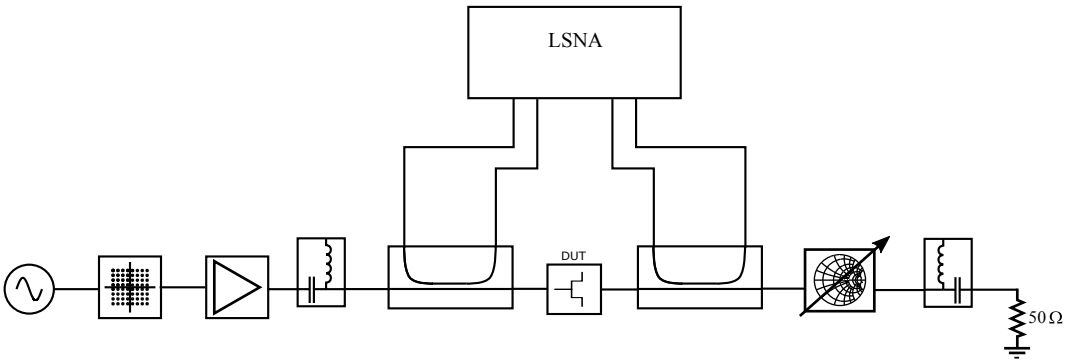


Figure 5.21: Block diagram of pulsed RF measurement setup.

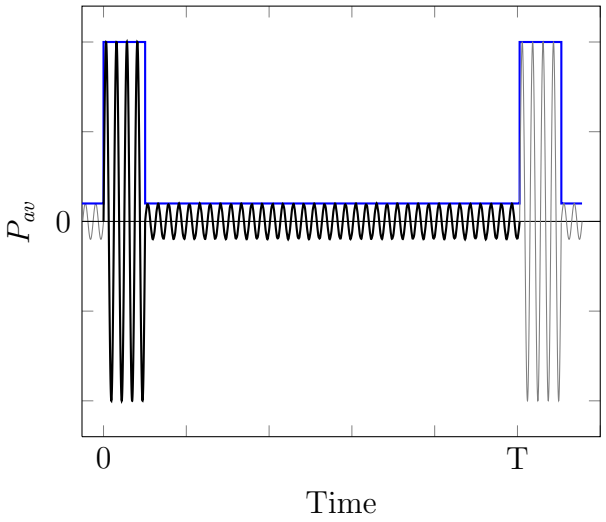


Figure 5.22: Schematic representation of pulsed input signal. Envelope in blue.

as done in [14]. The pulsed modulated signal is then amplified and applied to the gate of the device. A schematic representation of the signal that is pulsed between a low and high power is shown in Fig. 5.22. On the output a passive tuner is used to present an opportune load impedance to the device at the carrier frequency. Before the measurement the tuner is characterized with the LSNA replacing the DUT with a Thru. During the pulsed characterization the current on the DC path of the bias tee is also monitored with a wideband current probe connected to an oscilloscope.

To reproduce realistic working conditions of a class-AB power amplifier an opportune bias point is selected and the load impedance is chosen for maximum output power. This is done performing a load-pull measurement with a CW signal at the carrier frequency.

A commercial AlGaN/GaN device with a periphery of $8 \times 50\,\mu m$ has been characterized in this way. The selected bias point is $V_{D0} = 20\,V$, $V_{G0} = -2.3\,V$, with a corresponding quiescent current $I_{D0} = 44\,mA$ ($\approx 15\,\%$ of $I_{DSS} = 288\,mA$). The optimum reflection coefficient for maximum output power has been found to be $G_L = 0.4 + j0.4$ which correspond to the load impedance $Z_L = 65.64 + j77$. In Fig. 5.23 is reported the measured static characteristic of the device with the loadline corresponding to $\Re(Z_L)$ and the selected bias point.

The carrier frequency is 4 GHz and the pulse modulation has a period $T = 1\,ms$

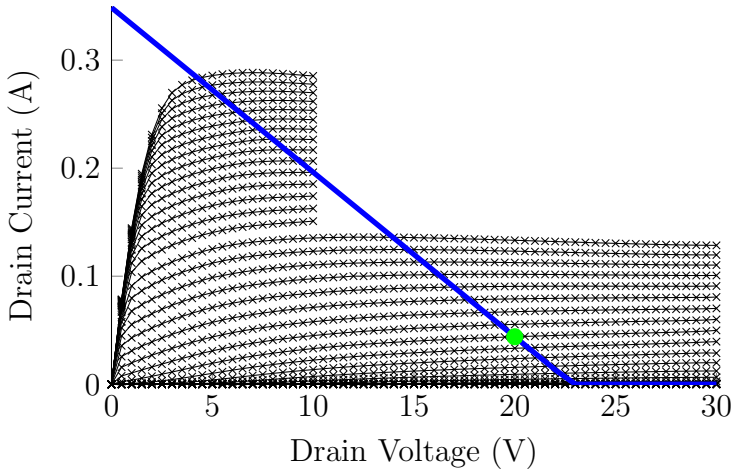


Figure 5.23: Commercial GaN device ($8 \times 50\,\mu s$): measured DC-IV characteristic (black lines) and ideal resistive load line for maximum output power as determined with load-pull measurements (blue). Class-AB bias point used for pulsed RF characterization (green).

and width $\tau = 10\,\mu s$ (duty cycle $\delta = 1\,\%$). In Fig. 5.24a is shown the time domain source available power calculated from the $a_1(t)$ wave as

$$P_{av}(dBm) = 10 \log_{10} \left(\frac{|a_1|^2}{100} \right) + 30 \tag{5.6}$$

The measured time domain gain and drain current are shown in Fig. 5.24b and Fig. 5.24c respectively. It is evident how in this case both the RF gain and the drain current present a slow transient after the RF pulse. Inside the pulse the gain is lower due to output power compression. The drain current inside the pulse is instead higher, this is due to AC to DC nonlinear conversion. These measurements confirm that dispersive effects due to traps manifest as long term memory also on the RF device performances. This could be especially critical with high PAPR burst modulated signals where this memory effect could lead to added distortion and inter-symbol-interference.

5.8 Conclusions

In this Chapter, a transient drain current characterization setup has been presented with some validation measurements on resistors and LDMOS device. The setup

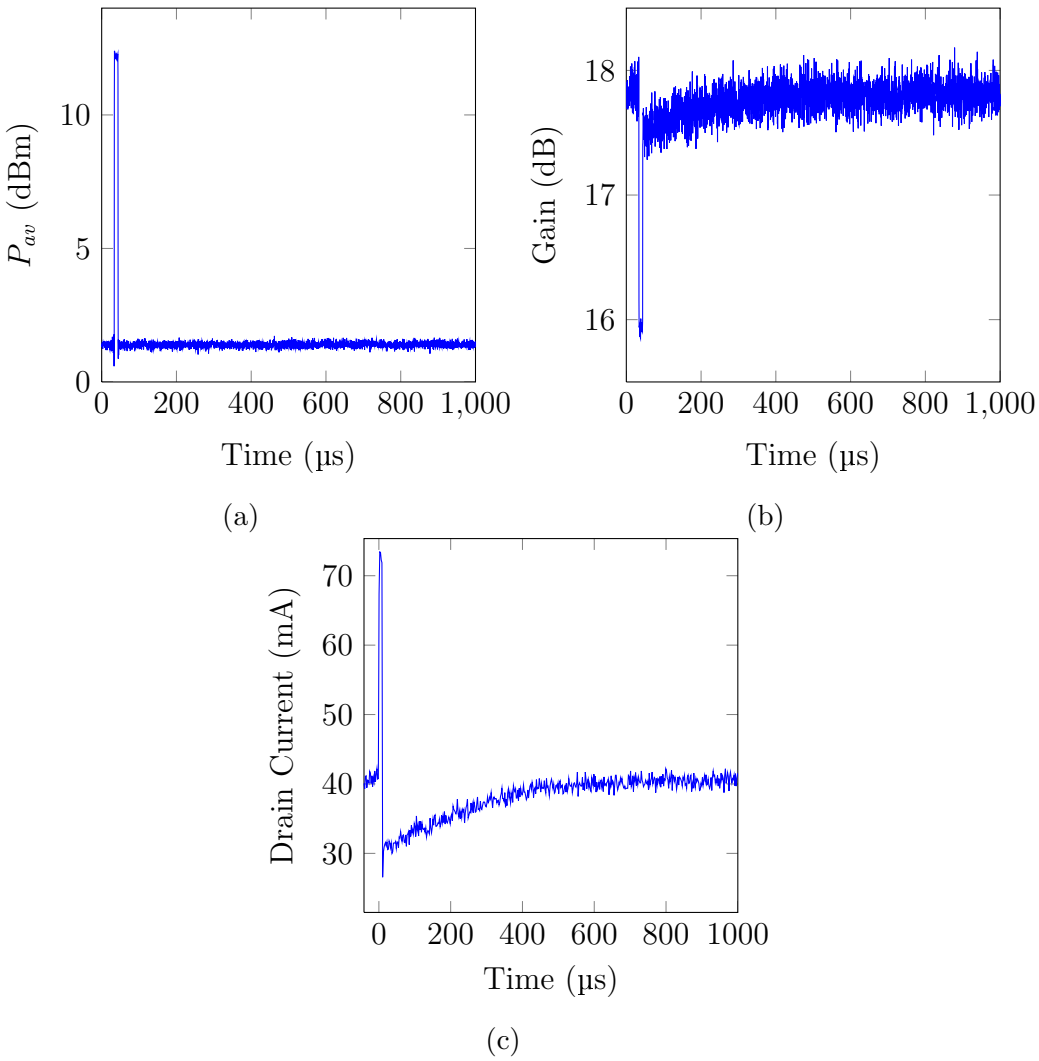


Figure 5.24: AlGaN/GaN HEMT: time-domain input available power envelope (a), gain (b) and drain current (c) for a period of periodic pulsed RF excitation.

allows to study an to compare traps effects on devices and has been used to characterize the transient response of GaN HEMTs to pulsed voltages excitation. It has been shown that pulsing from a class-AB bias point, the dynamic behaviour of the current is highly dependent on the direction of applied pulses. The asymmetry of the effect is due to the asymmetry in capture and emission time constants of the traps. These traps are probably located in the GaN buffer or under the gate but not on the surface being all measured devices passivated. The effect is present also in commercial AlGaN/GaN devices. A simple exponential model of the transient after the pulse excitation is proposed. The fitting of measurements for

different pulse voltage amplitudes shows how the time constant and the reduction of current after pulses are linearly dependent on the peak drain voltage. The method can be used to compare different devices and allow to extract parameters that could be useful for the development of advanced models of devices. Finally, a pulsed RF characterization setup has been presented. The setup has been used to demonstrate that also a pulsed RF excitation is able to activate these traps with detrimental effects on RF performances. In fact, traps introduce long-term memory effects that are an added source of distortion for power amplifiers. The characterization presented here can be useful for the development of behavioural models to be used in digital predistortion.

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Chapter 6

Conclusions

During the Ph.D. course I had the opportunity of carrying out research on different but strongly linked topics; from device characterization, through the development of instruments and models, to the design of circuits. This thesis tries to summarize the work done during these three years.

The properties and the advantages offered by the AlGaN/GaN HEMT technology have been reviewed. The design and the measurements of some GaN-based MMIC high power amplifiers have been presented. At high frequency the technology is able to offer an order of magnitude higher RF power density, higher efficiency and bandwidth than other semiconductor technologies.

Despite this, the technology is not yet fully mature. Some problems related to dispersive phenomena due to traps and thermal effects are still present. A better understanding of these phenomena and how these can impact on performances in real applications is needed. Some of these issues have been addressed through new characterization techniques and instruments.

A nonlinear thermal resistance model and characterization procedure that involves only multi-bias small-signal S-parameter and DC I/V measurements at different base plate temperatures has been proposed.

Pulsed characteristics of devices are at the basis of many compact models used for the design of high frequency nonlinear circuits. A new fully-calibrated pulsed measurement setup that enables the use of very short pulses has been presented and described in detail. The setup was used to characterize GaAs and GaN devices and allowed to show the nonlinear and asymmetric behaviour of traps.

The long-term memory effects of traps in GaN HEMTs can be an added source

of distortion for wideband modulated signals. The characterization of the transient response of the drain current to pulsed voltages excitations can give new insight into trapping and detrapping mechanisms. To this aim a measurement setup has been developed. Obtained results show clearly that emission time constants of the involved traps change with the peak of applied pulses. It has also been demonstrated that these traps can impact RF performances.

These techniques can be used both for the development of more accurate models of devices and to compare different technologies, materials and foundry processes with the aim of further improving the technology.

6.1 Publications

The work presented in this thesis is based on the following publications and on the research conducted as a visiting Ph.D. student at the *Department of Microtechnology and Nanoscience* at *Chalmers University of Technology* - Sweden.

- A. Santarelli, R. Cignani, V. Di Giacomo, S. D'Angelo, D. Niessen, and F. Filicori, "Large-signal characterization of GaN-based transistors for accurate nonlinear modelling of dispersive effects," in *Integrated Nonlinear Microwave and Millimeter-Wave Circuits (INMMIC), 2010 Workshop on*, Apr. 2010, pp. 115–118

- A. Santarelli, V. Di Giacomo, R. Cignani, S. D"Angelo, D. Niessen, and F. Filicori, "Nonlinear thermal resistance characterization for compact electrothermal GaN HEMT modelling," in *Microwave Integrated Circuits Conference (EuMIC), 2010 European*, Sep. 2010, pp. 82–85

- A. Santarelli, R. Cignani, D. Niessen, S. D"Angelo, and F. Filicori, "Electrothermal characterization and compact modelling of GaN HEMTs for microwave applications," in *Riunione Annuale Gruppo Elettronica, Trani*, Jul. 6–8, 2011

- A. Santarelli, R. Cignani, D. Niessen, S. D'Angelo, P. A. Traverso, and F. Filicori, "Characterization of GaN and GaAs FETs through a new pulsed measurement system," in *Microwave Integrated Circuits Conference (EuMIC), 2011 European*, Oct. 2011, pp. 1–4

- A. Santarelli, R. Cignani, D. Niessen, P. A. Traverso, and F. Filicori, "New pulsed measurement setup for GaN and GaAs FETs characterization," *International Journal of Microwave and Wireless Technologies*, vol. 4, pp. 387–397, 5 2012

- C. Florian, R. Cignani, D. Niessen, and A. Santarelli, "A C-Band AlGaN-GaN MMIC HPA for SAR," *Microwave and Wireless Components Letters, IEEE*, vol. 22, no. 9, pp. 471–473, Sep. 2012

- A. Santarelli, R. Cignani, G. Gibiino, D. Niessen, P. A. Traverso, C. Florian, C. Lanzieri, A. Nanni, D. Schreurs, and F. Filicori, "Nonlinear charge trapping effects on pulsed I/V characteristics of gan FETs," Microwave Integrated Circuits Conference (EuMIC), 2011 European, 2013, to be published