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DESIGN METHODOLOGIES OF MICROWAVE INTEGRATED CIRCUITS FOR SATELLITE TELECOMMUNICATIONS

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I would like to explicitly thank Prof. Vito Monaco, which believed in me and, with me, in the necessity to perform, even more today, that "*Technological Transfer*", between Universities and Industries, often acclaimed but seldom applied.

INTRODUCTION

The running innovation processes of the microwave transistor technologies, used in the implementation of microwave circuits, have to be supported by the study and development of proper design methodologies which, depending on the applications, will fully exploit the technology potentialities. After the choice of the technology to be used in the particular application, the circuit designer has few degrees of freedom when carrying out his design; in the most cases, due to the technological constrains, all the foundries develop and provide customized processes optimized for a specific performance such as power, low-noise, linearity, broadband etc. For these reasons circuit design is always a “compromise”, an investigation for the best solution to reach a trade off between the desired performances.

This approach becomes crucial in the design of microwave systems to be used in satellite applications; the tight space constraints impose to reach the best performances under proper electrical and thermal de-rated conditions, respect to the maximum ratings provided by the used technology, in order to ensure adequate levels of reliability. In particular this work is about one of the most critical components in the front-end of a satellite antenna, the High Power Amplifier (*HPA*). The HPA is the main power dissipation source and so the element which mostly engrave on space, weight and cost of telecommunication apparatus; it is clear from the above reasons that design strategies addressing optimization of power density, efficiency and reliability are of major concern.

Many transactions and publications demonstrate different methods for the design of power amplifiers, highlighting the availability to obtain very good levels of output power, efficiency and gain. Starting from existing knowledge, the target of the research activities summarized in this dissertation was to develop a design methodology capable optimize power amplifier performances complying all the constraints imposed by the space applications, tacking into account the thermal behaviour in the same manner of the power and the efficiency.

After a reminder of the existing theories about the power amplifier design, in the first section of this work, the effectiveness of the methodology based on the accurate control of the dynamic *Load Line* and her shaping will be described, explaining all steps in the design of two different kinds of high power amplifiers. Considering the trade-off between the main performances and reliability issues as the target of the design activity, we will demonstrate that the expected results could be obtained working on the characteristics of the Load Line at the intrinsic terminals of the selected active device.

The methodology proposed in this first part is based on the assumption that designer has the availability of an accurate electrical model of the device; the variety of publications about this argument demonstrates that it is so difficult to carry out a CAD model capable to taking into account all the non-ideal phenomena which occur when the amplifier operates at such high frequency and power levels. For that, especially for the emerging technology of Gallium Nitride (GaN), in the second section a new approach for power amplifier design will be described, basing on the experimental characterization of the intrinsic Load Line by means of a low frequency high power measurements bench.

Thanks to the possibility to develop my Ph.D. in an academic spin-off, *MEC – Microwave Electronics for Communications*, the results of this activity has been applied to important research programs requested by space agencies, with the aim support the technological transfer from universities to industrial world and to promote a science-based entrepreneurship. For these reasons the proposed design methodology will be explained basing on many experimental results.

Chapter 1

Theory of microwave Power Amplifier

This chapter is to summarize the fundamental aspects of the theories that represent, up today, the pillar of power amplifier design techniques. Power amplifier design is a key aspect in order to meet the severe performance (e.g., efficiency, reliability) required for modern micro- and millimeter-wave systems. Such a kind of circuit is usually designed by exploiting a mix of three different approaches [1-2]: Cripps load-line theory, load-pull measurements and iterative harmonic-balance analyses based on nonlinear models of electron devices (ED).

It is worth to notice that the sections below are not just a bibliography research about the themes discussed in this thesis, but the main purpose is to highlight the starting basis of the new proposed methods in order to put in evidence, in the next chapters, the comparison with them.

1.1 Elementary Load Line Theory

With the coming of Solid State Power Amplifiers (*SSPA*) a lot of design techniques were be developed focusing on their particular aspects and performances, basing on the different kind of applications. So, various approaches could be applied if the targets are high power, high linearity, high efficiency or low noise amplifiers, but we can consider all of them as an evolution of the elementary Load Line theory developed by Cripps [3].

The starting point of this analysis is a heavily idealized device model, shown in *Figure 1.1a*, based on the assumption that the main cause of non linear behaviour inside the active device is the voltage-controlled current source, with zero output conductance and zero turn-on (or “knee”), representing the active channel modulated by the applied gate voltage. This reasonable assumption is combined with the effect of device’s hard limitations, including breakdown, forward gate conduction and current saturation effects; for that, the transconductance is linear except for its strong nonlinearities

represented by pinchoff (for input voltage below the threshold V_t) and hard saturation, at I_{max} (*Figure 1.1b*). A key feature of this analysis is that the device is never allowed to breach those limits of linear operation; in this sense, the analysis is valid up to, but not beyond, the onset of gain compression. Other nonlinear elements of the active device, like the reactive ones (namely C_{gs} and C_{gd}), are considered linear; moreover the effects of feedback elements and parasitics are ignored.

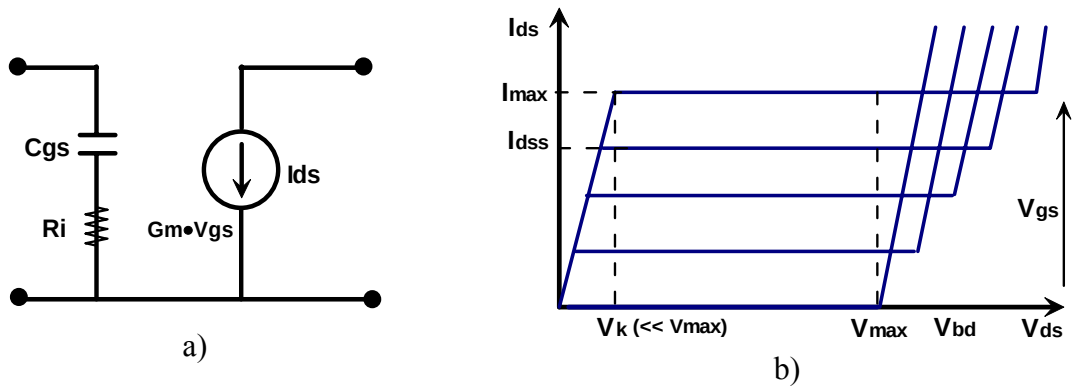


Figure 1.1 - Simplified Model of the active device (a); Output characteristic of non linear device included in the description of the controlled source (b).

Assuming to operate in the simple case of a Class A amplifier, the quiescent bias point is fixed by the (1.1) and so, under the assumption of negligible knee voltage, it is half the V_{max}; the load line theory says that to deliver the maximum power to the load both current ($0 \rightarrow I_{max}$) and voltage ($0 \rightarrow V_{max}$) swings must be maximized, staying up to their linear range (*Figure 1.2*) [4]. Clearly, the load line resistor in this optimum power matched condition has the value indicated in the (1.2).

$$\text{Bias Point}\begin{cases} V_{DC} = \dfrac{V_{\max} - V_k}{2} \approx \dfrac{V_{\max}}{2} \\ \mathrm{I_{DC}} = \dfrac{\mathrm{I_{max}}}{2} \end{cases} \qquad (1.1)$$

$$R_{opt} = V_{dc} / (I_{\max}/2) = V_{dc} / I_{dc} \qquad (1.2)$$

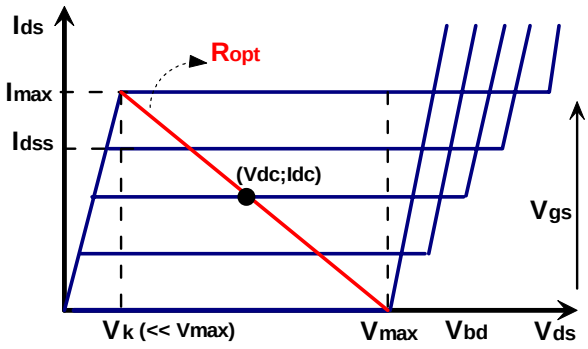


Figure 1.2 - Load Line in the ideal optimum power-matched condition

Applying their standard definitions to this idealized treatment, the output power and the efficiency assume the value below:

$$P_{opt} = \frac{1}{2} V_{dc} \cdot I_{dc} \quad (1.3) \qquad \eta = 100 \cdot \frac{P_{dc}}{P_{opt}} = 100 \cdot \frac{1}{2} \frac{V_{dc} \cdot I_{dc}}{V_{dc} \cdot I_{dc}} = 50\% \quad (1.4)$$

It is clear that the ideal operating condition presented above is so far to be applied in a realistic power amplifier design, but we can consider it like a starting point for a more realistic treatment of the problem.

From all design amplifier theories is trivial that to enhance the efficiency the first step is to bias the active device to a low quiescent current and to allow the RF signal to swing the device into conduction. But the merely reduction of the conduction angle of an RF power amplifier is not sufficient in itself to give an useful improvement in efficiency; moreover it is also necessary to increase the drive level substantially from the Class A condition and to provide suitable impedance terminations at harmonics of the signal frequency, that become very important when the strong non linear regions are involved.

Defining α as the entire angle of conduction in the RF cycle, including the equal contributions on either side of the zero time point, *Figure 1.3* shows as the reduction affects the current waveform, where, basing on the definition, the current cut-off points are at $\pm\alpha/2$.

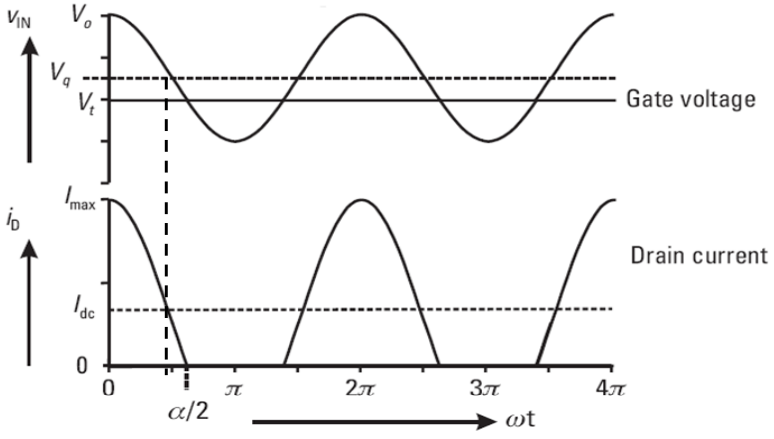


Figure 1.3 - Reduced conduction angle current waveform.

From the current waveform is intuitive that a reduction of the conduction angle implies a decreasing of the current mean component, or dc supply. *Table 1.1* shows the definition of the classical modes of operation, in terms of quiescent bias point and conduction angle.

Mode	Bias Point (Vq)	Quiescent current	Conduction angle
A	0.5	0.5	2π
AB	0 – 0.5	0 – 0.5	π - 2π
B	0	0	π
C	< 0	0	0 - π

Table 1.1 - Classical Modes of Operation; Vq and Iq are normalized considering the threshold V_t=0 and the maximum voltage V_0 =1.

To understand what happen to the fundamental component and to the harmonics is needful to perform the Fourier analysis of the RF current waveform, which can be written as indicated in the follows.

$$i_d(\theta) = \begin{cases} I_q + I_{pk} \cdot \cos\theta & -\alpha/2 < \theta < \alpha/2 \\ 0 & -\pi < \theta < -\alpha/2;\ -\alpha/2 < \theta < \pi \end{cases}$$

$$\cos(\alpha/2) = -\left(\frac{I_q}{I_{pk}}\right) \text{ and } I_{pk} = I_{\max} - I_q \qquad (1.5)$$

$$i_d(\theta) = \frac{I_{\max}}{1-\cos(\alpha/2)}\left[\cos\theta - \cos(\alpha/2)\right]$$

From the (1.5), integrating in the conduction period, the DC component and the magnitude of the *n*th harmonic of the drain current can be expressed like the (1.6) and the (1.7), while the DC and the fundamental components are determined in (1.8) and (1.9).

$$I_{dc} = \frac{1}{2\pi}\int_{-\alpha/2}^{\alpha/2} \frac{I_{\max}}{1-\cos(\alpha/2)}\left[\cos\theta - \cos(\alpha/2)\right]d\theta \qquad (1.6)$$

$$I_n = \frac{1}{\pi}\int_{-\alpha/2}^{\alpha/2} \frac{I_{\max}}{1-\cos(\alpha/2)}\left[\cos\theta - \cos(\alpha/2)\right]\cdot\cos n\theta\, d\theta \qquad (1.7)$$

$$I_{dc} = \frac{I_{\max}}{2\pi}\frac{2\sin(\alpha/2) - \alpha\cos(\alpha/2)}{1-\cos(\alpha/2)} \qquad (1.8)$$ *Result of (1.6) for DC component*

$$I_1 = \frac{I_{\max}}{2\pi}\frac{\alpha - \sin\alpha}{1-\cos(\alpha/2)} \qquad (1.9)$$ *Result of (1.7) for the fundamental frequency*

The results from the evaluation of these integrals up to n=5 are shown in *Figure 1.4*, where we can observe how the dc component decreases monotonically as the conduction angle is reduced, while, affecting the strong nonlinearities, there is a growth of the harmonic components.

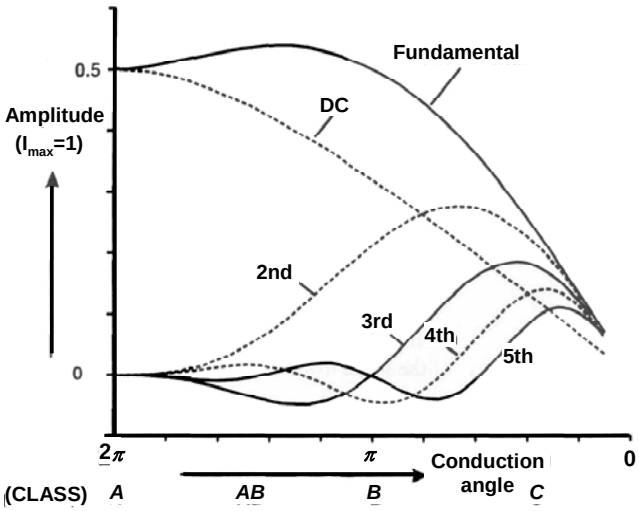


Figure 1.4 - Fourier analysis of reduced conduction angle mode

Just observing the graph above you can see that the reduction of the conduction angle from 2π (class A) to about π (class B) implies a reduction of the DC supply power while the RF fundamental component remains essentially the same, with a consequent improvement of the amplifier efficiency. Comparing the current values of both A and B classes, from the (1.8) and (1.9), we obtain that the efficiency raises form the 50% to the 78.5% (1.10).

$$I_{dc}(ClassA) = I_{dc}(2\pi) = \frac{I_{\max}}{2} = I_1(ClassA)$$

$$I_{dc}(ClassB) = I_{dc}(\pi) = \frac{I_{\max}}{\pi} \qquad I_1(ClassB) = \frac{I_{\max}}{2}$$

$$\frac{\eta_A}{\eta_B} = \frac{I_{dc}(B)}{I_{dc}(A)} = \frac{2}{\pi} \Rightarrow \eta_B = \frac{\pi}{2}\cdot\eta_A = \frac{\pi}{4} = 78.5\% \qquad (1.10)$$

To complete the analysis about the effect of the reduction of the conduction angle on the amplifier performance we can see that for conduction angles lower than π, corresponding to class C operation, the dc continues to drop, but the fundamental

component of current also starts to drop below its class A level. This results in a higher efficiency but fundamental power lower then the class A rating of transistor.

From *Figure 1.4*, throughout the class AB range and up to the midway class B condition, the only significant harmonics are the second one, in phase with the fundamental, and the third one, which is in anti-phase. As we will see in the next sections, an accurate control of load impedances at the harmonics is crucial for the optimization of the amplifier performances.

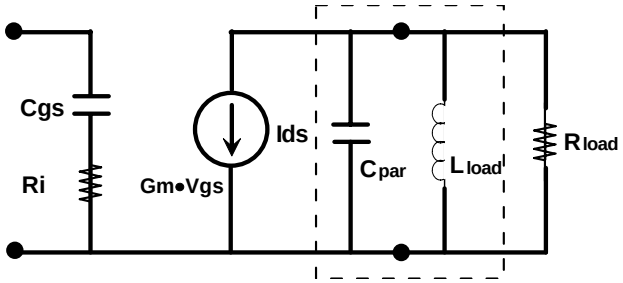
Instead of the drain efficiency (η), in the power amplifier design is more useful to consider the Power Added Efficiency (*PAE*); this index gives the opportunity to take into account not only the dc power supplied to the amplifier but also the RF input power, introducing the Gain as another important target in the trade-off of the performance. From this point of view, the best operating condition to optimize both output power and PAE is the Class AB operating mode.

In the next paragraph, a simplified method for class AB design will be exposed.

1.2 Class AB Power Amplifier Design

The design of high-power and high-efficiency narrowband amplifiers implies a careful choice of bias point, loading and input power level. As we seen before, the choice of class A, AB, B or C is based on a compromise between gain, output power, efficiency and distortion contents [5]. Qualitative and quantitative considerations must therefore be made by the designer in order to obtain the best performances from a power stage [6-7]. In this paragraph general guidelines and a quick design procedure will be described.

The starting point of this analysis is the same simplified active device model shown in *Figure 1.1*. Power amplifier has to be output-matched with the conjugate of the large-signal output impedance in order to resonate the parasitic capacitances at the operating frequency; to do that, a "tuned" output circuit, which transfers the active power from the intrinsic transistor to the load, has been added to the model as shown in *Figure 1.5* [8]. We may therefore assume that voltage and current are in phase at the intrinsic drain terminal; if we also assume a perfect resonator, or alternatively a short circuit load at higher harmonics, we may take the output voltage as a sinusoid.



$$V_{ds} = R_{load} \cdot I_1 \qquad G = \frac{P_1}{P_{in}}$$

$$P_{dc} = V_{dd} \cdot I_0 \qquad \eta_{drain} = \frac{P_1}{P_{dc}}$$

$$P_1 = \frac{1}{2} V_{ds} \cdot I_1 \qquad PAE = \frac{(P_1 - P_{in})}{P_{dc}} \qquad (1.11)$$

Figure 1.5 - Output tuned Circuit - Main Power Amplifier parameters

For given bias point and load resistance the output current waveform can be determined for every input power; from its Fourier coefficients I_n, expressed in the (1.7), all the main power amplifier characteristics could be computed (1.11).

From the $I_d - V_{ds}$ characteristic, plotted in *Figure 1.6*, we can assume the identification of the following physical parameters: V_k (drain saturation voltage), I_{max} (maximum drain current at V_{gs}=V_{bi}), V_{bro} (drain-source breakdown voltage with $V_{gs} = 0$) and V_p (pinch-off voltage); we can also consider as known the small-signal gain of the amplifier.

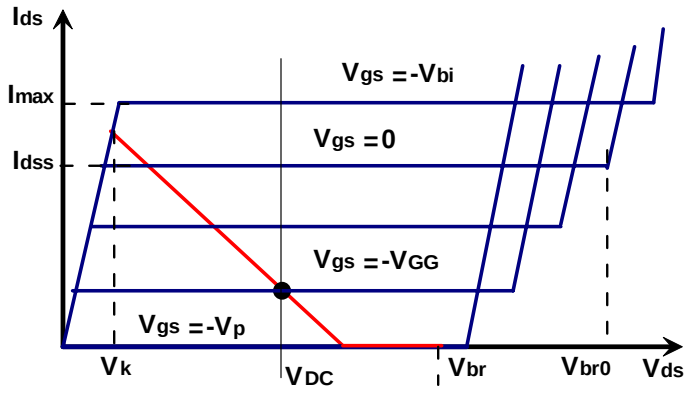


Figure 1.6 - Output characteristics with a class AB Load Line.

Considering the electrical constrains for the operating conditions of the transistor, the Drain bias voltage can be expressed as:

$$V_{dc} = V_k + \frac{(V_{br0} - V_k - 2 \cdot |V_{GG}| - V_{bi})}{2} \qquad (1.12)$$

Defining the working quantity θ, related to the ratio between the RF output voltage amplitude and the DC bias voltage, the bias current and the load resistance are related to this quantity and to the conduction angle α through the (1.13) and the (1.14), where R_s is the slope of the output characteristics in the ohmic region.

$$R_{load}(\alpha,\theta) = 2\pi \cdot R_s \cdot \frac{(1-\theta)}{\theta} \cdot (1-\cos(\alpha/2)) \cdot \frac{1}{[\alpha - \sin(\alpha)]} \qquad (1.13)$$

$$\left[\theta = 1 - \frac{V_{ds}}{V_{dc}}\right]$$

$$\frac{I_{dc}}{I_{\max}}(\alpha) = -\frac{\cos(\alpha/2)}{1-\cos(\alpha/2)} \qquad (1.14)$$

In figures *1.7b* and *1.8* the output power and power-added efficiency, as computed from the model, are plotted Vs. α**,** with θ as a parameter; by means of these graphs, the choice of the optimum α and θ can be made. The behavior of the PAE is strongly influenced by the gain of the transistor; therefore two cases for 9 and 12 dB small-signal gain are also reported.

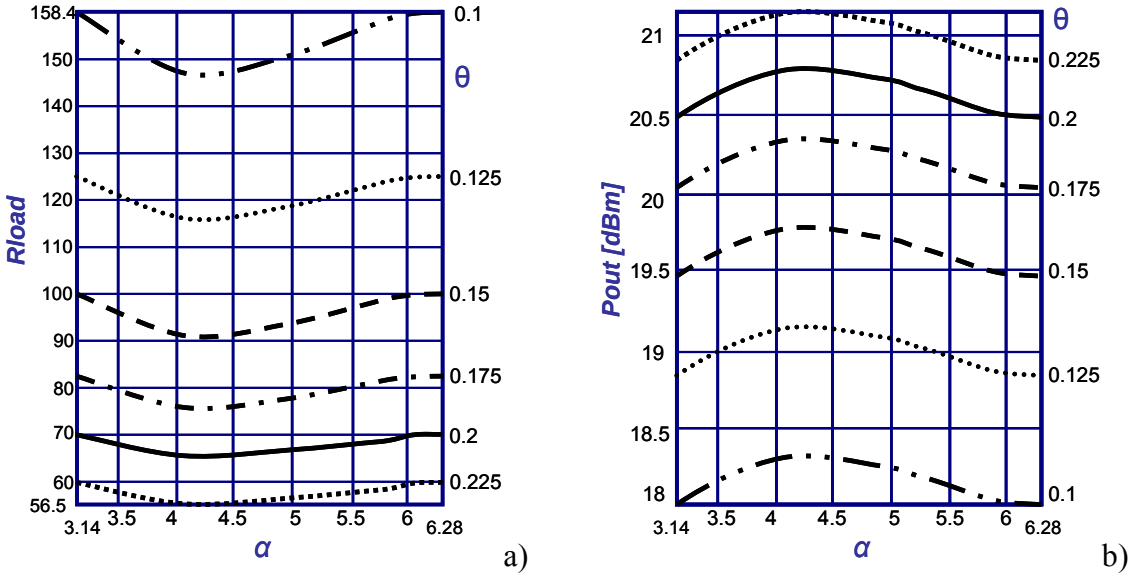


Figure 1.7 - Rload (a) and Pout (b) Vs. the conduction angle $\boldsymbol{\alpha}$*, with* $\boldsymbol{\theta}$ *as parameter.*

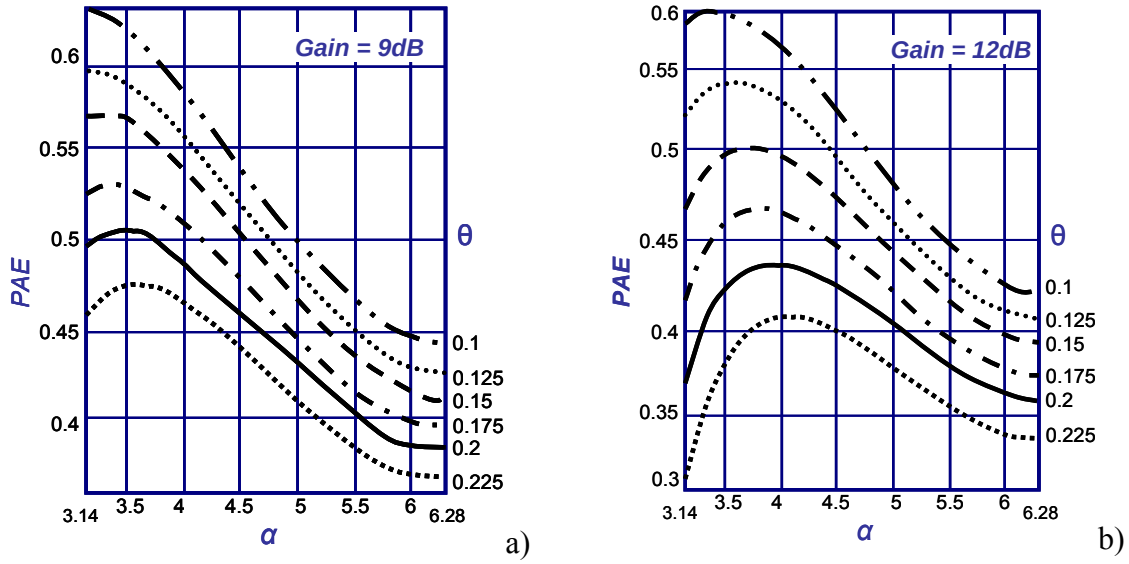


*Figure 1.8 - PAE Vs. the conduction angle **α**, with **θ** as parameter, for two different gain values.*

From the plots, we can see that for decreasing θ (i.e. increasing load resistances) the output power decreases, but power-added efficiency increases because of the prevailing effect of the increased gain: at this point, the designer has to define the best compromise between the two. It is also apparent from the plots that the output power is weakly dependent on the circulation angle α (i.e. on the bias current), while the power-added efficiency is much more dependent; in particular the two contrasting effects of decreasing DC power dissipation and decreasing gain (going from class-A to class-B, i.e. from $\alpha = 6.28$ to $\alpha = 3.14$) produce a clear maximum. Here again the choice of the compromise between best output power and best efficiency is left to the designer.

Once the optimum α and θ are chosen, the optimum bias and load resistance are easily computed from formula (1.14) above. At this point the actual values of V_k and V_{GG} can be re-introduced into the formula for V_{dc}, and the procedure repeated; however, if the first guess was close to the final result, as is usually the case, only negligible readjustments are found. The design is therefore completed.

1.3 Harmonic Tuned Power Amplifiers

The design approaches summarized above are based on the hypothesis of negligible or shorted harmonic frequency components. This assumption is not longer realistic in the design of high frequency and high power amplifiers, where the contribute of the harmonics becomes more influent and an accurate control of their terminations is

a crucial target for designers [9-11]. This paragraph explains some basic information about the design of high power and high efficiency power amplifiers basing on the harmonic tuning of the load impedances [12].

From the (1.15), derived from a simple power balance consideration, it's clear that, to maximize the drain efficiency, at least one of the two following equivalent conditions have to be satisfied: (a) maximize the fundamental output power $P_{out,f}$ or minimize both output harmonic terminations ($P_{out,nf}$, n>1) and the dissipated power on the device (P_{diss}). Since the target of the following analysis is to provide a useful design mean, it is easier to manage the former condition instead of the latter.

$$\eta = \frac{P_{out,f}}{P_{dc}} = \frac{P_{out,f}}{P_{diss} + P_{out,f} + \sum_{n>1} P_{out,nf}} \tag{1.15}$$

Assuming the active device as a voltage controlled source, as indicated in *Figure 1.5*, maximization of the fundamental output power corresponds to the maximization of the fundamental drain voltage component, with the constraint that the resulting voltage waveform has to be physically consistent. Assuming a periodic steady state, the drain current and the drain voltage waveforms can be expressed as the (1.16) and (1.17) respectively, where the limitations due to the intrinsic characteristics of the active device and the circuit complexity limit the output harmonic terminations control up to *3f*. If the output harmonic terminations are assumed as purely resistive, the voltage and current components can be related by the (1.18).

$$I_{ds}(t) = I_0 + \sum_{n=1}^{\infty} I_n \cdot \cos(n\omega t) \tag{1.16}$$

$$v_{ds}(t) = V_{dd} - V_1 \cdot \left[\cos(\omega t) + k_2 \cdot \cos(2\omega t) + k_3 \cdot \cos(3\omega t)\right] \tag{1.17}$$

$$\begin{bmatrix} K_2 = \frac{V_2}{V_1} \\ K_3 = \frac{V_3}{V_1} \end{bmatrix}$$

$$R_{L,nf} = \frac{V_n}{I_n} \tag{1.18}$$

Then, for a fixed I_n, the maximization of the efficiency is transformed in the selection of the two parameters k_2 and k_3 values maximizing V_1, with the condition that the drain

voltage is maintained lower than the breakdown. The results of this problem are summarized in the following table [13].

Controlled Frequencies		**k2**	**k3**	**δ**	**β**	**Achievable V1**
f	**Tuned Load**	0	0	1	1	V_{dd}
f, 3f	**Class F**	0	-0.17	1.15	1	1.15 - V_{dd}
f, 2f	**2nd h. tuning**	-0.35	0	1.41	1.91	1.41 - V_{dd}
f, 2f, 3f	**Class FG**	-0.55	0.17	1.62	2.8	1.62 - V_{dd}

Table 1.2 - Results obtainable with different Harmonic control.

In the table above, the quantity δ (*Voltage Gain Function*) relates the fundamental drain voltage amplitude V_1, obtainable by proper harmonic terminations, to the bias voltage V_{dd}, that can be considered as the fundamental amplitude for the unmanipulated approach (TL case); the *Voltage Overshoot Function*, β, quantifies the overshoot phenomena due to the use of even harmonic components. The two figures are defined as:

$$\delta(k_2,k_3)=\frac{V_1}{V_{dd}} \quad ; \quad \beta(k_2,k_3)=\frac{\max[v_{ds}(t)]}{V_{dd}} \tag{1.19}$$

The δ function directly gives the improvement on drain efficiency η with respect to the Tuned Load (TL) case. However, the δ values have to be considered carefully, not to violate physical constraints. In fact, since drain voltage harmonic components V_n are generated by the current harmonic ones, I_n, through the drain impedances $R_{L,nf}$ (1.18), the k_2 and k_3 optimum values must be physically synthesized, i.e. the corresponding impedances $R_{L,2f}$ and $R_{L,3f}$ must be positive values. I_2 and I_3 have therefore to satisfy proper phase relationships with respect to I_1 (*Table 1.2*, sign of k_2 and k_3). Such relationships are very important, since if not fulfilled may lead to detrimental results.

These analytical results are at the base of the design approaches discussed in this thesis, because they directly influence the load line shape; in fact, as we will see in next

chapters, a proper control of the shaping of the Load Line at the intrinsic terminals of the active device allows optimizing the power amplifier's performances.

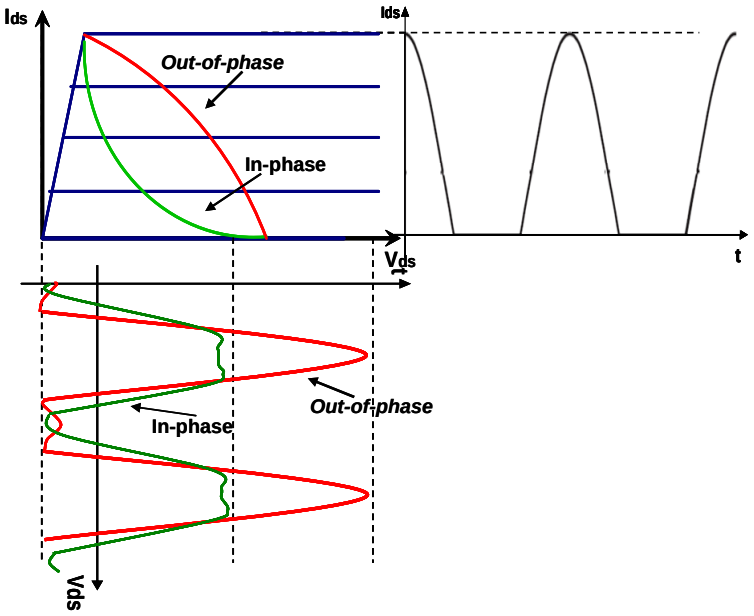


Figure 1.9 - Output load curve for 2nd harmonic tuning approach with proper (out-of-phase) or wrong (in-phase) voltage components

Optimum load impedances for the intrinsic drain current source can be determined as the (1.20). Thus, the harmonic "output" approach can be useful if the generated drain current waveform allows positive values for $R_{L,nf}$, according to that equation. In fact, even if there is a power dissipation on such harmonic loads, that could be interpreted as a detrimental phenomena, the fundamental output power is maximized, simultaneously maximizing the drain efficiency.

1.4 The Load-Pull Techniques

In the advanced design of high power amplifiers, the *Load-Pull* technique represents a powerful tool to search and to synthesize proper load impedances, taking into account the needful trade-off between several amplifier's characteristics. This method is based on the definition of the active device performances for different load impedances and, then, for different points on the smith chart. In this way, closed contours can be plotted on the chart, marking the boundaries of specified levels of output power, efficiency, gain, etc., (*Figure 1.10*) [14]. For example, if the target of the

design is a compromise between minimum levels of both output power and efficiency, superimposing on the same graph their contours, the designer can chose the particular impedance for which both conditions are satisfied.

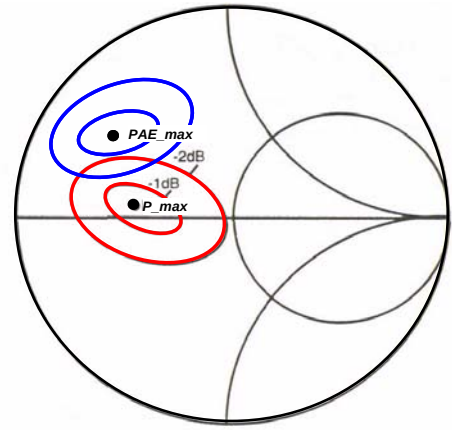


Figure 1.10 - Typical Load Pull contours for power and efficiency.

The Load Pull technique can be applied by different approaches: one is based on large signal simulations, the other on measurements and experimental results. In the former case, a full non linear model for active device is needed, joined with non linear analysis algorithms. For this approach, the major drawbacks are related to the use of an appropriate and accurate non linear model [15-16] and to the complexity of the computation in the design CAD tools when strong levels of non linearity have to be reached.

The experimental approach is based on Load Pull systems, in which the active device is fully characterized in terms of output power, matching impedances, efficiency, and any other required performance, by means of exhaustive and intensive measurement activity [17-20]. At the moment there are two different kinds of Load Pull systems, the active one and the passive one, basing on an active or a passive load synthesis. For the purpose of this work, in this paragraph, a brief description of the only passive Load Pull bench will be exposed.

Figure 1.11 shows a typical Load Pull setup, where both Source and Load impedances of the DUT are synthesized and modified by means of two *Programmable Tuners*. This setup allows measuring the main characteristics of the DUT for different load conditions and then producing, by specific software, the needed Load Pull contours. Such a system provides a complete large-signal characterization of the DUT

to the designer, which can chose the proper input and output impedances to satisfy the required performances.

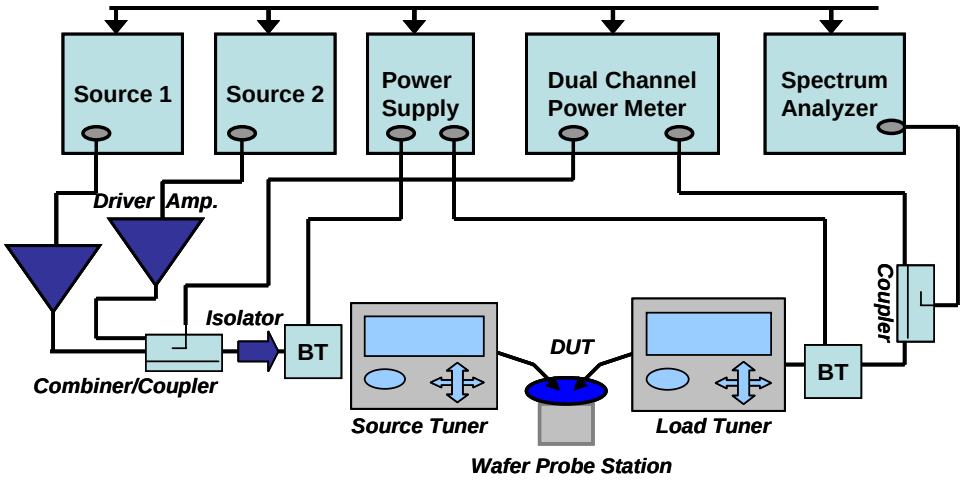


Figure 1.11 - Typical Passive Load Pull Setup.

The Active Load Pull systems have the same target of the passive one, that is to synthesize a wide range of impedances at the input or output of the DUT, but the main difference is in using a "virtual load": part of the outgoing signal is modified in amplitude and phase by amplifier/phase shifter network and re-injected into the output port the DUT. The device sees a load reflection factor that could be equal or larger than 1, because amplifier is involved, compensating for the loss of cable and test fixtures, and then covering every impedances in the smith chart plane.

However, also load-pull setups, both active and passive, present some relevant drawbacks; first of all they are frequency and power limited, and their cost dramatically increases when high operating power and/or frequencies are required. Then, a major limitation of this technique is related to the difficulty in synthesizing the full range of device terminations: especially when on-wafer devices having a large periphery are considered, passive load-pull suffers from the inability to synthesize very low impedances (*Figure 1.12*), whereas active load-pull may become critical from the stability point of view. Moreover, once load-pull contours have been drawn, no information is given about the intrinsic ED Load Line, that, as explained in the paragraphs above, plays a fundamental role in the design activity: loading conditions which show similar microwave performance can correspond to very different Load Lines at the intrinsic device. This is a vital aspect since reliability conditions are defined

at the intrinsic ED ports [21] as the passive access structures to the active area do not have any major impact on reliability (for instance, the device breakdown condition is related to the breakdown of the intrinsic gate-drain diode).

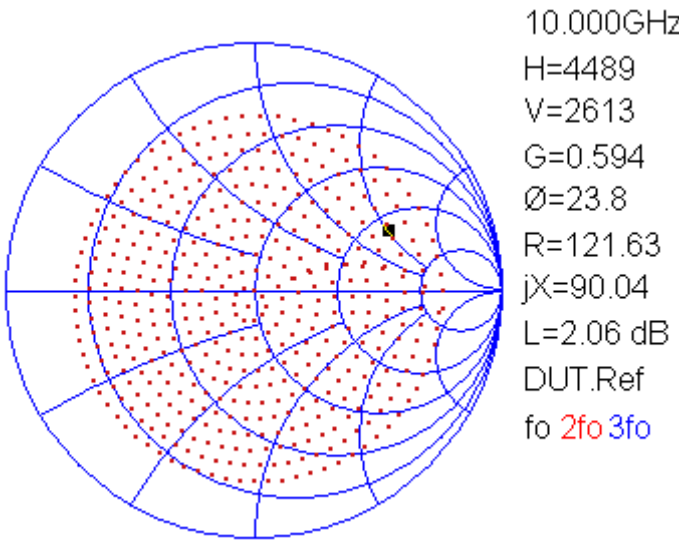


Figure 1.12 - Typical map of the achievable impedances in a passive load pull system.

The figure above shows a typical map of the impedances achievable by a Passive Load Pull system at *10 GHz*, where the minimum input impedance which can be synthesize has a reflection coefficient of about *0.75*.

1.5 Summary

In this chapter, the theories, that represent the pillar of the power amplifier design techniques, have been summarized. In particular, we saw as such a kind of circuits is usually designed by exploiting a mix of three different approaches: Cripps load-line theory, load-pull measurements, and iterative harmonic-balance analyses based on nonlinear models of electron devices (ED).

Furthermore, basing on these theories, the main approaches for the definition of the best load impedances for high efficiency high power amplifiers have been explained, focusing on the fundamental role of the harmonic tuning in the optimization of both output power and Power Added Efficiency.

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Chapter 2

Design of Hybrid HPA for Space Applications

In the previous chapter, the main design methodologies for power amplifiers were presented, starting with the more theoretical one and, then, describing the more experimental approaches. The evolution of these methods has been applied to develop very different techniques for design of power amplifiers for different kinds of applications. The main purpose of the research activity described in this thesis is the definition and application of a quite simple design methodology capable to produce the best performances but, at the same time, satisfying the tight constrains imposed by space applications.

In this chapter, after a description of the motivations for that constraints required by satellite systems, the proposed methodology will be explained by means of the design of a hybrid high power amplifier to be used in a *SAR* (*Synthetic Aperture Radar*) antenna. The final results will be the realization of a TR module representing the state of the art in this particular field of application.

2.1 Effects of Space constrains on power amplifier design

It is trivial to understand that a very crucial point for every kind of space system is the reliability. That is not just because, after the launch, any maintenance operation is not possible but also for the sever environment conditions in which the system has to work. The reliability issues involve every component of the vehicle, both mechanical and electrical; concerning the power amplifiers or, more in general, the overall TR module, designer has to taking into account how the space constraints engrave on the times of life and on the performances of the electronics components but, also, how the mechanical limitations, for example on the bonding wires, have influence on the degrees of freedom of the entire project.

To assure proper reliability levels, each component of satellite equipment has to operate in "*derating*" conditions, defined by the agencies for space standardization [1]. The term derating refers to the intentional reduction of electrical, thermal and mechanical stresses on components to levels below their specified rating. Derating is a means of extending component life, increasing reliability and enhancing the end-of-life performance of equipment. It provides a safety margin between the applied stress and the demonstrated limits of the component capabilities. In addition, derating participates in the protection of components from unexpected application anomalies and board design variations. Derating requirement shall be taken into account at the beginning of the design cycle of equipment for any consequential design trade-off to be made.

Concerning power amplifier design, derating has to be applied to both temperature and electrical limits recommended by the foundry for both active and passive structures, engraving, certainly, on the circuit's performances. This means that, during design activity, several factors must be kept carefully under control; some of them are listed below:

- Junction temperature at maximum operating conditions;
- Power rating and dissipation;
- Maximum voltage and current;

In particular, while the channel temperature of active devices is tightly linked to its MTBF (*Mean Time before Failure*), current and voltage levels have to be compared to the most destructive phenomena of breakdown. Conjecturing that, as usually happen, designer has to apply a derating of the 20% respect of the maximum rating provided by

the foundries, it means that he has a reduction of the maximum dynamic swing for both currents and voltages, with a consequent abatement of the maximum deliverable power.

The component parameter strength defines the limits and the performance component technology in the particular application and varies from manufacturer to manufacturer, from type to type, and from lot to lot and can be represented by a statistical distribution. Likewise, component stress can be represented by a statistical distribution. *Figure 2.1* illustrates the strength of a component and the stress applied at a given time, where each characteristic is represented by a probability density function. A component operates in a reliable way if its parameter strength exceeds the parameter stress. The designer shall strive to make sure that the stress applied does not exceed the component parameter strength. This is represented by the intersection (*shaded area*) in the picture. The larger the shaded area, the higher the possibility of failure becomes.

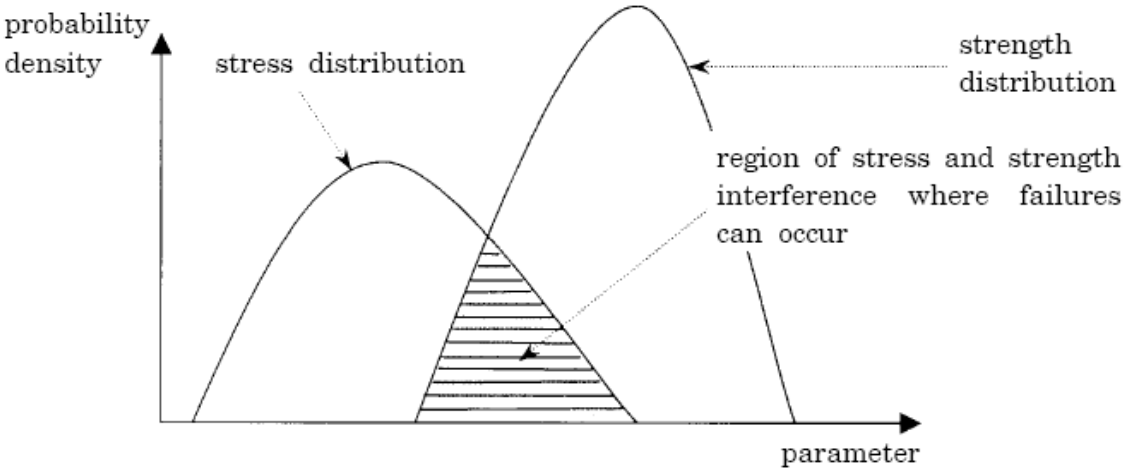


Figure 2.1- Parameter stress vs. strength relationship.

There are two ways, which may be used simultaneously, in which the shaded area can be decreased:

- Decrease the stress applied (which moves the stress distribution to the left).
- Increase the component parameter strength (by selecting over-sized components) thereby moving the strength distribution to the right.

The goal is to minimize the stress-to-strength ratio of the component. Derating moves the parameter stress distribution to the left while the selection processes applied to the components for space applications contribute to moving the parameter strength distribution to the right. The selection processes also reduce the uncertainty associated with the component parameter strength. Derating reduces the probability of failure,

improves the end-of-life performance of components and provides additional design margins. Another effect of derating is to provide a safety margin for design. It allows integrating parameter distribution from one component to another and from one procurement to another.

2.2 HPA - Application context

To define a design methodology capable to maximize the performance of power amplifiers for space applications, complying the tight constrains, an HPA has been studied and developed, to be used in a L-band TR module for a SAR (*Synthetic Aperture Radar*) antenna for earth observation (*Figure 2.2*).

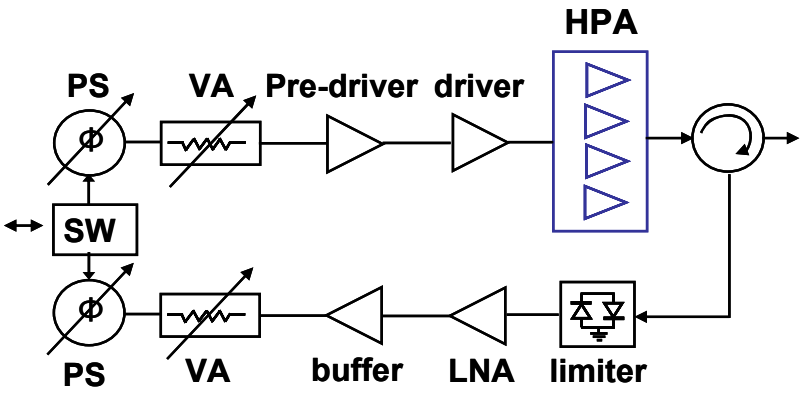


Figure 2.2 - Schematic of a TR module.

Synthetic aperture radar can provide measurements key to the water cycle (e.g. soil moisture and water level), global ecosystem (biomass estimation, land cover change), and ocean circulation and ice mass (ice motion). L-band radar provides the ability to make these measurements under a variety of topographic and land cover conditions, day or night, with wide coverage at fine resolution and with minimal temporal de-correlation [2, 3]. L-band is the preferred frequency for land-related studies because the wavelength favours long-term correlation, is less sensitive to ionospheric disturbances and has sufficient frequency allocated bandwidth. For all these reasons, L-band represents an important segment for many space programs world-wide [4-6] Electronically-steered phased array antennas are required for beam agility to enable rapid accessibility, global coverage and short revisit times [7].

Space-based radar places significant demands on the spacecraft resources (mass, power, data rate) and is therefore very expensive to implement. These systems typically require active phased-array antennas with hundreds or thousands of Transmit/Receive (T/R) modules distributed on the array. High Efficiency is a vitally important figure of merit for the radar T/R module because it reduces the power consumption and therefore makes best possible use of the limited power available. High efficiency also improves the thermal design and reliability. Beside efficiency, high output power is also requested to reduce the number of the modules, and then mass and space, and to enhance the SAR performance and the system service capability [8].

In order to reach the state of the art in this filed, the target of the design activity has been to realize an HPA capable to deliver an output power of about 40 Watts with a Power Added Efficiency (*PAE*) better than the 40% and fully compliant with the space application constrains. To reach such levels of power at this relatively low frequency, the Hybrid is the only possible solution, based on the combination of discrete active devices, lamped components and microstrip structures on high frequency laminates.

2.3 HPA Design

The starting point of the design activity is a proper choice of the technology to be used, basing on the design specifications and on the availability of a space qualified process. Basically, the available technologies for that application are Silicon LDMOS and Bipolar, GaAs FET, GaAs HFET, GaAs pHEMT and GaInP HBT. The frequency of the application, the requested power and efficiency levels, the thermal constrains and the reliability issues impose to choose a GaAS pHEMT process, the only one capable to make a trade-off between all that conditions.

After a preliminary study of all possible solutions, a space qualified *0.35-um* gate length GaAs p-HEMT process from Triquint Semiconductors Texas has been identified as the best solution for this application. This process is characterized by a V_{DS} breakdown exceeding *24 Volts*, a maximum current density of *650 mA/mm* and it can reach *1.2 W/mm* power density at 10 GHz at maximum ratings; due to the space application constraints, the HPA performances must be obtained using devices at de rated conditions. For this application these were identified as *20%* de-rating on

breakdown voltages and current densities. As mentioned above, the only viable approach identified is represented by the hybrid combination of 4 discrete *high power bar*, realized by the union of some pHEMT basic active cells (*Figure 2.3*) [9].

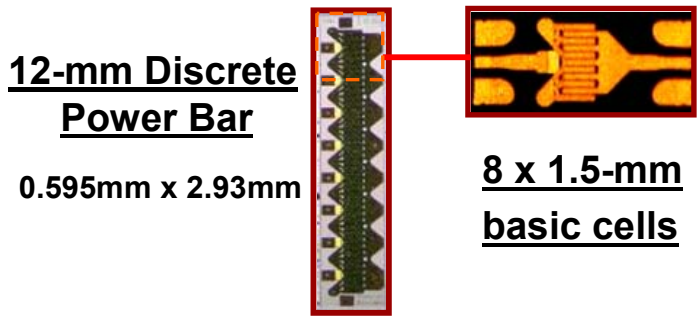


Figure 2.3 - The adopted 0.35µm pHEMT discrete bar: 8 unit cells (1.5 mm periphery each) for a total 12 mm gate periphery.

The power bar, in figure above, is composed of 8 pHEMT cells of *1.5 mm* periphery each for a total gate periphery of *12 mm*: this is the largest discrete device available as foundry standard product. The 8 cells are combined with a very high packing density: all the drains and the gates are connected on chip in a bus-bar like solution and are then, to a good extent, equipotential. Moreover, 8 gate and drain pads are available for wire bonding for a uniform distribution of the RF signal along the big periphery device. At maximum ratings condition this discrete pHEMT is rated to deliver *14 Watt* output power at 10 GHz. However these performances can't be achieved applying the de-rating rules required for space application, which are in particular *20%* de-rating on breakdown voltages and current densities, and maximum channel temperature below *120°C*, despite of the *150°C* suggested by the foundry to obtain the same *MTBF*.

The design focus is on the choice, for the elementary cell, of a proper bias and dynamic load-line which are able to optimize circuit performances like power and efficiency within the de-rated operating conditions. Taking into account the existing design methods presented in the *Chapter 1*, the approach explained below is based on a proper control and shaping of the dynamic load-line, monitored at the intrinsic terminals of the active device; imposing a particular shape to the load-line, a trade-off between power and efficiency can be reached and, at the same time, electron device currents and voltages related to reliability issues can be directly monitored.

Single Cell Design

As said before, the elementary cell, composing the power bar, has a total gate periphery of *1.5 mm* (10 gate fingers x 150 um width); optimizing the foundry design kit models for L band by means of linear and non-linear (load pull) measurements on some samples, the non linear model for the device was perfected and used in a simulation CAD tools for design.

The need to maintain the channel temperature of the device below *120°C*, for each electrical condition and at the maximum ambient temperature of about *40°C*, and to work in a high efficiency condition, imposes to choose the AB class as the operating condition of the amplifier, corresponding to the quiescent Bias values indicated in the table below.

Quiescent Bias Point		
V_{ds} = *10 V*	I_{ds} = *113 mA*	V_{gs} = *-0.625 V*

Table 2.1 - Polarization values of the single active cell of the HPA.

Considering that for this technology, in maximum rating conditions, the Drain-Source breakdown voltage could exceed about *24 Volts*, the V_{ds} of *10 V* allows to comply the derating of *20%* imposed by the application.

The active device is made unconditionally stable, form DC to cut-off frequency, by mean of a combined series-shunt RC stabilizing network, ensuring a good trade-off with the achievable gain. *Figure 2.4* shows a schematic of that network and its effects on the stability factor μ.

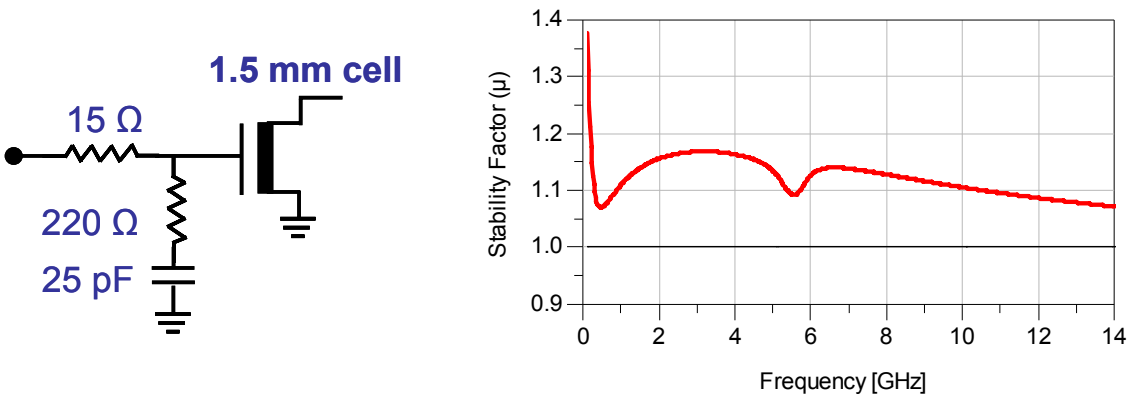


Figure 2.4 - Stabilizing Network for the 1.5 mm Cell and relative stability factor.

After the unconditional stabilization has been assured, the next and the most important step is to define the optimum impedance load for the device; that is the Γ_L (*Figure 2.5*) which allows reaching the required performances in terms of output power and efficiency and the needed level of reliability, at the central frequency of *1.275 GHz*.

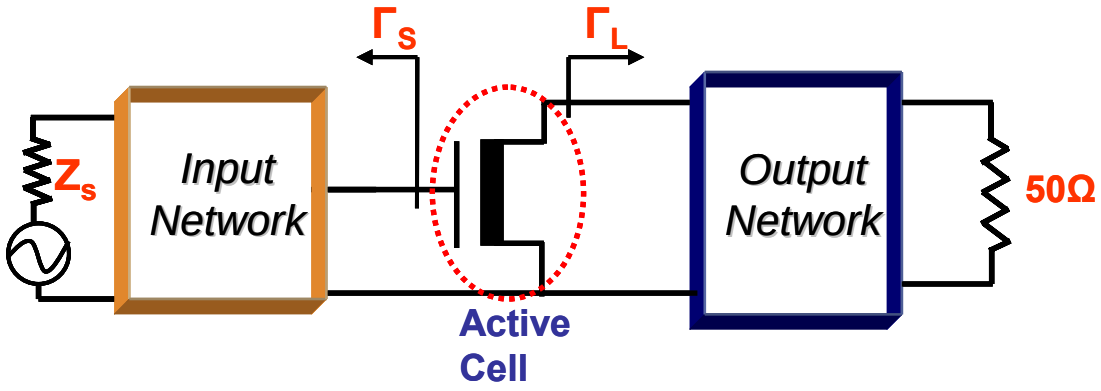


Figure 2.5 - Schematic of PA structure.

As said before, the method is based on a proper shaping of the dynamic load-line evaluated at the intrinsic terminals of the Electron Device (*ED*). As *Figure 2.6* shows, after the definition of the optimum impedance at intrinsic terminals (Z_{Lin}), which are accessible for the model used, the impedance to be synthesized by the output network (Z_L) can be obtained adding the effects of the parasitics network.

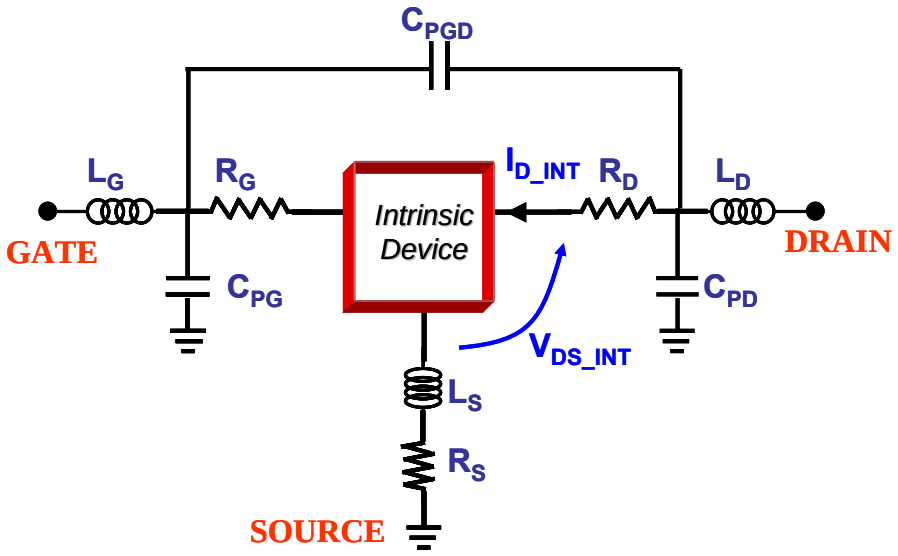


Figure 2.6 - Schematic of the electrical model used to design. Intrinsic Device and parasitic elements are pointed out.

The starting point is to define an appropriate Z_L, at fundamental frequency, in order to compensate the phase shifting between the drain current and voltage, due to then nonlinear capacity C_{DS}, and try to reach, at the same time, both saturation and interdiction zones. While the former condition, recognizable by the rectification of the load-line, allows to reduce reactive contributions to the power, the latter one, as viewed before, allows to maximize both current and voltage swing, improving the power level. Figures below show the first choice of the load impedance (Z_{L1}), without any operation at the harmonic components, the relative load-line superimposed on the pulsed *I-V* characteristics and main performances of the single active cell in an operating condition relative at a gain compression of about *2.8 dB*.

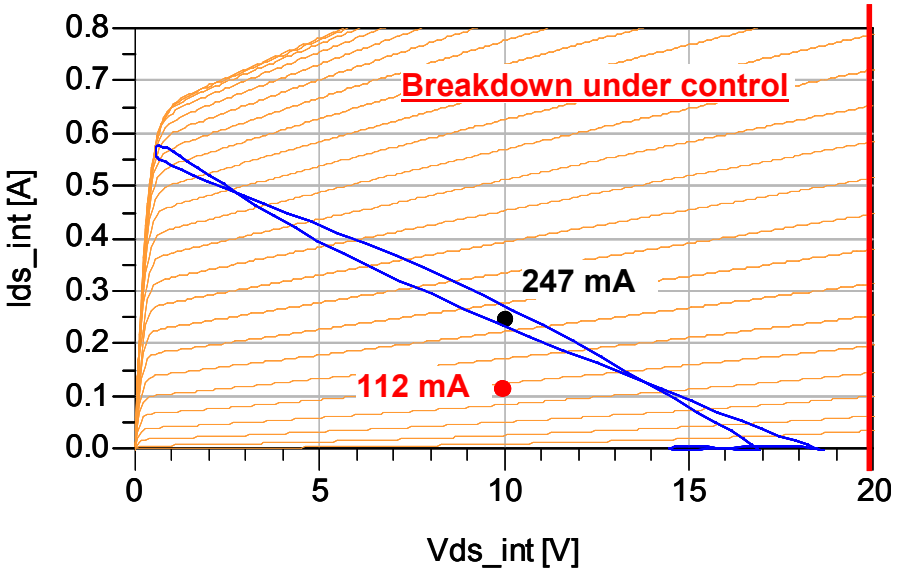


Figure 2.7 - First solution for the intrinsic dynamic Load-Line corresponding to Z_{L1}.

As the picture shows, at large signal condition the operating current rises from *112 mA* to *247 mA*, due to the auto-biasing phenomena, but, at the same time, there is a shifting of the dynamic load-line to a more dissipative region; that implies, as demonstrate in *Figure 2.8*, a not best condition for both efficiency and temperature. Beside the relative performances, *Figure 2.7* explains the importance of monitoring the intrinsic load-line, because the designer can monitor the drain voltage does not reach, dynamically, the breakdown limits.

Figure 2.8 shows the output power, the PAE and the junction temperature in terms of the input power; considering an operating condition at about *2.8 dB* of gain

compression, the single active device could deliver a power of about *31.3 dBm*, with the *53%* of PAE and a maximum channel temperature of about *114°C*.

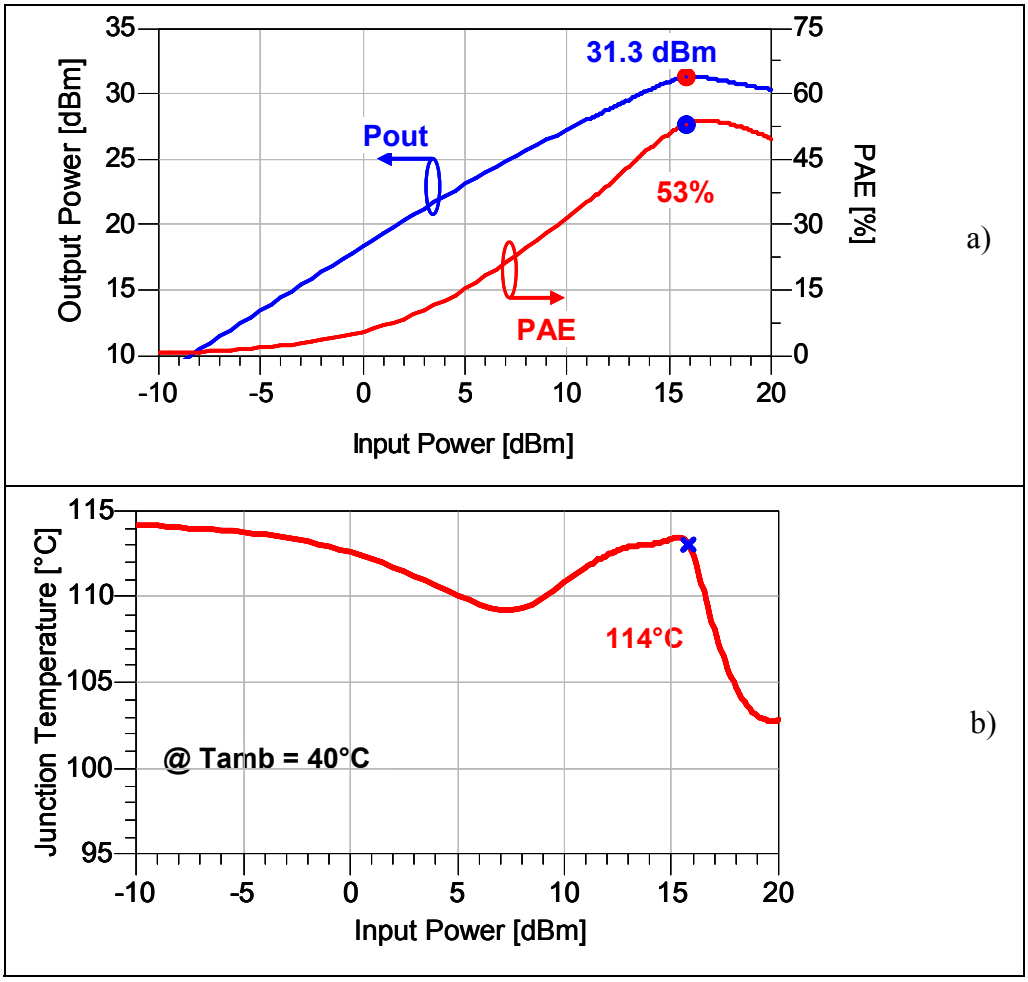


Figure 2.8 - Output Power, PAE (a) and Junction Temperature (b) for the 1.5mm single cell for a load impedance corresponding to Z_{L1}.

In these conditions, the efficiency can be improved, preserving the same level of power, forcing the load-line to work in a less dissipative region, reaching, anyway, the maximum levels of both drain current and voltage. To give to the load-line this particular shaping a harmonic tuning has to be performed, choosing appropriate values for the second and the third harmonics of the load impedance (respectively Z_{L2} and Z_{L3}).

Figure 2.9 shows as, starting from the standard condition with shorted harmonics, the proper tuning of Z_{L2} and Z_{L3} allows to give the desired shape to the load-line, confirmed by an enhancement of about three percentage points in terms of PAE and by a very good level of the output power (*Figure 2.10a*). Working in more

efficient conditions, also a reduction of the channel temperature can be observed (*Figure 2.10b*).

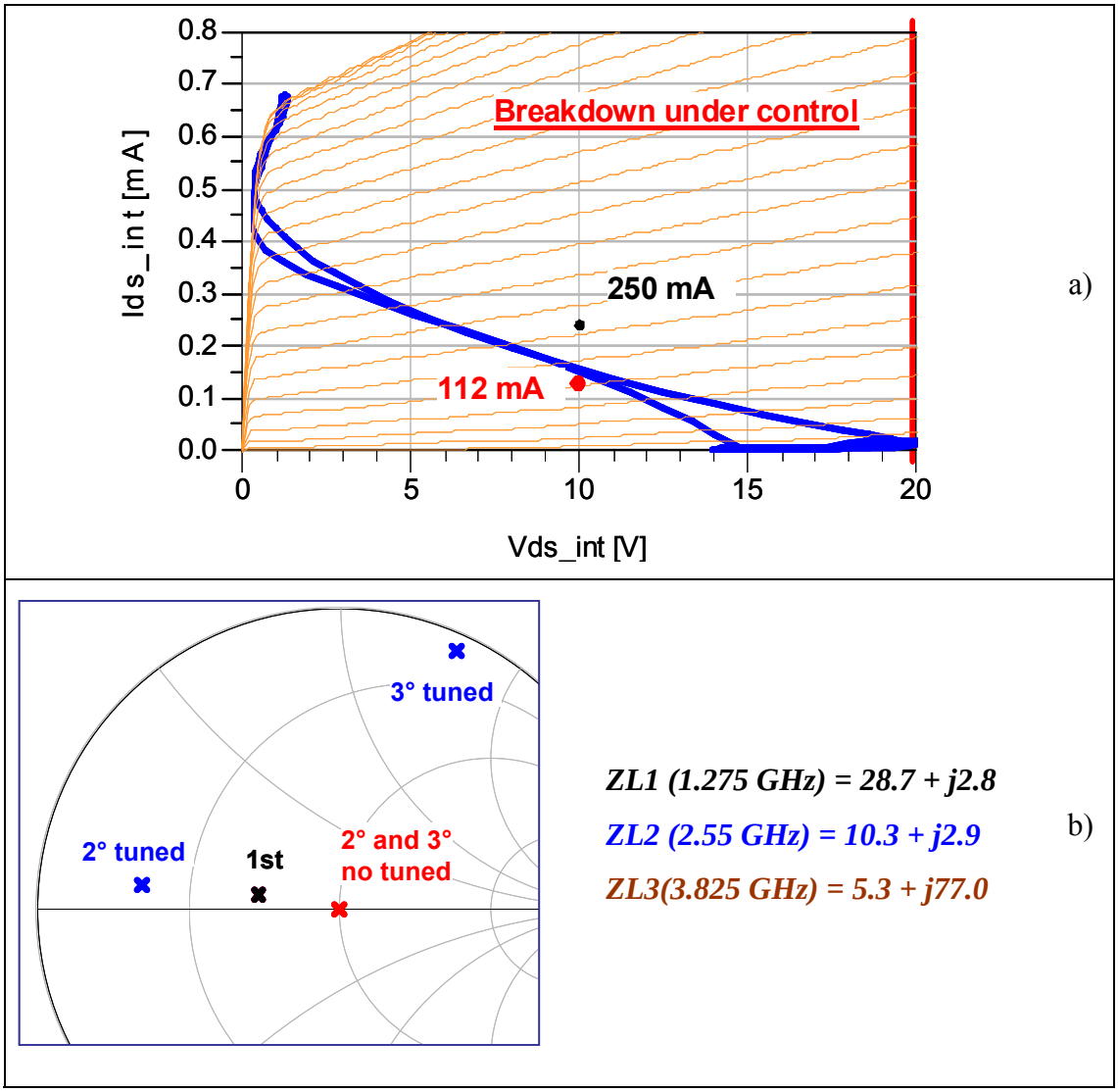


Figure 2.9 - Harmonic tuned dynamic Load-Line (a); Load Impedance at fundamental, second and third harmonic.

Figure below shows as, after harmonic tuning, the Power Added Efficiency rises up to *59%*, with an output power of about *31.8 dBm*, and the junction temperature decreases to *104°C*.

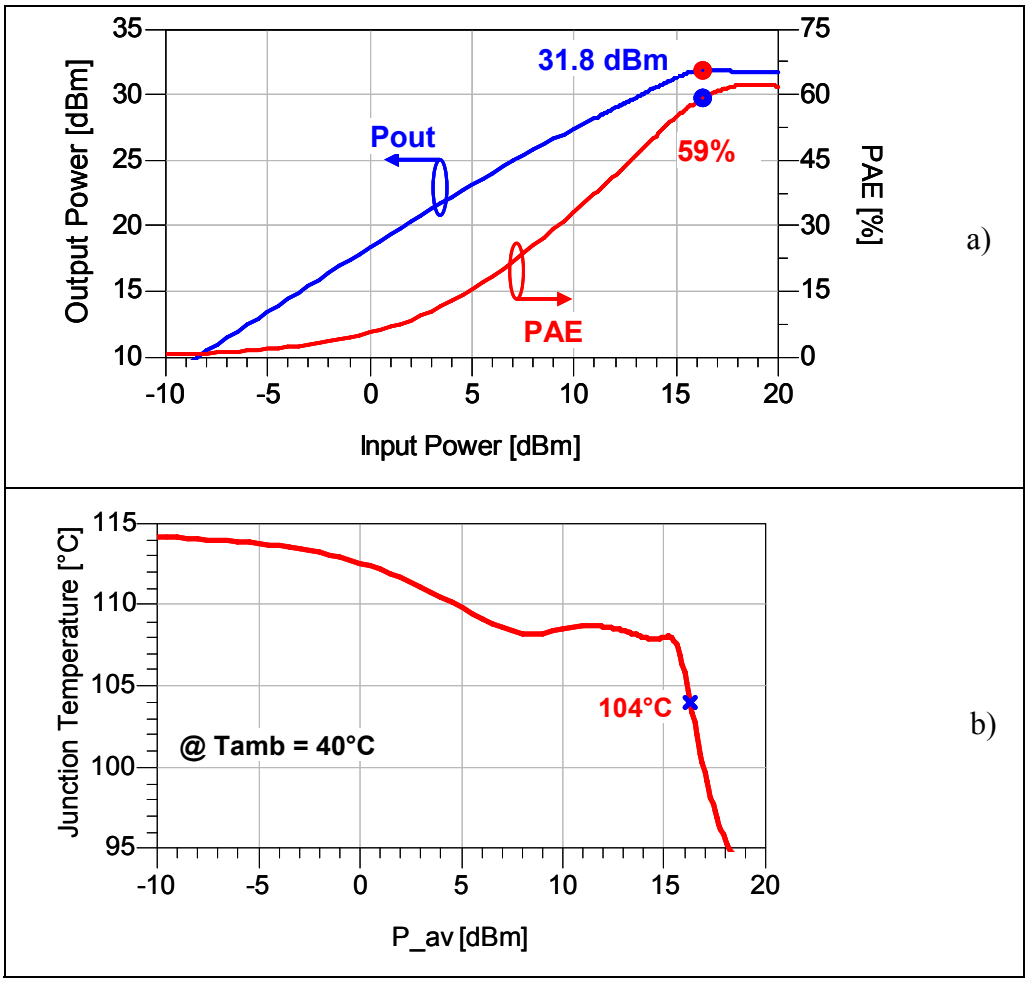


Figure 2.10 - Output Power, PAE (a) and Junction Temperature (b) for the 1.5mm single cell for the tuned load impedance.

The comparison between the two load-lines of figures *2.7* and *2.9* is at the base of the proposed approach. Imposing a proper shape to the load-line, the designer can perform the desired trade-off between the target performances and, at the same time, the electrical quantities that affect the reliability can be kept under control. In this particular case, where the target is design a HPA with high power and high efficiency, a sinking of the load-line in a region at lower dissipation, by mean of harmonic tuning, it gives a substantial improvement to the efficiency. In other cases, when, for example, linearity is researched, the target is to maintain the line as straight as possible.

Discrete Power Bar Performances

The optimum load conditions defined for the single active device have to be scaled for the entire Power Bar, with a total gate periphery of *12mm* realized by the combination of 8 elementary cell of *1.5 mm* (*Figure 2.11*).

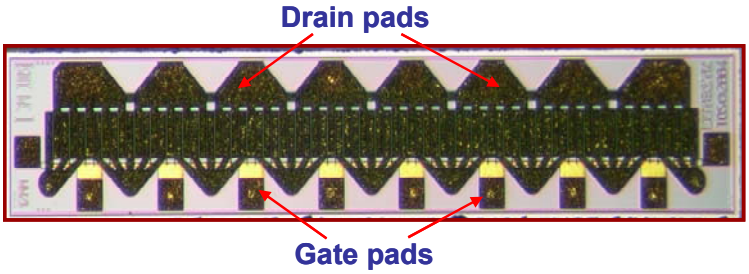
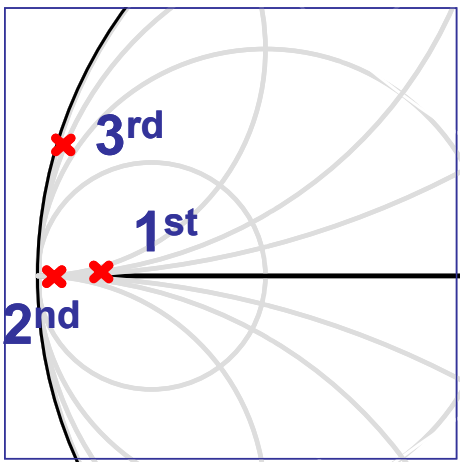


Figure 2.11 - The adopted 0.35um pHEMT Discrete Power Bar.

Basing on the performances obtained for the single cell, the entire Power Bar should deliver, at *1.275 GHz*, a total output power of about *12 Watts*. Simply scaling from the single cell, the quiescent Bias point becomes: V_{DS}=*10V*, I_{DS}=*900mA* and V_{GS}=*-0.625V*, with the current that, at large signal conditions, has to rise up to *1.9A*. *Figure 2.12* shows the load impedance for the entire Bar, at both fundamental and harmonic frequencies; that impedance has to ensure each of the elementary devices to be loaded in the optimum condition described above, preserving, hence, the optimum load-line.



ZL1 (1.275 GHz) = 6.7 + j0.6

ZL2 (2.55 GHz) = 0.5 + j0.1

ZL3(3.825 GHz) = 0.3 + j7.5

Figure 2.12 - Load Impedance for the entire discrete Power Bar.

As plotted in the figure below, the Power Bar should deliver an output power of about *12 W*, preserving the same efficiency of the single cell, *59%*.

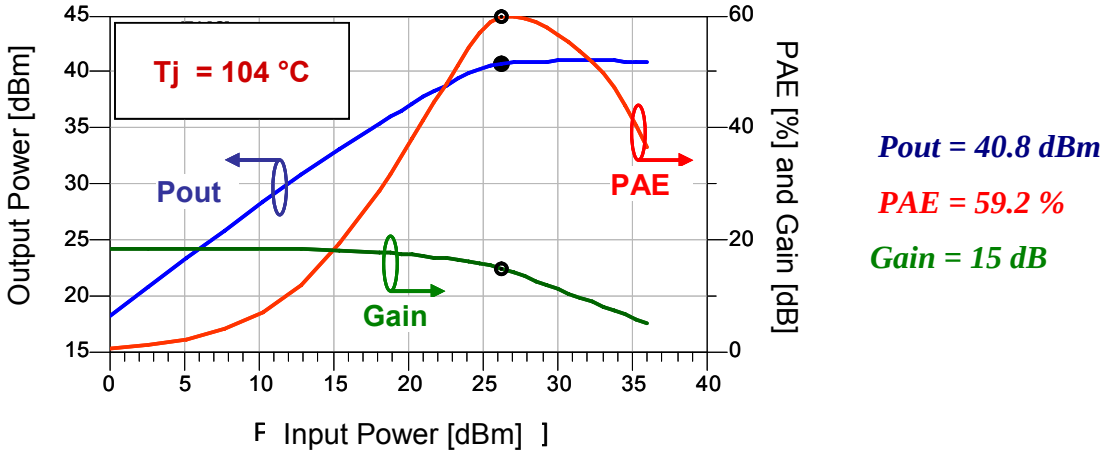


Figure 2.13 - Simulated Performances for the Power Bar.

A verification that single cells work properly inside the Power Bar is given by the waveforms of both drain current and voltage plotted in *Figure 2.14*; the maximum and minimum levels of the two quantities are the same evident from the load-line in *Figure 2.9,* and the clipping of the voltage curve denotes that devices are working in a high efficiency condition.

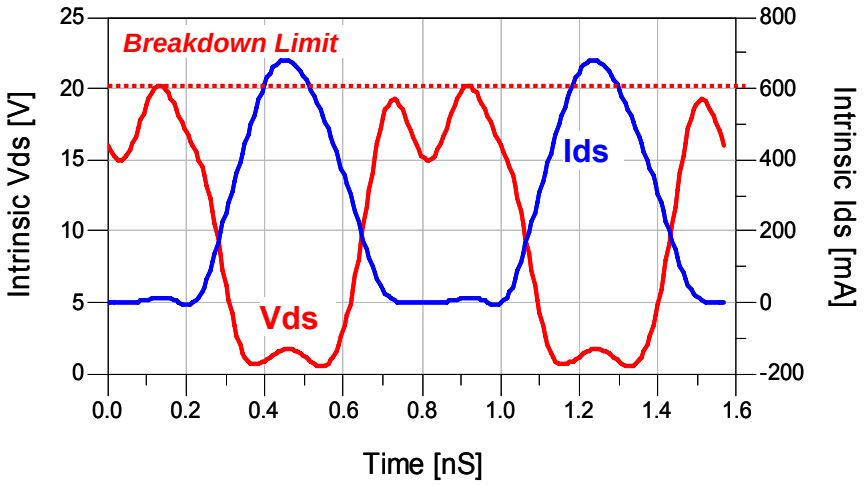


Figure 2.14 - Drain voltage and Current Waveforms.

2.4 Experimental Verifications

Results explained above are based just on theory and CAD simulations; even if the used electrical models have been verified by small and large signal measurement, a wide experimental activity was performed in order to verify the goodness of the design approach, taking into account all the unavoidable limits imposed by the practical realization of the amplifier.

Remembering that the final result was to apply the design method for the realization of an entire TR module, capable to deliver about *40W* in L band, this was reached through the design and realization of two "intermediate" prototype of power amplifier. In a first step, a 12 Watt HPA was carried out exploiting the described Power Bar, in order to verify expected results; afterwards, the opportunity to apply the design results to a parallel of 4 power bars has been investigate by the realization of a 42 Watt HPA. At the end, all results were applied to the entire power line-up of the TR module.

12 Watt Hybrid HPA

Once found the optimum load impedance for the bar, the entire matching networks have to be designed and realized. The prototype hybrid HPA has been implemented by adopting microstrip distributed input/output matching networks and SMD components, in order to synthesize the impedance transformer sketched in the figure below.

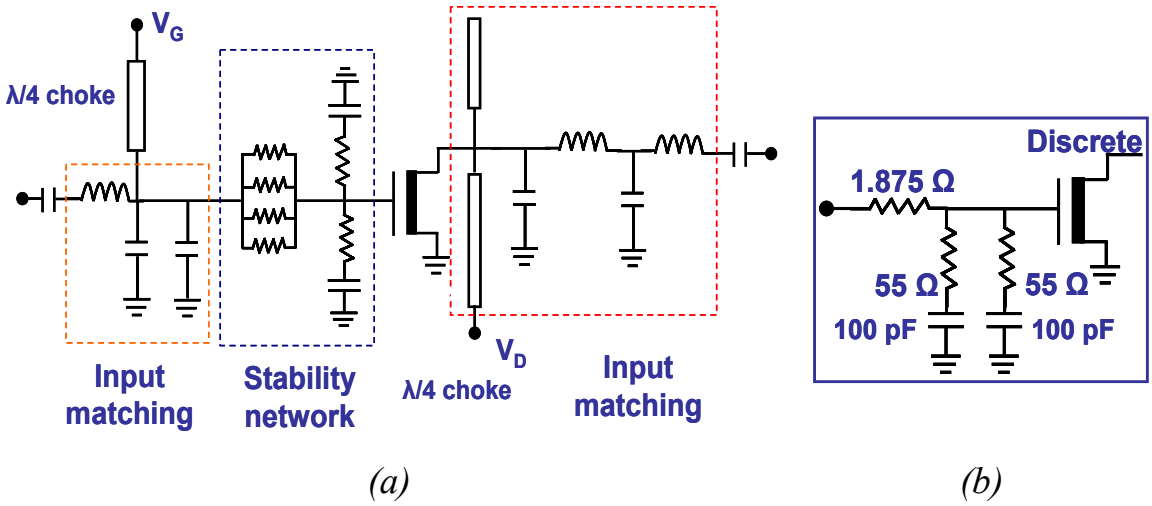
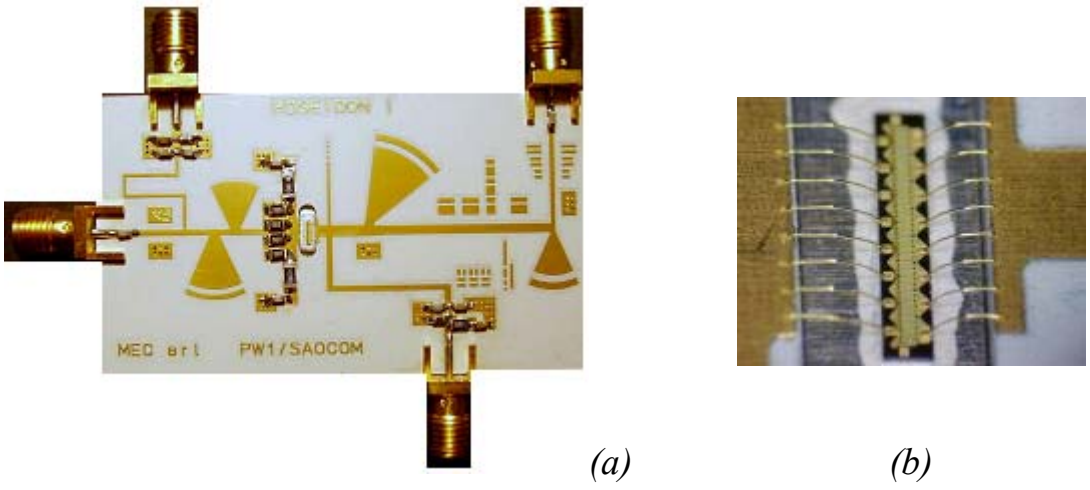


Figure 2.15 - Schematic of the Matching and stability Networks of the HPA

At the device input, a combined series-shunt RC stabilizing network is implemented by means of SMD thin film resistors and single layer chip ceramic capacitors; *Figure 2.15b* shows as the network has been readjusted for the discrete device starting from the stabilization of the single cell. This network makes the device unconditionally stable from DC to cut-off frequency. This stabilization network will be integrated inside the GaAs chip distributed at every unit cell gate in the final version of the amplifier for the T/R module space application.

At the device output, as is pictured in *Figure 2.16a*, stubs are used to tune the 2nd and 3rd harmonic to improve efficiency, as defined before. Gate and drain bias networks employ high impedance $\lambda/4$ microstrip lines with shunted SMD single layer chip capacitors placed before the SMA bias connectors. These capacitors are placed to shunt residual RF signals at the bias connections and avoid low frequency instabilities.

In *Figure 2.16b* the realized Hybrid HPA are pictured, with a zoom to the used discrete Power Bar where also bonding wires are visible; for the distributed structures a high frequency substrate has been exploited.



(a) *(b)*

Figure 2.16 - 12Watt hybrid power amplifier with a single pHEMT discrete bar.

The measured performances of the HPA are plotted in *Figure 2.17*; at an operating condition corresponding to a gain compression of about *2dB*, the Power Amplifier is able to deliver at the output connector a power of *12W* with a Power Added Efficiency of *56.5%*. The amplifier reaches a compressed gain of *12.3dB* and the converted drain current rises up to *1.9A*. These results confirm the expected performances obtained by simulations, taking into account that the matching network losses are included in the measured quantities.

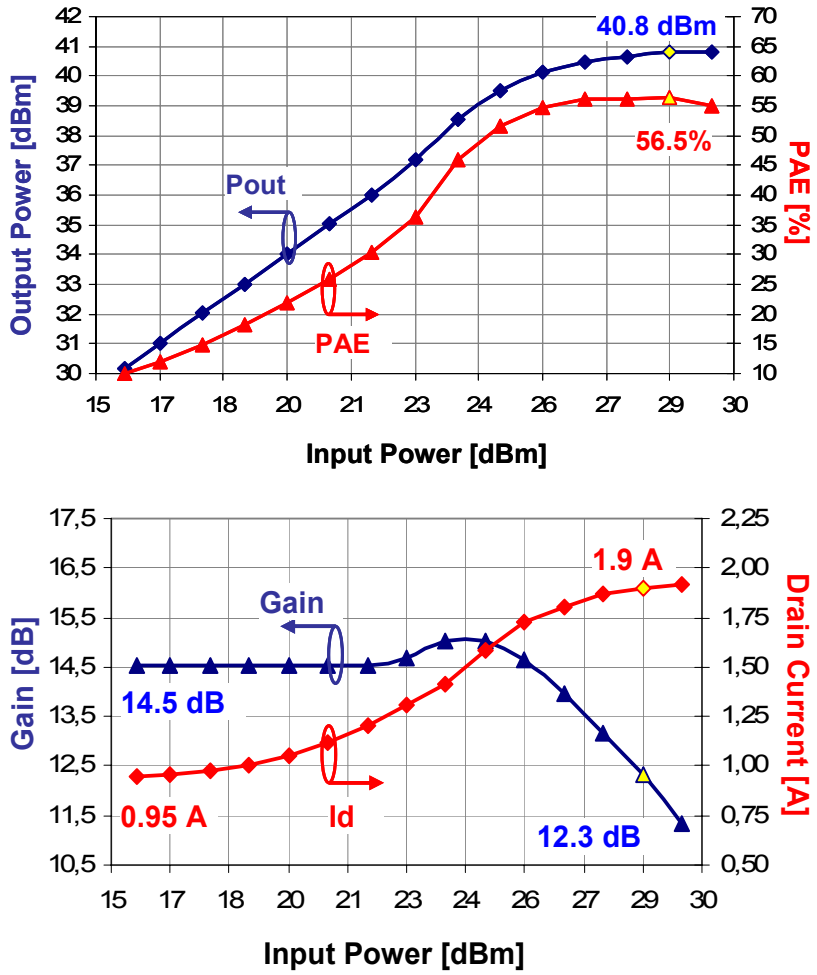


Figure 2.17 - Measured performance of the hybrid power amplifier with a single pHEMT discrete bar. Pout=12 Watts, PAE=56.5%, Gain=12.32 dB @ 2.18 dB compression.

The figure below shows the high power measurement bench used for the HPA characterization.

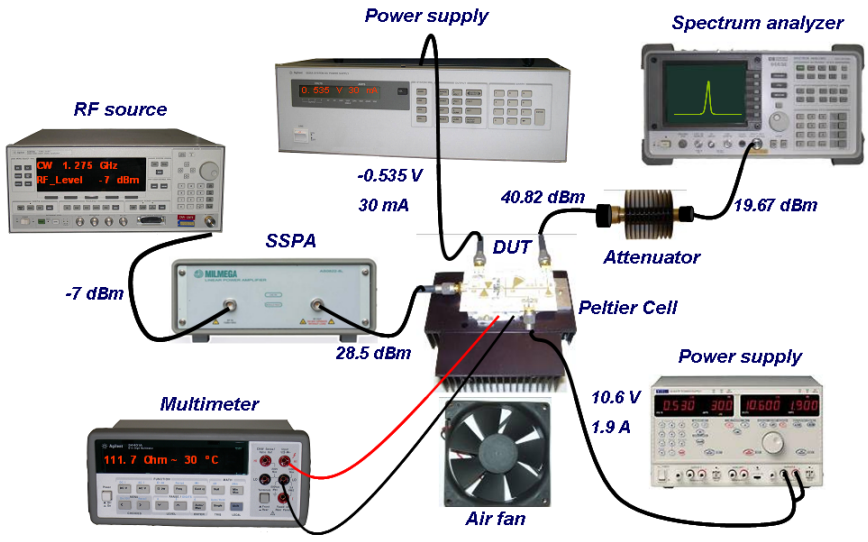


Figure 2.18 - High Power measurement bench.

42 Watt Hybrid HPA

Once the discrete power bar performance and the models' predictive capability have been proven with the implemented single-device HPA, a higher power amplifier has been designed and implemented with the topology shown in *Figure 2.19*.
The amplifier features four Power Bars combined by means of 4-ways input/output microstrip forks. The technologies used for the implementation and the design and modeling instruments are the same exploited for the previous amplifier.

The MIM capacitors used for the device output matching forms with the bonding wires an LC-LC lumped matching network as depicted in *Figure 2.19*. This low pass filtering lumped-element matching network is compulsory at such low frequency and for the high impedance transformation ratio required: indeed, for obvious space limitation, only a limited impedance transformation is performed in the output microstrip combining network by accurately tuning line lengths and characteristic impedance and radial stubs.

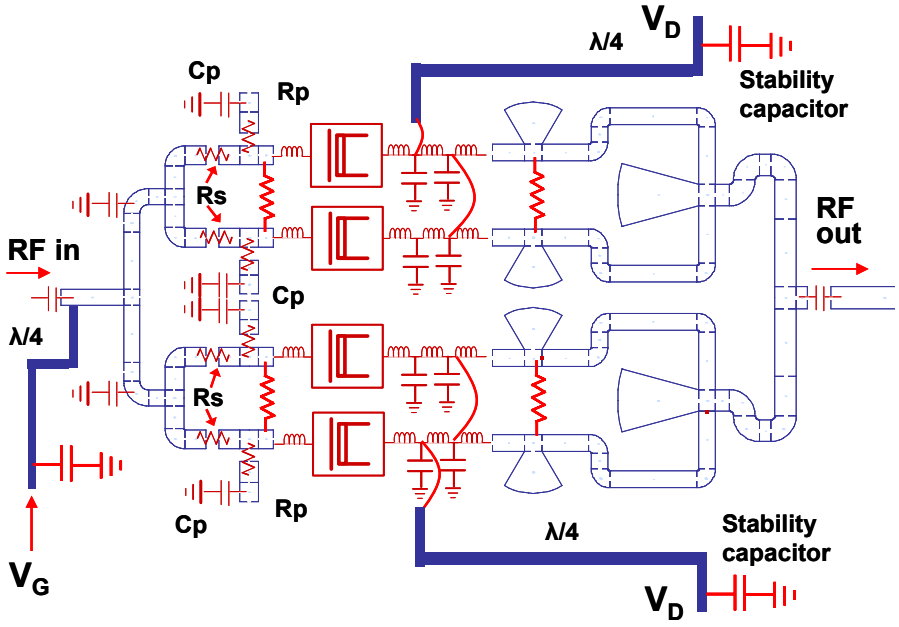


Figure 2.19 - Topology of the 42W Hybrid Power Amplifier.

Considering output matching at 50Ohm, the optimum drain impedance of the discrete device less than 5Ohm and the presence of a 4-way combiner, the impedance transformation ratio required is about 40. Even though the application bandwidth is relatively small (100MHz), also the selectivity of the matching network has to be taken into consideration, and then its order of complexity. From these considerations, and

taking into account series losses minimization the actual matching network is a 4th order one, with two lumped LC reactance transformation steps (wire bonding and MIM capacitors), and two distributed transformation (lines and stubs) in the combining microstrip structure. In effect the microstrip combiner transforms the impedance from the *50Ω*, at the output, to *11Ω* at each of the own four branches; the lumped network of bonding wires and MIM ceramic capacitors performs the remaining impedance step, synthesizing the wanted Z_L at the output of each discrete cells (*Figure 2.20*).

The ceramic MIM capacitors have been custom designed: their dielectric material, thickness and capacitance value were chosen in order to optimize the Q factor to minimize the power losses and to fit the geometrical dimensions of the discrete bars at which they are connected. The total losses of the output network are evaluated to be *0.44 dB*, *0.3 dB* in the lumped matching network and *0.14 dB* in the microstrip fork; minimization of losses is very important in the design because they are strictly connected to the efficiency optimization.

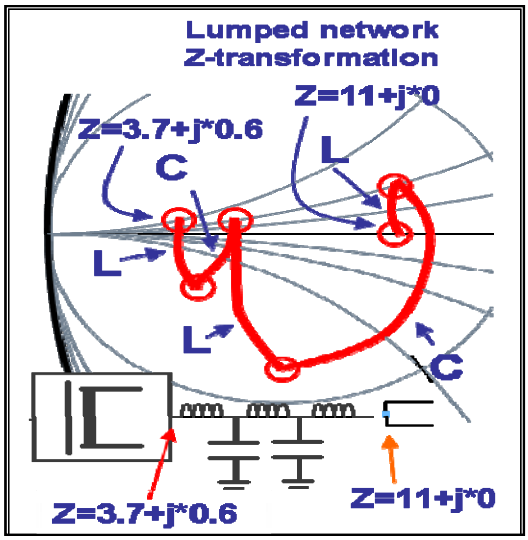


Figure 2.20 - Impedance Transformation realized by Lumped L-C-L Network.

The input matching didn't require any lumped network but only the microstrip splitter and two SMD capacitors to ground. The same type of series/parallel LC stabilizing network mentioned before is implemented for this amplifier also with SMD resistors and capacitors. The drain bias is fed with λ/4 lines symmetrically by two SMA connectors. Each connector feeds the drain bias current to a couple of discrete bars.

Figure 2.21 shows the prototype realized basing on the consideration discussed above; a picture of the output lumped network is also shown.

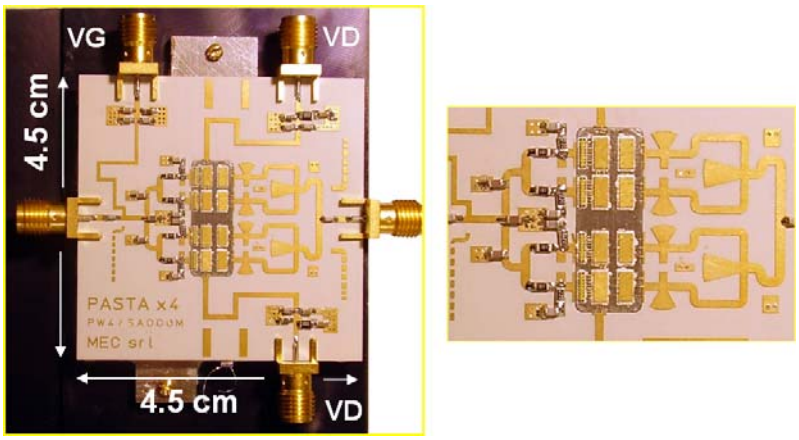


Figure 2.21 - Picture of the 4-device hybrid HPA and magnification of the lumped wire bonding – MIM capacitor matching.

Confirming the results obtained with the *12W* power amplifier, *Figure 2.17*, the measured performances for the HPA are *42 Watts* (*46.25dBm*) of output power with *13dB* compressed gain (*2.5dB* compression) and an overall PAE of *50%*. The total DC drain current is *3.82A* equally partitioned in the two harms (*Figure 2.22*).

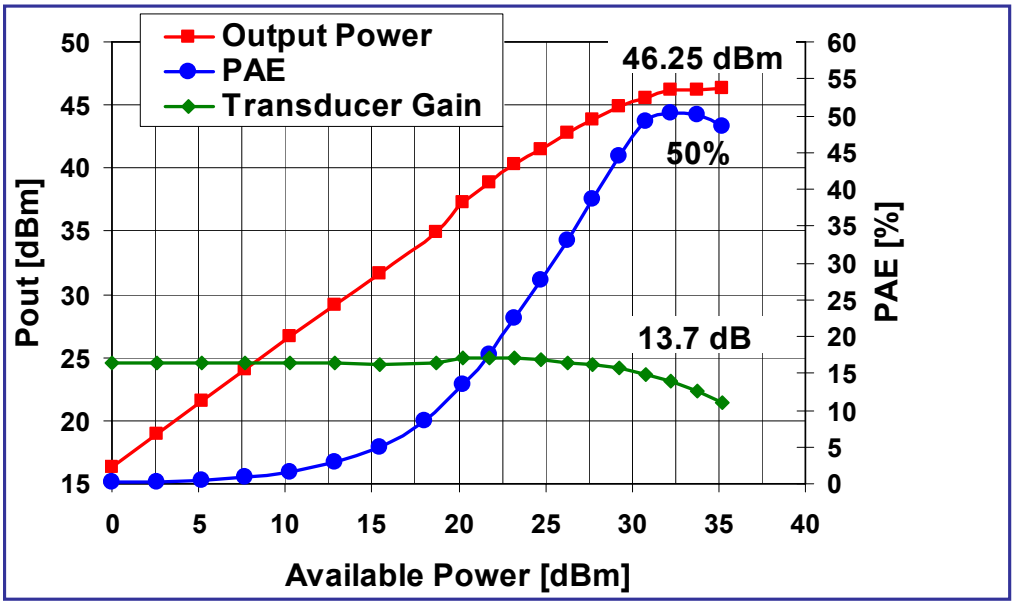


Figure 2.22 - Measured performance of the hybrid power amplifier with 4 combined pHEMT.

These results were again very similar to the simulated ones, even though some differences (*0.2dB* on output power) were observed. These small discrepancies are due to the difficulty to model with very high accuracy the MIM capacitor losses and the bonding wires self and mutual impedance.

48 Watt Power Line-Up

As the final act of the described activity, the proposed design approach has been applied to the entire Power section of a TR module, used in the array of a SAR antenna and manufactured by TAS-I (*Tales Alenia Space-Italia*). The entire line-up described below, is composed of three stages, namely pre-driver, driver and final-stage HPA, for an overall small-signal gain of *60 dB* at *1275 MHz* central frequency [10].

Basing on the design criterion applied to the 42W amplifier described above, the HPA in the final stage has been realized exploiting a combination of 4 Power Bars, obtained by a modification of the discrete device used up to now. The new bar features ten *1.5-mm* basic cells for a total gate width of *15 mm*, instead of the 8 used in the first version. The 10 devices share a common drain and gate terminal, but 10 contact pads are available at both sides of the chip for a proper distribution of the signal along the bar (*Figure 2.23*).

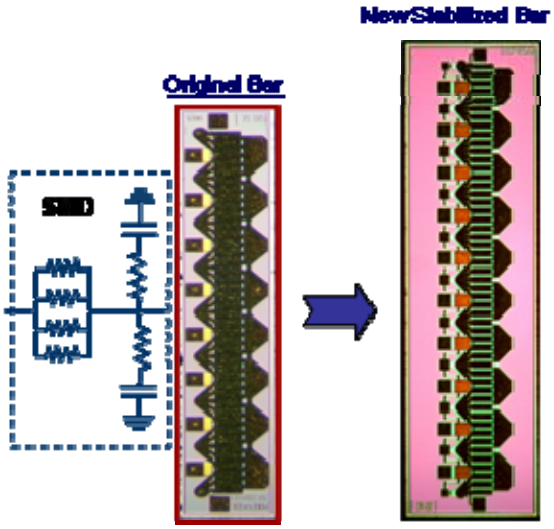


Figure 2.23 - The new 15mm power bar with integrated distributed stabilization network exploited for the final stage HPA implementations.

Furthermore, as shown in the figure above, the bar features an integrated network of metal resistors and MIM capacitors equally distributed along the 10 active devices. This network was designed for multiple objectives at the same time. Indeed it guarantees common mode unconditional stability, differential mode equalization, partial pre-matching and the optimized value for the gate series bias resistance.

In more detail, the stabilization network of each elementary cell, shown in *Figure 2.4,* has been integrated inside the power bar; with an obvious optimization of the HPA's area and a more accurate control of the lumped element values (*Figure 2.24*).

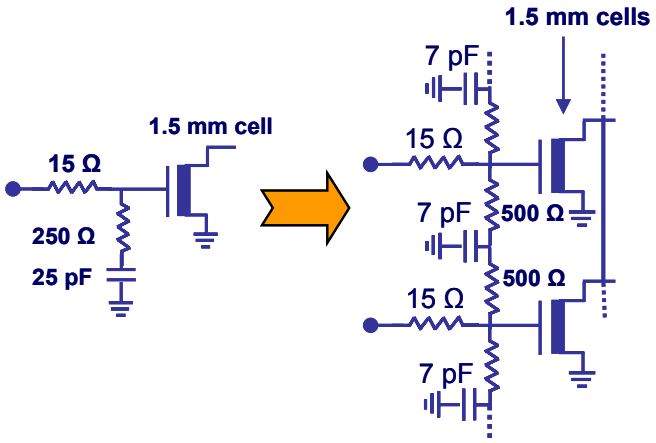


Figure 2.24 - Redistribution of the stabilizing network for each of the 10 elementary cells in the Power Bar.

As said before, the entire power line up is composed by three different stages (Pre Driver, Driver and HPA). The enhanced Power Bar was used for the implementation of both final and driver stage of the TR Module, while the stage of gain used upstream is a fully integrated monolithic circuit (*Figure 2.25*).

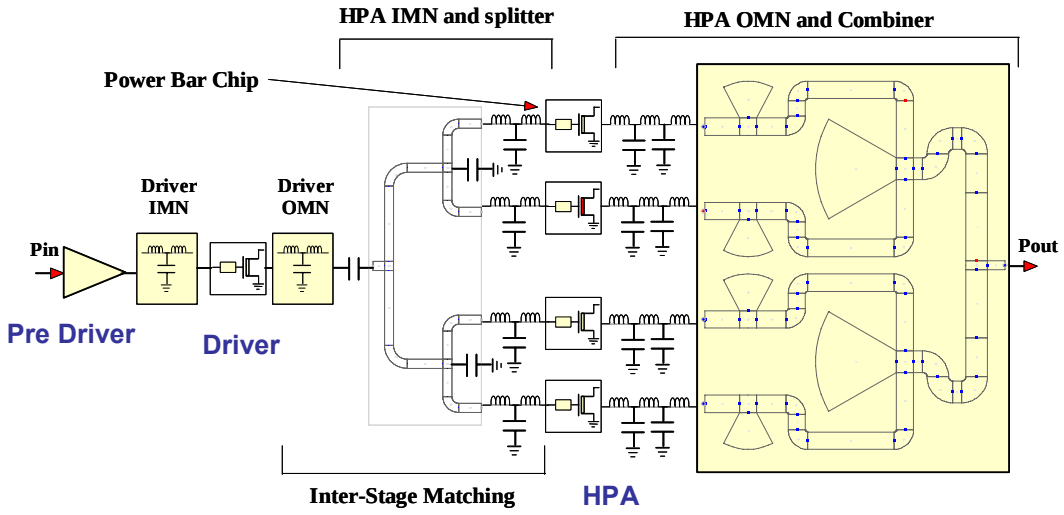


Figure 2.25 - Schematic representation of the entire line-up: Pre Driver, Driver and HPA.

While the pre-driver section is a conventional 50 Ohm-matched gain block, the driver and the HPA can't be conveniently divided into two separate stages, since there isn't a 50-Ohm section between the two, but rather they form together an unique two-stage amplifier. As described in *Figure 2.25*, the driver section consists of a single power bar as active stage; the input matching network is a lumped LCL low pass filter made with bonding wires, a ceramic MIM capacitor and a high impedance microstrip

line on alumina substrate. The output matching network of the driver is indeed an inter-stage network between the driver and the final stage HPA. It is composed of a hybrid lumped LCL section (bonding wires, and a ceramic MIM capacitor) followed by a 4-way power splitter on alumina substrate which feeds the signal to the gates of the 4 power bars which form the HPA stage. Between the microstrip power splitter and the power bars, a lumped LCL matching network is implemented with bonding wires and custom-designed ceramic MIM capacitors.

Reproducing the design philosophy applied to the *42W* amplifier, also the output matching network of the HPA employs a first step of lumped matching network made with bonding wires and MIM capacitors before the microstrip power combiner on alumina substrate. This output matching network is clearly critical for power and efficiency performance: critical points are the synthesis of very low impedance at the device output (as low as *3 Ohm*), the control of the harmonic impedances, and the need to keep the losses as low as possible. Additional constrains are the current limitation of the bonding wires, the limitation of their length and the space availability inside the module hermetic enclosure. For these reasons, beside the active device modeling, also the accuracy of the modeling of both the MIM capacitors and the bonding wires was an extremely important and critical point. Thin film resistors were also placed between symmetric harms of the output combiner to avoid potential differential instability start-ups.

In *Figure 2.26* the realized power Line-Up is depicted, where Pre Driver, Driver and HPA are easily recognizable.

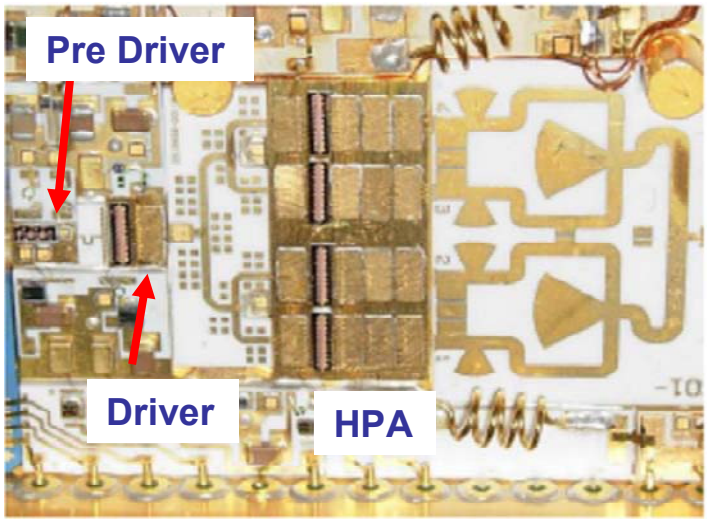


Figure 2.26 - Picture of the entire transmitting line-up.

Measurements of the entire transmitting line up were carried out at Thales Alenia Space Italia laboratories; the figure below shows the main measured performance of the entire Line-Up. The goodness of the described design approach is proved by the high power delivered at the output of the entire TR module, about *50 W*; in effect, de-embedding the results from the overall losses introduced by the connector and the circulator, about *0.35dB*, the only HPA deliver an output power of about *53 Watts*, with a Power Added Efficiency of *53%*. An important result is that an overall power density of about *0.83 W /mm* has been obtained satisfying all the space de-rating constraints.

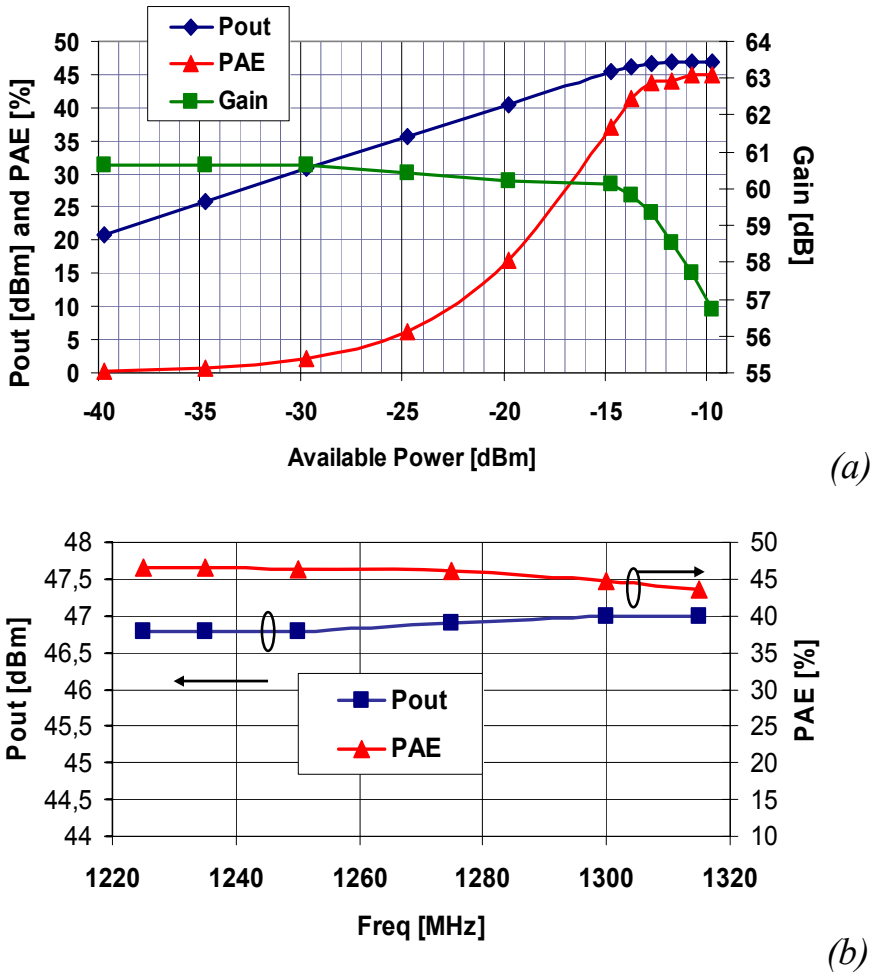


Figure 2.27 - Pulsed output power, gain and PAE of the entire line-up at the circulator output vs. Input Power at 1.275GHz (a). Pout and PAE in the overall frequency band.

2.5 Summary

In this chapter, after a description of the tight constraints required by satellite systems and their influence on the design of HPAs, a design methodology, based on a proper shaping of the ED intrinsic dynamic Load-Line, was explained. Has been demonstrate that imposing a particular shape to the load-line a trade-off between power and efficiency can be reached and, at the same time, electron device currents and voltages related to reliability issues can be directly monitored. To reach the wished results, harmonic tuning is needful and so the load impedance has to be defined not just at the fundamental frequency but also at second and third harmonics.

The proposed method has been verified designing a hybrid L-band high power amplifier to be used in the power line-up of the TR module of a *SAR* (*Synthetic Aperture Radar*) antenna. It was formerly applied to define the optimum load impedance for the elementary active cell of a discrete power bar, then, two amplifier prototypes of *12W* and *42W*, exploiting respectively 1 and 4 power bars, have been implemented and tested to validate the goodness of the method. At the end, the implementation and the measured performances of the entire power line-up of the TR module have been explained.

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Chapter 3

Design of MMIC HPA for Space Applications

In the previous chapter, the proposed design methodology was explained and applied in the design of an L-band Hybrid high power amplifier; the next step is to verify the methodology for higher frequency circuits in a fully integrated solution.

Therefore, in this chapter, after a description of the issues of MMICs (*Microwave Monolithic Integrated Circuits*), the design of a 10 Watt high efficiency HPA for Ku-band Space application will be described. In particular, the final result will be an amplifier to be used in the power section of a downlink satellite transmitter for TT&C (*Telemetry Tacking and Command*) systems. Due to the space application, also in this case, special attention must be put on the process and MMIC reliability: to this aim performances must be guaranteed in de-rated conditions respect to the process maximum ratings and, in addition, the channel temperature of the active devices must be kept within the value established by Space Requirements and carefully controlled. This makes the design objective very tight, but, basing the design on the Load-Line method, both performances and reliability requirement will be satisfied.

3.1 MMICs in Gallium Arsenide Technology

Supported by defense and space industries, design and fabrication of GaAs (*Gallium Arsenide*) circuits have been, in the last decade, a prominent growth to be applied in high frequency circuits for radars and secure communications, where high reliability levels are essential. Some of the advances achieved with GaAs technology included the use of higher frequencies to avoid spectrum crowding, new digital transmission techniques that require linear amplifiers at higher RF power levels, and lower voltage/lower current amplifiers to maximize the operating and standby times of equipment that had to be powered by batteries.

As seen in the previous chapter, the GaAs technology is largely exploited in the design of Hybrid circuits but, especially at high frequencies, the enhancement of the Monolithic solutions - where the active and passive components are formed on the substrate - allowed to solve many problems in terms of performances, reliability, accuracy of the design, space and cost. The monolithic microwave integrated circuit uses an insulating crystalline material as both the dielectric and the active layer material. For many new applications, GaAs has become the material of choice because of its ability to perform at high frequencies. It also has a high-resistivity semi-insulating property that reduces cross talk between devices. This permits the integration of active (radiofrequency) devices, control (logic) devices, transmission lines, and passive elements on a single substrate.

At the other hand, unlike the hybrid MICs, a GaAs MMIC's performance cannot be easily "tuned" by adjusting lumped or distributed elements. Once the circuit is processed, its performances are, for the most part, set. Therefore, the design of the MMIC must be based on accurate physical and electrical models for both the passive and active elements, including effects due to manufacturing process tolerances. This design process uses powerful interactive software programs for the synthesis, analysis, and layout of linear and nonlinear circuits.

In comparison to the other forms of microwave technology, GaAs MMICs offer the following advantages:

(1) Size and weight reduction.

(2) Cost reduction for medium- to large-scale production volumes.

(3) Enhanced system performance from the inclusion of several functions (e.g., RF and logic) on a single circuit.

(4) Enhanced reproducibility from uniform processing and integration of all parts of the circuit.

(5) Enhanced reliability from integration and process-control improvements.

(6) Wider frequency-bandwidth performance from the reduction of parasitics in discrete device packaging.

(7) Design performance realized without several iterations—the result of processing and material repeatability, and computer-aided design enhancement.

For all kinds of space applications, the MMICs solutions provide the optimization of space and mass of the satellite apparatus, with a consequent reduction of the overall power consumption. In the particular case of a TT&C system of geostationary satellite, where Telemetry, Tracking and Command are vital functions for the satellite survival, the availability of a fully integrated HPA with high power and efficiency permits to substitute the actually used hybrid power section with a more compact and reliable transmitter (*Figure 3.1*).

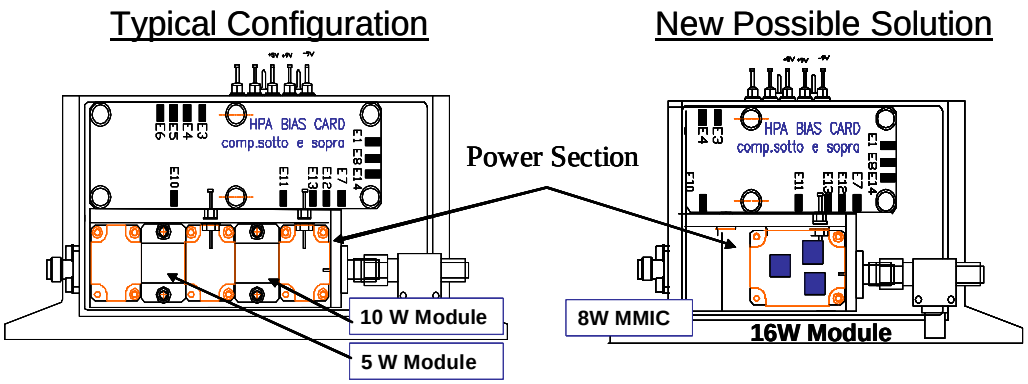

Figure 3.1 - Comparison between the actual configuration and the new possible solution for the power section of the TT&C Transmitter.

In effect, for satellite transmitters, until the end of the past decade, the final power stage has usually been provided by hybrid amplifiers [1] or pre-matched FET mini-modules [2], delivered in hermetic sealed ceramic packages, while availability of GaAs p-HEMT and HBT processes with very high power densities gives nowadays the opportunity to synthesize these functions in a monolithic die, with obvious advantages in terms of cost, space, reliability and performance reproducibility. For all these

reasons, in the paragraphs below, the opportunity to enhance the MMIC performance by the Load-Line design methodology will be investigated.

3.2 MMIC HPA Design

In the context described above, a 10 Watt monolithic power amplifier at Ku band has been designed and developed exploiting a commercial p-HEMT power process to be used as the final stage of an on-board transmitter. The state of the art maximum power level achieved with the mentioned technologies for a monolithic amplifier at X and Ku band is around *40 dBm* [3]-[4] with fabrication process used near the maximum ratings (i.e. without the space de-rating compliance). Comparable performances are achieved for a space product, exploiting a high performance p-HEMT process and applying the proposed design methodology, an accurate design strategy for the optimization of output power and efficiency.

To reach a high output power, a large number of active devices have to be adopted in the amplifier output stage, thus, a special attention must be focused on the stability analysis (especially the odd-mode instability must be prevented). Another fundamental point in the design for space applications is to guarantee high reliability and to this aim the performances have to be reached by keeping the device operating conditions at a proper de-rating with respect to the process maximum ratings provided by the foundry and imposed by the particular application. Since one of the fundamental goal is the highest output power, the V_{DS} breakdown voltage and the maximum channel temperature of the devices are the constrains which represent the biggest challenge. In fact, on one side the reliability is strongly dependent on the channel temperature and the peak voltages, while the maximum output power is limited by the V_{DS} breakdown. The design focus is on the choice of a proper bias and dynamic load line which are able to optimize circuit performances like power and efficiency within the de-rated operating conditions.

In sections below, the single cell performance, in terms of power added efficiency (PAE), output power and gain, and the amplifier design flow will be described.

Process Characteristics

As did for the Hybrid HPAs described in the previous chapter, a space qualified *0.35µm* gate length GaAs p-HEMT process from Triquint Semiconductors Texas was selected for this application. Calling back its characteristics, this process has a V_{DS} breakdown exceeding *24 Volts*, a maximum current density of *650 mA/mm* and can reach *1.2 W/mm* power density at *10 GHz* at maximum ratings; due to the space application constraints, MMIC performances must be obtained using devices at de-rated conditions. For this application, these were identified as *20%* de-rating on breakdown voltages and current densities. A power cell with *1440 um* of active periphery (12 gate fingers, 120 µm width) has been selected for both the final and driver stages. In order to achieve the best power performance and to assure a junction temperature to guarantee reliability (*MTBF* greater than $5x10^7$), a strongly symmetrical two stage amplifier solution was adopted, with 8 devices in the final stage and 4 devices as drivers, maintaining a 2:1 active periphery ratio between the two stages.

Single Cell Performances

A sample of the power cells chosen for the HPA has been fully characterized in small and large signal conditions in order to verify the electrical models accuracy. Small signal measure has been performed in a de-rated bias condition, to maintain the temperature of the device under the limits suggested by the foundry and also to adopt the same bias point available for the linear electrical model.

Figure 3.2 shows the Source/Load Pull system used to define the best load and source impedances for both maximum output power and maximum PAE of the single power cell; even though the system allows to carefully control the impedances at one frequency up to 26.5 GHz, it gives the opportunity to track also the second and the third harmonics. As can be seen below, the results of large signal measurements fully match the optimum impedance analysis performed with the Harmonic Balance simulations using Agilent's ADS (Advanced Design System) and the TOM3 model provided by the Foundry.

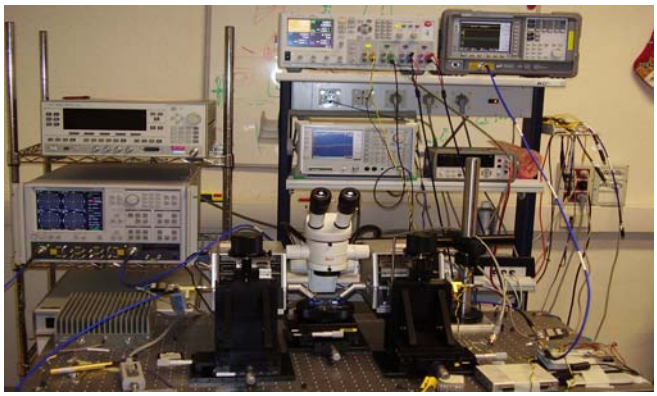

Figure 3.2 - Source/Load Pull measurement bench. The bench includes also instrumentations needful for the calibration procedures.

The need to maintain the channel temperature of the devices below *130°C*, for each electrical condition and at the maximum ambient temperature of about *70°C*, and to work in a high efficiency condition, imposes to choose the AB class as the operating condition for the devices used in the final stage of the amplifier, corresponding to the quiescent Bias values indicated in the table below.

Quiescent Bias Point		
V_{ds} = *9.6 V*	I_{ds} = *115 mA*	V_{gs} = *-0.65 V*

Table 3.1 - Polarization values of the single active cell of the HPA.

Considering that for this technology, in maximum rating conditions, the Drain-Source breakdown voltage could exceed about *24 Volts*, the V_{ds} of *9.6 V* allows to comply the derating of *20%* imposed by the application.

Also in this case, the stability of each active device inside the MMIC has been assured with a lumped RC network in series with the gate: in this way the device is made unconditionally stable from *200 MHz* upward, ensuring a good trade-off with the achievable gain. *Figure 3.3* shows a schematic and a picture of that network and its effects on the stability factor μ and on the Maximum Available Gain (*MAG*) of the *1440µm* device. This network can avoid common mode instabilities, but it is not adequate to prevent also differential mode instabilities; this problem will be discussed in a next section, when all the matching networks will be defined.

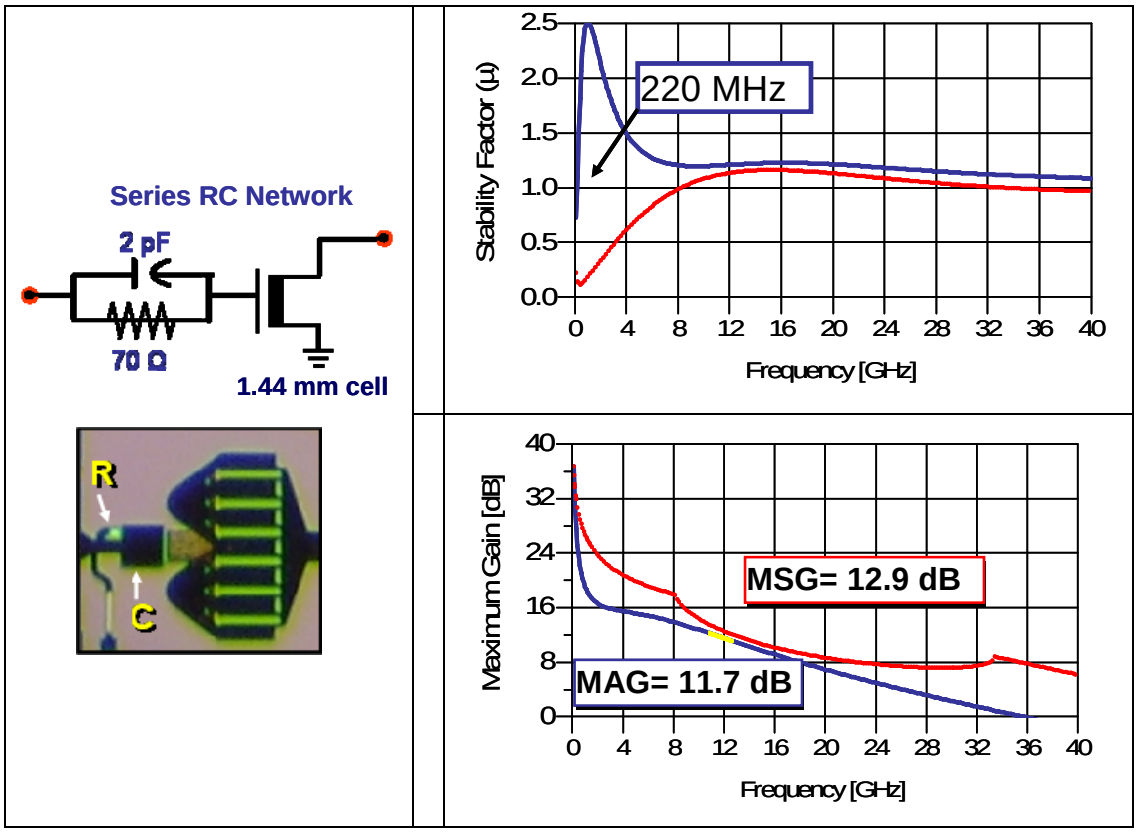

Figure 3.3 - Stabilizing Network for the 1.44 mm Cell; stability factor and available Gain before and after the stabilization.

Once defined the proper Bias conditions and stabilized the single device, the Load-Line method can be applied, in order to find the best load for optimization of output power, efficiency and reliability. For the final application, the frequency range form *10.7 GHz* to *12.7 GHz* was considered but, has explained before, a tuning operation on the 2nd and 3rd harmonics has to be implemented.

Figure 3.4 shows how the synthesized Load-Line, at the intrinsic terminals of the devices exploited in the final stage, matches the best load conditions to optimize both power and efficiency, assuring, at the same time, adequate margins form the Breakdown voltage. In effect, as depicted in the picture, the chosen load impedance at the fundamental frequency is inside the both contours at maximum PAE and output power, carried out form the Load-Pull measurements. The high frequency of the application poses some issues in performing an accurate tuning at 2nd and 3rd harmonics, which are at *25* and *34 GHz*. Taking into account the intrinsic limitations of the monolithic solution, in terms of space and Q-factor of the lumped elements, the load impedances synthesized at the harmonics however allow the device to work in a low dissipative region.

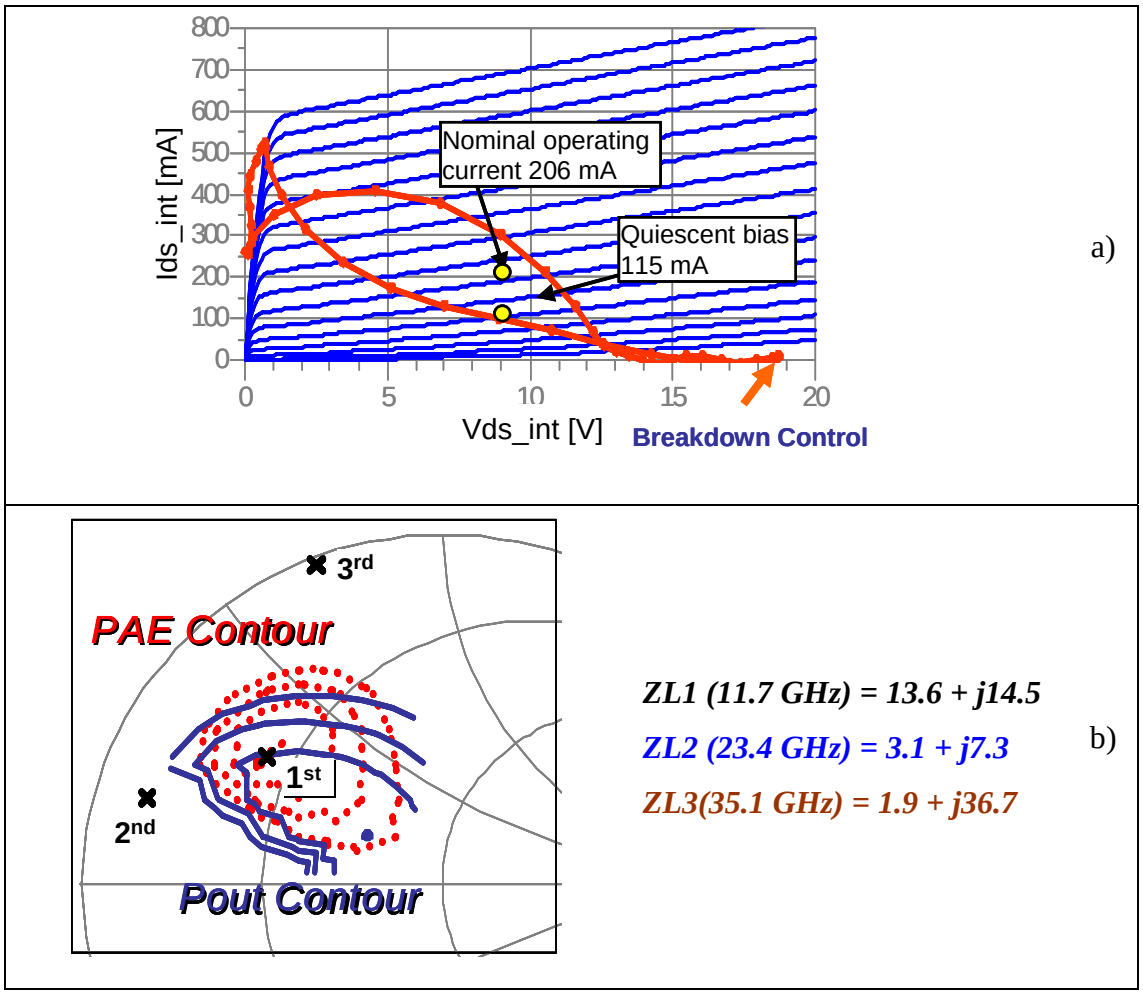

Figure 3.4 - Harmonic tuned dynamic Load-Line superimposed on the pulsed I-V characteristics (a); Load Impedance at fundamental frequency compared with measured PAE and Output Power Load-Pull contour.

The situation depicted in the figure above refers to an operating condition of 2 dB gain compression: by proper selection of drain and gate bias and the adequate tailoring of the load line the simulated maximum V_{DS} voltage is below *19 V*, which is more than *20%* lower than breakdown (*24V*). Moreover, under large signal conditions, due to non-linear DC conversion, the drain average current I_D rises form *115 mA* to *206 mA*. This condition allows to obtain from a single cell an output saturated power of about *1.5 Watts* with *56% PAE* at 2 dB compression point, while the junction temperature, for both final and driver active devices, is kept under *130°C* with a base plate temperature of *70°C*. To accurately estimate the thermal behavior of the active devices, a thermal simulator based on a finite difference solver has been adopted. By analysis, a thermal resistance of about *65.5°C/W* for the *12x120 µm* device has been extracted.

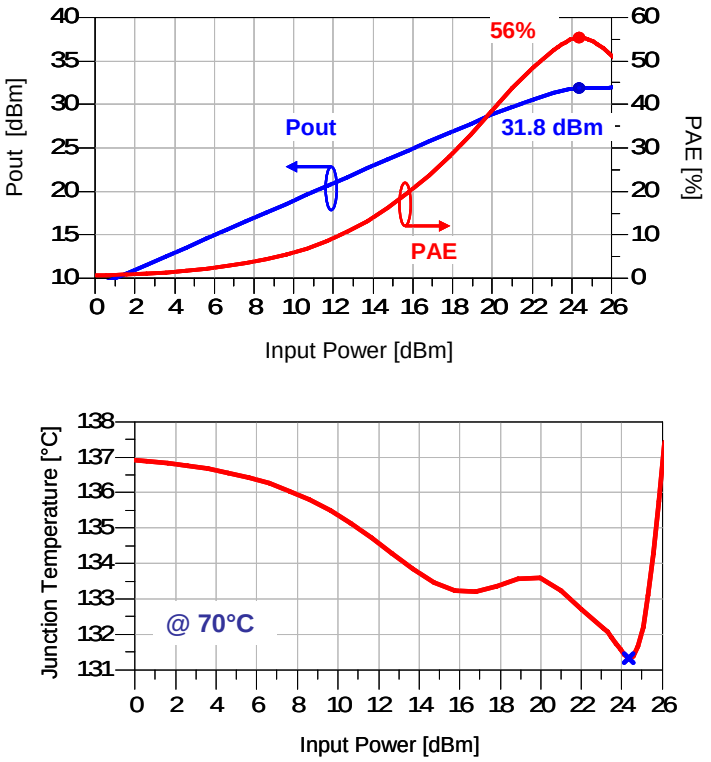

Figure 3.5 - Output Power, PAE and Junction temperature for the 12x120 device loaded with the impedance of Figure 3.4.

HPA Design

Once defined the best load impedances for the single device, the entire power amplifier has to be dimensioned, designing the output matching network, to proper load each device in the final stage, the inter-stage and input networks, to reach the desired performances in terms of Gain, Gain flatness and Return Loss.

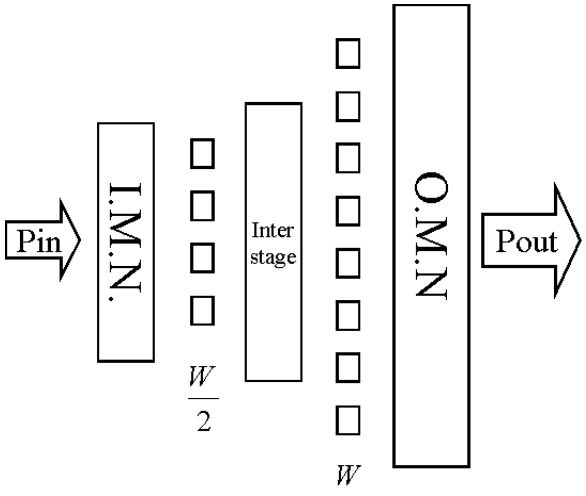

Figure 3.6 - HPA schematic topology.

As *Figure 3.6* shows, the HPA is characterized by two stages of gain, exploiting *8* active devices, of *1.44mm* each, in the final stage and *4* devices of same periphery in the driver stage. The choice to maintain a 2:1 ratio between the two stages is to have at the input of the final cells the needed power to be driven to the desired conditions of operation.

A strongly symmetrical output network was designed to combine the 8 devices in the final stage, for a total active periphery of about *11.52 mm*; the network is composed by a bus bar structure, cascaded with a 4:1 tree combining network. The outputs of the last stage devices are connected together through the wide bus bar which feeds the DC current to all the drains. Shunt MIM capacitors are placed at proper symmetric points on the bus bar and the RF power is tapped off at other symmetric points along the bar. In this way the drain bias path does not need a conventional RF choke, and a decoupling shunt capacitor is sufficient to decouple the path to the external DC circuitry [5].

The 4:1 tree combining network completes the impedance transformation by means of distributed (microstrip lines) and lumped (shunt capacitors) elements. The thick metal layer provided by the process (three metal layers are available for a total thickness of 6.7 um) and the good Q factor of the lumped elements adopted are able to guarantee a very low loss output network (about *0.5 dB*), which improves the total circuit efficiency and the amplifier output power.

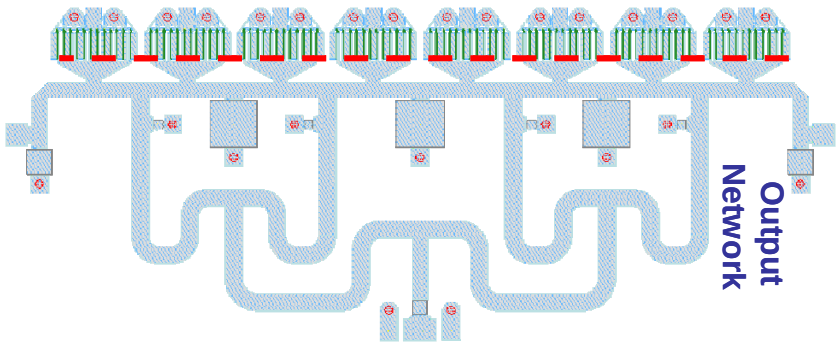

Figure 3.7 - Final stage of the HPA with the 8 devices and the output matching network.

With the adopted solution the (*Figure 3.7*), symmetry of the structure plays a fundamental role in the synthesis of the load impedances, because identical operating conditions must to be imposed to all the final cells. To verify that, the load admittances of the devices are shown in *Figure 3.8*, where the crosses represent the optimum for

both real and imaginary parts of the admittances and the curves show that the realised impedances for the 8 devices are practically identical.

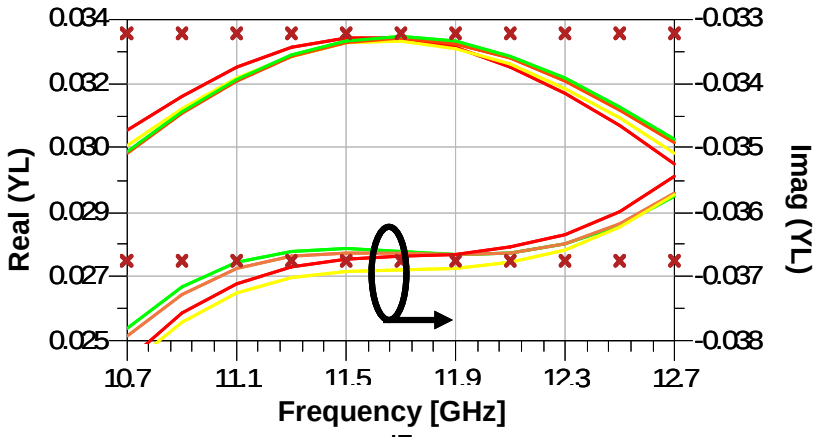

Figure 3.8 - Real and Imaginary parts of the admittances synthesized at the out of the 8 devices in the final stage.

The inter-stage network design has been carried out considering a trade-off between different factors: layout dimension and topology, load impedance of the driver cells and gain flatness: a flat gain has to be obtained in a 20% bandwidth. The 2:1 combining network and the 1:4 splitting network have been designed to preserve a symmetrical structure, while the choice to carry the RF signal to one central point (red circle in *Figure 3.9*) and then to split it to the final cells has the aim to avoid some possible spurious paths between the two stages, which can trigger some differential mode oscillations. In the inter-stage network some losses have been necessarily added in order to obtain a good flatness of the gain.

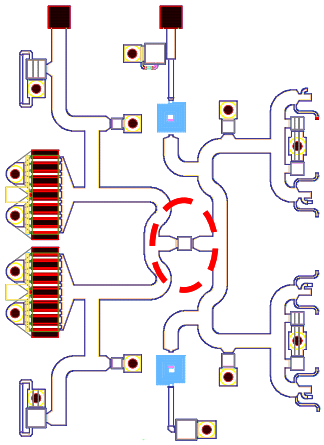

Figure 3.9 - A section of the Inter-stage network.

Concerning the Input Matching Network, a 2 dB resistor attenuator has been added to the RF path and it is composed by a 1:4 power splitter, with the scope to improve the input return loss and to give the desired shape to the gain over all the bandwidth.

The realized MMIC has a very compact dimension (*4.7mm* x *4mm*) and it is pictured in *Figure 3.10*. The high frequency of the application imposes every passive structure to be simulated electromagnetically, in order to verify the relative electrical models and to taking into account possible coupling between nearest lines.

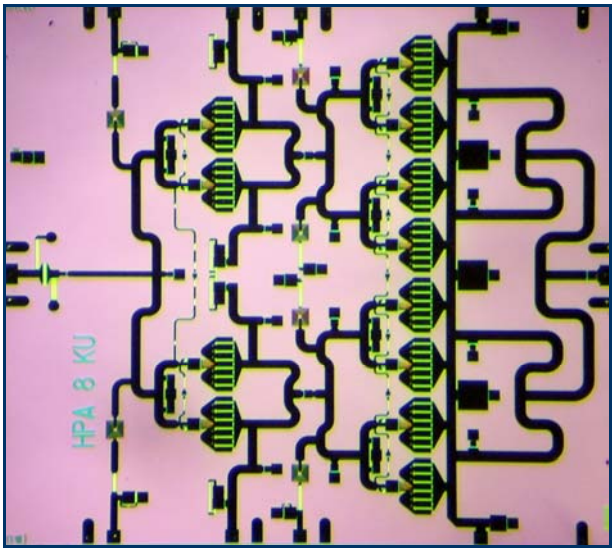

Figure 3.10 - Picture of the MMIC High Power Amplifier.

In a structure with such number of devices, even tough the devices are made unconditionally stable, a deep analysis of possible differential mode instabilities is compulsory. In this case by means of a suitable CAD tool, the analysis suggested by Ohtomo has been performed considering up to 24 possible feedback-loops. Then, applying the Nyquist criterion on the obtained open-loop transfer functions, it results that some differential instabilities could start up. As can be seen form the picture, carefully dimensioned resistive branches have been introduced between the symmetrical points of the circuit identified as more sensitive to potential differential instability. *Figure 3.11* shows the effect of the resistances on the open transfer functions in the polar diagram; basing on Nyquist criterion, when an open-loop transfer function crosses the real axis of the polar diagram after the value 1 (blu line), instability could sturt up. The inner curve shows that, after the insertion of resistive branches, that condition is no longer valid.

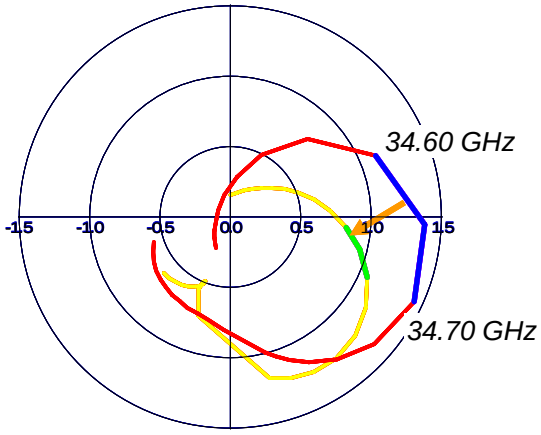

Figure 3.11 - Effect of the resistive branches on the potential start up of differential instabilities.

3.3 HPA - Measured Performances

To fully verify the design methodology applied for the realization of the Ku-band MMIC amplifier, the measured performances will be now illustrated.

A preliminary small-signal characterization of the MMIC was carried out directly on wafer in order to test the chip performance without the influence of the external circuitry. Due to the poor thermal dissipation of the on-wafer measurement system, the scattering parameters have been first measured at a de-rated bias condition to keep the device temperature within the maximum limits.

For proper characterization (small signal and power) at the nominal operating point, the test jig shown in *Figure 3.12* has been used. The die has been attached on a gilded brass carrier using epoxy glue, with high thermal and electrical conductivity, and then bonded to the test circuit, that includes off-chip decoupling capacitors, implemented on a high frequency laminate. The test board has been then mounted on a cooling system in order to have good control on the base plate temperature. Due to the high operating frequencies, the effect of the access structures (including bonding wires) was considered during the design of input and output matching networks. A TRL calibration kit, carried out on the same substrate of the test board, allowed the proper de-embedding of the whole test jig.

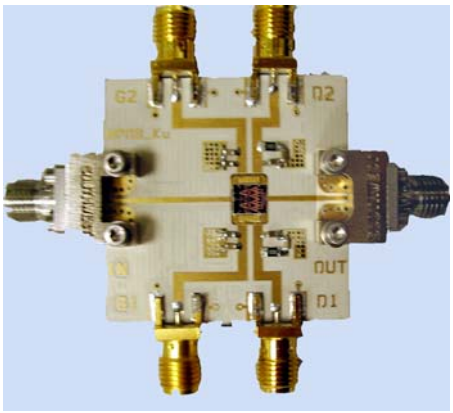

Figure 3.12 -Test Jig developed for the Amplifier Characterization.

As shown in *Figure 3.13*, measured small-signal gain is not less than *11.5 dB* with a flatness of about *±1.5 dB* over the frequency range. The input VSWR does not exceed *2:1* between *11.3 GHz* and *12.7 GHz*, while the output VSWR does not exceed *1.6:1* in the bandwidth of interest.

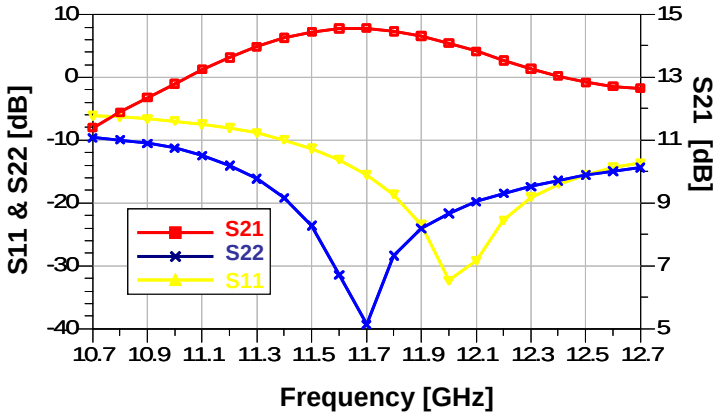

Figure 3.13 - Small Signal amplifier measurements: S(1,1) triangles, S(2,2) cross and S(2,1) squares. These measurements have been done in the nominal quiescent bias condition.

Figure 3.14 shows power gain, output power and PAE plotted as a function of the available input power at *11.7 GHz*. As can be seen, an output power of *10 Watts* is obtained at 2 dB gain compression with a PAE higher than *47%*. An important result is the high power density obtained despite the tight space constrains and dimensions: indeed, taking into account *11.52 mm* of active periphery, the computed power density is *0.87 W/mm*, representing the state of the art in this particular field of application.

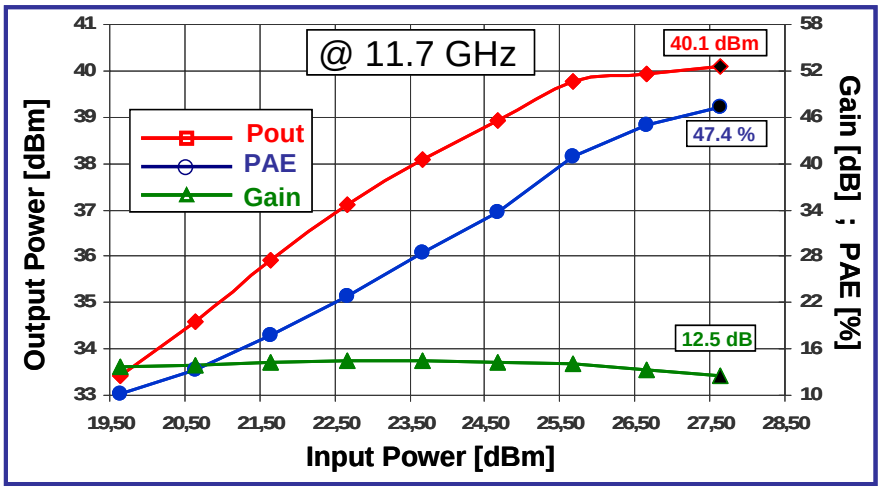

Figure 3.14 - Power Gain, Output Power and PAE @11.7 GHz as a function of input power.

Figure 3.15 shows output power, PAE and Gain at 2 dB gain compression for the entire bandwidth. Measurements show *8 Watts* of output power over the bandwidth with a peak of *10 Watts* at *11.7 GHz*. The power gain ripple is within 2 dB.

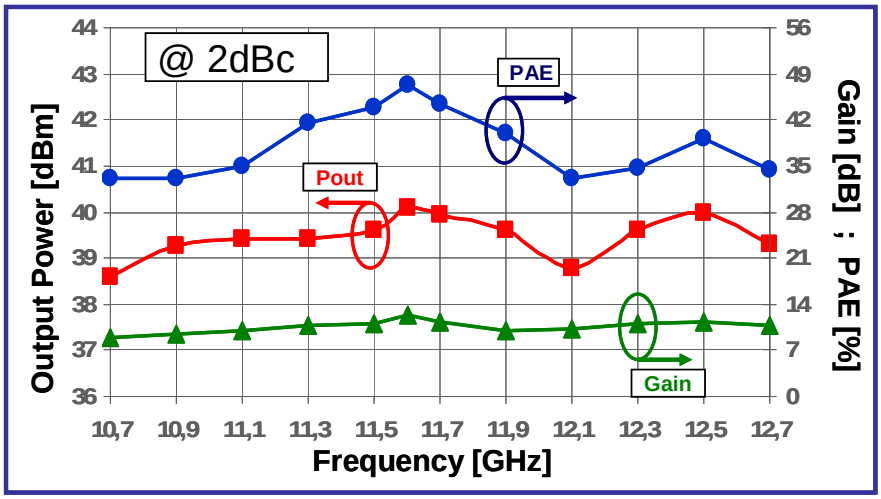

Figure 3.15 - Power Gain, Output Power and PAE slope within the frequency band at 2 dB gain compression point.

The chosen Bias Point, the defined operating conditions and the shaping applied to the intrinsic Load-Lines, for both Driver and Final devices, assure levels of MTBF (*Mean Time Before Failure*) compliant with the space application constrains. *Figure 3.16* shows the channel temperatures for Driver and Final Devices as a function of the input power, at the maximum ambient temperature foreseen by the application; in particular, when only the Bias is applied, the worst condition, the MTBF index is over than 40 millions of hours, while in the operating condition, with the RF applied, the Mean Time Before Failure rises up to 50 millions of hours.

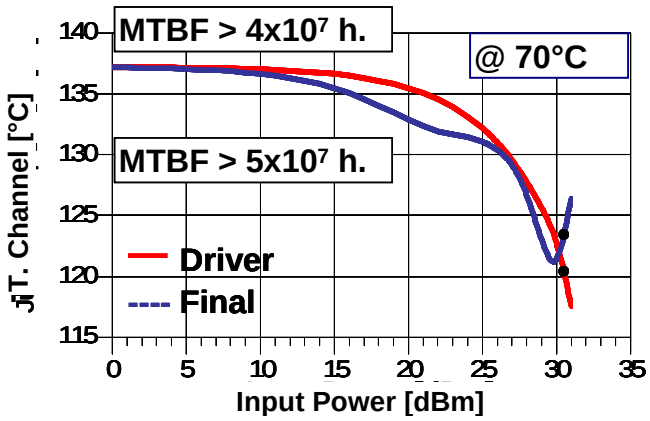

Figure 3.16 - Channel temperature vs. input power for both Driver and Final devices @ 70°C.

3.4 Summary

In this chapter the design methodology, based on a proper shaping of the Electron Device intrinsic dynamic Load Line, has been verified designing a fully monolithic Ku-band high power amplifier. While in the previous chapter the new approach was applied for a hybrid L-band amplifier, here the intrinsic issues of the MMIC solution and of the higher frequency of operation posed new challenges.

In detail, a fully monolithic high power amplifier for space applications has been described. The use of a specific p-HEMT process, tailored for high power density in Ku band, and the proper design technique, allowed the development of a single MMIC that can potentially replace the functionality of big and expensive modules based on discrete devices. The amplifier is capable to deliver up to *10 Watts* of output power with a *47 %* of power added efficiency at *11.7 GHz*. Along the *2 GHz* bandwidth (*10.7 GHz* to *12.7 GHz*) an output power higher than *8 Watts* was obtained in conjunction with a minimum of *33 %* PAE.

In all design steps, all the tight constrains imposed by the TT&C application have been considered and satisfied; the proper shaping of the ED dynamic Load Line allowed to reach the best trade-off between power and efficiency performances and high power density, with the consequent reduction of maximum channel temperatures and the optimization of the area occupation and of the power consumption.

References

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Chapter 4

Experimental Characterization of the Intrinsic Electron-Device Load-line

The design methodology proposed in previous chapters is based on the assumption that designer has the availability of an accurate electrical model of the devices, in order to accurately control the shape of the intrinsic dynamic Load-Line; the variety of publications about this argument demonstrates that it is so difficult to carry out a CAD model capable to taking into account all the non-ideal phenomena which occur when the amplifier operates at high frequencies and power levels. Those difficulties are more considerable especially for the emerging technology of Gallium Nitride (GaN), characterized by very high electric fields and power levels; the need to exploit the high performances, of which this kind of technology is capable, collides with the hindrances in carrying out an accurate electrical model, due, first of all, to the presence of some critical phenomena like high level of carrier injection, low frequency dispersion (Traps and Thermal Effects) and RF Walkout.

For all these reasons, taking into account the described Load-Line method, a new, original approach for power amplifier design was defined, mainly based on low-frequency, nonlinear empirical electron device characterization. The proposed technique enables the same level of accuracy provided by expensive load-pull measurement systems to be obtained through a relatively simple and low-cost setup. Moreover, electron device currents and voltages related to reliability issues can be directly monitored.

At the end of this chapter, the design and the implementation of a hybrid high power amplifier in GaN technology will be described, as verification of the proposed experimental methodology.

4.1 Limitations of Experimental Design Methods

Previous chapters explained how power amplifier design represents a key aspect in order to meet the severe performance (e.g., efficiency, reliability) required for modern micro- and millimeter-wave systems. As seen before, such a kind of circuit is usually designed by exploiting a mix of three different approaches: Cripps load-line theory, load-pull measurements, and iterative harmonic-balance analyses based on nonlinear models of electron devices (ED).

The Cripps load-line theory exploits, in its original version, an elementary electron device description (i.e., zero knee voltage, zero output conductance, and linear transconductance except for the pinch-off and hard saturation at the maximum allowable current) based on static current\voltage (I\V) output characteristics. Such an approach is limited by the simplified device description. For instance, due to the hard saturation mechanism, it cannot be adopted when dealing with high distorted regimes. Moreover, since low-frequency dispersion (i.e., traps and thermal effects [1-5]) is totally neglected, the Cripps load-line method is not particularly adequate for exploring emerging technologies (e.g., GaN, SiC) where dispersive effects usually play a major role. Finally, as clearly stated in *Chapter 1*, such a technique has to be considered only as a starting point for power amplifier design.

Load-pull measurements, based on both passive and active load synthesis, represent the most common aid for power amplifier design. Indeed electron devices can be characterized under actual operating conditions, by imposing different input and output impedances at the device ports. However, load-pull setups are frequency and power limited, and their cost dramatically increases when high operating power and/or frequencies are required.

A major limitation of this technique is related to the difficulty in synthesizing the full range of device terminations: especially when on-wafer devices having a large periphery are considered, passive load-pull suffers from the inability to synthesize very low impedances, whereas active load-pull may become critical from the stability point of view. Moreover, once load-pull contours have been drawn, no information is given about the intrinsic ED load-line: loading conditions which show similar microwave performance can correspond to very different load-lines at the intrinsic device. As widely described before, this is a vital aspect since reliability conditions are defined at the intrinsic ED ports as the passive access structures to the active area do not have any

major impact on reliability (for instance, the device breakdown condition is related to the breakdown of the intrinsic gate-drain diode).

High-frequency time-domain measurement systems (large-signal network analyzers - LSNA), which provide a vectorial information, do not overcome the above problem since the measured load-line still refers to the extrinsic device. Moreover, the frequency restriction of LSNAs limits their application.

Preliminary design choices carried out by means of load-line theory and/or load-pull measurements represent the starting point for successive power amplifier design refinements based on harmonic-balance analyses. These ones obviously rely on the accuracy of the electron device models adopted. An accurate model could overcome the need for load-pull measurements: in principle, load-pull contours could be traced by using simulation results only. In practice, however, electron device models usually available from the foundries, provide accurate nonlinear performance prediction only in a relatively narrow neighborhood of given bias and load conditions [6]. Thus, the availability of a load-pull (or a similar one) measurement system is always a valuable aid.

In this chapter an alternative, original approach to power amplifier design is proposed which overcomes the major problems previously mentioned. It is mainly based on low-frequency, nonlinear experimental electron device characterization and enables the same level of accuracy provided by load-pull measurements to be obtained through a relatively simple and low-cost setup. Moreover, device currents and voltages compatible with reliability requirements can be directly monitored. The aim of this work is to demonstrate the validity of the proposed approach in providing valuable information for power amplifier design, whereas specific design techniques are not dealt with.

4.2 Nonlinear Device Modeling Issues

Figure 4.1 shows a nonlinear equivalent circuit model for a FET device; we will focus on such a kind of electron device since it plays a major role in micro- and millimeter-wave power amplifier design, nevertheless the following considerations could be extended to bipolar transistors too.

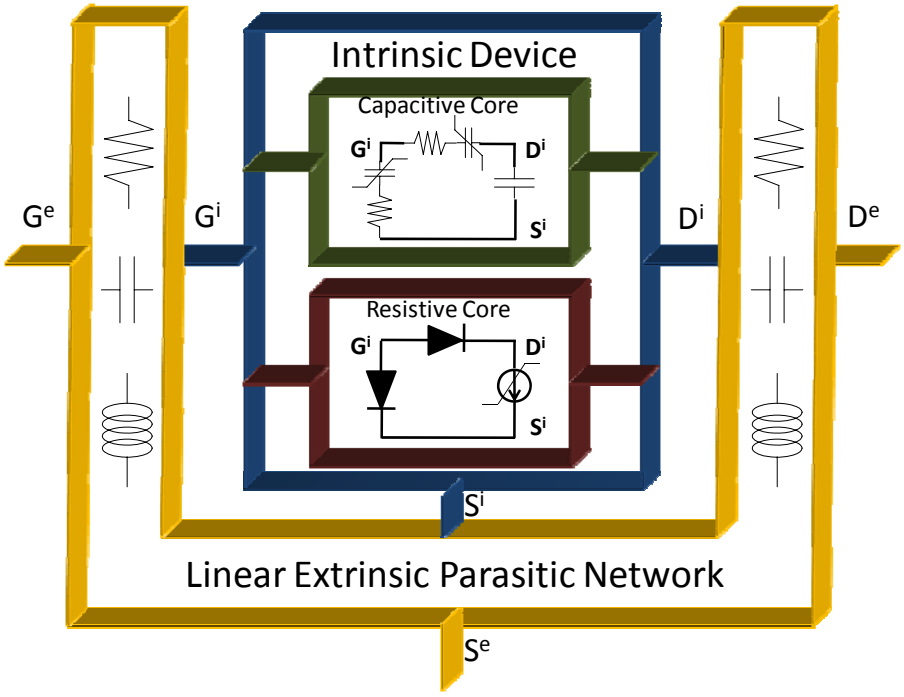


Figure 4.1 - Nonlinear equivalent circuit for a FET electron device.

The linear extrinsic parasitic network in the figure above describes the access passive structure to the device active area and accounts for metallization and dielectric losses as well as for associated inductive and capacitive effects. Its correct modelling is a fundamental issue to obtain accurate model predictions. Parasitic elements can be characterised by exploiting conventional lumped descriptions [7-8], which can be identified by only using small-signal measurements, or, alternatively, by adopting electro-magnetic simulations of the device layout [9-10]. As clearly shown in *Figure 4.1*, the *"intrinsic device"* can be divided into two parts, which can be considered strictly in parallel: a "*capacitive core"* describing the nonlinear dynamic phenomena, and a "*resistive core"* accounting for the dc and low-frequency (LF)

I\V device characteristics. The latter ones differ from the dc response due to surface state densities, deep-level traps and thermal phenomena.

The ED resistive core modelling is extremely complex, not only because a number of important nonlinear phenomena must be considered (e.g., breakdown, forward conduction of the gate-source diode, knee of the I\V curves, etc..) but also due to the non negligible presence of dispersive effects [1-5], which, de facto, impose the exploitation of nonlinear dynamic measurements in order to obtain good prediction capabilities. To probe further this issue we must consider that the drain and gate currents at the intrinsic ED ports, above the cut-off of LF dispersive effects (i.e., some hundreds of kilohertz) but at frequencies low enough to neglect the reactive effects related to the capacitive core, can be expressed as follows (4.1 and 4.2):

$$i_g(t) = h\left(\underline{v}(t), P_0, \theta_{case}\right) \qquad (4.1)$$

$$i_d(t) = f\left(\underline{v}(t), V_0, P_0, \theta_{case}\right) \qquad (4.2)$$

In (1.1), h and f are two algebraic (i.e., memory-less) functions, $\underline{v}$ is the vector of the intrinsic voltages, V_0 its average value, P_0 the average dissipated power, and, lastly, θ_{case} is the device case temperature. The dependence on V_0 accounts for the influence of traps and surface state densities [1-4], while P_0 and θ_{case} determine, through the thermal resistance, the device I\V characteristic dependence on the junction temperature. Identification of (4.1), in particular the drain current equation, is quite a prohibitive task mostly due to the complex dependence on its large number of controlling variables. Moreover, traps and thermal effects can not be separately dealt with, both because the time constants of those phenomena are not always different and also since the device thermal state influences the trapping state [2]-[11]. Thus identification of (4.1) necessarily requires the introduction of suitable approximations to make the problem affordable.

A number of LF modelling approaches have been proposed in the literature [1-5] both based on look-up tables or analytical expressions. Some of them introduce assumptions which enable the models to be identified on the basis of bias-dependent dc and ac small-signal differential measurements carried out above the cut-off of low-frequency dispersion. However, in practice, model accuracy is commonly improved by

exploiting in the identification phase, besides ac and dc measurements, large-signal dynamic measurements as, for instance, pulsed I\V characteristics [12-13]. Despite the use of quite expensive, special-purpose pulsed I\V setup's, the identification of an accurate, *global* model for the resistive core still remains a very complex and hard task and this justifies why foundry models often properly work in a limited number of given quiescent bias conditions: typically, a limited set of pulsed I\V measurements is fitted. Such a kind of approach inevitably leads to *local* models which cannot provide accurate information outside the range of the few quiescent bias conditions considered.

As far as the capacitive core is concerned, dispersive phenomena due to traps and thermal behaviour represent second order effects regularly neglected in electron device models oriented to power amplifier design [14-20]. A π model of capacitors (usually assuming C_{gs} and C_{gd} nonlinearly dependent on the intrinsic device voltages, and C_{ds} constant) is often adopted; as an alternative, gate-source and gate-drain RC series, as shown in *Figure 4.1*, are introduced to describe nonquasi-static effects which accounts for a finite device memory time. Provided a careful de-embedding of the parasitic network is carried out, small-signal, bias/frequency-dependent S-parameter measurements are usually sufficient to accurately determine the voltage-dependent capacitor values. These ones can be "fitted" trough suitable analytical expressions, or directly stored into look-up tables to build a nonlinear dynamic model. Even problems related to charge conservation, although dealt with in the literature, do not seem to represent a major problem once suitable expedients are adopted [21-22].

To summarise, mostly due to low-frequency dispersion phenomena and important nonlinear effects, the modelling of the resistive core is by far the most complex issues in nonlinear ED modelling while the capacitive core can be more easily identified. This assumption represents the basis of the new design approach introduced in the following and preliminarily justifies why it provides excellent results despite its inherent simplicity.

4.3 The Proposed Approach

As a possible alternative and additional aid to power amplifier design based on nonlinear ED models and load-pull measurements, a new approach is presented here. The aim is to overcome the accuracy limitations due to the complex modeling of the ED resistive core, by using a direct experimental characterization of the LF I\V load-line. To this end, the measurement system shown in *Figure 4.2* has been adopted which is based on sinusoidal excitations: a *2 MHz* fundamental frequency is conveniently adopted in order to operate well above the cut-off of LF dispersive effects. Such a setup is similar to the one described in [23] but in the present work both the channels of the function generator are exploited in order to achieve active load synthesis capabilities.

More precisely, for a given bias, different load conditions can be synthesized by controlling the gate and drain incident signal amplitudes (A_g and A_d) and their relative phase ($\Delta\varphi$). It is worth observing that such a setup can be implemented by means of only general purpose instrumentation (typically available in any microwave laboratory) whereas the most expensive instrument, considering the LF excitation, is a 100-MHz four-channel oscilloscope.

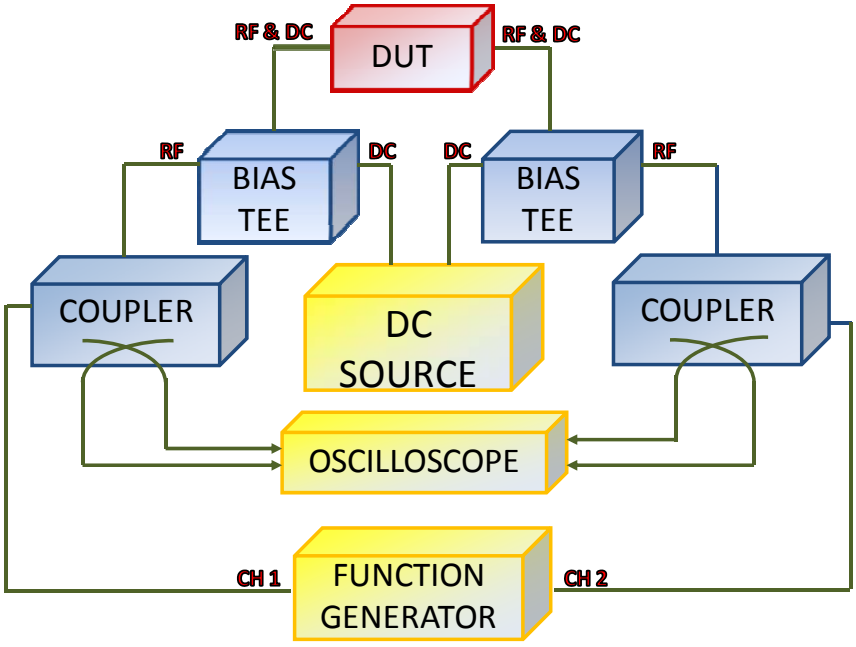


Figure 4.2 - Block-diagram of the measurement system adopted for the LF device characterization.

At the frequencies of few megahertz, the FET representation in *Figure 4.1* is strongly simplified since the parasitic network can be represented by means of parasitic resistances (accounting for metallization and channel access losses), while the reactive elements can be completely neglected. Therefore, the LF load-line synthesized at the external terminals is practically coincident with the load-line imposed at the resistive core of the intrinsic electron device. Since the associated electrical regime uniquely identifies the ED delivered power and efficiency, the set-up in *Figure 4.2* provides an easy way to carry out the choice of the load-line, which defines given power amplifier performance as will be shown more in detail in the following. Moreover, reliability issues related to high-field operations [24-26], which must be considered at the intrinsic device drain-gate terminals, can be directly controlled.

An example of the measurement system capabilities is shown in *Figure 4.3* where measurements performed on an *800-µm GaN HEMT* device biased under class-A operation are shown. The different load-lines were obtained by imposing a constant amplitude of the gate incident signal and sweeping the amplitude of the drain incident signal, moreover two different values of the signals relative phase were considered. It is well evident that the system is fully able to synthesize desired load-lines at the intrinsic device.

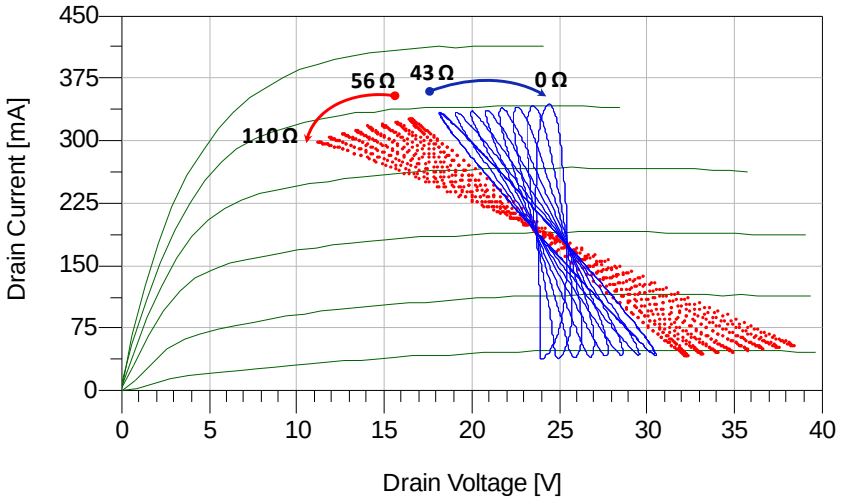


Figure 4.3 - Measurements performed, by exploiting the LF measurement system, on an 800-µm GaN HEMT.

The device is biased at (V_{g0} = *-2 V*, V_{d0} = *25 V*); the amplitude of the gate incident signal is A_g = *1 V*, the amplitude of the drain incident signal is $1\ V \le A_d \le 8V$ and the relative phase is $\Delta\varphi = 0°$ (continuous lines) and $\Delta\varphi = 180°$ (dotted lines). Load-lines

are superimposed to pulsed characteristics (*-3 V* ≤ V_g ≤ *-0.5 V*) carried out from the considered quiescent bias condition.

In order to explain how the LF load-line measured at the extrinsic electron device ports can be used for power amplifier design, it is convenient to express intrinsic and extrinsic voltages and currents in terms of their practically finite number *M* of spectral components:

$$x(t) = \sum_{k=-M}^{M} X(k\omega) \cdot e^{jk\omega t} \tag{4.3}$$

By considering for the parasitic network in *Figure 4.1* any possible topology (based on lumped or distributed elements), intrinsic and extrinsic electrical variables are conveniently related by the following equations in the frequency domain:

$$\begin{bmatrix} V^i{}_{gs}(k\omega) \\ V^i{}_{ds}(k\omega) \\ I^i{}_g(k\omega) \\ I^i{}_d(k\omega) \end{bmatrix} = \underline{H}(k\omega) \cdot \begin{bmatrix} V^e{}_{gs}(k\omega) \\ V^e{}_{ds}(k\omega) \\ I^e{}_g(k\omega) \\ I^e{}_d(k\omega) \end{bmatrix}, \qquad k = -M,...,M \tag{4.4}$$

where $\underline{H}(\omega)$ is a suitable hybrid-matrix description of the linear extrinsic parasitic network. When considering the LF load-line characterization carried out with sinusoidal excitations at the fundamental frequency $\omega = \omega_{LF}$ through the set-up in *Figure 4.2*, $\underline{H}(\omega)$ practically becomes a real and frequency-independent matrix, and (4.4) enables to directly compute, starting from the knowledge of the LF harmonic components of the extrinsic voltages and currents, the intrinsic electrical variables (and, as consequence, the intrinsic load-line) at the electron device resistive core:

$$V^i{}_{gs}(k\omega), \quad V^i{}_{ds}(k\omega), \quad I^i{}_g(k\omega), \quad I^i{}_d(k\omega)$$

.

In order to exploit the LF load-line characterization for microwave power amplifier design, the extrinsic device load and source conditions must be computed,

which enables the electrical regime corresponding to the chosen intrinsic load-line to be imposed at the design frequency. To this end, the displacement currents related to the ED capacitive core must be evaluated according to the following, explicit equations:

$$\begin{bmatrix} i^{i,C}{}_g(t) \\ i^{i,C}{}_d(t) \end{bmatrix} = \begin{bmatrix} \sum_{k=-M}^{k=M} I^{i,C}{}_g(k\omega_{RF}) \cdot e^{jk\omega_{RF}t} \\ \sum_{k=-M}^{k=M} I^{i,C}{}_d(k\omega_{RF}) \cdot e^{jk\omega_{RF}t} \end{bmatrix} = \tag{4.5}$$

$$= \sum_{k=-M}^{k=M} jk\omega_{RF} \underline{C}\left(v^i{}_{gs}(t), v^i{}_{ds}(t)\right) \cdot \begin{bmatrix} v^i{}_{gs}(k\omega_{LF}) \cdot e^{jk\omega_{RF}t} \\ v^i{}_{ds}(k\omega_{LF}) \cdot e^{jk\omega_{RF}t} \end{bmatrix}$$

ω_{RF} being the fundamental operating frequency of the power amplifier with

$$v^i{}_{gs}(t) = \sum_{k=-M}^{k=M} V^i{}_{gs}(k\omega_{LF}) \cdot e^{jk\omega_{RF}t}$$

$$v^i{}_{ds}(t) = \sum_{k=-M}^{k=M} V^i{}_{ds}(k\omega_{LF}) \cdot e^{jk\omega_{RF}t} \tag{4.6}$$

As previously said, the capacitance matrix $\underline{C}$ in (4.5) can be identified on the basis of frequency- and bias-dependent S-parameter measurements. Alternatively, the capacitive core of a suitable, already available, nonlinear model can be used.

Once the harmonic components of the "global" intrinsic currents, composed of the sum of the conduction and displacement currents, have been evaluated:

$$\begin{bmatrix} I^i{}_g(k\omega_{RF}) \\ \\ I^i{}_d(k\omega_{RF}) \end{bmatrix} = \begin{bmatrix} I^{i,R}_{\ g}(k\omega_{RF}) + I^{i,C}_{\ g}(k\omega_{RF}) \\ \\ I^{i,R}_{\ d}(k\omega_{RF}) + I^{i,C}_{\ d}(k\omega_{RF}) \end{bmatrix}, \qquad k = -M,....,M \tag{4.7}$$

the extrinsic electrical variables, which define the load and source extrinsic regime, can be computed by:

$$\begin{bmatrix} V^{e}{}_{gs}(k\omega_{RF}) \\ V^{e}{}_{ds}(k\omega_{RF}) \\ I^{e}{}_{g}(k\omega_{RF}) \\ I^{e}{}_{d}(k\omega_{RF}) \end{bmatrix} = \underline{H}^{-1}(k\omega_{RF}) \cdot \begin{bmatrix} V^{i}{}_{gs}(k\omega_{RF}) \\ V^{i}{}_{gs}(k\omega_{RF}) \\ I^{i}{}_{g}(k\omega_{RF}) \\ I^{i}{}_{d}(k\omega_{RF}) \end{bmatrix}, \qquad k = -M \tag{4.8}$$

and finally, the load impedance at the fundamental and harmonic frequencies can be obtained:

$$Z_{L}(k\omega_{RF}) = -\frac{V^{e}{}_{ds}(k\omega_{RF})}{I^{e}{}_{d}(k\omega_{RF})} \tag{4.9}$$

In addition, also the input device "large-signal impedance" can be easily computed:

$$Z_{IN}(k\omega_{RF}) = -\frac{V^{e}{}_{gs}(k\omega_{RF})}{I^{e}{}_{g}(k\omega_{RF})} \tag{4.10}$$

which, for instance, can be used to synthesize the optimum source impedance (i.e., $Z_s = conj(Z_{IN})$) which provides a matching condition under large-signal operation. It should be outlined that this information is not obtainable through scalar load-pull systems, but only by adopting a time-domain load-pull measurement setup.

To summarize, the proposed approach, which is based on low-frequency, large-signal measurements and bias/frequency-dependent small-signal measurements performed in the frequency range of interest for the considered design, is fully able to provide the same kind of information obtainable by means of expensive nonlinear measurement setups operating at microwave frequencies. The only assumption is that a negligible uncertainty can be achieved in the description of the intrinsic ED capacitive core. As will be demonstrated in the following paragraph, by adopting very different experimental examples, such a hypothesis is more than reasonable from a practical point of view.

The flowchart reported in *Figure 4.4* summarizes the fundamental stages of the proposed design techniques.

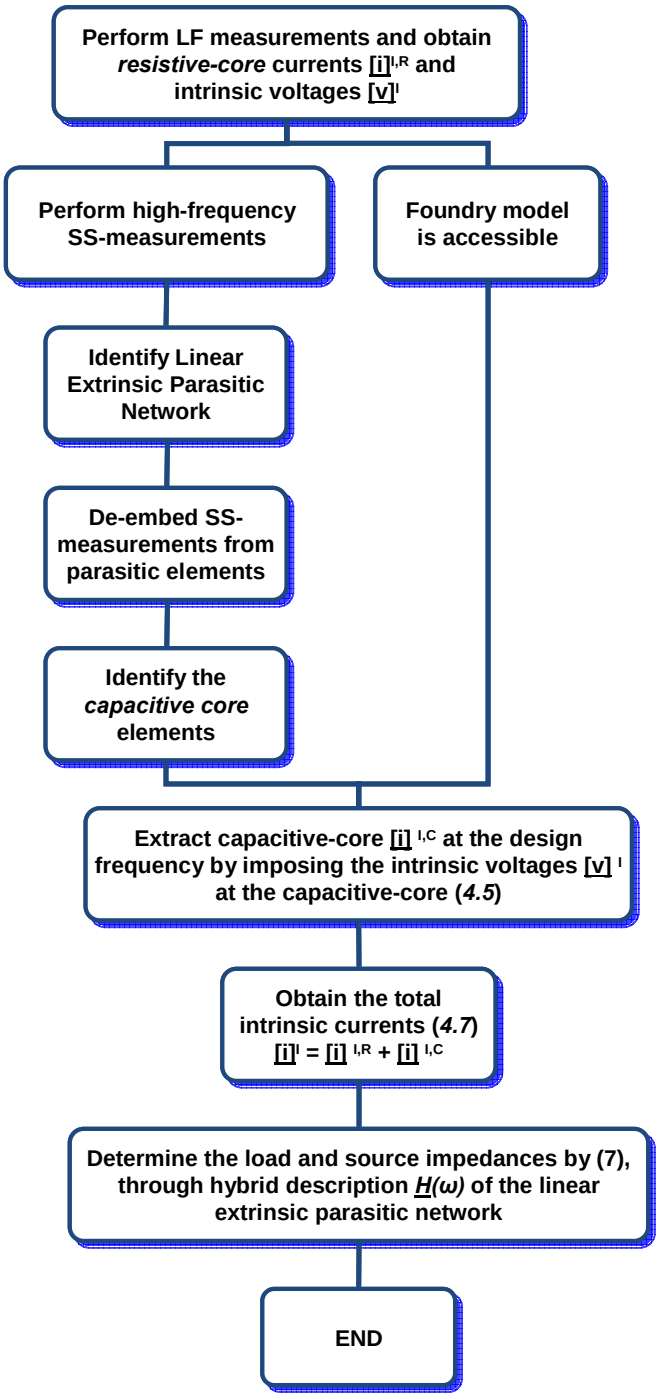


Figure 4.4 - Flowchart describing the proposed design technique.

4.4 Experimental Results

The validation of the proposed approach has been carried out by considering several power amplifier designs. With the aim of validating the method, a rough, although more than reasonable, choice of the load-line was carried out for the different designs, exploiting both the affirmed GaAs technology and the emerging GaN Technology.

As a first example, an on-wafer *0.35x960-μm² GaAs PHEMT* device, suitable for X-band power amplifier design, has been considered: this process is the same used for the HPAs described in previous chapters and its foundry specifications are reminded in *Table 4.1*. The goal is to exploit the technology under class-AB operation and to compare the results obtainable with the experimental approach with those carried out using the foundry electrical models. To this end the device has been biased at (V_{g0} = -0.6V, V_{d0} = 10 V, I_{d0} = 90 mA).

TQT 0.35um GaAs pHEMT process	
Quantity	*Value*
Breakdown Voltage	22 V
Pinch-off Voltage	-1 V
Idss	300 mA/mm
Saturated Output Power	1.2 W/mm

Table 4.1 - 0.35-μm GaAs PHEMT Technology Specifications.

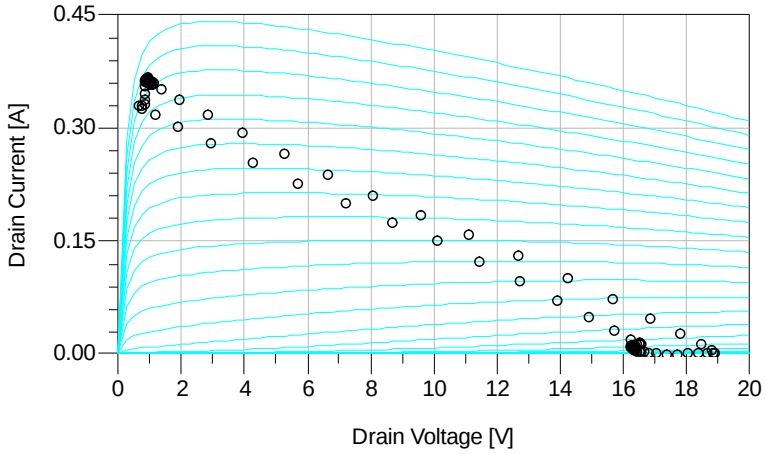
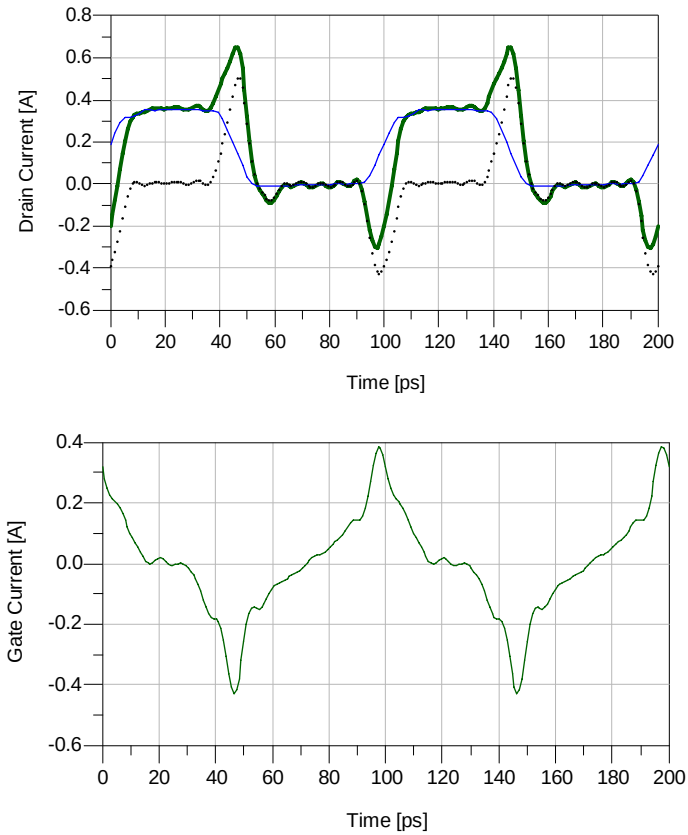


Figure 4.5 - Load-line chosen for a 960-μm GaAs PHEMT by exploiting the LF measurement system shown in Figure 4.2.

LF measurements have been carried out and the load-line plotted in *Figure 4.5* has been chosen which corresponds to an output power of *30.2 dBm* (1.1 W/mm) and a

67% drain efficiency. The measured device is biased at V_{g0} = -0.6 V, V_{d0} = 10 V, I_{d0} = 90 mA, the amplitude of the gate incident signal is Ag = 2 V, the amplitude of the drain incident signal is Ad = 1 V and the signals relative phase is $\Delta\varphi = 0°$.

Two design examples (at 4 and 10 GHz) have then been considered and, according to the procedure described in the previous paragraph, the capacitive core of the foundry model has been adopted to compute the displacement currents (4.5) and, successively, the total intrinsic currents (4.7). *Figure 4.6a* shows, for the 10 GHz case, the drain current and its conduction and displacement components, while in *Figure 4.6b* the gate current (which practically coincides with its displacement component) is plotted. Finally, by adopting the linear parasitic network description of the foundry model, the extrinsic currents and voltages have been obtained.



a)

b)

Figure 4.6 - Drain current at the intrinsic device (green thick solid line) and its two components: the capacitive one (dots) and the resistive one (blue thin solid line) (a). Total gate current at the intrinsic device (b).

Table 4.2 shows the obtained load impedance values, whereas the source impedance has been chosen to avoid highly mismatched impedances, which would emphasize the uncertainty of the high-frequency LP measurements exploited to validate

the consistence of the proposed approach. In particular, large-signal measurements were carried out by exploiting the *4-26 GHz* load-pull system described in the *Chapter 1*, which enables device source and load impedances at the fundamental frequency to be controlled. Measurements carried out at *4 GHz* on the selected device, by adopting the impedance values reported in *Table 4.2*, are shown in *Figure 4.7*.

Source Impedance	*Frequency*	*Load Impedance*
9.40 + i·11.62 Ω	4 GHz	39.44 + i·14.75 Ω
	8 GHz	34.43 + i·23.07 Ω
	12 GHz	23.40 + i·27.98 Ω
8.26 + i·5.7 Ω	10 GHz	26.5 + i·21.53 Ω
	20 GHz	14.43 + i·19.93 Ω
	30 GHz	5.97 + i·15.33 Ω

Table 4.2 - Synthesized Source and Load Impedances for the4-GHz and 10-GHz GaAs PHEMT power amplifier Designs.

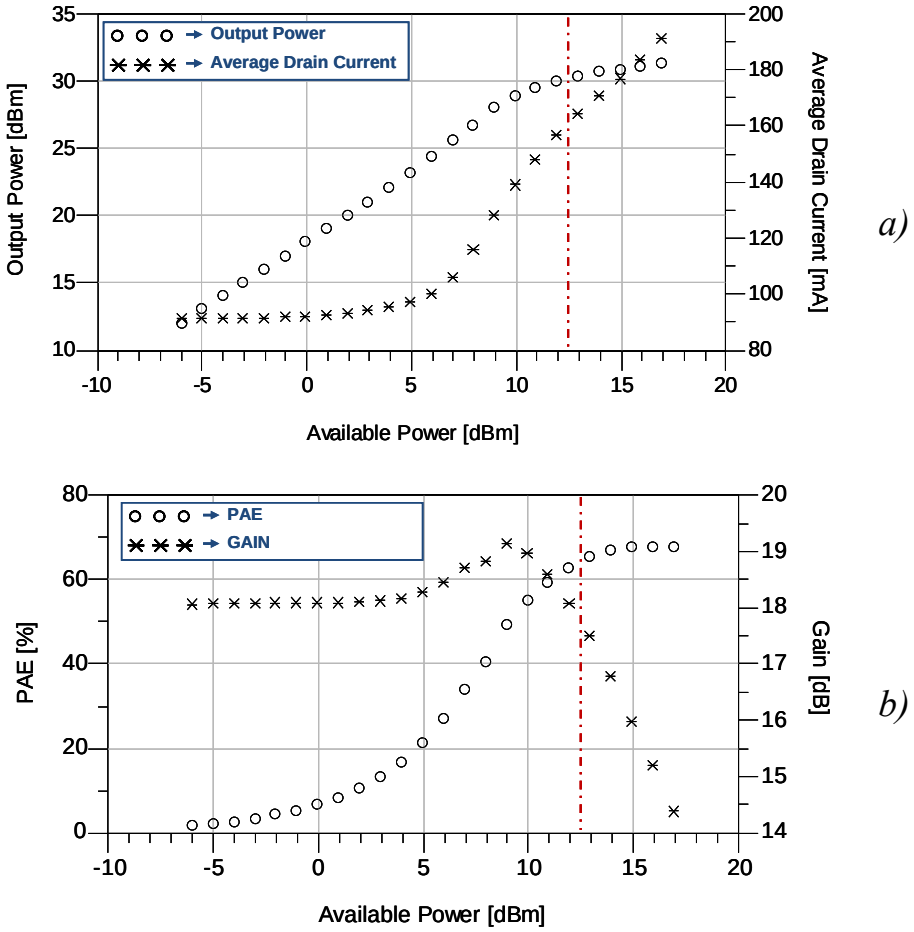


Figure 4.7 - Load-pull measurements carried out at 4 GHz by imposing the load and source impedances synthesized through the proposed approach and summarized in the Table 4.2. The dotted vertical lines identify the values corresponding to the output power level of interest.

The experimental results in *Table 4.3* compare predictions obtained by means of the proposed approach and load-pull data for the output power level of interest (i.e., *30.2 dBm*). The good agreement is evident despite, especially at 10 GHz, the importance of the displacement currents (see *Figure 4.6*). In particular, a good prediction has been obtained of the high level of converted dc drain current (*159 mA* starting from a quiescent condition of *90 mA*).

Predicted		*Quantity*	*Measured*	
4 GHz	*10 GHz*		*4 GHz*	*10 GHz*
159 mA		Average drain current	160.5 mA	170 mA
66.7 %		Drain Efficiency	65.9 %	62 %
15.9 dB	10.8 dB	Gain	17.8 dB	12.3 dB
65 %	61.2 %	PAE	64.3 %	58.3 %

Table 4.3 - Comparison between device performance Predicted by the proposed Technique and Measurement data (P_{OUT} = 1.06 W).

The acceptable discrepancies (more evident at 10 GHz) between large-signal measurements and predictions are essentially associated to two problems: the uncertainty related to the LP setup and the accuracy of the capacitive core description. In fact, in the present example, a nonlinear model based on analytical expressions for the capacitive core (which allows for optimum simulation times but cannot guarantee the same level of accuracy of look-up-table approaches) has been adopted. Also the lack of control on the harmonic LP terminations has a noticeable influence: they might be responsible for a *5%* discrepancy on the converted dc current as indicated by simulations carried out with the nonlinear model.

As a further example an on-wafer C-band, *0.7x800 μm^2 GaN HEMT* device has been considered whose foundry specifications are reported in *Table 4.4*. The bias condition has been chosen under the constraints of operating under weakly nonlinear operation (V_{g0} = *-2 V*) and limiting, for safety reasons, the quiescent dissipated power to *4.75 W* (V_{d0} = *25 V,* I_{d0} = *190 mA*). A *110* Ω loading condition (see *Figure 4.3*) has been considered which provides an output power (P_{out}) of *29.5 dBm* and a drain efficiency of *20.5 %*.

Quantity	*Value*
Breakdown Voltage	80 V
Pinch-off Voltage	-3.5 V
Idss	700 mA/mm
Saturated Output Power	4 W/mm

Table 4.4 - 0.7μm GAN HEMT Technology Specifications.

In this case S-parameter measurements (*40 MHz – 40 GHz*) were performed in a wide range of bias conditions (- 8 V < V_{g0} < 1 V, 0 V < V_{d0} < 40 V), and, after the identification and de-embedding of the parasitic network, equation (4.5) was adopted for the computation of the *capacitive-core* behavior. Nonquasi-static effects have been neglected since, assuming a design frequency of 4 GHz, they are of minor importance up to 8 GHz, as clearly shown in *Figure 4.8*. The gate and drain currents are shown in *Figure 4.9*. It is well evident the large contribution deriving from the capacitive core.

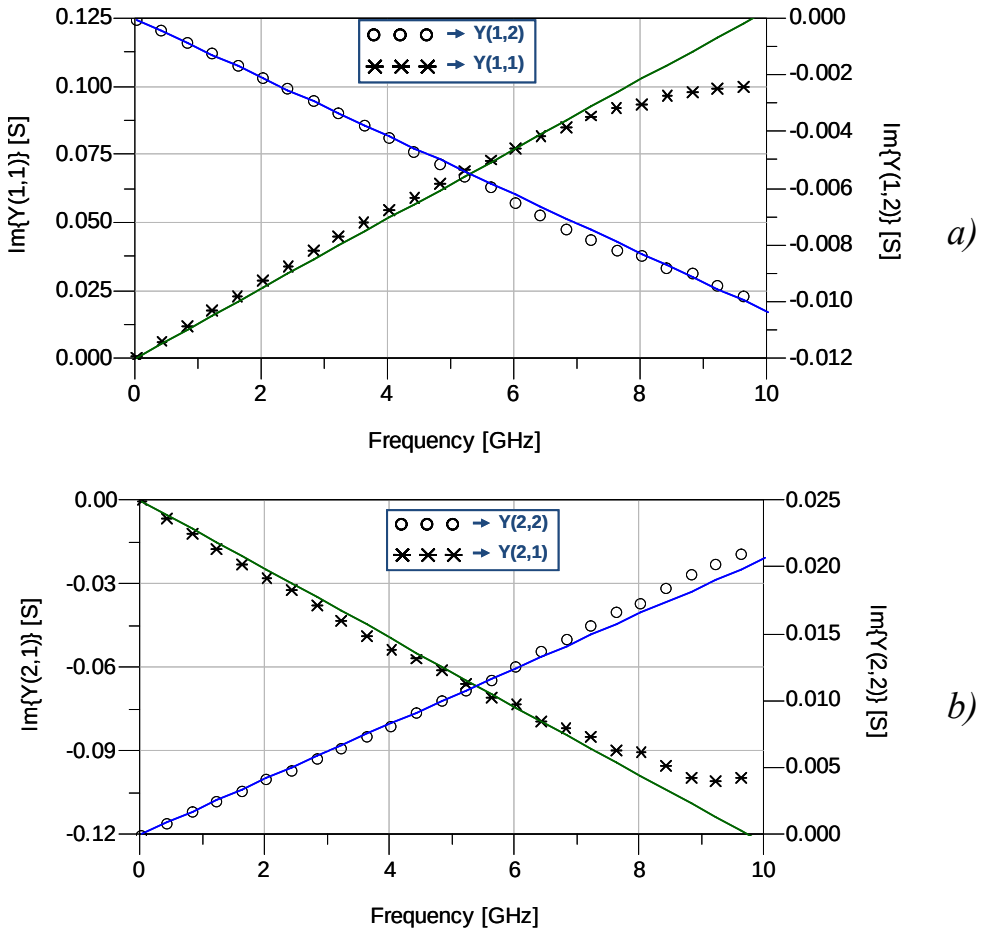


Figure 4.8 - Measurements (symbols) versus predictions (continuous lines) at (Vg0 = -2 V, Vd0 = 25 V) of the Y-parameter imaginary parts at the intrinsic device.

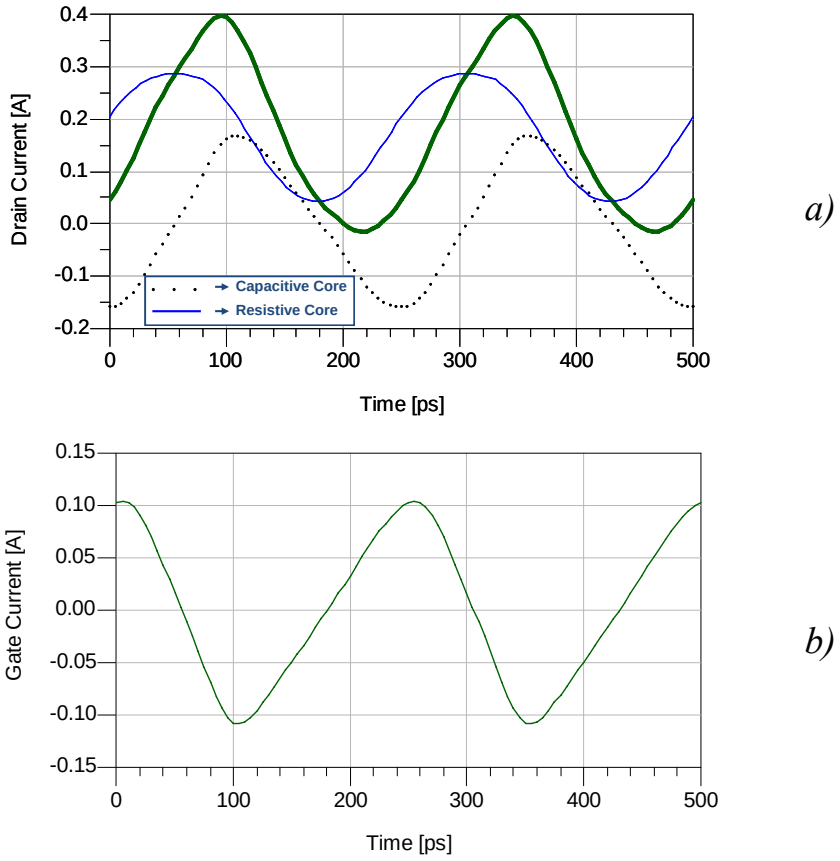


Figure 4.9 - Drain current at the intrinsic device I_d^i (green thick solid line) and its two capacitive and the resistive cores (a). Total gate current at the intrinsic device I_g^i (b).

The synthesized load and source impedances (in this case, the latter has been chosen equal to the conjugate of the large-signal device input impedance) are listed in *Table* 4.5, while the corresponding LP measurements are shown in *Figure 4.10*. The experimental results corresponding to the output power of *29.5 dBm* are summarized in *Table 4.6* and demonstrate an impressive agreement. It is evident the accuracy improvement obtainable, with respect to the previous example, when using a look-up-table based model of the capacitive core.

Source Impedance	*Frequency*	*Load Impedance*
3.41 + i·10.21 Ω	(f_0) 4 GHz	42.42 + i·54.22 Ω
	($2f_0$) 8 GHz	16.28 - i·12.18 Ω
	($3f_0$) 12 GHz	14.55 + i·25.79 Ω

Table 4.5 - Synthesized Source and Load Impedances for the 800-µm GaN HEMT.

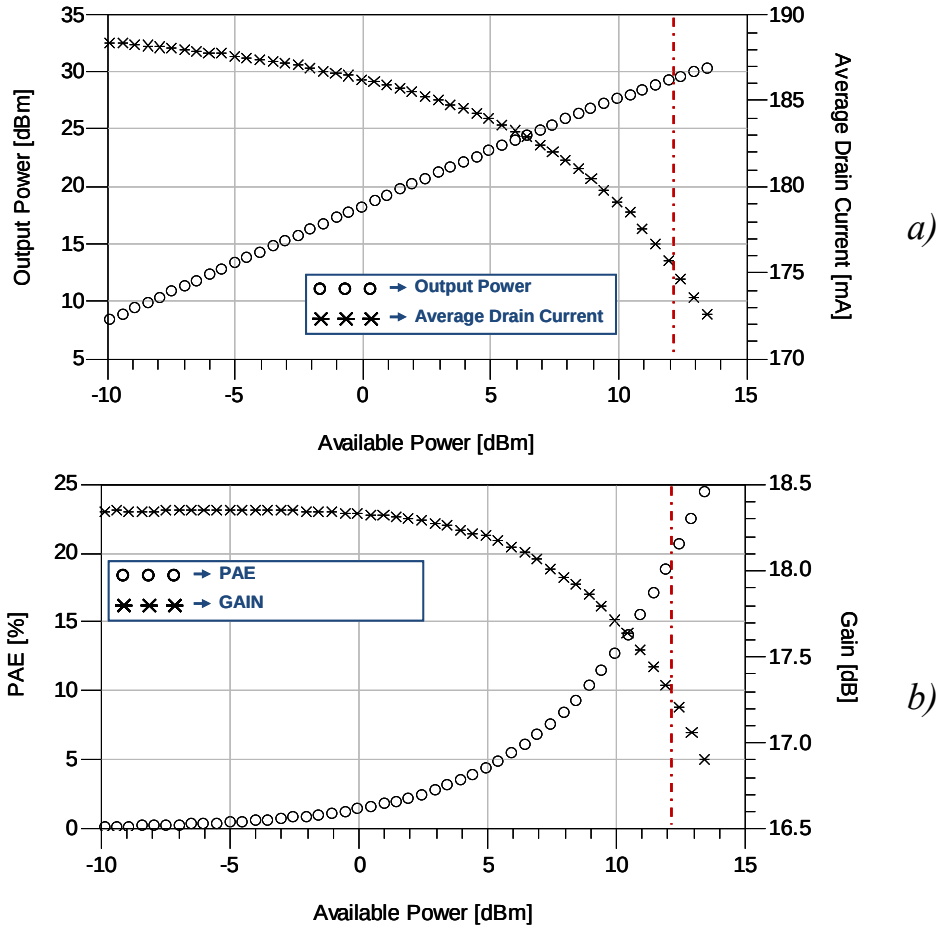


Figure 4.10 - Load-pull measurements carried out at 4 GHz by imposing the load and source impedances synthesized through the proposed approach (Table 4.5). The dotted vertical lines identify the values corresponding to the output power level of interest.

Predicted	*Quantity*	*Measured*
172 mA	Average drain current	175 mA
20.5 %	Drain Efficiency	20.1 %
17.3 dB	Gain	17.3 dB
20.1 %	PAE	19.7 %

Table 4.6 - Comparison between Device Performance Predicted by the Proposed Technique and Measurement Data (P_{out} = 881 mW).

4.5 L-band Hybrid HPA in GaN Technology

As anticipated in the introduction of this chapter, over the last 10 years, the Gallium Nitride (GaN) semiconductors have shown to be the new frontier for a technological leap in the RF and Microwave Power amplifiers. The main technological advantages of the GaN are:

- the high Band-Gap, of *3.4eV* instead of the *1.4eV* and *1.1eV* of the GaAs and Silicon semiconductors respectively, with consequent very high Breakdown Voltages, around 100 Volts;
- the high electron mobility and space-charge density, which allow to reach current densities of about *1-1.4 mA/mm*;
- the high thermal conductivity of the SiC substrate, where GaN is grown, and the intrinsic capability of GaN to work at channel temperatures up to 200°C.

The high voltages allow reaching very high power densities, of about 5x and 20x instead of the GaAs process, and, hence, to exploit devices with smaller periphery and high load impedances, which imply simpler matching networks and wider frequency bandwidth.

On the other hand, the unripeness of that technology and the presence of important low-frequency dispersive phenomena (i.e. traps and thermal effects) pose some issues in terms of electrical models and hence in the design of power amplifiers. For that reasons, the proposed procedure has been adopted for the design and realization of a hybrid L-band high-power amplifier exploiting a discrete GaN HEMT power bar, with two different targets: first, have a confirmation of the usefulness of the new design approach, second, to obtain the same performance of the GaAs hybrid HPA shown in Chapter 2, exploiting a GaN discrete device with a quarter of the total periphery used that case.

The bar is of the same process described above, it is composed of six *2-mm* cells for a total gate periphery of *12 mm* and is capable of delivering a saturated output power of about *47 W*. The proposed procedure has been applied to the 2-mm elementary cell in order to define the optimum load impedance. The bias condition has been chosen for class-AB operation (V_{g0} = *-3 V,* V_{d0} = *35 V,* I_{d0} = *140 mA*), and the load-line shown in *Figure 4.11* has been selected which provides a single-cell output power of *38.8 dBm* (3.8 W/mm) and a drain efficiency of *67 %*.

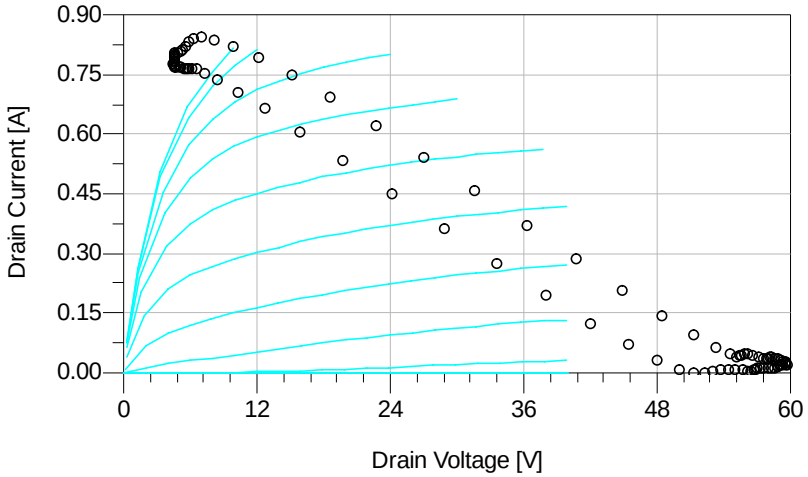


Figure 4.11 - Load-line of a 2-mm GaN HEMT device, chosen by exploiting the LF measurement system shown in Figure 4.2.

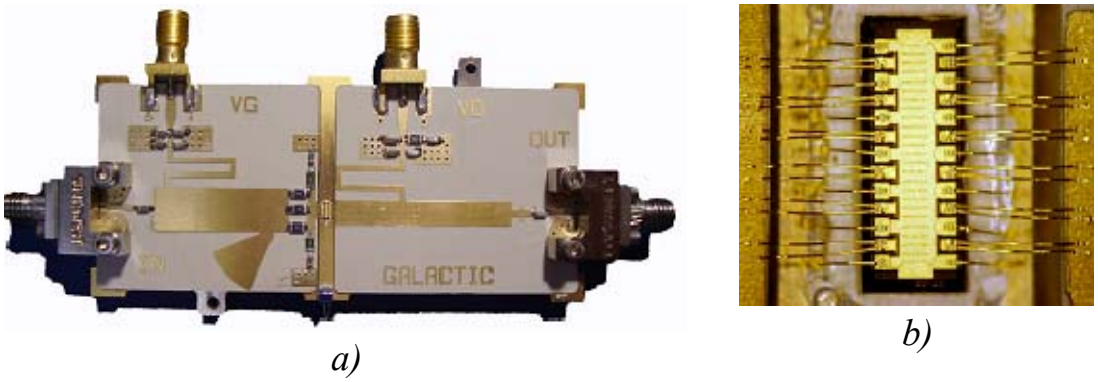
The measured device is biased at $V_{g0} = -3\ V$ and $V_{d0} = 35\ V$, the amplitude of the gate incident signal is $A_g = 5\ V$, the amplitude of the drain incident signal $A_d = 9\ V$ and the signals relative phase is $\Delta\varphi = 180°$.

The capacitive core of the foundry models was exploited in order to compute the displacement currents. The load impedance has then been evaluated according to the already described procedure, while the source one was chosen equal to the conjugate of the device input large-signal impedance, as explained in *Table 4.7*, where also load harmonic impedances are considered.

Source Impedance	*Frequency*	*Load Impedance*
9.31 + i·23.58 Ω	1.275 GHz	58.32 + i·23.06 Ω
	2.550 GHz	31.05 + i·25.80 Ω
	3.825 GHz	26.10 + i·22.52 Ω

Table 4.7 - Synthesized Source and Load Impedances for the 2-mm GaN HEMT.

Exploiting the same facilities described in *Chapter 2*, the hybrid L-band power amplifier has been designed by synthesizing, on the high frequency laminate, an output network which provides the chosen load impedance to each single 2-mm cell of the power bar. A picture of the realized amplifier and of the discrete power bar is shown in *Figure 4.12*.



a) *b)*

Figure 4.12 - GaN Amplifier for L band application exploiting a Coplanar Technology Integrated Circuit (a). The active device is a 12-mm GaN power bar combining six 2-mm elementary cells (b).

The high load impedance required by the GaN devices allows for impedance transformation through a simple microstrip step-impedance network connected to the six elementary cells by means of six bonding wires. An input network composed of a radial stub and a step-impedance solution optimizes the transducer gain. Furthermore, a combined series-shunt RC stabilizing network, implemented by means of SMD resistors and ceramic capacitors, makes the device unconditionally stable from dc to the cut-off frequency. Gate and drain bias networks employ high impedance λ/4 microstrip lines with shunted SMD chip capacitors.

Figure 4.13 shows the main performance of the amplifier: a saturated output power of about *47 W* and a *63%* efficiency fully comply with the expected performance of the technology.

In *Table 4.8* the L-band power amplifier measured performance are compared with the predictions obtained through the proposed technique with reference to the same level of output power (*46.6 dBm*). Considering the unavoidable dispersion in the realization phases and that only the load impedance at the fundamental frequency has been accurately synthesized, the results definitely indicate the effectiveness of the proposed approach for the design of power amplifiers. In particular, a good prediction has been obtained of the high level of converted dc drain current (*2.1 A* starting from a quiescent condition of *840 mA*).

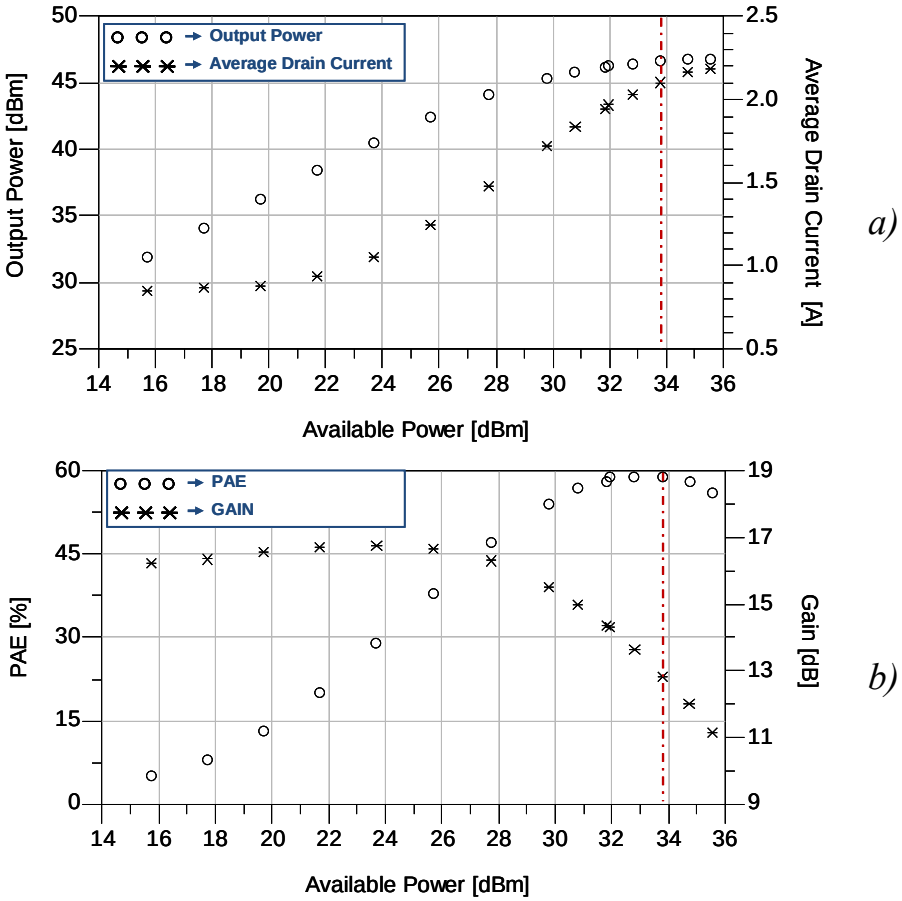


Figure 4.13 - Measured performance of the hybrid L-band high-power amplifier. The dotted vertical lines identify the values corresponding to the output power level of interest.

Predicted	*Quantity*	*Measured*
1.95 A	Average drain current	2.1 A
67 %	Drain Efficiency	63 %
13.4 dB	Gain	12.8 dB
64 %	PAE	59 %

Table 4.8 - Comparison between Device Performance Predicted by the Proposed Technique and Measurement Data (P_{out} = 46.1 W).

4.6 Summary

In this chapter a new approach to power amplifier design based on the experimental characterization of the electron device load-line has been proposed. The method mainly relies on large-signal measurements carried out at low frequency that enables the most important electron device nonlinear effects to be exactly accounted for. Bias/frequency-dependent small-signal measurements are used to identify the ED capacitive core and compute the displacement currents. Alternatively, the capacitive core of an existing, nonlinear device model can be adopted.

The method has provided excellent agreement with experimental results obtained by means of complex and expensive high-frequency load-pull setups. Finally, after brief of the Gallium Nitride characteristics, the design of a Hybrid L-band high-power GaN amplifier has been carried out, in order to definitely confirm the effectiveness of the proposed approach. The amplifier delivers a power of about 47 Watts with a power added efficiency of 59%, exploiting a single power bar of *12mm* of gate periphery; these performances are quite better than that obtained with the *48mm* of gate periphery GaAs amplifier described in *Chapter 2*.

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Conclusions

The research activity's target, explained in this Thesis, was to develop and to define design methodologies capable to optimize high power amplifier performances, complying the tight constraints imposed by space applications. In effect, for satellite systems, the designer has to reach the best performances under proper electrical and thermal de-rated conditions, respect to the maximum ratings provided by the used technology, in order to ensure proper levels of reliability.

As described in the first chapter, the main design methods exploit a mix of three different approaches, which represent the pillars in power amplifier design: the Cripps load-line theory, the load-pull measurements and the iterative harmonic-balance analyses based on nonlinear models of electron devices (ED). The scope of the research activity was to conjugate the main principles, on which those methods are based on, in a design approaches suitable for space application and, on the other hand, to overcome their intrinsic limitations in terms of frequency range, power levels and modelling issues.

In the first part of this dissertation, a design methodology, based on the intrinsic Load-Line shaping, was explained and demonstrated. In effect, we saw that a proper control of the dynamic load-line, at the intrinsic terminals of the Electron Devices, allows to optimize the performances of the Power Amplifier and, at the same time, to take under control both thermal and electrical parameters involved in the reliability constrains. Basing on the availability of a good non-linear electrical model of the Electron Device, the methodology was verified by the design of two different HPAs: an L-band (*1-2 GHz*) hybrid high power amplifier, to be used in the power line-up of a satellite TR module, and a fully monolithic amplifier in Ku band (*10.7 -12.7 GHz*), for the power section of Telemetry, Tracking and Command systems. In this way, the validity of the proposed approach has been demonstrated for both low frequency hybrid solutions and high frequency MMIC amplifiers.

Starting form the high potentiality of the Gallium Nitride (GaN) emerging technology, the proposed load-line method was applied to develop a new experimental approach for power amplifier design, in order to overcome the difficulty to define accurate electrical models for the new process. The method mainly relies on large-signal

measurements carried out at low frequency that enables the most important electron device nonlinear effects to be exactly accounted for. In this way, the experimental characterization of the intrinsic dynamic load-line is possible, providing a powerful instrument for power amplifier design. Also in this case, many experimental verification was illustrated; in particular, an L-band HPA, exploiting a 12mm GaN power Bar, was realized with two main purpose: to verify the new design approach and to demonstrate the high potentialities of Gallium Nitride in High Power Amplifiers design.

Publications

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