



ALMA MATER STUDIORUM
UNIVERSITÀ DI BOLOGNA

DOTTORATO DI RICERCA IN
INGEGNERIA ELETTRONICA, TELECOMUNICAZIONI E TECNOLOGIE
DELL'INFORMAZIONE

Ciclo 38

Settore Concorsuale: 09/E3 - ELETTRONICA

Settore Scientifico Disciplinare: ING-INF/01 - ELETTRONICA

ADVANCED TCAD MODELING OF CHARGE TRAPPING PHENOMENA IN
ALGAN/GAN AND ALSCN/GAN HEMTS

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Esame finale anno 2026

Keep a little fire burning; however small, however hidden.
The Road - Cormac McCarthy

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List of Abbreviations

2DEG	Two-Dimensional Electron Gas
AlGaN	Aluminum Gallium Nitride
AlN	Aluminum Nitride
AlScN	Aluminum Scandium Nitride
AlYN	Aluminum Yttrium Nitride
BTBT	Band-To-Band Tunneling
BTE	Boltzmann Transport Equation
C	Carbon (deep acceptor dopant)
CB	Conduction Band
C-V	Capacitance–Voltage
DC	Direct Current
DUT	Device Under Test
eBT_{B2B}	electron Band-to-Band Barrier Tunneling
E-field	Electric field
E_C	Conduction-band edge minimum
E_F	Fermi Level
E_V	Valence-band edge maximum
E_t	Trap energy level
Fe	Iron (deep acceptor dopant)
FET	Field–Effect Transistor
FOM	Figure Of Merit
$f_{\max}$	Maximum Oscillation Frequency
f_T	Cutoff Frequency
GAA	Gate–All–Around
GaN	Gallium Nitride
g_m	Transconductance
HEMT	High Electron Mobility Transistor
hBT	hole Barrier Tunneling
HTRB	High-Temperature Reverse Bias
I-V	Current–Voltage characteristics
I_D	Drain current

I_G	G ate current
I_S	S ource current
MC	M onte C arlo (simulation)
MIGS	M etal- I nduced G ap S tates
MOCVD	M etal- O rganic C hemical V apor D eposition
MOSFET	M etal- O xide- S emiconductor F ield- E ffect T ransistor
ϕ_M	M etal work function
n_s	E lectron sheet density
NS	N anosheets
NW	N anowires
p-GaN	p -type G allium N itride
R_{ON}	O n- R esistance
RF	R adio F requency
SHE-BTE	S pherical- H armonics E xpansion B TE
SiC	S ilicon C arbide
SiN	S ilicon N itride (passivation layer)
SRH	S hockley- R ead- H all (recombination model)
TAT	T rap- A ssisted T unneling
TCAD	T echnology C omputer A ided D esign
UWBG	U ltra W ide B and G ap (semiconductor)
V_{BR}	B reakdown V oltage
V_D	D rain voltage
VB	V alence B and
V_G	G ate voltage
V_S	S ource voltage
V_{TH}	T hreshold voltage
WBG	W ide B and G ap (semiconductor)

UNIVERSITY OF BOLOGNA

Abstract

ARCES-DEI

Doctor of Philosophy

**Advanced TCAD Modeling of Charge Trapping Phenomena in AlGa_N/Ga_N
and AlSc_N/Ga_N HEMTs**

by Franco Ercolano

Gallium nitride (Ga_N) High Electron Mobility Transistors (HEMTs) have emerged as key enablers of high-efficiency power conversion and radio-frequency (RF) applications, due to their wide bandgap (WBG), high critical electric field, and strong polarization-induced two-dimensional electron gas (2DEG). However, the immaturity of Ga_N technology, particularly in epitaxial growth, interface engineering, and passivation, still results in a high density of bulk and surface traps. These process-induced defects, are the primary source of charge trapping and high-field degradation, which continue to limit device reliability and large-scale industrial adoption.

This thesis develops an advanced Technology Computer-Aided Design (TCAD)-based modeling framework to analyze gate leakage in enhancement-mode p-type Ga_N (p-Ga_N) gate HEMTs, as well as charge trapping dynamics and reliability degradation in depletion-mode Ga_N HEMTs featuring AlGa_N and AlSc_N barrier layers. The work bridges experimental characterization and physical simulation, aiming to establish predictive, quantitatively calibrated models that link material-level defects to device-level degradation mechanisms.

After introducing the theoretical foundations of semiconductor charge transport, the work provides an overview of Ga_N technology, followed by the main challenges and principles of TCAD modeling. The first analysis focuses on enhancement-mode p-Ga_N gate HEMTs, where a comprehensive gate-leakage model is developed and validated by combining field-assisted and trap-assisted tunneling mechanisms within realistic two-dimensional geometries. The analysis reveals that corner fields at the metal/p-Ga_N interface strongly affect the leakage current distribution, and that accurate representation of these effects allows the reproduction of experimental I_G-V_G and I_D-V_G characteristics. This establishes a reliable foundation for the subsequent reliability-oriented studies.

The second analysis deepens the study by focusing on the reliability of depletion-mode AlGa_N/Ga_N HEMTs through a combined experimental–simulation approach,

integrating DC, pulsed I–V, and High-Temperature Reverse Bias (HTRB) step-stress data. The calibrated TCAD model identifies two dominant defect families: deep Fe-related acceptor traps in the buffer/channel and donor-like traps at the SiN/GaN-cap interface. Pulsed measurements reveal that the incomplete detrapping of Fe-related acceptors, whose emission times exceed the pulse period, drives current collapse and dynamic on-resistance increase. A refined analysis also highlights a limited contribution of surface donor traps, whose charge compensation interplay with Fe-related centers stabilizes the surface potential. Under HTRB stress, degradation is primarily driven by field-assisted detrapping of pre-existing donor-like states located at the passivation interface. These traps modulate the 2DEG density along the gate–drain access region and control the long-term drift of the drain current. This framework successfully reproduces the measured degradation trends and provides insight into the microscopic origins of device instability.

Finally, the last analysis extends the modeling strategy to emerging AlScN/GaN HEMTs, leveraging the enhanced spontaneous polarization of AlScN, which leads to higher 2DEG density and improved transconductance. A combined analysis of experimental stress data and TCAD simulations, complemented by a comparison with AlGaN reference devices, reveals three key degradation pathways: under-gate acceptor-trap buildup causing threshold-voltage shifts, donor detrapping in the access region leading to transconductance reduction, and field-assisted gate leakage correlated with overall drain current collapse. This joint approach clarifies the intrinsic performance–reliability trade-off introduced by the AlScN barrier and emphasizes the critical role of interface quality and barrier thickness optimization.

Overall, this work establishes a coherent physical framework that bridges experimental data and TCAD simulations across different GaN HEMT architectures, i.e., p-GaN gate, AlGaN/GaN, and AlScN/GaN, linking microscopic defect physics to macroscopic degradation trends. The developed methodology enhances the predictive capability of TCAD for GaN device reliability, provides actionable guidelines for interface and barrier engineering, and lays the groundwork for future extensions toward electro-thermal and RF stress modeling.

Introduction

The continuous demand for higher efficiency, faster switching, and increased power density is driving a profound transformation in modern power and radio-frequency (RF) electronics. Applications such as 5G communications, electric vehicles, renewable energy conversion, and aerospace systems increasingly rely on semiconductor devices that can sustain high voltages, operate at high frequencies, and maintain reliability under harsh environmental and thermal conditions. To meet these requirements, a new class of materials, WBG semiconductors, has emerged as the foundation for the next generation of high-performance electronic devices.

Among WBG materials, GaN stands out as a particularly promising candidate. Its combination of wide bandgap, high critical electric field, high electron mobility, and strong polarization enables exceptional performance in terms of switching speed, power conversion efficiency, and high-frequency operation. In GaN-based HEMTs, a thin barrier layer with a larger bandgap (typically AlGaIn) is epitaxially grown on a GaN channel. The discontinuity in spontaneous and piezoelectric polarization across the heterointerface causes a strong bending of the energy bands, creating a triangular potential well at the interface. Electrons become confined in this well, forming a quantized population along the growth direction, known as the 2DEG, responsible for the high sheet carrier density and mobility typical of GaN-based HEMTs. This intrinsic advantage, together with the material low parasitic capacitance, has led to widespread adoption of GaN HEMTs in both RF and power domains, from radar and base stations to converters and automotive traction systems.

However, the industrial maturity of GaN technology remains behind that of Si or even SiC. Despite impressive performance metrics, GaN devices still face significant reliability challenges. The presence of a large density of native and process-induced traps, both in the buffer and at the surface, strongly affects the electrical stability of the HEMTs, leading to dynamic current collapse, threshold voltage drift, and increased gate leakage under high-field and high-temperature conditions. These degradation mechanisms are particularly critical under long-term electrical stress, such as HTRB, where trapped charges gradually modify the electrostatics of the device. Addressing these phenomena is essential for the large-scale deployment of GaN-based technologies in mission-critical and safety-sensitive systems.

The physical understanding of these degradation processes is still under active

investigation, mainly due to the complex electrostatics and transport behavior of III-nitride heterostructures and the relative immaturity of GaN technology compared to silicon. Moreover, while Technology Computer-Aided Design (TCAD) simulation has become an indispensable tool for device research and optimization, its application to GaN is far from trivial. Strong polarization fields, wide bandgap, and defect-related trapping mechanisms introduce additional modeling complexity, while numerical instabilities, convergence issues, and incomplete physical models limit predictive accuracy. Consequently, a quantitatively calibrated TCAD framework capable of reproducing both transient and long-term degradation phenomena is required to bridge the gap between physical mechanisms and device-level reliability.

This Ph.D. work, entitled “*Study of transport properties and reliability of novel GaN-based HFETs for high-voltage and high-frequency applications*”, addresses these challenges through an advanced TCAD-based modeling framework. The research focuses on the physical interpretation and numerical modeling of charge-trapping phenomena, gate leakage, and stress-induced degradation in different GaN HEMT technologies. The work was conducted primarily through TCAD simulations, while experimental measurements of static, pulsed, and HTRB step-stress characteristics were provided by external partners and used to constrain and validate the models. By combining experimental input and physical modeling, the study establishes a consistent approach for correlating device-level defects with electrical degradation trends across multiple device platforms.

The main objectives of this thesis are threefold: (i) Develop and validate a physically based TCAD framework for modeling gate leakage mechanisms in enhancement-mode p-GaN HEMTs. (ii) Analyze degradation mechanisms in depletion-mode AlGaIn/GaN HEMTs under pulsed and HTRB step-stress conditions. (iii) Extend the latter modeling framework to emerging AlScN/GaN HEMTs, evaluating their performance and reliability trade-offs against their conventional AlGaIn/GaN counterparts.

The original contributions of this thesis can be summarized as follows: (i) Development of a comprehensive and quantitatively calibrated TCAD framework for GaN-based HEMTs, capable of reproducing experimental DC, pulsed I-V, and stress-induced degradation characteristics. (ii) Implementation of a physically based model for gate leakage in enhancement-mode p-GaN HEMTs, capturing both direct tunneling and trap-assisted conduction mechanisms, and highlighting the influence of device geometry on leakage distribution. (iii) Investigation of degradation mechanisms in AlGaIn/GaN HEMTs under pulsed and HTRB step-stress conditions, revealing the influence and mutual interplay between deep Fe-related acceptor traps in the buffer and donor-like interface traps at the passivation/cap interface. (iv) Extension of the TCAD framework to AlScN/GaN HEMTs, providing a comparative reliability study

against AlGaIn devices and clarifying how barrier composition and polarization engineering affect gate leakage, trapping dynamics, and stress response.

The outcomes of this research provide a physically consistent and quantitatively validated methodology for reliability-oriented TCAD modeling of GaN-based HEMTs. The developed framework enhances the predictive capability of simulation for future device design and contributes to a deeper understanding of the degradation mechanisms that limit the long-term stability of WBG transistors.

The manuscript is organized as follows:

(I) Chapter 1 introduces the physical foundations of charge transport in semiconductors, presenting the semi-classical formulation of the fundamental transport equations and their implementation in TCAD environments. The discussion covers polarization effects in III-nitride heterostructures, thermal and self-heating phenomena, and carrier generation–recombination processes, concluding with a summary that highlights their relevance to the modeling activities developed in this work.

(II) Chapter 2 presents GaN technology from both material and device perspectives, providing an overview of GaN as a wide bandgap semiconductor and describing, layer by layer, the structure of the HEMT and the role of each region in determining device performance and reliability. The chapter concludes with an introduction to the key figures of merit and an outline of the reliability landscape that motivates the subsequent modeling analysis.

(III) Chapter 3 discusses the principles of TCAD modeling and its application to device design and reliability analysis, describing in detail the physical models adopted and calibrated within the TCAD framework. Furthermore, it addresses the challenges of modeling GaN-based devices in commercial TCAD tools and outlines the numerical and physical strategies adopted to overcome them.

(IV) Chapter 4 focuses on gate-leakage mechanisms in p-GaN HEMTs, presenting a comprehensive TCAD analysis supported by experimental calibration. The chapter begins with an overview of the physical origin of gate-leakage processes and the motivation for their study, followed by the description of the device structure and the simulation setup. One-dimensional and two-dimensional simulations are then employed to investigate the contribution of field-assisted and trap-assisted tunneling mechanisms and to assess the influence of geometrical effects on the gate current. The chapter concludes with a discussion of the main findings and establishes the connection to the subsequent reliability analysis.

(V) Chapter 5 investigates the degradation mechanisms in AlGaIn/GaN HEMTs

under pulsed I–V and HTRB step-stress conditions, combining experimental evidence with TCAD simulations. After describing the model calibration and benchmarking process, the chapter analyzes transient degradation through pulsed I–V measurements and long-term degradation under HTRB stress, identifying the dominant trap states responsible for drain current reduction. A final discussion addresses the sensitivity of reliability predictions to key physical parameters, summarizing the implications of the results for TCAD-based reliability modeling.

(VI) Chapter 6 extends the developed TCAD modeling framework to AlScN/GaN HEMTs, evaluating their performance–reliability trade-offs and benchmarking them against AlGaN-based counterparts. The chapter presents the device technology and experimental data, followed by the implementation, calibration, and validation of the TCAD model. Pulsed I–V and HTRB step-stress analyses are then performed to investigate the short- and long-term degradation mechanisms. The discussion highlights the impact of enhanced polarization and trap dynamics on the electrical behavior of AlScN/GaN HEMTs, providing a comparative assessment of their advantages and challenges relative to conventional AlGaN devices.

Finally, (VII) Chapter 7 summarizes the main conclusions of the research and outlines perspectives for future work. It revisits the key findings on gate-leakage and two-dimensional effects in p-GaN HEMTs, the dynamic trapping and degradation mechanisms in AlGaN/GaN devices, and the performance–reliability trade-offs identified in AlScN/GaN technology. The chapter also highlights the methodological contributions achieved through advanced TCAD calibration and reliability-oriented modeling, and concludes by discussing possible extensions of this work toward electro-thermal modeling, RF stress analysis, and the exploration of next-generation barrier materials.

Chapter 1

Charge Transport in Semiconductor Devices: A Semi-classical and TCAD Perspective

Chapter Overview

This chapter introduces the fundamental physical mechanisms governing charge transport in semiconductor devices, emphasizing their semi-classical representation and the models typically available in TCAD tools. After a review of the drift-diffusion framework and the main recombination-generation processes, particular attention is given to high-field transport effects, polarization in III-nitrides, and the role of traps and defects. The discussion progressively connects the theoretical foundations to their practical implementation in TCAD, laying the groundwork for the device-specific modeling efforts presented in the following chapters.

1.1 Fundamental Transport Equations

1.1.1 Poisson's Equation

The simulation of charge transport in semiconductor devices begins with solving the Poisson equation, which determines the electrostatic potential ϕ based on the spatial distribution of charges [1]–[3]. Under the quasi-static approximation, which is valid in semiconductor devices at typical operating frequencies, the electric field can be expressed as follows:

$$E = -\nabla\phi \quad (1.1)$$

where ϕ is the electrostatic potential. The quasi-static approximation assumes that time-varying electromagnetic effects, such as displacement currents and inductive fields, can be neglected due to the relatively low operating frequencies typical of most semiconductor devices. As a result, the Maxwell's equations reduce to their electrostatic and magnetostatic forms, allowing the electric field to be described as the negative gradient of the electrostatic potential. This simplification significantly reduces computational complexity in device simulation and is commonly adopted in TCAD tools. This approximation remains valid for the DC and transient reliability studies performed in this work. Despite this, it should be noted that GaN-based HEMTs are also designed for high-frequency applications. For accurate modeling of RF behavior at mm-wave frequencies, the full set of Maxwell's equations, including time-dependent electromagnetic terms, may be required. Such simulations typically involve EM-TCAD co-simulation techniques, which fall outside the scope of this work. So, in its general form, the electrostatic potential ϕ in a semiconductor is governed by the Poisson equation as:

$$\nabla \cdot (\epsilon \nabla \phi) = -\rho \quad (1.2)$$

where ϵ is the permittivity of the material, and ρ is the charge density, which includes:

$$\rho = q(p - n + N_D^+ - N_A^-) + \rho_t \quad (1.3)$$

with, n, p electron and hole concentrations, N_D^+, N_A^- ionized donor and acceptor densities and ρ_t charge density contributed by traps and fixed charges (e.g., from defects or interfaces).

Although standard analytical formulations of the Poisson equation often exclude fixed charge terms such as interface or polarization charges, TCAD implementations allow the explicit inclusion of these contributions, which is essential for accurate

modeling of GaN-based devices, where the spontaneous and piezoelectric polarization effect significantly affect the electrostatic (see Subsec. 1.2). Accurately resolving the electrostatic potential represents a primary challenge in device simulation, as it defines the relationship between the spatial charge distribution and the resulting electric field, even in complex heterostructures.

1.1.2 Carrier Continuity Equations

Once the electrostatic potential is obtained from the Poisson equation, the next step in modeling semiconductor devices involves determining the behavior of free carriers, which are electrons and holes, over time and space. This is described by the continuity equations, which account for the conservation of charge under drift, diffusion, and generation-recombination mechanisms. The continuity equations for electrons and holes are given by:

$$\frac{\partial n}{\partial t} = \frac{1}{q} \nabla \cdot \vec{J}_n + G_n - R_n \quad (1.4)$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q} \nabla \cdot \vec{J}_p + G_p - R_p \quad (1.5)$$

where, $\vec{J}_n, \vec{J}_p$ are the current densities for electrons and holes, G_n, G_p are the generation rates and R_n, R_p are the recombination rates.

These equations describe the time evolution of carriers and are essential for both DC and transient simulations. In the steady-state regime, such as under constant bias conditions, the time derivatives $\frac{\partial n}{\partial t}$ and $\frac{\partial p}{\partial t}$ become zero. In this case, the equations reduce to a balance between the divergence of current and the net recombination-generation rate:

$$\nabla \cdot \vec{J}_n = q(R_n - G_n) \quad (1.6)$$

$$\nabla \cdot \vec{J}_p = -q(R_p - G_p) \quad (1.7)$$

However, in transient simulations, such as those used to evaluate dynamic switching behavior or degradation under pulsed stress conditions, the time-dependent terms are retained and play a crucial role in capturing carrier dynamics and charge-trapping effects.

Although in many idealized models the generation and recombination terms are treated symmetrically (i.e., $G_n = G_p$ and $R_n = R_p$), this assumption does not always

hold. In GaN-based devices, particularly under high electric field or stress conditions, generation and recombination may be mediated by traps with asymmetrical capture/emission rates. As such, advanced TCAD simulations typically treat G_n , G_p , R_n , and R_p independently, allowing a more accurate representation of physical processes including Shockley-Read-Hall (SRH) recombination, impact ionization, and trap-assisted tunneling. These aspects, including generation and recombination mechanisms, will be further discussed in a dedicated section later in this chapter. Finally, solving the coupled system of Poisson's equation and the continuity equations, collectively referred to as the semiconductor equations, allows us to determine all the quantities of interest: the electron and hole concentrations n and p , and the electrostatic field E , derived from the potential ϕ . In general, an analytical solution of this nonlinear system is not feasible, and one must rely on commercial numerical device simulators such as Sentaurus (Synopsys) or ATLAS (Silvaco) to obtain physically accurate solutions.

1.1.3 Current Density Expressions

To complete the system of equations describing carrier transport in semiconductors, the current densities for electrons and holes must be defined. In most device simulations, the drift-diffusion (DD) model provides a reasonable balance between physical accuracy and computational efficiency [2], [4]. It is widely used in TCAD tools and well suited to both DC and transient simulations, particularly when carrier temperatures remain close to the lattice temperature.

Under the drift-diffusion model, the current densities for electrons and holes are expressed as:

$$\vec{J}_n = q\mu_n n \vec{E} + qD_n \nabla n \quad (1.8)$$

$$\vec{J}_p = q\mu_p p \vec{E} - qD_p \nabla p \quad (1.9)$$

where, q is the elementary electron charge (1.602×10^{-19} C), μ_n, μ_p are the electron and hole mobilities, D_n, D_p are the electron and hole diffusion coefficients, $\vec{E}$ is the electric field, defined as $\vec{E} = -\nabla\phi$.

The first term in each equation represents the drift current, driven by the electric field, while the second term accounts for the diffusion of carriers due to spatial concentration gradients.

In numerical simulators, the Einstein relation is used to link mobility and diffusivity under thermal equilibrium:

$$D_n = \frac{k_B T}{q} \mu_n \quad ; \quad D_p = \frac{k_B T}{q} \mu_p \quad (1.10)$$

where k_B is the Boltzmann constant and T is the absolute temperature. Although more sophisticated transport models exist, such as the modified drift-diffusion, the thermodynamic, the hydrodynamic and Monte Carlo (MC), they are generally reserved for scenarios where, carrier heating, hot-electron effects, energy or ballistic transport become significant. In this work, the drift-diffusion model provides an accurate and efficient framework for analyzing steady-state and transient behavior in GaN HEMTs under various electrical stress conditions.

1.1.4 Thermionic Emission Current

At a heterojunction interface, the conduction mechanism is governed by *thermionic emission*, which accounts for the probability of carriers surmounting the potential barrier between two materials.

The electron thermionic emission current density can be expressed in the semi-classical approximation as:

$$J_n = A^* T^2 \exp\left(-\frac{q\phi_B}{kT}\right) \left[\exp\left(-\frac{qV}{kT}\right) - 1 \right], \quad (1.11)$$

where A^* is the effective Richardson constant, ϕ_B is the effective barrier height, and V is the applied potential. This expression originates from the assumption that only electrons with kinetic energy greater than the potential barrier contribute to the net current, while others are reflected.

In compound semiconductors such as AlGaIn/GaN or AlScN/GaN, the barrier height ϕ_B is influenced by both the material composition and the polarization-induced band bending. Therefore, thermionic emission becomes particularly relevant in the modeling of heterostructure interfaces and Schottky contacts in high-electron-mobility transistors (HEMTs).

Following the formalism of Schroeder [5], the interface conditions for electron current density and energy flux density, $J_{n,2}$, $S_{n,2}$ entering material 2 and $J_{n,1}$, $S_{n,1}$ leaving material 1 across the interface with a positive conduction-band offset $\Delta E_C >$

0 are:

$$J_{n,2} = J_{n,1} \quad (1.12)$$

$$J_{n,2} = a_n q \left(v_{n,2} n_2 - \frac{m_{n,2}}{m_{n,1}} v_{n,1} n_1 \exp \left(-\frac{\Delta E_C}{kT_{n,1}} \right) \right), \quad (1.13)$$

$$S_{n,2} = S_{n,1} + \frac{c_n}{q} J_{n,2} \Delta E_C \quad (1.14)$$

$$S_{n,2} = -b_n \left(v_{n,2} n_2 kT_{n,2} - \frac{m_{n,2}}{m_{n,1}} v_{n,1} n_1 kT_{n,1} \exp \left(-\frac{\Delta E_C}{kT_{n,1}} \right) \right), \quad (1.15)$$

where the emission velocities are defined as:

$$v_{n,i} = \sqrt{\frac{kT_{n,i}}{2\pi m_{n,i}}}. \quad (1.16)$$

The coefficients a_n , b_n , and c_n are empirical parameters that control the scaling of current and energy flux, typically set to $a_n = 2$, $b_n = 4$, and $c_n = 1$ according to literature.

An equivalent set of equations applies for holes, where ΔE_V replaces ΔE_C and carrier quantities are denoted by the subscript p :

$$J_{p,2} = J_{p,1} \quad (1.17)$$

$$J_{p,2} = -a_p q \left(v_{p,2} p_2 - \frac{m_{p,2}}{m_{p,1}} v_{p,1} p_1 \exp \left(\frac{\Delta E_V}{kT_{p,1}} \right) \right), \quad (1.18)$$

$$S_{p,2} = S_{p,1} + \frac{c_p}{q} J_{p,2} \Delta E_V \quad (1.19)$$

$$S_{p,2} = -b_p \left(v_{p,2} p_2 kT_{p,2} - \frac{m_{p,2}}{m_{p,1}} v_{p,1} p_1 kT_{p,1} \exp \left(\frac{\Delta E_V}{kT_{p,1}} \right) \right). \quad (1.20)$$

In cases of high carrier density, where the Boltzmann approximation is no longer valid, the model can be reformulated under *Fermi statistics* using the Fermi–Dirac integral correction terms ζ_n and ζ_p . This refinement ensures accurate evaluation of carrier fluxes in degenerate semiconductors, with the following replacements:

$$J_{n,2} = a_n q \left(v_{n,2} N_{C,2} \zeta_{n,2} - \frac{m_{n,2}}{m_{n,1}} v_{n,1} N_{C,1} \zeta_{n,1} \right), \quad (1.21)$$

$$S_{n,2} = -b_n \left(v_{n,2} kT_{n,2} N_{C,2} \zeta_{n,2} - \frac{m_{n,2}}{m_{n,1}} v_{n,1} kT_{n,1} N_{C,1} \zeta_{n,1} \right), \quad (1.22)$$

$$\zeta_{n,2} = \ln(1 + \exp(-\eta_{n,2})) + \eta_{n,2} \quad (1.23)$$

$$\zeta_{n,1} = \ln(1 + \exp(-\eta_{n,1})) + \eta_{n,1} \quad (1.24)$$

$$\eta_{n,1} = \eta_{n,1} - \frac{\Delta E_C}{kT_{n,1}}, \quad (1.25)$$

with:

$$\eta_n = \frac{E_{F,n} - E_C}{kT}, \quad (1.26)$$

$$N_C(T_n) = N_C(300K) \left(\frac{T_n}{300K} \right)^{3/2} \quad (1.27)$$

being N_C the effective density of states in the conduction band. Overall, thermionic emission provides a bridge between semiclassical transport and interface-limited conduction, serving as a cornerstone for modeling heterostructure behavior in advanced GaN-based HEMTs.

1.1.5 Carrier Mobility

In the absence of an external electric field and assuming a uniform carrier concentration at $T > 0$ K, free electrons in a semiconductor undergo random thermal motion with an average thermal velocity $v_{th,n}$ given by

$$\frac{1}{2} m_n v_{th,n}^2 = \frac{3}{2} k_B T \quad \Rightarrow \quad v_{th,n} = \sqrt{\frac{3k_B T}{m_n}}, \quad (1.28)$$

where m_n is the electron effective mass. This random motion does not contribute to a net current flow since the carrier velocities are isotropically distributed.

When an electric field E is applied, electrons acquire an average drift velocity v_n superimposed on the random thermal motion. Between two successive collisions, the carrier momentum evolves according to Newton's second law:

$$m_n \frac{dv}{dt} = -qE. \quad (1.29)$$

Integrating over the mean free time between collisions τ_{cn} yields the average drift velocity [6]:

$$v_n = -\frac{q\tau_{cn}}{m_n} E. \quad (1.30)$$

The proportionality constant

$$\mu_n = \frac{q\tau_{cn}}{m_n} \quad (1.31)$$

defines the electron mobility, expressed in units of $\text{cm}^2/\text{V}\cdot\text{s}$, which quantifies the carrier's ability to move through the lattice under the influence of an electric field. Hence, the drift velocity can be compactly written as:

$$v_n = -\mu_n E. \quad (1.32)$$

Carrier mobility (μ) therefore represents a key quantity linking microscopic scattering processes to macroscopic current flow. In III-nitride semiconductors, μ is strongly influenced by various scattering mechanisms, as discussed in the following [7], [8].

At low electric fields, carriers experience drift motion that is primarily limited by lattice vibrations (phonon scattering) and by Coulomb interactions with charged impurities [9]. The total mobility can therefore be expressed through Matthiessen's rule as the reciprocal sum of the individual contributions from each scattering mechanism. In lightly doped or intrinsic regions, phonon scattering dominates, leading to a temperature dependence of the form $\mu \propto T^{-\zeta}$, with $\zeta \approx 1.5$ –2 for most semiconductors (in this work is used 1 for the electrons). As the doping concentration increases, impurity scattering becomes significant, reducing mobility through enhanced carrier deflection by ionized dopants.

Under high electric fields, carrier velocity no longer increases linearly with the applied field but tends to saturate due to optical phonon emission [10], [11]. In GaN, velocity saturation occurs around $v_{\text{sat}} \approx 2.5 \times 10^7$ cm/s, depending on temperature and material quality. At still higher fields, non-parabolicity of the conduction band may lead to intervalley transfer of electrons into higher-energy valleys with larger effective mass, a mechanism responsible for the onset of negative differential mobility observed in some III–V compounds (called Gunn-effect)[12], [13].

In heterostructures such as AlGaIn/GaN or AlScN/GaN HEMTs, additional mobility degradation arises from alloy disorder, interface roughness, and polar optical phonon scattering at the barrier/channel interface [9]. These mechanisms contribute to reducing the effective channel mobility of the 2DEG, particularly in devices with high polarization fields.

The quantitative description of mobility in numerical simulations relies on empirical or semi-empirical formulations that capture its dependence on temperature, doping, and electric field. The most common implementations include temperature-dependent, doping-dependent, and field-dependent mobility models, which are discussed in Chapter 3, together with their calibration and impact on device characteristics.

1.2 Polarization Effects in III-Nitride Heterostructures

In semiconductor devices based on III-nitride materials, such as AlGaIn/GaN or AlScN/GaN heterostructures, polarization effects play a fundamental role in determining the electrostatics of the device and the formation of the 2DEG at the heterointerface. These polarization effects arise because of the non-centrosymmetric

nature of the wurtzite crystal structure, which is characteristic of III-nitride semiconductors like GaN, AlN, and InN. In contrast, conventional semiconductors with centrosymmetric cubic structures, such as Si or GaAs, do not exhibit spontaneous or piezoelectric polarization under normal conditions.

1.2.1 Spontaneous and Piezoelectric Polarization

In wurtzite III-nitride materials such as GaN and its alloys, polarization effects play a fundamental role in determining the electrostatics of heterostructure devices. The starting point is the definition of the electric displacement field:

$$\vec{D} = \epsilon_r \epsilon_0 \vec{E} + \vec{P} \quad (1.33)$$

where ϵ_0 is the vacuum permittivity (8.854×10^{-12} F/m), ϵ_r is the relative dielectric constant of the material, and $\vec{P}$ represents the total polarization vector. In polar materials, $\vec{P}$ includes both induced and spontaneous contributions.

In III-nitrides, spontaneous polarization arises intrinsically from the lack of inversion symmetry in the wurtzite lattice. This results in a net polarization vector even in the absence of external stress or electric field. The value of spontaneous polarization depends on the material composition, with typical values increasing from GaN to AlN.

In addition to spontaneous effects, piezoelectric polarization emerges due to strain in the crystal lattice when layers with different lattice constants are grown epitaxially. For instance, an AlGaN layer grown on GaN is typically under tensile stress due to lattice mismatch, inducing a piezoelectric polarization along the c-axis of the crystal.

The total polarization in each layer is therefore expressed as:

$$\vec{P}_{tot} = \vec{P}_{sp} + \vec{P}_{pz} \quad (1.34)$$

where, $\vec{P}_{sp}$ denotes the spontaneous polarization vector [C/cm²], and $\vec{P}_{pz}$ the piezoelectric polarization vector [C/cm²].

1.2.2 Polarization Discontinuity and Fixed Charges

When a heterojunction is formed, such as between AlGaN and GaN, there is a discontinuity in polarization across the interface:

$$\sigma_{pol} = P_{tot}^{(upper\ layer)} - P_{tot}^{(lower\ layer)} \quad (1.35)$$

where σ_{pol} is the total net polarization charge across the interface, and P_{tot} are the charge contributes [14].

In the case of an AlGaIn/GaN heterostructure, for example, this polarization discontinuity gives rise to a positive fixed sheet of bound charge at the heterointerface, which in turn creates an internal electric field that bends the energy bands of the underlying GaN layer. The resulting potential well confines electrons near the interface, leading to the spontaneous formation of a high-density 2DEG, the key enabler of HEMT operation, without intentional doping [15]–[17].

1.2.3 Impact on Poisson's Equation and TCAD Modeling

In TCAD simulations, polarization effects are incorporated into the right-hand side of the Poisson equation through an additional fixed charge term:

$$\nabla \cdot \vec{D} = -q(p - n + N_D^+ - N_A^-) + \rho_{PE} \quad (1.36)$$

where ρ_{PE} represents the spatial distribution of polarization-induced charges. These can be treated as, fixed sheet charges (interface-based), or volume charges (if polarization varies continuously, e.g., in graded layers).

Commercial TCAD tools such as Synopsys Sentaurus [18] allow users to define both spontaneous and piezoelectric polarization contributions using material-dependent models or custom user-defined expressions. For abrupt interfaces, fixed interface charges can be explicitly inserted at heterojunctions.

1.2.4 Importance for GaN Devices

In GaN-based HEMTs, polarization effects are not a secondary correction, but rather the primary mechanism enabling 2DEG formation and high-performance operation. The Al content in AlGaIn (or Sc content in AlScN) directly influences the polarization discontinuity and, therefore, the carrier density and electrostatics of the channel.

For example, replacing AlGaIn with AlScN as a barrier layer enhances the polarization discontinuity due to the higher spontaneous piezoelectric coefficients, leading to stronger internal electric fields, higher 2DEG densities, increased transconductance, and output current, but also potentially stronger electric-field-induced degradation mechanisms.

For these reasons, accurate modeling of polarization charges is essential in the design and simulation of modern GaN-based power and RF devices, particularly for evaluating device stability and reliability under high electric fields.

1.3 Thermal Effects and Self-Heating Models

GaN HEMTs, especially those designed for high-power or high-voltage applications, are prone to self-heating due to high current densities and electric fields. The resulting temperature rise can significantly impact carrier mobility, threshold voltage, leakage currents, and accelerate degradation mechanisms, making thermal analysis an essential aspect of device reliability.

To model these effects, TCAD tools solve the lattice heat conduction equation:

$$\nabla \cdot (k \nabla T) + H = 0 \quad (1.37)$$

where k is the thermal conductivity (potentially temperature-dependent), and H is the volumetric heat generation rate, typically dominated by Joule heating $H = \vec{J} \cdot \vec{E}$.

In the Sentaurus Device, thermal effects can be modeled by activating the thermodynamic option, which accounts for self-heating.

A more advanced formulation with the Hydrodynamic model accounts for energy-exchange mechanisms involving carrier transport and recombination. Although these implementations enable more accurate modeling of temperature distributions, especially under high-field or transient conditions, it remains outside the scope of this work.

In this work, temperature effects were included through the temperature dependence of transport and recombination models within the drift–diffusion formulation, under isothermal conditions set to match the experimental stress environment (e.g., during HTRB). This allows a realistic evaluation of degradation trends at elevated temperature without resorting to full electro-thermal coupling.

These advanced thermal models may be incorporated into future analyses to better evaluate temperature-related contributions to stress-induced degradation, which are currently not included due to convergence challenges encountered during preliminary simulation attempts.

1.4 Recombination and Generation Processes

Carrier generation and recombination mechanisms govern the transitions of electrons between the valence and conduction bands, fundamentally affecting carrier dynamics in semiconductors. The physical mechanisms discussed in this section are well established and widely treated in the semiconductor physics literature, and can be broadly classified into direct and trap-assisted mechanisms. In direct transitions, carriers recombine or are generated without the involvement of intermediate energy states, as in the case of Auger recombination or impact ionization. In contrast, trap-assisted

processes involve localized energy states within the bandgap, commonly introduced by defects in the crystal lattice, which facilitate carrier transitions. This class of processes is described by the SRH theory [19], and is particularly relevant in the modeling of GaN-based devices where defect-related traps can strongly influence leakage currents and reliability behavior.

1.4.1 Shockley–Read–Hall Recombination

The SRH model describes trap-assisted thermal generation and recombination processes by considering a discrete energy level E_t within the bandgap, typically associated with lattice defects or impurities. In its standard formulation, under steady-state conditions, the SRH theory assumes the presence of a single dominant trap level. In this framework, the different capture and emission processes illustrated in Fig. 1.1 refer to the same energy level, which must therefore be interpreted as being energetically aligned across the various transitions. If multiple trap levels are physically present, the SRH formalism can be applied independently to each level, and the total recombination–generation rate is obtained by summing the individual contributions.

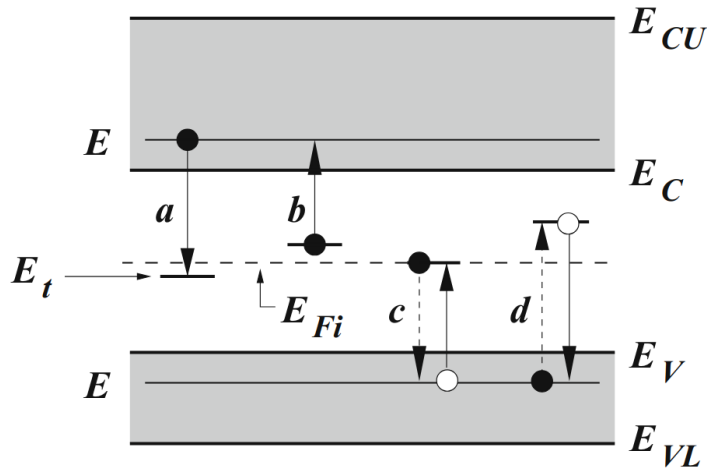


Figure 1.1: Schematic representation of different trap-assisted transitions involved in Shockley–Read–Hall recombination and generation, adapted from [2]. The illustrated transitions refer to a single trap level E_t , which must be interpreted as being energetically aligned across the different processes. In this notation, E_{Fi} is the Fermi level, E_C and E_V denote the lower edge of the conduction band and the upper edge of the valence band, respectively, while E_{CU} and E_{VL} indicate the upper and lower edges of the conduction and valence bands.

The SRH recombination rate is expressed as:

$$U_{\text{SRH}} = \frac{np - n_i^2}{\tau_p(n + n_1) + \tau_n(p + p_1)} \quad (1.38)$$

Here, n_i is the intrinsic concentration value, and τ_n, τ_p are the characteristic electron and hole lifetimes. The terms n_1 and p_1 reflect the influence of the trap level and are given by:

$$n_1 = n_i \exp\left(\frac{E_t - E_i}{k_B T}\right) \quad (1.39a)$$

$$p_1 = n_i \exp\left(\frac{E_i - E_t}{k_B T}\right) \quad (1.39b)$$

where E_i is the intrinsic Fermi level, E_t the trap energy level.

As part of the SRH formalism, trap-assisted recombination can be described in terms of carrier capture and emission processes occurring at the trap level. For electrons, the capture rate is defined as $c_n = \sigma_n v_{\text{th}} n$, where σ_n is the capture cross section, v_{th} the thermal velocity, and n the electron concentration. The corresponding emission rate is expressed as $e_n = \sigma_n v_{\text{th}} n_i \exp\left(\frac{E_t - E_i}{k_B T}\right)$, where n_i is the intrinsic carrier concentration. Both processes are thermally activated and strongly depend on the trap position within the bandgap.

As evident from the exponential dependence, SRH recombination is highly sensitive to both the energy position of the trap and the temperature, with elevated temperatures typically enhancing the emission and capture rates.

The net SRH rate becomes positive (recombination-dominated) when $np > n_i^2$, and negative (generation-dominated) when $np < n_i^2$, thus depending on the deviation of the carrier product from its equilibrium value.

1.4.2 Donor- and Acceptor-like Traps in Semiconductors

Defects and impurities in the semiconductor lattice introduce localized energy states within the bandgap, commonly referred to as traps. Depending on their charge transition levels, these traps can behave as *donor-like* or *acceptor-like* centers. Donor traps are neutral when empty and become positively charged when fully occupied, while acceptor traps are neutral when unoccupied and negatively charged when filled. Their occupancy depends on the Fermi level position and on the capture and emission processes described in the SRH formalism.

The energy distribution of traps can vary significantly depending on the material and growth conditions. In wide bandgap semiconductors such as GaN, both deep and shallow traps coexist, often associated with point defects (e.g., vacancies, impurities)

or extended defects (e.g., dislocations). Deep-level traps, particularly those located near mid-gap, are the most effective in modifying carrier dynamics and contributing to current collapse, threshold voltage shifts, or leakage.

In advanced TCAD frameworks, these traps can later be explicitly defined with specific charge states and energy distributions to reproduce their experimental behavior. A detailed discussion on the implementation of these trap models within the simulation environment is provided in Chapter 3, subsection 3.5.2.

1.4.3 Nonlocal Tunneling at Interfaces, Contacts, and Junctions

Tunneling through potential barriers is an inherently nonlocal quantum-mechanical process, since the tunneling probability depends on the energy-band profile along the entire path between the points connected by tunneling. In wide-bandgap semiconductors such as GaN or AlGaIn, the large potential barriers make tunneling an essential transport mechanism, particularly at interfaces, contacts, and heterojunctions under high electric fields [20]–[22].

In the nonlocal formulation implemented in Sentaurus Device, the band-edge profile is obtained self-consistently from the coupled solution of the Poisson and carrier-transport equations. This ensures that the local potential variations and electric-field distribution are fully taken into account when evaluating the transmission probability.

The model is based on the WKB approximation, which uses the local (imaginary) wave number of a carrier with energy ε at position r . For electrons tunneling through the conduction band, the wave number is

$$\kappa_{C,v}(r, \varepsilon) = \sqrt{2m_C(r) |E_{C,v}(r) - \varepsilon|} \Theta[E_{C,v}(r) - \varepsilon] / \hbar, \quad (1.40)$$

where m_C is the tunneling effective mass, $E_{C,v}$ is the v -th shifted conduction-band edge, and Θ is the Heaviside function. For holes, an analogous expression holds:

$$\kappa_{V,v}(r, \varepsilon) = \sqrt{2m_V(r) |\varepsilon - E_{V,v}(r)|} \Theta[\varepsilon - E_{V,v}(r)] / \hbar, \quad (1.41)$$

where m_V and $E_{V,v}$ denote the valence-band tunneling mass and the shifted valence-band energy, respectively.

The tunneling probability between two spatial points l and $u > l$ for a carrier of energy ε is then obtained as

$$\Gamma_{CC,v}(u, l, \varepsilon) = T_{CC,v}(l, \varepsilon) \exp \left[-2 \int_l^u \kappa_{C,v}(r, \varepsilon) dr \right] T_{CC,v}(u, \varepsilon), \quad (1.42)$$

$$\Gamma_{VV,v}(u, l, \varepsilon) = T_{VV,v}(l, \varepsilon) \exp \left[-2 \int_l^u \kappa_{V,v}(r, \varepsilon) dr \right] T_{VV,v}(u, \varepsilon), \quad (1.43)$$

where $T_{CC,v}$ and $T_{VV,v}$ are the interface transmission coefficients at the lower and upper ends of the tunneling path.

When both conduction- and valence-band contributions are relevant, Sentaurus Device uses a two-band (Franz) dispersion relation that smoothly interpolates between the two regimes:

$$\kappa_v = \frac{\kappa_{C,v} \kappa_{V,v}}{\sqrt{\kappa_{C,v}^2 + \kappa_{V,v}^2}}. \quad (1.44)$$

Near the band edges this reduces to the single-band expressions above, while in the intermediate regime it accurately represents mixed band-to-band tunneling (BTBT) processes.

Overall, the nonlocal tunneling current is obtained by integrating the transmission probability along the nonlocal path, multiplied by the carrier distribution and the density of states. A schematic representation of these contributions is shown in Fig. 1.2, where J_{cc} and J_{vv} denote same-band tunneling contributions (conduction-to-conduction and valence-to-valence), which are evaluated at the interface, while J_{cv} and J_{vc} represent band-to-band tunneling processes between conduction and valence bands across the barrier. This formalism provides the physical basis for the modeling of Schottky barriers, metal–semiconductor contacts, and heterointerfaces in GaN-based devices. The same framework is extended to include trap-mediated tunneling processes, as discussed in Section 1.4.4.

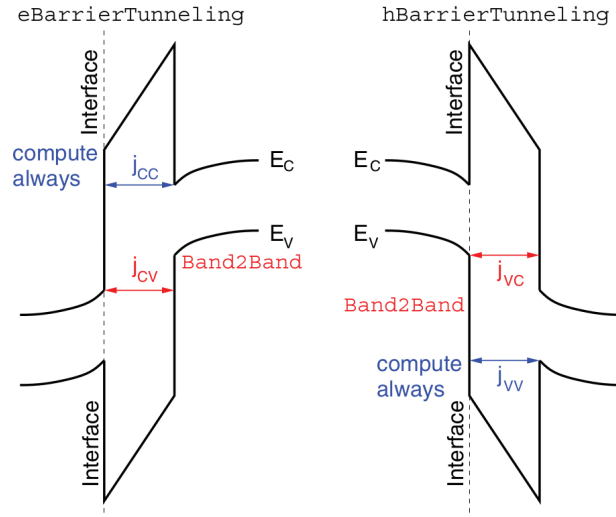


Figure 1.2: Schematic illustration of the various non-local tunneling current contributions in a semiconductor band diagram. The terms J_{cc} and J_{vv} indicate same-band tunneling components, while J_{cv} and J_{vc} denote band-to-band tunneling contributions across the barrier. The tunneling generation depends on the band profile along the entire tunneling path (adapted from [18]).

1.4.4 Nonlocal Trap-Assisted Tunneling (nonlocal TAT)

The nonlocal tunneling formalism introduced in the previous section can be extended to describe carrier exchange between traps and remote regions such as interfaces or contacts. In this framework, traps are no longer restricted to local capture and emission processes but can interact with external carrier reservoirs through tunneling across the potential barrier. This mechanism, referred to as nonlocal trap-assisted tunneling (nonlocal TAT), enables the simulation of field-enhanced leakage through insulating or wide-bandgap layers in semiconductor devices. The phenomenon is illustrated in Fig. 1.3.

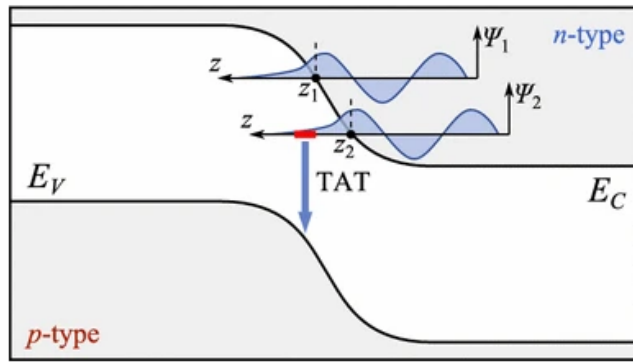


Figure 1.3: Schematic illustration of trap-assisted tunneling (TAT) in the band diagram of a forward-biased p–n junction adapted from [23]. In the presence of defect levels within the bandgap, carriers can tunnel through the barrier via localized trap states, enabling recombination processes that are otherwise forbidden in a defect-free structure.

In the Sentaurus Device implementation, traps can be coupled to nearby interfaces or contacts by means of tunneling paths defined on a dedicated nonlocal mesh. Each nonlocal line connects the spatial position of the trap to a corresponding point at the interface or contact, allowing the simulator to evaluate the tunneling probability along that path. The overall nonlocal TAT current is modeled as the sum of two distinct physical contributions: an *elastic* process, in which the carrier tunnels without energy exchange, and a *phonon-assisted inelastic* process, where multiple phonons are emitted or absorbed during tunneling[24], [25]. The total trap-to-band capture rate is obtained as the sum of these two components:

$$c_C = c_{C,\text{elastic}} + c_{C,\text{phonon}}, \quad (1.45)$$

and analogous expressions hold for holes in the valence band [24], [25].

Both capture rates depend on the local band-edge alignment and on the ratio of

the electronic wavefunctions at the trap site and the interface, which is computed according to the WKB tunneling probability described in Section 1.4.3. For the inelastic process, the rate also depends on the phonon energy $\hbar\omega$, the Huang–Rhys factor S , and the Bose–Einstein occupation of the phonon state $f_B = [\exp(\hbar\omega/k_B T) - 1]^{-1}$, which together determine the strength of electron–phonon coupling. The trap interaction volume V_T and the tunneling mass m_t are further parameters that control the spatial extent of the coupling and the tunneling efficiency.

In the elastic transition, the electron tunnels directly from the conduction band to the trap level, and the capture rate depends on the barrier height, the trap interaction volume V_T , the tunneling mass m_t , the occupation of trap state and on the WKB transmission probability evaluated at the trap energy. In contrast, in the inelastic phonon-assisted process, the carrier undergoes an energy relaxation mediated by the emission of l phonons, with a probability proportional to $\exp[-S(2f_B + 1)]$. The emission and capture rates are related through the principle of detailed balance, ensuring that the model remains thermodynamically consistent.

This nonlocal TAT formulation provides a physically accurate framework to describe carrier transport through traps embedded in dielectric or barrier regions. It is particularly important in GaN-based HEMTs, where leakage under forward or reverse bias is dominated by field-assisted tunneling mechanisms involving deep trap states at the dielectric/barrier interface or within the barrier layers. The implementation of this model within the TCAD environment is presented in Chapter 3.5.4, while it is adopted in Chapter 4.

1.4.5 Radiative Recombination

Radiative recombination corresponds to a direct band-to-band transition in which electron–hole recombination is accompanied by the emission of a photon, while the inverse process, optical generation, occurs through photon absorption with energy exceeding the bandgap.

A schematic illustration of radiative recombination and optical generation processes is shown in Fig. 1.4. In this representation, h denotes Planck’s constant, ν the photon frequency, and E_g the semiconductor bandgap. Process (a) corresponds to radiative recombination, where the energy difference between the initial and final states is released as a photon, while process (b) represents optical generation due to photon absorption with $h\nu > E_g$.

Although GaN is a direct-bandgap semiconductor widely exploited in optoelectronic devices, radiative generation–recombination processes are negligible in GaN HEMTs designed for power and RF applications, due to the absence of optical excitation and the dominance of trap-assisted and high-field transport mechanisms. For

this reason, radiative recombination is not included in the simulations presented in this work, and will not be discussed further.

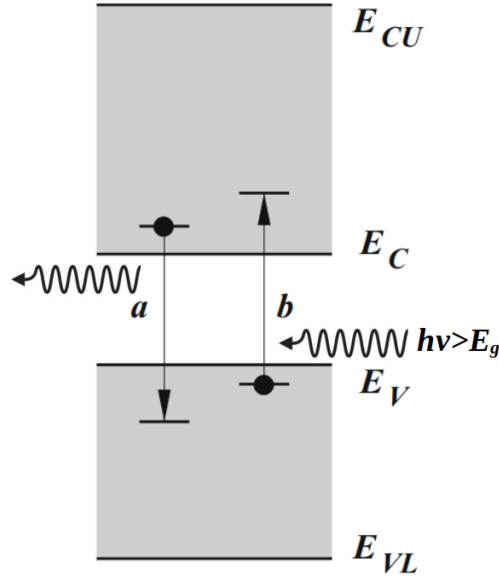


Figure 1.4: Schematic representation of direct optical recombination (a) and optical generation (b). In radiative recombination, the energy released during electron–hole recombination is emitted as a photon, whereas optical generation occurs through photon absorption with energy exceeding the bandgap ($h\nu > E_g$). Adapted from [2].

1.4.6 Auger Recombination

Auger recombination is a non-radiative, direct interband process in which the recombination energy of an electron-hole pair is transferred to a third carrier, rather than being emitted as a photon. This mechanism can be initiated either by electrons or holes and becomes significant in conditions of high carrier concentration. The phenomenon due to the electron-electron or hole-hole collision is illustrated in Fig. 1.5.

In the case of electron-initiated Auger recombination, two electrons in the conduction band interact: one recombines with a hole in the valence band, while the other receives the excess energy and is excited to a higher state in the conduction band. An analogous process occurs for hole-initiated Auger recombination, involving two holes and one electron. These processes can be described by the following expressions:

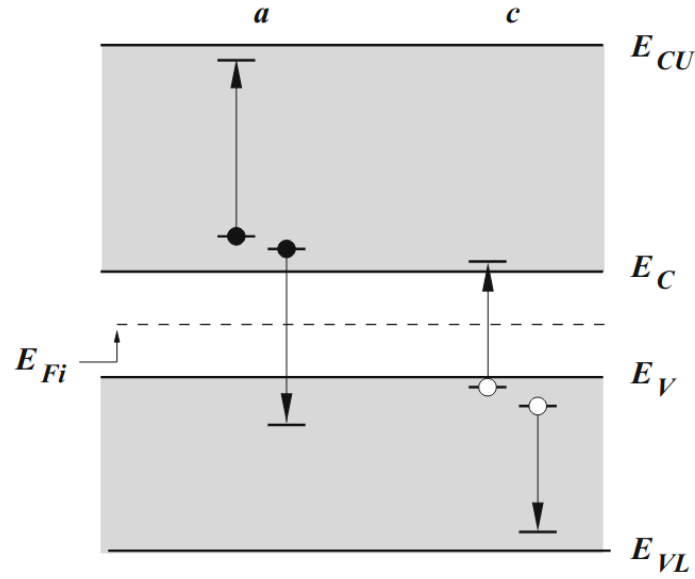


Figure 1.5: Schematic view of Auger recombination initiated by electrons (a) and holes (c), adapted from [2].

$$U_{An} = c_n n^2 p \quad (1.46a)$$

$$U_{Ap} = c_p p^2 n \quad (1.46b)$$

where c_n and c_p are the Auger recombination coefficients for electron- and hole-initiated processes, respectively, and n and p are the local electron and hole concentrations.

Due to the cubic dependence on carrier density, Auger recombination is typically negligible at room temperature under low-injection conditions, where phonon interactions dominate carrier scattering. However, it becomes particularly relevant in heavily doped regions, in high-injection scenarios, or under strong electric field conditions, such as those encountered in power devices based on GaN.

Although the wide bandgap of GaN generally suppresses Auger recombination compared to narrower-gap semiconductors (e.g., GaAs), recent experimental and theoretical studies have suggested that Auger processes may still play a non-negligible role, particularly in high-current-density devices such as LEDs and HEMTs under high bias [26]. In the present simulations, the Auger recombination model was enabled to ensure a complete description of carrier recombination phenomena. However, its specific contribution was not explicitly isolated or analyzed, as no clear evidence of Auger-limited behavior emerged from the simulated conditions. Its inclusion mainly serves to guarantee physical consistency under possible high carrier

injection or high-field conditions.

1.4.7 Impact Ionization / Avalanche Generation

Impact ionization is another critical generation process in GaN devices, particularly under high electric field conditions that can arise during off-state stress or breakdown events. This process involves the creation of electron-hole pairs via carrier impact, potentially leading to avalanche multiplication and device degradation. The impact-ionization transitions are illustrated in Fig. 1.6. However, including impact ionization in TCAD simulations introduces significant numerical challenges, often resulting in convergence difficulties when combined with complex trap and thermal models. Consequently, impact ionization has not been incorporated in the current simulation framework, but it remains a subject for future study to better understand breakdown and reliability phenomena.

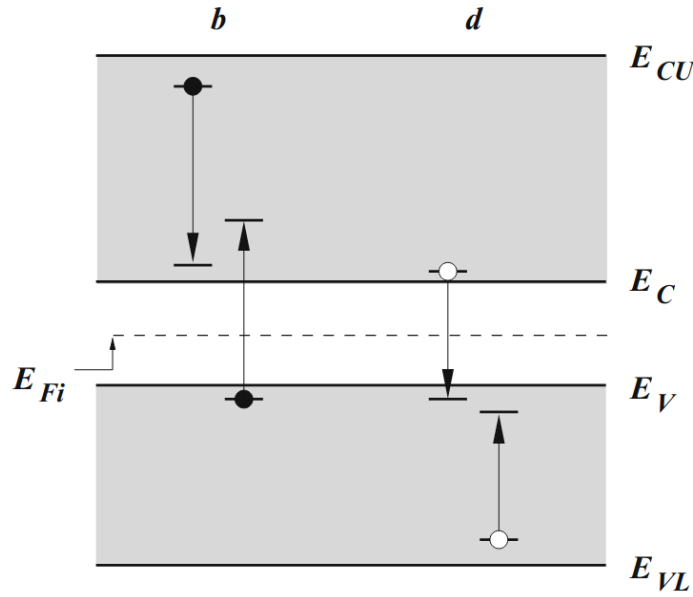


Figure 1.6: Schematic view of Impact-ionization transitions initiated by electrons (b) and holes (d), adapted from [2].

1.5 Implementation in the TCAD Tool

The physical models discussed throughout this chapter are implemented in commercial TCAD frameworks such as Synopsys Sentaurus, which provide a comprehensive set of numerical solvers and user-configurable physical models. The drift-diffusion

equations are solved self-consistently with Poisson's equation and carrier continuity relations on a discretized spatial mesh, using either Newton or Gummel iterative schemes depending on convergence requirements.

Carrier mobility is typically modeled through empirical or semi-empirical formulations such as the Masetti model for doping-dependent mobility degradation, and the Caughey-Thomas expression for field-dependent velocity saturation. These models are often complemented by anisotropic corrections in the case of GaN-based devices. Polarization charges are introduced either as fixed interface charges or as distributed charge densities, and their values must be carefully calibrated to reproduce the experimentally observed two-dimensional electron gas (2DEG) concentration. Trap-assisted recombination and leakage processes are described using the Shockley-Read-Hall framework, complemented by field-enhanced emission mechanisms such as the tunneling-assisted transitions when required.

Calibration plays a central role in ensuring the predictive capability of TCAD simulations. Experimental transfer and output characteristics are employed to fine-tune mobility, polarization, and trap parameters, while capacitance-voltage (C-V) and Hall measurements provide key constraints for 2DEG density and threshold voltage extraction. Numerical robustness is another critical aspect: convergence difficulties often arise in the presence of abrupt heterointerfaces, strong polarization fields, or dense trap distributions. Common strategies to mitigate these issues include adaptive mesh refinement, transient pre-biasing, and stepwise voltage ramping to achieve stable and physically consistent solutions.

Overall, the implementation of these physical models in TCAD offers a highly flexible yet non-trivial simulation environment, where physical accuracy must be balanced with numerical stability and calibration fidelity.

1.6 Summary and Relevance to This Work

This chapter has outlined the theoretical background and numerical formulations required to model charge transport, recombination-generation mechanisms, high-field effects, polarization, and trapping phenomena in semiconductor devices. These concepts constitute the foundation upon which the TCAD analyses of GaN-based HEMTs are built. In particular, the accurate treatment of polarization-induced charges, trap-assisted conduction, and mobility degradation mechanisms will be essential to capture both the static behavior and the long-term reliability of these devices.

While the discussion presented here focused on general semiconductor models and their implementation within commercial TCAD tools, the subsequent chapters

progressively specialize this framework. Chapter 2 introduces GaN technology in detail, emphasizing its material properties, advantages over other wide-bandgap semiconductors, and the key role of AlGaN/GaN heterostructures in enabling high-performance transistors. Chapter 3 then addresses the practical challenges of applying these models to GaN HEMTs, highlighting the calibration procedures, physical limitations, and numerical instabilities that may arise in advanced simulations.

By bridging theoretical modeling with numerical implementation, this chapter provides the essential background for understanding the device-level analyses and reliability investigations presented in the following sections of this thesis.

Chapter 2

GaN Technology: From Materials to Device Architectures

Chapter Overview

This chapter reviews GaN technology from a device- and TCAD-oriented perspective. It begins with a concise introduction to GaN as a WBG semiconductor, comparing its key physical properties with those of Si, SiC, diamond, and AlN, and summarizing the main HEMT device variants (enhancement- and depletion-mode). Subsequently, a GaN transistor is conceptually built from the substrate upward, analyzing the function of each layer (substrate, nucleation/buffer, channel, barrier, cap/passivation, and contacts), together with the associated materials, defects, and their modeling relevance. The chapter concludes with an overview of reliability mechanisms, providing the motivation for the calibrated TCAD approach discussed in Chapter 3

2.1 Introduction to GaN as a Wide Bandgap Semiconductor

This introductory subsection describes the evolution of GaN technology, from early milestones achieved in the laboratory to the commercial production of high-performance HEMT devices, thus laying the groundwork for the discussions on the material and devices that follow.

2.1.1 The Rise of Gallium Nitride Technology

GaN technology emerged as a compelling alternative to silicon in the early 2000s, driven by the demand for higher blocking voltages, faster switching speeds, and superior power density in both RF and power conversion systems (see Fig. 2.1 for the evolution of GaN HEMT technology). Early commercial developments began around 2004, when the Japanese firm *Eudyna Corporation* introduced depletion-mode GaN HEMTs for RF applications, fabricated on GaN-on-SiC substrates [27].

The concept underlying the HEMT architecture can be traced back to the pioneering work of Mimura *et al.* (1975) and Khan *et al.* (1994), who independently demonstrated the unusually high electron mobility, identified as a 2DEG, at the heterointerface between AlGaN and GaN layers [28], [29]. This discovery provided the physical foundation for polarization-induced electron confinement in III-nitride heterostructures, marking the birth of the GaN HEMT concept.

In 2005, Nitronex Corporation introduced the first depletion-mode RF HEMT fabricated on silicon substrates, paving the way for cost-effective large-area GaN growth. Four years later, in 2009, Efficient Power Conversion (EPC) Corporation commercialized the first enhancement-mode GaN-on-Si field effect transistors (FETs) optimized for power electronics, demonstrating reliable normally-off operation and CMOS-compatible packaging.

The superior performance of GaN arises from its wide bandgap, high critical electric field, and the strong spontaneous and piezoelectric polarization intrinsic to its wurtzite lattice. These properties enable lateral transistor architectures with extremely thin drift regions, reduced parasitic capacitances, and the formation of a high-density 2DEG at III-nitride heterointerfaces, resulting in record transconductances, current densities, and switching efficiencies. Such attributes translate into high power density, wide-bandwidth operation, and superior energy efficiency compared to traditional silicon devices. By the 2010s, major semiconductor manufacturers announced their intention to manufacture GaN transistor for the power conversion market. A significant milestone was reached in 2018 with the demonstration of a

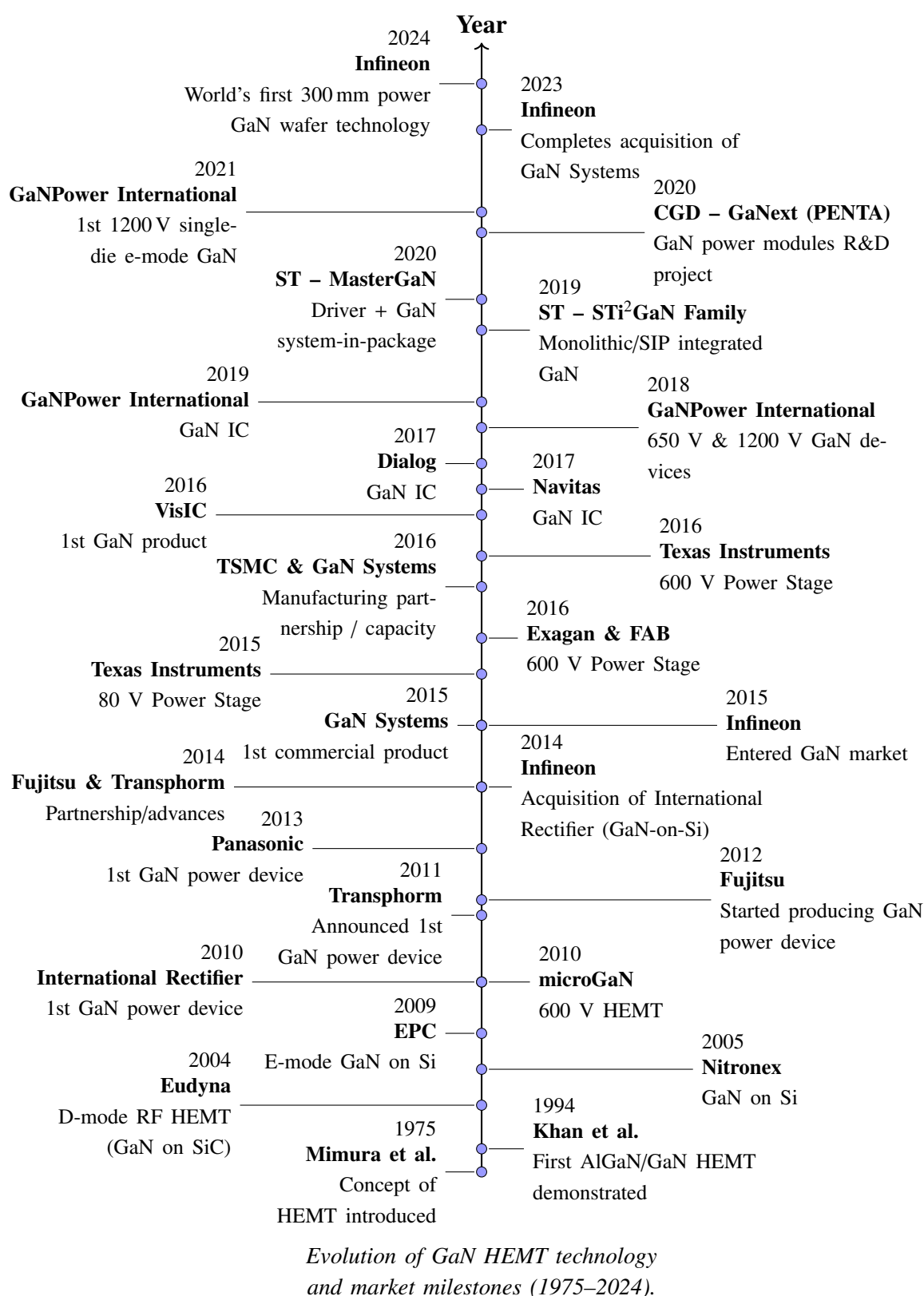


Figure 2.1: Vertical timeline of GaN HEMT technology and market milestones (1975–2024).

1200 V lateral GaN HEMT, confirming that GaN was no longer limited to niche RF applications but had matured into a competitive solution for high-voltage power electronics.

Today, GaN devices are deployed across a broad range of domains, from 650 V-class power converters in data centers and electric vehicles to mm-wave RF amplifiers in satellite and defense systems. Continuous advancements in epitaxial growth, packaging, and reliability have established GaN as a cornerstone among wide-bandgap technologies. Nonetheless, the full exploitation of its potential depends on the technology ripeness, which is supported by the accurate modeling of polarization effects, trapping phenomena, and electrothermal interactions, topics that will be addressed in the following sections.

This section has outlined the historical and technological evolution of GaN, providing the context for its comparison with other incumbent (Si, SiC) and emerging (AlN, diamond) materials discussed next.

2.1.2 Physical Properties of GaN vs. Si, SiC, Diamond, and AlN

The outstanding performance of GaN-based devices arises from a unique combination of intrinsic material parameters that differ markedly from those of conventional semiconductors.

The bandgap of a semiconductor (E_g) is closely related to the strength of the chemical bonds within its crystal lattice. Stronger bonds make it more difficult for electrons the transition from the valence to the conduction band. GaN exhibits a direct bandgap of approximately 3.4 eV at 300 K, much wider than that of Si (1.12 eV) and comparable to that of 4H-SiC (3.26 eV). Both GaN and SiC are therefore classified as WBG semiconductors, offering enhanced blocking capability and thermal stability compared to silicon. Larger gaps are observed in AlN (6.0 eV) and diamond (5.5 eV), placing them in the class of ultra-wide-bandgap (UWBG) semiconductors, relevant for extreme-field and high-temperature operation. The WBG drastically reduces the intrinsic carrier concentration, leading to lower leakage current and stable operation at elevated temperatures, both essential for high-power and high-frequency devices [30], [31].

The same strong atomic bonds responsible for the latter also yield a higher critical electric field (E_{crit}), i.e., the field strength required to initiate avalanche breakdown through impact ionization. For GaN, E_{crit} lies in the 3–3.5 MV/cm range, about ten times that of Si (0.3 MV/cm) and slightly higher than that of SiC (2.5–3 MV/cm). This property allows GaN devices to sustain large voltages with thinner drift regions,

resulting in lower specific on-resistance R_{on} , as described by Baliga's figure of merit (FOM) [32].

The breakdown voltage V_{BR} can be approximated as:

$$V_{\text{BR}} \approx \frac{1}{2} w_{\text{drift}} \cdot E_{\text{crit}}, \quad (2.1)$$

where w_{drift} is the width of the drift region. Under conditions of complete depletion, Poisson's equation yields the charge balance in the n -type drift layer as:

$$qN_{\text{D}} = \epsilon_0 \epsilon_r \frac{E_{\text{crit}}}{w_{\text{drift}}}. \quad (2.2)$$

From this relation, if the critical field is ten times higher, the drift region can be ten times thinner for the same voltage rating, enabling a hundredfold increase in carrier density N_{D} . This explains why GaN and other WBG materials can achieve far lower R_{on} and higher efficiency than silicon in power conversion systems [33].

Thermal management represents a key challenge for GaN devices. The thermal conductivity of bulk GaN ranges from 130 to 240 W/m·K, lower than that of SiC (370 W/m·K) and much lower than diamond (~ 2000 W/m·K), yet still sufficient for most lateral HEMTs when grown on thermally conductive substrates such as SiC. The limited thermal conductivity, however, can lead to self-heating and thermal runaway in high-power or high-frequency operation, making thermal modeling crucial in TCAD simulations [10], [34]–[36].

From a transport perspective, GaN exhibits room-temperature electron mobilities in the 1000–1800 cm²/V·s range, slightly lower than silicon but combined with a high saturation velocity ($v_{\text{sat}} \approx 2.5 \times 10^7$ cm/s). This supports rapid carrier transit and enables switching frequencies in the multi-megahertz regime [37], [38]. Carrier transport in GaN is primarily limited by polar optical phonon scattering and interface roughness, both of which must be carefully modeled in calibrated mobility expressions for accurate TCAD predictions [9].

A key differentiator of GaN and related III-nitrides is the presence of strong spontaneous and piezoelectric polarization due to the lack of inversion symmetry in the wurtzite crystal structure. At heterointerfaces such as Al(Ga,Sc)N/GaN, discontinuities in these polarization fields induce bound charges that create an internal electric field. This field bends the energy bands and forms a triangular quantum well at the interface, confining electrons in a narrow region, known as the 2DEG, without the need for intentional doping [16], [39].

The 2DEG sheet density n_s , typically in the range of $1\text{--}2 \times 10^{13}$ cm⁻², depends on the barrier composition (material and molar fraction), strain, and interface conditions. This channel supports extremely high current densities and transconductance

Table 2.1: Key Physical Properties of Si, 4H-SiC, GaN, AlN, and Diamond at 300 K.

Property	Si	4H-SiC	GaN	AlN	Diamond
Bandgap E_g (eV)	1.12	3.26	3.40	6.00	5.50
Electron mobility μ_n (cm ² /Vs)	1400	950	1350	300	2200
Hole mobility μ_p (cm ² /Vs)	450	115	150	20	1800
Critical field E_{crit} (MV/cm)	0.3	2.5–3.0	3.0–3.5	15	10
Thermal conductivity κ (W/m·K)	150	370	130–240	285	2000
Saturation velocity v_{sat} (cm/s)	1.0×10^7	2.0×10^7	2.5×10^7	2.7×10^7	2.7×10^7
Relative permittivity ϵ_r	11.8	9.7	8.9	8.5	5.5
Intrinsic carrier conc. n_i (cm ⁻³)	1.45×10^{10}	< 1	< 1	$\ll 1$	$\ll 1$
Breakdown field / bandgap ratio (MV/cm·eV)	0.27	0.83	1.03	1.67	1.82

Data from [16], [30]–[33], [37]–[39]. Values are typical for 300 K; ranges indicate material- and orientation-dependent variability.

while minimizing scattering. The polarization-induced 2DEG is the fundamental mechanism enabling high electron mobility, low access resistance, and efficient lateral device scaling in GaN HEMTs. In advanced structures employing AlScN barriers, the large spontaneous piezoelectric coefficient of Sc enhances polarization-induced charge even further, increasing n_s but also introducing potential reliability issues—topics discussed in later chapters [40]–[42].

Table 2.1 summarizes the key physical constants of Si, 4H-SiC, GaN, AlN, and diamond, highlighting how GaN has already become a core wide-bandgap material for high-efficiency power and RF electronics, while remaining a promising platform for further technological advancement [30], [31], [39].

2.1.3 GaN Transistor Structures: Enhancement vs. Depletion Mode

Conventional AlGaIn/GaN HEMTs are *normally-on* (depletion-mode, D-mode), since the polarization-induced 2DEG is present at $V_{\text{GS}} = 0$. For power electronics, *normally-off* (enhancement-mode, E-mode) operation is preferred for fail-safe behavior and gate driving [30], [43]. Several device strategies enable a positive threshold while balancing on-resistance, dynamic performance, and reliability.

The recessed gate adopts a local thinning of the barrier under the gate depletes the 2DEG and shifts V_{th} to positive values. The recess can be implemented in Schottky- or MIS-gate stacks; process control (Atomic layer etching/Inductively Coupled Plasma Etching, post-anneal) is crucial to limit interface damage and gate leakage [44]–[47]. Recessed InAlN/AlN/GaN and AlGaN/GaN MIS-HEMTs have demonstrated E-mode with low leakage and high ON/OFF ratios, at the expense of tighter etch tolerances, a great influence from the barrier height and trap densities [44], [45].

Fluorine (F) implantation introduces negative fixed charge in the barrier beneath the gate region, electrostatically depleting the channel and pushing V_{th} to positive values [48]–[50]. The approach is mask- and process-compatible (plasma treatment), but reproducibility, V_{th} instabilities, long-term charge stability, hysteresis, and bias-temperature stress effects demand careful reliability assessment [43].

One of the most adopted configuration is the p-GaN gate HEMT. A thin Mg-doped p -GaN gate above the barrier forms a p – n junction that suppresses the 2DEG under the gate at zero bias, yielding a robust positive V_{th} and an industrially adopted E-mode architecture [51]–[53]. Gate stack engineering involves trade-offs between leakage and dynamic R_{on} ; challenges include gate reliability (hard/soft breakdown, TAT) and threshold stability under high-field stress [51]–[59].

Among the normally-off configurations, two notable approaches are the cascode and the recessed-gate hybrid MIS-HEMT. The cascode configuration combines a low-voltage normally-off Si or SiC MOSFET in series with a high-voltage normally-on GaN HEMT, enabling overall enhancement-mode behavior while retaining the switching performance of GaN [43]. Alternatively, recessed-gate hybrid MIS-HEMTs can optimize the threshold voltage (V_{th}) up to +2 V while maintaining low R_{on} . In these devices, the barrier under the gate is partially removed by plasma etching, and the recessed GaN region is subsequently passivated with a dielectric layer [39], [43].

E-mode solutions inherently balance threshold control vs. access resistance and dynamic performance. Recess improves gate control but is sensitive to etch-induced defects; fluorine-based methods are simple but may introduce charge-instability and hysteresis; p -GaN gates offer a stable, industry-proven V_{th} with attention to gate leakage and robustness; hybrid stacks can mitigate single-technique drawbacks at the expense of process complexity [39], [43], [51].

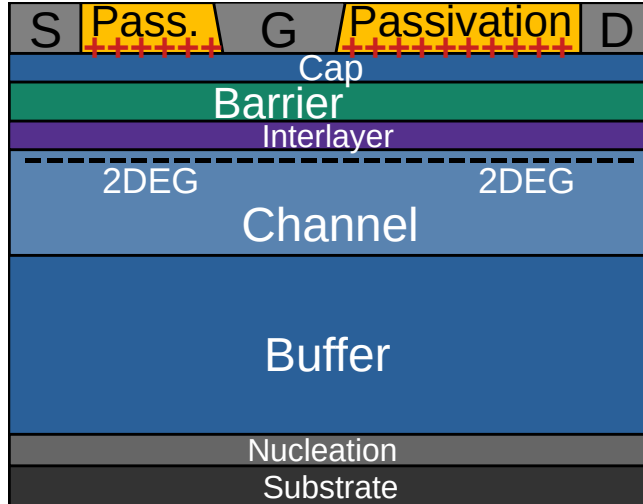


Figure 2.2: Schematic cross-section of a lateral Al(Ga,Sc)N/GaN HEMT highlighting the main layers and interfaces.

2.2 Building a GaN Transistor: A Layer-by-Layer Perspective

In practical devices, the intrinsic advantages of III-nitride materials are realized through a carefully engineered stack (Fig. 2.2). This section follows a *layer-by-layer* perspective from substrate to contacts, linking epitaxial and process choices to their electronic signatures, reliability implications, and TCAD representations.

2.2.1 Substrates and Heteroepitaxy

The choice of substrate is a fundamental step in GaN HEMT fabrication, as it determines the crystalline quality, thermal management, mechanical stability, and ultimately the device reliability and yield. Because bulk GaN substrates remain expensive and limited in diameter, most commercial and research devices rely on *heteroepitaxial growth* of GaN on foreign substrates such as silicon carbide (SiC), silicon (Si), or sapphire. Each option offers a distinct balance between lattice and thermal compatibility, cost, and performance (see Tab. 2.2) [16], [37], [43], [60]–[66].

SiC provides the highest thermal conductivity among substrates (~ 370 W/m·K at 300 K) and a relatively small lattice mismatch to GaN (~ 3.4 – 3.5%), which together support lower threading-dislocation densities (typically 10^7 – 10^8 cm $^{-2}$ for well-optimized stacks) and efficient heat extraction [30], [67]. As a result, GaN-on-SiC remains the benchmark platform for high-frequency and high-power RF devices, where thermal management and reliability outweigh cost considerations [30], [39], [66].

Table 2.2: Structural and thermal parameters of common substrates used for GaN epitaxy at 300 K. All materials except Si (cubic diamond structure, FCC) crystallize in the wurtzite-type hexagonal phase (HCP).

Parameter	Si	4H-SiC	Sapphire	AlN	GaN
Crystal structure	FCC	HCP	HCP	HCP	HCP
Lattice constant a (Å)	5.431	3.081	4.758	3.112	3.189
Lattice mismatch to GaN (%)	-16.9	+3.5	+16.1	+2.4	–
Thermal expansion α ($10^{-6}/\text{K}$)	3.59	4.3	7.3	4.15	5.59
Thermal mismatch to GaN (%)	+55	+30	-23	+34	–
Thermal conductivity ($\text{W}/\text{m}\cdot\text{K}$)	150	370	35	285	230
Typical dislocation density (cm^{-2})	$> 10^9$ (GaN/Si)	$\sim 10^8$ (GaN/SiC)	$> 10^9$	$\sim 10^7$	$< 10^6$

Data from [16], [30], [43], [44], [68], [69]. Mismatch values are relative to GaN ($a_{\text{GaN}} = 3.189$ Å) at 300 K. Dislocation densities refer to typical threading dislocation densities (TDD) for GaN layers grown on each substrate.

Silicon offers large wafer diameters (up to 300 mm) and low cost, supporting mass production for power electronics. However, the lattice and thermal expansion mismatches between GaN and Si ($\approx 17\%$ and $\approx 55\%$, respectively) induce high tensile stress during growth and cooling, often leading to wafer bowing, cracking, and elevated threading dislocation densities ($> 10^9 \text{ cm}^{-2}$) [67], [70]–[72]. Complex buffer architectures—typically combining AlN nucleation layers (superlattice structures), step graded AlGaIn transitions, and stress-compensating interlayers are required to mitigate these mismatches [43], [72]. When properly engineered, GaN-on-Si HEMTs can achieve competitive performance in the 650–900 V range, offering scalability and integration potential at reduced cost [62], [63], [66], [72].

Sapphire was historically used in early GaN research due to its availability and optical transparency, but it exhibits poor thermal conductivity and large lattice mismatch, limiting its use for high-power operation [60], [66], [70]. Conversely, native GaN substrates grown by hydride vapor phase epitaxy (HVPE) or ammonothermal methods—enable homoepitaxial growth with threading dislocation densities down to

the order of $10^6 - 10^7 \text{ cm}^{-2}$ and negligible wafer bowing [73]. Although still more expensive, they represent the reference platform for investigating intrinsic material limits and long-term reliability [74].

Threading dislocations in GaN layers act as electrically active defects that critically impact leakage, trapping, and long-term reliability. They can serve as preferential leakage paths or as deep trap centers, degrading the blocking capability and increasing off-state and buffer leakage currents under high electric field and temperature stress [75]. The electrical activity of dislocations depends strongly on their core type and chemical decoration: screw and mixed dislocations are generally associated with vertical and gate-related leakage, whereas edge dislocations correlate with current collapse and dynamic R_{on} dispersion through associated deep-level states [76], [77]. Experimental and modeling studies have demonstrated that dislocation-related states contribute to increased gate and drain currents, bias-temperature instabilities, and early degradation phenomena in AlGaIn/GaN HEMTs [68], [69], [71]. These findings highlight the importance of including dislocation-induced traps, defined by appropriate energy levels, densities, and capture cross sections in TCAD models for GaN-on-Si and GaN-on-SiC buffer layers [68], [69], [78].

Modeling note. In this work, the substrate was represented in TCAD primarily through its electrical and thermal boundary conditions. The substrate contact was defined as the global reference node for potential (ground) and, where applicable, as the thermal sink for heat dissipation. The only physical mechanism extending across the entire structure is the piezoelectric polarization, which is inherently coupled to the strain distribution within the device. No other explicit modeling of strain fields, dislocations, or substrate-related traps was included, as their possible effects were implicitly accounted for through experimental calibration of the device characteristics.

Having discussed the substrates that provide the mechanical and thermal foundations for GaN epitaxy, attention now turns to the buffer layers, a critical transition region that accommodates lattice and thermal mismatch while electrically isolating the active device from the substrate. Its design has a direct impact on the breakdown voltage, the leakage current, and the long-term reliability.

2.2.2 Buffer Engineering

The buffer layer plays a determining role in GaN HEMT technology, serving both structural and electrical functions. Its effectiveness, however, begins with the quality of the underlying *nucleation layer*, which accommodates the large lattice and thermal mismatch between GaN and the foreign substrate. An optimized nucleation

Table 2.3: Comparison of Fe- and C-doped GaN buffer layers.

Property	Fe-doped GaN	C-doped GaN
Compensation type	Deep acceptor ($\text{Fe}^{3+/2+}$)	Deep acceptor (C_N)
Energy level ($E_\text{C} - E_\text{t}$)	0.5–0.7 eV	0.8–1.0 eV
Memory effect	Strong (reactor contamination)	Negligible
Resistivity control	Limited	Tunable via growth parameters
Interface abruptness	Challenging	Good
Thermal stability	High	High
Impact on leakage	Moderate suppression	Strong suppression
Typical applications	RF, early-generation GaN-on-SiC	Power, GaN-on-Si

Data from [30], [43], [78].

process, typically involving AlN or graded AlGaN interlayers, can significantly reduce the density of threading dislocations and surface pits propagating toward the active region [69]. This reduction is essential to ensure uniform epitaxial growth and to prevent extended defects from reaching the 2DEG channel, where they can act as scattering centers or leakage paths, ultimately degrading mobility and dynamic device performance.

The buffer itself must further relax residual stress while providing high resistivity to suppress leakage and prevent parasitic conduction paths. Inadequate buffer design can lead to premature breakdown, vertical leakage, and dynamic performance degradation such as current collapse and R_on dispersion [30], [43], [78].

Undoped GaN layers typically exhibit unintentional n-type conductivity due to the presence of residual shallow donors such as oxygen and silicon introduced during epitaxial growth, furthermore also dislocations assist the charge transport, resulting in low resistivity unsuitable for power devices [15], [37], [69]. To achieve semi-insulating behavior, deep acceptor dopants are introduced to compensate these donors (Tab. 2.3). Historically, iron (Fe) was the first p-type dopant adopted in GaN buffers because of its deep acceptor level ($E_\text{C} - E_\text{t} \approx 0.5\text{--}0.7$ eV) and strong carrier-trapping capability [43]. However, Fe suffers from a significant memory effect in MOCVD reactors, leading to contamination of subsequent epitaxial layers and difficulties in obtaining abrupt interfaces (Fig. 2.3)[78]–[80]. Carbon (C) has therefore become the preferred compensating dopant: it produces deep acceptor levels ($E_\text{C} - E_\text{t} \approx 0.8\text{--}1.0$ eV) without memory effects, and its incorporation can be finely

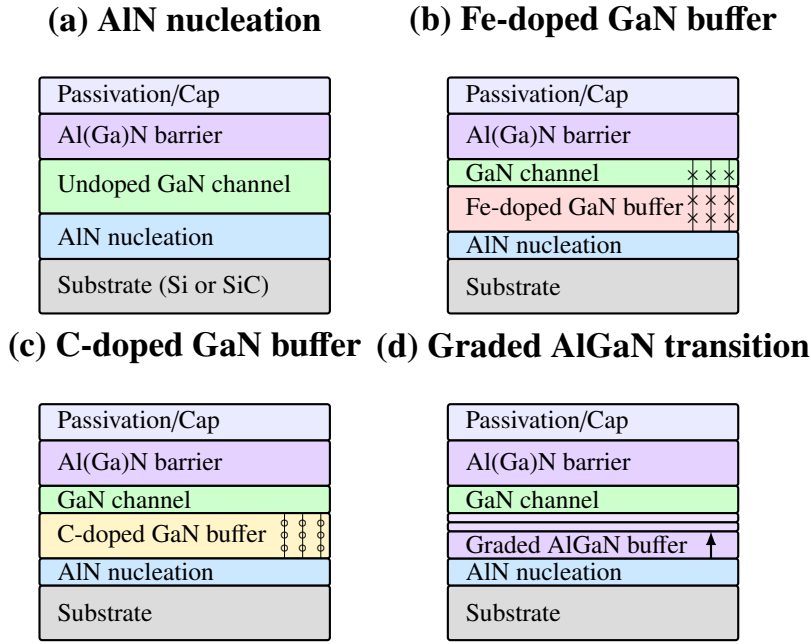


Figure 2.3: Schematic cross-sections of typical buffer configurations in GaN HEMTs: (a) AlN nucleation layer for stress relief on foreign substrates; (b) Fe-doped GaN semi-insulating buffer (deep Fe acceptors, memory effect in MOCVD) with AlN nucleation; (c) C-doped GaN semi-insulating buffer (C_N acceptors with tunable resistivity and breakdown) with AlN nucleation; (d) graded AlGaIn transition layers for strain management and electric-field shaping with AlN nucleation. Labels indicate layer functions; symbols ($\times$, $\circ$) depict representative dislocations/traps for illustration.

tuned through precursor flow and growth temperature (Fig. 2.3). Adjusting C concentration enables control over buffer resistivity and breakdown voltage, providing a practical route to high-voltage, low-leakage GaN buffers [30], [78], [81], [82]. Beyond chemical compensation, several epitaxial buffer designs have been developed to mitigate stress and enhance breakdown (Fig. 2.3). These include graded AlGaIn buffers that gradually transition lattice parameters between substrate and channel, GaN/AlN - GaN/AlGaIn superlattices that distribute mechanical strain, and low-temperature (LT) GaN layers or AlN insertions for reduced dislocation and stress relaxation [69], [78], [83]. For GaN-on-Si, AlN nucleation layers are essential to prevent Ga-Si reactions at high temperature and to ensure smooth, crack-free morphology [84]–[86].

Despite their crucial role, buffer layers are also a major source of degradation and reliability issues in GaN HEMTs. Deep acceptor-like traps in the buffer can capture electrons under high field, leading to vertical leakage, dynamic R_{on} increase, and current collapse during switching [75], [87]. Under long-term stress (e.g., HTRB or off-state operation), these traps can induce permanent threshold shifts and drain

current degradation, highlighting the importance of accurate buffer design and trap characterization [88], [89].

Modeling note. In the present work, the buffer layer was modeled as a compensated GaN region containing deep acceptor traps (C- or Fe-related), defined by their energy level, density, and capture cross sections. The polarization discontinuity between the nucleation and buffer layers was partially compensated by introducing an acceptor-like interface trap, which partially balances the interfacial charge. Out of polarization effects, included throughout the device according to material parameters and strain-dependent constants, no other explicit strain or dislocation modeling was implemented.

A recent technological trend in GaN HEMTs is the development of *buffer-less* structures, where the conventional compensated GaN buffer is omitted to minimize thermal resistance and trapping effects. Two main approaches have emerged. The first exploits low-dislocation native GaN substrates, enabling homoepitaxial growth with negligible lattice mismatch and eliminating deep acceptor traps associated with p-type compensation layers [90]. The second, more recent approach demonstrates direct GaN growth on Si/SiC following only an AlN nucleation layer, using optimized MOVPE conditions to control stress and prevent cracking. In this case, threading dislocation densities comparable to conventional buffered GaN-on-Si structures are achieved, while the GaN-to-substrate thermal resistance is reduced by an order of magnitude, enhancing heat extraction and long-term reliability [91].

The absence of a semi-insulating buffer reduces charge trapping and vertical leakage paths, leading to improved dynamic behavior, lower current collapse, and enhanced threshold stability under high-voltage operation [92], [93]. Moreover, the simplified epitaxial stack enables more accurate electric-field control and improved thermal management. While buffer-less architectures are still constrained by substrate quality, wafer size, and mechanical stress control, they represent a promising pathway toward realizing the intrinsic limits of GaN technology for next-generation power and RF devices.

2.2.3 Channel and 2DEG Confinement

The channel of an Al(Ga,Sc)N/GaN HEMT hosts the 2DEG that enables high current density and low on-resistance. Unlike conventional semiconductors, where carriers are introduced by intentional doping, the 2DEG in III-nitride heterostructures originates from the discontinuity of spontaneous and piezoelectric polarization fields at the barrier/channel interface [15], [17]. The resulting fixed polarization charge induces a sheet of mobile electrons on the GaN side of the interface, confined within a triangular quantum well typically 2–4 nm below the surface [14], [16].

In AlGaIn/GaN heterostructures, n_s is typically in the range of $(0.2 - 2) \times 10^{13} \text{ cm}^{-2}$, depending on the Al mole fraction, barrier thickness, and residual strain [15], [16]. In emerging AlScN/GaN stacks, the increase in spontaneous polarization coefficients allow for a further increase in n_s up to $5 \times 10^{13} \text{ cm}^{-2}$, enabling stronger confinement and enhanced transconductance [94], [95], [96], [97], [98], [99], [41].

The quality of the 2DEG strongly depends on the channel thickness, unintentional doping, interface roughness, and barrier composition. Self-heating and carrier–phonon interactions limit electron velocity in the high-field regime, where velocity saturation ($v_{\text{sat}} \sim 2.5 \times 10^7 \text{ cm/s}$ for GaN) constrains the achievable current density [37]. Fluctuations in surface states can partially deplete the 2DEG near the access regions, thereby increasing access resistance [88]. Under high-field operation, trapping phenomena at the barrier/channel interface further contribute to dynamic R_{on} degradation and current-collapse effects [39].

Modeling note. In TCAD simulations, the channel was modeled according to the specific doping profile defined in the device design, while the 2DEG was reproduced through the piezoelectric polarization model enabled at the heterojunctions. The resulting 2DEG density was verified through polarization charge balance, including donor-type traps at the passivation interface with the cap or barrier layers, and compared against experimental Hall-effect measurements. Electron transport was described using a combination of models: the Masetti model for doping dependence, a calibrated Caughey–Thomas model for field-dependent mobility, and the Lombardi model for surface-scattering corrections. This combination ensured an accurate reproduction of both transfer and output characteristics.

2.2.4 Barrier Materials and Polarization Engineering

The barrier layer plays a central role in GaN HEMTs, as it determines the 2DEG density, confinement strength, and gate controllability. Its composition, thickness, and strain state define the balance between spontaneous and piezoelectric polarization, which sets the interfacial charge and, consequently, the sheet carrier concentration in the underlying GaN channel [15]–[17].

Conventional $\text{Al}_x\text{Ga}_{1-x}\text{N}$ barriers ($x = 0.20\text{--}0.30$) remain the technological baseline for GaN HEMTs, enabling strong polarization-induced confinement of the 2DEG. The 2DEG density at the AlGaIn/GaN interface results from the combined action of spontaneous and piezoelectric polarization, and depends critically on the alloy composition, strain, thickness, and doping level of the barrier [16], [98]. Increasing the Al mole fraction enhances the polarization discontinuity and thus the 2DEG sheet density, but at the expense of larger tensile strain and increased lattice mismatch. When the Al content exceeds about 35–40%, partial strain relaxation and dislocation

formation occur, limiting the maximum achievable polarization charge and degrading interface quality [16], [30], [43].

Optimized $\text{Al}_x\text{Ga}_{1-x}\text{N}$ barriers typically have thicknesses of 15–25 nm and Al compositions between 0.20 and 0.35, providing a balance between polarization charge and mechanical stability. The resulting sheet carrier densities generally range between 8×10^{12} and $1.5 \times 10^{13} \text{ cm}^{-2}$, consistent with self-consistent Poisson–Schrödinger simulations [16]. However, deviations from the ideal 2DEG behavior may arise from dislocation-induced traps, interface roughness, and surface states, which can scatter electrons or locally deplete the 2DEG [16]. The density of threading dislocations (10^8 – 10^9 cm^{-2}) can introduce charged line defects acting as electron traps, thereby reducing the sheet carrier density by up to several 10^{11} cm^{-2} . In addition, non-abrupt interfaces or polarity inversion domains may lead to partial cancellation of polarization fields, decreasing the effective 2DEG concentration.

Surface Fermi-level pinning and associated band bending at the AlGaN surface further modulate the carrier distribution in the barrier, potentially affecting gate control and leakage [17]. To mitigate these effects, barrier composition and thickness must be carefully optimized in conjunction with cap and passivation layers to ensure uniform polarization charge, high mobility, and long-term electrical reliability under high-field operation [30], [43].

$\text{In}_{0.17}\text{Al}_{0.83}\text{N}$ is nearly lattice-matched to GaN, allowing a high polarization field without introducing significant tensile stress [100], [101]. Such heterostructures can achieve high 2DEG densities ($> 2 \times 10^{13} \text{ cm}^{-2}$) with excellent mobility and thermal stability [98], [102]. However, the growth of thick InAlN layers is intrinsically prone to morphological degradation, even in the absence of threading dislocations. During MOVPE, kinetic roughening leads to the formation of surface hillocks and V-defects once a critical thickness is reached. These V-defects promote local compositional variations due to differential indium incorporation on concave and convex facets, resulting in In-rich and In-poor regions and ultimately in phase separation within the layer [100]. Such mechanisms introduce interface roughness and alloy disorder, limiting reproducibility and reliability in large-area devices.

Introducing scandium into AlN yields $\text{Al}_{1-x}\text{Sc}_x\text{N}$, a material with extremely high spontaneous and piezoelectric polarization, and a tunable lattice constant. First-principles calculations and experimental studies have shown that pseudomorphic $\text{Al}_{1-x}\text{Sc}_x\text{N}/\text{GaN}$ heterostructures with x between 0.15 and 0.25 exhibit polarization-induced interface charges exceeding those of AlGaN/GaN by more than a factor of two, resulting in sheet carrier densities above $5 \times 10^{13} \text{ cm}^{-2}$ and correspondingly reduced channel resistivity [98]. The lattice-matched composition near $x = 0.20$ allows high 2DEG density and transconductance while mitigating strain compared to

AlN barriers.

Recent advances in metal–organic chemical vapor deposition (MOCVD) have enabled the growth of high-quality AlScN/GaN heterostructures [41], [42], [103]. Optimized growth conditions at 900–1000 °C yield barriers with Sc contents of 10–15%, sheet resistances as low as 170–200 Ω/sq , and mobilities exceeding 1000 cm^2/Vs . The structural and electrical quality is highly sensitive to the Sc precursor purity, interface abruptness, and growth temperature. Low growth temperatures minimize Al–Ga interdiffusion and suppress the formation of graded AlGa_xN interlayers, leading to improved 2DEG confinement and homogeneous electrical performance across 4-inch wafers [40], [104].

At millimeter-wave frequencies, AlScN/GaN HEMTs demonstrate power densities exceeding 8 W/mm at 30 GHz and power-added efficiencies approaching 50%, outperforming equivalent AlGa_xN/GaN devices [103], [104]. However, AlScN remains technologically challenging due to phase segregation, Sc-rich surface termination, and the high reactivity of Sc with oxygen. These effects can induce interface roughness, charge trapping, and potential reliability degradation under high electric field stress [103]. To prevent oxidation and maintain interface integrity, thin AlN interlayers and GaN caps of controlled thickness are employed to stabilize the surface and avoid the formation of parasitic conductive channels [103].

Despite these challenges, AlScN/GaN heterostructures represent a key pathway toward next-generation GaN HEMTs, combining high sheet charge density, superior polarization control, and scalable MOCVD growth for both high-frequency and high-power applications.

AlN/GaN heterostructures represent an extreme case of polarization-induced 2DEG formation, offering one of the highest spontaneous and piezoelectric polarization discontinuity among III-nitride systems. The absence of alloy disorder and the wide AlN bandgap provide excellent confinement and gate robustness, enabling 2DEG densities up to $(2\text{--}4) \times 10^{13} \text{ cm}^{-2}$ with mobilities of 1000–1800 cm^2/Vs [16], [98].

Recent advances in epitaxial growth have demonstrated high-performance AlN/GaN HEMTs featuring thick AlN barriers ($\sim 7 \text{ nm}$) and regrown n^+ -Ga_xN ohmic contacts, achieving high current density (1.6 A/mm) and power efficiency at low operating voltages [105]. Similar MIS-HEMT architectures on 6-inch Si substrates have shown record power-added efficiency in the K- and Ka-band, confirming the potential of AlN as a high-polarization barrier for next-generation RF applications [106].

At the device level, optimized ohmic processes, such as selective etching and regrown n^+ -Ga_xN, enable contact resistances as low as 0.25 $\Omega \cdot \text{mm}$ and interface resistances approaching the quantum conductance limit, while preserving the *in situ* SiN passivation [107]. From a thermal standpoint, double-heterostructures AlN/GaN/AlN

offer superior carrier confinement and breakdown voltage, with optimized AlN buffer thicknesses ($\sim 2 \mu\text{m}$ on 6H-SiC or $\sim 0.7 \mu\text{m}$ on diamond) reducing channel temperature rise by up to 50% compared to AlGaIn/GaN on SiC [108].

Although the large polarization fields in AlN/GaN enhance 2DEG density and transconductance, they also demand precise control of interface abruptness, surface states, and strain to ensure stability and reliability. Proper epitaxial design and passivation are therefore essential to exploit the intrinsic potential of AlN/GaN for compact, low-voltage, and high-frequency GaN HEMTs.

Modeling note. In TCAD simulations, polarization effects are implemented through the spontaneous and piezoelectric constants of each material, combined with the local strain tensor at the heterointerfaces. For AlScN, the elastic constants and strain model must be carefully considered due to variation of the crystallographic structure between AlN and ScN [109]. Therefore, it is good practice to directly adopt the material parameters corresponding to the specific Sc mole fraction to ensure an accurate representation of the polarization-induced charge and n_s . When calibrating against experimental data, both polarization-induced and interface-trap charges should be adjusted to reproduce the measured threshold voltage and 2DEG density.

2.2.5 Cap and Passivation Layers

Surface and interface engineering is critical in GaN HEMTs because the large bound polarization charge ($\sim 10^{13} \text{ cm}^{-2}$) at nitride surfaces/interfaces requires compensation, and a poorly controlled compensation mechanism promotes trap-assisted phenomena, gate leakage, and current collapse [110]. Cap and passivation layers stabilize the surface potential, screen polarization fields, and mitigate dispersion by suppressing defect-mediated charging near the access and gate-drain regions.

Silicon nitride (SiN_x) and silicon dioxide (SiO_2) are the most widely used dielectrics for both channel passivation and (in MIS-HEMTs) gate insulation, owing to their maturity and process flexibility. SiN_x often offers a favorable trade-off between dielectric constant and bandgap, is less prone to oxidize the III-N surface during deposition, and can passivate N-vacancy-related defects; in many reports it reduces leakage and current collapse as effectively as atomic layer deposition (ALD) SiO_2 . Al_2O_3 , HfO_2 , and AlN have also been investigated as gate dielectrics and passivants to suppress tunneling and stabilize the surface, with performance that depends sensitively on pre-clean, plasma pretreatments, deposition chemistry, and post-deposition anneals [110]. Practically, stacking (e.g., Al_2O_3 /in-situ SiN) combines large band offsets with robust interface chemistry and has proven effective for high-efficiency K/Ka-band MIS-HEMTs on Si [106].

A high density of surface/interface electronic states (order of 10^{13} cm^{-2}) is inherent to III-N surfaces; only a small fraction (e.g., $\sim 10^{10} \text{ cm}^{-2}$) needs to be active traps to impact dispersion and leakage. Their nature and occupancy are strongly affected by surface preparation and dielectric deposition (oxygen coverage, native oxide, carbon contamination, vacancy complexes, plasma-induced defects), and by subsequent thermal treatments. Cleaning sequences (e.g., NH_4OH , HF/HCl , UV/O_3) and in-situ plasmas (N_2 , NH_3) can reduce oxides and adjust terminations, but outcomes are process-specific and device-function dependent (gate dielectric vs. channel passivation) [110].

Under high field, donor-like surface/interface states can be filled, forming a *virtual gate* that expands depletion in the gate–drain access region, causing current collapse and dynamic R_{on} degradation; relaxation transients reflect both a discrete peak in the trap distribution and a broader continuum of surface states characterized by different time constants [110]–[112]. Proper passivation lowers the effective density of active states and reduces surface charging, while field plates further reshape the peak field and lower the trapping rate in the access region [113], [114].

Modeling note. In TCAD, the barrier/passivation interface is represented by donor-like surface states (energy distribution, density, capture/emission parameters) whose occupancy is solved self-consistently with the device electrostatics. In this work, the parameters are analysed in depth and calibrated to pulsed I-V and current-collapse measurements; field plates are included as metal boundaries that shape the electric field and the dynamic trapping profile (Chapters 5, 6) [30], [43], [88], [89], [110], [115].

2.2.6 Gate Stack and Contact Technologies

Schottky-gate HEMTs enable low capacitance and high cutoff frequency (f_T), but are susceptible to gate leakage via multiple mechanisms (thermionic emission, thermionic-field emission, trap-assisted tunneling, Fowler–Nordheim, Poole-Frenkel), with the dominant path depending on temperature, bias, and defects and geometry. MIS-HEMTs insert a dielectric (e.g., Al_2O_3 , HfO_2 , SiN_x) to increase the barrier for tunneling and to decouple the gate from the defect-rich surface, reducing leakage by several orders of magnitude and improving stability provided that the interface trap density is controlled [116]–[123]. Stacked dielectrics (e.g., Al_2O_3 /in-situ SiN) have shown state-of-the-art Power Added Efficiency (PAE) at 18–29 GHz on 6-inch Si, indicating good interface quality and robustness under RF stress [106]. The choice of dielectric, pretreatment, and anneal must balance band offsets, dielectric constant, interface chemistry, and stress to minimize trap-assisted processes and hysteresis [110].

Conventional alloyed metallizations for ohmic contacts (e.g., Ti/Al-based stacks) remain common, but aggressively scaled nodes and ultrathin barriers benefit from *regrown* n^+ -GaN ohmics, which can achieve very low contact resistances while preserving passivation integrity. Selective-etch plus regrowth flows have demonstrated $R_C \approx 0.25 \, \Omega \cdot \text{mm}$ and a 3D–2D interface resistance approaching the quantum conductance limit ($\sim 0.06 \, \Omega \cdot \text{mm}$), without damaging in-situ SiN or the AlN surface, thereby enabling tighter source–drain spacing and improved RF performance [107]. Gate metallization directly on in-situ SiN (for Schottky or MIS gates) avoids exposing reactive nitride surfaces and helps maintain reproducibility in scaled processes.

Gate leakage and dispersion are tightly connected to the near-surface defect spectrum and polarization-driven band bending; stress can activate additional leakage paths (e.g., via enhanced fields at the gate edge) and modify trap populations [110], [124]. Process choices that reduce native oxides, control oxygen/carbon incorporation, and passivate vacancies (e.g., Al_2O_3 with N_2 plasma pretreatments, or optimized SiN_x) are effective routes to lower interface-state density and stabilize threshold and transconductance under operation [30], [43], [110].

Modeling note. Gate stacks were modeled using Schottky or MIS boundary conditions, with the barrier height determined by the metal work function adopted in each device, or calibrated against experimental data to reproduce gate leakage, threshold voltage, and output characteristics [88], [89], [115]. Depending on the technology under study, the gate contact was placed on the p-GaN layer (Chapter 4), on the AlGaN cap (Chapter 5), or directly on the AlScN barrier (Chapter 6). Gate leakage mechanisms were described through thermionic emission (TE) and nonlocal tunneling, employing a nonlocal mesh to resolve carrier transport across the potential barrier with calibrated parameters such as the relative effective tunneling mass. Trap-assisted tunneling (TAT) was not applied directly at the Schottky interface but was instead introduced within the AlGaN barrier region for the p-GaN gate device to capture leakage effects [115], [125]. Source and drain contacts were represented by low work-function Schottky boundaries with a reduced relative effective tunneling mass (on the order of 10^{-3}) and adjacent n-type doped regions to emulate ohmic behavior [88], [126].

2.3 Device-Level Performance and Figures of Merit

The performance of GaN-based HEMTs is governed by the balance between polarization induced charge, carrier transport, electric field distribution, and thermal management. Several figures of merit (FoMs) are commonly adopted to benchmark

material and device performance, linking the intrinsic semiconductor properties to the extrinsic device architecture and application domain.

Two FoMs are widely recognized in the literature for assessing the intrinsic capability of a semiconductor for high-speed and high-power operation: the *Johnson* and *Baliga* figures of merit [39], [127], [128]. The *Johnson FoM* quantifies the trade-off between breakdown voltage and maximum frequency of operation:

$$\text{FoM}_J = f_T \cdot V_{DS,max} = \frac{E_{\text{crit}} v_{\text{sat}}}{2\pi}, \quad (2.3)$$

where E_{crit} is the critical electric field and v_{sat} the electron saturation velocity, while the cutoff frequency f_T reads:

$$f_T = \frac{g_m}{2\pi C_G} \quad (2.4)$$

where g_m is the transconductance and C_G is the gate capacitance.

The *Baliga FoM* instead measures the material capability to minimize conduction losses in power switching devices:

$$\text{FoM}_B = \mu \varepsilon E_{\text{crit}}^3, \quad (2.5)$$

where ε is the permittivity. These quantities highlight the advantage of wide-bandgap semiconductors, where high E_{crit} and v_{sat} translate into superior high-voltage and high-frequency performance. For GaN, the Johnson FoM is roughly one order of magnitude higher than Si and GaAs, and lower than AlN and diamond due to the much higher E_{crit} (Tab.2.1) [39].

At the device scale, performance is quantified by figures of merit directly linked to the channel and geometry, including the n_s , mobility $\mu_{2\text{DEG}}$, transconductance g_m , maximum drain current $I_{D,max}$, specific on-resistance $R_{\text{on,sp}}$, and the frequency parameters f_T and the maximum oscillation frequency f_{max} (see Fig. 2.4) [98], [106], [129]. Typical AlGaIn/GaN HEMTs exhibit n_s in the range $(8\text{--}20) \times 10^{12} \text{ cm}^{-2}$ and $\mu_{2\text{DEG}}$ between 1200 and 2000 cm^2/Vs , depending on the barrier composition and interface quality. Recent devices on SiC and Si substrates have achieved f_T above 100 GHz and f_{max} approaching 250 GHz, with Johnson FoMs exceeding $6 \times 10^{12} \text{ V/s}$ (as $20 \times 10^{12} \text{ V/s}$) and Baliga FoMs surpassing those of SiC by nearly an order of magnitude [127], [129]. Power-switching HEMTs routinely demonstrate breakdown voltages between 600 and 1200 V and power efficiencies above 90%, consolidating GaN position as a leading wide-bandgap technology for both RF and power domains.

Table 2.4 compares the normalized Johnson and Baliga figures of merit among major semiconductors. GaN emerges as the optimal trade-off between breakdown

Table 2.4: Normalized Johnson and Baliga figures of merit for major semiconductor materials, highlighting GaN balance between high-frequency and high-power performance [39], [127].

Material	Johnson FoM (norm.)	Baliga FoM (norm.)	Main application domain
Si	0.04	0.02	Low-voltage, mature CMOS
GaAs	0.05	0.03	RF, optoelectronics
SiC (4H)	0.56	0.50	Power switching (600–1700 V)
GaN	1.00	1.00	RF and power (20–1200 V)
AlN	2.7	10.0	Research, ultra-wide bandgap
Diamond	2.5	20.0	Theoretical limit

strength and high-frequency capability: while SiC offers comparable voltage ratings, GaN provides superior speed and polarization control. AlN and diamond exhibit significantly higher FoMs, but their technological maturity, growth complexity, and cost currently limit practical implementation. Hence, GaN remains the most balanced and scalable wide-bandgap semiconductor for high-efficiency RF and power devices.

Each FoM reflects the interplay among multiple design parameters:

- *Barrier thickness and composition* set the 2DEG charge and threshold voltage through polarization and strain.
- *Buffer design* controls leakage and dynamic R_{on} through deep-level traps.
- *Gate stack and passivation* determine leakage pathways, charge stability, and field distribution.
- *Thermal management* governs the maximum achievable current density and long-term reliability.

Optimization therefore requires trade-offs between high-frequency gain, power density, and reliability. Increasing Al or Sc content enhances n_s and f_T , but may increase strain, dislocation density, and gate leakage. Conversely, thicker buffers improve isolation and breakdown but can worsen thermal dissipation and dynamic resistance recovery.

Modeling note. Calibration of TCAD device models follows a hierarchical strategy: (I) Electrostatics and polarization: adjust spontaneous/piezoelectric constants and interface charges to reproduce n_s and V_{th} ; (II) Transport calibration: tune mobility and velocity-saturation models to match g_m and I_D ; (III) Dynamic behavior: include traps or degradation models to capture pulsed I-V gate and drain lag; (IV) Stress and reliability: extend with temperature- and field-dependent degradation models to reproduce stress at high temperature and/or high bias trends.

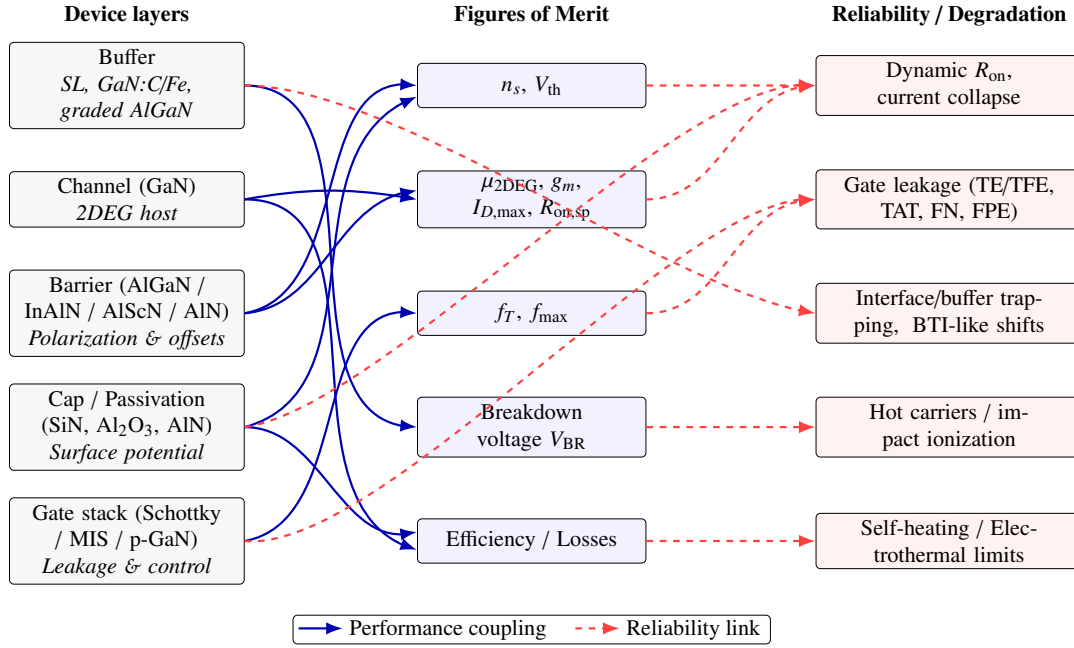


Figure 2.4: Interdependence between GaN HEMT layer design (left), device-level figures of merit (center), and reliability phenomena (right). Polarization and interface control set n_s and V_{th} ; transport and parasitics determine $g_m, I_{D,max}, R_{on,sp}, f_T, f_{max}$; field shaping and vertical isolation impact V_{BR} and dynamic behavior.

This approach ensures a consistent transition from static to dynamic and stress simulations, forming the foundation for the reliability-oriented TCAD framework discussed in Chapter 3.

2.4 Reliability Landscape and Modeling Motivation

The reliability of GaN-based high-electron-mobility transistors (HEMTs) is governed by several physical mechanisms that endanger and limit long-term stability. The most relevant are: (i) surface and interface trapping, responsible for current collapse and dynamic R_{on} increase; (ii) buffer trapping, leading to dynamic R_{on} increase and threshold voltage drift under prolonged reverse bias (HTRB/H³TRB); (iii) gate degradation in Schottky-, MIS-, and p-GaN-gate configurations leading to off-state leakage increase (contact and barrier deterioration); and (iv) hot-carrier and impact-ionization phenomena in the high-field gate-drain access region [39]. A comprehensive overview of these mechanisms, including the taxonomy of defect states and their interaction with the device architecture, is presented in [130].

Understanding and predicting these degradation modes requires bridging the gap between experimental observables and their underlying physics. *TCAD bridges this*

gap, enabling the inclusion of polarization, traps, tunneling, and electrothermal effects within a self-consistent framework. When properly calibrated against experiments, TCAD simulations allow for the deconvolution of overlapping degradation processes and for quantitative prediction of long-term trends, which are essential for technology optimization and lifetime assessment.

2.4.1 Modeling of the Gate in p-GaN HEMTs

The introduction of a p-GaN gate enables normally-off operation but also introduces new reliability concerns, primarily related to gate leakage and breakdown. In [131], the gate conduction mechanisms in p-GaN/AlGaIn/GaN HEMTs were analyzed through temperature-dependent measurements and physical modeling. Distinct conduction regimes were identified: Poole–Frenkel emission (PFE) in reverse bias, thermionic emission (TE) at low positive bias, and thermally assisted tunneling (TAT) at higher gate voltages. Process-dependent improvements of the metal/p-GaN interface were shown to extend device lifetime and mitigate field-enhanced leakage.

In [125], dynamic threshold voltage hysteresis in p-GaN HEMTs was reproduced through Sentaurus TCAD simulations. The study demonstrated that charge and discharge dynamics in the floating p-GaN layer, rather than barrier traps, dominate the transient behavior under fast sweeping conditions. In [132], the reverse-biased gate leakage in AlGaIn/GaN HEMTs was analyzed, showing that Poole–Frenkel and trap-assisted tunneling (TAT) through dislocation-related states govern the leakage path at the metal–semiconductor interface. Together, these studies establish a consistent modeling framework for gate reliability, capturing the transition between thermionic, tunneling, and field-enhanced conduction mechanisms that define the degradation landscape of p-GaN HEMTs.

2.4.2 Modeling of Pulsed I–V and Dynamic Trapping Effects

Pulsed I–V measurements are fundamental to quantifying trapping phenomena in GaN HEMTs, as they separate self-heating from charge-trapping effects through appropriate timing control. In [133], the principles of pulsed measurement waveforms were defined, highlighting the importance of quiescent bias and pulse width in controlling trap occupancy. Subsequent work [134] introduced the isotrap method, enabling controlled pre-pulse conditions for reproducible trapping states. In [135], fast-pulsed characterization was implemented within lifestest systems, allowing the in-situ monitoring of trap dynamics during long-term device operation.

A comprehensive review of trapping mechanisms and suppression strategies was reported in [130], where surface and buffer traps were correlated with dynamic degradation and current collapse. In [39], experimental and physical models were compared, linking drain current transients, pulsed I–V, and electroluminescence signatures to distinct defect families. Advanced studies also demonstrated that interface engineering using SiN_x or AlN passivation [136] mitigates dynamic degradation by modifying polarization-induced surface fields and reducing interface trap density. Through proper TCAD calibration, both static and dynamic I–V characteristics can be reproduced, bridging experimental pulsed measurements with the underlying physical models of charge trapping.

2.4.3 Modeling of HTRB Step-Stress and Long-Term Reliability

HTRB tests are used to accelerate degradation mechanisms occurring under off-state stress, enabling the extraction of defect generation rates and the evaluation of buffer and surface stability. In [137], step-stress HTRB measurements were shown to separate thermally and electrically activated degradation processes, revealing two dominant regimes: below 150°C , buffer-related trapping dominates, while above 150°C , surface charging and the virtual gate effect induce a positive V_{TH} shift. In [138], the evolution of drain and gate currents under HTRB was correlated with the generation of acceptor-like traps in the barrier/buffer, localized near the gate edge on the drain side. These findings were consistent with TCAD predictions identifying deep acceptor states around $E_t = E_C - (0.5 - 0.9) \text{ eV}$ responsible for drain current reduction and knee-voltage smoothing. More recent analyses of p-GaN gate HEMTs [139] revealed temperature-dependent leakage and threshold voltage drifts consistent with interface degradation and hole injection near the metal/p-GaN junction. Early long-term studies [140] confirmed that, even at moderate voltages, electric field concentration at the drain-side gate edge represents the main reliability bottleneck, linking field stress, trapping, and thermally activated degradation.

Overall, these results converge toward a unified interpretation of HTRB degradation as the combined action of surface and buffer trapping, field-induced defect creation, and charge redistribution, which can be quantitatively analyzed through physics-based TCAD models.

2.4.4 Modeling of Emerging Barrier Materials: AlScN/GaN

Recent advances in barrier engineering have introduced AlScN as a promising alternative to AlGaN, owing to its stronger spontaneous and piezoelectric polarization, which increases 2DEG density and transconductance. While these properties offer

improved RF and power performance, the reliability of AlScN/GaN HEMTs remains largely unexplored. Preliminary modeling studies suggest stronger field localization and higher sensitivity to interface trap states, emphasizing the need for optimized barrier composition and passivation schemes. In this thesis, TCAD modeling will be extended to AlScN barriers to assess their impact on charge trapping, current stability, and degradation under electrical stress, enabling a direct comparison with AlGaN-based counterparts.

2.5 Summary

This section summarized the main reliability challenges of GaN HEMTs, linking material properties, device architecture, and degradation mechanisms such as trapping, gate leakage, and stress-induced instabilities. The discussion outlined how calibrated TCAD simulations provide a physics-based framework to separate and quantify these effects, bridging experimental observations and microscopic models. Chapter 3 builds on this foundation to discuss the challenges of modeling polarization, traps, and convergence in commercial TCAD tools, and the strategies adopted in this work to achieve reliable calibration against DC, pulsed, and stress data.

Chapter 3

Challenges in GaN Device Modeling Using Commercial TCAD Tools

3.1 Overview

Technology Computer-Aided Design (TCAD) plays a central role in modern semiconductor research and development, providing a quantitative framework to analyze charge transport, electrostatics, and reliability phenomena prior to fabrication. In the context of WBG semiconductors such as GaN, TCAD enables predictive evaluation of device performance and degradation under realistic electrical and thermal stress conditions [141], [142], [143].

Although TCAD has reached a high level of maturity for conventional Si-based technologies, its application to III–nitride materials remains challenging. These challenges arise from both physical and numerical aspects: the very low intrinsic carrier density resulting from the wide bandgap of the material, the strong polarization fields inherent to polar materials, the high density of native and process-induced defects, and the numerical difficulties arising from steep potential gradients and material discontinuities [144], [145], [146].

This chapter reviews these issues and outlines the modeling strategies typically employed to overcome them in commercial simulation environments. It provides the methodological foundation for the device-level modeling work presented in Chapters 4–6, based on the physical principles discussed in Chapter 1 and the material properties introduced in Chapter 2.

3.2 Introduction

In the rapidly evolving semiconductor industry, the ability to predict and optimize device performance before fabrication is crucial. Technology Computer-Aided Design (TCAD), a branch of Electronic Design Automation (EDA), refers to the use of simulations to develop and optimize semiconductor processes and devices [141], [142]. By employing TCAD tools, engineers can model both the fabrication process and the physical electrical behavior of devices, enabling efficient design iterations and reducing dependence on costly experimental prototypes [147], [148]. TCAD simulations are generally categorized into two main domains.

The first domain of process simulation, models the various steps involved in semiconductor fabrication, such as oxidation, ion implantation, and diffusion, as representative examples. Accurate process simulation ensures that the desired device structures and doping profiles are achieved, which are critical for device performance [149].

The second domain of device simulation, focuses on predicting the behavior of semiconductor devices under different operating conditions. By solving the fundamental semiconductor physics equations, device simulation provides insights into current-voltage characteristics, charge-voltage relationships, time-dependent transients, and other performance metrics [150].

The integration of these simulations allows for a comprehensive understanding of how process variations impact device performance, enabling the optimization of both fabrication processes and device architectures [146], [151]. As semiconductor technologies continue to advance, TCAD remains an indispensable tool for innovation, supporting the development of next-generation electronic devices [143], [152], [153], [154]. The following section discusses the fundamental principles underlying device-level TCAD simulations, which form the methodological core of this work.

3.3 Principles of TCAD Modeling

Technology Computer-Aided Design (TCAD) relies on a combination of numerical methods, such as the Finite-Element Method (FEM), Finite-Volume Method (FVM), and, more recently, Artificial Neural Networks (ANN), to solve the complex equations involved in process and device simulations. In the present work, the focus is placed on device-level simulations.

In the case of FEM, the device domain is discretized into smaller elements, allowing for the numerical solution of the partial differential equations that govern

semiconductor behavior. This technique is essential for accurately modeling devices with intricate geometries.

To construct such a virtual representation, the real semiconductor device (e.g., a transistor) is mapped onto a nonuniform *grid* or *mesh* of nodes. This implies that any simulated device is an approximation of the real structure. The device geometry defines the spatial regions of the structure, including boundaries, material types, and electrical contacts, and specifies the locations of all discrete nodes and their connectivity.

Depending on the required level of physical accuracy, TCAD tools offer different transport formulations, from the standard drift–diffusion approach (Chapter 1), suitable for most GaN HEMT simulations, to thermodynamic, hydrodynamic, and full-band MC solvers that account for energy transport and non-equilibrium carrier dynamics under high electric fields [2], [4], [150].

Prominent commercial TCAD tools implementing these techniques include *Synopsys Sentaurus* and *Silvaco Victory*.

Modern TCAD tools integrate a wide range of physical models that describe carrier transport, recombination, tunneling, and thermal effects [155].

For WBG materials, device modeling presents additional challenges compared to silicon. The relatively low intrinsic carrier concentrations and strong electric fields can lead to numerical instabilities, requiring tighter convergence criteria and finer spatial discretization [156]. Moreover, key physical parameters such as carrier mobility, trap densities, and polarization charges are not yet standardized across different GaN and SiC technologies, making calibration against experimental data essential for accurate simulation results.

In this work, the TCAD models were specifically adjusted and benchmarked on measured GaN HEMT data to ensure physical consistency and predictive capability, with particular attention devoted to mobility degradation, polarization-induced interface charges, and trap-assisted conduction, which will be discussed in detail in the following sections.

3.4 Applications in Device Design and Reliability

Technology Computer-Aided Design (TCAD) plays a pivotal role in both the development and reliability assessment of modern semiconductor devices, including Metal–Oxide–Semiconductor Field–Effect Transistors (MOSFETs), HEMTs, power devices, memories, FinFETs, and emerging nanoscale architectures such as nanowires (NW), nanosheets (NS), and Gate–All–Around (GAA) transistors. By enabling detailed physical simulations, TCAD allows engineers to predict device behavior under

various operating and stress conditions, supporting design optimization and early identification of potential reliability issues.

In reliability modeling, TCAD is particularly effective in elucidating degradation mechanisms such as hot-carrier effects, bias-induced instabilities, and charge trapping, which limit the long-term performance of GaN-based transistors. A notable example is the study presented in [157], where TCAD simulations were combined with Electron Beam Induced Current measurements to reveal the presence of a parasitic sidewall transistor in p-GaN gate HEMTs. The simulations demonstrated that a conductive sidewall path could form at gate biases corresponding to experimental leakage activation, explaining the observed degradation and lifetime reduction. Based on this insight, process modifications were proposed and experimentally validated, resulting in a significant improvement in gate reliability without compromising device performance. This work exemplifies how TCAD-based physical analysis can directly guide technological optimization by linking microscopic degradation mechanisms to macroscopic reliability outcomes.

A further example of TCAD application to GaN reliability and optimization is provided in [158], where the correlation between drain and gate leakage currents in AlGaIn/GaN HEMTs was analyzed through calibrated simulations. The study identified the buffer trap concentration as a critical factor influencing both the subthreshold drain current and the gate current behavior. By systematically varying the trap parameters, the authors demonstrated that tuning the buffer epitaxy can mitigate threshold voltage shifts and improve the overall device stability, providing a clear link between epitaxial quality, trapping effects, and electrical performance.

Another representative study is presented in [159], which investigated the impact of drain field-plate (FP) geometry on semi-ON degradation in AlGaIn/GaN HEMTs. Through a combination of pulsed stress measurements and two-dimensional hydrodynamic TCAD simulations, the work revealed that longer field plates enhance hot-electron trapping at the passivation/AlGaIn interface near the drain edge. This localized trapping modifies the electric-field distribution and accelerates drain-current degradation, explaining the experimentally observed correlation between FP length and performance deterioration. Such studies highlight how TCAD can accurately capture field-dependent trapping mechanisms and provide quantitative guidance for optimizing device layout and reliability under high-power operation.

Together, these examples demonstrate how TCAD serves not only as a diagnostic tool for understanding degradation phenomena but also as a predictive framework for process refinement and structural optimization in GaN-based technologies. The following section discusses the models adopted in this work.

3.5 Adopted and Calibrated Physical Models in TCAD

The practical modeling of GaN HEMTs in commercial TCAD platforms relies on a combination of active models that require dedicated parameter tuning and validation to accurately reproduce experimental results.

As discussed in Section 3.3, TCAD tools support multiple semiconductor materials through predefined parameter libraries. Each material is characterized by a set of parameters, such as bandgap energy, dielectric constant, effective masses, mobility prefactors, polarization coefficients, and several other quantities related to the physical mechanisms described by the active models. Although common materials such as Si, GaAs, GaN, and SiC are already implemented, the introduction of novel materials, such as AlScN, requires the explicit definition of all relevant material parameters associated with the selected physical models. If these parameters are not specified, the simulator defaults to the standard silicon values, which lead to physically inconsistent or misleading results.

In this context, and as detailed in Chapter 6, the modeling of the AlScN barrier material includes specific material properties and datasets derived from theoretical calculations, experimental measurements, and dedicated calibration procedures.

The following subsections summarize the main physical models adopted throughout this work, along with the underlying physics and rationale behind their selection.

3.5.1 Generation–Recombination Models

Generation–recombination (G–R) processes describe the exchange of carriers between the conduction and valence bands through mechanisms that control carrier lifetime and steady-state densities. Their theoretical formulation, including the SRH, radiative, Auger, and tunneling-assisted components, has been discussed in Chapter 1. Here, only the models effectively adopted in the present work are summarized.

Carrier recombination through deep traps is modeled using the SRH formalism, with energy level, capture cross sections, and trap density as key adjustable parameters. For completeness, Auger recombination term is enabled but found negligible under the bias and temperature ranges investigated, due to the low carrier densities typical of GaN HEMTs.

Finally, nonlocal trap–assisted tunneling (TAT) is included where required to reproduce field–enhanced gate and barrier leakage, as detailed in Subsection 3.5.4. Overall, the inclusion of these G–R models was essential to capture leakage, breakdown, and transient recovery phenomena in GaN–based devices.

3.5.2 Trap and Defect Modeling

Traps are distributed throughout the AlGaIn/GaN HEMT structure. Some originate from imperfections introduced during the growth of nucleation and relaxation layers, while others form at interfaces between semiconductor layers, at the passivation surface, or at the channel interface of GaN "MOS" structures, where they can cause non-idealities in C–V characteristics. All these traps can significantly influence device behavior; however, their profiles, types, and properties depend strongly on the specific details of the fabrication technology.

Traps can also influence the low-field mobility (μ_{LF}) through Coulomb and phonon scattering mechanisms, particularly when located near the 2DEG or in the buffer region. In this work traps are treated as fixed charge centers, and their effect on mobility is included through doping-dependent mobility formulation or others dependent on the total doping N (such as Lombardi) using a specific keyword (see Subsection 3.5.5). Similar modeling strategies have been reported in literature for AlGaIn/GaN HEMTs, where trap-induced compensation and isolation are reproduced without explicitly coupling traps to mobility degradation [23], [125], [160].

Traps play a crucial role in device physics, as they contribute to doping compensation, enhance carrier recombination, and increase leakage through insulating regions. Several models, such as the SRH recombination model, implicitly account for traps without explicitly describing them. Commercial TCAD tools, however, allow the explicit definition of different trap types and energy distributions, providing several models for carrier capture and emission processes. Traps can be defined both in bulk regions and at interfaces.

The main trap types are: (i) *fixed charges*, which are always fully occupied; (ii) *acceptor traps*, which are neutral when unoccupied and negatively charged when fully occupied; and (iii) *donor traps*, which are neutral when empty and positively charged when filled.

Different energy distributions can be assigned to these traps, including: *level* (single-energy level), *uniform* (uniform distribution over an energy interval), *exponential* (exponentially decaying density), *Gaussian* (Gaussian energy distribution), and *table* (user-defined tabulated distribution). These distributions are referenced to a specific energy band (e.g., conduction or valence band), and the corresponding energy ranges are defined through appropriate keywords in the TCAD setup. Another essential parameter is the capture cross section, which determines the capture and emission times associated with each trap. Once these parameters are defined, the simulator computes the trap occupancy self-consistently, accounting for all capture and emission processes.

In III–N devices, interface traps often act as passivation centers that compensate the polarization-induced interface charge. For instance, the polarization discontinuity between the top AlGaN barrier and the passivation layer generates a large negative interface charge. Introducing donor-like trap levels at this interface allows the capture of holes, thereby neutralizing the excess negative charge. In this work, such traps play a key role in the calibration of experimental 2DEG density, gate leakage, and I–V characteristics [88], [89], [161], [162], [160], [163], [164]. These interface states are believed to contribute to the 2DEG population, as discussed in Chapter 2.

A similar compensation mechanism occurs at the nucleation–wafer interface, where acceptor-like trap levels capture electrons to balance the positive polarization charge. Throughout the epitaxial stack, bulk traps are also present, with material quality typically improving along the growth direction. Nonetheless, the nucleation, relaxation, and buffer layers often contain high concentrations of structural imperfections and deep levels.

In this work, bulk traps were introduced to model doping near the contacts and buffer isolation, using externally defined one-dimensional profiles with discrete energy levels along the device structure (see Chapters 4, 5, and 6). In Chapter 4, a uniform energy distribution of bulk traps in the barrier region was employed to reproduce the gate leakage current through the trap-assisted tunneling (TAT) mechanism [23], [125], [115].

Overall, the inclusion of both interface and bulk traps in the TCAD framework ensures a realistic representation of charge trapping phenomena, which are fundamental for understanding device degradation under electrical stress.

3.5.3 Nonlocal Tunneling Model

The nonlocal tunneling model implemented in Sentaurus Device provides a quantum–mechanical description of carrier transport through potential barriers at interfaces, contacts, and heterojunctions. Unlike local transport models, which assume that tunneling depends only on the field at a single point, the nonlocal formulation explicitly accounts for the entire energy–band profile between the points connected by tunneling, as described in Chapter 1, Section 1.4.3. This makes tunneling an inherently nonlocal process whose probability depends on the solution of the Poisson and carrier–transport equations throughout the tunneling path.

In Sentaurus Device, the band–edge profile and local potential variations are evaluated self-consistently to determine the tunneling probability along the path. To enable this, a dedicated *nonlocal mesh* must be defined for each region where tunneling occurs. A nonlocal mesh consists of a set of virtual lines, referred to as *nonlocal*

lines, that connect points inside the semiconductor to an adjacent interface or contact. The simulator automatically connects all vertices located within a specified distance (defined by the keyword `Length`) from the interface to the corresponding points on the interface, forming the backbone of the tunneling paths along which the WKB transmission probability is computed.

Each tunneling event corresponds to a connection between two points on a non-local line. Sentaurus distinguishes between tunneling to the conduction and valence bands at the lower end of the line. By default, all tunneling to the conduction band at the lower point originates from the conduction band at the upper point, corresponding to an electron component $j_C = j_{CC}$. Similarly, tunneling to the valence band at the lower point originates from the valence band at the upper point, giving a hole component $j_V = j_{VV}$.

In addition to these single-band processes, Sentaurus Device supports nonlocal band-to-band tunneling. When the option `Band2Band=Simple` is specified within the `eBarrierTunneling` statement, the total electron tunneling current includes both conduction-to-conduction and conduction-to-valence contributions, $j_C = j_{CC} + j_{CV}$. Analogously, when `Band2Band=Simple` is applied to `hBarrierTunneling`, the hole current includes both $j_V = j_{VV}$ and j_{VC} . For a more rigorous treatment, the `Band2Band=Full` option activates the dynamic nonlocal path formulation, which employs the direct tunneling model based on the Franz two-band dispersion relation (Eq. 1.44) for full consistency with the physical model described in Chapter 1.

This formulation allows Sentaurus Device to calculate the tunneling current by integrating the transmission probability along the entire nonlocal path, weighted by the carrier distribution and density of states. In this way, local field variations and band bending effects are correctly accounted for. The model is essential for describing carrier transport through thin barriers or Schottky interfaces in GaN-based HEMTs, where the high electric field induces significant quantum-mechanical tunneling components. Its inclusion enables the accurate reproduction of gate and junction leakage phenomena, particularly under reverse-bias conditions, as demonstrated in Chapters 4, 5, and 6.

3.5.4 Nonlocal Trap-Assisted Tunneling (nonlocal TAT)

The nonlocal trap-assisted tunneling (TAT) model in Sentaurus Device extends the standard Shockley-Read-Hall formalism by enabling traps to exchange carriers with spatially separated regions, such as interfaces or contacts, through tunneling. This model provides a physically consistent description of field-enhanced carrier leakage across insulating or wide-bandgap layers, particularly relevant in GaN-based

HEMTs, where deep traps in the barrier or dielectric can dominate the gate leakage under reverse bias conditions.

In this approach, traps are coupled to nearby interfaces and contacts by tunneling, using the nonlocal framework described in Section ???. Each trap is associated with a set of tunneling paths defined by nonlocal meshes (Section ???), which describe the possible quantum-mechanical connections between the trap and the interface (or contact) region. The coupling is specified in the TCAD input through the keywords `eBarrierTunneling` and `hBarrierTunneling`, corresponding to tunneling to the conduction and valence bands, respectively. Each statement includes the name of the nonlocal meshes to which the trap is connected via the `NonLocal` parameter. The same trap may be coupled to multiple interfaces by assigning several meshes, a requirement for modeling tunneling through barriers containing traps.

For example:

```
Traps(
  eNeutral Conc=1e15 FromMidBandGap EnergyMid=0.0 Level
  TrapVolume=1e-7
  eBarrierTunneling(NonLocal="NLM_top" NonLocal="NLM_bottom")
)
```

The model computes the tunneling-assisted capture rates for electrons and holes as the sum of two physical components: an *elastic* term, in which the carrier tunnels directly without energy exchange, and a *phonon-assisted inelastic* term, in which multiple phonons are emitted or absorbed during the transition. Both components depend on the ratio of the electronic wavefunctions at the trap site and at the interface, as obtained from the WKB tunneling probability described in Chapter 1, Section 1.4.3. The elastic capture rate is evaluated at the trap energy, while the inelastic term depends additionally on the phonon energy $\hbar\omega$, the Huang–Rhys factor S , and the Bose–Einstein occupation factor $f_B = [\exp(\hbar\omega/k_B T) - 1]^{-1}$, which governs the strength of the electron–phonon coupling. These parameters are specified through the keywords `PhononEnergy`, `HuangRhys`, and `alpha`, respectively.

Additional parameters include the tunneling mass m_t (which controls the exponential attenuation of the wavefunction through the barrier), the trap interaction volume `TrapVolume`, and the interface Richardson constant prefactor g_C . Together, these quantities determine the spatial extent and efficiency of the tunneling process. The emission rates are automatically derived from the capture rates through the principle of detailed balance, ensuring thermodynamic consistency.

The complete nonlocal TAT current is obtained by summing the trap-to-band tunneling contributions over all traps and energy levels. This formalism allows for the

realistic simulation of leakage mechanisms in GaN-based devices, including AlGaN barriers, where the measured gate current exhibits a clear exponential dependence on the applied electric field, typical of field-assisted tunneling. In this work, the nonlocal TAT model was calibrated and employed to reproduce the experimental gate leakage behavior of p-GaN and Al(Ga,Sc)N/GaN HEMTs, as discussed in Chapters 4, 5, and 6.

3.5.5 Carrier Mobility

Carrier mobility in III-nitride semiconductors is affected by multiple scattering mechanisms, including phonon, impurity, alloy disorder, and interface roughness scattering [2], [165]. In commercial TCAD tools, mobility is typically modeled through empirical or semi-empirical formulations.

The first adopted model is the *constant mobility model*, which is also active by default. This model accounts only for phonon scattering and is therefore dependent solely on the lattice temperature:

$$\mu_{\text{const}} = \mu_L \left(\frac{T}{300} \right)^{-\zeta} \quad (3.1)$$

where μ_L is the phonon-limited mobility. The default parameter for GaN of μ_L is modified based on Hall mobility measurements reported in [104], while the exponent ζ , which defines the temperature dependence, was kept at its default value (1).

The second model accounts for doping-dependent mobility degradation. In doped semiconductors, carrier scattering by charged impurity ions leads to a reduction in mobility (Chapter 1). Among the various models supported in Sentaurus, the Masetti model was adopted in this work [9], [166]:

$$\mu_{\text{dop}} = \mu_{\text{min1}} e^{-P_c/N} + \frac{\mu_{\text{const}} - \mu_{\text{min2}}}{1 + \left(\frac{N}{C_r} \right)^\alpha} - \frac{\mu_1}{1 + \left(\frac{C_s}{N} \right)^\beta} \quad (3.2)$$

where μ_{const} is taken from the constant mobility model, N denotes the doping concentration, and the other quantities are model parameters calibrated for GaN [166].

An additional model (Lombardi) accounts for surface acoustic phonon scattering (μ_{ac}) and surface roughness scattering (μ_{sr}). The same temperature dependence due to bulk phonons in Eq. (3.1) is implemented for the surface acoustic phonon contribution:

$$\mu_{ac} = \frac{B}{F_\perp} + \frac{C \cdot N^\lambda}{F_\perp^{1/3}} \left(\frac{T}{300} \right)^{-1} \quad (3.3)$$

and the surface roughness contribution is expressed as:

$$\mu_{sr}^{-1} = \frac{F_{\perp}^2}{\delta} + \frac{F_{\perp}^3}{\eta} \quad (3.4)$$

where $F_{\perp}$ is the normal electric field, while B , C , δ , and η are calibration parameters for each contribution. The parameter λ accounts for the screening effect induced by the doping concentration N . The surface-related contributions are combined with the Masetti bulk mobility (Eq. 3.2) through Matthiessen's rule to determine the total low-field mobility, which is subsequently included in the high-field model discussed below [18].

Under high-field conditions, carrier velocity saturation becomes dominant. In GaN, velocity saturation occurs around $v_{\text{sat}} \approx 2.5 \times 10^7$ cm/s, requiring field-dependent mobility models to avoid overestimation of the current density.

The model adopted in this work is the Caughey–Thomas formulation [167], [168]:

$$\mu_{\text{HF}} = \frac{\mu_{\text{LF}}}{\left[1 + \left(\frac{\mu_{\text{LF}} E}{v_{\text{sat}}}\right)^{\beta}\right]^{1/\beta}}, \quad (3.5)$$

where μ_{LF} is the low-field mobility, v_{sat} the saturation velocity, and β an empirical fitting factor. This model proved effective for the present simulations. Under such conditions, the mobility dependence on the electric field deviates from the ideal trend, mainly due to alloy scattering and polarized Coulomb field (PCF) scattering [166], [168]–[170]. A typical value of $v_{\text{sat}} \approx 1.3 \times 10^7$ cm/s is adopted [166], [169], consistent with the calibration values used in this work.

Regarding high-field transport, III–V (nitride) materials may exhibit *negative differential mobility* under strong driving fields. This effect originates from the transfer of electrons into higher-energy side valleys of the conduction band, where the effective mass is larger. The transferred-electron model available in the TCAD framework describes this phenomenon by accounting for the four lowest conduction-band valleys, following the analytical formulation in [171]. However, due to its higher computational complexity and convergence issues, this model is not employed in the present study.

The described models are essential for reproducing realistic transfer and output characteristics, particularly in power HEMTs with long gate-to-drain distances (see Chapters 5, 6).

3.5.6 Piezoelectric Polarization and Interface Charges

Polarization effects are a defining feature of III-nitride HEMTs. The combined contributions of spontaneous and piezoelectric polarization determine the fixed charge densities at heterointerfaces, which are responsible for the formation of the 2DEG in AlGaIn/GaN and AlScN/GaN structures [15], [98], [172], [173], [174].

In TCAD, these polarization-induced charges can be implemented either as fixed interface charge sheets or as continuous polarization gradients. Accurate modeling therefore requires a careful specification of the polarization constants, material composition, and strain state. Even small deviations in barrier composition or relaxation can lead to significant variations in 2DEG concentration and threshold voltage.

Recent first-principles studies have revisited the determination of spontaneous and piezoelectric polarization constants in wurtzite III-nitrides, highlighting the importance of a consistent choice of reference structure and of the proper formulation of piezoelectric coefficients [175]. While different implementations may lead to quantitative differences in the calculated polarization charge, these variations are generally small for the material compositions and strain conditions considered in this work. Accordingly, the present simulations adopt the default polarization parameters implemented in Sentaurus Device, which are consistent with the modern theory of polarization and with the revised formulations reported in the recent literature [98], [175]. Residual discrepancies between theoretical polarization constants and experimental observations are addressed through the polarization activation factor within the TCAD framework. This parameter is selectively applied only in the AlScN/GaN case to calibrate the effective polarization charge against experimental data, and is consistently used in the simulations presented in Chapter 6.

By default, in ternary systems, a linear mole-fraction dependence of the model parameters is assumed, where each parameter P is expressed as:

$$P(x) = x \cdot P(\text{M1}) + (1 - x) \cdot P(\text{M2}),$$

with M1 and M2 representing the binary materials corresponding to $x = 0$ and $x = 1$. This approach is valid for $\text{Al}_{0.31}\text{Ga}_{0.69}\text{N}$ (see Chapter 5); however, a more complex configuration is required for $\text{Al}_{0.95}\text{Sc}_{0.05}\text{N}$ (see Chapter 6) due to the crystallographic transition observed between AlN and ScN [15], [98], [109], [172], [173], [174]. Therefore, for the latter, parameters corresponding to the specific mole fraction are directly adopted.

The polarization model considers the c-axis component, corresponding to the z -axis in the normal growth direction, which is given by:

Material	P_z^{sp} [10^{-6}C/cm^2]	d_{31} [10^{-10}cm/V]	c_{11} [10^{11} Pa]	c_{12} [10^{11} Pa]	c_{13} [10^{11} Pa]	c_{33} [10^{11} Pa]
GaN	-3.4	-1.6	3.9	1.45	1.06	3.98

Table 3.1: Spontaneous polarization, piezoelectric and elastic constants for GaN adopted in this work within the strain-based polarization model. Default Sentaurus parameters are used [18].

$$[P_z] = P_z^{sp} + 2d_{31}\varepsilon_z \left(c_{11} + c_{12} - 2\frac{c_{13}^2}{c_{33}} \right), \quad (3.6)$$

where P_z^{sp} is the spontaneous polarization term, c_{ij} are the stiffness matrix coefficients, d_{31} is the piezoelectric coefficient, and ε_z is the mechanical strain in the z -direction. Based on the polarization vector $\mathbf{P}$, the piezoelectric charge density (see Chapter 1) is computed as:

$$q_{PE} = -\text{activation} \nabla \cdot \mathbf{P}, \quad (3.7)$$

where *activation* is a non-negative real calibration parameter (default value = 1). This factor allows adjustment of the net piezoelectric contribution, enabling calibration of the interface charge density to match experimental or simulation requirements. In this work, polarization effects are modeled using the strain-based formulation implemented in Sentaurus Device, where the piezoelectric charge density is computed according to Eq. (3.6). For GaN, the spontaneous polarization, piezoelectric, and elastic constants adopted in the simulations are reported in Table 3.1. Unless otherwise specified, the polarization activation parameter is set to its default value.

3.5.7 Thermionic Emission Model in TCAD Sentaurus

In *Synopsys Sentaurus Device*, the thermionic emission model implements the physical description of carrier transport across heterojunctions, following the formulation of [5] and the numerical validation of [176] seen in Chapter 1, subsection 1.1.4.

The model can be activated at a region or material interface by specifying the appropriate physics keyword. For electrons, `eThermionic`, for holes `hThermionic`, or both simultaneously `Thermionic`. These options are defined within the `Physics` section of the material/region interface. When activated, the model computes carrier and energy fluxes across the heterojunction according to Eqs. (1.13) and (1.15) or Eqs. (1.21) and (1.22). These formulations depend on the local temperature T_i , carrier density n_i or p_i , and effective mass m_i . The emission coefficients can be customized in the parameter file using the `ThermionicEmission` block, where the

parameters A, B, and C correspond to the scaling factor, barrier-shape coefficient, and energy-flux weighting, respectively. When Fermi–Dirac statistics are enabled, the revised formulation must be selected by setting $\text{Formula}=1$, otherwise, the Boltzmann-like model ($\text{Formula}=0$) is applied by default.

In GaN-based HEMTs, proper activation of the thermionic emission model is essential for accurately reproducing, (i) gate leakage in p-GaN Schottky contacts, (ii) barrier-limited transport across Al(Ga,Sc)N/GaN interfaces, and (iii) the temperature-dependent transition between thermionic and field-assisted conduction. This model thus represents an important step in achieving physical consistency between experimental leakage data and TCAD simulations of GaN-based heterostructures.

3.5.8 Numerical and Convergence Challenges

Simulations involving wide-bandgap materials are particularly prone to convergence issues due to the numerical challenges of handling extremely low intrinsic carrier concentrations and strong internal electric fields [166]. In III–nitride devices, the coupled Poisson and continuity equations often fail to converge under off–state or high–bias conditions unless specific stabilization strategies are applied.

In this work, convergence issues were mainly encountered in three contexts: (i) the presence of nonlocal meshes for tunneling calculations, (ii) large–signal bias sweeps in DC and pulsed simulations, and (iii) abrupt doping or field profiles in the buffer region. The nonlocal tunneling mesh, essential for describing Schottky and trap–assisted tunneling mechanisms, significantly increases the computational load and may cause slow or unstable convergence. To mitigate this, the nonlocal mesh length was minimized, and the spatial mesh was refined in the regions involved in tunneling with a step size below 1 nm, ensuring numerical consistency without compromising physical accuracy.

For DC transfer characteristics, direct biasing from the off–state always led to numerical divergence due to strong field gradients and charge redistribution. Stable convergence was achieved by initializing the device from equilibrium and gradually ramping the gate and drain biases through transient simulations, allowing progressive carrier redistribution. A similar approach was required for pulsed characterizations, where convergence was lost for drain voltages above 15 V when using sharp rise/fall times (1 ns). Increasing the rise/fall transition time or subdividing the voltage steps restored stability and preserved the transient accuracy.

During HTRB stress simulations, longer transient time scales facilitated convergence despite the combined bias and temperature variations. Convergence failures occurred only in rare cases with excessively high trap densities or deep energy levels, causing numerical oscillations.

For steep doping gradients, convergence issues also arise. These were resolved by smoothing the doping profiles and adopting physically graded transitions, which effectively removed spurious electric-field peaks and stabilized the simulation.

These results highlight the delicate balance between spatial discretization, numerical precision, and physical accuracy in GaN TCAD modeling. The combination of adaptive meshing, transient bias ramping, and controlled precision arithmetic proved essential to maintain convergence up to high drain voltages and temperatures, enabling accurate evaluation of leakage, trapping, and degradation mechanisms in both AlGaIn/GaN and AlScN/GaN HEMTs.

3.6 Summary and Relevance to This Work

This chapter outlined the main challenges encountered in modeling GaN-based HEMTs with commercial TCAD tools. The primary difficulties stem from the accurate representation of polarization-induced charges, interface and bulk traps, and their impact on transport and reliability, as well as from numerical convergence issues caused by the large bandgap and steep field gradients typical of III–nitride materials.

Despite these challenges, calibrated TCAD frameworks, particularly *Synopsys Sentaurus Device*, adopted in this work, remain indispensable for bridging experimental observations with physical understanding. When properly tuned and benchmarked against measurements, TCAD simulations provide a reliable means to analyze charge trapping, carrier transport, and degradation processes that cannot be directly observed experimentally.

The methodologies and calibrated models introduced in this chapter form the foundation of the simulation work presented in the following chapters. Chapter 4 focuses on gate leakage and Schottky interface modeling in p-GaN gate HEMTs, while Chapters 5 and 6 extend the discussion to stress-induced degradation (HTRB step-stress and pulsed I–V tests) in AlGaIn and AlScN barrier technologies, highlighting the role of TCAD in linking experimental reliability data with physical mechanisms.

Chapter 4

Gate Leakage Mechanisms and TCAD Modeling of p-GaN Gate HEMTs

Chapter Overview

This chapter presents a comprehensive study of gate leakage mechanisms in p-GaN gate HEMTs through calibrated TCAD simulations. The analysis begins with simplified 1D domains to separately investigate the Schottky contact and the AlGaN barrier, identifying the role of tunneling and trap-assisted mechanisms. The discussion then extends to 2D device geometries, where the effect of realistic gate-metal corners and their contribution to the overall leakage current are examined. By correlating the simulated results with experimental data, the study highlights the interplay between physical models and device geometry, providing insight into the dominant leakage paths and their impact on device operation. The findings serve as a foundation for understanding the reliability of p-GaN HEMTs and motivate the subsequent chapters on dynamic and long-term degradation.

4.1 Introduction and Motivation

Enhancement-mode GaN high-electron-mobility transistors (HEMTs) with a p-GaN gate represent one of the most promising device architectures for power electronics applications (see Chapter 2, Subsection 2.1.3) [177]. Their normally-off behavior ensures safe operation and compliance with industrial requirements for fail-safe switching, making them attractive for automotive, power conversion, and RF systems [51], [178]. However, the introduction of the p-GaN gate stack brings new reliability concerns, particularly related to gate leakage and long-term degradation under bias stress.

A number of experimental studies have demonstrated a correlation between initial gate leakage and progressive gate degradation, ultimately leading to time-dependent gate breakdown [56], [179]. As a consequence, understanding and controlling the gate leakage mechanisms has become a central aspect of device design and qualification [180]. The gate stack of a p-GaN HEMT is highly complex and, usually modelled as two back-to-back diodes: the Schottky barrier formed at the metal/p-GaN interface coexists with the underlying p-GaN/AlGaIn/GaN heterostructure, giving rise to multiple leakage paths [181]. These include thermionic emission, direct tunneling, trap-assisted tunneling (TAT) through the barrier, and hole-related processes at the Schottky contact [165].

Experimental studies and analytical models have consistently highlighted that reverse tunneling of holes at the Schottky contact represents a major contribution to the gate current [131]. Conversely, the presence of deep traps within the AlGaIn barrier has been linked to pronounced threshold-voltage instabilities, driven by both electron and hole trapping mechanisms [161]. Despite these findings, the combined impact of these processes on the evolution of both gate and drain currents remains not fully clarified.

While analytical models provide insight into the dominant mechanisms, the intricate geometry and interaction of leakage paths require a TCAD-based approach to capture their combined effect on both gate and drain currents. Previous modeling attempts have addressed tunneling of carriers across the Schottky barrier as well as TAT through the AlGaIn barrier, but a consistent simulation framework that links these contributions to experimental data is still lacking [182], [183]. In this chapter, a comprehensive TCAD study is presented, highlighting the physical mechanisms responsible for gate leakage and their impact on device operation, with particular attention to the role of gate geometry, metal work function and tunneling contributions [115].

4.2 Physical Mechanisms of Gate Leakage

The gate current in p-GaN HEMTs arises from multiple transport mechanisms, each exhibiting a distinct dependence on bias conditions, temperature, and electric field. At the metal/p-GaN Schottky interface, the dominant contributions to the gate leakage are generally attributed to hole barrier tunneling (hBT), where holes are injected from the gate metal into the p-GaN valence band, and to electron band-to-band barrier tunneling (eBT_{B2B}), which corresponds to electron transitions from the p-GaN valence band into metal [165], [131], [184]. The relative weight of these mechanisms depends on the position of the Fermi level with respect to the p-GaN band edges at the Schottky junction (Fig. 4.1).

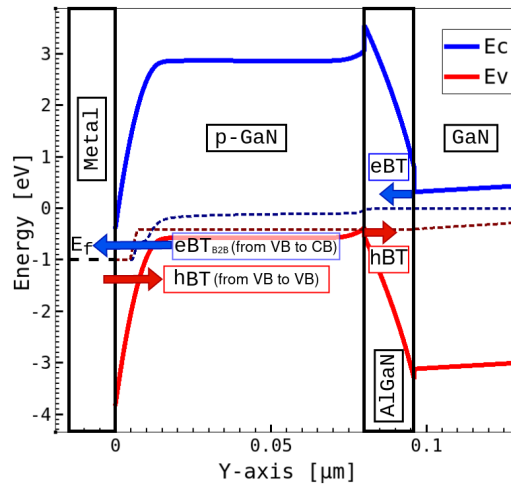


Figure 4.1: Energy-band diagram of the p-GaN HEMT at $V_{GS} = 1V$, at $T = 300 K$, with all the main tunneling processes considered in this work and discussed in the following sections.

Both processes are strongly affected by the effective Schottky barrier height, which in practice differs considerably from the ideal value predicted by the Schottky–Mott relation, based solely on the difference between metal work function and semiconductor electron affinity. One of the reasons for this discrepancy is the phenomenon of Fermi level pinning (FLP). At a metal–semiconductor interface, chemical interactions at the termination of the semiconductor crystal induce electronic states inside the bandgap. These so-called metal-induced gap states (MIGS) tend to fix, or "pin", the Fermi level close to a specific energy, often near the mid-gap, regardless of the work function of the contact metal. As a consequence, the Schottky barrier heights observed in practice show little dependence on the chosen metal or semiconductor work functions, in strong contrast to the ideal Schottky–Mott rule [185]. This effect is particularly relevant in GaN-based devices, where the presence of charged interface states at the metal/p-GaN junction can significantly lower the

apparent barrier for both carriers, thereby enhancing tunneling contributions to the gate leakage [181], [56].

In addition to Schottky-related leakage, the AlGa_N barrier introduces trap-assisted tunneling paths (as reported in Fig. 4.1). Defects and dislocations in the AlGa_N layer act as intermediate energy states, enabling electron and hole tunneling across the barrier under bias [125]. Such mechanisms are particularly relevant at moderate gate voltages, where pure thermionic emission would underestimate the experimental leakage. The spatial distribution of traps, their energy levels, capture cross-sections, trap volume, Huang-Rhys factor, and phonon energy determine the quantitative contribution of TAT to the overall gate current, as discussed in Chapter 1 (see Subsections 1.4.3 and 1.4.4).

The combined action of these processes not only controls the gate leakage characteristics, but also influences significantly the drain current through modulation of the 2DEG at the AlGa_N/Ga_N interface in the channel region. Accurate modeling therefore requires a multi-scale approach, where localized tunneling at the Schottky contact and distributed TAT in the barrier are treated consistently. In the following sections, simplified one-dimensional domains are first used to isolate and calibrate the models, before extending the analysis to the full two-dimensional device geometry.

4.3 Device Structure and TCAD Simulation Setup

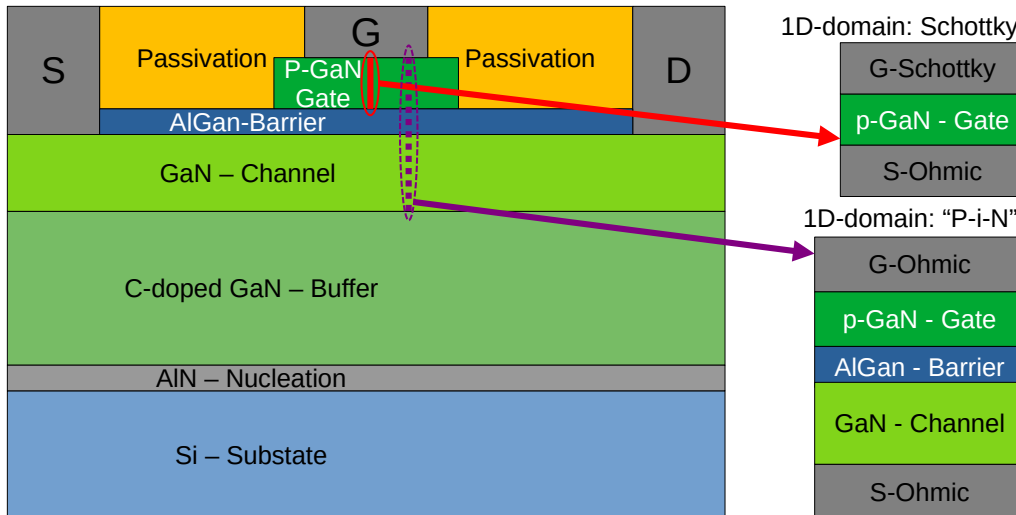


Figure 4.2: Schematic view of the full device. Solid line: 1D Schottky diode domain (top inset). Dashed line: 1D p-GaN/AlGa_N/GaN domain (bottom inset).

The reference device under investigation is a normally-off p-GaN gate HEMT for power applications. The schematic cross-section of the structure is shown in Fig. 4.2, together with the cutlines adopted to extract simplified one-dimensional domains for preliminary analyses. The device consists of a TiN gate metal deposited on top of the p-GaN layer, which is grown over an AlGaIn barrier and an unintentionally doped GaN channel. The stack is completed by the underlying GaN buffer and AlN nucleation layer on a SiC substrate, though in the simulations the focus is placed on the gate stack and the channel region.

The p-GaN region is heavily Mg-doped; however, due to the large activation energy of Mg acceptors, incomplete ionization was explicitly considered in order to correctly capture the carrier concentration and electrostatics. The doping profiles were derived from SIMS measurements provided by the fabrication partner and implemented in the TCAD environment. The incomplete ionization model available in Sentaurus Device was enabled, allowing the ionized acceptor concentration to be computed self-consistently as a function of temperature and activation energy ($\approx 160 - 200$ meV), the latter taken from literature data for Mg in GaN [186], [187], [188], [189]. At the TiN/p-GaN interface, a Schottky contact was modeled with a nominal metal work function of $\Phi_M = 4.6$ eV. This value, consistent with experimental reports for TiN ($\approx 4.1 - 5.3$ eV), was varied in some calibration steps to explore the sensitivity of the barrier height to metal properties and interface conditions [190], [191].

To clarify the individual contributions to the gate current, two simplified 1D domains were extracted: i) the metal/p-GaN Schottky diode, and ii) the vertical p-GaN/AlGaIn/GaN stack, which can be represented as a "P-i-N" diode, forming together the two back-to-back diodes (Fig. 4.2). These domains allow a separate investigation of the tunneling and trap-assisted mechanisms before moving to the full two-dimensional geometry. The 1D analyses serve as playground to fully understand the main features of the proposed physical models identified in the literature as main contributions to the gate current. The complete 2D structure includes the lateral extension of the gate and the shape of the p-GaN mesa, as provided by the external partner, thus enabling the study of edge effects and gate-corner electric field concentration.

Numerical simulations were carried out using Synopsys Sentaurus Device [141]. A refined non-local mesh was employed in the gate stack to resolve the thin depletion regions and tunneling paths, while a coarser mesh was sufficient in the buffer and substrate regions (as seen in Chapter 3). Specifically, the non-local tunneling at the metal/semiconductor contact was modeled with a non-local mesh defined over a 25 nm region under the gate. The effective masses used in the WKB tunneling

calculation were set to $m_{te} = 0.25 m_0$ and $m_{th} = 0.4 m_0$ for the electrons and holes, respectively. The mesh in this region was refined to accurately resolve the depletion layer and tunneling paths (≈ 1 nm). The material parameters were taken from standard III-nitride references, with particular attention to the bandgap, dielectric constants, and polarization coefficients of GaN and AlGaIn [192].

For the p-GaN layer, a Mg acceptor concentration in the range of $1 \times 10^{19} \text{ cm}^{-3}$ was assumed, corresponding to the nominal chemical doping introduced during growth. Hydrogen passivation effects are implicitly accounted for through the adoption of an incomplete ionization model for Mg acceptors, which limits the fraction of electrically active dopants and results in effective hole concentrations in the range typically reported for p-type GaN layers [193]–[198]. It is worth noting that the Mg acceptor activation energy $E_i = E_t - E_V$, where E_V is the valence band maximum, is known to decrease with increasing doping concentration [188]. Accordingly, for a Mg concentration of $1 \times 10^{19} \text{ cm}^{-3}$, an activation energy of $E_i = 170 \text{ meV}$ is assumed, in agreement with reported experimental and theoretical studies [199], [200].

The main physical models included in the setup are: thermionic emission at the Schottky junction and heterointerfaces, non-local tunneling for the contacts, Shockley–Read–Hall recombination, trap-assisted tunneling in the AlGaIn barrier, piezoelectric polarization at heterointerfaces and Fermi statistics (see Chapters 1 and 3 and Table 4.1 for a detailed summary).

This simulation framework provides the baseline for the subsequent analyses of gate leakage mechanisms. In the following, the simplified one-dimensional domains are first considered to disentangle the role of individual contributions before turning to the more realistic two-dimensional geometry.

Unless otherwise specified, all parameters associated with the physical models are set to the default values provided by the Sentaurus Device simulator.

4.4 One-Dimensional Simulation Domains

4.4.1 1D-Domain: Schottky Diode

The first simulation domain isolates the TiN/p-GaN Schottky junction, highlighted in Fig. 4.2 (top inset). This domain isolates the contribution of the gate Schottky junction and allows a detailed inspection of the tunneling processes at the metal/p-GaN interface. Because Mg acceptors in GaN have a relatively high activation energy (as reported above), only a small fraction of them are ionized at room temperature. Therefore, incomplete ionization was considered in the p-GaN region to accurately model the free hole concentration, which determines the electric field distribution

Table 4.1: Summary of physical models adopted in the TCAD simulations

Physics Models	Parameters
Fermi–Dirac Statistics	default
Constant mobility	$\mu_{\max} = 1500 \text{ cm}^2/\text{Vs}$
Doping-dependent mobility	default
High-field saturation	$v_{\text{sat}} = 1.8 \times 10^7 \text{ cm/s}$
SRH Recombination	default
Incomplete ionization (Mg acceptors)	$E_t = E_V + 0.17 \text{ eV}$, $N_A = 10^{19} \text{ cm}^{-3}$
Polarization (strain)	default
Thermionic emission	default
Gate workfunction	4.6 eV
Source/drain workfunction	4.3 eV
Gate nonlocal barrier tunneling	$m_{\text{te}} = 0.25 m_0$ (electrons), $m_{\text{th}} = 0.4 m_0$ (holes)
Source/drain nonlocal barrier tunneling	$m_{\text{te}} = 0.001 m_0$ (electrons), $m_{\text{th}} = 0.001 m_0$ (holes)
AlGaN nonlocal TAT	Uniform distribution, $N_T = 2.2 \cdot 10^{18} \text{ cm}^{-3}$, $E_t = E_i - 0.2 \text{ eV}$, $\sigma = 3.4 \text{ eV}$; $m_{\text{te}} = 0.1 m_0$ (electrons), $m_{\text{th}} = 0.1 m_0$ (holes)

and the depletion width at the metal/p-GaN interface [182]. At the metal contact, both thermionic emission and tunneling mechanisms were enabled (see Chapter 1). The tunneling processes were modeled using a non-local approach, in which the tunneling probability depends explicitly on the energy barrier profile rather than on a local field approximation (Fig. 4.3). The effective barrier extracted from experimental I_G – V_G curves at different temperatures typically ranges between 0.6 and 0.7 eV [131], significantly lower than the theoretical value of about 2.3–2.6 eV expected from the TiN work function ($\Phi_M \approx 4.6 \text{ eV}$) as shown in Fig. 4.3a. This discrepancy is attributed to strong tunneling contributions, which effectively reduce the apparent barrier height (see Fig. 4.3b). When only hBT is included, the simulated I_G – V_G characteristics exhibit a high onset voltage. The additional contribution of eBT_{B2B} enhances the total gate current, lowers the onset voltage, and becomes a dominant component of the overall I_G . Although this contribution might appear unphysical in the simplified 1D picture, its inclusion reproduces the experimentally observed leakage trends. Further validation of these findings is obtained by extending the analysis to the full 2D device geometry.

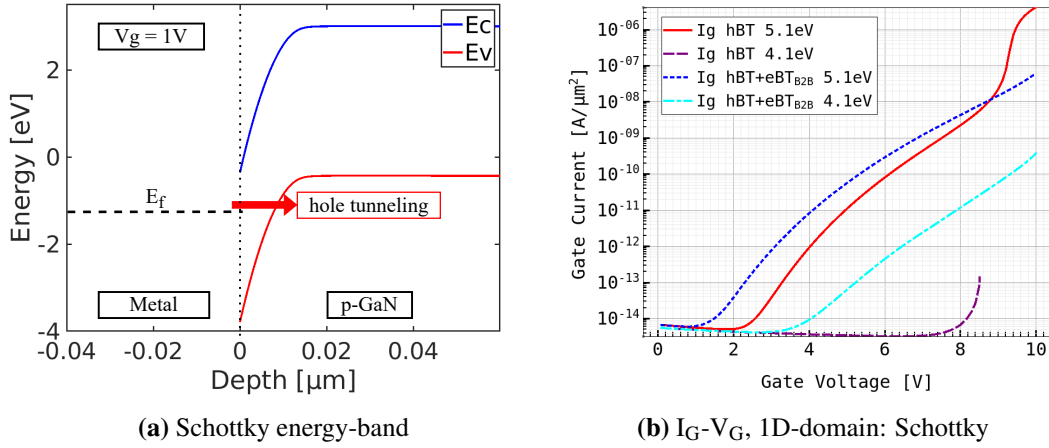


Figure 4.3: 4.3a Energy-band diagram of the 1D Schottky diode at $V_g = 1\text{V}$, at $T = 300\text{K}$. 4.3b Simulated I_G - V_G curves with different models (hBT and hBT+eBT_{B2B}) and for two different metal workfunctions (5.1 eV and 4.1 eV), at $T = 300\text{K}$. Solid and dashed lines: model hBT; Dotted and dot-dash lines: models hBT+eBT_{B2B}, respectively with 5.1eV and 4.1eV workfunctions.

4.4.2 1D-domain: AlGaN-barrier P-i-N Diode

In order to complement the Schottky diode analysis, a second simplified structure was considered, corresponding to the vertical p-GaN/AlGaN/GaN stack (bottom inset of Fig. 4.2). This configuration resembles a "P-i-N" diode, where the p-GaN cap acts as the p-side, the AlGaN barrier as the intrinsic region, and the unintentionally doped GaN channel as the n-side. By isolating this vertical domain, it becomes possible to investigate the leakage mechanisms across the AlGaN barrier without the lateral contributions of the full gate geometry. In this case, ohmic boundary conditions were applied at the top and bottom GaN contacts, in order to avoid additional effects to focus exclusively on barrier transport. In this analysis, the leakage current across the AlGaN barrier was modeled as the sum of a thermionic contribution and trap-assisted tunneling mechanisms (TAT). The TAT process was described using acceptor-type traps with uniform spatial distribution across the AlGaN layer, with a broad energetic uniform distribution inside the bandgap shown in Fig. 4.4, as suggested in earlier studies on GaN-based diodes [125], [23].

We emphasize that, while this approach is widely adopted in the literature, it primarily serves as a *calibration knob* to control the leakage current through the AlGaN barrier [125]. It does not imply that the real defect distribution in the material is uniform or has a flat energetic profile; the physical nature of the traps may involve more complex mechanisms such as trap-to-trap hopping or localized defect states, which are not explicitly resolved in this work.

Specifically, both electron and hole tunneling paths were considered: hole TAT

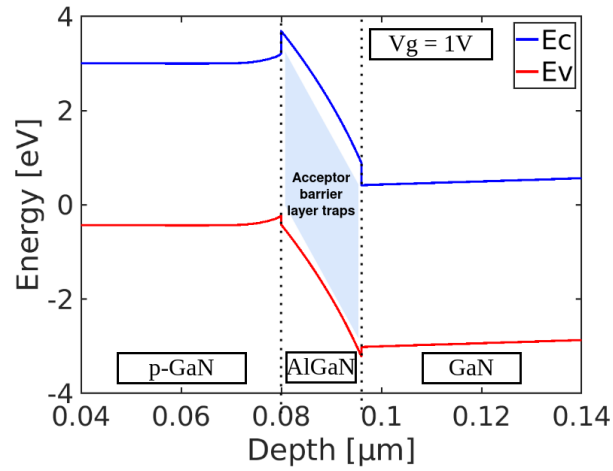


Figure 4.4: Energy-band diagram of the 1D P-i-N diode at $V_g = 1V$, at $T = 300 K$. The blue area represents the uniform spatial and energy distribution of acceptor traps within the barrier layer.

(hTAT) at the p-GaN/AlGaN interface, and electron TAT (eTAT) at the AlGaN/GaN-channel interface, as sketched in Fig. 4.5a. Fig. 4.5b reports the simulated I_G – V_G characteristics for different values of the relative tunneling masses (m_t) used in the TAT model (see Chapter 1, subsection 1.4.4). The relative tunneling masses for electrons and holes were treated as calibration parameters, they have been kept symmetric for the two carrier types and varied between 0.1 and 0.4 to match the experimental I_G – V_G characteristics. The analysis confirms that TAT plays a dominant role at low gate biases, particularly for $V_G < V_{TH}$, whereas the thermionic contribution becomes more relevant at higher biases. The insight from the two complemen-

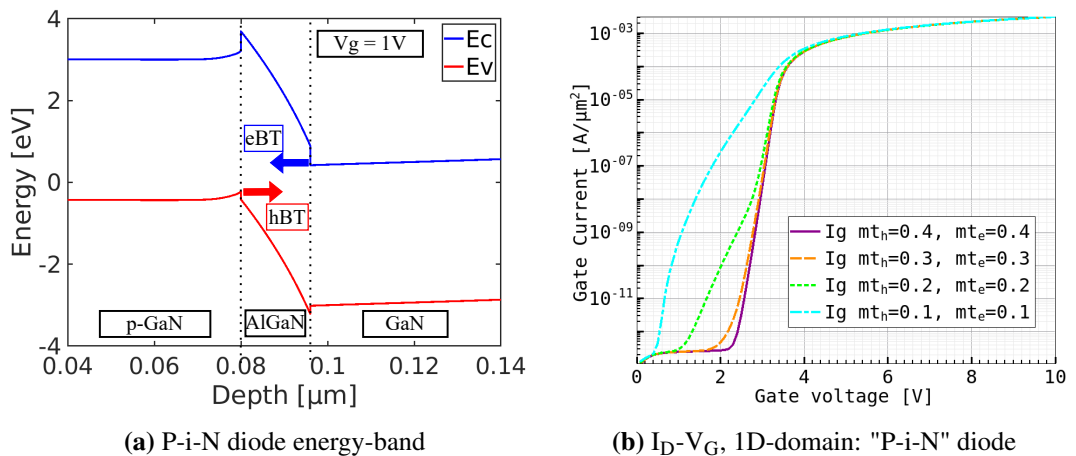


Figure 4.5: 4.5a Energy-band diagram of the 1D P-i-N diode at $V_g = 1V$, at $T = 300 K$. Arrows indicate the contributions given by the adopted models. 4.5b Simulated I_G – V_G curves of the P-i-N diode with the electron and hole TAT models in the AlGaN barrier for different electron and hole tunneling relative masses, at $T = 300 K$.

tary one-dimensional domains provides a first understanding of the different leakage mechanisms. The simulations confirm that TAT dominates the leakage in the sub-threshold regime, while at higher gate biases the Schottky-related tunneling mechanisms become increasingly important. The separate analysis of the Schottky and P-i-N domains thus provides a clear physical interpretation: while the gate metal/p-GaN interface determines/limits the high-bias leakage, the AlGaN barrier traps are responsible for the gate current at lower voltages and for the associated threshold voltage instabilities [125].

In the next section, the full two-dimensional device geometry is simulated, in order to capture the realistic gate architecture, the electric field concentration at the corners and the combined impact of Schottky barrier and AlGaN layer contributions on both gate and drain currents.

4.4.3 Summary of 1D Analysis

The 1D simulations highlight the sensitivity of gate leakage to a small number of key parameters: the Schottky barrier height (controlled by the metal work function) and the electron/hole tunneling masses for TAT. Although simplified, this approach clarifies the fundamental mechanisms and sets the stage for the more realistic two-dimensional simulations, where the combined action of corner fields, barrier traps, and Schottky tunneling is consistently included.

4.5 2D Simulations and Geometry Effects

The one-dimensional analyses presented in the previous subsections provided clear insight into the individual contributions of the Schottky junction and the AlGaN barrier to the gate leakage. However, these simplified domains neglect the impact of the full device geometry, in particular the lateral extension of the gate, the interaction between the p-GaN and the passivation, and the strong electric field crowding at the metal corners. Such effects are intrinsically two-dimensional and can significantly alter both the magnitude and spatial distribution of the leakage current.

In this section, the full HEMT structure sketched in Fig. 4.2 is simulated, including passivation, the p-GaN gate, the AlGaN barrier, the unintentionally doped GaN channel, the buffer, the nucleation, the substrate, as well as the gate, source and drain metal contacts with realistic workfunction. Following this initial analysis, rounding will be applied to the corners of the Schottky contact gate and the pGaN region, as shown in the following paragraphs. By combining the models previously validated in 1D (hole barrier tunneling at the Schottky interface and trap-assisted tunneling in

the AlGaIn barrier), the 2D setup allows us to directly compare the simulated gate and drain currents against experimental measurements.

Special attention is devoted to the spatial distribution of the electric field near the gate edges, where sharp geometrical features can induce enhanced tunneling and field-driven leakage. This makes the 2D analysis essential not only for reproducing the experimental I_G-V_G and I_D-V_G curves, but also for identifying the physical origin of the dominant leakage paths in realistic device conditions.

4.5.1 2D Device Configuration

The transition from 1D to 2D simulation requires accounting for the full HEMT geometry, including the vertical stack of p-GaN/AlGaIn/GaN layers and the lateral extension of the gate region. The gate metal work function, Mg doping, and incomplete ionization previously discussed are also reproduced in the 2D structure.

Below 80 nm of the p-GaN gate, the AlGaIn barrier is defined with a thickness of 16 nm and Al composition values of 25%, while the unintentionally doped GaN channel ($0.4\ \mu\text{m}$) extends towards the buffer ($1\ \mu\text{m}$). Donor and acceptor trap concentrations down to the buffer region are implemented by external 1d-profiles extracted by SIMS measurements. These external profiles give rise also to the n-type doping of the GaN channel in the order of $1 \times 10^{15}\ \text{cm}^{-3}$. The buffer region is C-doped GaN, with a carbon concentration of $5 \times 10^{17}\ \text{cm}^{-3}$.

In order to resolve the strong field crowding near the gate edges, a locally refined mesh is adopted in the gate region, with element sizes reduced to the nanometer scale. A nonlocal mesh is also used for the metal contacts with a proper extension to account for the tunneling. This allows the tunneling current density at the Schottky junction to be correctly evaluated, particularly at the corners, as well as the one for the source and drain contacts, which are considered as ohmic using a low workfunction and a high doping close to the contact. The trap-assisted tunneling (TAT) model implemented in the AlGaIn barrier is retained from the 1D study, with traps distributed across the bandgap and localized at the p-GaN/AlGaIn and AlGaIn/GaN interfaces thanks to two different nonlocal meshes as explained in Chapter 3, subsection 3.5.4.

The 2D device setup therefore combines the physical models separately validated in the 1D domains: hole barrier tunneling at the Schottky contact and, TAT across the AlGaIn region. This enables a direct correlation between the simulated and experimental gate (I_G-V_G) and drain (I_D-V_G) current characteristics, and allows the identification of spatial leakage distributions not accessible in 1D analyses.

4.5.2 2D Simulation Results and Discussion

Starting from the validated 1D models, the 2D simulations have been carried out to evaluate the combined effect of Schottky-barrier tunneling and AlGaIn trap-assisted conduction within the full device geometry. The gate leakage current I_G and the corresponding drain characteristics I_D are first analyzed by selectively enabling or disabling the TAT contribution in the AlGaIn barrier as visible in Fig. 4.6a. As expected, the inclusion of TAT leads to a significant change in the I_G - V_G curve, improving the agreement with experiments especially at low biases. At the same time, a relevant positive threshold voltage shift is observed in the I_D - V_G characteristics, which can be attributed to electron depletion in the 2DEG channel caused by trap-assisted leakage paths. To further explore the role of Schottky tunneling, simulations

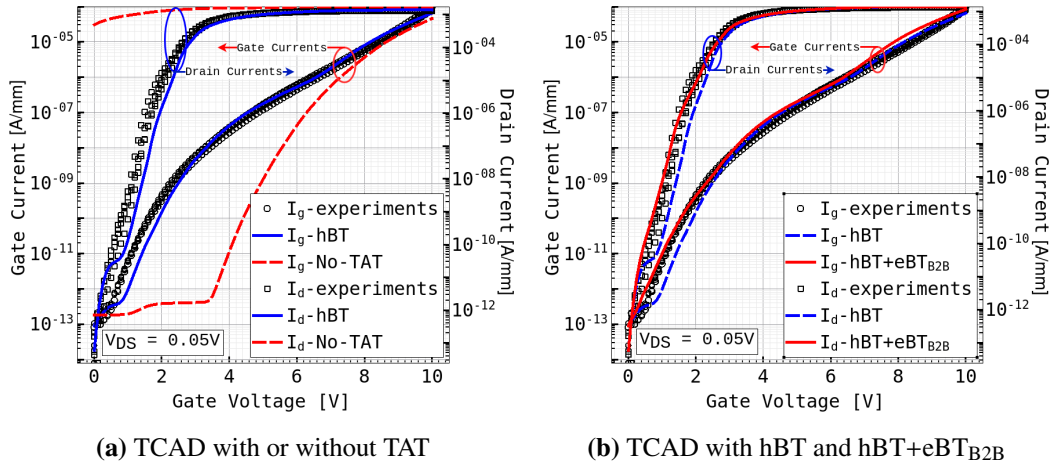


Figure 4.6: 4.6a I_G - V_G and I_D - V_G with hBT model at Schottky barrier and with or w/o TAT on the AlGaIn barrier. Measurement conditions $V_{DS} = 0.05V$, at $T = 300K$. Symbols: experiments. 4.6b I_G - V_G and I_D - V_G with TAT on the AlGaIn barrier and with hBT or hBT+eBT_{B2B} at the Schottky barrier. Measurement conditions $V_{DS} = 0.05V$, at $T = 300K$. Symbols: experiments.

are also performed with and without the band-to-band electron tunneling (eBT_{B2B}) model as shown in Fig. 4.6b. In the 2D device, the contribution of eBT_{B2B} is found to be less critical compared to the 1D case, as the more realistic geometry already captures the enhanced leakage at the gate edges. This indicates that the dominant conduction mechanisms can be primarily explained by hole tunneling (hBT) at the Schottky contact, together with TAT in the AlGaIn barrier.

These results highlight the necessity of 2D modeling for p-GaN gate HEMTs: while 1D analyses are useful for identifying an understanding individual transport mechanisms, only the 2D geometry allows for a correct evaluation of electric-field crowding at the gate edges and the resulting localized leakage paths.

4.5.3 Electric Field Distribution and Role of Gate Corners

To gain further physical insight into the leakage mechanisms, the electric field distribution around the gate contact is analyzed. As shown in the 2D field maps in Fig. 4.7, the maximum field is strongly concentrated at the edges of the gate metal, confirming the relevance of localized tunneling paths. In simulations including only hole tunneling (hBT) at the Schottky barrier (Fig. 4.7a), the field peaks at the corners up to $1.769 \times 10^7 \text{ V/cm}^{-1}$. When the additional band-to-band electron tunneling (eBT_{B2B}) contribution is included (Fig. 4.7b), the local carrier concentration at the Schottky junction decreases, and the field distribution changes accordingly. The analysis of the

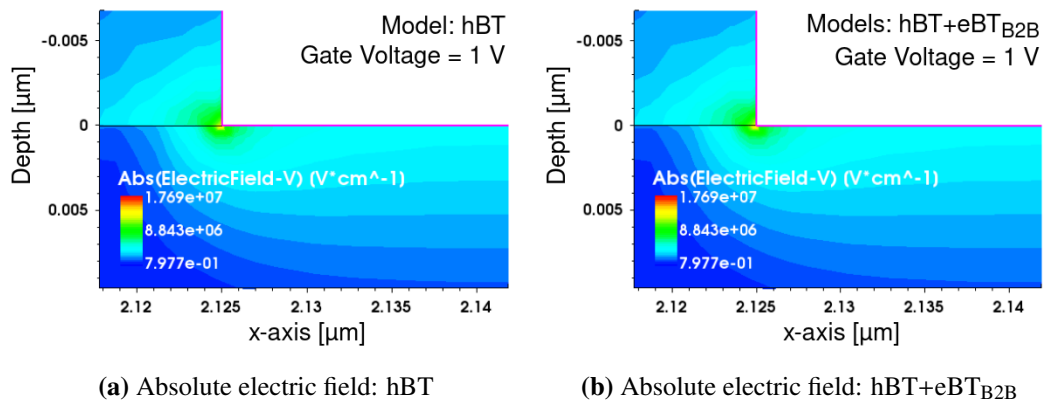


Figure 4.7: 4.7a 2D plot of the absolute electric field around the left edge of the gate contact obtained with the hBT model at the Schottky contact for $V_G=1\text{ V}$, $V_{DS} = 0.05\text{ V}$, at $T = 300\text{ K}$. 4.7b 2D plot of the absolute electric field around the left edge of the gate contact obtained with the hBT+eBT_{B2B} models at the Schottky contact for $V_G=1\text{ V}$, $V_{DS} = 0.05\text{ V}$, at $T = 300\text{ K}$.

electric field distribution obtained from the .tdr files (Figs. 4.7a and 4.7b) clearly reveals that the sharp gate edges induce severe field crowding, leading to unrealistically high local fields. Such artifacts strongly affect the simulated leakage current, suggesting that a more realistic description of the gate geometry is required. Scanning electron microscopy (SEM) inspections usually reveal rounded corners in the gate geometry. To this end, the gate contact is split into planar and corner regions, and the corner profile is modified with rounded edges, allowing us to better isolate and quantify the contribution of the edge leakage mechanisms. This refinement not only reduces the peak electric field at the metal edge but also redistributes the tunneling current, yielding a better agreement with the measured I_G-V_G and I_D-V_G curves.

4.5.4 Contact Splitting and Gate Current Components

In order to achieve a more realistic representation of the gate region, the effect of corner rounding was investigated based on cross-section images of fabricated devices obtained by SEM [124]. Fig.4.8 reports the gate region highlighting the sidewalls and with a zoom in the rounded metal corners. The SEM images revealed that the

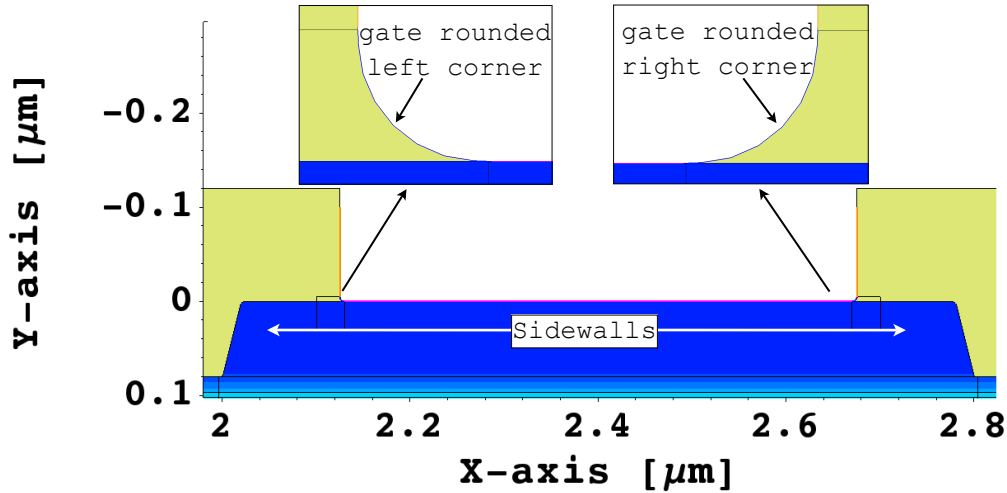


Figure 4.8: View of the gate region. A more realistic rounding of the metal edges is applied to the TCAD setup as highlighted in the insets of the two corners.

vertical p-GaN sidewalls are not strictly perpendicular to the AlGaIn surface, but exhibit a finite slope, as previously reported in [124]. TCAD simulations confirmed that such inclination of the sidewalls has negligible impact on either gate or drain current, likely due to the idealized assumptions adopted at these edges (e.g., absence of traps). In contrast, the rounding of the metal corners was found to play a fundamental role in reducing the field crowding and lastly in reproducing the measured leakage characteristics. Figure 4.9 illustrates the geometry implemented in Sentaurus with sidewall inclination and rounded gate corners. The electric field distribution extracted from the .tdr output files including corner rounding, highlights that the field enhancement is mitigated (Figs. 4.10a–4.10b), and the resulting leakage becomes more consistent with experimental evidence (Fig. 4.11). This confirms that 2D simulations with accurate geometry are essential, since simplified sharp-corner approximations overestimate the gate current. To further separate the contributions of different regions, the gate contact was split into three domains: (i) the central metal/p-GaN Schottky interface, and (ii) the two corner regions representing the metal/passivation interface (Fig. 4.11). The simulation results in Fig. 4.11 show that the central Schottky area dominates the leakage at high gate biases, whereas the

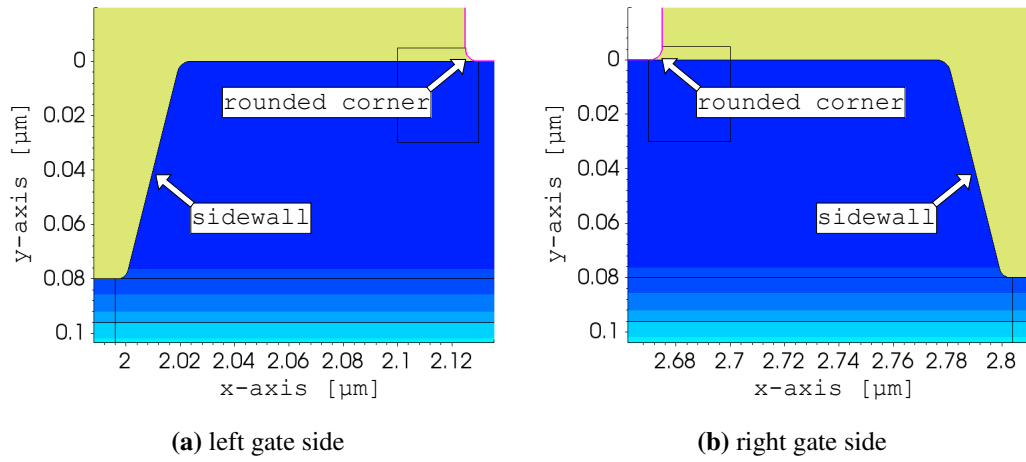


Figure 4.9: 4.9a Device geometry accounting for rounded metal corner (left side). 4.9b Device geometry accounting for rounded metal corner (right side).

rounded corners contribute significantly at low biases due to enhanced local tunneling. Interestingly, the simulations revealed that using a uniform work function across the gate no longer reproduced the experimental I_G - V_G trends once corner rounding was introduced. A better agreement was obtained by assigning $\Phi_M = 5.8$ eV to the central Schottky interface (thus lowering the effective hole barrier height), while maintaining $\Phi_M = 4.6$ eV at the corner/passivation regions. This configuration provided a good fit to both the high-bias and low-bias gate leakage regimes. The comparison between simulations with and without the band-to-band electron tunneling (eBT_{B2B}) model confirmed that, in the realistic rounded-corner geometry, the additional electron path is no longer required to reproduce experiments. In fact, the hBT alone accurately describes both I_G and I_D characteristics, while including eBT_{B2B} slightly worsens the agreement. This indicates that the apparent need for additional leakage mechanisms in simplified geometries originates from unphysical fields rather than from intrinsic device physics.

Overall, this analysis demonstrates that the central Schottky region governs the high-bias leakage regime, while the corner regions dominate the subthreshold leakage due to field localization. In sum, realistic gate rounding is essential to capture both gate and drain current behavior without overestimating leakage.

These findings confirm that gate leakage in p-GaN HEMTs is inherently two-dimensional and strongly dependent on local electrostatics at the gate edges, highlighting the importance of accurate geometric representation in TCAD frameworks.

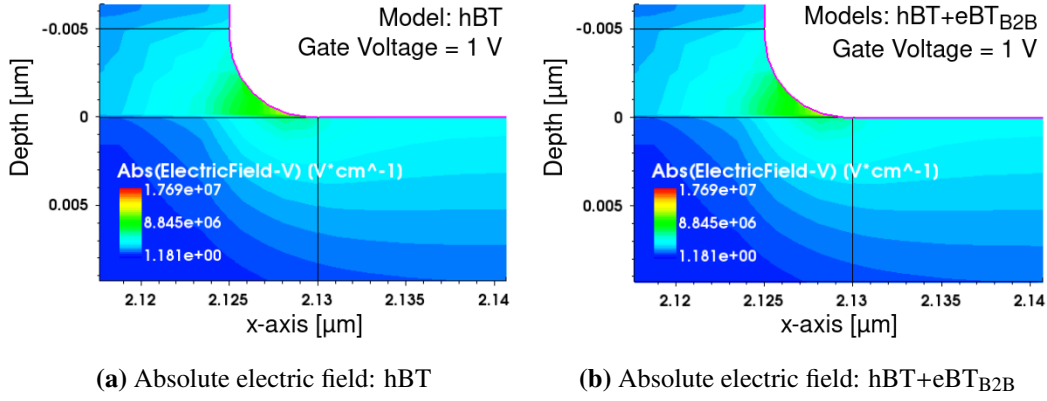


Figure 4.10: 4.10a Absolute electric field at the rounded left edge of the gate contact obtained with the hBT model on the Schottky contact for $V_G=1V$, $V_{DS} = 0.05 V$, at $T = 300 K$. 4.10b Absolute electric field at the rounded left edge of the gate contact obtained with the hBT+eBT_{B2B} models on the Schottky contact for $V_G=1V$, $V_{DS} = 0.05 V$, at $T = 300 K$.

4.6 Concluding Remarks and Transition to Reliability Analysis

In this chapter, a comprehensive TCAD study of gate leakage mechanisms in p-GaN gate HEMTs has been presented. Starting from simplified 1D structures, the main physical contributions to gate current were identified: hBT at the Schottky contact and trap-assisted tunneling (TAT) through the AlGa_N barrier. Although band-to-band electron tunneling (eBT_{B2B}) can artificially improve the fit in oversimplified models, it was shown that its role is not essential when a realistic 2D geometry is considered.

Two-dimensional simulations highlighted the critical importance of the gate geometry. Sharp corners at the metal/p-GaN interface generate unrealistically high electric fields, leading to an overestimation of tunneling currents. By introducing rounded gate corners, consistent with experimental device cross-sections, the simulated I_G-V_G and I_D-V_G characteristics achieved excellent agreement with the measurements without invoking additional leakage mechanisms.

The splitting of the gate contact into central and corner regions provided further physical insight. It was demonstrated that the central Schottky region dominates the leakage at high gate biases, while the corner regions are responsible for enhanced leakage at low biases due to localized electric fields. This confirms that leakage in p-GaN gate HEMTs is inherently a two-dimensional phenomenon and cannot be fully captured by 1D approaches.

Overall, the proposed simulation framework establishes a reliable methodology for modeling gate leakage in normally-off GaN HEMTs. The insights gained here

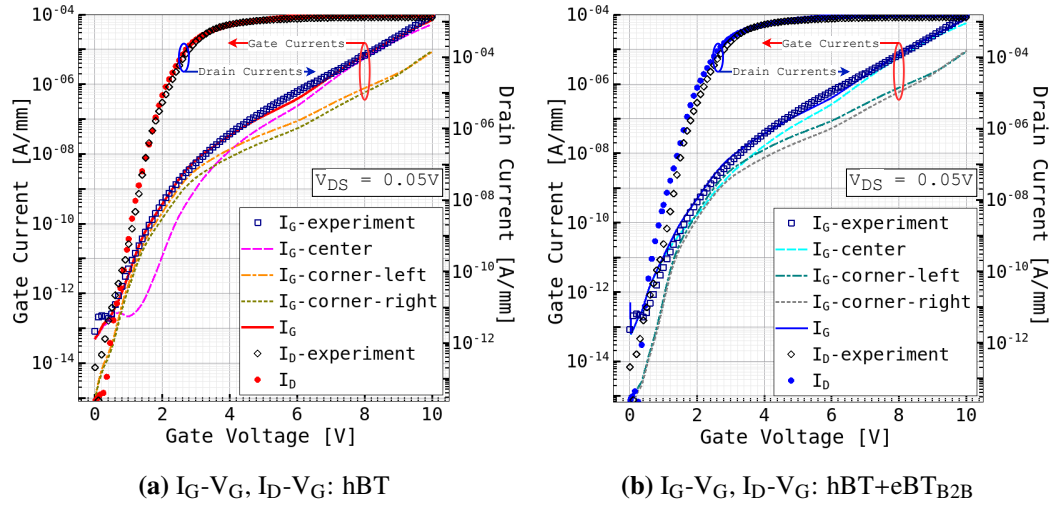


Figure 4.11: 4.11a I_G - V_G and I_D - V_G when splitting the contact with the hBT model on the Schottky barrier, with $V_{DS} = 0.05$ V, at $T = 300$ K. Symbols in black: experiments. Solid line: total I_G , red symbol total I_D . Dashed, line-dot and dotted lines: center and corners I_G components. 4.11b I_G - V_G and I_D - V_G when splitting the contact with the hBT+eBT_{B2B} models on the Schottky barrier, with $V_{DS} = 0.05$ V, at $T = 300$ K. Symbols in black: experiments. Solid line: total I_G , blue symbol total I_D . Dashed, line-dot and dotted lines: center and corners I_G components.

provide a solid foundation for the subsequent chapters, where the focus will shift from static leakage analysis to dynamic and long-term degradation under stress conditions.

The modeling of gate leakage presented in this chapter represents a fundamental step toward a deeper understanding of GaN HEMT reliability. While static simulations have clarified the relative contributions of hole tunneling, trap-assisted mechanisms, and the impact of device geometry, long-term reliability cannot be addressed without considering the dynamic response of the device under electrical stress.

In particular, time-dependent trapping and detrapping processes strongly affect drain current stability and threshold voltage shifts. These effects can be revealed through pulsed-IV characterization, which separates static from dynamic behavior, and through HTRB step-stress experiments, which accelerate degradation mechanisms.

The next chapters therefore extend the analysis from static gate leakage to dynamic and stress-induced degradation, by combining experimental measurements with calibrated TCAD simulations. This approach enables a quantitative evaluation of trap dynamics at different interfaces and their impact on device performance over time.

Chapter 5

TCAD Modeling and Degradation Study of AlGaN/GaN HEMTs under Pulsed I-V and HTRB Step-Stress Conditions

Chapter overview

This chapter presents a comprehensive study on the reliability and degradation mechanisms of AlGaN/GaN high-electron-mobility transistors (HEMTs), combining experimental characterization with calibrated TCAD simulations. The analysis aims to establish a physically grounded reference framework for subsequent investigations on alternative barrier technologies.

A full calibration of the TCAD setup is first performed by benchmarking against measured transfer, input, and output characteristics, ensuring accurate reproduction of the device electrostatics and transport behavior. Once validated, the model is employed to investigate charge-trapping phenomena and stress-induced degradation through two complementary regimes: pulsed I–V characterization and HTRB step-stress testing. The pulsed regime enables the identification of trapping dynamics under controlled quiescent conditions, while the HTRB analysis accelerates long-term degradation mechanisms at elevated temperature and electric field.

The pulsed I–V section extends the experimental investigation by separating the contributions of donor traps at the passivation/cap interface and Fe-related acceptor traps in the buffer and channel. Through systematic TCAD simulations, the interplay between these two trap families is clarified, revealing how their relative energy levels and concentrations govern the observed current collapse and recovery behavior under different bias conditions. This analysis demonstrates the necessity of jointly

modeling interface and bulk traps to reproduce experimental data and correctly explain transient degradation mechanisms.

The HTRB step-stress analysis complements this study by exploring progressive degradation under high-voltage operation. Experimental and simulated results are compared to understand the evolution of drain current and gate leakage. Extended parametric analyses are carried out to quantify the impact of donor concentration, donor energy depth, and leakage pathways on long-term reliability. The results emphasize the key role of donor detrapping at the SiN/GaN-Cap interface and field-assisted leakage in determining the overall degradation trend.

Overall, this chapter establishes the AlGaIn/GaN HEMT as a calibrated benchmark for subsequent reliability studies. The combined experimental–simulation framework provides valuable insight into the intertwined effects of interface and buffer traps, forming the physical baseline for the comparative analysis of AlScN/GaN devices discussed in Chapter 6.

5.1 Introduction

High-electron-mobility transistors (HEMTs) based on the wide-bandgap AlGaIn/GaN have become a cornerstone technology for high-frequency and high-power electronics [43], [201]–[203]. Their success stems from the unique ability of polar III-nitrides to form a high-density 2DEG at the heterointerface through the combined effects of spontaneous and piezoelectric polarization [15], [16], [172]. This intrinsic mechanism enables high electron mobility and low channel resistance without intentional doping, making AlGaIn/GaN HEMTs ideally suited for applications such as power conversion, automotive electronics, and RF amplification, including satellite and 5G/6G infrastructure [204]–[208].

Despite their outstanding performance, the widespread adoption of GaN HEMTs in commercial systems critically depends on their long-term reliability. Compared with established semiconductor technologies such as Si and SiC, GaN-based devices still face several reliability challenges, including current collapse, bias instabilities, and leakage dispersion [104], [209]. These issues originate from charge trapping phenomena occurring at multiple locations, such as the passivation/barrier interface, the barrier/channel interface, and the buffer region, that are strongly influenced by material quality and processing conditions. Over the past decade, research has converged on two major reliability concerns: (i) off-state leakage currents, and (ii) trap-related degradation leading to threshold-voltage (V_{th}) shifts and dynamic on-resistance (R_{ON}) increase [39], [51], [87], [210]–[215].

To mitigate leakage and enhance breakdown robustness, various buffer architectures have been introduced, including undoped, carbon-doped, Fe-doped GaN, and more complex AlN or superlattice-based designs [113], [213], [216], [217]. Among these, Fe-doped buffers are widely used because of their deep acceptor levels, which compensate residual donors and suppress parasitic conduction. However, Fe atoms can diffuse toward the channel, reducing the 2DEG density and introducing acceptor-like traps that compete with donor states at the passivation interface [79], [80]. This interplay between bulk and interface traps critically impacts both short-term and long-term reliability [88], [218], [219].

Pulsed I–V measurements provide a powerful diagnostic of these dynamic trapping effects under controlled quiescent conditions. By choosing suitable (V_{GS} , V_{DS}) bias points, one can selectively activate different trap families and probe their dynamics over distinct time scales, while avoiding self-heating and equilibrium effects typical of DC sweeps [220]–[222]. Recent works have linked current collapse and recovery behavior to the complex electrostatic interaction between Fe-related acceptor traps in the channel/buffer and donor-type interface traps near the surface. This study adopts a calibrated TCAD framework to reproduce and interpret these pulsed I–V experiments, highlighting how the concurrent presence of both trap families determines the transient response and the observed current degradation [160], [162]–[164].

Complementing the pulsed characterization, fast long-term reliability is assessed through HTRB step-stress experiments. This accelerated aging method applies increasing drain bias under high-temperature off-state conditions to stimulate progressive defect activation and leakage evolution [88], [209], [223], [224]. Unlike conventional HTRB tests lasting hundreds of hours, the step-stress approach uses shorter stress intervals, typically minutes, to reveal early-stage degradation and identify sensitive failure mechanisms. Experimentally, the method allows monitoring the evolution of drain and gate currents after each stress phase, providing insight into both recoverable and permanent damage.

TCAD simulations play a key role in connecting these experimental observations with their physical origins. By incorporating realistic trap distributions, polarization-induced charges, and transport models, the simulation framework reproduces the measured electrical characteristics and allows separate evaluation of the effects associated with interface, barrier, and buffer traps. Through parameter variations, such as donor trap energy level, density, and gate-leakage modeling, the approach captures the main features of the current collapse and the long-term degradation observed during HTRB. In particular, it reveals that Fe-related acceptor traps dominate transient effects in pulsed operation, while the partial discharge of donor states at the

SiN/AlGaN interface drives the progressive degradation under HTRB stress.

Building upon the author's previous studies, in which step-stress HTRB and pulsed I–V measurements were jointly analyzed through TCAD [88], [89], this chapter consolidates and extends the understanding of degradation mechanisms in AlGaN/GaN HEMTs. The combined experimental–simulation methodology developed here serves as the baseline reference for the next chapter, which applies the same approach to AlScN/GaN devices to elucidate the performance–reliability trade-offs introduced by the novel barrier.

5.2 TCAD Calibration and Benchmarking

5.2.1 Device structure and model setup

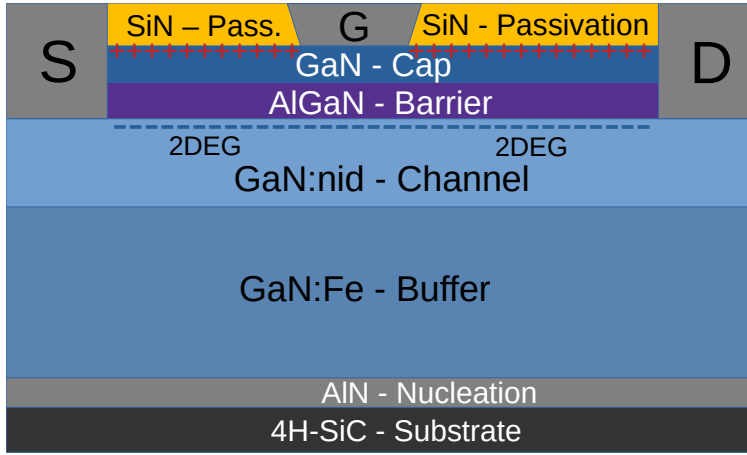


Figure 5.1: Schematic view of the AlGaN/GaN device. The gate opening is $0.15\text{-}\mu\text{m}$. The gate distances between source and drain are $0.7\text{ }\mu\text{m}$ and $1.2\text{ }\mu\text{m}$, respectively. All other device specifications can be found in [88], [104]. Donor trapped charges at SiN/cap interface are indicated with "+", and 2DEG with "-", respectively.

The reference device is an AlGaN/GaN HEMT on a 100-mm semi-insulating 4H-SiC substrate (Fig. 5.1). The stack comprises: AlN nucleation, Fe-doped GaN buffer, non-intentionally doped (n.i.d.) GaN channel, a 14-nm $\text{Al}_{0.31}\text{Ga}_{0.69}\text{N}$ barrier, a 4-nm GaN cap, and SiN passivation [99]. Source (S) and drain (D) ohmic contacts are realized via heavily Si implantation under the metal; the Schottky gate uses Pt/Au metal stack. A dual field-plate layout improves drain-side field shaping, enhancing the breakdown capabilities and ensuring a limited R_{ON} degradation [113], [114]. Device processing uses an advanced version of GaN15, with a gate length is $0.15\text{ }\mu\text{m}$, a distance gate-source $L_{\text{GS}} = 0.7\text{ }\mu\text{m}$, and a spacing gate-drain $L_{\text{GD}} = 1.2\text{ }\mu\text{m}$. The device under study was fabricated by an external industrial partner, which also

provided the experimental characterization data used in this work for model calibration and analysis [104]. The drift–diffusion transport with Fermi–Dirac statistics is adopted in the TCAD deck (Synopsys *Sentaurus Device* [18]). Key models enabled: thermionic emission at heterointerfaces, anisotropic permittivity, spontaneous and piezoelectric polarization, Shockley–Read–Hall recombination, Caughey–Thomas (CT) high-field mobility, and non-local electron tunneling at the Schottky gate and at S/D for ohmic contact emulation (See Chapter 3). Uniform Fe-related acceptor traps are included in the buffer ($1 \times 10^{18} \text{ cm}^{-3}$), with an exponential tail extending into the channel/barrier/cap as in [88], [225], [226], to capture the experimentally observed 2DEG reduction and strengthened confinement. The adopted trap profile and concentration were defined in agreement with the process development group responsible for the device fabrication.

The main physical models included in the setup are summarized in Table 5.1.

Table 5.1: Summary of physical models adopted in the TCAD simulations

Physics Models	Parameters
Fermi–Dirac Statistics	default
Constant mobility	$\mu_{\text{max}} = 1660 \text{ cm}^2/\text{Vs}$
Doping-dependent mobility	default
High-field saturation	$v_{\text{sat}} = 1.2\text{--}1.35 \times 10^7 \text{ cm/s}$, $\beta = 1.0$
SRH Recombination	default
Polarization (strain)	default
Thermionic emission	default
Gate workfunction	6.75–7.2 eV (It is emphasized that these values are not claimed as physical metal work functions; rather, they compactly encode unmodeled interface/electrostatic effects while leaving gate-leakage calibration to m_{te})
Source/drain workfunction	4.3eV
Gate nonlocal barrier tunneling	$m_{\text{te}} = 0.012 m_0$ (electrons), $m_{\text{th}} = 0.4 m_0$ (holes)
Source/drain nonlocal barrier tunneling	$m_{\text{te}} = 0.001 m_0$ (electrons), $m_{\text{th}} = 0.001 m_0$ (holes)

Unless otherwise specified, all parameters associated with the physical models are set to the default values provided by the Sentaurus Device simulator.

5.2.2 Mobility models and transport calibration

The low-field mobility is calibrated based on Hall-effect measurements of the 2DEG provided by the fabrication partner. Since the Hall mobility μ_H differs from the drift mobility μ_{drift} by the Hall factor $r_H = \mu_H/\mu_{\text{drift}}$, which depends on the dominant scattering mechanisms, this correction was evaluated from literature data. According to [9], the Hall factor for GaN is typically close to unity under polar optical scattering, while it slightly increases ($r_H \approx 1.1$) when piezoelectric or ionized impurity scattering mechanisms are dominant. Given that polar optical phonon scattering dominates at room temperature in AlGaN/GaN heterostructures, it is assumed $r_H \approx 1$ as a reasonable approximation, substituting its value directly in Eq. 3.1.

The doping dependence of the mobility is modeled using the Masetti formulation with standard GaN parameters, effectively describing impurity-scattering degradation without additional fitting coefficients (see Chapter 3, subsection 3.5.5).

At high electric fields, carrier transport was modeled using the Caughey–Thomas (CT) empirical model (Chapter 3, subsection 3.5.5, Eq. 3.5) [227]. The best agreement with the measured output characteristics is obtained for $v_{\text{sat}} = (1.2\text{--}1.35) \times 10^7$ cm/s and $\beta = 1.0$, consistent with literature values for GaN-based heterostructures [99], [228]–[230]. This formulation allows a smooth transition from drift-diffusion behavior at low fields to velocity saturation at high fields, ensuring stable convergence and accurate reproduction of the measured I – V curves. The gate current was calibrated independently by adjusting the effective electron tunneling mass m_{te} within the non-local tunneling framework (see Chapter 3, subsection 3.5.3). This parameter governs the tunneling probability through the Schottky barrier and was fine-tuned to reproduce mainly the reverse I_G characteristics, achieving good agreement with experiments with a value for $m_{\text{te}} = 0.012m_0$ (Fig. 5.2).

5.2.3 2DEG concentration and threshold alignment

The 2DEG is established by the interplay of polarization charges, surface donors at the SiN/cap interface, and the presence of unwanted defects inside the channel [88]. Following [15], [18], [88], the measured experimental sheet density of $n_s = 9.3 \times 10^{12}$ cm $^{-2}$, is matched using donor states at the SiN/GaN-cap with $N_D = 5 \times 10^{13}$ cm $^{-2}$ at $E_t = E_C - 1.55$ eV, with E_C the conduction band edge minimum [110], [172], [231]. The latter traps compensate for the piezoelectric polarization charges modeled with default values in [18], leading to the desired 2DEG density [15], [104]. Furthermore, also Fe-related traps have their own contribution (see Subsec 5.2.4).

A distinctive feature of these devices is a threshold voltage less negative than typical for depletion-mode AlGaN/GaN HEMTs (here close to -2 V rather than ~ -4 V).

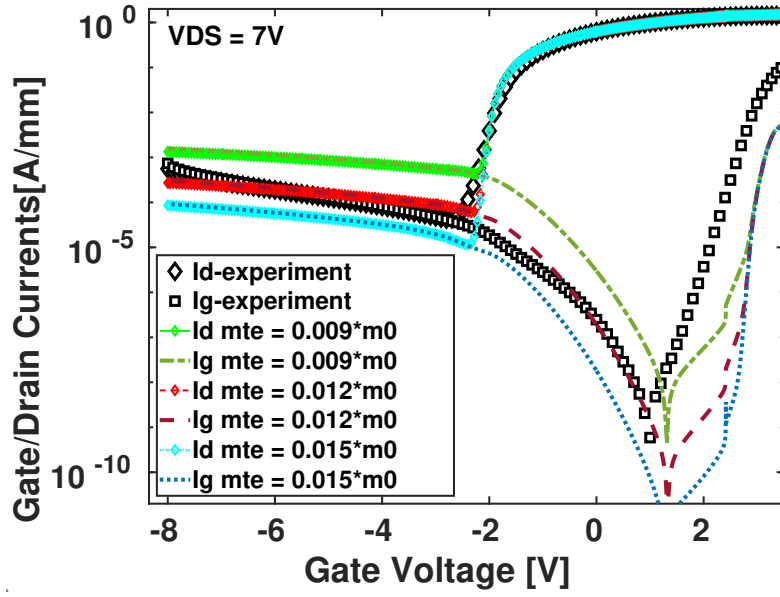


Figure 5.2: Semi-log I-V curves of AlGaIn/GaN HEMTs, measured at $V_{DS} = 7V$, at $T = 300$ K. Experiments vs. TCAD for different electron tunneling masses: $m_{te} = 0.009m_0, 0.012m_0$, and $0.015m_0$.

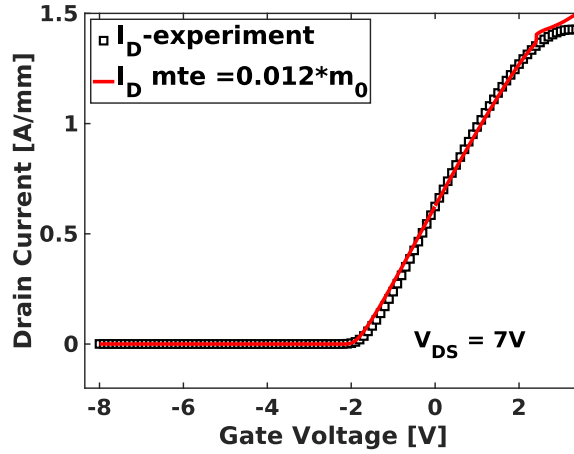


Figure 5.3: DC transfer characteristic of AlGaIn/GaN HEMT, measured at $V_{DS} = 7$ V, at $T = 300$ K. Experiments vs. TCAD data.

When the above interface/polarization charge configuration is enforced to reproduce n_s , the matching of the measured V_{th} requires an effective Schottky work function Φ_M^{eff} larger than the nominal Au-Pt value [232]. In TCAD, we therefore use Φ_M^{eff} as a calibration parameter that compactly absorbs: (i) metal/semiconductor Fermi-level pinning and interfacial dipoles at the gate, (ii) partial relaxation/compensation of polarization charge at channel/barrier, barrier/cap and cap/passivation (most likely the main problem with the high extracted work function), and (iii) fixed/contact-induced charges near the gate edge [233]–[238]. Quantitatively, $\Phi_M^{eff} \approx 7.2$ eV reproduces

the transfer curve of Fig. 5.3 (same die used for I_G calibration in Fig. 5.2), while a second dataset (Fig. 5.4, different die) is fitted with $\Phi_M^{\text{eff}} \approx 6.75$ eV together with a slight v_{sat} adjustment, from 1.2×10^7 cm/s in the first case to 1.35×10^7 cm/s in the latter. It is emphasized that these values are *not* claimed as physical metal work functions; rather, they compactly encode unmodeled interface/electrostatic effects while leaving gate-leakage calibration to m_{te} [18]. The resulting transfer/input characteristics show close agreement with experiments in both linear and log scales (Fig. 5.3, Fig. 5.2), and the output family is captured under the fresh (0, 0) V quiescent condition (Fig. 5.4).

5.2.4 Band diagram comparison and validation

Figure 5.5 summarizes the access-region electrostatics: (a) the conduction-band diagram shows the channel confinement and Fermi-level position at equilibrium; (b) the net charge map details polarization sheets and compensating donor charge at SiN/cap, with the 2DEG indicated at the AlGaN/GaN interface. The charge absolute value is consistent with the measured n_s . The Fe-tail in the GaN channel helps the 2DEG confinement, more specifically, Fig. 5.6a shows the adopted exponential tail of the Fe doping, that reduces in module of about one order of magnitude moving from the GaN buffer (uniform doping of 1×10^{18} cm $^{-3}$) towards the AlGaN barrier. The doping profiles are all defined as acceptor-type bulk traps with energy level $E_t = E_C - 0.5$ eV, fixed in accordance to [239], [240], [241], [242]. Even if a range of values are reported in the experimental analysis [243], [244], [245], [241], [242], small variations of E_t are not expected to produce appreciable changes in the

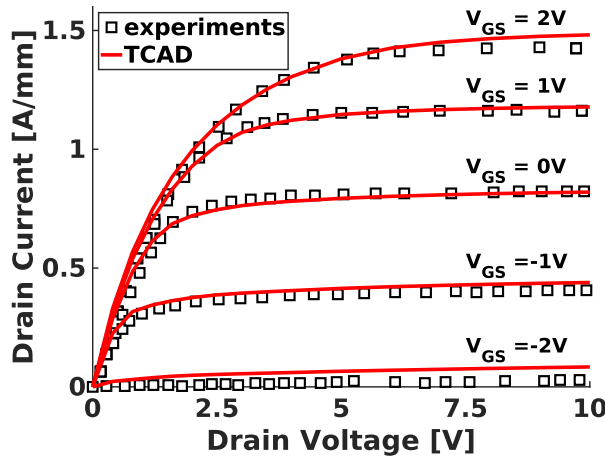


Figure 5.4: Pulsed DC-IV data vs. TCAD simulations of AlGaN/GaN HEMT. The device V_{GS} ranging from -2 V to 2 V in steps of 1 V. The quiescent bias condition is (0V,0V), at $T = 300$ K.

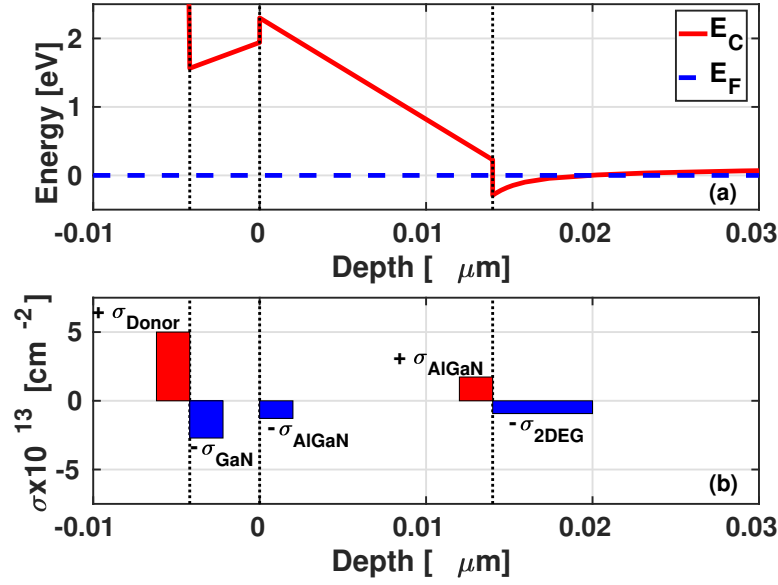


Figure 5.5: (a) Energy band diagram of the AlGaIn/GaN heterostructure in the access region. (b) Net charge distribution at different interfaces, with visible 2DEG charge, given by electrons supplied by surface donor states.

simulated device characteristics. In the same figure, the ionized concentration of Fe-related doping is reported showing a relevant activated doping in the GaN channel. If compared to the case of doping without the exponential tail, a significant difference can be observed for the ionized Fe distributions. To better understand their effect, the band structures calculated in the two cases and without Fe doping are reported in Fig. 5.6b, along with the extracted 2DEG concentrations: the presence of Fe ions in the channel causes a reduction of the 2DEG and a more effective confinement in the channel region due to the correlated band banding.

Altogether, the benchmark in Figs. 5.2, 5.3, and 5.4 confirms that the calibrated deck reproduces the subthreshold/on-state behavior and the gate-current dispersion under reverse/forward bias. This baseline will be used in the next sections to (i) decompose pulsed I-V degradation into bulk vs. interface trapping contributions and (ii) analyze HTRB step-stress sensitivity to passivation-interface donors and gate-leakage evolution.

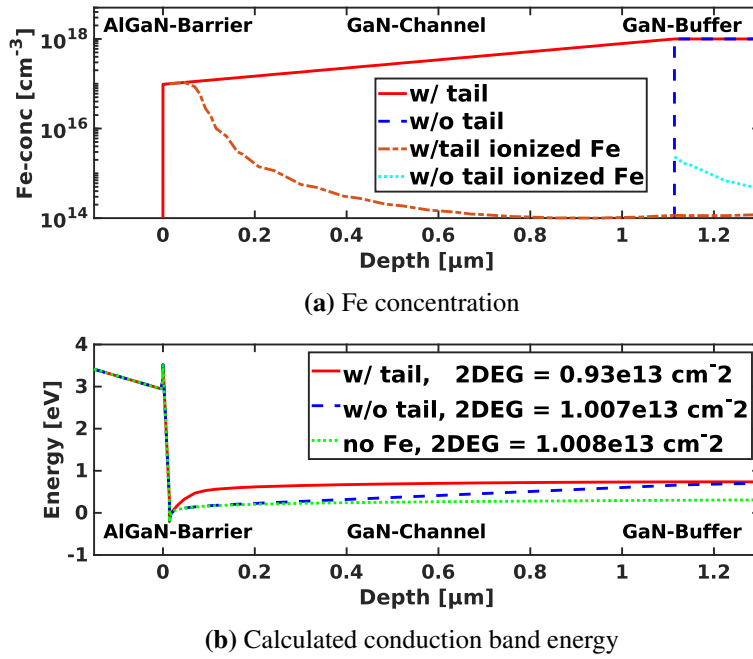


Figure 5.6: (a) Fe distribution and ionized atoms (active concentration) with and without the exponential tail used in the TCAD setup. (b) Calculated conduction band energy at equilibrium w/ and w/o exponential tail and without Fe doping. The corresponding 2DEG concentration is reported in each label.

5.3 Pulsed I–V Analysis

5.3.1 Methodology

Pulsed I-V measurements were employed to probe and capture a *snapshot* of the trapping-state dynamics in the AlGaN/GaN HEMTs under different quiescent operating conditions.

This technique allows separating trapping-related transients from self-heating and long-term bias-history effects, thus providing a clear assessment of the dynamic behavior of the device.

The measurement sequence follows the standard double-pulse methodology [220]–[222]. In this protocol, the device is first biased at a fixed quiescent state ($V_{GS,Q}$, $V_{DS,Q}$) long enough to establish steady-state trap occupancy. Subsequently, short voltage pulses are applied to the gate and drain terminals to probe the instantaneous channel response, preventing significant charge redistribution during the measurement and temperature increase. In this way, ultra-fast trapping effects are filtered out, and the contribution of slower traps, typically associated with interface or buffer states, can be effectively isolated.

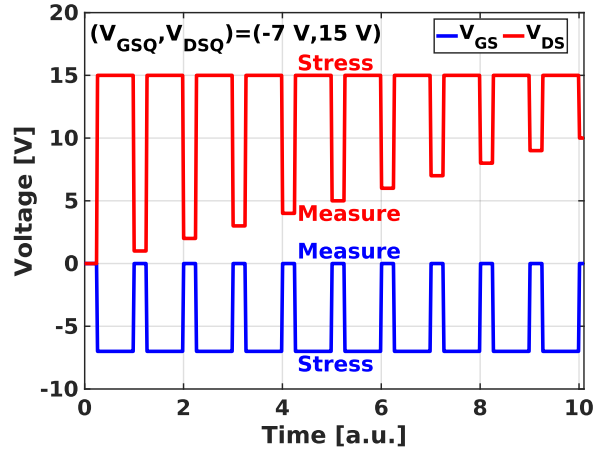


Figure 5.7: Pulsed measurement condition in the case of the hot pinch-off state (iii) $(-7 \text{ V}, 15 \text{ V})$ and the measurement for the case of $V_{GS} = 0 \text{ V}$. The same is valid for each quiescent state and V_{GS} measurement, performed at $T = 300 \text{ K}$. Measurements have a pulse width of 900 ns and a duty cycle of 1%. To improve readability, the time axis is expressed in arbitrary units and not to scale.

Four quiescent bias conditions were investigated, $(0 \text{ V}, 0 \text{ V})$ - zero-bias (reference) state, $(-7 \text{ V}, 0 \text{ V})$ - cold pinch-off, $(-7 \text{ V}, 15 \text{ V})$ - hot pinch-off, $(-7 \text{ V}, 30 \text{ V})$ - high-stress hot pinch-off.

Each pulse has a width of 9 ns (t_{meas}) and a duty cycle of 1 %, corresponding to a period of 900 ns (quiescent phase during $t_{\text{sq}} \approx 881 \text{ ns}$). These conditions ensure negligible self-heating and allow the device to preserve the quiescent-state equilibrium during the entire pulse train. The schematic timing diagram of the pulsed sequence is shown in Fig. 5.7 for the representative hot pinch-off condition $(-7, 15) \text{ V}$. The time axis is reported in arbitrary units (a.u.) for clarity, as the actual quiescent phase, lasting several orders of magnitude longer than the pulse width, is omitted for readability.

The pulsed measurements were used as the experimental reference for the subsequent TCAD transient simulations, which reproduce the same bias sequence to identify the underlying physical mechanisms of current collapse.

5.3.2 Experimental results and TCAD calibration

The experimentally measured pulsed output characteristics are reported in Fig. 5.8. To provide an alternative view of the data, the drain current I_D has been extracted as a function of the quiescent bias conditions both in the saturation region, at $V_{DS} = 10 \text{ V}$, and in the linear region, at $V_{DS} = 0.4 \text{ V}$, as shown in Fig. 5.9. These two extraction points enable the separate evaluation of the trapping effects influencing the channel

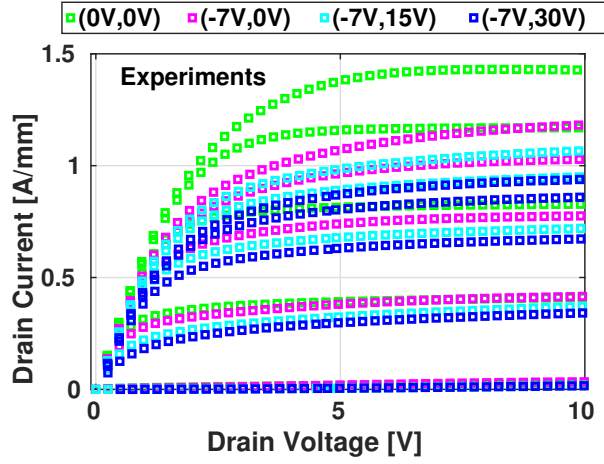


Figure 5.8: DC-IV experimental pulsed outputs data of $2 \times 25\text{-}\mu\text{m}$ AlGaN/GaN HEMTs, measured with a pulse width of 900 ns and a duty cycle of 1%. The devices were measured for a V_{GS} between -2 V and 2 V in steps of 1 V, at $T = 300\text{ K}$ [104], [88]

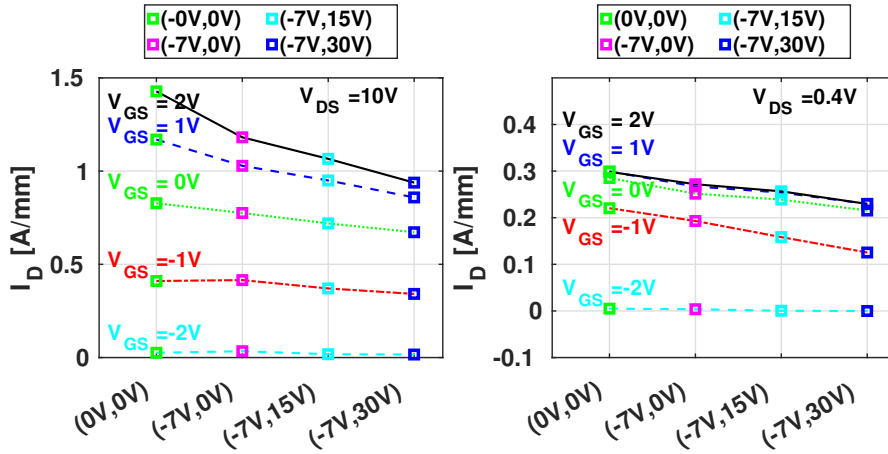


Figure 5.9: Left and Right: Experimental pulsed I_D extracted at $V_{DS} = 10\text{ V}$ and $V_{DS} = 0.4\text{ V}$ for each V_{GS} as function of the quiescent state, at $T = 300\text{ K}$.

access resistance and those impacting the overall current saturation. The first set of simulations reproduced these measurements under equivalent bias conditions, adopting the trap configuration previously calibrated in Section 5.2. Figure 5.10 reports the simulated pulsed output characteristics for the quiescent states $(0, 0)\text{ V}$, $(-7, 0)\text{ V}$, $(-7, 15)\text{ V}$, and $(-7, 30)\text{ V}$, for three V_{GS} values, for better clarity. The predicted drain-current collapse, visible in both the linear and saturation regions, highlights the role of two concurrent phenomena: (i) charge trapping in the channel region, which causes a reduction in the saturation current, and (ii) trapping in the gate-to-drain access region, which increases the dynamic R_{ON} . The TCAD results are in good agreement with experimental data, confirming the validity of the physical models

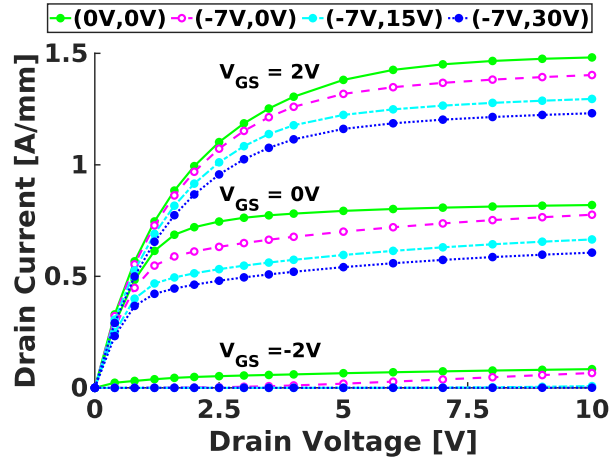


Figure 5.10: Pulsed DC-IV TCAD simulations of AlGaIn/GaN HEMT. The device V_{GS} ranging from -2 V to 2 V in steps of 2 V. The quiescent bias conditions, at $T = 300$ K are (0V, 0V), (-7V, 0V), (-7V, 15V) and (-7V, 30V), respectively. The predicted drain current collapse is in good agreement with the experimental trend.

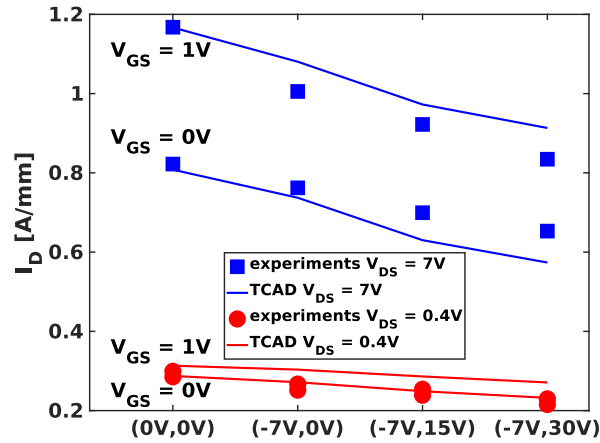


Figure 5.11: I_{DS} at two different V_{GS} in linear ($V_{DS} = 0.4$ V) and saturation ($V_{DS} = 7$ V) regimes, measured in the four different quiescent states, namely, the zero bias, the cold pinch-off and the hot pinch-off cases, at $T = 300$ K. The pulsed-stress cases show an increasing collapse, nicely predicted by the TCAD simulations in all regimes.

and the adopted trap configuration [104]. A direct comparison between simulated and experimental I_D values in the linear and saturation regions is shown in Fig. 5.11, where the drain current is plotted versus the quiescent bias condition for two gate voltages in both linear and saturation regions. Among the investigated configurations, the donor traps located at the SiN/GaN-cap interface remain inactive during pulsed operation due to their deep energy level ($E_t = E_C - 1.55$ eV), which prevents significant capture/emission events. Conversely, the Fe-related acceptor traps

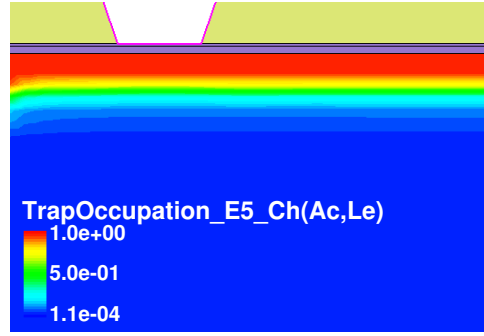


Figure 5.12: 2D plot of the occupation function for the Fe acceptor traps at the quiescent bias (0V, 0V), at $T = 300$ K. A uniform distribution is found corresponding to the equilibrium band configuration reported in Fig. 5.6b.

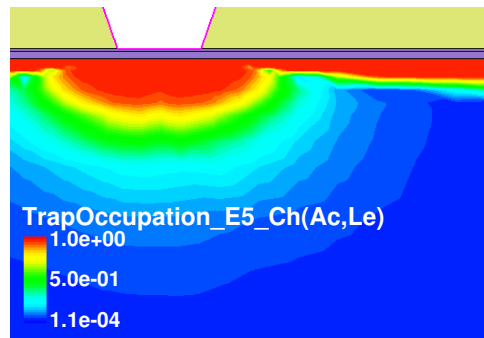


Figure 5.13: 2D plot of the occupation function for the Fe acceptor traps at the quiescent bias (-7V, 0V), at $T = 300$ K. The relevant contribution of the trapping under the gate is evident and clearly explains the dynamic on-resistance collapse in Fig. 5.10.

($E_t = E_C - 0.5$ eV) located in the GaN channel are the main contributors to the current collapse. Given the short pulse duration, these traps do not have sufficient time to release the captured charge, leading to a degradation of the drain current.

To better understand the physical origin of this degradation, the occupation probability of the Fe-related traps has been analyzed in the channel and access regions. As shown in Figs. 5.12-5.15, the trap occupation is uniform under the zero-bias condition, consistent with equilibrium band bending (Fig. 5.6a). At $(-7, 0)$ V, a localized increase in trap occupancy occurs beneath the gate, corresponding to charge capture during the off-state bias. When a drain bias is added, additional trap filling appears along the gate-to-drain access region, indicating that Fe-related traps are actively involved in the hot pinch-off collapse mechanism. These results provide a consistent physical interpretation of the dynamic I_D degradation observed experimentally, confirming that the Fe-related acceptor traps in the channel dominate the trapping phenomena responsible for current collapse and dynamic on-resistance degradation.

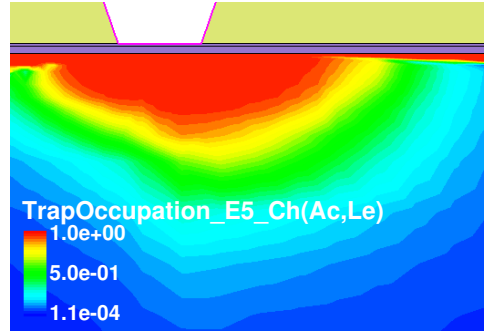


Figure 5.14: 2D plot of the occupation function for the Fe acceptor traps at the quiescent bias (-7V, 15V), at $T = 300$ K. A significant contribution of the trapping under the gate-to-drain region is evident in addition to the bulk trapping under the gate, in accordance with the current collapse in the saturation regime in Fig. 5.10.

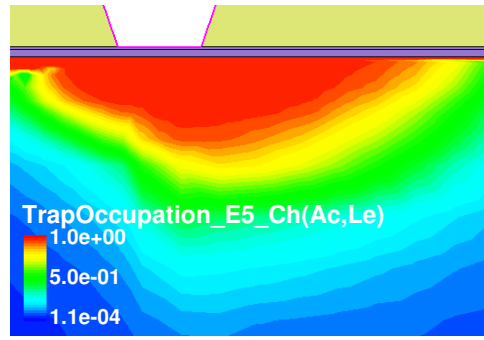


Figure 5.15: 2D plot of the occupation function for the Fe acceptor traps at the quiescent bias (-7V, 30V), at $T = 300$ K. The contribution of the trapping under the gate-to-drain region is similar to the case at (-7V, 15V) explaining the limited effects observed in the output curves in Fig. 5.10.

5.3.3 Separation of trapping contributions

To investigate in more detail both the iron and the surface traps contributions, an upgraded setup is built to perform faster simulations. Instead of the faithful reproduction of the pulsed analysis (computational intensive, see Fig. 5.7), a simplified test configurations, such as a single fast pulse following a quiescent bias phase, and the freezing of trap states prior to output characteristic extraction, were explored to reduce computational complexity and simulation time. Ultimately, the most efficient TCAD configuration implement a first 100s-long pre-biasing at the quiescent stress to reach the quasi-stationary state, followed by a single 9ns-long voltage I–V ramp. This simplified fast-ramp successfully replicates the faithful pulsed I–V TCAD curves while optimizing computational resources (simplified in Fig. 5.16, with a worst-case difference of less than 0.07%.

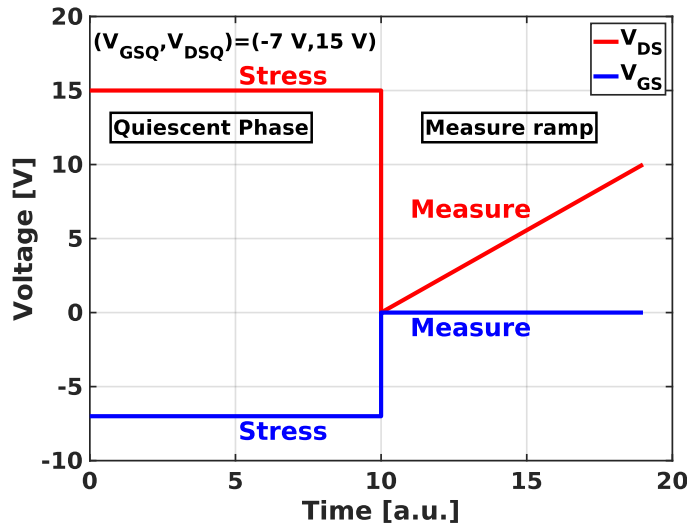


Figure 5.16: Most efficient pulsed simulation configuration in the case of the hot pinch-off condition (iii) (-7 V, 15 V) and the measurement of the $V_{GS} = 0$ V. The same is valid for each quiescent state and V_{GS} simulation, performed at $T = 300$ K. The simulation consists of a 100 s quiescent stress phase followed by a single 9 ns voltage pulse. To improve readability, the time axis is expressed in arbitrary units and not to scale.

The acceptor traps identifying the iron doping and donor traps at the SiN/GaN-cap interface are initially analyzed individually.

First, in the case of the Fe-acceptors, donor-like traps at the SiN/cap interface are replaced with a fixed positive charge equal to $+3.128 \times 10^{13} \text{ cm}^{-2}$, with the gate workfunction fixed to 6.93 eV. The simulated characteristics, shown in Fig. 5.17, point out the role of Fe traps on the I_D collapsing behaviors (previously commented in Subsection 5.3.2). Afterwards, analyses are carried out by varying the energy level of the donor traps between 1.55 eV and 0.35 eV from the conduction band, and their concentration from $5 \times 10^{13} \text{ cm}^{-2}$ to $3.25 \times 10^{13} \text{ cm}^{-2}$: the latter value is chosen well below the total polarization charge, thus it is no more able to pin E_C below the Fermi level for the 2DEG formation. In the latter analyses, in order to avoid variations of the 2DEG concentration and/or threshold voltage shifts, the barrier/channel piezoelectric activation and the gate workfunction are modified consistently. At the same time iron traps are eliminated to avoid their influence. The analyses are reported in the next subsection.

5.3.4 Energy and concentration dependence of donor traps

Afterwards, donor-like traps were reintroduced at the passivation-cap interface, while the Fe-related traps were intentionally removed to isolate the role of surface donors

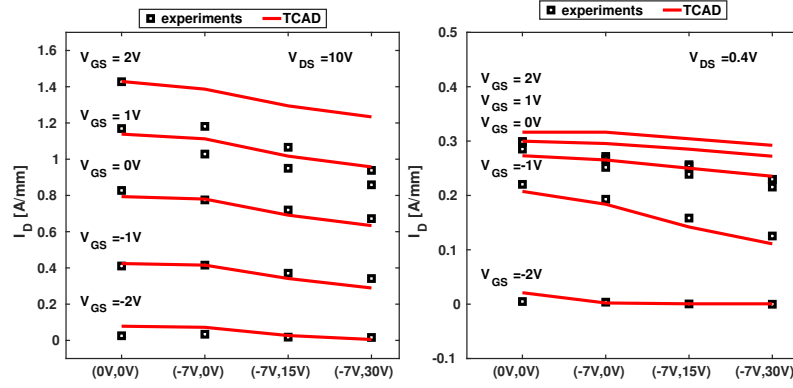


Figure 5.17: I_D in saturation ($V_{DS} = 10$ V) and linear ($V_{DS} = 0.4$ V) regimes, measured in the four quiescent bias states, at $T = 300$ K. The TCAD predictions show an increasing collapse due to the occupation increase of the iron-related acceptor traps in the channel layer (iron-tail). The (V_{GS}, V_{DS}) bias conditions influence the traps occupation trend in the gate and gate-drain regions (with the V_{DS} increase).

on the pulsed behavior. The analysis was conducted by varying both their concentration and energy level to evaluate the resulting effects under different quiescent stress conditions, as summarized in Fig. 5.18.

In the first set of simulations, the donor-trap concentration was swept from $5 \times 10^{13} \text{ cm}^{-2}$ down to $3.25 \times 10^{13} \text{ cm}^{-2}$, while keeping the energy position fixed at $E_t = E_C - 1.55 \text{ eV}$ (Fig. 5.18, left). To maintain consistency with the experimental 2DEG concentration at equilibrium, the polarization activation at the barrier–channel interface and the gate work function were slightly adjusted for each case, as summarized in Table 5.2. The reported results correspond to $V_{GS} = 2$ V, where the most pronounced effects are observed. To better highlight relative variations, the drain current I_D values are normalized to the $(0 \text{ V}, 0 \text{ V})$ condition, since the absolute current magnitude is strongly affected by the absence of bulk Fe traps in these simulations. In the second analysis, the donor energy level was varied while fixing the concen-

Energy Level	Concentration	Activation	Work Function
$E_t = E_C - 1.55 \text{ eV}$	$5.00 \times 10^{13} \text{ cm}^{-2}$	0.926	6.75 eV
	$4.00 \times 10^{13} \text{ cm}^{-2}$	0.928	6.75 eV
	$3.75 \times 10^{13} \text{ cm}^{-2}$	0.976	6.78 eV
	$3.50 \times 10^{13} \text{ cm}^{-2}$	0.978	6.80 eV
	$3.25 \times 10^{13} \text{ cm}^{-2}$	0.984	6.81 eV

Table 5.2: Donor-trap concentration at the passivation–cap interface, corresponding polarization activation at the barrier–channel interface, and gate work function used in the concentration-dependence analysis.

tration to $5 \times 10^{13} \text{ cm}^{-2}$. The same calibration procedure was adopted, adjusting

Concentration	Energy Level	Activation	Work Function
$5.00 \times 10^{13} \text{ cm}^{-2}$	$E_t = E_C - 1.55 \text{ eV}$	0.926	6.75 eV
	$E_t = E_C - 1.20 \text{ eV}$	0.916	6.40 eV
	$E_t = E_C - 1.00 \text{ eV}$	0.885	6.20 eV
	$E_t = E_C - 0.70 \text{ eV}$	0.792	5.90 eV
	$E_t = E_C - 0.35 \text{ eV}$	0.737	5.56 eV

Table 5.3: Donor-like trap energy levels at the passivation–cap interface, together with the corresponding polarization activation factors and gate work function values adopted in the energy-dependence analysis. The investigated trap energy range is motivated by the donor-related defect levels reported for SiN passivation layers, although the specific values are explored parametrically in this work [246].

polarization activation and gate work function, to preserve the experimental 2DEG concentration at equilibrium. The corresponding parameters are summarized in Table 5.3. Simulation results show that donor traps mainly affect the hot pinch-off conditions, with secondary influence under cold pinch-off when the donor energy level approaches 0.7–0.8 eV below the conduction band. This behavior can be explained by considering that very deep donor traps are barely affected by the gate negative bias, whereas shallower states become more responsive to V_{GS} , leading to enhanced trap discharge and a more pronounced current collapse. In this simplified analysis, each case assumes a single discrete trap level to capture first-order effects; a broader energy distribution would require another dedicated experimental characterization, which lies beyond the scope of the present study.

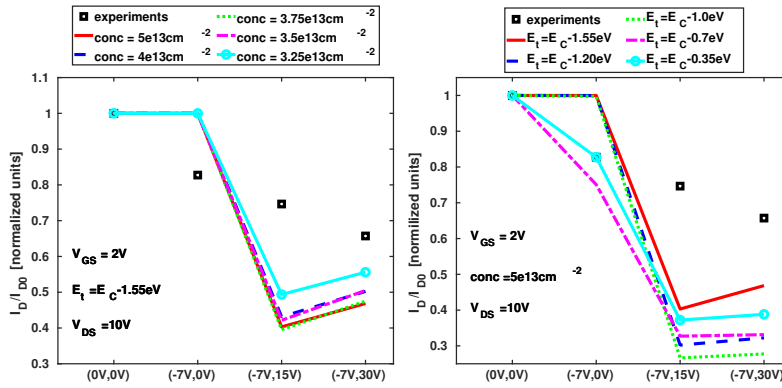


Figure 5.18: Normalized drain current I_D in the saturation regime ($V_{DS} = 10 \text{ V}$, $V_{GS} = 2 \text{ V}$) under the four quiescent bias conditions, at $T = 300 \text{ K}$. TCAD simulations excluding Fe-related traps are compared for different donor-trap concentrations (left) and energy levels (right). Black symbols: experiments. Donor traps exhibit a strong impact under hot pinch-off, while shallower levels also affect cold pinch-off due to shorter capture times and higher electron density in the cap layer.

Donor Concentration	Donor Energy Level	Activation	Work Function	Iron Energy Level
$5 \times 10^{13} \text{ cm}^{-2}$	$E_t = E_C - 0.8 \text{ eV}$	0.85	6.1 eV	$E_t = E_C - 0.5 \text{ eV}$

Table 5.4: Final parameters of the best-case TCAD configuration: donor-trap concentration and energy level at the passivation–cap interface, polarization activation at the barrier–channel interface, gate work function, and iron-trap energy level.

5.3.5 Best-case TCAD setup

Finally, both types of traps, Fe-related acceptors in the GaN channel and donor-like states at the passivation–cap interface, were included simultaneously in the simulation framework. The combined configuration revealed a mutual interaction between the two mechanisms. The presence of Fe-induced negative charge effectively mitigates the strong influence of surface donor traps under both cold and hot pinch-off conditions. In particular, the iron-related traps stabilize the positive charge state of donor traps during stress, thus reducing excessive discharge and improving overall agreement with experiments.

The simulation results indicate that Fe-related traps mainly contribute to the threshold-voltage (V_{th}) shift under cold pinch-off, while both trap types influence the dynamic on-resistance (R_{ON}) degradation under hot pinch-off conditions (Figs. 5.19 and 5.20). This complementary behavior confirms that channel and surface traps act together to determine the transient response of the device, with their interplay depending on the specific bias regime.

The full calibration process involved the fine-tuning of the polarization activation at the barrier–channel interface, the gate work function, and the effective electron tunneling mass. The final parameter set, corresponding to the best agreement with experimental pulsed I–V data, is summarized in Table 5.4.

Overall, the calibrated TCAD configuration provides a consistent representation of both the static and dynamic device behavior, capturing the essential interaction between bulk and surface trapping phenomena that govern current collapse and bias-dependent degradation in AlGaIn/GaN HEMTs.

These results complete the trapping investigation under pulsed operation, establishing a calibrated TCAD framework capable of reproducing dynamic behavior with high accuracy. In the following section, the same setup is extended to the HTRB step-stress regime, in order to assess long-term degradation mechanisms and their correlation with the transient effects discussed above.

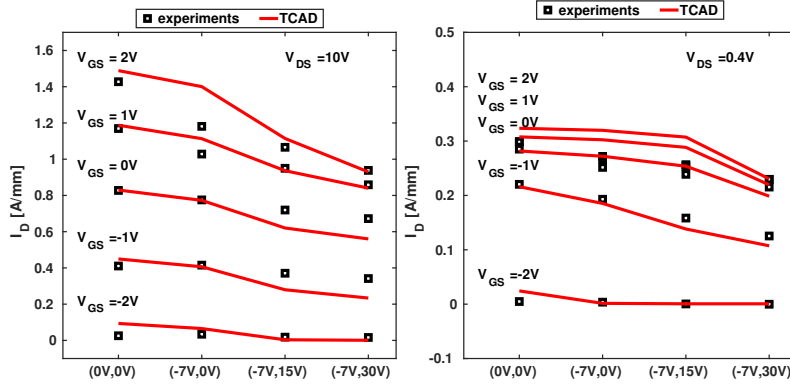


Figure 5.19: Drain current I_D in the saturation ($V_{DS} = 10$ V) and linear ($V_{DS} = 0.4$ V) regimes under the four quiescent bias conditions, at $T = 300$ K. The combined effect of donor traps at the SiN/cap interface and Fe-related acceptors in the channel (parameters in Table 5.4) results in minimal detrapping at cold pinch-off for $V_{GS} = 2$ V, while achieving very good agreement across all bias conditions for lower V_{GS} values.

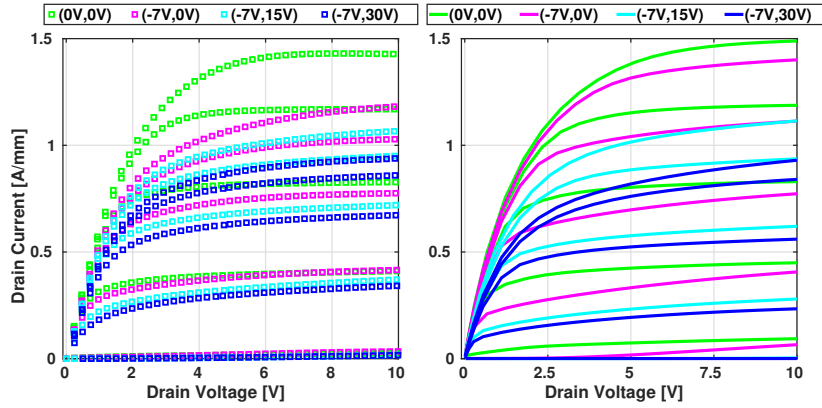


Figure 5.20: Left: experimental I_D measured under four quiescent bias conditions for gate voltages between -2 V and 2 V in 1 V steps, at $T = 300$ K [88], [104]. Right: simulated I_D under the same conditions using the best-case configuration reported in Table 5.4. The residual mismatch at cold pinch-off reveals a limited detrapping effect mainly at $V_{GS} = 2$ V, whereas excellent overall agreement is achieved for lower gate biases.

5.4 HTRB Step-Stress Analysis

5.4.1 Experimental procedure and simulation setup

The accelerated degradation analysis was carried out under HTRB step-stress conditions. During the test, the gate voltage was kept constant at $V_{GS} = -7$ V, while the drain voltage V_{DS} was progressively increased from 0 V up to 120 V in 2 V increments, at a temperature of 398.15 K (125°C). Each voltage step consisted of a

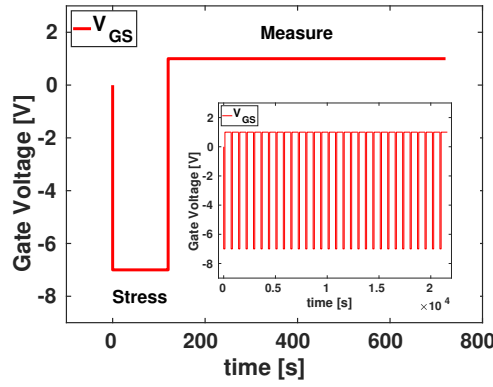


Figure 5.21: Gate voltage during the HTRB analysis. A 120 s stress phase is executed at -7 V, at $T = 398$ K, followed by the measurement of the $I_{D,ss}$, carried out with $V_{GS} = 1$ V, at $T = 323$ K. This is repeated for each stress cycle until V_{DS} reaches $V_{max} = 120$ V (60 cycles). Inset: half train of 30 cycles.

2-minute stress period, followed by a 10-minute electrical characterization phase, as schematically illustrated in Figs. 5.21 and 5.22.

The drain current in saturation, $I_{D,ss}$, was monitored at $V_{GS} = 1$ V and $V_{DS} = 7$ V, at $T = 323.15$ K to track device degradation throughout the stress sequence. Although the adopted step-stress HTRB procedure does not strictly conform to standard JEDEC reliability protocols [247], it represents an effective on-wafer accelerated testing approach [224], capable of revealing degradation trends within a reduced experimental timeframe. Despite the relatively short total duration of approximately 12 hours, the test provides meaningful insight into the main degradation mechanisms and their evolution under progressive reverse-bias stress.

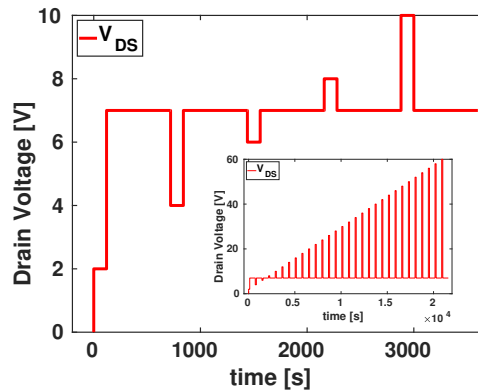


Figure 5.22: Drain voltage during the HTRB analysis. Starting from 0 V, V_{DS} is increased with 2 V step till $V_{max} = 120$ V (full train of 60 cycles) during the stress phases performed at $T = 398$ K. In the measuring phase, V_{DS} is kept at 7 V, at $T = 323$ K. Inset: half train of 30 cycles.

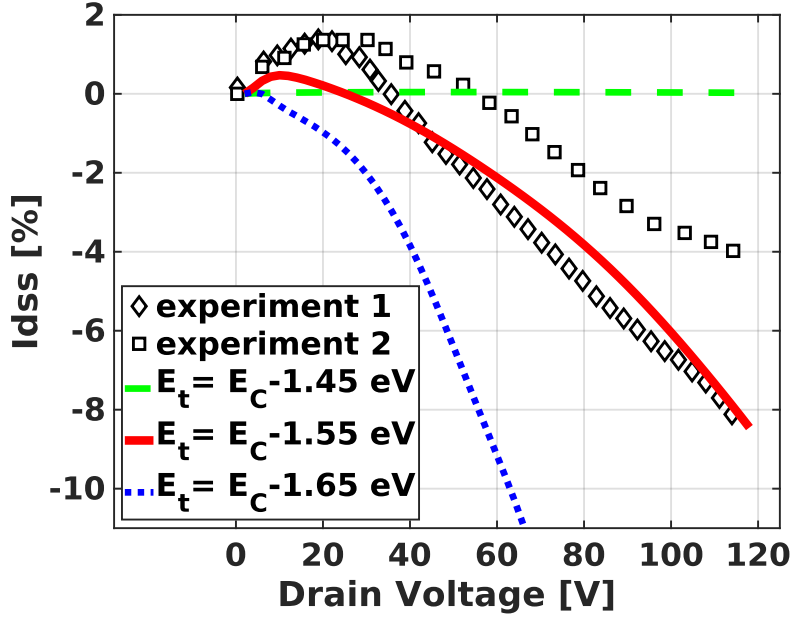


Figure 5.23: HTRB $I_{D,ss}$ percentage change for different Donor energies at SiN/GaN-Cap interface. The $I_{D,ss}$ current is measured at the conditions $V_{GS} = 1$ V, $V_{DS} = 7$ V, at $T = 323$ K, after the applied stress condition.

5.4.2 Experimental results and TCAD correlation

In the HTRB step-stress analysis, the degradation of the saturation drain current ($I_{D,ss}$) is primarily attributed to the charging and discharging dynamics of pre-existing traps located both in the GaN buffer and at the passivation/GaN-cap interface. Figure 5.23 reports the simulated relative variation of $I_{D,ss}$, extracted at $V_{GS} = 1$ V and $V_{DS} = 7$ V, for three different donor-trap energy levels at the SiN/GaN-cap interface, compared with the experimental data obtained from two devices (labeled as: "experiment 1" and "experiment 2"). The selected donor-trap energy range follows the state-of-the-art indications from [248]. No significant contribution was observed from Fe-related acceptor traps in the GaN buffer, as the measurement phase between stress steps was sufficiently long to ensure full recovery of their initial occupation state. Conversely, interface donor traps exhibited a clear influence on the $I_{D,ss}$ evolution depending on their energy depth. When located at $E_t = E_C - 1.45$ eV, their behavior resembled that of Fe-related traps, leading to negligible degradation. For deeper energy levels, however, a distinct decrease in $I_{D,ss}$ was observed, in close agreement with the experimental data.

At the early stress stages ($V_{DS} \leq 20$ V), a slight increase in $I_{D,ss}$ was detected before the onset of degradation. This transient enhancement can be ascribed to the

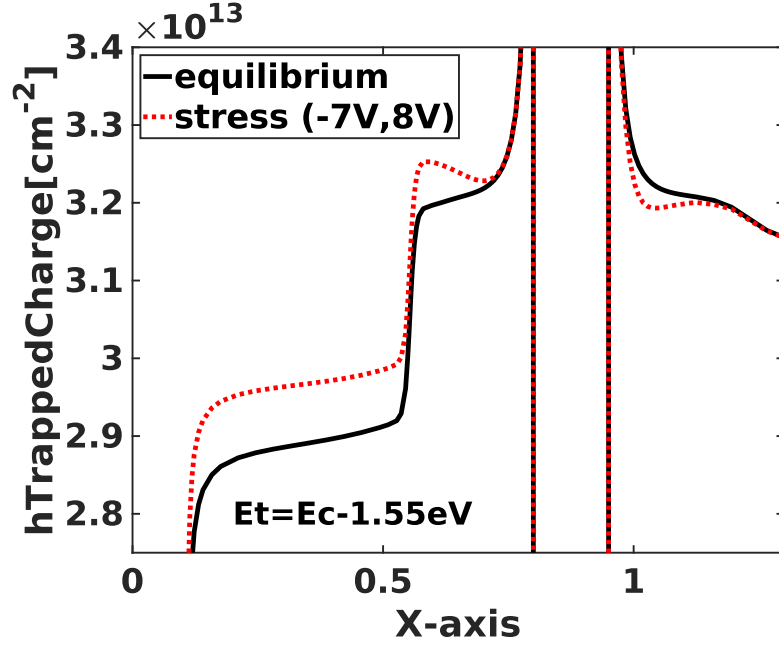


Figure 5.24: Trapped hole charge at the SiN/GaN-Cap interface shown at the $I_{D,ss}$ conditions: $V_{GS} = 1$ V, $V_{DS} = 7$ V, at $T = 323$ K after the equilibrium condition ($V_{GS} = V_{DS} = 0$ V), and after the stress condition ($V_{GS} = -7$ V, $V_{DS} = 8$ V), at $T = 323$ K. $E_t = E_C - 1.55$ eV.

accumulation of positive charge at the passivation/cap interface in the gate–source region, as illustrated in Fig. 5.24 for the stress condition ($V_{GS} = -7$ V, $V_{DS} = 8$ V). A comparison between the equilibrium condition ($(0, 0)$ V) and the stressed state confirms the formation of positive trapped charge near the gate edge, effectively reducing both the threshold voltage and the gate–source resistance.

At higher stress voltages, the dominant degradation mechanism shifts toward the gate–drain region, where donor-trap occupation and subsequent detrapping processes govern the observed current reduction. This behavior is evident in Figs. 5.25 and 5.26, which show the spatial distribution of trapped charge at equilibrium and after the final stress step ($V_{DS} = 120$ V), respectively. The simulations reveal that deeper donor levels enhance the hole detrapping rate along the gate–drain path, leading to a pronounced reduction of the 2DEG density in this region. As a consequence, a clear degradation of $I_{D,ss}$ is observed for the deepest traps, consistent with the experimental trends shown in Fig. 5.23.

5.4.3 Parameter sensitivity analyses

To gain deeper insight into the degradation mechanisms associated with interface traps, three complementary parameter analyses were performed.

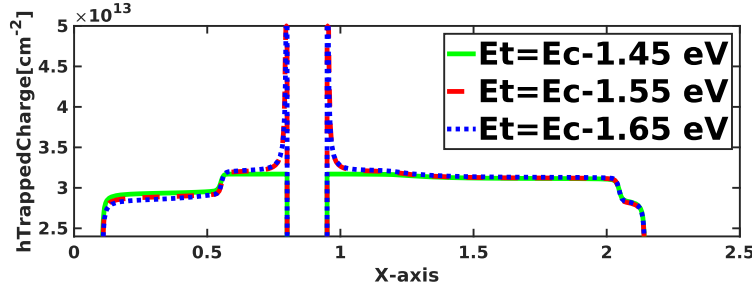


Figure 5.25: Trapped hole charge at the SiN/GaN-Cap interface for different energies shown at the $I_{D,ss}$ conditions: $V_{GS} = 1$ V, $V_{DS} = 7$ V, after the equilibrium condition ($V_{GS} = V_{DS} = 0$ V), at $T = 323$ K.

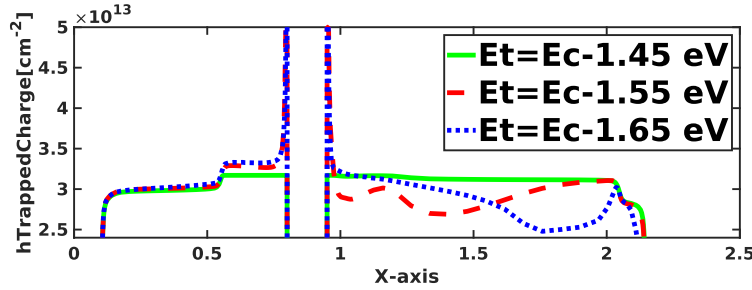


Figure 5.26: Trapped hole charge at the SiN/GaN-Cap interface for different energies shown at the $I_{D,ss}$ conditions: $V_{GS} = 1$ V, $V_{DS} = 7$ V, after the last stress condition ($V_{GS} = -7$ V, $V_{DS} = 120$ V), at $T = 323$ K.

First, the influence of donor-trap concentration (N_D) at the passivation/cap interface was examined. The trap concentration was varied together with the piezoelectric polarization charge to preserve the equilibrium 2DEG concentration, while keeping the trap energy level fixed at $E_t = E_C - 1.55$ eV. This approach allowed the identification of how the trapped positive charge evolves during HTRB stress when only the trap density is modified.

Second, the donor-trap E_t was varied, while N_D was simultaneously adjusted to maintain the same 2DEG equilibrium value. In this case, the piezoelectric activation was kept constant, isolating the effect of trap depth on charge trapping and detrapping under high-field stress. This analysis provides direct evidence of how shallower traps contribute to faster detrapping dynamics compared to deeper ones, which tend to retain charge over longer stress intervals.

Finally, the impact of the gate tunneling effective mass (m_{te}) was investigated. This parameter critically affects the gate leakage current (I_G) by modulating electron tunneling through the Schottky barrier during the OFF-state phase of HTRB. Changes in m_{te} thus influence the injected charge in the gate region and indirectly affect the 2DEG concentration and the corresponding $I_{D,ss}$ variation.

The simulated $I_{D,ss}$ and I_G trends were compared with experimental data from

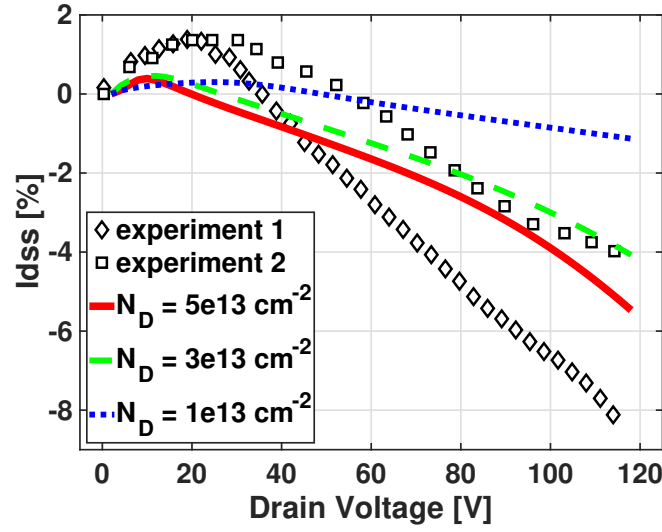


Figure 5.27: Percentage change in HTRB $I_{D,ss}$ for different donor concentrations at the SiN/GaN-Cap interface, with simultaneous variation of the piezoelectric charge to maintain a fixed 2DEG concentration. Measurement conditions: $V_{GS} = 1$ V, $V_{DS} = 7$ V, at $T = 323$ K.

two representative HEMTs ("experiment 1" and "experiment 2"), enabling a clear correlation between stress-induced electrical shifts and the underlying physical mechanisms responsible for long-term degradation.

Effect of donor concentration

The impact of donor-trap concentration (N_D) at the passivation/cap interface on device degradation during HTRB stress is illustrated in Figs. 5.27 and 5.28. A slight initial increase in $I_{D,ss}$ (about 1.36–1.37%) is observed for V_{DS} values up to 20 V, followed by a progressive degradation at higher stress voltages. Beyond this regime, the $I_{D,ss}$ decrease is primarily driven by donor detrapping along the gate–drain access region (Fig. 5.29), which reduces the local 2DEG density. Since the gate current (I_G) remains nearly constant during stress, the degradation is attributed to 2DEG modulation rather than changes in leakage behavior. In this context, I_G itself may act as the electron supply that neutralizes positively charged donor states, leading to the observed I_D collapse. This interpretation is supported by both experimental and simulated data, which consistently reproduce the same trend across all analyzed devices.

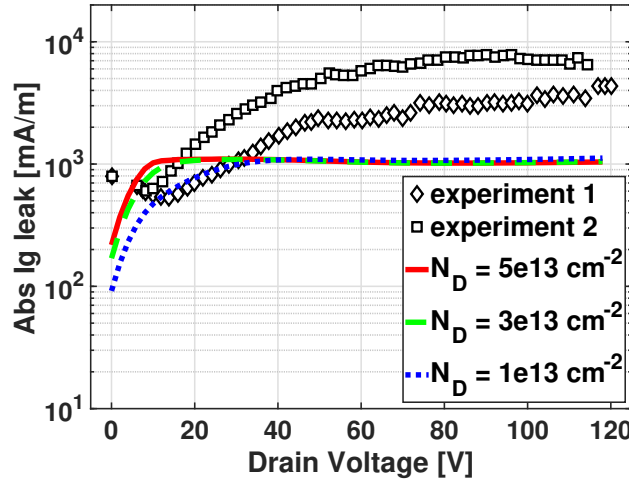


Figure 5.28: Absolute I_G leakage in HTRB for different donor concentrations at the SiN/GaN-Cap interface, with simultaneous variation of the piezoelectric charge to maintain a fixed 2DEG concentration. Measurement conditions: $V_{GS} = 1$ V, $V_{DS} = 7$ V, at $T = 323$ K.

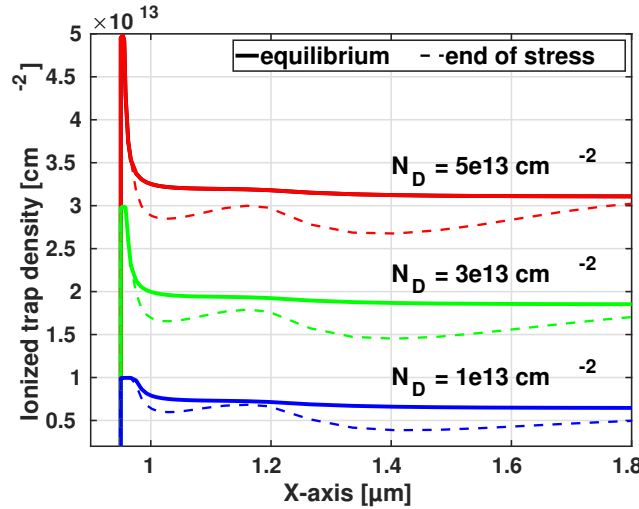


Figure 5.29: Ionized donor trap density at the SiN/GaN-Cap interface under equilibrium (solid lines) and after the final step-stress condition at $V_{DS} = 120$ V (dashed lines) for three different donor concentrations (N_D). Measurement conditions: $V_{GS} = 1$ V, $V_{DS} = 7$ V, at $T = 323$ K. The simulations were performed while varying the piezoelectric activation to maintain a constant 2DEG concentration at equilibrium.

Effect of donor energy level

The influence of the donor-trap energy level on the degradation behavior during HTRB stress is presented in Figs. 5.30 and 5.31. A clear dependence emerges between the trap depth and the severity of current degradation: the deeper the donor level, the stronger the detrapping effect and the more pronounced the reduction of $I_{D,ss}$ (Fig. 5.32). This behavior reflects the slower emission dynamics of deep states,

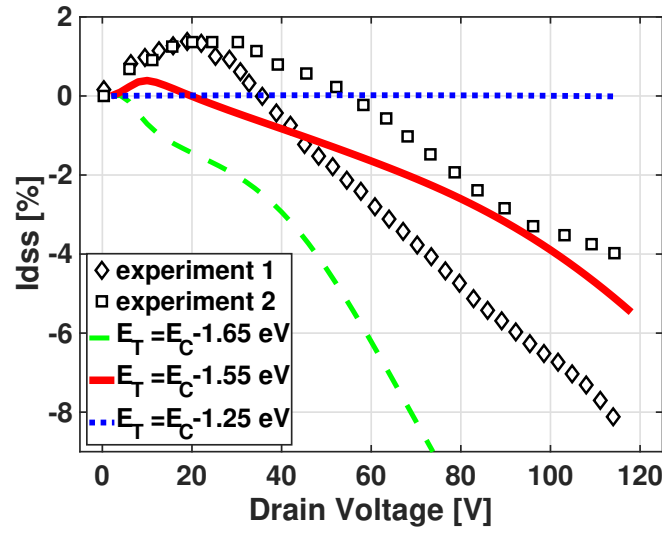


Figure 5.30: Percentage change in HTRB $I_{D,ss}$ for different donor trap energy levels at the SiN/GaN-Cap interface. The donor concentration is simultaneously varied to maintain a fixed 2DEG concentration, with the piezoelectric polarization activation kept unchanged. Measurement conditions: $V_{GS} = 1$ V, $V_{DS} = 7$ V, at $T = 323$ K.

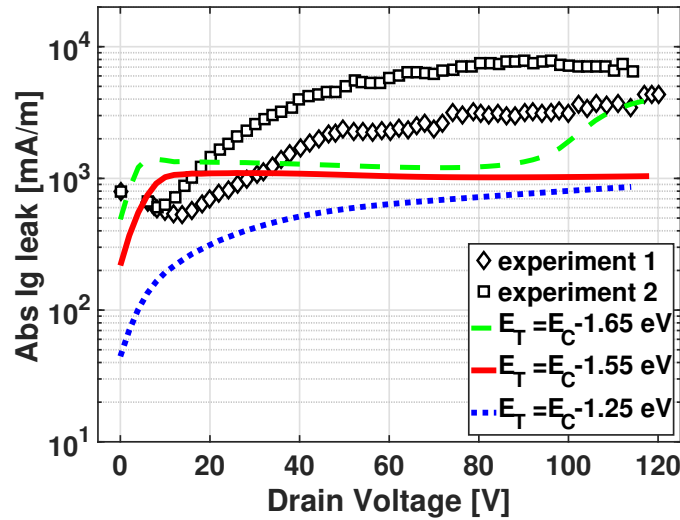


Figure 5.31: Absolute I_G leakage in HTRB for different donor trap energy levels at the SiN/GaN-Cap interface. The donor concentration is simultaneously varied to maintain a fixed 2DEG concentration, with the piezoelectric polarization activation kept unchanged. Measurement conditions: $V_{GS} = 1$ V, $V_{DS} = 7$ V, at $T = 323$ K.

which retain charge longer and thus induce stronger 2DEG depletion under high electric fields.

In particular, as V_{DS} increases, the lateral electric field promotes enhanced donor detrapping along the gate–drain path, widening the depletion region and leading to a larger current collapse due to R_{ON} increase. Conversely, shallower traps—being

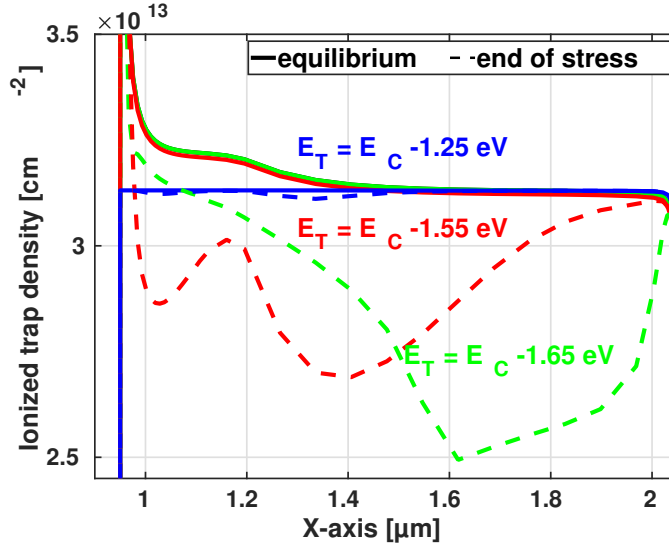


Figure 5.32: Ionized donor trap density at the SiN/GaN-Cap interface under equilibrium (solid lines) and after the final step-stress condition at $V_{DS} = 120$ V (dashed lines) for three different donor E_t . The analysis was conducted while varying the donor concentration to maintain a constant 2DEG concentration at equilibrium, with the piezoelectric polarization activation kept unchanged. Measurement conditions: $V_{GS} = 1$ V, $V_{DS} = 7$ V, at $T = 323$ K.

more easily discharged—produce a lower net positive charge near the channel edges (Fig. 5.32), slightly reducing I_G and resulting in a better match with the experimental gate-current trend (Fig. 5.31). However, despite the improved reproduction of I_G , this configuration does not fully capture the experimentally observed degradation in $I_{D,ss}$, indicating that additional charge-trapping mechanisms may contribute under long-term HTRB stress.

Influence of Gate Injection on Stress-Induced Degradation

The evolution of the gate current (I_G) during HTRB stress plays a crucial role in determining the overall degradation behavior. To investigate this effect, the effective electron tunneling mass (m_{te}) at the Schottky gate barrier was varied, directly influencing the tunneling probability and hence the injected electron current. Simulations indicate that lowering m_{te} enhances electron tunneling through the barrier, leading to an increased I_G during stress (Fig. 5.34).

A higher gate current improves the local charge neutrality in the gate–drain access region by supplying electrons that compensate positively charged donor states, thereby reducing donor detrapping and mitigating $I_{D,ss}$ degradation. This correlation is consistent with the experimental observations shown in Figs. 5.33 and 5.34, where

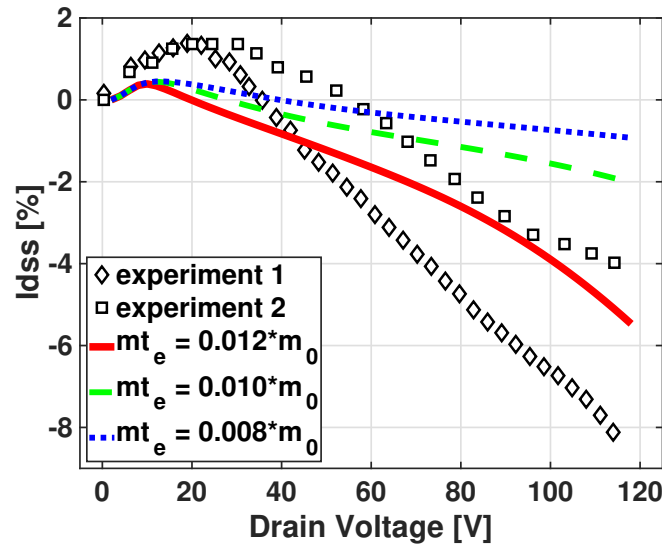


Figure 5.33: Percentage change in HTRB $I_{D,ss}$ for three different tunneling effective masses (m_{te}) at the Schottky gate contact. Donor traps are fixed at $E_T = E_C - 1.55$ eV with a concentration of $5 \times 10^{13} \text{ cm}^{-2}$, and no variations were applied to the trap conditions or the piezoelectric polarization activation. Measurement conditions: $V_{GS} = 1$ V, $V_{DS} = 7$ V, at $T = 323$ K.

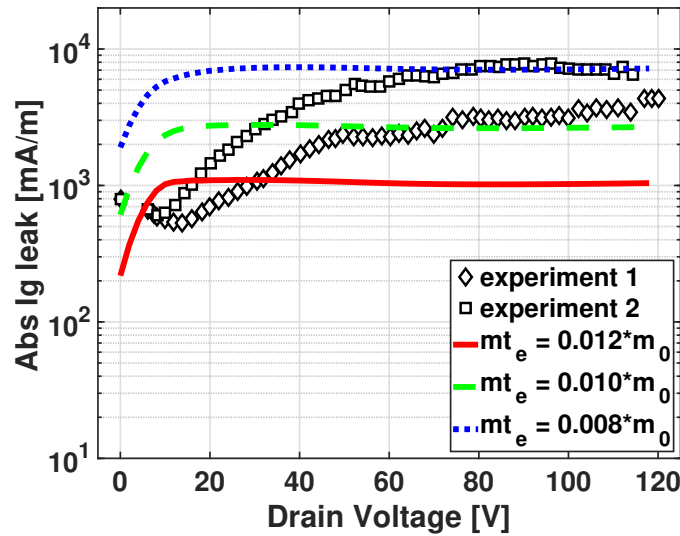


Figure 5.34: Absolute I_G leakage in HTRB for three different tunneling effective masses (m_{te}) at the Schottky gate contact. Donor traps are fixed at $E_T = E_C - 1.55$ eV with a concentration of $5 \times 10^{13} \text{ cm}^{-2}$, and no variations were applied to the trap conditions or the piezoelectric polarization activation. Measurement conditions: $V_{GS} = 1$ V, $V_{DS} = 7$ V, at $T = 323$ K.

devices exhibiting larger gate leakage also display reduced current collapse under HTRB stress (Fig. 5.35).

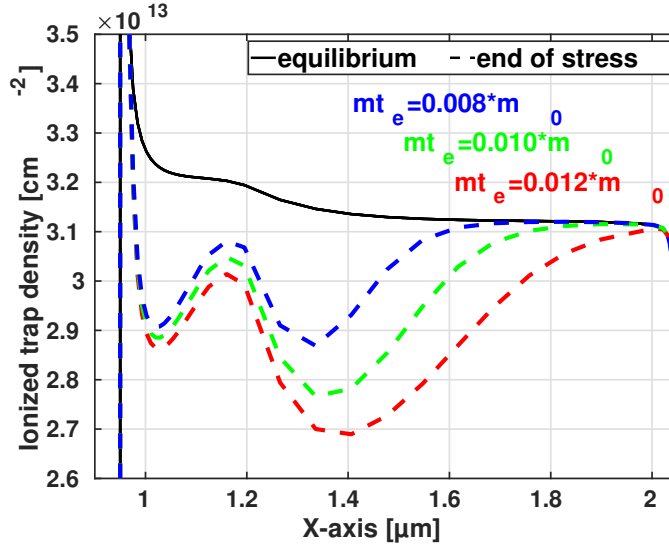


Figure 5.35: Ionized donor trap density at the SiN/GaN-Cap interface under equilibrium (solid lines) and after the final step-stress condition at $V_{DS} = 120$ V (dashed lines) for three different tunneling effective masses (m_{te}) at the Schottky gate contact. Measurement conditions: $V_{GS} = 1$ V, $V_{DS} = 7$ V, at $T = 323$ K. The donor traps are fixed at $E_T = E_C - 1.55$ eV with a concentration of $5 \times 10^{13} \text{ cm}^{-2}$, and no variations were applied to either the trap conditions or the piezoelectric polarization activation.

5.5 On TCAD Reliability and Parameter Sensitivity

Identifying a single and universal parameter set that accurately reproduces both the experimental drain and gate current behaviors under HTRB stress remains a challenging task. This intrinsic difficulty partly explains the skepticism that often surrounds TCAD-based reliability analyses. Nevertheless, overlooking these approaches would mean missing a powerful opportunity to extract deeper physical insights and to reveal consistent correlations across different stress regimes, particularly when experimental data and simulations are cross-referenced, thereby ensuring the reliability of the obtained results. However, every technology requires its own specific fine-tuning, given the still-maturing nature of GaN device technology. Despite this, the results obtained here demonstrate that the underlying physical trends remain consistent across different GaN HEMT platforms.

These considerations form the basis for the comparative discussion presented in the next section, where the interplay between interface, barrier, and buffer traps is critically examined in light of both short- and long-term stress behaviors.

5.6 Discussion

The comprehensive TCAD calibration performed throughout this work enabled a consistent interpretation of both pulsed and HTRB stress data. By combining calibrated transport, polarization, and trap parameters, the simulated devices successfully reproduced the measured transfer, output, and pulsed I–V characteristics as well as the degradation trends observed during HTRB testing. This validation confirms that the adopted physical framework and parameterization are capable of accurately capturing the main degradation mechanisms in AlGaIn/GaN HEMTs.

Under pulsed operation, the degradation originates primarily from the dynamic trapping of electrons in deep Fe-related acceptor states located within the GaN buffer and channel regions. The trap capture time is mainly governed by the local electron concentration in the affected region, whereas the emission time strongly depends on the trap energy level, in this case resulting in much longer emission than capture time. As a consequence, these deep traps, whose emission time constants exceed the actual t_{meas} of the pulsed measurement, act as electron capture centers during the off-state bias and are only partially discharged during the short pulse intervals. This incomplete detrapping leads to drain current collapse and an increase in dynamic on-resistance. In contrast, donor-like traps at the SiN/GaN-cap interface—although less responsive to short stress times, become increasingly relevant under high-field conditions, where their partial charging alters the surface potential and the 2DEG density. The simultaneous presence of both trap types produces a self-compensating electrostatic effect: negatively charged Fe traps mitigate the impact of donor states, improving agreement between simulated and measured pulsed data. This interplay between bulk and surface traps proves essential for reproducing the full dynamic behavior of the device.

During HTRB stress, the degradation mechanism shifts from transient trapping to field-assisted detrapping. In this regime, Fe-related acceptor traps in the buffer are fully recovered between stress cycles, whereas donor-like interface traps dominate the degradation process. The depth and concentration of these donor states critically influence the evolution of the drain current degradation, with deeper traps producing more severe 2DEG depletion along the gate–drain access region. Electron injection from the gate electrode at the SiN/cap interface reduces the population of ionized donor traps due to the combined effects of high electric field, elevated temperature, and prolonged stress duration, which enhance the neutralization of positively charged donor states in the gate–drain access region. Additionally, the gate current plays a decisive role: increasing electron injection through a lower tunneling effective mass

alleviates the donor detrapping process, thereby reducing the observed $I_{D,ss}$ degradation. This mechanism suggests that proper engineering of the gate Schottky barrier and optimization of the interface quality can be exploited to improve device reliability under reverse-bias stress.

Beyond the specific degradation mechanisms discussed above, two key technological insights can be drawn from the overall analysis. (i) Minimizing Fe diffusion or contamination tails within the channel region is essential to mitigate dynamic current collapse [79], [80]. (ii) Improving the passivation/cap interface, by reducing the donor trap density and tailoring their energy distribution, together with a careful optimization of the gate barrier properties (which directly affect I_G) can significantly enhance device stability and long-term reliability [172], [248]. In this study, single discrete energy levels were deliberately adopted for both donor and Fe-related traps to maintain a transparent and physically traceable modeling framework. While more realistic continuous trap energy distributions could be introduced, they would require complementary experimental datasets, such as DLTS or dispersive C-V measurements, to properly constrain the parameter space.

These considerations bridge the microscopic trapping mechanisms with practical design guidelines, forming a consistent picture of how material quality, interface engineering, and gate design jointly determine the device degradation trends under stress.

Overall, the analyses presented in this chapter demonstrate that the combined modeling of Fe-induced acceptor traps and donor-like interface states is indispensable for a physically consistent description of AlGaIn/GaN HEMT degradation. While Fe traps govern short-term dynamic effects such as current collapse, donor traps control the long-term evolution under HTRB stress. The TCAD framework developed here therefore provides a robust foundation for predictive reliability modeling and for future optimization of trap-related design parameters. These findings are further consolidated in the following summary section.

5.7 Summary

This chapter presented a comprehensive TCAD framework for the electrical and reliability characterization of AlGaIn/GaN HEMTs. The model was calibrated against experimental DC, pulsed, and HTRB data, enabling a physically consistent description of the trapping and detrapping phenomena governing device degradation. Through systematic parameter variations, the respective roles of Fe-related acceptor traps in the channel/buffer and donor-like interface traps at the passivation/cap interface were

identified and quantitatively assessed. The analyses revealed how trap energy levels and concentrations modulate current collapse, and gate leakage behavior under different bias and field conditions. Overall, the developed framework provides a robust reference for understanding the interplay between interface and bulk trapping phenomena in GaN-based HEMTs, laying the groundwork for the comparative study presented in the next chapter.

Chapter 6

AlScN/GaN HEMTs: Modeling, Performance Evaluation, and Comparison with AlGaN Counterparts

Chapter overview

This chapter investigates the reliability of AlScN/GaN high-electron-mobility transistors (HEMTs) through a combined experimental and TCAD-based approach. Two complementary stress regimes are analyzed: pulsed I–V characterization, which probes charge-trapping dynamics under controlled quiescent conditions, and step-stress HTRB testing, which accelerates long-term degradation mechanisms. Beyond reproducing the experimental trends, the calibrated TCAD framework is employed to disentangle and quantify the individual contributions of V_{th} shift, g_m degradation, and gate-leakage evolution to the overall I_D collapse. Finally, the obtained results are benchmarked against an AlGaN/GaN reference technology, clarifying the performance–reliability trade-offs introduced by the AlScN barrier and providing physical insights for next-generation device optimization.

6.1 Introduction

As discussed in Chapter 5, the reliability of AlGaN/GaN HEMTs is strongly influenced by charge trapping phenomena occurring at the passivation/barrier interface and within the channel/buffer regions. While the results seen in the previous chapter establish a detailed understanding of degradation under pulsed and HTRB stress conditions, the search for enhanced performance has recently shifted attention towards alternative barrier materials capable of offering higher polarization and improved electrostatics [249].

GaN HEMTs have consolidated their role as a key enabling technology for high-frequency and high-power applications, including RF amplification and power conversion [43], [201], [202]. Their success stems from the combination of a wide bandgap, a high critical electric field, and the formation of a high-density 2DEG at polar heterointerfaces, which together enable high breakdown voltages, fast switching speeds, and superior power efficiency [204], [205], [206].

Over the past decade, extensive research has focused on barrier engineering to further improve the performance and scalability of GaN-based HEMTs. Among the explored materials, aluminum scandium nitride (AlScN) has recently emerged as a promising alternative to the conventional AlGaN barrier [250], [249], [251], [252], [253], [254], [42], [255]. The incorporation of scandium into AlN substantially enhances both spontaneous and piezoelectric polarization, enabling a larger polarization-induced charge at the heterointerface and thus a higher 2DEG density. Reported sheet carrier concentrations reach up to $5 \times 10^{13} \text{ cm}^{-2}$, which translates into higher saturation current and improved transconductance [41], [94], [98], [99]. Additionally, the possibility of near lattice matching to GaN makes AlScN an attractive choice for mitigating strain-related degradation. Nevertheless, these benefits come with technological challenges. The incorporation of scandium tends to increase alloy and interface scattering, reducing carrier mobility. To counteract this effect, a thin AlN interlayer is often introduced between the AlScN barrier and the GaN channel, balancing the trade-off between 2DEG enhancement and transport degradation [170]. While promising DC performance metrics have been reported, the long-term reliability and degradation mechanisms of AlScN/GaN HEMTs remain largely unexplored. In particular, the relative impact of buffer defects, interface traps, and gate-stack leakage under realistic operating conditions is still unclear [104], [88], [89].

In this framework, understanding the reliability of AlScN barriers becomes critical for their industrial adoption. Two complementary stress methodologies are employed to investigate device stability: (i) pulsed I-V characterization, which probes

trapping and detrapping dynamics under controlled quiescent conditions and suppresses the contribution of ultra-fast traps through a double-pulse technique [256], [257], [258] and (ii) accelerated HTRB step-stress testing, which emulates long-term stress evolution through successive voltage increments, providing a rapid yet representative assessment of degradation trends. While the former captures the transient redistribution of trapped charge within the device, the latter reveals cumulative degradation effects driven by electric field and temperature acceleration. The device under study was fabricated by an external industrial partner, which also provided the discussed experimental characterization data used in this work for model calibration and analysis.

Building upon the modeling framework established in Chapters 1-3 and the reliability analysis developed for AlGaIn barriers in Chapter 5, this chapter develops and validates a comprehensive TCAD simulation strategy for AlScN/GaN HEMTs, capable of reproducing both pulsed and HTRB experimental data. The model incorporates the distinct polarization characteristics of AlScN, realistic donor/acceptor trap landscapes, and temperature-dependent transport parameters. The calibrated simulations are then used to correlate experimental degradation trends with specific physical mechanisms, including threshold-voltage shift, transconductance degradation, and gate-leakage evolution.

The combined experimental and simulation results allow the identification of dominant degradation pathways in AlScN/GaN HEMTs and provide a direct comparison with the previously studied AlGaIn technology (Chapter 5). In doing so, the analysis clarifies the performance-reliability trade-offs associated with the AlScN barrier, highlighting its potential and the remaining challenges for robust next-generation GaN power and RF devices.

Chapter outline. Section 6.2 describes the device technology and experimental methodologies, including pulsed I-V and HTRB step-stress tests. Section 6.3 introduces the TCAD framework and material modeling, followed by calibration and validation in Section 6.4. Sections 6.5 and 6.6 present the pulsed and HTRB analyses, respectively, while Section 6.7 discusses the physical interpretation of degradation mechanisms. Finally, Section 6.8 summarizes the main findings and outlines their implications for AlScN technology development.

6.2 Device Technology and Experiments

6.2.1 Device under test (DUT)

The AlScN/GaN HEMT investigated in this study was fabricated within the GaN15 GaN-on-SiC technology platform [104]. A schematic cross-section of the device is shown in Fig. 6.1. The stack is grown on a 4H-SiC substrate and begins with an AlN nucleation layer, followed by a Fe-doped GaN buffer that ensures both electrical isolation and thermal stability. Above the buffer, an unintentionally doped (n.i.d.) GaN channel hosts the high-mobility 2DEG, which forms at the top heterointerface. The barrier region consists of a 0.7 nm AlN interlayer and an 8.5 nm Al_{0.95}Sc_{0.05}N layer, topped by a 8 nm SiN_x passivation cap to prevent the surface oxidation of AlScN [41], [40].

An a -lattice parameter matching of Al_{1-x}Sc_xN with GaN suggests that strain-free barriers with reduced dislocation density can be achieved for specific Sc compositions. It is still under debate whether full lattice matching occurs at approximately 18% Sc [259] or closer to 13% Sc [260]. Achieving lattice matching is expected to enhance device lifetime and is particularly beneficial for HEMTs employed as high-current switches in power conversion, as the drain current I_D increases with barrier thickness [261], [262].

The gate length is 0.15 μm , with gate-to-source and gate-to-drain distances of $L_{GS} = 0.7 \mu\text{m}$ and $L_{GD} = 1.2 \mu\text{m}$, respectively. A dual field-plate configuration is implemented to optimize the electric field distribution both at the gate edge on the drain side and within the gate-to-drain access region [113], [114]. The Schottky gate contact is composed of an Au/Pt metal stack, providing stable barrier characteristics

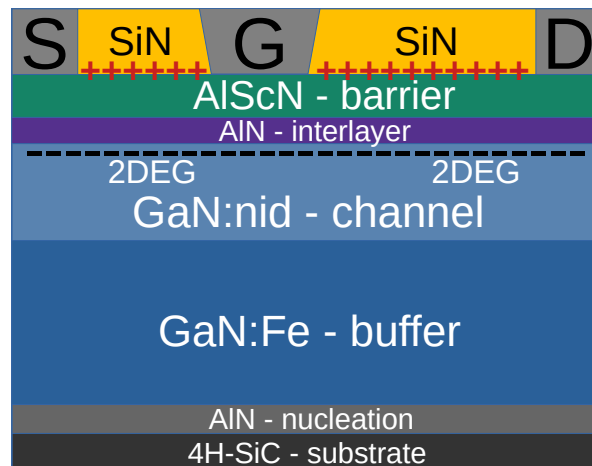


Figure 6.1: Schematic cross-section of the AlScN/GaN HEMT. Donor traps at the SiN/AlScN interface are indicated with "+" and the 2DEG with "-".

over temperature.

Hall-effect measurements on SiN_x -passivated wafers revealed a sheet carrier concentration of $n_s = 1.5 \times 10^{13} \text{ cm}^{-2}$ and a channel mobility of $\mu = 920 \text{ cm}^2/\text{V}\cdot\text{s}$, confirming strong 2DEG confinement and good interface quality [104]. These parameters are also used as reference for TCAD calibration in Section 6.3.

6.2.2 Pulsed I-V characterization

Pulsed I-V measurements were carried out to analyze the trapping and detrapping dynamics in the AlScN/GaN HEMTs under different operating conditions. The experimental procedure follows the same methodology described in Chapter 5. In contrast, the TCAD simulations adopt a modified approach discussed in the following sections. The experimental trends are compared with TCAD results in Section 6.5.

6.2.3 HTRB step-stress protocol

The long-term reliability of the devices was evaluated through HTRB step-stress testing, which is used to study defect generation and charge trapping under combined electric and thermal acceleration [89], [263]. The experimental procedure follows the same methodology described in Chapter 5, with the only difference being that for the AlScN samples each stress step lasts 5 minutes, followed by a 3-minute measurement phase. The experimental trends are compared with TCAD results in Section 6.6

6.3 TCAD Framework and Modeling

6.3.1 Numerical setup

The device simulations were performed using the *Sentaurus Device* simulator, employing a fully coupled drift-diffusion transport model with Fermi-Dirac carrier statistics [18]. This approach provides a good trade-off between physical accuracy and numerical stability, ensuring a realistic description of carrier transport over a wide range of operating conditions. The simulation domain reproduces the actual device geometry and incorporates a non-uniform mesh with enhanced refinement at the heterointerfaces and in the vicinity of the gate edges, where strong electric field gradients are expected.

Ohmic boundary conditions are applied to the source and drain contacts adopting a low workfunction of $\Phi_M = 4.3 \text{ eV}$, a non-local tunneling with a small effective relative electron mass $m_{te} = 0.001$ and including high n-type doping in the contact region equal to $1 \times 10^{19} \text{ cm}^{-3}$ (as provided from the external partner) [126]. The

gate contact is modeled as a Schottky junction with a metal work function of $\Phi_M = 5.65$ eV. Gate leakage is modeled through a combination of thermionic emission and non-local tunneling mechanisms, the latter being essential to capture field-assisted transport through the AlScN barrier.

Carrier mobility is described by a temperature-dependent model combining Masetti and Lombardi formulations for low-field mobility with the high-field Caughey-Thomas expression. This combination allows the accurate reproduction of the experimental transconductance roll-off and current saturation behavior across different bias and temperature conditions.

The numerical solver uses a coupled Newton–Gummel iteration scheme with adaptive timestep and potential damping to ensure convergence during transient simulations. This setup is particularly relevant for the HTRB step-stress simulations, where the progressive increase in drain voltage can otherwise introduce numerical instabilities.

6.3.2 Polarization and interface charge

The electrostatics of AlScN/GaN heterostructures is governed by the interplay between spontaneous and piezoelectric polarization effects. Both contributions were explicitly included in the simulation framework, using polarization constants from [42], [98] for the binary and ternary compounds. The resulting polarization-induced charge densities were further scaled through an *activation* factor to account for partial relaxation and screening effects observed in experimental samples.

At the SiN/AlScN interface, a sheet of positively charged donor-like surface states was introduced to compensate the net negative polarization charge at the AlScN/GaN interface. This donor sheet acts as the primary source of the free electrons populating the 2DEG channel, in agreement with recent experimental evidence and theoretical studies discussed in Chapter 2. The total interface charge density was calibrated in Section 6.4 to simultaneously match the simulated 2DEG density and the experimental threshold voltage.

The combined treatment of polarization and surface donor states enables the correct reproduction of both electrostatic equilibrium and field distribution under off-state conditions, which are crucial for assessing degradation during HTRB stress.

6.3.3 AlScN material parameters

Accurate material parameterization is essential to model the physical behavior of AlScN/GaN HEMTs. The bandgap and electron affinity of each layer were modeled

Material	$E_g(0)$ [eV]	α [10^{-3} eV/K]	β [10^2 K]	$\chi(0)$ [eV]
GaN	3.507	0.909	8.36	2.1
$\text{Al}_{0.31}\text{Ga}_{0.69}\text{N}$	4.3511	1.2	10.3	3.3261
$\text{Al}_{0.95}\text{Sc}_{0.05}\text{N}$	5.9232	1.79	14.62	2.2612
AlN	6.23	1.79	14.62	1.999

Table 6.1: Main band gap parameters in GaN, AlN and in the case of study of the $\text{Al}_{0.95}\text{Sc}_{0.05}\text{N}$ [109], compared to the $\text{Al}_{0.31}\text{Ga}_{0.69}\text{N}$ counterpart, used in this work as a reference. The parameters refer to eqs. 6.1 and 6.2. The values for GaN, AlGa_{0.69}N and AlN are the default ones [18].

as temperature-dependent according to Varshni's empirical relation:

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{(\beta + T)}, \quad (6.1)$$

$$\chi(T) = \chi(0) - \frac{\alpha T^2}{2(\beta + T)} \quad (6.2)$$

where $E_g(0)$, and $\chi(0)$ are the bandgap, and electron affinity at 0 Kelvin, while α , and β the empirical material-dependent constants. By default, in ternary systems a linear mole-fraction dependence of the model parameters is implemented with each parameter P calculated as $P(x) = x \cdot P(\text{M1}) + (1-x) \cdot P(\text{M2})$ where M1 and M2 are the asymptotic ($x = 0$ and $x = 1$) binary materials. This is true for the case of the $\text{Al}_{0.31}\text{Ga}_{0.69}\text{N}$, while a more complex configuration would be necessary for $\text{Al}_{0.95}\text{Sc}_{0.05}\text{N}$ as a crystallographic structure variation is observed between AlN and ScN [109]. Thus, the parameters for the specific mole fraction ($\text{Al}_{0.95}\text{Sc}_{0.05}\text{N}$) are taken from [109] are directly adopted. They are reported in Table 6.1 and compared with reference values of GaN, AlN and $\text{Al}_{0.31}\text{Ga}_{0.69}\text{N}$ [18].

Elastic and piezoelectric constants, reported in Table 6.2, were taken from [42], [98], [173], [174], [250]. The incorporation of a 5% Sc fraction was found to reduce the elastic stiffness constants c_{33} , while having higher c_{12} , and c_{13} . The spontaneous polarization term is larger, leading to an overall increase in the total polarization charge at the heterointerface. This polarization enhancement is one of the key mechanisms enabling higher sheet carrier concentrations in AlScN-based HEMTs.

6.3.4 Trap landscape

A realistic representation of trap states is fundamental to capture the degradation dynamics observed during pulsed and HTRB stress tests. In the present model, two

Material	P_z^{SP} [10^{-6}C/cm^2]	d_{31} [10^{-10}cm/V]	c_{11} [10^{11} Pa]	c_{12} [10^{11} Pa]	c_{13} [10^{11} Pa]	c_{33} [10^{11} Pa]
GaN	-3.4	-1.6	3.9	1.45	1.06	3.98
Al _{0.31} Ga _{0.69} N	-5.136	-1.755	3.9186	1.4252	1.0662	3.9025
Al _{0.95} Sc _{0.05} N	-9.31	-1.7058	3.791325	1.39	1.149	3.35
AlN	-9.00	-2.1	3.96	1.37	1.08	3.73

Table 6.2: Piezoelectric parameters of the strain model in GaN, AlN and in the case of study of the Al_{0.95}Sc_{0.05}N, compared to the Al_{0.31}Ga_{0.69}N counterpart, used in this work as a reference. The values for GaN, AlGaN and AlN are the default ones [18].

main classes of traps were included, reflecting the dominant physical defects known for GaN-based heterostructures.

First, Fe-related acceptor traps are introduced in the buffer and lower channel regions to reproduce the typical semi-insulating behavior and deep-level trapping observed in Fe-doped GaN.

Following [88], iron-related deep acceptor traps are included in the TCAD setup to model the doping compensation mechanisms typically observed in Fe-doped GaN buffers. An exponential tail distribution is assumed in the channel region, while a uniform trap concentration of 10^{18} cm^{-3} is adopted in the buffer, as illustrated in Fig. 5.6a. The trap energy level is set to $E_t = E_C - 0.6\text{ eV}$, consistently with experimental reports on Fe-doped GaN [241], [245], where E_C denotes the conduction band minimum. This value is slightly deeper than that commonly assumed for AlGaN-based devices ($E_C - 0.5\text{ eV}$), as adopted in Chapter 5 and reported in the literature [239], [240], [242]. However, this small variation does not lead to significant differences in the simulated device characteristics.

Second, donor-like traps were placed at the SiN/AlScN interface, with an energy level centered around $E_t = E_C - 1.6\text{ eV}$, consistent with experimental evidence of surface states associated with nitrogen vacancies and donor-type defects [42], [89]. These traps are particularly relevant under gate-side high-field conditions, where their progressive charging and partial detrapping directly affect the off-state leakage and transconductance degradation.

The combined trap configuration reproduces both the transient and steady-state degradation observed in experiments, enabling a consistent description of the device behavior across different stress regimes. Further quantitative calibration of trap concentrations and energy depths is discussed in Section 6.4.

6.4 Model Calibration and Baseline Validation

The numerical framework described in Section 6.3 was calibrated to reproduce the measured electrical characteristics of the AlScN/GaN HEMTs at room and elevated temperatures. The calibration aimed to establish a consistent baseline across experimental and simulated data, ensuring that all subsequent stress simulations (pulsed and HTRB) originate from a physically meaningful initial state. The key parameters adjusted in this phase were the polarization activation factor, surface-donor sheet charge, and mobility model constants, as discussed below.

6.4.1 2DEG and threshold alignment

Different experimental datasets were employed to calibrate the TCAD model of the AlScN/GaN HEMT against measurements. As a first step, Hall-effect data of the sheet carrier density n_s were used to adjust the combined effects of donor trap concentration at the SiN/AlScN interface in the gate-to-drain access region and the polarization charges at the heterointerfaces. The donor trap energy level was set to $E_t = E_C - 1.6\text{eV}$, following the discussion in [88], [231]. This choice is consistent with the state-of-the-art understanding of similar nitride interfaces and, in particular, with the previous analysis performed on the AlGaN/GaN reference structure, due to the limited availability of experimental information for the SiN/AlScN case [40].

The donor concentration was fitted to the experimental n_s value to compensate the overall polarization charge arising from the SiN/AlScN, AlScN/AlN, and AlN/GaN interfaces. Since no experimental data are currently available to independently calibrate each interface, the activation parameter of the piezoelectric polarization model introduced in the previous subsection was assumed identical across all interfaces above the 2DEG.

To further refine the activation parameter governing polarization effects in the device, its influence on the electrostatic response of the complete gate stack was evaluated through the DC transfer characteristic (I_D - V_{GS}) at room temperature. The gate metal work function was fixed at 5.65 eV, corresponding to the upper limit expected for the Au/Pt stack used in fabrication [232]. Under this assumption, an activation parameter of 0.33 was selected to reproduce the experimental V_{th} . Accordingly, a donor trap concentration of $2.3 \times 10^{13} \text{ cm}^{-2}$ was adopted in the access region to compensate the total piezoelectric charge and yield the expected 2DEG density. A direct comparison between the simulated band diagrams of AlScN/GaN and the reference AlGaN/GaN stack is shown in Fig. 6.2. The net interface charge values for both stacks are also reported, indicating that a higher donor-trap density is required in the AlGaN case to sustain the 2DEG formation, which nonetheless remains

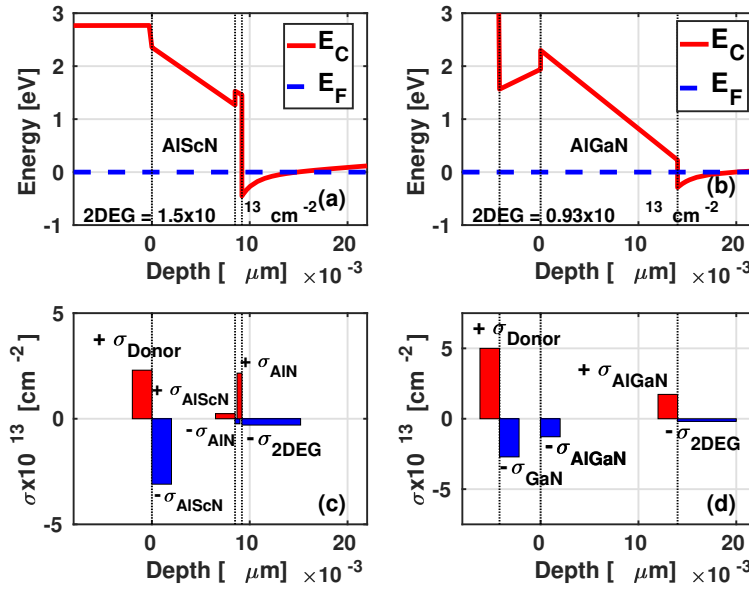


Figure 6.2: (a) Energy band diagram of the AlScN/GaN heterostructure in the access region. (b) Energy band diagram of the AlGaN/GaN heterostructure in the access region [89]. (c) & (d) Net charge distribution at different interfaces, with visible 2DEG charge, given by electrons supplied by surface donor states in the cases of AlScN and AlGaN barriers, respectively. The enhanced band bending in AlScN corresponds to the stronger polarization and higher 2DEG density.

lower than in the AlScN-based device. The deeper conduction-band bending in the AlScN structure reflects the stronger polarization-induced potential drop, resulting in enhanced 2DEG confinement. The figure further illustrates the slightly different charge distributions needed to reproduce the measured electrical equilibrium in the two technologies.

6.4.2 DC transfer/input characteristics

Once the equilibrium electrostatics was validated, the next step involved calibrating the DC transfer and input characteristics in the subthreshold region. The room-temperature subthreshold leakage is modeled through a combination of thermionic emission and non-local tunneling (see Chapters 1 and 3). The effective tunneling mass for electrons, m_{te} , is fixed to $0.031 m_0$, with m_0 the free electron mass, playing a key role in the reverse-bias regime, providing a sensitive parameter to fine-tune the experimental data [89]. This value ensures a correct prediction of the measured leakage gate current magnitude, particularly over the negative bias range that will serve as base for the pulsed and HTRB analyses.

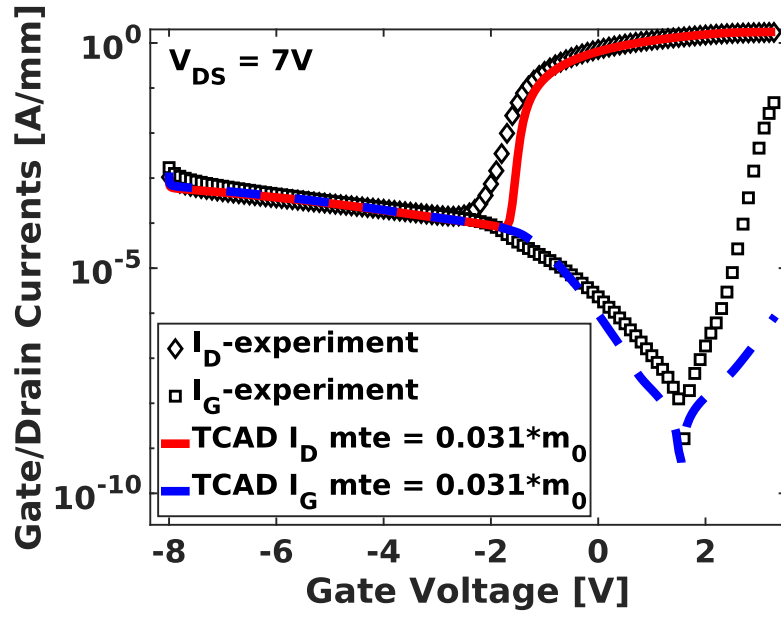


Figure 6.3: Semi-log I_G - V_{GS} and I_D - V_{GS} curves of the AlScN/GaN HEMT as a function of gate voltage, for $V_{DS} = 7V$, at 300 K.

Fig. 6.3 confirms that the calibrated model accurately reproduces the experimental I_D - V_{GS} and I_G - V_{GS} characteristics at different biases, validating the leakage mechanisms.

Fig. 6.3 confirms that the calibrated model accurately reproduces the experimental I_D - V_{GS} characteristics across the entire gate voltage range. In contrast, the simulated I_G - V_{GS} curves show very good agreement in the reverse-bias region, while deviations appear under forward-bias conditions, where the leakage is not fully captured.

6.4.3 Mobility model

The low-field mobility is calibrated based on Hall-effect measurements of the 2DEG provided by the fabrication partner, with the same consideration seen in Chapter 5, subsection 5.2.2 [104]. The doping dependence of the bulk mobility was modeled using the Masetti formulation with default GaN parameters [18]. No additional temperature-dependent term was introduced in this model.

To capture the degradation of mobility near the semiconductor surface, the Lombardi model was adopted to describe the effects of surface acoustic phonons (μ_{ac}) and surface roughness (μ_{sr}) (see Chapter 3) [40].

The surface acoustic-phonon contribution follows the same temperature dependence adopted for the bulk term in Eq. (3.1), consistently with the Lombardi mobility model described by Eqs. (3.3) and (3.4). The parameters adopted in the analysis are

Parameters	B [cm/s]	C [cm ^{5/3} /V ^{2/3} s]	δ [V/s]	η [V ² /cm·s]
GaN default	4.75×10^7	580	5.82×10^{14}	5.82×10^{30}
DC/HTRB data	7.5×10^6	275	2.5×10^{15}	1×10^{23}
Pulsed I-V	2.0×10^4	920	1.33×10^{15}	1.35×10^{22}

Table 6.3: Mobility-model parameters (default, DC/HTRB, and pulsed sets). Modified parameters in the Lombardi model compared to default parameters for GaN.

summarized in Table 6.3. The screening effects induced by the local doping concentration N are accounted for through the parameter λ , which is set to $\lambda = 0.125$ in this work.

The surface terms were then combined with the bulk Masetti mobility through Matthiessen's rule to obtain the total low-field mobility (see Chapter 3) [18].

As shown in Table 6.3, a moderate tuning of the Lombardi parameters was required to achieve a quantitative match between simulated and measured I_D – V_{GS} characteristics under DC/HTRB and pulsed conditions. This adjustment reflects the use of different devices for the various characterization sets provided by the external partner [104].

At high electric fields, carrier velocity saturation was included using the Caughey–Thomas model, with a saturation velocity $v_{\text{sat}} = 1.3 \times 10^7$ cm/s and a field-dependence exponent $\beta = 1.7$ applied consistently across all simulations (see Chapter 3). These values are in agreement with the MC analysis reported in [169]. The possible temperature dependence of β was neglected due to its minor influence in the explored bias and temperature range.

Temperature-dependent mobility modeling is essential to ensure the physical reliability of the simulations, particularly for the HTRB step-stress tests, which involve stressing at 398 K and subsequent measurements at 323 K. Accordingly, the calibrated mobility set was validated against fresh DC I – V measurements at 323 K, performed on two different samples. Experimental and TCAD results are compared in Fig. 6.4 using both linear and logarithmic scales, allowing the accuracy of the model to be assessed in subthreshold and on-state regimes.

The comparison confirms a consistent temperature behavior of the adopted models, with minor discrepancies between measured datasets primarily attributed to device-to-device variability, such as fluctuations in 2DEG density, interface-trap distribution, and local mobility. Although no direct electrical measurements were performed at 398 K, the proposed mobility framework exhibits stable and physically consistent predictions across the entire operating temperature range.

6.4.4 Summary of Physical Models

For completeness, Table 6.4 summarizes the physical models adopted in the TCAD simulations. Calibrated parameters for bandgap, mobility, polarization, and tunneling are reported in the corresponding tables in Sections 6.3.3 and 6.4.3.

Table 6.4: Summary of physical models adopted in the TCAD simulations of AlScN/GaN HEMTs. Calibrated parameters are reported in Tables 6.1, 6.2, and 6.3.

Physics Models	Parameters
Fermi–Dirac Statistics	default
Constant mobility	$\mu_{\max} = 920 \text{ cm}^2/\text{Vs}$
Doping-dependent mobility	default
Surface effects	see table 6.3.
High-field saturation	$v_{\text{sat}} = 1.3 \times 10^7 \text{ cm/s}$, $\beta = 1.7$
SRH Recombination	default
Polarization (strain)	see table 6.2, <i>activation</i> = 0.33
Thermionic emission	default
Gate workfunction	5.65 eV
Source/drain workfunction	4.3eV
Gate nonlocal barrier tunneling	$m_{\text{te}} = 0.031 m_0$ (electrons), $m_{\text{th}} = 0.4 m_0$ (holes)
Source/drain nonlocal barrier tunneling	$m_{\text{te}} = 0.001 m_0$ (electrons), $m_{\text{th}} = 0.001 m_0$ (holes)

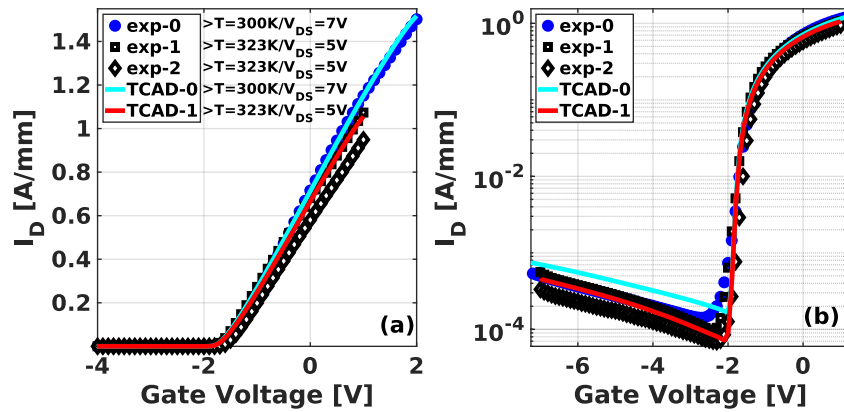


Figure 6.4: DC I_D - V_{GS} at 300K for $V_{DS} = 7$ V and at 323K for $V_{DS} = 5$ V. Black closed symbols: DC experiments at 300K, one sample. Open symbols: DC experiments at 323K, two samples. Cyan line: TCAD DC simulations at 300K, $V_{DS} = 7$ V. Red line: TCAD DC simulations at 323K, $V_{DS} = 5$ V. Simulation parameters for the Lombardi model correspond to the "DC/HTRB data" in Tab. 6.3. (a) I_D - V_{GS} in lin scale, (b) I_D - V_{GS} in log scale.

Unless otherwise specified, all parameters associated with the physical models are set to the default values provided by the Sentaurus Device simulator.

6.5 Pulsed I-V Analysis

Unlike DC sweeps, pulsed I-V characterizations offer a sensitive indicator of charge exchange processes occurring at different time scales and spatial locations within the device structure. In this section, the experimental pulsed I-V characteristics of the AlScN/GaN HEMT are compared with calibrated TCAD simulations to identify the dominant physical mechanisms responsible for the observed current collapse and to highlight the differences with respect to the AlGaN reference technology.

6.5.1 Experimental observations

A comprehensive set of pulsed measurements was performed to investigate the dynamic performance and trapping effects in AlScN/GaN HEMTs [104]. The experimental protocol employs different quiescent bias conditions, following the approach previously adopted in Chapter 5, Section 5.3, Subsection 5.3.1. For each condition, the device was pre-biased long enough to reach a quasi-stationary state prior to applying the pulse sequence [220]–[222]. The pulse width was set to 9 ns with a duty cycle of 1%, corresponding to a period of 900 ns, ensuring negligible self-heating and preserving the quiescent-state equilibrium during the measurement. The corresponding timing diagram of the pulsed sequence is shown in Fig. 5.7.

Figure 6.5 shows the pulsed I_D – V_{DS} characteristics at quiescent zero bias, used as the baseline for TCAD calibration. The measurements were performed on dies different from those used for DC characterization, which may introduce slight variability in threshold voltage or mobility; however, such variations do not affect the overall calibration consistency. The complete set of pulsed measurements across all quiescent states is reported in Fig. 6.6, illustrating the progressive current degradation with increasing quiescent V_{DS} , a signature of field-enhanced trap occupation.

6.5.2 TCAD interpretation

In the TCAD framework, the pulsed regime was reproduced through a simplified transient simulation flow consisting of a 100s pre-biasing phase to reach quasi-stationary equilibrium, followed by a 9ns voltage ramp for each IV curve. This approach, while not a strict replication of the experimental waveform, yields an equivalent response with a worst-case deviation below 0.07% and significantly reduces computational time (Fig. 6.7). To match the experimental pulsed output characteristics at the

(0, 0) V quiescent state, minor adjustments were introduced in the model parameters. Specifically, the polarization activation coefficients at the SiN/AlScN, AlScN/AlN, and AlN/GaN interfaces were tuned from 0.33 to 0.307 and 0.30, respectively, to reproduce the observed threshold-voltage shift with respect to the DC data. Moreover, the Lombardi mobility parameters were updated (see Table 6.3, set “Pulsed I-V”) to account for the dynamic transport behavior across both linear and saturation regimes. As shown in Fig. 6.5, the resulting TCAD curves exhibit an excellent fit with experimental data across the entire V_{GS} range.

Figure 6.8 summarizes the extracted I_D trends at $V_{DS} = 9.7$ V (saturation) and $V_{DS} = 0.49$ V (linear region) for all quiescent bias conditions, chosen according to the available experimental data. The observed degradation with increasing quiescent drain bias is attributed to enhanced occupation of Fe-related traps in the GaN channel. During cold pinch-off ($V_{DS} = 0$), trap filling occurs mainly beneath the gate, while under hot pinch-off (positive V_{DS}), the occupation front extends toward the gate-drain region, resulting in additional current collapse. In saturation, TCAD simulations accurately capture the experimental degradation trends, while in the linear regime a slight overestimation appears at $V_{GS} > 0$ V, likely caused by residual Schottky barrier effects at the source and drain ohmic contacts not included in the model [264].

The analysis confirms that the pulsed degradation in AlScN/GaN HEMTs is dominated by Fe-related acceptor traps in the channel region, with negligible contribution from donor states at the passivation/barrier interface. This behavior contrasts with the

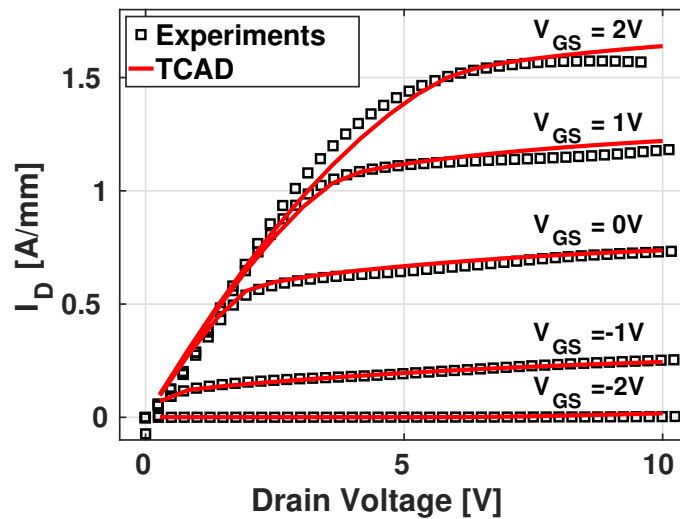


Figure 6.5: Experimental pulsed I_D - V_{DS} characteristics of a $2 \times 25 \mu\text{m}$ AlScN/GaN HEMT, measured with a 900 ns pulse width and 1% duty cycle for V_{GS} from -2 V to 2 V in 1 V steps, at $T = 300$ K. Black symbols: experiments; red line: TCAD simulation.

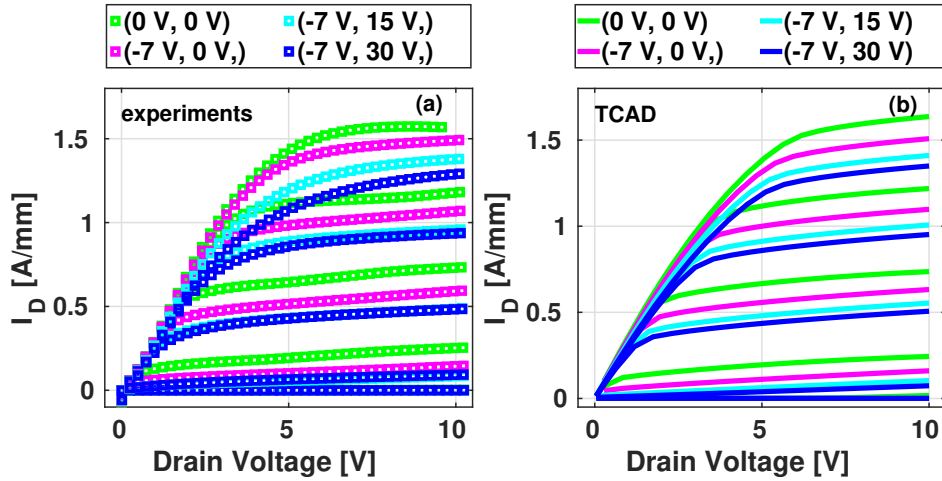


Figure 6.6: (a) Measured and (b) simulated pulsed I_D - V_{DS} curves under four quiescent bias conditions, at $T = 300$ K [88], [104]. Simulations include donor traps at the SiN/AlScN interface ($E_t = E_C - 1.6$ eV) and Fe-related acceptor traps in the channel ($E_t = E_C - 0.6$ eV). Excellent agreement is obtained across all quiescent states.

reference AlGaN/GaN technology, where surface traps strongly influence dynamic performance. In the AlScN-based device, the lower density of interface states at the SiN/AlScN interface (see Fig. 6.2) effectively decouples surface trapping from transient degradation, leading to reduced current collapse. These findings further emphasize the importance of minimizing iron contamination in the channel or adopting alternative isolation buffer designs to ensure optimal dynamic performance and long-term reliability of AlScN-based HEMTs [265].

6.6 HTRB Step-Stress Analysis

The HTRB step-stress test provides a complementary perspective on device reliability with respect to the pulsed I-V characterization discussed in Section 6.5. While pulsed measurements probe trapping and detrapping dynamics under controlled quiescent conditions, the HTRB step-stress test focuses on progressive and cumulative degradation processes that occur under sustained high electric field and elevated temperature. By gradually increasing drain bias during stress, this accelerated reliability test enables the identification of field- and temperature-activated mechanisms such as charge build-up, interface trap generation, and gate leak evolution.

The step-stress approach adopted here allows an accelerated yet controlled evaluation of device robustness, capturing the onset and progression of degradation over intermediate time scales, significantly shorter than conventional long-duration HTRB

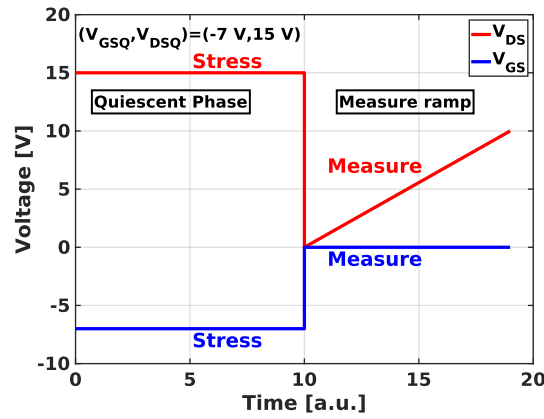


Figure 6.7: Most efficient pulsed simulation configuration in the case of the hot pinch-off condition (iii) (-7 V, 15 V) and the measurement of the $V_{GS} = 0$ V, at $T = 300$ K. The same is valid for each quiescent state and V_{GS} simulation. The simulation consists of a 100 s quiescent stress phase followed by a single 9 ns voltage pulse. To improve readability, the time axis is expressed in arbitrary units and not to scale.

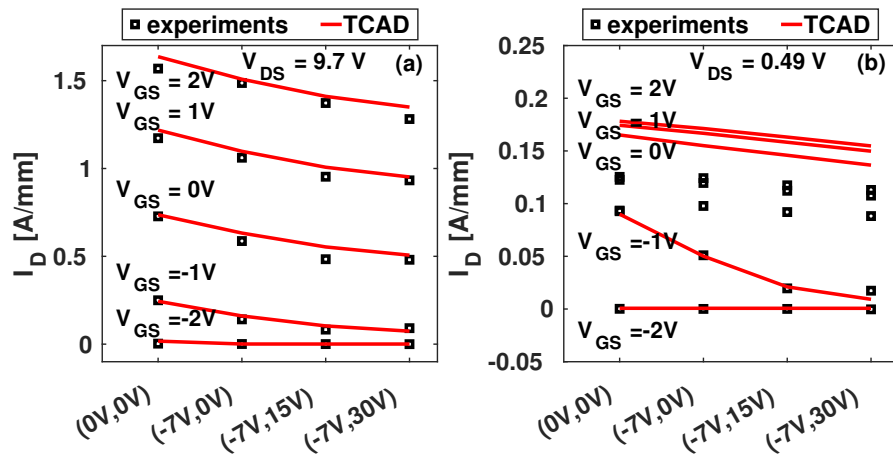


Figure 6.8: Measured and simulated drain current I_D for different quiescent bias states at (a) $V_{DS} = 9.7$ V (saturation) and (b) $V_{DS} = 0.49$ V (linear region), at $T = 300$ K. The model provides excellent agreement in saturation and near-perfect matching in the linear regime.

tests, yet sufficiently long to reveal permanent or quasi-permanent defect activation. Combined with the pulsed I-V characterization, this analysis provides a comprehensive understanding of both reversible and irreversible phenomena governing the electrical stability of AlScN/GaN HEMTs.

The experimental bias sequence adopted for the HTRB step-stress measurements are the same as seen in Chapter 5, section 5.4.

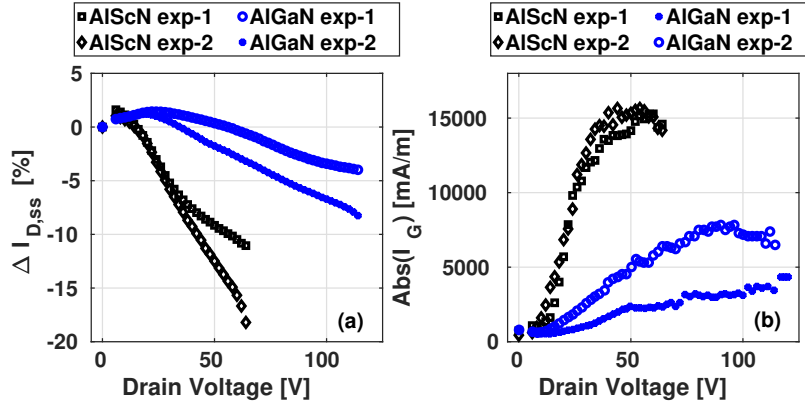


Figure 6.9: (a) Relative $\Delta I_{D,ss}$ [%] and (b) absolute I_G in mA/m for four AlGaN/GaN and AlScN/GaN samples, at $T = 323$ K after each stress step of the HTRB. Black symbols: AlScN experiments; blue symbols: AlGaN experiments;

6.6.1 Experimental procedure and data trends

The HTRB step-stress test was performed to assess the long-term reliability of the AlScN/GaN HEMTs. The procedure is slightly different from that seen previously in section 5.4. This time each stress step lasts 5 minutes, followed by a 3-minute measurement phase. During the measurements, the transfer characteristics, input gate-leakage current, Schottky diode behavior, and output characteristics were recorded at $V_{GS} = 1$ V (on-state) and $V_{GS} = -7$ V (off-state) [89]. The temperatures used during the test are the same as those indicated in section 5.4. TCAD simulations were performed under the same thermal conditions for direct comparison.

Lastly, the drain current in saturation ($I_{D,ss}$) was extracted from the transfer characteristics at $V_{GS} = 1$ V and $V_{DS} = 5$ V. Partial recovery of $I_{D,ss}$ was observed during the intermediate measurement phases, likely due to detrapping effects and partial charge redistribution [263].

Figure 6.9 compares the relative degradation of the saturation drain current, $\Delta I_{D,ss}$ [%], and the absolute value of the gate current in mA/m, I_G , for four AlScN and AlGaN devices, namely exp-1, and exp-2 for each technology. Experimental data for the AlGaN technology are taken from the previous Chapter 5 and serve as reference [89]. The differences between the two technologies primarily originate from the distinct barrier stacks, the passivation/barrier interfaces above the 2DEG, and the gate Schottky contact geometry.

AlScN-based devices exhibit a higher I_G due to the thinner barrier in the gate stack (see Fig. 6.2), which in turn correlates with a stronger I_D collapse, opposite to the behavior observed in AlGaN HEMTs. The $\Delta I_{D,ss}$ [%] shows an almost linear degradation trend with increasing V_{DS} , apart from a negligible initial increase

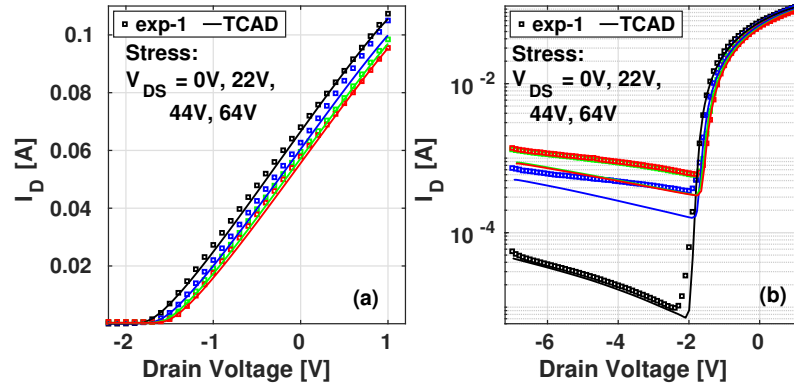


Figure 6.10: DC I_D – V_{GS} at 323 K for $V_{DS} = 5$ V after stress steps corresponding to $V_{DS} = 0, 22, 44,$ and 64 V, respectively. Symbols: experiments; lines: TCAD results. (a) Linear scale. (b) Logarithmic scale.

(< 2%), while I_G tends to saturate at high stress levels. To clarify the physical origin of these trends, the following sections separate the contributions associated with threshold-voltage and transconductance shifts.

6.6.2 Separating V_{th} and g_m contributions

To identify the mechanisms responsible for the observed current degradation, the full I_D – V_{GS} curves acquired at the end of each stress step were analyzed. These curves were used to separate the relative impact of threshold-voltage shifts and transconductance variations on $\Delta I_{D,ss}[\%]$, allowing the localization of degradation phenomena in either the channel or the gate–drain access region.

Figure 6.10 shows the experimental and simulated I_D – V_{GS} curves at various stress levels ($V_{DS} = 0, 22, 44, 64$ V), in both linear and logarithmic scales, enabling evaluation in the subthreshold and on-state regimes. The threshold-voltage shift, ΔV_{th} , was extracted at a fixed drain current of 1 mA in the subthreshold region. The corresponding $\Delta I_{D,ss-V_{th}}[\%]$ was determined by translating the pristine I_D curve by the measured ΔV_{th} . Since no significant subthreshold slope changes were observed, the remaining variation in $\Delta I_{D,ss}[\%]$ was attributed to transconductance degradation, denoted as $\Delta I_{D,ss-gm}[\%]$, obtained as:

$$\Delta I_{D,ss-gm}[\%] = \Delta I_{D,ss}[\%] - \Delta I_{D,ss-V_{th}}[\%].$$

The extracted trends are reported in Fig. 6.11. For AlGaIn-based HEMTs, a small positive $\Delta I_{D,ss-V_{th}}[\%]$ is observed, consistent with minor in-situ trapping and negligible hot-carrier generation at high stress biases [211]. Conversely, AlScN-based

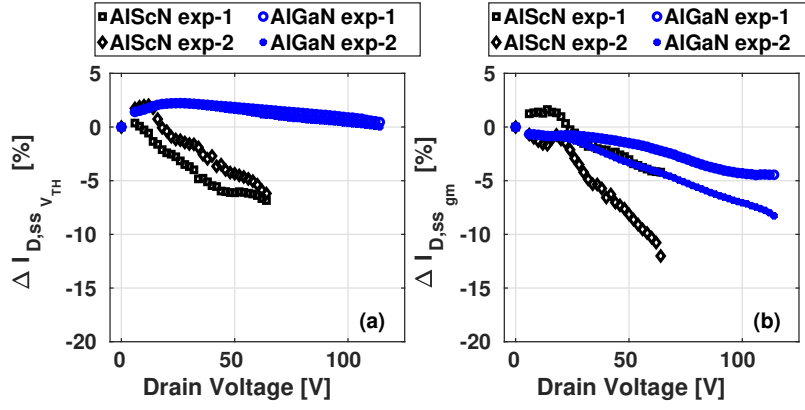


Figure 6.11: (a) Extracted contributions of V_{th} shift and (b) g_m degradation to the relative $\Delta I_{D,ss}$ [%] at $T = 323$ K after each stress step of the HTRB. Black symbols: AlScN experiments; blue symbols: AlGaN experiments; red lines: TCAD simulations.

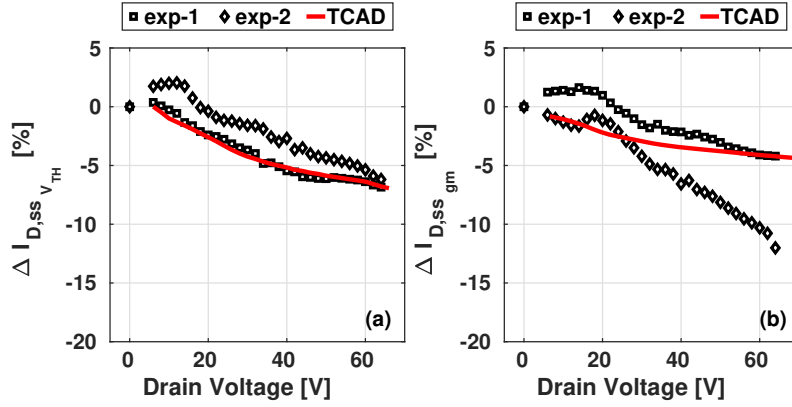


Figure 6.12: Extracted contributions of (a) V_{th} shift and (b) g_m degradation to $\Delta I_{D,ss}$ [%] at $T = 323$ K after each stress step of the HTRB. Black symbols: experiments; red lines: TCAD simulations.

devices show a negative $\Delta I_{D,ss-V_{th}}$ [%] increasing with V_{DS} , attributed to hot-carrier-induced degradation in the channel region. The $\Delta I_{D,ss-gm}$ [%] curves display a consistent negative trend across all devices, though slightly more pronounced in AlScN samples due to the combined influence of channel and gate-drain region degradation.

6.6.3 TCAD modeling of degradation

The HTRB step-stress experiment was reproduced in TCAD by applying a progressive V_{DS} ramp and saving the device state after each stress level. Although recovery effects during measurement phases were not included, leading to a slight mismatch at low V_{DS} , the overall degradation evolution is accurately captured. Post-processing was used to extract the full I_D – V_{GS} curves and corresponding $I_{D,ss}$ values from each saved state (Fig. 6.10) [88], [89].

As shown in Fig. 6.12, the extracted $\Delta I_{D,ss-V_{th}}[\%]$ and $\Delta I_{D,ss-gm}[\%]$ from experiments are well reproduced by TCAD simulations. The observed threshold-voltage shift (0–0.249 V) is modeled through the progressive introduction of interface traps beneath the gate, with densities increasing from 0 to $1.45 \times 10^{12} \text{ cm}^{-2}$. Following [88], the $\Delta I_{D,ss-gm}[\%]$ component is attributed to the partial detrapping of donor traps at the SiN/AlScN interface. A parametric sweep of the donor-trap energy level (Fig. 6.13) highlights its effect on $\Delta I_{D,ss-gm}[\%]$ and the total $\Delta I_{D,ss}[\%]$. The best agreement with experiments is achieved for $E_t = E_C - 1.6 \text{ eV}$, consistent with donor states observed in similar heterostructures.

6.6.4 Correlation with gate leakage

The relationship between the degradation of $I_{D,ss}$ and the evolution of gate current I_G during HTRB stress is illustrated in Fig. 6.14. The joint analysis of both quantities further validates the TCAD model calibration. A slight overestimation of $\Delta I_{D,ss}[\%]$ at low V_{DS} values is mainly attributed to the exclusion of recovery mechanisms between stress steps. Nevertheless, the slope evolution and degradation saturation at high voltages are accurately reproduced.

The TCAD results capture both the saturation of I_G and the progressive increase of $\Delta I_{D,ss}[\%]$, confirming the mutual correlation between charge trapping in the gate–drain access region and gate-leakage evolution. The higher I_G observed in AlScN devices, compared to AlGaIn, may stem from oxygen or silicon contamination during epitaxy or from the formation of vacancy complexes that create localized conductive paths [211], [254], [266]. Although the inclusion of such complex defect-assisted conduction mechanisms lies beyond the present modeling scope, the experimental

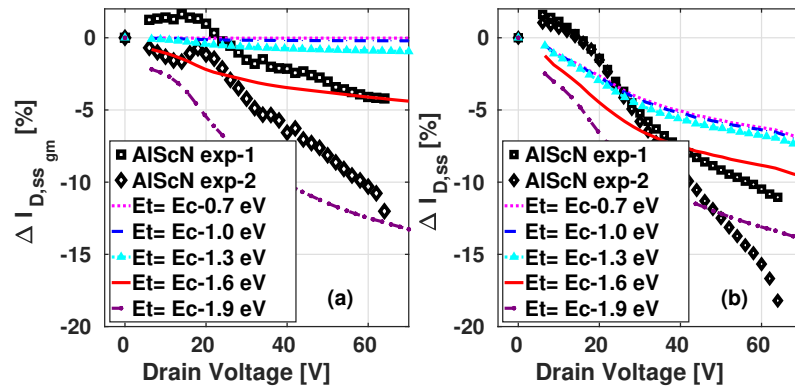


Figure 6.13: (a) Simulated $\Delta I_{D,ss-gm}[\%]$ and (b) total $\Delta I_{D,ss}[\%]$ as a function of donor energy level, at $T = 323 \text{ K}$ after each stress step of the HTRB; black symbols: experiments; lines: TCAD simulations.

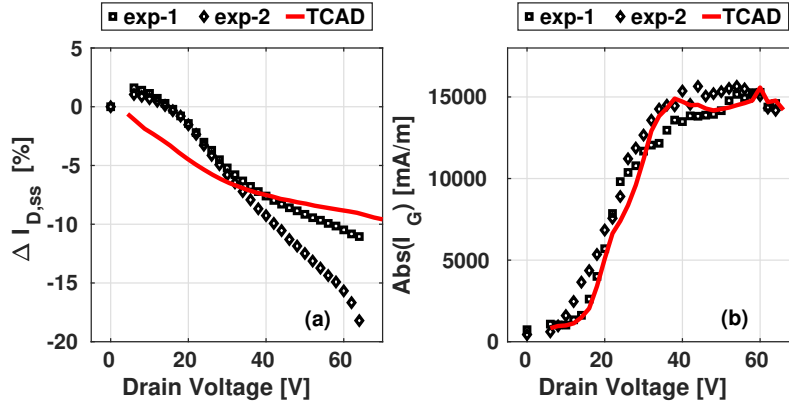


Figure 6.14: (a) Relative $\Delta I_{D,ss} [\%]$ and (b) absolute I_G at $T = 323$ K after each stress step of the HTRB. Black symbols: experiments; red lines: TCAD simulations.

I_G behavior is satisfactorily reproduced by adjusting the tunneling effective mass m_{te} from $0.031m_0$ to $0.01355m_0$ across successive stress steps.

6.7 Discussion

The comprehensive study presented in this chapter combines experimental characterization and TCAD simulations to investigate the reliability of AlScN/GaN HEMTs. The analysis spans from static calibration to dynamic and long-term stress characterization, providing a consistent physical interpretation of degradation mechanisms in comparison with conventional AlGaN/GaN technology.

A dedicated TCAD setup for AlScN/GaN HEMTs was developed and calibrated using both theoretical and experimental references from the literature, together with the construction of a parameter file for AlScN in order to perform the simulations [40]–[42], [96], [98], [99], [104], [109], [173], [174], [255]. The initial calibration focused on matching the input, transfer, and output characteristics at 300 K, reproducing both threshold voltage and 2DEG density extracted from Hall and DC measurements. The fitting of the mobility and polarization models, together with the inclusion of donor and acceptor traps, provided an accurate baseline for reproducing experimental trends across different operating regimes.

Pulsed I-V measurements were then used to validate the dynamic response of the calibrated setup under different quiescent states. This step was essential to assess how the model captured charge trapping and detrapping processes without the interference of self-heating or ultra-fast transient effects. The analysis demonstrated that the TCAD model accurately reproduced the pulsed output characteristics across

all bias conditions, as shown in Figs. 6.6, 6.8, confirming its reliability in transient regimes.

The comparison between measurements and simulations revealed a high on-resistance in the output characteristics. In fact, a slight Schottky-like behavior at low V_{DS} was observed experimentally for $V_{GS} \geq 0$ V (Figs. 6.6a, 6.8b), possibly due to non-ideal ohmic contacts on the AlScN barrier which still need to be technologically improved [104]. The presence of Fe-related traps in the channel, enhance isolation but contribute to current collapse. Nevertheless, the overall fitting quality confirmed that the main trapping effects were correctly captured, with donor states at the SiN/AlScN interface having negligible impact under pulsed timing. The results also emphasized the superior decoupling of surface traps in AlScN compared to that of AlGaN, leading to a reduced surface-driven current collapse during switching events.

A comparative HTRB step-stress analysis between AlScN and AlGaN HEMTs was performed to examine long-term degradation mechanisms. Both technologies share the same buffer and channel layers, isolating the effects of the barrier stack and gate interface. As shown in Fig. 6.9, the AlScN-based devices exhibit a higher gate current due to their thinner barrier, which correlates with an earlier onset of drain current degradation. This behavior suggests a stronger coupling between gate leakage and drain collapse in AlScN devices, consistent with the increased current and electric-field penetration across the thinner barrier layer.

The nearly linear degradation trend of $\Delta I_{D,ss}[\%]$ with stress voltage and the saturation of I_G at high V_{DS} indicate progressive donor detrapping and partial recovery processes during the measurement phases [263]. A minor initial enhancement of the drain current (below 2%) was occasionally observed and can be attributed to transient charge release from deep buffer traps or Fe compensation, as reported in [267]–[270], as well as donor surface trap charging as reported in [88]. While this effect was not explicitly modeled, it remains negligible within the overall degradation dynamics.

The step-stress TCAD simulations reproduced the experimental HTRB conditions and successfully decoupled the contributions of threshold voltage and transconductance degradation (Fig. 6.12). A progressive V_{th} shift up to 0.249 V was reproduced by introducing acceptor-like interface traps beneath the gate region, consistent with the formation of localized trapping in the thin AlN interlayer or at the $Al_{0.95}Sc_{0.05}N$ barrier [271]. In parallel, the partial donor detrapping at the SiN/AlScN interface reproduced the measured $\Delta I_{D,ss-gm}$ degradation, confirming the relevance of the surface donor states in the access region [40].

A parametric analysis of donor trap energy levels (Fig. 6.13) highlighted that an energy depth of $E_t = E_C - 1.6$ eV best matches the experimental $\Delta I_{D,ss}[\%]$ trend

and the degradation saturation at high stress voltages. This energy level aligns with similar reported donor-like defects responsible for trapping in at the SiN passivation interface [88], [89], [172], [248]. Overall, the TCAD model accurately captured the interplay between channel-related degradation (ΔV_{th}) and access-region donor detrapping (Δg_m), both contributing to the overall drain current collapse.

The correlation between $\Delta I_{D,ss}[\%]$ and I_G (Fig. 6.14) reinforces the strong coupling between gate leakage and degradation in AlScN-based HEMTs. The higher I_G values measured experimentally can be linked to field-assisted tunneling and possible oxygen/silicon contamination during epitaxy, which may form conductive filaments or vacancy complexes [211], [254], [266]. Although these microscopic effects are beyond the current modeling scope, the TCAD framework effectively reproduces the measured leakage evolution by adjusting the tunneling effective mass m_{te} across stress steps, ensuring a physically consistent calibration.

The comparison with AlGaN highlights an intrinsic trade-off between performance and reliability in AlScN devices: while the higher polarization and thinner barrier enable enhanced 2DEG density, and improved transconductance, they also lead to stronger electric-field stress under reverse bias, making the gate stack more prone to leakage and defect activation. This suggests that optimization of the barrier stack thickness, interface trap density, and buffer design will be critical for future AlScN-based HEMTs to achieve robust long-term reliability.

In summary, the combined experimental and TCAD analyses identify three dominant mechanisms governing degradation in AlScN/GaN HEMTs under HTRB stress: (i) under-gate acceptor-trap buildup causing ΔV_{th} shifts, (ii) donor detrapping in the gate-drain access region leading to Δg_m reduction, and (iii) field-assisted gate leakage correlating with overall drain current collapse. Compared to AlGaN devices, AlScN-based HEMTs exhibit reduced surface-trap coupling under pulsed operation but greater susceptibility to gate-driven degradation during long-term stress. These findings provide valuable insight for future barrier engineering and device optimization, emphasizing the importance of interface quality and barrier composition in balancing performance and reliability.

6.8 Summary

This chapter developed and validated a comprehensive TCAD framework for AlScN/GaN HEMTs, calibrated against DC, pulsed, and HTRB experimental data. The proposed model successfully reproduced the measured electrical characteristics and enabled a physical decomposition of the overall $\Delta I_{D,ss}[\%]$ degradation into its threshold-voltage (ΔV_{th}) and transconductance (Δg_m) components. Through progressive stress

simulations, the donor energy depth at the SiN/AlScN interface was identified as a critical parameter governing the HTRB evolution, together with the field-assisted increase of the gate leakage current during reverse bias stress.

The analysis highlighted that quiescent state trapping, highlighted by pulsed probing, is predominantly driven by Fe-related states within the GaN channel, whereas long-term degradation under HTRB arises from a combination of under-gate interface-trap buildup and donor detrapping in the gate–drain access region. The joint interpretation of experimental and simulation data provided a consistent understanding of how these distinct physical processes contribute to the observed drain current collapse and its correlation with gate leakage.

Finally, the comparison with the AlGaN reference technology clarified the intrinsic performance–reliability trade-offs introduced by the AlScN barrier. While the enhanced polarization and carrier confinement of AlScN enable improved transconductance and transient stability, they also increase the sensitivity to electric-field–assisted degradation and donor-related traps. These insights establish the basis for future optimization of passivation interfaces, barrier composition, and buffer design, as further discussed in Chapter 7.

Chapter 7

General Conclusions and Outlook

This thesis addressed the modeling and physical understanding of degradation mechanisms in GaN-based HEMTs, with particular emphasis on the role of charge trapping phenomena under static, dynamic, and long-term stress conditions. By combining experimental measurements and calibrated TCAD simulations, the work established a coherent framework that bridges device physics and reliability modeling across different GaN HEMTs platforms, from enhancement-mode p-GaN gate devices, to conventional depletion-mode AlGaIn/GaN, and emerging AlScN/GaN technologies.

The first part of the thesis focused on the gate stack, where a comprehensive TCAD study elucidated the physical origins of leakage in p-GaN gate HEMTs. One dimensional simulations were initially employed to separate the contributions of hBT at the Schottky barrier and trap-assisted tunneling (TAT) through the AlGaIn layer. However, only two-dimensional geometries provided realistic electric-field distributions, revealing that sharp metal/p-GaN corners lead to overestimated tunneling currents. By introducing rounded gate corners and splitting the gate into central and edge regions, the simulated I_G-V_G and I_D-V_G characteristics achieved quantitative agreement with experimental data. The analysis confirmed that leakage is governed by hole transport through the Schottky barrier and by localized field enhancement at the gate periphery, while band-to-band electron tunneling plays a negligible role. These findings defined a physically consistent baseline for subsequent reliability-oriented simulations.

Building on the calibrated framework, the thesis analyzed transient and long-term degradation mechanisms in AlGaIn/GaN HEMTs under pulsed and HTRB conditions. The calibrated TCAD model, constrained by DC, pulsed, and step-stress measurements, identified two dominant defect families: deep Fe-related acceptor traps in the buffer/channel region and donor-like interface traps at the SiN/GaN-cap interface.

Under pulsed operation, a first-order analysis revealed that only the channel and buffer traps were responsible for the observed drain current collapse. This behavior

originated from the incomplete detrapping of Fe-related acceptors, whose emission time constants exceed the pulse period, leading to current collapse and an increase in V_{th} and dynamic on-resistance. A second-order analysis inspected the contribution of donor-like traps located at the passivation interface, revealing their participation in the degradation process. However, their effect was found to be limited by the presence of the negatively charged Fe-related centers in the buffer and channel, which produce a charge-compensation interplay. As a result, both acceptor and donor traps were identified as jointly responsible for the drain current degradation experienced by the device.

During HTRB stress, the degradation mechanism shifts entirely toward the field-assisted detrapping of pre-existing donor-like traps at the passivation/cap interface. In this regime, the Fe-related acceptor states in the buffer recover to equilibrium within the measurement time scale and no longer contribute to the final degradation trend. The evolution of the drain and gate currents with bias is therefore successfully reproduced by considering only donor-type traps, whose depth and concentration govern the rate and magnitude of the degradation. Possible discrepancies between expected and simulated trends can be attributed to additional trap species not included in the present setup.

Two main technological implications emerge from this analysis: (i) minimizing Fe diffusion into the channel mitigates dynamic degradation during switching operation, and (ii) optimizing the passivation/cap interface, both in donor density and energy distribution, can significantly enhance stability under reverse-bias stress.

The final part of the work extended the modeling framework to AlScN-barrier HEMTs, exploring the impact of barrier composition on performance and degradation. A dedicated TCAD setup for AlScN/GaN devices was developed and calibrated against DC, pulsed, and HTRB data, enabling direct comparison with the AlGaN reference technology. Pulsed I–V analysis revealed reduced surface-trap coupling and improved transient behavior, consistent with the enhanced polarization of AlScN. However, under HTRB step-stress, AlScN devices exhibited stronger gate-driven degradation due to their thinner barrier and higher electric-field penetration. Three concurrent mechanisms were identified: (i) under-gate acceptor trap build-up causing threshold voltage shifts, (ii) donor detrapping in the gate–drain access region leading to increased transconductance, and (iii) field-assisted gate leakage correlating with overall drain current collapse. The comparison between the two barrier technologies highlighted a fundamental trade-off between performance and reliability: while AlScN offers superior transconductance and carrier confinement, it also increases sensitivity to field-induced degradation. These results emphasize the importance of barrier engineering, interface quality, and optimized gate stack design in achieving stable

operation of next-generation GaN HEMTs.

Overall, the thesis provides a comprehensive and physically grounded understanding of charge trapping and degradation in GaN HEMTs, bridging experimental characterization and simulation. It establishes a unified TCAD-based approach that connects microscopic defect physics to macroscopic device behavior, offering both interpretive insight and practical guidance for the design of reliable, high-performance GaN technologies.

Beyond the individual device studies, the thesis established a general methodology for physics-based reliability modeling using commercial TCAD tools. The integration of calibrated transport, polarization, and trap models enabled quantitative correlation between simulation and experiment under both steady-state and stress conditions. The approach demonstrates that, with appropriate parameterization and geometry-aware modeling, TCAD can reproduce not only electrical characteristics but also degradation trends observed experimentally. This capability represents a step toward predictive simulation of device aging and provides a reference framework for future reliability-oriented process optimization.

The results presented in this thesis open several avenues for further investigation. From a modeling perspective, the inclusion of continuous trap energy distributions and time-dependent defect generation models would enable a more accurate description of long-term aging. Experimentally, combining HTRB data with complementary techniques such as DLTS, C–V dispersion, or electroluminescence mapping could provide independent constraints for trap parameter extraction. At the material level, exploring higher Sc compositions, alternative passivation schemes, optimized barrier thicknesses, and novel barrier materials beyond AlScN will be essential to further enhance the trade-off between performance and reliability. Finally, extending this modeling framework to high-frequency and high-temperature operation would further consolidate the predictive capability of TCAD in GaN reliability studies.

Bibliography

- [1] R. Baets, C. Snowden, J. Barker, *et al.*, *Semiconductor Device Modelling*. Springer London, 2012, ISBN: 9781447110330. [Online]. Available: <https://books.google.it/books?id=hSHjBwAAQBAJ>.
- [2] M. Rudan *et al.*, *Physics of semiconductor devices*. Springer, 2015.
- [3] S. M. Sze, Y. Li, and K. K. Ng, *Physics of Semiconductor Devices*. John wiley & sons, 2021.
- [4] M. Rudan, R. Brunetti, S. Reggiani, *et al.*, *Springer handbook of semiconductor devices*. Springer, 2023.
- [5] D. Schroeder, *Modelling of interface carrier transport for device simulation*. Springer Science & Business Media, 1994.
- [6] C. Herring, “Transport Properties of a Many-Valley Semiconductor,” *The Bell System Technical Journal*, vol. 34, no. 2, pp. 237–290, 1955.
- [7] T. T. Mnatsakanov, M. E. Levinshtein, L. I. Pomortseva, S. N. Yurkov, G. S. Simin, and M. A. Khan, “Carrier Mobility Model for GaN,” *Solid-State Electronics*, vol. 47, no. 1, pp. 111–115, 2003.
- [8] F. Bertazzi, M. Moresco, and E. Bellotti, “Theory of High Field Carrier Transport and Impact Ionization in Wurtzite GaN. Part I: A Full Band Monte Carlo Model,” *Journal of Applied Physics*, vol. 106, no. 6, 2009.
- [9] M Shur, B Gelmont, and M Asif Khan, “Electron Mobility in Two-Dimensional Electron Gas in AlGa_N/Ga_N Heterostructures and in Bulk Ga_N,” *Journal of electronic materials*, vol. 25, no. 5, pp. 777–785, 1996.
- [10] M. E. Levinshtein, S. L. Rumyantsev, and M. S. Shur, *Properties of Advanced Semiconductor Materials: GaN, AlN, InN, BN, SiC, SiGe*. John Wiley & Sons, 2001.
- [11] L. Balestra, F. Ercolano, E. Gnani, and S. Reggiani, “TCAD Modeling of High-Field Electron Transport in Bulk Wurtzite GaN: The Full-Band SHE-BTE,” *IEEE Access*, vol. 11, pp. 6293–6298, 2023.

- [12] A Chynoweth, “Current Understanding of HF Instabilities in Bulk Semiconductors,” in *1966 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, IEEE, vol. 9, 1966, pp. 80–81.
- [13] E. De Castro, *Fondamenti di Elettronica*. UTET, 1975.
- [14] B. Foutz, O Ambacher, M. Murphy, V Tilak, and L. Eastman, “Polarization Induced Charge at Heterojunctions of the III–V Nitrides and Their Alloys,” *physica status solidi (b)*, vol. 216, no. 1, pp. 415–418, 1999.
- [15] O Ambacher, J Smart, J. Shealy, *et al.*, “Two-Dimensional Electron Gases Induced by Spontaneous and Piezoelectric Polarization Charges in N- and Ga-face AlGa_N/Ga_N Heterostructures,” *Journal of applied physics*, vol. 85, no. 6, pp. 3222–3233, 1999.
- [16] O. Ambacher, B Foutz, J. Smart, *et al.*, “Two Dimensional Electron Gases Induced by Spontaneous and Piezoelectric Polarization in Undoped and Doped AlGa_N/Ga_N Heterostructures,” *Journal of applied physics*, vol. 87, no. 1, pp. 334–344, 2000.
- [17] J. P. Ibbetson, P. Fini, K. Ness, S. DenBaars, J. Speck, and U. Mishra, “Polarization Effects, Surface States, and the Source of Electrons in AlGa_N/Ga_N Heterostructure Field Effect Transistors,” *Applied Physics Letters*, vol. 77, no. 2, pp. 250–252, 2000.
- [18] Synopsys, *Sentaurus Device Manual*, December 2024.
- [19] T. Goudon, V. Miljanović, and C. Schmeiser, “On the Shockley–Read–Hall Model: Generation-Recombination in Semiconductors,” *SIAM Journal on Applied Mathematics*, vol. 67, no. 4, pp. 1183–1201, 2007.
- [20] A. Schenk and G. Heiser, “Modeling and Simulation of Tunneling Through Ultra-Thin Gate Dielectrics,” *Journal of applied physics*, vol. 81, no. 12, pp. 7900–7908, 1997.
- [21] M. Jeong, P. M. Solomon, S. Laux, H.-S. Wong, and D. Chidambarrao, “Comparison of Raised and Schottky Source/Drain MOSFETs Using a Novel Tunneling Contact Model,” in *International Electron Devices Meeting 1998. Technical Digest (Cat. No. 98CH36217)*, IEEE, 1998, pp. 733–736.
- [22] F. Li, S. Mudanai, Y.-Y. Fan, L. Register, and S. Banerjee, “Compact Model of Mosfet Electron Tunneling Current Through Ultra-Thin SiO₂ and High-k Gate Stacks,” in *61st Device Research Conference. Conference Digest (Cat. No. 03TH8663)*, IEEE, 2003, pp. 47–48.

- [23] M. Mandurrino, M. Goano, M. Vallone, *et al.*, “Semiclassical simulation of trap-assisted tunneling in GaN-based light-emitting diodes,” *Journal of Computational Electronics*, vol. 14, no. 2, pp. 444–455, 2015.
- [24] A Palma, A Godoy, J. Jimenez-Tejada, J. Carceller, and J. Lopez-Villanueva, “Quantum Two-Dimensional Calculation of time Constants of Random Telegraph Signals in Metal-Oxide–Semiconductor Structures,” *Physical Review B*, vol. 56, no. 15, p. 9565, 1997.
- [25] F Jiménez-Molinos, F Gámiz, A Palma, P Cartujo, and J. López-Villanueva, “Direct and Trap-Assisted Elastic Tunneling Through Ultrathin Gate Oxides,” *Journal of Applied Physics*, vol. 91, no. 8, pp. 5116–5124, 2002.
- [26] E. Kioupakis, P. Rinke, K. T. Delaney, and C. G. Van de Walle, “Indirect Auger Recombination as a Cause of Efficiency Drop in Nitride Light-Emitting Diodes,” *Applied Physics Letters*, vol. 98, no. 16, 2011.
- [27] E. Mitani, H. Haematsu, S. Yokogawa, J. Nikaido, and Y. Tateno, “Mass Production of High Voltage GaAs and GaN Devices,” in *cs mantech conference*, 2006, pp. 24–27.
- [28] T Mimura, N Yokoyama, H Kusakawa, K Suyama, and M Fukuta, “GaAs MOSFET for Low-Power High-Speed Logic Applications,” in *IEEE TRANSACTIONS ON ELECTRON DEVICES*, IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC 345 E 47TH ST, NEW YORK, NY . . . , vol. 26, 1979, pp. 1828–1828.
- [29] M Asif Khan, A Bhattarai, J. Kuznia, and D. Olson, “High Electron Mobility Transistor Based on a $GaN - Al_xGa_{1-x}N$ Heterojunction,” *Applied Physics Letters*, vol. 63, no. 9, pp. 1214–1215, 1993.
- [30] M. Meneghini, G. Meneghesso, and E. Zanoni, “Power GaN Devices: Materials, Applications and Reliability,” 2017.
- [31] B. J. Baliga, *Wide Bandgap Semiconductor Power Devices: Materials, Physics, Design, and Applications*. Woodhead Publishing, 2018.
- [32] B. J. Baliga, “Power Semiconductor Device Figure of Merit for High-Frequency Applications,” *IEEE Electron Device Letters*, vol. 10, no. 10, pp. 455–457, 2002.
- [33] A. Lidow, M. De Rooij, J. Strydom, D. Reusch, and J. Glaser, *GaN Transistors for Efficient Power Conversion*. John Wiley & Sons, 2019.
- [34] Q. Zheng, C. Li, A. Rai, J. H. Leach, D. A. Broido, and D. G. Cahill, “Thermal Conductivity of GaN, ^{71}GaN , and SiC from 150 K to 850 K,” *Physical Review Materials*, vol. 3, no. 1, p. 014 601, 2019.

- [35] M. S. B. Hoque, Y. R. Koh, J. L. Braun, *et al.*, “High In-Plane Thermal Conductivity of Aluminum Nitride Thin Films,” *ACS nano*, vol. 15, no. 6, pp. 9588–9599, 2021.
- [36] E. Sichel and J. Pankove, “Thermal Conductivity of GaN, 25–360 K,” *Journal of physics and chemistry of solids*, vol. 38, no. 3, p. 330, 1977.
- [37] U. K. Mishra, L. Shen, T. E. Kazior, and Y.-F. Wu, “GaN-Based RF Power Devices and Amplifiers,” *Proceedings of the IEEE*, vol. 96, no. 2, pp. 287–305, 2008.
- [38] D. C. Look and J. Sizelove, “Predicted Maximum Mobility in Bulk GaN,” *Applied Physics Letters*, vol. 79, no. 8, pp. 1133–1135, 2001.
- [39] M. Meneghini, C. De Santi, I. Abid, *et al.*, “GaN-based power devices: Physics, reliability, and perspectives,” *Journal of Applied Physics*, vol. 130, no. 18, 2021.
- [40] I. Streicher, S. Leone, M. Zhang, *et al.*, “Understanding Interfaces in AlScN/GaN Heterostructures,” *Advanced Functional Materials*, p. 2403027, 2024.
- [41] I. Streicher, S. Leone, C. Manz, *et al.*, “Effect of AlN and AlGaIn interlayers on AlScN/GaN heterostructures grown by metal–organic chemical vapor deposition,” *Crystal Growth & Design*, vol. 23, no. 2, pp. 782–791, 2023.
- [42] I. Streicher, S. Leone, L. Kirste, *et al.*, “Enhanced AlScN/GaN Heterostructures Grown With a Novel Precursor by Metal–Organic Chemical Vapor Deposition,” *physica status solidi–Rapid Research Letters*, vol. 17, no. 2, p. 2200387, 2023.
- [43] F. Roccaforte, G. Greco, P. Fiorenza, and F. Iucolano, “An Overview of Normally-Off GaN-Based High Electron Mobility Transistors,” *Materials*, vol. 12, no. 10, 2019, ISSN: 1996-1944. doi: 10.3390/ma12101599. [Online]. Available: <https://www.mdpi.com/1996-1944/12/10/1599>.
- [44] T.-L. Wu, S.-W. Tang, and H.-J. Jiang, “Investigation of Recessed Gate AlGaIn/GaN MIS-HEMTs with Double AlGaIn Barrier Designs Toward an Enhancement-Mode Characteristic,” *Micromachines*, vol. 11, no. 2, p. 163, 2020.
- [45] R. Wang, P. Saunier, Y. Tang, *et al.*, “Enhancement-Mode InAlN/AlN/GaN HEMTs With 10^{-12} A/mm Leakage Current and 10^{12} On/Off Current Ratio,” *IEEE electron device letters*, vol. 32, no. 3, pp. 309–311, 2011.
- [46] B. Sensale-Rodriguez, J. Guo, R. Wang, *et al.*, “Time Delay Analysis in High Speed Gate-Recessed E-mode InAlN HEMTs,” *Solid-state electronics*, vol. 80, pp. 67–71, 2013.

- [47] C. Miersch, S. Seidel, A. Schmid, T. Fuhs, J. Heitmann, and F. C. Beyer, "Morphological and Electrical Characterization of Gate Recessed AlGa_N/Ga_N High Electron Mobility Transistor Device by Purge-Free Atomic Layer Etching," *Journal of Vacuum Science & Technology A*, vol. 42, no. 2, 2024.
- [48] Y. Cai, Y. Zhou, K. M. Lau, and K. J. Chen, "Control of Threshold Voltage of AlGa_N/Ga_N HEMTs by Fluoride-Based Plasma Treatment: From Depletion Mode to Enhancement Mode," *IEEE transactions on electron devices*, vol. 53, no. 9, pp. 2207–2215, 2006.
- [49] Z. Gao, B. Hou, Y. Liu, and X. Ma, "Impact of Fluorine Plasma Treatment on AlGa_N/Ga_N High Electronic Mobility Transistors by Simulated and Experimental Results," *Microelectronic Engineering*, vol. 154, pp. 22–25, 2016.
- [50] N. Sun, H. Huang, Z. Sun, *et al.*, "Improving Gate Reliability of 6-in E-mode Ga_N-based MIS-HEMTs by Employing Mixed Oxygen and Fluorine Plasma Treatment," *IEEE Transactions on Electron Devices*, vol. 69, no. 1, pp. 82–87, 2021.
- [51] M. Meneghini, O. Hilt, J. Wuerfl, and G. Meneghesso, "Technology and reliability of normally-off Ga_N HEMTs with p-type gate," *Energies*, vol. 10, no. 2, p. 153, 2017.
- [52] G. Greco, F. Iucolano, and F. Roccaforte, "Review of Technology for Normally-Off HEMTs with p-Ga_N Gate," *Materials Science in Semiconductor Processing*, vol. 78, pp. 96–106, 2018.
- [53] Z. Wang, J. Nan, Z. Tian, P. Liu, Y. Wu, and J. Zhang, "Review on Main Mate Characteristics of P-type Ga_N Gate High-Electron-Mobility Transistors," *Micromachines*, vol. 15, no. 1, p. 80, 2023.
- [54] J. Ajayan, A. K. Panigrahy, S. Sen, M. Kumar, and S. Tayal, "Reliability Issues and Degradation Mechanisms of p-Ga_N Gated E-Mode AlGa_N/Ga_N Power HEMTs: A Critical Review," *IEEE Access*, 2025.
- [55] M. Zhu, G. Li, H. Li, *et al.*, "Challenges and advancements in p-Ga_N gate based high electron mobility transistors (HEMTs) on silicon substrates," *Journal of Materials Chemistry C*, 2024.
- [56] A. N. Tallarico, S. Stoffels, P. Magnone, *et al.*, "Investigation of the p-Ga_N gate breakdown in forward-biased Ga_N-based power HEMTs," *IEEE Electron Device Letters*, vol. 38, no. 1, pp. 99–102, 2016.

- [57] A. N. Tallarico, S. Stoffels, N. Posthuma, S. Decoutere, E. Sangiorgi, and C. Fiegna, "Threshold Voltage Instability in GaN HEMTs With p-Type Gate: Mg Doping Compensation," *IEEE Electron Device Letters*, vol. 40, no. 4, pp. 518–521, 2019. doi: 10.1109/LED.2019.2897911.
- [58] A. N. Tallarico, M. Millesimo, B. Bakeroot, *et al.*, "TCAD Modeling of the Dynamic VTH Hysteresis Under Fast Sweeping Characterization in p-GaN Gate HEMTs," *IEEE Transactions on Electron Devices*, vol. 69, no. 2, pp. 507–513, 2022. doi: 10.1109/TED.2021.3134928.
- [59] J. Li, Y. Yin, N. Zeng, *et al.*, "Normally-off AlGaN/AlN/GaN HEMT with a composite recessed gate," *Superlattices and Microstructures*, vol. 161, p. 107 064, 2022.
- [60] S. Nakamura *et al.*, "GaN growth using GaN buffer layer," *Jpn. J. Appl. Phys.*, vol. 30, no. 10A, pp. L1705–L1707, 1991.
- [61] T Yoshida, Y Oshima, T Eri, K Watanabe, M Shibata, and T Mishima, "Preparation of 3 inch freestanding GaN substrates by hydride vapor phase epitaxy with void-assisted separation," *physica status solidi (a)*, vol. 205, no. 5, pp. 1053–1055, 2008.
- [62] I. B. Rowena, S. L. Selvaraj, and T. Egawa, "Buffer thickness contribution to suppress vertical leakage current with high breakdown field (2.3 MV/cm) for GaN on Si," *IEEE Electron Device Letters*, vol. 32, no. 11, pp. 1534–1536, 2011.
- [63] S. L. Selvaraj, A. Watanabe, A. Wakejima, and T. Egawa, "1.4-kV breakdown voltage for AlGaIn/GaN high-electron-mobility transistors on silicon substrate," *IEEE electron device letters*, vol. 33, no. 10, pp. 1375–1377, 2012.
- [64] S. Chowdhury, "GaN-on-GaN power device design and fabrication," in *Wide Bandgap Semiconductor Power Devices*, Elsevier, 2019, pp. 209–248.
- [65] K. Xu, J. Wang, G. Ren, and Z. Liu, "Ammonothermal Method," in *GaN Single Crystal Growth and Application*, Springer, 2025, pp. 119–139.
- [66] D. Zhao, S. Xu, M. Xie, S. Tong, and H. Yang, "Stress and its effect on optical properties of GaN epilayers grown on Si (111), 6H-SiC (0001), and c-plane sapphire," *Applied physics letters*, vol. 83, no. 4, pp. 677–679, 2003.
- [67] A. Jarndal, L. Arivazhagan, and D. Nirmal, "On the performance of GaN-on-Silicon, Silicon-Carbide, and Diamond substrates," *International Journal of RF and Microwave Computer-Aided Engineering*, vol. 30, no. 6, e22196, 2020. doi: <https://doi.org/10.1002/mmce.22196>. eprint: <https://onlinelibrary.wiley.com/doi/pdf/10.1002/mmce.22196>.

- [Online]. Available: <https://onlinelibrary.wiley.com/doi/abs/10.1002/mmce.22196>.
- [68] E. B. Yakimov, A. Y. Polyakov, I.-H. Lee, and S. J. Pearton, "Recombination properties of dislocations in GaN," *Journal of Applied Physics*, vol. 123, no. 16, 2018.
- [69] Y. Yao, S. Huang, R. Cao, *et al.*, "Dislocation-assisted electron and hole transport in GaN epitaxial layers," *Nature Communications*, vol. 16, no. 1, p. 6448, 2025.
- [70] H. Aida, H. Takeda, N. Aota, and K. Koyama, "Reduction of bowing in GaN-on-sapphire and GaN-on-silicon substrates by stress implantation by internally focused laser processing," *Japanese Journal of Applied Physics*, vol. 51, no. 1R, p. 016 504, 2011.
- [71] S. Besendörfer, E. Meissner, T. Zweipfennig, *et al.*, "Interplay between C-doping, threading dislocations, breakdown, and leakage in GaN on Si HEMT structures," *AIP Advances*, vol. 10, no. 4, 2020.
- [72] L.-H. Hsu, Y.-Y. Lai, P.-T. Tu, *et al.*, "Development of GaN HEMTs fabricated on silicon, silicon-on-insulator, and engineered substrates and the heterogeneous integration," *Micromachines*, vol. 12, no. 10, p. 1159, 2021.
- [73] R. Kucharski, T. Sochacki, B. Lucznik, and M. Bockowski, "Growth of bulk GaN crystals," *Journal of Applied Physics*, vol. 128, no. 5, 2020.
- [74] J. K. Hite, "A review of homoepitaxy of III-nitride semiconductors by metal organic chemical vapor deposition and the effects on vertical devices," *Crystals*, vol. 13, no. 3, p. 387, 2023.
- [75] B. Setera and A. Christou, "Impact of threading dislocations in GaN power switching devices," *ECS Transactions*, vol. 102, no. 3, p. 25, 2021.
- [76] C. Soh, S. Chua, H. Lim, D. Chi, W. Liu, and S. Tripathy, "Identification of deep levels in GaN associated with dislocations," *Journal of Physics: Condensed Matter*, vol. 16, no. 34, p. 6305, 2004.
- [77] S. Besendörfer, E. Meissner, F. Medjdoub, J. Derluyn, J. Friedrich, and T. Erlbacher, "The impact of dislocations on AlGaIn/GaN Schottky diodes and on gate failure of high electron mobility transistors," *Scientific reports*, vol. 10, no. 1, p. 17 252, 2020.
- [78] A.-C. Liu, P.-T. Tu, C. Langpoklakpam, *et al.*, "The Evolution of Manufacturing Technology for GaN Electronic Devices," *Micromachines*, vol. 12, no. 7, 2021, ISSN: 2072-666X. DOI: 10.3390/mi12070737. [Online]. Available: <https://www.mdpi.com/2072-666X/12/7/737>.

- [79] S. Leone, F. Benkhelifa, L. Kirste, *et al.*, “Suppression of Iron Memory Effect in GaN Epitaxial Layers,” *physica status solidi (b)*, vol. 255, no. 5, p. 1700377, 2018. doi: <https://doi.org/10.1002/pssb.201700377>. eprint: <https://onlinelibrary.wiley.com/doi/pdf/10.1002/pssb.201700377>. [Online]. Available: <https://onlinelibrary.wiley.com/doi/abs/10.1002/pssb.201700377>.
- [80] D. S. Arteev, A. V. Sakharov, W. V. Lundin, *et al.*, “Influence of doping profile of GaN:Fe buffer layer on the properties of AlGaN/AlN/GaN heterostructures for high-electron mobility transistors,” *Journal of Physics: Conference Series*, vol. 1697, no. 1, p. 012206, 2020. doi: 10.1088/1742-6596/1697/1/012206. [Online]. Available: <https://dx.doi.org/10.1088/1742-6596/1697/1/012206>.
- [81] N. Zagni, F. Puglisi, P. Pavan, A. Chini, and G. Verzellesi, “Insights into the off-state breakdown mechanisms in power GaN HEMTs,” *Microelectronics Reliability*, vol. 100, p. 113374, 2019.
- [82] N. Zagni, A. Chini, F. M. Puglisi, P. Pavan, and G. Verzellesi, “The Role of Carbon Doping on Breakdown, Current Collapse, and Dynamic On-Resistance Recovery in AlGaN/GaN High Electron Mobility Transistors on Semi-Insulating SiC Substrates,” *physica status solidi (a)*, vol. 217, no. 7, p. 1900762, 2020.
- [83] S. Yamaguchi, M. Kosaki, Y. Watanabe, *et al.*, “Metalorganic vapor phase epitaxy growth of crack-free AlN on GaN and its application to high-mobility AlN/GaN superlattices,” *Applied Physics Letters*, vol. 79, no. 19, pp. 3062–3064, 2001.
- [84] J. Freedman, A. Watanabe, Y. Yamaoka, T. Kubo, and T. Egawa, “Influence of AlN nucleation layer on vertical breakdown characteristics for GaN-on-Si,” *physica status solidi (a)*, vol. 213, no. 2, pp. 424–428, 2016.
- [85] T. Novák, P. Kostelník, M. Konečný, J. Čechal, M. Kolíbal, and T. Šíkola, “Temperature effect on Al predose and AlN nucleation affecting the buffer layer performance for the GaN-on-Si based high-voltage devices,” *Japanese Journal of Applied Physics*, vol. 58, no. SC, SC1018, 2019.
- [86] S. Chang, M. Zhao, V. Spampinato, A. Franquet, and L. Chang, “The influence of AlN nucleation layer on RF transmission loss of GaN buffer on high resistivity Si (111) substrate,” *Semiconductor Science and Technology*, vol. 35, no. 3, p. 035029, 2020.

- [87] G. Meneghesso, G. Verzellesi, F. Danesin, *et al.*, “Reliability of GaN High-Electron-Mobility Transistors: State of the Art and Perspectives,” *IEEE Transactions on Device and Materials Reliability*, vol. 8, no. 2, pp. 332–343, 2008. doi: 10.1109/TDMR.2008.923743.
- [88] F. Ercolano, L. Balestra, S. Krause, *et al.*, “Role of trapping/detrapping in HTRB Stress and pulsed DC conditions in AlGa_N/Ga_N HEMTs analyzed via TCAD simulations,” in *2023 IEEE International Integrated Reliability Workshop (IIRW)*, IEEE, 2023, pp. 1–7.
- [89] F. Ercolano, L. Balestra, S. Leone, *et al.*, “TCAD analysis of the high-temperature reverse-bias stress on AlGa_N/Ga_N HEMTs,” *Power Electronic Devices and Components*, p. 100 080, 2025.
- [90] B. Hult, *Design, Fabrication and Characterization of GaN HEMTs for Power Switching Applications*. Chalmers Tekniska Hogskola (Sweden), 2022.
- [91] S. Ghosh, M. Frentrup, A. M. Hinz, *et al.*, “Buffer-Less Gallium Nitride High Electron Mobility Heterostructures on Silicon,” *Advanced Materials*, vol. 37, no. 9, p. 2 413 127, 2025.
- [92] F. De Pieri, M. Fornasier, V. G. Zhan, *et al.*, “Self-induced photoionization of traps in buffer-free AlGa_N/Ga_N HEMTs,” *IEEE Electron Device Letters*, 2024.
- [93] F. De Pieri, M. Fregolent, M. Saro, *et al.*, “Comprehensive Analysis of Deep level Effects and in-situ Photoionization in 0.15 μ m buffer-free AlGa_N/Ga_N HEMTs for RF applications,” in *2025 IEEE International Reliability Physics Symposium (IRPS)*, IEEE, 2025, pp. 1–5.
- [94] N. Kurz, F. Parsapour, V. Pashchenko, *et al.*, “Determination of Elastic and Piezoelectric Properties of Al_{0.84}Sc_{0.16}N Thin Films,” in *2018 IEEE International Ultrasonics Symposium (IUS)*, 2018, pp. 1–5. doi: 10.1109/ULTSYM.2018.8579706.
- [95] O. Rogall, N. M. Feil, A. Ding, *et al.*, “Determining Elastic Constants of AlScN Films on Silicon Substrates by Laser Ultrasonics,” in *2020 IEEE International Ultrasonics Symposium (IUS)*, 2020, pp. 1–4. doi: 10.1109/IUS46767.2020.9251632.
- [96] O. Ambacher, S. Mihalic, M. Yassine, A. Yassine, N. Afshar, and B. Christian, “Structural, Elastic, and Thermodynamic Properties of Cubic and Hexagonal Sc_xAl_{1-x}N Crystals,” *Journal of Applied Physics*, vol. 134, no. 16, 2023.

- [97] M. A. Caro, S. Zhang, T. Riekkinen, *et al.*, “Piezoelectric Coefficients and Spontaneous Polarization of ScAlN,” *Journal of Physics: Condensed Matter*, vol. 27, no. 24, p. 245 901, 2015.
- [98] O. Ambacher, B Christian, M. Yassine, M. Baeumler, S. Leone, and R. Quay, “Polarization Induced Interface and Electron Sheet Charges of Pseudomorphic ScAlN/GaN, GaAlN/GaN, InAlN/GaN, and InAlN/InN Heterostructures,” *Journal of Applied Physics*, vol. 129, no. 20, 2021.
- [99] S. Krause, P. Döring, I. Streicher, P. Waltereit, P. Brückner, and S. Leone, “(Invited) Recent Advances and Challenges of MOCVD-Grown AlScN/GaN HEMTs,” *ECS Meeting Abstracts*, vol. MA2023-02, no. 32, p. 1578, 2023. doi: 10.1149/MA2023-02321578mtgabs. [Online]. Available: <https://dx.doi.org/10.1149/MA2023-02321578mtgabs>.
- [100] G. Perillat-Merceroz, G. Cosendey, J.-F. Carlin, R. Butté, and N. Grandjean, “Intrinsic degradation mechanism of nearly lattice-matched InAlN layers grown on GaN substrates,” *Journal of Applied Physics*, vol. 113, no. 6, 2013.
- [101] J. Manuel, F. Morales, J. Lozano, *et al.*, “Structural and compositional homogeneity of InAlN epitaxial layers nearly lattice-matched to GaN,” *Acta Materialia*, vol. 58, no. 12, pp. 4120–4125, 2010.
- [102] S Ravi, C Priya, A Mohanbabu, S Maheswari, A Lakshmi Narayana, and P Murugapandiyam, “Lattice-matched InAlN/GaN high-electron-mobility transistors (HEMTs),” *Journal of Materials Science*, pp. 1–55, 2025.
- [103] I. Streicher, “Epitaxy of novel AlScN/GaN and AlYN/GaN heterostructures by metal-organic chemical vapour deposition,” Ph.D. dissertation, Dissertation, Universität Freiburg, 2024, 2024.
- [104] S. Krause, I. Streicher, P. Waltereit, L. Kirste, P. Brückner, and S. Leone, “AlScN/GaN HEMTs Grown by Metal-Organic Chemical Vapor Deposition With 8.4 W/mm Output Power and 48% Power-Added Efficiency at 30 GHz,” *IEEE Electron Device Letters*, vol. 44, no. 1, pp. 17–20, 2022.
- [105] H. Zhang, M. Zhang, H. Wang, *et al.*, “Thick-AlN-barrier AlN/GaN-based HEMTs with superior power and noise performance for low-voltage RF front-end applications,” *Applied Physics Letters*, vol. 126, no. 12, 2025.
- [106] L. Qin, J. Zhu, Q. Zhu, *et al.*, “High-Efficiency AlN/GaN HEMTs With High-Quality Stacked Gate Dielectrics on Si Substrate for K-and Ka-Band Applications,” *IEEE Transactions on Electron Devices*, 2025.

- [107] C. Cao, S. I. Rahman, C. Chae, *et al.*, “In situ SiN/AlN/GaN HEMTs with regrown contacts using selective etching,” *Applied Physics Express*, vol. 18, no. 3, p. 036 501, 2025.
- [108] S. Kim, E. Kim, H. Walwil, *et al.*, “Thermal characterization and design of AlN/GaN/AlN HEMTs on foreign substrates,” *IEEE Electron Device Letters*, 2025.
- [109] L. Balestra, E. Gnani, and S. Reggiani, “Electron effective masses of $\text{Sc}_x\text{Al}_{1-x}\text{N}$ and $\text{Al}_x\text{Ga}_{1-x}\text{N}$ from first-principles calculations of unfolded band structure,” *Journal of Applied Physics*, vol. 132, no. 21, p. 215 108, Dec. 2022, issn: 0021-8979. doi: 10.1063/5.0115512. eprint: https://pubs.aip.org/aip/jap/article-pdf/doi/10.1063/5.0115512/16521706/215108_1/_online.pdf. [Online]. Available: <https://doi.org/10.1063/5.0115512>.
- [110] B. S. Eller, J. Yang, and R. J. Nemanich, “Electronic surface and dielectric interface states on GaN and AlGa_N,” *Journal of Vacuum Science & Technology A*, vol. 31, no. 5, 2013.
- [111] R. Vetury, N. Q. Zhang, S. Keller, and U. K. Mishra, “The impact of surface states on the DC and RF characteristics of AlGa_N/GaN HFETs,” *IEEE Transactions on electron devices*, vol. 48, no. 3, pp. 560–566, 2002.
- [112] H. Hasegawa, T. Inagaki, S. Ootomo, and T. Hashizume, “Mechanisms of current collapse and gate leakage currents in AlGa_N/GaN heterostructure field effect transistors,” *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena*, vol. 21, no. 4, pp. 1844–1855, 2003.
- [113] S. Karmalkar and U. K. Mishra, “Enhancement of breakdown voltage in Al-GaN/GaN high electron mobility transistors using a field plate,” *IEEE transactions on electron devices*, vol. 48, no. 8, pp. 1515–1521, 2002.
- [114] W. Saito, Y. Kakiuchi, T. Nitta, *et al.*, “Field-plate structure dependence of current collapse phenomena in high-voltage GaN-HEMTs,” *IEEE Electron Device Letters*, vol. 31, no. 7, pp. 659–661, 2010.
- [115] F. Ercolano, A. N. Tallarico, M. Millesimo, *et al.*, “GaN HEMT with p-Type Schottky gate: A case study of TCAD modeling of the gate leakage current,” in *Annual meeting of the Italian electronics society*, Springer, 2023, pp. 288–297.

- [116] S. Mizuno, Y. Ohno, S. Kishimoto, K. Maezawa, and T. Mizutani, "Large gate leakage current in AlGa_N/Ga_N high electron mobility transistors," *Japanese journal of applied physics*, vol. 41, no. 8R, p. 5125, 2002.
- [117] J. Carrano, T Li, P. Grudowski, C. Eiting, R. Dupuis, and J. Campbell, "Current transport mechanisms in Ga_N-based metal–semiconductor–metal photodetectors," *Applied physics letters*, vol. 72, no. 5, pp. 542–544, 1998.
- [118] C.-F. Shih, K. Hung, C. Hsiao, S. Shu, and W. Li, "Investigations of Ga_N metal-oxide-semiconductor capacitors with sputtered *HfO*₂ gate dielectrics," *Journal of alloys and compounds*, vol. 480, no. 2, pp. 541–546, 2009.
- [119] X. Cao, S. Pearton, G Dang, A. Zhang, F Ren, and J. Van Hove, "Effects of interfacial oxides on Schottky barrier contacts to n-and p-type Ga_N," *Applied Physics Letters*, vol. 75, no. 26, pp. 4130–4132, 1999.
- [120] E. Miller, E. Yu, P Waltereit, and J. Speck, "Analysis of reverse-bias leakage current mechanisms in Ga_N grown by molecular-beam epitaxy," *Applied physics letters*, vol. 84, no. 4, pp. 535–537, 2004.
- [121] B. Lambert, N. Labat, D. Carisetti, *et al.*, "Evidence of relationship between mechanical stress and leakage current in AlGa_N/Ga_N transistor after storage test," *Microelectronics Reliability*, vol. 52, no. 9-10, pp. 2184–2187, 2012.
- [122] A Fontserè, A. Perez-Tomas, M. Placidi, *et al.*, "Gate current analysis of AlGa_N/Ga_N on silicon heterojunction transistors at the nanoscale," *Applied physics letters*, vol. 101, no. 9, 2012.
- [123] Z. Liu, G. Ng, S Arulkumaran, Y. Maung, and H Zhou, "Temperature-dependent forward gate current transport in atomic-layer-deposited *Al*₂*O*₃/AlGa_N/Ga_N metal-insulator-semiconductor high electron mobility transistor," *Applied Physics Letters*, vol. 98, no. 16, 2011.
- [124] A. Tallarico, S Stoffels, N Posthuma, *et al.*, "Gate Reliability of p-Ga_N HEMT with Gate Metal Retraction," *IEEE Transactions on Electron Devices*, vol. 66, no. 11, pp. 4829–4835, 2019.
- [125] A. Tallarico, M Millesimo, B Bakeroot, *et al.*, "TCAD Modeling of the Dynamic *V*_{th} Hysteresis Under Fast Sweeping Characterization in p-Ga_N Gate HEMTs," *IEEE Transactions on Electron Devices*, vol. 69, no. 2, pp. 507–513, 2021.

- [126] P. Vigneshwara Raja, J.-C. Nallatamby, N. DasGupta, and A. DasGupta, "Trapping effects on AlGa_N/Ga_N HEMT characteristics," *Solid-State Electronics*, vol. 176, p. 107 929, 2021, issn: 0038-1101. doi: <https://doi.org/10.1016/j.sse.2020.107929>. [Online]. Available: <https://www.sciencedirect.com/science/article/pii/S0038110120303968>.
- [127] F. Marino, N. Faralli, D. Ferry, S. Goodnick, and M. Saraniti, "Figures of merit in high-frequency and high-power Ga_N HEMTs," in *Journal of Physics: Conference Series*, IOP Publishing, vol. 193, 2009, p. 012 040.
- [128] R. L. Coffie, "High power high frequency transistors: a material's perspective," in *High-Frequency Ga_N Electronic Devices*, Springer, 2019, pp. 5–41.
- [129] S. Huang, K. Wei, G. Liu, *et al.*, "High- f_{MAX} High Johnson's Figure-of-Merit 0.2- μ m Gate AlGa_N/Ga_N HEMTs on Silicon Substrate With Al_N/Si_N_x Passivation," *IEEE electron device letters*, vol. 35, no. 3, pp. 315–317, 2014.
- [130] R. Ye, X. Cai, C. Du, *et al.*, "An overview on analyses and suppression methods of trapping effects in AlGa_N/Ga_N HEMTs," *IEEE Access*, vol. 10, pp. 21 759–21 773, 2021.
- [131] A. Stockman, F. Masin, M. Meneghini, *et al.*, "Gate conduction mechanisms and lifetime modeling of p-gate AlGa_N/Ga_N high-electron-mobility transistors," *IEEE Transactions on Electron Devices*, vol. 65, no. 12, pp. 5365–5372, 2018.
- [132] N. Rai, R. Sarkar, A. Mahajan, A. Laha, D. Saha, and S. Ganguly, "Analysis and modeling of reverse-biased gate leakage current in AlGa_N/Ga_N high electron mobility transistors," *Journal of Applied Physics*, vol. 134, no. 24, 2023.
- [133] C. Baylis and L. Dunleavy, "Understanding pulsed IV measurement waveforms," in *The 11th IEEE International Symposium on Electron Devices for Microwave and Optoelectronic Applications, 2003. EDMO 2003.*, IEEE, 2003, pp. 223–228.
- [134] G. P. Gibiino, C. Florian, A. Santarelli, T. Cappello, and Z. Popović, "Isotrap pulsed IV characterization of Ga_N HEMTs for PA design," *IEEE Microwave and Wireless Components Letters*, vol. 28, no. 8, pp. 672–674, 2018.
- [135] B. M. Paine, S. R. Polmanter, V. T. Ng, N. T. Kubota, and C. R. Ignacio, "Fast-pulsed characterization of RF Ga_N HEMTs in lifetest systems," *IEEE Transactions on Device and Materials Reliability*, vol. 17, no. 1, pp. 130–137, 2016.

- [136] S. Yang, Z. Tang, M. Hua, *et al.*, “Investigation of SiN_x and AlN passivation for AlGaIn/GaN high-electron-mobility transistors: Role of interface traps and polarization charges,” *IEEE Journal of the Electron Devices Society*, vol. 8, pp. 358–364, 2020.
- [137] O. Chihani, L. Theolier, J.-Y. Deletage, E. Woïrgard, A. Bensoussan, and A. Durier, “Temperature and voltage effects on HTRB and HTGB stresses for AlGaIn/GaN HEMTs,” in *2018 IEEE International Reliability Physics Symposium (IRPS)*, IEEE, 2018, P–RT.
- [138] P. V. Raja, J.-C. Nallatamby, M. Bouslama, *et al.*, “HTRB Stress Effects on Static and Dynamic Characteristics of 0.15 μm AlGaIn/GaN HEMTs,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 71, no. 5, pp. 1957–1966, 2022.
- [139] L. Tang, J. Zhou, B. Qiu, *et al.*, “A Comprehensive Study on Device Reliability and Failure Mechanism of 650V p-GaN Gate HEMTs Under Long-Term HTRB Stress Beyond 150° C,” in *2025 37th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, IEEE, 2025, pp. 189–192.
- [140] P. Waltereit, W. Bronner, R. Quay, *et al.*, “GaN HEMT and MMIC development at Fraunhofer IAF: performance and reliability,” *physica status solidi (a)*, vol. 206, no. 6, pp. 1215–1220, 2009.
- [141] Synopsys, *Synopsys TCAD, Technology Computer Aided Design (TCAD)*, January 2025. [Online]. Available: <https://www.synopsys.com/manufacturing/tcad.html?utm>.
- [142] Silvaco Group, *Silvaco TCAD: Introduction and the Basics*, January 2025. [Online]. Available: <https://silvaco.com/webinar/silvaco-tcad-introduction-and-the-basics-part-1/>.
- [143] C. Medina-Bailon, T. Dutta, A. Rezaei, *et al.*, “Simulation and modeling of novel electronic device architectures with NESS (nano-electronic simulation software): A modular nano TCAD simulation framework,” *Micromachines*, vol. 12, no. 6, p. 680, 2021.
- [144] S. Strauss, A. Erlebach, T. Cilento, D. Marcon, S. Stoffels, and B. Bakeroort, “TCAD methodology for simulation of GaN-HEMT power devices,” in *2014 IEEE 26th International Symposium on Power Semiconductor Devices & IC’s (ISPSD)*, IEEE, 2014, pp. 257–260.
- [145] O. Demchenko, D. Zykov, and N. Kurbanova, “Research possibilities of Silvaco TCAD for physical simulation of gallium nitride power transistor,” in *AIP Conference Proceedings*, AIP Publishing LLC, vol. 1772, 2016, p. 060 007.

- [146] C. K. Maiti, *Introducing technology computer-aided design (TCAD): fundamentals, simulations, and applications*. Jenny Stanford Publishing, 2017.
- [147] I. Bork, V. Moroz, L. Bomholt, and D. Pramanik, “Trends, Demands and Challenges in TCAD,” *Materials Science and Engineering: B*, vol. 124, pp. 81–85, 2005.
- [148] P. Pfäffli, H. Y. Wong, X Xu, *et al.*, “TCAD Modeling for Reliability,” *Microelectronics Reliability*, vol. 88, pp. 1083–1089, 2018.
- [149] I. Martin-Bragado, R. Borges, J. P. Balbuena, and M. Jaraiz, “Kinetic Monte Carlo simulation for semiconductor processing: A review,” *Progress in Materials Science*, vol. 92, pp. 1–32, 2018.
- [150] W. Fichtner, D. J. Rose, and R. E. Bank, “Semiconductor device simulation,” *SIAM Journal on Scientific and Statistical Computing*, vol. 4, no. 3, pp. 391–415, 1983.
- [151] S. Li and S. Li, *3D TCAD Simulation for Semiconductor Processes, Devices and Optoelectronics*. Springer Science & Business Media, 2011.
- [152] S. K. Saha, “Managing technology CAD for competitive advantage: An efficient approach for integrated circuit fabrication technology development,” *IEEE Transactions on Engineering Management*, vol. 46, no. 2, pp. 221–229, 1999.
- [153] L. De Cilladi, T. Corradino, G.-F. Dalla Betta, C. Neubüser, and L. Pancheri, “Fully depleted monolithic active microstrip sensors: TCAD simulation study of an innovative design concept,” *Sensors*, vol. 21, no. 6, p. 1990, 2021.
- [154] T. Dutta, C. Medina-Bailon, A. Rezaei, *et al.*, “TCAD simulation of novel semiconductor devices,” in *2021 IEEE 14th International Conference on ASIC (ASICON)*, IEEE, 2021, pp. 1–4.
- [155] S. Myung, J. Kim, Y. Jeon, *et al.*, “Real-time TCAD: A new paradigm for TCAD in the artificial intelligence era,” in *2020 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, IEEE, 2020, pp. 347–350.
- [156] K. F. Brennan, E. Bellotti, M. Farahmand, *et al.*, “Materials theory based modeling of wide band gap semiconductors: from basic properties to devices,” *Solid-State Electronics*, vol. 44, no. 2, pp. 195–204, 2000.
- [157] S. Stoffels, N. Posthuma, S. Decoutere, *et al.*, “Perimeter Driven Transport in the p-GaN Gate as a Limiting Factor for Gate Reliability,” in *2019 IEEE International Reliability Physics Symposium (IRPS)*, IEEE, 2019, pp. 1–10.

- [158] C. Miccoli, V. Cerantonio, A. Chini, and F. Iucolano, “T-CAD Simulations Study on Drain Leakage Current and its Correlation with Gate Current for AlGa_N/Ga_N HEMTs,” in *2021 IEEE 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, IEEE, 2021, pp. 255–258.
- [159] A. Minetto, N. Modolo, L. Sayadi, *et al.*, “Drain Field Plate Impact on the Hard-Switching Performance of AlGa_N/Ga_N HEMTs,” *IEEE Transactions on Electron Devices*, vol. 68, no. 10, pp. 5003–5008, 2021.
- [160] V. Joshi, S. D. Gupta, R. R. Chaudhuri, and M. Shrivastava, “Interplay of device design and carbon-doped Ga_N buffer parameters in determining dynamic in AlGa_N/Ga_N HEMTs,” *IEEE Transactions on Electron Devices*, vol. 69, no. 11, pp. 6035–6042, 2022.
- [161] A. N. Tallarico, S. Stoffels, N. Posthuma, *et al.*, “PBTI in Ga_N-HEMTs With p-Type Gate: Role of the Aluminum Content on ΔV_{th} and Underlying Degradation Mechanisms,” *IEEE Transactions on Electron Devices*, vol. 65, no. 1, pp. 38–44, 2017.
- [162] V. Joshi, S. D. Gupta, R. R. Chaudhuri, and M. Shrivastava, “Interplay between surface and buffer traps in governing breakdown characteristics of AlGa_N/Ga_N HEMTs—Part II,” *IEEE Transactions on Electron Devices*, vol. 68, no. 1, pp. 80–87, 2020.
- [163] M. A. Mir, V. Joshi, R. R. Chaudhuri, M. A. Munshi, R. R. Malik, and M. Shrivastava, “Dynamic interplay of surface and buffer traps in determining drain current injection induced device instability in OFF-state of AlGa_N/Ga_N HEMTs,” in *2023 IEEE International Reliability Physics Symposium (IRPS)*, IEEE, 2023, pp. 1–6.
- [164] S. Ghosh, S. Das, S. M. Dinara, *et al.*, “OFF-state leakage and current collapse in AlGa_N/Ga_N HEMTs: A virtual gate induced by dislocations,” *IEEE Transactions on Electron Devices*, vol. 65, no. 4, pp. 1333–1339, 2018.
- [165] B. Bakeroot, S. Stoffels, N. Posthuma, D. Wellekens, and S. Decoutere, “Trading off between threshold voltage and subthreshold slope in AlGa_N/Ga_N HEMTs with a p-Ga_N gate,” in *2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, IEEE, 2019, pp. 419–422.
- [166] N. Lophitis, A. Arvanitopoulos, S. Perkins, M. Antoniou, and Y. K. Sharma, “TCAD device modelling and simulation of wide bandgap power semiconductors,” *Disruptive Wide Bandgap Semiconductors, Related Technologies, and Their Applications*, 2018.

- [167] D. M. Caughey and R. Thomas, "Carrier mobilities in silicon empirically related to doping and field," *Proceedings of the IEEE*, vol. 55, no. 12, pp. 2192–2193, 1967.
- [168] C. Canali, G Majni, R Minder, and G Ottaviani, "Electron and hole drift velocity measurements in silicon and their empirical relation to electric field and temperature," *IEEE Transactions on electron devices*, vol. 22, no. 11, pp. 1045–1047, 2005.
- [169] M. Wang, Y. Lv, Z. Wen, H. Zhou, P. Cui, and Z. Lin, "Monte Carlo investigation of high-field electron transport properties in AlGa_N/Ga_N HFETs," *IEEE Electron Device Letters*, vol. 43, no. 12, pp. 2041–2044, 2022.
- [170] J. Casamento, T.-S. Nguyen, Y. Cho, *et al.*, "Transport properties of polarization-induced 2D electron gases in epitaxial AlSc_N/Ga_N heterojunctions," *Applied Physics Letters*, vol. 121, no. 19, 2022.
- [171] M. Farahmand, C. Garetto, E. Bellotti, *et al.*, "Monte Carlo simulation of electron transport in the III-nitride wurtzite phase materials system: binaries and ternaries," *IEEE Transactions on electron devices*, vol. 48, no. 3, pp. 535–542, 2002.
- [172] R Dimitrov, M Murphy, J Smart, *et al.*, "Two-Dimensional Electron Gases in Ga-face and N-face AlGa_N/Ga_N Heterostructures Grown by Plasma-Induced Molecular Beam Epitaxy and Metalorganic Chemical Vapor Deposition on Sapphire," *Journal of Applied Physics*, vol. 87, no. 7, pp. 3375–3380, 2000.
- [173] O. Ambacher, B Christian, N Feil, *et al.*, "Wurtzite ScAl_N, InAl_N, and GaAl_N crystals, a comparison of structural, elastic, dielectric, and piezoelectric properties," *Journal of Applied Physics*, vol. 130, no. 4, 2021.
- [174] O. Ambacher, A. Yassine, M Yassine, S. Mihalic, E. Wade, and B Christian, "Electron Accumulation and Distribution at Interfaces of Hexagonal $Sc_xAl_{(1-x)}N/GaN$ -and $Sc_xAl_{(1-x)}N/InN$ -Heterostructures," *Journal of Applied Physics*, vol. 131, no. 24, 2022.
- [175] C. E. Dreyer, A. Janotti, C. G. Van de Walle, and D. Vanderbilt, "Correct implementation of polarization constants in wurtzite materials and impact on III-nitrides," *Physical Review X*, vol. 6, no. 2, p. 021 038, 2016.
- [176] K. Horio and H. Yanai, "Numerical modeling of heterojunctions including the thermionic emission mechanism at the heterojunction interface," *IEEE transactions on electron devices*, vol. 37, no. 4, pp. 1093–1098, 2002.

- [177] M. Zhu, G. Li, H. Li, *et al.*, “Challenges and advancements in p-GaN gate based high electron mobility transistors (HEMTs) on silicon substrates,” *Journal of Materials Chemistry C*, 2024.
- [178] N. Posthuma, S. You, S. Stoffels, H. Liang, M. Zhao, and S. Decoutere, “Gate architecture design for enhancement mode p-GaN gate HEMTs for 200 and 650V applications,” in *2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, IEEE, 2018, pp. 188–191.
- [179] P. Moens and A. Stockman, “A physical-statistical approach to AlGaIn/GaN HEMT reliability,” in *2019 IEEE International Reliability Physics Symposium (IRPS)*, IEEE, 2019, pp. 1–6.
- [180] M Millesimo, C Fiegna, N Posthuma, *et al.*, “High-Temperature Time-Dependent Gate Breakdown of p-GaN HEMTs,” *IEEE Transactions on Electron Devices*, vol. 68, no. 11, pp. 5701–5706, 2021.
- [181] S Stoffels, B Bakeroot, T.-L. Wu, *et al.*, “Failure mode for p-GaN gates under forward gate stress with varying Mg concentration,” in *2017 IEEE International Reliability Physics Symposium (IRPS)*, IEEE, 2017, 4B–4.
- [182] *Simulation of Leakage due to Tunneling in p-GaN Schottky Barriers*, available from TCAD Sentaurus Version S-2021.06 installation, go to Applications_Library/Power/GaN/pGate_Schottky_1D.
- [183] *Two-Dimensional Device Simulation of p-GaN Gate HEMTs*, available from TCAD Sentaurus Version S-2021.06 installation, go to Applications_Library/Power/GaN/pGate_HEMT.
- [184] *Threshold Voltage Instability in p-GaN Gate HEMTs Under Gate Voltage Stress*, available from TCAD Sentaurus Version vU-2022.12 installation, go to Applications_Library/Power/GaN/pGate_HEMT_VtInstability.
- [185] R. T. Tung, “The Physics and Chemistry of the Schottky Barrier Height,” *Applied Physics Reviews*, vol. 1, no. 1, 2014.
- [186] K Saarinen, J Nissilä, P Hautojärvi, *et al.*, “The Influence of Mg Doping on the Formation of Ga Vacancies and Negative Ions in GaN Bulk Crystals,” *Applied physics letters*, vol. 75, no. 16, pp. 2441–2443, 1999.
- [187] J Han, A. Baca, R. Shul, *et al.*, “Growth and Fabrication of GaN/AlGaIn Heterojunction Bipolar Transistor,” *Applied physics letters*, vol. 74, no. 18, pp. 2702–2704, 1999.

- [188] S. Brochen, J. Brault, S. Chenot, A. Dussaigne, M. Leroux, and B. Damilano, "Dependence of the Mg-related acceptor ionization energy with the acceptor concentration in p-type GaN layers grown by molecular beam epitaxy," *Applied Physics Letters*, vol. 103, no. 3, 2013.
- [189] D. Kim, D. Ryu, N. Bojarczuk, *et al.*, "Thermal activation energies of Mg in GaN: Mg measured by the Hall effect and admittance spectroscopy," *Journal of Applied Physics*, vol. 88, no. 5, pp. 2564–2569, 2000.
- [190] A. Calzolari and A. Catellani, "Controlling the TiN Electrode Work Function at the Atomistic Level: A First Principles Investigation," *IEEE Access*, vol. 8, pp. 156 308–156 313, 2020. doi: 10.1109/ACCESS.2020.3017726.
- [191] R. Mishra, A. Dubey, C.-W. Chang, *et al.*, "Epitaxial TiN/GaN Heterostructure for Efficient Photonic Energy Harvesting," *ACS Photonics*, vol. 9, no. 6, pp. 1895–1901, 2022.
- [192] I Vurgaftman and J. n. Meyer, "Band parameters for nitrogen-containing semiconductors," *Journal of Applied Physics*, vol. 94, no. 6, pp. 3675–3696, 2003.
- [193] A. Wright, "Influence of crystal structure on the lattice sites and formation energies of hydrogen in wurtzite and zinc-blende GaN," *Physical Review B*, vol. 60, no. 8, R5101, 1999.
- [194] J. Neugebauer and C. G. Van de Walle, "Role of hydrogen in doping of GaN," *Applied Physics Letters*, vol. 68, no. 13, pp. 1829–1831, Mar. 1996, issn: 0003-6951. doi: 10.1063/1.116027. eprint: https://pubs.aip.org/aip/apl/article-pdf/68/13/1829/18518041/1829_1_online.pdf. [Online]. Available: <https://doi.org/10.1063/1.116027>.
- [195] H. Amano, M. Kito, K. Hiramatsu, and I. Akasaki, "P-type conduction in Mg-doped GaN treated with low-energy electron beam irradiation (LEEBI)," *Japanese journal of applied physics*, vol. 28, no. 12A, p. L2112, 1989.
- [196] S. Nakamura, N. Iwasa, M. S. Masayuki Senoh, and T. M. Takashi Mukai, "Hole compensation mechanism of p-type GaN films," *Japanese Journal of Applied Physics*, vol. 31, no. 5R, p. 1258, 1992.
- [197] J.-J. Dai, T. T. Mai, S.-K. Wu, *et al.*, "High hole concentration and diffusion suppression of heavily Mg-doped p-GaN for application in enhanced-mode GaN HEMT," *Nanomaterials*, vol. 11, no. 7, p. 1766, 2021.

- [198] N. E. Posthuma, S. You, H. Liang, *et al.*, “Impact of mg out-diffusion and activation on the p-gan gate hemt device performance,” in *2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2016, pp. 95–98. doi: 10.1109/ISPSD.2016.7520786.
- [199] G. Miceli and A. Pasquarello, “Self-compensation due to point defects in Mg-doped GaN,” *Physical Review B*, vol. 93, no. 16, p. 165 207, 2016.
- [200] A Hoffmann, A Kaschner, and C Thomsen, “Local vibrational modes and compensation effects in Mg-doped GaN,” *physica status solidi (c)*, no. 6, pp. 1783–1794, 2003.
- [201] M Buffolo, D Favero, A Marcuzzi, *et al.*, “Review and outlook on GaN and SiC power devices: industrial state-of-the-art, applications, and perspectives,” *IEEE Transactions on Electron Devices*, 2024.
- [202] J. Kemmerling, “The Development of Gallium Nitride Super-Heterojunction Transistors for 10-kV Blocking and 3-kV Switching,” Ph.D. dissertation, The Pennsylvania State University, 2025.
- [203] K. Benson, “GaN breaks barriers—RF power amplifiers go wide and high,” *10 Massive MIMO and Beamforming: The Signal Processing Behind the 5G Buzzwords*, p. 45, 2017.
- [204] R. Quay, *Gallium Nitride Electronics*. Springer Science & Business Media, 2008, vol. 96.
- [205] F. Medjdoub, *Gallium nitride (GaN): Physics, Devices, and Technology*. CRC Press, 2017.
- [206] F. Roccaforte and M. Leszczynski, “Introduction to Gallium Nitride Properties and Applications,” *Nitride Semiconductor Technology: Power Electronics and Optoelectronic Devices*, pp. 1–39, 2020.
- [207] N. Cahoon, P Srinivasan, and F. Guarin, “6G roadmap for semiconductor technologies: Challenges and advances,” in *2022 IEEE International Reliability Physics Symposium (IRPS)*, IEEE, 2022, 11B–1.
- [208] E. Zanoni, C. De Santi, Z. Gao, *et al.*, “Microwave and Millimeter-Wave GaN HEMTs: Impact of Epitaxial Structure on Short-Channel Effects, Electron Trapping, and Reliability,” *IEEE Transactions on Electron Devices*, vol. 71, no. 3, pp. 1396–1407, 2024. doi: 10.1109/TED.2023.3318564.

- [209] P. Vigneshwara Raja, J.-C. Nallatamby, M. Bouslama, *et al.*, “HTRB Stress Effects on 0.15 μm AlGaIn/GaN HEMT Performance,” in *2022 IEEE MTT-S International Conference on Numerical Electromagnetic and Multiphysics Modeling and Optimization (NEMO)*, 2022, pp. 1–4. doi: 10.1109/NEMO51452.2022.10038964.
- [210] T. Ohki, T. Kikkawa, Y. Inoue, *et al.*, “Reliability of GaN HEMTs: current status and future technology,” in *2009 IEEE International Reliability Physics Symposium*, 2009, pp. 61–70. doi: 10.1109/IRPS.2009.5173225.
- [211] G. Meneghesso, M. Meneghini, A. Stocco, *et al.*, “Degradation of AlGaIn/GaN HEMT devices: Role of reverse-bias and hot electron stress,” *Microelectronic engineering*, vol. 109, pp. 257–261, 2013.
- [212] G. Meneghesso, M. Meneghini, I. Rossetto, *et al.*, “Reliability and parasitic issues in GaN-based power HEMTs: A review,” *Semiconductor Science and Technology*, vol. 31, no. 9, p. 093 004, 2016.
- [213] M. Meneghini, I. Rossetto, D. Bisi, *et al.*, “Buffer traps in Fe-doped AlGaIn/GaN HEMTs: Investigation of the physical properties based on pulsed and transient measurements,” *IEEE Transactions on Electron Devices*, vol. 61, no. 12, pp. 4070–4077, 2014.
- [214] N. Roccato, F. Piva, C. De Santi, *et al.*, “Modeling the electrical degradation of AlGaIn-based UV-C LEDs by combined deep-level optical spectroscopy and TCAD simulations,” *Applied Physics Letters*, vol. 122, no. 16, p. 161 105, Apr. 2023, issn: 0003-6951. doi: 10.1063/5.0144721. eprint: https://pubs.aip.org/aip/apl/article-pdf/doi/10.1063/5.0144721/18258307/161105_1_5.0144721.pdf. [Online]. Available: <https://doi.org/10.1063/5.0144721>.
- [215] C. Leurquin, “Study of degradation mechanisms and dynamic reliability of GaN on Si devices,” Ph.D. dissertation, Université Grenoble Alpes [2020-....], 2024.
- [216] O. Hilt, F. Brunner, E. B. Treidel, M. Wolf, and J. Würfl, “GaN-channel HEMTs with AlN buffer for high-voltage switching,” in *2021 Device Research Conference (DRC)*, IEEE, 2021, pp. 1–2.
- [217] Y. Wu, M. Nuo, J. Yang, *et al.*, “Suppression of buffer trapping effect in GaN-on-Si active-passivation p-GaN gate HEMT via light/hole pumping,” *IEEE Transactions on Electron Devices*, vol. 71, no. 1, pp. 484–489, 2023.

- [218] F. Jia, X. Ma, L. Yang, *et al.*, “The influence of Fe doping tail in unintentionally doped GaN layer on DC and RF performance of AlGaIn/GaN HEMTs,” *IEEE Transactions on Electron Devices*, vol. 68, no. 12, pp. 6069–6075, 2021.
- [219] M. Meneghini, A. Tajalli, P. Moens, A. Banerjee, E. Zanoni, and G. Meneghesso, “Trapping phenomena and degradation mechanisms in GaN-based power HEMTs,” *Materials Science in Semiconductor Processing*, vol. 78, pp. 118–126, 2018.
- [220] C. Baylis and L. Dunleavy, “Understanding pulsed IV measurement waveforms,” in *The 11th IEEE International Symposium on Electron Devices for Microwave and Optoelectronic Applications, 2003. EDMO 2003.*, 2003, pp. 223–228. doi: 10.1109/EDMO.2003.1260055.
- [221] B. M. Paine, S. R. Polmanter, V. T. Ng, N. T. Kubota, and C. R. Ignacio, “Fast-pulsed characterization of RF GaN HEMTs in lifetest systems,” *IEEE Transactions on Device and Materials Reliability*, vol. 17, no. 1, pp. 130–137, 2016.
- [222] A. Divay, C. Duperrier, F. Temcamani, and O. Latry, “Effects of drain quiescent voltage on the ageing of AlGaIn/GaN HEMT devices in pulsed RF mode,” *Microelectronics Reliability*, vol. 64, pp. 585–588, 2016.
- [223] M. White, M. Cooper, Y. Chen, and J. Bernstein, “Impact of junction temperature on microelectronic device reliability and considerations for space applications,” in *IEEE International Integrated Reliability Workshop Final Report, 2003*, 2003, pp. 133–136. doi: 10.1109/IRWS.2003.1283320.
- [224] M. Oualli, C. Dua, O. Patard, *et al.*, “Stability and robustness of InAlGaIn/GaN HEMT in short-term DC tests for different passivation schemes,” *Microelectronics Reliability*, vol. 88-90, pp. 418–422, 2018, 29th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF 2018), issn: 0026-2714. doi: <https://doi.org/10.1016/j.microrel.2018.07.142>. [Online]. Available: <https://www.sciencedirect.com/science/article/pii/S0026271418307406>.
- [225] S. Leone, F. Benkhelifa, L. Kirste, *et al.*, “Suppression of Iron Memory Effect in GaN Epitaxial Layers,” *physica status solidi (b)*, vol. 255, no. 5, p. 1700377, 2018. doi: <https://doi.org/10.1002/pssb.201700377>. eprint: <https://onlinelibrary.wiley.com/doi/pdf/10.1002/pssb.201700377>. [Online]. Available: <https://onlinelibrary.wiley.com/doi/abs/10.1002/pssb.201700377>.

- [226] D. S. Arteev, A. V. Sakharov, W. V. Lundin, *et al.*, “Influence of doping profile of GaN:Fe buffer layer on the properties of AlGaN/AlN/GaN heterostructures for high-electron mobility transistors,” *Journal of Physics: Conference Series*, vol. 1697, no. 1, p. 012 206, 2020. doi: 10.1088/1742-6596/1697/1/012206. [Online]. Available: <https://dx.doi.org/10.1088/1742-6596/1697/1/012206>.
- [227] D. Caughey and R. Thomas, “Carrier mobilities in silicon empirically related to doping and field,” *Proceedings of the IEEE*, vol. 55, no. 12, pp. 2192–2193, 1967. doi: 10.1109/PROC.1967.6123.
- [228] J. M. Tirado, F. Mieville, X. Zhao, J. Chung, J. L. Sanchez-Rojas, and T. Palacios, “Origin of the increasing access resistance in AlGaIn/GaN HEMTs,” in *2008 Device Research Conference*, IEEE, 2008, pp. 203–204.
- [229] M. Wang, Y. Lv, Z. Wen, H. Zhou, P. Cui, and Z. Lin, “Monte Carlo Investigation of High-Field Electron Transport Properties in AlGaIn/GaN HFETs,” *IEEE Electron Device Letters*, vol. 43, no. 12, pp. 2041–2044, 2022. doi: 10.1109/LED.2022.3217127.
- [230] N. K. Subramani, A. K. Sahoo, J.-C. Nallatamby, *et al.*, “Characterization of parasitic resistances of AlN/GaN/AlGaIn HEMTs through TCAD-based device simulations and on-wafer measurements,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 5, pp. 1351–1358, 2016.
- [231] B. Jogai, “Influence of surface states on the two-dimensional electron gas in AlGaIn/GaN heterojunction field-effect transistors,” *Journal of applied physics*, vol. 93, no. 3, pp. 1631–1635, 2003.
- [232] B. Ofuonye, J. Lee, M. Yan, C. Sun, J.-M. Zuo, and I. Adesida, “Electrical and microstructural properties of thermally annealed Ni/Au and Ni/Pt/Au Schottky contacts on AlGaIn/GaN heterostructures,” *Semiconductor science and technology*, vol. 29, no. 9, p. 095 005, 2014.
- [233] W. Schottky, “Halbleitertheorie der sperrschicht,” *Naturwissenschaften*, vol. 26, no. 52, pp. 843–843, 1938.
- [234] N. F. Mott, “Note on the contact between a metal and an insulator or semiconductor,” in *Mathematical Proceedings of the Cambridge Philosophical Society*, Cambridge University Press, vol. 34, 1938, pp. 568–572.
- [235] V. W. Schottky, “Abweichungen vom ohmschen gesetz in halbleitern,” in *Electronic Structure of Metal-Semiconductor Contacts*, Springer, 1940, pp. 59–62.

- [236] J. Bardeen, "Surface states and rectification at a metal semi-conductor contact," *Physical review*, vol. 71, no. 10, p. 717, 1947.
- [237] W Mönch, "Role of virtual gap states and defects in metal-semiconductor contacts," *Physical review letters*, vol. 58, no. 12, p. 1260, 1987.
- [238] J.-K. Kim, S.-H. Kim, T. Kim, and H.-Y. Yu, "Universal Metal–Interlayer–Semiconductor Contact Modeling Considering Interface-State Effect on Contact Resistivity Degradation," *IEEE Transactions on Electron Devices*, vol. 65, no. 11, pp. 4982–4987, 2018.
- [239] M. J. Uren, J. Moreke, and M. Kuball, "Buffer design to minimize current collapse in gan/algan hfets," *IEEE Transactions on Electron Devices*, vol. 59, no. 12, pp. 3327–3333, 2012. doi: 10.1109/TED.2012.2216535.
- [240] A. Polyakov, N. Smirnov, A. Govorkov, *et al.*, "Properties and annealing stability of fe doped semi-insulating gan structures," *physica status solidi (c)*, vol. 2, no. 7, pp. 2476–2479, 2005.
- [241] D. Wickramaratne, J.-X. Shen, C. E. Dreyer, *et al.*, "Iron as a source of efficient shockley-read-hall recombination in gan," *Applied Physics Letters*, vol. 109, no. 16, 2016.
- [242] Y. Puzyrev, R. Schrimpf, D. Fleetwood, and S. Pantelides, "Role of fe impurity complexes in the degradation of gan/algan high-electron-mobility transistors," *Applied Physics Letters*, vol. 106, no. 5, 2015.
- [243] R Heitz, P Maxim, L Eckey, *et al.*, "Excited states of fe 3+ in gan," *Physical Review B*, vol. 55, no. 7, p. 4382, 1997.
- [244] T. Aggerstam, A. Pinos, S Marcinkevičius, M. Linnarsson, and S. Lourdu-doss, "Electron and hole capture cross-sections of fe acceptors in gan: Fe epitaxially grown on sapphire," *Journal of electronic materials*, vol. 36, no. 12, pp. 1621–1624, 2007.
- [245] P Kordoš, M Morvic, J Betko, J Novák, J Flynn, and G. Brandes, "Conductivity and hall effect of free-standing highly resistive epitaxial gan: Fe substrates," *Applied physics letters*, vol. 85, no. 23, pp. 5616–5618, 2004.
- [246] J. Wu, D. Han, W. Yang, S. Chen, X. Jiang, and J. Chen, "Comprehensive investigations on charge diffusion physics in sin-based 3d nand flash memory through systematical ab initio calculations," in *2017 IEEE International Electron Devices Meeting (IEDM)*, IEEE, 2017, pp. 4–5.

- [247] *JEDEC Standard: Temperature, Bias, and Operating Life*, JEDEC Standard No. JESD22-A108G (Revision of JESD22-A108F dated July 2017), JEDEC Solid State Technology Association, 2022]. [Online]. Available: <https://www.jedec.org/system/files/docs/22A108G.pdf>.
- [248] B. Jogai, "Influence of surface states on the two-dimensional electron gas in AlGaIn/GaN heterojunction field-effect transistors," *Journal of Applied Physics*, vol. 93, no. 3, pp. 1631–1635, Feb. 2003, ISSN: 0021-8979. doi: 10.1063/1.1530729. eprint: https://pubs.aip.org/aip/jap/article-pdf/93/3/1631/10627015/1631_1_online.pdf. [Online]. Available: <https://doi.org/10.1063/1.1530729>.
- [249] A. J. Green, J. K. Gillespie, R. C. Fitch, *et al.*, "ScAlN/GaN High-Electron-Mobility Transistors with 2.4-A/mm Current Density and 0.67-S/mm Transconductance," *IEEE Electron Device Letters*, vol. 40, no. 7, pp. 1056–1059, 2019.
- [250] P. Döring, S. Krause, P. Waltereit, *et al.*, "Voltage-margin limiting mechanisms of AlScN-based HEMTs," *Applied Physics Letters*, vol. 123, no. 3, 2023.
- [251] A. J. Green, N. Moser, N. C. Miller, *et al.*, "RF power performance of Sc (Al, Ga) N/GaN HEMTs at Ka-band," *IEEE Electron Device Letters*, vol. 41, no. 8, pp. 1181–1184, 2020.
- [252] T. E. Kazior, E. M. Chumbes, B. Schultz, J. Logan, D. J. Meyer, and M. T. Hardy, "High power density ScAlN-based heterostructure FETs for mm-wave applications," in *2019 IEEE MTT-S International Microwave Symposium (IMS)*, IEEE, 2019, pp. 1136–1139.
- [253] M. B. Tahhan, J. A. Logan, M. T. Hardy, *et al.*, "Passivation schemes for ScAlN-barrier mm-wave high electron mobility transistors," *IEEE Transactions on Electron Devices*, vol. 69, no. 3, pp. 962–967, 2022.
- [254] C. Manz, S. Leone, L. Kirste, *et al.*, "Improved AlScN/GaN heterostructures grown by metal-organic chemical vapor deposition," *Semiconductor Science and Technology*, vol. 36, no. 3, p. 034 003, 2021.
- [255] S. Leone, I. Streicher, M. Prescher, P. Straňák, and L. Kirste, "Metal-Organic Chemical Vapor Deposition of Aluminum Yttrium Nitride," *physica status solidi (RRL)–Rapid Research Letters*, vol. 17, no. 10, p. 2 300 091, 2023.
- [256] A. Santarelli, R. Cignani, G. P. Gibiino, *et al.*, "A double-pulse technique for the dynamic I/V characterization of GaN FETs," *IEEE Microwave and Wireless Components Letters*, vol. 24, no. 2, pp. 132–134, 2013.

- [257] A. Santarelli, R. Cignani, G. P. Gibiino, *et al.*, “Nonlinear charge trapping effects on pulsed I/V characteristics of GaN FETs,” in *2013 European Microwave Integrated Circuit Conference*, IEEE, 2013, pp. 404–407.
- [258] A. Santarelli, D. Niessen, R. Cignani, *et al.*, “GaN FET Nonlinear Modeling Based on Double Pulse I/V Characteristics,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 12, pp. 3262–3273, 2014.
- [259] X. Zhang, E. A. Stach, W. Meng, and A. C. Meng, “Nanoscale Compositional Segregation in Epitaxial AlScN on Si (111),” *Nanoscale Horizons*, vol. 8, no. 5, pp. 674–684, 2023.
- [260] D. V. Dinh, J. Lähnemann, L. Geelhaar, and O. Brandt, “Lattice Parameters of Sc_xAl_{1-x}N Layers Grown on GaN (0001) by Plasma-Assisted Molecular Beam Epitaxy,” *Applied Physics Letters*, vol. 122, no. 15, 2023.
- [261] V. Tilak, B. Green, V. Kaper, *et al.*, “Influence of Barrier Thickness on the High-Power Performance of AlGaIn/GaN HEMTs,” *IEEE Electron Device Letters*, vol. 22, no. 11, pp. 504–506, 2001.
- [262] P. Waltereit, W. Bronner, M. Musser, *et al.*, “Influence of AlGaIn barrier thickness on electrical and device properties in Al_{0.14}Ga_{0.86}N/GaN high electron mobility transistor structures,” *Journal of Applied Physics*, vol. 112, no. 5, 2012.
- [263] M. Dammann, H. Czap, J. Rüster, *et al.*, “Reverse Bias Stress Test of GaN HEMTs for High-Voltage Switching Applications,” in *2012 IEEE International Integrated Reliability Workshop Final Report*, 2012, pp. 105–108. doi: 10.1109/IIRW.2012.6468930.
- [264] C. Zhou, W. Chen, E. L. Piner, and K. J. Chen, “Schottky-ohmic drain AlGaIn/GaN normally off HEMT with reverse drain blocking capability,” *IEEE electron device letters*, vol. 31, no. 7, pp. 668–670, 2010.
- [265] S. Leone, F. Benkhelifa, L. Kirste, *et al.*, “Suppression of iron memory effect in GaN epitaxial layers,” *physica status solidi (b)*, vol. 255, no. 5, p. 1 700 377, 2018.
- [266] R. Guido, T. Mikolajick, U. Schroeder, and P. D. Lomenzo, “Role of Defects in the Breakdown Phenomenon of Al_(1-x)Sc_xN: From Ferroelectric to Filamentary Resistive Switching,” *Nano Letters*, vol. 23, no. 15, pp. 7213–7220, 2023.
- [267] R. Ye, X. Cai, C. Du, *et al.*, “An Overview on Analyses and Suppression Methods of Trapping Effects in AlGaIn/GaN HEMTs,” *IEEE Access*, vol. 10, pp. 21 759–21 773, 2022. doi: 10.1109/ACCESS.2021.3139443.

- [268] M. Singh, M. J. Uren, T. Martin, S. Karboyan, H. Chandrasekar, and M. Kuball, ““Kink” in AlGa_N/Ga_N-HEMTs: floating buffer model,” *IEEE Transactions on Electron Devices*, vol. 65, no. 9, pp. 3746–3753, 2018.
- [269] A. Bag, S. Das, P. Mukhopadhyay, and D. Biswas, “Observation and analysis of kink effect during drain current inception of Ga_N HEMT,” *Superlattices and Microstructures*, vol. 120, pp. 101–107, 2018.
- [270] G. Meneghesso, F. Zanon, M. J. Uren, and E. Zanoni, “Anomalous kink effect in Ga_N high electron mobility transistors,” *IEEE Electron Device Letters*, vol. 30, no. 2, pp. 100–102, 2008.
- [271] G. Greco, P. Fiorenza, F. Iucolano, A. Severino, F. Giannazzo, and F. Roccaforte, “Conduction Mechanisms at Interface of Al_N/Si_N Dielectric Stacks with AlGa_N/Ga_N Heterostructures for Normally-off High Electron Mobility Transistors: Correlating Device Behavior with Nanoscale Interfaces Properties,” *ACS Applied Materials & Interfaces*, vol. 9, no. 40, pp. 35 383–35 390, 2017, PMID: 28920438. doi: 10.1021/acsami.7b08935. eprint: <https://doi.org/10.1021/acsami.7b08935>. [Online]. Available: <https://doi.org/10.1021/acsami.7b08935>.