ALMA MATER STUDIORUM
UNIVERSITÀ DI BOLOGNA

DOTTORATO DI RICERCA IN

INGEGNERIA BIOMEDICA, ELETTRICA E DEI SISTEMI

Ciclo 38

Settore Concorsuale: 09/E1 - ELETTROTECNICA

Settore Scientifico Disciplinare: ING-IND/31 - ELETTROTECNICA

POWER ELECTRONIC CONVERTERS FOR PARTICLE ACCELERATORS AND NUCLEAR FUSION APPLICATIONS

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Esame finale anno 2026

Abstract

Driven by the need for clean, large-scale energy generation, rising electricity demand, and global climate goals, controlled thermonuclear fusion has become a central focus in the development of advanced energy systems. In parallel, increasing investment in medical infrastructure, particularly for cancer treatment, and continued progress in fundamental scientific research are accelerating advancements in particle accelerator technologies. These applications require power converters with high-current handling capabilities, bidirectional load power flow, unity power factor operation, efficient load energy recovery, and precise load control under dynamic operating conditions. This thesis focuses on two significant parts of such power converters: the active front-end (AFE) stage based on a neutral point clamped topology, and the back-end DC/DC stage employing interleaved H-bridges (HBs) topology.

The first part of the thesis investigates the AFE implemented in CERN's POPS-B power converter, with particular emphasis on its role as a reactive power compensator under light-load conditions. A novel control strategy based on instantaneous energy balance is proposed for regulating the variable DC-bus voltage, enabling dual functionality while maintaining stable load operation without inducing over-modulation or violating DC-bus voltage drop limits. The performance of the AFE is analyzed using two conventional grid control strategies, the synchronous rotating $dq-$frame and the stationary $\alpha\beta-$frame, showing comparable results, with the $\alpha\beta-$frame offering improved decoupling between active and reactive power regulation. Furthermore, a detailed analysis of the neutral point current and its harmonic spectrum is provided, along with a harmonic spectrum analysis of the semi-DC-bus voltages and DC-bus voltage, validated through both numerical simulations and experimental measurements under varying reactive power conditions.

The second part of the thesis focuses on the interleaved HB based back-end converter, comparing two architectural variants: the common DC-bus configuration (CDC) and the split DC-bus configuration (SDC). A key challenge addressed is the presence of circulating currents in CDC, which increase thermal and electrical stress on power components. Analytical models are developed to evaluate RMS currents and non-zero frequency components in both configurations under ideal and non-ideal conditions of the interleaving inductors. A normalization method is introduced to decouple the circulating current effect from the output current. Based on these insights, an algorithm is proposed to automatically select the optimal back-end topology based on design parameters and circulating current constraints. The algorithm is validated through numerical simulations and illustrative design cases. Additionally, the core principle of the algorithm, based on the RMS of the non-zero frequency current component in the CDC, is experimentally validated using two distinct numbers of HB setups.

Overall, this thesis contributes to advancing power converter design by enhancing reactive power management in AFE converters and addressing circulating current behavior in interleaved HB architectures. These contributions support the effective development of power converters for next-generation scientific and high-energy infrastructures.

Index Terms−Nuclear Fusion; Particle Accelerators; Low-Ripple; High-Current; Active Front-End; Reactive Power Compensator; Interleaved H-Bridge Converter; Common DC-bus Configuration; Split DC-bus Configuration; Circulating Currents.

Acknowledgements

First and foremost, I would like to express my sincere gratitude to OCEM Power Electronics, part of Energy Technology s.r.l., for giving me the opportunity to pursue my high apprenticeship Ph.D. in collaboration with the University of Bologna, Department of Electrical, Electronic, and Information Engineering (DEI), within the Power Electronic Circuits and Photovoltaics – SOLARTRONIC group. I am deeply grateful to the management for their ongoing support and for creating an environment that fosters both academic and professional development.

My heartfelt thanks go to Dr. Felice Liccardo, R&D Manager at OCEM Power Electronics and my industrial supervisor during the final year of my Ph.D., for his unwavering support, and valuable guidance. I am especially thankful to Ing. Gaetano Longo, my former team leader and industrial supervisor during the first two years of my Ph.D., for mentoring, generously sharing his expertise and providing essential insights into real-world engineering applications. I would also like to extend special thanks to Ing. Miguel Pretelli for enabling my collaboration with CERN for my period abroad research activity. I wish to express my special and heartfelt appreciation to Riccardo Testa, Matteo Civale, Saverino Carozza, and Marco Farioli. From the very beginning of my journey at OCEM Power Electronics, they supported me with patience and generosity, consistently sharing their knowledge and experience. Their guidance was instrumental in shaping my development as an engineer throughout those three and a half years. Their mentorship, encouragement, and continuous support have left a lasting impact on my professional growth. Finally, I would like to extend my sincere appreciation to all my former colleagues in the R&D department at OCEM Power Electronics. Each of them, in different ways, contributed to my professional and personal journey over these three and a half years.

I wish to express my deep gratitude to my academic supervisor, Prof. Vincenzo Cirimele, for his steady guidance, support, and encouragement throughout my doctoral studies. I am also grateful to my co-supervisor, Prof. Riccardo Mandrioli, for facilitating my academic collaboration with the University of Bologna and for his guidance. I am thankful for the collegial environment and the interactions I shared with the professors and Ph.D. students of the SOLARTRONIC group.

I am sincerely thankful to Ing. Davide Aguglia of CERN's Electrical Power Converters (EPC) group for offering me the opportunity to join their team during my research stay. My special thanks to Ing. Manuel Colmenero Moratalla for his mentorship during my time at CERN, and to all the EPC colleagues with whom I had the pleasure of meeting.

Finally, I owe my deepest gratitude to my family, Bhupal Reddy Gudala, Vijaya Nirmala Gudala, Jeevana Gudala, and Rajesh Reddy Thipparthi, for their unconditional love, belief in me, and unwavering support throughout this journey and every stage of my life. Without them, none of this would have been possible.

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List of Acronyms

AFE Active Front-End.

CDC Common DC-bus Configuration.

CERN European Organization for Nuclear Research.

CMVI Common-Mode Voltage Injection.

FCC Future Circular Collider.

GSI Helmholtz Center for Heavy Ion Research.

HB H-Bridge.

ITER International Thermonuclear Experimental Reactor.

JET Joint European Torus.

JT-60SA Japanese Torus-60 Super Advanced.

LHC Large Hadron Collider.

NPC Neutral Point-Clamped.

PC Power converter.

PCC Point of Common Coupling.

PI Proportional-Integral.

PLL Phase-Locked Loop.

POPS-B Power Supply for the Proton Synchrotron Booster.

PR Proportional-Resonant Controller.

PWM Pulse Width Modulation.

RMS Root-Mean-Square.

SDC Split DC-bus Configuration.

SPARC Smallest Possible ARC.

TRIUMF TRI University Meson Facility.

Chapter 1

Introduction

Power converters (PCs) play a pivotal role in high-energy physics applications, where the reliable supply and precise regulation of electrical power are indispensable [1, 2]. They serve as the critical interface between the electrical grid and the load [3]. Their role extends beyond power delivery, providing fine control of current and voltage waveforms [4]. In high-energy physics applications, the demands on power quality are exceptionally stringent, as even small fluctuations in load current or load voltage can compromise the basic operation of the load [5]. For this reason, PCs are an enabling technology, forming the backbone of advanced facilities such as particle accelerators and nuclear fusion reactors [6].

1.1 Motivation and Applications

Nuclear fusion reactors, such as the International Thermonuclear Experimental Reactor (ITER), Japanese Torus-60 Super Advanced (JT-60SA), Joint European Torus (JET), Smallest Possible ARC (SPARC), are some of the most demanding applications of PC [7, 8, 9, 10]. Nuclear fusion is widely regarded as a potential source of large-scale, carbon-free electricity generation, but sustaining the

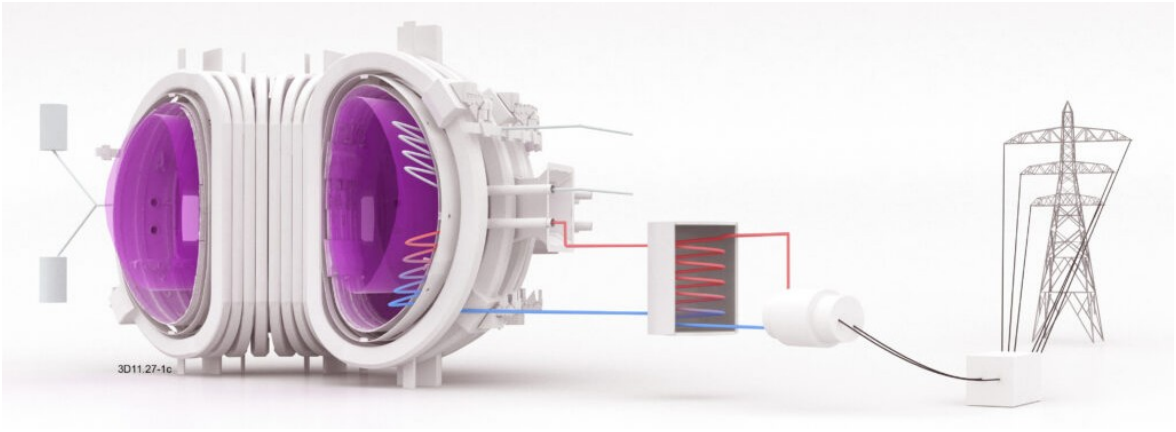


Figure 1.1: Simplified artistic impression of a tokamak connected to the grid. Image © UKAEA. Source: https://euro-fusion.org/programme/demo/.

extreme plasma conditions required for fusion demands highly controlled and reliable power delivery (Fig. 1.1) [11, 12, 13, 14]. PCs supply the toroidal, poloidal, central solenoid, and vertical stabilization coils, as well as plasma heating and auxiliary systems, ensuring precise current regulation under dynamic conditions [15, 16, 17].

Particle accelerators are another critical area where PCs are indispensable [18]. They accelerate charged particles to extremely high energies for both fundamental research and practical applications such as cancer treatment [19]. Major research centers include CERN, Helmholtz Center for Heavy Ion Research (GSI), Diamond Light Source, Fermi National Accelerator Laboratory [20, 21, 22, 23]. In addition to their role in fundamental physics research, particle accelerators have also found critical applications in medicine. Particle beam therapy, for instance, requires precise and controllable beams to target cancerous tissues while minimizing damage to surrounding healthy cells [19].

In both nuclear fusion and accelerator systems, the key infrastructure components are the coils [24]. In particle accelerators, magnets such as dipole magnets, quadrupole magnets, and sextupole magnets are used for various purposes, including beam generation, steering, focusing, and overall manipulation of particle trajectories [25]. In nuclear fusion reactors, coils play an equally critical role by generating the strong magnetic fields required to confine and maintain plasma at extremely high temperatures [26].

These coils can be broadly classified into two types: conventional electromagnets and superconducting magnets [27]. High currents are required in both types, as the coils need substantial energy to generate the strong magnetic fields necessary for their operation [28]. Conventional electromagnets, made with copper windings, exhibit significant resistive losses, leading to higher voltage requirements for a given current. In contrast, superconducting magnets have negligible internal resistance, resulting in much lower voltage requirements while enabling very high current operation [29]. As a result, PCs in these applications must support a wide output voltage range, from low to high, while delivering currents up to 100's of kilo amperes [30, 31].

The basic architecture of the voltage source converter is depicted in Fig. 1.2. Typically, the PCs that feed the coil consist of main components, such as the AC/DC converter on the front-end, the energy storage bank, usually a capacitor bank, and the DC/DC section, which forms the back-end converter [32]. Besides the voltage source converters in nuclear fusion and particle accelerators, there also exist current source converters to exchange the energy between the two coils, such as the architectures proposed by the authors in [33, 34, 35].

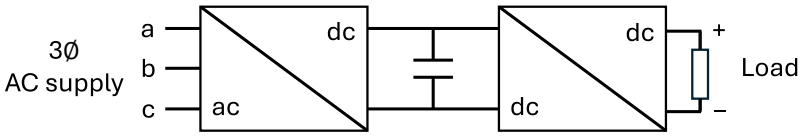


Figure 1.2: Typical voltage source converter architecture.

Specific characteristics are commonly found in PCs designed for coil applications.

- unity power factor operation at the Point of Common Coupling (PCC);
- galvanic isolation from the grid;
- bulky energy storage devices;

- modular back-end architecture;
- bi-directional load power flow;
- low output ripple; and
- output accuracy in parts per million

1.2 Background on Active Front-End Converter as Reactive Power Compensator

The AC/DC stage of the PC can be implemented using an uncontrolled rectifier, a thyristor-based controlled rectifier, or an AFE [36, 37]. For medium- or high-voltage levels, the NPC architecture is one of the most commonly implemented topologies, as it effectively handles the high-voltage requirements of the DC-bus [38]. In addition to voltage handling, the NPC architecture offers several advantages, including improved voltage sharing across switching devices, reduced output voltage harmonics, and lower switching losses. These features make it a highly efficient and reliable choice for high-power medium-voltage applications [39].

In real-world applications, there are many cases where an NPC based AFE is utilized as the AC/DC stage of a PC. One such application is the POPS-B PC at CERN, which is used to feed one of the magnets in the BOOSTER ring. The accelerator complex of CERN is shown in Fig. 1.3.

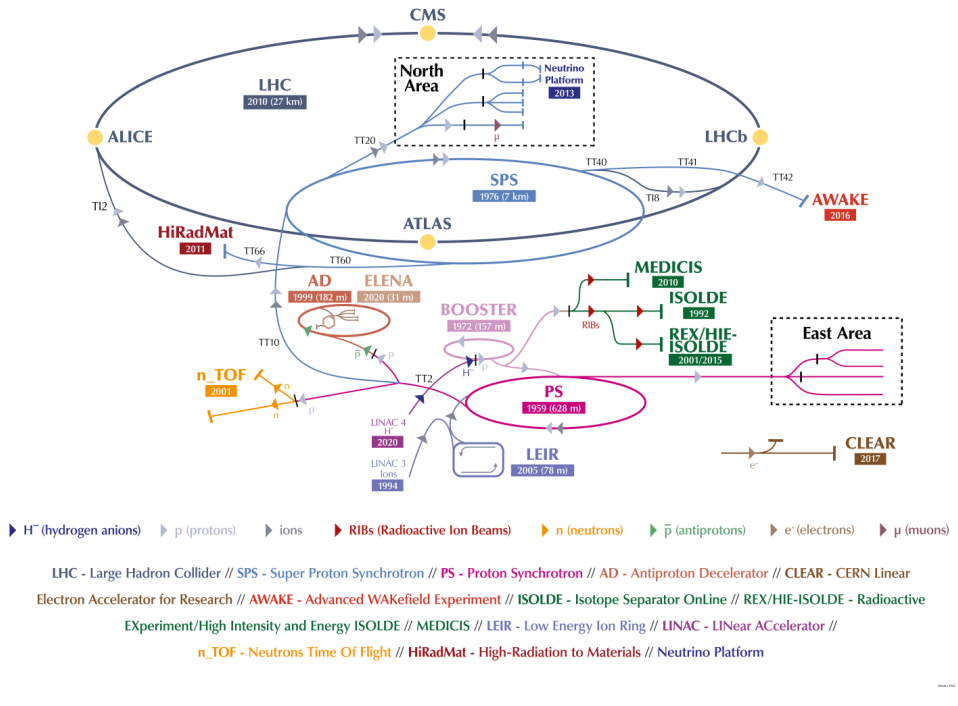


Figure 1.3: Adapted from the image of CERN accelerator complex. Image © CERN. Source: https://home.cern/science/accelerators/accelerator-complex.

At CERN, the proposed next-generation accelerator with a circumference of approximately $100\ \mathrm{km}$ is called the FCC [40]. A possible location for this accelerator ring is illustrated in Fig. 1.4. The FCC is designed to significantly surpass the energy levels of the current Large Hadron Collider (LHC), with planned collision energies increasing from $14\ \mathrm{TeV}$ in the LHC to up to $100\ \mathrm{TeV}$ in the FCC. This substantial increase in energy will enable physicists to probe deeper into fundamental questions in particle physics.

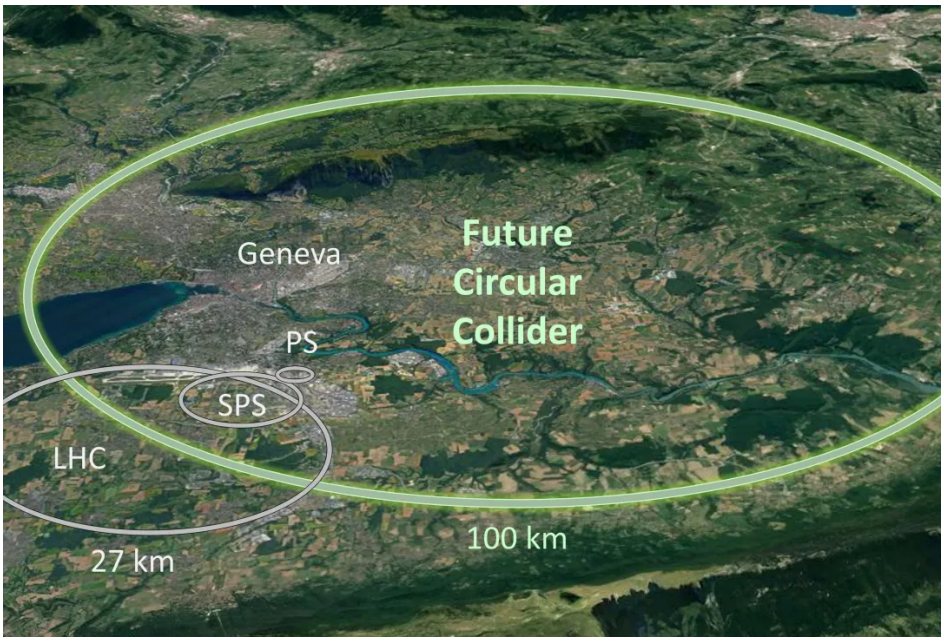


Figure 1.4: Map displaying the possible location of the FCC project at CERN. Image © CERN. Source: https://cds.cern.ch/record/2653532.

To support these higher energy levels, the energy stored in the coils must be increased, which will be achieved by raising both the inductance and current ratings of the superconducting magnets. However, this increase in inductive load imposes greater demands on the power grid, particularly in terms of reactive power management. The existing grid connection and compensation systems are designed for the current operational loads and may not be sufficient for the increased demands of the FCC. Although static thyristor compensators are currently in operation to maintain voltage stability and provide reactive power compensation, new methods and upgraded systems will need to be investigated and developed to meet the significantly higher requirements of the FCC [41].

Most problems related to reactive power in the grid can be alleviated or resolved using passive inductive or capacitive filters, static thyristor compensators, or static synchronous compensators. However, these solutions are not always technically or economically effective. One possible approach is to investigate the use of the AFE not only for its primary function of AC/DC power conversion and load supply, but also as a means of providing reactive power compensation by leveraging the bidirectional power flow and control capabilities of AFE converters. Developing a reactive power compensation method in the grid using AFE will allow for reducing the reactive power level at the PCC without the need for additional compensation devices.

Many studies have investigated the role of AFE converters in reactive power control and also for various other purposes. The authors in [42], analyzed the grid-connected inverter using a preprogrammable PWM technique to control reactive power, by deriving a mathematical relation between the reactive power level, DC-bus voltage, and a constant modulation index. The work in [43] investigated the behavior of the AFE converter to operate at unity power factor with different time duration voltage sags by developing the simulation model. To overcome current harmonics and provide fast response, the authors in [44] proposed an improved dynamic average value model for AFE rectifiers, considering the lack of control signals during the starting stage and dead-time periods. In [45], a shunt active power filter is analyzed as a front-end converter for DC loads, applying generalized p-q theory with PWM technique. Additionally, NPC based recitifers are utilized in applications such as the low-frequency resonance suppressor in the tokamak power system, where they help mitigate low-frequency harmonics generated during tokamak operation [46].

Although many researchers have proposed using AFE as both an AC/DC converter and a reactive power compensator, most of their studies have focused on single-phase systems or under a constant DC-bus voltage. For instance, authors in [47] proposed a generalized average-current-mode-control for a $20\ \mathrm{kW}$, $10\ \mathrm{kHz}$, single-phase multilevel AFE used as a static reactive power compensator. Similarly, authors in [48] proposed a method for generating reactive power using AFE with a fixed DC-bus voltage in electric drive applications. Due to these limitations, the part of the thesis focuses on utilizing the AFE converter as a reactive power compensator in three-phase systems where the DC-bus voltage is not constant, such as the POPS-B converter at CERN.

Furthermore, while prior studies [49, 50, 51] have examined the RMS values and harmonic spectra of capacitor currents in a three-level NPC converter, they do not address how these parameters change with varying reactive power demands. Similarly, although neutral point potential voltage has been studied [52], the corresponding variation in neutral point current under different reactive power conditions remains largely unexplored. Therefore, a part of the thesis focuses on analyzing the impact of varying reactive power on neutral point current and semi-DC-bus voltage harmonic spectra with respect to reactive power, and also provides a comprehensive analysis of the AFE part of the PC as a reactive power compensator. These aspects are discussed in detail in chapter 2.

1.3 Background on Interleaved H-Bridge Converters

The subsequent part of this thesis shifts focus to the back-end converter stage, which interfaces the DC output of the rectifier with the coil load. In both particle accelerator and fusion applications, the coils can release stored energy back into the DC-bus during unloading conditions [53]. The DC-bus capacitors are primarily sized to store and supply the energy required by the coils [54]. Consequently, these capacitors effectively stabilize the DC-bus voltage and minimize the ripple. Additionally, the DC-bus provides near-complete decoupling between the front-end and back-end converter stages. This bidirectional energy flow necessitates that the DC/DC converter operate in all four quadrants, making HB topologies a preferred choice [55, 56, 57]. Particularly, parallel HB configurations are commonly employed to facilitate the use of low-power semiconductor switches in medium- and high-power applications [58, 59]. This is largely due to the cost-effectiveness and higher efficiency of lower-rated semiconductor modules when compared to their high-power counterparts. Parallelizing multiple HBs is a standard method to meet higher current demands [60], while also improving redundancy and system reliability [61].

However, directly paralleling HBs can introduce thermal imbalance. This arises from the negative temperature coefficient of semiconductor devices such as IGBTs and diodes, which may lead to thermal runaway [62]. To mitigate this risk, inductive elements are used to decouple the outputs of the HBs. With this configuration, the PWM carriers of each HB can be phase-shifted to reduce output current ripple, a technique known as interleaved operation or phase-shift PWM [63]. This method offers straightforward scalability and ease of implementation [64, 65, 66].

Two configurations for the DC/DC stage of the PC, both employing interleaved parallel HBs, have been explored: the CDC and the SDC. In the CDC approach, all HBs are connected to a single DC-bus. While this simplifies the architecture, the absence of galvanic isolation between HBs leads to circulating currents, which increase the electrical and thermal stress on semiconductors and inductors, ultimately reducing the PCs lifespan. In contrast, the SDC configuration introduces galvanic isolation between HBs, effectively eliminating circulating currents. However, this benefit comes at the cost of increasing the number of front-end components.

The analysis of circulating currents in interleaved HBs is not trivial, but it is fundamental to understanding the problem and finding effective solutions. An analysis limited to 2 HBs was conducted in [67]. Although subsequent studies have extended this analysis to a generic number of HBs in the CDC configuration, their primary focus has been on advanced control strategies rather than on analyzing the circulating current behavior with an increasing number of HBs. For instance, [68] proposed a new unipolar phase-shift modulation technique for the CDC configuration, aiming to control the internal circulating current and thereby reduce HB current distortion and PC losses. [69] Introduced a model predictive control combined with a sphere-decoding algorithm to achieve a very-fast transient response and guarantee a low load current tracking error for effective current sharing among HBs. However, these works do not analyze how the effect of the circulating current varies as the number of HBs increases, which is a key aspect in PC design addressed in this work. On the PC design side, to avoid circulating currents, [70] adopted the SDC topology with 4 parallel HBs in an interleaved configuration to supply $6\ \mathrm{kA}$ to the toroidal coil of the SMall Aspect Ratio Tokamak at the University of Seville. However, no criteria were provided for selecting the specific number of parallel HBs. In a similar way, [71] adopted the SDC topology with 10 parallel HBs in interleaving to provide $18\ \mathrm{kA}$ to the magnets in the high-luminosity particle accelerator LHC at CERN. Additionally, [72] adopted a topology involving 5 DC-buses, each DC-bus connected to 2 parallel HBs, to provide a current of $\pm 10\ \mathrm{kA}$ to the in-vessel vertical stabilization coil. Similarly, [73] adopted a topology involving 2 DC-buses, each DC-bus connected to 8 parallel power blocks, with each power block consisting of three parallel legs, to deliver an output current of $20\ \mathrm{kA}$ to the main magnet of the cyclotron at TRI University Meson Facility (TRIUMF). In a more focused study, [74] investigated the optimization of the number of parallel connected semiconductor switches to minimize losses in high-efficiency PC. However, the study conducted by [74] did not consider the CDC configuration.

A review of the literature shows that no general rule exists for selecting the back-end topology when functional requirements, such as the effect of circulating current percentage, are unconstrained. However, when such constraints are present, it becomes essential to establish design criteria that ensure the chosen topology meets all relevant requirements. To this end, part of the thesis proposes an algorithm that automatically determines the back-end converter topology, primarily addressing the drawbacks of circulating current effects. An in-depth discussion on validating the effect on the circulating current percentage in a generic number of parallel connected HBs and an algorithm proposal for topology selection of back-end converter are made in chapter 3.

1.4 Thesis Outline

The following chapters present various analyses of PC architectures used in particle accelerator and nuclear fusion reactor applications.

Chapter 2 provides a comprehensive study of the NPC based AFE stage of the POPS-B PC employed in CERNs BOOSTER ring, with a particular focus on its operation as a reactive power compensator. A DC-bus voltage control technique based on instantaneous energy balance is proposed and experimentally validated on a CERN prototype, enabling stable AFE operation under light-load conditions without violating the DC-bus voltage discharge limits or inducing over-modulation of the AFE. Experimental results confirm the viability of the proposed control strategy, demonstrating reliable regulation of both active and reactive power. Furthermore, the chapter delves into the analysis of the neutral point current inherent to the NPC topology, including its harmonic behavior under various reactive power scenarios, supported by both analytical and numerical analyses using two conventional grid control strategies: the synchronous rotating $dq-$frame; and the stationary $\alpha\beta-$frame. Additionally, the semi-DC-bus voltages and the harmonic spectrum of the DC-bus voltage are analytically characterized and experimentally validated.

Chapter 3 presents a comparative investigation of two back-end topologies composed of a generic number of interleaved parallel HBs: the CDC and the SDC. These configurations are analyzed with a focus on the RMS current in interleaved branches and the percentage of circulating current effect in CDC. The study examines the RMS currents in both configurations as functions of the number of HBs and gain ratios, with particular attention to the RMS of non-zero frequency components that indicate the presence of circulating currents in CDC. A normalization technique for the RMS current in CDC is introduced to decouple the output current and the effect of circulating current. Analytical models are validated both numerically and experimentally across a range of gain ratios and numbers of HBs. Furthermore, an algorithm is developed to determine the back-end converter topology based on system constraints, and its effectiveness is demonstrated through case studies.

Finally, chapter 4 concludes the dissertation by summarizing the main contributions and outlining potential directions for future research.

Chapter 2

Neutral Point-Clamped Active Front-End

This chapter presents a comprehensive analysis of the POPS-B PC existing at CERNs BOOSTER ring, in particular, the NPC based AFE as a reactive power compensator. Two conventional grid power control strategies, the $dq-$frame and $\alpha\beta-$frame, are investigated through MATLAB/Simulink simulations. Both strategies exhibit comparable performance, although the $\alpha\beta-$frame offers enhanced decoupling between active and reactive power regulation. The neutral point current that exists in NPC and its harmonic components are investigated analytically under varying reactive power cases and validated numerically. Furthermore, an instantaneous energy balance based DC-bus voltage control technique is proposed and implemented on a CERN prototype converter, enabling the AFE part to operate as a reactive power compensator under light load conditions. The capability of the AFE to regulate both active and reactive power is experimentally validated, confirming the effectiveness of the proposed control strategy without reducing the DC-bus voltage below a safe limit or causing over-modulation.

The NPC architecture is a widely used AC/DC AFE topology, particularly suited for high-voltage applications [75]. At CERN, an NPC-based PC is implemented in the BOOSTER accelerator ring, as illustrated in Fig. 2.1, and is referred to as POPS-B converter. The capacitor bank generally referred as DC-bus is used to exchange energy with the load during operation. The DC/DC stage of the POPS-B converter is designed as an HB, with each leg formed by three parallel-connected NPC legs. Switching is carried out at $333\ \mathrm{Hz}$ per leg, with a 120° phase shift between legs. This interleaving raises the effective switching frequency of the HB to $2\ \mathrm{kHz}$. The key parameters of the POPS-B converter are summarized in Table 2.1.

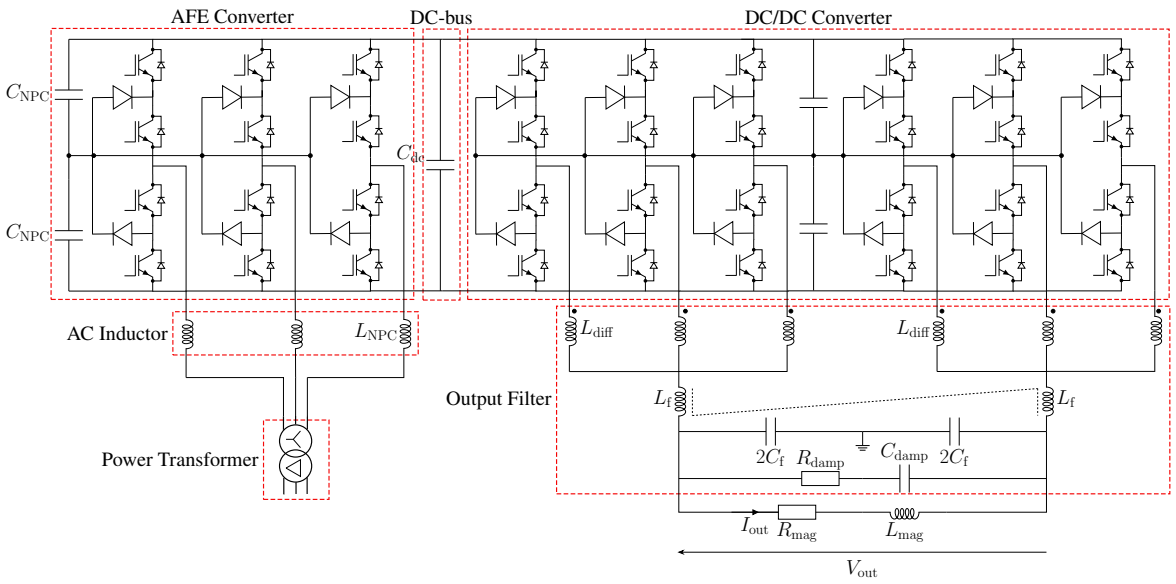


Figure 2.1: Electrical schematic of the POPS-B converter.

Table 2.1: POPS-B converter parameters.

Parameter	**Symbol**	**Value**	**Unit**
Transformer apparent power	S	3	MVA
Transformer primary voltage	V_{p}	18	kV
Transformer secondary voltage	V_{s}	1.95	kV
NPC inductance	L_{NPC}	700	μH
NPC capacitance	C_{NPC}	18	mF
DC-bus capacitance	C_{dc}	0.28	F
DC-bus voltage	$V_{\mathrm{dc,max}}$	5	kV
Magnet resistance	R_{mag}	270	mΩ
Magnet inductance	L_{mag}	100	mH
Maximum magnet current	I_{out}	6	kA
Maximum magnet voltage	V_{out}	3	kV
AFE switching frequency	$f_{\mathrm{s,AFE}}$	1	kHz
HB converter switching frequency	$f_{\mathrm{s,HB}}$	2	kHz

The POPS-B PC is rated for a maximum output current of 6 kA and a maximum output voltage of 3 kV. Each load cycle lasts 1.2 s and is continuously repeated throughout the year, operating for approximately 250 days. The output current i_{out} and voltage v_{out} waveforms corresponding to a single cycle are illustrated in Fig. 2.2.

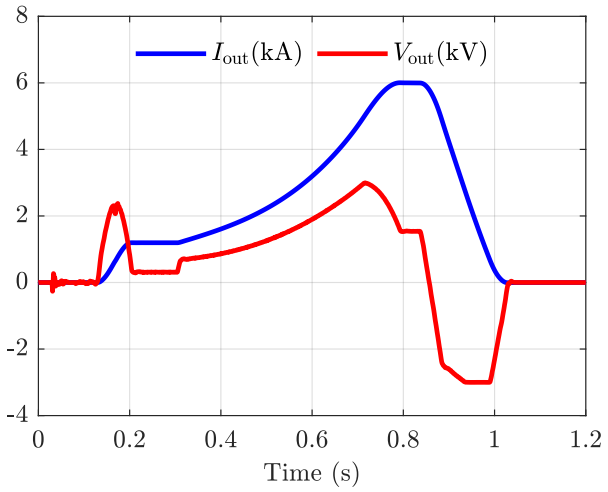


Figure 2.2: POPS-B power converters output current and voltage profile.

Considering the load magnet parameters ($L_{\text{mag}} = 100$ mH & $R_{\text{mag}} = 270$ mΩ), the peak power losses per cycle reaches 9.72 MW as shown in Fig. 2.3. In contrast, the peak active drawn from the grid is limited to 3 MW, also depicted in Fig. 2.3.

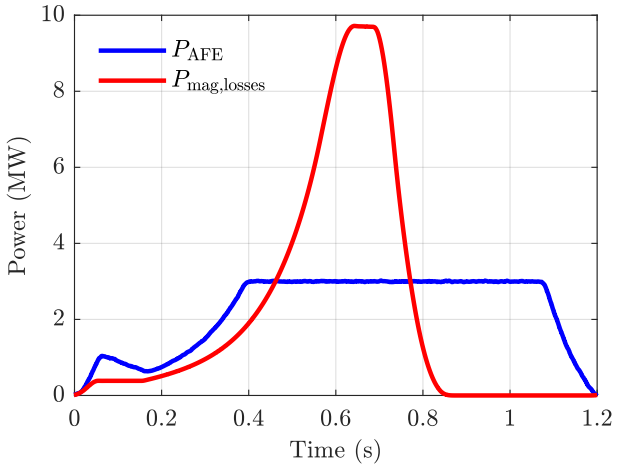


Figure 2.3: POPS-B power converters power profiles.

In typical coil-load applications, PCs draw active power from the grid equal to the resistive losses of the coil. The POPS-B converter at CERNs, however, adopts a different strategy: its AFE is designed to consume grid active power, not equivalent to the coil losses. This design choice results in more discharge of the DC-bus and extends the duration of peak grid power consumption. From the grid's perspective, this approach is advantageous, as it mitigates large active power swings and helps to flatten the active power consumption profile. In coil-load applications, the energy required by the load is primarily supplied by the storage medium, which is the capacitor bank of the feeding power converter, while the grid compensates for resistive losses in both the coil and the PC.

If, however, the resistive losses of both the coil and the PC are supplied directly from the grid, the corresponding DC-bus voltage discharge $v_{\text{dc}}(t)$, obtained from the energy balance of the PC, can be expressed as:

$$v_{\text{dc}}(t) = \sqrt{V_{\text{dc,max}}^2 - \left[\frac{L_{\text{mag}}}{C_{\text{dc}}} i_{\text{out}}(t)^2\right]}\,. \tag{2.1}$$

The discharge behavior of the DC-bus voltage under nominal load conditions, i.e., $I_{\text{mag,pk}} = 6\ \text{kA}$, as well as reduced operating conditions with $I_{\text{out,pk}} = 5\ \text{kA}, 4\ \text{kA}$, and $3\ \text{kA}$ is illustrated in Fig. 2.4. As the output current decreases, the energy storage requirement of the coil correspondingly reduces, leading to a smaller discharge from the capacitor bank. Under maximum output current conditions of $6\ \text{kA}$, the analytical evaluation yields a minimum DC-bus voltage of $3.48\ \text{kV}$.

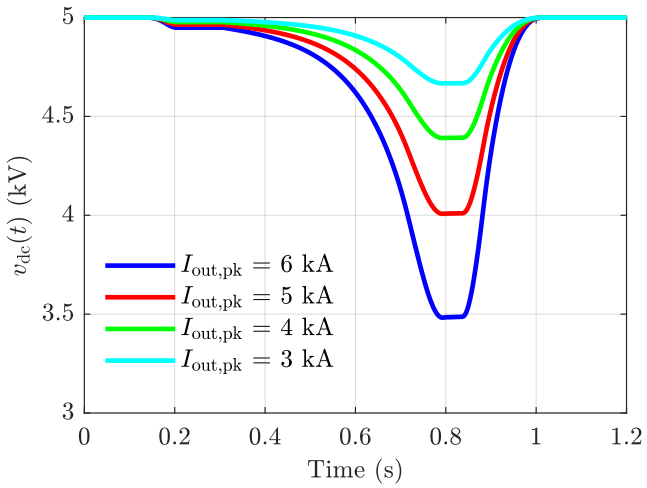


Figure 2.4: POPS-B converter DC-bus voltage profiles at various load current conditions.

The main objective of the AFE stage of the POPS-B converter is to perform AC/DC power conversion, maintain a unity power factor with the grid, and limit the input active power swing to $\pm 3\ \text{MW}$. At CERN, the current research focuses on the front-end stage of the POPS-B converter, with particular attention to its dual function as an AC/DC converter and as a reactive power compensator during the load cycle. Consequently, the studies are focused solely on the front-end stage of the POPS-B converter. With a clear understanding of the POPS-B converter architecture and operational objectives, the following section presents the control strategies implemented to ensure its desired operation.

2.1 Control Techniques

This section discusses the control strategies employed in the AFE stage of the POPS-B PC. These control strategies are implemented to ensure effective AC/DC power conversion, regulate both active and reactive power flow, maintain voltage balance across the semi-DC-buses, and regulate the DC-bus voltage under varying load conditions.

- *Grid power regulation:* Manages the exchange of active P_{AFE} and reactive power Q_{AFE} with the electrical grid.
- *Semi-DC-bus voltage balancing:* Ensures voltage symmetry across the semi-DC-buses (positive semi-DC-bus voltage $+V_{\mathrm{dc}}/2$, and negative semi-DC-bus voltage $-V_{\mathrm{dc}}/2$), which may otherwise differ due to variations in component characteristics or manufacturing inconsistencies.
- *Common-mode voltage injection:* Implements a control method that allows utilization of an additional 15% of the available DC-bus voltage.
- *Sinusoidal PWM modulation:* Generates PWM signals required for commutating the switching devices in the NPC converter legs.
- *DC-bus voltage regulation:* Controls the DC-bus voltage in the POPS-B converter.

2.1.1 Grid Power Regulation

This subsection provides a detailed analysis of the control techniques investigated for regulating power exchange between the grid and the POPS-B converter. Two reference frame-based methods are explored: the $dq-$frame control technique, which is currently implemented in the existing POSP-B converter and is widely used in AFE converters [76], [77], and the $\alpha\beta-$frame control technique, which is considered as an alternative [78], [79].

The mathematical model of the POSP-B converter AFE in the synchronous rotating $dq-$reference frame is given by:

$$v_{\mathrm{AFE,d}} = v_{\mathrm{g,d}} - \left(L\frac{\mathrm{d}i_{\mathrm{d}}}{\mathrm{d}t} + R_{\mathrm{NPC}} i_{\mathrm{d}} \right) + \omega L i_{\mathrm{q}} \,, \tag{2.2}$$

$$v_{\mathrm{AFE,q}} = v_{\mathrm{g,q}} - \left(L\frac{\mathrm{d}i_{\mathrm{q}}}{\mathrm{d}t} + R_{\mathrm{NPC}} i_{\mathrm{q}} \right) - \omega L i_{\mathrm{d}} \,. \tag{2.3}$$

Where, $v_{\mathrm{AFE,d}}$ and $v_{\mathrm{AFE,q}}$ are the AFE voltages in the $d-$and $q-$axis, respectively, while $v_{\mathrm{g,d}}$, and $v_{\mathrm{g,q}}$ are the $d-$ and $q-$ axis components of the grid voltage. Similarly, i_{d} and i_{q} represent the gird current components in the $d-$ and $q-$axes. The variable ω is the angular frequency of the rotating reference frame, and R_{NPC} is the internal resistance of the AFE inductor (L_{NPC}). The total inductance L includes both the AFE inductor and the equivalent inductance of the grid-connected transformer referred to its secondary side (L_{TF}):

$$L_{\mathrm{NPC}} + L_{\mathrm{TF}} \,. \tag{2.4}$$

The control architecture corresponding to the model of the system expressed in (2.2) and (2.3) is illustrated in Fig. 2.5.

In the schematic shown in Fig. 2.5, the output quantity is the three-phase AFE input voltage in the abc reference frame, denoted as $v_{\mathrm{AFE,abc(dq)}}$. The notation (dq) indicates that this three-phase voltage references are generated using a $dq-$frame control technique. The Phase-Locked Loop (PLL) is used to estimate the grid angular frequency ω, which is required for the transformation of three-phase abc quantities into the dq reference frame. The Proportional-Integral (PI) is used in the closed loop control structure.

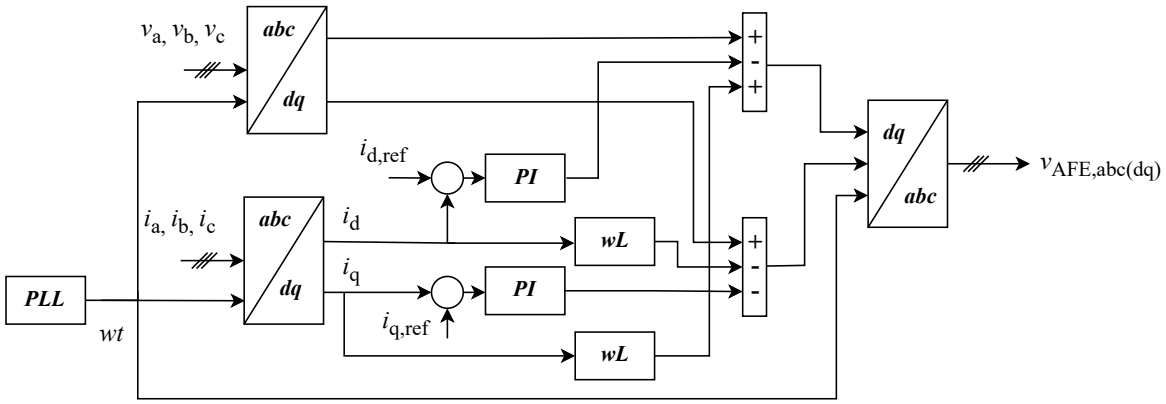


Figure 2.5: Schematic of the *dq*−frame reference control technique.

The active ($P_{\mathrm{AFE,d}}$) and reactive power ($Q_{\mathrm{AFE,d}}$) transferred between the AFE and the grid, in the synchronous reference frame *dq*-frame, can be expressed as:

$$\begin{cases} P_{\mathrm{AFE,d}} = \frac{3}{2} v_{\mathrm{g}} i_{\mathrm{d}} \\ Q_{\mathrm{AFE,d}} = \frac{3}{2} v_{\mathrm{g}} i_{\mathrm{q}} \end{cases} . \tag{2.5}$$

In an ideally decoupled system, (2.5) indicates that active power P_{AFE} is directly proportional to the $d-$axis component of the grid current i_{d} ($P_{\mathrm{AFE,dq}} \propto i_{\mathrm{d}}$), and reactive power $Q_{\mathrm{AFE,dq}}$ is directly proportional to the $q-$axis component of the grid current i_{q} ($Q_{\mathrm{AFE,dq}} \propto i_{\mathrm{q}}$). Hence, to maintain a unity power factor at the PCC, the controller sets ($i_{\mathrm{q,ref}} = 0$), thereby minimizing reactive power flow. The i_{d} component is then modulated to regulate the active power flow and, consequently, to control the DC-bus voltage. To achieve DC-bus voltage regulation V_{dc}, the i_{d} current can be obtained through the internal voltage u_{d}:

$$L \frac{\mathrm{d}i_{\mathrm{d}}}{\mathrm{d}t} + R_{\mathrm{NPC}} i_{\mathrm{d}} = u_{\mathrm{d}} , \tag{2.6}$$

where:

$$u_{\mathrm{d}} = v_{\mathrm{g,d}} - v_{\mathrm{AFE,d}} + \omega L i_{\mathrm{q}} . \tag{2.7}$$

Similarly, the $q-$axis current i_{q} is controlled through internal voltage u_{q}:

$$L \frac{\mathrm{d}i_{\mathrm{q}}}{\mathrm{d}t} + R_{\mathrm{NPC}} i_{\mathrm{q}} = u_{\mathrm{q}} , \tag{2.8}$$

with:

$$u_{\mathrm{q}} = v_{\mathrm{g,q}} - v_{\mathrm{AFE,q}} - \omega L i_{\mathrm{d}} . \tag{2.9}$$

If the reference frame is aligned such that the $d-$axis of the AFE voltage is aligned with the $d-$axis of the grid voltage, then:

$$v_{\mathrm{g}} = v_{\mathrm{g,d}} , \tag{2.10}$$

and,

$$v_{\mathrm{g,q}} = 0 . \tag{2.11}$$

Under steady-state conditions, and neglecting the voltage drop across the internal resistance, the simplified current expression for $d-$axis and $q-$axis component of grid current becomes:

$$i_{\mathrm{d}} \simeq \frac{v_{\mathrm{g,q}} - v_{\mathrm{AFE,q}}}{\omega L} \,, \tag{2.12}$$

$$i_{\mathrm{q}} \simeq \frac{v_{\mathrm{AFE,d}} - v_{\mathrm{g,d}}}{\omega L} \,. \tag{2.13}$$

Substituting (2.10) into the above (2.12) and (2.13):

$$i_{\mathrm{d}} \simeq -\frac{v_{\mathrm{AFE,q}}}{\omega L} \,, \tag{2.14}$$

$$i_{\mathrm{q}} \simeq \frac{v_{\mathrm{AFE,d}} - v_{\mathrm{g}}}{\omega L} \,. \tag{2.15}$$

From (2.14) and (2.15), it is evident that varying the $d-$axis component of the AFE voltage varies the $q-$axis component of the grid current, which controls reactive power. Varying the $q-$axis component of the AFE voltage varies the $d-$axis component of the current in the grid, thereby regulating the active power.

As illustrated in Fig. 2.6, controlling the magnitude of the AFE voltage enables reactive power regulation, while adjusting the phase affects the active power exchange with the grid.

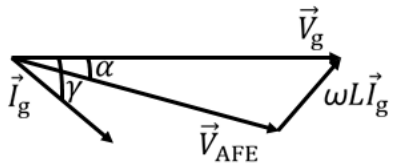


Figure 2.6: Phasor diagram of grid and AFE voltages.

One of the notable limitations of the *dq*-frame control technique is the presence of cross-coupling components in the dynamic model of the system ((2.2) and (2.3)). In the absence of proper decoupling between the $d-$axis and $q-$axis components of the grid currents may no longer respect the direct and independent proportionality relationship with the grid active and reactive power, respectively. Although the *dq*-frame control strategy facilitates effective decoupling between i_{d} and i_{q} components, its implementation is heavily dependent on a PLL for precise synchronization with the grid. The PLL estimates the instantaneous phase angle of the grid voltage, thereby ensuring accurate alignment of the rotating reference frame. However, this dependency introduces increased complexity, sensitivity to grid disturbances (such as voltage sags and harmonics), and potential stability challenges [80]. To overcome these limitations, an alternative control strategy, known as the $\alpha\beta-$frame, exists in the literature and has been investigated for the POPS-B converter [81].

Similar to the previously discussed $dq-$frame representation, the mathematical model of the AFE stage of the POPS-B converter can also be formulated in the stationary $\alpha\beta-$frame reference. The corresponding voltage equations are:

$$v_{\mathrm{AFE},\alpha} = v_{\mathrm{g},\alpha} - L\frac{\mathrm{d}i_{\alpha}}{\mathrm{d}t} - R_{\mathrm{NPC}}i_{\alpha} \,, \tag{2.16}$$

$$v_{\mathrm{AFE},\beta} = v_{\mathrm{g},\beta} - L\frac{\mathrm{d}i_\beta}{\mathrm{d}t} - R_{\mathrm{NPC}}i_\beta \ . \tag{2.17}$$

Where, $v_{\mathrm{AFE},\alpha}$ and $v_{\mathrm{AFE},\beta}$ represent the α and β components of the AFE voltages, while $v_{\mathrm{g},\alpha}$ and $v_{\mathrm{g},\beta}$ are the respective components of the grid voltages. Similarly, i_α and i_β represent the gird current components in the $\alpha\beta-$frame.

From (2.16) and (2.17), it is evident that the α component of AFE voltage has no terms of β components. Similarly, the β component of the AFE voltage has no terms of α components. This explains that there is no cross-coupling between the equations, which represent the dynamic model of the AFE. This inherently decoupled nature of the $\alpha\beta-$frame provides a distinct advantage over the $dq-$frame representation, particularly under dynamic operating conditions.

In $\alpha\beta-$frame grid voltage ($\overrightarrow{v_{\mathrm{g},\alpha\beta}}$) and current space ($\overrightarrow{i_{\alpha\beta}}$) phasors can be expressed as:

$$\overrightarrow{v_{\mathrm{g},\alpha\beta}}(t) = v_{\mathrm{g},\alpha}(t) + jv_{\mathrm{g},\beta}(t) \ , \tag{2.18}$$

$$\overrightarrow{i_{\alpha\beta}}^*(t) = i_\alpha(t) - ji_\beta(t) \ . \tag{2.19}$$

Using (2.18) and (2.19) expressions, the instantaneous active power $p_{\mathrm{AFE},\alpha\beta}$ consumption and reactive power $q_{\mathrm{AFE},\alpha\beta}$ exchanged between the grid and the POPS-B converter in the $\alpha\beta-$frame can be derived as:

$$p_{\mathrm{AFE},\alpha\beta}(t) = Re\left\{\frac{3}{2}\overrightarrow{v_{\mathrm{g},\alpha\beta}}(t)\overrightarrow{i_{\alpha\beta}}^*(t)\right\} = \frac{3}{2}\left[v_{\mathrm{g},\alpha}(t)i_\alpha(t) + v_{\mathrm{g},\beta}(t)i_\beta(t)\right] \ , \tag{2.20}$$

$$q_{\mathrm{AFE},\alpha\beta}(t) = Im\left\{\frac{3}{2}\overrightarrow{v_{\mathrm{g},\alpha\beta}}(t)\overrightarrow{i_{\alpha\beta}}^*(t)\right\} = \frac{3}{2}\left[-v_{\mathrm{g},\alpha}(t)i_\beta(t) + v_{\mathrm{g},\beta}(t)i_\alpha(t)\right] \ . \tag{2.21}$$

From (2.20) and (2.21), it can be seen that the active $p_{\mathrm{AFE},\alpha\beta}$ and reactive power $q_{\mathrm{AFE},\alpha\beta}$ flows can be directly regulated by adjusting the current components i_α and i_β.

If $i_\alpha = i_{\alpha,\mathrm{ref}}$, and $i_\beta = i_{\beta,\mathrm{ref}}$ then $p_{\mathrm{AFE},\alpha\beta}$ in (2.20) becomes $p_{\mathrm{AFE},\alpha\beta,\mathrm{ref}}$ and $q_{\mathrm{AFE},\alpha\beta}$ in (2.21) becomes $q_{\mathrm{AFE},\alpha\beta,\mathrm{ref}}$. Therefore, (2.20) and (2.21) can also be expressed as:

$$i_{\alpha,ref}(t) = \frac{2}{3}\left[\frac{v_{g,\alpha}}{v_{g,\alpha}^2 + v_{g,\beta}^2}p_{\mathrm{AFE},\alpha\beta,\mathrm{ref}}(t) + \frac{v_{g,\beta}}{v_{g,\alpha}^2 + v_{g,\beta}^2}q_{\mathrm{AFE},\alpha\beta,\mathrm{ref}}(t)\right] \ , \tag{2.22}$$

$$i_{\beta,ref}(t) = \frac{2}{3}\left[\frac{v_{g,\beta}}{v_{g,\alpha}^2 + v_{g,\beta}^2}p_{\mathrm{AFE},\alpha\beta,\mathrm{ref}}(t) + \frac{v_{g,\alpha}}{v_{g,\alpha}^2 + v_{g,\beta}^2}q_{\mathrm{AFE},\alpha\beta,\mathrm{ref}}(t)\right] \ . \tag{2.23}$$

Equations (2.22) and (2.23) suggest that $p_{\mathrm{AFE},\alpha\beta}$ and $q_{\mathrm{AFE},\alpha\beta}$ can be controlled independently. This is the salient feature of the $\alpha\beta-$frame control strategy. The implemented control strategy for regulating the active and reactive power in the $\alpha\beta-$frame is shown in Fig. 2.7.

The $\alpha\beta-$frame control technique requires a Proportional-Resonant Controller (PR) as shown in Fig. 2.7 [82]. It is evident from Fig. 2.7 that there is no requirement for the PLL. This simplification reduces control complexity and prevents synchronization errors associated with grid disturbances. Regardless of whether the grid power regulation is implemented in the *dq*$-$frame or $\alpha\beta-$frame, the resulting rectifier voltage v_{AFE} is used downstream to generate PWM signals for switching the NPC semiconductors.

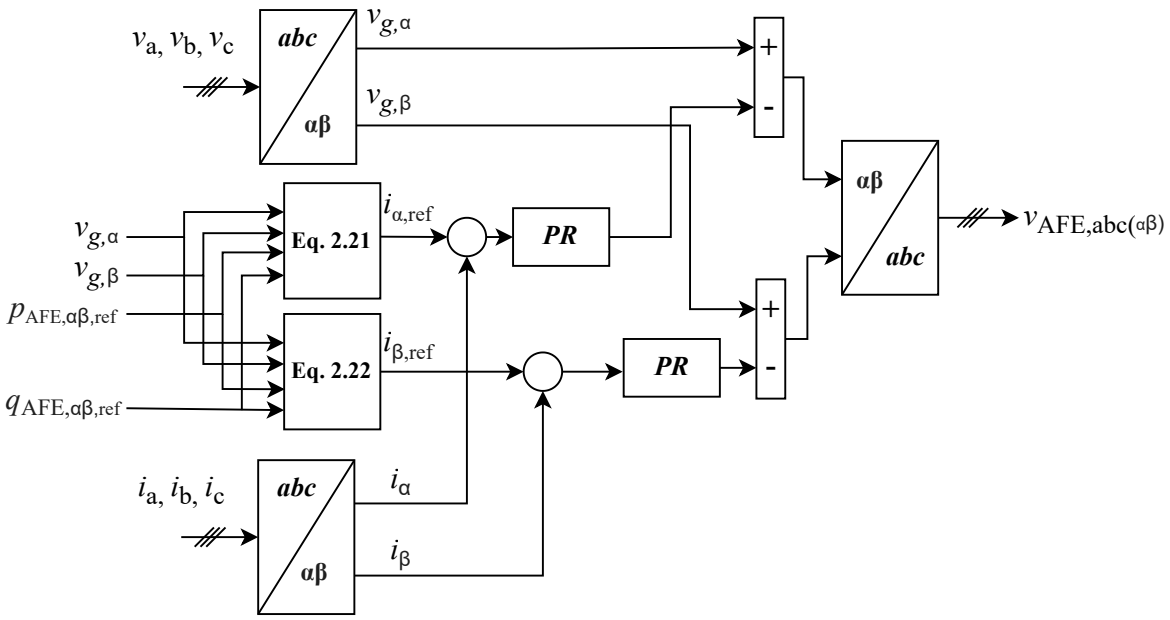
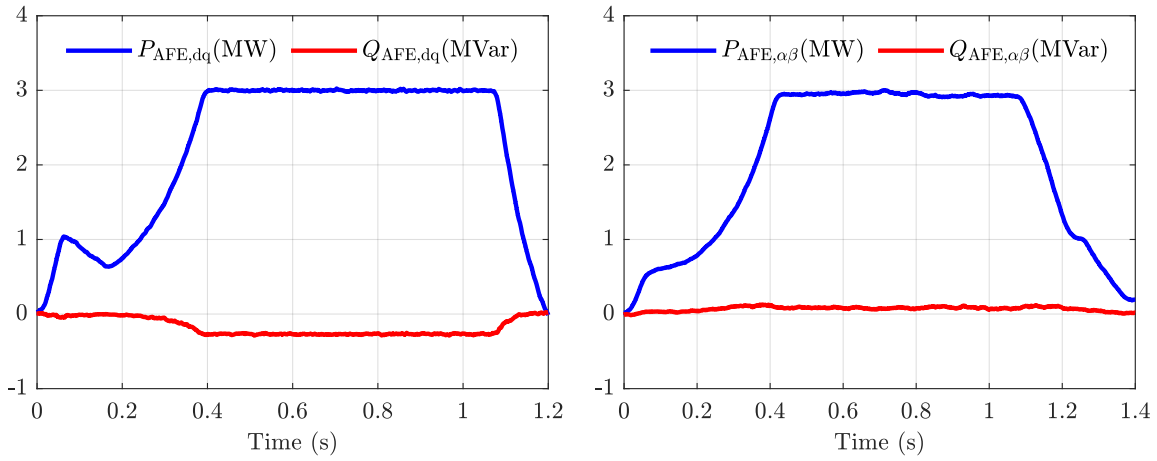


Figure 2.7: Schematic of $\alpha\beta-$frame control technique.

To validate the analytical developments of both the $dq-$frame and $\alpha\beta-$frame control technique for regulating the active power and reactive power consumption from the grid, numerical simulations were conducted in MATLAB/Simulink. A detailed numerical model was developed using the parameters listed in Table 2.1. The POPS-B converter is operated to supply a load current profile as shown in Fig. 2.2, with a peak active power draw of 3 MW and zero reactive power exchange 0 MVar.



(a) (b)

Figure 2.8: Active and reactive power profiles of the POPS-B converter operating with (a) $dq-$frame and (b) $\alpha\beta-$frame control technique.

The resulting active and reactive power profiles for both control methods are shown in Fig. 2.8(a) and Fig. 2.8(b), respectively. In the case of $dq-$frame control (Fig. 2.8(a)), even though the reference for the $q-$axis component i_{q} is set to zero ($i_{\mathrm{q,ref}} = 0$), the reactive power does not remain strictly zero. This deviation is attributed to the improper decoupling between the $d-$ and $q-$axes components, especially during the time instants when the active power demand is saturated. Conversely, in the $\alpha\beta-$frame control technique (Fig. 2.8(b)), the effect of the decoupling is much evident; the reactive power consumption across the entire load profile is almost equal to 0 Var, confirming the effectiveness of the control scheme.

2.1.2 Semi-DC-bus Voltage Balancing

This subsection details the control strategy employed to maintain voltage balance between the two semi-DC-buses in the AFE part of the POPS-B converter. Imbalances between the positive semi-DC-bus voltage $+V_{\mathrm{dc}}/2$, and negative semi-DC-bus voltage $-V_{\mathrm{dc}}/2$ can arise due to factors such as manufacturing tolerances in the balancing capacitors (C_{NPC}), inconsistent switching behavior of power devices, or asymmetries in the input grid voltages. These imbalances can lead to detrimental effects, including increased THD in the AC side voltage and premature failure of the switching devices due to overvoltage stress [83].

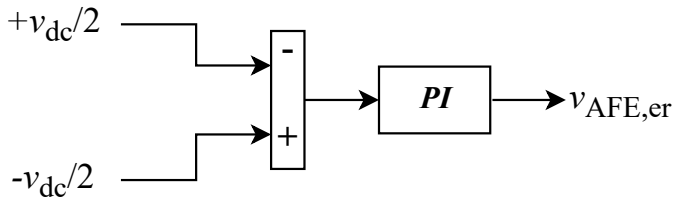


Figure 2.9: Control schematic for semi-DC-bus voltages balancing.

To mitigate these issues, a dedicated feedback control mechanism is necessary to ensure voltage balance between the positive semi-DC-bus and the negative semi-DC-bus. In this work, a simple yet effective PI controller is implemented for this purpose. The control strategy involves continuously monitoring the two semi-DC-bus voltages ($+V_{\mathrm{dc}}/2$ and $-V_{\mathrm{dc}}/2$) and calculating the error between them. This error signal is then processed by the PI controller, which generates a corrective offset. This offset is subsequently added to the rectifier voltage reference, thereby modifying the modulation index to compensate for the imbalance. The schematic of the semi-DC-bus voltage control technique is illustrated in Fig. 2.9. In the literature, other robust control techniques for balancing the semi-DC-bus voltages of the NPC converter also exist, such as those proposed in [84].

2.1.3 Common-mode Voltage Injection

This subsection presents the Common-Mode Voltage Injection (CMVI) control technique, which is implemented to extend the effective utilization of the DC-bus voltage of the POPS-B converter. As is well known in the literature, the CMVI method allows for the utilization of the magnitude of AFE voltage over 15% [85, 86]. The injected common-mode voltage is computed as:

$$v_{\mathrm{AFE,CMVI}}(t) = -\frac{1}{2}\left[\max\left(v_{\mathrm{AFE,a}}, v_{\mathrm{AFE,b}}, v_{\mathrm{AFE,c}}\right) + \min\left(v_{\mathrm{AFE,a}}, v_{\mathrm{AFE,b}}, v_{\mathrm{AFE,c}}\right)\right] . \quad (2.24)$$

The implementation of this technique becomes particularly crucial when the converter operates near the modulation limits, where over-modulation can constrain performance. This aspect is further discussed in Section 2.3. The schematic representation of the CMVI control strategy is shown in Fig. 2.10.

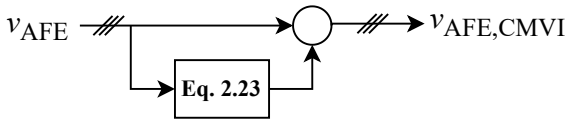


Figure 2.10: Schematic of common-mode voltage injection technique.

2.1.4 Sinusoidal PWM Modulation

This subsection describes the conventional sinusoidal PWM technique used for generating the switching signals required to control the semiconductor devices in each leg of the NPC converter [87]. The modulating signals for each leg of the NPC are obtained using the following expression:

$$m_{\text{AFE,x}} = \frac{2v_{\text{AFE,x}}}{v_{\text{dc}}}\,, \tag{2.25}$$

where x signifies the individual phases of the grid, namely a, b, and c. The term $v_{\text{AFE,x}}$ represents the reference voltage for the rectifier leg, which is synthesized as the sum of outputs from multiple control loops: the grid power regulation (operating in either the $dq-$ or $\alpha\beta-$ reference frame), the semi-DC-bus voltage balancing controller, and the common-mode voltage injection block.

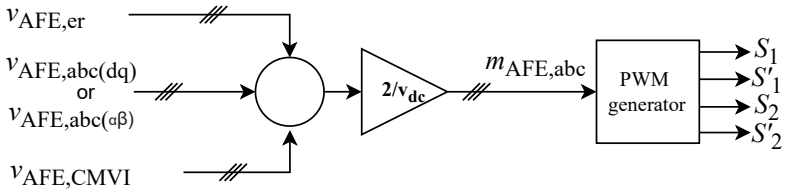


Figure 2.11: Schematic for PWMs generation.

This approach ensures that each PWM signal accurately reflects the combined control objectives of power flow regulation, voltage balancing, and over-modulation. The schematic of the PWM generation control architecture is shown in Fig. 2.11.

2.1.5 DC-bus Voltage Regulation

This section presents three different control strategies for regulating the DC-bus voltage, depending on the grid power flow requirements and system design constraints. These strategies include a constant, variable, and instantaneous energy balance based approach, each suited to specific applications.

Constant DC-bus Voltage Control

In systems with constant load profiles, the DC-bus voltage tends to remain constant. Therefore, a conventional control approach from the literature can be employed, as illustrated in Fig. 2.12.

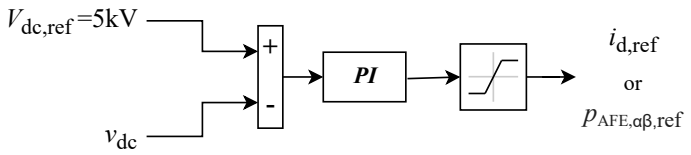


Figure 2.12: Schematic of the constant DC-bus voltage control.

This method is used to generate the reference signal for grid active power regulation, either the $d-$axis current component i_{d} in the *dq* control frame or the active power reference $p_{\mathrm{AFE},\alpha\beta,\mathrm{ref}}$ in the $\alpha\beta-$frame control.

Currently, a constant DC-bus voltage controller is implemented in the AFE stage of the POPS-B PC. This controller aims to regulate the power drawn from the grid to compensate for the converter's total power losses, estimated to be $9.72\ \mathrm{MW}$. However, since the AFE is rated only for $3\ \mathrm{MW}$, a saturation block is incorporated to limit the active power reference or corresponding $d-$axis component of the grid current value. The schematic of the existing DC-bus voltage control technique is shown in Fig. 2.12.

Variable DC-bus Voltage Control

In scenarios where the output current varies and the AFE rating matches the coil losses (i.e., $P_{\mathrm{AFE}} = P_{\mathrm{mag,loss}}$), a variable DC-bus voltage control scheme can be adopted, although this condition does not apply to the POPS-B converter. In this case, the energy balance in the PC can be described by:

$$\frac{1}{2}C_{\mathrm{dc}}\left[V_{\mathrm{dc,max}}^2 - v(t)^2\right] = \frac{1}{2}L_{\mathrm{mag}}i_{\mathrm{out}}(t)^2\,. \tag{2.26}$$

In this case, the total resistive losses in the circuit are drawn from the grid; therefore, the discharge of the capacitor bank is only to charge the output coil. Therefore, the reference for the DC-bus voltage can then be derived as:

$$v_{\mathrm{dc,ref}}(t) = \sqrt{V_{\mathrm{dc,max}}^2 - \left[\frac{L_{\mathrm{mag}}}{C_{\mathrm{dc}}}i_{\mathrm{out}}(t)^2\right]}\,. \tag{2.27}$$

Instead of applying a constant DC-bus voltage reference, this approach provides a time-varying trajectory for the voltage reference. The schematic for the variable DC-bus voltage control is shown in Fig. 2.13.

Instantaneous Energy Balance Based Approach for DC-bus Voltage Control

In applications such as the POPS-B converter, where the AFE power rating does not equal the PCs coil losses ($P_{\mathrm{AFE}} \neq P_{\mathrm{mag,loss}}$), a more generalized approach for controlling the DC-bus is implemented. This technique is derived from the instantaneous energy balance equation of the PC, formulated as:

$$\int p_{\mathrm{AFE}}(t)dt + \frac{C_{\mathrm{dc}}}{2}\left[V_{\mathrm{dc,max}}^2 - v_{\mathrm{dc}}^2(t)\right] = \int R_{\mathrm{mag}}i_{\mathrm{out}}^2(t)dt + \int L_{\mathrm{mag}}i_{\mathrm{out}}(t)\frac{\Delta i_{\mathrm{out}}}{\Delta t}dt\,. \tag{2.28}$$

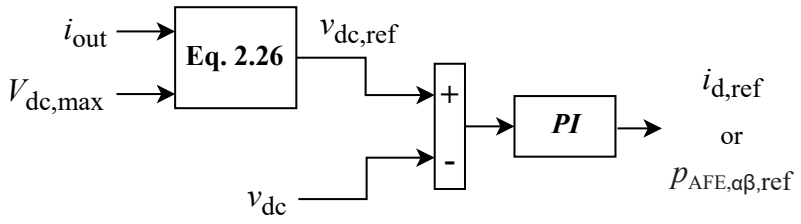


Figure 2.13: Schematic of the variable DC-bus voltage control.

Rearranging the terms gives the voltage reference as:

$$v_{\text{dc}} = \sqrt{V_{\text{dc,max}}^2 - \frac{2}{C_{\text{dc}}}\left[\int R_{\text{mag}} i_{\text{out}}^2(t)dt - \int p_{\text{AFE}}(t)dt + \int L_{\text{mag}} i_{\text{out}}(t)\frac{\Delta i_{\text{out}}}{\Delta t}dt\right]}. \quad (2.29)$$

This control strategy requires both the instantaneous output current $i_{\text{out}}(t)$ and the instantaneous grid power $p_{\text{AFE}}(t)$ as input signals. This strategy allows for providing a constant magnitude as an active power reference or a time-varying active power signal as a reference throughout the load cycle. Therefore, this instantaneous energy balance based approach for the DC-bus voltage makes it particularly suitable for applications where the active power consumption from the grid has to be varied based on the load profile. The schematic of the instantaneous energy balance based approach for the DC-bus voltage is provided in Fig. 2.14.

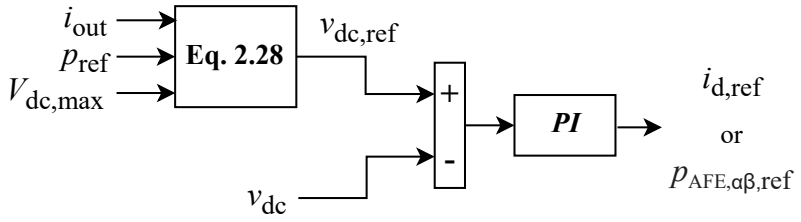


Figure 2.14: Schematic of instantaneous energy balance based DC-bus voltage control.

2.2 Neutral Point Current and Semi-DC-bus Voltages Analysis

This section presents a detailed analysis of the neutral point current and the semi-DC-bus voltages in the front-end stage of the POPS-B converter. The neutral point current is a critical parameter as it directly influences the voltage balance of the semi-DC-buses and increases the stress on the storage capacitor bank.

2.2.1 Neutral Point Current Analysis

This subsection focuses on the analytical derivation and harmonic evaluation of the neutral point current in the front-end stage of the POPS-B converter. The neutral point current is analyzed as a

function of AFE modulation indices and grid current, and its harmonics are characterized. Additionally, the subsection validates the analytical model with numerical simulations under various power factor conditions using both $dq-$frame and $\alpha\beta-$frame grid power regulation control strategies.

It is well known in the AFE configuration of the PC that the voltage across the AFE $v_{\mathrm{AFE,x}}(t)$ can be controlled by acting on its modulation index m_{x} from (2.25). One of the objectives of the AFE is to generate balanced three-phase voltages on the grid side terminal voltage. Hence, modulation indexes m_{x} must also be a balanced three-phase sinusoidal function of time with the required amplitude $m(t)$, frequency f_{g}, and phase angle ϕ. The three-phase modulation indexes are defined as:

$$\begin{cases} m_{\mathrm{a}}(t) = m(t)\cos\big[\varepsilon(t)\big] \,, \\ m_{\mathrm{b}}(t) = m(t)\cos\big[\varepsilon(t) - \dfrac{2\pi}{3}\big] \,, \\ m_{\mathrm{c}}(t) = m(t)\cos\big[\varepsilon(t) - \dfrac{4\pi}{3}\big] \,. \end{cases} \tag{2.30}$$

Here, $\varepsilon(t) = (\omega t + \phi)$, denotes the phase angle and frequency.

Similarly, the three-phase AFE currents are expressed as:

$$\begin{cases} i_{\mathrm{a}}(t) = i(t)\cos\big[\varepsilon(t) - \gamma\big] \,, \\ i_{\mathrm{b}}(t) = i(t)\cos\big[\varepsilon(t) - \gamma - \dfrac{2\pi}{3}\big] \,, \\ i_{\mathrm{c}}(t) = i(t)\cos\big[\varepsilon(t) - \gamma - \dfrac{4\pi}{3}\big] \,. \end{cases} \tag{2.31}$$

Where γ represents the phase displacement between the grid current and the corresponding grid voltage, commonly referred to as the power factor angle.

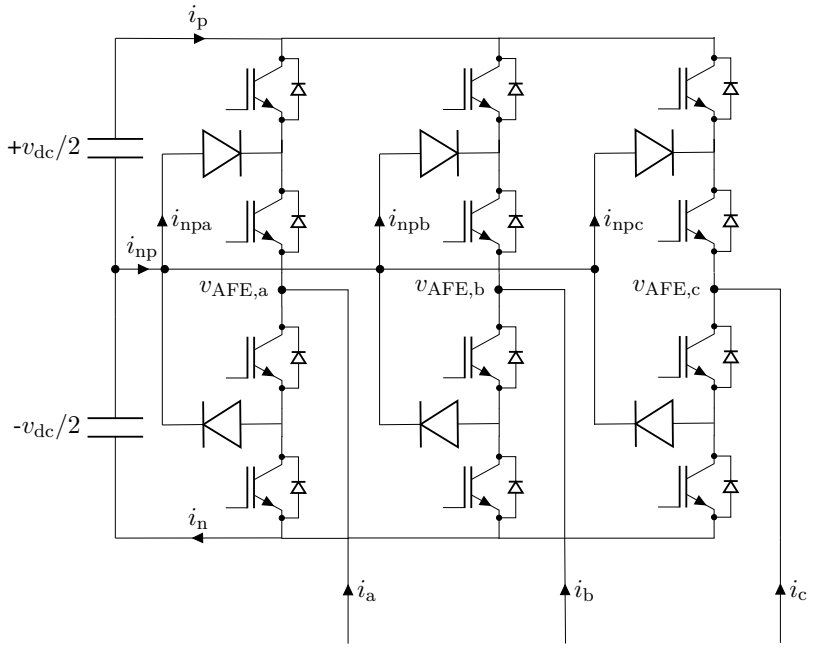


Figure 2.15: Schematic of the NPC converter.

From Fig. 2.15, the neutral point current at each phase terminal of the NPC can be expressed as:

$$i_{\mathrm{np,x}} = i_{\mathrm{x}}(t) - (i_{\mathrm{p,x}} + i_{\mathrm{n,x}}) \ , \tag{2.32}$$

where $i_{\mathrm{p,x}}$ and $i_{\mathrm{n,x}}$ denote the positive and negative side currents, respectively, of phase x in the AFE. These currents, expressed in terms of the modulation index m_{x}, are given by:

$$\begin{cases} i_{\mathrm{p,x}} = sgn(m_{\mathrm{x}})\, m_{\mathrm{x}}(t)\, i_{\mathrm{x}}(t) \ , \\ i_{\mathrm{n,x}} = -sgn(-m_{\mathrm{x}})\, m_{\mathrm{x}}(t)\, i_{\mathrm{x}}(t) \ . \end{cases} \tag{2.33}$$

Substituting (2.33) into (2.32) yeilds:

$$i_{\mathrm{np,x}} = i_{\mathrm{x}}(t) - m_{\mathrm{x}}(t) i_{\mathrm{x}}(t) \left[sgn(m_{\mathrm{x}}) - sgn(-m_{\mathrm{x}}) \right] \ . \tag{2.34}$$

Equation (2.34) can be simplified to:

$$i_{\mathrm{np,x}} = i_{\mathrm{x}}(t) - f_{\mathrm{x}}(t) \ , \tag{2.35}$$

where:

$$f_{\mathrm{x}}(t) = m_{\mathrm{x}}(t) i_{\mathrm{x}}(t) \left[sgn(m_{\mathrm{x}}) - sgn(-m_{\mathrm{x}}) \right] \ . \tag{2.36}$$

The neutral point current that flows into the midpoint of the semi-DC-bus voltages i_{np} is then expressed as the sum of the individual phase contributions.

$$i_{\mathrm{np}} = i_{\mathrm{np,a}} + i_{\mathrm{np,b}} + i_{\mathrm{np,c}} \ . \tag{2.37}$$

Substituting (2.35) into (2.37) results in:

$$i_{\mathrm{np}} = i_{\mathrm{a}}(t) + i_{\mathrm{b}}(t) + i_{\mathrm{c}}(t) - \left[f_{\mathrm{a}}(t) + f_{\mathrm{b}}(t) + f_{\mathrm{c}}(t) \right] \ . \tag{2.38}$$

In a balanced three-phase system, the sum of the phase currents is zero $(i_{\mathrm{a}}(t) + i_{\mathrm{b}}(t) + i_{\mathrm{c}}(t) = 0)$. Therefore, (2.38) simplifies to:

$$i_{\mathrm{np}} = - \left[f_{\mathrm{a}}(t) + f_{\mathrm{b}}(t) + f_{\mathrm{c}}(t) \right] \ . \tag{2.39}$$

Equation (2.39) shows that the neutral point current is governed by the sum of the functions $f_{\mathrm{a}}(t)$, $f_{\mathrm{b}}(t)$, and $f_{\mathrm{c}}(t)$. Since these functions are periodic, they can be represented by their Fourier series. In a balanced three-phase system $f_{\mathrm{b}}(t)$ and $f_{\mathrm{c}}(t)$ are phase-shifted versions of $f_{\mathrm{a}}(t)$, with delays of $-2\pi/3$ and $-4\pi/3$ respectively. Consequently, the summation $[f_{\mathrm{a}}(t) + f_{\mathrm{b}}(t) + f_{\mathrm{c}}(t)]$ cancels out for all harmonic components except the DC component and integer multiples of three.

By substituting, the $a-$phase modulation index (2.30) and $a-$phase AFE current (2.31) into (2.36), and applying trigonometric identities, the function $f_{\mathrm{a}}(t)$ becomes:

$$f_{\mathrm{a}}(t) = \left(\frac{mi}{2} \right) \left[\cos(\gamma) + \cos(2\varepsilon - \gamma) \right] \left[sgn(m_{\mathrm{a}}) - sgn(-m_{\mathrm{a}}) \right] \ . \tag{2.40}$$

Here, m is the maximum value of the three phase modulation index, i is the maximum value of the three phase grid current, and the term $[sgn(m_{\mathrm{a}}) - sgn(-m_{\mathrm{a}})]$ is a periodic function, and can therefore be expanded into a Fourier series:

$$sgn(m_{\mathrm{a}}) - sgn(-m_{\mathrm{a}}) = \left(\frac{4}{\pi}\right) \sum_{h=1,3,5,..}^{\infty} \frac{1}{h} \sin(\frac{h\pi}{2}) \cos(h\varepsilon) \; . \tag{2.41}$$

In (2.41), h is the harmonic index; thus, $\cos(h\varepsilon)$ corresponds the h-th harmonic component of the periodic waveform, where $h = 1, 3, 5, ...$

Substituting (2.41) into (2.40) and simplifying with the trigonometric properties gives:

$$\begin{aligned} f_{\mathrm{a}}(t) = \left(\frac{2mi}{\pi}\right) \Bigg[\cos\gamma \sum_{h=1,3,5,..}^{\infty} \frac{1}{h} \sin\left(\frac{h\pi}{2}\right) \cos(h\varepsilon) \\ + \sum_{h=1,3,5,..}^{\infty} \frac{1}{h} \sin\left(\frac{h\pi}{2}\right) \cos(h\varepsilon) \cos(2\varepsilon - \gamma) \Bigg] \; . \end{aligned} \tag{2.42}$$

Similarly, expanding the functions $f_{\mathrm{b}}(t)$ and $f_{\mathrm{c}}(t)$, and substituting into (2.39), the resulting neutral-point current can be expressed as:

$$\begin{aligned} i_{\mathrm{np}}(t) = &- \left(\frac{6mi}{\pi}\right) \cos\gamma \sum_{h=3,9,15,..}^{\infty} \frac{1}{h} \sin\left(\frac{h\pi}{2}\right) \cos(h\varepsilon) \\ &- \left(\frac{3mi}{\pi}\right) \sum_{h=5,11,17,..}^{\infty} \frac{1}{h} \sin\left(\frac{h\pi}{2}\right) \cos\left[(h-2)\varepsilon + \gamma\right] \\ &- \left(\frac{3mi}{\pi}\right) \sum_{h=1,7,13,..}^{\infty} \frac{1}{h} \sin\left(\frac{h\pi}{2}\right) \cos\left[(h+2)\varepsilon - \gamma\right] \; . \end{aligned} \tag{2.43}$$

Equation (2.43) can be rearranged into an alternative, more compact form:

$$\begin{aligned} i_{\mathrm{np}}(t) = &- \left(\frac{6mi}{\pi}\right) \cos\gamma \sum_{h=3,9,15,..}^{\infty} \frac{1}{h} \sin\left(\frac{h\pi}{2}\right) \cos(h\varepsilon) \\ &+ \left(\frac{3mi}{\pi}\right) \sum_{h=3,9,15,..}^{\infty} \frac{1}{h+2} \sin\left(\frac{h\pi}{2}\right) \cos\left[h\varepsilon + \gamma\right] \\ &+ \left(\frac{3mi}{\pi}\right) \sum_{h=3,9,15,..}^{\infty} \frac{1}{h-2} \sin\left(\frac{h\pi}{2}\right) \cos\left[h\varepsilon - \gamma\right] \; . \end{aligned} \tag{2.44}$$

The analytical formulation in (2.44) demonstrates that the neutral point current contains no DC component. Instead, it is composed exclusively of odd triple$-n$ harmonics, with the third harmonic

being the most significant. Accordingly, the neutral point current can be well approximated by retaining only the third harmonic term, giving:

$$\begin{aligned} i_{\mathrm{np}}(t) \cong &- \left(\frac{6mi}{\pi}\right) \cos\gamma \frac{1}{3} \sin\left(\frac{3\pi}{2}\right) \cos\left(3\varepsilon\right) \\ &+ \left(\frac{3mi}{\pi}\right) \frac{1}{5} \sin\left(\frac{3\pi}{2}\right) \cos\left[3\varepsilon + \gamma\right] \\ &+ \left(\frac{3mi}{\pi}\right) \sin\left(\frac{3\pi}{2}\right) \cos\left[3\varepsilon - \gamma\right] \ . \end{aligned} \tag{2.45}$$

Equation (2.45) can be further simplified to:

$$i_{\mathrm{np}}(t) \approx \left(\frac{4mi}{5\pi}\right) \left[-2\cos\gamma\cos\left(3\varepsilon\right) - 3\sin\gamma\sin\left(3\varepsilon\right)\right] \ . \tag{2.46}$$

Rearranging (2.46) yields:

$$i_{\mathrm{np}}(t) \approx \left(\frac{4mi}{5\pi}\right) \sqrt{4 + 5\sin^2\gamma} \cos\left[3\varepsilon + \pi - \tan^{-1}(1.5\tan\gamma)\right] \ , \tag{2.47}$$

or equivalently,

$$i_{\mathrm{np}}(t) \approx \left(\frac{4mi}{5\pi}\right) \sqrt{9 - 5\cos^2\gamma} cos\left[3\varepsilon + \pi - \tan^{-1}(1.5\tan\gamma)\right] \ . \tag{2.48}$$

The neutral point current is therefore dependent on the AFE operating point. From (2.47) and (2.48), it is evident that the amplitude of the neutral point current i_{np} is linearly proportional to the AC-side terminal voltage v_{AFE}, since the modulation index m is a function of v_{AFE} from (2.25). In contrast, the neutral point current i_{np} has a non-linear relationship with the AFE power factor γ.

The maximum magnitude of i_{np} occurs when the NPC operates at zero power factor. The magnitude of neutral point current at zero power factor is expressed as:

$$i_{\mathrm{np}}(t) \approx \left(\frac{4mi}{5\pi}\right) \sqrt{9} \approx 0.76mi \ . \tag{2.49}$$

Equation (2.49) shows that the magnitude of neutral point current can be as high as 76% of the amplitude of the converters AC side grid current and the product of modulation index, especially when exchanging power with the AC side of the system as a static compensator.

On the other hand, the magnitude of the neutral point current has the smallest value when it exchanges power at a unity power factor:

$$i_{\mathrm{np}}(t) \approx \left(\frac{4mi}{5\pi}\right) \sqrt{9 - 5} \approx 0.51mi \ . \tag{2.50}$$

Even under unity power factor, the amplitude of the neutral point current i_{np} is approximately 51% of the modulation index and grid current product. This highlights the importance of analyzing the neutral point current in the NPC based front-end stage of the POPS-B converter, as the storage capacitor must accommodate this additional neutral point current, in addition to the current required for the load

energy. Moreover, it is essential to investigate the variation of the neutral point current magnitude with various reactive power cases, as the POPS-B converter will be analyzed for its use as a reactive power compensator in the following sections.

To validate the analytical developments of the neutral point current and to characterize its harmonic components under both $dq-$frame and $\alpha\beta-$frame control, numerical simulations were carried out in the Matlab/Simulink environment using the circuit shown in Fig. 2.1. The simulations considered a maximum load current of 5.4 kA and a maximum active power consumption from the grid of 2.82 MW, at various reactive power cases such as 0 MVar, 1 MVar (inductive) and -1 MVar (capacitive). The harmonic components of the neutral point current were obtained using a Fast Fourier Transform applied to the simulated waveforms. The frequency range of interest was limited to 1.2 kHz, corresponding to a maximum harmonic order of $h = 24$ for a 50 Hz grid frequency.

The waveforms in Fig. 2.16 show the neutral point current under the $dq-$frame control technique. The waveforms in Fig. 2.16(a) correspond to the neutral point current at $P_{\mathrm{AFE}} = 2.82$ MW and $Q_{\mathrm{AFE}} = 0$ MVar. Similarly, Fig. 2.16(b) correspond to the neutral point current at $P_{\mathrm{AFE}} = 2.82$ MW and $Q_{\mathrm{AFE}} = 1$ MVar, and Fig. 2.16(c) correspond to the neutral point current at $P_{\mathrm{AFE}} = 2.82$ MW and $Q_{\mathrm{AFE}} = -1$ MVar.

The blue traces in the Fig. 2.16 correspond to the instantaneous neutral point current obtained from analytical results, while the red envelope corresponds to the peak value of the neutral point current obtained from numerical results. To quantitatively assess the accuracy of the analytical model, the relative peak error is defined as the absolute difference between the analytical and numerical peak values, normalized with respect to the numerical result.

At $P_{\mathrm{AFE}} = 2.82$ MW and $Q_{\mathrm{AFE}} = 0$ MVar, the peak value of the neutral point current from numerical results is 586.7 A and from analytical results is 552.3 A, yielding a relative error of 5.86%. For $P_{\mathrm{AFE}} = 2.82$ MW and $Q_{\mathrm{AFE}} = 1$ MVar, the peak value of the neutral point current from numerical results is 601.5 A and from analytical results is 574.5 A, corresponding to a relative error of 4.49%. For $P_{\mathrm{AFE}} = 2.82$ MW and $Q_{\mathrm{AFE}} = -1$ MVar, the peak value of the neutral point current from numerical results is 658.5 A and from analytical results is 642.81 A, resulting in a relative error of 2.38%. In all reactive power cases, numerical results correspond to the peak value of the neutral point current is higher compared to the peak value of the neutral point current obtained from analytical results, due to the reason that the developed analytical model for the neutral point current (2.48) is approximated to its third harmonic component, whereas the numerical results include harmonic components up to the 24^{th} order. It is also observed that the difference in the peak values obtained from numerical simulations with analytical results at each reactive power case is low compared to the magnitudes of the neutral point current, since the most dominant harmonics in the neutral point current are the 3^{rd} harmonic component, which is at 150 Hz.

From both the analytical and numerical results in Fig. 2.16, it is evident that the peak value of neutral point current at the cases with $Q_{\mathrm{AFE}} = -1$ MVar and $Q_{\mathrm{AFE}} = 1$ MVar is higher compared to $Q_{\mathrm{AFE}} = 0$ MVar, since the neutral point current is also a function of the modulation index m, where m depends on the AFE voltage $v_{\mathrm{AFE,dq}}$. The magnitude of $v_{\mathrm{AFE,dq}}$ is dependent on the reactive power. From Fig. 2.16, in both the analytical results and numerical results, it is evident that the peak value of the neutral point current corresponding to the case $Q_{\mathrm{AFE}} = -1$ MVar is larger than the case with $Q_{\mathrm{AFE}} = 1$ MVar since the $v_{\mathrm{AFE,dq}}$ corresponding to capacitive reactive power is higher than the inductive reactive power.

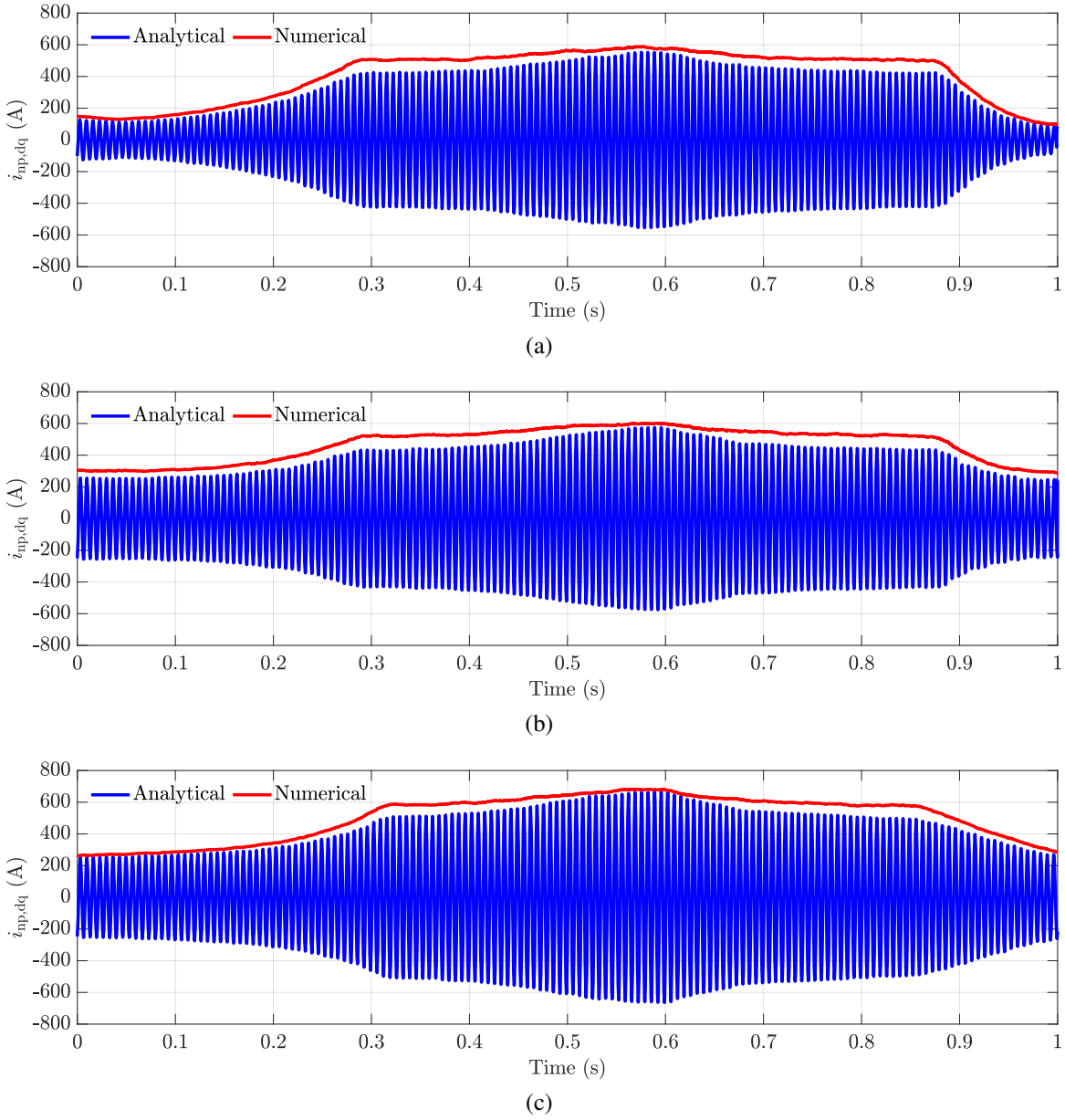


Figure 2.16: Analytical and numerical results of neutral point current with $dq-$frame control technique at $P_{\mathrm{AFE,max}} = 2.82$ MW and: (a) $Q_{\mathrm{AFE}} = 0$ MVar; (b) $Q_{\mathrm{AFE}} = 1$ MVar; and (c) $Q_{\mathrm{AFE}} = -1$ MVar.

A similar validation was conducted for the $\alpha\beta-$frame control, as shown in Fig. 2.17. Table 2.2 consists of the analytical and numerical peak values of the neutral point current for all considered reactive power cases, along with the relative error. The relative error decreases as the reactive power changes from 0 MVar to -1 MVar which is from 5.56% to 2.63% respectively, confirming that the analytical model provides a good approximation of the neutral point current in the $\alpha\beta$-frame.

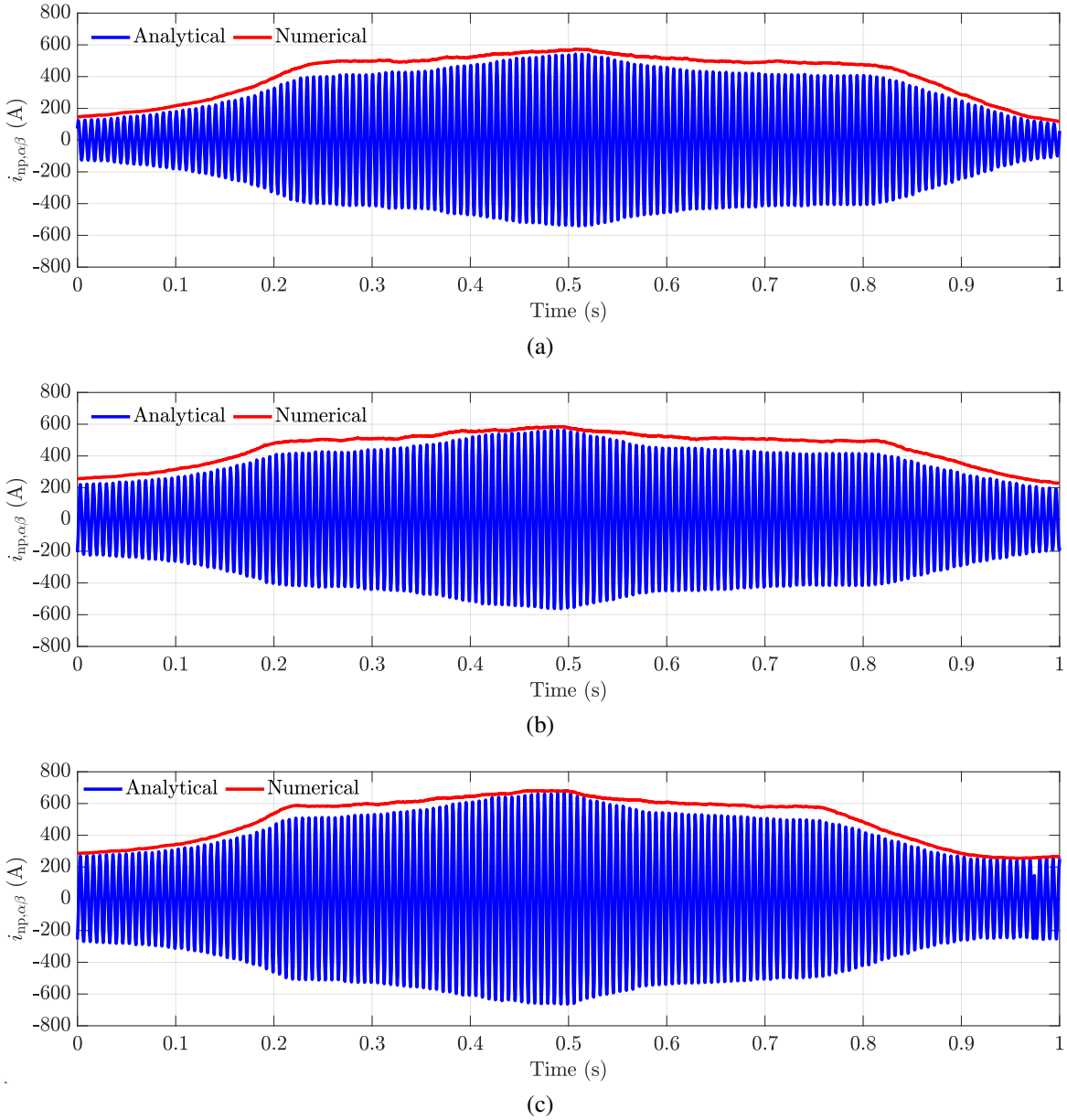


Figure 2.17: Analytical and numerical results of neutral point current with $\alpha\beta-$frame control technique at $P_{\mathrm{AFE,max}} = 2.82$ MW and: (a) $Q_{\mathrm{AFE}} = 0$ MVar; (b) $Q_{\mathrm{AFE}} = 1$ MVar; (c) $Q_{\mathrm{AFE}} = -1$ MVar.

The results for the analysis of neutral point current using $dq-$frame control and $\alpha\beta-$frame control technique fairly agree. Additionally, the results obtained using the $\alpha\beta-$frame control technique show that the magnitudes of the peak neutral point current, as calculated from numerical simulations, are higher than those obtained from analytical results. This is because numerical simulations encompass all the harmonic components present in the i_{np}.

Table 2.2: Summary of neutral point currents in $dq-$ and $\alpha\beta-$frame control techniques at various reactive power cases.

$P_{\mathbf{AFE,dq}}$	$Q_{\mathbf{AFE,dq}}$	$i_{\mathbf{np,dq}}$			$i_{\mathbf{np,\alpha\beta}}$		
		Analytical	**Numerical**	**Error**	**Analytical**	**Numerical**	**Error**
2.82 MW	0 MVar	552.3 A	586.7 A	5.86%	542.1 A	574 A	5.56%
2.82 MW	1 MVar	574.5 A	601.5 A	4.49%	562.2 A	585.1 A	3.91%
2.82 MW	−1 MVar	642.8 A	658.5 A	2.38%	663.1 A	681.02 A	2.63%

Similar to the $dq-$frame control technique, in both the analytical results and numerical results, the peak value of neutral point current at the case $Q_{\mathrm{AFE}} = -1$ MVar is larger than $Q_{\mathrm{AFE}} = 1$ MVar, and is larger than $Q_{\mathrm{AFE}} = 0$ MVar. The summary of the peak value of the neutral point current in the various reactive power cases obtained from the $dq-$frame control technique and the $\alpha\beta-$frame control technique is presented in Table 2.2.

The harmonic spectrum of the neutral point current relative to grid frequency f_{g} is expressed as:

$$f_{\mathrm{np,g}} = 3kf_{\mathrm{g}}, \qquad k = 1, 3, 5, ... \tag{2.51}$$

In addition, sideband harmonics appear around the switching frequency $f_{\mathrm{s,AFE}}$ of the AFE, expressed as:

$$f_{\mathrm{np,sb}} = nf_{\mathrm{s,AFE}} \pm kf_{\mathrm{g}}\,, \qquad n = 1, 2, 3, ... \tag{2.52}$$

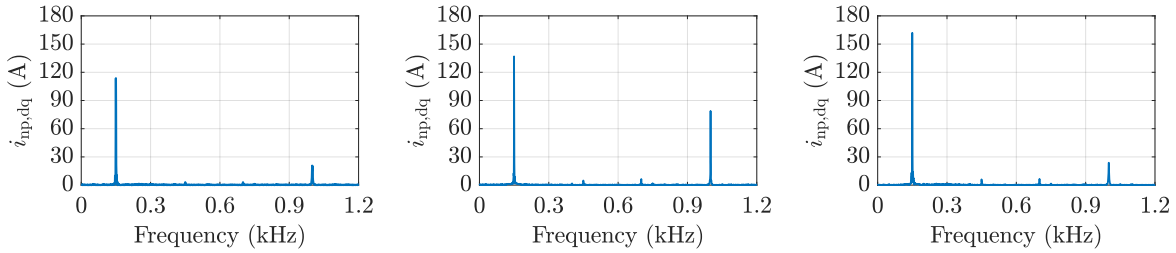


Figure 2.18: Harmonic spectra of neutral point current in $dq-$frame at $P_{\mathrm{AFE,max}} = 2.82$ MW and: (a) $Q_{\mathrm{AFE}} = 0$ MVar; (b) $Q_{\mathrm{AFE}} = 1$ MVar; (c) $Q_{\mathrm{AFE}} = -1$ MVar.

Table 2.3: Neutral point current harmonics at 150 Hz and 450 Hz.

$P_{\mathbf{AFE,dq}}$	$Q_{\mathbf{AFE,dq}}$	$dq-$frame		$\alpha\beta-$frame	
		$\mathbf{3^{rd}}$ **= 150 Hz**	$\mathbf{9^{th}}$ **= 450 Hz**	$\mathbf{3^{rd}}$ **=150 Hz**	$\mathbf{9^{th}}$ **= 450 Hz**
2.82 MW	0 MVar	113.6 A	3.1 A	105.6 A	2.4 A
2.82 MW	1 MVar	136.9 A	4.9 A	125.1 A	4.3 A
2.82 MW	−1 MVar	161.9 A	6.1 A	167.9 A	6.5 A

However, in NPC topologies, the contribution of switching frequency harmonics is negligible compared to the third-order grid harmonic [88]. The harmonic spectrum of the neutral point current

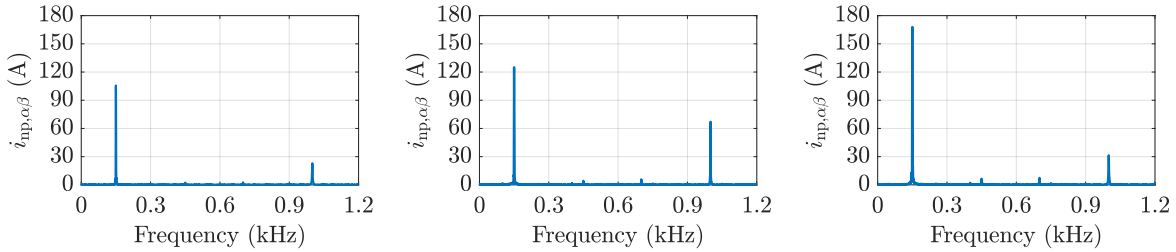


Figure 2.19: Harmonic spectra of neutral point current in $\alpha\beta-$frame at $P_{\mathrm{AFE,max}} = 2.82$ MW and: (a) $Q_{\mathrm{AFE}} = 0$ MVar; (b) $Q_{\mathrm{AFE}} = 1$ MVar; (c) $Q_{\mathrm{AFE}} = -1$ MVar.

with various reactive power cases obtained from numerical simulations using the $dq-$frame control technique and the $\alpha\beta-$frame control technique is shown in Fig. 2.18 and Fig. 2.19, respectively. The spectra in Fig. 2.18 and Fig. 2.19 confirm that the neutral point current has no DC component and contains only odd multiples of triple harmonics. Among these the 3^{rd} harmonic component at 150 Hz is dominant, while higher-order components such as 15^{th}, 21^{st}.., components, which are at frequencies 450 Hz, and 750 Hz respectively, are significantly smaller, in all reactive power cases. The magnitude of the neutral point current harmonics at 150 Hz and 450 Hz are presented in Table 2.3.

The results obtained from the $dq-$frame are in close agreement with those from the $\alpha\beta-$frame control technique. As summarized in Table 2.3, both approaches exhibit a consistent trend with respect to harmonic magnitudes across different reactive power cases. Specifically, for the 150 Hz harmonic, the magnitude at $Q = 0$ Var is lower than at $Q = 160$ Var, which in turn is lower than at $Q = -160$ Var. A similar ordering is observed for the 450 Hz component, where $Q = 0$ Var yields the smallest magnitude, followed by $Q = 160$ Var, and finally $Q = -160$ Var, which results in the largest value. This same pattern is consistently observed when using the $\alpha\beta-$frame control technique.

2.2.2 Semi-DC-bus Voltages and DC-bus Voltage Harmonic Analysis

In addition to the neutral point current, the semi-DC-bus voltages in the NPC converter, namely the positive semi-DC-bus voltage $+v_{\mathrm{dc}}/2$ and the negative semi-DC-bus voltage $-v_{\mathrm{dc}}/2$, also exhibit harmonic components. Analyzing these voltages provides insight into the behavior of the DC-bus voltage under different reactive power conditions.

The harmonic content present in the neutral point current is similarly reflected in the semi-DC-bus voltages. Besides the DC component, the harmonic spectrum of the semi-DC-bus voltages at the grid frequency $f_{\mathrm{sdc,g}}$ can be expressed as:

$$f_{\mathrm{sdc,g}} = 3kf_{\mathrm{g}}\,, \tag{2.53}$$

while the harmonic spectrum of the semi-DC-bus voltages corresponding to the switching frequency $f_{\mathrm{sdc,sw}}$ are given by:

$$f_{\mathrm{sdc,sw}} = nf_{\mathrm{sw}}\,, \tag{2.54}$$

and the sideband harmonics around the switching frequency $f_{\mathrm{sdc,sb}}$ are:

$$f_{\mathrm{sdc,sb}} = nf_{\mathrm{sw}} \pm kf_{\mathrm{g}}\,, \tag{2.55}$$

where $k = 1, 3, 5, \ldots$ and $n = 1, 2, 3, \ldots$.

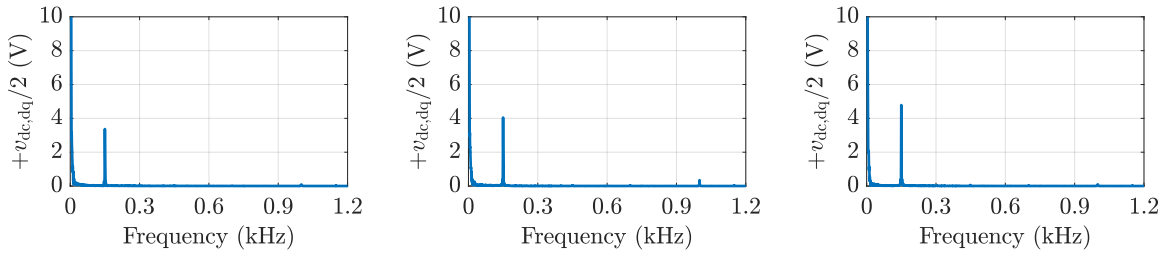


Figure 2.20: Harmonic spectra of positive semi-DC-bus voltage in $dq-$frame at $P_{\text{AFE,max}} = 2.82$ MW and: (a) $Q_{\text{AFE}} = 0$ MVar; (b) $Q_{\text{AFE}} = 1$ MVar; and (c) $Q_{\text{AFE}} = -1$ MVar.

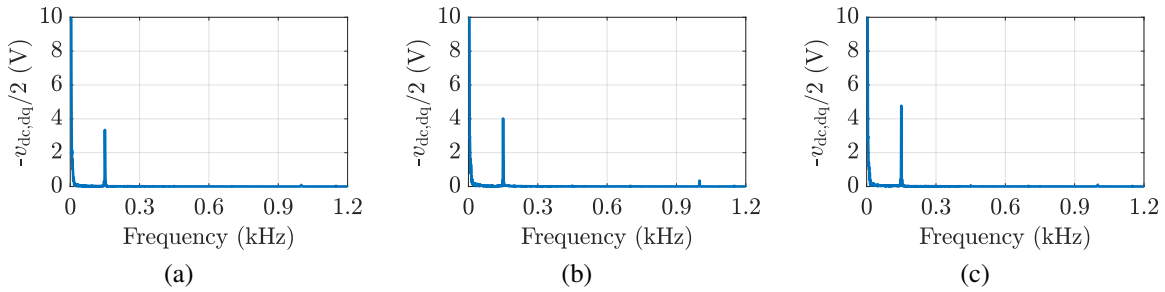


Figure 2.21: Harmonic spectra of negative semi-DC-bus voltage in $dq-$frame at $P_{\text{AFE,max}} = 2.82$ MW and: (a) $Q_{\text{AFE}} = 0$ MVar; (b) $Q_{\text{AFE}} = 1$ MVar; and (c) $Q_{\text{AFE}} = -1$ MVar.

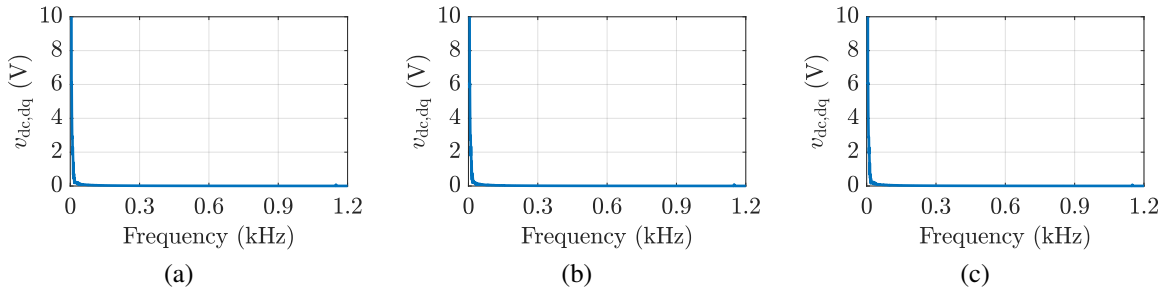


Figure 2.22: Harmonic spectra of DC-bus voltage in $dq-$frame at $P_{\text{AFE,max}} = 2.82$ MW and: (a) $Q_{\text{AFE}} = 0$ MVar; (b) $Q_{\text{AFE}} = 1$ MVar; (c) $Q_{\text{AFE}} = -1$ MVar.

The plots in Fig. 2.20, Fig. 2.21, and Fig. 2.22 illustrate the harmonic specta of the positive semi-DC-bus voltage, negative semi-DC-bus voltage, and DC-bus voltage, respectively, for $P_{\text{AFE,max}} = 2.82$ MW and $Q_{\text{AFE}} = 0$ MVar, 1 MVar, -1 MVar using the $dq-$frame control technique. In Fig. 2.20 and Fig. 2.21, similar to the neutral point current, the third-order harmonic is the dominant component, and its amplitude is largest for $Q_{\text{AFE}} = -1$ MVar, followed by $Q_{\text{AFE}} = 1$ MVar case, and smallest at $Q_{\text{AFE}} = 0$ MVar. However, in all cases, the dominant third-order harmonic is insignificant compared to the DC component of 2.5 kV. Table 2.4 summarizes the 150 Hz harmonic

magnitudes of both positive and negative semi-DC-bus voltages. It is evident from Table 2.4 that the harmonic magnitudes are almost similar for both positive and negative semi-DC-bus voltages across all reactive power cases.

Table 2.4: positive semi-dc-bus voltage and negative semi-dc-bus voltage harmonics at 150 Hz in $dq-$frame control technique and $\alpha\beta-$frame control technique.

$\boldsymbol{P_{\mathrm{AFE,dq}}}$	$\boldsymbol{Q_{\mathrm{AFE,dq}}}$	$\boldsymbol{dq}-$frame		$\boldsymbol{\alpha\beta}-$frame	
		$\boldsymbol{+v_{\mathrm{dc}}/2}$ **150 Hz**	$\boldsymbol{-v_{\mathrm{dc}}/2}$ **150 Hz**	$\boldsymbol{+v_{\mathrm{dc}}/2}$ **150 Hz**	$\boldsymbol{-v_{\mathrm{dc}}/2}$ **150 Hz**
2.82 MW	0 MVar	3.37 V	3.34 V	3.28 V	3.25 V
2.82 MW	1 MVar	4.05 V	4.02 V	3.71 V	3.69 V
2.82 MW	-1 MVar	4.78 V	4.77 V	4.96 V	4.95 V

Fig. 2.22 illustrates the harmonic spectrum of the DC-bus voltage in the $P_{\mathrm{AFE,max}} = 2.82$ MW and $Q_{\mathrm{AFE}} = 0$ MVar, $Q_{\mathrm{AFE}} = 1$ MVar, $Q_{\mathrm{AFE}} = -1$ MVar cases. The harmonic spectrum of the total DC-bus voltage, shown in Fig. 2.22, does not contain a significant third-order component, confirming that the DC-bus voltage is largely free of low-order harmonics.

The harmonic analysis performed using the $\alpha\beta-$frame control technique shown in Fig. 2.23, Fig. 2.24, and Fig. 2.25, respectively, correspond to the harmonic spectrum of positive semi-DC-bus voltage, negative semi-DC-bus voltage, and DC-bus voltage at $P_{\mathrm{AFE,max}} = 2.82$ MW and $Q_{\mathrm{AFE}} = 0$ MVar, $Q_{\mathrm{AFE}} = 1$ MVar, and $Q_{\mathrm{AFE}} = -1$ MVar cases.

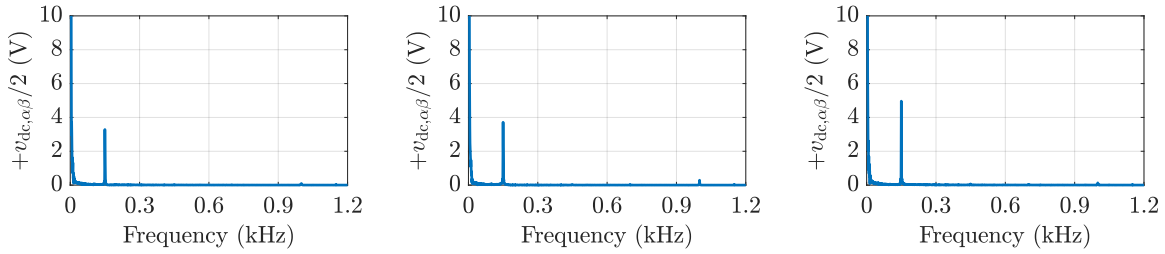


Figure 2.23: Harmonic spectra of positive semi-DC-bus voltage in $\alpha\beta-$frame at $P_{\mathrm{AFE,max}} = 2.82$ MW and: (a) $Q_{\mathrm{AFE}} = 0$ MVar; (b) $Q_{\mathrm{AFE}} = 1$ MVar; (c) $Q_{\mathrm{AFE}} = -1$ MVar.

Consistent with the observations from the $dq-$frame control technique, the $\alpha\beta-$frame control results exhibit a similar pattern in harmonic variation across different reactive power cases. As shown in Fig. 2.25, the DC-bus voltage does not display the third-order harmonic. Table 2.4 summarizes the 150 Hz harmonic magnitudes for both the positive and negative semi-DC-bus voltages under the $\alpha\beta$-frame control technique. Overall, the harmonic analysis results obtained from the $dq-$frame and $\alpha\beta-$frame control techniques show good agreement.

In summary, the semi-DC-bus voltages display third-order harmonics that follow the same trends as the neutral point current, while the overall DC-bus voltage remains largely unaffected by low-order harmonics. The consistency between $dq-$frame and $\alpha\beta-$frame analyses validates the accuracy of the harmonic characterization for different reactive power cases.

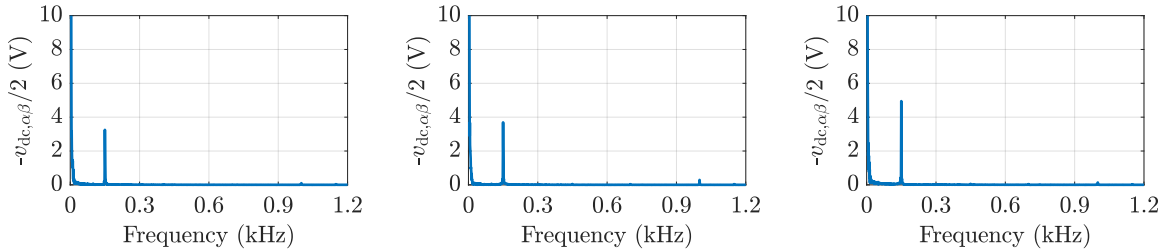


Figure 2.24: Harmonic spectra of negative semi-DC-bus voltage in $\alpha\beta-$frame at $P_{\mathrm{AFE,max}} = 2.82$ MW and: (a) $Q_{\mathrm{AFE}} = 0$ MVar; (b) $Q_{\mathrm{AFE}} = 1$ MVar; (c) $Q_{\mathrm{AFE}} = -1$ MVar.

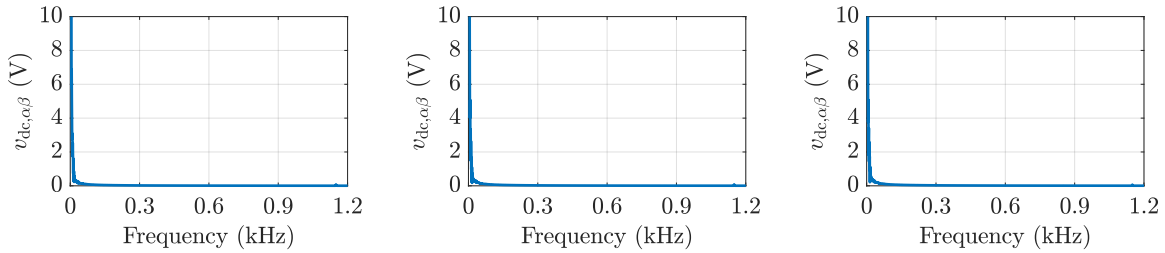


Figure 2.25: Harmonic spectra of DC-bus voltage in $\alpha\beta-$frame at $P_{\mathrm{AFE,max}} = 2.82$ MW and: (a) $Q_{\mathrm{AFE}} = 0$ MVar; (b) $Q_{\mathrm{AFE}} = 1$ MVar; (c) $Q_{\mathrm{AFE}} = -1$ MVar.

2.3 Analysis of the Active Front-End as a Reactive Power Compensator

The analysis of the AFE converter extends beyond its conventional role of regulating the DC-bus voltage while maintaining unity power factor at the PCC. It also includes the AFEs capability to function as a reactive power compensator under light load conditions. In such scenarios, the active power drawn from the grid is considerably reduced, leaving underutilized AFE capacity that can be leveraged to exchange reactive power with the grid. This capability is particularly useful for injecting capacitive reactive power, as the CERN network is predominantly composed of inductive loads.

The capability of the AFE to operate as a reactive power compensator is subject to certain limitations:

- *The apparent power rating of the grid-connected transformer.*
- *The overmodulation limit of the AFE.*

At CERN, the POPS-B converter and its associated grid-connected transformer are already designed, with the transformer rated for a nominal apparent power of 3 MVA. Consequently, when the AFE operates to exchange reactive power with the grid, the total apparent power, given by $S = \sqrt{P_{\mathrm{AFE}}^2 + Q_{\mathrm{AFE}}^2}$, must not exceed this rating. Hence, for this specific application, the apparent power rating of the grid-connected transformer imposes a limit on the AFEs operation as a reactive power compensator.

Under full load conditions, the POPS-B converter must provide a peak current of $6\ \mathrm{kA}$ and a peak voltage of $3\ \mathrm{kV}$, corresponding to a peak active power consumption of $3\ \mathrm{MW}$. In this scenario, the DC-bus voltage drops to $3.48\ \mathrm{kV}$, leaving a little margin between the minimum DC-bus voltage and the maximum output voltage. Consequently, there is minimal scope to further reduce active power consumption, limiting the AFEs ability to provide capacitive reactive power to the grid. In contrast, during light load conditions, reducing the active power drawn from the grid increases the DC-bus capacitor discharge and allows the AFE to inject capacitive reactive power into the grid.

Reducing the active power consumption from the grid increases the DC-bus capacitor discharge, while increasing the exchange of capacitive reactive power raises the AFE voltage magnitude. In both cases, whether by reducing active power consumption or by supplying capacitive reactive power, the modulation index of the AFE increases, as indicated in (2.25). This highlights the importance of the CMVI control technique, which extends the usable AFE voltage margin by approximately 15%.

To regulate the exchange of active and reactive power with the grid while operating the AFE as a reactive power compensator, the instantaneous energy based DC-bus voltage control technique proposed in Section 2.1.5 is utilized. For the analysis, a light load condition is considered, defined by $i_{\mathrm{out,pk}} = 30\ \mathrm{A}$ and a minimum DC-bus voltage discharge of $45\ \mathrm{V}$, with the maximum DC-bus voltage limited to $50\ \mathrm{V}$. In particular, $i_{\mathrm{out,pk}} = 30\ \mathrm{A}$ is analyzed since the same load profile condition is used for experimental validation in Section 2.4.

The objective is to determine two independent limits:

- The minimum active power that can be drawn from the grid without reducing the DC-bus voltage below $45\ \mathrm{V}$.
- The maximum reactive power that can be exchanged with the grid without exceeding the AFE modulation index defined limit.

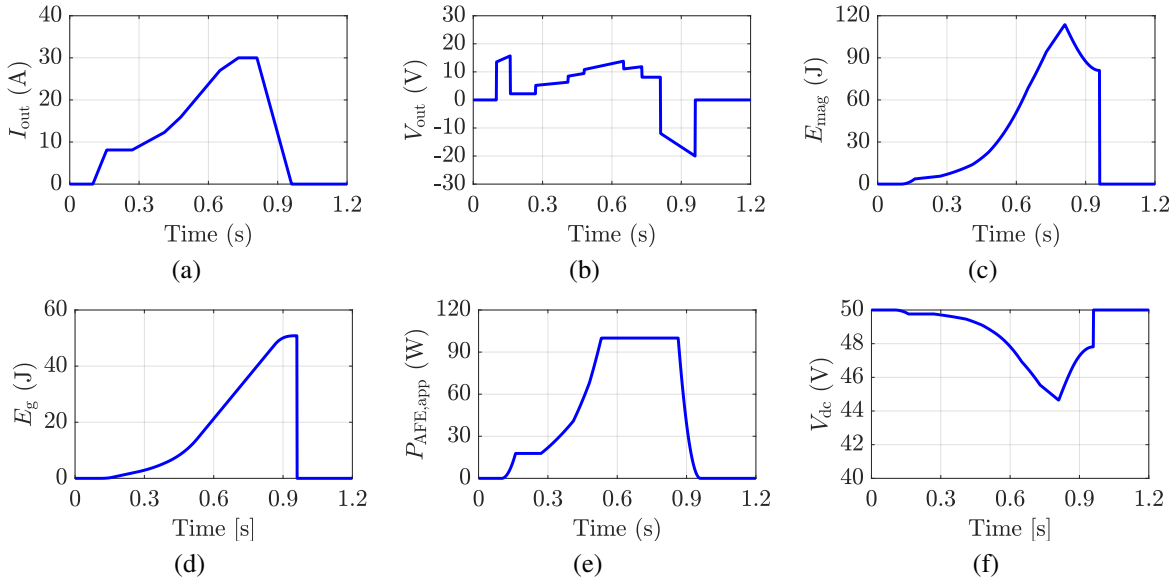


Figure 2.26: Analytical results for (a) output current; (b) output voltage; (c) magnet energy; (d) energy from the grid; (e) active power; and (f) DC-bus voltage profiles.

To estimate the minimum active power consumption and maximum capacitive reactive power injection into the grid, both are analytically evaluated independently. First, to estimate the maximum value of the active power, a piecewise linear equation is used to generate the output current reference profile, similar to Fig. 2.2, but with the peak value limited to 30 A, as shown in Fig. 2.26(a). With the magnet specifications known, the voltage across it is obtained (Fig. 2.26(b)), followed by the calculation of magnet energy via power integration (Fig. 2.26(c)). To obtain the maximum active power corresponding to the current profile depicted in Fig. 2.26(a), the instantaneous energy balance equation (2.28) is applied. By allowing the DC-bus voltage to discharge down to 45 V and solving (2.28) using the substitution method, both the DC-bus voltage profile and the grid active power consumption profile are obtained. The resulting waveforms are presented in Fig. 2.26(f) and Fig. 2.26(e), respectively.

The upper bound for capacitive reactive power injection is evaluated under the condition that the AFE does not enter overmodulation when the DC-bus voltage drops to 45 V. For a three-phase system, the relationship between reactive power exchange and AFE voltage magnitude can be expressed as:

$$Q_{\mathrm{AFE}} = \sqrt{3}\frac{V_{\mathrm{g}}V_{\mathrm{AFE}}\cos\alpha - V_{\mathrm{AFE}}^2}{X_{\mathrm{l}}} \,. \tag{2.56}$$

Here, V_{g} is the RMS line-to-line grid voltage, V_{AFE} is the RMS AFE voltage, $\cos\alpha$ is the phase angle between V_{g} and V_{AFE}, and X_{l} represents the equivalent reactance between the grid and the AFE. It is well known that the reactive power primarily depends on the magnitude of the AFE voltage. Considering this relationship, and by substituting the values of V_{g} and X_{l}, the nonlinear equation is linearized using Taylor series expansion. Accordingly, the reactive power as a function of AFE voltage can be expressed as:

$$Q_{\mathrm{AFE}} = -\frac{1}{5.5e^{-4}}\left(\frac{V_{\mathrm{AFE}} + 4.785}{21.1} - 1\right) \,. \tag{2.57}$$

With the minimum DC-bus voltage limited to 45 V, the maximum attainable voltage across the AFE V_{AFE} is also limited by (2.25), assuming a maximum modulation index of $m_{\max} = 0.8$. This conservative modulation limit is chosen due to the approximations involved in deriving (2.57). Moreover, a small variation in V_{AFE} greatly affects the magnitude of Q_{AFE}. By obtaining the required maximum AFE voltage from (2.25) and substituting it into (2.57), the resulting reactive power is $Q_{\mathrm{AFE}} = -164.4$ Var. The analytical values obtained for both active power and capacitive reactive power exchange under a 30 A peak load profile are later confirmed through experimental validation in Section 2.4. These results demonstrate the feasibility of operating the AFE as a reactive power compensator under light-load conditions while respecting system constraints.

2.4 Experimental Validation

In this section, the experimental validation of the AFE operating as a reactive power compensator is primarily reported, including the characterization semi-DC-bus voltages and DC-bus voltage harmonics. Table 2.5 collects the prototype converter main parameters. The prototype used for experimental validation replicates the POPS-B converter architecture illustrated in Fig. 2.1, with system parameters equivalent to the POPS-B converter but scaled down in current and voltage ratings by a factor of 100.

Table 2.5: POPS-B prototype parameters.

Parameter	**Symbol**	**Value**	**Unit**
Transformer apparent power	S	500	VA
Transformer primary voltage	V_{p}	400	V
Transformer secondary voltage	V_{s}	19.5	V
NPC inductance	L_{NPC}	800	μH
NPC capacitance	C_{NPC}	18	mF
DC-bus capacitance	C_{dc}	0.28	F
DC-bus voltage	V_{dc}	50	V
Magnet resistance	R_{mag}	270	mΩ
Magnet inductance	L_{mag}	100	mH
Maximum magnet current	I_{out}	50	A
Maximum magnet voltage	V_{out}	30	V
AFE switching frequency	$f_{\mathrm{s,AFE}}$	1	kHz
HB converter switching frequency	$f_{\mathrm{s,HB}}$	2	kHz

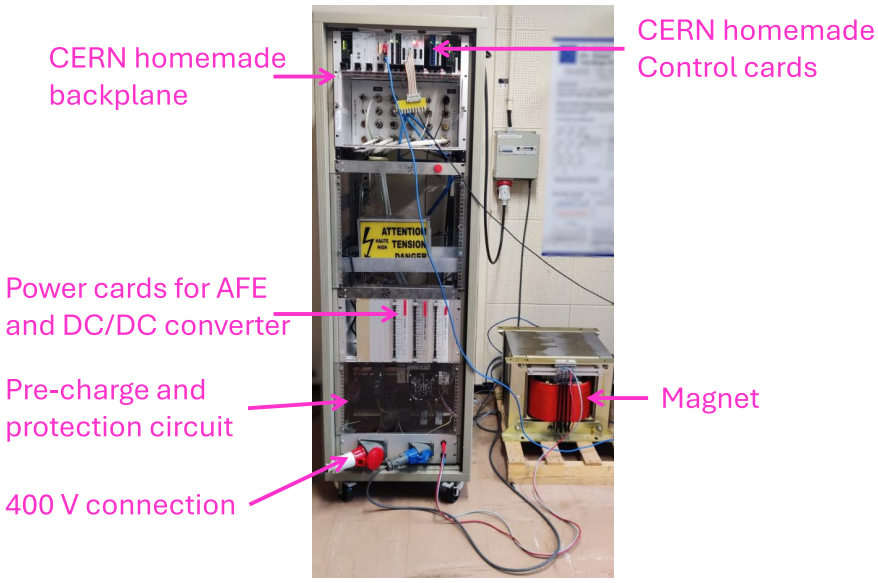


Figure 2.27: Experimental setup.

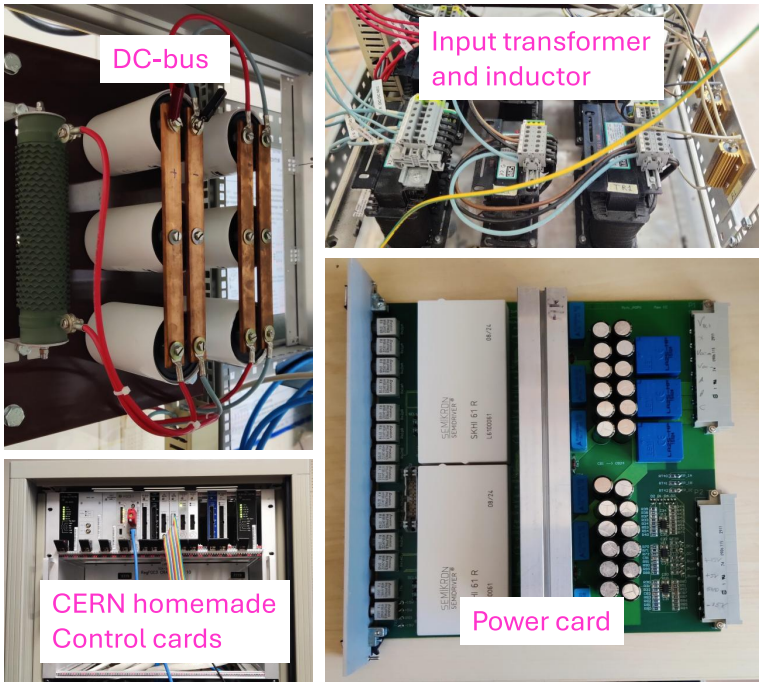


Figure 2.28: Detailed views of prototype converter.

The experimental setup is shown in Fig. 2.27. Key components include the grid-connected transformer, AFE inductance, DC-bus capacitors, power card containing the three legs of the NPC including three current sensors for the measurement of each phase current, CERNs homemade backplane, auxiliary power supply card, state machine card, DSP-based control card, digital and analog signal acquisition cards which are present inside the prototype converter, are shown in Fig. 2.28. The prototype converter is connected to a $100\ \mathrm{mH}$, $270\ \mathrm{m\Omega}$ magnet load.

The POPS-B converter is controlled using a $dq-$frame control technique for regulating both active and reactive power. Other control techniques, semi-DC-bus voltage balancing, common-mode voltage injection, and sinusoidal PWM modulation, are implemented in the DSP controller. Two different control strategies are experimentally validated: constant DC-bus voltage regulation and instantaneous energy balance based DC-bus voltage regulation. The constant DC-bus voltage control technique is used to validate harmonic spectra in the semi-DC-bus voltages and DC-bus voltage, while the instantaneous energy balance based DC-bus voltage control technique is employed to validate the AFE operation as a reactive power compensator.

For the experiments, a reduced load condition is considered, with a peak output current of $i_{\mathrm{out,pk}} = 30\ \mathrm{A}$. Although the prototype converter can supply currents up to $50\ \mathrm{A}$, the focus is on operating the AFE as a reactive power compensator under light load conditions while supplying the magnet. Accordingly, an output current profile with a peak of $30\ \mathrm{A}$ and a corresponding peak output voltage of $18.5\ \mathrm{V}$ is chosen for experimental validation. The chosen output current replicates the load profile of the POPS-B converter, including the duration of the load cycle. The peak power losses on the load coil with $30\ \mathrm{A}$ of load profile are $243\ \mathrm{W}$.

For validating the harmonic spectra of semi-DC-bus voltages, and DC-bus voltage, the $d-$axis

current reference is set to correspond to 250 W of active power, which is supplied to the grid power regulator along the actual $d-$axis current generated from the constant DC-bus voltage regulator.

The plots in Fig. 2.29(a) show the output current and voltage profile. The maximum output current reaches 30 A, while the peak output voltage during the transients is 26.4 V. At the maximum load current, the output voltage is 18.1 V. Fig. 2.29(b) presents the semi-DC-bus voltages, DC-bus voltage, and grid a-phase current. From Fig. 2.29(b), it is evident that the positive semi-DC-bus voltage ($+v_{\mathrm{dc}}/2$) and negative semi-DC-bus voltage ($-v_{\mathrm{dc}}/2$) remain balanced. To charge the load current to 30 A, the DC-bus voltage drops from 50 V to 42.86 V, while the grid phase$-a$ current (i_{a}) rises to 11.77 A to compensate for both converter and magnet resistive losses. With the maximum active power reference set to 250 W and no reactive power exchange with the grid, the measured maximum average active power is 252.77 W, as shown in Fig. 2.29(c). The operation of the unity power factor of the AFE is evident from Fig. 2.29(d), as it is clearly evident that the voltage and current of the grid are in phase with each other.

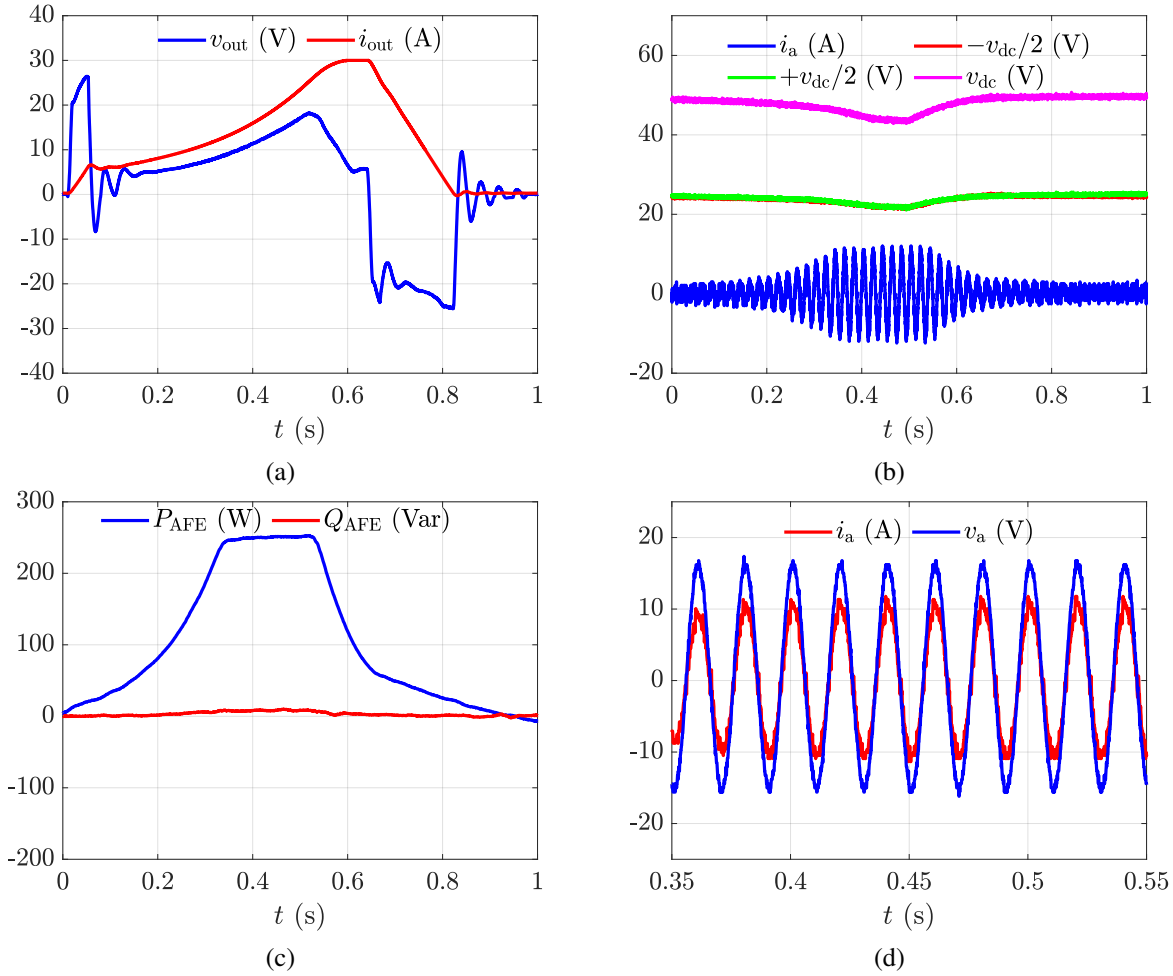


Figure 2.29: Experimental results under constant DC-bus voltage control, showing (a) output current, output voltage; (b) grid current, DC-bus voltage, semi-DC-bus voltages; (c) grid active, reactive power profiles and (d) grid voltage, grid current profiles for $P_{\mathrm{AFE}} = 250$ W with $Q_{\mathrm{AFE}} = 0$ Var.

The AFE operation as an inductive reactive power compensator is also verified. In this case, the constant DC-bus voltage controller is set with a limit of active power consumption almost equal to the load coil's resistive power losses, that is, 250 W, while the reference for the reactive power is set to 160 Var. ($Q = \sqrt{S^2 - P^2} = \sqrt{300^2 - 250^2} \approx 160$ Var). From Fig. 2.30(a), the maximum output current reaches 30.01 A, and the maximum output voltage during the transients is 26.4 V, while the voltage at maximum load current is 18.3 V. From Fig. 2.30(b), it is evident that even in the presence of inductive reactive power, the positive semi-DC-bus voltage ($+v_{\rm dc}/2$) and negative semi-DC-bus voltage ($-v_{\rm dc}/2$) remain balanced. To charge the load current to 30 A, the DC-bus voltage is discharged to 42.38 V from 50 V, whereas, the peak value of grid phase$-a$ current ($i_{\rm a}$) is 14.13 A to compensate for prototype converter and magnet losses and absorb 160 Var of inductive reactive power from the grid. The resultant maximum averaged active power is 244.7 W, and the average reactive power is 176.54 Var, which are evident from Fig. 2.30(c). Due to the exchange of

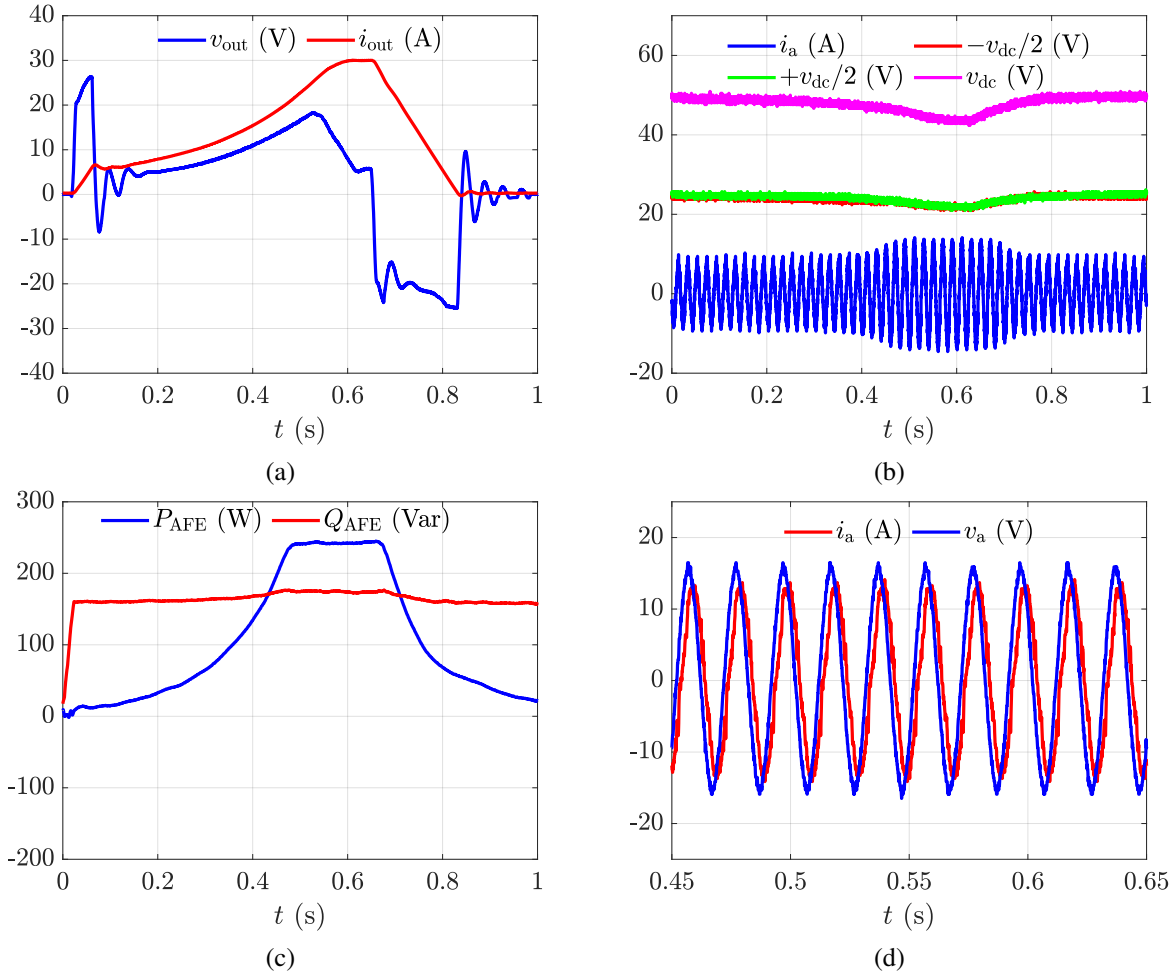


Figure 2.30: Experimental results under constant DC-bus voltage control, showing (a) output current, output voltage; (b) grid current, DC-bus voltage, semi-DC-bus voltages; (c) grid active, reactive power profiles and (d) grid voltage, grid current profiles for $P_{\rm AFE} = 250$ W with $Q_{\rm AFE} = 160$ Var.

164.7 Var inductive reactive power with the grid, the unity power factor operation of the AFE is no longer respected, as evident from Fig. 2.30(d).

The AFE operation as a capacitive reactive power compensator is similarly validated. The constant DC-bus voltage controller is set with a limit of active power consumption equal to 250 W, while the reference for the capacitive reactive power is set to -160 Var. From Fig. 2.31(a), it is observed that the maximum output current is 30 A, and the maximum output voltage during transients is 26.35 V, while the output voltage at the maximum load current is 18.2 V. From Fig. 2.31(b), it is evident that even in the presence of capacitive reactive power, the positive semi-DC-bus voltage ($+v_{\rm dc}/2$) and negative semi-DC-bus voltage ($-v_{\rm dc}/2$) remain balanced. To charge the load current to 30 A, the DC-bus is discharged to 42.38 V from 50 V, and the peak value of grid phase$-a$ current ($i_{\rm a}$) is 14.13 A to compensate for prototype converter losses, resistive losses in the magnet, and inject -160 Var of capacitive reactive power to the grid. The measured maximum averaged active power

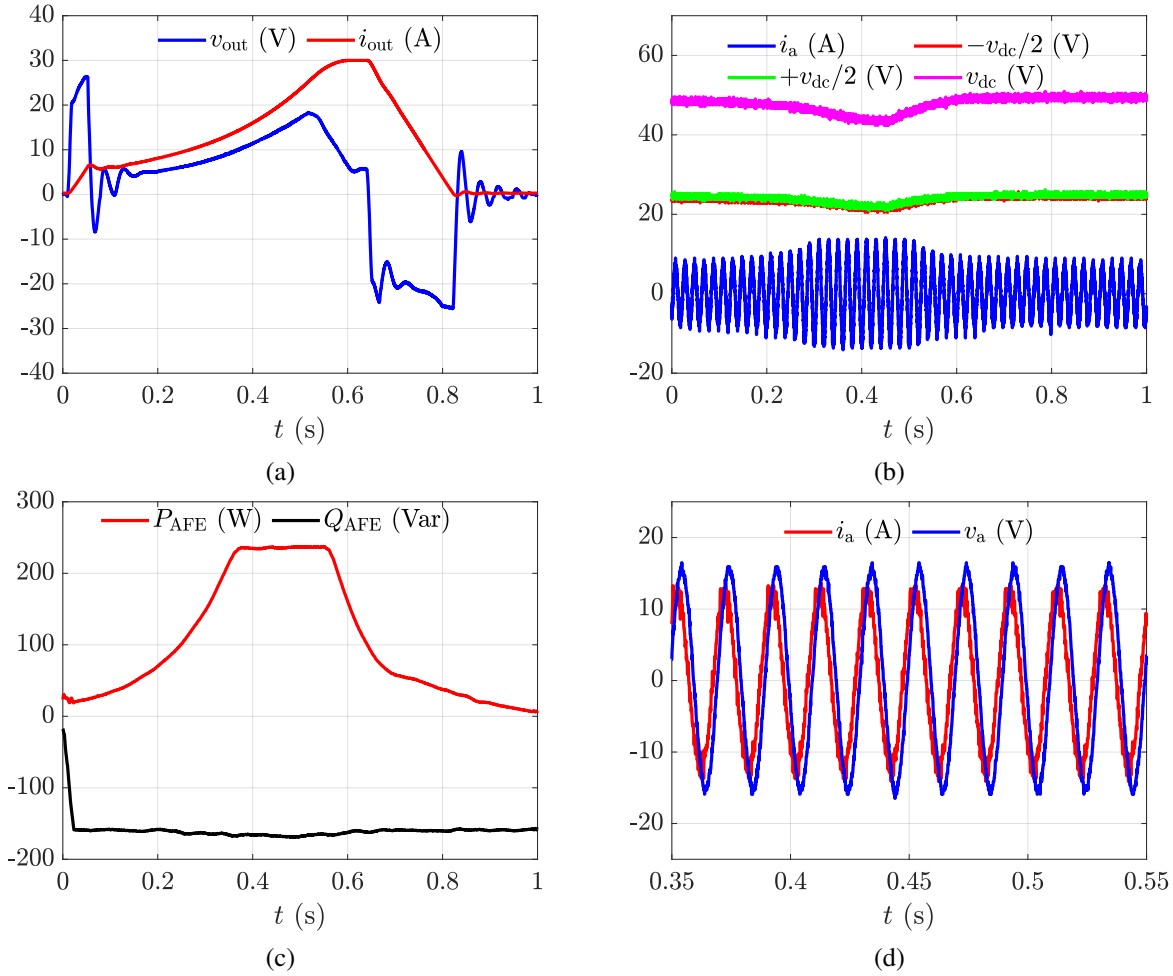


Figure 2.31: Experimental results under constant DC-bus voltage control, showing (a) output current, output voltage; (b) grid current, DC-bus voltage, semi-DC-bus voltages; (c) grid active, reactive power profiles and (d) grid voltage, grid current profiles for $P_{\rm AFE} = 250$ W with $Q_{\rm AFE} = -160$ Var.

is 237.1 W, and the average reactive power is -169 Var, as shown in Fig. 2.31(c). Similar to the inductive reactive power case, the exchange of -169 Var capacitive reactive power from the grid, the unity power factor operation of the AFE is no longer respected, as evident from Fig. 2.31(d).

From, Fig. 2.29, Fig. 2.30, and Fig. 2.31, it can be observed that the discharge of DC-bus voltage discharges to approximately 42.38 V to supply a 30 A load current regardless of the reactive power exchanged. This indicates that the discharge of the DC-bus capacitor bank is independent of the reactive power magnitude. However, the grid current increases during both positive and inductive reactive power exchange compared to the unity power factor case.

Due to the absence of a neutral point connection in the AFE power card, harmonic characterization of the semi-DC-bus voltages and DC-bus voltage was performed for $P_{\mathrm{AFE}} = 250$ W with $Q_{\mathrm{AFE}} = 0$ Var, $Q_{\mathrm{AFE}} = 160$ Var, and $Q_{\mathrm{AFE}} = -160$ Var, with the results shown in Fig. 2.32.

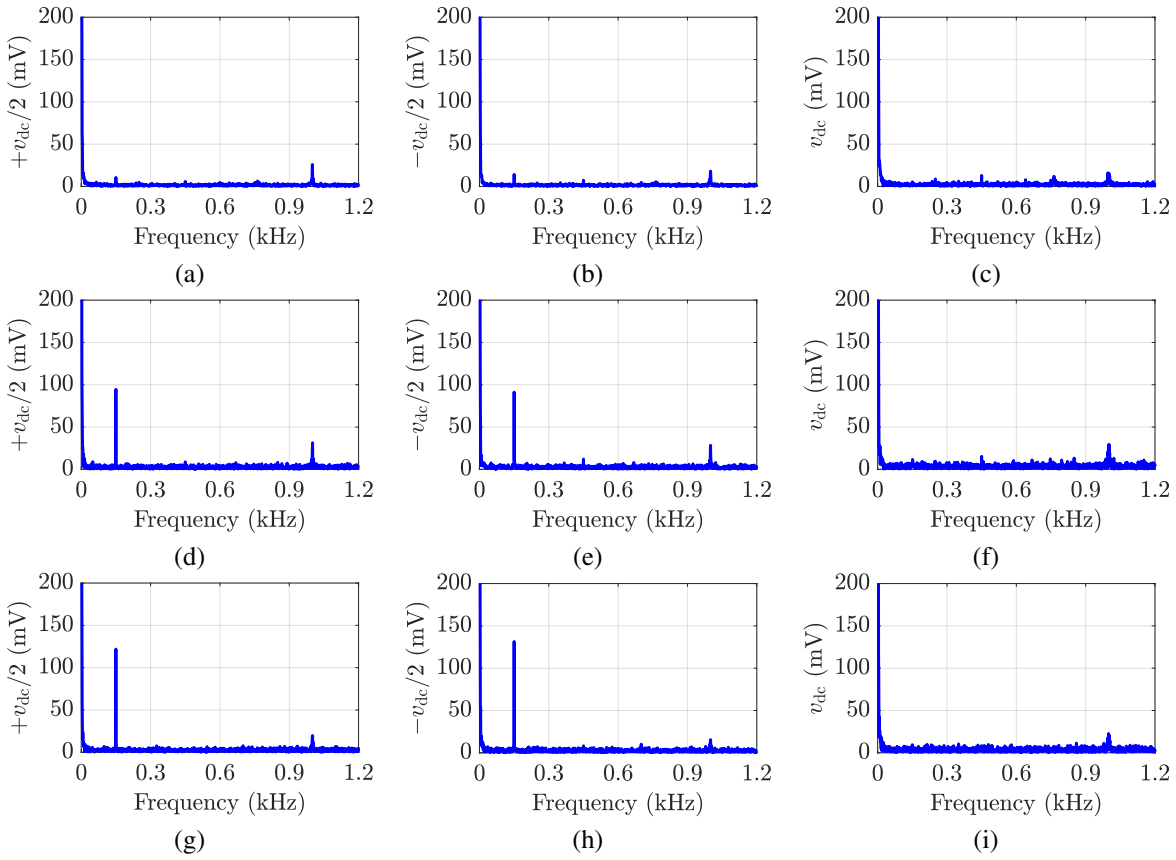


Figure 2.32: Experimental results for the positive semi-DC-bus voltage, negative semi-DC-bus voltage, DC-bus voltage harmonic spectra at $P_{\mathrm{AFE,max}} = 250$ W with $Q_{\mathrm{AFE}} = 0$ Var, 160 Var, and -160 Var, respectively.

From Fig. 2.32(a), Fig. 2.32(d), and Fig. 2.32(g) the 150 Hz component of the positive semi-DC-bus voltage at $P_{\mathrm{AFE,max}} = 250$ W is observed to be 10.5 mV, 94.5 mV, and 121.8 mV for $Q_{\mathrm{AFE}} = 0$ Var, 160 Var, and -160 Var, respectively. Similarly, from Fig. 2.32(b), Fig. 2.32(e), and Fig. 2.32(h), the 150 Hz component of the negative semi-DC-bus voltage is 14.2 mV, 91.2 mV, and 131.4 mV for the same reactive power values. Although a 450 Hz component is present in both

semi-DC-bus voltages for each reactive power case, its magnitude is negligible compared to the DC component of 25 V. As also observed in Section 2.2.2, the 150 Hz component of both positive semi-DC-bus voltage and negative semi-DC-bus voltage increases with the magnitude of the capacitive reactive power, being largest for $Q_{\mathrm{AFE}} = -160$ Var, followed by $Q_{\mathrm{AFE}} = 160$ Var, and smallest for $Q_{\mathrm{AFE}} = 0$ Var. Moreover, for each reactive power case, the 150 Hz components of the positive semi-DC-bus voltage and negative semi-DC-bus voltage are approximately equal, while the 150 Hz component of the total DC-bus voltage remains close to zero.

To experimentally validate the analysis performed in Section 2.3 regarding the AFE operating as a reactive power compensator, an instantaneous energy balance based DC-bus voltage control technique is implemented. According to the analysis in Section 2.3, the maximum average active power and capacitive reactive power that can be exchanged with the grid are 100 W and −160 Var, respectively.

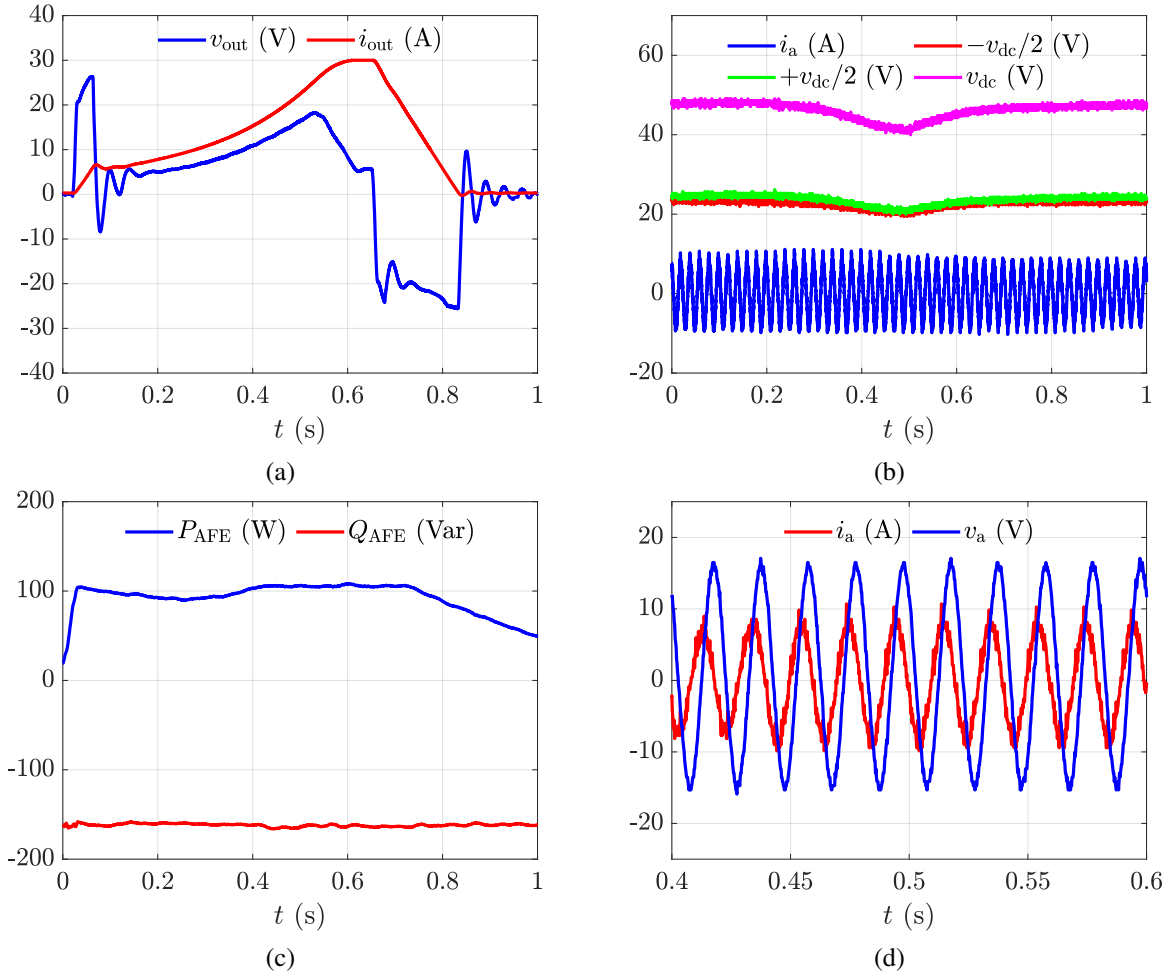


Figure 2.33: Experimental results under instantaneous energy balance–based DC-bus voltage control, showing: (a) output current, output voltage, (b) DC-bus voltage, semi-DC-bus-voltages, grid current, (c) grid active, reactive power, (d) grid voltage and current profiles for $P_{\mathrm{AFE}} = 100$ W and $Q_{\mathrm{AFE}} = -160$ Var.

Accordingly, the experiments are conducted by applying the DC-bus voltage control technique illustrated in Fig. 2.14. To regulate the capacitive reactive power of -160 Var, the corresponding $q-$axis current is used as the reference input to the grid power regulation control, as shown in Fig. 2.5.

From Fig. 2.33(a), it can be seen that the maximum output current is 30 A, and the maximum output voltage during transients is 26.4 V, while the output voltage at the maximum load current is 18.3 V. Although the peak active power requirement is 250 W, the prototype consumes only 100 W, yet it is still able to charge the load current to 30 A. This is achieved by discharging the DC-bus to a lower voltage of approximately 40 V, as shown in Fig. 2.33(b), compared to 42.38 V in the $P_{\mathrm{AFE}} = 250$ W case. Analytically, the active power drawn from the grid is limited to 100 W, considering that the DC-bus voltage should not drop below 45 V. Experimentally, the DC-bus voltage discharges slightly more, down to 40 V, due to resistive losses in the prototype converter. The positive and negative semi-DC-bus voltages ($+v_{\mathrm{dc}}/2$ and $-v_{\mathrm{dc}}/2$) remain balanced, as shown in Fig. 2.33(b). The peak value of grid phase$-a$ current (i_{a}) is 11.13 A with a peak average active power of 108.4 W and a peak average reactive power of -166.3 Var, as depicted in Fig. 2.33(c). Due to the combined exchange of -166.3 Var capacitive reactive power and 100 W of active power, the AFE no longer operates at unity power factor, which is evident from Fig. 2.33(d).

Overall, the experimental results effectively validate the AFEs capability to regulate active and reactive power under light load conditions, confirming the feasibility of the proposed instantaneous energy balance based DC-bus voltage control strategy.

2.5 Summary

This chapter presents an in-depth analysis of the NPC architecture-based AFE of the POPS-B converter, currently operating at CERNs BOOSTER ring. The main objective of the studies is to operate the AFE stage of the PC as a reactive power compensator while supplying the load under light load conditions. Operating the AFE as a reactive power compensator requires regulating the exchange of active and reactive power between the grid and the AFE stage of the PC; hence, two conventional control techniques, the $dq-$frame and $\alpha\beta-$frame, are investigated numerically using a MATLAB/Simulink simulation environment. Analytically, both approaches yield nearly comparable results in terms of DC-bus voltage, active power, reactive power, neutral point current, its harmonics, and semi-DC-bus voltages. However, the $\alpha\beta-$frame offers inherent decoupling of active and reactive power regulation, which becomes evident when comparing the corresponding active and reactive power profiles.

The neutral point current, which exists in NPC architecture, is investigated analytically and validated numerically under various reactive power scenarios, including zero, inductive, and capacitive cases, with both control techniques producing similar outcomes. The neutral point current has its best case when the NPC acts at unity power factor, and the worst when it acts at zero power factor, since the neutral point current is a function of power factor angle and the modulation index of the AFE. The neutral point current contains the dominant three-order harmonics and varies with the reactive power; hence, it is analyzed numerically, as the DC-bus must accommodate this neutral point current. The harmonics present in the neutral point current also exist in the semi-DC-bus voltages, which are analyzed numerically and experimentally validated under various reactive power cases. The magnitude of the third-order harmonic that exists in the semi-DC-bus voltages is insignificant compared to their DC component.

Finally, an instantaneous energy balance based DC-bus voltage control technique is proposed for the POPS-B converter. This technique is also applicable to applications where the AFE stage of the PC is not rated equal to the peak power losses in the load coil. Analytical evaluations determine the minimum active power that can be drawn from the grid while injecting maximum capacitive reactive power, without reducing the DC-bus voltage below a specified threshold or operating the AFE in over-modulation. The proposed control strategy is experimentally validated on a CERN prototype, successfully demonstrating AFE operation as a reactive power compensator under light load conditions.

Chapter 3

Interleaved DC/DC Back-End

This chapter presents a comprehensive analysis of two possible architectures for the back-end converter with a generic number of interleaved HBs: the CDC configuration and the SDC configuration. A comparison of RMS currents in CDC and SDC configurations is performed as a function of the number of HBs to analyze the effect of circulating currents under both ideal and non-ideal conditions. Additionally, the HB currents, RMS currents, the RMS of the non-zero frequency components, and the associated losses are compared under non-ideal conditions. Normalization of the RMS current in CDC configuration is proposed to decouple the effect of the circulating current from the output current. Analytical developments for both configurations under ideal conditions are numerically validated, considering a wide range of parallel HBs and gain ratios. The RMS of the non-zero frequency component of the current in CDC configuration, which differs from that in SDC configuration due to the presence of circulating current, is validated experimentally over specific sets of parallel HBs and gain ratios. Highlighting the advantages and disadvantages of CDC and SDC configurations, an algorithm is proposed to automatically select the most appropriate topology for the PC. The functionality of the proposed algorithm is demonstrated through illustrative design cases and validated numerically under varying system parameters and algorithm inputs.

This chapter focuses on the analysis and design of interleaved DC/DC converter topologies used in the back-end stage of PCs. The interleaving technique, commonly adopted to reduce output current ripple and improve thermal performance, introduces specific design challenges, particularly in relation to the DC-bus architecture and its influence on overall system behavior. Two widely used configurations, the CDC and SDC configurations, are introduced and analyzed under ideal and non-ideal conditions of the interleaving inductors. Particular emphasis is placed on the impact of circulating currents, which are inherent to the CDC configuration and contribute to increased component stress and power losses.

3.1 Common DC and Split DC Topologies

This section presents and compares two of the possible architectures with interleaved HBs: the CDC configuration and the SDC configuration. To simplify the representation of the back-end converter

for analytical purposes, all front-end components, such as the line frequency transformer, protection devices, rectifier unit, and input filter components, along with the DC-bus, are represented as an ideal constant DC voltage source, denoted as V_{dc}. The two configurations under investigation, namely the CDC and SDC configurations, are illustrated in Fig. 3.1(a), and Fig. 3.1(b) respectively.

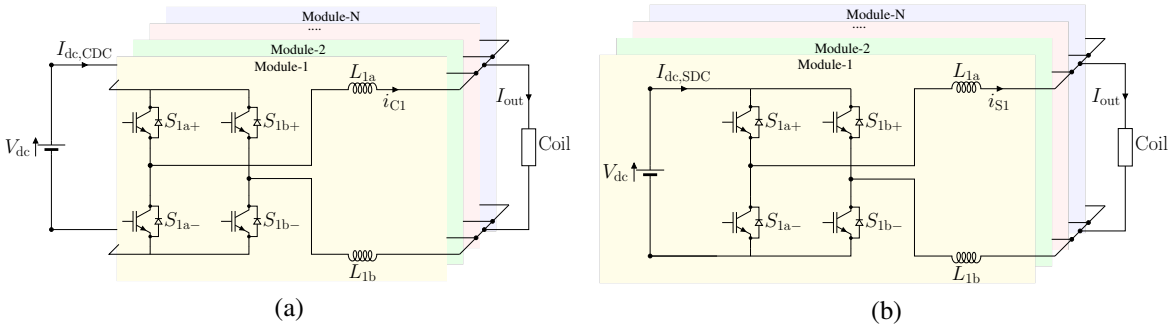


Figure 3.1: Typical topologies for N-module interleaved HBs under the ideal case. (a) CDC. (b) SDC.

For a consistent comparison between the CDC and SDC configurations, the value of the inductances L_{na}, L_{nb} connected to each HB is assumed to be the same and equal to a generic inductance L (i.e., $L_{na} = L_{nb} = L$). The legs are distinguished using the index n, whose value ranges from 1 to N, where N represents the number of interleaved HBs. In nuclear fusion and particle accelerator applications, the load is a coil characterized by an inductance L_{c} and a series resistance R_{c}.

From the schematic in Fig. 3.1(b), it is evident that the implementation of the SDC configuration requires a separate set of front-end components for each HBmodule. Consequently, the number of such components scales linearly with N, leading to an increase in overall PCs footprint, complexity, and cost. In contrast, the CDC configuration employs a single front-end stage shared among all HB modules, offering a more compact and cost-effective solution. However, CDC configuration introduces a significant drawback: the absence of galvanic isolation between the HBs allows the formation of closed-loop paths between the N parallel connected HBs and the common DC-bus. The presence of these closed paths, along with the phase-shift difference in the carriers, can give rise to undesired currents, which circulate only among the HB modules without affecting the output current. Such currents are typically referred to as circulating currents.

These circulating currents do not contribute to the output current but instead flow among the HBs. Their presence leads to increased current stress on the semiconductor and inductors (L_{na} and L_{nb}), resulting in higher conduction losses, elevated thermal stress, and ultimately a reduction in the lifespan and reliability of the PCs [89]. On the other hand, the SDC inherently avoids the circulating currents issue due to the galvanic isolation provided by the individual power transformers on each DC-bus, effectively eliminating the paths through which circulating currents could flow, even when phase-shifted carrier signals are employed.

Similar to a multiphase interleaved DC/DC buck converter analyzed in [90], the peak-to-peak current ripple of an interleaved HB converter can be expressed as:

$$\Delta i_{\mathrm{rip}} = \frac{V_{\mathrm{dc}}}{4 L f_{\mathrm{s,IHB}}} \delta \left(1 - \delta\right) \ , \tag{3.1}$$

where $f_{\mathrm{s,IHB}}$ represents the switching frequency of the interleaved HBconverter, and δ denotes the

HB gain ratio, which varies between 0 to 1. In this context, the gain ratio δ is defined as the difference in the duty cycle of leg a and leg b for any n-th HB, i.e.:

$$\delta = \delta_{\mathrm{na}} - \delta_{\mathrm{nb}} \, , \tag{3.2}$$

where δ_{na} equals to $0.5 + \delta/2$ and δ_{nb} equals to $0.5 - \delta/2$.

Furthermore, the relation between the peak-to-peak output current ripple (Δi_{out}) and the gain ratio δ, for a given number of interleaved HBs (N) under steady-state operating conditions, is given by:

$$\Delta i_{\mathrm{out}} = \frac{V_{\mathrm{dc}}}{4 L f_{\mathrm{s,IHB}}} \left[\delta - \frac{\mathrm{ceil}\,(N\delta) - 1}{N} \right] \left\{ 1 - N \left[\delta - \frac{\mathrm{ceil}\,(N\delta) - 1}{N} \right] \right\} \, , \tag{3.3}$$

where the function $\mathrm{ceil}\,(N\delta)$ is the closest highest integer of $N\delta$.

Equation (3.3) is applicable to both the CDC and SDC configurations since the circulating currents inherent to the CDC configuration do not influence the load current. On the other hand, (3.1) is valid only in the case of SDC since the derived equation does not consider any contributions from circulating current.

To accurately analyze the CDC configuration, the effects of circulating current must be explicitly incorporated. This is achieved by formulating the RMS current through the inductors and comparing it to that in the SDC configuration case. The analysis relies on the orthogonality between the DC component of the current, which arises from the load and is uniformly distributed across the N HBs (i.e., I_{out}/N), and the high-frequency ripple component (I_{rip}). Notably, the non-zero frequency component differs between the two topologies due to the presence of circulating currents in the CDC configuration.

In the subsequent subsections, a comprehensive analytical framework is presented to evaluate the RMS current in the HB legs for both CDC and SDC configurations, under the assumption of N interleaved HBs.

3.1.1 Analysis of RMS Currents in SDC Configuration

This subsection derives an analytical expression for the RMS current in the inductors of the SDC configuration, considering that the coil is decoupled from the interleaved HB stage of the PC.

Assuming orthogonality between the DC component and the non-zero frequency, the RMS value of the inductor current in the leg a of the n-th HB(I_{Sn}) can be expressed as:

$$I_{\mathrm{Sn}} = \sqrt{\left(\frac{I_{\mathrm{out}}}{N} \right)^2 + \left(I_{\mathrm{rip}}\big|_{\mathrm{SDC}} \right)^2} \, , \tag{3.4}$$

where I_{out} denotes the average output current delivered to the load, and $I_{\mathrm{rip}}\big|_{\mathrm{SDC}}$ is the RMS of the current ripple in the inductor of the SDC configuration.

Based on the earlier result for the peak-to-peak current ripple in (3.1), the RMS value of the triangular current ripple waveform in each inductor of the SDC configuration is given by:

$$I_{\mathrm{rip}}\big|_{\mathrm{SDC}} = \frac{\Delta i_{\mathrm{rip}}}{2\sqrt{3}} = \frac{V_{\mathrm{dc}}}{8\sqrt{3} L f_{\mathrm{s,IHB}}} \delta \left(1 - \delta \right) \, . \tag{3.5}$$

Substituting (3.5) into (3.4) results in:

$$I_{\mathrm{Sn}} = \sqrt{\left(\frac{I_{\mathrm{out}}}{N}\right)^2 + \left(\frac{V_{\mathrm{dc}}}{8\sqrt{3}Lf_{\mathrm{s,IHB}}}\delta\left(1-\delta\right)\right)^2}\,, \tag{3.6}$$

which represents the RMS current in the n-th HB module of the SDC configuration. It is important to note that the RMS current derived in (3.6) does not account for circulating current effects, as such currents are inherently absent in the SDC configuration due to the galvanic isolation provided between HBs. Consequently, this formulation does not apply to the CDC configuration, where circulating currents contribute significantly to the RMS current in HB.

3.1.2 Analysis of RMS Currents in CDC Configuration

As circulating current exist in the CDC configuration, the analytical approach used in Section 3.1.1 for the SDC configuration cannot be directly used here. Therefore, to accurately determine the RMS current in HB of the CDC configuration, the influence of the circulating currents must be accounted for. To facilitate this, an equivalent electrical circuit model, depicted in Fig. 3.2 is considered.

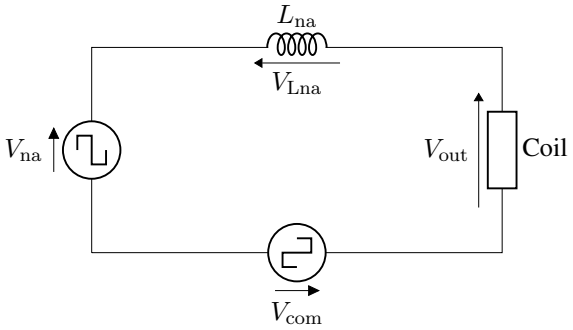


Figure 3.2: Equivalent electrical schematic.

Fig. 3.2 illustrates the electrical equivalence for the n-th HB, connected to the output coil, as well as its interaction with the remaining $N-1$ interleaved HBs. In Fig. 3.2, V_{na} represents the average phase voltage of leg a in the n-th HB, V_{Lna} represents the mean voltage of the inductor present at leg a of the n-th HB, and V_{com} refers to the common-mode voltage between leg a of the n-th HB and the output negative terminal.

To derive relevant equations, Kirchhoff's voltage law is applied to the equivalent circuit represented in Fig. 3.2, obtaining:

$$V_{\mathrm{na}} = V_{\mathrm{Lna}} + V_{\mathrm{out}} + V_{\mathrm{com}}\,. \tag{3.7}$$

The mean voltage of leg a in the n-th HB can be expressed in terms of DC-bus voltage and its duty cycle:

$$V_{\mathrm{na}} = \delta_{\mathrm{na}} V_{\mathrm{dc}}\,, \tag{3.8}$$

Similarly, the output voltage V_{out} in terms of the DC-bus voltage V_{dc} can be defined as:

$$V_{\mathrm{out}} = \delta V_{\mathrm{dc}}\,. \tag{3.9}$$

In a switching time period, the average component of the voltage in the leg a of the n-th HB is zero, hence substituting the expressions of V_{na} and V_{out} in (3.7) yields:

$$V_{\mathrm{com}} = \frac{V_{\mathrm{dc}}}{2}\left(1-\delta\right) \ . \tag{3.10}$$

The RMS of the current ripple in the inductor of the CDC configuration ($I_{\mathrm{rip}}\big|_{\mathrm{CDC}}$) is expressed as:

$$I_{\mathrm{rip}}\big|_{\mathrm{CDC}} = \frac{t_{\mathrm{on}}}{2\sqrt{3}L} V_{\mathrm{Lna}}|_{t_{\mathrm{on}}} \ . \tag{3.11}$$

where $V_{\mathrm{Lna}}|_{t_{\mathrm{on}}}$is the voltage across the inductor in the leg a of the n-th HB during the conduction of switch $S_{\mathrm{na+}}$ in Fig. 3.1(a). The difference in this voltage with respect to the SDC configuration is precisely the source of the circulating current.

Thereby, substituting (3.8), (3.9) and, (3.10) in (3.7) at t_{on} it results in:

$$V_{\mathrm{Lna}}|_{t_{\mathrm{on}}} = \frac{V_{\mathrm{dc}}}{2}\left(1-\delta\right) \ . \tag{3.12}$$

The conduction time t_{on} of switch $S_{\mathrm{na+}}$ is related to its duty cycle:

$$t_{\mathrm{on}} = \frac{\delta_{\mathrm{na}}}{f_{\mathrm{s,IHB}}} \ . \tag{3.13}$$

Substituting (3.12) and (3.13) into (3.11), the final expression for the RMS of the current ripple in the inductor of the CDC configuration results in:

$$I_{\mathrm{rip}}\big|_{\mathrm{CDC}} = \frac{V_{\mathrm{dc}}}{8\sqrt{3}Lf_{\mathrm{s,IHB}}}\left(1-\delta^2\right) \ . \tag{3.14}$$

Finally, the total RMS current in the inductor at leg a in the n-th HB in CDC configuration (I_{Cn}), accounts for both the average output current and the ripple component can be expressed as:

$$I_{\mathrm{Cn}} = \sqrt{\left(\frac{I_{\mathrm{out}}}{N}\right)^2 + \left(I_{\mathrm{rip}}\big|_{\mathrm{CDC}}\right)^2} \ , \tag{3.15}$$

leading to:

$$I_{\mathrm{Cn}} = \sqrt{\left(\frac{I_{\mathrm{out}}}{N}\right)^2 + \left[\frac{V_{\mathrm{dc}}}{8\sqrt{3}Lf_{\mathrm{s,IHB}}}\left(1-\delta^2\right)\right]^2} \ , \tag{3.16}$$

which represents the RMS current in the n-th HB module of the CDC configuration, explicitly accounting for the influence of circulating currents through the modified ripple term.

3.1.3 Comparison of RMS Currents in CDC and SDC Configurations

This subsection aims to highlight and analyze the key differences between the RMS currents in the CDC and SDC configurations, based on the expressions derived previously, and also to introduce a normalization of RMS currents in CDC. By comparing the RMS current equations derived in (3.6) and (3.16), it is evident that while the DC component, directly related to the output load current

divided by the number of HBs (i.e., I_{out}/N), remains identical in both configurations. However, the non-zero frequency component, provided by the harmonics, differs significantly.

The non-zero frequency current components, represented by $I_{\mathrm{rip}}\big|_{\mathrm{CDC}}$ and $I_{\mathrm{rip}}\big|_{\mathrm{SDC}}$, are not equal ($I_{\mathrm{rip}}\big|_{\mathrm{CDC}} \neq I_{\mathrm{rip}}\big|_{\mathrm{SDC}}$), indicating that the circulating currents inherent in the CDC configuration introduce additional ripple current that does not appear in the SDC configuration.

In order to partially decouple and understand the impact of these ripple currents on the RMS current in the CDC configuration, a normalization approach is employed. Specifically, the RMS current in the n-th HB of the CDC configuration is normalized by the corresponding DC current contribution I_{out}/N, yielding:

$$I_{\mathrm{C}} = \frac{I_{\mathrm{Cn}}}{\frac{I_{\mathrm{out}}}{N}} = N\frac{I_{\mathrm{Cn}}}{I_{\mathrm{out}}}\,. \tag{3.17}$$

This normalized RMS current I_{rip} provides valuable insight into how circulating currents influence the HB current stress as the number of interleaved HBs increases.

The significance of this result lies in the observation that, while the output current I_{out} remains fixed, increasing the number of parallel HBs N reduces the output current handled by each HB. However, the ripple current $I_{\mathrm{rip}}\big|_{\mathrm{CDC}}$, which includes circulating current components in CDC configuration, remains effectively constant and independent of N.

Consequently, as N increases, larger to meet higher output current demands while sharing a single DC-bus, the relative contribution of circulating current to the overall RMS current in each HB becomes more pronounced. This phenomenon can lead to increased conduction losses and higher thermal stress in the CDC configuration in comparison to the SDC configuration, which should be carefully considered during PCs topology selection and design.

In practical terms, the normalized RMS current expression in (3.17) serves as a critical metric to evaluate the trade-offs involved in choosing between CDC and SDC configurations, especially when increasing the number of parallel HBs to achieve desired output current levels. The choice of topology selection based on the effect of circulating current and several other factors are explained in detail in Section 3.3.

3.1.4 Numerical Results

To validate the analytical expressions and theoretical insights developed in the previous subsections, detailed numerical simulations were conducted using the PLECS environment (Plexim GmbH). The

Table 3.1: Main system parameters used for the simulations.

Parameter	**Symbol**	**Value**	**Unit**
DC-bus voltage	V_{dc}	1	kV
Output current	I_{out}	10	kA
Inductors	$L_{\mathrm{na}} = L_{\mathrm{nb}} = L$	25	μH
Coil resistance	R_{c}	0.1	Ω
Switching frequency	$f_{\mathrm{s,IHB}}$	2	kHz
Number of HBs	N	15	-

two configurations under study, CDC and SDC, depicted in Fig. 3.1(a) and Fig. 3.1(b), respectively,

were modeled and simulated under various operating conditions. For the purposes of numerical validation, three distinct gain ratios $\delta = 0.3, 0.6$, and 0.9 were chosen to reflect different operating points. The main system parameters employed in the simulations are summarized in Table 3.1.

Fig. 3.3 compares the current waveforms of the HBs for both CDC and SDC configurations when $N = 15$ HBs. Specifically, Fig. 3.3(a), Fig. 3.3(c), and Fig. 3.3(e) represent the HB currents over two switching cycles in the CDC configuration for gain ratios $\delta = 0.3, 0.6$, and 0.9, respectively. Similarly, Fig. 3.3(b), Fig. 3.3(d), and Fig. 3.3(f) present the HB currents in the SDC configuration for the same gain ratios.

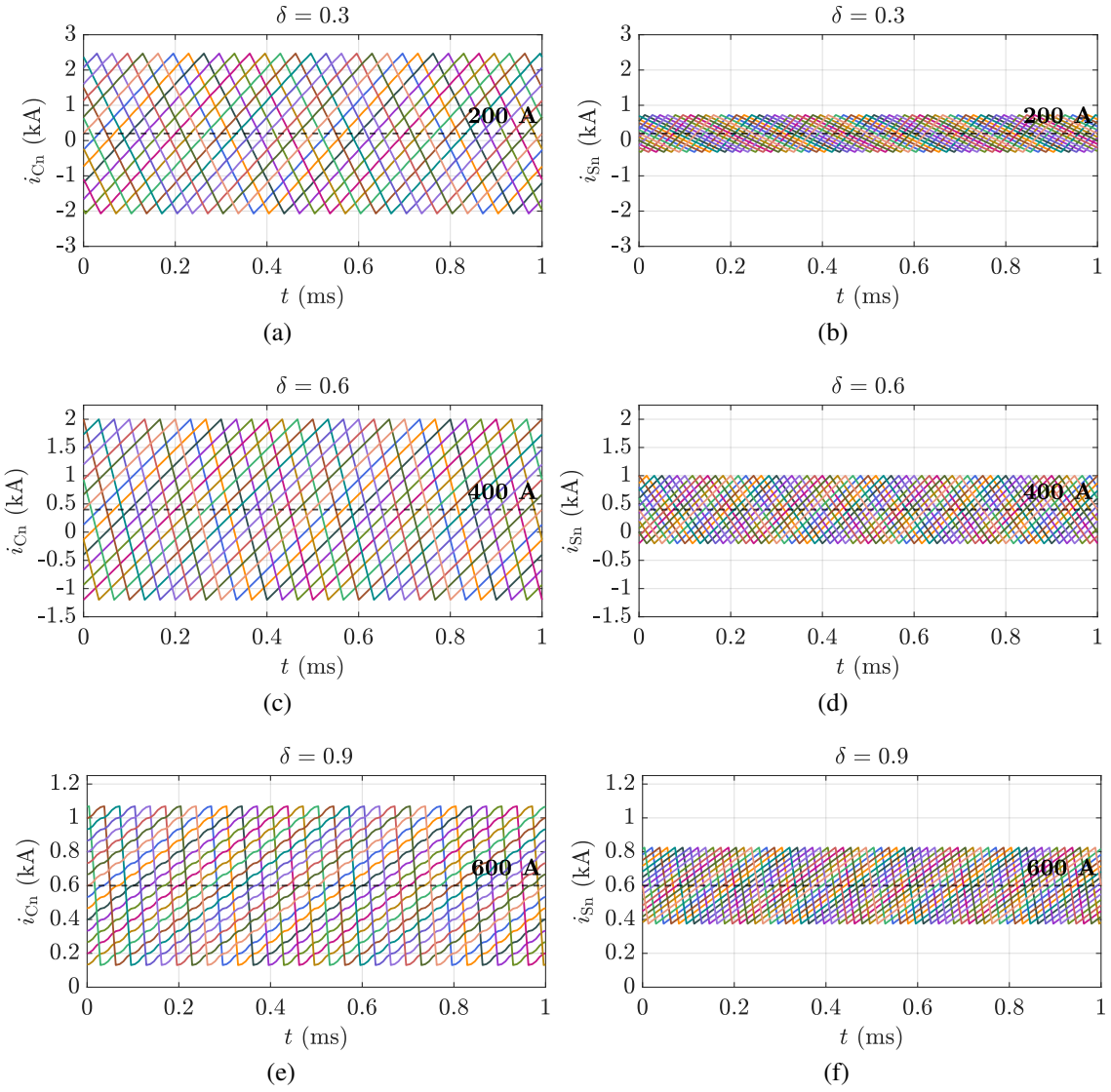


Figure 3.3: Interleaved HB currents with $N = 15$ in case of:(a) CDC at δ = 0.3, (b) SDC at δ = 0.3, (c) CDC at δ = 0.6, (d) SDC at δ = 0.6, (e) CDC at δ = 0.9 and, (f) SDC at δ = 0.9.

Consistent with the analysis presented in Section 3.1.3, the simulations confirm that at a fixed number of HBs, the DC component of the current remains identical between CDC and SDC configurations, whereas the current ripple differs substantially. The CDC configuration exhibits significantly higher ripple currents due to the presence of circulating currents across all validated gain ratios.

For example, comparing Fig. 3.3(a) and Fig. 3.3(b) for $\delta = 0.3$, both topologies demonstrate an identical mean current of 200.0 A per HB. However, the peak-to-peak current ripple in the SDC configuration is 1038 A, whereas in the CDC configuration it increases to 4520 A, a more than fourfold increase attributable to circulating current effects. Similarly, at $\delta = 0.6$, from Fig. 3.3(c) and Fig. 3.3(d), the mean value of the current in both CDC and SDC configuration is 400.0 A, but the peak-to-peak current ripple in SDC configuration is 1188 A, while in CDC configuration, it is 3177 A. Furthermore, in the case of $\delta = 0.9$, from Fig. 3.3(e) and Fig. 3.3(f), the mean value of the current in both the CDC and SDC configurations is 600.0 A, but the peak-to-peak current ripple in SDC configuration is 449.9 A, while in CDC configuration, it is 938.5 A. Notably, the peak-to-peak current ripples in the SDC configuration fairly agree with the analytical equation (3.1).

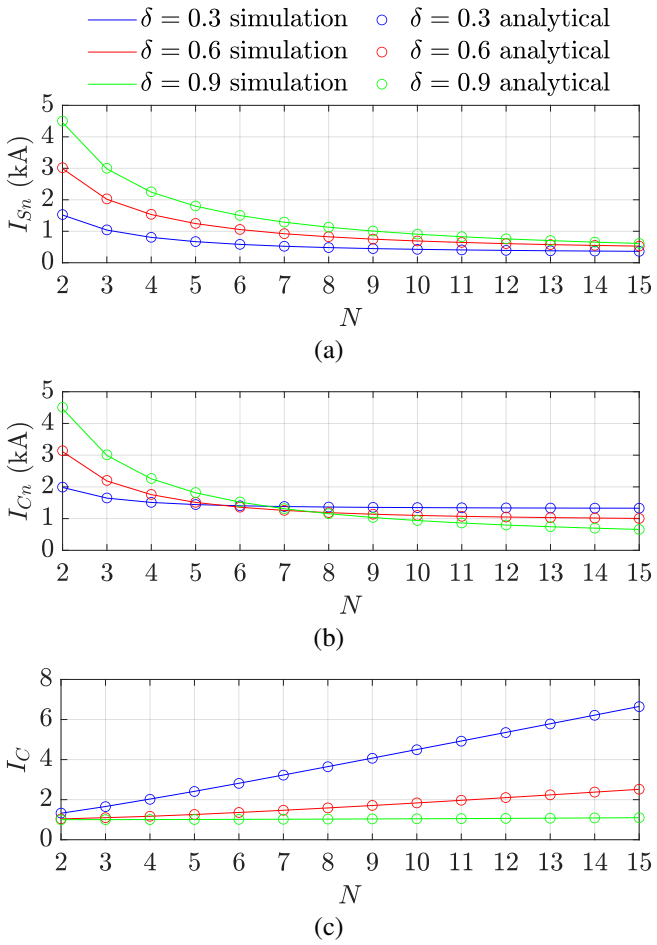


Figure 3.4: Numerical validation of RMS current in interleaved HBs at $\delta = 0.3, 0.6$, and 0.9: (a) in case of SDC; (b) in case of CDC; (c) normalization in case of CDC.

To further explore the influence of the number of HBs N on RMS current values, Fig. 3.4 presents the numerical results.

In particular, Fig. 3.4(a) presents the variation of RMS currents in SDC configuration by varying N from 2 to 15 for δ = 0.3, 0.6, and 0.9. Similarly, Fig. 3.4(b) presents the variation of RMS currents in CDC configuration for the same range of N and the same set of δ values. Comparing these two plots, for instance, at $N = 7$ and $\delta = 0.3$, the RMS current in SDC configuration is 0.5 kA, while in CDC, it is 1.4 kA. Similarly, at $N = 15$ and $\delta = 0.3$, the RMS current of HB in SDC configuration is 0.3 kA, whereas in CDC configuration it is 1.3 kA. These results suggest that the decay of RMS current in the CDC configuration does not follow a parabolic trend $(1/N)$. This is due to the fact that beyond a certain value of N (about $N = 6$), the circulating current predominates over the output current contribution. As foreseeable, lower values of gain ratio δ ensure lower RMS currents in the case of SDC configuration (see Fig. 3.4(a)) regardless of the number of modules N. Higher values of gain ratio δ lead to higher output currents I_{out} and therefore higher RMS currents. This behavior holds for low values of N also in the case of CDC configuration (see Fig. 3.4(b)). However, once N gets higher than 6, lower values of gain ratio δ lead to higher values of RMS currents. Such a trend inversion is attributable to the effect of the circulating currents. Current RMS values obtained numerically are in agreement with the analytical results.

Traces displayed in Fig. 3.4(c) correspond to the normalization of RMS current (3.17) in the case of CDC configuration as N varies from 2 to 15 for δ = 0.3, 0.6 and 0.9. It is immediately clear that higher values of N are more affected by the circulating current. In particular, lower values of gain ratio δ cause higher values of circulating currents throughout the whole N diapason. Such a statement was not directly apparent from the non-normalized RMS of Fig. 3.4(b).

Importantly, the output current I_{out} in both CDC and SDC configurations remains unaffected by circulating current, as confirmed by Fig. 3.5 across all gain ratios. This validates the theoretical premise that circulating currents primarily influence HBs rather than the load current.

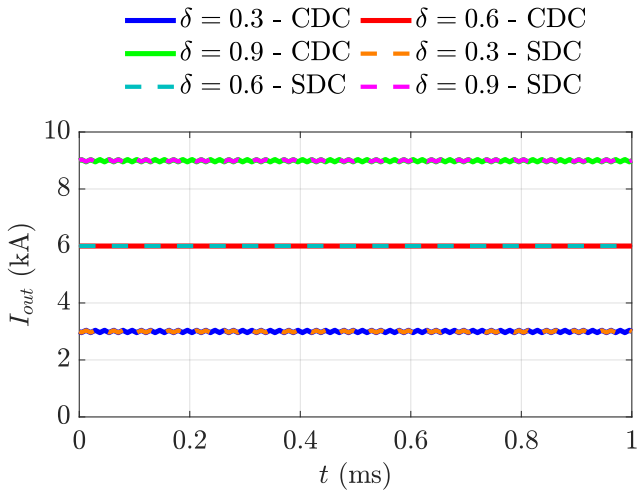
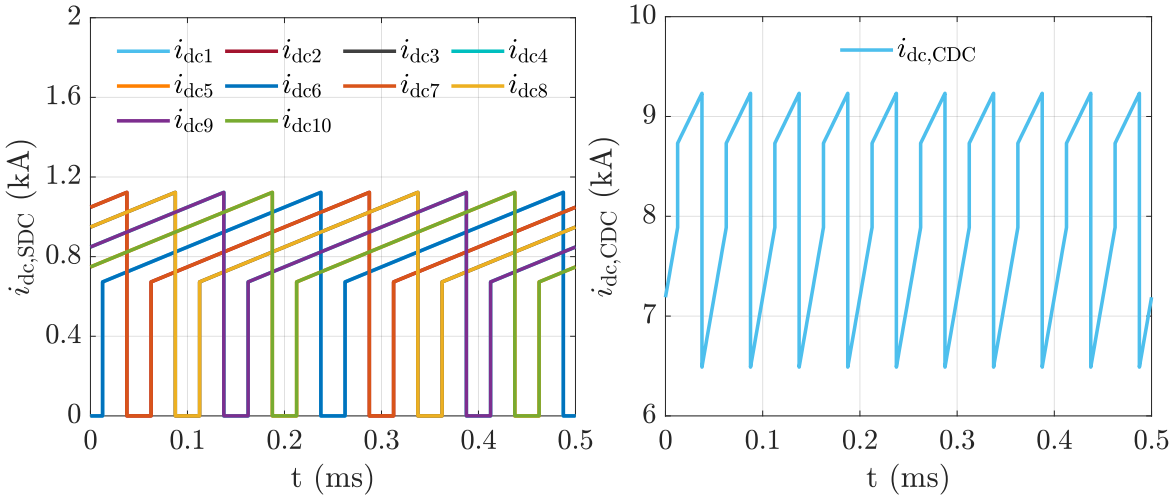


Figure 3.5: Numerical validation of output current in case of SDC and CDC configurations at δ = 0.3, 0.6, and 0.9.

To analyze the effect of circulating currents on the DC-bus in both the CDC and SDC configurations, simulations were performed with $N = 10$ HBs, $V_{\text{dc}} = 1$ kV, $I_{\text{out}} = 10$ kA, and $\delta = 0.9$. The results of the DC-bus currents in SDC and CDC configurations are shown, respectively, in Fig. 3.6(a) and Fig. 3.6(b).



(a) (b)

Figure 3.6: DC-bus current profiles with $N = 10$ HBs at $\delta = 0.9$: (a) SDC; (b) CDC.

The plots in Fig. 3.6(a) and Fig. 3.6(b) help to understand the impact of the circulating current on the sizing requirements of the DC-bus capacitors. The RMS and peak current through the DC-bus in CDC configuration are 8140.57 A and 9232.3 A, respectively. In the SDC configuration, the RMS and peak current per DC-bus are 861.01 A and 1122.93 A, respectively, resulting in a total of 8610.1 A RMS current and 11229.3 A peak current across all 10 split DC-buses. These results indicate that, although the circulating currents do affect the current demands of the DC-bus in the CDC configuration, the overall effect is less significant compared to the SDC configuration.

In summary, this section presents the analysis of RMS currents in CDC and SDC configurations, assuming that the load coil is decoupled from the back-end converter and the inductors at the outputs of each HB have no resistive component. In the following section, the same analysis is performed considering the resistive component of the inductor and the deviation in the output voltage, which affects the load current ripple when the load coil is not decoupled from the back-end converter.

3.2 Common DC and Split DC Topologies under Non-Ideal Conditions

Building on the idealized analysis of interleaved HBs in Section 3.1, this section investigates the behavior of both CDC and SDC configurations under conditions of more realistic parameters. In practical implementations, parasitic effects such as the winding resistance of inductors can significantly influence the PCs performance. This non-ideality affects key parameters, including voltage drops, power losses, and ultimately the accuracy of analytical models derived under ideal assumptions.

Fig. 3.7 shows the simplified representation of CDC and SDC configurations similar to Fig. 3.1, but additional considerations, such as the winding resistances of the inductors, are included.

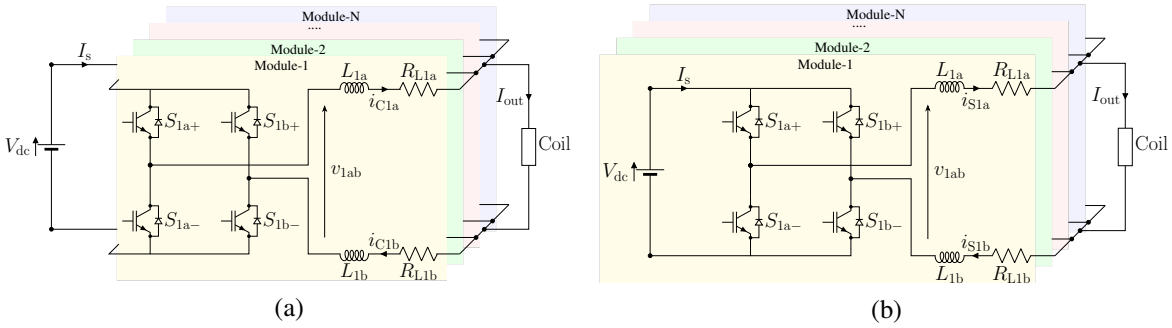


Figure 3.7: Typical topologies for N-module interleaved HBs under a non-ideal case. (a) CDC. (b) SDC.

For the sake of comparing the SDC and CDC configurations, in Fig. 3.7, similar to the inductance L, the value of the winding resistances R_{Lna}, R_{Lnb}, is assumed to be the same and equal to a generic resistance R_{L} (i.e., $R_{Lna} = R_{Lnb} = R_{\mathrm{L}}$). This addition makes the analysis more reflective of physical systems, where copper losses are non-negligible.

The analytical equations derived in Section 3.1.1 and Section 3.1.2 were based on the assumption that the load coil is electrically decoupled from the interleaved HBs through the use of appropriate filtering components. This assumption is valid for a wide range of applications, particularly those requiring precise regulation of current and voltage ripple, such as central solenoid coils, toroidal coils, and edge-localized mode coils in nuclear fusion reactors, as well as dipole magnets and quadrupole magnets in particle accelerators [91, 92]. In these applications, achieving stringent control of output current ripple is critical, and the PCs output is typically equipped with filters to meet the specific requirements of the connected coil loads [93].

However, not all coil applications permit such decoupling. For example, in the case of vertical stabilization coils in tokamak reactors, the demand for a rapid dynamic response to control plasma instabilities precludes the use of output-side filters, which would otherwise introduce unwanted delay and attenuate fast-changing signals [94]. In such cases, the interleaved HBs are directly connected to the coil. Under these conditions, the analytical formulations developed in the previous section and the current section still remain valid, although some errors may be introduced due to the difference in coil voltage, which was previously assumed constant.

In configurations where the coil is decoupled from the interleaved HBs via a low-pass filter, the output voltage across the load V_{out} can be treated as a constant. It is therefore valid to describe this voltage using the switching time-averaged formulation introduced earlier in (3.9).

On the other hand, when the coil is not decoupled from the interleaved HBs, the instantaneous output voltage v'_{out} is no longer constant and cannot be represented using (3.9). In this scenario, it becomes necessary to model the aggregate behavior of the interleaved HBs using an equivalent Millman representation, as depicted in Fig. 3.8. This approach allows the configuration to be analyzed using Millman's theorem, where interleaved HBs contribute to a voltage source v_{eq} and the equivalent impedance is dominated by the parallel combination of inductor impedances [95].

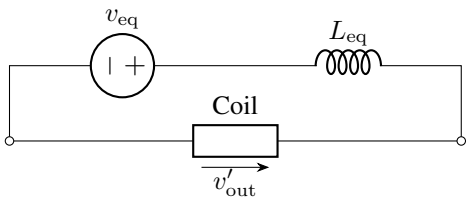


Figure 3.8: Millman equivalent circuit of the N parallel connected HBs.

In this representation, the equivalent voltage v_{eq} seen by the coil is the average of the instantaneous output voltages of N interleaved HBs, expressed mathematically as:

$$v_{\text{eq}} = \sum_{n=1}^{N} \frac{\frac{v_{\text{nab}}}{\overline{Z}_{\text{na}} + \overline{Z}_{\text{nb}}}}{\frac{1}{\overline{Z}_{\text{na}} + \overline{Z}_{\text{nb}}}} = \frac{\frac{1}{2\overline{Z}}}{\frac{N}{2\overline{Z}}} \sum_{n=1}^{N} v_{\text{nab}} = \frac{1}{N} \sum_{n=1}^{N} v_{\text{nab}} \,. \tag{3.18}$$

Similarly, the equivalent inductance seen at the coil terminal, L_{eq}, is given by the parallel combination of all individual inductor pairs across each HB:

$$L_{\text{eq}} = \frac{1}{\sum_{n=1}^{N} \frac{1}{L_{\text{na}} + L_{\text{nb}}}} = \frac{2L}{N} \,. \tag{3.19}$$

Where v_{nab} is the instantaneous voltage of the n-th HB, this result comes from the uniformity in the inductive impedance across HBs, assuming $\overline{Z} = \overline{Z}_{\text{na}} = \overline{Z}_{\text{nb}} = j\omega L$, and leveraging the symmetry in the interleaved configuration.

Using the voltage divider rule, the instantaneous voltage across the load coil, now denoted as v'_{out}, can be expressed as:

$$v'_{\text{out}} = v_{\text{eq}} \frac{L_{\text{c}}}{L_{\text{c}} + L_{\text{eq}}} \,, \tag{3.20}$$

which, upon substituting (3.19) becomes:

$$v'_{\text{out}} = v_{\text{eq}} \frac{N}{N + \frac{2L}{L_{\text{c}}}} \,. \tag{3.21}$$

Equation (3.21) reveals that the output voltage seen by the coil is attenuated relative to the average HB voltage, and this attenuation is a function of both the number of interleaved modules and the relative inductances of the HB legs and the load coil.

Averaging (3.21) over one time-period ($1/N f_{\text{s,IHB}}$), leads to the following expression:

$$V'_{\text{out}} = \delta V_{\text{dc}} \frac{N}{N + \frac{2L}{L_{\text{c}}}} \,. \tag{3.22}$$

From (3.22), it is evident that the average output voltage V'_{out}, in the absence of decoupling, approaches to that of the decoupled case (3.9) as the N increases or L_{c} is sufficiently high, making the ratio of $(2L/L_{\text{c}})$ negligible.

3.2.1 Analysis of Interleaved HB in CDC and SDC Configurations under Non-Ideal Conditions

The RMS current expressions for the interleaved HBs in both the CDC and SDC configurations were previously derived in Section 3.1.1 and Section 3.1.2, respectively.

However, those analyses were based on two simplifying assumptions: the winding resistance of the inductors was neglected, and the load coil was considered fully decoupled from the interleaved HB stage. In this subsection, these assumptions are partially relaxed. Specifically, the RMS current equations are reformulated to account for the winding resistance of the inductors, while still maintaining the assumption of load decoupling from the interleaved HBs.

The RMS current of the n-th HB, taking into account the winding resistance of the inductor in both the SDC and CDC configurations, is derived in this subsection. As detailed in Section 3.1, the non-zero-frequency components in the SDC and CDC configurations differ, primarily due to the presence of circulating currents in the CDC configuration. Since the winding resistance of the inductor does not affect the current ripple, the RMS of the current ripple in the inductor of SDC configuration $I_{\mathrm{rip}}\big|_{\mathrm{SDC}}$, under non-ideal conditions, can still be expressed as in (3.5). Similarly, the RMS of the current ripple in the inductor of the CDC configuration $I_{\mathrm{rip}}\big|_{\mathrm{CDC}}$, under non-ideal conditions, can be expressed as in (3.14).

Conversely, these equations (3.5) and (3.14) can also be utilized during the design phase of the PCs to determine the required value of inductance L either in SDC or CDC configuration when a limit is imposed on the acceptable current ripple in interleaved HBs.

It is also evident from (3.5) and (3.14) that the RMS of the current ripple in interleaved HBs in both configurations is independent of the DC component of the current, which represents the load contribution (I_{avg}).

The DC component I_{avg}, representing the load current contribution, is the same for both CDC and SDC configurations and can be expressed as:

$$I_{\mathrm{avg}} = \frac{I'_{\mathrm{out}}}{N} \,, \tag{3.23}$$

where I'_{out} is the output current under non-ideal conditions.

When considering the winding resistance of the inductors, the output current I'_{out} is expressed as:

$$I'_{\mathrm{out}} = \frac{\delta V_{\mathrm{dc}}}{R_{\mathrm{eq}}} \,, \tag{3.24}$$

and having assumed the winding resistances of the inductors, the equivalent resistance R_{eq} seen by the output current is given by:

$$R_{\mathrm{eq}} = R_{\mathrm{c}} + \frac{2R_{\mathrm{L}}}{N} \,. \tag{3.25}$$

Replacing (3.14) and (3.24) in (3.15), the RMS value of the inductor current at leg a of the n-th HB in the non-ideal condition of the CDC configuration (I'_{Cn}) is expressed as:

$$I'_{\mathrm{Cn}} = \sqrt{\left(\frac{\delta V_{\mathrm{dc}}}{N R_{\mathrm{eq}}}\right)^2 + \left[\frac{V_{\mathrm{dc}}}{8\sqrt{3} L f_{\mathrm{s}}}\left(1-\delta^2\right)\right]^2} \,. \tag{3.26}$$

Due to the symmetry between leg a and leg b of the HB, (3.26) derived for the leg a of n-th HB holds valid for the leg b of n-th HB in the CDC configuration.

Similarly, by replacing (3.5) and (3.24) into (3.4), the RMS value of the inductor current in the leg a of the n-th HB in the non-ideal condition of the SDC configuration (I'_{Sn}) is expressed as:

$$I'_{\mathrm{Sn}} = \sqrt{\left(\frac{\delta V_{\mathrm{dc}}}{N R_{\mathrm{eq}}}\right)^2 + \left[\frac{V_{\mathrm{dc}}}{8\sqrt{3} L f_{\mathrm{s}}}\delta\left(1-\delta\right)\right]^2} \,. \tag{3.27}$$

Equation (3.27) holds valid for the leg b of the n-th HB in SDC configuration.

In both (3.26) and (3.27), although the average current component (I'_{out}/N) is ideally the same in all legs of the N interleaved HBs, practical factors, component tolerances, may cause a current imbalance among the HB legs in the CDC configuration. This, in turn, may impact the accuracy of power loss calculations. To address this limitation, current balancing techniques may be implemented. Hardware-based approaches, which require using current sensors in each leg of the HBs, or control-based solutions, such as sensorless estimation methods, can help mitigate the current imbalance. However, both techniques contribute to an increase in the complexity of the control [96].

Similarly, analogous to the approach under ideal conditions discussed in Section 3.1.3, a normalization factor (I'_{out}/N) is applied to partially decouple the computed RMS in the CDC configuration from the influence of the output current I'_{out}. Specifically, the normalized current for the n-th HB in the CDC configuration is expressed as:

$$I_{\mathrm{C}} = N\frac{I'_{\mathrm{Cn}}}{I'_{\mathrm{out}}} \,. \tag{3.28}$$

3.2.2 Interleaved HB and Inductor Losses

In nuclear fusion and particle accelerator applications, power loss is a more relevant performance indicator than overall PCs efficiency, due to the short duration of load profiles, and the output power mainly corresponds to the resistive losses in the coil. Hence, in this section, total losses in the CDC and SDC configurations are analyzed.

In the SDC configuration, the current stress on semiconductors and inductors, on a first approximation, is mainly due to the load contribution current. In contrast, in the CDC, the current stress is increased due to the circulating current. This increased stress results in higher losses in the CDC configuration compared to the SDC configuration. Therefore, when selecting the topology for the PCs, it is essential to consider these losses, as they significantly influence the design of the cooling system.

The losses in the N parallel HBs of a CDC or SDC configurations can be divided into two components: losses in the semiconductor P_{sw} and losses in the inductor P_{L}. Considering that all the N HBs are identical, and each HB has two legs, the total losses can be expressed as:

$$P_{\mathrm{loss}} = 2N\left(P_{\mathrm{sw}} + P_{\mathrm{L}}\right) \,. \tag{3.29}$$

The losses associated with the switches can be further classified into conduction losses P_{cond}, commutation losses P_{com}, as well as auxiliary supply power required by semiconductor gate drivers P_{a}.

$$P_{\mathrm{sw}} = P_{\mathrm{cond}} + P_{\mathrm{com}} + P_{\mathrm{a}} \,. \tag{3.30}$$

During each switching cycle, within each leg of an HB, the conduction losses are expressed as:

$$P_{\mathrm{cond}} = \delta_{\mathrm{a}}\left(V_{\mathrm{CEO}} I_{\mathrm{L}} + R_{\mathrm{sw}} I_{\mathrm{L}}^2\right) + \delta_{\mathrm{b}}\left(V_{\mathrm{d}} I_{\mathrm{L}} + R_{\mathrm{d}} I_{\mathrm{L}}^2\right) \,, \tag{3.31}$$

where V_{CEO} is the on-state voltage threshold of the semiconductor, I_{L} is the RMS of HB current, R_{sw} is the on-state resistance of the semiconductor, V_{d} is the diode forward voltage, and R_{d} is the on-state resistance of the diode.

The commutation losses are given by:

$$P_{\mathrm{com}} = \frac{f_{\mathrm{s,IHB}} V_{\mathrm{dc}} I_{\mathrm{L}}}{V_{\mathrm{t}} I_{\mathrm{t}}} \left[(E_{\mathrm{on}} + E_{\mathrm{off}}) + E_{\mathrm{rec}} \right] , \tag{3.32}$$

where E_{rec} is the reverse recovery energy of the diode, and E_{on} and E_{off} are the energy dissipated during the turn-on and turn-off transitions of the semiconductor, respectively. These values of energy can be typically taken from the component datasheets under specific voltage V_{t} and current I_{t} conditions.

For what concerns the inductor, its losses are split into losses in the ferromagnetic core P_{fe} and losses in the copper windings P_{cu}, i.e.:

$$P_{\mathrm{L}} = P_{\mathrm{fe}} + P_{\mathrm{cu}} . \tag{3.33}$$

As discussed in [97], the copper losses and iron losses are approximately equal at the nominal current for an efficiently designed inductor. Therefore, the losses in the inductor P_{L} can be represented as:

$$P_{\mathrm{L}} = I_{\mathrm{L}}^2 \left(R_{\mathrm{ESR,fe}} + R_{\mathrm{ESR,cu}} \right) . \tag{3.34}$$

Where $R_{\mathrm{ESR,cu}}$ is the portion of equivalent series resistance associated with copper losses, and $R_{\mathrm{ESR,fe}}$ corresponds to the portion of equivalent series resistance related to ferromagnetic core losses. Once the inductor has been selected and the operating frequency is fixed, the losses in the ferromagnetic core become only dependent on the induction peak. Assuming that the core material operates in the linearity region, it is therefore possible to state that the losses in the inductor are dependent on the current value alone. Consequently, $R_{\mathrm{ESR,fe}}$ can be scaled as a function of the inductor current.

Replacing the expressions of (3.34), (3.32), (3.31), and (3.30) in (3.29) results in:

$$\begin{aligned} P_{\mathrm{loss}} =& 2N \Bigg\{ P_{\mathrm{a}} + I_{\mathrm{L}} \left[\frac{f_{\mathrm{s,IHB}} V_{\mathrm{dc}}}{V_{\mathrm{t}} I_{\mathrm{t}}} \left(E_{\mathrm{on}} + E_{\mathrm{off}} + E_{\mathrm{rec}} \right) + \delta_{\mathrm{a}} V_{\mathrm{CEO}} + \delta_{\mathrm{b}} V_{\mathrm{d}} \right] + \\ & I_{\mathrm{L}}^2 \left[R_{\mathrm{ESR,fe}} + R_{\mathrm{ESR,cu}} + \delta_{\mathrm{a}} R_{\mathrm{sw}} + \delta_{\mathrm{b}} R_{\mathrm{d}} \right] \Bigg\} . \end{aligned} \tag{3.35}$$

Deriving the general form of losses in (3.35), it is possible to distinguish the losses specific to the CDC and SDC configurations. For the CDC configuration, the losses $P_{\mathrm{loss}}\big|_{\mathrm{CDC}}$ can be expressed as:

$$P_{\mathrm{loss}}\big|_{\mathrm{CDC}} = P_{\mathrm{loss}}\big|_{\mathrm{I_L = I'_{Cn}}} , \tag{3.36}$$

and for the SDC configuration, the losses $P_{\mathrm{loss}}\big|_{\mathrm{SDC}}$ are given by:

$$P_{\mathrm{loss}}\big|_{\mathrm{SDC}} = P_{\mathrm{loss}}\big|_{\mathrm{I_L = I'_{Sn}}} . \tag{3.37}$$

Equation (3.36) provides information about the losses in the N interleaved HBs, considering the effect of circulating current.

A numerical case study is conducted for 10 interleaved HBs to evaluate and compare the variation of losses in CDC and SDC configurations. For the sake of comparison, as described in Section 3.1, the parameters of the PCs are considered equal.

For calculating losses in both CDC and SDC configurations, the Infineon FF1800R17IP5 module is used as the model for each leg of the 10 parallel connected HBs. An air-core inductor with an inductance of 25 μH is considered for each HB leg. The switching frequency is fixed at 2 kHz, and the winding resistance of each inductor is assumed constant at 50 mΩ. The considered values for the DC-bus voltage are $V_{\mathrm{dc}} = 1$ kV, and the output current is $I_{\mathrm{out}} = 10$ kA. For simplification, the auxiliary power consumption of the gate drivers, denoted as P_{a}, is excluded from the loss calculations, since it does not vary with the current through the HB legs and thus has no impact on comparative analysis between the two topologies.

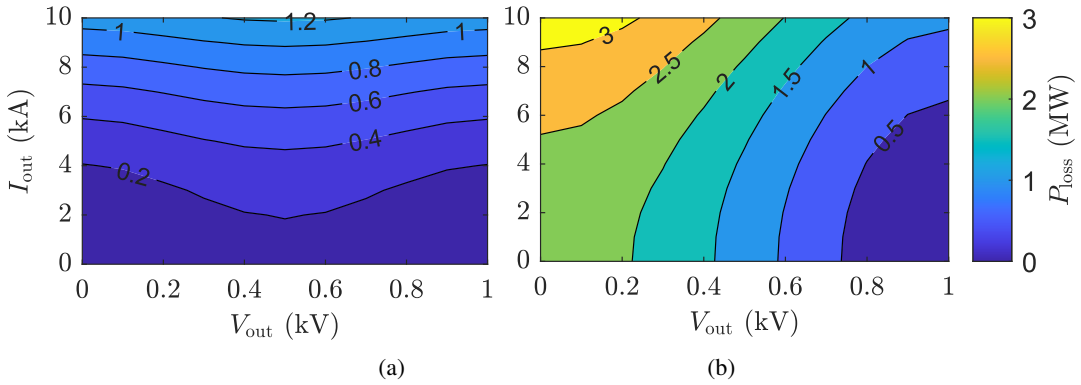


Figure 3.9: Power losses in 10 parallel connected HBs: (a) SDC configuration; (b) CDC configuration.

The variation in losses while delivering the equal output power in SDC and CDC configurations is shown in Fig. 3.9(a) and Fig. 3.9(b), respectively. The losses are computed by varying the output current I_{out}, and output voltage V_{out} across a range from 0 to 100% of their rated values. As evident from Fig. 3.9, the CDC configuration consistently exhibits higher losses than the SDC configuration across the entire operating range. This increased loss in the CDC configuration is primarily attributed to the presence of circulating currents, which impose additional current stress on the semiconductors and inductors. For both topologies, total losses rise with increasing output current, as higher current levels lead to increased conduction and switching losses in both the semiconductors and inductors.

However, in the case of CDC configuration, at constant output current, for instance, at $I_{\mathrm{out}} = 2$ kA, the losses are higher at lower output voltage $V_{\mathrm{out}} = 0$ kV compared to higher output voltage $V_{\mathrm{out}} = 1$ kV. This is because circulating currents dominate at lower gain ratios, as compared to the higher gain ratios. In both CDC and SDC configurations, the losses are not zero even when no power is delivered to the load, as is the case when V_{out} = 0 V, due to 0.5 duty cycle of leg a and leg b of each of the ten interleaved HBs.

Estimation of these losses plays a critical role in the selection of the most suitable topology for the PC. Once the maximum allowable junction temperature of the semiconductors and the design specifications of the cooling system are estimated, the maximum losses manageable by the cooling system can be evaluated using analytical equations available in the literature [98]. This evaluation serves as one of the inputs for the algorithm discussed in the following section.

3.3 Back-End Converter Design Algorithm

Based on the analytical equations derived in Section 3.2 (whose experimental validation is reported in Section 3.4), an algorithm is proposed in this section to determine the topology of the PC [99]. The proposed algorithm considers the drawbacks associated with the circulating current in the CDC configuration and the increase in the number of galvanically isolated DC-buses.

3.3.1 Algorithm Description

The algorithm is illustrated in the flowchart in Fig. 3.10. In this flowchart, blue blocks represent

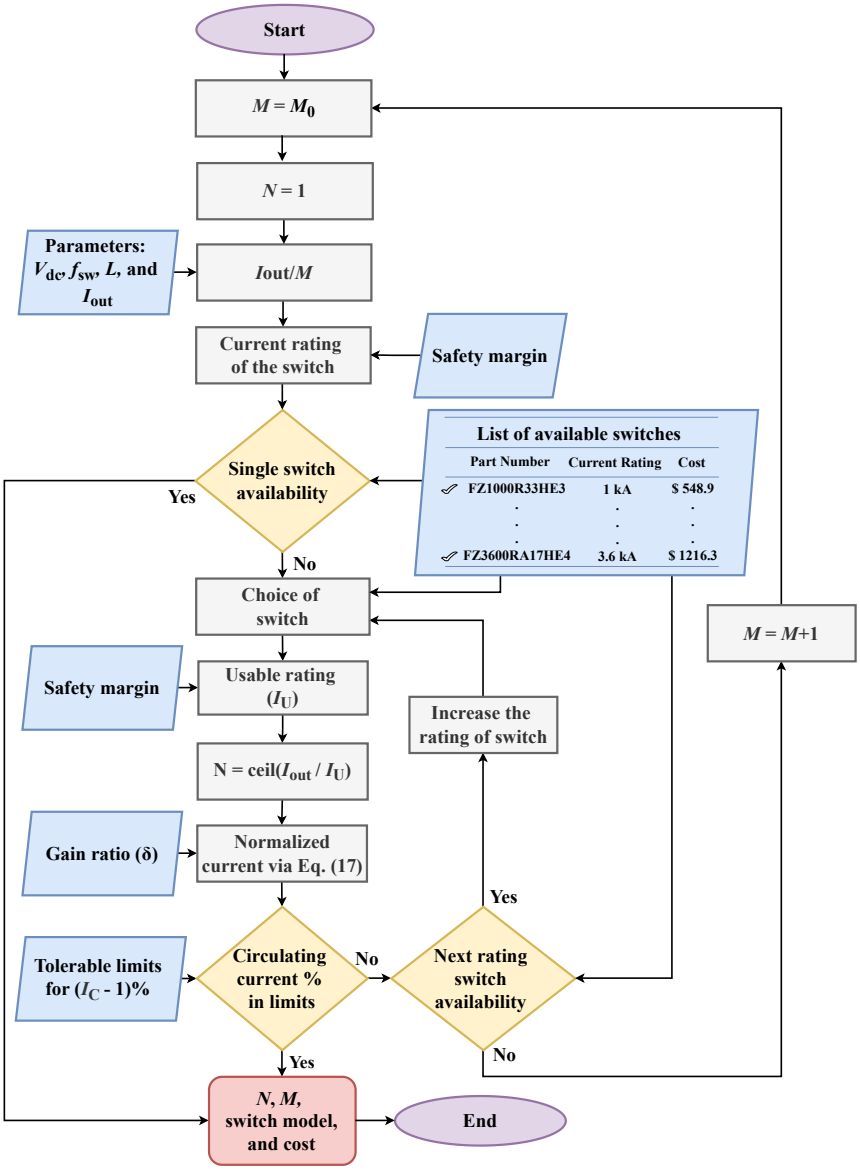


Figure 3.10: Flowchart for the topology selection of the PC.

the required inputs for the algorithm, gray blocks perform the computations, yellow blocks indicate decision-making steps, and the red block signifies the output of the algorithm. The main input parameters for the algorithm are the output current I_{out}, DC-bus voltage V_{dc}, inductor inductance L, switching frequency $f_{\mathrm{sw,IHB}}$, gain ratio δ, safety margin, assumed with respect to the thermal limits and the safe operating area of the semiconductor, and the tolerable limit for the effect of circulating current percentage. The latter is defined based on the maximum losses that the cooling system can dissipate.

The algorithm begins by assuming the number of galvanically isolated DC-buses M to an initial value M_0, and the number of HBs for a single DC-bus N equal to 1. The value of M_0 can be set to any integer greater than 1. This choice was made to offer the user the possibility of assuming a certain number of isolated DC-buses from the outset. The algorithm first verifies whether a single semiconductor in the HB configuration can handle the output current I_{out} while remaining within safety margin limits. If this condition is met, the algorithm outputs $N = 1$ and $M = M_0$ along with the choice of semiconductor. However, if the single semiconductor cannot handle I_{out}, the algorithm proceeds by considering the parallel of HBs by increasing N.

At this stage, the semiconductor selection process begins with the lowest-rated option and iterates through the available semiconductors, progressing to the next available option. In each iteration, the effect of the circulating current in percentage is computed using (3.28). The algorithm checks whether the computed percentage of circulating current effect $(I_{\mathrm{C}}-1)100\%$, remains within acceptable limits, as defined in the *Tolerable limits for* $(I_{\mathrm{C}} - 1)\%$ block. Suppose the circulating current percentage exceeds the acceptable threshold; the algorithm selects a higher-rated semiconductor and decreases N for a single DC-bus to reduce the effect of circulating current I_{C}. Suppose the effect of the circulating current continues to exceed the limit even with the highest-rated semiconductor; the algorithm increases the number of DC-buses M and reevaluates the percentage of the circulating current effect to strike a balance between the increased number of galvanically isolated DC-buses and the effect of the circulating current, thereby resulting in a configuration that meets the design requirements of the PC. At the end of the iteration, the algorithm outputs a topology based on N HBs, M DC-bus, switch model, and rated current for the design topology, including the cost of the PC.

The other inputs visible in Fig. 3.10 serve to take operational and implementation constraints into account. For the *Safety margin* block, the input represents the percentage of current flowing through the semiconductor with respect to its rated value. This parameter considers both the semiconductors safe operating area and its junction temperature, which also depends on the current through it. The usable rating of semiconductor I_{U} in Fig. 3.10 is computed as the product of the safety margin times the rated current.

The *Gain ratio* input block requires a fixed value of δ. For a constant output current profile or constant output voltage profile, δ can be set to a higher value close to one, a zero-ripple corresponding value, or a combination of both $\delta = (N - 1)/N$, as analyzed in [90]. Alternatively, in the case of varying output voltage, δ can correspond to a worst-case scenario.

The *Tolerable limits for* $(I_{\mathrm{C}}-1)\%$ block allows for the provision of the information corresponding to the maximum losses that the chosen cooling system can dissipate.

The *List of the available switch* input block contains information on the semiconductor models available in the users database, including part number, rated current, and cost, sorted in ascending order of current ratings. This input block also enables the user to activate or deactivate specific semiconductors in the list, allowing exploration of various combinations based on availability, preference,

or economic constraints. In particular, if cost evaluation is of interest, the user can enable the cost-based selection within this block. In doing so, the algorithm outputs, in addition to the number of HBs, galvanically isolated DC-buses, the semiconductor model, and an estimated cost for the semiconductors in the DC/DC section. It is worth noting how the initial value M_0 can also be adjusted and used to explore different configurations and evaluate variations in the switch cost. A more complete cost evaluation can be performed in a subsequent step, once the topology has been defined. This includes adding the costs of interleaving inductors, sensors, and auxiliary circuits.

3.3.2 Illustrative Design Cases

To demonstrate its functionality, the proposed algorithm is applied to a set of design cases, which are subsequently validated through numerical simulations. The selected parameters are consistent with the order of magnitudes typically observed in the nuclear fusion and particle accelerator applications. Specifically: I_{out} = 10 kA, and V_{dc} = 1 kV. The inductance, winding resistance of the air-cored inductor, and switching frequency are fixed equal to 25 μH, 50 mΩ, and 2 kHz, respectively. These values are representative of practical ranges found in the aforementioned applications and serve to illustrate how the algorithm operates under typical design parameters. These same parameters have been used to determine the PCs losses in Section 3.2.2. A safety margin of 25% is assumed, limiting the selected semiconductor to operate at a maximum of 75% of its rated current. The gain ratio δ is fixed at 0.8, subsequently providing the inputs for the effect of the circulating current percentage. These results are obtained for different cases.

CASE-I: When the limit for circulating current percentage is set to 5%; the algorithm results in a CDC configuration (i.e., $M = 1$) with a number of parallel connected HBs $N = 6$, and the choice of a semiconductor rated for 2.4 kA.

CASE-II: If the limit for the effect of the circulating current percentage is increased to 10%, the topology remains CDC ($M = 1$), but the number of parallel connected HBs increases to $N = 8$, with the semiconductor rating reduced to 1.8 kA.

The results of case-II suggest that allowing a higher percentage of circulating current effect in the HBs equal to 10%, increases N to 8 while utilizing the smaller rated semiconductors 1.8 kA compared to case-I. In contrast, with stricter limits of 5%, case-I results in a lower number of HBs, requiring higher rated semiconductors 2.4 kA compared to case-II. These results align with the fundamental principles of the proposed algorithm.

In the next set of cases, the system parameters are adjusted by reducing the inductance of the inductor to 15 μH and lowering the gain ratio to 0.6, while the rest of the system parameters remain unchanged. Reducing both the inductance and gain ratio worsens the effect of the circulating current, thus creating a more challenging design scenario to evaluate the robustness and adaptability of the proposed algorithm.

CASE-III: With a safety margin of 10% and a circulating current percentage limit of 20%, the algorithm results in a topology with $N = 2$ and $M = 2$, with the choice of semiconductor rated for 3.6 kA. The resulting PCs topology consists of two galvanically isolated DC-buses, and each DC-bus is connected to two parallel HBs.

CASE-IV: If the circulating current limit is reduced to 4%, while keeping the same system parameters as in case-III, the algorithm results in $M = 4$ and $N = 1$, leading to an SDC with four parallel connected HBs.

As expected, reducing the inductance and gain ratio increases the effect of circulating current. In case-III, the higher allowable limit for the percentage of circulating current 20% results in a hybrid design that combines both the CDC and SDC configurations ($M = 2$ and $N = 2$). To accommodate the increased circulating current caused by decreasing the inductance and gain ratio parameters, the algorithm selects larger semiconductors rated at 3.6 kA, while also reducing the overall number of HBs ($M \cdot N = 4$).

In contrast, in case-IV, stricter limits of 4% on circulating current percentage, combined with the same reduced inductance and gain ratio parameters as in case-III, result in a topology favoring the SDC. This choice could be driven by the need to suppress circulating currents effectively, even if it means increasing the front-end components. The summary of design cases and algorithm results is presented in Table 3.2.

Table 3.2: Summary of design cases and algorithm results.

	Input Parameters				**Algorithm Output**			
	$\boldsymbol{\delta}$	$\boldsymbol{L}$	$\boldsymbol{f_{\mathrm{sw}}}$	$\boldsymbol{(I_{\mathrm{C}}-1)100\%}$	$\boldsymbol{M}$	$\boldsymbol{N}$	**Current rating**	**Topology**
CASE-I	0.8	25 μH	2 kHz	5%	1	6	2.4 kA	CDC
CASE-II	0.8	25 μH	2 kHz	10%	1	8	1.8 kA	CDC
CASE-III	0.6	15 μH	2 kHz	20%	2	2	3.6 kA	Hybrid
CASE-IV	0.6	15 μH	2 kHz	4%	4	1	3.6 kA	SDC

Numerical validations have been performed on the PLECS (Plexim GmbH) environment for each of the design cases demonstrated. Numerical simulations were performed with the same parameters δ, L, f_{sw}, I_{out}, and V_{dc} as those used in the design cases. Fig. 3.11(a), and Fig. 3.11(b) illustrate the variation of RMS currents in the interleaved HBs and the corresponding effect of circulating current as the number of HBs N ranges from 2 to 10. From Fig. 3.11(a) and Fig. 3.11(b), it is observed that for $N = 6$ in a CDC configuration, the percentage of circulating current is 4.7%, with each HB carrying an RMS current of 1.74 kA. These values fall within the requirements set for design case-I, where the percentage of circulating current is 5%. Accordingly, the selected semiconductor is rated at 2.4 kA, ensuring a minimum safety margin of 25%. In the case of $N = 8$, which still corresponds to a CDC configuration, the percentage of circulating current rises to 8.3%, while the RMS current in each HB drops to 1.35 kA. These results comply with the 10% limit defined for case-II, justifying the selection of a semiconductor rated at 1.8 kA with at least a 25% safety margin.

Fig. 3.11(c), and Fig. 3.11(d) correspond to the hybrid configuration $M = 2$, with N varying from 2 to 10 for each isolated DC-bus. These numerical simulations reflect the parameters of case-III. As shown in Fig. 3.11(d), when $N = 2$, the percentage of circulating current reaches 17.2%, remaining below the set limit of 20%. The RMS current in each HB at $M = 2$ and $N = 2$ is 2.95 kA, justifying the choice of a semiconductor rated at 3.6 kA with at least a 10% safety margin.

Fig. 3.11(e), and Fig. 3.11(f) correspond to the numerical validation results for case-IV. From Fig. 3.11(f), it is clearly evident that even with $N = 2$, the percentage of circulating current is 4.6%, which supports the selection of SDC configuration for this case. Meanwhile, Fig. 3.11(e) illustrates the RMS currents in the SDC configuration as N varies from 2 to 10. At $N = 4$, each interleaved HB carries an RMS current of 2.54 kA, validating the use of 3.6 kA rated semiconductor with at least a 10% safety margin.

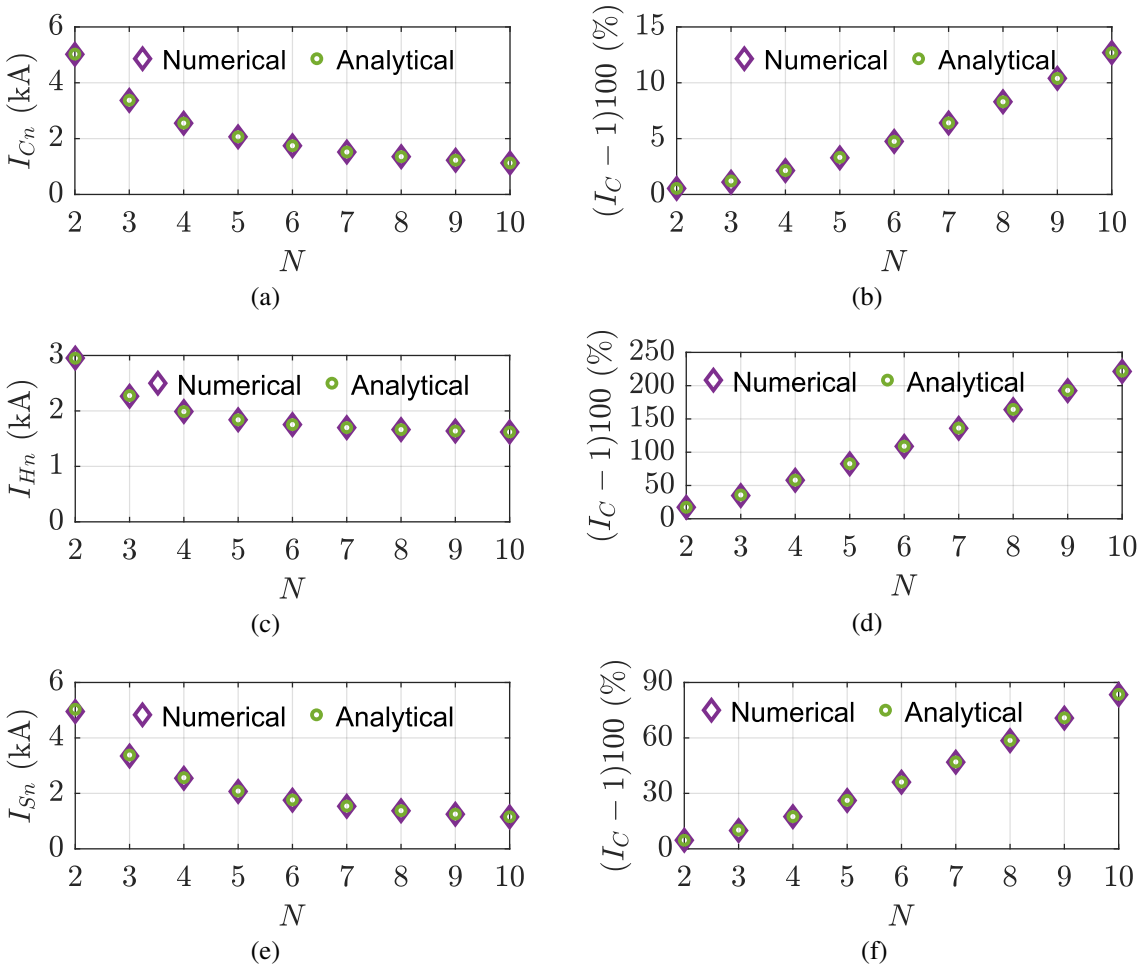


Figure 3.11: Numerical validation of the proposed algorithms analytical results: (a) RMS current in CDC, and (b) effect of circulating current at $\delta = 0.8$ and $L = 25$ μH; (c) RMS current in SDC, and (d) effect of circulating current in CDC at $\delta = 0.6$ and $L = 15$ μH ; (e) RMS current in hybrid configuration, and (f) effect of circulating current at $\delta = 0.6$ and $L = 15$ μH.

Overall, the results of the numerical simulation are in agreement with the analytical results of the proposed algorithm. These findings are consistent with the core principle of the proposed algorithm: balancing the effect of circulating current and the number of HBs to derive the most appropriate PCs topology. The outcomes demonstrate the robustness and adaptability of the proposed algorithm in handling varying system parameters and application requirements.

The RMS of the non-zero frequency component of the current in the n-th HB is fundamental to the formulation of the normalized current (3.28), which serves as the core analytical expression of the algorithm proposed in this section for selecting the appropriate PCs topology. Therefore, experimental validations are performed to validate the RMS of the non-zero frequency component, and are explained in greater detail in the following section.

3.4 Experimental Validation

The circulating current exists only in the CDC configuration and affects only the RMS of non-zero frequency components of the current. To validate the theoretical analysis and analytical developments discussed in Section 3.2.1, experimental tests were carried out, with a particular focus on the interleaved HB currents and the RMS of the non-zero frequency component of the current in the CDC configuration. It is trivial to experimentally validate the average component of the current, which is the same in both topologies and corresponds to I_{avg}. Furthermore, in the aforementioned applications, I_{avg} purely depends on the coils current profile. In addition, numerical simulations were also carried out to compare them with the experimental results for the PCs topology illustrated in Fig. 3.7(a). Taking advantage of the scalability of the analysis discussed in Section 3.2.1, a low-scale setup was built, as shown in Fig. 3.12, to facilitate the experimental validation.

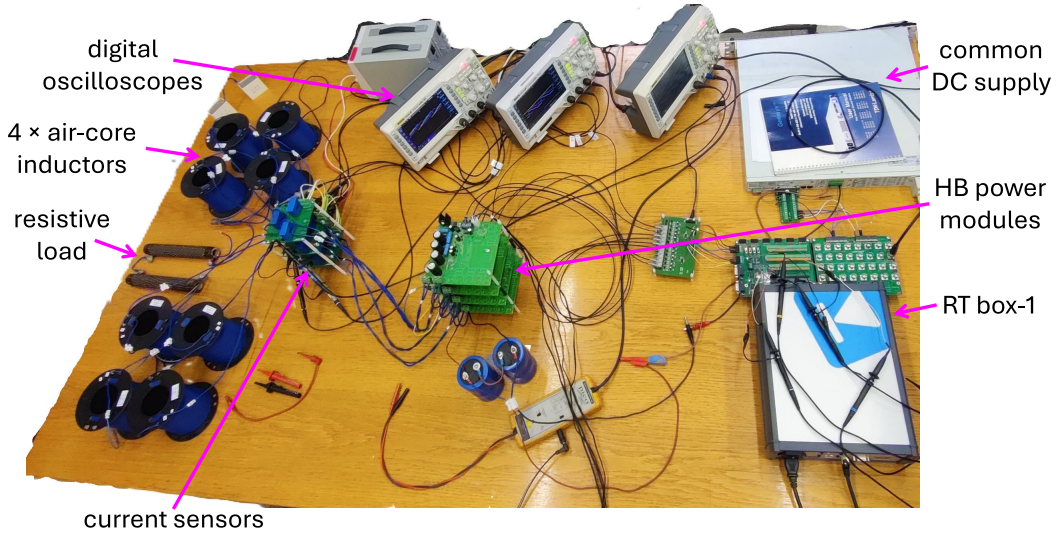


Figure 3.12: View of the laboratory experimental setup.

Both numerical simulation and experiments are iterated twice, first with three parallel HBs ($N = 3$), and then with four parallel HBs ($N = 4$), to analyze the HB currents and non-zero frequency components of the current under different numbers of HBs and gain ratios. The main parameters

Table 3.3: Experimental setup circuit parameters.

Parameter	**Symbol**	**Value**	**Unit**
DC-bus voltage	V_{dc}	45	V
Maximum output current	I_{out}	2.5	A
Interphase inductance	L	1.73	mH
Interphase inductor resistance	R_{L}	0.73	Ω
Load resistance	R_{c}	20	Ω
Switching frequency	$f_{\text{s,IHB}}$	2	kHz
Number of HBs	N	3 & 4	-

used in the numerical simulations performed in this section and experimental setup are summarized in Table 3.3.

The experimental setup is implemented using IGBT power modules, specifically PS22A76 from Mitsubishi Electric. The PWM signals required for controlling the IGBTs are generated by a Plexim RT-box 1. The setup also includes eight air-core inductors, a resistive load, and a controllable DC power supply, the GEN100-33 model from TDK-Lambda, which supplies power to the HBs. Currents in each leg of the parallel connected HB were measured using LA 55-p (LEM) current transducers, each powered by a ± 15 V supply. Data were acquired using three synchronized DS1054Z digital oscilloscopes (Rigol Technologies), each operating at a sampling rate 250 MS/s. PVP2150 probes were used with an attenuation ratio of $1\times$ (i.e., no attenuation). This setup ensured real-time synchronization of the HB current waveforms without any need for post-process synchronization.

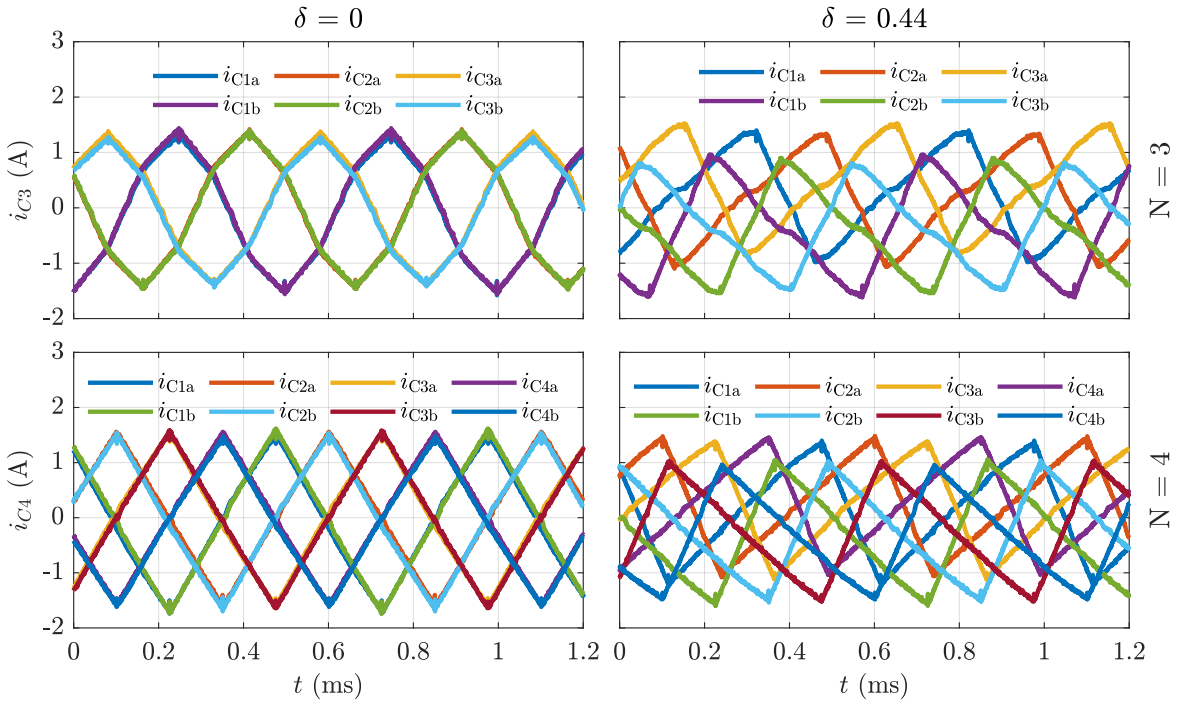


Figure 3.13: Experimental results for the currents in the interleaved HBs at $N = 3$, and 4, at $\delta = 0$ and 0.44.

The obtained current waveforms for $N = 3$ and 4 HBs, at $\delta = 0$ and 0.44 in the CDC configuration, are shown in Fig. 3.13 and Fig. 3.14, respectively.

In typical interleaved topologies, phase currents generally exhibit a triangular waveform. However, due to the presence of circulating current in the CDC configuration, the HB current waveforms deviate from the triangular shape, as evidenced by the experimental results shown in Fig. 3.13 and the numerical results shown in Fig. 3.14. In these figures, the up-shifted currents at $\delta = 0.44$ correspond to the currents in the leg a of the interleaved HBs, while the down-shifted currents correspond to the leg b. In Fig. 3.13, it can be observed that HB currents are lightly imbalanced. This is mainly due to slight differences in the inductance values at each HB output, as also discussed in [100].

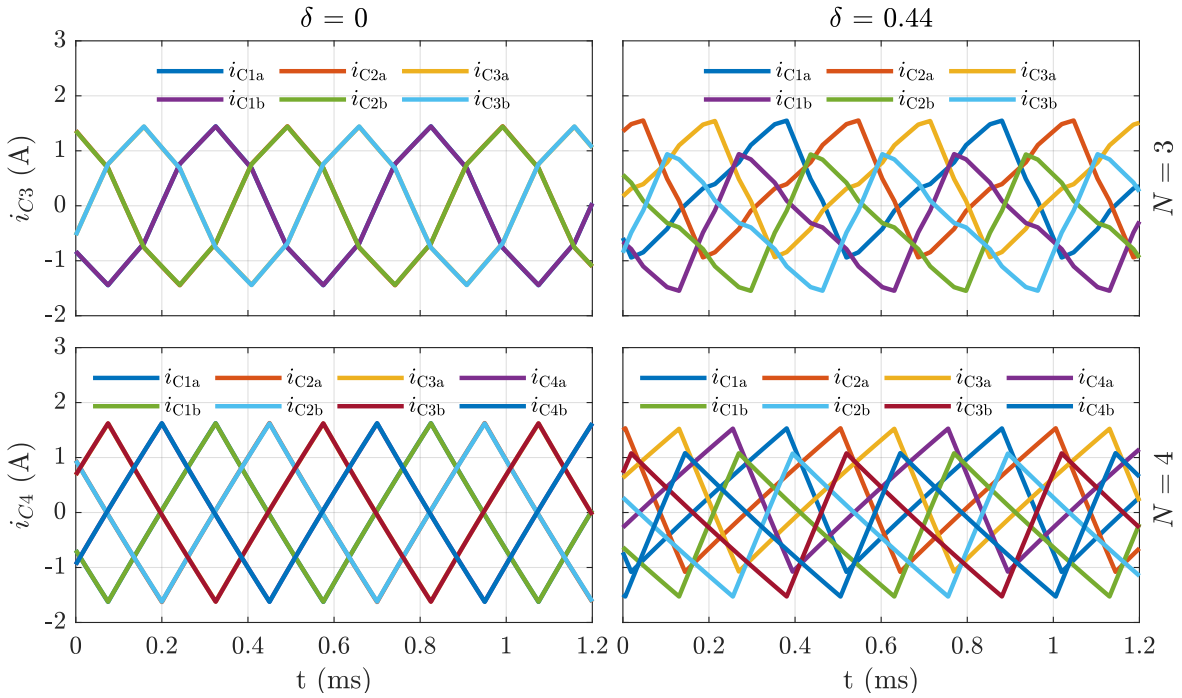


Figure 3.14: Numerical results for the currents in the interleaved HBs at $N = 3$, and 4, at $\delta = 0$ and 0.44.

As analyzed in Section 3.1, the current ripple in the CDC configuration increases as with the number of HBs. In particular, lower gain ratio values result in higher current ripple values due to the dominance of circulating currents, as evident from both the experimental results shown in Fig. 3.13 and the numerical results shown in Fig. 3.14. In particular, for both $\delta = 0$ and $\delta = 0.44$, increasing the number of HB from $N = 3$ to $N = 4$ results in higher peak-to-peak current ripple in leg a of the first HB. The numerical results closely match the experimental results, confirming the same behavior across all considered gain ratios and number of HBs. A quantitative comparison between experimental and numerical peak-to-peak current ripple values is summarized in Table 3.4, demonstrating good agreement between the two.

Table 3.4: Summary of experimental and numerical results.

N	δ	**Current Ripple Experimental**	**Current Ripple Numerical**
3	0	2.88 A	2.89 A
	0.44	2.44 A	2.49 A
4	0	3.28 A	3.25 A
	0.44	2.62 A	2.61 A

To further validate the RMS of the non-zero frequency component of the current derived for CDC configuration in (3.14), both analytical results and experimental results corresponding to each leg of HB at $N = 3$ and 4 are shown in Fig. 3.15.

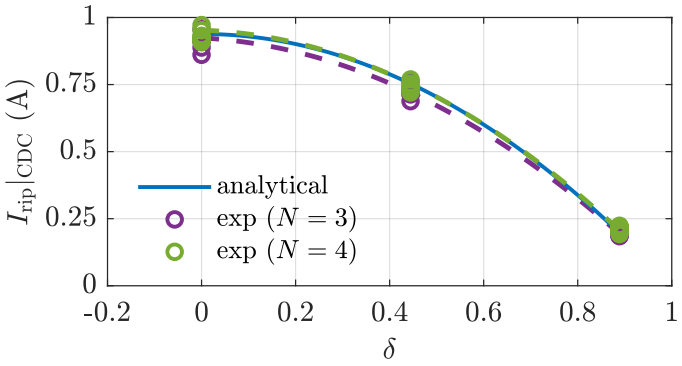


Figure 3.15: RMS currents of non-zero frequency components at $N = 3$ and 4.

The results corresponding to the experimentation are obtained by calculating the RMS after removing the average component (3.23) from the currents shown in Fig. 3.13. As explained in Section 3.1.3, the RMS of the non-zero frequency component decreases as the gain ratio or output voltage increases, which is evident from Fig. 3.15. For instance, at $N = 3$, the $I_{\text{rip}}|_{\text{CDC}}$ in leg a of 1st HB at $\delta = 0$ is 0.72 A, while at $\delta = 0.44$, it is 0.19 A. Similarly, at $N = 4$, the $I_{\text{rip}}|_{\text{CDC}}$ at $\delta = 0.44$ and 0.89 are 0.75 A and 0.21 A respectively. These experimental results in the case of $N = 3$ and 4 show good alignment with the analytical developments (3.14), and the intermediate experimental data points were interpolated using a second-order polynomial fit to generate the continuous curves in Fig. 3.15.

Although the experimental validation was performed at low power levels, the underlying concept behind the proposed algorithm, centered on the analysis of the non-zero frequency component of the current in HB, is inherently scalable. This scalability implies that the insights and results obtained at reduced power levels can be extrapolated with confidence to high power levels, making the findings broadly representative.

From a design perspective, when scaling up to higher power levels, the primary challenges are not associated with the algorithm itself but rather with practical engineering considerations. The most critical of these include effective thermal management and the appropriate selection of power components rated to withstand higher voltage, current, and temperature stresses. Notably, the auxiliary components and additional circuitry, such as control hardware and gate drivers, typically remain largely unchanged across different power levels.

In addition to these aspects, further practical considerations arise at higher power levels. These include the enhanced need for insulation, increased creepage and clearance distances, which directly influence the mechanical design, busbar layout, and overall enclosure dimensions. Moreover, increased electromagnetic interference and signal noise necessitate careful shielding, filtering, and, in some cases, the use of differential sensing or fiber optic links for reliable control and measurement. Nonetheless, it is essential to emphasize that the proposed algorithm, which relies on the analysis of non-zero frequency components of the HB current, remains fully scalable and fundamentally independent of the power level. These practical considerations primarily affect the physical implementation, rather than the algorithmic approach itself, and must be carefully addressed during the engineering and installation phases.

3.5 Summary

In applications such as nuclear fusion and particle accelerators, the DC-bus is typically large, resulting in negligible voltage ripple. This large DC-bus also effectively decouples the front-end and back-end stages of the PC. Consequently, this chapter focuses solely on analyzing the back-end converter topologies, specifically the CDC and SDC, rather than on the front-end components or auxiliary components.

This chapter begins by discussing the variation in the RMS value of the non-zero frequency component of the current in CDC and SDC configurations under ideal conditions. The analytical developments are then validated through numerical simulations across a range of gain ratios, showing good agreement with the analytical developments. Subsequently, the analysis is extended to non-ideal conditions, considering factors such as the winding resistance of the inductors. Analytical expressions for the RMS of the non-zero frequency component of the current and the RMS current in a generic number of parallel-connected HBs are derived for both the CDC and SDC configurations. Eventually, these outcomes are validated experimentally and compared with numerical simulations for 3 and 4 HBs in the CDC configuration, across various gain ratios. The experimentally obtained RMS values of the non-zero frequency current components show fair agreement with the analytical developments.

Further analysis introduces the concept of normalized RMS current in the CDC configuration, which decouples the effect of circulating currents from the output current. This provides deeper insights into the contribution of circulating current in each HB, especially as the number of parallel connections increases for a single DC-bus to achieve higher output currents with the goal of reducing front-end components. Additionally, this chapter examines the variation in power losses due to circulating currents in the CDC configuration. Analytical expressions for these losses, applicable to a generic number of parallel HBs, are derived for both the CDC and SDC configurations and compared accordingly.

In conclusion, this chapter highlights the trade-offs between the drawbacks of circulating current in the CDC configuration and the need for multiple galvanically isolated DC-buses in the SDC configuration. By leveraging the analysis of normalized RMS current in the CDC configuration, an algorithm is proposed to facilitate the automatic selection of the PCs topology for an operationally effective solution. The proposed algorithm is demonstrated through illustrative design cases, revealing its ability to balance the trade-offs between circulating current effects and the number of galvanically isolated DC-buses. These design cases are further validated through numerical simulations, with results aligning coherently with the fundamental principles of the proposed algorithm, highlighting its robustness and adaptability for applications such as particle accelerators and nuclear fusion systems.

Chapter 4

Conclusion and Perspectives

This thesis first focused on the functionality of the AFE part of PC as a reactive power compensator, and then analyzed two possible configurations in the back-end stage of PC for nuclear fusion and particle accelerator applications. Throughout the thesis, the main focus has been devoted to understanding the critical requirements of load coils and investigating existing PC configurations, taking into consideration the interests in the whole operation of the accelerator systems and nuclear fusion reactors.

This approach allows the investigation of the dual functionality of the AFE part of PC as a reactive power compensator, during light-load conditions, thereby reducing the reliance on traditional reactive power compensation methods on the grid side. As well as analysing the effect of circulating current in interleaved HB configurations when connected to a common DC-bus, with the objective of reducing front-end components, thus reducing the footprint and cost. However, this advantage comes at the expense of compromised back-end converter performance due to the increasing effect of circulating current as the number of HBs increases to support higher output current.

To address both aspects in this thesis, an instantaneous energy based DC-bus voltage control technique is proposed to enable the operation of the AFE of PCs as a reactive power compensator. In addition, an algorithm is developed to automatically determine the most appropriate for the back-end stage of the PCs, taking into account the respective advantages and disadvantages of SDC and CDC architectures. Every original proposal and analysis has been described analytically and validated under various operating conditions. Numerical simulations and experimental tests validated the effectiveness of the proposed developments.

4.1 Contributions

The thesis begins by introducing the motivation for the research, emphasizing the importance of PCs in nuclear fusion and particle accelerator applications. It discusses the critical role of coils as key infrastructure components and outlines the main characteristics of the PCs that supply them. Particular attention is given to the need for operating AFE as a reactive power compensators at CERN, highlighting current limitations in the literature. The introduction also presents the relevance of interleaved HB configurations in such applications, discussing the benefits and drawbacks of the CDC and SDC configurations and motivating the development of an algorithm to assist in the selection of appropriate PC topologies.

The subsequent chapter focuses on the NPC based AFE converter implemented in CERNs POPS-B converter. It begins by reviewing the control techniques applied in the POPS-B converter, including grid power control based on the synchronous reference $dq-$frame, semi-DC-bus voltage balancing, CMVI method, sinusoidal PWM, and DC-bus voltage regulation methods. The potential use of the stationary reference $\alpha\beta-$frame as an alternative grid control strategy is also investigated. Building upon these foundations, a novel DC-bus voltage control method based on instantaneous energy balance and variable DC-bus operation is proposed and analyzed for its suitability in light-load conditions and for various AFE design rating considerations relevant to nuclear fusion and particle accelerator applications. The chapter then presents an in-depth analysis of the neutral point current and its variation under different reactive power operating conditions, supported by analytical models and numerical validation using both $dq-$ and $\alpha\beta-$frame grid power control techniques. The harmonic characteristics of the neutral point current are also examined and verified numerically. Furthermore, the behavior of the semi-DC-bus voltages and the DC-bus voltage harmonics is investigated and validated numerically and experimentally across a range of reactive power scenarios using both grid control methods. Finally, the AFEs capability to operate as a reactive power compensator is analyzed through the proposed instantaneous energy based DC-bus voltage control strategy and a simplified analytical model for reactive power control. Analytical results demonstrate the PCs ability to regulate both active and reactive power effectively under light-load conditions. These findings are confirmed experimentally on a CERN prototype, where the behavior of the semi-DC-bus voltages, DC-bus voltage harmonics, and overall reactive power performance are validated under light-load operation of the prototype converter. Experimental tests performed on a CERN prototype confirm the effectiveness of the proposed control approach and the AFEs ability to regulate both active and reactive power desirably.

The following chapter investigates interleaved DC/DC converter topologies for the back-end stage of the PC in nuclear fusion and particle accelerator applications, with a comparative analysis of the CDC and SDC configurations. Analytical models are developed to evaluate RMS currents in both configurations, introducing the concept of normalized RMS current to decouple the effect of load contribution currents in the CDC case. Numerical validation of HB currents and variation of RMS currents in both the configurations at distinct gain ratios are performed. The study is then extended to include non-ideal inductor characteristics and possible output voltage deviations under coupled load coil conditions in the interleaved HB section. Moreover, a comparison of total losses in both the CDC and SDC configurations are made and validated through numerical analysis. An algorithm for automatic topology selection is proposed and demonstrated through illustrative design cases and validated with numerical simulations. The chapter concludes with experimental verification of the non-zero frequency component of the RMS current in CDC configurations with two different parallel HB setups, as this is a core component of the proposed algorithm. Additionally, HB currents are experimentally validated to assess potential waveform deviations caused by circulating currents.

Finally, the thesis concludes by summarizing its main contributions and outlining potential directions for future research.

4.2 Perspectives

Future research can address the remaining gaps and extend the original developments presented in this thesis. Firstly, in the context of AFE operation as a reactive compensator, providing feedback on

reactive power at the PCC could improve control effectiveness. Given that the magnitude of neutral point current varies with reactive power, it could serve as a limiting factor in AFE operation for reactive power compensation. Regarding the investigation of the generic number of parallel HBs, and the effect of circulating current in a CDC configuration, future work could extend these findings to other two-quadrant configurations such as buck and boost converters. Additionally hardware-based solution such at utilizing the common-mode chokes at the output of HBs could be investigated to mitigate the effect of circulating current on individual HBs.

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