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MULTI-MHZ ISOLATED RESONANT DC-DC CONVERTERS IN WIDE-BANDGAP TECHNOLOGY

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Abstract

Modern electronic systems demand compact, portable, and energy-efficient power supplies, yet converter size is often dominated by passive components – especially inductors and transformers. Increasing the switching frequency reduces the energy storage requirements and thus the dimensions of the magnetic components. However, hard-switching losses scale with frequency and can dominate at multi-MHz frequency ranges, degrading efficiency and reliability. Resonant topologies that achieve zero-voltage switching (ZVS) mitigate these losses and allow higher operating frequencies. Concurrently, Wide-Bandgap (WBG) devices such as gallium nitride (GaN) and silicon carbide (SiC) – offering higher breakdown field, lower parasitics and on-resistance, and higher allowable junction temperatures – further enable high-frequency, high-power-density operation.

This thesis investigates the design, modelling, and control of isolated dc-dc converters operating in the multi-MHz regime and using Wide-Bandgap devices.

A 140 W, 12 MHz isolated Class EF_2 dc-dc converter with an air-core PCB transformer is demonstrated, achieving 80.8% peak efficiency. A parasitic-aware workflow is detailed, comprising full PCB layout parasitic extraction via electromagnetic simulation to construct a lumped equivalent model of the converter that accurately predicts performance and detuning due to parasitics. Although such parasitics are often negligible in conventional converters, in the multi-MHz regime they become comparable to nominal component values and can be a primary source of detuning and loss related to circulating ac currents; their explicit inclusion enables accurate prediction of behaviour and mitigates the need for post-fabrication retuning. The model is validated against VNA S-parameter measurements, showing close agreement across the relevant frequency range. In addition, a first-harmonic-approximation model is derived to obtain the dc-dc voltage gain as a function of switching frequency, establishing frequency modulation as an effective means of output voltage regulation under load and input voltage variations and providing a basis for closed-loop control.

The design of a Class E^2 push-pull isolated dc-dc converter operating at 5 MHz and delivering 260 W (36 V, 7 A) using a high-frequency ferrite-cored transformer is also carried out, achieving 90% efficiency. MCU-based closed-loop control via frequency modulation over 5-7 MHz, with duty-cycle adjustment to maintain ZVS, is demonstrated on the same converter. A practical implementation framework is established by estimating the control-to-output transfer function from simulated time-domain step responses, enabling model-based controller tuning. The implemented closed-loop control achieves output-voltage regulation with a recovery time below 200 μs and maintains approximately 90% efficiency over a wide load range (from 260 W down to 35 W). It further enables operation in regions where open-loop control would fail due to increased device dissipation. A qualitative analysis is presented to investigate the origin of the right-half-plane (RHP) zero in the control-to-output transfer function, which limits the maximum achievable bandwidth. The analysis suggests that adopting a finite input-inductor design can eliminate the RHP zero and thereby enable a higher control bandwidth.

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Acronyms

ADC Analog to Digital Converter

ADS Advanced Design Systems

CAD Circuit Aided Design

DCT Drain Current Transients

EM Electro-Magnetic

FHA First Harmonic Approximation

GaN Gallium Nitride

HEMT High Electron Mobility Transistor

HF High Frequency

HRTIM High-Resolution Timer

HV High Voltage

IMN Input matching network

ISR Interrupt Service Routine

LTI Linear Time Invariant

MFA Multifrequency Averaging

MN Matching Network

MOS Metal Oxide Semiconductor

OMN Output Matching Network

PCB Printed Circuit Board

PID Proportional Integral Derivative

RF Radio-Frequency

Si Silicon

SiC Silicon Carbide

SMPS Switch Mode Power Supply

THD Total Harmonic Distortion

VNA Vector Network Analyzer

ZDS Zero Derivative Switching

ZOH Zero-Order Hold

ZVDS Zero Voltage Derivative Switching

ZVS Zero Voltage Switching

Chapter 1

Introduction

Nowadays, electronics pervades every aspect of daily life – from household appliances and smart TVs to mobile phones and computers. The growing importance of electronics is accompanied by an ever-increasing demand for compactness, portability, and energy efficiency, particularly in consumer electronics and other space-constrained applications. A substantial portion of the cost and size of modern electronic systems is tied to the power supplies necessary for their operation. Power conversion stages rely on passive components (capacitors, inductors, and transformers) whose dimensions often dominate the overall converter volume, especially the inductors. Addressing miniaturisation in power-electronic circuits therefore calls for design methods and technologies that reduce energy-storage requirements.

One approach to shrinking converter size is to raise the switching frequency, as the required values of passive components in switch-mode converters scale approximately inversely with the switching frequency. Furthermore, air-core transformers and inductors become promising alternatives to their cored counterparts. In addition to eliminating core losses, they offer the added benefit of being embeddable into the printed circuit board (PCB), significantly reducing costs, weight, and overall volume [9].

In hard-switched converters, the switching frequency is limited by switching losses associated with finite device transition times. These losses grow roughly in proportion to the operating frequency and become the dominant dissipation mechanism at high frequency. Thus, while increasing frequency tends to reduce size, it also degrades efficiency, an unacceptable trade-off in practice, as higher dissipation elevates operating temperature, increases failure probability (reducing reliability), and drives up cooling cost and volume [10].

A well-established solution is to employ resonant converters that achieve zero-voltage switching (ZVS), enabling operation at elevated switching frequencies while maintaining high efficiency. Compared with hard switching, resonant operation substantially reduces turn-on/turn-off losses, allowing the frequency increases needed for miniaturisation.

In addition to resonant topologies, the availability of wide-bandgap (WBG) semiconductor devices such as gallium nitride (GaN) and silicon carbide (SiC) has further enabled high-frequency, high-efficiency operation [1]. These devices outperform silicon in maximum operating temperature, switching speed, and achievable power density. Owing to their higher critical electric field, WBG devices can be smaller than silicon counterparts for the same breakdown voltage. They also support higher operating temperature – reducing heat-sinking requirements – and exhibit lower conduction losses at a given breakdown rating due to reduced on-resistance. Their use in power converters therefore allows simultaneous reductions in size and cost while preserving high efficiency. GaN devices are particularly well-suited for multi-MHz applications thanks to low parasitic capacitances.

This chapter provides a brief introduction to wide-bandgap (WBG) devices, resonant converters, and common zero-voltage-switching (ZVS) topologies for multi-MHz operation. The thesis objectives and outline are also presented.

1.1 Wide-Bandgap Semiconductor Devices

The miniaturisation of power electronics is enabled by the availability of new semiconductor technologies that allow higher switching frequencies without compromising efficiency. Silicon power devices are approaching a performance plateau, and further improvements tend to be incremental and costly in terms of R&D and manufacturing complexity. Over the last decade, attention has shifted to wide-bandgap (WBG) semiconductors, which surpass silicon in maximum operating temperature, achievable power density, operating frequency, and voltage capability [1].

The impact of semiconductor material on device behaviour can be assessed by considering the well-known *Baliga Figure of Merit* (BFOM) [5],

$$\text{BFOM} \;=\; \mu\,\varepsilon\,E_{\text{BD}}^{3}, \tag{1.1}$$

where $\varepsilon = \varepsilon_0\varepsilon_r$ is the semiconductor permittivity, E_{BD} the breakdown electric field, and μ the electron mobility.

This FOM enables comparison among semiconductor materials, since the device conduction specific on-resistance R_{on} can be expressed as

$$R_{\text{on}}A \;=\; \frac{4V_{\text{BD}}^2}{\mu\,\varepsilon\,E_{\text{BD}}^3}, \tag{1.2}$$

with V_{BD} the breakdown voltage and A the device area. From the above, a larger BFOM implies a lower $R_{\text{on}}A$ at a given breakdown voltage and, consequently, higher conduction efficiency [5].

Normalising the BFOM of silicon to unity and comparing it with wide-bandgap (WBG) materials such as silicon carbide (SiC) and gallium nitride (GaN) shows *orders-of-magnitude* improvements. In particular, GaN's breakdown field is roughly an order of magnitude higher than silicon [6, 11], yielding a BFOM that is larger by hundreds of times, implying that, within the drift-region limit and for the same V_{BD}, the specific on-resistance $R_{\text{on}}A$ can be lower by a similarly large factor.

The higher E_{BD} in WBG materials stems from their larger bandgap E_g, which measures the energy required to move electrons from the valence to the conduction band. A larger E_g generally correlates with a higher breakdown field, enabling smaller device dimensions for the same voltage rating and, consequently, reduced parasitic capacitances and faster switching.

Another key advantage of a large bandgap is elevated-temperature operation. The intrinsic carrier concentration n_i decreases exponentially with E_g,

$$n_i \propto e^{\left(-\frac{E_g}{2kT}\right)}, \tag{1.3}$$

therefore WBG devices maintain low leakage currents at temperatures where silicon devices would suffer unacceptable leakage. Higher operating temperature eases cooling requirements and can reduce system size and cost by minimising heat-sinking needs.

To illustrate the differences among common semiconductor materials, Table 1.1 compares representative properties and the resulting normalised BFOM.

In summary, WBG semiconductors – and specifically GaN [11] – exhibit highly desirable properties for power devices, including high thermal conductivity, large critical electric field, and high electron mobility. As a result, GaN devices can switch at very high speeds, operate at elevated temperatures (easing cooling requirements), and withstand high voltages and currents. Their use in power converters thus enables higher efficiency, reduced size, and potentially lower cost.

Table 1.1: Representative material properties and normalised Baliga figure of merit (BFOM) [1,5–7]

Property	**Si**	**SiC**	**GaN**
Breakdown electric field E_{BD} [MV/cm]	0.3	3.5	3.0
Electron mobility μ [cm^2/Vs]	1350	900	2000
Bandgap E_g [eV]	1.12	3.26	3.39
Relative dielectric constant ε_r	11.7	9.7	9.5
Bandgap E_g [eV]	1.12	3.26	3.39
Thermal conductivity λ [W/cm K]	1.5	4.5	1.3
Melting point T_m [K]	1690	3103	2400
Electron saturation velocity V_{sat} [10^7cm/s]	1	2	2.5
Normalized BFOM	1	119	537

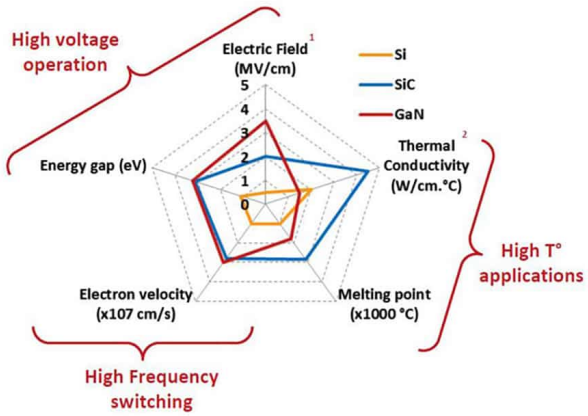

Figure 1.1: Comparison between materials properties [1].

Fig. 1.1 summarises the comparison between the relevant characteristics of GaN, Si and SiC [1].

1.2 Resonant topologies for Multi-MHz Operation

1.2.1 Soft-switching operation

Hard-switching SMPS (switch-mode power supplies) suffer from an inherent frequency limitation related to switching losses. A real power device cannot switch instantaneously between the on- and off-states; this leads to a temporary overlap between the device voltage and current waveforms during the transitions from on to off and vice versa [2,12] (see Fig. 1.2). The device energy loss during a transition can be expressed as

$$W_c^{\mathrm{on/off}} = \tfrac{1}{2}\, I_o V_d\, t_c^{\mathrm{on/off}},$$

where V_d is the device voltage in the off-state, I_o is the device current in the on-state, and $t_c^{\text{on/off}}$ is the effective turn-on/turn-off transition time. The average power dissipated during switching, P_T^{SW} (device switching loss), is therefore [2, 12, 13]:

$$P_T^{\text{SW}} = \tfrac{1}{2}\, I_o V_d \left(t_c^{\text{on}} + t_c^{\text{off}}\right) f_s, \tag{1.4}$$

where f_s is the switching frequency.

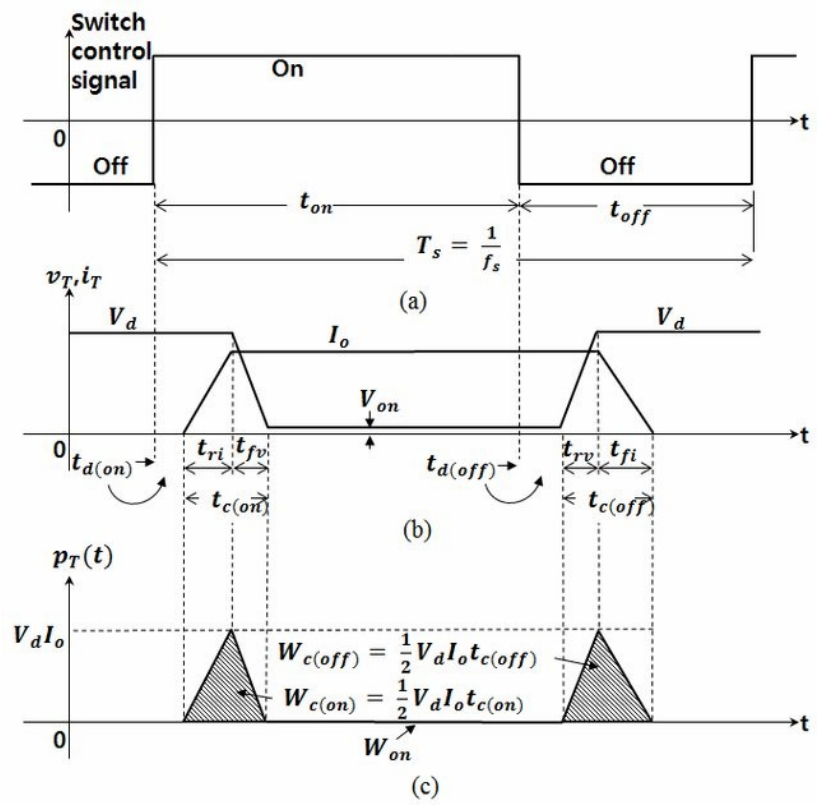

Figure 1.2: Idealised device switching waveforms in an SMPS with finite turn-on and turn-off times [2].

From (1.4), minimising switching losses requires short turn-on and turn-off times. Consequently, faster devices such as GaN transistors can markedly improve efficiency, as their transition times are often several times lower than those of silicon devices. However, when moving from the typical switching frequencies of commercially available GaN converters (often below 200 kHz) into the MHz range, even very fast transitions are no longer sufficient. For example, assuming $V_d = 400\,\text{V}$ and $I_o = 10\,\text{A}$, a 650 V, 30 A GaN device [14] with $t_c^{\text{on}} = 4.9\,\text{ns}$ and $t_c^{\text{off}} = 3.4\,\text{ns}$ yields a switching loss of 3.32 W at $f_s = 200\,\text{kHz}$, rising to a prohibitive loss of 33.2 W at $f_s = 2\,\text{MHz}$.

As a consequence, achieving high efficiency at high switching frequencies generally requires *soft-switching* converters, in which the devices' voltage and current waveforms are shaped to minimise overlap during transitions – thereby reducing switching loss and enabling high-efficiency operation at high power and frequency [2, 12, 15, 16].

In a soft transition, the voltage across the device and/or the current through it is forced to (near) zero before the switching instant, minimising overlap loss:

- **Zero-voltage switching (ZVS):** the device turns on and/or off when the voltage across it is near zero. At turn-on, this requires the device voltage to be brought to zero before the device is turned on; at turn-off, ZVS implies delaying the voltage rise.
- **Zero-current switching (ZCS):** the device turns on and/or off when the current through it is near zero. At turn-on, this implies delaying the current rise; at turn-off, ZCS requires that the device current to be brought to zero before the device is turned off.

Most converter topologies and switching strategies that achieve soft switching rely on LC resonance, hence the broad term *resonant converters* [2]. The most common categories are *resonant-switch* converters and *load-resonant* converters [2, 12, 15]. Resonant-switch converters start from a conventional PWM topology and replace the hard-switched device with a *resonant switch* that incorporates an LC network to enforce ZVS or ZCS; within each switching period, there are resonant and non-resonant intervals, hence the name *quasi-resonant* [2, 12].

Conversely, load-resonant converters employ an LC resonant tank so that the effective load seen by the switches is inductive or capacitive depending on the switching frequency f_s relative to the tank resonance f_r. When $f_s > f_\mathrm{r}$, the effective load is inductive (current lags voltage); when $f_s < f_\mathrm{r}$, it is capacitive (voltage lags current). These phase relations create intervals in which either device voltage or device current is (near) zero; turn-on/off events are then scheduled within those intervals to realise ZVS or ZCS. In such converters, power flow is also controlled via the resonant-tank impedance. In this thesis, the focus is on load-resonant topologies, specifically Class E-derived resonant converters.

An isolated resonant dc-dc converter can be realised by cascading a resonant dc-ac inverter, a high-frequency transformer, and a resonant ac-dc rectifier, as shown in Fig. 1.3.

A classic analysis approach for Class E-based converters is the *fundamental-frequency approximation* (FFA), which assumes that the inverter output current and the rectifier input current are sinusoidal [15, 17, 18]:

- If the rectifier input current is sinusoidal, only the fundamental component transfers power from ac to dc; thus, the rectifier can be replaced by its input impedance

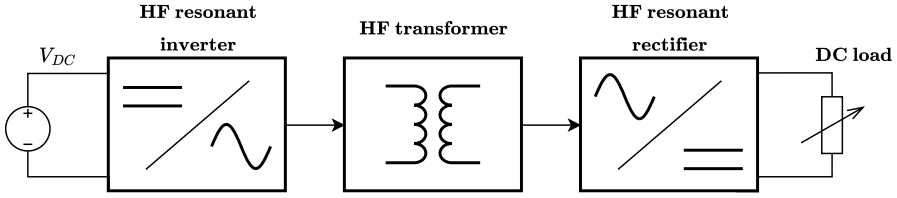

Figure 1.3: General block scheme of an isolated resonant dc-dc converter.

evaluated at the fundamental frequency.

- If the loaded quality factor of the inverter's output tank is sufficiently high and the switching frequency is close to the tank resonance, the resonant inverter forces an (approximately) sinusoidal output current and can be modelled as a sinusoidal current source.

Under these assumptions, the inverter and rectifier can be analysed and designed independently. In this work, following the standard Class E-derived dc-dc design flow [19–21], the rectifier is first replaced by its fundamental-frequency input impedance; the resulting load seen by the inverter is then computed and used to tune the inverter network, as detailed in the relevant sections.

In the following sections, two topologies that are going to be employed throughout this thesis (with variations) are briefly recalled: the Class E and the Class EF_2. Both topologies are often employed in Wireless Power Transfer (WPT) applications.

1.2.2 Class E topology

The Class E ZVS inverter is among the most well-known single-low-side device resonant inverter topologies [17, 18, 22–24]. It enables efficient operation at MHz frequencies, by displacing the switch current and voltage waveforms with respect to time so as to minimise the overlap during the switching intervals, yielding virtually zero switching losses.

The circuit (Fig. 1.4) comprises a single low-side transistor Q_1, a choke inductor L_1, a shunt capacitance C_1 across the switch (which includes the device output capacitance C_{oss}), a series resonant network L_{eq}-C_{s_1}, and the ac load R_{eq}.

By suitable choice of the resonant components, the switch is commanded to turn on when its voltage is zero. In *optimum* operation, the switch voltage $V_{C_1}(\theta)$ satisfies two boundary conditions at the turn-on instant:

$$V_{C_1}(\theta)\Big|_{\theta=2\pi} = 0 \quad \text{(ZVS)}, \qquad \frac{d}{d(\theta)} V_{C_1}(\theta)\Big|_{\theta=2\pi} = 0 \quad \text{(ZVDS)}. \tag{1.5}$$

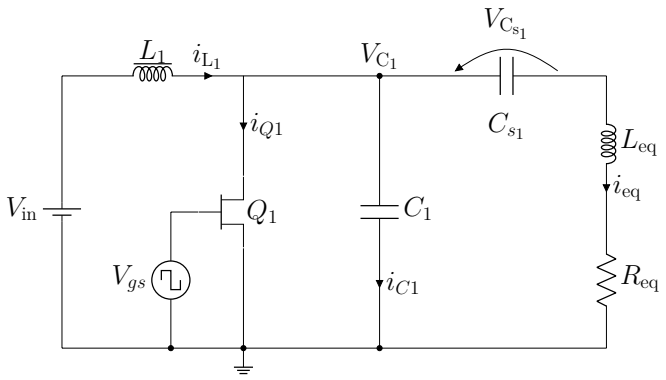

Figure 1.4: Single ended Class E inverter.

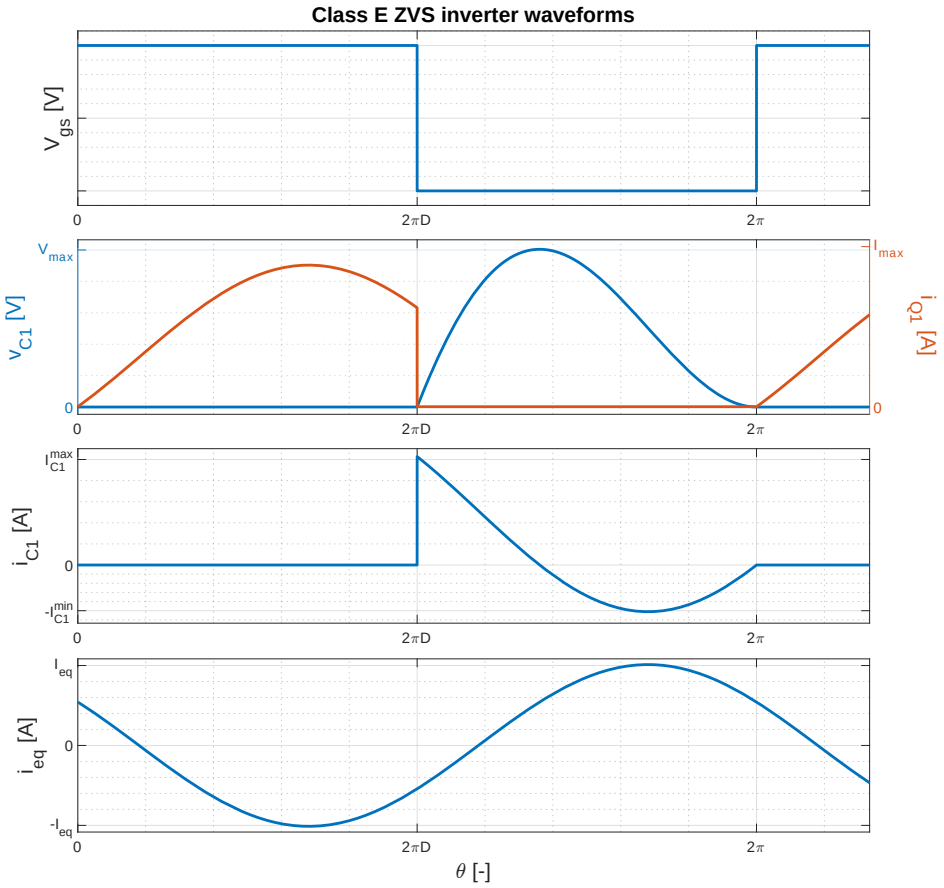

Figure 1.5: Class E ZVS inverter ideal waveforms. D is the switch duty cycle.

The first ensures that the shunt capacitor is fully discharged at turn-on; the second enforces a zero voltage derivative (ZVDS) at turn-on [23,25]. Both ZVS and ZVDS are satisfied simultaneously only at an optimum load R^{opt} [15, 24]. Deviations from the optimum load cause loss of ZVS (if $R_{\text{eq}} > R^{\text{opt}}$), or reverse conduction (if $R_{\text{eq}} < R^{\text{opt}}$).

Fig. 1.5 shows the ideal waveforms of a Class E inverter. Finite choke variations of this circuit exist [23] which trade off filtering requirements with an additional degree of freedom.

The corresponding Class E rectifier, shown in Fig. 1.6, can be obtained from the inverter by applying the time-reversal duality principle, as explained in [26, 27]. The current-driven rectifier [15, 28, 29] consists of a diode D_1, the output filter $L_1 - C_{\text{out}}$ (which ensures the output ripple stays below a certain level) and a shunt capacitance C_1 (which includes the diode's junction capacitance). DC power is delivered to the load resistor R_{out}.

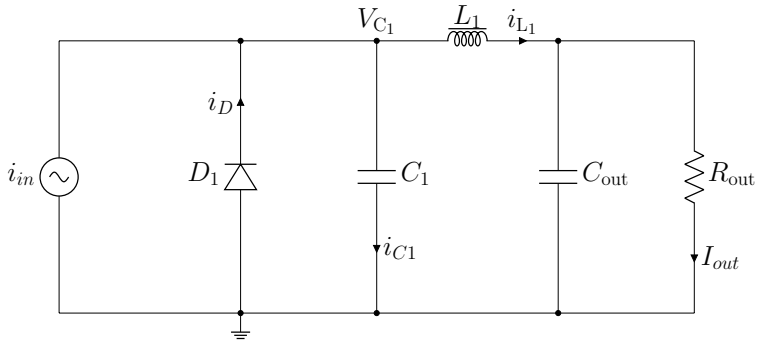

Figure 1.6: Single ended Class E rectifier.

Fig. 1.7 shows the ideal waveforms of the single ended Class E rectifier.

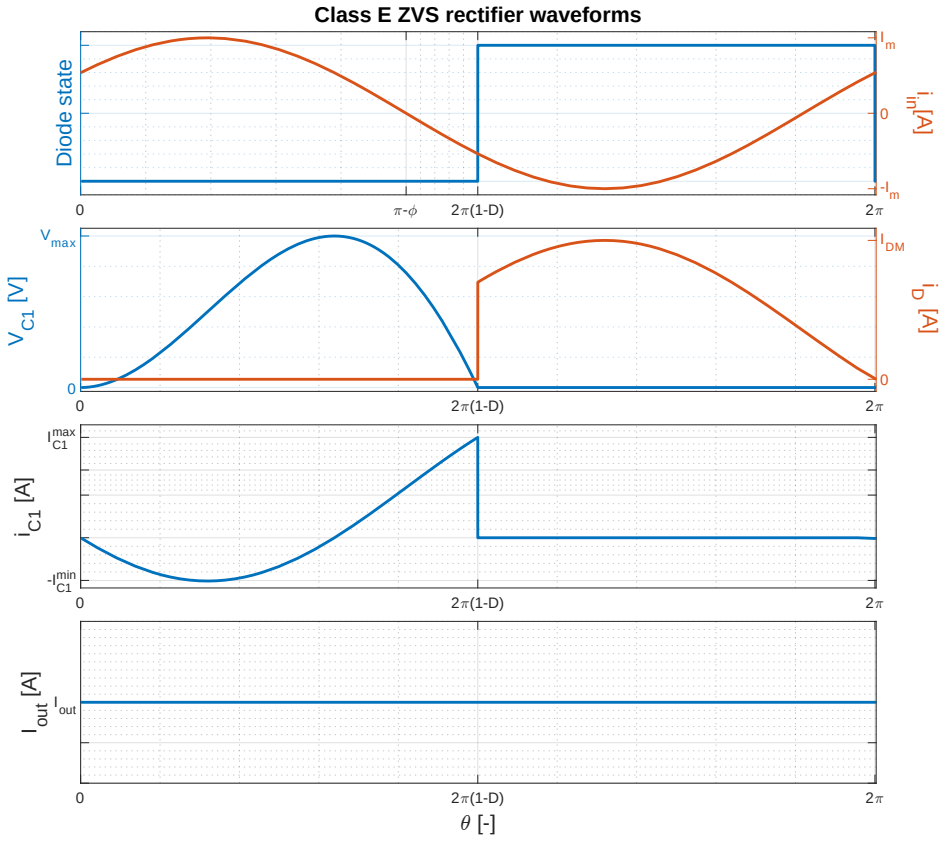

Figure 1.7: Class E rectifier ideal waveforms. D is the duty cycle of the diode and ϕ is the phase angle of the input current.

1.2.3 Class EF_2 topology

The main drawback of the Class E topology is the high voltage stress on the switching device, with the peak voltage reaching approximately 3.6 times the input voltage [25]. To address this, a series LC branch tuned to the second harmonic of the switching frequency can be added in parallel with the device [17,30]. By suppressing the second harmonic, the drain voltage waveform approximates a square wave, reducing the stress to about 2.5 times the input voltage. This modified configuration is known as the Class EF_2 inverter, shown in Fig. 1.8 and analysed in [17,31–33]. The circuit diagram

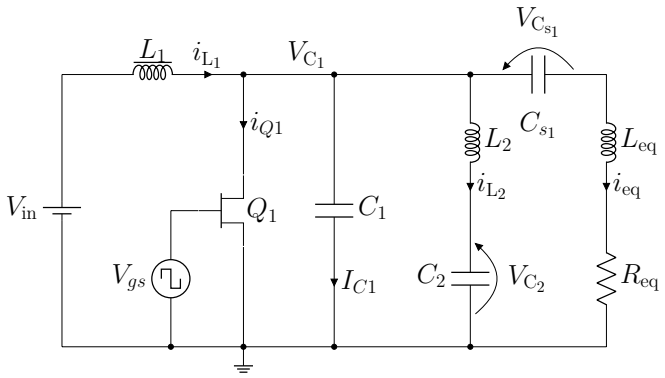

Figure 1.8: Class EF_2 inverter.

of an ideal Class EF_2 inverter consists of an input choke inductor L_1, a low-side switch Q_1, and a shunt capacitor C_1 (including the device output capacitance C_{oss}); the parallel resonant ϕ-branch network $L_2 - C_2$ tuned to the second harmonic of the switching frequency; and the output tank L_{eq}-C_{s1}. Power is delivered to the ac load R_{eq}.

A state-space (SS) description of the inverter, based on [31], is provided here. A SS representation is a compact way of writing the differential equations that describe the behaviour of a system [12,34]. It consists in expressing the derivatives $\dot{q}_i$ of the state variables q_i (inductor currents and capacitor voltages) as linear combinations of the independent inputs u_i and of the state variables themselves. The derivatives of the state variables are proportional to the inductor voltages and the capacitor currents,

respectively. Applying KVL and KCL to the circuit in Fig. 1.8 yields:

$$\begin{cases} \dot{i_{\mathrm{L_1}}} = \frac{V_{\mathrm{in}} - V_{\mathrm{C_1}}}{\omega L_1} \\ \dot{v_{\mathrm{C_1}}} = \frac{i_{\mathrm{L_1}} - \frac{V_{\mathrm{C_1}}}{R_{\mathrm{sw}}^{ON/OFF}} - i_{\mathrm{L_2}} - i_{\mathrm{L_{eq}}}}{\omega C_1} \\ \dot{i_{\mathrm{L_2}}} = \frac{V_{\mathrm{C_1}} - V_{\mathrm{C_2}}}{\omega L_2} \\ \dot{v_{\mathrm{C_2}}} = \frac{i_{\mathrm{L_2}}}{\omega C_2} \\ \dot{v_{\mathrm{C_{s_1}}}} = \frac{i_{\mathrm{L_{eq}}}}{\omega C_{s_1}} \\ \dot{i_{\mathrm{L_{eq}}}} = \frac{V_{\mathrm{C_1}} - V_{\mathrm{C_{s_1}}} - R_{\mathrm{eq}} i_{\mathrm{L_{eq}}}}{\omega L_{\mathrm{eq}}} \end{cases} \tag{1.6}$$

From 1.6, the piece-wise state-space representation of the inverter is given by

$$\dot{\mathbf{q}}(\theta) = \mathbf{A}\mathbf{q}(\theta) + \mathbf{B}u(\theta) \tag{1.7}$$

where $\theta = \omega t$, u is the unit step function, $\mathbf{q}(\theta)$ is the state vector

$$\mathbf{q}(\theta) = \begin{bmatrix} i_{\mathrm{L_1}}(\theta) & V_{\mathrm{C_1}}(\theta) & i_{\mathrm{L_2}}(\theta) & V_{\mathrm{C_2}}(\theta) & V_{\mathrm{C_{s_1}}}(\theta) & i_{\mathrm{L_{eq}}}(\theta) \end{bmatrix}^T \tag{1.8}$$

and $\mathbf{A}$ and $\mathbf{B}$ are defined as follows:

$$\mathbf{A}_{\mathrm{ON/OFF}} = \frac{1}{\omega} \begin{bmatrix} 0 & -\frac{1}{L_1} & 0 & 0 & 0 & 0 \\ \frac{1}{C_1} & -\frac{1}{C_1 R_{\mathrm{sw}}^{ON/OFF}} & -\frac{1}{C_1} & 0 & 0 & -\frac{1}{C_1} \\ 0 & \frac{1}{L_2} & 0 & -\frac{1}{L_2} & 0 & 0 \\ 0 & 0 & \frac{1}{C_2} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{C_{\mathrm{s_1}}} \\ 0 & \frac{1}{L_{\mathrm{eq}}} & 0 & 0 & -\frac{1}{L_{\mathrm{eq}}} & -\frac{R_{\mathrm{eq}}}{L_{\mathrm{eq}}} \end{bmatrix} \tag{1.9}$$

$$\mathbf{B} = \begin{bmatrix} \frac{V_{\mathrm{in}}}{\omega L_1} & 0 & 0 & 0 & 0 & 0 \end{bmatrix}^T \tag{1.10}$$

The switch is modelled as a variable resistance $R_{\mathrm{SW}}^{\mathrm{ON/OFF}}$, leading to the piecewise description. Equation (1.7) is solved separately over the two subintervals of the period – $0 \leq \theta < 2\pi D$ (device on) and $2\pi D \leq \theta < 2\pi$ (device off) – with D the duty cycle. The solutions are

$$\begin{aligned} \mathbf{q}_{\mathrm{ON}}(\theta) &= \mathrm{e}^{\theta \mathbf{A}_{\mathrm{ON}}} \mathbf{q}_{\mathrm{ON}} + \mathbf{A}_{\mathrm{ON}}^{-1} \left(\mathrm{e}^{\theta \mathbf{A}_{\mathrm{ON}}} - I \right) \mathbf{B}, \qquad 0 \leq \theta < 2\pi D \\ \mathbf{q}_{\mathrm{OFF}}(\theta) &= \mathrm{e}^{(\theta - 2\pi D) \mathbf{A}_{\mathrm{OFF}}} \mathbf{q}_{\mathrm{OFF}} + \mathbf{A}_{\mathrm{OFF}}^{-1} \left(\mathrm{e}^{(\theta - 2\pi D) \mathbf{A}_{\mathrm{OFF}}} - I \right) \mathbf{B}, \qquad 2\pi D \leq \theta < 2\pi \end{aligned} \tag{1.11}$$

In 1.11, $q_{\mathrm{ON/OFF}}$ is obtained by enforcing the boundary continuation conditions at the switching instants – $\mathbf{q}_{\mathrm{ON}}(0) = \mathbf{q}_{\mathrm{OFF}}(2\pi)$ and $\mathbf{q}_{\mathrm{ON}}(2\pi D) = \mathbf{q}_{\mathrm{OFF}}(2\pi D)$ – which can be expressed as follows:

$$\begin{bmatrix} \mathbf{q}_{\mathrm{ON}} \\ \mathbf{q}_{\mathrm{OFF}} \end{bmatrix} = \mathbf{C}^{-1}\,\mathbf{E}$$

$$\mathbf{C} = \begin{bmatrix} \mathbf{I} & -\mathrm{e}^{\left((2\pi(1-D))\,\mathbf{A}_{\mathrm{OFF}}\right)} \\ -\mathrm{e}^{\left(2\pi D\,\mathbf{A}_{\mathrm{ON}}\right)} & \mathbf{I} \end{bmatrix} \tag{1.12}$$

$$\mathbf{E} = \begin{bmatrix} \mathbf{A}_{\mathrm{OFF}}^{-1}\left(\mathrm{e}^{\left(2\pi(1-D)\,\mathbf{A}_{\mathrm{OFF}}\right)} - \mathbf{I}\right)\mathbf{B} \\ \mathbf{A}_{\mathrm{ON}}^{-1}\left(\mathrm{e}^{\left(2\pi D\mathbf{A}_{\mathrm{ON}}\right)} - \mathbf{I}\right)\mathbf{B} \end{bmatrix}. \tag{1.13}$$

where $\mathbf{I}$ is the identity matrix.

Figure 1.9 shows the typical waveforms of the Class EF_2 inverter.

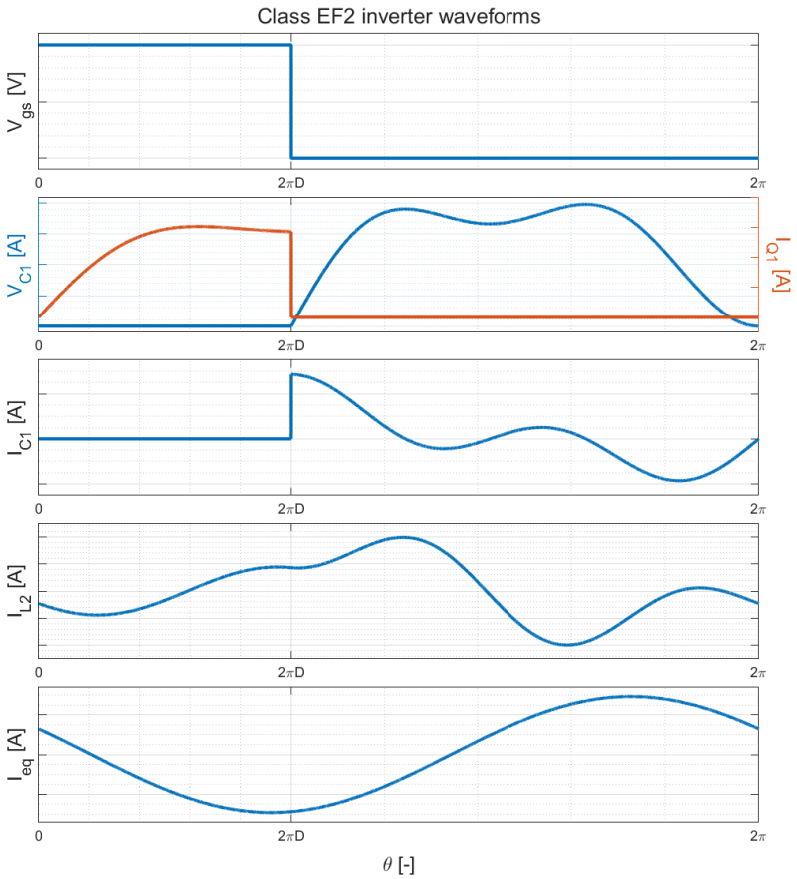

Figure 1.9: Class EF_2 inverter typical waveforms.

As with the Class-E inverter, a version of this circuit with finite input inductance exists, commonly referred to as Class-Φ_2 [35, 36].

1.3 This Work

1.3.1 Objectives

This thesis investigates the design, modelling, and control of isolated dc-dc converters operating in the multi-MHz regime and using Wide-Bandgap devices.

First, it proposes a design workflow for converters operating in this frequency range that incorporates full PCB layout parasitic characterisation and modelling; unlike typical converters operating near 100 kHz – where parasitics are often negligible – at multi-MHz frequencies they can cause detuning and performance degradation. Consequently, their identification is essential to determine whether they can be absorbed into the design or minimised through layout modifications. This characterisation enables more accurate performance prediction and reduces the need for post-fabrication retuning.

A further aim is to demonstrate the practical limits and feasibility of multi-MHz dc-dc conversion in the presented prototypes and to delineate domains where technological or topological changes (e.g., magnetic materials, board materials/stack-up, circuit topology) appear most promising for additional performance gains.

Finally, the work seeks to demonstrate closed-loop controllability of a multi-MHz converter using a general-purpose STM32 platform by developing a reproducible controller-design workflow based on model-based tuning and system identification, and to discuss hardware limitations that arise when employing a general-purpose MCU for high-frequency control.

1.3.2 Thesis Outline

The thesis is organised as follows:

- **Chapter 2** describes the design of a 12 MHz isolated dc-dc converter employing an air-core transformer. Frequency modulation with coordinated duty-cycle adjustment to maintain ZVS is investigated and validated.
- **Chapter 3** presents the design of a 5 MHz isolated dc-dc converter using a high-frequency ferrite-core transformer, including magnetic design trade-offs.

- **Chapter 4** details the framework for developing a closed-loop control algorithm for output-voltage regulation of the converter designed and analysed in Chapter 3, including system identification, controller implementation, limitations, and experimental results.
- **Chapter 5** concludes the thesis and outlines directions for future work.

Funding and Collaboration Statement

This work was sponsored and carried out in collaboration with STMicroelectronics, under the supervision of Dr. Roberto La Rosa and Ing. Natale Aiello.

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Chapter 2

Design of a Class EF_2-based DC-DC converter with integrated PCB air-core transformer

Multi-MHz operation, enabled by modern Wide Band-Gap (WBG) semiconductor devices, offers an effective path toward achieving high power density in power supplies. At these frequencies, printed circuit board (PCB) air-core transformers emerge as a practical alternative to conventional magnetic-core transformers, providing advantages in weight and size reduction, cost, and manufacturing repeatability.

This chapter presents the design of a 12 MHz GaN-based isolated dc-dc converter employing a Class EF_2 inverter. Galvanic isolation between the high-frequency (HF) inverter stages is realised using a PCB-integrated air-core transformer.

A possible target application of this converter is the HF dc-dc stage of an ac-dc converter for wall charging applications. In the complete system, shown in Fig. 2.1, the HF dc-dc stage is preceded by a front-end Power Factor Correction (PFC) and mains rectification block. In typical boost-based PFC designs, the input dc voltage to the dc-dc converter exceeds 350 V dc for 230 V rms distribution networks [37], necessitating an intermediate step-down dc-dc conversion due to the 650 V rating of commercially available GaN devices. Alternatively, a buck-based PFC topology could be employed. Whereas, for 120 V rms distribution networks the input dc voltage remains within the safe operating area of GaN devices [38]. The Class EF_2 topology was selected for the inverter stage due to its suitability for high-voltage operation compared to Class E inverters.

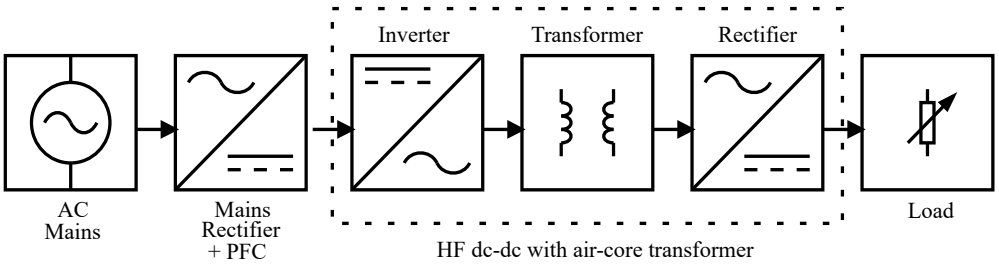


Figure 2.1: Block diagram of the ac-dc converter system for wall charging applications.

This chapter is organised as follows. First, the comprehensive design process of the multi-resonant power stage is outlined, followed by a simulated analysis of the air-core transformer. The experimental prototype is then presented, along with practical design considerations addressing the impact of PCB parasitics on efficiency. Next, output voltage regulation through frequency control is demonstrated and shown to be effective across a wide range of input voltages and loads, where open-loop operation fails. Zero Voltage Switching (ZVS) is also achieved under these conditions. Finally, a First Harmonic Approximation (FHA) model is used to derive the converter's dc-dc voltage gain as a function of switching frequency.

2.1 Power Stage Design

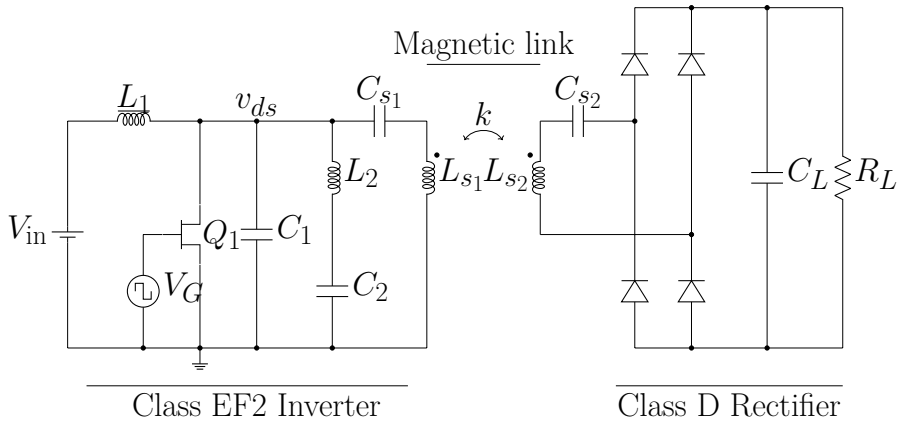


Figure 2.2: Circuit diagram of the proposed dc-dc converter.

The circuit diagram of the designed HF dc-dc converter is shown in Fig. 2.2. A passive full-bridge Class D rectifier, implemented with SiC Schottky diodes, was selected for the rectification stage for its simplicity. Isolation is achieved through the magnetic link L_{s_1}-L_{s_2}, designed to maximise the coupling coefficient k. A Class EF2 inverter drives the primary winding, where V_{in} is the dc input voltage, L_1 is the input choke, Q_1 is the device driven by the gate signal V_G, C_1 is the shunt capacitor, L_2-C_2 is the

ϕ-branch, and C_{s_1} and L_{s_1} form the output resonant tank. The secondary resonant tank consist of L_{s_2} and C_{s_2} in series, C_L is the output filter capacitor, and R_L is the dc load.

Following an RF-inspired workflow rather than a conventional power-converter approach, the design begins by evaluating the rectifier's input impedance at the fundamental frequency. This impedance is then referred to the primary side of the transformer, providing the equivalent load seen by the inverter. Based on this equivalent load, the Class EF_2 inverter is designed. The following paragraphs describe each step in detail.

2.1.1 Rectifier input impedance

At the fundamental frequency, the current driven full-bridge class D rectifier, can be modelled as an equivalent input impedance $\overline{Z}_{\mathrm{in_{rect}}}$, as shown in Fig. 2.3:

$$\overline{Z}_{\mathrm{in_{rect}}} = R_{\mathrm{in_{rect}}} + \mathrm{j}X_{\mathrm{in_{rect}}} = R_{\mathrm{in_{rect}}} - \mathrm{j}\frac{1}{\omega C_{\mathrm{in_{rect}}}} \tag{2.1}$$

where $X_{\mathrm{in_{rect}}}$ is the input reactance, $R_{\mathrm{in_{rect}}}$ is the input resistance, $C_{\mathrm{in_{rect}}}$ is the input capacitance, $\mathrm{j} = \sqrt{-1}$, and ω is the angular frequency.

At MHz frequencies the junction capacitance of the diodes (C_j) is non-negligible and effectively turns the operation of the rectifier into Class DE.

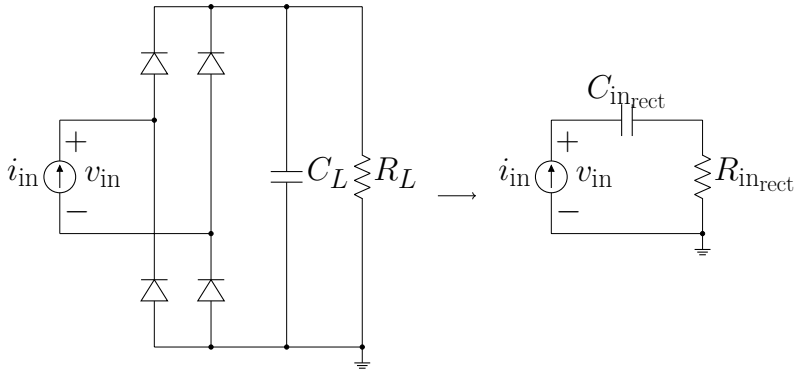


Figure 2.3: HF current-driven Class D rectifier and equivalent input impedance at the operating frequency.

Assuming that the rectifier is driven by a sinusoidal current source $i_{\mathrm{in}} = I_{\mathrm{in}} \sin \omega t$, where I_{in} is the input current amplitude and t is the time, the equivalent input impedance of the rectifier is given by [39, 40]:

$$\overline{Z}_{\mathrm{in_{rect}}} = \frac{\sin^2 \phi + \mathrm{j}\left(\sin \phi \cos \phi - \phi\right)}{\pi \omega C_j} \tag{2.2}$$

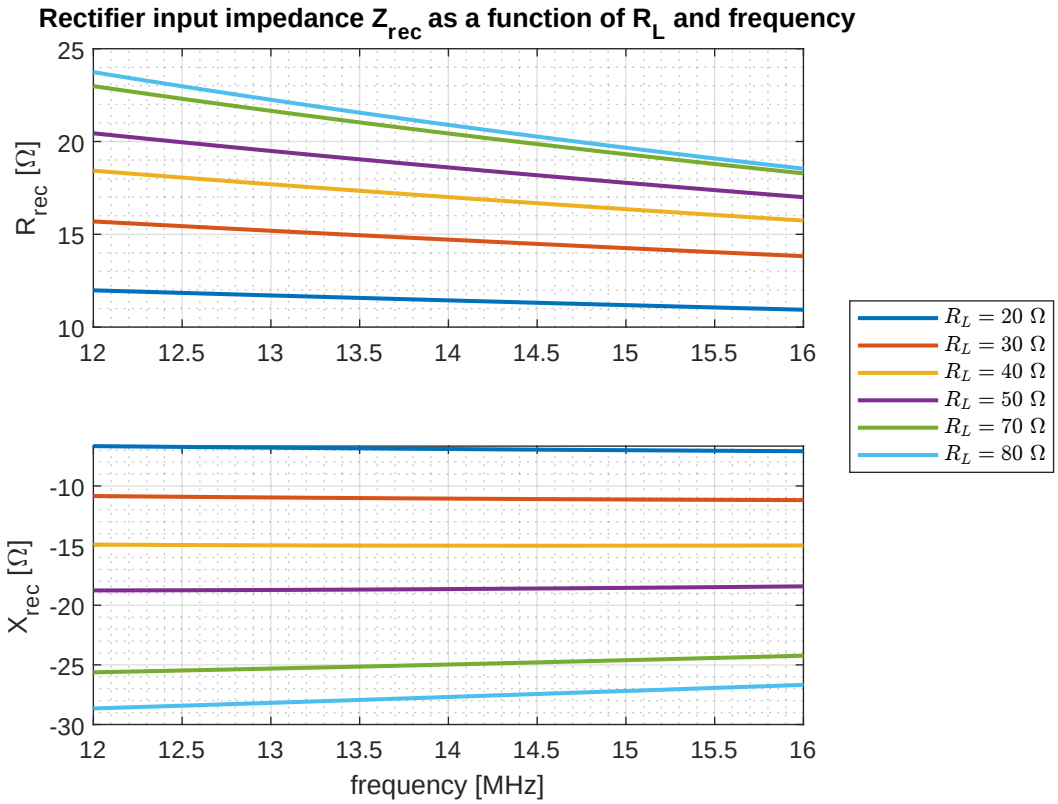


Figure 2.4: Class D rectifier input impedance $\overline{Z}_{\text{in}_{\text{rect}}}$ as a function of frequency f and DC load R_L. It is assumed $C_j = 170\,\text{pF}$.

$$\phi = \arctan\left(2\frac{\sqrt{\pi\omega C_j R_L}}{\pi - \omega C_j R_L}\right). \tag{2.3}$$

where C_j is the junction capacitance of the diodes and ϕ is the phase delay between input current i_{in} and input voltage v_{in}.

Fig. 2.4 shows the Class D full bridge rectifier input impedance $\overline{Z}_{\text{in}_{\text{rect}}}(f, R_L)$ as a function of frequency and DC load R_L.

2.1.2 Reflected impedance

As previously discussed, the rectifier input impedance at the fundamental frequency is used to determine the equivalent impedance of the link referred to the primary side, denoted as $\overline{Z}_{\text{eq}}$, which serves as the load for the inverter.

The equivalent circuit of the coupled inductors L_{s_1} and L_{s_2}, together with the secondary-side compensation capacitor C_{s_2} and the rectifier input impedance, is shown in Fig. 2.5. R_{s_1}, R_{s_2} are the primary and secondary series parasitic resistances. The mutual coupling is represented by the induced voltages jI_1X_M and $-jI_2X_M$, where X_M denotes

the reactance associated with the mutual inductance M, given by:

$$X_M = k\sqrt{X_{L_{s_1}} X_{L_{s_2}}}. \tag{2.4}$$

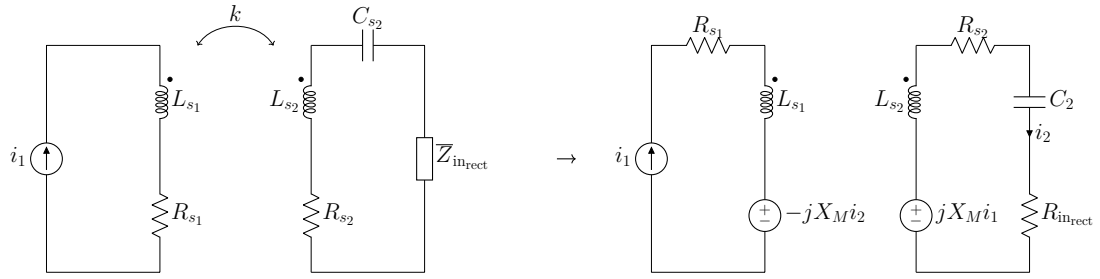


Figure 2.5: Circuit diagram of the converter ac equivalent (left). The rectifier is represented by the equivalent input impedance $\overline{Z}_{\text{in}_{\text{rect}}}$ and the inverter by the current source i_1. Equivalent circuit of the link for reflected input impedance $\overline{Z}_{\text{eq}}$ calculation (right).

In (2.4), $X_{L_{s_1}}$ and $X_{L_{s_2}}$ are the reactances of the primary and secondary windings, respectively, and k is the coupling coefficient. The capacitor C_2 represents the series combination of the secondary-side compensation capacitor C_{s_2} and the rectifier input capacitance $C_{\text{in}_{\text{rect}}}$, with an equivalent reactance X_2.

$$X_2 = X_{\text{in}_{\text{rect}}} + X_{C_{s_2}} = -\frac{1}{\omega C_2} \tag{2.5}$$

$$C_2 = \frac{C_{\text{in}_{\text{rect}}} C_{s_2}}{C_{\text{in}_{\text{rect}}} + C_{s_2}}. \tag{2.6}$$

Applying KVL to the circuit in Fig. 2.5 leads to the following system:

$$\begin{cases} v_1 = R_{s_1} i_1 + jX_{L_{s_1}} i_1 - jX_M i_2, \\ (R_{s_2} + R_{\text{in}_{\text{rect}}}) i_2 + jX_{L_{s_2}} i_2 + jX_2 i_2 = jX_M i_1, \end{cases} \tag{2.7}$$

By solving the second equation of (2.7) for i_2 and substituting it into the first, the equivalent input impedance of the link can be written as

$$\overline{Z}\text{eq} = \frac{v_1}{i_1} = R\text{eq} + jX_{\text{eq}}, \tag{2.8}$$

where

$$R_{\text{eq}} = R_{s_1} + \frac{X_M^2 (R_{\text{in}_{\text{rect}}} + R_{s_2})}{(R_{\text{in}_{\text{rect}}} + R_{s_2})^2 + (X_{L_{s_2}} + X_2)^2} \tag{2.9}$$

and

$$X_{\text{eq}} = X_{L_{s_1}} - \frac{X_M^2 (X_{L_{s_2}} + X_2)}{(R_{\text{in}_{\text{rect}}} + R_{s_2})^2 + (X_{L_{s_2}} + X_2)^2}. \tag{2.10}$$

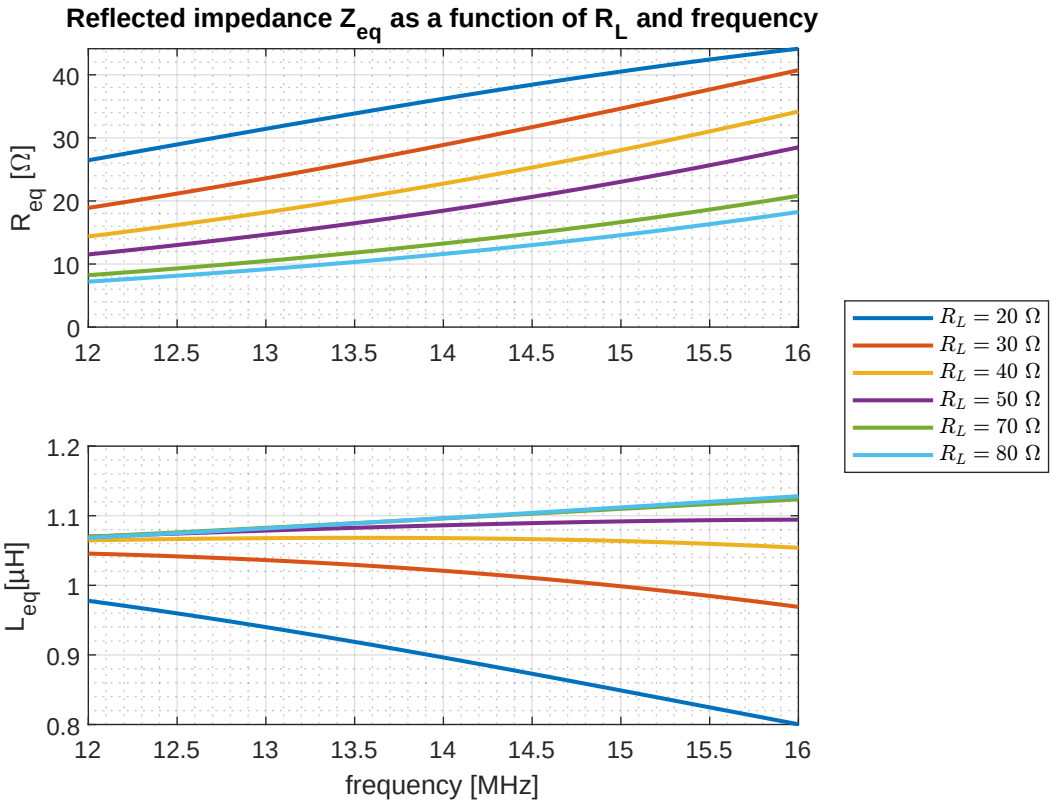


Figure 2.6: Link reflected impedance Z_{eq} as a function of frequency f and DC load R_L. It is assumed $L_{s_1} = 1\,\mu\text{H}$, $L_{s_2} = 150\,\text{nH}$, $k = 0.65$ and $C_{s_2} = 3\,\text{nF}$.

However, since $C_2 \leq \min\{C_{s_2}, C_{\text{in}_{\text{rect}}}\}$, achieving secondary side resonance might not always be feasible for any value of L_{s_2}, which can be constrained by a certain turn ratio as well as a maximum value of inductance to minimise copper losses.

To account for off-resonance operation, it is convenient to introduce a resonance factor γ, defined as the ratio between the secondary side resonant frequency and the operating switching frequency:

$$\gamma = \frac{1}{\omega\sqrt{L_{s_2}C_2}} \qquad \Longrightarrow \; X_2 = -\gamma^2 X_{L_{s_2}} \tag{2.11}$$

Finally, substituting (2.11) and (2.4) into (2.9) and (2.10) yields:

$$R_{\text{eq}} = R_{s_1} + \frac{k^2 X_{L_{s_1}} X_{L_{s_2}} (R_{\text{in}_{\text{rect}}} + R_{s_2})}{(R_{\text{in}_{\text{rect}}} + R_{s_2})^2 + (X_{L_{s_2}}(1-\gamma^2))^2} \tag{2.12}$$

$$X_{\text{eq}} = X_{L_{s_1}} - \frac{k^2 X_{L_{s_1}} X_{L_{s_2}} (X_{L_{s_2}} + X_2)}{(R_{\text{in}_{\text{rect}}} + R_{s_2})^2 + (X_{L_{s_2}}(1-\gamma^2))^2} \tag{2.13}$$

The previous equations represent the link reflected impedance as seen from the primary for a given DC load R_L and frequency f. However, $\overline{Z}_{\text{eq}}(f, R_L)$ depends on both

frequency and load R_L through $\overline{Z}_{\text{in}_{\text{rect}}}$. Fig. 2.6 shows the reflected resistance R_{eq} and the reflected inductance $L_{eq} = \frac{X_{eq}}{\omega}$ for varying load R_L and frequency f.

Fig. 2.7 illustrates R_{eq} and X_{eq} as functions of k and γ, normalised with respect to their values under the secondary-side resonance condition ($\gamma = 1$). The primary loaded quality factor, defined as $Q_L = X_{\text{eq}}/R_{\text{eq}}$ as a function of γ and k is also shown. Q_L is a critical parameter for the inverter design, as it must be sufficiently high to ensure a sinusoidal current in the inverter's output $L - C$ branch [22]. For a given rectifier reflected impedance and switching frequency, a higher coupling coefficient k leads to a lower Q_L. As shown in Fig. 2.7, for a given k, Q_L increases as γ exceeds 1.Conversely, if γ is less than 1, the reflected impedance becomes capacitive, partially cancelling the primary inductance and resulting in a ratio $X_{\text{eq}}/X_{L_{s_1}}$ below 1.

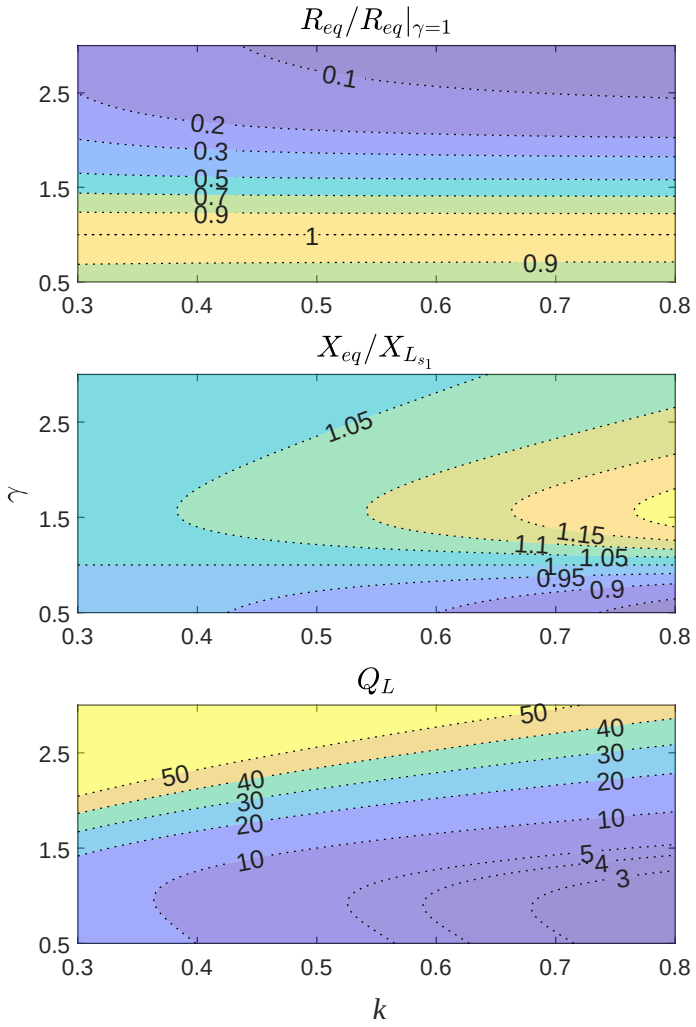


Figure 2.7: Normalised intensity plots, from top to bottom, of R_{eq}, X_{eq} and Q_L as functions of k and γ according to (2.12) and (2.13).

Due to constraints on space and the need to minimise copper losses, the primary and

secondary inductances were fixed at $L_{s_1} = 1\,\mu\text{H}$ and $L_{s_2} = 150\,\text{nH}$, respectively. To maximise transmission efficiency, the coupling coefficient was chosen to be as close as possible to $k \approx 0.7$ (as discussed in the next chapter). Under these conditions, achieving secondary-side resonance at the switching frequency for the nominal load was not feasible without adding an external inductor on the secondary side. Moreover, even if resonance were achieved, the resulting primary loaded quality factor would be $Q < 3$, insufficient to maintain a sinusoidal primary current at the inverter output. Consequently, the converter is intentionally designed to operate off-resonance at the secondary side, in contrast with typical WPT designs. This off-resonance operation has the additional advantage of effectively increasing the inverter's output inductance.

2.1.3 Class EF_2 inverter design

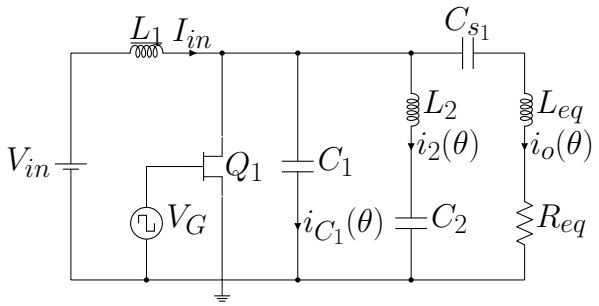


Figure 2.8: Schematic representation of a class EF_2 inverter. R_{eq} and L_{eq} are the reflected input resistance and inductance as seen from the primary side of the transformer.

The last step of the design process is the tuning of the Class EF_2 inverter, following the procedure described in [17, 31–33]. For completeness, a brief description is included here. Figure 2.8 shows the circuit diagram of the inverter. The circuit consists of the input choke L_1, the shunt capacitance C_1 (including the device drain output capacitance C_{oss}), the L_2-C_2 branch forming the second-harmonic trap, and the series capacitor C_{s_1} together with the reflected link impedance $R_{\text{eq}} + j\omega L_{\text{eq}}$, which form the output network.

In contrast to the Class E inverter, where usable closed-form solutions exist, an analytical solution for the Class EF_2 component values exists but it is complex and impractical to use [17,32]. For this reason, the design equations are solved numerically in MATLAB using `fsolve`.

The current $i_2(\theta)$ in the second-harmonic trap is given by [20, 31, 32]:

$$i_2(\theta) = \begin{cases} I_{\text{in}}\Big(A_1\cos(2\theta) + A_2\sin(2\theta)\Big), & 0 \le \theta < 2\pi D, \\ I_{\text{in}}\left(A_3\cos(q_2\theta) + A_4\sin(q_2\theta) - \dfrac{q_2^2 p}{q_2^2-1}\sin(\theta+\phi) + \dfrac{1}{\lambda+1}\right), & 2\pi D \le \theta < 2\pi, \end{cases} \tag{2.14}$$

where $p = I_m/((\lambda{+}1)I_{\text{in}})$, $q_2 = 2\sqrt{\frac{\lambda+1}{\lambda}}$, and $\lambda = C_1/C_2$. ϕ is the phase of the sinusoidal output current $i_o(\theta) = I_m\sin(\theta+\phi)$ with respect to the gate signal. The second equation in (2.14) is obtained from the solution of the differential equation governing the Φ-branch. The coefficients A_1, A_2, A_3, A_4 are found by imposing continuity of current and voltage in correspondence of device turn-on and turn-off:

$$\begin{cases} i_2(2\pi D^-) = i_2(2\pi D^+), \\ \left.\dfrac{di_2}{d\theta}\right|_{\theta=2\pi D^-} = \left.\dfrac{di_2}{d\theta}\right|_{\theta=2\pi D^+}, \\ i_2(0) = i_2(2\pi), \\ \left.\dfrac{di_2}{d\theta}\right|_{\theta=0} = \left.\dfrac{di_2}{d\theta}\right|_{\theta=2\pi}. \end{cases} \tag{2.15}$$

The shunt capacitor current $i_{C_1}(\theta)$ is given by:

$$i_{C_1}(\theta) = \begin{cases} 0, & 0 \le \theta < 2\pi D, \\ I_{\text{in}}\Big(1 - p(\lambda+1)\sin(\theta+\phi)\Big) - i_2(\theta), & 2\pi D \le \theta < 2\pi. \end{cases} \tag{2.16}$$

The drain voltage $v_{DS}(\theta)$ can be expressed as:

$$v_{DS}(\theta) = \begin{cases} 0, & 0 < \theta < 2\pi D, \\ V_{\text{in}}\dfrac{2\pi\int_{2\pi D}^{\theta} i_{C_1}(\xi)\,\mathrm{d}\xi}{\displaystyle\int_{2\pi D}^{2\pi}\int_{2\pi D}^{\theta} i_{C_1}(\xi)\,\mathrm{d}\xi\,\mathrm{d}\theta}, & 2\pi D < \theta < 2\pi. \end{cases} \tag{2.17}$$

Imposing the ZVS condition $v_{DS}(2\pi) = 0$ and the ZDS condition $\left.\frac{dv_{DS}}{d\theta}\right|_{\theta=2\pi} = 0$ gives the following two additional equations:

$$\begin{cases} 2\pi\dfrac{\lambda}{\lambda+1}(1-D) + p\Big(\cos(2\pi D+\phi) - \cos\phi\Big)\left(\dfrac{q_2^2}{q_2^2-1} - (\lambda+1)\right) \\ \quad + \dfrac{A_3}{q_2}\Big(\sin(q_2 2\pi D) - \sin(2\pi q_2)\Big) + \dfrac{A_4}{q_2}\Big(\cos(2\pi q_2) - \cos(q_2 2\pi D)\Big) = 0, \\ \frac{\lambda}{\lambda+1} + p\sin\phi\Big(\frac{q_2^2}{q_2^2-1} - (\lambda+1)\Big) - \Big(A_3\cos(2\pi q_2) + A_4\sin(2\pi q_2)\Big) = 0. \end{cases} \tag{2.18}$$

Equations (2.15) and (2.18) form a system of six equations in six unknowns (A_1, A_2, A_3, A_4, ϕ, λ) that can be solved numerically using `fsolve`.

The input variables for the design are the output power P_{out}, input voltage V_{in}, switching frequency $f = \omega/2\pi$, duty cycle D, AC load R_{eq}, and output inductance L_{eq}. For a given R_{eq} and desired P_{out}, the output current amplitude is:

$$I_m = \sqrt{\frac{2P_{out}}{R_{eq}}}. \tag{2.19}$$

Assuming $P_{out} = P_{in}$, the input current is simply:

$$I_{in} = \frac{P_{out}}{V_{in}}. \tag{2.20}$$

The shunt capacitance C_1 is determined by enforcing that the average drain voltage equals V_{in}:

$$V_{in} = \int_{2\pi D}^{2\pi} \frac{1}{\omega C_1} \int_{2\pi D}^{\theta} i_{C_1}(\xi)\, \mathrm{d}\xi\, \mathrm{d}\theta. \tag{2.21}$$

Then C_2 is given by $C_2 = C_1/\lambda$, and L_2 by:

$$L_2 = \frac{1}{4\omega^2 C_2}. \tag{2.22}$$

Table 2.1: Component values of the dc-dc converter.

Component	Value	Component
L_1	27 µH	Bourns SRR1240-220M
C_1	8 pF	Vishay HighFreq Series 1111
L_2	830 nH	Coilcraft 2929SQ-431 and 2929SQ-391
C_2	42 pF	Vishay HighFreq Series 1111
C_{s_1}	320 pF	Kemet C0G 1812
L_{s_1}	1 µH	-
L_{s_2}	150 nH	-
C_{s_2}	3 nF	Kemet C0G 1206
k	0.65	-

To determine C_{s_1}, only the fundamental component of v_{DS} is considered, since the output current $i_o(\theta)$ is assumed to be nearly sinusoidal. The first-harmonic amplitude and phase of v_{DS} are obtained by Fourier analysis:

$$V_{DS}^1 = \sqrt{\left(\frac{1}{\pi}\int_0^{2\pi} v_{DS}\cos\theta\, d\theta\right)^2 + \left(\frac{1}{\pi}\int_0^{2\pi} v_{DS}\sin\theta\, d\theta\right)^2}, \tag{2.23}$$

$$\psi = \tan^{-1}\frac{\frac{1}{\pi}\int v_{DS}\cos\theta\, d\theta}{\frac{1}{\pi}\int v_{DS}\sin\theta\, d\theta}. \tag{2.24}$$

The phasor of the sinusoidal output current $i_o(\theta) = I_m\sin(\theta+\phi)$, is $\overline{I} = I_m/\sqrt{2}\angle\phi$.

The impedance seen by the drain is then obtained from the phasor ratio:

$$\overline{Z} = \frac{\overline{V}}{\overline{I}} = \frac{V_{DS}^1}{I_m}\angle(\psi - \phi) = R_{\text{eq}} + jX, \tag{2.25}$$

where X is the output tank reactance:

$$X = \omega L_{\text{eq}} - \frac{1}{\omega C_{s_1}}. \tag{2.26}$$

From (2.25) the real and the imaginary parts of the output tank impedance can be expressed as follows:

$$R_{\text{eq}} = \frac{V_{DS}^1}{I_m}\cos(\psi - \phi), \qquad X = \frac{V_{DS}^1}{I_m}\sin(\psi - \phi). \tag{2.27}$$

Finally, C_{s_1} is determined by equating the imaginary part of the impedance $\overline{Z}$ to the reactance of the series branch:

$$X = \omega L_{\text{eq}} - \frac{1}{\omega C_{s_1}} \quad \Longrightarrow \quad C_{s_1} = \frac{1}{\omega\Big(\omega L_{\text{eq}} - X\Big)}. \tag{2.28}$$

The input choke inductance L_1 is chosen so that its impedance is much larger than the input resistance R_{in} of the inverter [21]:

$$L_1 \gg \frac{R_{\text{in}}}{\omega} = \frac{V_{in}}{\omega I_{in}}. \tag{2.29}$$

Figure 2.9: Photograph of the designed dc-dc converter. An extra inductor is shown on the secondary side, added for flexibility in achieving resonance at the switching frequency, but it was not used in the actual prototype.

The final component values and the part numbers for the HF dc-dc power supply are listed in Table 2.1. The design was carried out assuming $P_{out} = 150\,\text{W}$, $f = 13.56\,\text{MHz}$,

$V_{in} = 200\,\mathrm{V}$ and $D = 0.3$. Additional manual tuning was required to account for the device output capacitance C_{oss} in simulation.

The employed transistor is a 650 V, 15 A GaN Enhancement mode High Electron Mobility Transistor (E-HEMT) (GS66504B), driven by the LMG1020 gate driver. Discrete air-core inductors were chosen for the ϕ-branch from Coilcraft.

A photograph of the fabricated prototype is shown in Fig. 2.9. The overall dimensions of the 4-layer PCB board are $9.5{\times}5.5{\times}0.2\,\mathrm{cm}^3$.

2.2 Air-core Transformer Design

As noted earlier, at high switching frequencies the required inductance values decrease significantly, making it feasible to implement them on printed circuit boards (PCB coils). The advantages of using PCB coils as inductors or planar transformers are multiple: (i) reduced cost; (ii) simpler fabrication; and (iii) the ability to realise a wide variety of geometries.

Among the most common PCB magnetic structures are the spiral, solenoidal, and toroidal forms. Both spiral and solenoidal inductors exhibit a significant external magnetic field and therefore tend to be more challenging from an EMI (electromagnetic interference) perspective, often requiring shielding at the product level. By contrast, the toroidal geometry largely confines the magnetic field within the structure [41].

Another important consideration is design flexibility. In this respect, the spiral inductor is generally superior to the other structures: it can be realised on a single copper layer (whereas the others typically require at least two layers), can implement a non-integer number of turns, and allows terminal placement to be optimised for the surrounding circuitry. The toroidal geometry typically exhibits the lowest inductance-per-area among the three, as well as the highest dc and ac resistance; consequently, it tends to have the lowest quality factor Q [8]. Table 2.2 summarises the main advantages and drawbacks of each geometry.

Table 2.2: Comparison between different PCB inductor geometries [8].

Geometry	Advantages	Disadvantages
Spiral	High Q High design flexibility Single layer	High extrernal magnetic field (EMI)
Solenoid	High Q	High extrernal magnetic field (EMI)
Toroid	Confined magnetic field	Low design flexibility Low Q Lowest inductance per-area

In this work, the spiral structure was selected for its higher quality factor and superior design flexibility. Unlike typical WPT applications, the coupled coils constituting the air-core transformer are integrated directly onto the same PCB, as are the High-Frequency (HF) inverter and rectifier. The two spiral inductors are vertically aligned on adjacent PCB layers. Only two layers are strictly required to realise a PCB spiral transformer (although the structure can be made more complex by series/parallel interconnection of spirals, which then requires additional layers). However, using a

four-layer PCB provides greater flexibility for implementing underpasses and for routing the coil terminals to the rest of the circuit. The coils were designed to achieve tight coupling to maximise transfer efficiency [42,43], while keeping the required board space to less than $50\times50\,\mathrm{mm}^2$. The geometric parameters of a spiral PCB transformer are: the number of turns in the primary and secondary (N_p, N_s); trace width w; turn-to-turn spacing s; outer and inner diameters $(d_{\mathrm{out}}, d_{\mathrm{in}})$; copper thickness t; and the dielectric thickness between the two coils d_ε. The magnetic coupling between the two PCB coils increases when the spiral outer diameter is enlarged or when the dielectric thickness between layers is reduced [44, 45]. The former increases the footprint of the transformer, while the latter is limited by the dielectric strength and minimum manufacturable thickness of the substrate.

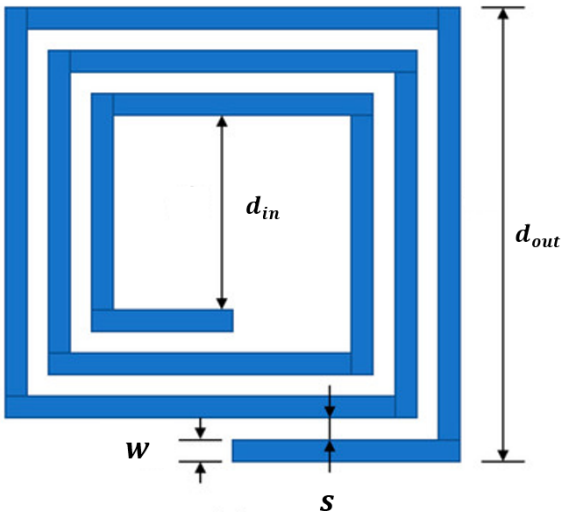


Figure 2.10: Parameters of square spiral inductor.

The primary and secondary inductances of the air-core transformer are 1 µH and 150 nH, respectively, to optimise area occupation on the PCB, maintain a high loaded quality factor in the inverter's output resonant tank, and achieve the desired step-down voltage conversion. This choice results in a turns ratio of approximately 2.5. The PCB air-core transformer was designed with constraints of a maximum area of $40\times40\,\mathrm{mm}^2$ and a target coupling coefficient of 0.7. Square planar spiral coils were selected due to their higher inductance per unit area compared to other spiral geometries (e.g. circular, hexagonal, etc.) [43, 46], as well as their ease of design.

An analytical estimation of the coils' self-inductance was obtained using the formula provided in [46, 47]:

$$L = \frac{1.27\mu_0 N^2 d_{\mathrm{avg}}}{2}\left[\ln\left(\frac{2.07}{\varphi}\right) + 0.18\varphi + 0.13\varphi^2\right] \tag{2.30}$$

where

$$d_{avg} = (d_{out} + d_{in})/2 \tag{2.31}$$

$$\varphi = \frac{d_{out} - d_{in}}{d_{out} + d_{in}}. \tag{2.32}$$

In the previous expressions, N is the number of turns, d_{out} and d_{in} denote the outer and inner diameters of the spiral, respectively. The parameter d_{out} is constrained to be 40 mm. At 12 MHz, the skin depth of copper is approximately 20 µm. Therefore, a copper weight of 2 oz was selected. The spacing s between the turns was set to 0.3 mm – the minimum track-to-track clearance supported by standard PCB fabrication for 2 oz copper – as the self-inductance of a spiral coil is inversely proportional to s [46]. To obtain the desired inductance values, the primary coil was designed with 4 turns and the secondary coil with 1.2 turns, both with a trace width of 1.5 mm. The two square spirals are parallel, concentric, and are located on the first and second copper layers of the PCB, respectively. The dielectric thickness, d_ϵ, separating the primary and secondary coils, was set to 0.5 mm.

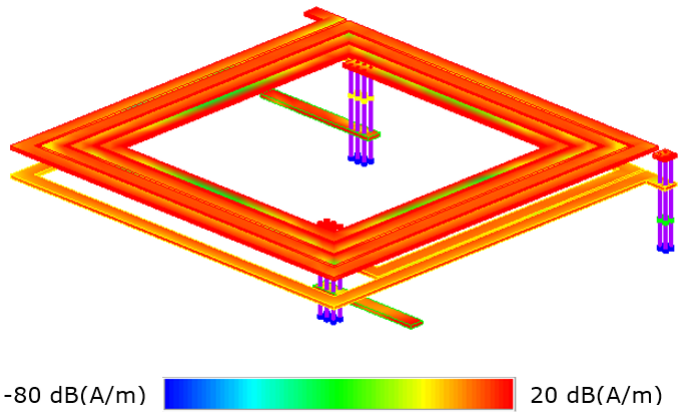


Figure 2.11: Current density simulation of the designed air-core PCB transformer.

The transformer design was carried out using ADS Momentum, a Method of Moments (MoM) 3D planar Electromagnetic (EM) simulator by Keysight Technologies. A 3D rendering of the transformer is shown in Fig. 2.11, with the simulated current distribution. The lumped model of the air-core transformer was extracted from S-parameters obtained via EM simulation of the structure. The S-parameters were first converted to the impedance matrix Z, from which the parameters of the lumped model were computed as follows:

$$L_p = \frac{\Im\{Z(1,1)\}}{\omega}, \qquad L_s = \frac{\Im\{Z(2,2)\}}{\omega}$$

$$R_p = \Re\{Z(1,1)\}, \qquad R_s = \Re\{Z(2,2)\}$$

$$M = \frac{\Im\{Z(1,2)\}}{\omega}, \qquad k = \frac{M}{\sqrt{L_p\, L_s}} \tag{2.33}$$

where $\omega = 2\pi\, f$ is the angular frequency. Fig. 2.12 shows the relevant parameters of the air-core transformer for the definition of its lumped model and the corresponding values are shown in Table 2.3.

Table 2.3: Air-core transformer parameters extracted from EM simulation.

Parameter	**Description**	**Value from EM simulation**
L_p	Primary inductance	994 nH
L_s	Secondary inductance	154 nH
R_p	Primary-side parasitic resistance	0.56 Ω
R_s	Secondary-side parasitic resistance	0.2 Ω
$L_{p_{\mathrm{sc}}}$	Short-circuit primary inductance	557 nH
k	Coupling coefficient	66 %
M	Mutual inductance	260 nH

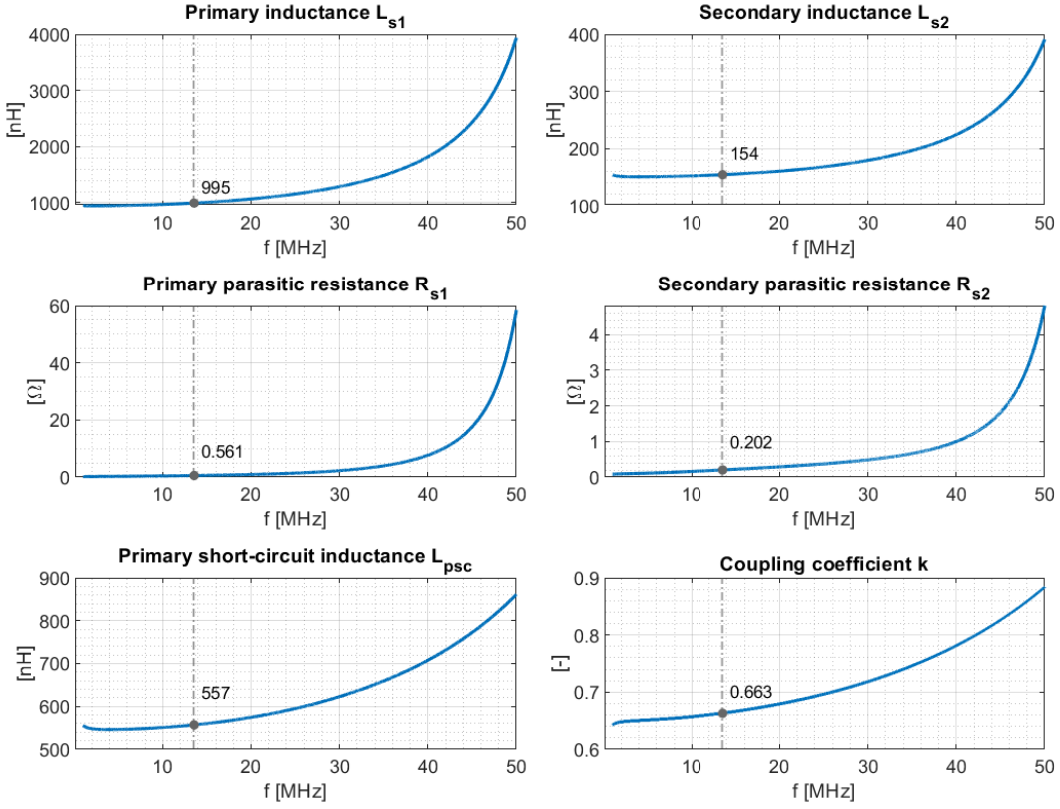
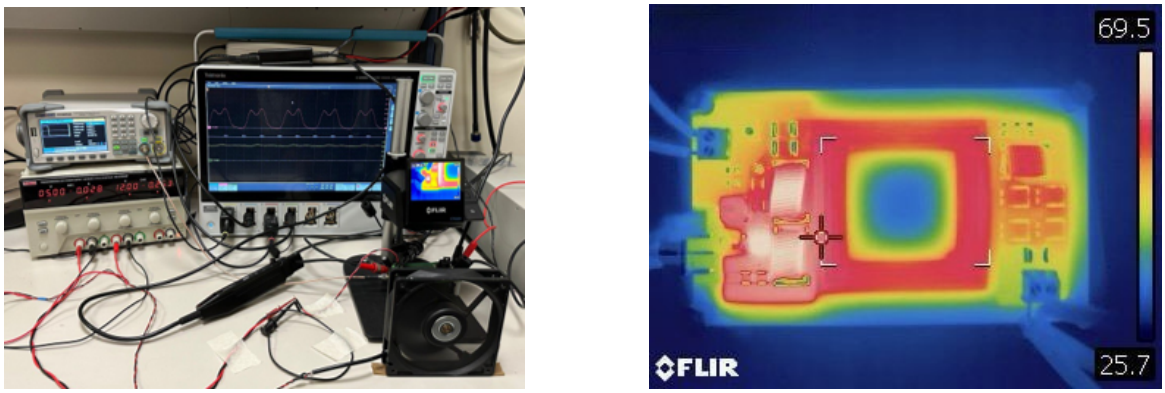


Figure 2.12: Transformer parameters extracted from EM simulation (Momentum ADS Keysight)

2.3 Experimental results

The experimental setup, shown in Fig. 2.13a, consists of two bidirectional power supplies (IT6018C-1500-40) used as source and DC load for the prototype under test. The drain voltage across the switching device was monitored using a high-voltage passive probe (P5100A). The gate signal for the inverter was provided by a SDG6052X AWG. Device temperature was continuously monitored using a thermal camera to ensure safe operating conditions.



(a) Experimental setup.

(b) Thermal camera image.

Figure 2.13: Experimental setup used for the efficiency characterisation of the implemented converter.

Fig. 2.14 shows the measured dc-dc efficiency of the prototype as a function of the output power for an input voltage of 130 V. The load was varied from 20 Ω to 60 Ω. A dc-dc efficiency of 80.8 % is reached at 145 W output power. The output voltage ripple is less than 5% and the estimated power density of the converter is 13.8 W/cm^3.

A thermal image of the implemented converter is shown in Fig. 2.13b .

2.3.1 Impact of PCB layout parasitics

Time-domain simulations of the converter were performed, incorporating the non-linear dynamic models of SiC diodes and GaN transistor, the linear models of the discrete air-core inductors and choke, and the equivalent circuit of the air-core transformer based on the parameters provided in Table 2.3. The results demonstrated a simulated efficiency exceeding 87 %, compared to the measured 80.8 %, as it is shown by the orange markers in Fig. 2.14.

The reason for this difference was found to be non-negligible detuning caused by PCB layout parasitics, which play a critical role in HF Systems' performance. The parasitics that can't be absorbed into the design must be minimised as to reduce the circulating

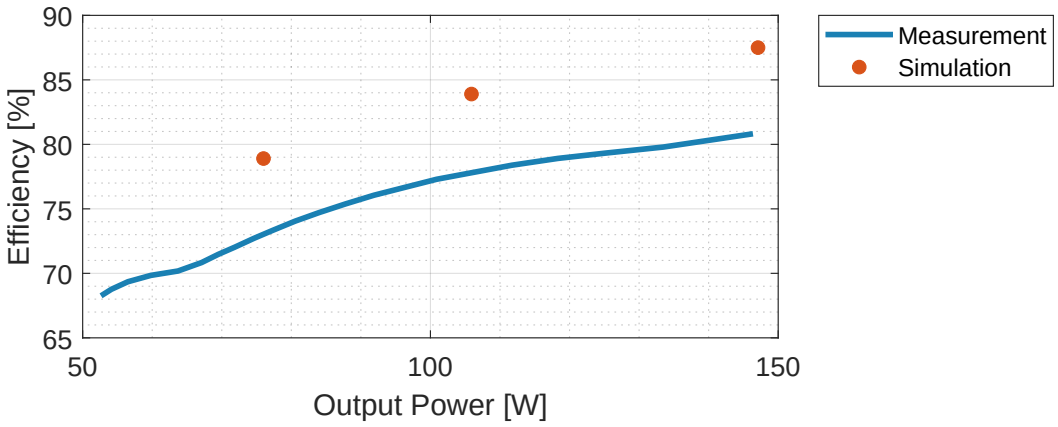


Figure 2.14: Measured dc-dc conversion efficiency across a range of output power levels. Orange markers indicate efficiency estimated using LTspice simulations.

ac currents that do not contribute to power as well as causing detrimental detuning to the power stage.The effect of these parasitics cannot be corrected without re-designing the power stage, therefore identifying and minimising these parasitics is essential to accurately predict and optimise the converter's performance.

The investigation of the PCB parasitics was carried out to quantify their significance and to extract an equivalent lumped model of the converter that more accurately represents the real hardware. This analysis also served to validate the accuracy of EM simulations in estimating the parasitics.

The EM simulator Momentum (Keysight ADS) was used to extract the parasitic capacitances at critical circuit nodes. The red arrows in 2.15 indicate the locations of the EM ports used in the simulation.

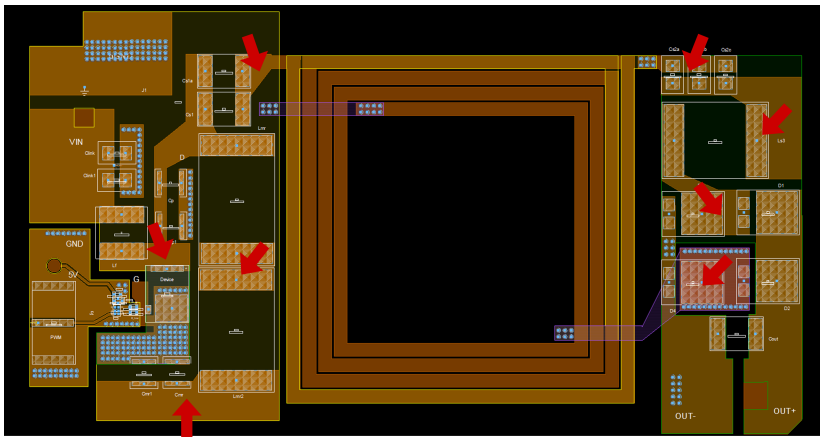


Figure 2.15: Layout view of the implemented prototype in EM simulator Momentum ADS by Keysight Technologies. The red arrows represent the EM ports placed in the simulation.

From the S-parameters obtained in the EM simulation, the parasitic capacitances

associated with each port were extracted.

The resulting equivalent network, including the extracted parasitic capacitances, is shown in Fig. 2.16, while their numerical values are summarised in Table 2.4.

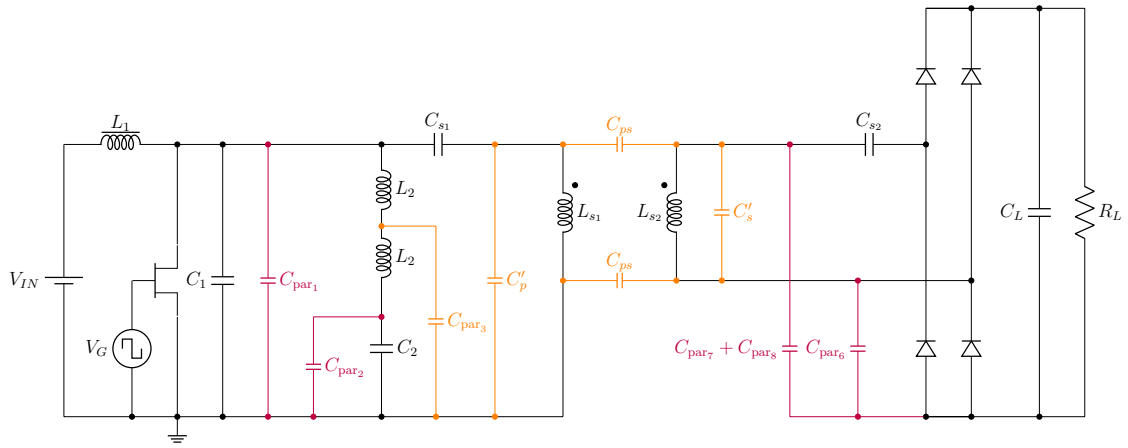


Figure 2.16: Circuit diagram of the dc-dc converter including the parasitic capacitances of the PCB, extracted from EM simulation. Actual circuit components are in black, PCB parasitics that can be absorbed are in red, and critical parasitic capacitances are in yellow.

Table 2.4: Values of parasitics capacitances extracted from EM simulation and comparison with the discrete capacitances of the prototype.

	Parameter	Value [pF]
Primary side	C_{par_1}	11.7
	C_1	7.8
	C_{par_2}	10.7
	C_2	42.0
	C_{par_3}	5.0
	C_{par_4}	2.45
	C_{s_1}	320.0
Secondary side	C_{par_5}	0.8
	C_{par_6}	4.0
	C_{par_7}	3.8
	C_{par_8}	2.9
	C_{par_9}	1.0

Fig. 2.17 show the parasitic capacitances identified through EM simulation at the primary and secondary sides of the circuit, respectively.

As shown in Table 2.4, which also reports the values of the discrete capacitors used in the design, the parasitic capacitances are on the order of a few tens of pF or less. Nevertheless, they are comparable in magnitude to the discrete capacitors of the power stage, causing a significant detuning that cannot be compensated without modifying the design.

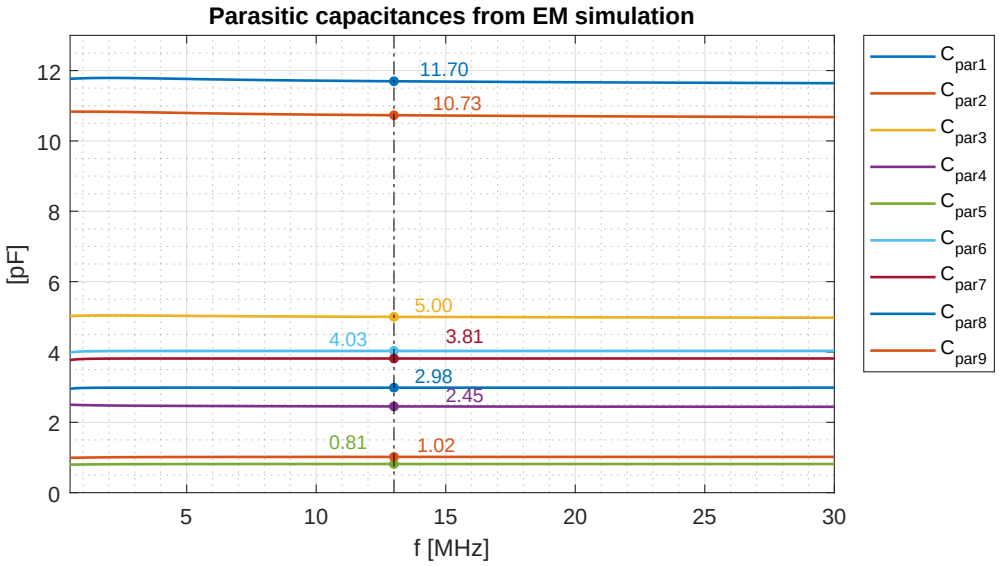


Figure 2.17: Parasitic capacitances derived from EM simulation

Time-domain simulation of the circuit in Fig. 2.16 successfully reproduces the measured input-output behaviour, efficiency, and the drain voltage waveform, shown in Fig. 2.18.

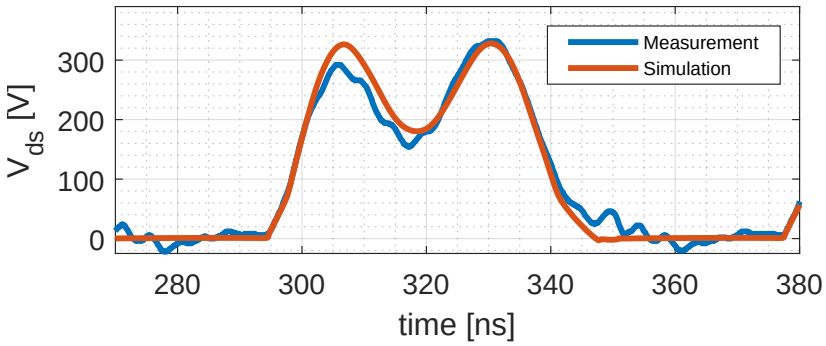


Figure 2.18: Drain voltage waveforms from measurements and simulation. The high-frequency ripple on the measured waveform is caused by the long ground lead of the probe.

By comparing the LTspice simulation results of the network including parasitics with those of the ideal network (without parasitics), the detuning observed in the hardware is confirmed. This is illustrated in Fig. 2.19, where the blue waveforms correspond to the case with parasitics and the orange waveforms to the case without parasitics. The two networks are compared for the same output power and the same load R_L. The detuning caused by the presence of the parasitics shifts the operating frequency downwards and changes the optimal load with respect to the design inputs, therefore the switching frequency had to be adjusted in the case with parasitics. The same operating conditions as the design case cannot be achieved at the same switching frequency without changing the design.

The current through the transformer interwinding capacitance C_{ps}, one of the most critical parasitics, is also shown in yellow in Fig. 2.19. This capacitance, together with the other parasitic elements, gives rise to circulating AC currents that do not contribute to the output power and therefore reduce the overall efficiency of the converter.

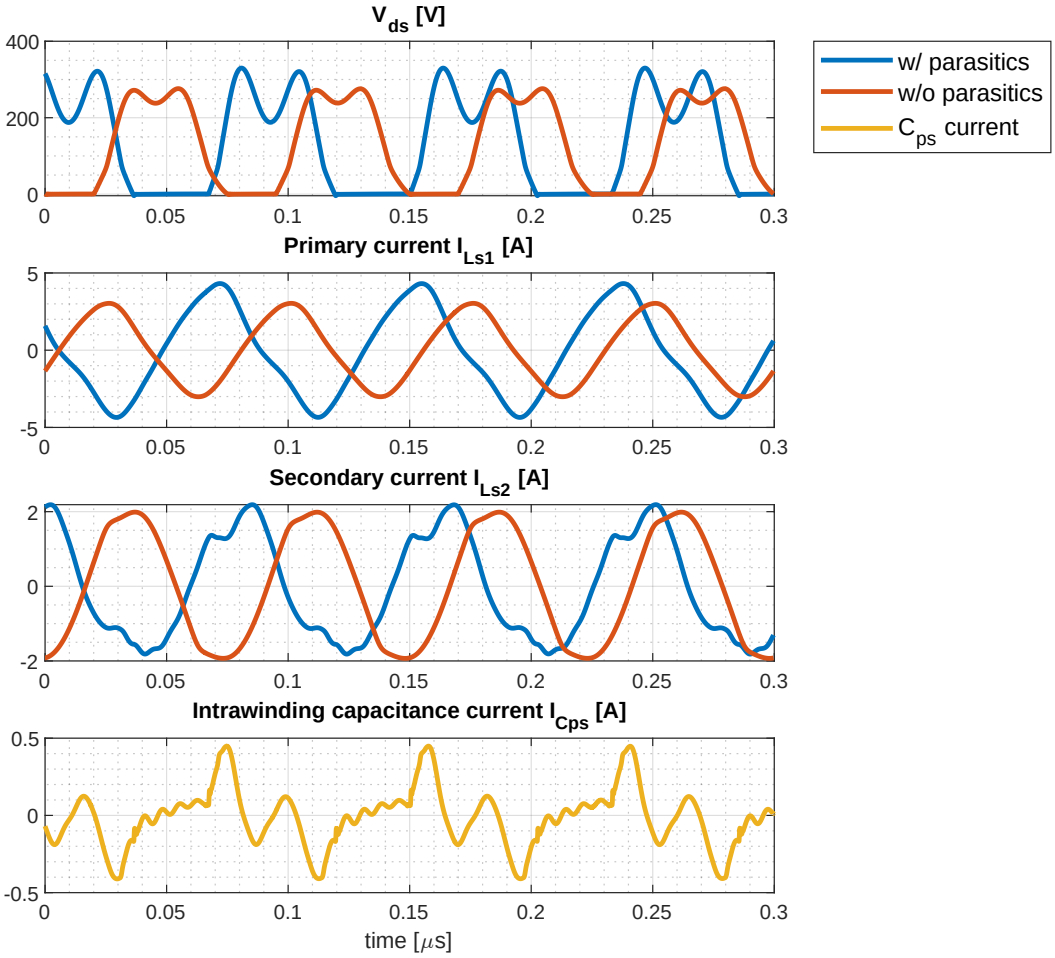


Figure 2.19: Simulated converter waveforms with and without parasitic capacitances.

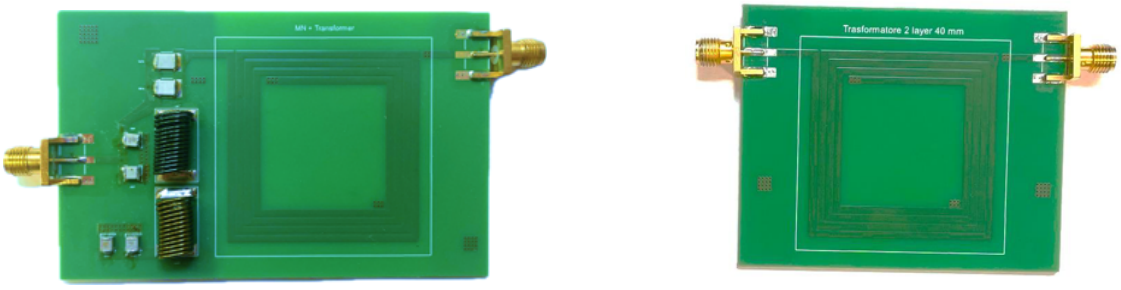
2.3.2 Model validation

To assess the accuracy of the estimated parasitics, impedance measurements were performed with a VNA (Siglent SVA1032X) on a standalone board containing the inverter matching network and the air-core transformer. The measured results were then compared with the simulated S-parameters of the equivalent network with and without parasitics.

Inverter Matching Network

Figure 2.20 show the circuit cut-outs used for this study: the passive network of the inverter, consisting of L_2, C_2, C_1, C_{s_1} and the air-core transformer) and the stand-alone

air-core transformer.



(a) Inverter MN cut-out (b) Air-Core transformer cut-out

Figure 2.20: Circuit cut-outs. (a) Inverter MN, consisting of L_2, C_2, C_1, C_{s_1} and the air-core transformer. (b) Stand-alone board of the transformer.

As shown in Fig. 2.21, the measured S_{11} parameter of the inverter matching network (blue curve) exhibits a significant mismatch compared to the simulated S_{11} of the corresponding lumped-element network without parasitics (orange curve).

When the parasitic capacitances extracted from EM simulation (as shown in Fig. 2.16) are included in the equivalent network, the simulated S_{11} shows very good agreement with the measurements, as evidenced by the close overlap of the blue and yellow curves in Fig. 2.21.

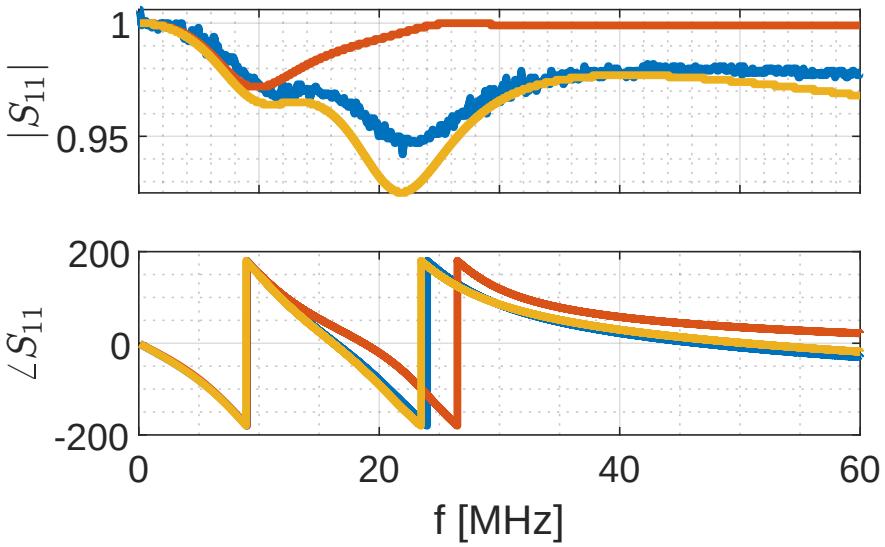


Figure 2.21: S11 parameter of the inverter's passive network and air-core transformer. The blue curve represents measured data from the VNA, the yellow curve shows simulated data accounting for parasitics, and the orange curve represents the simulated S11 of the ideal network.

Transformer parasitics

As previously discussed, one of the most critical parasitic capacitances, both in terms of magnitude and impact, was found to be the transformer's interwinding (primary-to-secondary) capacitance C_{ps}. This capacitance is particularly detrimental because it allows circulating currents that do not contribute to power transfer and it also adds additional equivalent shunt capacitance causing detuning of the circuit as it cannot be absorbed in the design. For this reason, it is essential to properly characterise all parasitic capacitances of the transformer when designing HF power conversion systems. Figure 2.22 shows the complete HF transformer model, including the primary and secondary-side intra-winding capacitances C_p and C_s, and the interwinding capacitance C_{ps}. The extraction of the transformer inductances L_{s_1}, L_{s_2} and the coupling coefficient

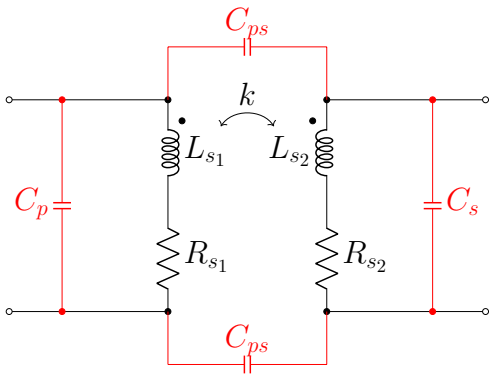


Figure 2.22: High-frequency transformer equivalent circuit model including primary- and secondary-side intra-winding capacitances C_p and C_s, and interwinding capacitance C_{ps}.

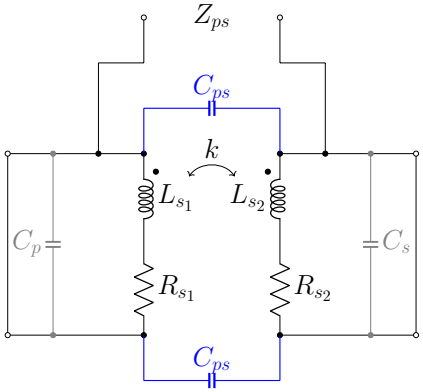
k was described in Section 2.2 . This section focuses on the procedure for extracting the parasitic capacitances. The same methodology applies whether S-parameter data is obtained from EM simulation or from VNA measurements.

To evaluate the interwinding capacitance C_{ps}, both the primary and secondary windings must be shorted, and the input impedance (or equivalently S_{11}) measured across port 1 and port 2. The capacitance is then calculated from the imaginary part of the measured impedance Z_{ps}:

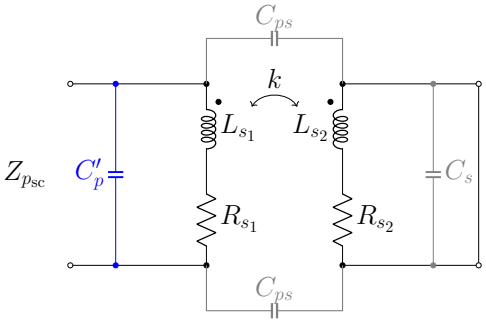
$$C_{ps} = \frac{1}{2\omega\, \Im\{Z_{ps}\}}, \tag{2.34}$$

where $\omega = 2\pi f$ is the angular switching frequency.

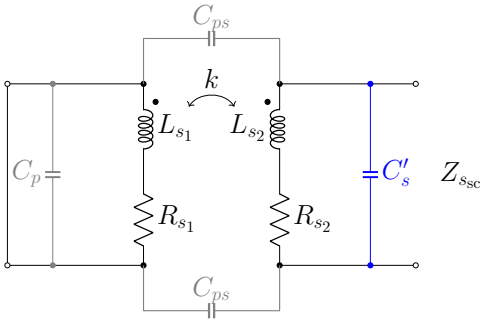
The primary and secondary side intra-winding capacitances C_p and C_s cannot be measured directly but can be determined from the resonant frequencies of the input impedances $Z_{p_{\mathrm{sc}}}$ and $Z_{s_{\mathrm{sc}}}$, seen from the primary and secondary sides respectively, when the opposite side is shorted.



(a) Setup for C_{ps} extraction (both windings shorted).



(b) Setup for C_p extraction (secondary shorted).



(c) Setup for C_s extraction (primary shorted).

Figure 2.23: Measurement setups used for transformer parasitic capacitance extraction: (a) inter-winding capacitance C_{ps}, (b) primary-side intra-winding capacitance C_p, and (c) secondary-side intra-winding capacitance C_s.

When the secondary is shorted, the input impedance $Z_{p_{sc}}$ seen from the primary is:

$$Z_{p_{sc}} = j\omega L_{p_{sc}} \parallel \frac{1}{j\omega C'_p}, \tag{2.35}$$

where

$$C'_p = C_p + 2C_{ps}, \qquad L_{p_{sc}} = (1 - k^2)L_{s_1}. \tag{2.36}$$

In (2.36), $L_{p_{sc}}$ is the primary short-circuit inductance and k the coupling coefficient.

From the resonant frequency $f_{p_{sc}}$ of $Z_{p_{sc}}$, the intra-winding primary capacitance C_p is obtained as:

$$C_p = \frac{1}{(2\pi f_{p_{sc}})^2 L_{p_{sc}}} - 2C_{ps}. \tag{2.37}$$

Similarly, when the primary is shorted, the impedance seen from the secondary is:

$$Z_{s_{sc}} = j\omega L_{s_{sc}} \parallel \frac{1}{j\omega C'_s}, \tag{2.38}$$

where

$$C'_s = C_s + 2C_{ps}, \qquad L_{s_{\mathrm{sc}}} = (1 - k^2)L_{s_2}. \tag{2.39}$$

In (2.39), $L_{s_{\mathrm{sc}}}$ is the secondary short-circuit inductance.

From the resonant frequency $f_{s_{\mathrm{sc}}}$ of $Z_{s_{\mathrm{sc}}}$, the secondary-side intra-winding capacitance C_s is given by:

$$C_s = \frac{1}{(2\pi f_{s_{\mathrm{sc}}})^2 L_{s_{\mathrm{sc}}}} - 2C_{ps}. \tag{2.40}$$

Figure 2.23 shows the measurement setups used to extract the parasitic capacitances.

Table 2.5: Air-Core Transformer complete characterisation from EM simulation.

Parameter	**Description**	**Value**
L_p	Primary inductance	995 nH
L_s	Secondary inductance	154 nH
C_p	Primary-side intrawinding capacitance	7.07 pF
C_s	Secondary-side intrawinding capacitance	9.5 pF
R_p	Primary-side parasitic resistance	0.56 Ω
R_s	Secondary-side parasitic resistance	0.2 Ω
C_{ps}	Interwinding capacitance	21 pF
k	Coupling coefficient	66 %
M	Mutual inductance	260 nH
$f_{p_{\mathrm{sc}}}$	Primary resonance	80 MHz
$f_{s_{\mathrm{sc}}}$	Secondary resonance	175 MHz
$L_{p_{sc}}$	Primary short-circuit inductance at $f_{p_{\mathrm{sc}}}$	14.25 µH
$L_{s_{sc}}$	Secondary short-circuit inductance at $f_{s_{\mathrm{sc}}}$	1.15 µH

Figure 2.24 summarises the transformer parameters extracted from EM simulation, including inductances, coupling coefficient, and parasitic capacitances. The ADS Momentum simulator provides the S-parameter data of the transformer layout, which can then be imported as a 2-port block in a schematic simulation. This block can be used exactly like a DUT in a VNA setup: one side can be shorted or terminated to evaluate the parameters as described previously. This allows reproducing in simulation the same measurement conditions used during bench characterisation, enabling a direct comparison between simulated and measured results.

As done previously for the inverter matching network, the validity of the derived lumped model was confirmed by comparing the simulated S-parameters of the lumped network including parasitics with those obtained from EM simulation and from VNA measurements of the stand-alone transformer shown in Fig. 2.20b.

Figure 2.25 compares the measured S-parameters (blue), the EM simulation (orange), and the lumped model simulation (yellow). Excellent agreement is observed in the

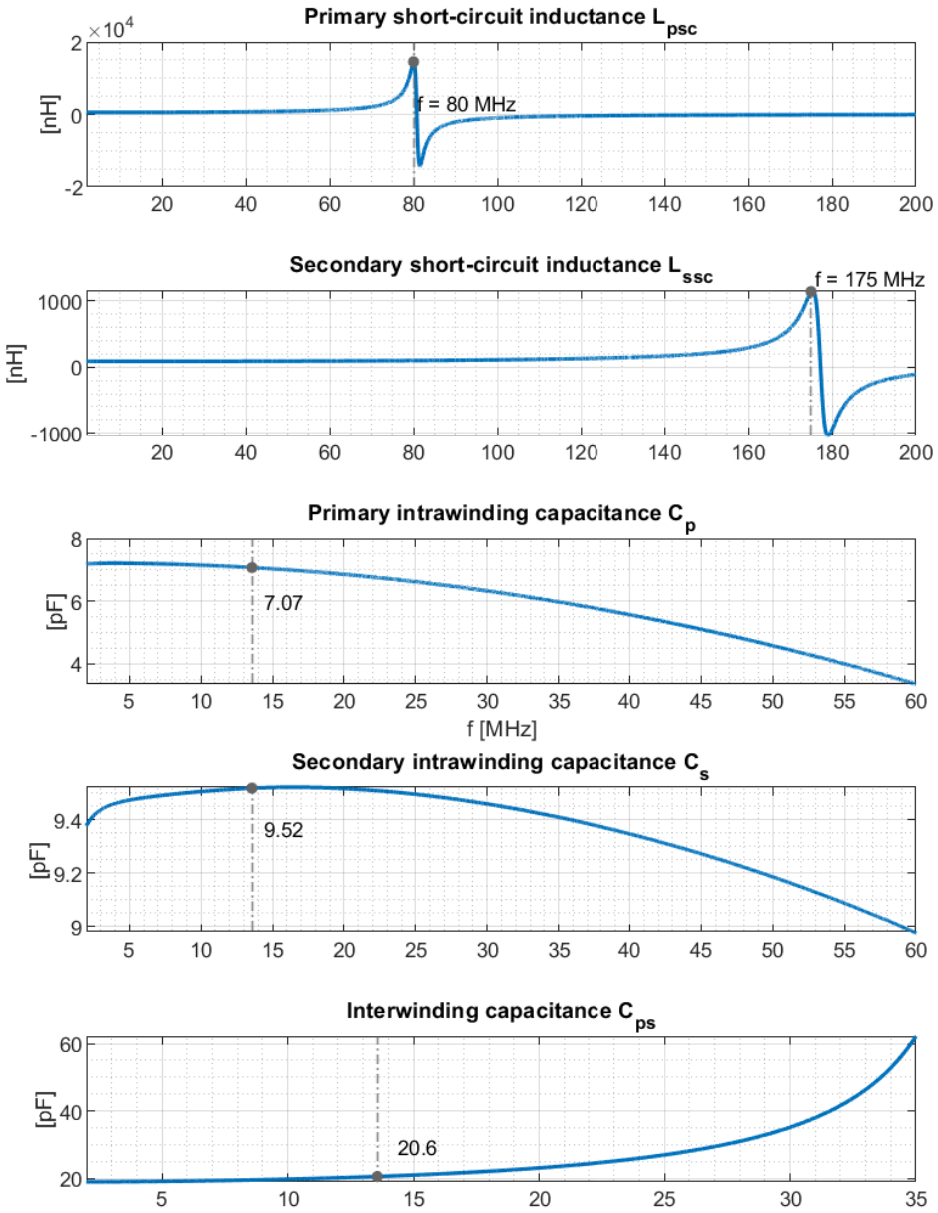


Figure 2.24: Transformer parasitic capacitances extracted from EM simulation. The plot also shows the primary and secondary short-circuit inductances and their resonant frequencies.

frequency range of interest, confirming that the extracted lumped model accurately reproduces the transformer's high-frequency behaviour.

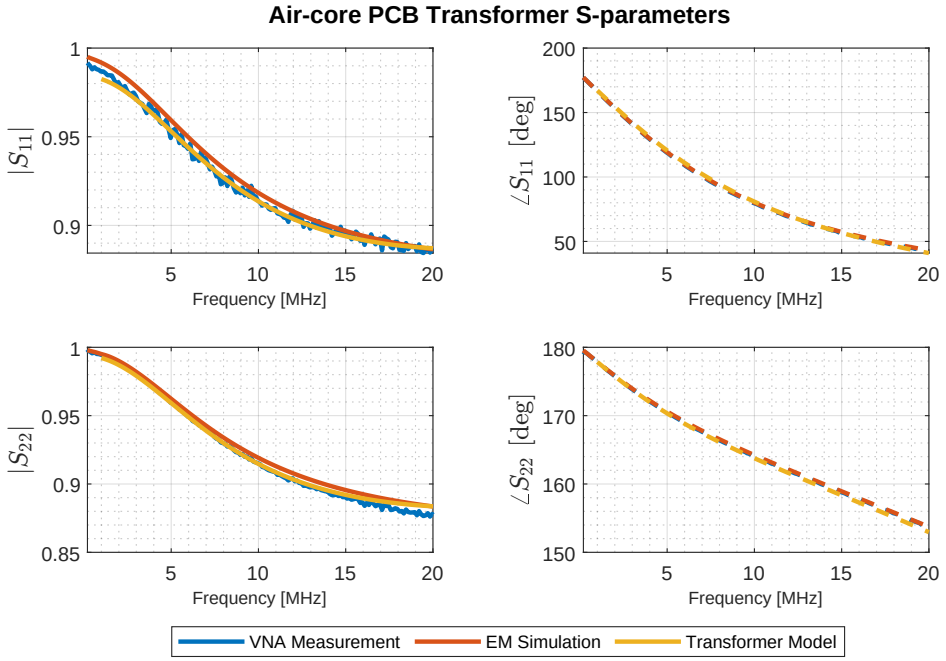


Figure 2.25: Comparison of the transformer S-parameters from VNA measurement (blue), EM simulation (orange), and lumped model simulation (yellow).

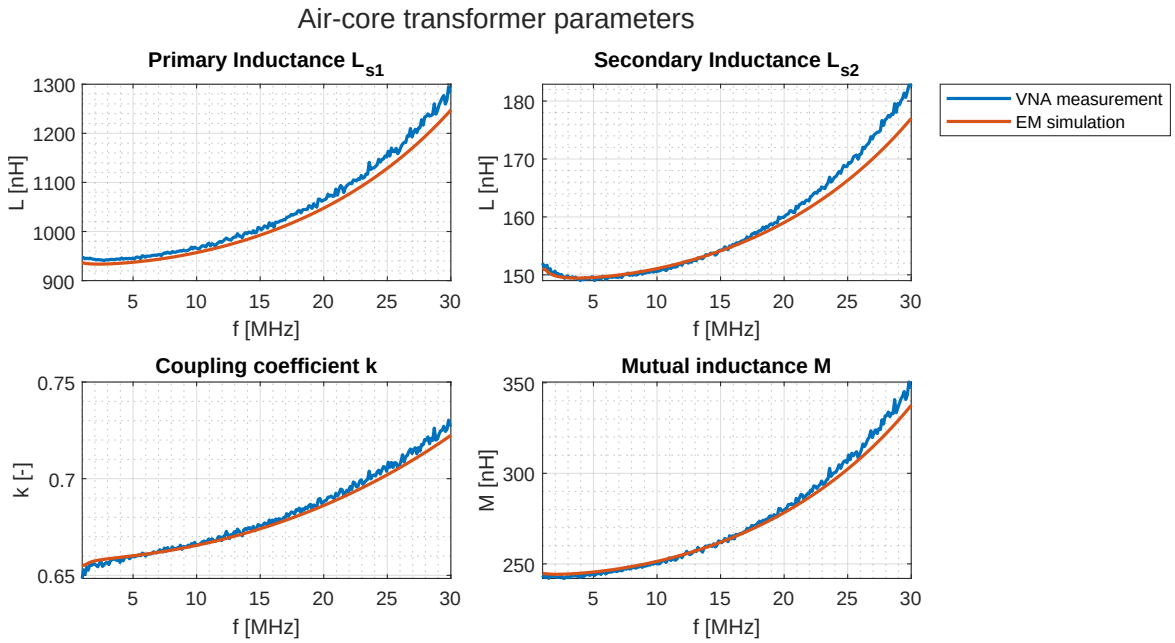


Figure 2.26: Comparison of transformer lumped model parameters obtained from EM simulation (orange) and VNA measurement (blue).

Finally, Fig. 2.26 compares the extracted lumped model parameters from VNA measurements (blue) with those from EM simulation (orange), further confirming the

accuracy of the EM simulation in predicting transformer parasitics.

2.3.3 Conclusions

These findings emphasise the critical role of parasitic effects to HF systems' performance. It is crucial that parasitics that cannot be absorbed into the circuit components (depicted in red in Fig. 2.16) are minimised, to reduce circulating ac currents that do not contribute to output power. Specifically for this prototype, it was shown that placing the ground plane at the adjacent PCB layer to the power plane, close to nodes connected to inductors, had high impact on detuning and efficiency degradation.

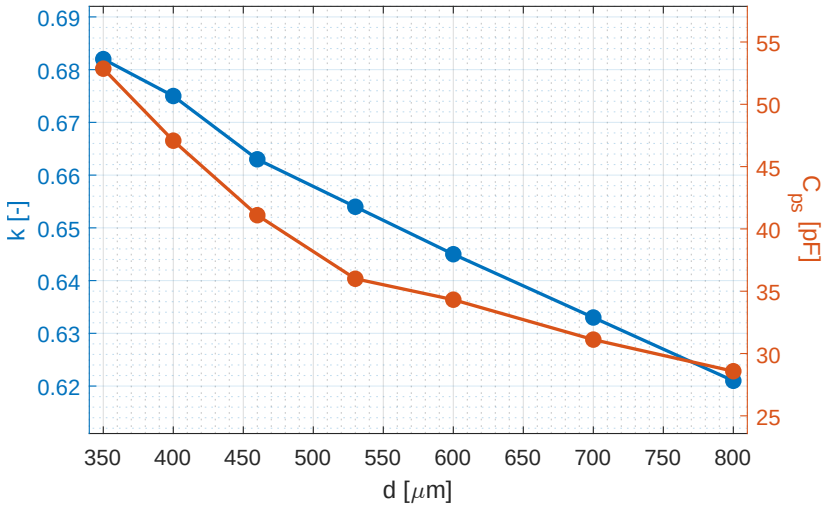


Figure 2.27: Effect of coil spacing d_ε on coupling coefficient k and interwinding capacitance C_{ps} for the prototype transformer geometry.

A significant role is also played by the transformer's primary-to-secondary capacitance (C_{ps}), which must be minimised. As a first approximation, C_{ps} can be modelled as a parallel-plate capacitance

$$C_{ps} \approx \varepsilon_0 \varepsilon_r \frac{A_{\text{ov}}}{d_\varepsilon}, \tag{2.41}$$

where A_{ov} is the facing (overlap) area between the windings and d_ε is the distance between the two coils. Minimising C_{ps} thus calls for reducing A_{ov} and/or increasing d_ε. For air-core windings, both reducing the facing area and increasing the spacing decrease the mutual inductance and the coupling coefficient k, as the shared flux linkage decreases when the coils overlap less or are farther apart. Figure 2.27 shows how the coupling coefficient k and the interwinding capacitance C_{ps} vary with the spacing d_ε between the two coils (i.e., the thickness of the FR-4 dielectric between the first and second PCB layers). The values were obtained from electromagnetic simulations of the transformer used in the prototype, sweeping only d_ε while keeping all

other dimensions unchanged.As d_ε increases, both C_{ps} and k decrease, illustrating the trade-off between reduced interwinding capacitance and reduced magnetic coupling.

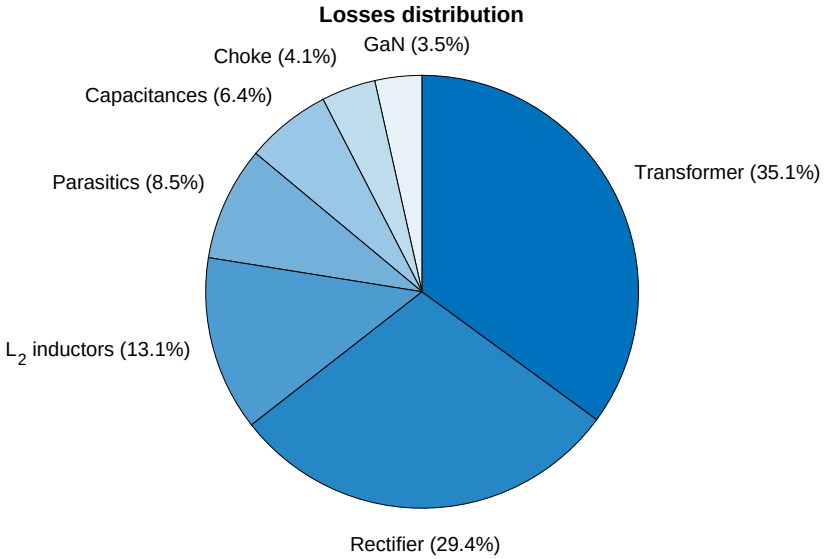


Figure 2.28: Losses distribution.

The loss breakdown of the designed converter, based on simulations incorporating all the extracted parasitics and manufacturers' circuit models for the components, shows that over 25 % of the total losses are attributed to the bridge rectifier, while 13 % arise from the ϕ-branch inductor L_2. Efficiency improvements can therefore be anticipated by adopting an alternative rectifier topology and using air-core inductors with higher Q factors. Additionally, an inverter design with increased shunt capacitance could lower device losses by reducing the current flowing through the transistor's output capacitance.

The largest loss component arises from transformer copper losses. Proximity effects are pronounced where currents flow in the same direction in contiguous branches of the spirals, leading to current crowding and elevated ac resistance [48–51]. A practical mitigation is a *current-ballasting* (tapered) layout, in which the trace width w is gradually reduced as the spiral approaches its centre; this equalises current density across branches and lowers the effective R_{ac} [49, 50]. In addition, tapering increases the inner diameter and thus the average turn radius; this can increase inductance per turn and allow the target inductance to be met with fewer turns [46]. Electromagnetic simulations of the transformer with a moderate tapered layout showed a reduction of total ac resistance by approximately 3% at the operating frequency, together with a 5.2% increase in inductance. While the direct R_{ac} reduction is modest, the higher inductance per turn offers leverage to meet the target inductance with slightly fewer

turns, which can further reduce copper loss. Notably, the taper applied here is very modest – the trace width changes only from 1.5 mm on the outermost turn to 1.2 mm on the innermost – and could be further optimised to yield additional reductions in R_{ac}. Figure 2.29 compares the simulated surface current density for a uniform-width spiral (left) and the tapered spiral. Tapering equalises the sheet current on the inner turns, reducing proximity-induced crowding at the inner corners.

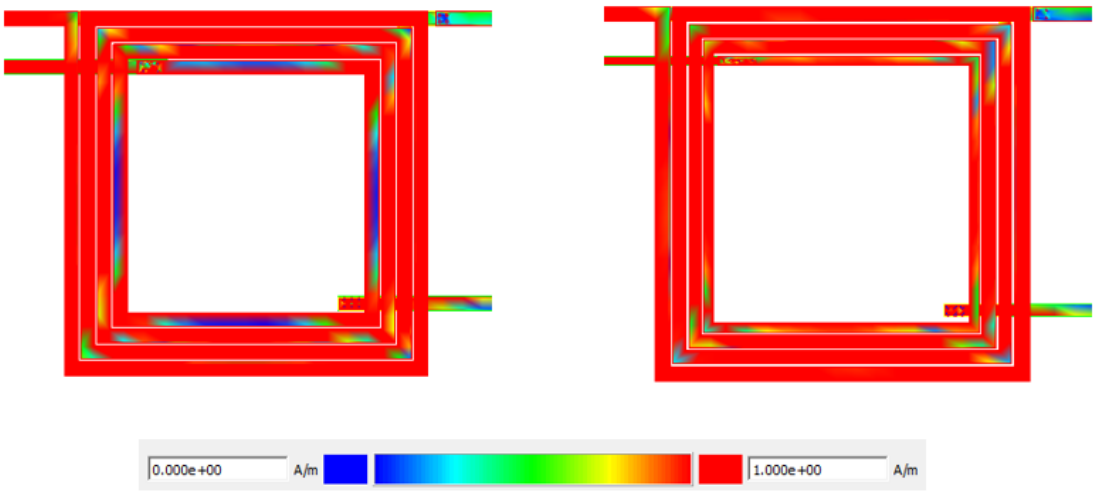


Figure 2.29: Simulated surface current density on the transformer spiral: *left* - uniform trace width; *right* - tapered layout.

2.4 Output Voltage Regulation

Class E-type inverters achieve optimal operation only for a specific load [22]. Output regulation is not possible with Pulse Width Modulation (PWM) techniques because the gain of the converter is not sensitive to duty cycle variation. Instead, adjusting the switching frequency changes the impedance of the output branch, enabling output control through frequency modulation [40]. In this section, a First Harmonic Approximation (FHA) model of the converter is derived to obtain the dc-dc voltage gain $G_v(f)$ as a function of the switching frequency f, thereby demonstrating frequency-controlled gain. The analytical model is then validated against time-domain simulations and experimental data. Finally, open-loop measurements are presented to show voltage regulation achieved via frequency control under both load and input-voltage variations.

2.4.1 FHA modelling

FHA, introduced in [52], enables the analysis of resonant converters by means of classical complex ac circuit analysis. This technique assumes that power transfer is dominated by the fundamental components of voltages and currents, enabling a linear approximation of the converter's inherently non-linear, non-sinusoidal behaviour. The Class EF_2 inverter applies a near-square wave voltage to the primary resonant tank, which suppresses higher-order harmonics, resulting in an approximately sinusoidal current at the input of the link. The FHA model replaces the inverter with a sinusoidal voltage source equal to the fundamental component of v_{ds} and the link and rectifier with an equivalent impedance, as illustrated in Fig. 2.30.

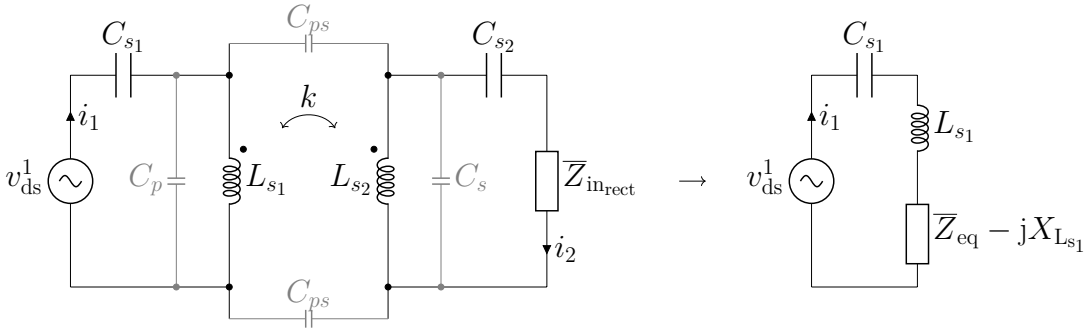


Figure 2.30: FHA model of the converter. Transformer's parasitic capacitances are shown in gray.

For a given load R_L, the rectifier input impedance $\overline{Z}_{\mathrm{in_{rect}}}$ is calculated via (2.2) and used to evaluate the reflected impedance seen from the primary side $\overline{Z}_{\mathrm{eq}}$ using (2.12)-(2.13). $\overline{Z}_{\mathrm{eq}}$ serves as the output impedance of the Class EF_2 inverter in its state-space

representation [31] to compute the drain voltage v_{ds} and extract the first harmonic v_{ds}^1. The amplitude I_2 of the sinusoidal current input to the rectifier is given by $I_2 = G_i(f, R_L)V_{\text{ds}}^1$, where the current gain G_i, which depends on both frequency f and load R_L, is defined as the ratio of the amplitudes of i_2 and v_{ds}^1:

$$G_i(f, R_L) = \frac{I_2}{V_{\text{ds}}^1}. \tag{2.42}$$

From (2.7), and considering the FHA model in Fig. 2.30, the secondary current I_2 can be expressed as follows:

$$i_2 = \frac{i_1 \overline{Z}_{\text{ref}}}{-jX_M} \tag{2.43}$$

where $\overline{Z}_{\text{ref}}$ is the reflected impedance of the link:

$$\overline{Z}_{\text{ref}} = \overline{Z}_{\text{eq}} - jX_{L_{s_1}} \tag{2.44}$$

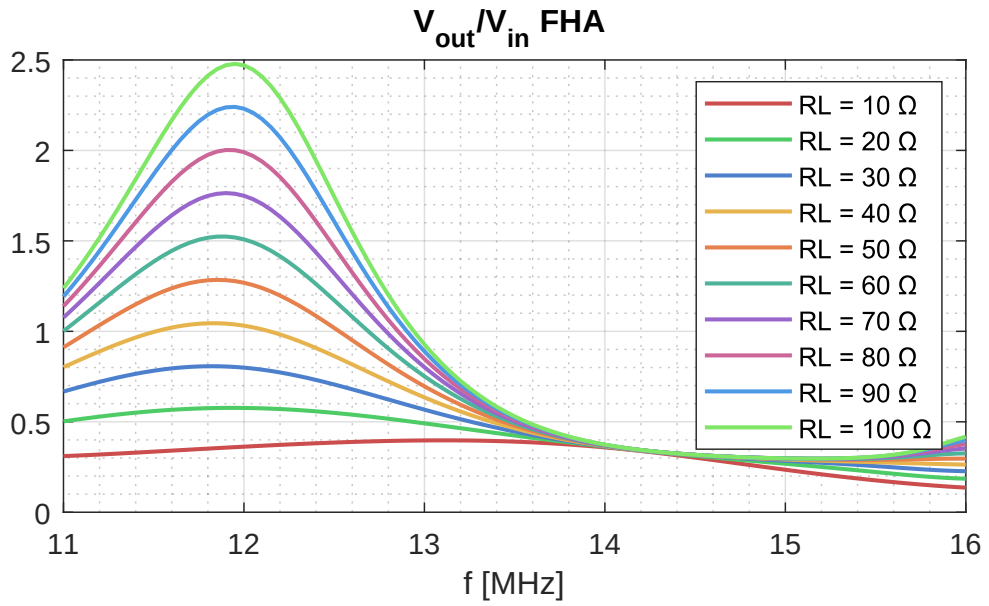


Figure 2.31: FHA dc-dc voltage gain curves for different loads R_L.

The primary current i_1 from Fig. 2.30 can be expressed as:

$$i_1 = \frac{v_{\text{ds}}^1}{j(X_{C_{s_1}} + X_{L_{s_1}}) + \overline{Z}_{\text{eq}} - jX_{L_{s_1}}} = \frac{v_{\text{ds}}^1}{jX_{C_{s_1}} + \overline{Z}_{\text{eq}}} \tag{2.45}$$

As a result, the current gain $G_i(f, R_L)$ can be written as:

$$G_i(f, R_L) = \frac{I_2}{V_{\text{ds}}^1} = \left| \frac{\overline{Z}_{\text{eq}} - \text{j}X_{\text{L}_{s_1}}}{\text{j}X_{\text{M}}(\overline{Z}_{\text{eq}} + \text{j}X_{\text{C}_{s_1}})} \right|. \tag{2.46}$$

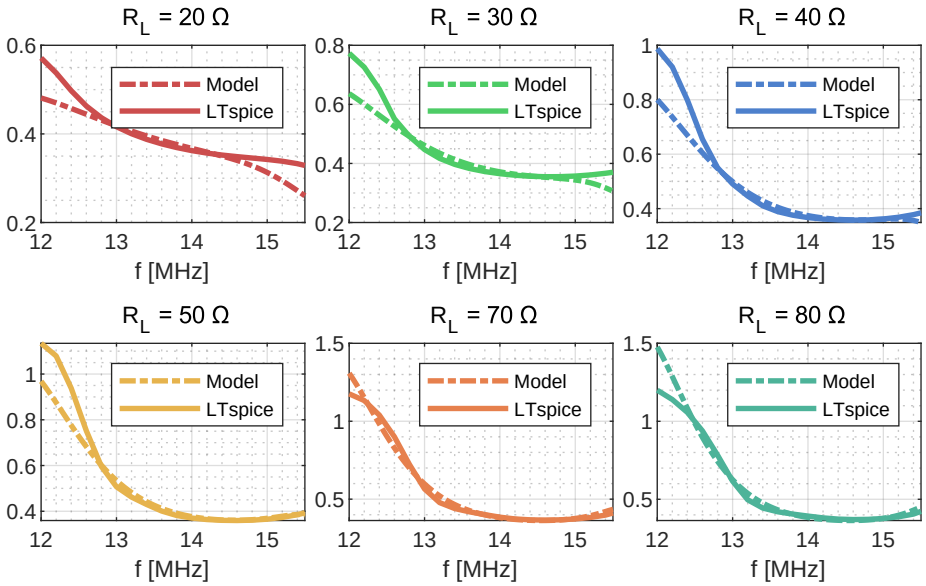


Figure 2.32: Comparison of FHA dc-dc voltage gain curves and LTspice simulation for different loads R_L.

In (2.46), $X_{\mathrm{M}} = \omega k\sqrt{L_{s_1} L_{s_2}}$ and $X_{\mathrm{C}_{s_1}}$ is the reactance of the primary side compensation capacitor C_{s_1}. Finally, the dc-dc voltage gain $G_v(f, R_L)$ is obtained by computing the output voltage V_{out} [39] and normalising it with respect to the input voltage V_{in}:

$$G_v(f, R_L) = \frac{1}{V_{\mathrm{in}}} \frac{2V_{\mathrm{ds}}^1 G_i R_L}{\pi + 2\omega C_j R_L}. \tag{2.47}$$

Fig. 2.31 shows the dc-dc voltage gain G_v predicted by the FHA model as a function of f for various load values R_L. To assess the model's accuracy, the FHA predicted gain is compared with results from non-linear LTspice simulations, as shown in Fig. 2.32, where dashed lines represent FHA results and the solid lines correspond to simulated gains. As shown, the linear model closely matches simulation results within the frequency range of interest. Deviations occur, as expected, when inverter output current distortion becomes significant, violating the assumption of a purely sinusoidal link input current. This is highlighted in Fig. 2.33, where the total harmonic distortion (THD) of the primary current calculated from the state space of the inverter is shown.

To account for frequency detuning from PCB parasitics, the model was refined to include the transformer's primary and secondary intra-winding capacitances C_{p} and C_{s}, and inter-winding capacitance C_{ps}. The equivalent reflected impedance of the link as seen from the primary side including the parasitics can be evaluated by using the equivalent circuit in Fig. 2.34, where $\overline{Z}_{\mathrm{s}}$ is equal to

$$\overline{Z}_{\mathrm{s}} = \frac{j(\overline{Z}_{\mathrm{in_{rect}}} + \mathrm{j}X_{\mathrm{C}_{s_2}})X_{\mathrm{C_s}}}{\overline{Z}_{\mathrm{in_{rect}}} + \mathrm{j}X_{\mathrm{C}_{s_2}} + \mathrm{j}X_{\mathrm{C_s}}}. \tag{2.48}$$

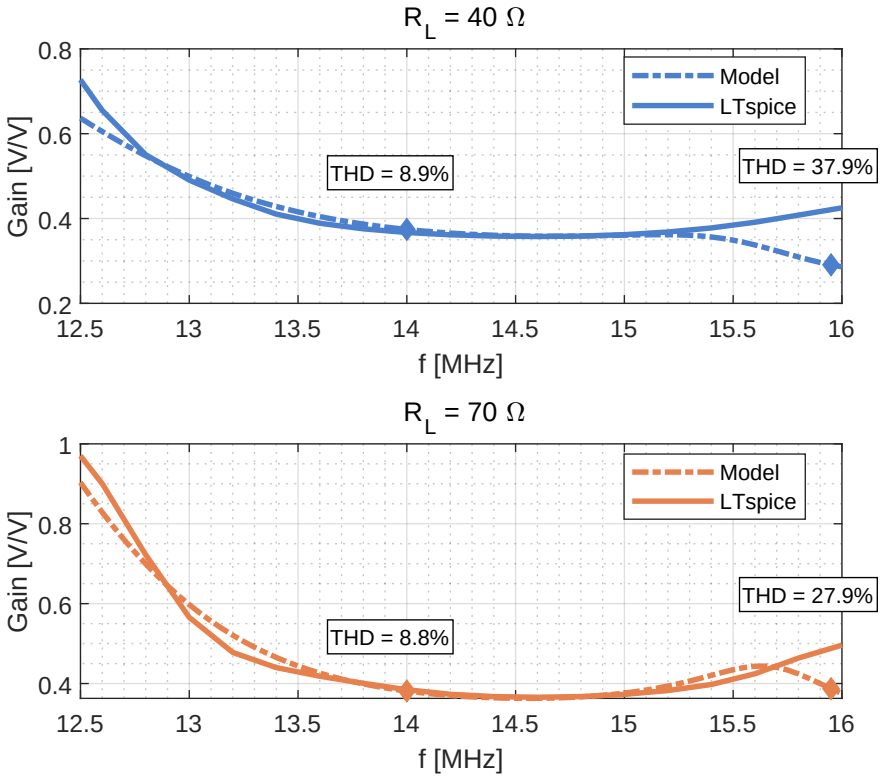


Figure 2.33: Comparison between FHA model and gain extracted from LTspice simulation. Model deviates from simulation when the total harmonic distortion of the primary current is high enough to violate the assumption of sinusoidal inverter output current.

X_{C_s} is the reactance of the secondary intra-winding capacitance C_s.

By applying KVL and KCL, the following system of equations is obtained:

$$\begin{cases} i_{\text{in}} = i_p + i_1 + i_{ps} \\ i_{ps} = i_2 + i_o \\ i_o = \frac{v_o}{Z_s} \\ v_o = jX_{L_{s_2}} i_2 + jX_M i_1 \\ v_{\text{in}} = jX_{L_{s_1}} i_1 - jX_M i_2 \\ i_{ps} = -j\frac{(v_{\text{in}} - v_o)}{X_{C_{ps}}} \\ i_p = -j\frac{v_{\text{in}}}{X_{C_p}} \end{cases} \tag{2.49}$$

where X_{C_p}, X_{C_s}, and $X_{C_{ps}}$ are the corresponding capacitive reactances. The system

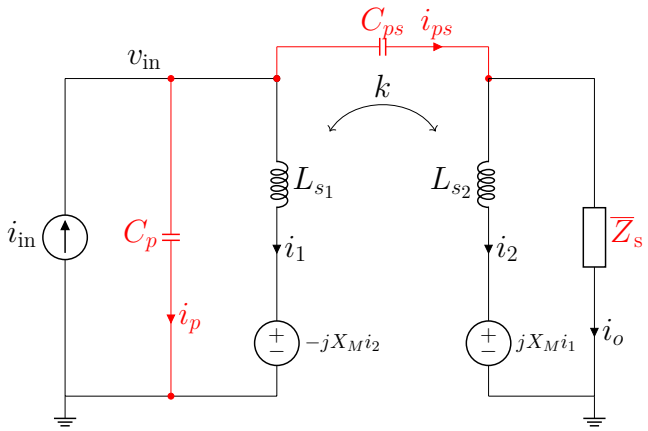


Figure 2.34: Equivalent circuit for the derivation of the link input impedance as seen from the primary side considering all the transformer parasitic capacitances.

in (2.49) can be rewritten as:

$$\begin{cases} i_{\text{in}} = -j\frac{v_{\text{in}}}{X_{\text{Cp}}} + i_1 - j\frac{(v_{\text{in}}-v_{\text{o}})}{X_{\text{Cps}}} \\ i_2 = -j\frac{(v_{\text{in}}-v_{\text{o}})}{X_{\text{Cps}}} - \frac{v_{\text{o}}}{Z_{\text{s}}} \\ i_o = \frac{v_{\text{o}}}{Z_{\text{s}}} \\ v_o = jX_{L_{s_2}} i_2 + jX_M i_1 \\ v_{\text{in}} = jX_{L_{s_1}} i_1 - jX_M i_2 \\ i_{ps} = -j\frac{(v_{\text{in}}-v_{\text{o}})}{X_{\text{Cps}}} \\ i_p = -j\frac{v_{\text{in}}}{X_{\text{Cp}}} \end{cases} \tag{2.50}$$

Solving for v_1 as a function of i_1 yields the link input impedance $\overline{Z}_{\text{eq}}^{\text{par}}$,

$$\overline{Z}_{\text{eq}}^{\text{par}} = \frac{X_{\text{Cp}}((\overline{Z}_{\text{s}}+\text{j}X_{\text{Cps}})(X_{\text{M}}^2-X_{\text{Ls}_1}X_{\text{Ls}_2})-X_{\text{Cps}}X_{\text{Ls}_1}\overline{Z}_{\text{s}})}{(X_{\text{M}}^2-X_{\text{Ls}_1}X_{\text{Ls}_2})(X_{\text{Cps}}+X_{\text{Cp}}-\text{j}\overline{Z}_{\text{s}})+X_{\text{Cps}}(\text{j}X_{\text{Ls}_1}Z_{\text{s}}-X_{\text{Cp}}X_{\text{Ls}_2})+\text{j}X_{\text{Cp}}\overline{Z}_{\text{s}}(X_{\text{Cps}}+X_{\text{Ls}_1}+X_{\text{Ls}_2}-2X_{\text{M}})} \tag{2.51}$$

Fig. 2.35 shows the comparison between the real and the imaginary parts of the link reflected impedance as seen from the primary in the ideal case and considering the transformer' parasitic capacitances.

The equation in (2.51) substitutes $\overline{Z}_{\text{eq}}$ in the expression of the DC gain to account for the presence of transformer parasitics. As shown in Fig. 2.32, the gain curve from the FHA model including transformer parasitics (in yellow) closely matches both the LTspice simulation (in purple) and experimental results (in orange), confirming the model's accuracy within the converter's operating frequency range.

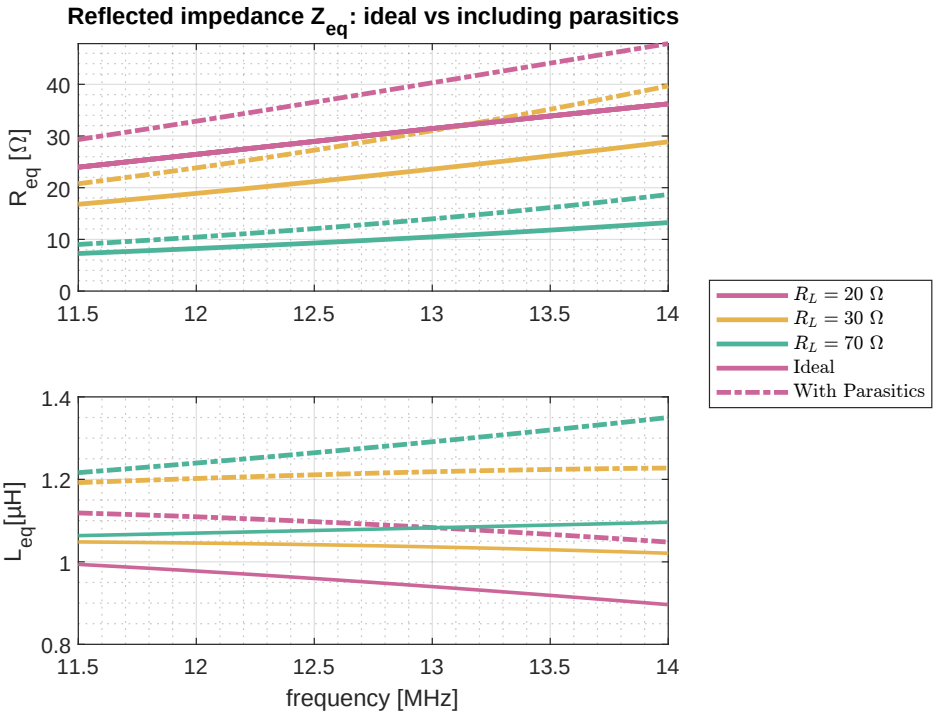


Figure 2.35: Comparison between the link reflected impedance seen from the primary in the ideal case and when considering the intra-winding and interwinding capacitances.

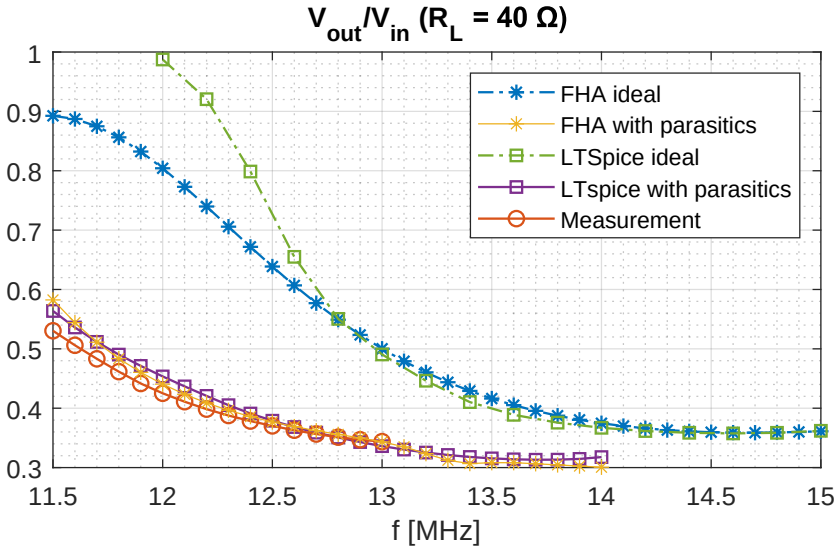


Figure 2.36: Comparison of dc-dc voltage gain curves obtained from LTspice simulation both ideal (green) and including PCB layout parasitics (purple), from the FHA model both ideal (blue) and including parasitics (yellow) and the actual measurements (in orange) for a given load R_L and $V_{\text{in}} = 90V$.

2.4.2 Experimental Results

The FHA model derived in the previous section confirms that the dc-dc gain can be adjusted via switching-frequency control. Consequently, output-voltage regulation is achievable under both load and input-voltage variations. Experimental validation was performed in open loop by manually tuning the switching frequency to maintain a constant output voltage of 40 V across varying load and input conditions, while the duty cycle was adjusted only to preserve soft switching (ZVS).

Within the useful operating band, the gain is approximately monotonic with frequency: for a given load, increasing the switching frequency reduces the output voltage, and decreasing it increases the output voltage. Variations of duty cycle have a negligible effect on the output level but are effective for maintaining ZVS and minimising switching loss.

Varying Output Load

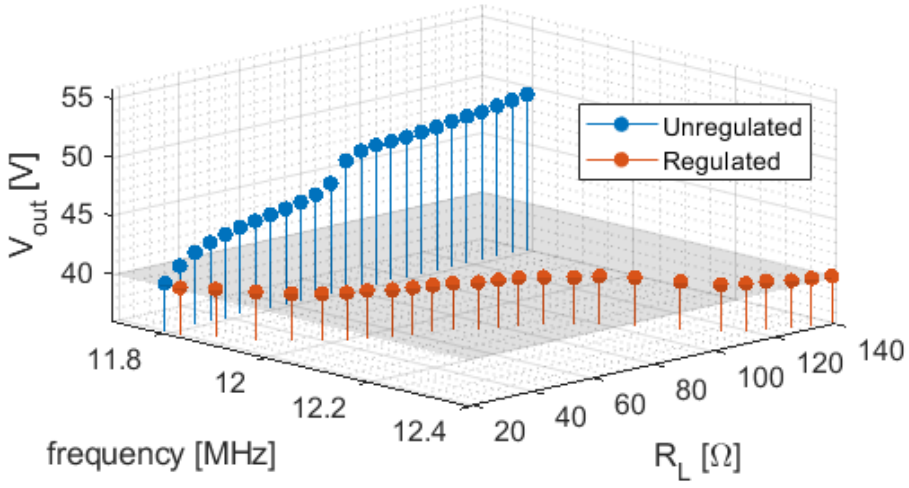


Figure 2.37: Output voltage regulation for varying load R_L through frequency control, for a fixed $V_{\text{in}} = 90\,\text{V}$. The gray plane represents the target output voltage.

An experimental comparison of output regulation through frequency control effectiveness for a range of output loads is shown in Fig. 2.37. The blue dots represent the output voltage for varying load R_L considering a fixed switching frequency of 11.8 MHz. The orange dots represent the output voltage after frequency adjustment to keep the output voltage fixed at 40 V. The desired output voltage is represented by the gray plane. The duty cycle was also adjusted so that the working temperature of the device was minimised.

Varying Input Voltage

Frequency control can also be employed to regulate the output voltage for varying input voltage, as shown in Fig. 2.38. The blue dots represent the output voltage for different values of V_{in} while the load is kept constant to 46 Ω and the switching frequency is fixed. By adjusting the switching frequency and the duty cycle, it is possible to keep the output voltage constant for an input voltage range of 80 V to 130 V, while maintaining ZVS, as depicted by the orange dots in Fig. 2.38.

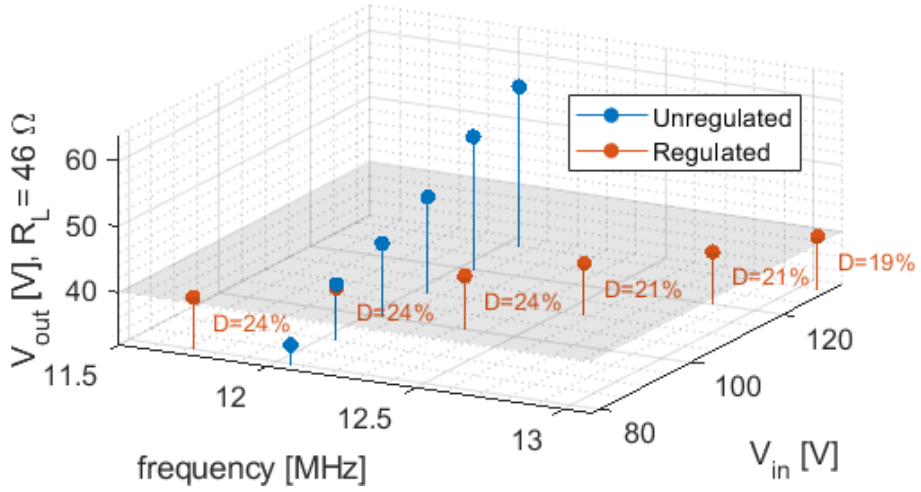


Figure 2.38: Output voltage regulation for varying V_{in} through frequency and duty cycle control. The gray plane represents the target output voltage (load is kept constant).

These results indicate that a closed-loop implementation based on frequency-control is feasible. A possible approach is to construct a lookup table $G_v(f; R_L, V_{\text{in}})$ (or equivalently $f^\star(R_L, V_{\text{in}}, V^\star_{\text{out}})$) from the FHA model and calibration data. The controller can then use table lookup and interpolation to determine the switching frequency required to achieve the target V_{out} for the estimated load, with a small duty adjustment to maintain ZVS.

2.5 Summary

This chapter presented the modelling, design, and experimental validation of a 12 MHz GaN-based isolated dc-dc converter for wall-charging applications, employing an air-core PCB transformer.

The power-stage design process was covered in detail along with the electromagnetic evaluation of the air-core transformer. Discrepancies between simulation and measurement were addressed through a comprehensive parasitic characterisation of the implemented board, validated by VNA measurements.

Experimental tests demonstrated an efficiency of 80.8 % at an output power of 145 W. The impact of layout parasitics was discussed, and power-loss budget estimated from simulation was provided, identifying the rectifier diodes and the transformer as the dominant sources of loss.

Foundations for output-voltage regulation by frequency control were established through a first-harmonic-approximation (FHA) model used to predict the dc-dc conversion gain as a function of switching frequency. The FHA-derived gain was compared against time-domain simulations and measurements, showing very good agreement within the operating range. The model's limitations were also identified, with accuracy degrading as the link-current waveforms departed from sinusoidal behaviour under increased distortion.

Finally, an experimental characterisation of the frequency-dependent voltage gain was provided, demonstrating output voltage regulation across varying loads and input voltages using frequency modulation and duty-cycle adjustments to maintain ZVS.

Chapter 3

Design of a 5 MHz Isolated Class E^2 Push-Pull dc-dc Converter with HF Magnetic Core

The work presented in this chapter is part of two projects conducted at the Wireless Power Lab at Imperial College London, namely "Ultra Compact, High-power Supply Units for the Emerging Energy Demands of AI Data Centres" funded by the Impact Acceleration Account (IAA), and the project "Safe Power Delivery Using a Reconfigurable Mesh of Inductive Transceivers" funded by the Engineering and Physical Sciences Research Council (EPSRC). The author completed a three-month visiting student period at the laboratory during which a substantial portion of this work was carried out.

Chapter 2 presented a 12 MHz air-core implementation. In this chapter, a higher-power prototype is introduced at 5 MHz with a cored transformer. According to [9, 53], air-core inductors surpass cored inductors only well into the VHF range – on a volumetric basis around 50 MHz and on a mass basis around 10 MHz – while cored structures show superior performance in the tens of megahertz. In line with these observations, the operating frequency is set to 5 MHz and a cored transformer, employing a high-frequency ferrite [3], is adopted. A cored design can offer higher inductance per turn, tighter coupling (lower leakage), and better field containment/EMI due to a guided flux path.

The idea is to explore the application of Class E-derived dc-dc conversion [17, 19, 26, 54] for data-centre/server power modules. The hardware presented here is conceived

as a research testbed to probe performance limits and controllability; accordingly, the chosen input/output specifications are not intended to conform to server-module standards, but to enable systematic evaluation of the topology, magnetic design, and control framework. The selected ratings prioritise controllability, safe operation, and instrumentation access, providing a tractable platform for validating the concept before migration to application-specific voltages, power levels, and form factors.

To increase the achievable output power while keeping the input voltage relatively low (so as to limit the device voltage stress inherent to Class E topology) a push-pull configuration was adopted for both the inverter and the rectifier, enabling higher power transfer at the same input voltage by sharing current between two phases [55] and also reducing device voltage stress. Higher power could be achieved by paralleling multiple push-pull blocks [56, 57].

This chapter is organised as follows. First, the power-stage design of the 5 MHz push-pull Class E^2 converter is described in detail, including the high-frequency transformer implementation, key device selections and layout considerations to minimise parasitics. Next, experimental results are presented together with an efficiency discussion supported by a simulation-extracted power-loss budget that identifies the dominant loss mechanisms. Finally, a first harmonic approximation (FHA) model of the dc conversion gain as a function of switching frequency is developed and validated, confirming frequency as an effective control variable for output voltage regulation.

3.1 Power stage design

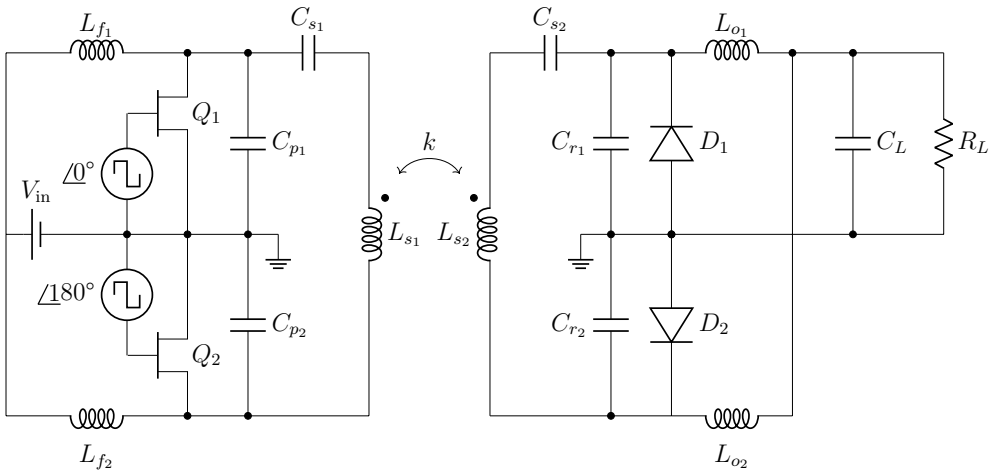


Figure 3.1: Circuit diagram of the Class E^2 push-pull dc-dc converter.

Figure 3.1 shows the schematic of the isolated push-pull Class E^2 dc-dc converter. The topology comprises a push-pull Class E inverter and a complementary push-pull Class E rectifier; galvanic isolation is provided by a high-frequency ferrite-cored transformer. The detailed design and component selection are presented in the following sections.

3.1.1 Rectifier design

The design of the power stage starts, as outlined previously for the air-core dc-dc converter in the preceding chapter, from the design of the rectifier, which relies on the first-order approximation equations derived for the single-ended Class E converter in [15, 29], suitably adapted for the push-pull case.

The dc load resistance R_L is computed from the desired output voltage V_{out} and output power P_{out} as:

$$R_L = \frac{V_{\text{out}}^2}{P_{\text{out}}}. \tag{3.1}$$

For a chosen duty cycle D_{rect} and switching frequency $f = \omega/2\pi$, the shunt capacitance $C_{r_{1,2}}$ is given by:

$$C_{r_{1,2}} = \frac{1 - 2\pi^2(1 - D_{\text{rect}})^2 - \cos(2\pi D_{\text{rect}}) + \dfrac{(2\pi(1 - D_{\text{rect}}) + \sin(2\pi D_{\text{rect}}))^2}{1 - \cos(2\pi D_{\text{rect}})}}{2\pi\,\omega\,R_L}. \tag{3.2}$$

The minimum value of the output inductance $L_{o_{1,2}}$ can be evaluated using the rela-

tionship:

$$L_{o_{1,2}} > L_{o_{\min}} = \frac{V_{\text{out}}(1 - D_{\text{rect}})}{f\,\Delta I_{\text{out}}}, \tag{3.3}$$

where ΔI_{out} is the maximum acceptable peak-to-peak output current ripple.

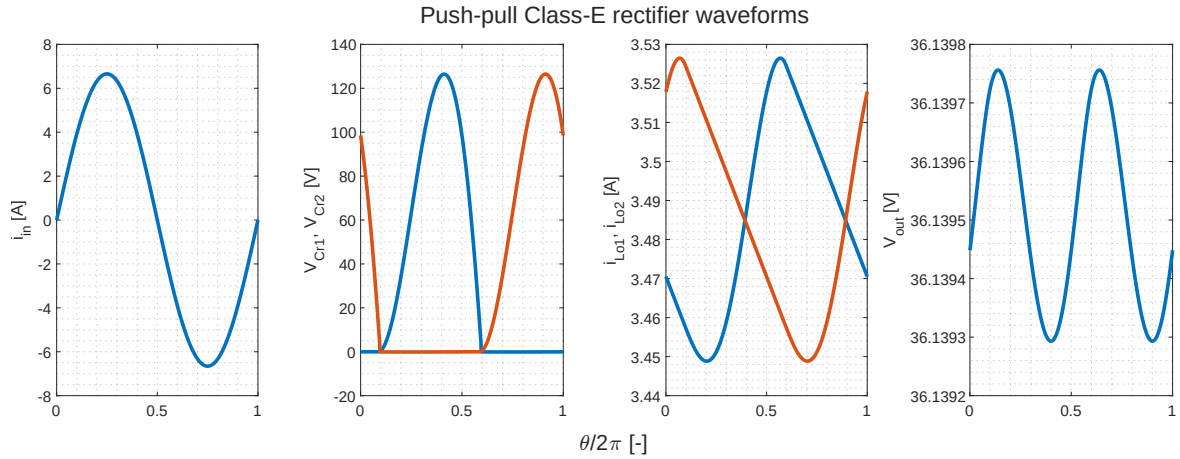


Figure 3.2: Simulated ideal waveforms of the push-pull Class E rectifier.

The constraint on the output capacitance C_L is related to the corner frequency of the output filter, which should be at least a decade below the operating frequency. This yields:

$$C_L > \frac{25}{\pi^2 f^2 L_{o_{\min}}}. \tag{3.4}$$

The input current to the rectifier, $i_{\text{in}}(\theta)$, is expressed as:

$$i_{\text{in}}(\theta) = \frac{V_{\text{out}}}{R_L \sin(\phi_{\text{rect}})} \sin(\theta + \phi_{\text{rect}}), \tag{3.5}$$

where ϕ_{rect} is the input current phase angle:

$$\phi_{\text{rect}} = \arctan\left(\frac{1 - \cos(2\pi D_{\text{rect}})}{2\pi(1 - D_{\text{rect}}) + \sin(2\pi D_{\text{rect}})}\right). \tag{3.6}$$

During the respective off-time intervals, the voltage across the shunt capacitances $C_{r_{1,2}}$ is given by:

$$v_{C_{r_{1,2}}}(\theta) = \frac{I_o}{\omega C_r}\left[\theta - \sin(\theta) + \frac{\cos(\theta) - 1}{\tan(\phi_{\text{rect}})}\right]. \tag{3.7}$$

Table 3.1 summarises the parameters of the designed rectifier, obtained from the above analytical expressions.

The simulated rectifier waveforms obtained for the selected parameters under ideal switching conditions are shown in Fig. 3.2.

Table 3.1: Component values for the push-pull Class E rectifier.

Parameter	Value
V_{out}	36 V
P_{out}	250 W
f	5 MHz
D_{rect}	0.5
$L_{o_{1,2}}$	54 µH
$C_{r_{1,2}}$	1.05 nF
C_L	1.2 µF

3.1.2 High-Frequency Transformer Design

The transformer was designed using a commercially available Fair-Rite Material 67 toroidal core (5967003801) [58]. Material 67 by FairRite is a nickel-zinc ferrite, which is characterised by low permeability ($\mu_i = 40$) and a high resistivity ($\rho = 1 \times 10^7\,\Omega \cdot$ cm) [3]. The optimal frequency range for this material is between 5 MHz and 20 MHz, as can be seen from the complex permeability graph $\mu_r = \mu_r' - j\mu_r''$ in Fig. 3.3, where the imaginary term of the permeability accounts for the core losses [3, 59].

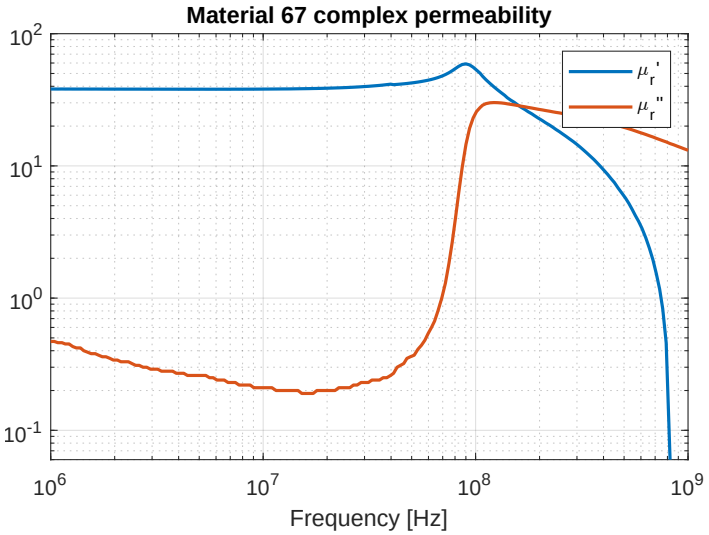


Figure 3.3: Complex permeability of Fair-Rite Material 67, from the manufacturer's material datasheet [3].

The choice of the transformer self-inductances resulted from a trade-off between minimising winding losses – since the objective was to assess the performance of the high-frequency core material – and the practical constraints of system design and physical implementation. In particular, a sufficiently high primary inductance was required to ensure a quasi-sinusoidal inverter current, while the number of turns had to remain adequate for both magnetic coupling and the mechanical feasibility of securely

winding the 1.5 mm enamelled copper wire around the toroidal core. The resulting configuration employs four turns on the primary and two turns on the secondary.

To maximise magnetic coupling, the windings were arranged in an interleaved configuration. A photograph of the realised transformer is shown in Fig. 3.4. Figures 3.5-3.7 present the screen captures from the Keysight E4990A impedance analyser used for the characterisation of the implemented transformer.

From the open-secondary impedance measurement, the primary self-inductance L_{s_1} was found to be 1.57 µH. The secondary self-inductance L_{s_2}, extracted from the open-primary measurement, was equal to 492 nH. The coupling coefficient k was determined according to

$$k = \sqrt{1 - \frac{L_{s_1}^{SC}}{L_{s_1}}}, \tag{3.8}$$

where $L_{s_1}^{SC}$ is the primary short-circuit inductance, obtained by measuring the primary impedance with the secondary shorted. The shorted-secondary impedance is shown in Fig. 3.7 and the resulting $L_{s_1}^{SC}$ was found to be equal to 466 nH. Table 3.2 summarises the key transformer parameters.

Table 3.2: Parameters of the implemented transformer.

Parameter	**Value**
Primary inductance L_{s_1}	1.57 µH
Secondary inductance L_{s_2}	492 nH
Primary short-circuit inductance $L_{s_1}^{SC}$	466 nH
Coupling coefficient k	0.8385
Primary turns N_1	4
Secondary turns N_2	2
Wire diameter	1.5 mm (enameled Cu wire)
Core material	Fair-Rite 67 (part no. 5967003801)

(a) Top view of the implemented transformer.

(b) Lateral view of the implemented transformer.

Figure 3.4: Photographs of the implemented transformer prototype.

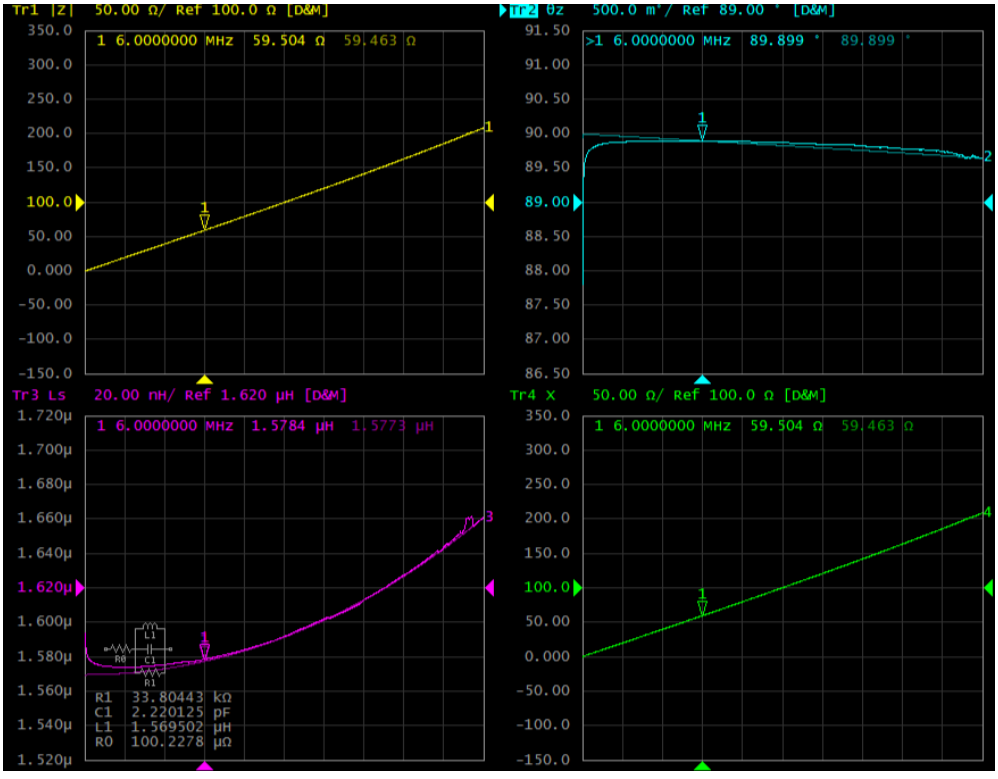


Figure 3.5: E4990A Impedance Analyser screen-capture: open-secondary impedance. The image shows the primary inductance value and its Q factor.

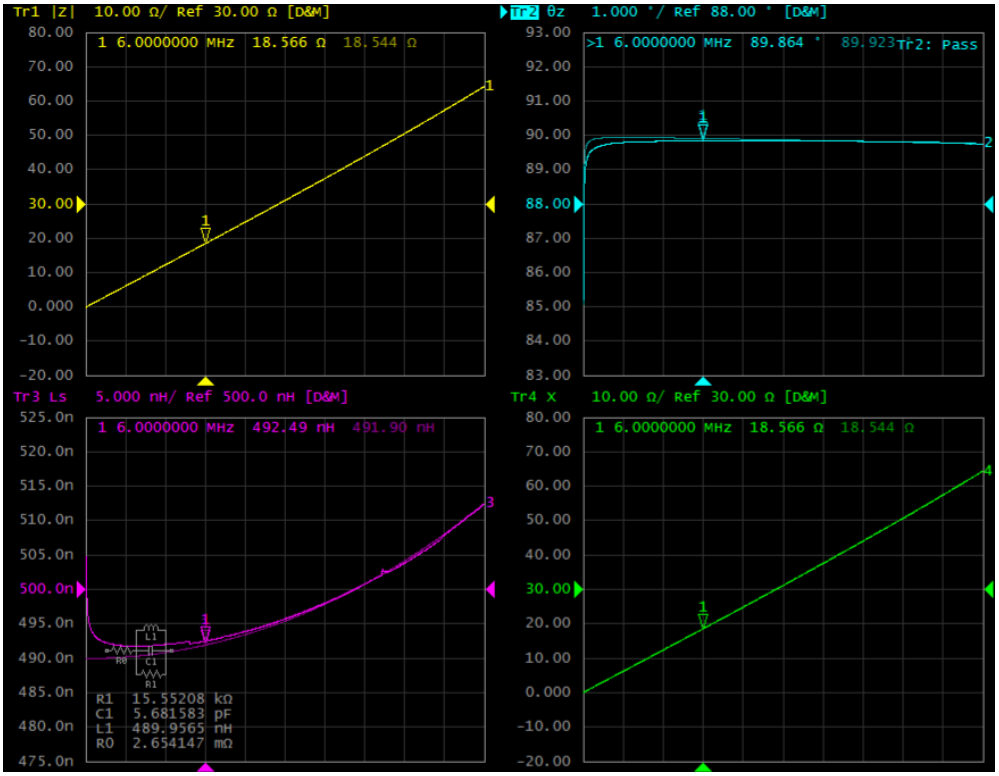


Figure 3.6: E4990A Impedance Analyser screen-capture: open-primary impedance. The image shows the secondary inductance value and its Q factor.

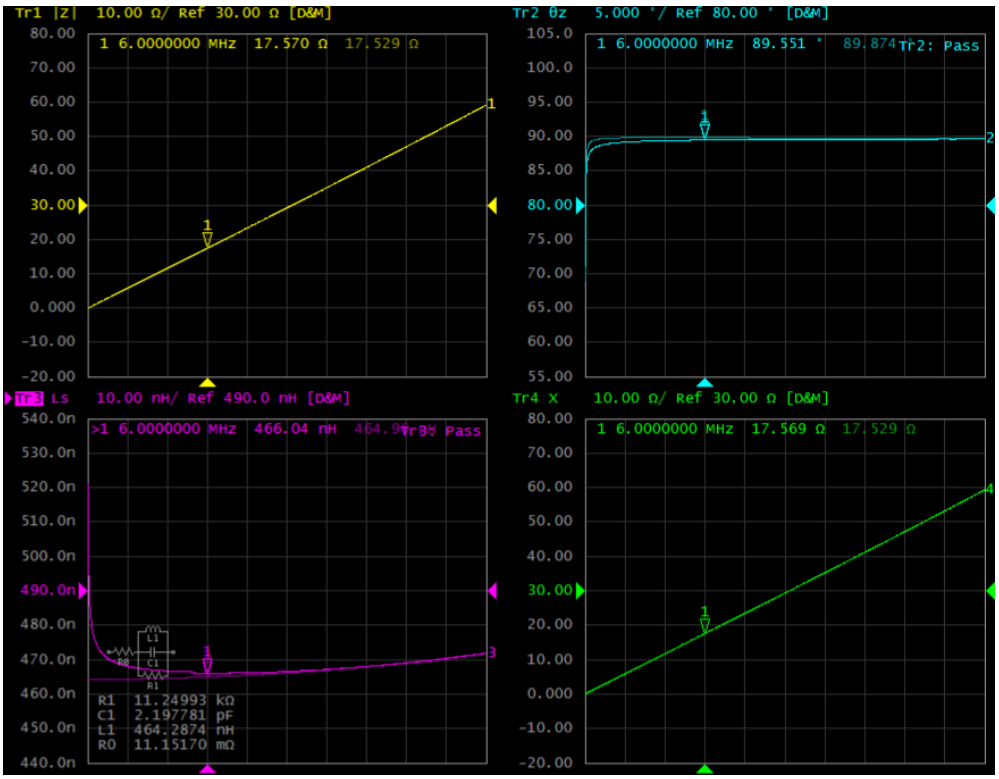


Figure 3.7: E4990A Impedance Analyser screen-capture: shorted-secondary impedance. The image shows the short-circuit primary inductance value used to evaluate the coupling coefficient.

3.1.3 Inverter design

Following the same approach described for the air-core design, the design of the inverter requires the evaluation of the reflected impedance as seen from the primary side, $\overline{Z}\text{eq}$, given by (2.12)-(2.13), where the rectifier input impedance $\overline{Z}\text{in}_{\text{rect}} = R_{\text{in}_{\text{rect}}} + jX_{\text{in}_{\text{rect}}}$ is expressed as [15, 18, 23]:

$$R_{\text{in}_{\text{rect}}} = 8R_L \sin^2(\phi_{\text{rect}}) \tag{3.9}$$

$$\begin{aligned} X_{\text{in}_{\text{rect}}} = -\frac{1}{\pi^2 f\omega C_r}\Big(&\pi(1-D_{\text{rect}}) + \sin(2\pi D_{\text{rect}}) - \frac{1}{4}\cos(2\phi_{\text{rect}})\sin(4\pi D_{\text{rect}}) \\ &- \frac{1}{2}\sin(2\phi_{\text{rect}})\sin^2(2\pi D_{\text{rect}}) \\ &- 2\pi(1-D_{\text{rect}})\sin(\phi_{\text{rect}})\sin(2\pi D_{\text{rect}} - \phi_{\text{rect}})\Big). \end{aligned} \tag{3.10}$$

where ϕ_{rect} is given by (3.6) and D_{rect} denotes the duty cycle of the rectifier diodes. As in the other design case, to ensure a high enough Q-factor at primary side, the converter operates off resonance at the secondary. In particular, the resonance factor γ was chosen equal to 1.48 to achieve a loaded Q-factor equal to 5.5. The equivalent impedance $\overline{Z}_{\text{eq}} = R_{\text{eq}} + jX_{\text{eq}}$ is then employed as the load of the inverter in the design equations [15].

For a given desired output power P_{out} and input voltage V_{in}, assuming $P_{\text{out}} = P_{\text{in}}$ yields a relationship between the amplitude of the sinusoidal output current of the inverter I_m and the input dc current $I_{\text{in}} = P_{\text{out}}/V_{\text{in}}$ [15]:

$$\frac{I_m}{I_{\text{in}}} = \frac{2\pi(1-D_{\text{inv}})}{\cos(2\pi D_{\text{inv}} + \phi_{\text{inv}}) - \cos(\phi_{\text{inv}})}, \tag{3.11}$$

where D_{inv} is the inverter duty cycle and ϕ_{inv} is the initial phase of the output current with respect to the gate signals, expressed as:

$$\phi_{\text{inv}} = \pi + \arctan\left(\frac{\cos(2\pi D_{\text{inv}}) - 1}{2\pi(1-D_{\text{inv}}) + \sin(2\pi D_{\text{inv}})}\right). \tag{3.12}$$

Substituting (3.12) into (3.11) yields an equation in which the only unknown is D_{inv}, which can be solved numerically.

The shunt capacitance $C_{p_{1,2}}$ is calculated as:

$$\begin{aligned} C_{p_{1,2}} = &\frac{1}{\omega R_{\text{eq}}}\left[(1-D_{\text{inv}})\pi\cos(\pi D_{\text{inv}}) + \sin(\pi D_{\text{inv}})\right] \\ &\cdot \frac{2\sin(\pi D_{\text{inv}})\cos(\pi D_{\text{inv}} + \phi_{\text{inv}})\sin(\pi D_{\text{inv}} + \phi_{\text{inv}})}{\pi^2(1-D_{\text{inv}})}. \end{aligned} \tag{3.13}$$

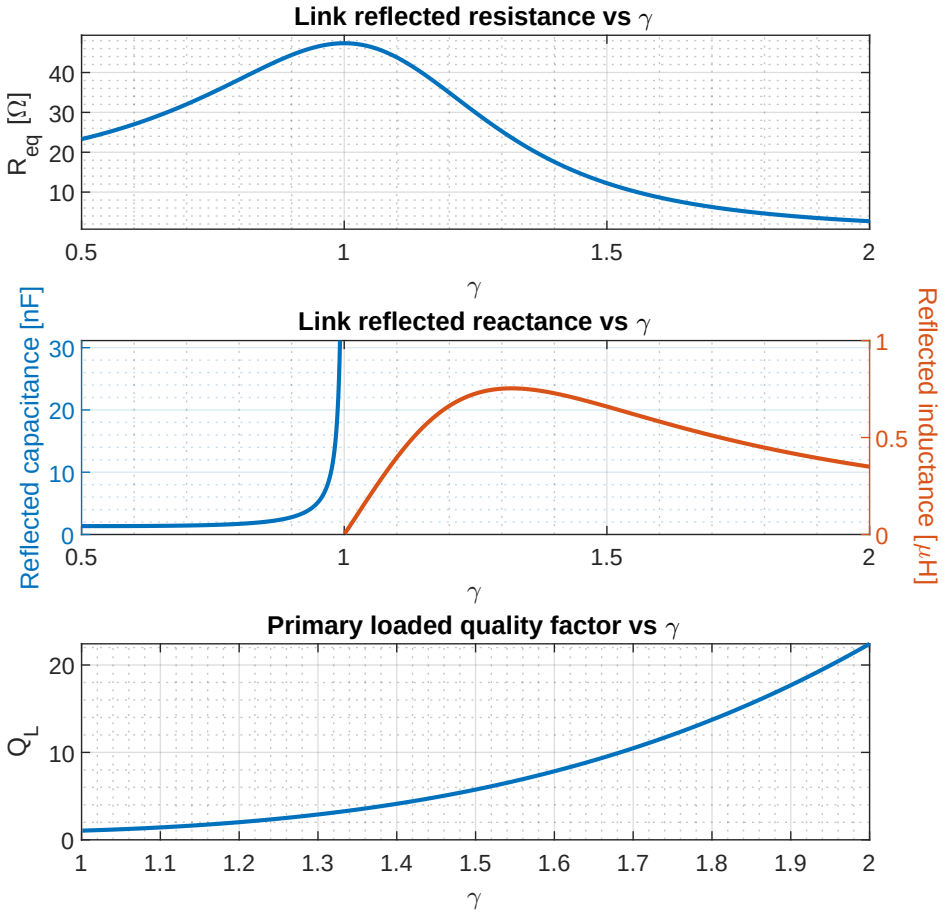


Figure 3.8: Effect of the resonance factor γ on the reflected impedance of the link. (Top) Reflected resistance R_{eq}, (middle) reflected reactance expressed as equivalent capacitance and inductance, and (bottom) primary loaded quality factor Q_{L}.

The output inductance L_{eq} can be split into two components, $L_{\text{eq}} = L_b + L_a$, where L_a resonates with the output tank capacitor C_{s_1} at the switching frequency $f = \omega/2\pi$. Therefore,

$$C_{s_1} = \frac{1}{2\omega^2(L_{\text{eq}} - L_b)}, \tag{3.14}$$

where

$$L_b = \frac{1}{\pi\,\omega^2\,C_p}\Big(\tfrac{3}{2}\cos\phi\sin\phi + 2\pi(1-D)\sin^2\phi - 2\cos(2\pi D+\phi)\sin\phi \\ + \pi(1-D) + \tfrac{1}{4}\sin(4\pi D + 2\phi)\Big). \tag{3.15}$$

Equations (3.11)-(3.15) provide the analytical starting point for the inverter design, but parameters (particularly C_{s_1} and C_p) must be refined using time-domain simulations of the complete dc-dc converter, including the transformer and rectifier, to ensure ZVS operation. This refinement is necessary because the analytical derivation

assumes purely sinusoidal currents in the link; in practice, harmonic components cause deviations from the idealised theoretical results.

Table 3.3 summarises the final parameters of the designed inverter.

Table 3.3: Component values for the push-pull Class E inverter.

Parameter	Value
V_{in}	60 V
f	5 MHz
$L_{f_{1,2}}$	81 µH
$C_{p_{1,2}}$	1.02 nF
C_{s_1}	740 pF

3.1.4 Final tuning and PCB layout

Once the ideal component values were obtained, time-domain simulations including the non-linear models of the selected switching devices (GS-065-030-2-L GaN transistors for the inverter and C6D10065Q SiC diodes for the rectifier) were performed. These simulations required additional tuning of the design parameters to account for the effects of the devices' non-linear capacitances as well as deviations from the high-Q assumption, since the primary and secondary currents are not perfectly sinusoidal. The final component values and device selections used in the hardware prototype are summarised in Table 3.4.

Table 3.4: Parameters values and components of the implemented dc-dc prototype.

Parameter/Component	Value	Description
$L_{f_{1,2}}$	81 µH	3×SER2211-273MED
$L_{o_{1,2}}$	54 µH	2×SER2211-273MED
$C_{p_{1,2}}$	360 pF	C0G 1812
$C_{r_{1,2}}$	945 pF	C0G 1812
C_{s_1}	740 pF	C0G 3838
C_{s_2}	1.5 nF	C0G 3838
C_L	1.2 µF	C0G 1812
GaN HEMTs $Q_{1,2}$	-	GS-065-030-2-L
SiC diodes $D_{1,2}$	-	C6D10065Q
Gate drivers for $Q_{1,2}$	-	BD2311NVX
Opto-isolators	-	TLP2767
Trimmable HV capacitors	$10 - 100$ pF	AJ20-4

Figure 3.9 presents the 3D rendering of the printed circuit board (PCB) layout developed in *Altium Designer* [4]. In this design, compactness was not the primary objective;

rather, the layout was conceived to facilitate experimental testing and troubleshooting. Accordingly, a modular architecture was adopted, comprising two separate boards for the inverter and rectifier stages. From a layout and component-rating perspective, the board was dimensioned to support output powers well above 260 W, which is the operating point chosen for controller development and validation, illustrated in 4. Given the inherent symmetry between the inverter and rectifier topologies (both implementing a push-pull Class E configuration) a single PCB layout was employed for both stages. This approach simplifies design and assembly while promoting an even distribution of PCB-related parasitics between the two modules.

Two low-side single-channel high-frequency gate drivers by ROHM (BD2311NVX) were employed. To provide galvanic isolation, two opto-isolators by Toshiba (TLP2767), denoted by `ICx`, were placed upstream of the gate drivers. The driving signals can be supplied externally through the SMA connectors `JPWM_1` and `JPWM_2`. The input lines can be 50 Ω-matched using resistors `R1` and `R3`. The boards were also designed to accommodate high-voltage, high-precision trimmable capacitors in the pF range, denoted as `CTRIMx`, for potential fine-tuning if required. Additionally, spring-loaded connectors were included to facilitate easy replacement of the series compensation capacitors.

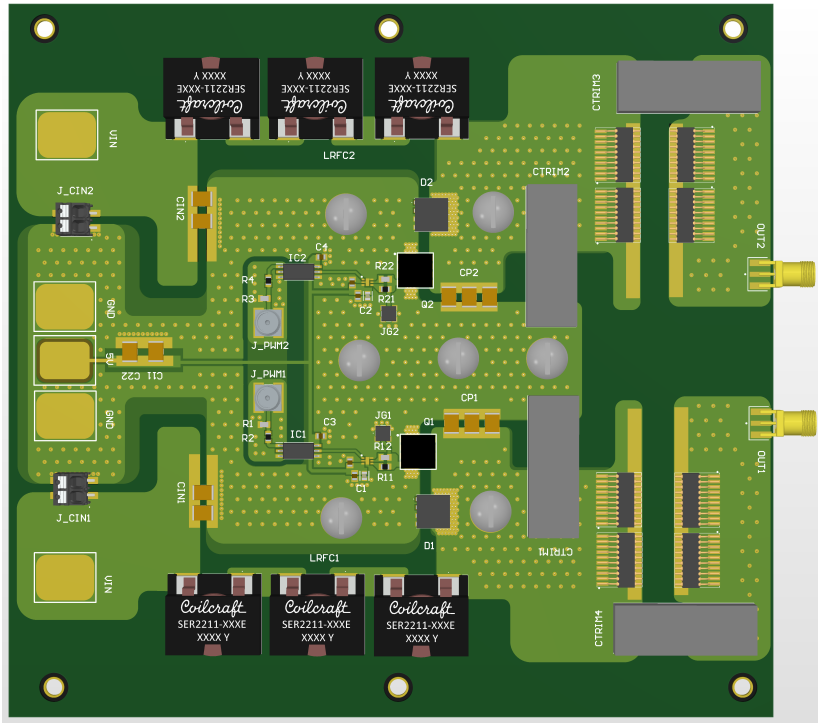


Figure 3.9: PCB layout of the inverter/rectifier boards in *Altium Designer* [4].

None of these fine-tuning provisions were ultimately required, as the PCB layout was

designed to minimise parasitic effects. In particular, no ground plane was placed beneath the choke inductors or under the switching devices to reduce parasitic capacitances, while the power tracks were deliberately made wide to minimise parasitic inductance.

3.2 Experimental Results

Figure 3.10 shows the experimental setup used to measure the dc-dc efficiency of the implemented converter. Optically isolated probes (Tektronix IsoVu) were used to measure the device drain voltage. The STM32 microcontroller board used for closed-loop control is also visible in the photograph (the controller design is presented in Chapter 4). The converter was supplied by a DC source (Keysight N8740A) and loaded with an electronic load (B&K Precision 8612). A power analyser (Yokogawa WT332E) measured dc-dc efficiency.

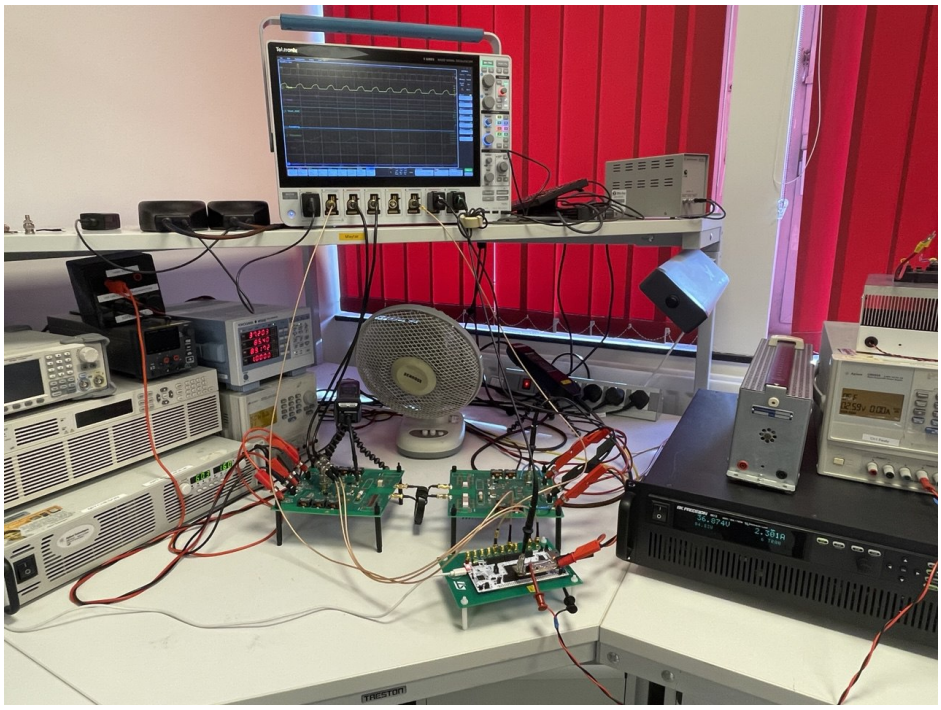


Figure 3.10: Bench setup for efficiency measurements

At a maximum output power of 260 W ($V_{\text{out}} \approx 36\,\text{V}$, $I_{\text{out}} \approx 7.2\,\text{A}$), the measured efficiency is $\eta = 90.8\,\%$.

Time-domain simulations using non-linear device and choke models were performed to estimate the loss budget. The transformer core losses P_v were also estimated by computing the peak flux density B_{pk} in the magnetic core and using the manufacturer's

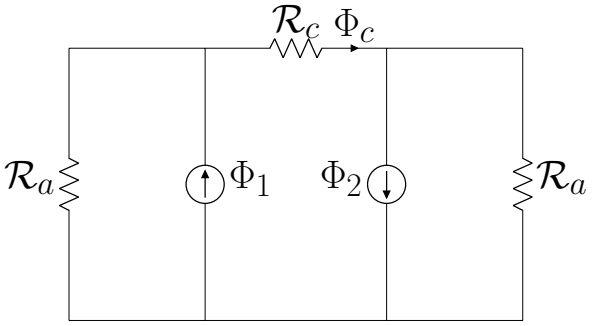


Figure 3.11: Reluctance model of the transformer.

material curves of volumetric power loss versus B_{pk} (Fig. 3.12).

The flux computation uses the reluctance model of Fig. 3.11, where $\mathcal{R}_c$ is the core reluctance and $\mathcal{R}_a$ represents the leakage path in air due to the material's low permeability. The magnetic flux is

$$\Phi_i = A_e B_i, \tag{3.16}$$

with A_e the core cross-section. The flux density is obtained from the simulated inductor voltage $V_{L_{s_i}}$ via

$$B_i = \frac{1}{N_i A_e} \int V_{L_{s_i}} \, \mathrm{d}t, \tag{3.17}$$

where N_i denotes the effective number of turns,

$$N_i = \sqrt{L_{s_i} \, \mathcal{R}_{\mathrm{eff}}}, \qquad \mathcal{R}_{\mathrm{eff}} = \left(\frac{1}{\mathcal{R}_c} + \frac{1}{\mathcal{R}_a} \right)^{-1}. \tag{3.18}$$

Using

$$L_{s_1} = N_1^2 \left(\frac{1}{\mathcal{R}_c} + \frac{1}{\mathcal{R}_a} \right), \quad L_{s_2} = N_2^2 \left(\frac{1}{\mathcal{R}_c} + \frac{1}{\mathcal{R}_a} \right), \quad M = \frac{N_1 N_2}{\mathcal{R}_c}, \tag{3.19}$$

the coupling coefficient is

$$k = \frac{M}{\sqrt{L_{s_1} L_{s_2}}} = \frac{\frac{1}{\mathcal{R}_c}}{\frac{1}{\mathcal{R}_c} + \frac{1}{\mathcal{R}_a}} = \frac{\mathcal{R}_a}{\mathcal{R}_a + \mathcal{R}_c}. \tag{3.20}$$

From the above,

$$\mathcal{R}_a = \frac{k}{1-k} \, \mathcal{R}_c, \qquad \mathcal{R}_{\mathrm{eff}} = k \, \mathcal{R}_c. \tag{3.21}$$

The core flux Φ_c follows directly from Fig. 3.11 and (3.16); the peak flux density is $B_{\mathrm{pk}} = \Phi_{c_{pk}} / A_e$. In simulation, $B_{\mathrm{pk}} \approx 15.5\,\mathrm{mT}$, yielding approximately 8 W of core loss at 25 °C from the Material 67 data.

Figure 3.13 summarises the simulated loss partition, scaled to the measured total loss at $P_{\mathrm{out}} = 260$ W and $\eta = 90.8\%$. The dominant contributor is the diode conduction loss (∼33%, ∼8.8 W), roughly three times the GaN devices losses. Replacing

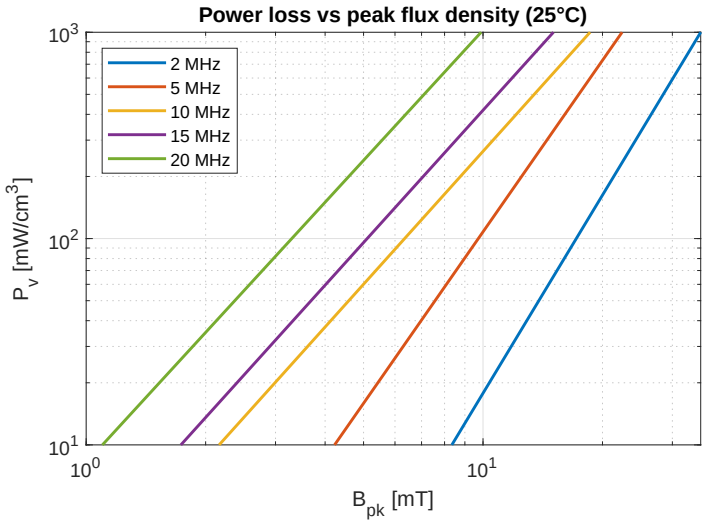


Figure 3.12: Volumetric power loss of Fair-Rite Material 67 as a function of peak flux density at 25 °C, from the manufacturer's material datasheet [3].

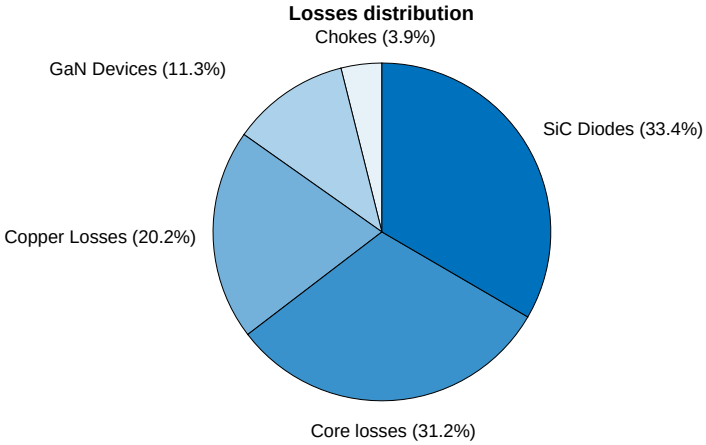


Figure 3.13: Estimated loss distribution of the implemented converter at $P_{\text{out}} = 260\,\text{W}$, $\eta = 90.8\,\%$.

the diodes with synchronous rectification is therefore expected to improve overall efficiency by about 2-3 percentage points at this operating point. Core losses form the second-largest slice (∼31%, ∼8.2 W), suggesting that reducing B_{pk} would be beneficial. Regarding the active devices, further savings are possible by lowering package inductance. For example, simulations with a lower-inductance package (GS66508B) indicate an incremental efficiency gain of ∼0.4 percentage points under the same test conditions.

3.3 State-space representation of the push-pull Class E inverter

In this section, the state-space representation of the push-pull Class E inverter is briefly recalled, since it will be required in the following section to extract the dc voltage gain curves of the converter. The derivation follows the same methodology and notation as presented in [31], adapted here to the push-pull Class E inverter. Fig. 3.14 shows the circuit diagram of the inverter, where L_{eq} and R_{eq} represent respectively the imaginary and real components of the link reflected impedance.

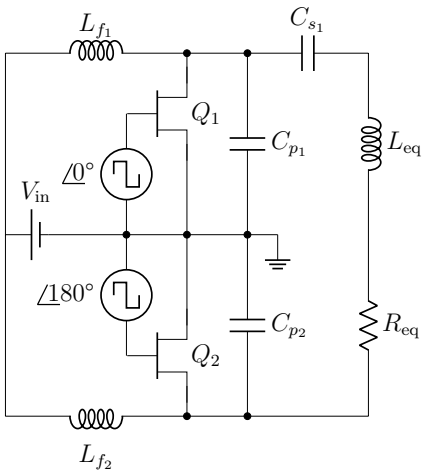


Figure 3.14: Circuit diagram of the push-pull Class E inverter. L_{eq} and R_{eq} represent the real and imaginary part of the link reflected impedance.

The inverter can be represented in state-space form as

$$\dot{\mathbf{q}}(\theta) = \mathbf{A}(\theta)\,\mathbf{q}(\theta) + \mathbf{b}\,u(\theta), \tag{3.22}$$

where $u(\theta)$ is the unit step function, and the state and input vectors are defined as

$$\mathbf{q}(\theta) = \begin{bmatrix} i_{Lf_1}(\theta) & i_{Lf_2}(\theta) & v_{Cp_1}(\theta) & v_{Cp_2}(\theta) & v_{Cs_1}(\theta) & i_{L_{eq}}(\theta) \end{bmatrix}^T, \tag{3.23}$$

$$\mathbf{b} = \frac{V_{\text{in}}}{\omega} \begin{bmatrix} \frac{1}{L_{f_1}} & \frac{1}{L_{f_2}} & 0 & 0 & 0 & 0 \end{bmatrix}^T. \tag{3.24}$$

The state matrix $\mathbf{A}(\theta)$, describing the inverter dynamics, takes the form

$$\mathbf{A}(\theta) = \frac{1}{\omega}\begin{bmatrix} 0 & 0 & -\frac{1}{L_{f_1}} & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{L_{f_2}} & 0 & 0 \\ \frac{1}{C_{p_1}} & 0 & -\frac{1}{C_{p_1}R_{Q_1}(\theta)} & 0 & 0 & -\frac{1}{C_{p_1}} \\ 0 & \frac{1}{C_{p_2}} & 0 & -\frac{1}{C_{p_2}R_{Q_2}(\theta)} & 0 & \frac{1}{C_{p_2}} \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{C_{s_1}} \\ 0 & 0 & \frac{1}{L_{\text{eq}}} & -\frac{1}{L_{\text{eq}}} & -\frac{1}{L_{\text{eq}}} & -\frac{R_{\text{eq}}}{L_{\text{eq}}} \end{bmatrix}. \tag{3.25}$$

Here, $R_{Q_i}(\theta)$ represents the conduction state of device Q_i, which is given by

$$R_{Q_i}(\theta) = \begin{cases} R^{\text{ON}}, & \text{if switch } Q_i \text{ is ON}, \\ R^{\text{OFF}}, & \text{if switch } Q_i \text{ is OFF}. \end{cases} \tag{3.26}$$

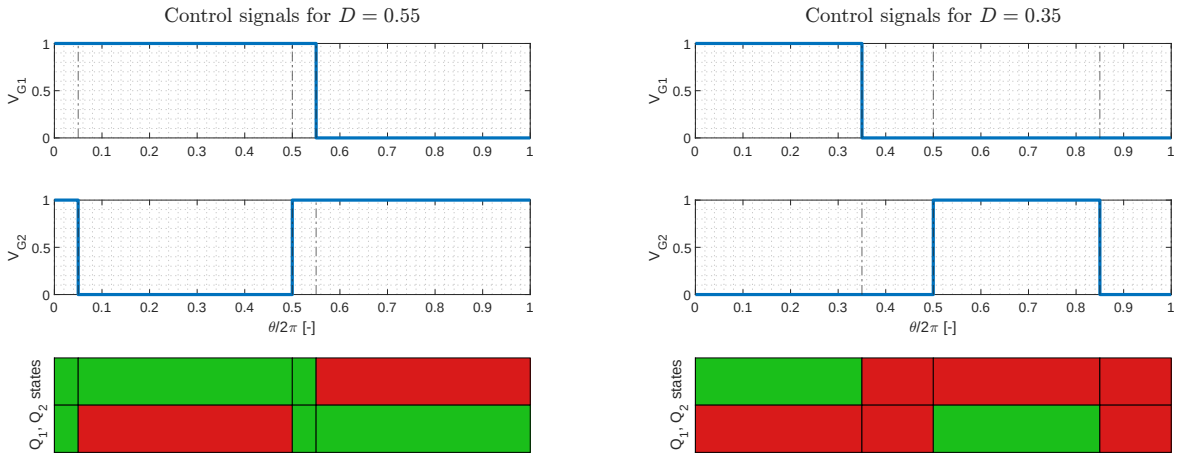


Figure 3.15: Switching cases for two different duty cycles. Red colour denotes the OFF state of the switch while green colour denotes the ON state.

The two devices operate with 180° phase shift and, depending on the duty cycle D, there are four possible switching cases (SC) that can occur within one period:

$$\text{SC} = \begin{bmatrix} Q_1 \\ Q_2 \end{bmatrix} \in \left\{ \begin{bmatrix} 0 \\ 0 \end{bmatrix}, \begin{bmatrix} 0 \\ 1 \end{bmatrix}, \begin{bmatrix} 1 \\ 0 \end{bmatrix}, \begin{bmatrix} 1 \\ 1 \end{bmatrix} \right\}, \tag{3.27}$$

where '0" denotes an OFF switch and '1" a ON device. Fig. 3.15 illustrates the switching cases for two different duty cycles.

Thus, the differential equation in (3.22) is solved in a piece-wise linear manner in each interval $[\theta_k, \theta_{k+1}]$ in the period characterised by a different switching case. Within each

interval $[\theta_k, \theta_{k+1}]$, the state matrix $\mathbf{A}(\theta) = \mathbf{A}_k$ is constant and the solution of (3.22) is given by

$$\mathbf{q}(\theta)|_{[\theta_k,\theta_{k+1}]} = e^{\mathbf{A}_k(\theta-\theta_k)}\,\mathbf{q}_k(0) + \mathbf{A}_k^{-1}\left(e^{\mathbf{A}_k(\theta-\theta_k)} - \mathbf{I}\right)\mathbf{b}. \tag{3.28}$$

where $\mathbf{I}$ is the identity matrix and $\mathbf{q}_k(0) = \mathbf{q}(\theta_k)$.

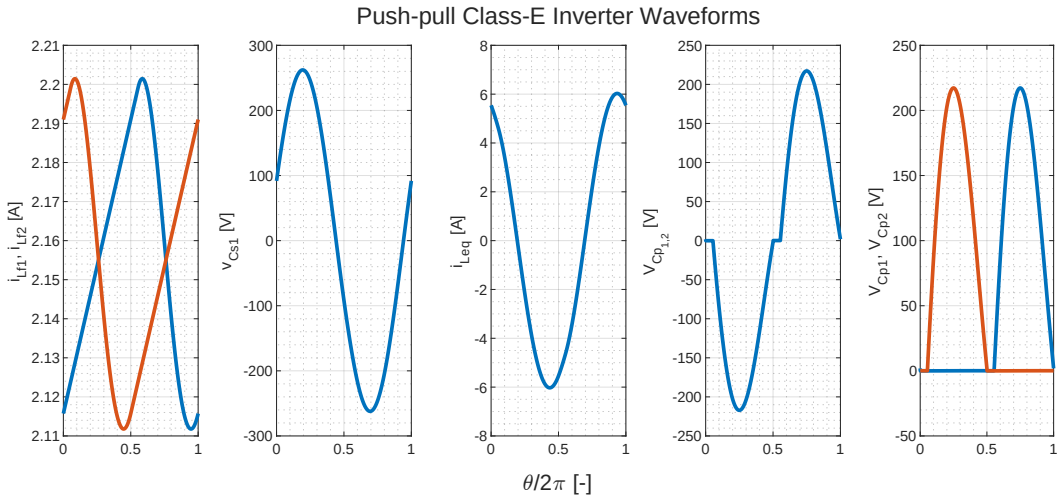


Figure 3.16: Waveforms of the push-pull Class E inverter obtained from the solution of the state-space representation.

Continuity of the state vector at each switching boundary requires

$$\mathbf{q}(\theta_k)|_{[\theta_{k-1},\theta_k]} = \mathbf{q}(\theta_k)|_{[\theta_k,\theta_{k+1}]}, \tag{3.29}$$

Assuming N switching cases in one period, the boundary conditions can be compactly expressed as

$$\mathbf{q}(0) = \mathbf{C}^{-1}\mathbf{E}, \tag{3.30}$$

where

$$\mathbf{E} = \begin{bmatrix} A_1^{-1}\left(e^{(\theta_2-\theta_1)A_1} - I\right)b \\ A_2^{-1}\left(e^{(\theta_3-\theta_2)A_2} - I\right)b \\ \vdots \\ A_N^{-1}\left(e^{(\theta_{N+1}-\theta_N)A_N} - I\right)b \end{bmatrix}, \tag{3.31}$$

$$\mathbf{C} = \begin{bmatrix} -e^{(\theta_2-\theta_1)A_1} & I & Z & \cdots & Z \\ Z & -e^{(\theta_3-\theta_2)A_2} & I & \cdots & Z \\ Z & Z & -e^{(\theta_4-\theta_3)A_3} & \ddots & Z \\ \vdots & \vdots & \ddots & \ddots & I \\ I & Z & \cdots & Z & -e^{(\theta_{N+1}-\theta_N)A_N} \end{bmatrix}, \tag{3.32}$$

with Z denoting the zero matrix. The last block row enforces periodicity by relating the state at $\theta_{N+1} = 2\pi$ to the initial state at $\theta_1 = 0$.

It is noted that this representation does not account for switch reverse conduction [31]. Accordingly, in the practical computation (performed in MATLAB), reverse conduction is handled by iteratively checking for zero crossings of the device drain-source voltage prior to the intended turn-on instant. If a zero crossing is detected, the switching boundaries are adjusted and the computation of the solution repeated until no zero crossings occur. The procedure can be further refined following the approach described in [31].

Fig. 3.16 shows the waveforms of the push-pull Class E inverter obtained from the solution of the state-space representation derived in this section. The output tank voltage $v_{C_{p_{1,2}}} = v_{C_{p_1}} - v_{C_{p_2}}$ is also shown as it will be used in the next section for the derivation of the converter dc voltage gain.

3.4 First Harmonic Approximation of the Class E^2 Push-Pull Converter

Following the same methodology used in Section 2.4.1 to derive the first harmonic approximation (FHA) model of the Class EF$_2$ dc-dc converter, an FHA model was developed here for the Class E^2 push-pull converter under study. From this model, the corresponding dc voltage gain curves as a function of the switching frequency are obtained. The purpose, as before, is to demonstrate the capability of regulating the output voltage by means of frequency control.

The push-pull Class E inverter applies a near-sinusoidal wave voltage $v_{C_{p1,2}} = v_{C_{p1}} - v_{C_{p2}}$ (the difference between the two complementary devices drain voltages) to the primary resonant tank, which suppresses higher-order harmonics, resulting in an approximately sinusoidal current at the input of the link. The FHA model replaces the inverter with a sinusoidal voltage source equal to the fundamental component of $C_{p_{1,2}}$ and the link and rectifier with an equivalent impedance, as illustrated in Fig. 3.17.

As done in the previous case, the rectifier is modelled as an equivalent input impedance $\overline{Z}_{\text{in}_{\text{rect}}}(f, R_L)$ at the fundamental frequency, which depends on both the switching frequency and the dc load R_L:

$$\overline{Z}_{\text{in}_{\text{rect}}}(f, R_L) = R_{\text{in}_{\text{rect}}}(f, R_L) + jX_{\text{in}_{\text{rect}}}(f, R_L) \tag{3.33}$$

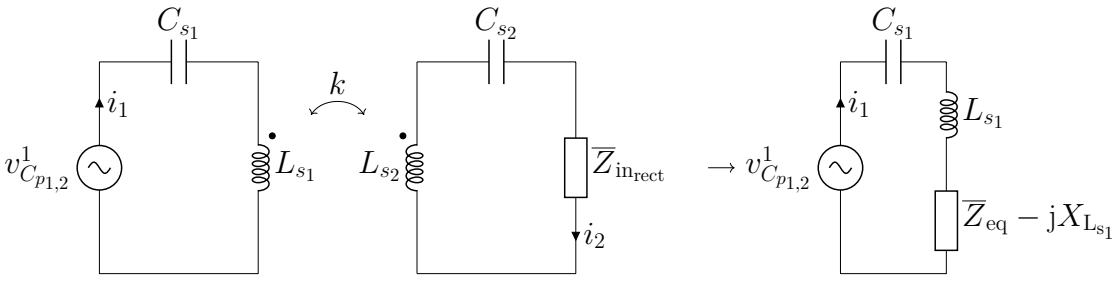


Figure 3.17: FHA model for the push-pull Class E^2 dc-dc converter.

The input impedance of the push-pull class E rectifier can be derived by adapting the equations originally developed for the single-ended class E rectifier [15]. The real and imaginary parts of the rectifier input impedance are expressed as

$$R_{\text{in}_{\text{rect}}} = 8R_L \sin^2(\phi_{\text{rect}}) \tag{3.34}$$

$$X_{\text{in}_{\text{rect}}} = -\frac{1}{\pi^2 f\omega C_r}\Big(\pi(1-D_{\text{rect}}) + \sin(2\pi D_{\text{rect}}) - \frac{1}{4}\cos(2\phi_{\text{rect}})\sin(4\pi D_{\text{rect}}) - \frac{1}{2}\sin(2\phi_{\text{rect}})\sin^2(2\pi D_{\text{rect}}) - 2\pi(1-D_{\text{rect}})\sin(\phi_{\text{rect}})\sin(2\pi D_{\text{rect}}-\phi_{\text{rect}})\Big). \tag{3.35}$$

where ϕ_{rect} is given by

$$\phi = \arctan\left(\frac{1-\cos(2\pi D_{\text{rect}})}{\sin(2\pi D_{\text{rect}}) + 2\pi(1-D_{\text{rect}})}\right), \tag{3.36}$$

and D_{rect} is the effective duty cycle of the rectifier diodes.

For a given switching frequency f and load R_L, the duty cycle $D_{\text{rect}}(f, R_L)$ is determined by solving the non-linear equation

$$1 - 2\pi^2(1-D_{\text{rect}})^2 - \cos(2\pi D_{\text{rect}}) + \frac{\left[2\pi(1-D_{\text{rect}}) + \sin(2\pi D_{\text{rect}})\right]^2}{1-\cos(2\pi D_{\text{rect}})} - 8\pi^2 f C_r R_L = 0, \tag{3.37}$$

Since no closed-form solution for D_{rect} exists, the equation must be solved numerically. For a given range of load resistance R_L and switching frequency f, the solution can be efficiently obtained using iterative root-finding algorithms such as Newton-Raphson `fzero` function in MATLAB.

Figure 3.18 shows the input impedance of the push-pull Class E rectifier, $\overline{Z}_{\text{in}_{\text{rect}}}$, with its real and imaginary components plotted as a function of the switching frequency f for different load resistances R_L. The curves were obtained from the analytical expressions (3.34)-(3.35).

This rectifier input impedance is then used to evaluate the reflected impedance of the link, as seen from the primary side, $\overline{Z}_{\text{eq}}(f, R_L)$, by means of (2.12)-(2.13).

The equivalent impedance $\overline{Z}_{\text{eq}}$ is employed as the load of the push-pull Class E inverter in its state-space representation, described in 3.3. This allows the computation of the voltage $v_{C_{p_{1,2}}}$ across the inverter output tank and the extraction of its fundamental component amplitude $V^1_{C_{p_{1,2}}}$:

$$V^1_{C_{p_{1,2}}} = \sqrt{\left(V^1_{C_{p_{1,2}}I}\right)^2 + \left(V^1_{C_{p_{1,2}}Q}\right)^2}$$

where the in-phase (I) and quadrature (Q) components are obtained by Fourier integration over one switching period ($\theta = \omega t \in [0, 2\pi]$):

$$\begin{aligned} V^1_{C_{p1,2}I} &= \frac{1}{\pi}\int_0^{2\pi} v_{C_{p1,2}}(\theta)\,\cos\theta\,d\theta, \\ V^1_{C_{p1,2}Q} &= \frac{1}{\pi}\int_0^{2\pi} v_{C_{p1,2}}(\theta)\,\sin\theta\,d\theta. \end{aligned} \tag{3.38}$$

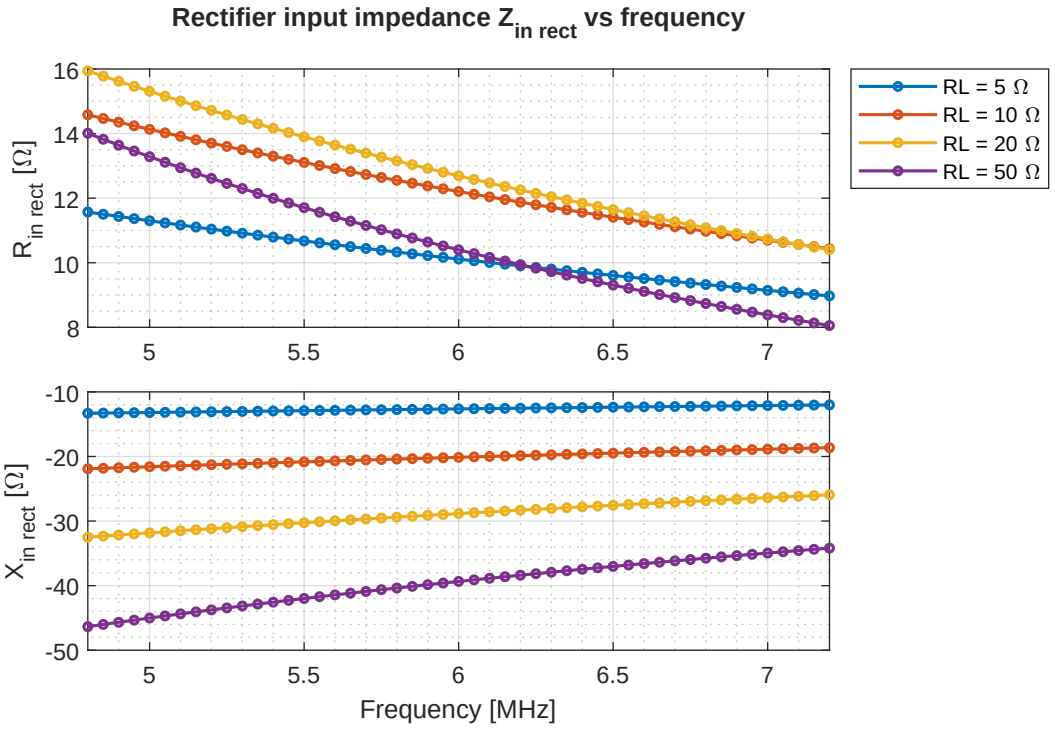


Figure 3.18: Input impedance of the push-pull Class E rectifier, $\overline{Z}_{\text{in}_{\text{rect}}}$, showing the real (resistive) and imaginary (reactive) components as a function of the switching frequency for different load values R_L.

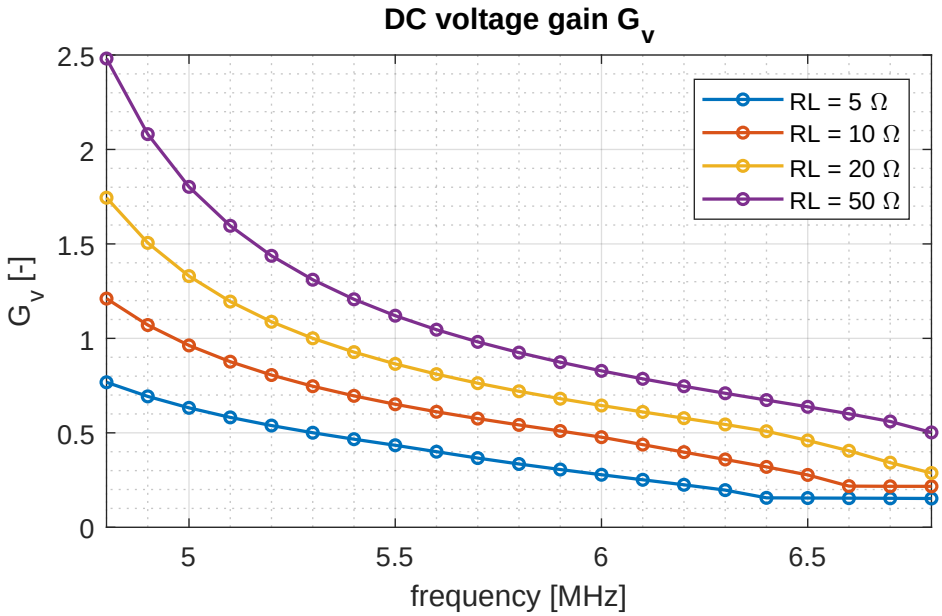


Figure 3.19: dc-dc voltage gain curves of the push-pull Class E² converter for different load resistances R_L, obtained from the FHA model.

The sinusoidal current i_2 entering the rectifier has amplitude

$$I_2 = G_i(f, R_L) V^1_{C_{p_{1,2}}}, \tag{3.39}$$

where $G_i(f, R_L)$ is the current gain, defined as the ratio of the amplitudes of i_2 and

$v^1_{C_{p_{1,2}}}$:

$$G_i(f, R_L) = \frac{I_2}{V^1_{C_{p_{1,2}}}}. \tag{3.40}$$

From the FHA model in Fig. 3.17, the secondary current can be expressed as

$$i_2 = -\frac{i_1 \overline{Z}_{\text{ref}}}{jX_{\text{M}}}, \tag{3.41}$$

where i_1 is the sinusoidal current flowing in the inverter output tank, $X_{\text{M}} = \omega k\sqrt{L_{s_1} L_{s_2}}$ is the mutual reactance, and $\overline{Z}_{\text{ref}}$ is the reflected impedance of the link defined as

$$\overline{Z}_{\text{ref}} = \overline{Z}_{\text{eq}} - jX_{L_{s_1}}. \tag{3.42}$$

The primary current i_1 can be written as

$$i_1 = \frac{v^1_{C_{p_{1,2}}}}{j(X_{C_{s_1}} + X_{L_{s_1}}) + \overline{Z}_{\text{eq}} - jX_{L_{s_1}}} = \frac{v^1_{C_{p_{1,2}}}}{jX_{C_{s_1}} + \overline{Z}_{\text{eq}}}. \tag{3.43}$$

Substituting, the current gain becomes

$$G_i(f, R_L) = \frac{I_2}{V^1_{C_{p_{1,2}}}} = \left| \frac{\overline{Z}_{\text{eq}} - jX_{L_{s_1}}}{jX_{\text{M}}\left(\overline{Z}_{\text{eq}} + jX_{C_{s_1}}\right)} \right|, \tag{3.44}$$

where $X_{C_{s_1}}$ is the reactance of the primary-side compensation capacitor C_{s_1}.

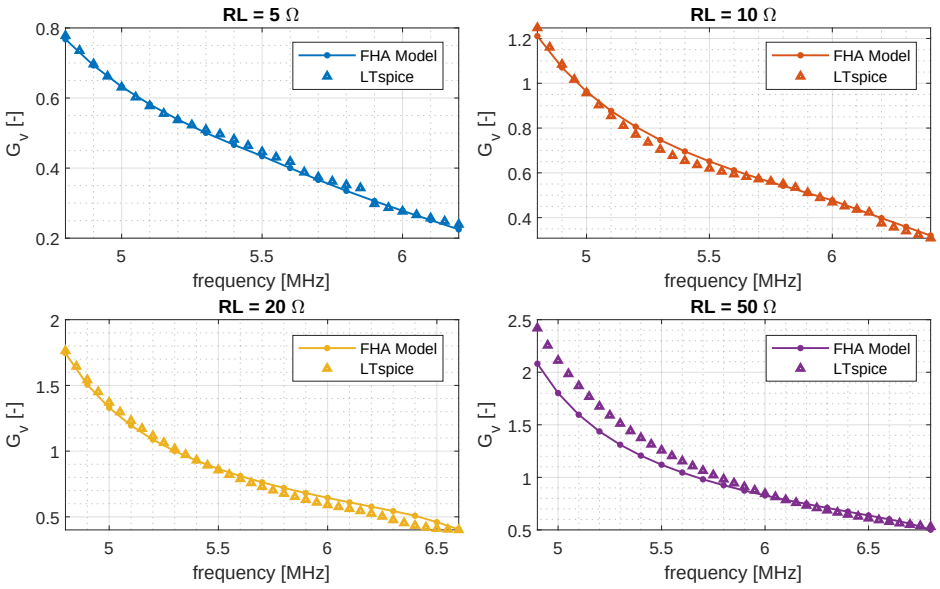


Figure 3.20: Comparison of the dc voltage gain of the push-pull Class E^2 converter: FHA model (solid lines) versus LTspice time-domain simulation (markers).

Finally, the FHA dc-dc voltage gain $G_v(f, R_L)$ is obtained by computing the output voltage V_{out} [15] and normalising it with respect to the input voltage V_{in}:

$$G_v(f, R_L) = \frac{2}{V_{\text{in}}} V^1_{C_{p1,2}} R_L G_i(f, R_L) \sin(\phi_{\text{rect}}). \tag{3.45}$$

Figure 3.19 shows the DC voltage gain curves of the push-pull Class E^2 converter as a function of the switching frequency, obtained from the FHA model derived in this section, for different values of the load resistance R_L.

The validity of the analytical model is verified in Fig. 3.20, where the gain curves from the FHA model are compared with those obtained from time-domain LTspice simulations. Very good agreement is observed over the entire frequency range of interest, confirming the accuracy of the FHA model.

3.5 Summary

This chapter presented the design of a 5 MHz isolated push-pull Class E^2 dc-dc converter and its high-frequency transformer. The intended application is an isolated dc-dc module for cyber-farm systems. A push-pull configuration was selected to enhance power-handling capability; however, the present hardware serves primarily as a performance and controllability testbed, so the input/output voltage levels were not constrained to server-grade specifications.

To explore alternatives to air-core implementations, a high-frequency, low-permeability ferrite (Fair-Rite Material 67) was adopted; the transformer design methodology and trade-offs were detailed. The prototype achieved 90.8% efficiency at 260 W output power. A simulation-based power-loss budget identified the rectifier diodes and the transformer core as the dominant loss contributors, indicating potential gains from synchronous rectification and motivating further work on reducing peak magnetic flux density.

A first-harmonic-approximation (FHA) model was derived to predict the dc conversion gain as a function of switching frequency. The resulting gain curves showed very good agreement with time-domain simulation across the frequency range of interest, validating the model for design and analysis.

Finally, this chapter established the basis for closed-loop regulation. The next chapter develops a frequency-modulated control scheme with duty-cycle adjustment, implemented on an STM32 microcontroller, to achieve output-voltage regulation while preserving soft switching.

Chapter 4

Converter Dynamics and Control

When operated at a fixed frequency, Class E-type converters maintain their optimal operating conditions and ZVS only at a specific load; any drift from this operating point leads to loss of soft switching and a sharp increase in losses. Moreover, load variations directly affect the output voltage. Therefore, maintaining a constant output voltage requires closed-loop control [60].

On/off control is the most popular output-voltage regulation method for resonant converters. It is simple to implement and preserves ZVS over a wide load range, achieving high efficiency at light load [61–64]. However, on/off control suffers from large low-frequency output-voltage ripple, as the on/off modulation frequency is usually lower than the switching frequency, and significant mode-transition losses due to discontinuous power flow [65]. An alternative is to employ variable energy-storage components (e.g., varactors or variable inductors) [66–68]; yet electrically controlled components are lossier and typically have lower power-handling capability. Out-phasing control regulates the output by adjusting the phase shift between two inverters while maintaining continuous power flow, but it requires two inverter stages and introduces additional complexity.

As demonstrated for the Class EF_2 dc-dc converter in Chapter 2 and for the push-pull Class E^2 converter in Chapter 3, frequency modulation with duty-cycle adjustment is an effective means of output voltage regulation that avoids extra components or inverter stages and while maintaining continuos power flow.

In this chapter, a proportional-integral-derivative (PID) control algorithm is developed for the dc-dc converter analysed in Chapter 3. The digital PID controller is implemented on an STM32 platform, and a model-based tuning approach is adopted using

system identification, which refers to the process of using measured data to derive a mathematical model of a system. The availability of such a model eliminates the need for manual controller tuning directly on hardware, which can be risk – particularly when employing heuristic methods such as Ziegler-Nichols [69], which require operating the system near instability to determine controller parameters. Related work includes a hybrid FM/on-off scheme for a 10 W isolated Class E dc-dc converter [65]; however, in that case the control-to-output transfer function of the converter is not analysed, whereas in this work such a model is explicitly identified and used for tuning.

The chapter is organised as follows. First, a time-domain simulation method for extracting the converter's small-signal model is presented. Next, the frequency-change sequence required for frequency control of the push-pull class-E^2 dc-dc converter is described, together with practical implementation aspects on the STM32 microcontroller. A relationship between operating frequency and duty cycle needed to achieve a target output voltage while maintaining soft switching is then derived. Finally, the PID tuning workflow in *Simulink* is outlined, and experimental hardware results are reported.

4.1 Background

In typical dc-dc converter applications, the output voltage V_{out} must be kept constant against variations of the load R_L or of the input dc voltage V_{in} [12]. This is achieved by introducing a circuit, the controller, that changes a certain control variable ψ (the duty cycle D, or the switching frequency f) in order to maintain the output voltage V_{out} to the desired reference value V^*_{ref}. The general diagram of a closed loop controlled power converter (the *plant*) is shown in Fig. 4.1. Designing a closed loop control system requires modelling the dynamics of the converter, which represent how variations of the control variable (or disturbances) affect the output voltage.

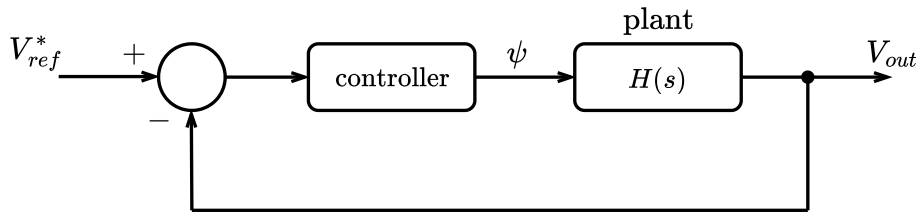


Figure 4.1: General diagram of a closed loop controlled power converter.

A SMPS exhibits inherently non-linear behaviour, but in order to apply classical con-

trol theory to power electronic systems, it is necessary to approximate its behaviour with a linear time-invariant (LTI) model valid around an operating point. The LTI representation of the system (transfer function $H(s)$ or state-space model) greatly simplifies the design process of the closed loop controlled system.

In this context, small-signal analysis is employed to study how small variations in the control variable and disturbances affect the output voltage, providing the basis for controller design. Indeed, when a small variation is introduced in the control variable ψ – the duty cycle in a PWM converter – of the form

$$\psi(t) = \psi_{\text{nom}} + \Psi_{\text{mod}} \sin(\omega_{\text{mod}} t) \tag{4.1}$$

where ψ_{nom} is the value of the control variable at the operating point, Ψ_{mod} is the small amplitude of the perturbation ($|\Psi_{\text{mod}}| \ll \psi_{\text{nom}}$), and ω_{mod} is its angular frequency (with $\omega_{\text{mod}} \ll \omega_{\text{nom}}$, the angular switching frequency of the converter), the spectrum of the output voltage $v_{\text{out}}(t)$ will contain a component at ω_{mod} whose magnitude and phase are determined by the frequency response of the converter. The objective of small signal analysis is to predict this low-frequency component of the output voltage, neglecting the switching ripple.

The most common ac modelling approach for PWM power converters consists in averaging the inductor current and capacitor voltage waveforms over one switching period in order to eliminate the switching ripple. The resulting averaged equations that describe the converter are generally non-linear, as they involve products of time-varying quantities, which generate harmonics and thus represent a non-linear process. Since classical ac analysis techniques cannot be applied to non-linear systems, these equations are linearised around the quiescent operating point by constructing a small-signal model. The underlying assumption is that the ac variations of the system variables are small compared to their dc operating values, allowing the non-linear ac terms to be neglected and yielding a small-signal linear ac model of the converter.

From the small-signal equations, the converter transfer function can be obtained by applying the Laplace transform and solving the resulting system in the s-domain. This yields the control-to-output transfer function $\hat{v}_{\text{out}}/\hat{\psi}$, which will in general depend on the values of the passive components (inductors, capacitors, and resistors) that constitute the converter.

An equivalent approach is *state-space averaging*, which is identical to the method described above, except that it uses the state-space description of dynamical sys-

tems [12, 34]. A PWM converter can be described by the following state equations:

$$\begin{aligned} \mathbf{K}\,\dot{\mathbf{x}}(t) &= \mathbf{A}^{1,2}\mathbf{x}(t) + \mathbf{B}^{1,2}\mathbf{u}(t) \\ \mathbf{y}(t) &= \mathbf{C}^{1,2}\mathbf{x}(t) + \mathbf{E}^{1,2}\mathbf{u}(t) \end{aligned} \tag{4.2}$$

where $\mathbf{A}^{1,2}, \mathbf{B}^{1,2}, \mathbf{C}^{1,2}, \mathbf{E}^{1,2}$ describe the system during the two subintervals of the switching period. By averaging over one switching period, the state equations become:

$$\begin{aligned} \mathbf{K}\,\langle\dot{\mathbf{x}}(t)\rangle &= \left(d(t)\mathbf{A}^1 + d'(t)\mathbf{A}^2\right)\langle\mathbf{x}(t)\rangle + \left(d(t)\mathbf{B}^1 + d'(t)\mathbf{B}^2\right)\langle\mathbf{u}(t)\rangle \\ \langle\mathbf{y}(t)\rangle &= \left(d(t)\mathbf{C}^1 + d'(t)\mathbf{C}^2\right)\langle\mathbf{x}(t)\rangle + \left(d(t)\mathbf{E}^1 + d'(t)\mathbf{E}^2\right)\langle\mathbf{u}(t)\rangle \end{aligned} \tag{4.3}$$

where $d(t)$ is the duty cycle and $d'(t) = 1 - d(t)$ is its complement. The angle brackets $\langle\cdot\rangle$ indicate averaging over one switching period. At equilibrium ($d(t) = D$, $\mathbf{u}(t) = \mathbf{U}$), the previous becomes:

$$\begin{aligned} 0 &= \left(D\mathbf{A}^1 + D'\mathbf{A}^2\right)\mathbf{X} + \left(D\mathbf{B}^1 + D'\mathbf{B}^2\right)\mathbf{U} = \mathbf{A}\mathbf{X} + \mathbf{B}\mathbf{U} \\ \mathbf{Y} &= \left(D\mathbf{C}^1 + D'\mathbf{C}^2\right)\mathbf{X} + \left(D\mathbf{E}^1 + D'\mathbf{E}^2\right)\mathbf{U} = \mathbf{C}\mathbf{X} + \mathbf{E}\mathbf{U} \end{aligned} \tag{4.4}$$

The set of equations in (4.3) can then be perturbed and linearised around the quiescent point given by (4.4) by substituting:

$$\begin{aligned} \langle\mathbf{x}(t)\rangle &= \mathbf{X} + \hat{\mathbf{x}}(t), \\ \langle\mathbf{u}(t)\rangle &= \mathbf{U} + \hat{\mathbf{u}}(t), \\ \langle\mathbf{y}(t)\rangle &= \mathbf{Y} + \hat{\mathbf{y}}(t), \\ d(t) &= D + \hat{d}(t), \\ d'(t) &= D' - \hat{d}(t). \end{aligned} \tag{4.5}$$

where quantities denoted with $\hat{\cdot}$ are small ac variations much smaller in magnitude compared to the quiescent values.

Substituting (4.5) into (4.3) yields:

$$\begin{aligned} \mathbf{K}\left\langle\dot{\hat{\mathbf{x}}}(t)\right\rangle = \underbrace{(\mathbf{A}\mathbf{X} + \mathbf{B}\mathbf{U})}_{\text{dc terms}} + \underbrace{\left[\mathbf{A}\hat{\mathbf{x}}(t) + \mathbf{B}\hat{\mathbf{u}}(t) + \left((\mathbf{A}^1 - \mathbf{A}^2)\mathbf{X} + (\mathbf{B}^1 - \mathbf{B}^2)\mathbf{U}\right)\hat{d}(t)\right]}_{\text{first-order ac terms}} \\ + \underbrace{\left[(\mathbf{A}^1 - \mathbf{A}^2)\hat{\mathbf{x}}(t)\hat{d}(t) + (\mathbf{B}^1 - \mathbf{B}^2)\hat{\mathbf{u}}(t)\hat{d}(t)\right]}_{\text{non-linear ac terms}}, \end{aligned} \tag{4.6}$$

$$\mathbf{Y} + \hat{\mathbf{y}}(t) = \underbrace{(\mathbf{CX} + \mathbf{EU})}_{\text{dc terms}} + \underbrace{\left[\mathbf{C}\hat{\mathbf{x}}(t) + \mathbf{E}\hat{\mathbf{u}}(t) + \left((\mathbf{C}^1 - \mathbf{C}^2)\mathbf{X} + (\mathbf{E}^1 - \mathbf{E}^2)\mathbf{U}\right)\hat{d}(t)\right]}_{\text{first-order ac terms}} + \underbrace{\left[(\mathbf{C}^1 - \mathbf{C}^2)\hat{\mathbf{x}}(t)\hat{d}(t) + (\mathbf{E}^1 - \mathbf{E}^2)\hat{\mathbf{u}}(t)\hat{d}(t)\right]}_{\text{non-linear ac terms}}. \tag{4.7}$$

Neglecting the non-linear ac terms (which are much smaller in magnitude than the first-order terms) and using the equilibrium condition from (4.4), the following small-signal linearised model is obtained [12, 34] :

$$\begin{aligned} \mathbf{K}\left\langle \dot{\hat{\mathbf{x}}}(t)\right\rangle &= \mathbf{A}\hat{\mathbf{x}}(t) + \mathbf{B}\hat{\mathbf{u}}(t) + \left((\mathbf{A}^1 - \mathbf{A}^2)\mathbf{X} + (\mathbf{B}^1 - \mathbf{B}^2)\mathbf{U}\right)\hat{d}(t), \\ \hat{\mathbf{y}}(t) &= \mathbf{C}\hat{\mathbf{x}}(t) + \mathbf{E}\hat{\mathbf{u}}(t) + \left((\mathbf{C}^1 - \mathbf{C}^2)\mathbf{X} + (\mathbf{E}^1 - \mathbf{E}^2)\mathbf{U}\right)\hat{d}(t). \end{aligned} \tag{4.8}$$

Another well-known technique to derive small-signal models for converters is the *switch averaging* method. In this approach, the converter switches are replaced with dependent voltage and current sources that reproduce the same waveforms as the original switches. This results in a time-invariant network, since the circuit connections no longer vary with time [12,34]. Once the time-invariant network is obtained, the switching harmonics are removed by averaging over one switching period, which yields the low-frequency behaviour of the system. Finally, the model is perturbed and linearised around a quiescent operating point, as in the other methods.

It is relevant to note that these approaches cannot be directly applied to resonant converters [70]. Both state-space averaging and switch averaging rely on the assumption that the relevant converter dynamics occur at frequencies much lower than the switching frequency, so that the switching action can be averaged over one period without losing essential information. This assumption holds for PWM converters, where the averaged behaviour accurately represents the low-frequency dynamics of interest for control design. In resonant topologies, however, the inductor current and capacitor voltage are large sinusoidal waveforms whose frequency is close to the switching frequency and whose instantaneous values determine the power transfer. Averaging over a switching period would remove this essential resonant behaviour and fail to capture the dependence of the converter dynamics on the switching frequency, leading to an inaccurate representation of the system.

An alternative and more accurate modelling technique for resonant and Class E based converters is the *multi-frequency averaging* (MFA) method. This approach extends the classical averaging concept by retaining not only the dc component but also selected harmonics of the switching frequency, thus preserving the essential resonant behaviour

of the circuit [70–72]. While MFA offers improved accuracy, it results in models of substantially increased order and algebraic complexity, making them difficult to handle analytically and impractical for control-oriented design. For this reason, MFA was not adopted in this work, in favour of modelling approaches that provide a more manageable balance between accuracy and simplicity.

Whenever an analytical small-signal model is not available, a common alternative is to use system identification techniques, which treat the converter as a black-box. The system is excited with a known perturbation of the control variable, and the resulting output is processed to infer a mathematical model that reproduces the observed input-output relationship. Several software tools, such as Simulink's Frequency Response Estimation or System Identification Toolbox, can automate this procedure. However, in practice we found that when applied to high-frequency converters these methods can be impractical, either because they require long simulation times or because the switching harmonics make it difficult to extract the small-signal dynamics accurately.

To overcome this limitation, in this thesis a simpler and more general approach that does not rely on external identification software is adopted, based on [73]. The converter is perturbed by a small step change of the control variable in a time-domain simulation, and the resulting output response is used directly to derive the plant transfer function. Since a step input excites a broad range of low-frequency dynamics relevant to control, this method provides a reliable approximation of the small-signal behaviour while remaining compatible with any time-domain circuit simulator, including SPICE-like tools. It thus avoids the limitations of black-box identification packages and remains consistent with the assumptions of classical small-signal modelling.

4.2 Extraction of plant transfer function from time-domain simulation

As introduced earlier in this chapter, averaging and small-signal linearisation provide a systematic way to derive analytical models for classical PWM converters. These models lead to compact expressions of the control-to-output transfer function, which are widely used for loop-gain analysis, stability assessment, and controller tuning. However, for resonant or strongly non-linear converters, such derivations are cumbersome and often impractical. In these cases, obtaining the small-signal transfer function directly from data (or simulation) becomes a practical alternative.

The *small-signal transfer function* describes the relationship between the control variable (duty cycle or switching frequency) and the regulated output (voltage or current). A direct numerical evaluation would involve perturbing the control variable with a small sinusoid and measuring the steady-state response for each frequency of interest, effectively sweeping across the frequency range point by point, as mentioned in the previous section. While conceptually straightforward, this approach is computationally expensive, especially for high-frequency converters: on the one hand, very small time steps are required to resolve the fast switching transitions, while on the other hand sufficiently long simulation times are needed to capture the slow small-signal dynamics relevant for control.

To overcome this limitation, in this work a method based on the step response of the system was used. A small step perturbation $u(t)$ (chosen sufficiently small so as not change the operating point) is applied to the control variable in a time-domain simulation (e.g., in LTspice or Simscape Electrical in Simulink), and the corresponding output response $y(t)$ is recorded. Since a step excites a broad range of frequencies, the recorded response contains the information required to reconstruct the converter's small-signal transfer function without repeated frequency sweeps. By processing the simulated step response in the Laplace domain, the control-to-output transfer function can be obtained efficiently.

This approach avoids the complexity of deriving analytical models for resonant converters and the computational cost of frequency-domain sweeps, while remaining compatible with any time-domain circuit simulator. It therefore provides a practical and general tool to extract the converter dynamics needed for control design and stability analysis.

With reference to Fig. 4.2, let $u(t)$ be the input step of amplitude A, whose Laplace

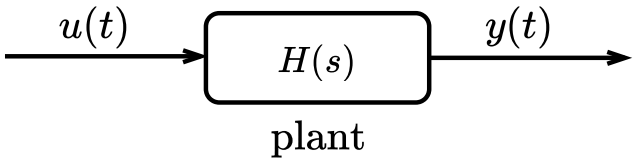


Figure 4.2: General diagram for step response evaluation.

transform is:

$$U(s) = \frac{A}{s}. \tag{4.9}$$

The Laplace transform of the output $y(t)$ is then:

$$Y(s) = H(s) \cdot U(s) = \frac{A}{s} H(s), \tag{4.10}$$

where $H(s)$ is the system transfer function. By the properties of the Laplace transform:

$$Y(s) = \mathcal{L}\{y(t)\} = \int_0^\infty y(t) e^{-st}\, dt = \frac{A}{s} H(s). \tag{4.11}$$

Differentiating $y(t)$ in time yields:

$$\int_0^\infty y'(t) e^{-st}\, dt = AH(s), \tag{4.12}$$

where $y'(t)$ is the time derivative of $y(t)$. Therefore, the transfer function can be written as:

$$H(s) = \frac{1}{A} \int_0^\infty y'(t) e^{-st}\, dt. \tag{4.13}$$

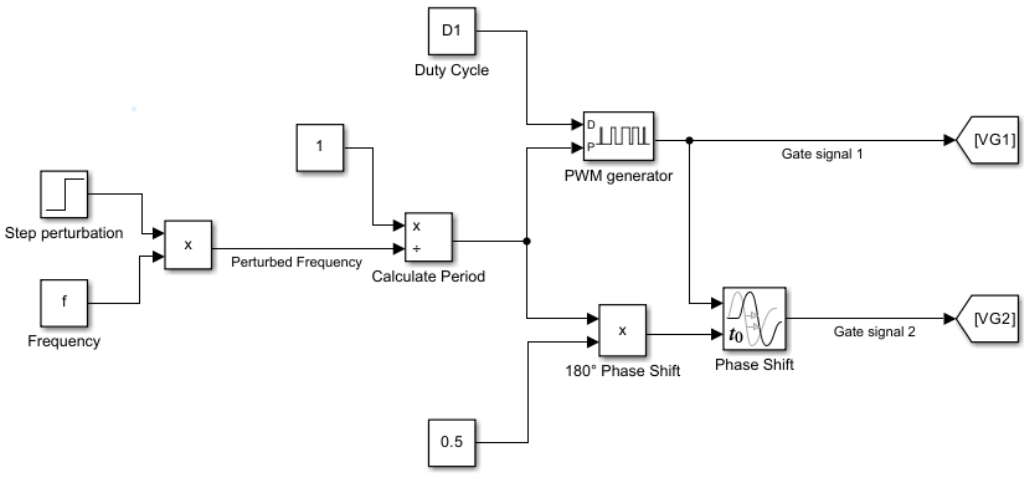


Figure 4.3: Switching frequency step perturbation in the Simulink model.

In discrete form, the integral in (4.13) becomes a finite sum (since $y(t)$ reaches steady state after a finite time):

$$H(s) = \frac{1}{A} \sum_{i=1}^{N-1} \Big(y(t_i) - y(t_{i-1})\Big) e^{-s(t_i - t_{i-1})}, \tag{4.14}$$

where $y(t_i)$ are the sampled output values, and N is the number of samples.

To compensate for the numerical delay introduced by the discretisation, a correction factor is applied:

$$H(s) = \frac{1}{A} \sum_{i=1}^{N-1} \Big(y(t_i) - y(t_{i-1})\Big) e^{-s\left(t_i - t_{i-1} - \frac{T_N}{2}\right)}, \tag{4.15}$$

where $T_N = T/(N-1)$ is the sampling period and T the total length of the recorded step response.

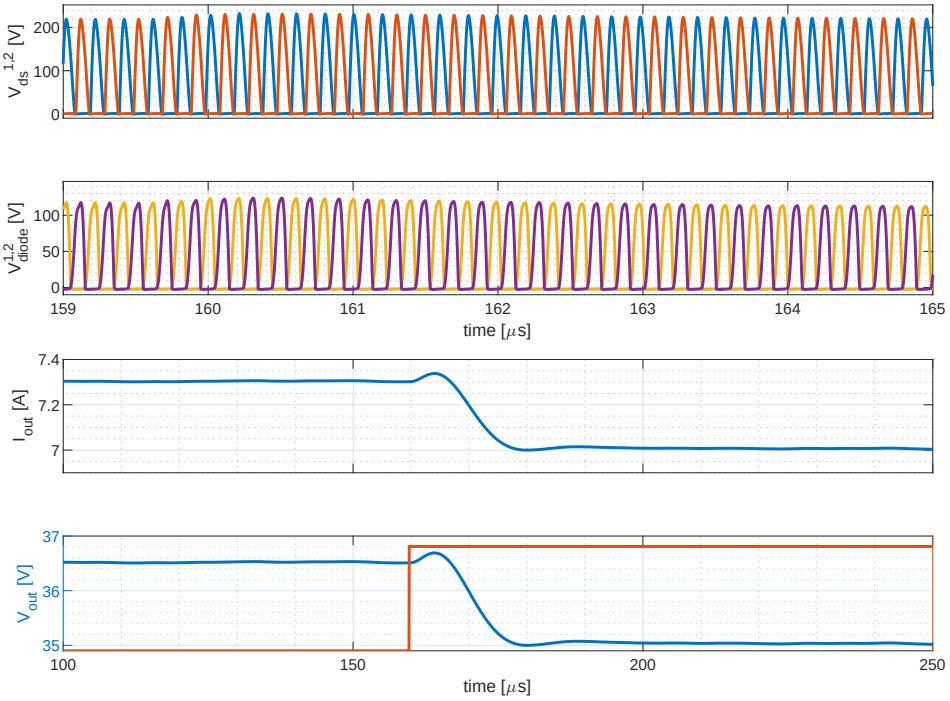


Figure 4.4: Converter waveforms when a small step perturbation is applied to the switching frequency. From top to bottom: inverter switch voltages, rectifier diode voltages, output current, and output voltage.

A Simscape Electrical model of the Class E^2 push-pull dc-dc converter described in this chapter was implemented in Simulink, exploiting the MATLAB-Simulink interface to automate the procedure. It should be noted, however, that the method is not limited to this environment: any time-domain circuit simulator can be used to generate the data, and the post-processing can be performed in any programming language.

The switching frequency f_{sw} is perturbed by a small step, applied at time t_0:

$$f_{\mathrm{sw}}(t) = \begin{cases} f_{\mathrm{sw}}, & t < t_0, \\ f_{\mathrm{sw}} A_0, & t \geq t_0, \end{cases} \tag{4.16}$$

where $A_0 = A + 1$ and A is sufficiently small so as not to disturb the operating mode. Fig. 4.3 shows the block diagram of the step perturbation of the switching frequency implemented in the Simulink model. The gate signal for device Q_1 is generated using a *Variable Pulse Generator* block, while the 180° phase-shifted gate signal for device Q_2 is obtained through a *Variable Time Delay* block with delay $0.5/f_{sw}(t)$, where $f_{sw}(t)$ is the instantaneous switching frequency. The duty cycle is kept constant, since in this class of converters it is not used for regulation but only to ensure ZVS operation.

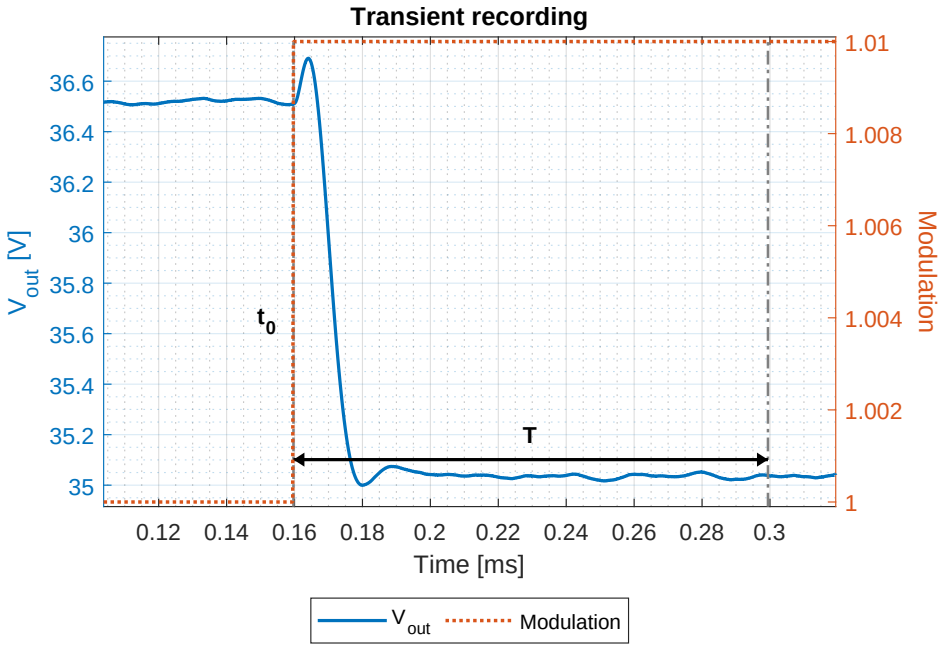


Figure 4.5: Transient response observation window.

Fig. 4.4 shows the drain waveforms of the devices (GaN transistors and diodes), together with the dc output voltage and current, obtained as a result of the step perturbation of the switching frequency.

The step response $y(t)$, which is the output voltage, is recorded from t_0 until $t_1 = t_0 + T$, ensuring steady state is reached at the end of the observation window, as shown in Fig. 4.5.

The data is resampled at a fixed sampling frequency before applying the discrete-time calculation of $H(s)$. This is shown in Fig. 4.6. The transfer function is thus obtained

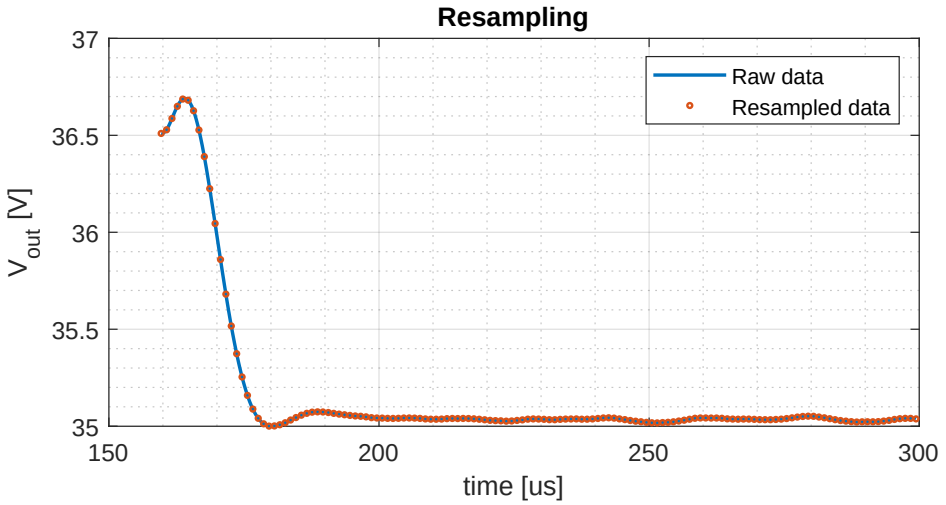


Figure 4.6: Resampling of the output response at a fixed sampling frequency.

in the following form, which is equivalent to (4.14):

$$H(s) = \frac{1}{A} \sum_{i=1}^{N-1} \Lambda_i e^{-s\Gamma_i}, \tag{4.17}$$

where

$$\Lambda_i = y(t_i) - y(t_{i-1}), \qquad \Gamma_i = t_i - t_{i-1} - \frac{T_N}{2}.$$

By substituting $s = j\omega$ into (4.17), the frequency response $H(j\omega)$ is obtained. The corresponding Bode plot of the plant control-to-output transfer function is shown in Fig. 4.7.

The system output can be reconstructed by exploiting the Laplace transform property:

$$Y(s) = \frac{A}{s} H(s) = \sum_{i=1}^{N-1} \frac{\Lambda_i}{s} e^{-s\Gamma_i}, \tag{4.18}$$

$$y(t) = \sum_{i=1}^{N-1} \Lambda_i \, u(t - \Gamma_i), \tag{4.19}$$

where $u(t)$ is the Heaviside step function. The reconstructed output waveform obtained using (4.19) is illustrated in Fig. 4.8.

The numerically obtained transfer function in (4.17) is approximated by a rational function. For the converter under study, the best approximation was obtained with a third-order numerator and a fifth-order denominator, corresponding to three zeros and five poles:

$$H_{\text{fit}}(s) = \frac{a_3 s^3 + a_2 s^2 + a_1 s + a_0}{s^5 + b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0}, \tag{4.20}$$

where $\{a_i\}$ and $\{b_i\}$ are the unknown polynomial coefficients of the numerator and denominator, respectively.

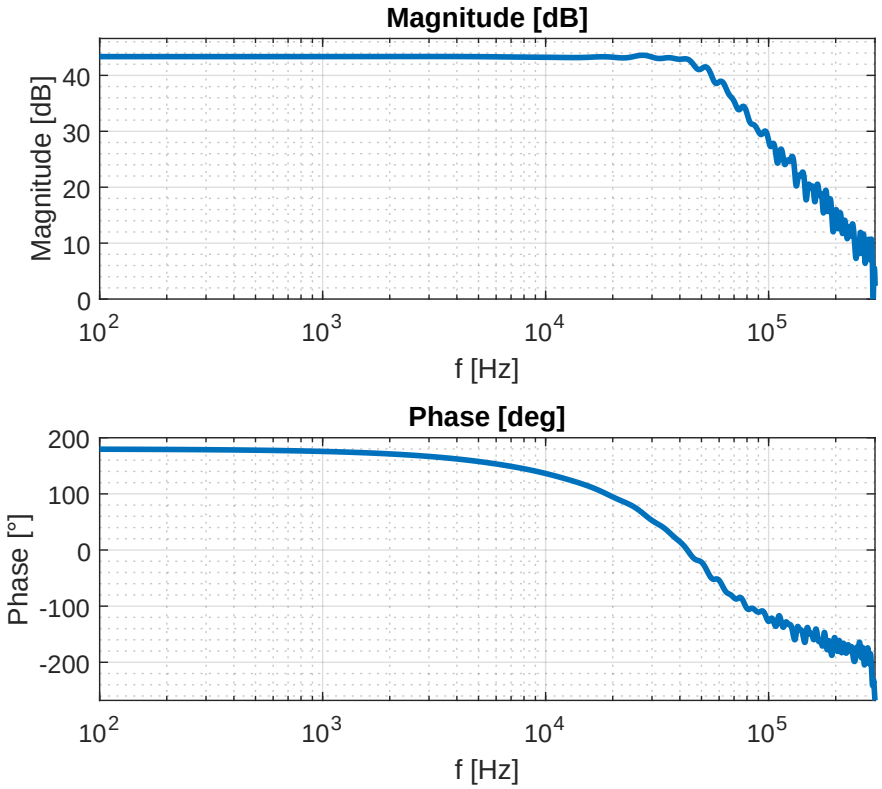


Figure 4.7: Bode plot of the control-to-output transfer function of the plant, showing both magnitude and phase.

These coefficients are estimated by solving a non-linear least-squares problem using the `lsqnonlin` solver in MATLAB with the Levenberg-Marquardt algorithm. Defining the parameter vector as

$$\boldsymbol{\theta} = [a_3, a_2, a_1, a_0, b_4, b_3, b_2, b_1, b_0]^\top,$$

the residual vector is constructed by stacking the real and imaginary errors of the fitted model with respect to the numerically obtained frequency response $H(j\omega)$:

$$\mathbf{r}(\boldsymbol{\theta}) = \begin{bmatrix} \Re\{H_{\text{fit}}(j\omega_1;\boldsymbol{\theta})\} - \Re\{H(j\omega_1)\} \\ \Im\{H_{\text{fit}}(j\omega_1;\boldsymbol{\theta})\} - \Im\{H(j\omega_1)\} \\ \vdots \\ \Re\{H_{\text{fit}}(j\omega_{N_\omega};\boldsymbol{\theta})\} - \Re\{H(j\omega_{N_\omega})\} \\ \Im\{H_{\text{fit}}(j\omega_{N_\omega};\boldsymbol{\theta})\} - \Im\{H(j\omega_{N_\omega})\} \end{bmatrix}. \tag{4.21}$$

The cost function minimised by `lsqnonlin` is the squared ℓ_2-norm of the residual vector:

$$\mathcal{J}(\boldsymbol{\theta}) = \|\mathbf{r}(\boldsymbol{\theta})\|_2^2 = \sum_{k=1}^{N_\omega} \Big(\Re\{H_{\text{fit}}(j\omega_k;\boldsymbol{\theta})\} - \Re\{H(j\omega_k)\}\Big)^2 + \Big(\Im\{H_{\text{fit}}(j\omega_k;\boldsymbol{\theta})\} - \Im\{H(j\omega_k)\}\Big)^2. \tag{4.22}$$

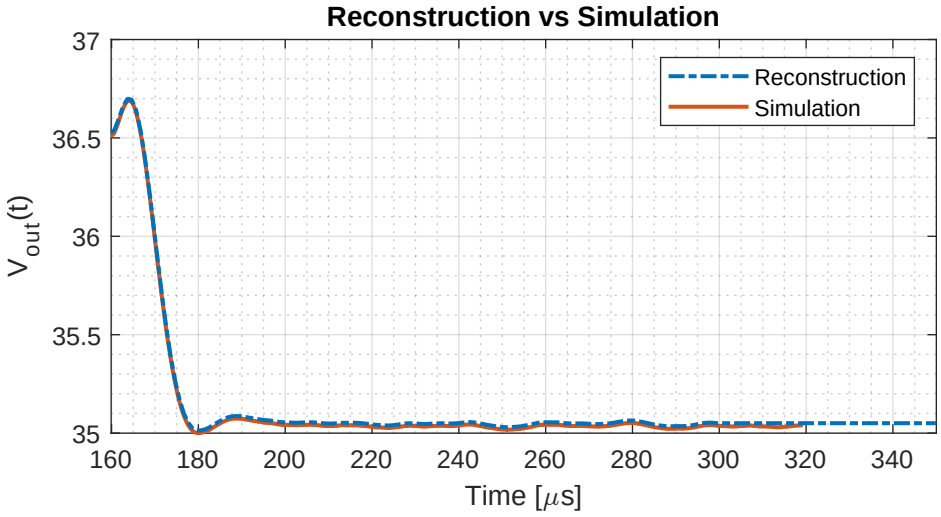


Figure 4.8: Output voltage reconstruction from $H(s)$.

The result of the polynomial fitting is shown in Fig. 4.9, where the real and imaginary parts of the numerically extracted frequency response $H(j\omega)$ are plotted as blue continuous lines, while the corresponding parts of the fitted response $H_{\text{fit}}(j\omega)$ are shown as orange dash-dotted lines.

The agreement between the polynomial fitting $H_{\text{fit}}(j\omega)$ and the simulated data $H(j\omega)$ can also be assessed in the Bode domain. Fig. 4.10 compares the Bode plots obtained from the numerically extracted frequency response and from the fitted model.

The transfer function $H_{\text{fit}}(s)$ in the s-domain can be expressed in factored form as

$$H_{\text{fit}}(s) = K \cdot \frac{\prod_i \left(1 + \frac{s}{2\pi f_{z,i}}\right)}{\prod_j \left(1 + \frac{s}{2\pi f_{p,j}}\right) \prod_k \left[\left(\frac{s}{\omega_{n,k}}\right)^2 + 2\zeta_k \frac{s}{\omega_{n,k}} + 1\right]}, \tag{4.23}$$

where $f_{z,i}$ and $f_{p,j}$ are the frequencies of real zeros and poles, and $(\omega_{n,k}, \zeta_k)$ are the natural frequency and damping ratio of complex-conjugate pole pairs.

For the identified converter, the fitted transfer function is

$$\begin{aligned} H_{\text{fit}}(s) = -147.1897 \cdot & \frac{\left(1 - \frac{s}{2\pi\cdot(1.683\times10^6)}\right)\left(1 + \frac{s}{2\pi\cdot(84.59\times10^3)}\right)\left(1 - \frac{s}{2\pi\cdot(45.65\times10^3)}\right)}{\left(1 + \frac{s}{2\pi\cdot(941.0\times10^3)}\right)\left(1 + \frac{s}{2\pi\cdot(71.81\times10^3)}\right)} \\ & \cdot \frac{1}{\left(1 + \frac{s}{2\pi\cdot(30.47\times10^3)}\right)\left[\left(\frac{s}{2\pi\cdot(49.52\times10^3)}\right)^2 + 2\cdot0.458\,\frac{s}{2\pi\cdot(49.52\times10^3)} + 1\right]} \end{aligned} \tag{4.24}$$

The pole-zero map of the fitted frequency response $H_{\text{fit}}(s)$ is shown in Fig. 4.11. The plot displays the location of the poles (cross markers) and zeros (circle markers) of the

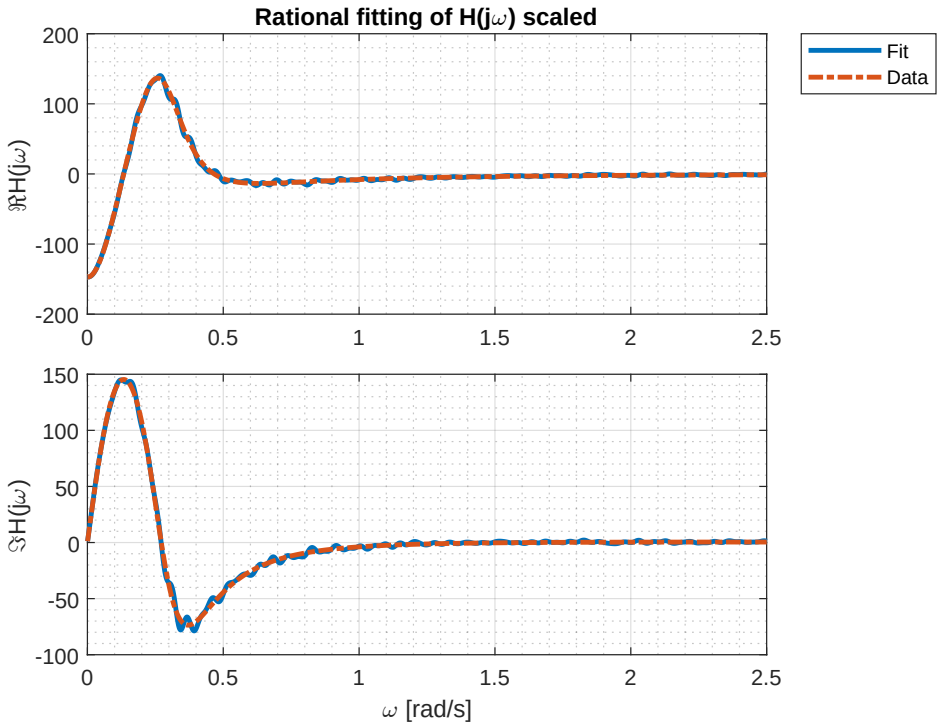


Figure 4.9: Rational fitting of the numerical transfer function. The real and imaginary parts of the extracted frequency response $H(j\omega)$ are shown in blue. The result of the polynomial fitting is shown in orange.

third-order numerator and fifth-order denominator model. For clarity, the x-axis has been divided into three sections in order to show all poles and zeros.

Non-minimum phase behaviour

The resulting fitted transfer function revealed the presence of two *right-half-plane (RHP) zeros* one of which at a frequency of approximately 45 kHz. This feature indicates that the system exhibits a non-minimum-phase behaviour: an increase in the control variable (switching frequency, in this case) initially produces an output response in the *opposite* direction before eventually converging to the steady-state value [12]. This effect can be illustrated by considering the s-domain expression for an RHP zero, $H_{RHPz}(s) = -s + a$. When a step input $U(s)$ is applied, the corresponding output $y(t)$, obtained using inverse Laplace transform properties, is:

$$y(t) = \mathcal{L}^{-1}\{(-s+a)\cdot U(s)\} = -\frac{d}{dt}u(t) + a\,u(t) \tag{4.25}$$

The negative sign of the derivative term highlights that a positive change in the input step initially produces a transient response in the opposite direction.

Control of systems with RHP zeros presents inherent challenges. The presence of the zero introduces an additional phase lag, reducing the achievable phase margin. At-

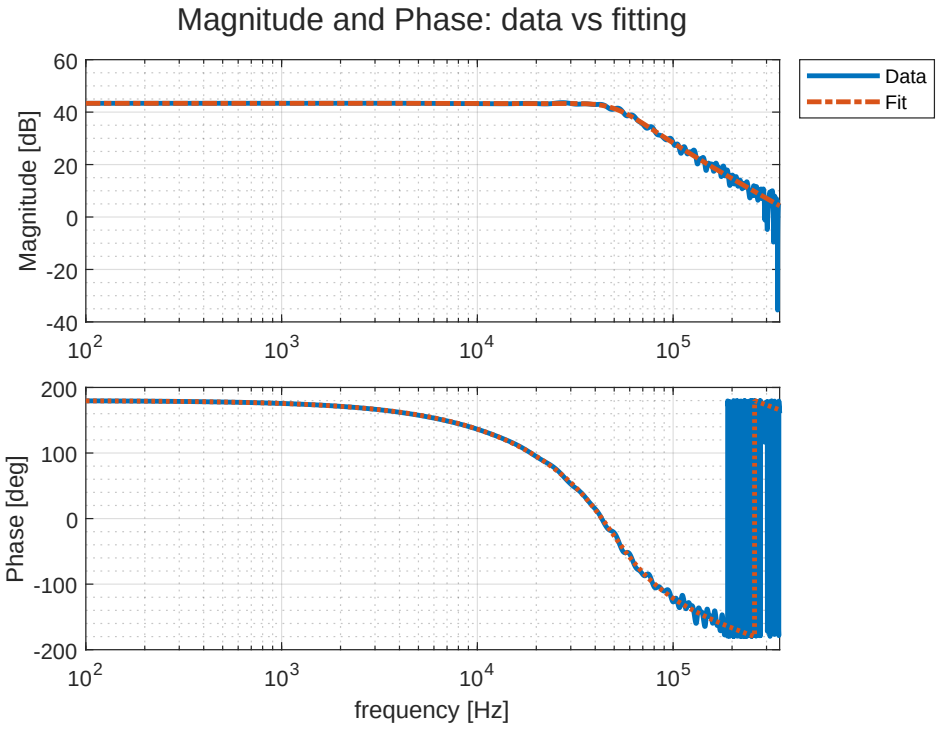


Figure 4.10: Comparison between the Bode plots of the control-to-output transfer function: numerical data (blue continuous lines) and polynomial fitting (orange dash-dotted lines).

tempting to increase the control bandwidth or to compensate the RHP zero directly with a pole in the right-half-plane would lead to instability. Therefore, the only practical approach is to reduce the controller bandwidth, effectively slowing down the control response so that it does not react to the initial inverse trajectory.

As a result, the RHP zero imposes a fundamental limitation on the achievable control bandwidth and transient speed, since higher crossover frequencies would inevitably degrade phase margin and potentially lead to oscillatory or unstable behaviour [74].

4.2.1 Comparison with sinusoidal perturbation

For comparison, the transfer function was also obtained by applying small sinusoidal perturbations to the control variable at discrete frequencies f_{pert} within the range of interest. This approach corresponds to the theoretical definition of AC small-signal analysis, as introduced in equation (4.1), and is used here to validate the results of the proposed step-based method.

The perturbed switching frequency was defined as

$$f_{\text{sw}}(t) = f_{\text{sw}} + A\sin(2\pi f_{\text{pert}} t), \tag{4.26}$$

with $|A| \ll f_{\text{sw}}$. The perturbation amplitude A was chosen small enough to produce

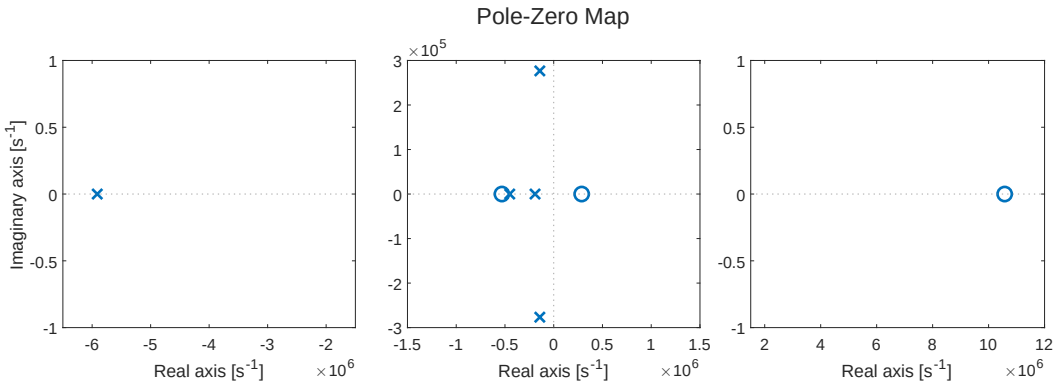


Figure 4.11: Pole-zero map of the fitted control-to-output transfer function $H_{\text{fit}}(j\omega)$. Crosses denote poles and circles denote zeros. The x-axis is divided into sections for clarity.

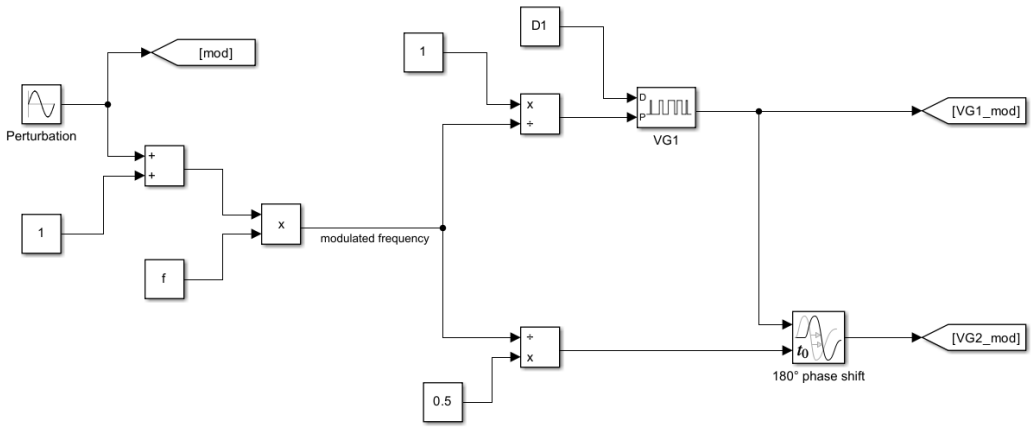


Figure 4.12: Block scheme used in Simulink to generate the sinusoidally perturbed switching frequency.

only a visible modulation of the dc output voltage, while avoiding the excitation of non-linear phenomena. The Simulink implementation is shown in Fig. 4.12, which differs from the step perturbation scheme of Fig. 4.3 only in that the perturbation is a sinusoid of small amplitude A and frequency f_{pert} rather than a step.

The perturbed switching frequency and the corresponding output response for different f_{pert} are illustrated in Fig. 4.13. As discussed earlier in this chapter, the output spectrum contains a clear component at the perturbation frequency f_{pert}, whose magnitude and phase encode the small-signal dynamics of the converter. In practice, one simulation is required for each perturbation frequency, and for lower f_{pert} the simulation time must be significantly extended to capture at least one full period in steady state, which increases computational cost.

The in-phase (I) and quadrature (Q) components of the output at each perturbation frequency were extracted using Fourier analysis, with the integration interval T chosen

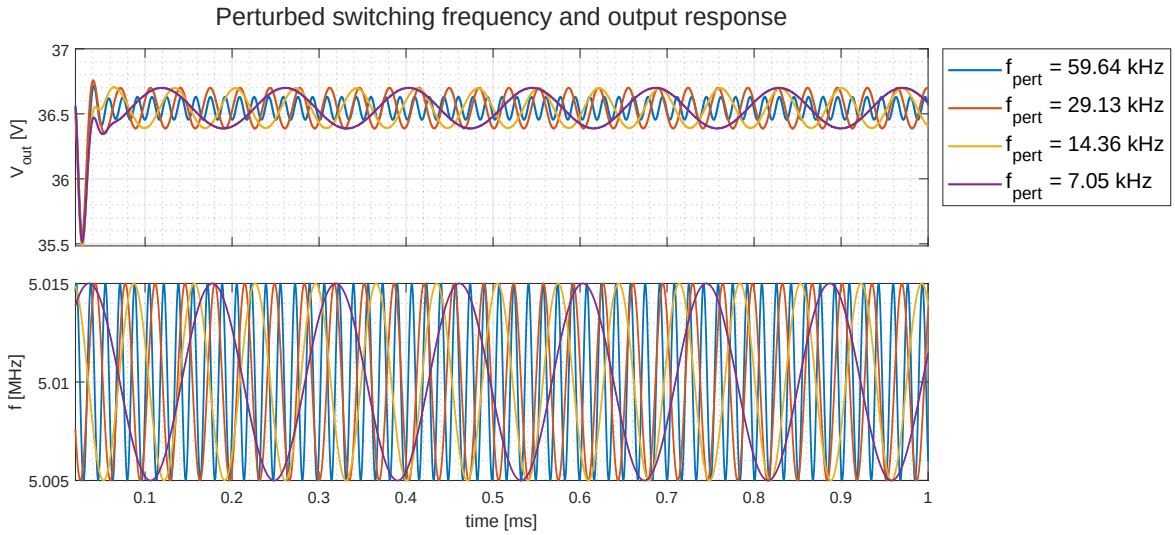


Figure 4.13: Perturbed switching frequency and resulting output response $v_{\text{out}}(t)$ for different perturbation frequencies f_{pert}.

as exactly one perturbation period in steady state (reached at $t = t_0$):

$$V_{\text{out,I}}^{f_{\text{pert}}} = \frac{2}{T}\int_{t_0}^{t_0+T} v_{\text{out}}(t)\,\sin\!\left(2\pi f_{\text{pert}} t\right)\,dt, \tag{4.27}$$

$$V_{\text{out,Q}}^{f_{\text{pert}}} = \frac{2}{T}\int_{t_0}^{t_0+T} v_{\text{out}}(t)\,\cos\!\left(2\pi f_{\text{pert}} t\right)\,dt. \tag{4.28}$$

The complex response is then

$$V_{\text{out}}^{f_{\text{pert}}} = V_{\text{out,I}}^{f_{\text{pert}}} + j\,V_{\text{out,Q}}^{f_{\text{pert}}}, \tag{4.29}$$

with magnitude and phase given by

$$\left|V_{\text{out}}^{f_{\text{pert}}}\right| = \sqrt{\left(V_{\text{out,I}}^{f_{\text{pert}}}\right)^2 + \left(V_{\text{out,Q}}^{f_{\text{pert}}}\right)^2}, \qquad \angle V_{\text{out}}^{f_{\text{pert}}} = \arctan\left(\frac{V_{\text{out,Q}}^{f_{\text{pert}}}}{V_{\text{out,I}}^{f_{\text{pert}}}}\right). \tag{4.30}$$

Finally, the Bode plot is obtained by plotting the phase $\angle V_{\text{out}}^{f_{\text{pert}}}$ and the magnitude in decibels:

$$20\log_{10}\left(\frac{|V_{\text{out}}^{f_{\text{pert}}}|}{A}\right), \tag{4.31}$$

where A is the amplitude of the sinusoidal perturbation.

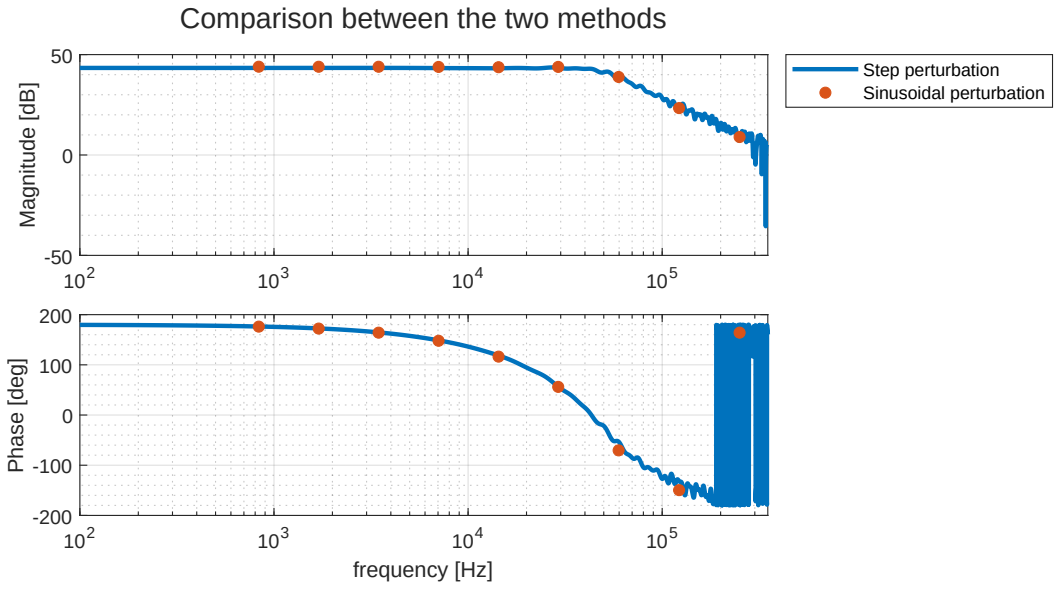


Figure 4.14: Comparison between the frequency response obtained with sinusoidal perturbation (orange dots) and step perturbation (blue line) of the control variable.

The comparison between the two identification methods is shown in Fig. 4.14. The orange dots correspond to the sinusoidal perturbation method, providing one point per frequency f_{pert}, while the blue line represents the transfer function extracted from the step perturbation. The results match closely, as expected from theory, thus confirming the validity of the proposed step-based approach.

The identification method for extracting the converter transfer function based on the simulated step response was experimentally validated by comparison with frequency-response measurements obtained using sinusoidal frequency perturbation. The open-loop transfer function was measured by applying gate signals whose switching frequency f_{sw}, was sinusoidally perturbed at different perturbation frequencies f_{pert}.

The frequency-modulated gate signals were generated using the modulation function of a Siglent SDG6052X arbitrary waveform generator. The applied PWM signals had a fixed duty cycle, whereas the switching frequency was sinusoidally modulated at a perturbation frequency f_{pert} with a modulation amplitude equal to 1% of the nominal switching frequency $f_{\text{sw}}(t) = \bar{f}_{\text{sw}}(1+0.01\sin(2\pi f_{\text{pert}}t)))$. For this measurement, the dc load consisted of two power resistors (Ohmite BA326622R0KE) connected in parallel, giving a total resistance of $R_{\text{L}} = 11\,\Omega$. A resistive load was chosen instead of an electronic load to avoid measuring the dynamic response of the load itself. The complex impedance of the dc load, including its parasitic inductance, was carefully characterised using a vector network analyzer (VNA) and included in the simulations. Fig. 4.15 shows the corresponding Smith chart obtained from the VNA measurements of the

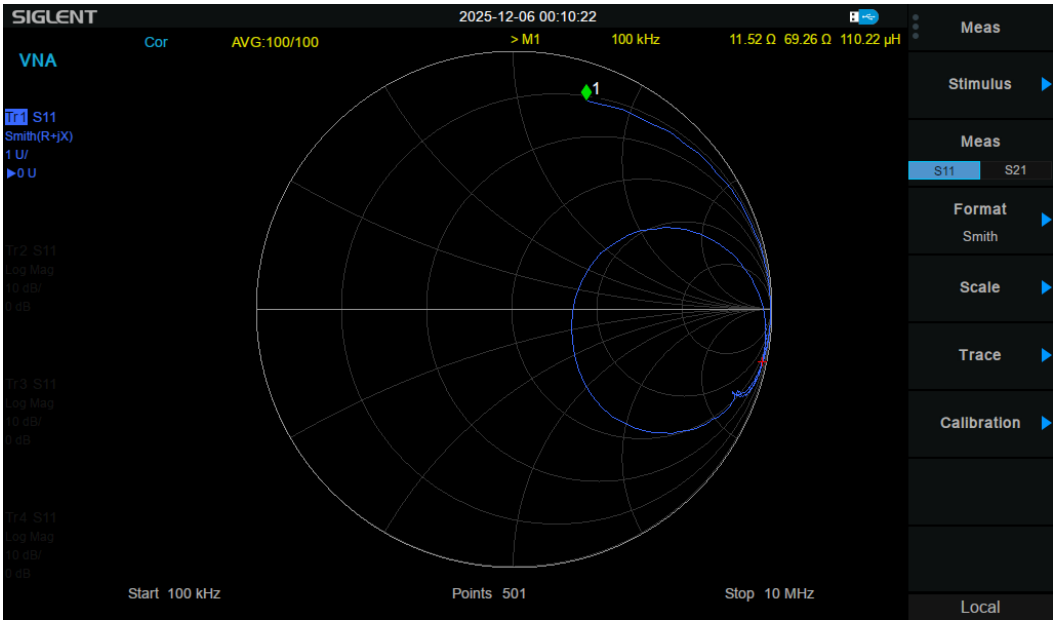


Figure 4.15: Smith chart of the measured impedance of the dc load consisting of two Ohmite BA326622R0KE power resistors connected in parallel.

employed dc load.

An example of the experimental waveforms acquired during the measurement is shown in Fig. 4.16. In this measurement, the switching frequency is sinusoidally modulated at $f_{\text{pert}} = 10\,\text{kHz}$, resulting in a low-frequency component superimposed on the converter output voltage. From top to bottom, the oscilloscope screen-capture shows the gate signals (orange), the AC component of converter output voltage (light blue), and the instantaneous switching frequency (green), which illustrates both the modulation frequency and amplitude.

For each perturbation frequency f_{pert}, the converter output voltage $v_{\text{out}}(t)$ was recorded, and the magnitude and phase of the superimposed sinusoidal component at that frequency were extracted to construct the Bode plot. The instantaneous normalised control variable x(t) is defined as

$$x(t) = \frac{f_{\text{sw}}(t) - \bar{f}_{\text{sw}}}{\bar{f}_{\text{sw}}}, \tag{4.32}$$

where $f_{\text{sw}}(t)$ is the instantaneous switching frequency and $\bar{f}_{\text{sw}}$ is the nominal switching frequency.

The complex phasors of the control variable $X(j\omega_{\text{pert}})$ and of the output voltage $Y(j\omega_{\text{pert}})$ at the perturbation frequency $\omega_{\text{pert}} = 2\pi f_{\text{pert}}$ are computed using

$$X(j\omega_{\text{pert}}) = \sum_{n=1}^{N} x(t_n) w(t_n) e^{-j\omega_{\text{pert}} t_n}, \quad Y(j\omega_{\text{pert}}) = \sum_{n=1}^{N} v_{\text{out}}(t_n) w(t_n) e^{-j\omega_{\text{pert}} t_n} \tag{4.33}$$

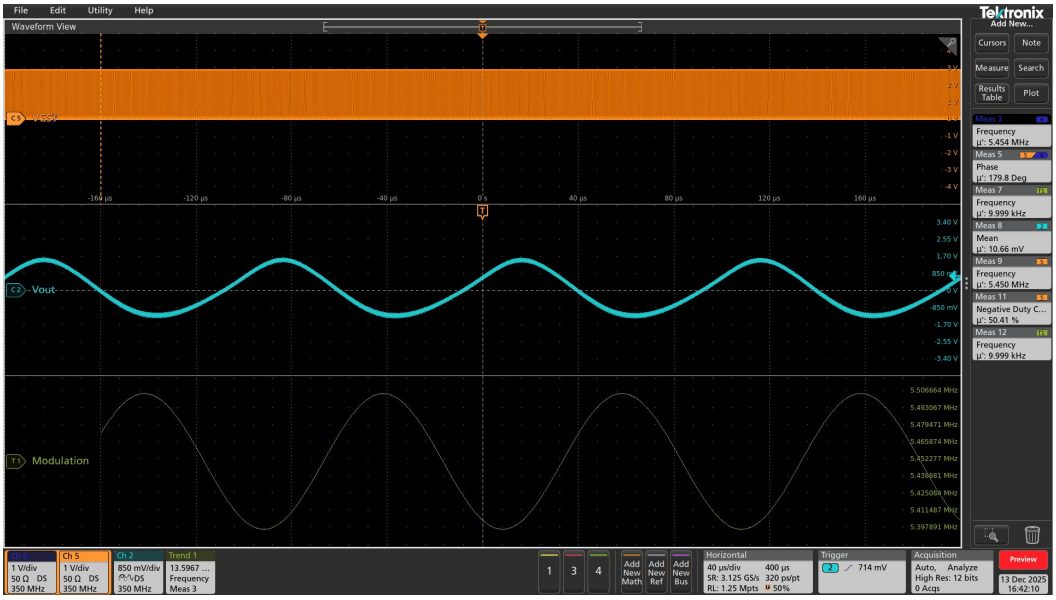


Figure 4.16: Experimental measurement of the open-loop frequency response of the converter using sinusoidal frequency perturbation. The switching frequency is sinusoidally modulated at $f_{\text{pert}} = 10\,\text{kHz}$. From top to bottom: gate signal, AC component of the converter output voltage and instantaneous switching frequency. The low-frequency component superimposed of the output voltage is used to extract magnitude and phase information for the Bode plot.

where $w(t_n)$ is a Hann window applied to reduce spectral leakage, and t_n are the discrete sampling times.

The transfer function at the perturbation frequency is then calculated as

$$H(j\omega_{\text{pert}}) = \frac{Y}{X} = |H(j\omega_{\text{pert}})|e^{j\angle H(j\omega_{\text{pert}})},$$

which provides both the magnitude $|H(f_{\text{pert}})|$ and phase $\angle H(f_{\text{pert}})$ of the Bode plot. By repeating this procedure for all perturbation frequencies f_{pert}, the complete frequency response of the converter was obtained.

Figure 4.17 compares the experimentally measured frequency response with the simulated response obtained using the proposed step-response-based method. The simulated response is shown in blue, the experimental measurements obtained via sinusoidal perturbation are shown as orange dots, and the fitting obtained using a rational function is shown in yellow for completeness. The results demonstrate excellent agreement between the simulated and measured frequency responses, validating the accuracy of the proposed method across the frequency range.

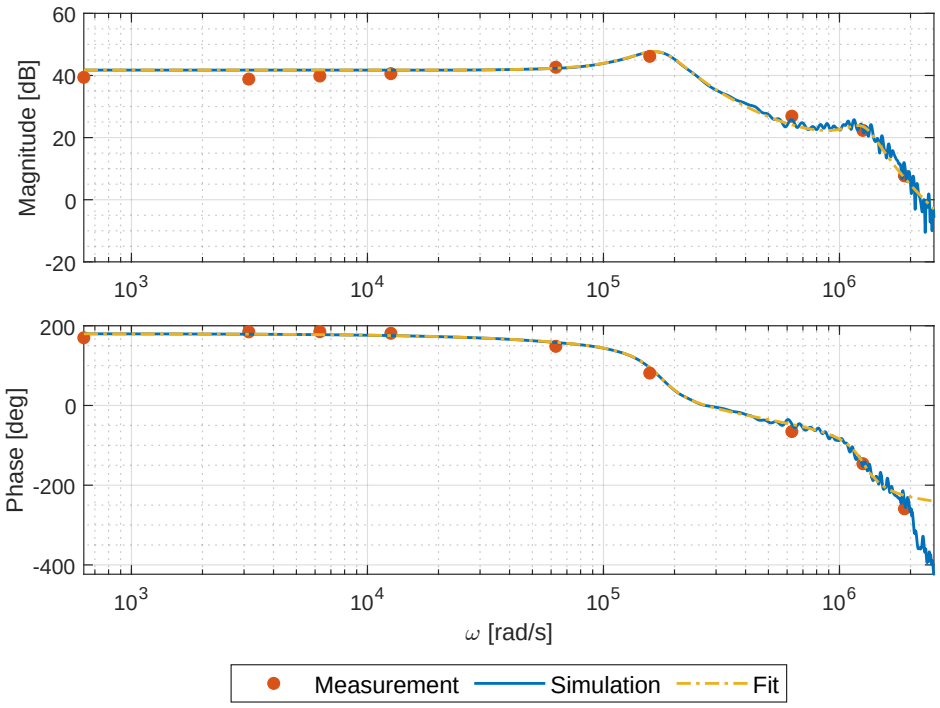


Figure 4.17: Bode plots of the converter's frequency response for $R_{\mathrm{L}} = 11\,\Omega$. The response extracted from the step response is shown in blue, experimental measurements using sinusoidal perturbation are indicated with orange dots, and the rational function fitting is shown in yellow. The close agreement between simulation and measurement confirms the validity of the proposed extraction method.

4.2.2 Impact of load R_L on converter dynamics

Because small-signal models are formally local (valid only in a neighbourhood of a given operating point), the step-response identification was repeated at multiple load resistances R_L while maintaining the same regulated output voltage. This serves two purposes. First, it verifies that the selected model structure (third-order numerator, fifth-order denominator) consistently captures the plant dynamics across the operating range. Second, it quantifies how poles and zeros move with load, revealing which dynamics are invariant and which are load-dependent.

Table 4.1: Operating parameters ensuring regulated output voltage at the selected load values.

Parameter	$R_L = 5\Omega$	$R_L = 10\Omega$	$R_L = 20\Omega$
f_{op}	5.01 MHz	5.4 MHz	6.03 MHz
D	0.56	0.5	0.21

Table 4.1 summarises the operating parameters corresponding to each tested load resistance. For every value of R_L, the duty cycle D and switching frequency f_{op} are adjusted to ensure that the output voltage remains regulated at the nominal value of 36 V.

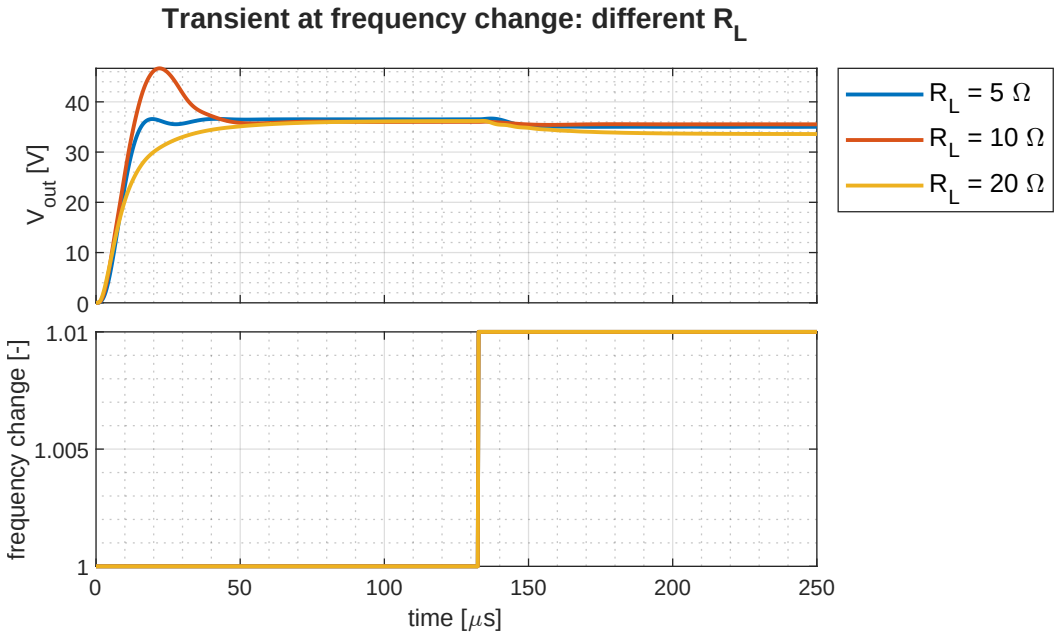


Figure 4.18: Output voltage transient response to the step perturbation for different loads R_L.

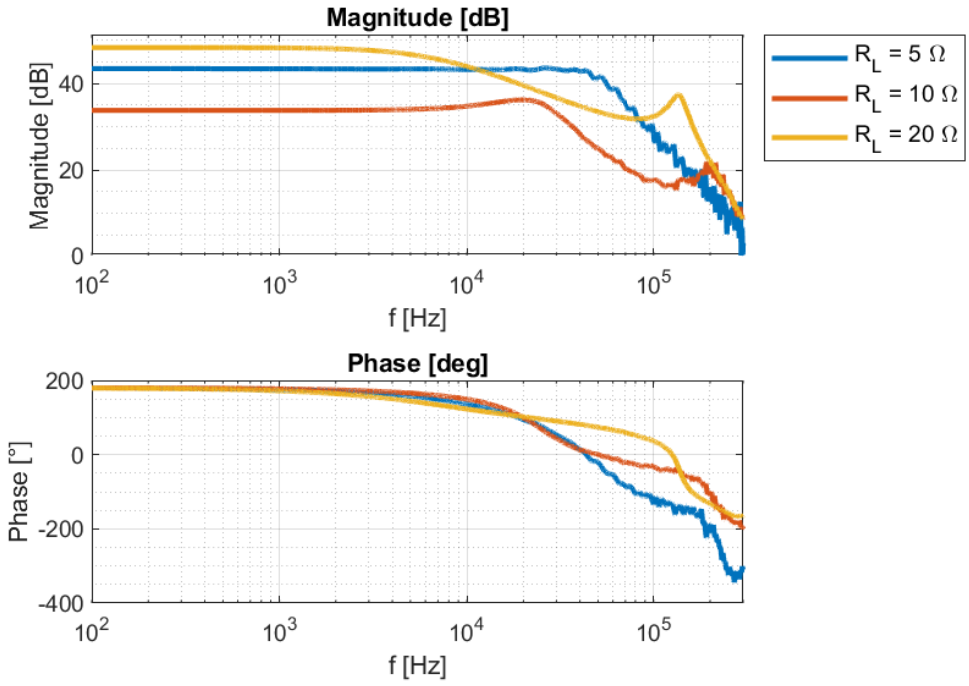


Figure 4.19: Bode plots of the converter transfer function for different load values R_L obtained from the step-perturbation method.

The procedure described in section 4.2 was repeated to evaluate the converter frequency response under different load conditions. For completeness, the main steps are briefly recalled here. Fig. 4.18 shows the applied normalised step perturbation and the corresponding output voltage transients for the three tested loads. In each case, the

output voltage response was isolated in steady state and resampled at a fixed rate, after which the corresponding control-to-output transfer function $H_{R_L}(s)$ was computed using equation (4.17). Fig. 4.19 presents the resulting Bode plots for the three selected load conditions.

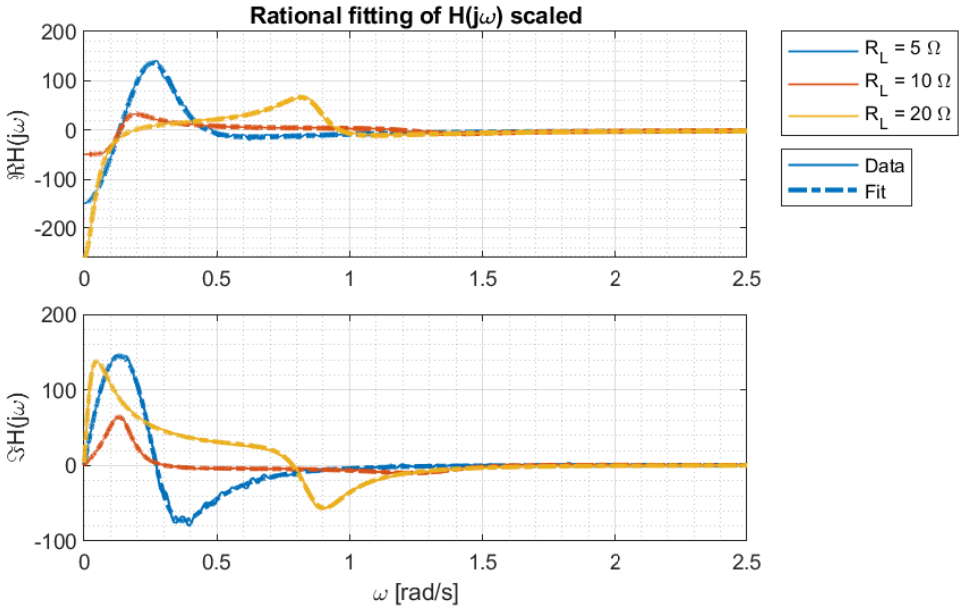


Figure 4.20: Real and imaginary components of the converter transfer function $H_{R_L}(j\omega)$ for different loads: numerical extraction (solid line) versus fitted model (dash-dotted line).

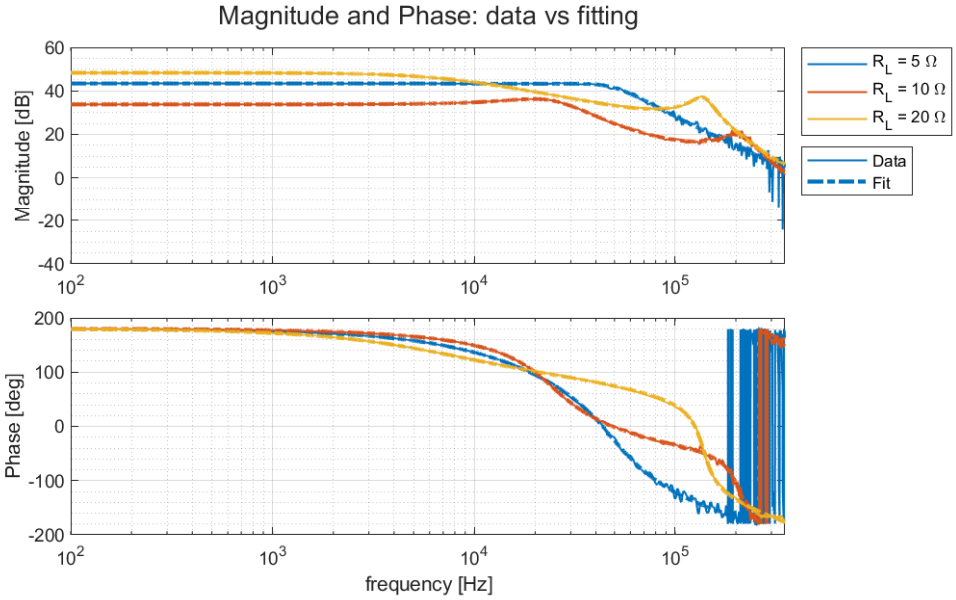


Figure 4.21: Bode plots of the converter transfer function for different loads R_L: comparison between the numerically obtained data (solid line) and the fitted model (dash-dotted line)

As in the previous section, a rational polynomial fitting was carried out, enforcing the

same model structure with three zeros and five poles as in (4.20). The good agreement between the data and the fitting can be appreciated in Figs. 4.20 and 4.21, where the numerically obtained data are compared against the fitted model. Specifically, Fig. 4.20 compares the real and imaginary parts of $H_{R_L}(j\omega)$, while Fig. 4.21 compares the corresponding Bode plots.

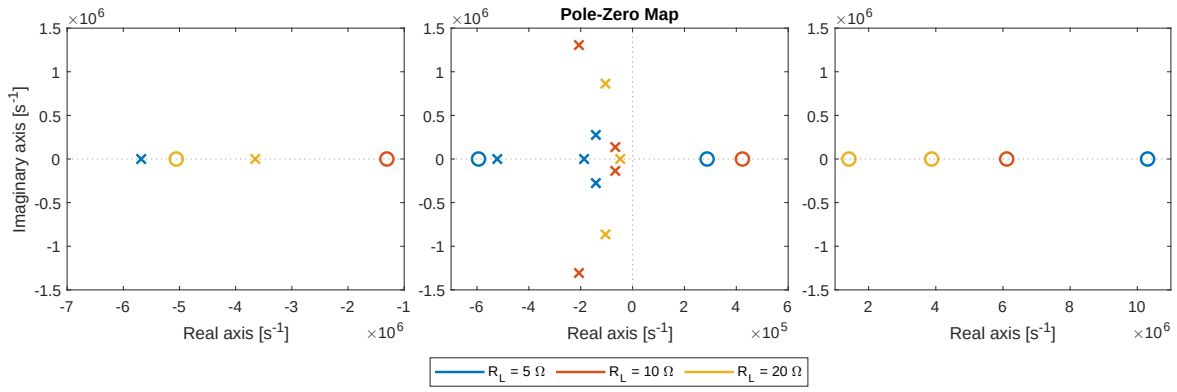


Figure 4.22: Pole-zero map of the converter transfer function for the selected loads. Crosses denotes poles and circles the zeros. For clarity, the plots are split into three sections of the x-axis.

Finally, Fig. 4.22 shows the pole-zero maps of the converter transfer functions $H_{R_L}(s)$ for the tested load values.

The results show that the converter is consistently described by a rational function with three zeros and five poles, confirming the invariance of the chosen structure. The location of poles and zeros vary with R_L, as illustrated in Fig. 4.22. The two right-half-plane zeros persist across all tested loads, reflecting an intrinsic property of the topology. Their frequency shifts with load, one moving slightly lower and the other slightly higher as R_L increases. The left-half-plane (LHP) zero exhibits a pronounced migration with load, moving toward higher frequencies for lighter loads.

This movement of the LHP zero is directly visible in the Bode plots of Fig. 4.19. At lighter loads, the magnitude response exhibits a noticeable inflection at higher frequencies, where the gain temporarily rises before resuming its roll-off. This feature corresponds to the LHP zero partially compensating the effect of the nearby poles. A modest phase recovery is observed in the same frequency range, consistent with the additional phase lead contributed by the zero. Together, these effects highlight that the dominant source of load-dependent variation in the dynamics is the shifting LHP zero.

It can be observed that the low-frequency gain of the small-signal transfer function also varies with load. This is consistent with the dc gain characteristic of the converter

$G_v(f, R_L) = V_{\text{out}}/V_{\text{in}}$, which describes the steady-state voltage gain as a function of the switching frequency and the load. When the perturbation Δf applied to the control variable is sufficiently slow, the converter responds quasi-statically, and the output variation can be approximated as

$$H(0) \approx V_{\text{in}} \left.\frac{\partial G_v(f, R_L)}{\partial f}\right|_{f=f_{\text{op}}} f_{\text{op}}. \tag{4.34}$$

This relation shows that the low-frequency gain of the small-signal transfer function is proportional to the local slope of the dc conversion curve $G_v(f, R_L)$ at the operating point f_{op}. If the slope is steep, small perturbations of the switching frequency cause larger changes in the output, resulting in a higher small-signal gain. Conversely, a flatter slope corresponds to a lower gain. This is shown in Fig. 4.23

Since the operating frequency must be adjusted to maintain the same regulated output voltage across different load conditions, the operating point shifts along the dc gain curve. The static small-signal gain therefore directly reflects the local slope of this curve.

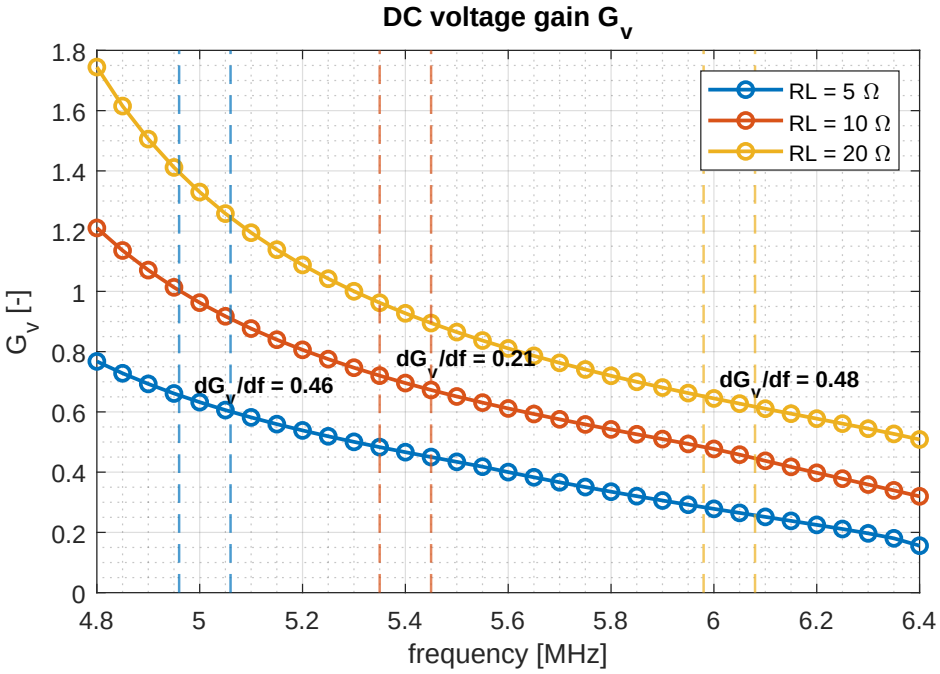
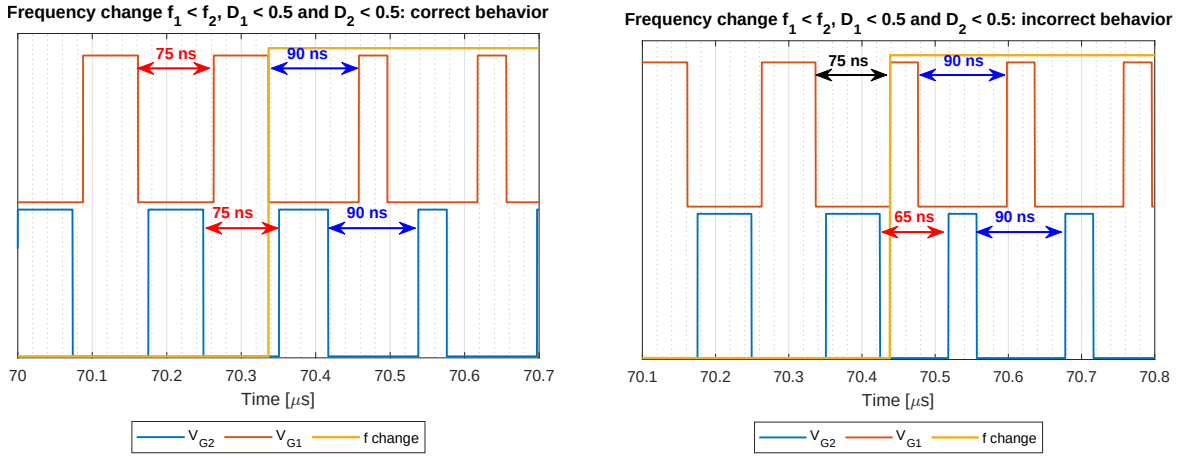


Figure 4.23: dc-dc gain curves as a function of the switching frequency for the three selected loads. The slope at the operating point is expressed in [1/MHz].

4.3 Practical considerations for frequency control

4.3.1 Frequency change update sequence

While the previous analysis confirms that output voltage regulation can be achieved through frequency variation, the implementation of frequency control requires particular care, especially during the frequency transition.



(a) (b)

Figure 4.24: Detail of the gate signals at the instant of frequency change: (a) symmetry of the off-times preserved (correct transition), (b) symmetry of the off-times not preserved (incorrect transition).

In a push-pull Class E inverter, the two transistors operate with 180° phase shift. For safe operation under frequency control, it is essential that the off-time of the two switches remains equal at the instant of a frequency change. This guarantees that the shunt capacitors C_{p_1} and C_{p_2} charge and discharge symmetrically, thereby preventing voltage imbalance between the two devices.

If a frequency step is applied without preserving symmetry, one device may be forced to turn on earlier than the other, leading to unequal capacitor voltages and unbalanced drain waveforms. This condition can cause excessive device dissipation, overstress, or even destructive over-voltage.

Figures 4.25 and 4.26 illustrate this effect using LTspice simulations for the case of an increase in frequency ($f_1 < f_2$) with duty cycles below 0.5. If the frequency step is applied without preserving the balance between the off-times, the two drain voltages become unbalanced, causing a voltage overstress on one of the devices. Although the first occurrence may not immediately destroy the switch, repeated operation under these conditions would inevitably lead to device failure. Conversely, when symmetri-

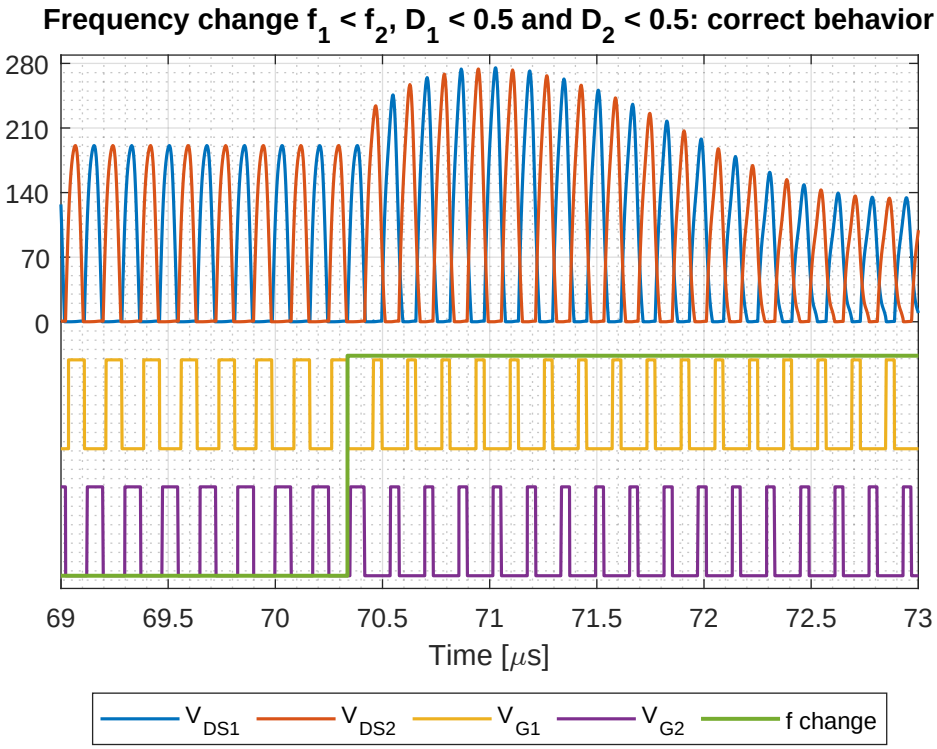


Figure 4.25: Frequency change from lower to higher frequency ($f_1 < f_2$) with duty cycles $D_1, D_2 < 0.5$ – *correct transition.*

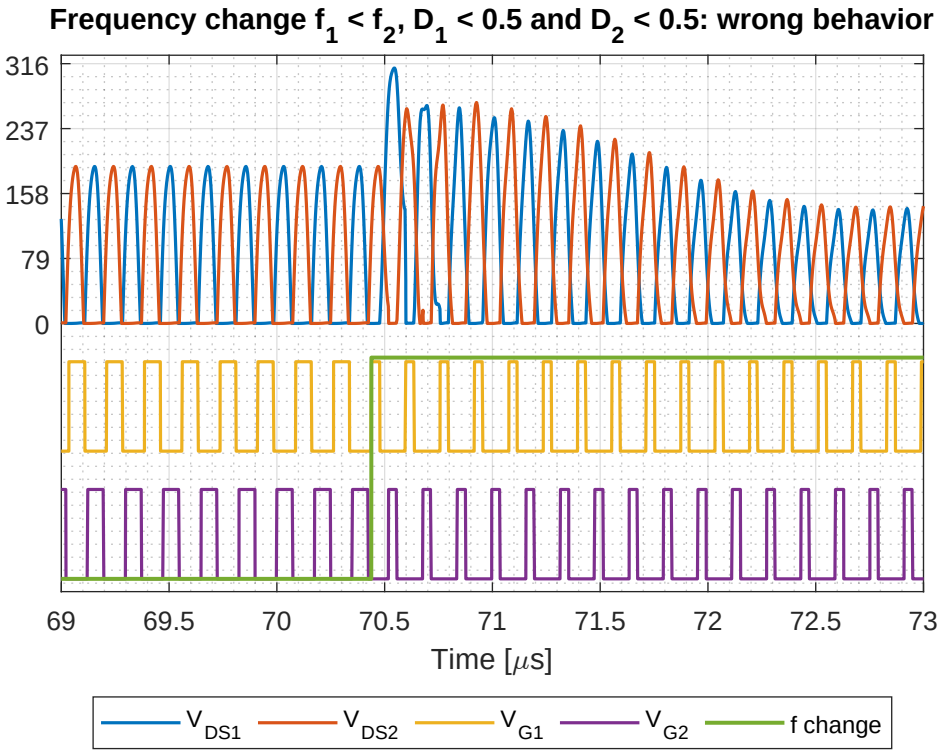


Figure 4.26: Frequency change from lower to higher frequency ($f_1 < f_2$) with duty cycles $D_1, D_2 < 0.5$ –*incorrect transition.*

cal off-times are maintained during the frequency change, the drain voltages remain balanced and the transition is smooth.

Figures 4.24a and 4.24b show the corresponding detail of the gate signals at the instant of the frequency transition in the correct and incorrect cases. It can be observed that correct behaviour is achieved when the off-times of the control signals remain equal across the change, even if the on-times differ.

Figures 4.27-4.30 show other simulated transition cases for $f_1 < f_2$ with duty cycles either below, above, or crossing $D = 0.5$. The same qualitative behaviour is observed: when the off-time symmetry is not preserved at the instant of frequency change, potentially damaging unbalance of the drain voltages is observed.

Although frequency transitions in both directions (frequency increase $f_1 < f_2$ or frequency decrease $f_1 > f_2$) can lead to unbalanced operation if the off-time symmetry is not preserved, the observed effects from simulation are different.

When the switching frequency is increased ($f_1 < f_2$), the effective period (and off-time) shortens leading to the asymmetric condition if the transition is not done correctly.

Conversely, when the frequency decreases ($f_1 > f_2$), the period (and the off-time) lengthens so both drain capacitors have likely sufficient time to discharge, making the switching transition generally less potentially damaging than the other case. However, asymmetric timing still causes unequal conduction intervals and unbalanced drain currents, leading to increased losses and thermal imbalance.

Figures 4.31-4.32 illustrates the behaviour observed when the switching frequency is decreased ($f_1 > f_2$), both in the correct and incorrect transition cases. In this case, the unbalance in the drain voltages doesn't result in an overshoot but the unequal conduction intervals between the two devices result in asymmetric current waveforms.

The discussion above highlights that frequency transitions must be carefully managed to preserve symmetry and avoid waveform imbalance. These requirements directly influence how frequency control can be implemented in practice on a digital platform. The next section describes how these aspects are realised on the STM32H7 microcontroller, outlining the implementation strategy as well as the practical limits imposed by the digital hardware.

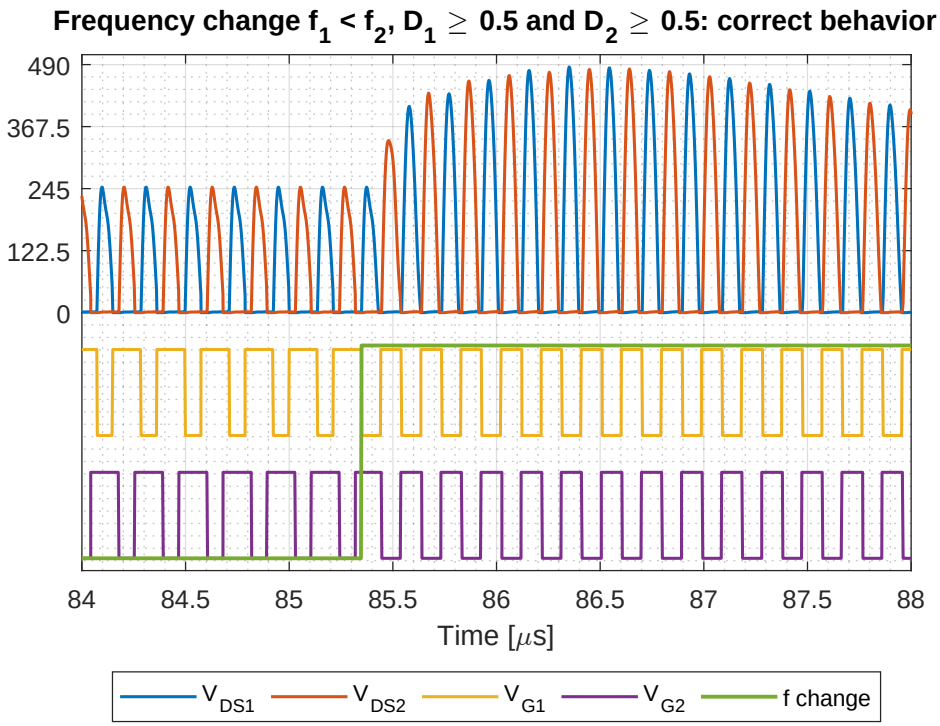


Figure 4.27: Frequency change from lower to higher frequency ($f_1 < f_2$) with duty cycles $D_1, D_2 \geq 0.5$ – *correct transition.*

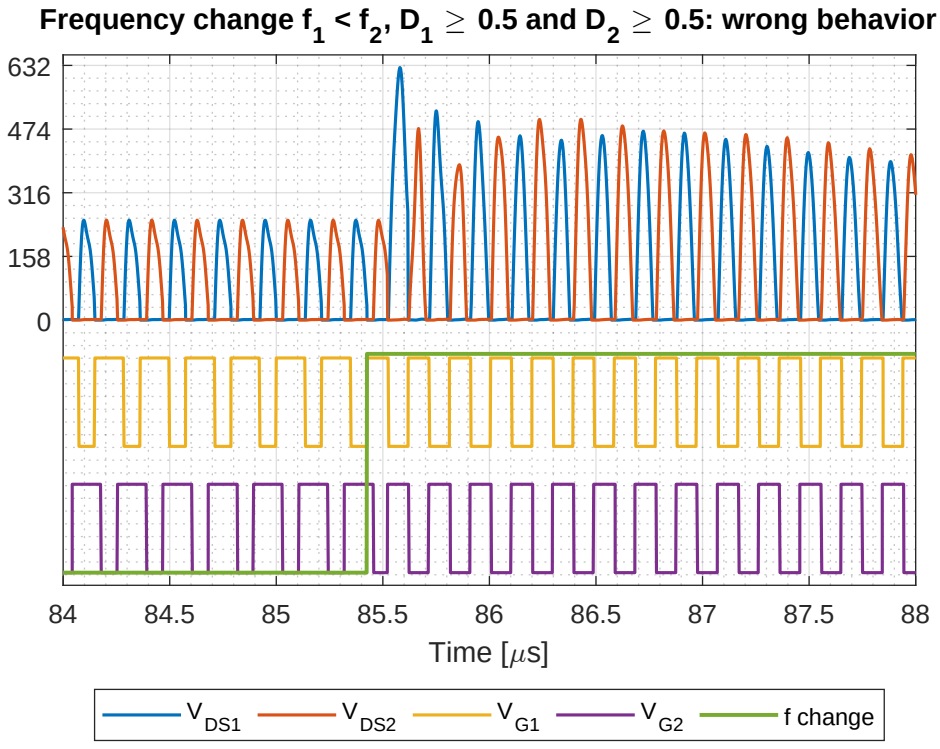


Figure 4.28: Frequency change from lower to higher frequency ($f_1 < f_2$) with duty cycles $D_1, D_2 \geq 0.5$ – *incorrect transition.*

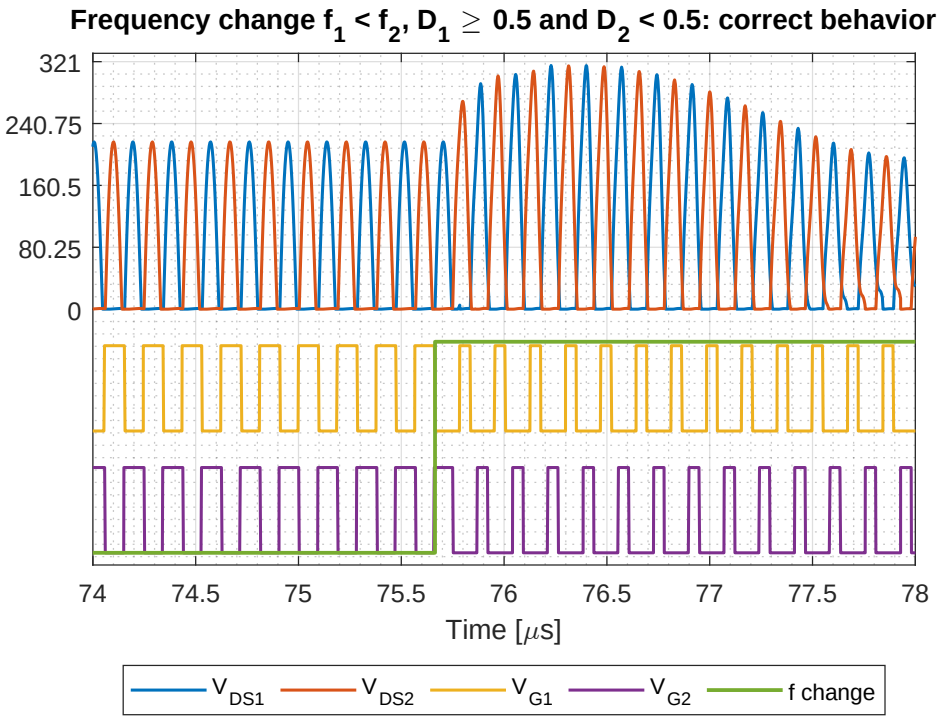


Figure 4.29: Frequency change from lower to higher frequency ($f_1 < f_2$) with duty cycles going from more than 0.5 to less than 0.5 ($D_1 \geq 0.5$, $D_2 < 0.5$) – *correct transition*.

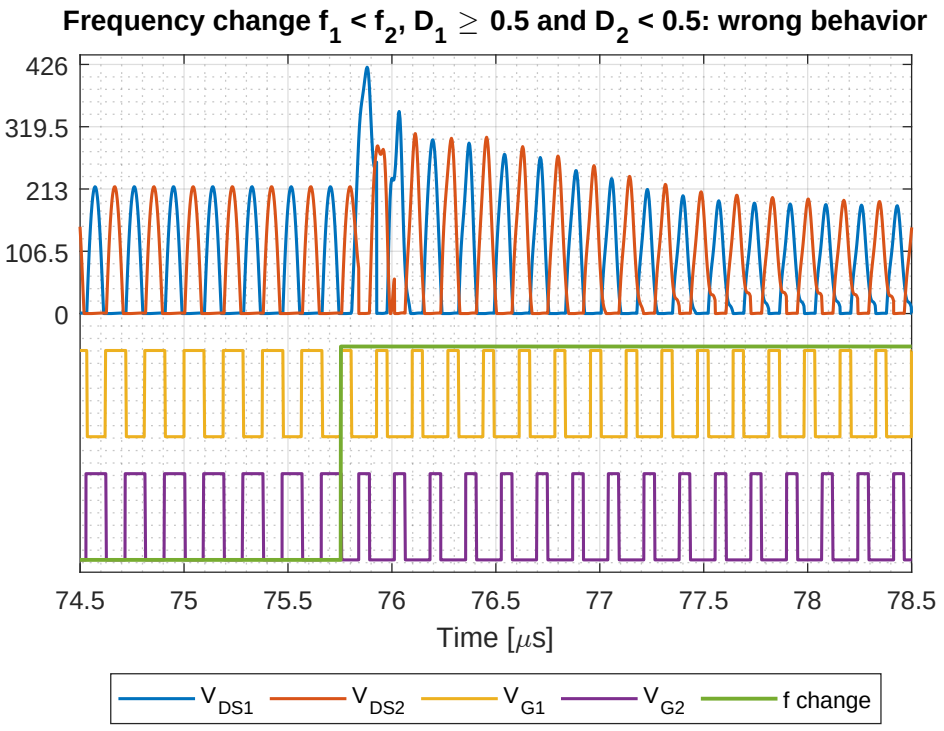


Figure 4.30: Frequency change from lower to higher frequency ($f_1 < f_2$) with duty cycles going from more than 0.5 to less than 0.5 ($D_1 \geq 0.5$, $D_2 < 0.5$) – *incorrect transition*.

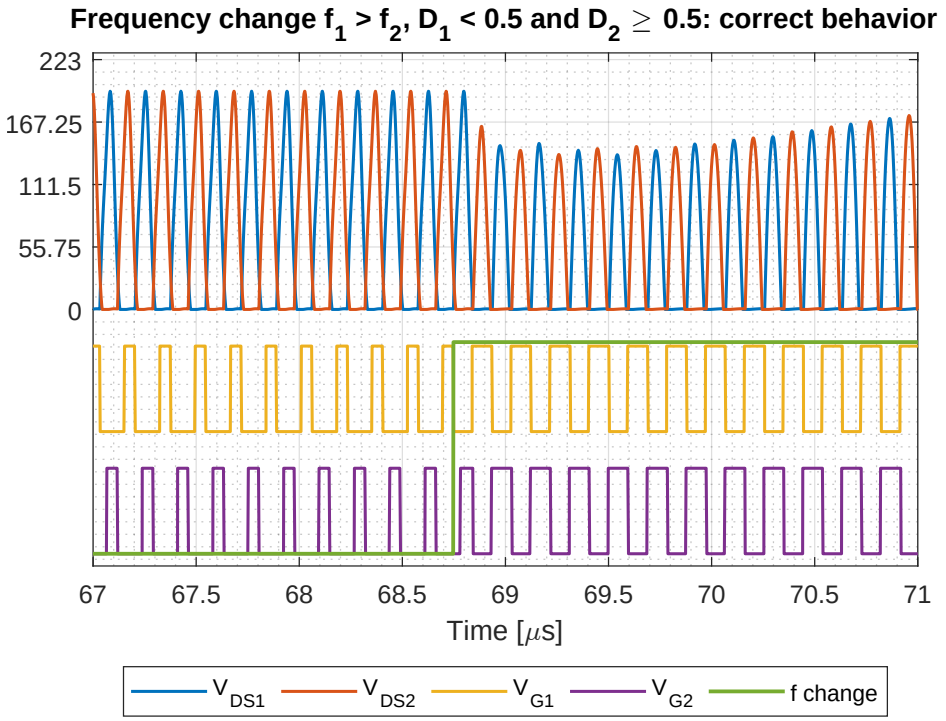


Figure 4.31: Frequency change from higher to lower frequency ($f_1 > f_2$) with duty cycles going from less than 0.5 to more than 0.5 ($D_1 < 0.5$, $D_2 \geq 0.5$) – *correct transition*.

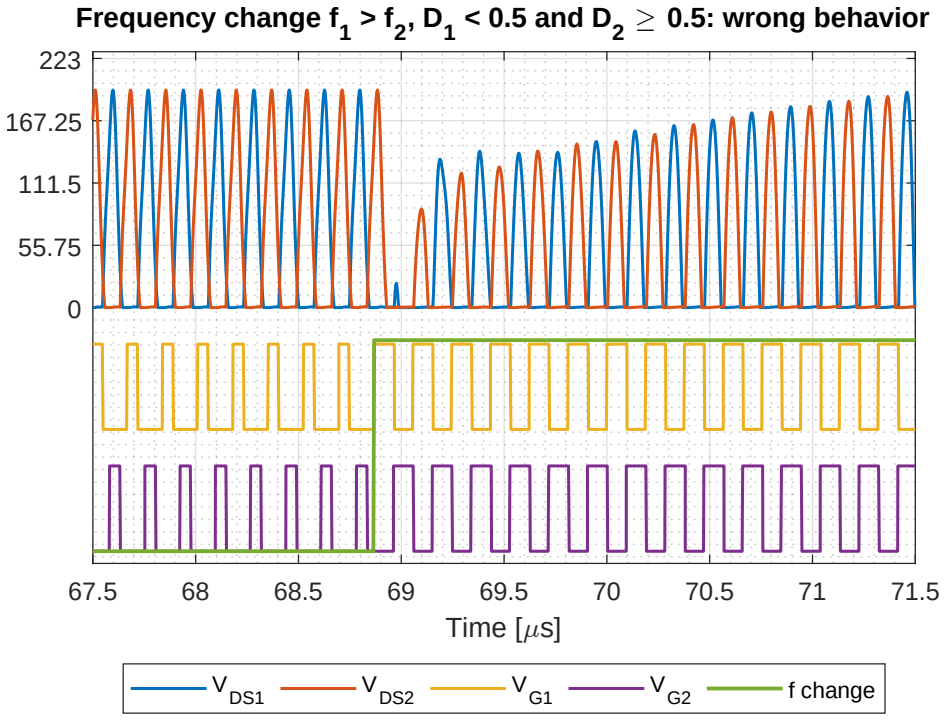


Figure 4.32: Frequency change from higher to lower frequency ($f_1 > f_2$) with duty cycles going from less than 0.5 to more than 0.5 ($D_1 < 0.5$, $D_2 \geq 0.5$) – *incorrect transition*.

4.3.2 STM32 implementation

The gate signals and control scheme were generated using a Nucleo-144 development board equipped with an STM32H743ZI microcontroller [75]. The implementation relies on the High-Resolution Timer (HRTIM) peripheral, which is specifically designed for digital power conversion applications and capable of producing precise and complex timing sequences, such as phase-shifted or complementary PWM signals [76]. Each HRTIM timer block includes an internal 16-bit counter clocked by the system frequency (480 MHz for the selected Nucleo board), providing a timing resolution of approximately 2 ns.

Each timer features two independent PWM output channels that share the same time base. Each channel can toggle its output either when the counter matches one of the four programmable comparator values or when the counter rolls over.

For synchronisation purposes, the two channels belonging to the same timer are used, since they inherently share the same counter. This avoids potential phase mismatches that may occur if two separate HRTIM timers were employed, due to small timing jitter between their respective counters.

To ensure deterministic and synchronous updates of both frequency and duty cycle, the *preload register* functionality of the HRTIM was also employed. This feature allows the new values of the period and comparator registers to be written in advance (preloaded) and then simultaneously transferred to the active registers upon a specific synchronisation event, typically at the timer roll-over. In this way, both PWM channels update their parameters at exactly the same instant, preventing any loss of phase alignment or unwanted transient behaviours during frequency transitions.

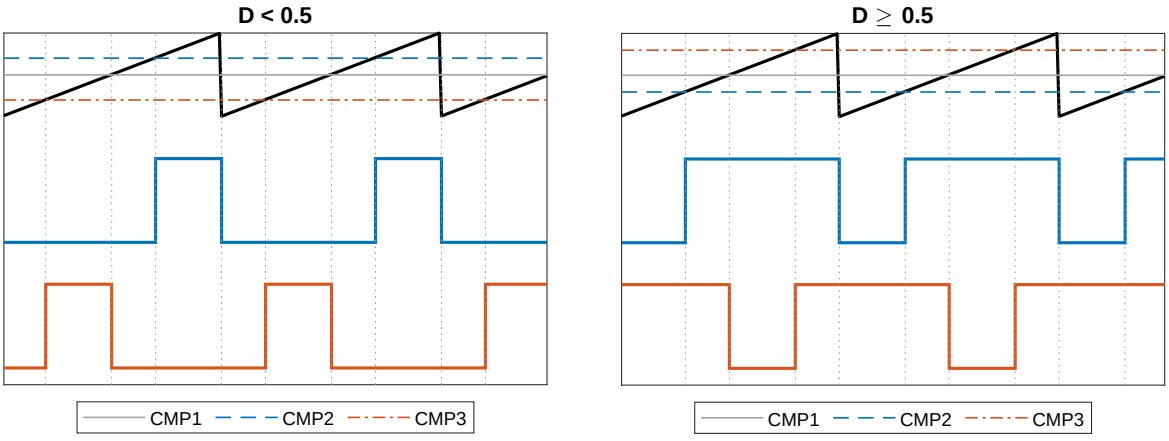
Since the symmetry between the off-times of the two switches must be preserved and their phase shift maintained at 180°, the most convenient choice is to apply the frequency and duty cycle updates at the falling edge of the "master" gate signal V_{G_1}. This ensures that the new period and on/off times are introduced synchronously while maintaining both the phase relationship and the required symmetry between the complementary gate signals. The "slave" gate signal V_{G_2} automatically follows with a 180° phase shift, as both signals are generated by the same HRTIM timer and share the same counter.

The counter operates in up-counting mode, generating a periodic waveform whose period defines the switching frequency of the converter. Given the counter clock frequency of 480 MHz, the number of timer clock cycles N_{clk} required to achieve a desired

switching frequency f is:

$$N_{\text{clk}} = \frac{480 \times 10^6}{f}. \tag{4.35}$$

This value is written to the period register of the HRTIM timer $\texttt{PER} = N_{\text{clk}}$, which determines the number of counter increments per switching period and thus directly sets the output frequency.



(a) (b)

Figure 4.33: Graphical explanation of the comparators configuration used to generate the gate signals for (a) $D < 0.5$ (b) for $D \geq 0.5$.

The duty cycle of each gate signal is defined by the timing of the rising and falling edges, which are controlled by the programmable comparator registers of the HRTIM. For the "master" gate signal V_{G_1}, the falling edge is aligned with the end of the period, while the rising edge – which sets the duty cycle – is triggered by comparator `CMP2`. The comparator value is computed as:

$$\texttt{CMP2} = (1 - D)\, N_{\text{clk}}, \tag{4.36}$$

where D is the duty cycle and N_{clk} is the total number of timer counts per period.

The "slave" gate signal V_{G_2} operates with a fixed 180° phase shift relative to the master. Its falling edge occurs at the midpoint of the period, defined by:

$$\texttt{CMP1} = \frac{N_{\text{clk}}}{2}, \tag{4.37}$$

while its rising edge, set by `CMP3`, depends on the duty cycle. To maintain symmetry between the two gate signals, the comparator value `CMP3` is defined as:

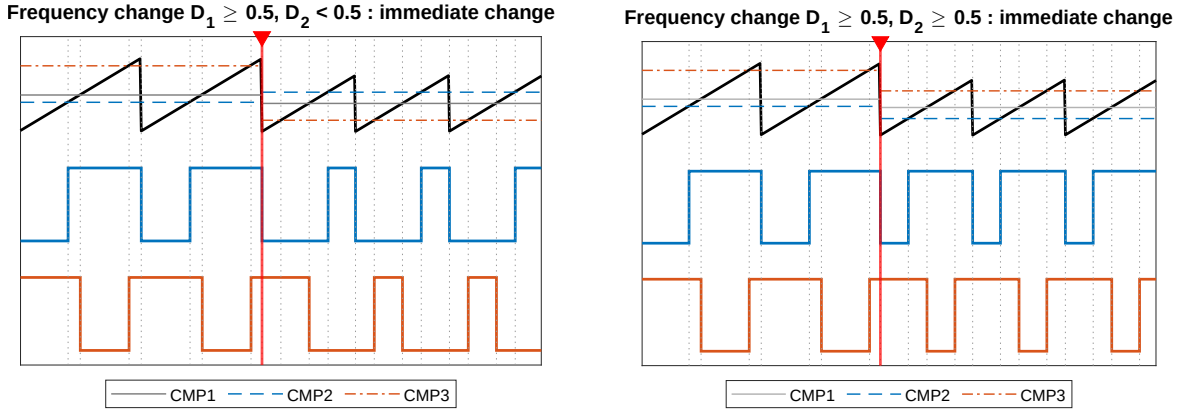
$$\texttt{CMP3} = \begin{cases} \texttt{CMP1} - D\, N_{\text{clk}}, & \text{if } D < 0.5, \\ \texttt{CMP1} + (1 - D)\, N_{\text{clk}}, & \text{if } D \geq 0.5. \end{cases} \tag{4.38}$$

This configuration guarantees that the two gate signals remain complementary and maintain the required 180° phase shift for any operating duty cycle.

The generation of the two complementary gate signals using the HRTIM is illustrated in Fig. 4.33. The black sawtooth waveform represents the timer counter, which resets at the end of each period. The blue and orange waveforms correspond to V_{G_1} and V_{G_2}, respectively. The horizontal lines indicate the comparator thresholds (`CMP1`, `CMP2`, and `CMP3`) that define the rising and falling edges of each signal depending on the duty cycle value.

When performing a frequency transition, simply enabling the preload registers of the HRTIM peripheral does not by itself guarantee that the symmetry of the off-times between the two gate signals is preserved. The correct timing of the updates must also account for the specific combination of the initial and final duty cycles. Depending on whether the duty cycle before and after the frequency change is above or below 50%, different update sequences must be applied to the HRTIM compare registers.

If the initial duty cycle D_1 is greater than 50%, all the affected registers – namely the period register `PER` and the compare registers `CMP1`, `CMP2`, and `CMP3` – can be updated simultaneously at the next timer roll-over event. This ensures that both gate signals maintain symmetrical off-times and a constant 180° phase shift.



(a) $D_1 \geq 0.5$, $D_2 < 0.5$ (b) $D_1 \geq 0.5$, $D_2 \geq 0.5$

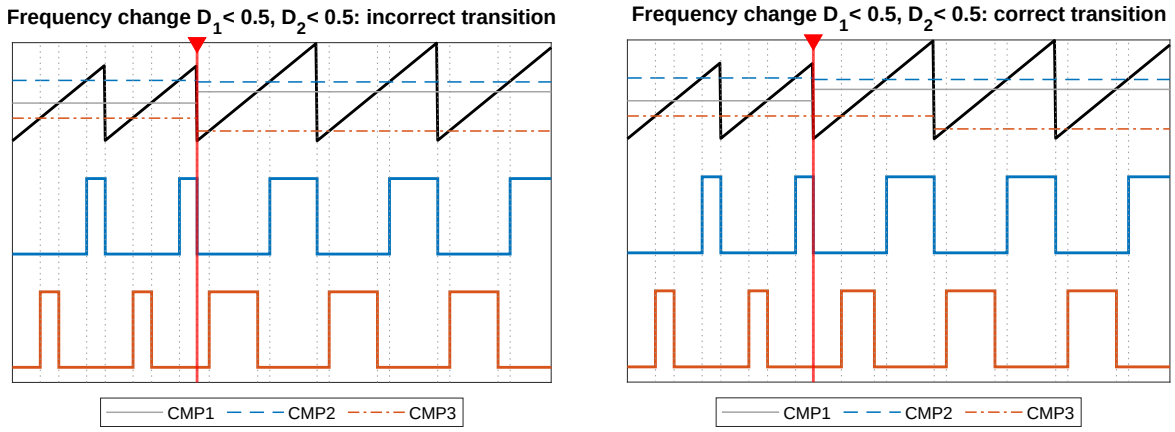
Figure 4.34: Update logic for the case $D_1 \geq 0.5$ and (a) $D_2 < 0.5$ or (b) $D_2 \geq 0.5$. The red cursor represents the instant of frequency and duty cycle update. All the affected registers can be updated simultaneously. It can be noticed that the on-time of V_{G_2} in the first period after the change is different than the final value.

Fig. 4.34 illustrates the update logic for the case where the initial duty cycle satisfies $D_1 \geq 0.5$. At the instant of the frequency update, indicated by the red cursor, the gate signal V_{G_2} is already high, having completed its off-time corresponding to the previous

PER value. Consequently, all HRTIM registers (PER, CMP1, CMP2, and CMP3) can be updated simultaneously without disrupting the symmetry between the off-times of the two gate signals across the frequency transition. This is verified both for an increase or a decrease in the switching frequency.

If the initial duty cycle is below 50%, an immediate update of CMP3 would break the symmetry between the gate signals, since V_{G2} has not yet completed its off-time corresponding to the previous PER value. In this case, a different update strategy must be applied to preserve the symmetry of the off-times during the frequency transition.

Two subcases can be distinguished depending on the final duty cycle D_2. If $D_2 < 0.5$, CMP3 must retain its previous value for one additional period following the frequency change, while the new PER, CMP1, and CMP2 values take effect immediately. CMP3 is then updated to its new value at the next timer roll-over event, thereby restoring full symmetry from that point onward.



(a) Incorrect transition.

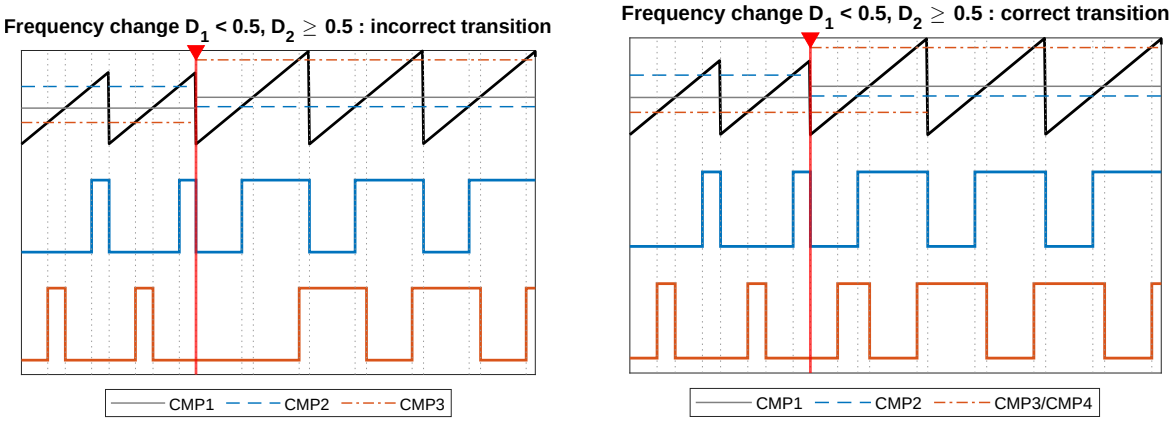
(b) Correct transition.

Figure 4.35: Update logic for the case $D_1 < 0.5$ and $D_2 < 0.5$. The red cursor represents the instant of frequency and duty cycle update. In (a) all the affected registers are updated simultaneously, leading to an incorrect transition. In (b), the register CMP3 is changed with a delay of one period to obtain the correct transition behaviour.

Fig. 4.35 illustrates the update logic for the case $D_1 < 0.5$ and $D_2 < 0.5$. Fig. 4.35a shows the incorrect transition, corresponding to the immediate update of all registers at the frequency change instant. As can be observed, this results in asymmetric off-times across the transition. Conversely, Fig. 4.35b shows the correct transition, in which CMP3 is updated to its new value one period later, ensuring that the off-times remain symmetric at the frequency change.

If $D_2 \geq 0.5$, the update logic employs an additional comparator, CMP4, since the

transition from a duty cycle below 50% to one above 50% requires the switching edge to move from before to after the period midpoint (CMP1). As in the previous case, the comparator CMP3 must retain its previous value for one additional period following the frequency change to preserve the off-time symmetry. Within the same first period after the update, however, the new duty cycle value must also take effect. This is achieved by assigning the new duty cycle to CMP4, which becomes active immediately at the update event, while CMP3 maintains the previous setting until the next roll-over. All other registers (PER, CMP1, and CMP2) are updated simultaneously at the transition. At the second period after the change, CMP3 is then updated to match CMP4, restoring the standard configuration.



(a) Incorrect transition.

(b) Correct transition.

Figure 4.36: Update logic for the case $D_1 < 0.5$ and $D_2 \geq 0.5$. The red cursor indicates the instant of frequency and duty cycle update. In (a), all registers are updated simultaneously, leading to an incorrect transition with loss of symmetry in the on-times. In (b), two comparators (CMP3 and CMP4) are used during the first period after the change to ensure that symmetry of the off-times is maintained. At the next period, CMP3 = CMP4, restoring the standard configuration.

Fig. 4.36 illustrates the update logic for the case $D_1 < 0.5$ and $D_2 \geq 0.5$. Fig. 4.36a shows the incorrect transition, corresponding to the immediate update of all registers at the frequency and duty change instant. In this case, the asymmetry between the on-times across the transition is evident, as one on-interval of V_{G_2} is missing during the first period after the change. Conversely, Figure 4.36b shows the correct transition, where both CMP3 and CMP4 are active during the first period to preserve symmetry. From the second period onward, CMP3 is set equal to CMP4.

This conditional update strategy guarantees that, regardless of the direction or magnitude of the frequency and duty cycle change, both gate signals preserve their complementary timing and symmetric off-time relationship, preventing waveform imbalance and overstress phenomena, as discussed in the previous section.

Table 4.2: Summary of HRTIM update logic for different duty-cycle transition cases.

Initial duty D_1	**Final duty D_2**	**Update logic description**
$D_1 \geq 0.5$	D_2 any	All registers `PER`, `CMP1`, `CMP2`, `CMP3` are updated simultaneously.
$D_1 < 0.5$	$D_2 < 0.5$	`CMP3` retains its previous value for one additional period after the frequency change, while `PER`, `CMP1`, and `CMP2` are updated immediately. `CMP3` is updated at the next roll–over event.
$D_1 < 0.5$	$D_2 \geq 0.5$	An auxiliary comparator `CMP4` is used. During the first period after the change, both `CMP3` (previous value) and `CMP4` (new value) are active to maintain symmetry. At the next period, `CMP3` is updated to match `CMP4`.

Table 4.2 summarises the different update strategies implemented depending on the initial and final duty cycle values.

Experimental validation and limits.

Figures 4.37-4.40 display the measured STM32 output signals V_{G_1} and V_{G_2} captured on a Tektronix MSO58 oscilloscope. These waveforms correspond to the different frequency and duty cycle transition cases discussed in the previous section.

The results confirm that the cases where $D_1 \geq 0.5$ to any D_2, shown in Fig. 4.37 and 4.38, and where $D_1 < 0.5$ and $D_2 \geq 0.5$, depicted in Fig. 4.39, behave as expected, always exhibiting symmetrical off-times across the update events.

However, for the case $D_1 < 0.5 \rightarrow D_2 < 0.5$, shown in Fig. 4.40 , the expected symmetry of the off-times across the frequency transition is sometimes preserved, but not always. Although the HRTIM peripheral supports synchronised register preloading, the internal propagation of updates to multiple compare registers may require several clock cycles to complete. In the specific case of $D_1 < 0.5 \rightarrow D_2 < 0.5$, all registers except `CMP3` are updated at the frequency change event, while `CMP3` is updated to the new value at the next timer roll-over to preserve the off-time symmetry. However, at the high operating frequencies considered here (5 MHz-7 MHz), each PWM period consists of only about 60-90 timer clock counts. Even though the STM32H7 microcontroller operates at 480 MHz, this limited time window can occasionally be insufficient for the `CMP3` update to be processed before the next roll-over. As a result, the new `CMP3` value may miss the update window, causing one PWM cycle to be generated with a mix of old and new compare values, which temporarily breaks the symmetry of

the gate signals.

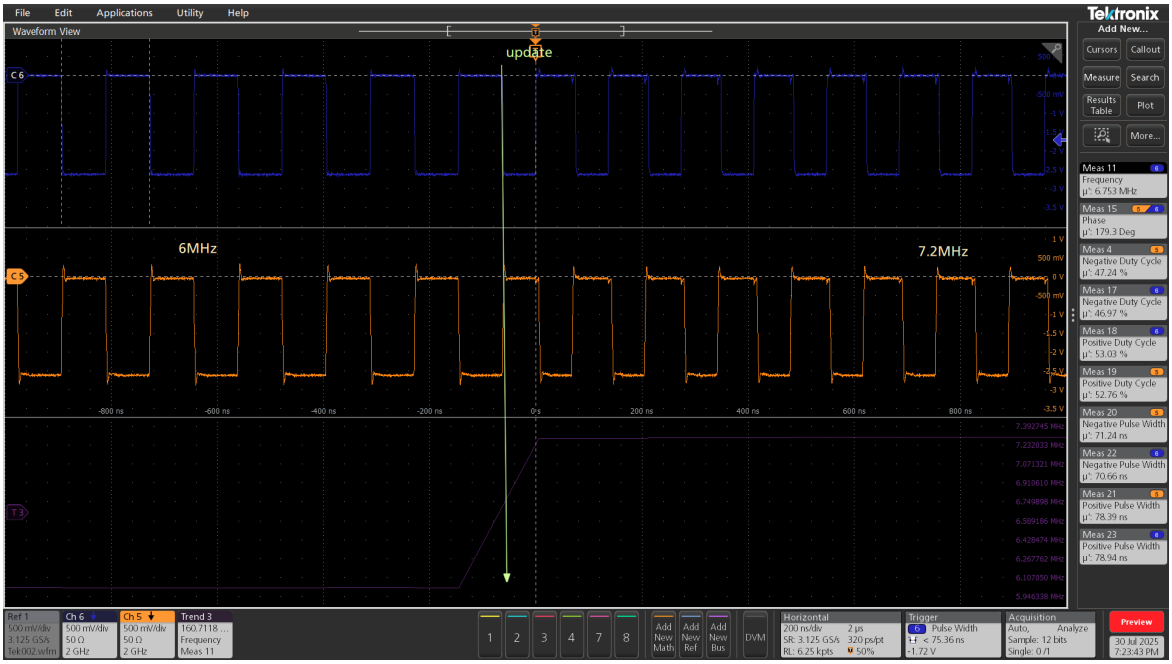


Figure 4.37: Oscilloscope screen-capture for the case $D_1 \geq 0.5 \rightarrow D_2 \geq 0.5$, showing a correct transition with preserved symmetry. The green arrow represents the update instant. On the last row, the frequency step is shown.

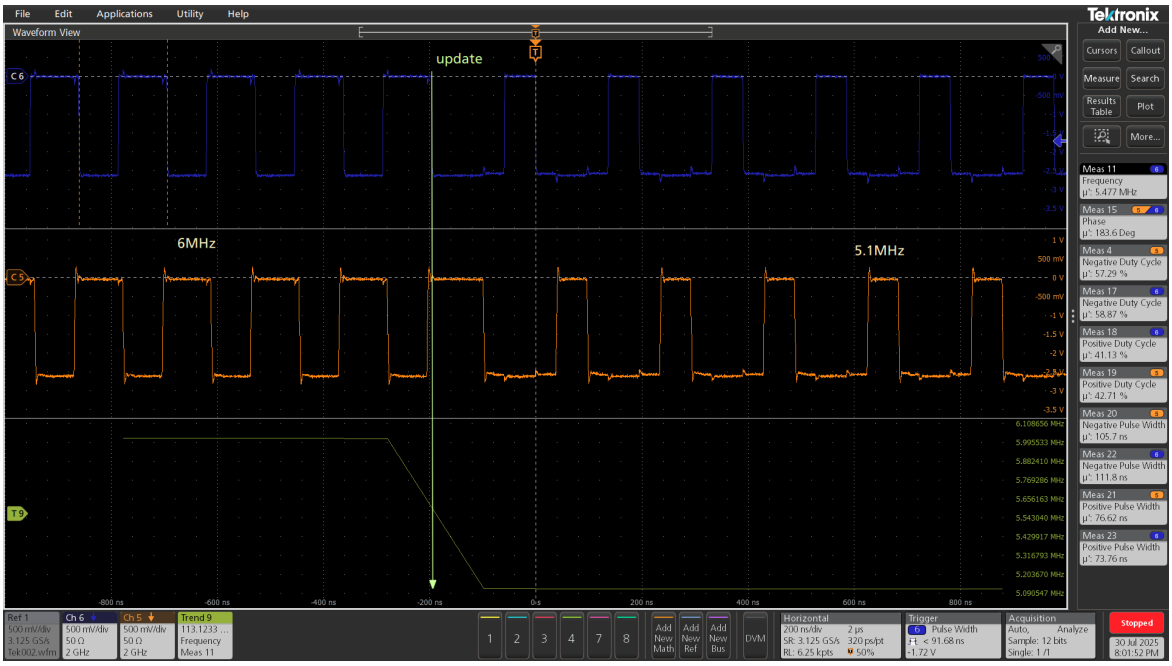


Figure 4.38: Oscilloscope screen-capture for the case $D_1 \geq 0.5 \rightarrow D_2 < 0.5$, demonstrating proper operation. The green arrow represents the update instant. On the last row, the frequency step is shown.

The case $D_1 < 0.5 \rightarrow D_2 \geq 0.5$, although it follows the same cycle-by-cycle update

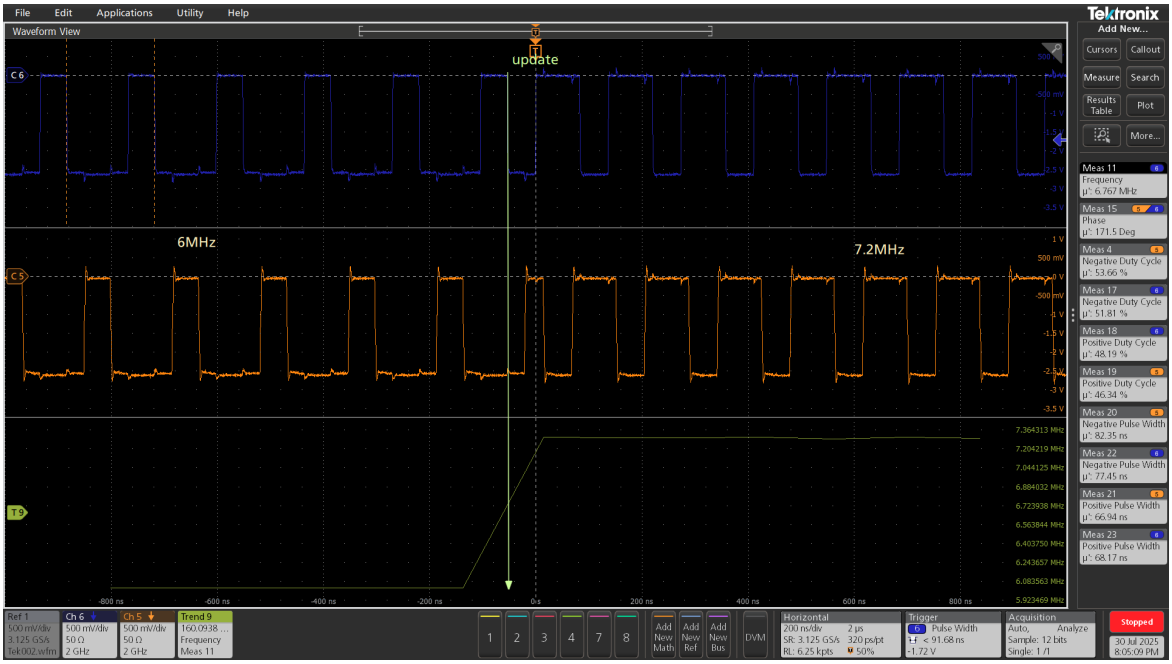


Figure 4.39: Oscilloscope screen-capture for the case $D_1 < 0.5 \rightarrow D_2 \geq 0.5$, showcasing a correct transition. The green arrow represents the update instant. On the last row, the frequency step is shown.

logic, does not suffer from this issue. In this configuration, `CMP3` occurs before the midpoint comparator `CMP1`. Therefore, even if the reassignment of `CMP3` to its new value is not completed in the second period after the update, the switching sequence remains unaffected. The gate signal V_{G_2} correctly sets at `CMP4` and resets at `CMP1`, preserving the intended symmetry. In practice, the timer simply ignores the set event at `CMP3` since the output is already high, preventing any visible distortion in the waveform.

To avoid the update inconsistencies observed in the case $D_1 < 0.5 \rightarrow D_2 < 0.5$, the update strategy was simplified: all compare registers, including `CMP3`, are updated simultaneously at the frequency transition event, without using the delayed update logic. This approach provides consistent results but requires the frequency step size to be limited, as the off-time symmetry is not preserved. By constraining the maximum frequency change per update, the resulting asymmetry between the off-times of the two gate signals remains small, minimising the imbalance between the waveforms. For larger frequency transitions, a gradual update procedure was implemented, in which both frequency and duty cycle are varied progressively in smaller steps until the desired operating point is reached.

Figure 4.41 shows an oscilloscope capture of the gradual update method. The fre-

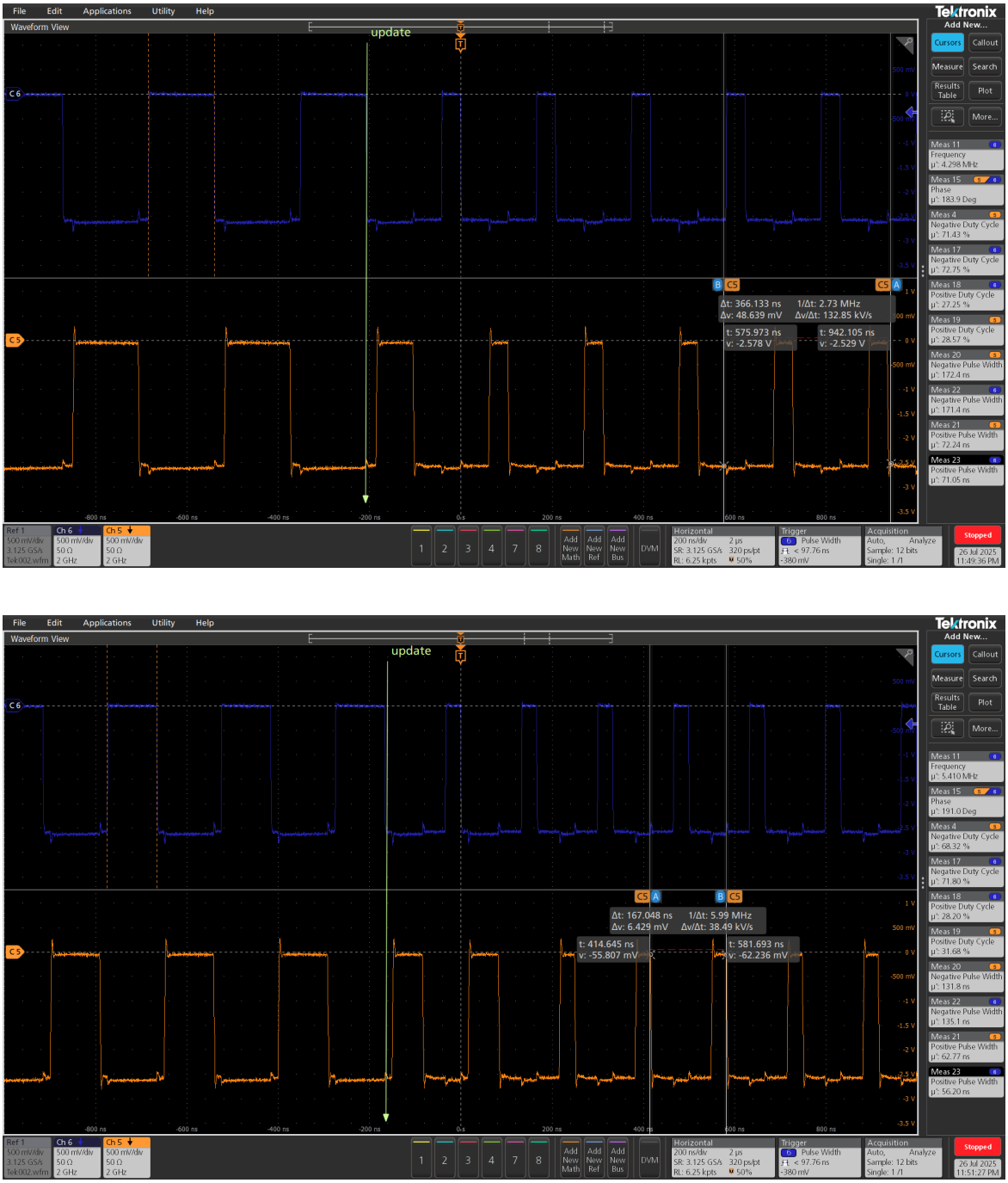


Figure 4.40: Experimental oscilloscope waveforms for the case $D_1 < 0.5, D_2 < 0.5$: (top) correct transition with preserved symmetry; (bottom) example of incorrect transition where `CMP3` misses the update window, leading to temporary asymmetry.

quency and duty cycle are changed gradually over several consecutive periods. The comparison between the correct transition, the incorrect transition, and the stepped update method for the case $D_1 < 0.5 \rightarrow D_2 < 0.5$ is shown in Fig. 4.42. In all three cases, the same overall frequency and duty cycle change is applied; however, in the stepped case, the transition is divided into five intermediate updates. As can

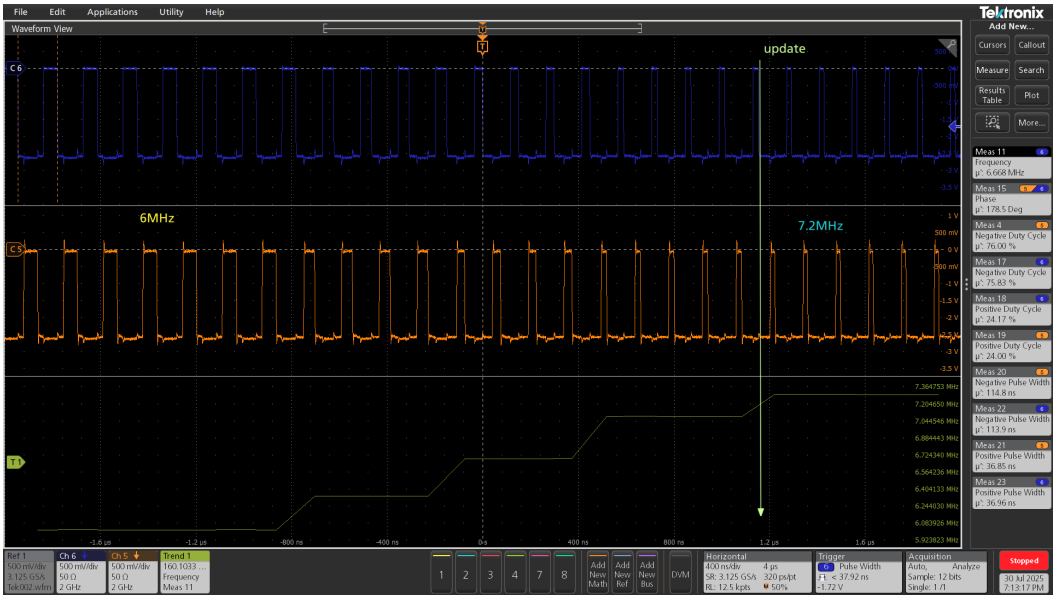


Figure 4.41: Experimental oscilloscope waveform showing the gradual frequency and duty cycle update method used to minimise off-time asymmetry of the gate signals during large transitions.

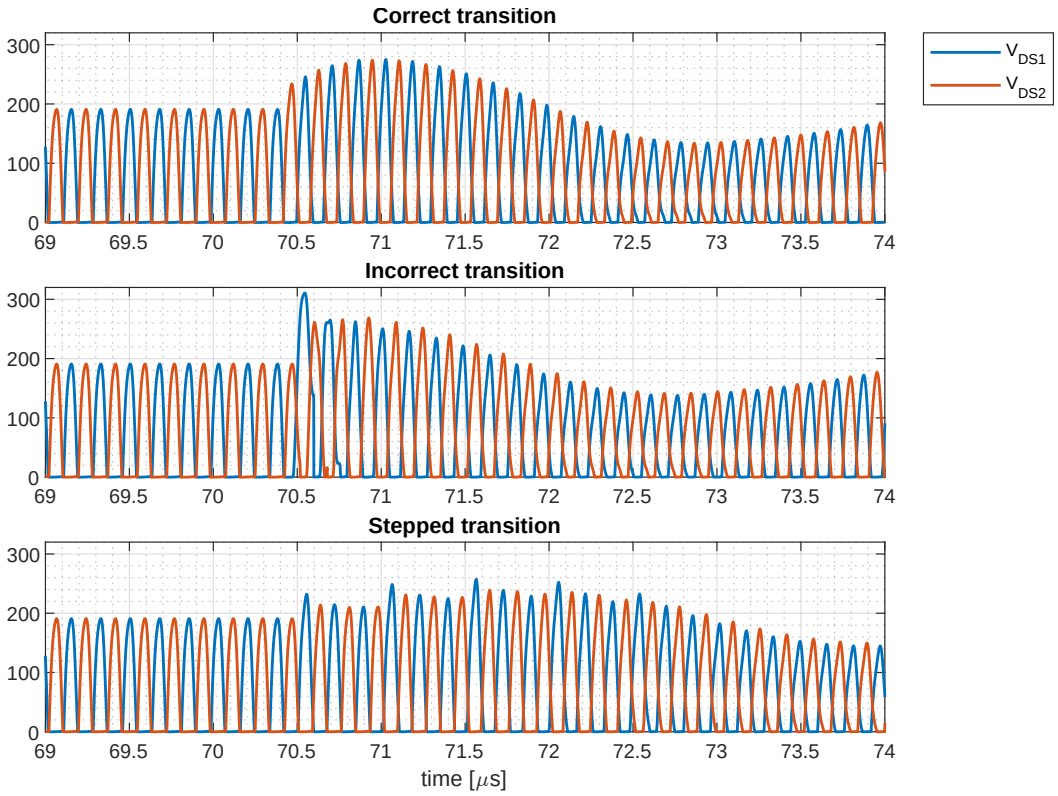


Figure 4.42: Comparison in simulation between the correct transition, incorrect transition, and stepped update method for the case $D_1 < 0.5 \rightarrow D_2 < 0.5$. The stepped case applies the same frequency and duty cycle change over five intermediate updates, significantly reducing the imbalance compared to the incorrect transition.

be observed, the voltage imbalance is significantly reduced compared to the immediate update using the incorrect transition method. This stepped approach should be regarded as a practical workaround to mitigate the limitations of the digital implementation. Naturally, it comes at the cost of a longer update time, since the transition extends over multiple switching periods. A faster microcontroller could alleviate this limitation by enabling reliable cycle-by-cycle registers update.

4.4 PID controller implementation

A discrete Proportional-Integral-Derivative (PID) controller was implemented for the output voltage regulation of the push-pull Class E^2 dc-dc converter. This control scheme was selected due to its well-established effectiveness, design flexibility, and ease of digital implementation.

Compared to analog controllers, digital controllers offer several advantages. They are less sensitive to environmental conditions, as they do not suffer from parameter drift caused by temperature variations or component ageing, which commonly affect analog implementations. Moreover, digital controllers provide greater flexibility, since their behaviour can be modified or reprogrammed at any time without requiring physical changes to the hardware components.

On the other hand, digital control systems typically exhibit a reduced bandwidth due to the effects of sampling and processing delays. They are also subject to quantisation errors and limitations imposed by the computational performance of the processing unit. Despite these drawbacks, the flexibility, reliability, and cost-effectiveness of digital controllers have made them the predominant choice for power converter control.

Table 4.3 summarises the main advantages and disadvantages of analog and digital controllers.

Table 4.3: Comparison of advantages and disadvantages between analog and digital controllers.

	Analog Controller	**Digital Controller**
Pros	• High bandwidth • High resolution • Simple implementation for low-order systems	• Reconfigurable • Immune to temperature drift and aging • Supports advanced control algorithms
Cons	• Sensitive to temperature and aging • Affected by component tolerances • Not flexible	• Limited bandwidth • Quantization and resolution limits • Dependent on CPU performance

In the next section, the PID controller transfer function is discretised from its s-domain form to obtain recursive (difference) equations suitable for implementation on a digital processor [77].

4.4.1 From Continuous-Time PID to Difference Equations

The general form of a PID controller in the s -domain is expressed as

$$C(s) = K_\mathrm{p} + \frac{K_\mathrm{i}}{s} + K_\mathrm{d}\,\frac{N}{1+\frac{N}{s}}, \tag{4.39}$$

where K_p, K_i, and K_d represent the proportional, integral, and derivative gains, respectively, and N denotes the derivative filter coefficient. The derivative term $K_\mathrm{d}s$ is implemented with a first-order low-pass filter to attenuate high-frequency noise components that would otherwise be amplified by the derivative action.

To obtain the discrete-time form suitable for digital implementation, the continuous-time transfer function is discretised using the bilinear transform [77] (also known as *Tustin's method*), which substitutes

$$s \to \frac{2}{T_\mathrm{s}}\frac{1-z^{-1}}{1+z^{-1}}, \tag{4.40}$$

where T_s is the sampling period. Applying this substitution to each term of $C(s)$ yields the discrete transfer function $C(z)$ in z-domain:

$$C(z) = K_\mathrm{p} + K_\mathrm{i}\,\frac{T_\mathrm{s}}{2}\,\frac{z+1}{z-1} + K_\mathrm{d}\,\frac{N}{1+N\,\frac{T_\mathrm{s}}{2}\,\frac{z+1}{z-1}}. \tag{4.41}$$

By expressing $C(z)$ as a rational function of z^{-1} – which represents a one-sample delay in time domain – and applying the inverse $\mathcal{Z}$-transform, the controller output can be written in the time domain as an algebraic recursive equation (difference equation) [77]:

$$\psi[k] \;=\; A_1\,\psi[k-1] \;+\; A_2\,\psi[k-2] \;+\; B_0\,e[k] \;+\; B_1\,e[k-1] \;+\; B_2\,e[k-2]. \tag{4.42}$$

In (4.42), $\psi[k]$ is the control output, $e[k]$ is the error signal, and the coefficients A_i, B_i are computed from K_p, K_i, K_d, N, and T_s according to the Tustin discretisation:

$$\begin{aligned}
A_1 \;&=\; 1-\frac{a_1}{a_0}, \qquad A_2 \;=\; \frac{a_1}{a_0}, \qquad B_i \;=\; \frac{b_i}{a_0}\;\; (i=0,1,2) \\
a_0 \;&=\; \frac{2}{T_\mathrm{s}} + N, \qquad a_1 \;=\; N - \frac{2}{T_\mathrm{s}} \\
b_0 &= K_\mathrm{p}\,a_0 \;+\; \frac{K_\mathrm{i}T_\mathrm{s}}{2}\,a_0 \;+\; K_\mathrm{d}\,N\,\frac{2}{T_\mathrm{s}}, \\
b_1 &= K_\mathrm{p}\,(-a_0+a_1) \;+\; \frac{K_\mathrm{i}T_\mathrm{s}}{2}\,(a_0+a_1) \;-\; 2\,K_\mathrm{d}\,N\,\frac{2}{T_\mathrm{s}}, \\
b_2 &= -K_\mathrm{p}\,a_1 \;+\; \frac{K_\mathrm{i}T_\mathrm{s}}{2}\,a_1 \;+\; K_\mathrm{d}\,N\,\frac{2}{T_\mathrm{s}}.
\end{aligned} \tag{4.43}$$

For embedded implementation in the C programming language, the same controller is conveniently realised as a set of finite-difference recursive equations:

$$\begin{aligned} I[k] &= I[k-1] + \frac{K_\mathrm{i}\, T_\mathrm{s}}{2}\Big(e[k] + e[k-1]\Big), \\ D[k] &= \alpha\, D[k-1] + \beta\Big(e[k] - e[k-1]\Big), \\ \psi[k] &= K_\mathrm{p}\, e[k] + I[k] + D[k], \end{aligned} \tag{4.44}$$

where $I[k]$ and $D[k]$ are the integral and derivative terms, respectively, and

$$\alpha \;=\; \frac{1 - \frac{NT_\mathrm{s}}{2}}{1 + \frac{NT_\mathrm{s}}{2}}, \qquad \beta \;=\; \frac{K_\mathrm{d}\, N}{1 + \frac{NT_\mathrm{s}}{2}}. \tag{4.45}$$

To ensure safe operation, the controller output is saturated within predefined limits $[\psi_\mathrm{min}, \psi_\mathrm{max}]$, so that

$$\psi_{sat}[k] = \min\{\max\{\psi[k], \psi_\mathrm{min}\},\, \psi_\mathrm{max}\} \tag{4.46}$$

A clamping protection mechanism is also implemented against integrator *wind-up*, based on conditional integration. If the saturated output is at its upper bound and the error would push it further up (or at its lower bound and the error would push it further down), integration is temporarily paused to prevent wind-up. Integration resumes automatically once the output re-enters the unsaturated region:

$$I[k] \;=\; \begin{cases} I[k-1], & \text{if } \Big(\psi_\mathrm{sat}[k] = \psi_\mathrm{max} \;\wedge\; e[k] > 0\Big) \;\vee\; \Big(\psi_\mathrm{sat}[k] = \psi_\mathrm{min} \;\wedge\; e[k] < 0\Big) \\ I[k-1] + \dfrac{K_\mathrm{i} T_\mathrm{s}}{2}\Big(e[k] + e[k-1]\Big), & \text{otherwise} \end{cases} . \tag{4.47}$$

4.4.2 PID Gain Tuning and Embedded Implementation

As mentioned earlier, having obtained a small-signal model of the plant via system identification, the PID tuning followed a model-based approach, enabling the use of automated tuning tools like Simulink Control Designer. Depending on the design domain, different design workflows are available [77]:

- **Continuous-time design**: if the controller is designed in the s-domain and then discretised;
- **Direct discrete-time design**: if the plant is discretised and the controller is tuned directly in the z-domain;

- **Mixed-domain design**: if the plant and the digital controller are kept respectively in s-domain and z-domain.

A digitally controlled power converter can be modelled as a sampled-data system: the plant evolves in continuous time, whereas sensing, computation, and actuation occur at discrete instants. SIMULINK natively supports simulation of hybrid (mixed-mode) and multi-rate models [78]. Beyond simulation, SIMULINK Control Design can *linearise* continuous-time, discrete-time, and multi-rate models – most commonly via block-by-block linearisation – thus enabling discrete PID tuning directly within hybrid models [79].

The PID Tuner in SIMULINK can then be used to interactively tune the *discrete* PID gains. The tool linearises the closed-loop model, computes an initial stabilising design, and provides interactive refinement of bandwidth and robustness/performance trade-offs [80].

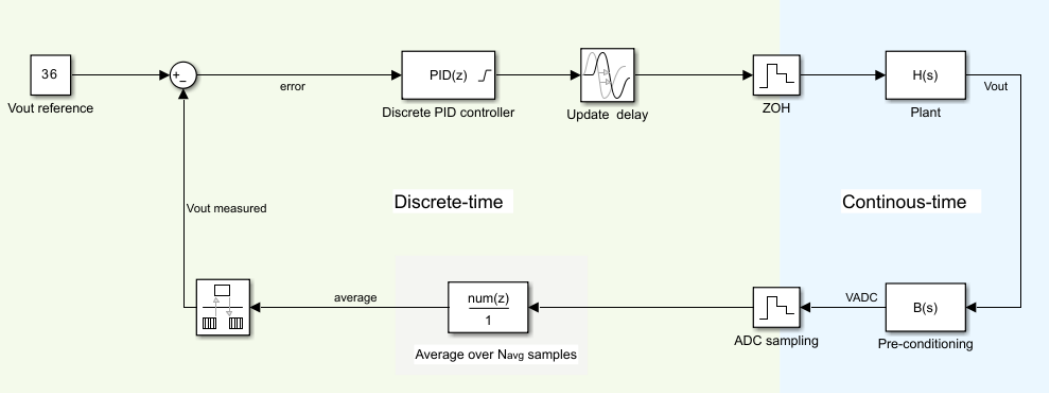


Figure 4.43: Mixed-domain model used for tuning and verification.

Figure 4.43 shows the block diagram used to tune the discrete PID controller in the SIMULINK model. At the interfaces between the continuous and discrete subsystems, explicit sampled-data blocks are used. On the *forward* path (controller → plant), a Zero-Order Hold (ZOH) converts the discrete controller output $\psi[k]$ into a continuous-time staircase by holding each sample over the interval between successive updates of the control variable. This update period is $T_\mathrm{s} = 1/f_\mathrm{ISR}$, where f_ISR is the frequency of the Interrupt Service Routine that computes the controller output on the embedded system. On the *feedback* path (plant → controller), a Sample-and-Hold (S&H) block represents ADC sampling of the measured voltage (after proper scaling and analog filtering), with sampling period $T_\mathrm{ADC} = 1/f_\mathrm{ADC}$. A *rate transition* block converts from the ADC rate f_ADC to the controller update rate f_ISR. A fixed *computation delay* on the forward path accounts for ISR execution latency.

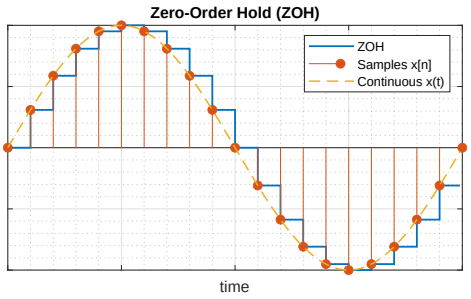


Figure 4.44: Zero-Order Hold

To attenuate high-frequency measurement noise, the sampled output is filtered by an N_{avg}-point moving average. The implementation sums the last N_{avg} samples and scales by $1/N_{\text{avg}}$; in the z-domain this is the length-N_{avg} boxcar FIR

$$M(z) \;=\; \frac{1}{N_{\text{avg}}} \sum_{i=0}^{N_{\text{avg}}-1} z^{-i} \;=\; \frac{1 - z^{-N_{\text{avg}}}}{N_{\text{avg}}\,(1 - z^{-1})}. \tag{4.48}$$

This filter has linear phase and an (approximately) constant group delay equal to half its window length, i.e.,

$$\tau_{\text{avg}} \;=\; \frac{N_{\text{avg}} - 1}{2}\,T_{\text{ADC}} \;\approx\; \frac{N_{\text{avg}}}{2}\,T_{\text{ADC}} \qquad (N_{\text{avg}} \gg 1). \tag{4.49}$$

Therefore, its dominant effect around crossover can be modelled as a pure time delay [81]. Accordingly, for loop-shaping and linearisation the averaging section was replaced with a delay block

$$e^{-s\,\tau_{\text{avg}}}, \qquad \tau_{\text{avg}} \;\approx\; \frac{N_{\text{avg}}}{2\,f_{\text{ADC}}}, \tag{4.50}$$

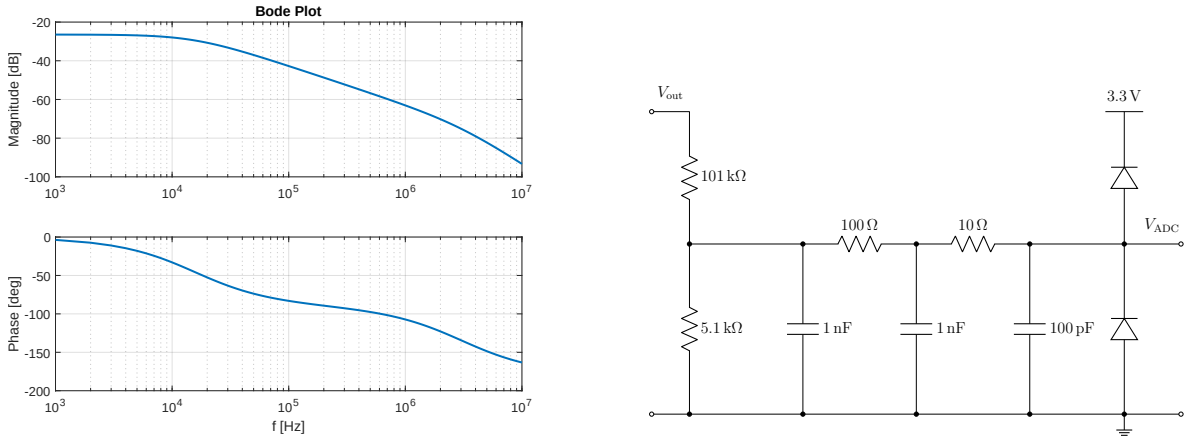
which preserves the phase lag contributed by the moving average at the relevant frequencies.

Pre-conditioning stage

A sensing/pre-conditioning stage $B(s)$ precedes the MCU ADC input on the feedback path. This stage consists of a voltage divider to scale the output voltage into the ADC input range (0-3.3 V), input protection against over-voltage at the ADC pin, and a low-pass filter to attenuate ripple and broadband noise.

The filtering proved critical in this prototype because the microcontroller board and the power stage reside on separate PCBs for ease of prototyping, testing, and debugging. The relatively long leads between the converter output and the ADC input increase susceptibility to high-frequency interference; the low-pass filter close to the ADC input mitigates this effect and preserves measurement fidelity.

Fig. 4.45 shows the Bode plot and the schematic of the filtering stage before the ADC input.



(a) Bode plot. (b) Schematic.

Figure 4.45: Bode plot and schematic of the pre-conditioning stage.

ISR Update Rate and Computational Latency

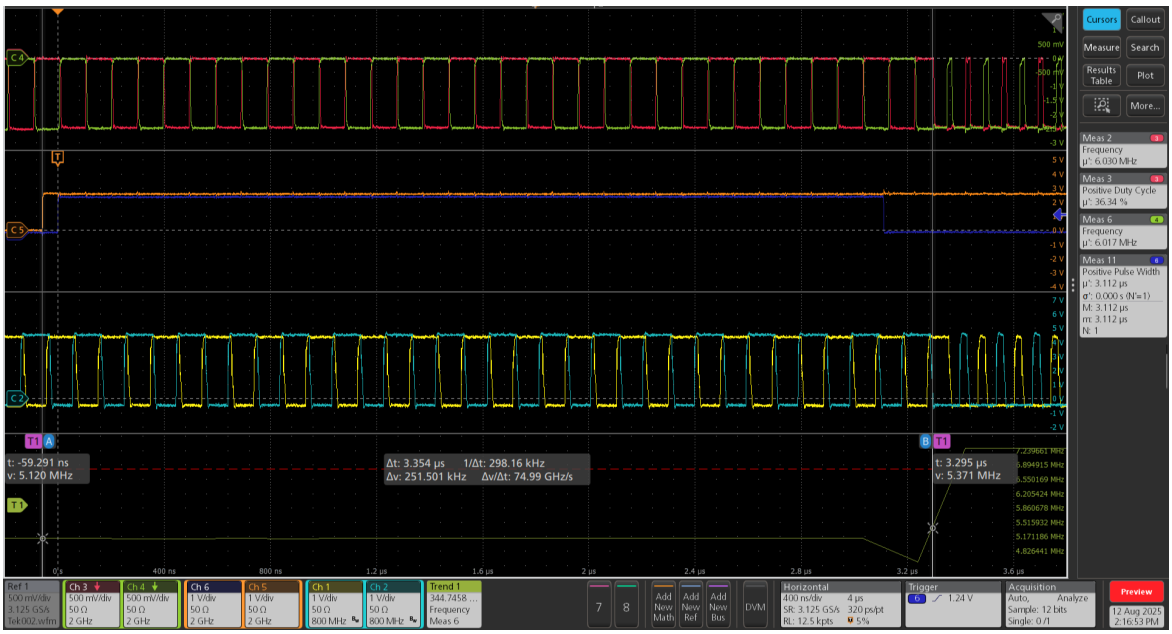


Figure 4.46: Oscilloscope capture showing the latency between ISR issuance and gate driver output update.

To quantify the end-to-end latency between control interrupt execution and actuation, two GPIO pins of the STM32 were configured as high-speed push-pull outputs and toggled by direct register writes to achieve deterministic timing. This approach ensures that the recorded transitions correspond precisely to specific points in the C code execution (e.g., interrupt request, start of computation, completion of the PWM

update sequence). Figure 4.46 shows the oscilloscope capture used to perform the measurement. The orange trace in the screenshot marks the issuance of the control ISR, while the blue trace goes high at the start of the computation and low when the PWM update sequence has completed.

In the same acquisition, the STM32 PWM outputs (green/red) and the gate-drivers outputs (yellow/blue) were captured, therefore the measured latency also includes the propagation through opto-isolators and gate drivers.

As indicated by the cursors in Fig. 4.46, the delay between the interrupt request and the observable change at the driver outputs is approximately 3.0-3.5 μs. When the control update requires stepped changes of both frequency and duty cycle (see Section 4.3.2), the total latency increases, as shown in Fig. 4.47.

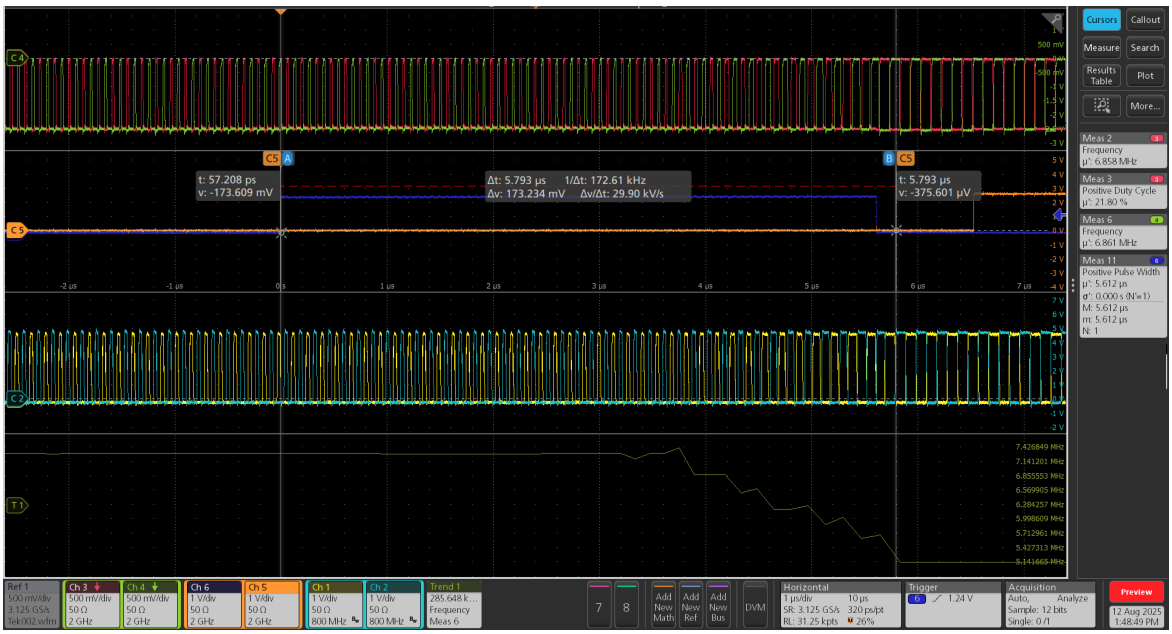


Figure 4.47: Measured ISR-to-actuation delay under a stepped update condition.

In order to avoid race conditions (i.e. a new interrupt being issued before the previous update has fully propagated to the hardware outputs), the ISR frequency – which defines the update rate of the system – was set to $f_{\mathrm{ISR}} = 80$ kHz. With this configuration, the measured latency represents only a fraction of the ISR period $T_{\mathrm{ISR}} = 12.5$ μs, ensuring that each update completes deterministically before the next interrupt is triggered.

In the block diagram of Fig. 4.43, the *Update Delay* block accounts for this latency.

Right-Half-Plane Zero and Bandwidth Limitation

As mentioned earlier in this chapter, the plant transfer function $H(s)$ exhibits a RHP zero at $f_{\mathrm{RHPZ}} \approx 45$ kHz. A RHP zero imposes a fundamental limit on the achievable crossover frequency f_{c} – the frequency at which the open-loop gain equals 0 dB – because it introduces an additional phase lag. To maintain sufficient phase margin and ensure closed-loop stability, the crossover frequency must therefore be kept safely below the RHP zero frequency. A widely adopted rule of thumb is to limit the crossover to approximately one-third to one-fifth of the RHP zero frequency [82]:

$$f_{\mathrm{c}} \lesssim \frac{1}{3\text{-}5} f_{\mathrm{RHPZ}} \tag{4.51}$$

which corresponds to a crossover frequency of approximately 8-15 kHz.

The selected interrupt rate of $f_{\mathrm{ISR}} = 80$ kHz not only ensures that each update is completed before the next interrupt, but also provides a high enough sampling ratio. Indeed, the interrupt rate f_{ISR} defines the effective sampling frequency f_{s} of the system, since each interrupt cycle involves computing the average of N_{avg} ADC samples of the output voltage, executing the control algorithm, and updating the PWM outputs. The sampling frequency therefore sets the temporal resolution at which the controller can observe and react to changes in the plant.

A well-established guideline in sampled-data control design is to maintain the sampling rate at least 7-10 times higher than the achievable open-loop crossover frequency f_{c} [77]. If the sampling frequency is too low, the discrete-time controller no longer behaves as its continuous-time counterpart, and additional phase lag from sampling and zero-order-hold effects can significantly reduce the phase margin. With $f_{\mathrm{ISR}} = f_{\mathrm{s}} = 80$ kHz and an achievable crossover frequency of $f_{\mathrm{c}} = 8$-15 kHz, the present system satisfies this criterion.

The achievable bandwidth is primarily constrained by the RHP zero at $f_{\mathrm{RHPZ}} \approx 45$ kHz and by sampled-data latency associated with the 80 kHz. The conditioning filter is chosen for measurement integrity: since its cut-off frequency ($f_{\mathrm{c,LPF}} \approx 15.5$ kHz) lies in the same decade as the achievable crossover ($f_{\mathrm{c}} \approx 8$-15 kHz), it contributes additional phase lag at the crossover frequency and slightly reduces the attainable bandwidth, but it does not fundamentally set the limit; rather, it enforces the existing constraint while ensuring clean and low-noise measurement.

In a more integrated prototype, with the MCU placed on the same PCB as the power stage, using shorter interconnects and optimised return paths and ground planes, the

analog filter cutoff could be increased, where feasible given noise constraints, to approximately 5-10 f_c in order to reduce its phase contribution. Nonetheless, the maximum achievable bandwidth would still be bounded by the RHP zero and the inherent digital latencies.

Tuning results

Table 4.4 summarises the parameters used in the SIMULINK model to tune the discrete PID controller via the PID Tuner Application, as well as the resulting gains obtained from the tuning process. As previously mentioned, the PID Tuner provides an initial set of gains that ensures closed-loop stability, while additional refinements were performed using the interactive interface.

Table 4.4: Parameters of the implemented digital control.

Parameter	Description	Value
f_{ADC}	ADC frequency	6 MHz
f_{ISR}	ISR frequency	80 kHz
N_{avg}	Averaged samples	32
K_{p}	Proportional gain	0.0558
K_{i}	Integral gain	2464.7
K_{d}	Derivative gain	962×10^{-9}
N	Derivative filter coefficient	19 145

The tuning of the PID controller was performed in SIMULINK by assembling the complete closed-loop system shown in Fig. 4.43. For linearisation purposes, the averaging of N_{avg} samples of the output voltage was replaced by a pure delay, as discussed earlier in this section. A step input was applied to the reference node, and the controller parameters were adjusted interactively to ensure that the output accurately tracked the reference while minimising overshoot and settling time.

To assess the stability margins, the frequency response of the loop gain, comprising the forward and feedback paths, was obtained from the SIMULINK model and is shown in Fig. 4.49. From the plot, the crossover frequency is identified at $f_c \approx 9$ kHz, where the magnitude crosses 0 dB. At this frequency, the phase margin is approximately $\mathrm{PM} = 68°$, while the gain margin, measured at the frequency where the phase crosses $-180°$, is GM = 6.2 dB. These margins confirm the closed-loop stability of the implemented control system.

To validate the performance of the designed discrete PID controller, a load-transient simulation was carried out using the complete converter model, including the tuned

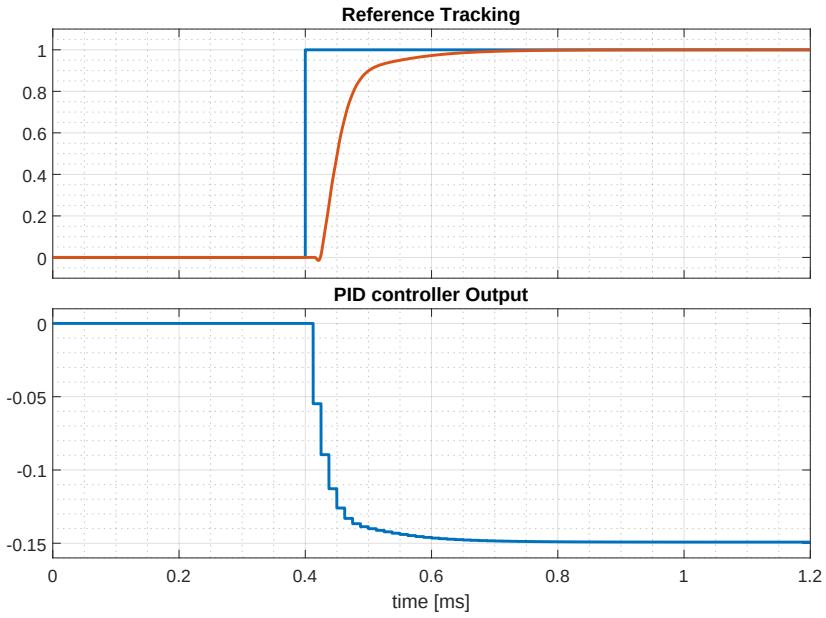


Figure 4.48: Simulated closed-loop response of the system to a reference step, obtained through closed-loop step-response tuning in SIMULINK.

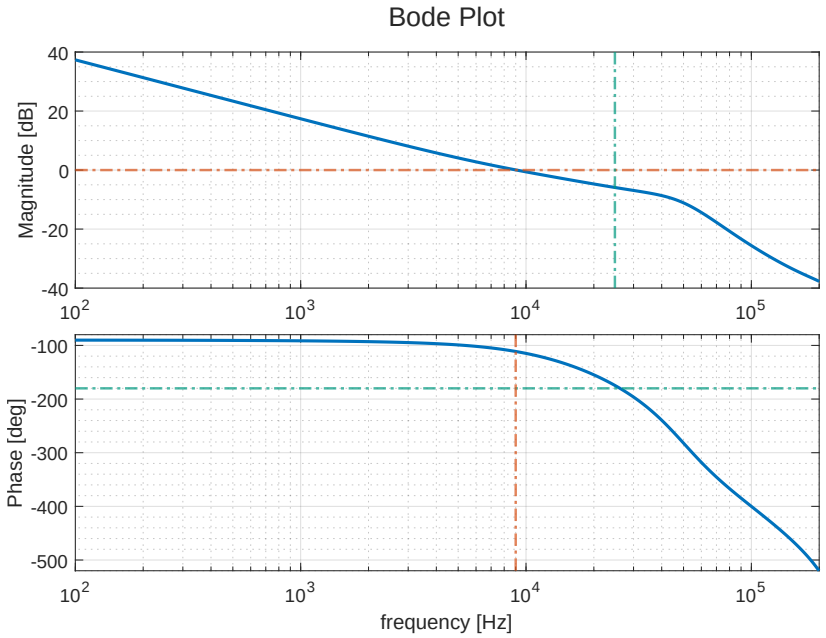


Figure 4.49: Bode plot of the loop transfer function showing stability margins.

digital control loop. A step in load current was applied from full load ($I_{\text{out}} = 7$ A) to half load ($I_{\text{out}} = 3.5$ A), with a controlled slew rate of 10 A/ms, representative of a fast transient condition within the controller's dynamic capability. This test evaluates the controller's ability to maintain output voltage regulation under large and rapid load disturbances. The resulting waveforms, shown in Fig. 4.50, illustrate the output voltage, load current, and switching frequency during the transient event. During the

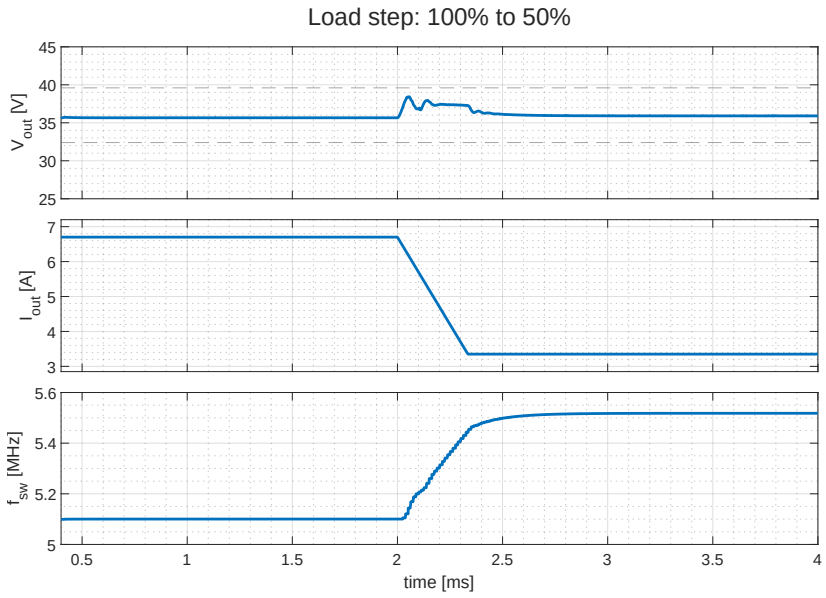


Figure 4.50: Simulated full-load to half-load transient with a slew rate of 10 A/ms, showing output voltage (V_{out}), load current (I_{out}), and switching frequency (f_{sw}).

load step, the output voltage exhibits a maximum overshoot of approximately 8%, settling back to its nominal value within 0.5 ms.

4.5 Duty-frequency relationship for ZVS operation

As mentioned, the inverter duty cycle D_{inv} is not a control variable for output-voltage regulation; instead, it is used to preserve zero-voltage switching (ZVS), thereby minimising switching losses. For each operating frequency f computed by the PID controller, a specific duty ratio is required to maintain ZVS. To achieve this in practice, a duty-frequency mapping was numerically extracted and then implemented in the microcontroller as a lookup table. The following subsection describes the procedure used to compute the relationship $D_{\text{inv}}(f)$.

The purpose of this analysis is to compute the push-pull Class E inverter duty cycle $D_{\text{inv}}(f, R_L)$ as a function of the operating frequency and load, and to identify the combinations that yield the desired output voltage V_{out}.

For ease of reading, the relevant equations are repeated here for convenience. The reflected impedance $\overline{Z}_{\text{eq}}(f, R_L)$ as seen from the primary side of the transformer is evaluated using (2.12)-(2.13) where the rectifier input impedance $\overline{Z}\text{in}_{\text{rect}} = R_{\text{in}_{\text{rect}}} + jX_{\text{in}_{\text{rect}}}$ is given by (3.9)-(3.10):

$$R_{\text{in}_{\text{rect}}} = 8R_L \, \sin^2(\phi_{\text{rect}})$$

$$\begin{aligned} X_{\text{in}_{\text{rect}}} = -\frac{1}{\pi^2 f \omega C_r} \Big(& \pi(1 - D_{\text{rect}}) + \sin(2\pi D_{\text{rect}}) - \frac{1}{4}\cos(2\phi_{\text{rect}})\sin(4\pi D_{\text{rect}}) \\ & - \frac{1}{2}\sin(2\phi_{\text{rect}})\sin^2(2\pi D_{\text{rect}}) \\ & - 2\pi(1 - D_{\text{rect}})\sin(\phi_{\text{rect}})\sin(2\pi D_{\text{rect}} - \phi_{\text{rect}}) \Big). \end{aligned} \tag{4.52}$$

In the above, the rectifier diodes' duty cycle $D_{\text{rect}}(f, R_L)$ can be computed numerically from [15, 22, 25]

$$1 - 2\pi^2(1 - D_{\text{rect}})^2 - \cos(2\pi D_{\text{rect}}) + \frac{(2\pi(1 - D_{\text{rect}}) + \sin(2\pi D_{\text{rect}}))^2}{1 - \cos(2\pi D_{\text{rect}})} = 4\pi \, f^2 \, R_L \, C_r \tag{4.53}$$

The rectifier input current phase angle $\phi_{\text{rect}}(f, R_L)$ is given by (3.6).

For a given $\overline{Z}_{\text{eq}}(f, R_L)$, the inverter duty cycle $D_{\text{inv}}(f, R_L)$ is computed solving the following:

$$\left((2\pi f)^2 \, L_{\text{eq}} - \frac{1}{C_{s_1}}\right) C_p = \frac{2(1 - D_{\text{inv}})^2\pi^2 - 1 + 2\cos(\phi_{\text{inv}})\cos(2\pi D_{\text{inv}} + \phi_{\text{inv}})}{\pi^2(1 - D_{\text{inv}})} \tag{4.54}$$

$$- \frac{\cos\Big(2(\pi D_{\text{inv}} + \phi_{\text{inv}})\Big)\Big(\cos(2\pi D_{\text{inv}})\Big)}{\pi^2(1 - D_{\text{inv}})} \tag{4.55}$$

$$+ \frac{\cos\Big(2(\pi D_{\text{inv}} + \phi_{\text{inv}})\Big)\Big(\pi(1 - D_{\text{inv}})\sin(2\pi D_{\text{inv}})\Big)}{\pi^2(1 - D_{\text{inv}})}. \tag{4.56}$$

where

$$\phi_{\text{inv}}(f, R_L) = \pi + \tan^{-1}\left(\frac{\cos(2\pi D_{\text{inv}}(f, R_L)) - 1}{2\pi(1 - D_{\text{inv}}(f, R_L)) + \sin(2\pi D_{\text{inv}}(f, R_L))}\right). \tag{4.57}$$

Figure 4.51 shows the inverter duty cycle required to maintain soft-switching as a function of the dc load R_L and operating frequency f. The dark region denotes operating points for which (4.56) admits no physically valid solution (e.g., $D_{\text{inv}} \notin (0, 1)$); in these conditions, ZVS is lost. The output voltage $V_{\text{out}}(f, R_L)$ is then evaluated for each operating point using

$$V_{\text{out}}(f, R_L) = 2 \, I_m \, G_i \, R_L \, \sin(\phi_{\text{rect}}), \tag{4.58}$$

where $I_m(f, R_L)$ is the amplitude of the inverter output current, expressed as [15, 42]:

$$I_m(f, R_L) = \sqrt{\frac{\sin^2(\pi D_{\text{inv}}) \, \sin^2(\pi D_{\text{inv}} + \phi_{\text{inv}}) \, V_{\text{in}}^2}{\pi^2 \, (1 - D_{\text{inv}})^2 \, R_{\text{eq}}^2}}, \tag{4.59}$$

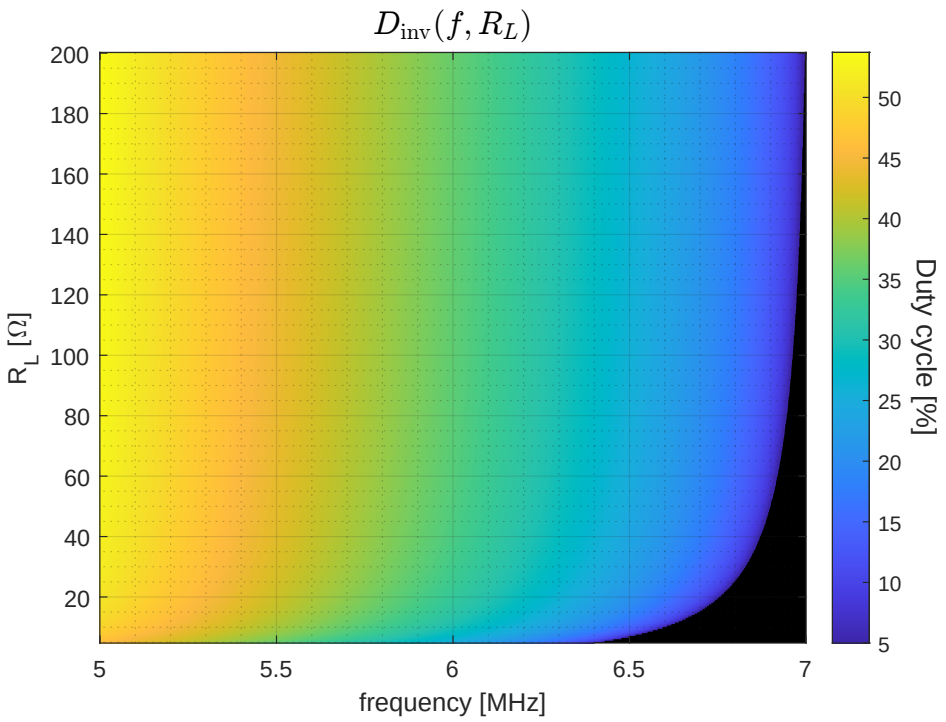


Figure 4.51: Duty cycle of the inverter as a function of dc load R_L and frequency f. The black region indicates operating conditions for which (4.56) has no valid solution, i.e., ZVS cannot be maintained.

and $G_i(f, R_L)$ is the link current gain:

$$G_i(f, R_L) = \left| \frac{jX_M}{jX_{L_{s_2}} + jX_{C_{s_2}} + \overline{Z}_{\text{rect}}} \right|. \tag{4.60}$$

In the previous expressions, ϕ_{rect}, D_{inv}, ϕ_{inv}, R_{eq}, and $\overline{Z}_{\text{rect}}$ are all functions of both f and R_L.

Figure 4.52 illustrates the relationship among the inverter duty cycle D_{inv}, operating frequency f, and dc load R_L. The output voltage V_{out} produced by each (D_{inv}, f, R_L) combination is encoded by the colour scale. Higher V_{out} values occur at larger duty cycles and lower switching frequencies, whereas the duty required to maintain soft switching decreases as the frequency increases.

All combinations of (f, R_L) that satisfy $V_{\text{out}} = V_{\text{out}}^*$ are then isolated to obtain the duty cycle that theoretically maintains ZVS for any given frequency in the range of interest. Figure 4.53 reports the resulting inverter duty cycle $D_{\text{inv}}(f)$ for a target output voltage of 36 V.

In the experimental implementation, the resulting relationship $D_{\text{inv}}(f)$ was stored in the microcontroller as a lookup table. During operation, the PID controller adjusted the switching frequency to regulate the output voltage, while the duty cycle was dynamically updated from the precomputed table corresponding to the current frequency.

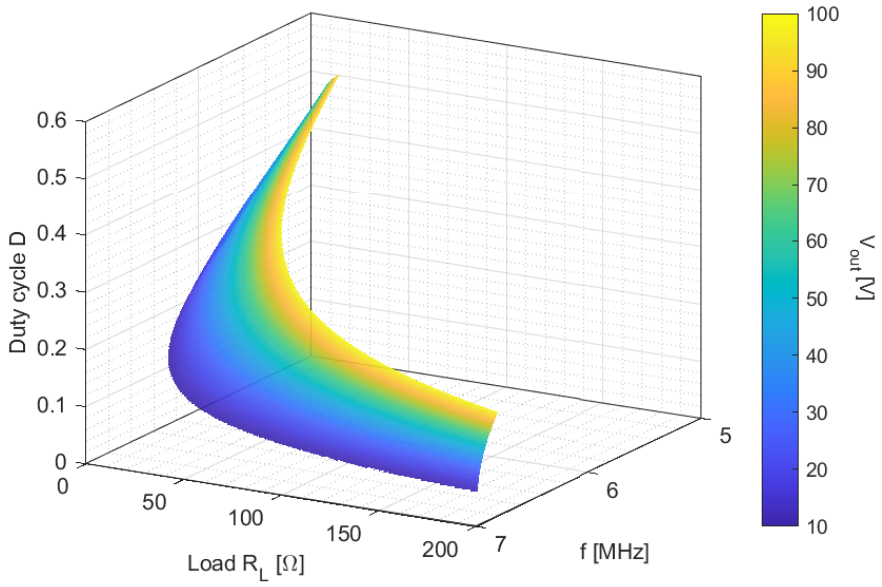


Figure 4.52: 3D surface of D_{inv} versus f and R_L, with color indicating V_{out}; higher voltages correspond to larger duty cycles and lower frequencies, while the duty that preserves soft switching diminishes with increasing frequency.

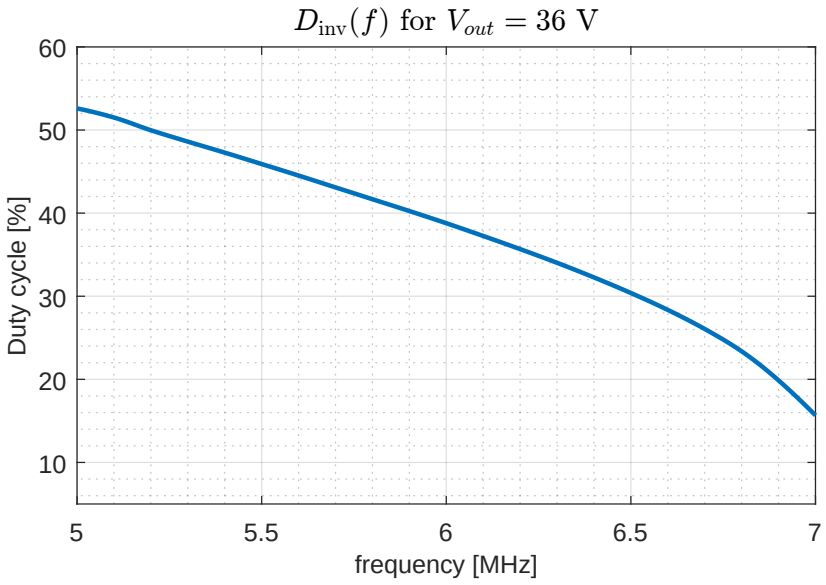


Figure 4.53: Duty cycle as a function of the operating frequency for a desired output voltage $V_{\text{out}}^{*} = 36\,\text{V}$.

It is noted that the resulting $D_{\text{inv}}(f)$ follows from a fundamental frequency approximation and thus serves as a *baseline* setting. In hardware, $D_{\text{inv}}(f)$ may be slightly trimmed to avoid unintended reverse conduction.

4.6 Experimental results

Figure 4.54 presents an oscilloscope screen capture of the load-transient test performed on the prototype hardware. The load current was stepped from full load ($I_{\text{out}} \simeq 7$ A) to approximately 30% load ($I_{\text{out}} \simeq 2$ A) with a controlled slew rate of 1 A/μs, corresponding to an extremely fast disturbance that exceeds the control loop bandwidth by more than one order of magnitude.

The measured waveforms include the output voltage V_{out} (pink), the filtered ADC voltage $V_{\text{out,ADC}}$ (green), the PWM sampling signal (blue), and the corresponding switching frequency (light green) and duty cycle (red) during the transient. As observed, the controller successfully restores the output voltage to its nominal value of 36 V within a few hundred microseconds. During the load release, the output voltage temporarily rises to a peak of approximately 50 V, corresponding to an overshoot of about 38%. This behaviour is consistent with the expected response of the converter when the load current changes faster than the controller can react.

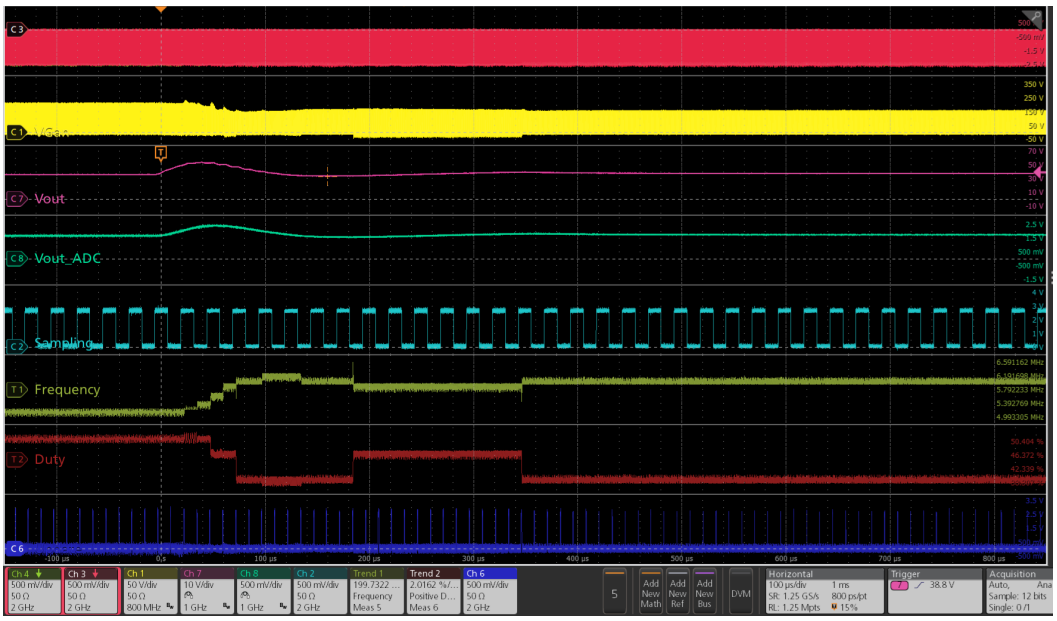


Figure 4.54: Measured full-to-partial-load transient response of the prototype converter. The HF yellow waveform is the drain voltage of one of the GaN devices, the magenta one is the PWM output of the MCU and the light-blue one is the sampling rate of the discrete controller.

Besides providing output-voltage regulation, closed-loop operation also maintains high efficiency over a wide range of load conditions. In open-loop operation, the switching frequency is fixed, resulting in suboptimal behaviour for load levels that deviate from the optimal one for that specific frequency. As a consequence, soft-switching is progressively lost, leading to increased switching losses in the GaN devices and a

corresponding drop in overall efficiency. In some operating conditions, the increase in switching losses can become so severe that operation at that particular load level and switching frequency is no longer feasible, as it could lead to device failure due to excessive power dissipation. Closed-loop operation ensures efficient and safe performance across the entire load range by adapting the switching frequency and duty cycle to preserve ZVS in each load condition.

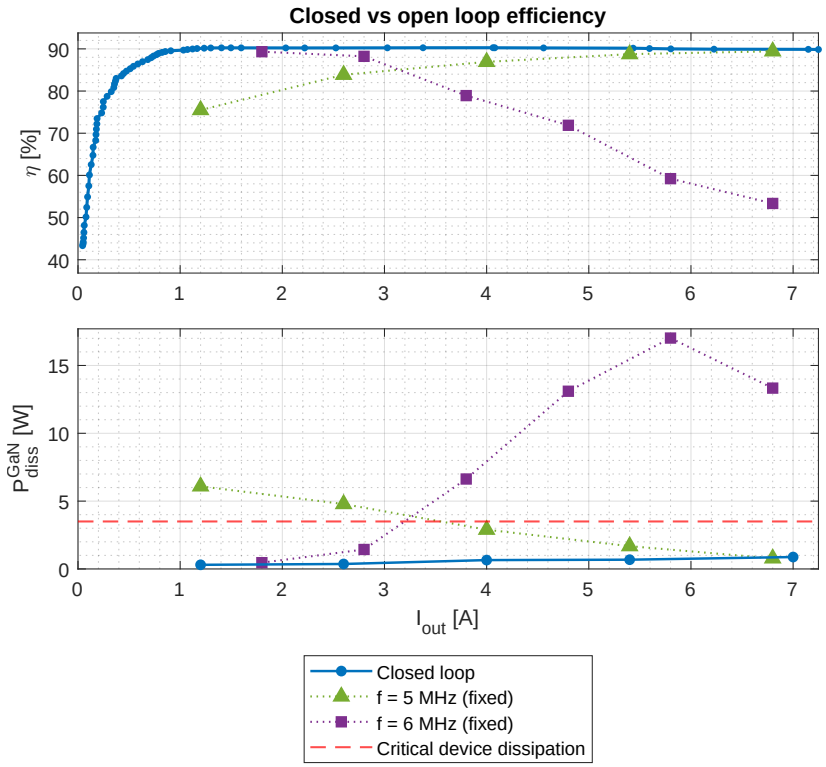


Figure 4.55: Comparison between closed-loop and open-loop operation. **Top:** Converter efficiency as a function of output current for closed-loop operation (measured) and open-loop operation at fixed switching frequencies (simulated). **Bottom:** Simulated GaN device power dissipation as a function of load current for closed-loop and open-loop operation.

Figure 4.55 compares, in the top plot, the measured efficiency of the prototype operating in closed-loop mode with the open-loop efficiency obtained from simulation at two fixed switching frequencies, as a function of the output current. As can be seen, the closed-loop efficiency remains close to 90% across the entire load range and starts to decrease only when the output power falls below approximately 40 W. In contrast, the two open-loop efficiency curves corresponding to fixed switching frequencies show high efficiency only around their respective optimal load currents, while efficiency drops significantly as the load deviates from that point.

The bottom plot of the same figure shows the simulated GaN device power dissipation for closed-loop and open-loop operation. In closed-loop mode, the device dissipation

remains well within the safe operating margin (indicated by the dashed red line), whereas in the fixed-frequency cases, dissipation can reach critical levels that may lead to excessive device stress or even failure.

Figures 4.56-4.57 show two simulated cases of load-step transitions performed at fixed switching frequency. In the first case, the load current is stepped from full load ($I_{\text{out}} = 7$ A) to 30% load while operating at $f_{\text{sw}} = 5$ MHz, corresponding to the frequency that maintains $V_{\text{out}} = 36$ V at full load. In the second case, the load is stepped back from 30% to full load at a fixed frequency of $f_{\text{sw}} = 6$ MHz, which maintains the nominal output voltage at 30% load.

After the load step, in both scenarios the converter loses zero-voltage-switching (ZVS) at steady state, and the GaN device power dissipation increases sharply, reaching critical levels. The simulated device power losses are approximately 5 W in the first case and exceed 10 W in the second, whereas under closed-loop operation they remain below 2 W. With closed-loop control (see Fig. 4.54), the same load-step transitions occur without excessive dissipation, ensuring stable, regulated, and safe operation of the converter.

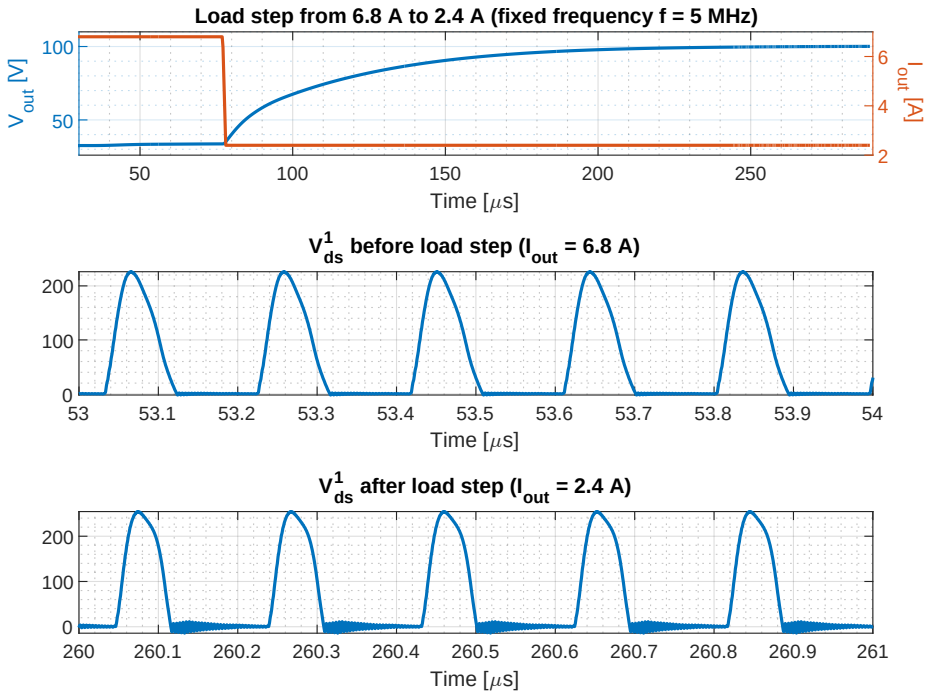


Figure 4.56: Load step change from full load to about 30% at a fixed frequency of 5MHz. The figure shows the output current and voltage during the load step and the device drain voltage before and after the step at regime.

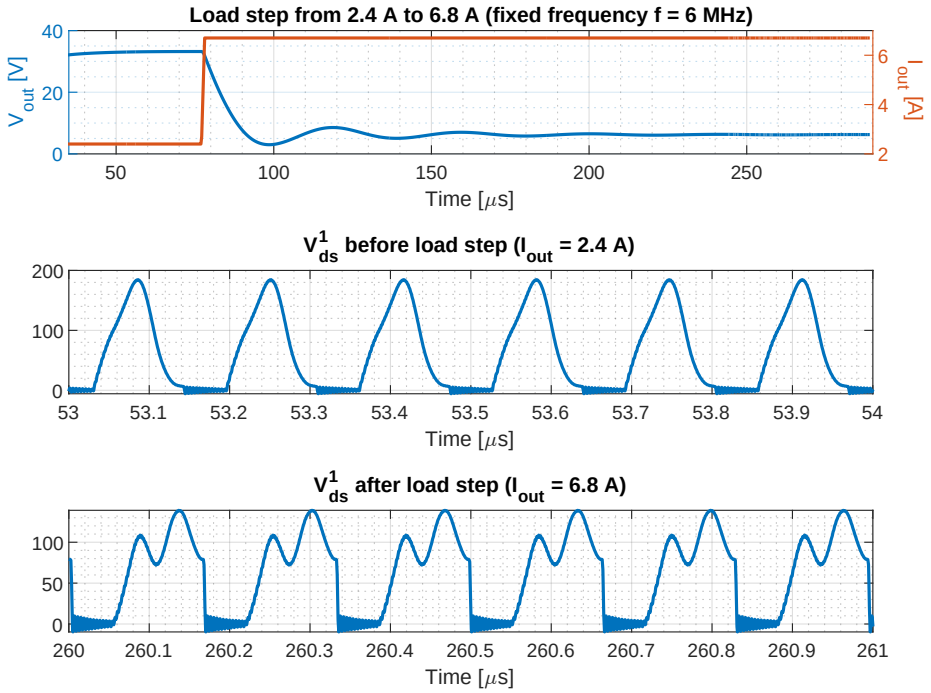


Figure 4.57: Load step change from about 30% to full load at a fixed frequency of 6MHz. The figure shows the output current and voltage during the load step and the device drain voltage before and after the step at regime.

4.7 Finite chokes case

In PWM converters, such as the boost and boost-derived families, the physical explanation for the presence of right-half-plane zeros in the transfer function is related to the energy-flow effect: after a small increase in duty ratio, the inductor current rises (longer on-time), but the output is fed for a shorter interval (shorter off-time), so the instantaneous power delivered to the load initially *decreases* before recovering. This inverse initial response produces a non-minimum-phase zero [12, 82–84], whose frequency depends on operating point and the relevant inductance values [12,82,84,85].

The dc-dc converter implemented here is not PWM-modulated; therefore the same mechanism cannot be assumed *a priori*. Nevertheless, the PWM case emphasises the role of inductors acting as quasi current sources over the control band, which motivated an investigation into whether the *choke inductors* (input and/or output) of a Class E-based dc-dc could similarly govern the presence or absence of non-minimum-phase behaviour.

In the classical formulation, Class E inverters and rectifiers employ ideal ("infinite") choke inductors, i.e., inductors large enough at the operating frequency that their current can be treated as essentially constant. By contrast, finite-choke variants (with finite L_{rfc}) intentionally make the feed inductance resonate with the shunt capacitances to maintain soft switching while enabling smaller, less bulky magnetics at MHz frequencies. The main trade-offs are higher feed-path RMS currents and increased device voltage stress, which must be accommodated in the design [86–89].

To assess how the RHP zero relates to the input/output inductances, four designs were implemented in simulation:

1. *infinite input / infinite output*
2. *infinite input / finite output*
3. *finite input / infinite output*
4. *finite input / finite output*

Starting from the design of case (1), the other cases were tuned by making the relevant inductors finite and then iteratively retuning the shunt capacitances to recover a common operating point across all circuits – namely, the same input and output power, the same output voltage, and closely matched drain-voltage waveforms.

Table 4.5 lists the component values for each design, and Fig. 4.58 shows the steady-

Table 4.5: Values of components in the four cases: infinite chokes, finite output chokes, finite input chokes, finite chokes

Parameter	Infinite chokes	Finite output chokes	Finite input chokes	Finite chokes
L_{in}	84 µH	84 µH	1.62 µH	1.62 µH
C_p	666 pF	666 pF	1.045 nF	1.061 nF
C_{s_1}	740 pF	740 pF	740 pF	740 pF
L_{s_1}	1.57 µH	1.57 µH	1.57 µH	1.57 µH
L_{s_2}	490 nH	490 nH	490 nH	490 nH
k	0.83	0.83	0.83	0.83
C_{s_2}	1.54 nF	1.54 nF	1.54 nF	1.54 nF
C_r	1.05 nF	1.77 nF	1.09 nF	1.77 nF
L_{o}	54 µH	1.08 µH	54 µH	1.08 µH

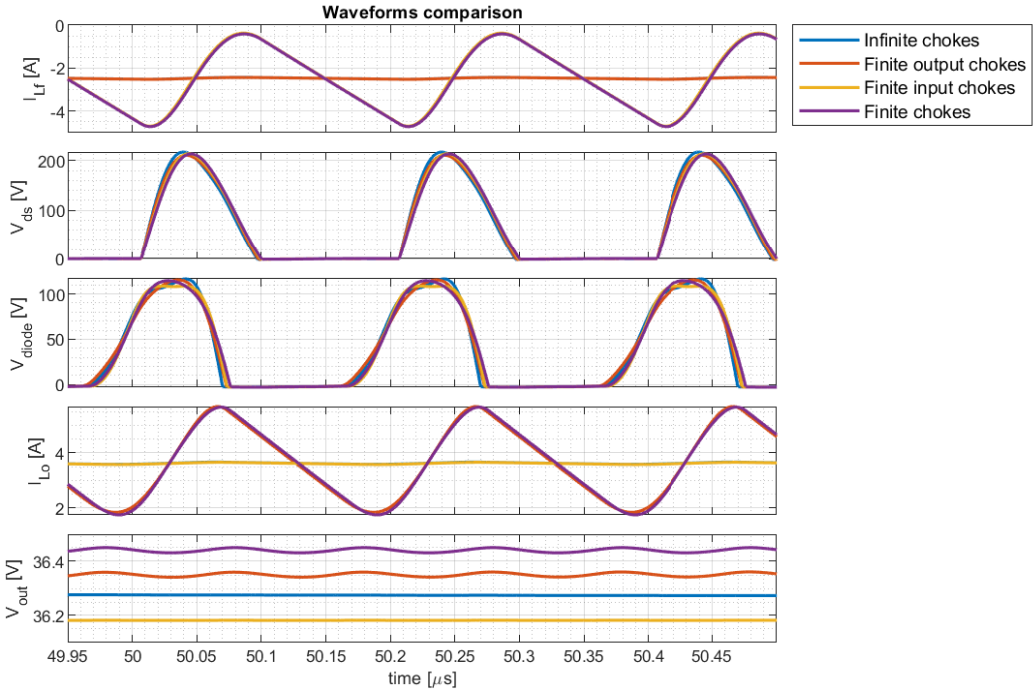


Figure 4.58: Steady-state waveforms for the four designs.

state waveforms for all four designs. As intended, the output voltage and drain-voltage waveforms are approximately identical in all designs, whereas the input and output currents exhibit behaviour consistent with the choke realisation (nearly constant with large/infinite inductance, and with pronounced ripple when the inductance is finite).

The procedure described in Sec. 4.2 was used to extract the control-to-output transfer functions in the four cases. Identical operating conditions were enforced for all four designs, and the same small frequency step was applied to obtain the responses. Figure 4.59 shows the output-voltage transient following the frequency perturbation. A difference is already evident in the time domain: the designs with a *finite input*

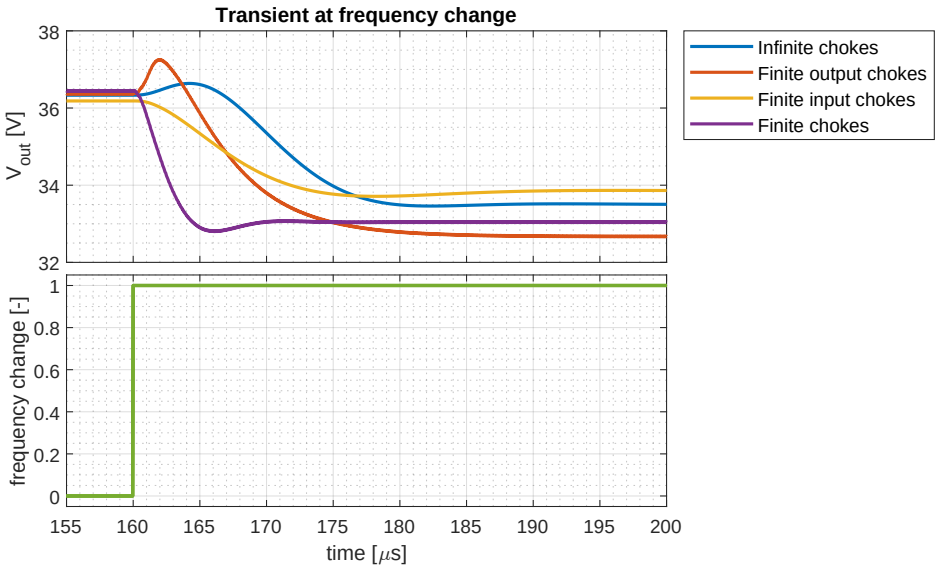


Figure 4.59: Transient response when a frequency step change is applied in the four cases.

inductance do not exhibit the initial inverse response characteristic of right-half-plane zeros, whereas the designs with an *infinite input* choke do.

The Bode plots of the extracted and fitted control-to-output transfer functions for the four cases are shown in Fig. 4.60. The responses with a *finite input* inductance (yellow

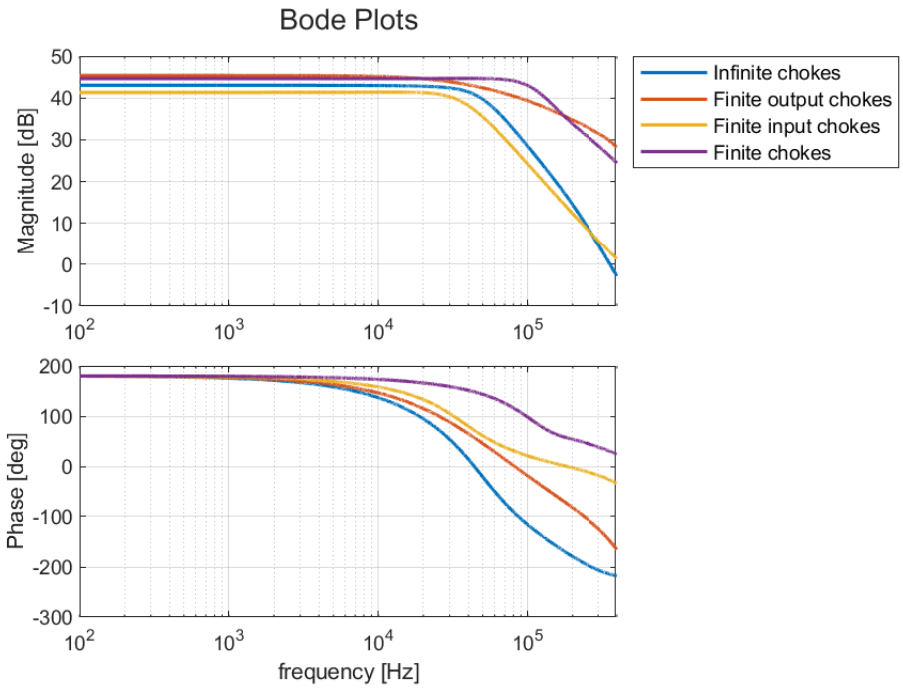


Figure 4.60: Fitted Bode plots of the control-to-output transfer function for the four input/output inductance realisations.

and purple) exhibit noticeably less phase lag than their infinite-input counterparts

(blue and orange). This behaviour is consistent with the absence of a right-half-plane zero over the measured band for the finite-input cases, whereas the infinite-input cases show the additional phase delay and high-frequency magnitude behaviour characteristic of a non-minimum-phase zero.

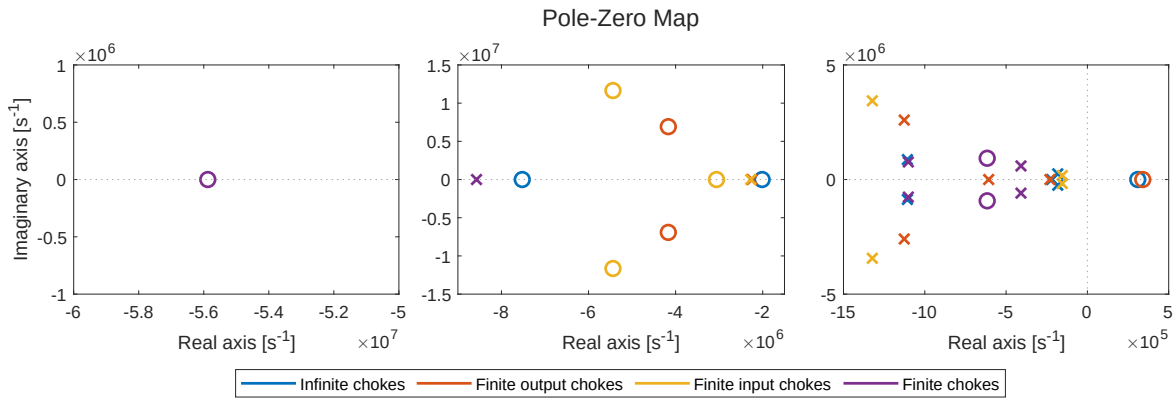


Figure 4.61: Pole-zero maps of the fitted control-to-output models for the four choke realisations.

Figure 4.61 summarises the identified pole-zero locations of the control-to-output models for the four choke implementations. The circles denote the zeros while the crosses the poles. For readability, the real axis is split into three panels with different ranges. The maps corroborate the time- and frequency-domain evidence, as the designs with a *finite input* inductor (yellow, purple) have all zeros in the left half-plane and thus are minimum-phase in the operating region.

This result seems to suggest that the RF-choke input inductance acting as a *stiff* current source is associated to the occurrence of RHP zeros.

The transfer function was evaluated for various designs by varying the *degree of finiteness* of the input choke L_{in}. The output choke L_o was maintained as infinite, as the preliminary results suggested the input choke might be primarily responsible for the RHP zero. As the input choke becomes increasingly finite, resulting in non-negligible input current ripple, the shunt capacitance C_p was adjusted to ensure the drain waveforms and output voltage remained consistent for all the designs. Table 4.6 shows the component values for the different design cases considered.

The steady-state operational waveforms for the various L_{in} design cases are illustrated in Figure 4.62, showing the input inductor current $I_{L_{in}}$, the GaNs drain-to-source voltage V_{ds}, and the primary and secondary transformer currents (I_{Ls1} and I_{Ls2}, respectively).

Figure 4.63 illustrates the output voltage step response for the different designs with

Table 4.6: Values of components in the different input choke designs cases.

Parameter	Case 1	Case 2	Case 3	Case 4	Case 5	Case 6	Case 7
L_{in}	81 µH	40.5 µH	16.2 µH	8.1 µH	2.27 µH	810 nH	405 nH
C_p	666 pF	666 pF	699 pF	726 pF	919 pF	1.34 nF	2.065 nF
C_{s_1}	740 pF	740 pF	740 pF	740 pF	740 pF	740 pF	740 pF
L_{s_1}	1.57 µH	1.57 µH	1.57 µH	1.57 µH	1.57 µH	1.57 µH	1.57 µH
L_{s_2}	490 nH	490 nH	490 nH	490 nH	490 nH	490 nH	490 nH
k	0.83	0.83	0.83	0.83	0.83	0.83	0.83
C_{s_2}	1.54 nF	1.54 nF	1.54 nF	1.54 nF	1.54 nF	1.54 nF	1.54 nF
C_r	1.05 nF	1.05 nF	1.05 nF	1.05 nF	1.05 nF	1.05 nF	1.05 nF
L_{o}	54 µH	54 µH	54 µH	54 µH	54 µH	54 µH	54 µH

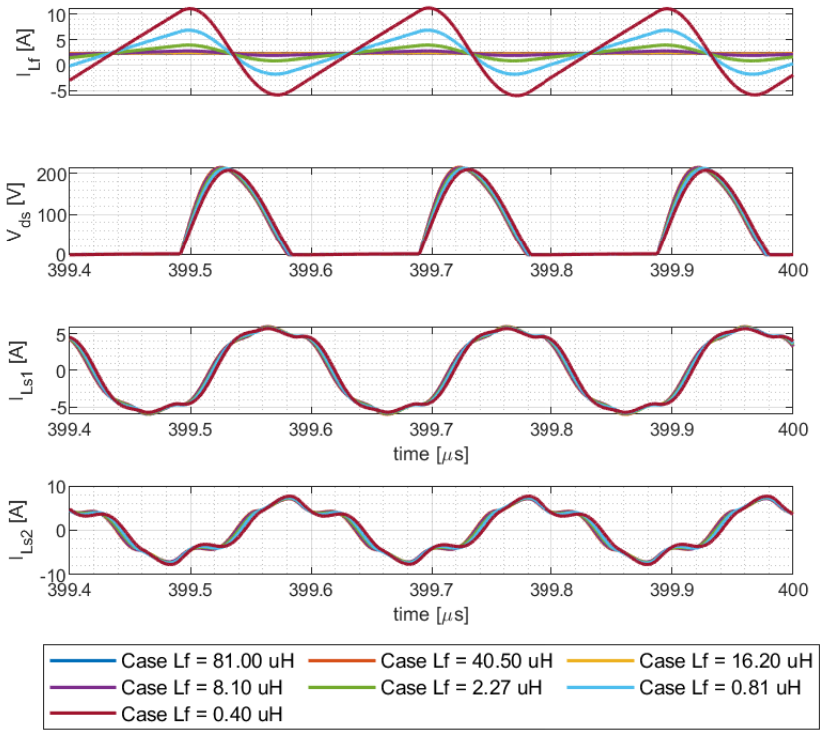


Figure 4.62: Steady-state converter waveforms across different L_{in} design cases. From top to bottom: input inductor current ($I_{L_{in}}$), GaN drain-to-source voltage (V_{ds}), and primary (I_{Ls1}) and secondary (I_{Ls2}) transformer currents. While the input choke finiteness significantly alters the $I_{L_{in}}$ ripple, the adjustment of C_p maintains consistent resonant tank behaviour and V_{ds}.

progressively more finite input inductance L_{in}. As can be qualitatively appreciated from the figure, as the input inductance progressively decreases from 81 µH to 400 nH, the inverse response typical of the presence of RHP zeros disappears.

To normalise the degree of finiteness across different input inductor designs, the input

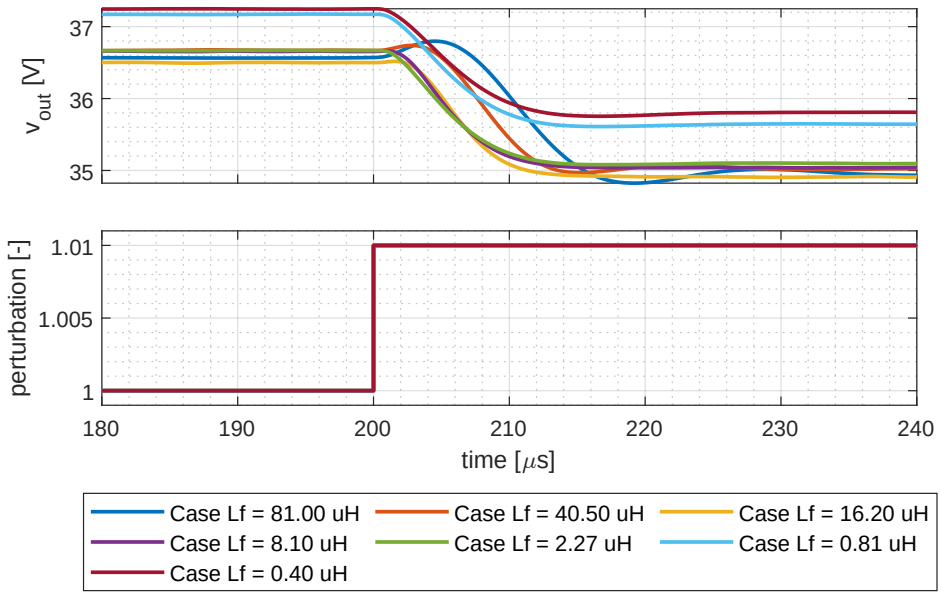


Figure 4.63: Output voltage transient response to the frequency step perturbation for the different input inductance L_{in} cases.

choke current ripple ratio r_L was employed as a dimensionless metric, defined as:

$$r_L(\%) = \frac{\Delta i_{L_{in}}}{I_{L_{in},avg}} \cdot 100 \tag{4.61}$$

where $I_{L_{in},avg}$ denotes the average inductor current and $\Delta i_{L_{in}}$ represents its peak-to-peak ripple.

From the extraction of the transfer function for all the different cases considered, it is found that the behaviour of the RHP zero exhibits two distinct phases, as illustrated in Fig. 4.64. For ripple ratios below 20% ($L_{in} \geq 16.20$ μH), the RHP zero is present and undergoes a frequency migration. Specifically, as the ripple increases, $f_{z,RHP}$ shifts from 45 kHz to approximately 200 kHz, suggesting that reduced inductance pushes the zero toward higher frequencies. When the ripple ratio exceeds 20%, the RHP zero disappears entirely for cases where $L_{in} \leq 8.10$ μH ($r_L \approx 35\%$), as shown in the lower pane of Fig. 4.64. In these high-ripple regimes, characterised by a higher degree of finiteness, the converter effectively becomes a minimum-phase system.

The numerical findings regarding the RHP zero dynamics are summarised in Table 4.7. This data illustrates the upward frequency migration of $f_{z,RHP}$ as the input inductance L_{in} is reduced, while utilising the ripple ratio r_L as a normalised metric to define the boundary where the non-minimum phase characteristic is effectively eliminated. The table also specifies whether the input choke current exhibits zero crossing within the switching cycle.

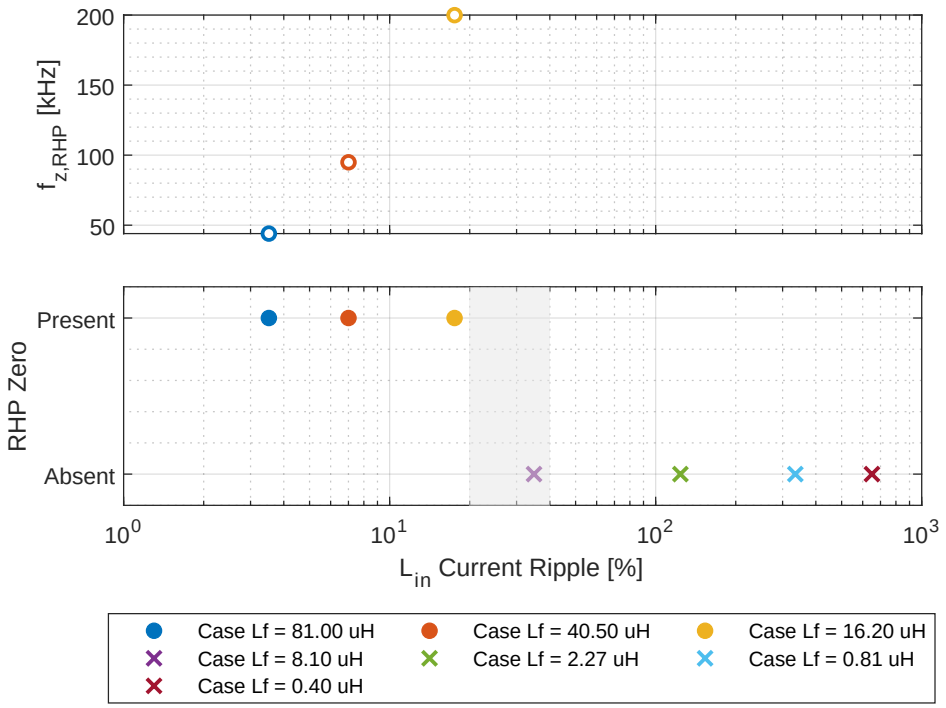


Figure 4.64: Analysis of RHP zero migration and existence as a function of the L_{in} current ripple ratio r_L. The top pane tracks the frequency of the RHP zero ($f_{z,RHP}$) when present, while the bottom pane indicates its existence. The shaded region denotes the transition zone ($20\% < r_L < 40\%$) where the system shifts from non-minimum phase to minimum-phase behaviour.

Table 4.7: Summary of RHP zero migration and existence relative to input choke finiteness.

Parameter	**Case 1**	**Case 2**	**Case 3**	**Case 4**	**Case 5**	**Case 6**	**Case 7**
L_{in} [μH]	81	40.5	16.2	8.1	2.27	0.81	0.4
r_L [%]	3.52	7.00	17.54	34.89	123.86	334.90	650.09
RHP Zero	Yes	Yes	Yes	No	No	No	No
$f_{z,RHP}$ [kHz]	44.00	94.89	199.9	–	–	–	–
$I_{L_{in}}$ zero crossing	No	No	No	No	No	Yes	Yes

Nonetheless, further investigation is required to elucidate the underlying mechanism and to quantify the specific role of the input choke.

In conclusion, while a finite input design trades off saturation margin and higher RMS currents in the feed path, it is advantageous from a control standpoint: the resulting control-to-output response does not exhibit a right-half-plane zero in the operating region considered, relaxing crossover-frequency limits and simplifying compensation.

4.8 Summary

In this chapter, a proportional-integral-derivative (PID) FM control algorithm was developed for a 5-7 MHz push-pull Class E^2 isolated dc-dc converter. A practical implementation framework was established that estimates the control-to-output transfer function $H(s)$ from time-domain step responses in simulation, enabling model-based controller tuning.

Implementation aspects were addressed, including safe frequency-change sequences to avoid imbalance between the two inverter devices and hardware constraints associated with the MHz-frequency PWM generation using the STM32 HRTIM peripheral.

A mapping between operating frequency and duty cycle required to achieve a target output voltage while maintaining soft switching (ZVS) was derived and deployed as a look-up table on the microcontroller to guarantee ZVS. The *Simulink*-based tuning workflow for the controller was also outlined.

Despite hardware limitations, the implemented controller successfully achieved regulation with output-voltage recovery in < 200 μs. The closed-loop control not only maintained a constant output voltage, but also high efficiency (about 90%) over a wide range of load conditions (from 260 W down to 35 W). It further enables operation in regions where open-loop control would fail due to increased device dissipation.

Finally, a qualitative analysis was presented to investigate the origin of the right-half-plane zero in the control-to-output transfer function $H(s)$ of the converter, which limits the maximum achievable bandwidth. The analysis suggested that adopting a finite input inductor design can eliminate this RHP zero and thereby enable a larger control bandwidth.

Chapter 5

Conclusions

5.1 Main achievements

This thesis advances isolated dc-dc conversion in the multi-MHz frequency range through experimentally validated hardware, modelling, and control results. The challenges and limitations of operating dc-dc converters at multi-MHz frequencies are examined and addressed.

An isolated Class EF_2 converter rated at 140 W and operating at 12 MHz with an air-core PCB transformer on commercial FR-4 is realised, achieving 80.8% peak efficiency. A predictive, parasitic-aware design workflow is established in which PCB layout parasitics are extracted via full-wave electromagnetic simulation and embedded in a lumped equivalent circuit model. The explicit inclusion of the parasitics enables accurate prediction of behaviour and mitigates post-fabrication retuning. The equivalent lumped model is validated against VNA S-parameter measurements across the relevant band, showing close agreement and correctly predicting performances.

An analytical first-harmonic-approximation model is developed to compute the dc-dc gain of the converter as a function of switching frequency, providing a foundation for frequency-modulation regulation under input-voltage and load variations and directly informing controller design.

Conducted at Imperial College London's Wireless Power Laboratory during a three-month visit, closed-loop controllability is demonstrated on a 5-7 MHz Class E^2 push-pull isolated converter using a general-purpose STM32 platform, with a reproducible workflow that combines system identification from simulated time-domain step responses and model-based tuning; the implemented controller maintains approximately

90% efficiency over a 260-35 W load range and achieves output-voltage recovery times below 200 μs, extending operation into regions where open-loop control would otherwise fail due to increased device dissipation. A qualitative analysis relates the right-half-plane zero in the control-to-output transfer function to the input inductance value and identifies a finite input-inductor design as a way to increase achievable bandwidth.

Collectively, the results indicate that, at multi-MHz, further performance gains are governed less by device technology changes and more by advances in magnetic materials (including the practicality of air-core implementations), board materials and stack-up, topology, and available digital-control resources; in particular, limitations of general-purpose microcontrollers (e.g., timer granularity, latency, and computational headroom) are documented alongside the proposed control workflow, delineating where higher-performance controllers would yield benefit. Dissemination includes the paper "*A Low-profile GaN-based Multi-MHz DC-DC Converter with an Air-Core PCB Transformer*" presented at the *IEEE Energy Conversion Congress & Exposition (ECCE) 2025* in Birmingham, UK, covering the air-core PCB transformer work; in addition, the closed-loop control results are being prepared for a journal publication, together with a journal extension of the air-core work.

5.2 Future work and research directions

Many developments naturally follow from the results obtained during the Ph.D. period. Selected improvements and next research goals are outlined below.

- **Publications.** A journal extension of the air-core PCB transformer work is in preparation, and a journal submission on the closed-loop control study is forthcoming.
- **Secondary-side rectification.** The loss budget shows that diode rectification on the secondary side contributes a significant fraction of the total losses in both implemented converters. Replacing diodes with synchronous rectification is expected to improve efficiency. Although this increases controller complexity and complicates practical implementation on a general-purpose microcontroller, it also introduces an additional control variable, i.e. the phase shift between primary and secondary-side devices, that can be exploited for regulation.
- **Transformer optimisation (air-core and ferrite).** Both the air-core and high-frequency ferrite designs can be further optimised. For the air-core PCB transformer, alternative geometries (e.g., tapered or multi-spiral layouts) and

board materials (low-loss dielectrics or the selective use of magnetic sheets) could be investigated to reduce ac resistance and leakage while maintaining isolation. For the ferrite design, circuit and magnetic parameters should be explored to lower peak flux density for a given output power without increasing core cross-section, overall dimensions, or turns count in order to minimise core and copper losses. *Ongoing work* evaluates alternative core materials suitable for multi-MHz operation to lower core loss and allow core size reduction at constant power.

- **Control architecture and plant design.** The controller performance for the push-pull Class E^2 dc-dc converter can be enhanced by optimising the pre-conditioning filter stage, adopting a faster microcontroller or dedicated digital logic, and moving to a finite input-inductance design as suggested by the qualitative analysis of the right-half-plane zero in the control-to-output transfer function. These steps are expected to extend bandwidth and improve the converter's transient response.
- **Power factor correction (PFC) integration.** Integrating PFC capability into Class E-based converters [90] without additional conversion stages appears to be a promising direction to further enhance power density. The push-pull Class E^2 stage could be preceded directly by a mains rectifier; the 50 Hz rectified input is quasi-constant over the much shorter period of the multi-MHz inverter. By adjusting the switching frequency, the input current can be shaped to be in phase with the input voltage and approximately sinusoidal. With active rectification, a multivariable control scheme – combining frequency and phase modulation – could simultaneously achieve output regulation and power factor correction without the need for an additional conversion stage.

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