ALMA MATER STUDIORUM
UNIVERSITÀ DI BOLOGNA

DOTTORATO DI RICERCA IN

INGEGNERIA BIOMEDICA, ELETTRICA E DEI SISTEMI

Ciclo 38

Settore Concorsuale: 09/E1 - ELETTROTECNICA

Settore Scientifico Disciplinare: ING-IND/31 - ELETTROTECNICA

ANALYSIS AND IMPROVEMENTS OF ISOLATED DC/DC CONVERTERS FOR DC MICROGRIDS

Presentata da: Lohith Kumar Pittala

Coordinatore Dottorato

Michele Monaci

Supervisore

Riccardo Mandrioli

Co-supervisore

Mattia Ricco

Esame finale anno 2026

Preface

This thesis represents the outcome of a journey that began during my Master's studies at the University of Bologna, where I carried out my thesis research under the supervision of Prof. Mattia Ricco and the co-supervision of Prof. Riccardo Mandrioli. Following this experience, I joined the Power Electronic Circuits and Photovoltaics group as a research assistant, which marked the first step toward a more sustained research activity in the field of power electronics. This eventually led me to begin my doctoral studies within the PhD Programme in Biomedical, Electrical, and Systems Engineering at the University of Bologna.

The converters analyzed in the first two chapters of this thesis were originally proposed by Prof. Riccardo Mandrioli and his research team (including the author himself) in October 2021. The developments in the final chapter were carried out in collaboration with Dr. Andrii Chub at Tallinn University of Technology, where I spent part of my doctoral period as a guest researcher. These collaborations have been essential in shaping both the direction and the scope of this dissertation.

A few words on the structure of this thesis: it is intentionally organized in a unique way that aims to help the reader grasp both the details and the broader perspective of the work. Each main chapter begins with an abstract and introduction, and concludes with a summary that highlights the key insights and contributions. In some cases, parameter labels are reused across chapters; however, every symbol is carefully redefined at its point of use to avoid ambiguity. Additionally, margin notes and highlights are included throughout to guide the reader and provide immediate clarification of selected concepts.

It is my hope that this thesis will serve as both a useful reference and a source of inspiration for further research in the area of power electronic converters and their applications in DC microgrids.

Bologna,
January 20, 2026

Eng. Lohith Kumar Pittala

Acknowledgements

I would like to express my deepest gratitude to my supervisor, **Asst. Prof. Riccardo Mandrioli**, for proposing me as a suitable candidate for the Ph.D. program to the Head of the Power Electronics and Photovoltaics Group – *Solartronic Lab*, **Prof. Gabriele Grandi**. I am sincerely thankful to both of them for welcoming me into their research group, for believing in my abilities, and for their continuous encouragement to pursue an independent research path while guiding me with their valuable experience whenever needed. I also wish to extend my heartfelt thanks to my co-supervisor, **Assoc. Prof. Mattia Ricco**, who has been my mentor since my Master's thesis, for his unwavering support from the very beginning of my academic career. I am deeply grateful for his insightful guidance, inspiring discussions, and for entrusting me with significant research responsibilities throughout our collaborative projects.

I would also like to thank my colleagues from the Power Electronics and Photovoltaics Group – *Solartronic Lab* for their friendship, technical support, and the collaborative spirit that made my research years in Bologna both enriching and enjoyable. In particular, I am grateful to **Assoc. Prof. Vincenzo Cirimele**, **Dr. Francesco Lo Franco**, **Dr. Riccardo Barbone**, and **Dr. Rudolf Francesco Palumbo Paternost** for creating a positive and welcoming environment during my initial days in the group. I would also like to extend my thanks to **Sara Baldisserri** and **Jiayi Geng** for the stimulating discussions and for sharing their knowledge, which led to fruitful collaborations and joint publications. Special thanks go to **Paolo Pilati**, **Costanza Luppi**, **Francesco Maria Tiburtini**, **Riccardo Adinolfi Borea**, and **Bhavana Gudala** for being part of my Ph.D. journey and for the many pleasant moments we shared along the way.

Furthermore, I am sincerely thankful to **Dr. Andrii Chub** and **Prof. Dmitri Vinnikov** for hosting me at the Department of Electrical Power Engineering and Mechatronics, **Tallinn University of Technology (TalTech)**, during my research stay in Estonia. In particular, Dr. Andrii's valuable guidance, constructive feedback, and thought-provoking discussions have greatly deepened my understanding of converter control and modulation techniques. I would also like to thank **Dr. Edivan Laercio Carvalho** for his collaboration, insightful suggestions, and constant encouragement throughout our joint research activities. My appreciation also extends to my colleagues **Dr. Oleksandr Matiushkin**, **Dr. Niwton Gabriel Feliciani dos Santos**, **Dr. Neelesh Yadav**, **Dr. Sachin Chauhan**, **Dr. Vinod Kumar Yadav**, **Salman Khan**, **Sayeed Hasan**, **Hossein Afshari**, and **Parham Mohseni** for their helpful discussions, technical exchanges, and for creating a friendly and motivating atmosphere in the lab. I am truly grateful to all members of the Power Electronics Research Group at TalTech for their warm hospitality and for fostering a collaborative and inspiring environment that made my stay both productive and memorable.

I am profoundly honored that **Assoc. Prof. Satish Naik Banavath** and **Dr. Filippo Pellitteri** agreed to serve as a member of the scientific committee evaluating this dissertation. I sincerely thank them for dedicating their valuable time and for their willingness to provide constructive comments and scientific insights that have helped strengthen this work.

Last but not least, I would like to express my deepest gratitude to my **family** for their unconditional love, patience, and constant encouragement throughout this journey. Their faith in me has been my greatest source of strength during the most challenging times. I am especially thankful to my **parents** for their endless support and sacrifices, and to my **friends** for their understanding, encouragement, and for bringing balance and joy to my life beyond research. This achievement would not have been possible without their unwavering belief in me.

Bologna,
January 20, 2026

Eng. Lohith Kumar Pittala

Abstract

The increasing adoption of DC microgrids in applications such as residential buildings, data centers, and electric vehicle charging stations calls for isolated DC/DC converters that combine efficiency, bidirectional capability, and modular scalability. This thesis focuses on the analysis and improvement of three representative isolated converter families: the dual-active bridge (DAB), the asymmetrical bidirectional DC/DC (AB-DC/DC) converter, and the series resonant converter operated as a DC transformer (SRC-DCX).

The research follows a three-stage methodology of analytical modeling, numerical simulations in PLECS, and experimental validation through hardware prototypes. For the DAB, the work derives closed-form zero-voltage switching (ZVS) boundaries and investigates auxiliary inductors as a means to extend ZVS at light load and wide voltage ratios. The analysis is further extended to the current-fed DAB (CF-DAB), providing new insights into unipolar and bipolar DC grid operation.

In the AB-DC/DC converter, passive power sharing between the active and diode bridges is shown to be highly sensitive to magnetic tolerances, which can compromise thermal balance in the semiconductor devices. A probabilistic framework is developed to quantify this effect, and novel active power sharing control and hybrid modulation strategies are introduced to enable controllable power distribution between the parallel-connected bridges. Large-scale simulations and an experimental prototype confirm the feasibility of these methods.

Finally, the thesis addresses the SRC-DCX, a topology well-suited for high-efficiency fixed-ratio conversion but lacking inherent power regulation. A sigma–delta cycle-skipping modulation is proposed to recover fine-grained power control without sacrificing soft-switching. The method is validated on a 1 kW prototype, and also verifies the effective current sharing between the input-parallel and output-parallel modular configuration.

Overall, the thesis provides analytical tools, control strategies, and experimental evidence that improve the efficiency, reliability, and controllability of isolated DC/DC converters in DC microgrids. The results are expected to support the development of scalable and robust converter architectures for next-generation energy systems.

Index Terms—Asymmetrical Bidirectional DC/DC (AB-DC/DC), Bidirectional converters, Cycle-Skipping Modulation, DC transformer (DCX), DC microgrids, Dual Active Bridge (DAB), Isolated DC/DC converters, Series Resonant Converter (SRC), Sigma–Delta modulation, Power sharing control, Zero-Voltage Switching (ZVS).

Contents

Preface i

Acknowledgements iii

Abstract v

Contents vii

1 Introduction 1
- 1.1 DC Microgrid Classifications . . . 1
- 1.2 Classification of DC Bus Voltages and Related Standards . . . 4
- 1.3 Isolated DC/DC Converters . . . 6
- 1.4 Basic Isolated DC/DC Converters . . . 6
  - 1.4.1 Flyback Converter . . . 6
  - 1.4.2 Forward Converter . . . 7
  - 1.4.3 Push–Pull Converter . . . 8
  - 1.4.4 Isolated Ćuk Converter . . . 8
- 1.5 Bridge-Based Isolated DC/DC Converters . . . 9
  - 1.5.1 Dual-Active Bridge . . . 10
  - 1.5.2 Combination of DAB and SAB . . . 11
  - 1.5.3 Series Resonant Converter . . . 12
- 1.6 Methodology and Motivation . . . 13
  - 1.6.1 Methodology . . . 13
  - 1.6.2 Motivation . . . 13
- 1.7 Thesis Outline . . . 14

2 Zero-Voltage Switching Analysis of Conventional and Current-Fed DAB Converters 15
- 2.1 Literature Review on Enhancement of ZVS in DAB Converter . . . 15
- 2.2 Background on DAB Operation . . . 17
  - 2.2.1 Ideal Boundary Conditions of the ZVS Region . . . 18
  - 2.2.2 Dead Time and Parasitic Capacitance Effects on ZVS . . . 18
- 2.3 ZVS Extension with Auxiliary Inductors . . . 20
  - 2.3.1 Auxiliary Inductor on the Input Side of the DAB . . . 20
  - 2.3.2 Auxiliary Inductor on the Output Side of the DAB . . . 21
  - 2.3.3 Evaluation of Switch Current RMS . . . 22
  - 2.3.4 Numerical Validations . . . 25
  - 2.3.5 Experimental Validations . . . 26
- 2.4 Current-Fed Dual-Active-Bridge Converter . . . 30
- 2.5 Working Principle of an Interleaved CF-DAB . . . 30
  - 2.5.1 ZVS Analysis without the DC Offset Case . . . 31
  - 2.5.2 ZVS Analysis with the DC Offset Case . . . 32
  - 2.5.3 Numerical Validations . . . 34
  - 2.5.4 Experimental Validations . . . 36
- 2.6 Summary . . . 38

3 Asymmetrical-Bidirectional DC/DC Converter 39
- 3.1 Introduction to Asymmetrical Bidirectional DC/DC Converter . . . 39

3.2 Single-Active Bridge Converter . . . 41
3.2.1 Power Transfer in SAB Converter . . . 41
3.2.2 DCM-CCM Boundary Conditions . . . 43
3.3 Asymmetrical-Bidirectional DC/DC Converter . . . 43
3.4 Passive Power Sharing Control . . . 44
3.4.1 Converter Leg Power PDF . . . 45
3.4.2 Bridge Power PDF . . . 47
3.4.3 Numerical Validations . . . 48
3.5 Active Power Sharing Control . . . 52
3.5.1 Discontinuous Conduction Mode Region . . . 53
3.5.2 Hybrid 1 Region . . . 54
3.5.3 Hybrid 2 Region . . . 55
3.5.4 Continuous Conduction Mode Region . . . 56
3.5.5 Dual-Active-Bridge Region . . . 56
3.5.6 Numerical Validations . . . 57
3.5.7 Efficiency Analysis . . . 58
3.5.8 Operation and Performance . . . 60
3.5.9 Experimental Validations . . . 62
3.6 Hybrid Modulation: Alternating Active Power Sharing and SAB Control . . . 66
3.6.1 Numerical Validation . . . 67
3.7 Summary . . . 70

4 Series Resonant DC Transformer **71**
4.1 Introduction to Series Resonant Converters . . . 71
4.2 Series Resonant Converter Operating as a DC Transformer . . . 73
4.3 Cycle-Skipping Modulation . . . 75
4.3.1 ZVS Analysis in the Series Resonant Converter . . . 76
4.3.2 Voltage Ripple Analysis in the Conventional CSM . . . 78
4.4 Sigma-Delta Based Cycle-Skipping Modulation . . . 78
4.4.1 Example: Conventional CSM and Sigma-Delta-based CSM . . . 79
4.4.2 Implementation of Sigma-Delta-based CSM in STM32 microcontrollers . . . 81
4.5 Hardware Design of a Series Resonant Converter . . . 83
4.5.1 Power Regulation of an SRC-DCX . . . 84
4.5.2 Experimental Validations . . . 85
4.6 Current Sharing Control in Input Parallel and Output Parallel SRC-DCX . . . 87
4.6.1 Experimental Validation . . . 88
4.6.2 Parallel Operation of an SRC-DCX . . . 88
4.6.3 Open-Loop Control Validation . . . 89
4.6.4 Closed-Loop Control Validation . . . 91
4.7 Summary . . . 95

5 Conclusion and Future Research **97**
5.1 Chapter Review and Contribution . . . 97
5.2 Proposal for Future Research . . . 99

Appendix **101**

A PLECS Simulation Script **103**
A.1 Parameter Sweep Analysis for Statistical Analysis . . . 103
A.2 Parameter Sweep Analysis for Active- and Diode Bridge Power Measurements . . . 104

List of figures **109**

List of tables **111**

Bibliography **113**

Nomenclature **123**

Introduction 1

Overview

This chapter introduces the global context, from which the motivation of the current thesis originates. The chapter deals with state-of-the-art and recent advancements in high-power converter topologies that are used in the direct-current (DC) microgrids.

1.1 DC Microgrid Classifications 1
1.2 Classification of DC Bus Voltages and Related Standards 4
1.3 Isolated DC/DC Converters 6
1.4 Basic Isolated DC/DC Converters 6
1.4.1 Flyback Converter 6
1.4.2 Forward Converter 7
1.4.3 Push–Pull Converter . . . 8
1.4.4 Isolated Ćuk Converter . 8
1.5 Bridge-Based Isolated DC/DC Converters 9
1.5.1 Dual-Active Bridge 10
1.5.2 Combination of DAB and SAB 11
1.5.3 Series Resonant Converter 12
1.6 Methodology and Motivation 13
1.6.1 Methodology 13
1.6.2 Motivation 13
1.7 Thesis Outline 14

DC microgrids are increasingly attracting attention due to their ability to reduce power-conversion losses and simplify the integration of renewable energy sources, storage units, and electronic loads [1]. Thanks to these advantages, as well as the growing presence of storage systems and DC-compatible loads, DC microgrids are becoming relevant across a wide range of applications. Examples include residential houses, commercial buildings, data centers, and agricultural farms. More recently, emerging applications such as electric vehicle (EV) charging infrastructures have further accelerated this trend. In particular, fast EV chargers inherently require a DC power supply, making DC microgrids an attractive platform, and several proposals have already been presented in this context [2].

In parallel, the rise of prosumers has become a key element in low-voltage (LV) distribution networks. Their seamless integration into LVDC systems is considered natural, as it enables cost savings and improved energy efficiency [3]. From a practical perspective, low-voltage DC microgrids typically operate at 380–400 V. These bus voltages are well-suited for servers, LED lighting, and battery systems, while also avoiding the need for back-to-back AC–DC conversions. However, renewable sources such as photovoltaic (PV) modules generally produce much lower DC voltages, typically in the 20–60 V range per panel [4]. As a result, step-up DC/DC converters are essential for interfacing low-voltage sources and storage devices with the high-voltage DC bus.

While these examples illustrate common practice, it is important to note that DC microgrid bus voltages are not arbitrary. In fact, several standardized classifications of DC voltage levels have been proposed, which serve as a reference for system design and ensure compatibility across different applications. These classifications are particularly relevant for defining the operating ranges of DC/DC converters. The following sections provides an overview of the DC microgrid classifications along with the voltage categories and their relation to existing standards.

1.1 DC Microgrid Classifications

Fig.1.1 depicts the simplest architecture of a DC microgrid with various loads and sources. This type of architecture is also known as single bus topology. Apart from this, there are radial topology, ring or loop topology, mesh topology, and interconnected topology in the literature [6], [7]. The choice of DC microgrid topology strongly influences reliability, protection, and control strategies. For instance, radial structures are easy to expand but vulnerable to single-point failures, whereas ring

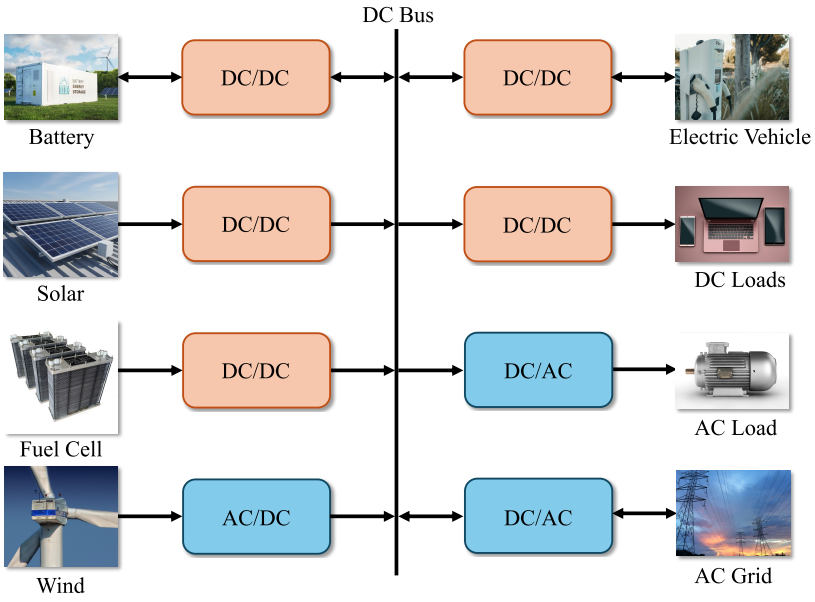


Figure 1.1: Typical architecture of a DC microgrid with various loads and sources [5].

and mesh topologies enhance resilience at the cost of higher complexity. Applications often dictate the choice: residential or small-scale systems typically employ single-bus or radial layouts, while critical infrastructures such as data centers and transportation networks increasingly consider ring or bipolar structures for improved reliability [1], [8]. At present, no dedicated standards exist for DC microgrid architectures, which limits their widespread adoption [2]. Existing efforts, including the IEEE standards on interconnection and interoperability of distributed energy resources with electric power system interfaces [9], [10], primarily address grid integration aspects and do not provide guidance on DC distribution layouts.

On the other hand, DC microgrids can also be configured in terms of wiring schemes, namely unipolar and bipolar configurations. The unipolar configuration is the simplest one, consisting of only two wires and therefore imposing a single DC voltage level [11]–[14]. In this case, all generators, loads, and storage systems are connected to the same pair of poles, as illustrated in Fig. 1.2.

In contrast, the bipolar configuration is more complex, as it employs three conductors, positive, neutral, and negative, thus enabling two distinct DC voltage levels, as shown in Fig. 1.3. This arrangement provides multiple possibilities for interfacing generators, loads, and storage systems: between the positive and neutral, between the negative and neutral, or across the full positive and negative poles. Consequently, the bipolar scheme offers greater flexibility, as it allows devices to operate either at the full pole-to-pole voltage or at half of it when connected through the neutral. Despite its added complexity, the bipolar approach enhances adaptability to technologies with varying voltage requirements and offers additional benefits, including higher efficiency, resilience, and fault tolerance. However, a notable drawback is the risk of voltage imbalance, which can arise from asymmetrical loading or bidirectional operation [15]–[17].

A summary of the main DC microgrid classifications, including both network topologies and wiring configurations, is provided in Table 1.1. This comparison highlights the trade-offs in terms of complexity, reliability,

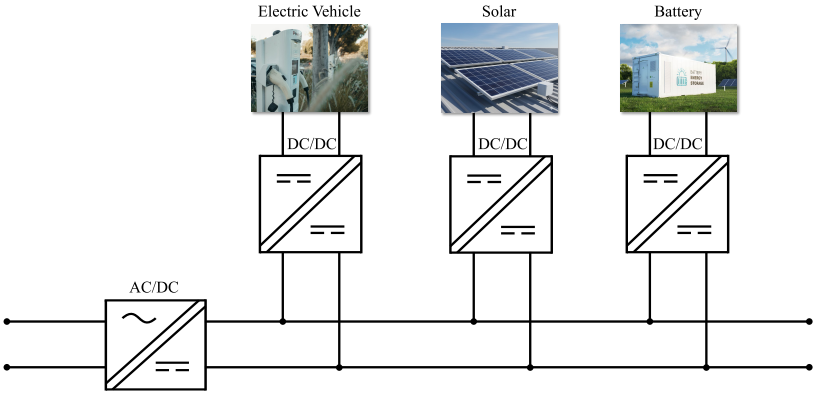


Figure 1.2: Unipolar configuration.

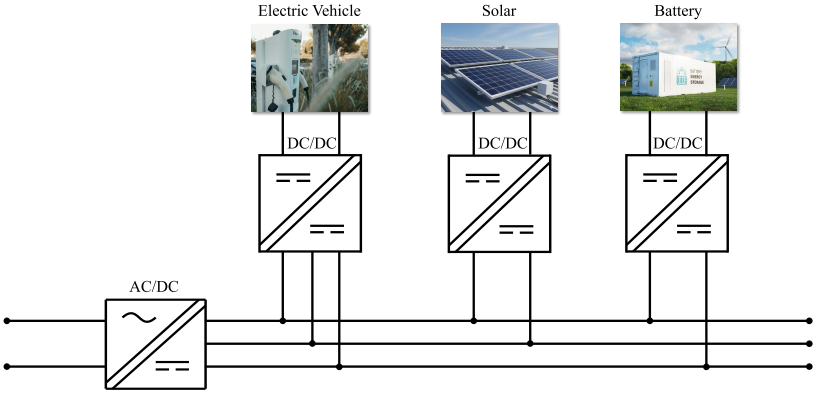


Figure 1.3: Bipolar configuration.

Table 1.1: Comparison of DC microgrid topologies and configurations.

Type	Features / Applications	Advantages / Limitations	References
Single-bus topology	Simplest structure, all sources and loads connected to a common bus. Used in small residential or stand-alone systems.	Low cost, simple control; but poor reliability and difficult fault isolation.	[6], [7]
Radial topology	Sources and loads distributed along radial feeders. Common in small communities or farms.	Easy expansion, simple protection; single-point failure risk.	[18], [19]
Ring/loop topology	Closed-loop feeder; often used in critical infrastructure.	Improved reliability and fault tolerance; requires more complex protection and control.	[20], [21]
Mesh/interconnected topology	Multiple interconnections between buses. Considered for large-scale or mission-critical DC systems.	Highest reliability and redundancy; high cost and complexity.	[22], [23]
Unipolar configuration	Two-wire system (single DC voltage level, e.g., 350 V).	Simple, low cost; but limited flexibility and no redundancy.	[11]–[14]
Bipolar configuration	Three-wire system (positive, neutral, negative), supports dual voltage levels (e.g., ±350 V).	Flexible voltage options, higher efficiency and resilience; risk of voltage imbalance under asymmetrical loading.	[15]–[17]

and applicability across different use cases.

Nevertheless, DC microgrids alone cannot fully replace AC systems, since most existing infrastructure and end-user equipment still rely on AC supply. Therefore, practical microgrid architectures typically integrate both DC/DC and AC/DC converters to ensure compatibility with a wide range of loads, as shown in Fig. 1.1. This hybrid architecture supports the

gradual transition toward DC microgrids without requiring a complete replacement of conventional AC-based systems [24]. Nonetheless, this thesis focuses exclusively on DC/DC converters, with particular emphasis on those providing galvanic isolation within the system.

Having discussed the main classifications of DC microgrids in terms of architecture and configuration, the following section addresses the classification of DC bus voltages and related standards, which are essential for defining the operating ranges of DC/DC converters.

1.2 Classification of DC Bus Voltages and Related Standards

The voltage level adopted in a DC microgrid is a fundamental design choice, as it directly affects the applicability and operating limits of DC/DC converters. For reference, on the AC side, single-phase systems typically operate between 110–240 V_{rms}, while three-phase systems are commonly standardized at 380–400 V_{rms}. On the DC side, supply levels span from extra-low voltages to several hundred volts within the LVDC domain [24].

According to IEC recommendations [25], a set of nominal DC voltage levels has been identified to guide practical implementations. In residential and office environments, a wide variety of DC loads is already present, including LED lighting, computers, and household appliances. To ensure user safety in such contexts, extra-low voltage DC levels or the use of galvanic isolation are generally preferred. Telecom systems also rely heavily on low-voltage buses, with critical loads often supplied at 12–60 V. Nevertheless, extra-low voltage buses are naturally constrained in terms of distance and power capability, since higher currents over long conductors lead to excessive conduction losses. As indicated in [25], their use is most suitable for short-distance distribution and power levels on the order of 1 kW.

At the next level, low-voltage DC in the 350–450 V range has gained significant traction, particularly for information and communication technology (ICT) and light industrial applications. A common example is the 380 V bus, which has become the de facto standard in data centers, server racks, and uninterruptible power supplies, as specified in the IEEE 1184-2022 standard [26]. These LVDC levels enable higher power transfer while still maintaining compatibility with typical building-scale installations such as nanogrids, e.g., see IEC TR 63282:2024 for recommended voltage ranges and power quality guidelines [27].

Higher DC bus levels in the range of 600–900 V and up to 1.5 kV are generally reserved for larger-scale or utility applications, where increased distribution distances justify the higher voltage. However, their adoption in residential or small commercial microgrids is limited, primarily due to the more stringent safety and protection requirements, as these levels pose a direct hazard to end-users, for example, IEEE trip systems cover DC circuits up to 1.5 kV [28]. Additionally, transportation applications, such as electric ships, aircraft, and railway traction, are increasingly considering higher DC bus levels.

To provide a unified view, several studies have proposed standardized

Table 1.2: Proposed classification of the main DC buses for DC microgrids [24].

Voltage level	Standards	DC bus classification	Power levels	Application
0–48 V dc	IEC 60364	extra low voltage auxiliary DC buses	~ 1 kW	Electronic devices with limited output current: home appliances, TVs, lighting, critical loads at data centers, medical equipment, emergency lighting.
60–120 V dc	IEC 60364	Auxiliary DC buses	< 6 kW	Typical household and office loads >1 kW; applicable in remote residential and commercial microgrids.
190–230 V dc	IEC 60364	Auxiliary DC buses	< 6 kW	Distribution-level buses in buildings, offices, and commercial facilities.
350–450 V dc	IEC 60364, NPR 9090	Main DC bus for building-scale microgrids (nanogrids)	~ 20 kW	Distribution buses in homes, offices, hospitals, and prosumer electrical installations (PEIs).
600–900 V dc	IEC 60364, NPR 9090	Main DC bus for industry-scale microgrids	< 0.5 MW	Industrial systems, transportation, and other high-power applications.
1–1.5 kV dc	IEC 60364, NPR 9090	Utility-scale DC bus	> 0.5 MW	Utility-scale PV plants and microgrids at distribution level.

classifications of DC bus voltage levels, which consider application domains, power ratings, and safety requirements. A few standards are mentioned above, and another classification is summarized in Table 1.2, adapted from [24], which organizes DC voltage levels for microgrids along with their standards, and representative use cases.

While the choice of voltage level defines the operating domain of a microgrid, it also determines the requirements imposed on the power conversion stage. For instance, in extra-low voltage buses (12–60 V), commonly adopted in ICT systems, converters are frequently required to operate under light-load conditions for long periods, which can result in degraded efficiency. In building-scale nanogrids around 380 V, energy storage systems introduce asymmetrical bidirectional power exchange, where the charging and discharging processes occur at different power levels. The same challenge appears in the EV charging systems when the power is flowing between the grid to vehicle (G2V) and vehicle to grid (V2G). Similarly, in renewable energy integration, unidirectional power transfer is often required, as photovoltaic sources must either step up or step down their voltage to interface with the DC bus. These examples illustrate the diversity of operating conditions, highlighting the need for converter topologies that can ensure efficient operation across different load scenarios and power flow directions.

A common requirement in all these applications is the use of galvanic isolation. Isolation not only improves safety against electric shocks at higher voltages, but also allows different voltage domains to be interconnected and provides fault separation between subsystems. Moreover, by adopting high-frequency transformers (HFTs) together with advanced wide-bandgap semiconductors such as SiC and GaN, isolated DC/DC converters can operate at much higher switching frequencies. This significantly reduces the size, volume, and

weight of the magnetic components, making them particularly attractive for modern DC microgrids. Besides safety and size reduction, galvanic isolation also improves electromagnetic compatibility by limiting the propagation of conducted noise between different domains. Furthermore, their design must also comply with general power electronic application guidelines. In this regard, IEEE Std 1662-2016 provides recommended practices for the design and application of power electronics in AC and DC electrical power systems, including converters, solid-state breakers, and energy storage systems [29].

1.3 Isolated DC/DC Converters

Isolated DC/DC converters can be broadly grouped into two categories: basic configurations, such as flyback, forward, push–pull converters, and isolated Ćuk converter, and bridge-based configurations, including half-bridge, full-bridge, and resonant topologies. Basic converters are commonly adopted in low- to medium-power applications, where simplicity, low cost, and ease of implementation are the main priorities. Bridge-based converters, on the other hand, are typically employed at higher power levels, as they offer superior efficiency, better scalability, and the potential for soft-switching.

The following sections present a detailed discussion of both families of converters. First, the operating principles and application areas of the basic configurations are introduced, highlighting their strengths and limitations. Then, the bridge-based topologies are discussed, with emphasis on their advantages in addressing the power, efficiency, and reliability requirements of modern DC microgrids.

1.4 Basic Isolated DC/DC Converters

1.4.1 Flyback Converter

The flyback converter is one of the simplest isolated topologies, shown in Fig. 1.4. It operates by storing energy in the transformer's magnetizing inductance when the primary switch is turned on, and releasing it to the secondary side when the switch is turned off. Because the transformer does not transfer energy simultaneously but rather in a two-step process, it effectively behaves like a coupled inductor. The main advantages of the flyback converter are its simplicity, low component count, and low

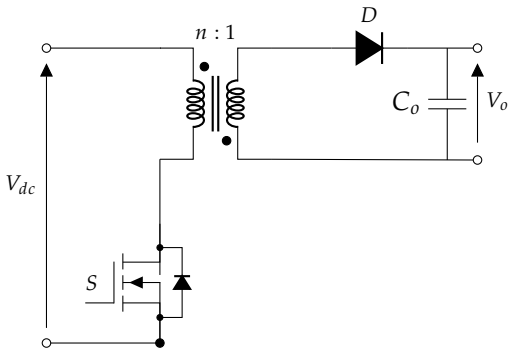


Figure 1.4: Basic topology of a flyback converter.

cost. For this reason, it is extensively used in low-power applications, typically below 150 W, such as auxiliary power supplies in consumer electronics, adapters, battery chargers, and standby supplies. However, the discontinuous energy transfer results in high current and voltage stress on the switches and transformer, significant output ripple, and poor efficiency at higher power levels [30]. In addition, the transformer design becomes challenging due to the large magnetizing current and leakage inductance. These drawbacks make the flyback converter unsuitable for medium- or high-power applications as encountered in DC microgrids.

1.4.2 Forward Converter

The forward converter improves efficiency over the flyback by transferring energy directly from the primary to the secondary during the ON period of the switch. Unlike the flyback, the transformer operates as a true transformer, requiring a demagnetizing circuit (reset winding or active clamp) to avoid core saturation. The basic topology of a forward converter is depicted in Fig. 1.5. Forward converters typically operate in the power range of 100 W to 500 W and are used in applications such as industrial control systems, instrumentation, and low- to medium-power distributed supplies. Its advantages include higher efficiency compared with the flyback, lower ripple currents, and better utilization of the transformer [31]. Nonetheless, it requires additional components for core reset, and its single-ended structure places voltage stress across the switch equal to twice the input voltage [32]. Moreover, scalability is limited because duty cycle constraints restrict the maximum power that can be handled

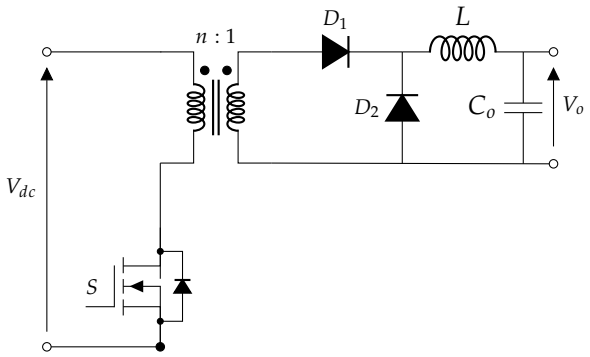


Figure 1.5: Basic topology of a forward converter.

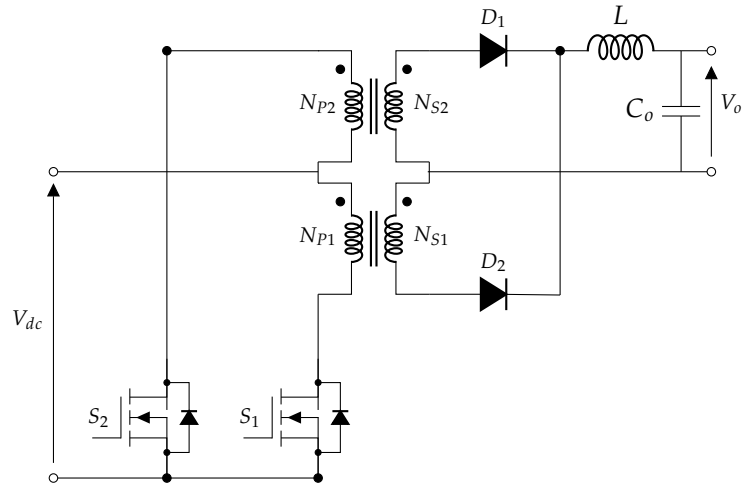


Figure 1.6: Basic topology of a push–pull converter.

efficiently [33]. For these reasons, forward converters are not generally applied in high-power DC microgrid systems.

1.4.3 Push–Pull Converter

The push–pull converter consists of two primary switches that alternately drive the transformer, resulting in bidirectional core magnetization and better utilization of the magnetic material. The converter topology is illustrated in Fig. 1.6. This enables higher power transfer capability compared with flyback and forward converters, typically up to 1 kW. It is widely employed in medium-power applications such as telecom power supplies, automotive electronics, and cost-sensitive distributed power systems [34]. The main advantages of the push–pull topology are its relatively simple structure, higher transformer utilization, and the possibility of stepping voltages up or down with moderate efficiency [35], [36]. However, it is susceptible to transformer saturation caused by an imbalance between the two switch drive signals, which can lead to core flux walking [37]. The topology also suffers from high voltage stress across the switches, equal to twice the input voltage, and limited soft-switching possibilities. As the power level increases, these drawbacks become significant, preventing push–pull converters from being a viable solution for DC microgrids operating in the kilowatt range and above.

1.4.4 Isolated Ćuk Converter

The isolated Ćuk converter, shown in Fig. 1.7, is derived from the conventional non-isolated Ćuk topology by replacing the series inductor with a high-frequency transformer, thereby introducing galvanic isolation and allowing a flexible turns ratio for voltage step-up or step-down. Its operation is based on the energy transfer through a series capacitor, which alternately charges and discharges depending on the switching state. This mechanism enables the converter to provide an inverted output voltage with respect to the input, while the transformer adds the advantage of isolation and voltage scalability.

A notable feature of the Ćuk family is the presence of inductors on both the input and output sides, which results in low input and output current ripple compared to flyback or forward converters. This makes the isolated Ćuk attractive in applications where smooth current is required, such as sensitive instrumentation or telecom supplies. Typical power levels range from a few tens of watts up to around 200–300 W, depending on design.

Despite these advantages, the isolated Ćuk suffers from several limitations. The additional series capacitor increases component count and voltage stress, leading to higher conduction losses. The transformer experiences

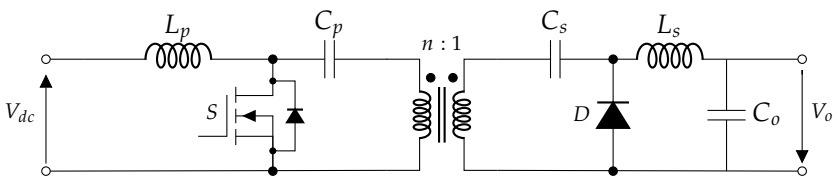


Figure 1.7: Basic topology of an isolated Ćuk converter.

Table 1.3: Comparison of basic isolated DC/DC converter topologies

Converter	Typical power range / applications	Advantages	Limitations
Flyback	Below ~150 W; adapters, battery chargers, standby supplies, consumer electronics.	Very simple, low cost, minimal components, inherent isolation.	High ripple, poor efficiency at higher power, high device stress, difficult transformer design, limited scalability.
Forward	100–500 W; industrial control, instrumentation, medium-power auxiliary supplies.	Higher efficiency than flyback, lower ripple currents, better transformer utilization.	Extra reset circuitry required, duty-cycle limitation, voltage stress up to $2V_{dc}$, limited scalability.
Push–Pull	Up to ~ 1 kW; telecom supplies, automotive electronics, distributed power.	Moderate efficiency, relatively simple, better power capability than flyback/forward.	Core imbalance risk (flux walking), voltage stress of $2V_{dc}$, transformer saturation issues, poor soft-switching, not suitable above ~1 kW.
Isolated Ćuk	Tens of watts up to ~200–300 W; telecom, instrumentation, low-noise supplies.	Low input/output current ripple due to dual inductors; flexible step-up/step-down capability.	Higher component count, higher conduction losses, efficiency limited at higher power.

significant voltage stress as well, and the control complexity increases due to the dual inductor and energy transfer capacitor design [38]. Moreover, efficiency degrades at higher power levels, and the topology is not easily scalable beyond a few hundred watts. For these reasons, isolated Ćuk converters are also mainly confined to low- to medium-power applications and are not widely adopted in DC microgrids, where kilowatt-level power processing is required. However, recent developments were made to achieve the scalability in such converters, see [39].

Notice that all the basic isolated converters illustrated from Fig. 1.4 to Fig. 1.7 are inherently unidirectional. However, bidirectional power flow can also be achieved by replacing the secondary-side diodes with actively controlled switches. A summary of the main characteristics of these basic isolated converter topologies is presented in Table 1.3. It highlights their operating power ranges, advantages, and limitations. While these converters are attractive for low- to medium-power auxiliary supplies due to their simplicity and low cost, the table also makes clear that their inherent limitations restrict their use in the higher power levels required by DC microgrids.

1.5 Bridge-Based Isolated DC/DC Converters

From the discussion above, it is clear that flyback, forward, push–pull, and isolated Ćuk converters provide simple and cost-effective solutions for auxiliary and low-power applications. These topologies remain relevant in domains such as consumer electronics, instrumentation, and telecom, where the power levels rarely exceed a few hundred watts. However, the focus of this thesis is on DC microgrids, where converters are required not only to interface low-voltage sources and storage, but also to

process power in the kilowatt range with high efficiency, scalability, and bidirectional capability. Under these conditions, the limitations of basic configurations in terms of efficiency, device stress, and scalability become critical. As a result, the attention is shifted toward bridge-based isolated converters, which offer superior performance, support higher power density, and enable the implementation of soft-switching techniques [5].

Bridge-based converters, such as the half-bridge, full-bridge, and resonant families of converters, overcome many of the limitations of basic configurations. By employing multiple switches and utilizing both halves of the transformer core, these topologies achieve higher efficiency, improved power-handling capability, and reduced voltage stress on devices. Furthermore, the possibility of incorporating soft-switching techniques, such as zero-voltage switching (ZVS) or zero-current switching (ZCS), significantly reduces switching losses and enhances overall system performance.

It is worth noting that the family of bridge-based isolated converters is broad and includes topologies such as the single-active bridge (SAB), dual-active half-bridge (DAHB), dual-active bridge (DAB), phase-shift full-bridge (PSFB), and in general, the multi-active bridge (MAB). Resonant converters, including the LLC, CLLC, and their hybrid derivatives, have also been widely investigated in the literature for applications ranging from renewable energy integration to electric vehicle charging [40], [41]. Nevertheless, in this thesis the scope is deliberately restricted to three representative converters: the dual-active bridge (DAB), the combination of DAB and single-active bridge (SAB) here after defined as asymmetrical-bidirectional DC/DC converter (AB-DC/DC), and the series resonant converter (SRC) operated as a DC transformer. The following sections focus on these three topologies and outline the key challenges that are addressed in this work.

1.5.1 Dual-Active Bridge

The DAB, illustrated in Fig. 1.8, is one of the most widely studied isolated DC/DC topologies for medium- and high-power applications in DC microgrids [42]. It consists of two active H-bridges interconnected through a high-frequency transformer and a series leakage inductance. Power transfer is regulated by modulating the relative phase shift between the two bridges. Several modulation strategies have been proposed in the literature, such as single-phase shift (SPS), dual-phase shift (DPS), extended-phase shift (EPS), and triple-phase shift (TPS), each aiming to improve efficiency, reduce circulating currents, or extend the soft-switching range [43], [44].

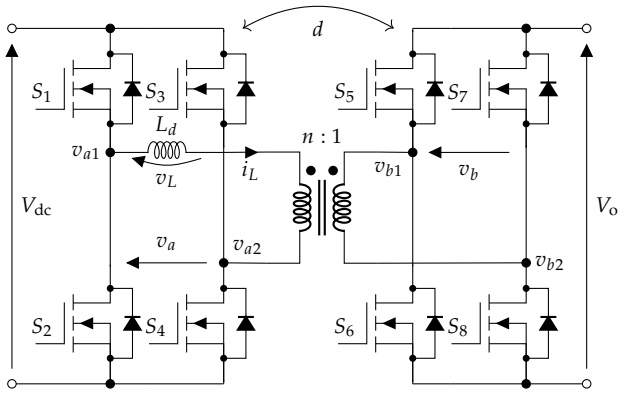


Figure 1.8: Dual-active-bridge converter.

A key limitation of the conventional DAB is that zero-voltage switching (ZVS) across the entire load range generally requires the voltage gain to remain close to unity, which constrains the converter's voltage conversion flexibility [45]. To address this issue, auxiliary elements or advanced modulation schemes are often introduced to enlarge the ZVS operating region and to mitigate partial-load losses.

Despite these challenges, the DAB remains one of the most attractive candidates for bidirectional energy exchange in DC microgrids, owing to its galvanic isolation, scalability, and high efficiency. Moreover, by introducing interleaved inductors, the converter's output DC link can be split into two, forming a current-fed DAB (CF-DAB). This configuration is particularly well-suited for both unipolar and bipolar DC grids. A detailed analysis of this converter is presented in the corresponding chapter.

1.5.2 Combination of DAB and SAB

The SAB, illustrated in Fig. 1.9, can be regarded as a simplified counterpart of the DAB, where only the primary H-bridge is active while the secondary side employs a diode bridge for rectification. This results in a unidirectional power flow capability, making the SAB particularly suitable for applications such as photovoltaic (PV) systems and unidirectional charging stages. Power control is achieved by introducing a phase shift between the two legs of the primary bridge, which enables operation in both continuous-conduction mode (CCM) and discontinuous-conduction mode (DCM) [46]. While the SAB is less flexible than the DAB, its reduced device count and control complexity make it an attractive solution for low-cost and unidirectional applications. Furthermore, when combined with the DAB, it gives rise to the asymmetrical bidirectional DC/DC (AB-DC/DC) converter, depicted in Fig. 1.10, which addresses the challenge of asymmetrical bidirectional power flow by leveraging both active and passive bridges [47]–[49].

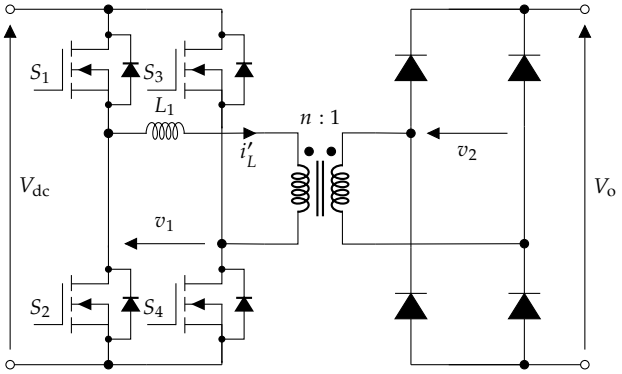


Figure 1.9: Single-active-bridge converter.

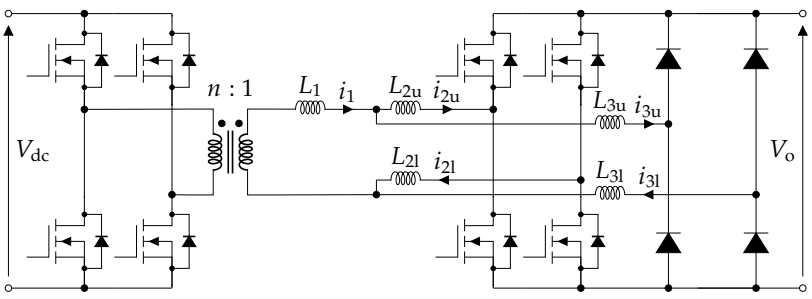


Figure 1.10: Asymmetrical bidirectional DC/DC converter.

1.5.3 Series Resonant Converter

The SRC belongs to the resonant family of bridge-based converters and is characterized by the inclusion of a resonant tank, typically composed of a series inductor and capacitor, between the inverter stage and the transformer, as illustrated in Fig. 1.11. Control of the SRC can be realized through phase-shift modulation (PSM), frequency modulation (FM), or hybrid schemes. When operated conventionally, the resonant tank enables soft-switching and high efficiency over a wide load range [50], [51]. However, when the SRC is operated as a DC transformer (DCX), the control freedom is largely lost: the converter behaves as a nearly load-independent stage, delivering power with very high efficiency but without the ability to regulate the output [52]. This makes the SRC-DCX an excellent candidate for applications requiring fixed-ratio conversion at high efficiency, though unsuitable for scenarios that demand dynamic power regulation. In this thesis, particular emphasis is placed on the analysis of output voltage ripple and the development of advanced modulation schemes to achieve power regulation while preserving the inherent advantages of the SRC-DCX.

Table 1.4 summarizes the main characteristics of the SAB, DAB, and SRC topologies. It highlights their application domains, advantages, and inherent limitations. While the SAB provides a cost-effective solution for unidirectional interfaces such as PV or auxiliary chargers, the DAB remains the most versatile option for bidirectional energy transfer in

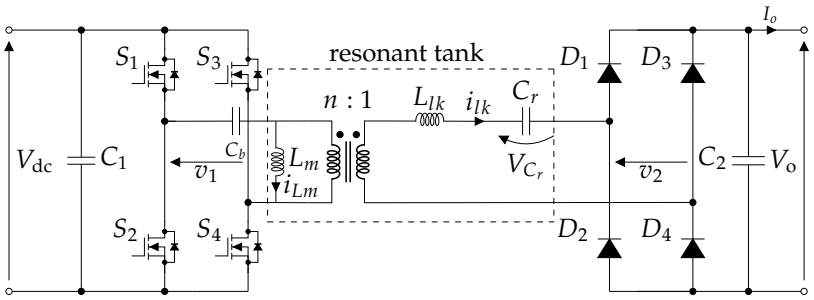


Figure 1.11: Series resonant converter operating as a DC transformer.

Table 1.4: Comparison of bridge-based isolated DC/DC converter topologies

Converter	Typical applications	Advantages	Limitations
DAB	Bidirectional DC microgrids, ESS integration, EV charging (G2V/V2G).	Bidirectional power flow, galvanic isolation, scalable to kW range, enables ZVS under suitable conditions, modularity.	ZVS across full load only at unity gain; circulating currents; reduced efficiency at light load without auxiliary measures.
AB-DC/DC (SAB+DAB)	Bidirectional DC microgrids, ESS integration, EV charging (G2V/V2G).	It has DAB advantages, and it is cost-effective, and possible soft-switching in certain conditions.	Increased number of total components count, Power-sharing between the parallel connected active and diode bridge.
SRC	Data centers, telecom, PV systems	Natural soft-switching, high efficiency, load-independent transfer in DCX mode, reduced EMI.	In DCX mode: no power regulation, sensitive to parameter variations; requires careful design for wide load adaptability.

DC microgrids, particularly in ESS integration and EV charging. The SRC, on the other hand, offers outstanding efficiency and soft-switching operation, especially when used as a fixed-ratio DC transformer (DCX).

A common feature of all these bridge-based converters is their scalability. By leveraging modular architectures and high-frequency transformers, they can be extended from a few kilowatts up to the megawatt range, thereby meeting the demands of future LVDC and bipolar DC microgrids. This scalability, combined with galvanic isolation and the potential for soft-switching, makes bridge-based isolated DC/DC converters the most promising candidates for next-generation high-power applications.

1.6 Methodology and Motivation

1.6.1 Methodology

The work presented in this thesis follows a multi-stage methodology that combines analytical modeling, numerical simulations, and experimental validation. First, analytical derivations are developed to capture the fundamental operation of the selected topologies. These models are employed to determine the ZVS boundaries in the DAB family, the power transfer characteristics in the AB-DC/DC converter, and the power regulation and ripple behavior in the SRC-DCX.

The analytical results are then verified through extensive numerical simulations performed in PLECS. These simulations enable evaluation over a wide range of operating scenarios, including light- and full-load conditions, bidirectional and unidirectional power flow, and unbalanced load operation as in bipolar DC grids. For the AB-DC/DC converter in particular, parameter sweep analyses were carried out to study the sensitivity of performance to variations in passive components and phase-shift values.

Finally, experimental validation is conducted using hardware prototypes designed to operate at representative power levels. The measured results are systematically compared with both analytical predictions and simulation outcomes, ensuring the theoretical developments are consistent with practical implementation.

1.6.2 Motivation

Bridge-based isolated converters are central to DC microgrids, yet three recurring limitations remain:

(i) *DAB soft-switching at light load and wide voltage ratios*: ZVS is often lost away from unity gain, causing hard-switching and performing under lower efficiencies. This motivates auxiliary inductors and refined modulations to extend ZVS with acceptable RMS cost. Moreover, the same analysis is extended to the CF-DAB, which is useful to operate in both unipolar and bipolar DC grids.

(ii) *Asymmetrical bidirectional power flow*: Solves the issue related to the practical systems (e.g., G2V/V2G, storage), where forward and reverse powers are unequal. Passive power sharing in AB-DC/DC is sensitive to component tolerances and can lead to thermal imbalance. This motivates

to develop a novel modulation technique that enable the active/hybrid power sharing strategies.

(iii) *SRC operated as a DC transformer (DCX)*: While offering excellent efficiency and inherent soft-switching, it sacrifices output power regulation. This motivates to develop a Sigma-Delta ($\Sigma\Delta$) based cycle-skipping modulation to recover controllable power flow and coordinated sharing in parallel SRC-DCX modules.

Together, these gaps justify the contributions developed in this thesis across DAB/CF-DAB, AB-DC/DC, and SRC-DCX.

1.7 Thesis Outline

The above-mentioned converters are analyzed across three main chapters, while the final chapter provides the overall conclusions of the thesis. The organization of the thesis is as follows:

- **Chapter 2 (Zero-Voltage Switching Analysis of Conventional and Current-Fed DAB Converters) on the facing page**
  Analytical ZVS boundaries for conventional DAB are derived and then extended using auxiliary inductors (input/output side), highlighting the ZVS–RMS trade-off; results are validated numerically and experimentally on a 300 W prototype.
  The analysis is then extended to the CF-DAB for unipolar/bipolar DC grids, deriving ZVS regions under zero and nonzero DC offset, with numerical confirmation and a 5 kW experiment prototype demonstrating the DC offset behavior.
- **Chapter 3 (Asymmetrical-Bidirectional DC/DC Converter) on page 39**
  Starting from SAB, closed-form power relations are obtained in DCM/CCM and used to build the AB-DC/DC framework. A probabilistic treatment shows passive power sharing is highly sensitive to magnetic tolerances; a new active power-sharing and a hybrid modulation are proposed, validated by large-scale PLECS studies (30k runs) and experiments on a 200 W prototype, achieving controlled redistribution and reduced thermal stress.
- **Chapter 4 (Series Resonant DC Transformer) on page 71**
  An SRC operated as DCX is studied with emphasis on restoring power regulation with $\Sigma\Delta$ cycle-skipping modulation; ZVS/output voltage ripple relations and hardware design guidlines of SRC-DCX are presented together with 1 kW prototypes. Input-parallel and output-parallel operation are demonstrated with current sharing control under the closed-loop, achieving high efficiency (near 98%) and robust modular scalability.
- **Chapter 5 (Conclusion and Future Research) on page 97**
  The concluding chapter provides a review of the contributions made in each chapter and outlines future research directions. Appendix closes the main body of the thesis with the PLECS simulation script of the parameter sweep analysis carried out in Chapter 3.

Zero-Voltage Switching Analysis of Conventional and Current-Fed DAB Converters

2

Abstract

This chapter is divided into two parts, each focused on analysing the ZVS conditions of DAB converters. In the first part, the analysis is conducted on a conventional DAB converter, with auxiliary inductors placed between the legs of the input or output H-bridges. Analytical models are developed to determine the ZVS boundary conditions and the associated switch current root-mean-square (RMS) values. These models provide insight into the trade-offs between extended ZVS regions and increased conduction losses. The analysis is validated through PLECS simulations and supported by experimental results from a 300 W prototype in the output-side auxiliary configuration. Additionally, an efficiency comparison between the conventional and auxiliary inductor cases is carried out, highlighting the practical benefits and limitations of this approach. The second part of the chapter extends the ZVS analysis to the CF-DAB architecture featuring interleaved inductors on the secondary side. The presence of zero or nonzero DC offset in the interleaved currents, arising from bipolar or unipolar grid configurations, is shown to affect the ZVS behavior significantly. Analytical expressions are derived for both offset scenarios, distinguishing between full and partial ZVS operation. Numerical simulations under worst-case conditions confirm the feasibility of the proposed ZVS boundary analysis with the help of instantaneous switch currents, while experimental validation is provided to determine the operating behavior of the converter in balanced and unbalanced load conditions, depicting no DC offset and DC offset currents in the interphase inductors. Together, these studies offer comprehensive guidelines for designing high-efficiency, soft-switching conventional and current-fed DAB converters across a range of operating conditions.

2.1 Literature Review on Enhancement of ZVS in DAB Converter 15
2.2 Background on DAB Operation 17
2.2.1 Ideal Boundary Conditions of the ZVS Region . 18
2.2.2 Dead Time and Parasitic Capacitance Effects on ZVS 18
2.3 ZVS Extension with Auxiliary Inductors . . . 20
2.3.1 Auxiliary Inductor on the Input Side of the DAB . . 20
2.3.2 Auxiliary Inductor on the Output Side of the DAB . 21
2.3.3 Evaluation of Switch Current RMS 22
2.3.4 Numerical Validations . . 25
2.3.5 Experimental Validations 26
2.4 Current-Fed Dual-Active-Bridge Converter 30
2.5 Working Principle of an Interleaved CF-DAB . . . 30
2.5.1 ZVS Analysis without the DC Offset Case 31
2.5.2 ZVS Analysis with the DC Offset Case 32
2.5.3 Numerical Validations . . 34
2.5.4 Experimental Validations 36
2.6 Summary 38

2.1 Literature Review on Enhancement of ZVS in DAB Converter

Among various isolated DC-DC converter topologies, the DAB configuration is one of the most widely adopted, owing to its ability to operate under soft-switching conditions, support full bidirectional power flow, and provide galvanic isolation. These features make DAB converters particularly suitable for applications such as electric vehicle (EV) on-board and off-board chargers, smart transformers, DC microgrids, and grid integration [53].

DAB converters typically achieve high efficiency by enabling ZVS during turn-on transitions, which significantly reduces switching losses. However, under wide output voltage variations and light-load conditions, ZVS is no longer guaranteed, leading to hard-switching behavior and increased losses [54]. To improve light-load efficiency and extend the ZVS operating range, various research efforts have focused on modifying the

magnetic components of the power stage. In [55]–[59], the magnetizing inductance of the high-frequency (HF) transformer is utilized to inject magnetizing current, thereby enabling ZVS across a wider load range. While effective in enhancing ZVS, this approach reduces transformer coupling, negatively affecting power transfer capability and increasing conduction losses.

As an alternative to modifying the transformer design, several works have explored the addition of auxiliary inductors or circuits [60]–[62]. For example, [60] introduces coupled inductors into the low-voltage-side full bridges of a parallel DAB structure to maintain soft-switching. Other works [61], [62] retain the classical single-phase DAB topology but incorporate a switched auxiliary inductor, requiring an additional modulation strategy to control the auxiliary switches.

Although the role of auxiliary inductors in enlarging the ZVS region has been well documented, their impact on converter performance, particularly in terms of switch RMS currents near the ZVS boundary, has not been fully explored. It is evident that adding an additional inductive component can increase the RMS current through the switches. This increase may lead to higher conduction losses, introducing a trade-off between reduced switching losses and increased conduction losses that requires careful evaluation.

Therefore, rather than introducing a new converter topology, this study investigates these less-addressed aspects of auxiliary inductor-based ZVS enhancement. Specifically, the analysis focuses on the placement of auxiliary inductors on both the input and output bridges of a conventional DAB converter. While existing studies primarily focus on the input side, a detailed analysis of ZVS behavior on the output bridge is largely absent. To address this gap, this chapter presents separate evaluations for both the input and output sides of the converter. This distinction is particularly relevant for applications such as integrated AC-DC systems, where interleaved inductors are used, for midpoint neutral formation, as proposed in [63]. Moreover, the insights from this analysis are applicable to the CF-DAB topology, which will be discussed in the subsequent sections [1].

Additionally, the switch current RMS values are derived and analyzed to quantify the conduction losses in each case. Due to its simplicity and practical relevance, a single phase-shift (SPS) modulation scheme is employed throughout the analysis to characterize the converter's behavior near the ZVS boundary.

The following sections are organized as follows: Section 2.2 provides background on the DAB converter along with the current state-of-the-art in ZVS analysis. Section 2.3 presents a discussion on the benefits of incorporating auxiliary inductors in both the input and output H-bridges of the DAB. Subsection 2.3.3 focuses on the evaluation of the switch current RMS under various operating conditions. Subsection 2.3.4 presents the numerical validation of the auxiliary inductor-based DAB for selected working points, as well as experimental verification of ZVS performance with and without auxiliary inductors in Subection 2.3.5.

1: The current literature review and the following sections focus on ZVS improvements in the conventional DAB converter through the use of auxiliary inductors, applicable to various DC microgrid scenarios. However, starting from Section 2.4, the discussion shifts to the CF-DAB converter, which is specifically suited for bipolar and unipolar configurations in DC microgrids.

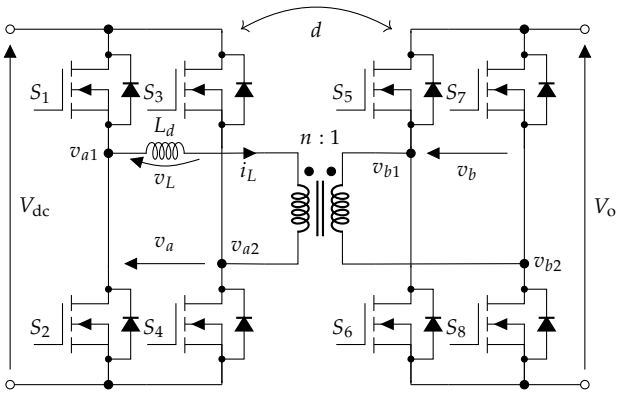


Figure 2.1: Dual-active-bridge converter.

2.2 Background on DAB Operation

Fig. 2.1 depicts the DAB converter consisting of two symmetrical active bridges connected by an HF transformer with a $n:1$ turns ratio. The two H-bridges (input and output bridges) allow full bidirectional power transfer, while the HF transformer enables galvanic isolation with reduced size, weight, volume, and cost. The leakage inductances L_d acts as an energy storage device, favoring soft-switching operation conditions. The simplest way to control the converter is to provide a phase-shift d between the two square wave voltages v_a and v_b (i.e., duty cycle $\delta = 0.5$), with the switching period serving as the normalization base. Being v_a and v_b periodic waveforms (with amplitudes V_a and V_b, respectively), the phase-shift can be limited to $-0.25 \leq d \leq +0.25$, where phase shift polarity determines the polarity of the power flow. This simple control technique is referred to as the well-known SPS control.

Note

In this chapter, the parameter d represents the phase-shift between the two H-bridges.

DAB can also be controlled by other modulation techniques such as, EPS, DPS, and TPS, detailed in [43]. Compared to the SPS, the other modulation techniques increase the degree of freedom, which optimizes the converter's performance. However, these modulations leads to complex calculation and lose the benefit of easy implementation, which is preferred by the industries. Therefore, SPS technique, having a sole degree of freedom, is selected and studied for the performance enhancements of the DAB converter.

Fig. 2.2 shows the leakage inductance current in a general case ($V_\mathrm{dc} \neq V_\mathrm{o}$) over half of the switching period T_sw. Thanks to topology and modulation symmetry, the leakage inductor current i_L can be deduced over a half period and can be solved for two different states $0 < t < dT_\mathrm{sw}$ and $dT_\mathrm{sw} < t < T_\mathrm{sw}/2$. The current through the leakage inductance i_L is:

$$i_\mathrm{L} = \frac{1}{L_\mathrm{d}} \int_0^{T_\mathrm{sw}} v_\mathrm{L} dt. \tag{2.1}$$

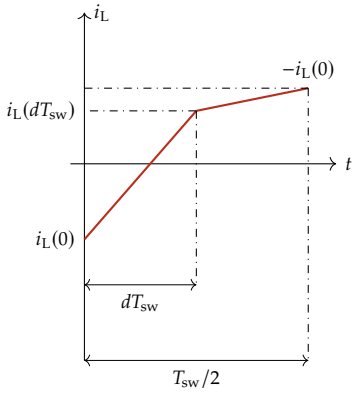


Figure 2.2: Leakage inductor current over half of the switching period T_sw.

where, v_L is the voltage across the inductor and can be defined in terms of the HF transformer primary v_a and secondary v_b voltages.

Using the i_L representation shown in Fig. 2.1 and referring all parameters to the primary side of the transformer, (2.1) can be solved over two different states of the converter as follows:

$$i_\mathrm{L}(0) + i_\mathrm{L}(dT_\mathrm{sw}) = \frac{V_\mathrm{a} + nV_\mathrm{b}}{L_\mathrm{d}} dT_\mathrm{sw}, \quad (0 < t \leq dT_\mathrm{sw}), \tag{2.2}$$

$$i_{\mathrm{L}}(0) - i_{\mathrm{L}}(dT_{\mathrm{sw}}) = \frac{V_{\mathrm{a}} - nV_{\mathrm{b}}}{L_{\mathrm{d}}}(1-d)T_{\mathrm{sw}}, \quad (dT_{\mathrm{sw}} < t \leq T). \tag{2.3}$$

Solving (2.2) and (2.3), one can obtain $i_{\mathrm{L}}(0)$ and $i_{\mathrm{L}}(dT_{\mathrm{sw}})$ at possible instants $t = 0$ and $t = dT_{\mathrm{sw}}$ as:

$$i_{\mathrm{L}}(0) = \frac{V_{\mathrm{a}}}{4f_{\mathrm{sw}}L_{\mathrm{d}}}[G(1-4d) - 1]\,, \tag{2.4}$$

$$i_{\mathrm{L}}(dT_{\mathrm{sw}}) = \frac{V_{\mathrm{a}}}{4f_{\mathrm{sw}}L_{\mathrm{d}}}[G + 4d - 1]\,, \tag{2.5}$$

having switching frequency f_{sw} and voltage gain $G = nV_{\mathrm{b}}/V_{\mathrm{a}}$.

2.2.1 Ideal Boundary Conditions of the ZVS Region

Note

In this chapter, the parameter G represents the voltage-gain ratio between the output and input.

The ZVS condition is fundamentally triggered when, during turn-on intervals, the anti-parallel diode enters in conduction before the switch. This effectively eliminates turn-on switching losses by exposing the switch to the diode forward voltage rather than the full V_{dc} shortly before its conduction. This condition translates into having $i_{\mathrm{L}}(0) \leq 0$ for the input bridge and $i_{\mathrm{L}}(dT_{\mathrm{sw}}) \geq 0$ for the output bridge. In light of (2.4) and (2.5), the following boundary conditions of the ZVS region can be determined for both input and output bridges:

$$G \leq \frac{1}{1-4d}\,, \tag{2.6}$$

$$G \geq 1 - 4d\,. \tag{2.7}$$

From (2.6) and (2.7) it is clear that at any moment at least one bridge is working under the ZVS commutation. When both conditions are met, a complete soft-switching turn-on action can be achieved. From Fig. 2.3(a), the shaded region in case $G < 1$ refers to the input ZVS, i.e., all the switches on the input side work under the ZVS and on contrary, the $G > 1$ refers to the output ZVS. The left over area labeled as ZVS represents conditions in which both the input and output side power switches work under the ZVS region. It stands out that only in the case of $G = 1$ it is possible to achieve full-load ZVS (FL-ZVS) at any value of d; Hence, the majority of applications (e.g., smart transformers) are based on the choice of the transformer ratio n such as to ensure $G \approx 1$.

2.2.2 Dead Time and Parasitic Capacitance Effects on ZVS

It should be noted that the effect of parasitic capacitance modifies (2.6) and (2.7), resulting in relevant effects in ultra-low and high voltage ratio conditions. To achieve FL ZVS, the energy stored in the leakage inductor must be greater than the energy stored in the parasitic capacitances [64] according to the condition

$$\frac{1}{2}L_{\mathrm{d}}i_{\mathrm{L}}^2 \geq N\frac{1}{2}C_{\mathrm{eq}}V_{\mathrm{c}}^2\,, \tag{2.8}$$

where, N represents the number of switching devices, C_{eq} is the equivalent parasitic capacitance of switching devices, V_{c} is either V_{a} or V_{b}, i_{L} may be $i_{\mathrm{L}}(0)$ or $i_{\mathrm{L}}(dT_{\mathrm{sw}})$ of input and output bridges in which the ZVS condition is evaluated. The easiest approach to estimate the equivalent

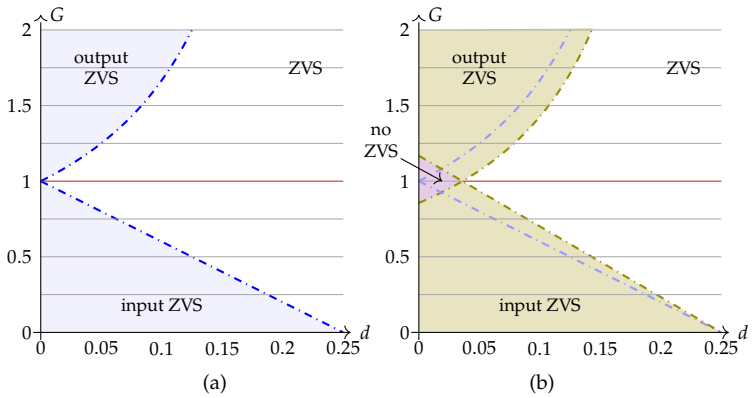


Figure 2.3: ZVS region in the $G-d$ plane: (a) ideal case; (b) parasitic capacitance effect.

capacitance is by considering it as the output parasitic capacitance value of the MOSFETs (C_{oss}) at a certain voltage.

Based on the condition on stored energy given in (2.8), the ideal ZVS boundary conditions defined in (2.6) and (2.7) are modified as:

$$\begin{cases} G \leq \dfrac{1-8f_{sw}\sqrt{C_{eq}L}}{1-4d} \\ G \geq \dfrac{1-4d}{1-8f_{sw}\sqrt{C_{eq}L}} \end{cases} . \tag{2.9}$$

Equation (2.9) tells that the boundary conditions not only depend on G and d, but also depend on the converter switching frequency, leakage inductance, and the parasitic capacitance of the power switches. Fig. 2.3(b) shows the effect of the parasitic capacitance on the ZVS boundary conditions, slightly narrowing the ideal ZVS region (whose edge is indicated by the brown lines). As a result, a no-ZVS region appears at light-loads, where both input and output bridges lose their soft-switching capability even in $G = 1$ case. It can be noticed that, if the parasitic capacitance effect can be neglected, the boundary conditions shown in (2.9) return to the ideal conditions represented in (2.6) and (2.7).

To achieve ZVS conditions, considerations on the dead time effect are also essential. The dead time should be consider in such a way that the parasitic capacitance must complete charging within the time zone. If the dead time period is too short, the converter might lose the ZVS. The minimal duration of dead time required for parasitic capacitance charging is [65]

$$t_d = \frac{2V_c^2 C_{eq}}{i_L} . \tag{2.10}$$

Dead time and parasitic capacitances often do not significantly alter the ZVS region's extent. Instead, acting in the ZVS region's border, i.e., a working point specifically examined in this article, may have a discernible effect. Yet, considering the predominant impact of the DC bus voltage variations, operating at this point is by no means trivial. In fact, the converter is often operated with a specific margin distance from the ZVS boundary to assure the ZVS commutation. Consequently, the effects of parasitic capacitances and dead time were neglected in the analytical formulations for understanding the behavior of the DAB at the ZVS boundary in terms of power losses.

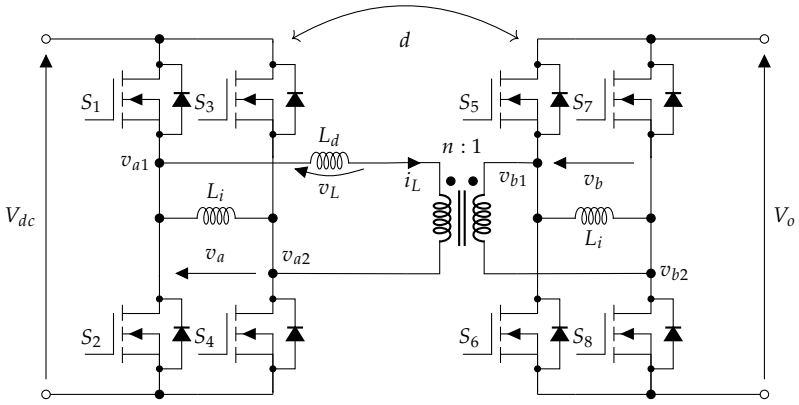


Figure 2.4: Dual-active-bridge converter with auxiliary inductors.

2.3 ZVS Extension with Auxiliary Inductors

As previously stated, the FL ZVS can be achieved by optimizing the transformer turns ratio n and maintaining $G = 1$ at any value of d. However, in real applications, it is not always possible to maintain a constant $G = 1$. The slight variation in G under light load conditions (i.e., low value of d) may prevent at least one of the converter H-bridges from achieving ZVS conditions. This issue could be addressed simply by adding an auxiliary inductor between the legs of either the input or output bridge, according to the DAB operation. By making, the ZVS region could expand and allow the converter to operate under the ZVS condition for any value of d. The DAB converter architecture with the auxiliary inductor L_i on both bridges is depicted in Fig. 2.4. Since in any of $G < 1$ or $G > 1$ cases, at least one bridge is operating under ZVS region, a separate study can be performed based on the ZVS requirement either for the input or the output bridge.

2.3.1 Auxiliary Inductor on the Input Side of the DAB

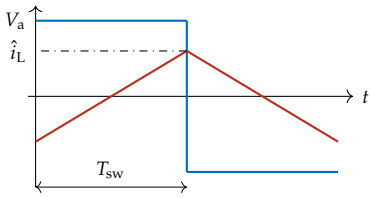


Figure 2.5: Voltage and current waveforms of an auxiliary inductor at the input side.

Let's consider Fig. 2.4, having an auxiliary inductor only on the input bridge. Fig. 2.5, shows the voltage and current waveforms of the inductor L_i over half of the switching period T_sw. The peak amplitude of the triangular ripple current through L_i can be formulated as:

$$\hat{i}_\mathrm{L} = \frac{V_\mathrm{a}}{4 f_\mathrm{sw} L_\mathrm{i}} \,. \tag{2.11}$$

On applying Kirchhoff's Current Law (KCL), the leakage inductor current of the input bridge $i_\mathrm{L}(0)$ defined in (2.4) modifies as:

$$i_\mathrm{L}(0) = \frac{V_\mathrm{a}}{4 f_\mathrm{sw} L_\mathrm{d}} [G(4d-1)+1] - \frac{V_\mathrm{a}}{4 f_\mathrm{sw} L_\mathrm{i}} \,, \tag{2.12}$$

that, by setting $\beta = L_\mathrm{i}/L_\mathrm{d}$, leads to the following ZVS criterion:

$$G \leq \frac{1}{1-4d} \frac{1+\beta}{\beta} \,, \tag{2.13}$$

thus, effectively enlarging the ZVS region to

$$\Delta G_{\mathrm{i}} = G - 1 = \frac{1}{\beta}\,, \tag{2.14}$$

where, ΔG_{i} represents the input bridge ZVS extension.

2.3.2 Auxiliary Inductor on the Output Side of the DAB

Similarly to the input side analysis, the effect of the auxiliary inductor can be depicted on the output side of the converter. Fig. 2.6, shows the voltage and current waveforms of an auxiliary inductor L_{i} over half of the switching period T_{sw}. The peak amplitude of the triangular ripple current through L_{i} can be formulated as:

$$\hat{i}_{\mathrm{L}} = \frac{nV_{\mathrm{b}}}{4f_{\mathrm{sw}}L_{\mathrm{i}}}\,. \tag{2.15}$$

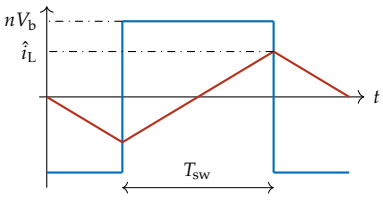


Figure 2.6: Voltage and current waveforms of an auxiliary inductor at the output side.

On applying KCL, the leakage inductor current of the output bridge $i_{\mathrm{L}}(dT_{\mathrm{sw}})$ defined in (2.5) modifies as:

$$i_{\mathrm{L}}(dT_{\mathrm{sw}}) = \frac{V_{\mathrm{a}}}{4f_{\mathrm{sw}}L_{\mathrm{d}}}[G + 4d - 1] + \frac{nV_{\mathrm{b}}}{4f_{\mathrm{sw}}L_{\mathrm{i}}}\,, \tag{2.16}$$

that by considering the same parameter $\beta = L_{\mathrm{i}}/L_{\mathrm{d}}$, the output side leads to the following ZVS criterion:

$$G \geq (1 - 4d)\frac{\beta}{1+\beta}\,, \tag{2.17}$$

thus, effectively enlarging ZVS region to

$$\Delta G_{\mathrm{o}} = 1 - G = \frac{1}{1+\beta}\,, \tag{2.18}$$

where, ΔG_{o} represents the output bridge ZVS extension.

Fig. 2.7 shows the extended region of ZVS for different cases of β. When the ΔG_{i} increases, the output side ZVS boundary condition shifts up, reducing the area of the output ZVS. When the ΔG_{o} is increasing, the input ZVS area reduces at the low power region (lower d value), keeping the maximum d at a fixed position. In both cases, the FL ZVS region is extended. Nevertheless, the ZVS condition resembles with the one

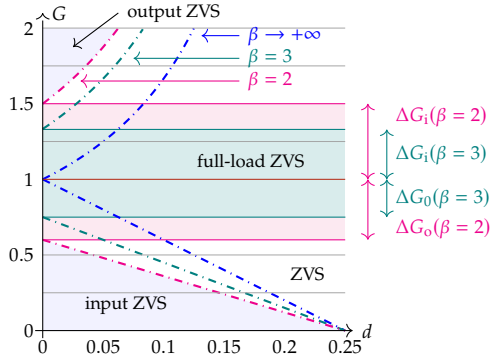


Figure 2.7: ZVS extension on the input and output sides of the DAB.

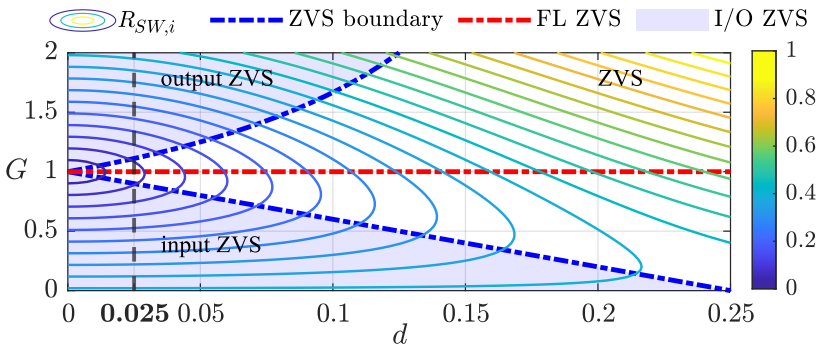


Figure 2.8: Contour plots of the normalized switch current RMS of the input H-bridge for $\beta \to +\infty$.

of conventional SPS in the case of $\beta \to +\infty$. It should be noted that this effect is similar to that introduced by HF transformer magnetizing current, whose light-load enhancing behavior has already been used in reduced coupling transformers [57].

2.3.3 Evaluation of Switch Current RMS

The choice of G and β parameters that allows achieving ZVS for all of the switches under light-load conditions, does not guarantee to operate under the lowest loss conditions for the entire conversion stage. Indeed, the RMS value of the switch currents can change depending on these same parameters then resulting in higher or lower conduction losses. Therefore, the switch current RMS for three different cases are discussed in this section. For simplifying the analysis, the switch currents have been normalized with respect to the base current defined as

$$I_{\text{base}} = \frac{V_{\text{a}}}{4 f_{\text{sw}} L_{\text{d}}} \,. \tag{2.19}$$

The first case refer to the RMS calculation of the input side switch currents in a typical DAB without an auxiliary inductor ($\beta \to +\infty$), i.e., $R_{\text{SW,i}}$. The other two cases refer to the RMS calculation in the auxiliary inductor located on either the input (R_{i}) or output side (R_{o}) of the DAB. Thanks to the circuit symmetry, the $R_{\text{SW,i}}$ evaluation can be restricted to a single switch on the converter's input H-bridge. Its value is put in relation to G and d through

$$R_{\text{SW,i}} = \sqrt{\frac{1 - 2(1 - 24d^2 + 32d^3)G + G^2}{6}} \,, \tag{2.20}$$

whereas the switch current RMS of the output H-bridge $R_{\text{SW,o}}$ can be obtained simply by using the transformer turn's ratio n as:

$$R_{\text{SW,o}} = n R_{\text{SW,i}} \,. \tag{2.21}$$

The RMS of the leakage inductor current can be simply obtained by with the multiplication of $\sqrt{2}$ to the R_{SW}. A visual representation derived from (2.20) is provided through the graph in Fig. 2.8. In both $G > 1$ and $G < 1$ cases, the contour lines of the current RMSs are having a similar trend in light-load operating conditions, and lower RMS values can be observed at $G = 1$. For example, $d = 0.025$ load line shows the behavior of RMS contour lines for different G values. As the load increases, the $G = 1$ case no longer maintains the lower RMS values, but the gradient of the current

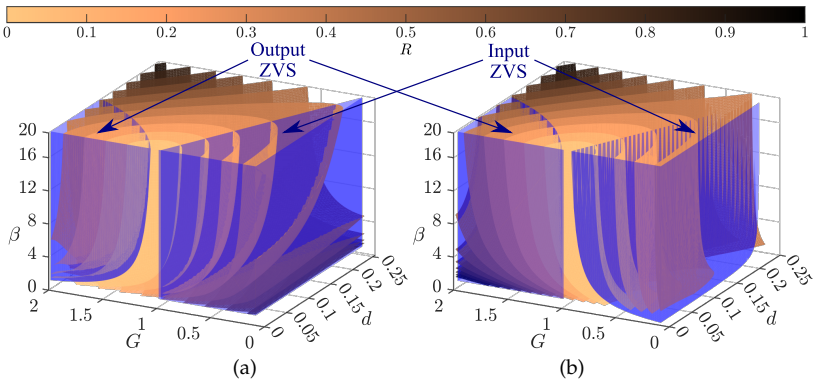


Figure 2.9: Isosurfaces of the normalized switch current RMS in auxiliary inductor case: (a) input bridge; (b) output bridge.

RMS isolines follows the output ZVS boundary. As well known, for higher d and G values, the current RMS reaches the highest value, leading to higher conduction losses.

Similarly, in presence of the auxiliary inductor and according to the bridge in which it is connected, R_i and R_o have been assessed separately and they are evaluated as

$$\begin{aligned} R_\mathrm{i} &= \sqrt{\left(R_{SW,i}^2 + \frac{1}{6\beta}\right)\left(1+\frac{1}{\beta}\right) - \frac{G^2}{6\beta}} \\ R_\mathrm{o} &= \sqrt{\left(R_{SW,o}^2 + \frac{G^2}{6\beta}\right)\left(1+\frac{1}{\beta}\right) - \frac{1}{6\beta}}\,. \end{aligned} \tag{2.22}$$

The dependency from G, β, and d shown in (2.22) is displayed in terms of switch current RMS (R) isosurfaces in Fig. 2.9 for input (a) and output (b) bridges. It is clear that for higher β values, the ZVS region becomes narrow and it tends toward the conventional SPS case where β reaches $+\infty$, whereas, for lower β values, a sensible increase in ZVS region can be seen. For a better understanding, the 2D contour plots are shown in Fig. 2.10 and Fig. 2.11 for the input and output H-bridges at particular G and β values, respectively.

The input side analysis is made by considering $G = 1.2$ and $\beta = 5$. The $G = 1.2$ confirms that the input bridge loses ZVS capability, whereas the output bridge is within the ZVS region. By adding the auxiliary inductor on the input side, the ZVS region could enlarge, making all the switches work under the ZVS. By choosing a lower inductor value, i.e., lower β value, the ZVS region can be widely extended, as visible in Fig. 2.9. Having such a wide ZVS region could be beneficial in reducing switching losses. However, it is crucial to analyze the current RMS in that region to have an overall idea of the converter behavior. Fig. 2.10 depicts the extended ZVS region and the current RMS contour plots in $G - d$ and $\beta - d$ planes.

In $G - d$ plot, the lower RMS can be seen in the FL ZVS region, but if the voltage gain is too high, the FL ZVS can be achieved with the lower inductance value increasing the current RMS due to the predominant effect of the current ripple that leads to higher conduction losses. A similar analysis can be drawn from the $\beta - d$ plot, where β is calculated as per (2.14) for $G = 1.2$ and $d = 0$ (no-load). $\beta = 5$ identifies the FL ZVS boundary condition, but it also represents a threshold for lower current RMS values. Indeed, when $\beta < 5$, the operation is ensured within the FL ZVS region, although the auxiliary inductance value is low enough to

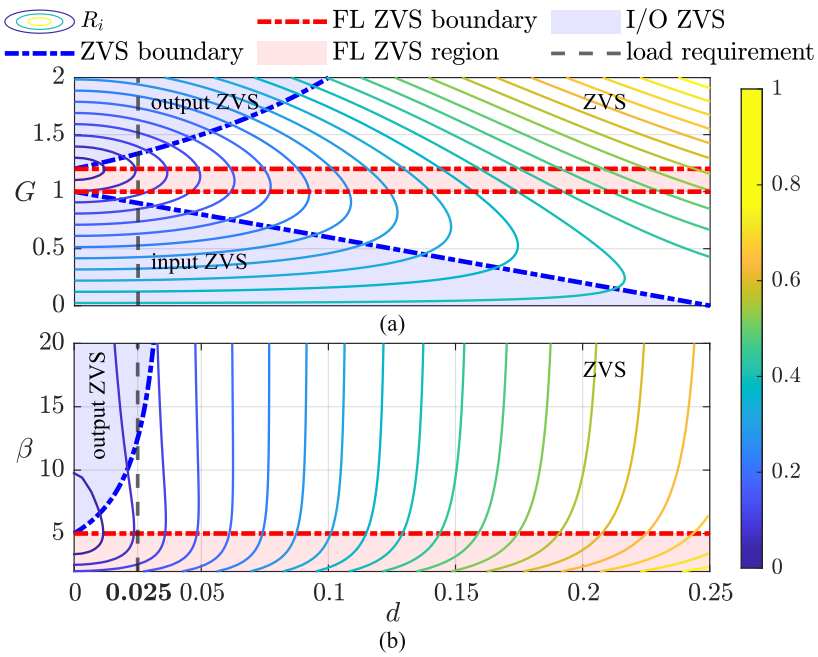


Figure 2.10: Contour plots of the input side normalized switch current RMS: (a) $\beta = 5$; (b) $G = 1.2$.

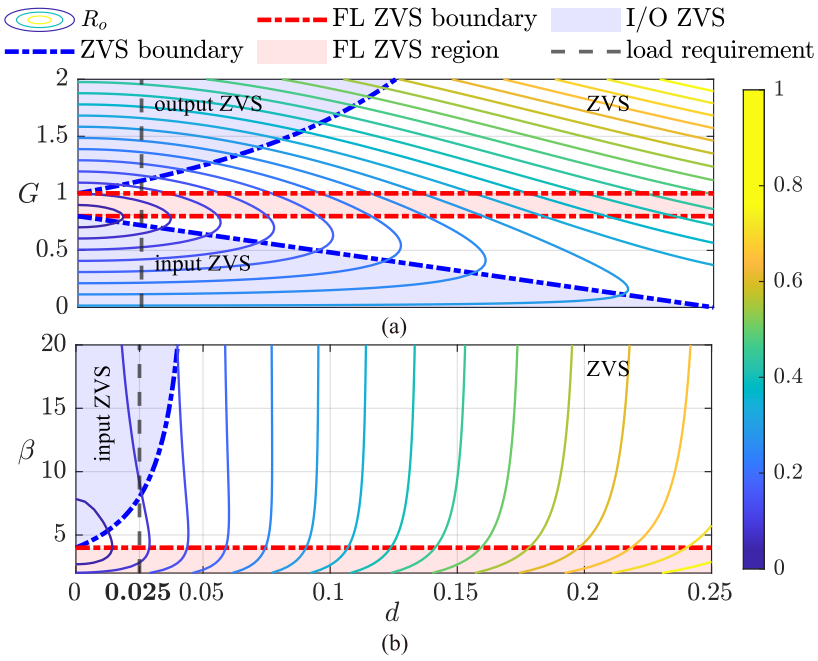


Figure 2.11: Contour plots of the output side normalized switch current RMS: (a) $\beta = 4$; (b) $G = 0.8$.

compromise the conduction losses. In this case, the current RMS values are higher, as depicted in $G - d$ plot. Given a specific load requirement, i.e., fixing d, and the corresponding value of β determined at the ZVS boundary (β_{BC}), the ZVS condition is ensured in the interval $5 < \beta < \beta_{BC}$. Within the latter interval, the current RMS is lower towards $\beta = 5$, while it is higher towards $\beta = \beta_{BC}$. In conclusion, these plots suggest that it is possible to design the auxiliary inductor based on (2.14) with a view to provide both ZVS commutation and lower current RMS values.

The output side analysis is made by considering $G = 0.8$ and $\beta = 4$, where β is calculated as per (2.18). The $G = 0.8$ confirms that the input bridge is within the ZVS region, whereas the output bridge loses the ZVS capability. By adding the auxiliary inductor on the output side, the ZVS region could enlarge, making all the switches work under the ZVS. Contrary to the input side analysis, the wide ZVS region appears when

the G is reducing. Fig. 2.11 depicts the extended ZVS region and the current RMS contour plots in $G-d$ and $\beta-d$ planes. The discussion made for the input side is valid for the output side analysis. For any $G<1$ value, it is possible to design the auxiliary inductor based on (2.18) with a view to provide both ZVS commutation and lower current RMS values. It is worth noticing that, for higher d values, the current RMS values are lower in the typical DAB than the auxiliary inductor-based DAB. To understand the latter statement, one should imagine the $\beta-d$ plot with more RMS isolines and β tending towards the $+\infty$. Hence, in many pieces of literature, these auxiliary inductors are usually controlled with an additional switch based on the output power [61], [62].

2.3.4 Numerical Validations

The topology depicted in Fig. 2.4 has been simulated on PLECS (Plexim GmbH) environment to validate the analytical results. Switch parameters have been extracted from AIMW120R060M1H SiC MOSFET and IDW40G120C5B SiC Schottky diode (Infineon Technologies AG) datasheets. Main parameters adopted values are reported in Table 2.1. Since adding an auxiliary inductor to the DAB is mostly benefited in the light-load conditions, the phase-shift d is chosen as 0.025 (5% of the rated power) for the simulation purposes. The same design parameters (G and d) chosen for switch current RMS evaluation in section 2.3.3 are considered here. With $G=1.2$, the input side analysis is carried out for three β cases. The $\beta\rightarrow+\infty$ case represents the absence of auxiliary inductors and no-ZVS condition for the input bridge. In presence of auxiliary inductor, $\beta=12.5$ and $\beta=5$ represent the ZVS boundary and FL ZVS boundary conditions (see Fig. 2.10) calculated using (2.13) and (2.14), respectively. Similarly for the output bridge, with $G=0.8$, three β cases are evaluated. The $\beta\rightarrow+\infty$ represents the no auxiliary inductor and no-ZVS condition for output bridge; and in presence of auxliary inductor, $\beta=8$, and $\beta=4$ represent the ZVS boundary and FL ZVS boundary conditions (see Fig. 2.11) calculated using (2.17) and (2.18), respectively. Based on these parameters, the switch current RMS is calculated using (2.20) and (2.22) and compared with the simulation results. As confirmed by the relative error ε_r in Table 2.2, numerical validations are in good agreement with the analytical formulations. Fig. 2.12 depicts the input side switch current, corresponding RMS value and commutation trajectory for three β cases considered in Table 2.2. The commutation trajectory shows both turn-on (ON) and turn-off (OFF) commutations for one switching period, depicting both hard-switching (HS) and soft-switching paths. As one may see, the $\beta\rightarrow+\infty$ case has no ZVS path, hence confirming the no-ZVS condition. On the other hand, $\beta=12.5$ case has both ZVS during

Parameter	Symbol	Value	Unit
Input voltage	V_{dc}	800	V
Output voltage	V_{o}	GV_{in}	V
Leakage Inductance	L_{d}	80	μH
Auxiliary Inductance	L_{i}	βL_{d}	μH
Switching frequency	f_{sw}	40	kHz
Switching period	T_{sw}	25	μs
Dead time	t_{d}	0.05	μs

Table 2.1: Auxiliary inductor-based DAB numerical plant main system parameters.

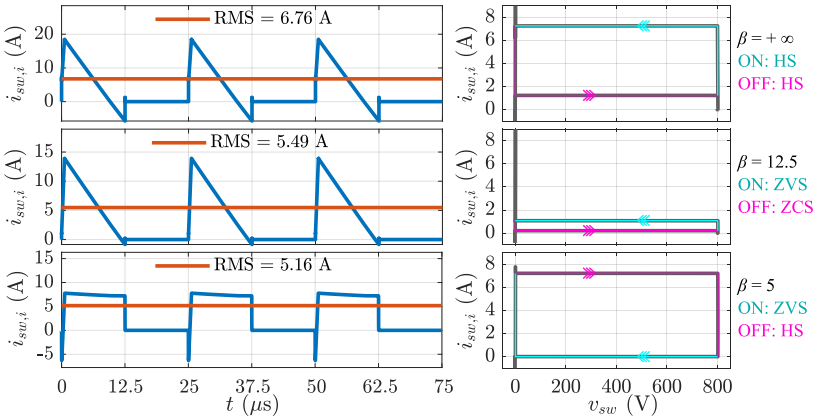


Figure 2.12: Input bridge current and commutation trajectory for three β cases.

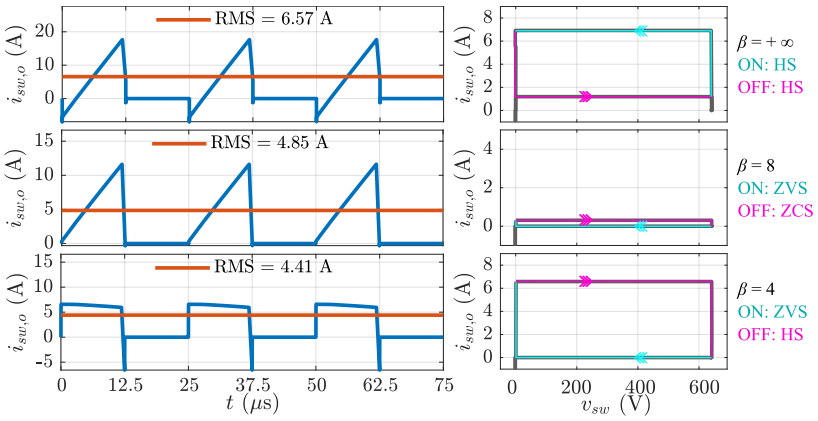


Figure 2.13: Output bridge current and commutation trajectory for three β cases.

turn-on and zero current switching (ZCS) during turn-off, resulting in a substantial reduction of the device switching losses. Indeed, operating on the boundary condition (2.13) leads to ZCS turn-off. This is similar to the triangular/trapezoidal modulation techniques, which allow for both ZVS and ZCS commutations [61]. However, in $\beta = 12.5$ case, the switch current RMS is higher than the $\beta = 5$ case, where there is only ZVS turn-on.

Similarly, Fig. 2.13 shows the output side switch current, associated RMS value, and commutation trajectory for three different β cases. As visible, the simulation results validate the previous discussion. Operating in the boundary condition (2.17), i.e., featuring both ZVS and ZCS commutation, the area below the commutation trajectory (i.e., switching losses) should be nearly zero. However, because of the inevitable non-ideality effects discussed in section 2.2.2, such as those due to dead time and parasitic capacitances, a non-negligible area can be seen in the commutation trajectory depicted in Fig. 2.12 and Fig. 2.13. Since the area is small, the switching losses will be comparatively lower than in the other ZVS cases. As a result, even without considering the non-ideality effects, the developed analytical analysis is far more relevant to the simulation results. The following section provides experimental validation of the ZVS-region expansion enabled by the auxiliary inductor.

2.3.5 Experimental Validations

The experimental validation has been conducted using a scale-down of 300 W prototype shown in Fig. 2.14, with parameters listed in Table 2.3. The corresponding gate pulses were generated using the STM32G474RE microcontroller. All experimental results were obtained under open-loop control.

Cases	β	Analytical	Numerical	ε_r
I. Input bridge ($d = 0.025$, $G = 1.2$)	$+\infty$	6.97 A	6.76 A	−3.01 %
	12.5	5.81 A	5.49 A	−5.51 %
	5	5.21 A	5.16 A	−0.96 %
II. Output bridge ($d = 0.025$, $G = 0.8$)	$+\infty$	6.41 A	6.57 A	+2.45 %
	8	4.84 A	4.85 A	+0.21 %
	4	4.34 A	4.41 A	+1.61 %

Table 2.2: Analytical and numerical evaluation of switch current RMS.

An auxiliary inductor is connected between the two legs of the secondary-side switches, replicating the DAB behavior described in Section 2.3.2.

Figs. 2.15 and 2.16 present the experimental waveforms of the converter operating without the auxiliary inductor. In Fig. 2.15, the top plot shows the primary and secondary side voltages v_a and v_b of the transformer, while the bottom plot displays the corresponding leakage inductor current i_L. A small phase shift of $d = 0.05$ is introduced between v_a and v_b, with the voltage gain of $G = 0.5$. Under these conditions, the absence of the auxiliary inductor results in the loss of ZVS on the output bridge.

Fig. 2.16 shows the drain-source voltage v_{ds} and gate-source voltage v_{gs} waveforms for a single switch on the primary side S_1 (top) and secondary side S_5 (bottom), respectively. The switch labels are depicted in Fig. 2.4. Due to the symmetrical structure of the converter, only one switch per side is shown. It can be observed that the primary-side switch S_1 achieves ZVS, while the secondary-side switch S_5 fails to do so, as seen during

Parameter	Symbol	Value	Unit
Input voltage	V_{dc}	200	V
Output voltage	V_o	100	V
Voltage gain	G	0.5	-
Leakage Inductance	L_d	81.7	μH
Auxiliary Inductance	L_i	118.5	μH
Transformer magnetizing inductance	L_m	775	μH
Dead time	t_d	200	ns
HF tranformer turns ratio	n	28:28	-
Switching frequency	f_{sw}	100	kHz

Table 2.3: Auxiliary inductor-based DAB experimental setup parameters.

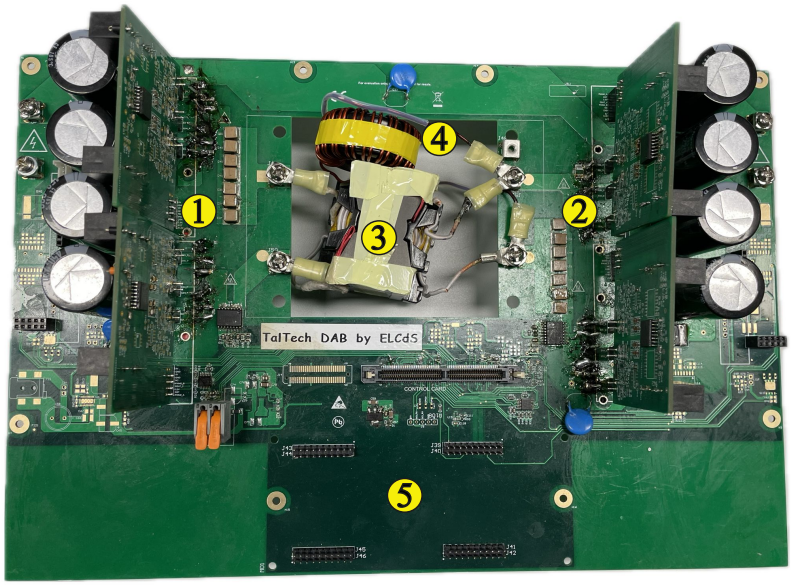


Figure 2.14: Experimental setup of auxiliary inductor-based DAB: (1) input bridge; (2) output bridge; (3) high-frequency transformer; (4) auxiliary inductor; (5) input pins for gate signals.

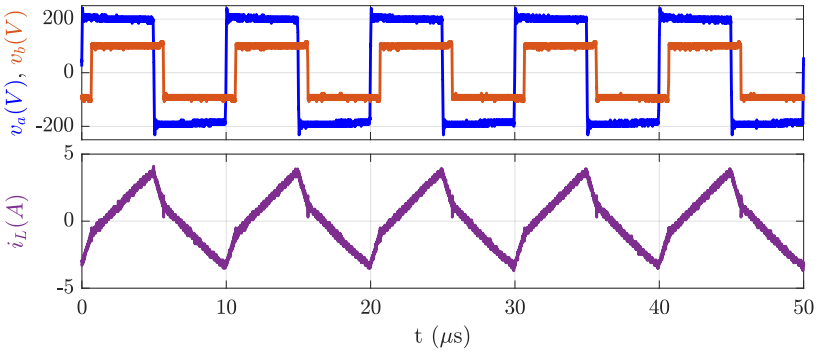


Figure 2.15: Primary and secondary side voltages (top) and the leakage current (bottom) of the transformer in case of conventional DAB.

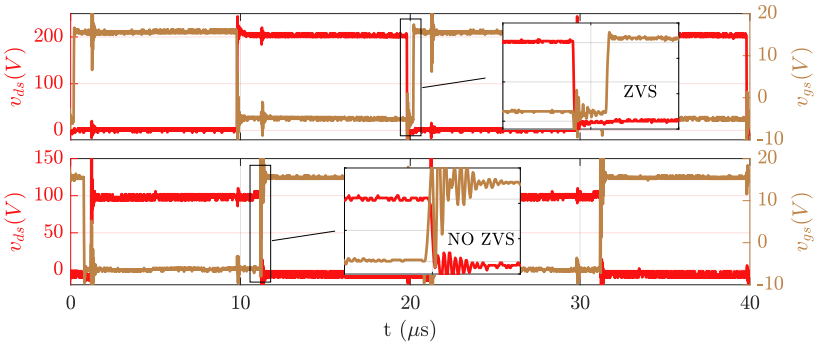


Figure 2.16: Drain-source voltage and gate source voltage: primary side switch S_1 (top) and secondary side switch S_5 (bottom) in case of conventional DAB.

the turn-on, the switch is exposed to maximum voltage V_o instead of zero voltage, which is clearly visible in Fig. 2.16 bottom zoomed plot. These results confirm the theoretical prediction that, under the given operating conditions, ZVS is not possible to achieve on the output bridge of a conventional DAB, particularly at light load.

Figs. 2.17 and 2.18 show the experimental results when an auxiliary inductor is introduced between the secondary-side legs. In Fig.2.17, the top and middle plots display the primary and secondary transformer voltages, v_a and v_b, along with the corresponding leakage inductor current i_L. The bottom plot presents the auxiliary inductor current i'_L. The converter is operated under the same conditions as in the no-auxiliary case; however, the introduction of the interphase inductor introduces the design parameter β.

In practice, the magnetizing inductance L_m of the transformer appears in parallel with the interphase inductor L_i, and those values are provided in Table 2.3. As a result, the total equivalent inductance is calculated to be 102.7 μH, leading to an effective $\beta = 1.25$, which satisfies the ZVS condition (2.17) for the output bridge operating under phase shift of $d = 0.05$ and voltage gain $G = 0.5$. The triangular shape of the auxiliary inductor current [2] i'_L confirms the theoretical prediction shown in Fig. 2.6.

2: The auxiliary inductor current exhibits zero average.

Fig. 2.18 displays the drain-source v_{ds} and gate-source v_{gs} voltages of the primary-side switch S_1 (top) and secondary-side switch S_5 (bottom). As seen in the zoomed view of the top plot, the input bridge continues to operate under ZVS, similar to the previous case. However, with the auxiliary inductor in place, ZVS is successfully achieved on the output bridge, as evidenced by the secondary-side switch S_5 turning on during the zero voltage. These results experimentally validate the theoretical analysis presented in Section 2.3, confirming that the auxiliary inductor effectively extends the ZVS region on the output bridge.

Furthermore, the efficiency of the converter operating with and without

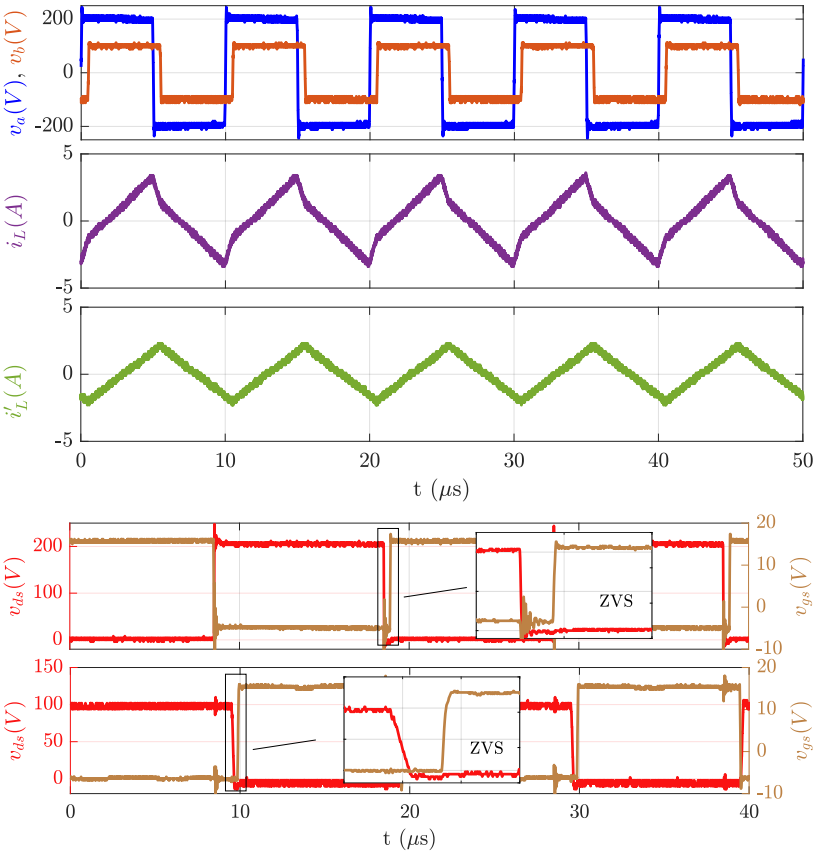


Figure 2.17: Primary and secondary side voltages (top), leakage current (middle) of the transformer, and auxiliary inductor current (bottom).

Figure 2.18: Drain-source voltage and gate source voltage: primary side switch S_1 (top) and secondary side switch S_5 (bottom) in case of auxiliary inductor based DAB.

the auxiliary inductor has been evaluated using a Yokogawa WT1800 power analyzer. As shown in Fig. 2.19, the dots represents the experimental data and the solid line is the interpolation curves achieved by using the following methodology outlined in [66]. The conventional DAB exhibits higher efficiency compared to the auxiliary inductor-based DAB. In general, efficiency reflects the combined effect of switching and conduction losses. While the inclusion of an auxiliary inductor enables soft-switching (ZVS) operation, it also introduces additional conduction losses due to higher RMS currents, which ultimately reduce the overall efficiency. As discussed in Section 2.3.3, a more effective approach is to control the connection of the auxiliary inductor using an additional switch, activated according to the output power level. This strategy enables achieving higher efficiency across the entire operating range.

Finally, the experimental results confirm that the addition of an auxiliary inductor to the conventional DAB extends the ZVS region under light-load conditions. However, in this scenario the efficiency of the auxiliary inductor-based DAB is lower compared to the conventional DAB, primarily due to increased conduction losses. The same methodology can be applied to

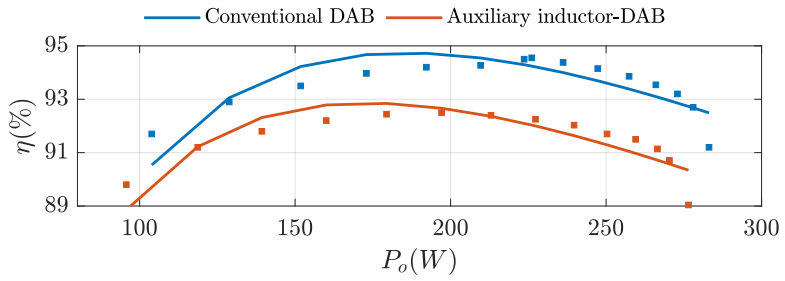


Figure 2.19: Efficiency of the DAB converter operating without and with auxiliary inductor.

investigate the ZVS performance of the CF-DAB, which will be discussed in the following sections, where the use of interphase inductors is unavoidable. In such cases, appropriate design guidelines, such as those outlined in [67], are essential to ensure efficiency improvements.

2.4 Current-Fed Dual-Active-Bridge Converter

A key challenge in advancing DC microgrids is the development of power electronic converters that can efficiently support both unipolar and bipolar systems while maintaining high reliability and cost-effectiveness, even under light-load and partial-load conditions. Wide conversion-ratio DC–DC converters are essential in meeting this need, as they ensure compatibility across diverse microgrid configurations and operating scenarios. In this regard, the authors in [68], [69] investigated an interleaved CF-DAB that supports both unipolar and bipolar outputs. While several studies have analyzed the ZVS behavior of CF-DAB converters [70]–[74], to the best of the authors' knowledge, a comprehensive ZVS analysis of the interleaved CF-DAB under SPS control has not yet been reported.

Therefore, the following sections present a detailed ZVS analysis of the interleaved CF-DAB operating under SPS modulation, with a particular focus on its application in both bipolar and unipolar DC microgrids. Section 2.5 describes the operation of the CF-DAB and provides analytical ZVS evaluation with and without DC offset for both bipolar and unipolar cases. Section 2.5.3 details the numerical validation of the proposed ZVS analysis, and Section 2.5.4 presents the experimental verification of the CF-DAB operating in both unipolar and bipolar configurations.

2.5 Working Principle of an Interleaved CF-DAB

The CF-DAB topology shown in Fig. 2.20 operates similarly to a conventional DAB under SPS control but includes two interphase inductors, L_1 and L_2, forming a two-leg interleaved buck structure on the secondary side. These inductors connect each converter leg's middle point to the split DC link, effectively distributing the output voltage across capacitors C_1 and C_2. In this work, both interphase inductors are assumed to be equal, i.e., $L_1 = L_2 = L$, allowing the output current I_o to split between the two legs. The output current that flows through the interleaved inductors is defined as $I_o = I_- - I_+$, where I_+ and I_- represent the currents flowing through the upper and lower DC rails, respectively, as shown

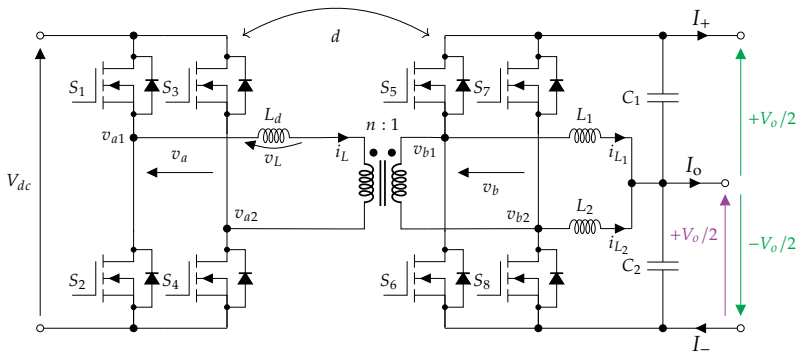


Figure 2.20: Interleaved current-fed dual-active-bridge converter.

in Fig. 2.20. This configuration supports a wide voltage gain due to the current-fed nature of the topology and is compatible with both unipolar and bipolar DC microgrids. In particular, bipolar grids utilize the $\pm V_o/2$ ports (indicated as green in Fig. 2.20), while unipolar grids connect to the $+V_o/2$ port (indicated as purple in Fig. 2.20).

In bipolar operation with balanced loads, the upper and lower DC rail currents are equal, $I_+ = I_-$, resulting in zero current at the midpoint, i.e., $I_o = 0$. Consequently, no DC offset appears in the interleaved inductor currents. However, under unbalanced conditions where $I_+ \neq I_-$, a net midpoint current arises, $I_o \neq 0$, introducing a DC offset in the interleaved inductors. Since both inductors are assumed equal ($L_1 = L_2 = L$), each inductor carries an offset of $I_o/2$. Whereas, in unipolar operation, if the load is connected between the midpoint and the lower DC rail, the upper DC rail current becomes zero ($I_+ = 0$), leading to $I_o = -I_-$. Conversely, if the load is connected between the upper DC rail and the midpoint, the lower DC rail current is zero ($I_- = 0$), resulting in $I_o = I_+$. In both cases, a nonzero DC offset current of either $+I_o$ or $-I_o$ flows through the interleaved inductors, depending on the load connection. Further, if the load is connected between the upper and lower DC rails, the middle point current becomes zero ($I_o = 0$), leading to zero DC offset case.

In summary, depending on the load conditions, the interphase inductors in the CF-DAB can exhibit either no DC offset or a positive/negative DC offset, in both bipolar and unipolar applications. Although the converter operates similarly to a conventional DAB, the presence of ripple due to switching actions and offset currents in the interphase inductors influences the conventional ZVS boundaries described in (2.6) and (2.7). Thus, by extending the same ZVS approach applied to the auxiliary inductor-based DAB, a detailed ZVS analysis of the CF-DAB under SPS control can be carried out, considering both zero and nonzero DC offset cases.

2.5.1 ZVS Analysis without the DC Offset Case

As shown in Fig. 2.21, the interphase inductor currents i_{L_1} and i_{L_2} over half of the switching period T_{sw}, exhibiting no DC offset current ($I_o = 0$). The circuit can be equivalently modeled using a single inductor with an effective inductance of $L_1 + L_2 = 2L$. The resulting inductor current i'_L captures the combined ripple behavior of i_{L_1} and i_{L_2}. The peak amplitude of this triangular ripple can be analytically expressed as:

$$\hat{i}_L = \frac{nV_b}{8f_{sw}L} \,. \tag{2.23}$$

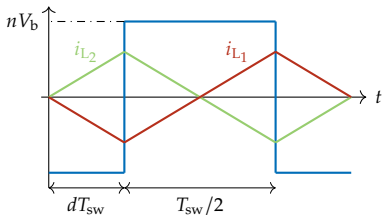


Figure 2.21: Voltage and current waveforms of the interphase inductors without the DC offset case.

On applying Kirchhoff's Current Law (KCL), the leakage inductor current of the output bridge $i_L(dT_{sw})$ defined in (2.5) modifies as:

$$i_L(dT_{sw}) = \frac{V_a}{4f_{sw}L_d}[G + 4d - 1] + \hat{i}_L \,, \tag{2.24}$$

that by considering the parameter $\beta = 2L/L_d$, the output side leads to the following ZVS criterion:

$$G \geq (1 - 4d)\frac{\beta}{1+\beta} \,. \tag{2.25}$$

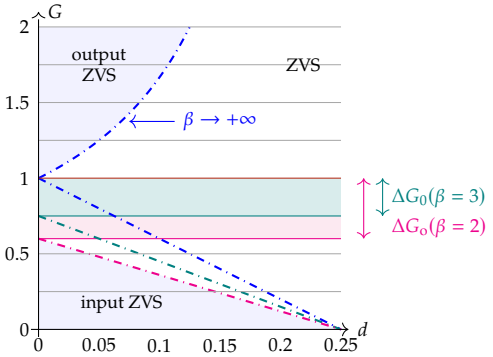


Figure 2.22: Without DC offset case ZVS region in the G vs d plane for the CF-DAB.

3: The ZVS analysis of the zero DC offset case is similar to the auxiliary inductor-based DAB discussed in Section 2.3. In the CF-DAB, since no DC offset current flows through the interphase inductors, the converter effectively behaves like the auxiliary inductor-based DAB. In contrast, the nonzero DC offset case introduces distinct ZVS behavior, as analyzed in the following section.

From (2.25), under no-load conditions ($d = 0$), the ZVS criterion simplifies, allowing the calculation of ΔG_o, which is similar to (2.18)[3], where ΔG_o represents the additional ZVS margin achieved due to the interleaved output structure. Fig. 2.22 illustrates the extended ZVS region for various values of β. The ZVS condition for the input bridge remains identical to that of a conventional DAB, determined by (2.6). In contrast, for the output bridge, due to the presence of interleaved inductors, the ZVS region expands toward the low-power operating range (i.e., smaller values of d), as quantified by the increase in ΔG_o. This expansion reduces the input ZVS area at light load while keeping the maximum d at a fixed position. However, reducing the β can increase the switch current RMS, as discussed in Section 2.3.3. Notably, as $\beta \to +\infty$, the ZVS condition (2.25) converges to that of the conventional SPS case given in (2.7). Moreover, if the interphase inductors are instead connected on the input side, the leakage inductor current $i_L(0)$ is altered, which in turn enlarges the ZVS region of the input bridge, similar to the discussion in Section 2.3. Therefore, the CF-DAB operating in zero DC offset case offers a clear advantage in enabling wide voltage gain operation while achieving ZVS on both bridges, even under light-load conditions, with the trade-off of higher switch current RMS.

2.5.2 ZVS Analysis with the DC Offset Case

As mentioned, the interphase inductors exhibiting a DC offset can be either positive ($I_o > 0$) or negative ($I_o < 0$), depending on the load connection. Fig. 2.23 depicts the inductor currents i_{L_1} and i_{L_2} under a positive DC offset condition. In this case, since $L_1 = L_2 = L$, the peak amplitude of the triangular ripple can be formulated as:

$$\hat{i}_L = \frac{nV_b}{8f_{sw}L} + \frac{I_o}{2}, \tag{2.26}$$

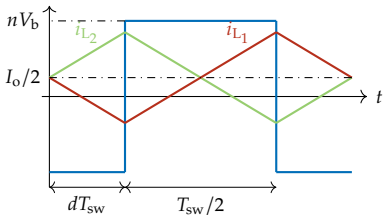


Figure 2.23: Voltage and current waveforms of the interphase inductors without the DC offset case.

Notice that when $I_o = 0$, (2.26) simplifies into (2.23). On applying KCL, the leakage inductor current of the output bridge $i_L(dT_{sw})$ defined in (2.5), modifies as:

$$i_L(dT_{sw}) = \frac{V_a}{4f_{sw}L_d}[G + 4d - 1] + \hat{i}_L, \tag{2.27}$$

that by considering the parameters $\beta = L/L_d$, the output bridge ZVS boundary now splits into two distinct conditions: one for the lower switches, G_L^{sw}, and one for the upper switches, G_U^{sw}. This results in the

following ZVS criterion:

$$G_{\mathrm{L}}^{sw} \geq (1 - 4d - \alpha)\frac{2\beta}{1 + 2\beta}\,, \tag{2.28}$$

$$G_{\mathrm{U}}^{sw} \geq (1 - 4d + \alpha)\frac{2\beta}{1 + 2\beta}\,, \tag{2.29}$$

where α is defined as:

$$\alpha = \frac{2 f_{\mathrm{sw}} L_{\mathrm{d}} I_{\mathrm{o}}}{V_{\mathrm{a}}}\,. \tag{2.30}$$

Note

Here α represents the DC offset parameter and β represents the auxiliary/interphase inductor design parameter.

As shown in Fig. 2.24(a), which corresponds to the case of $\beta \to \infty$ and $I_{\mathrm{o}} > 0$, the ZVS region of the input bridge remains defined by the conventional boundary. In contrast, the output bridge ZVS region splits into two distinct boundaries, denoted as G_{L}^{sw} and G_{U}^{sw}. The separation between these boundaries is governed by the parameter α, which increases with the output current I_{o}. As α increases, the region between G_{L}^{sw} and G_{U}^{sw} widens, indicating a broader operating range where only partial ZVS is achieved. Specifically, satisfying the condition G_{L}^{sw} ensures that the lower switches (S_6 and S_8 from Fig. 2.20) operate under ZVS, while the upper switches (S_5 and S_7 from Fig. 2.20) experience hard switching.

Similarly, Fig. 2.24(b) corresponds to the case of $\beta \to \infty$ and $I_{\mathrm{o}} < 0$. The ZVS region of the input bridge remains the same as the conventional boundary. However, the roles of the two output bridge ZVS boundaries are reversed, with $\alpha < 0$ representing the negative DC offset current.

In general, as $|\alpha|$ increases, the separation between G_{L}^{sw} and G_{U}^{sw} also increases, expanding the region where only partial ZVS occurs. To ensure

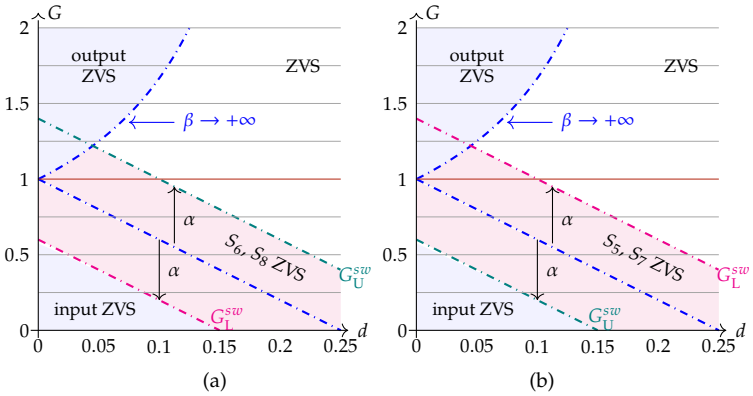


Figure 2.24: ZVS region in the G vs d plane for $\beta \to \infty$: (a) positive DC offset; (b) negative DC offset.

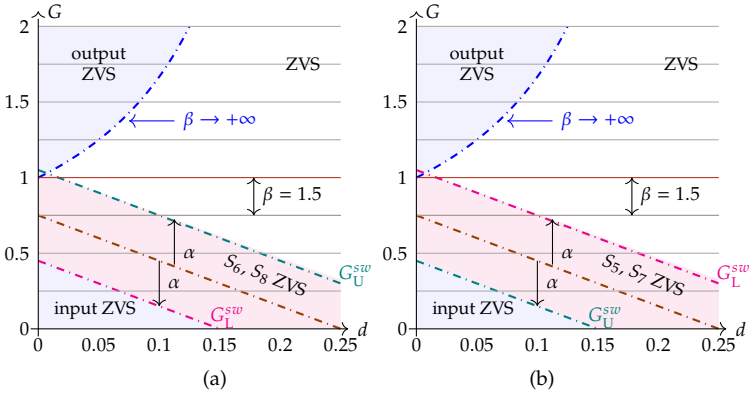


Figure 2.25: ZVS region in the G vs d plane for $\beta = 1.5$: (a) positive DC offset; (b) negative DC offset.

full ZVS on the output bridge, both boundary conditions G_{L}^{sw} and G_{U}^{sw} must be met. When $\alpha = 0$, corresponding to the zero DC offset case, the two boundaries coincide and resemble the ZVS boundary defined in (2.25). However, it should be noted that for a given phase shift d, the output current I_{o} also becomes fixed, which in turn determines the value of α and thus the separation between the two ZVS boundaries. Consequently, at lower d values, the reduced output power limits the maximum attainable DC offset I_{o}, thereby narrowing the region between G_{L}^{sw} and G_{U}^{sw}. This constraint is not reflected in Fig. 2.24 and will be addressed in detail in future work.

Fig. 2.25(a) and (b) correspond to the cases of $\beta = 1.5$ with $I_{\mathrm{o}} > 0$ and $I_{\mathrm{o}} < 0$, respectively. The input bridge ZVS remains unaffected due to the absence of interphase inductors. Whereas, the output bridge ZVS changes, with the boundary splitting into two as a result of the DC offset. As β decreased, both ZVS boundaries are shifted downward at lower d values, reducing the input ZVS region and narrowing the gap between G_{L}^{sw} and G_{U}^{sw} compared to the $\beta \to \infty$ case. However, reducing the β can increase the switch current RMS, similar to the zero DC offset case. Therefore, proper design guidelines must be followed to ensure wide voltage gain operation while maintaining lower switch current RMS and reliable ZVS conditions. A similar analysis can be extended to the case where the interleaved inductors are connected to the input bridge. In that scenario, the leakage inductor current $i_{\mathrm{L}}(0)$ is modified accordingly, leading to partial ZVS on the input bridge switches at particular operating conditions, as discussed in [45].

2.5.3 Numerical Validations

The CF-DAB shown in Fig. 2.20 has been simulated in the PLECS environment (Plexim GmbH) to validate [4] the ZVS analysis for both the zero-DC-offset and nonzero-DC-offset cases. The switch parameters were extracted from the datasheets of the AIMW120R060M1H SiC MOSFET and the IDW40G120C5B SiC Schottky diode (Infineon Technologies AG). The main adopted parameter values are summarized in Table 2.4. A relatively small phase-shift value of $d = 0.05$ was selected in order to evaluate the ZVS boundary conditions, since for higher phase-shift values the effective voltage gain G range increases and the switches operate under ZVS across all operating points. In addition, a voltage gain of $G = 0.5$ is chosen as a practical condition to highlight both hard-switching and ZVS operation, as it provides sufficient current stress to reveal boundary cases without forcing the converter into full-ZVS operation at all times.

It is well known that a MOSFET achieves ZVS if, just before turn-on, its current is negative (i.e., flowing through the body diode). In this state, the device's output capacitance is discharged by the negative current before the gate is driven, allowing the switch to turn on at nearly zero drain–source voltage. Hence, by monitoring the instantaneous switch currents, it is possible to determine whether ZVS is achieved. For this purpose, the instantaneous currents of switches S_5 and S_6 from Fig. 2.20 are evaluated in simulation for both the zero- and nonzero-DC-offset cases. Since the primary-side switches already achieve ZVS under the selected operating conditions, the validation on the secondary side can

4: The ZVS boundary conditions derived in Sections 2.5.1-2.5.2 are validated numerically (Section 2.5.3), while the experimental prototype (Section 2.5.4) is restricted to verifying the presence or absence of DC offset currents in bipolar and unipolar cases. Hence, direct hardware validation of ZVS regions remains outside the present scope. However, the experimental validation of the auxiliary inductor-based DAB (Section 2.3.5) can be regarded as representative of the CF-DAB zero-offset case, since the auxiliary inductor current exhibits a zero average, as shown in Fig. 2.17.

Parameter	Symbol	Value	Unit
Input voltage	V_{dc}	800	V
Output voltage	V_o	GV_{in}	V
Leakage Inductance	L_d	80	μH
Interphase Inductance	L_1, L_2	βL_d	μH
Switching frequency	f_{sw}	40	kHz
Switching period	T_{sw}	25	μs
Dead time	t_d	0.05	μs

Table 2.4: CF-DAB numerical plant main system parameters.

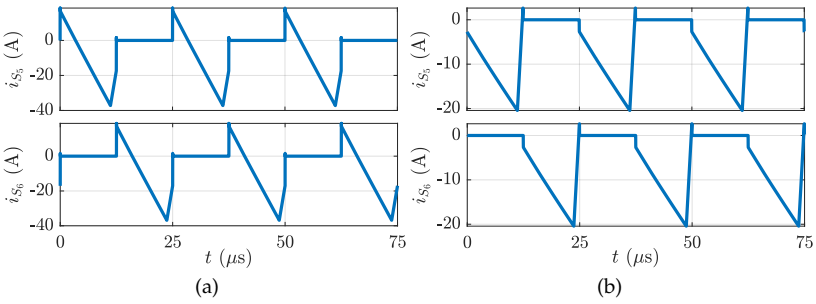


Figure 2.26: Instantaneous switch S_5 and S_6 currents in case of without DC offset: (a) Hard switching; (b) ZVS.

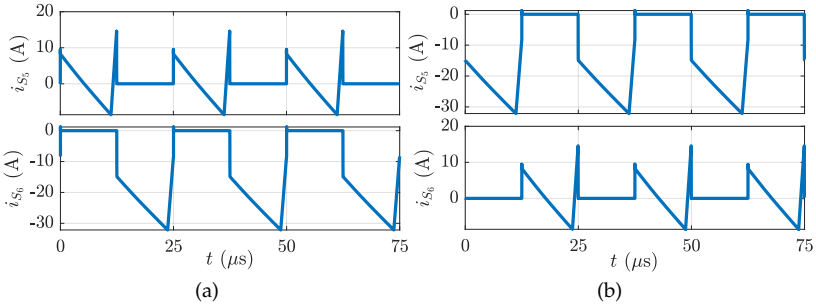


Figure 2.27: Instantaneous switch S_5 and S_6 currents in case of with DC offset: (a) Positive offset; (b) Negative offset

be restricted to S_5 and S_6, which represent the top and bottom devices, owing to the symmetrical behaviour of the converter.

Fig. 2.26 shows the instantaneous switch currents of S_5 and S_6 for the no-DC-offset case, where the load is connected between the upper and lower DC rails and the middle port is grounded. In Fig. 2.26(a), the parameter β is chosen with a high value, replicating the behavior of the conventional DAB. In this case, the switch currents are positive during turn-on, which prevents the discharge of the device output capacitances and leads to hard switching on the secondary side. However, as discussed in Section 2.5.1, the interphase inductors can be designed based on β. For the selected operating conditions, a value of $\beta = 1.5$ satisfies the design equation (2.25), thereby enlarging the ZVS region. This improvement is demonstrated in Fig. 2.26(b), where the instantaneous switch currents are negative during turn-on, validating the achievement of ZVS.

Fig. 2.27 shows the instantaneous switch currents for the case with positive and negative DC offset. The same β value has been chosen here to design the interphase inductors. In Fig. 2.27(a), corresponding to the positive DC offset, the upper switch current i_{S_5} is positive during turn-on, leading to hard switching, whereas the lower switch current i_{S_6} is negative during turn-on, thereby achieving ZVS. Conversely, in Fig. 2.27(b), corresponding to the negative DC offset, the roles are reversed: the lower switch S_6 operates under hard switching, while the upper switch S_5 achieves ZVS. This behavior is fully consistent with the ZVS analysis presented in Section 2.5.2.

2.5.4 Experimental Validations

To validate the proposed converter, a 5 kW experimental prototype has been built and tested, as shown in Fig. 2.28. The main design parameters are summarized in Table 2.5. The prototype is operated in open loop to evaluate its performance in both unipolar and bipolar configurations, specifically demonstrating the no DC offset case in the bipolar mode and the positive and negative DC offset cases in the unipolar mode.

Fig. 2.29(a) shows the main waveforms of the CF-DAB converter, including the primary v_{a} and secondary v_{b} transformer voltages, as well as the transformer current i_{L}. A small phase difference of $d = 0.028$ between v_{a} and v_{b} is observed, corresponding to the applied phase-shift modulation and CF-DAB control scheme. In this test, a balanced system with a bipolar DC connection of ±350 V is considered, delivering a total output power of 2 kW. Fig. 2.29(b) presents the interphase inductor currents i_{L_1} and i_{L_2}, which exhibit a zero average value due to system symmetry, while their ripple is caused by the switching action. It is important to note that, in the presence of load imbalance, the interphase inductor currents i_{L_1} and i_{L_2} would exhibit a DC offset, whose polarity (positive or negative) depends directly on the nature of the unbalance.

The unipolar configuration is illustrated in Fig. 2.30(a) and Fig. 2.30(b), where the load is connected between the lower DC rail and the middle port, and between the upper DC rail and the middle port, respectively. As shown in

Table 2.5: CF-DAB experimental setup parameters.

Parameter	Symbol	Value	Unit
Output voltage	$+V_{\mathrm{o}}/2$ $-V_{\mathrm{o}}/2$	+350 -350	V
Maximum output power	P_{max}	5	kW
Input voltage	V_{dc}	800	V
Interphase inductors	L_1 L_2	600	μH
Switching frequency	f_{sw}	100	kHz
HF transformer turns ratio	n	15:15	-
Leakage inductance	L_{d}	180	μH

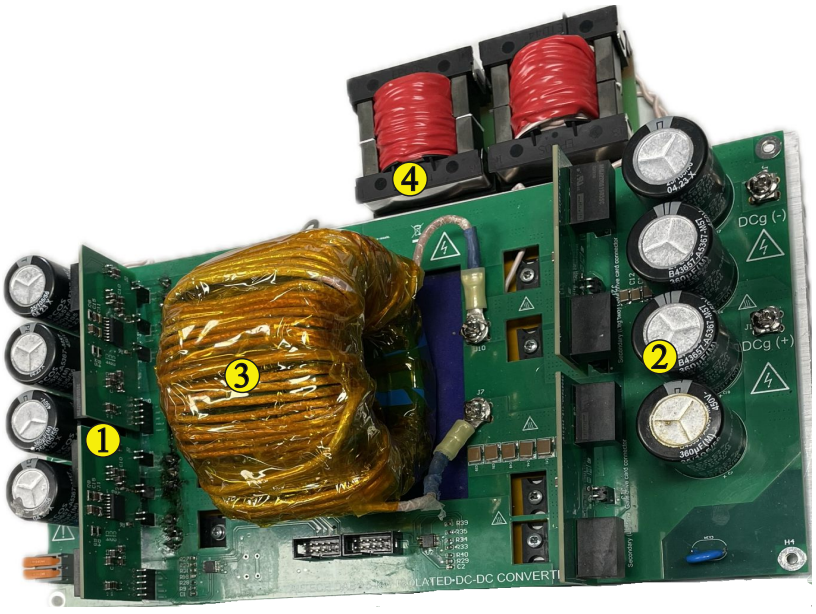
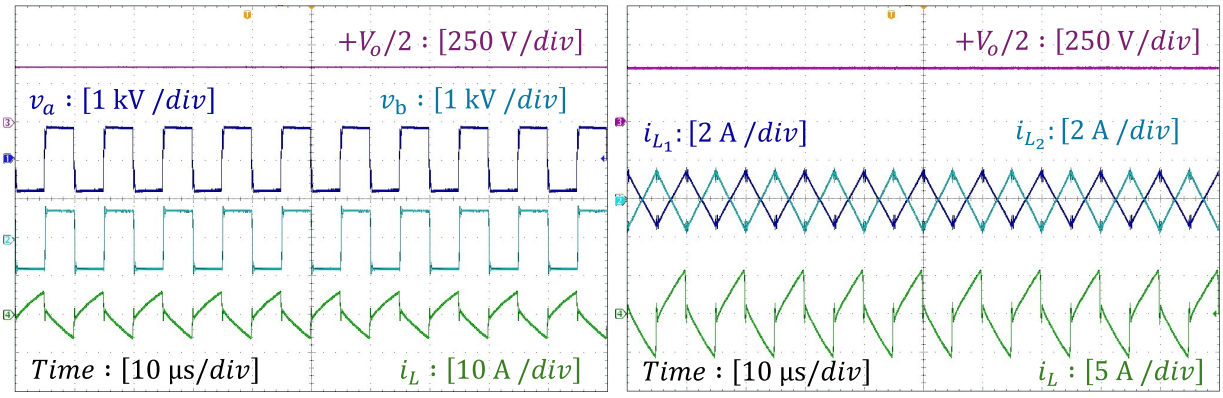
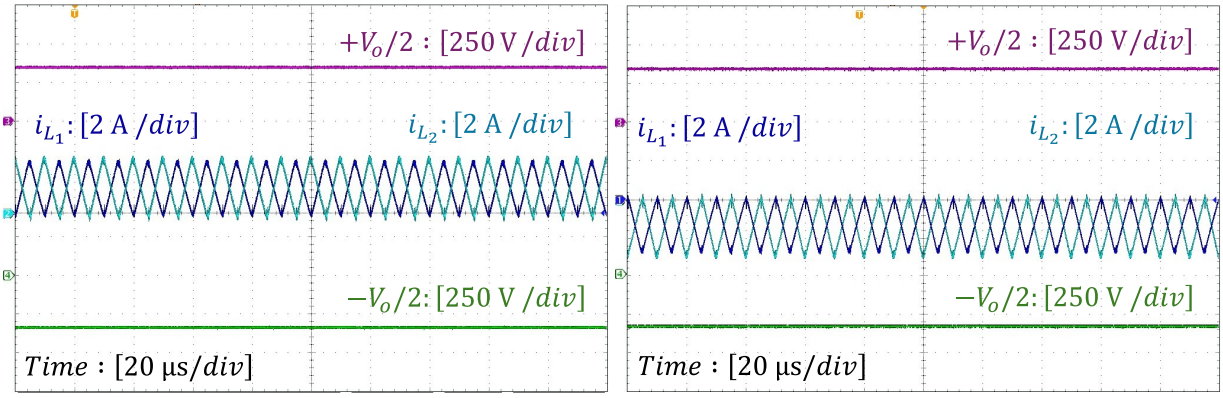


Figure 2.28: Experimental setup of CF-DAB: (1) input bridge; (2) output bridge; (3) high-frequency transformer; (4) interphase inductors.



(a) (b)

Figure 2.29: (a) Main waveforms of CF-DAB; (b) Interphase inductor currents without the DC offset in Bipolar configuration.



(a) (b)

Figure 2.30: (a) Interphase inductor currents with the positive DC offset in Unipolar configuration; (b) Interphase inductor currents with the negative DC offset in Unipolar configuration.

Fig. 2.30(a), the interphase inductors exhibit a positive DC offset, whereas in Fig. 2.30(b), they exhibit a negative DC offset, in full agreement with the analysis presented in Section 2.5. In both cases, the output power is 0.5 kW, and the resulting voltages remain balanced at approximately ±350 V, regardless from which output port the power is drawn. Furthermore, complete ripple cancellation is achieved, leading to smooth output current delivery. This effect is also visible in the traces of $+V_o/2$ and $-V_o/2$, whose voltages remain unaffected by the interphase inductor ripple. A complementary case occurs when the load is connected between the upper and lower DC rails with the middle port grounded; in this situation, the interphase inductor currents i_{L_1} and i_{L_2} do not exhibit any DC offset.

Furthermore, from these experimental results, small voltage deviations can be observed between the two output ports. Since the converter is operated in open loop, such deviations are acceptable, as no control system is implemented to actively regulate the output voltages. According to the measurements, the maximum voltage variation is $\Delta V = 3.97\%$ in the unipolar cases and $\Delta V = 1.20\%$ in the bipolar case, primarily caused by the voltage drop across the inductors. These deviations remain within an acceptable range, thereby validating the correct operation of the proposed system. It should be noted that experimental verification of the ZVS boundaries was not pursued, as the scope of the prototype validation was limited to demonstrating the presence or absence of DC offset currents in bipolar and unipolar configurations. Therefore, verification of the ZVS analysis is restricted only to the numerical simulations, which

are already discussed in Section 2.5.3. Nevertheless, as mentioned earlier, the experimental results (see Section 2.3.5) obtained for the auxiliary inductor-based DAB are directly applicable to without the DC offset case of the CF-DAB converter.

2.6 Summary

This chapter presented a comprehensive investigation of ZVS conditions in DAB converters, focusing first on the conventional topology with auxiliary inductors and then extending the analysis to the CF-DAB.

The first part provides the analytical models for ZVS boundaries for both input- and output-side auxiliary inductors. Their effect on the switch current RMS was evaluated, highlighting the trade-off between extended ZVS regions and increased conduction losses. These findings were validated through PLECS simulations and confirmed experimentally using a 300 W prototype, showing that auxiliary inductors successfully extend the ZVS region but may reduce efficiency due to higher RMS currents.

In the second part, the focus is shifted to the CF-DAB topology with interphase inductors, which is particularly suited for bipolar and unipolar DC microgrids. Analytical ZVS boundary conditions were derived for both zero and nonzero DC offset cases, showing how the presence of offset currents splits the ZVS region into partial and full-ZVS subregions. Numerical validation using detailed simulations confirmed the theoretical derivations and clarified the operating boundaries under different offset scenarios. Experimental results obtained from a 5 kW prototype, demonstrated the practical occurrence of zero and nonzero offset currents in bipolar and unipolar configurations, respectively, thereby supporting the theoretical framework. However, the experimental validation was restricted to DC offset verification, while the validation of ZVS boundary conditions relied on numerical simulations.

Overall, the analyses and validations presented in this chapter provide clear design guidelines for achieving soft-switching in both conventional and current-fed DAB converters. The results emphasize the importance of properly sizing auxiliary or interphase inductors to extend ZVS operation, while carefully balancing the associated conduction losses and efficiency trade-offs. The research outcomes from this chapter have led to the publications [45], [69], [75].

[45]: Pittala *et al.* (2023), 'Insights on DAB Converter with Auxiliary Inductors'
[69]: Carvalho *et al.* (2025), 'Universal Interlinking Converter for Prosumer DC Buildings: Operation with Different DC Grid Types'
[75]: Pittala *et al.* (2025), 'ZVS Analysis of an Interleaved Current-Fed DAB for Bipolar and Unipolar DC Grids'

Asymmetrical-Bidirectional DC/DC Converter

3

Abstract

The chapter begins by analysing the SAB converter and deriving closed-form analytical expressions for power transfer in both DCM and CCM, establishing the foundation for the subsequent extension to the AB-DC/DC topology. The mechanism of passive power sharing is then introduced, where the distribution between the diode and active bridges depends on the coupling inductance ratios. However, due to unavoidable tolerances in magnetic components, the passive method alone cannot guarantee equal sharing, potentially leading to uneven thermal stress. To overcome this, a novel active power-sharing modulation strategy is proposed, which enables controlled power transfer from the diode bridge to the active bridge by introducing a turn-on delay in the secondary-side switches. A detailed analytical framework is developed to describe the converter operation across six distinct operating regions: conventional DCM, conventional CCM, two hybrid regions, and the DAB forward and reverse modes. For each region, closed-form power expressions and boundary conditions are derived, enabling accurate prediction of power transfer under both passive and active sharing scenarios. The analysis shows how the proposed modulation strategy introduces additional voltage pulses in DCM and pulse shifts in the hybrid modes, effectively enlarging the operational envelope of the AB-DC/DC converter. The proposed models and modulation method are validated through extensive PLECS simulations and hardware experiments on a 200 V, 100 kHz laboratory prototype. The results confirm strong agreement between theoretical predictions, numerical analysis, and measured waveforms. In particular, the active power-sharing technique is shown to reliably shift power from the diode bridge to the active bridge, or completely shut down the diode bridge when required, thereby reducing thermal stress and enhancing system reliability.

3.1 Introduction to Asymmetrical Bidirectional DC/DC Converter 39
3.2 Single-Active Bridge Converter 41
3.2.1 Power Transfer in SAB Converter 41
3.2.2 DCM-CCM Boundary Conditions 43
3.3 Asymmetrical-Bidirectional DC/DC Converter 43
3.4 Passive Power Sharing Control 44
3.4.1 Converter Leg Power PDF 45
3.4.2 Bridge Power PDF 47
3.4.3 Numerical Validations . . 48
3.5 Active Power Sharing Control 52
3.5.1 Discontinuous Conduction Mode Region 53
3.5.2 Hybrid 1 Region 54
3.5.3 Hybrid 2 Region 55
3.5.4 Continuous Conduction Mode Region 56
3.5.5 Dual-Active-Bridge Region 56
3.5.6 Numerical Validations . . 57
3.5.7 Efficiency Analysis 58
3.5.8 Operation and Performance 60
3.5.9 Experimental Validations 62
3.6 Hybrid Modulation: Alternating Active Power Sharing and SAB Control 66
3.6.1 Numerical Validation . . 67
3.7 Summary 70

3.1 Introduction to Asymmetrical Bidirectional DC/DC Converter

In many applications like EV charging and industrial microgrids, reverse power flow is significantly lower than forward flow [76], making full-rated bidirectional designs inefficient and unnecessarily costly. To address cost inefficiencies under asymmetric power flow, several works have proposed modifying converter topologies. The hybrid multi-active bridge in [77] combines active and passive bridges via multi-winding transformers. In [78], an AB-DC/DC converter was introduced, integrating partially scaled passive and active bridges in parallel, effectively merging SAB and DAB functionalities. This design achieves notable semiconductor savings, reducing secondary-side device cost by up to 44% and total system cost by 9.7% compared to full-DAB converters.

Similarly, the work in [49] presented an improved topology aimed at reducing peak current stress during forward-mode operation. In [79], the authors focused on an active control method for a hybrid DC transformer to increase the range of power transmission compared to the uncontrolled rectification mode. While these works primarily focus on control flexibility, peak current reduction, and issues under reverse flow conditions, less attention has been given to passive power sharing imbalances that can arise in the AB-DC/DC converter described [78], due to practical factors such as magnetic component tolerances.

In literature, research on how circuit element tolerances affect the operating modes of power electronic devices is becoming increasingly important to ensure the desired device performance [80]. Any electronic system's reliability is directly correlated with the precision of the tolerance analysis accomplished during the design phase. Essentially, uncertainties arising from construction procedures always impact the values of the physical parameters of commercial components [81]. Further uncertainties arise due to the fact that all parameters are contingent upon the specific operating conditions in which the components function, influenced by various factors such as frequency, temperature, aging, and others [82]. Authors in [83] stated that modifications in the circuit element values have a substantial effect on the power electronic device's working mode in both quantitative and qualitative ways. The analysis was performed by establishing a ±20% tolerance in inductance for commercially available inductors, which is roughly in line with the actual state of the circuit elements that are sold on the market.

When two or more bridges are connected in parallel, ensuring adequate power sharing among them is essential [84]. However, factors such as environmental conditions, parasitic parameters, and tolerances in commercial components can impact power sharing between the bridges. These disparities may cause uneven thermal stress and component aging, ultimately affecting the lifetime and reliability of the system [85]. In order to ensure the robust performance of a converter, the aforementioned factors must be considered in a realistic design [86]. Therefore, it is important to investigate how magnetic component tolerances might affect the power sharing between the two partial-scale bridges when they are working in forward mode. This study could provide valuable insights, as any inaccuracies in power sharing might impact the choice of component sizes, highlighting the need for careful analysis in this area. Thus, in [87], a statistical analysis was conducted considering ±20% tolerances in the coupling inductors, showing that even minor deviations in inductance values can lead to significant imbalance in power sharing among the parallel-connected bridges.

To mitigate this issue, the authors in [88]–[90] proposed a novel modulation technique that enables active power-sharing control via a software-based solution. This innovative technique allows for the reduction of overloading effects on the diode bridge by transferring the diode bridge power to the active bridge. Additionally, the strategy can enable a complete shutdown of the diode bridge, offering an effective means to mitigate thermal stress on the system. However, the analysis in [88] was limited to DCM only. This concept has been extended in [89], [90], understanding the converter behavior in different regions, such as Hybrid 1, Hybrid 2, CCM, and DAB mode.

To facilitate a clear understanding of the proposed modulation strategy, the SAB converter has been analyzed, along with its fundamental power transfer characteristics have been derived, which are later extended to the AB-DC/DC topology. Further, a comprehensive analytical framework is developed to characterize the AB-DC/DC converter behavior across the new operating modes. Closed-form power expressions are derived for each mode, enabling accurate prediction of power flow dynamics between the partial-scale active bridge and partial-scale diode bridge. The proposed active power-sharing modulation strategy is thoroughly validated through numerical simulations and experimental results obtained using a hardware prototype. To ensure a fair comparison between simulation and experimental conditions, identical components and parameters were used. These contributions offer valuable insights into the complete operational envelope of the AB-DC/DC converter, addressing key challenges in asymmetric power distribution.

The remainder of this chapter is structured as follows. Section 3.2 introduces the SAB converter and derives the analytical power expressions for both discontinuous and continuous conduction modes. Section 3.3 provides the background on the AB-DC/DC converter with emphasis on forward power sharing. Section 3.4 discusses the passive power sharing mechanism in detail and develops a comprehensive mathematical derivation of the probability density function (PDF) for the power processed by the converter's secondary-side legs and the two partial-scale bridges. This probabilistic analysis is supported by numerical validation, carried out through 30,000 PLECS simulations with randomized inductance values. Building upon these results, Section 3.5 introduces the active power sharing control strategy and validates its effectiveness through both simulation and experimental results. Section 3.6 further examines the explicit implementation of the proposed modulation technique, particularly in discontinuous conduction mode. Finally, Section 3.7 summarizes the key findings and concludes the chapter.

3.2 Single-Active Bridge Converter

Fig. 3.1 illustrates the circuit diagram of a SAB converter, consisting of two bridges coupled via a high-frequency transformer. The primary side features an active H-bridge, while the secondary side employs a diode bridge, enabling power transfer only in the forward direction. Depending on the current in the transformer's leakage inductor L_1, the converter operates either in DCM or CCM. The corresponding waveforms for both conduction modes are shown in Fig. 3.2. It is worth noting that voltage oscillations may appear in the secondary-side AC voltage v_2 under DCM, primarily due to the presence of parasitic elements.

Note

In this chapter, the parameter d represents the phase-shift between the two legs of the primary side H-bridge.

3.2.1 Power Transfer in SAB Converter

From Fig. 3.2, it can be observed that the waveforms exhibit half-cycle symmetry over the switching period T_{sw}. Accordingly, the average active power transferred in DCM and CCM can be computed using:

$$P_{\text{o}} = \frac{2}{T_{\text{sw}}} \int_0^{dT_{\text{sw}}} v_1 \, i_1'(t) \, dt \, . \tag{3.1}$$

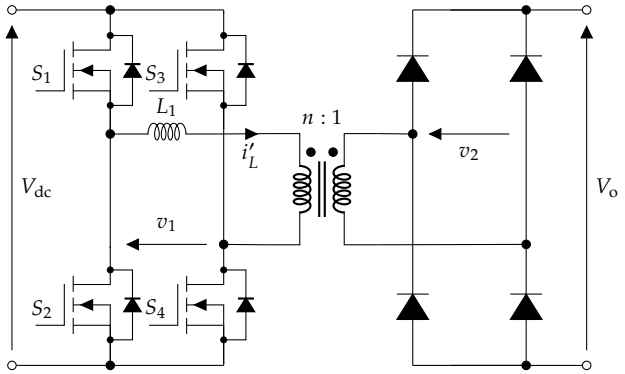


Figure 3.1: Single-active-bridge converter.

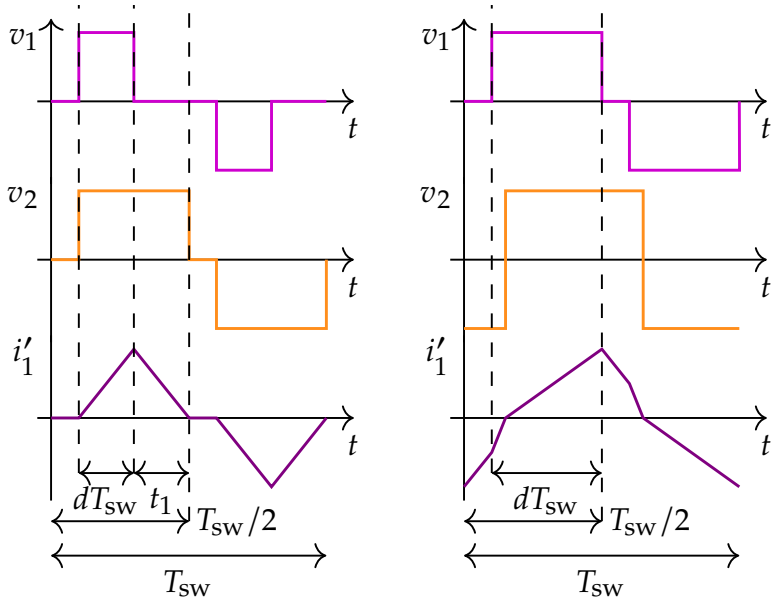


Figure 3.2: Waveforms of SAB converter: (a) DCM; (b) CCM.

In both cases, $i'_1(t)$ can be approximated as piecewise linear within the corresponding time intervals, shown in Fig. 3.2. This leads to a closed-form expression for the output power:

$$P_o = \begin{cases} \dfrac{(1-m)V_{dc}^2}{L_1 f_{sw}} d^2 & \text{DCM: } d < \frac{m}{2} \\ \dfrac{mV_{dc}^2}{L_1 f_{sw}} \left[\dfrac{d}{2}(1-d) - \dfrac{m^2}{8} \right] & \text{CCM: } d \geq \frac{m}{2} \end{cases}. \tag{3.2}$$

Note

In this chapter, the parameter m represents the voltage-gain ratio between the output and input.

The parameter d denotes the phase shift between the primary bridge legs, while m represents the voltage gain, defined as the ratio of the output voltage to the input voltage, i.e., $m = nV_o/V_{dc}$.

Fig. 3.3 illustrates the normalized output power P_o as a function of the phase shift d and voltage gain m. As observed, the power surface peaks around $d = 0.5$ and $m = 0.57$. The DCM region ($d < m/2$) exhibits a parabolic power increase, while in CCM, power tends to plateau or slightly decline with increasing d.

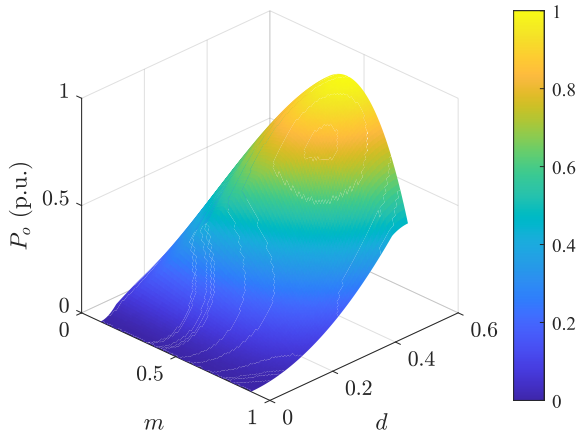


Figure 3.3: Normalized output power P_o (p.u.) as a function of voltage gain m and phase shift d.

3.2.2 DCM-CCM Boundary Conditions

The boundary between DCM and CCM occurs when the inductor current $i_1'(t)$ just returns to zero at the end of the half switching cycle. For example, in the DCM case, as shown in Fig. 3.2(a), the peak current can be obtained by calculating the area under the triangular current waveform:

$$I_{\text{pk}} = \frac{V_{\text{dc}}(1-m)dT_{\text{sw}}}{L_1} = \frac{nV_{\text{o}}}{L_1}t_1 \,. \tag{3.3}$$

Solving for t_1:

$$t_1 = \frac{(1-m)dT_{sw}}{m} \,. \tag{3.4}$$

The duration of the triangular current consists of two intervals: dT_{sw} for the rising edge and t_1 for the falling edge. At the boundary of DCM, the sum of these intervals is less than half of the switching period, thus obtaining:

$$dT_{\text{sw}} + t_1 < \frac{T_{\text{sw}}}{2} \,. \tag{3.5}$$

Substituting the expression for t_1 into (3.5), and solving for d, the following inequality is obtained:

$$d < \frac{m}{2} \,. \tag{3.6}$$

This inequality defines the DCM-CCM boundary. Specifically, when $d < m/2$, the converter operates in DCM; for $d \geq m/2$, it enters CCM.

3.3 Asymmetrical-Bidirectional DC/DC Converter

The basic concept of the AB-DC/DC converter is illustrated in Fig. 3.4. In [78], the authors proposed a power-sharing mechanism for forward operation by deactivating the secondary-side active bridge and allowing conduction through its body diodes. This effectively transforms the active bridge into a passive diode bridge. As a result, the secondary side of the AB-DC/DC converter behaves equivalently to a conventional SAB converter with two parallel diode bridges connected through four coupling inductors: $L_{2\text{u}}$, $L_{3\text{u}}$, $L_{2\text{l}}$, and $L_{3\text{l}}$.

Similar to the SAB converter, the AB-DC/DC topology can operate in

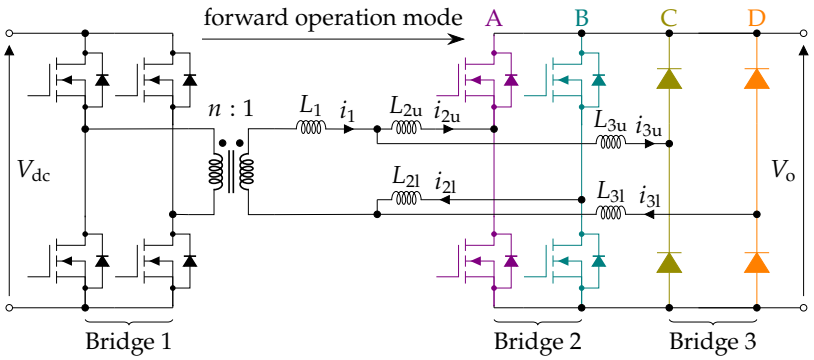


Figure 3.4: Asymmetrical bidirectional DC/DC converter.

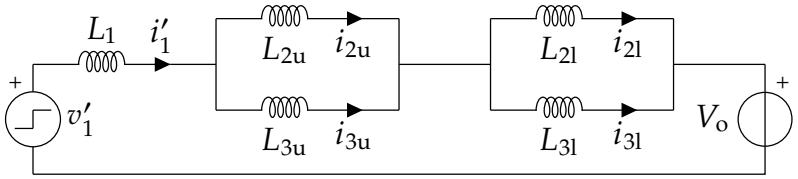


Figure 3.5: Equivalent circuit of the AB-DC/DC converter from the transformer secondary side.

either DCM or CCM. The output power transferred in the AB-DC/DC converter follows the same expression given in (3.2), with the inductor L_1 replaced by the total equivalent inductance L_{eq}, illustrated in Fig. 3.5, and calculated as:

$$L_{eq} = L_1 + \frac{L_{2u}L_{3u}}{L_{2u} + L_{3u}} + \frac{L_{2l}L_{3l}}{L_{2l} + L_{3l}} \,. \tag{3.7}$$

3.4 Passive Power Sharing Control

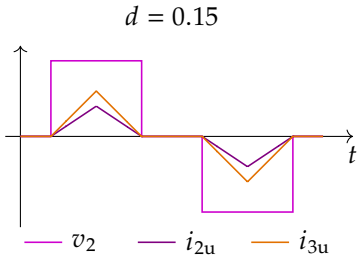


Figure 3.6: Voltage and current waveforms in conventional DCM.

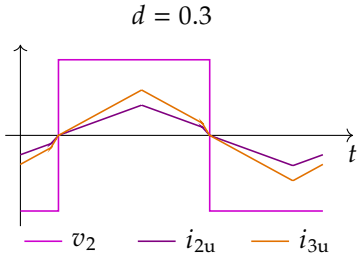


Figure 3.7: Voltage and current waveforms in conventional CCM.

Passive power sharing control can be achieved by appropriately sizing the coupling inductors L_{2u}, L_{3u}, L_{2l}, and L_{3l}. The main current and voltage waveforms are illustrated in Figs. 3.6 and 3.7, which highlight the operating regions of the converter, for a fixed voltage gain of $m = 0.5$. The Fig. 3.6 plot corresponds to the conventional DCM region, with a phase shift of $d = 0.15$, where both bridge currents, i_{2u} and i_{3u}, are discontinuous. In contrast, the Fig. 3.7 plot depicts the conventional CCM region, with a phase shift of $d = 0.3$, where both currents remain continuous throughout the switching period. Thus satisfying the boundary conditions discussed in Section 3.2.2.

It is important to note that the sum of i_{2u} and i_{3u} in the waveforms of Figs. 3.6 and 3.7 corresponds to the inductor current i'_1 shown in Fig 3.2. According to the notation in Fig. 3.4, the power theoretically processed by each leg (A, B, C, and D) can be predicted as:

$$\begin{aligned} P_A &= \frac{P_o}{2}\left[\frac{L_{3u}}{L_{2u}+L_{3u}}\right], \quad P_B = \frac{P_o}{2}\left[\frac{L_{3l}}{L_{2l}+L_{3l}}\right], \\ P_C &= \frac{P_o}{2}\left[\frac{L_{2u}}{L_{2u}+L_{3u}}\right], \quad P_D = \frac{P_o}{2}\left[\frac{L_{2l}}{L_{2l}+L_{3l}}\right]. \end{aligned} \tag{3.8}$$

From (3.8), it is evident that in ideal conditions, the power distribution within each branch can be regulated by selecting inductance ratios. However, real magnetics can significantly drift from the nominal val-

ues. Hence, it is necessary to assume a probability distribution for the tolerances considered. In practice, however, the manufacturers neither provide this information on the data sheets, nor indicate if the uncertainty is provided according to a deterministic or probabilistic method [91]. In case the distribution is not known, then the uncertainty value due to a given contribution is taken according to the principle of maximum entropy leading to a uniform distribution. For the sake of simplicity, all the here considered contributions have the same tolerance, i.e., ±20%. It is more useful to refer to normalized powers, as they depend solely on inductances, which are the only parameters affected by uncertainty for the purposes of this analysis. Taking $P_o/2$ as the normalization basis, and based on (3.8), the following expressions for the powers shared by the converter legs are obtained:

$$\begin{aligned} N_A &= \frac{L_{3u}}{L_{2u}+L_{3u}}\,, \quad N_B = \frac{L_{3l}}{L_{2l}+L_{3l}}\,, \\ N_C &= \frac{L_{2u}}{L_{2u}+L_{3u}}\,, \quad N_D = \frac{L_{2l}}{L_{2l}+L_{3l}}\,. \end{aligned} \tag{3.9}$$

It can be shown that the PDF of the power flowing in each branch can be closely approximated by a triangular distribution (T-PDF). To establish this result, the chapter first presents the detailed mathematical derivation of the actual PDF (A-PDF), which is then simplified into its triangular approximation. The resulting T-PDF is subsequently employed to characterize the power distribution of the partial-scale active bridge and the partial-scale diode bridge on the secondary side. This formulation provides valuable insight into the mechanism of passive power sharing between the two parallel-connected bridges.

3.4.1 Converter Leg Power PDF

In the following, reference is made to the power shared by the leg A of the converter depicted in Fig. 3.4. As per (3.9), the relative power N_A is a function of the sole inductances, and presents a PDF denoted with $\mathcal{N}_A$. To make computation steps easier, the reciprocal of $\mathcal{N}_A$ is first determined:

$$\frac{1}{\mathcal{N}_A(x)} = 1 + \frac{\mathcal{L}_{2u}(x)}{\mathcal{L}_{3u}(x)} = 1 + \mathcal{L}_{2u}(x)\mathcal{R}_{3u}(x)\,, \tag{3.10}$$

where $\mathcal{L}_{2u}$ and $\mathcal{L}_{3u}$ are the uniform PDFs for inductances L_{2u} and L_{3u}, respectively, and are represented as:

$$\begin{aligned} \mathcal{L}_{2u}(x) &= \frac{1}{0.4L_{2u}} \quad x \in [0.8L_{2u}, 1.2L_{2u}] \\ \mathcal{L}_{3u}(x) &= \frac{1}{0.4L_{3u}} \quad x \in [0.8L_{3u}, 1.2L_{3u}] \end{aligned}\,. \tag{3.11}$$

On the other hand, $\mathcal{R}_{3u}$ is another PDF corresponding the reciprocal of $\mathcal{L}_{3u}$, and it is computed from (3.11) as:

$$\mathcal{R}_{3u}(x) = \frac{\mathcal{L}_{3u}(\frac{1}{x})}{x^2} = \frac{5}{2L_{3u}x^2} \quad x \in \left[\frac{5}{6L_{3u}}, \frac{5}{4L_{3u}}\right]. \tag{3.12}$$

The PDF resulting from the product of $\mathscr{L}_{2u}$ and $\mathscr{R}_{3u}$ inside (3.10), here indicated as $\mathscr{H}_A$, can be computed using the approach outlined in [92] as:

$$\mathscr{H}_A(x) = \begin{cases} \displaystyle\int_{\alpha}^{\frac{x}{\gamma}} \frac{\mathscr{L}_{2u}(z)\mathscr{R}_{3u}\left(\frac{x}{z}\right)}{z} dz & \alpha\gamma \le x \le \beta\gamma \\ \displaystyle\int_{\frac{x}{\delta}}^{\beta} \frac{\mathscr{L}_{2u}(z)\mathscr{R}_{3u}\left(\frac{x}{z}\right)}{z} dz & \alpha\delta \le x \le \beta\delta \end{cases} \tag{3.13}$$

having:

$$\begin{aligned} \alpha &= 0.8L_{2u} \quad \gamma = \frac{1}{1.2L_{3u}} = \frac{1}{1.2kL_{2u}} \\ \beta &= 1.2L_{2u} \quad \delta = \frac{1}{0.8L_{3u}} = \frac{1}{0.8kL_{2u}} \end{aligned} . \tag{3.14}$$

Note

The parameters α and β are defined differently from those in Chapter 2 (Zero-Voltage Switching Analysis of Conventional and Current-Fed DAB Converters) on page 15. This note distinguishes to avoid confusion with the earlier use of α and β.

Using (3.13), the PDF of (3.10) can be obtained as:

$$\frac{1}{\mathscr{N}_A(x)} = \begin{cases} \dfrac{9k}{2} - \dfrac{2}{k(x-1)^2} & x \in \left[\dfrac{2}{3k}+1, \dfrac{1}{k}+1\right] \\ \dfrac{9}{2k(x-1)^2} - 2k & x \in \left[\dfrac{1}{k}+1, \dfrac{3}{2k}+1\right] \end{cases}, \tag{3.15}$$

where k is a function of the nominal inductances shown in Fig. 3.4. Later, it is also interpreted as the coupling inductance ratio, and it can exhibit distinct expressions for the legs between the two secondary-side bridges. Concerning leg A, (3.15) is evaluated with $k = L_{3u}/L_{2u}$. Finally, the PDF of the relative power $\mathscr{N}_l$ shared by a generic leg l can be computed as:

$$\mathscr{N}_l(x) = \begin{cases} \dfrac{9}{2k(1-x)^2} - \dfrac{2k}{x^2} & x \in \left[\dfrac{2k}{3+2k}, \dfrac{k}{1+k}\right] \\ \dfrac{9k}{2x^2} - \dfrac{2}{k(1-x)^2} & x \in \left[\dfrac{k}{1+k}, \dfrac{3k}{2+3k}\right] \end{cases}$$

$$k = \begin{cases} \dfrac{L_{3u}}{L_{2u}} & \text{for A} \\ \dfrac{L_{3l}}{L_{2l}} & \text{for B} \end{cases} \quad \text{and} \quad k = \begin{cases} \dfrac{L_{2u}}{L_{3u}} & \text{for C} \\ \dfrac{L_{2l}}{L_{3l}} & \text{for D} \end{cases} . \tag{3.16}$$

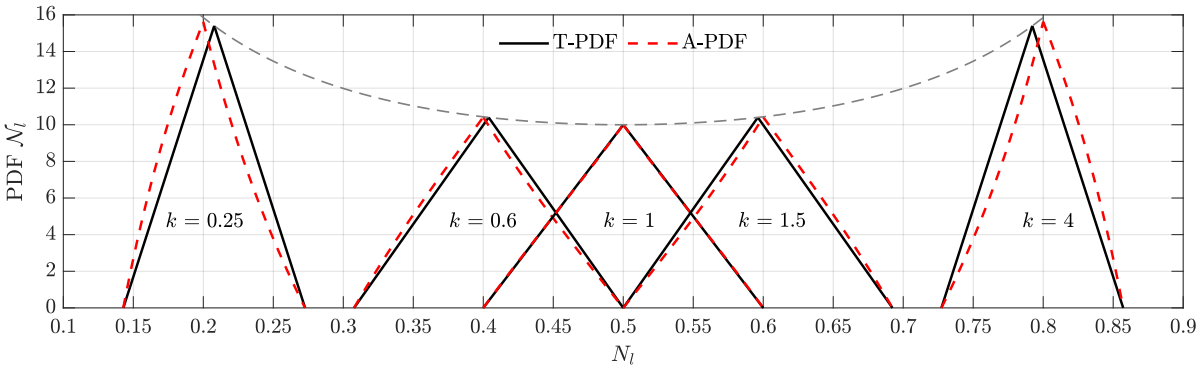


Figure 3.8: Actual and approximated triangular PDF of the converter leg power with different k.

Once the PDF of a random variable is available, one can determine both its expected value E and its standard deviation σ. Determining E and σ of the PDF reported in (3.16) might not be trivial, however, further considerations may be drawn by looking at Fig. 3.8. Fig. 3.8 shows the plots of $\mathcal{N}_l$, i.e., A-PDF, with different inductance ratios. It is evident that the shape of the A-PDF resembles that of a triangle, i.e., it can be approximated with a symmetric T-PDF. The parameters governing the resulting symmetric triangular distribution can be defined in relation to the factor k as:

$$\begin{aligned} &\text{Lower limit} \quad a = \frac{P_{\text{nom}}}{2}\frac{2k}{3+2k} \\ &\text{Upper limit} \quad b = \frac{P_{\text{nom}}}{2}\frac{3k}{2+3k} \quad \text{with} \\ &\text{Mode} \qquad\quad c = \frac{a+b}{2} \end{aligned} \tag{3.17}$$

$$k = \begin{cases} \dfrac{L_{3\text{u}}}{L_{2\text{u}}} & \text{for A} \\ \dfrac{L_{3\text{l}}}{L_{2\text{l}}} & \text{for B} \end{cases} \quad \text{and} \quad k = \begin{cases} \dfrac{L_{2\text{u}}}{L_{3\text{u}}} & \text{for C} \\ \dfrac{L_{2\text{l}}}{L_{3\text{l}}} & \text{for D} \end{cases} .$$

Based on the PDF given in (3.17), the expected value E^* and the standard deviation σ^* can be obtained as:

$$E^* = c \,, \qquad \sigma^* = \frac{b-a}{2\sqrt{6}} \,. \tag{3.18}$$

Looking at Fig. 3.8, one may see that the A-PDF in the $k = 1$ case perfectly matches the T-PDF. In the other cases (e.g., $k = 0.25, 0.6, 1.5, 4$, according to the figure), however, a slight deviation of the A-PDF from the approximated T-PDF may be observed. This discrepancy is all the more pronounced the further k moves away from unity.

3.4.2 Bridge Power PDF

The power processed by each bridge (the bridges are denoted as Bridge 2 and Bridge 3 in Fig. 3.4) can be determined as $P_2 = P_{\text{A}} + P_{\text{B}}$ and $P_3 = P_{\text{C}} + P_{\text{D}}$, and the normalized form can be obtained as $N_2 = N_{\text{A}} + N_{\text{B}}$ and $N_3 = N_{\text{C}} + N_{\text{D}}$. Considering that leg normalized powers are independent random variables, the PDF of the normalized bridge power $\mathcal{N}_b$ can be determined through convolution (see: [93]) as:

$$\begin{aligned} \mathcal{N}_2(x) &= \mathcal{N}_{\text{A}}(x) * \mathcal{N}_{\text{B}}(x) \\ \mathcal{N}_3(x) &= \mathcal{N}_{\text{C}}(x) * \mathcal{N}_{\text{D}}(x) \end{aligned} \,. \tag{3.19}$$

Assuming the same inductance ratio k for legs pertaining to the same bridge and taking advantage of T-PDF symmetry, it is possible to express

(3.19) as an Irwin–Hall distribution of the fourth order (see: [94]):

$$\mathcal{N}_b(x)=\begin{cases}\dfrac{b-a}{12}z^3 & x\in[2a,a+c]\\ \dfrac{b-a}{12}(-3z^3+12z^2-12z+4) & x\in[a+c,2c]\\ \dfrac{b-a}{12}(3z^3-24z^2+60z-44) & x\in[2c,b+c]\\ \dfrac{b-a}{12}(4-z)^3 & x\in[b+c,2b]\end{cases} \tag{3.20}$$

$$\text{having} \qquad z=\frac{2(x-2a)}{b-a},$$

$$k=\frac{L_{3u}}{L_{2u}}=\frac{L_{3l}}{L_{2l}} \quad \text{for Bridge 2,}$$

$$k=\frac{L_{2u}}{L_{3u}}=\frac{L_{2l}}{L_{3l}} \quad \text{for Bridge 3.}$$

Based on the PDF given in (3.20), the expected value E^* and the standard deviation σ^* can be obtained as:

$$E^*=2c\,, \qquad \sigma^*=\frac{b-a}{\sqrt{12}}\,. \tag{3.21}$$

As foreseeable, the expected value of the PDF associated with the bridge power is twice that of the leg power. Conversely, the standard deviation of the bridge PDF is $\sqrt{2}$ times higher than that of the legs.

3.4.3 Numerical Validations

To validate the above considerations, the converter of Fig. 3.4 is simulated 30k times on the PLECS (Plexim GmbH) environment, considering uniformly distributed randomized inductances, as shown in Table 3.1. In the analysis, three distinct cases (10k simulations each) were defined:

- **Case 1**: Bridge 2 (active) processes 40% of the nominal output power while Bridge 3 (passive) processes the remaining 60%.
- **Case 2**: Bridge 2 (active) processes 50% of the nominal output power while Bridge 3 (passive) processes the remaining 50%.

Table 3.1: Numerical plant main system parameters.

Parameter		Symbol	Value	Unit
Input voltage		V_{dc}	200	V
Voltage gain		m	0.5	-
Turn ratio		n	1	-
Nominal output power		P_{nom}	1475	W
Switching frequency		f_{sw}	20	kHz
Case 1	Inductances	L_1	38 ± 20%	μH
		L_{2u}, L_{2l}	15 ± 20%	μH
		L_{3u}, L_{3l}	10 ± 20%	μH
Case 2	Inductances	L_1	40 ± 20%	μH
		L_{2u}, L_{2l}	10 ± 20%	μH
		L_{3u}, L_{3l}	10 ± 20%	μH
Case 3	Inductances	L_1	34 ± 20%	μH
		L_{2u}, L_{2l}	40 ± 20%	μH
		L_{3u}, L_{3l}	10 ± 20%	μH

- **Case 3**: Bridge 2 (active) processes 20% of the nominal output power while Bridge 3 (passive) processes the remaining 80%.

PLECS Script

The power data was obtained from PLECS simulations by applying a uniform distribution of the coupling inductors. The complete simulation script is reported in Appendix A.1 for reference.

Fig. 3.9 illustrates the numerical validation of the normalized power distribution among each leg (A, B, C, D). The A-PDF, represented as a dashed red line and described by (3.16), perfectly aligns with the histogram data across all the cases. However, a slight deviation is noticeable between the T-PDF (solid line) and A-PDF in Case 1 and Case 3, as predicted in section 3.4.1. Furthermore, in Case 1, there is an additional power demand of +25% and +15% in each leg of Bridge 2 and Bridge 3, respectively. In Case 2, all legs experience a +20% additional power demand, whereas in Case 3, each leg of Bridge 2 and Bridge 3 faces a +35% and +10% additional power demand, respectively, in the worst-case scenario. This additional power demand necessitates the oversizing of silicon devices, potentially jeopardizing the converter's partial-scale feature.

As summarized in Table 3.2, the theoretical expected values E^* and standard deviations σ^* provided in (3.18) fairly match with the numerical acquisitions E and σ in Case 2. This alignment can be visually observed from the adequate fitting of the proposed T-PDF over the data histograms, as shown in Fig. 3.9. However, in Case 1 and Case 3, notable differences

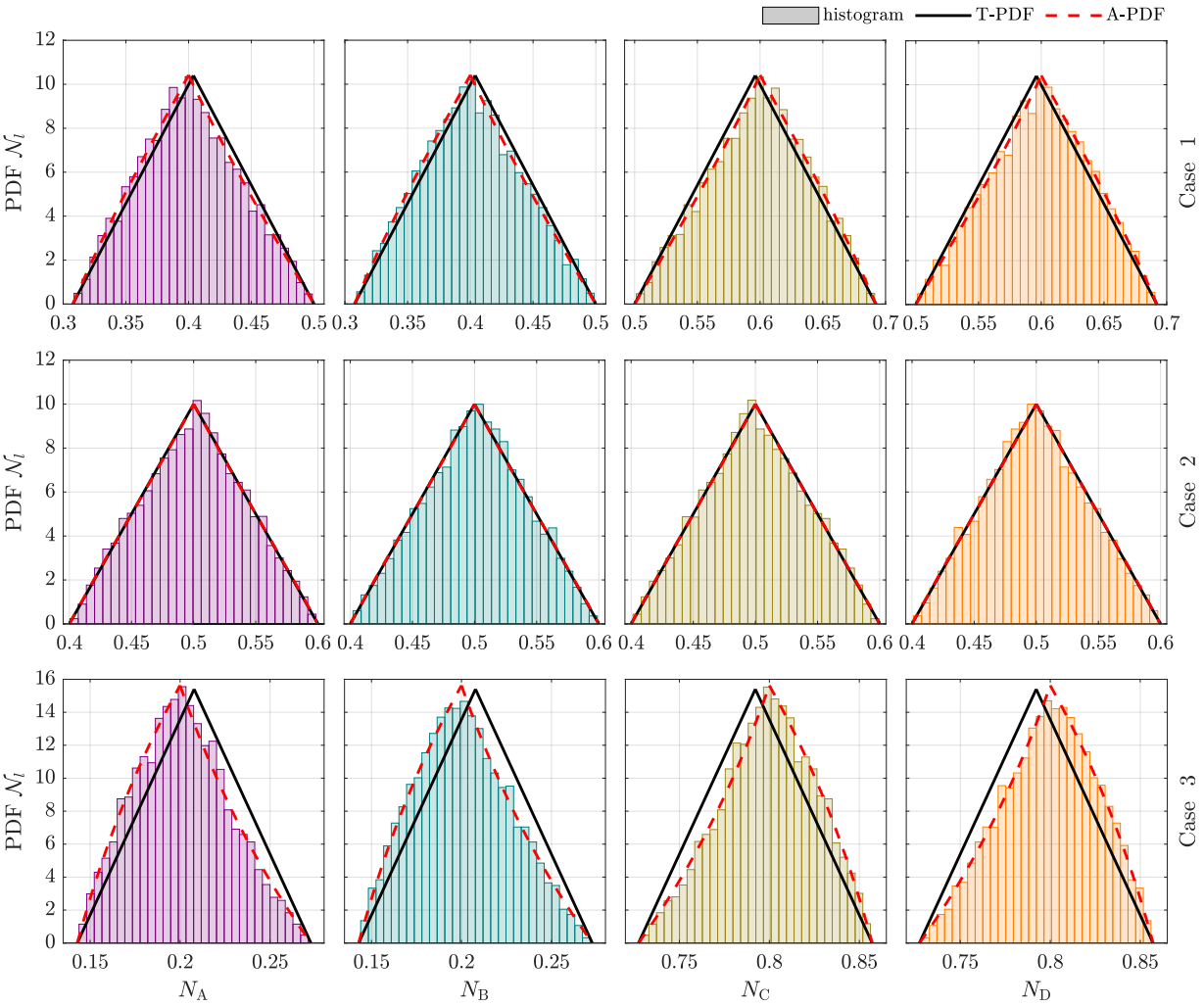


Figure 3.9: Numerical power distribution together with actual and approximated triangular PDFs of the normalized leg power. Legs A, B, C, and D from left to right. Case 1, 2, and 3 from top to bottom.

Table 3.2: Statistical analysis of measured and predicted powers in each leg.

	Leg	A	B	C	D	Unit
Case 1	E^*	297.8	297.8	439.7	439.7	W
	E	295.5	295.8	442.0	442.8	W
	σ^*	28.95	28.95	28.95	28.95	W
	σ	29.17	29.19	29.17	29.19	W
	RMSD	5.646	5.660	6.790	6.742	mW
Case 2	E^*	368.7	368.7	368.7	368.7	W
	E	368.8	368.8	368.8	368.8	W
	σ^*	30.10	30.10	30.10	30.10	W
	σ	30.30	29.81	30.30	29.81	W
	RMSD	6.135	6.111	6.103	6.093	mW
Case 3	E^*	153.2	153.2	584.2	584.2	W
	E	148.3	148.1	589.2	589.4	W
	σ^*	19.55	19.55	19.55	19.55	W
	σ	19.14	19.41	19.14	19.41	W
	RMSD	2.878	2.900	6.290	6.248	mW

Table 3.3: Statistical analysis of measured and predicted powers on the secondary-side bridges.

	Bridge	2	3	Unit
Case 1	E^*	595.7	879.3	W
	E	591.2	883.7	W
	σ^*	40.94	40.94	W
	σ	41.42	41.42	W
	RMSD	8.938	11.63	mW
Case 2	E^*	737.5	737.5	W
	E	738.0	736.9	W
	σ^*	42.57	42.57	W
	σ	42.76	42.76	W
	RMSD	10.15	10.09	mW
Case 3	E^*	306.5	1168.5	W
	E	296.4	1178.6	W
	σ^*	27.64	27.64	W
	σ	27.49	27.49	W
	RMSD	4.544	12.02	mW

between the theoretical and numerical expected values and standard deviation values emerge due to the discrepancy introduced by the approximated T-PDF outlined in (3.17).

As detailed in Section 3.4.2, the power flow in each bridge is characterized by the Irwin-Hall distribution, obtained through convolution of the approximated T-PDFs relevant to each converter's leg. Thus, in Fig. 3.10, the normalized power distributions related to Bridge 2 and Bridge 3 are depicted. The PDF, represented by a solid line, aligns perfectly with the histogram data in Case 2. However, a slight deviation is noticeable in Case 1 and Case 3, attributed to the considered approximation. These discrepancies are also observed in the theoretical expected values E^* and standard deviations σ^* (3.21) compared to the numerical values, as shown in Table 3.3.

Furthermore, the root mean square deviation (RMSD) between the measured power and the predicted one is provided for each leg in Table 3.2, and for each bridge in Table 3.3. As visible, RMSD absolute values present milliwatts order of magnitude. Such a deviation is in the range of 10 to 20 ppm, and it can be almost exclusively attributed to numerical errors in all cases. This is compelling evidence that the theoretical developments (3.8) are in good match with the numerical validation,

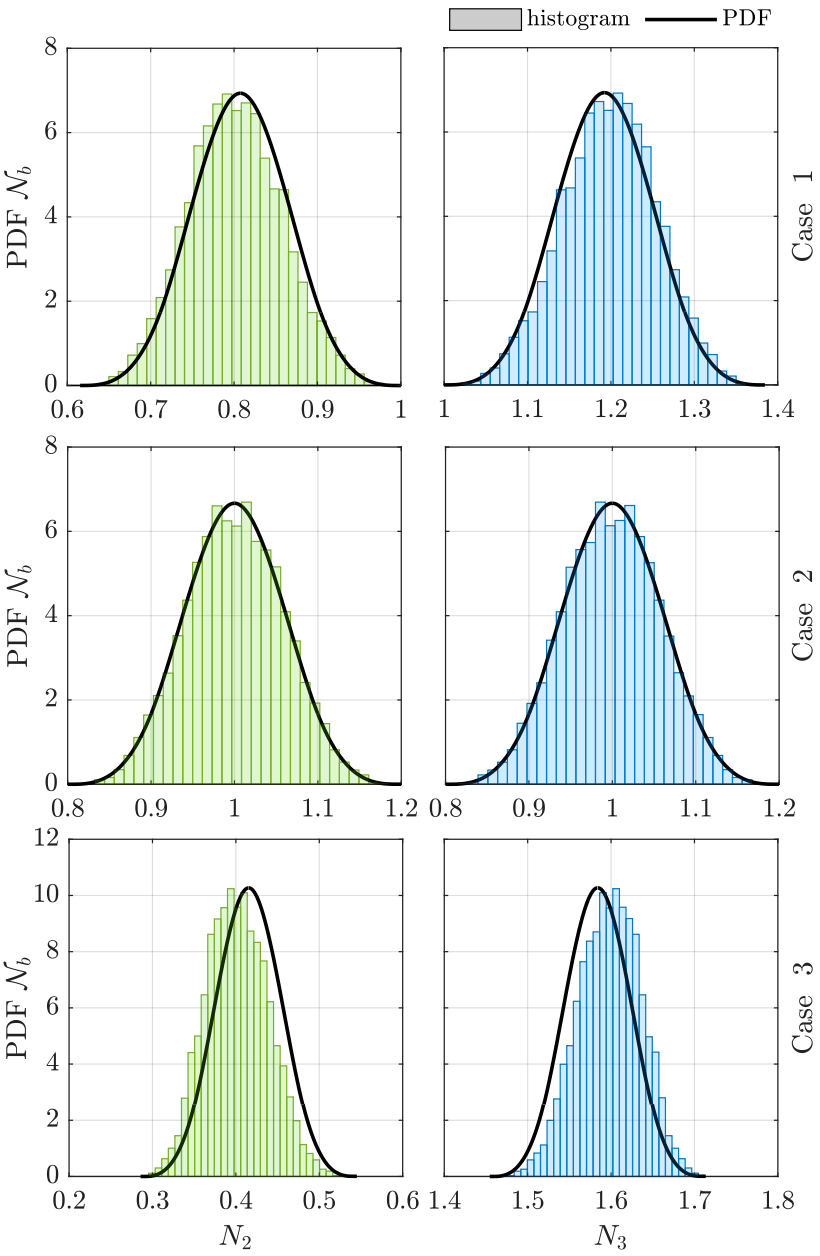


Figure 3.10: Numerical power distribution together with approximated Irwin-Hall PDF of the normalized bridge power. Bridges 2 and 3 from left to right. Case 1, 2, and 3 from top to bottom.

affirming the accuracy and reliability of the presented approach under non-ideal conditions.

The statistical results obtained from the large-scale numerical simulations, together with the corresponding histograms, clearly demonstrate that even minor variations in the magnetic components, such as the tolerances of the coupling inductors, lead to noticeable deviations from the idealized power distribution. As a consequence, the inherent balance expected from passive devices is lost, resulting in unequal allocation of power between the partial-scale active and diode bridges. This imbalance not only undermines the reliability of passive power sharing but also imposes additional thermal stress on specific branches, ultimately jeopardizing the converter's partial-scale feature. Therefore, these findings strongly highlight the necessity of introducing an active power sharing mechanism to ensure predictable operation and robust performance of the AB-DC/DC converter under realistic component tolerances. Thus, in

the following section, active-power-sharing control that enables power transfer from the diode bridge to the active bridge will be discussed.

3.5 Active Power Sharing Control

As introduced in Section 3.4.2, the power handled by each secondary bridge can be expressed as $P_2 = P_A + P_B$ and $P_3 = P_C + P_D$, where P_A, P_B, P_C, and P_D are defined in (3.8). Using the general power expression in (3.2), the sharing of output power between the active and diode bridges can be derived from simple inductive current division:

$$\begin{aligned} P_2 &= \frac{P_o}{2}\left(\frac{L_{3u}}{L_{2u}+L_{3u}} + \frac{L_{3l}}{L_{2l}+L_{3l}}\right) = P_o\frac{1}{1+k} \\ P_3 &= \frac{P_o}{2}\left(\frac{L_{2u}}{L_{2u}+L_{3u}} + \frac{L_{2l}}{L_{2l}+L_{3l}}\right) = P_o\frac{k}{1+k} \end{aligned}, \tag{3.22}$$

where P_2 and P_3 denote the powers of the active bridge and diode bridge, respectively. The power sharing ratio is then defined as

$$k_p = \frac{P_3}{P_2} = k, \tag{3.23}$$

with k determined by the coupling inductance ratio:

$$k = \frac{L_{2u}}{L_{3u}} = \frac{L_{2l}}{L_{3l}}\,. \tag{3.24}$$

If the ratio is instead defined in reverse (e.g., $k = L_{3u}/L_{2u}$), the roles of P_2 and P_3 are exchanged accordingly; however, the resulting expressions preserve the same final outcome. Equation (3.22) therefore extends the single active bridge (SAB) case to the more general AB-DC/DC structure by incorporating the passive current division imposed by the coupling inductors.

However, as highlighted in the numerical analysis of Section 3.4.3, even small deviations in the actual inductor values (e.g., due to manufacturing tolerances) lead to $k \neq k_p$. In such cases, the inherent passive power distribution between the active and diode bridges is no longer guaranteed. This motivates the introduction of an active power-sharing control strategy to ensure reliable and balanced operation.

In the proposed modulation technique, active power-sharing control is achieved by turning on the MOSFETs of the secondary side active bridge for a time cT_{sw} [88]. This approach introduces a parameter c, which reduces the time the diode bridge is conducting. For the diodes, the turn-on delay, cT_{sw}, facilitates the power shift from the passive bridge to the active one. The novel modulation technique, characterized by $c \neq 0$, expands the operating regions and introduces new modes, including a revised DCM, two hybrid modes, a CCM with no control, and the DAB mode over the active power-sharing. Based on this operating principle, the boundary conditions for these regions are discussed in the following sections. In the subsequent subsections, the subscripts 'DCM', 'h1', 'h2', 'CCM', and 'DAB' are used to distinguish the power contributions corresponding to each operating region.

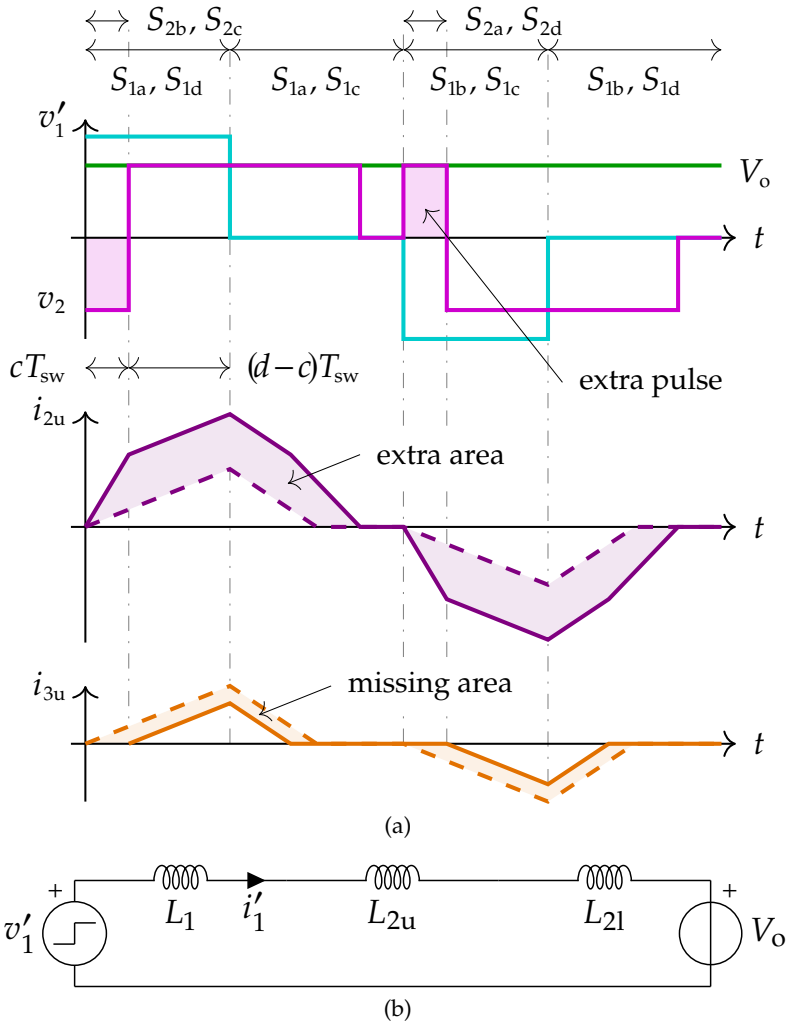


Figure 3.11: PSFB power shift operation in forward mode: (a) main voltage and current waveforms; (b) equivalent circuit from the transformer secondary side.

3.5.1 Discontinuous Conduction Mode Region

As foreseeable from (3.2) and (3.22), the power processed from the diode-bridge is directly proportional to the area underneath the current trace i_{3u}. The active-bridge is operated using the modulation visible in Fig. 3.11 to reduce the power processed from the diode-bridge. Such a technique introduces a pulse in the voltage v_2 opposite to the one of the input bridge, leading to a turn-on delay cT_{sw} of the diodes. Therefore, the diode-bridge operates similarly to what is described in section 3.3 with the sole difference that the triggering pulse lasts $(d-c)T_{sw}$ instead of dT_{sw} leading to:

$$P_{3,DCM} = \frac{V_{dc}^2(1-m)}{L_{eq}f_{sw}} \frac{(d-c)^2 k}{1+k} . \tag{3.25}$$

Turn-on delay cT_{sw} is the cause of the missing area that leads to the reduction of the power processed by the diode-bridge.

The analysis of the active-bridge is more complicated due to the extra-area visible in Fig. 3.11(a) introduced by the modulation technique. However, the area can be split into two components respectively generated by the diode commutations and the one given by the active-bridge pulses. The former can be quickly obtained with the same approach discussed for

$P_{3,\mathrm{DCM}}$ and it gives:

$$P'_{2,\mathrm{DCM}} = \frac{(1-m)V_{\mathrm{dc}}^2}{L_{\mathrm{eq}} f_{\mathrm{sw}}} \frac{(d-c)^2}{1+k} \,. \tag{3.26}$$

On the other hand, the one given by the active-bridge pulses can be derived by looking at the equivalent circuit of Fig. 3.11(b). In particular, input and output are connected by means of active switches passing through inductors L_1, $L_{2\mathrm{u}}$, and $L_{2\mathrm{l}}$. The active-bridge inductance in the time interval cT_{sw} becomes $L_{12} = L_1 + L_{2\mathrm{u}} + L_{2\mathrm{l}}$. Therefore, the power component can be calculated as:

$$P''_{2,\mathrm{DCM}} = \frac{2}{T_{\mathrm{sw}}} \int_0^{T_{\mathrm{sw}/2}} v'_1 i_1 dt = \frac{2V_{\mathrm{dc}}^2}{T_{\mathrm{sw}}} \frac{1-m}{L_{12}} \left[\int_0^{cT_{\mathrm{sw}}} t \, dt + \int_{cT_{\mathrm{sw}}}^{dT_{\mathrm{sw}}} \frac{c}{f_{\mathrm{sw}}} dt \right] . \tag{3.27}$$

The total power of the active-bridge can be calculated from (3.26) and (3.27) as:

$$P_{2,\mathrm{DCM}} = P'_{2,\mathrm{DCM}} + P''_{2,\mathrm{DCM}} = \frac{V_{\mathrm{dc}}^2(1-m)(d-c)^2}{L_{\mathrm{eq}} f_{\mathrm{sw}}(1+k)} + \frac{V_{\mathrm{dc}}^2(1+m)(2cd-c^2)}{L_{12} f_{\mathrm{sw}}} \,. \tag{3.28}$$

It is evident that by playing with parameters c and d, the power of the diode- and active-bridge can be tuned according to (3.25) and (3.28). In particular, compared with the base scenario (3.22), power $P_{2,\mathrm{DCM}}$ of the active-bridge can be increased while power $P_{3,\mathrm{DCM}}$ processed by the diode-bridge is reduced. If $c = 0$, (3.25) and (3.28) revert to the base scenario (3.22) while if $c = d$ the diode-bridge can be completely shut-down (i.e., $P_{3,\mathrm{DCM}} = 0$). Employing the proposed modulation, the power sharing ratio k_{p} does not necessarily coincide anymore with the coupling inductance ratio k. In fact, it can range the diapason $0 \le k_{\mathrm{p}} \le k$ according to the chosen values of c and d. It is important to note that the extra pulse on the v_2 and power equations of the partial scale bridges is valid exclusively for this region, with the boundary condition specified as:

$$\mathrm{DCM:} \begin{cases} 0 \le c \le d & \text{if } 0 \le d \le \dfrac{m}{4} \\ 0 \le c \le \dfrac{1}{4} - \dfrac{d}{2m} & \text{if } \dfrac{m}{4} \le d \le \dfrac{m}{2} \end{cases} . \tag{3.29}$$

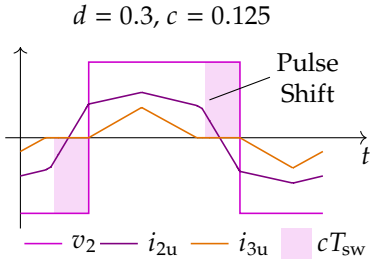


Figure 3.12: Voltage and current waveforms in Hybrid 1 region.

3.5.2 Hybrid 1 Region

Fig. 3.12 illustrates the Hybrid 1 region, with $d = 0.3$ for $c = 0.125$. The active bridge operates as CCM in this region, while the diode bridge remains in the same DCM as in the earlier operating region. The power processed by the active and diode bridges can be derived following the same methodology outlined for the DCM region, with the appropriate adjustment of the integration intervals to account for the different conduction patterns. Consequently, the power processed by the active bridge and diode bridge is given as:

$$P_{2,\mathrm{h1}} = \frac{V_{\mathrm{dc}}^2(1-m)(d-c)^2}{L_{\mathrm{eq}} f_{\mathrm{sw}}(1+k)} + \frac{V_{\mathrm{dc}}^2\left[2cd - d^2 + 0.5dm - c^2(1+m)\right]}{L_{12} f_{\mathrm{sw}}} \,, \tag{3.30}$$

$$P_{3,\mathrm{h1}} = \frac{V_{\mathrm{dc}}^2(1-m)}{L_{\mathrm{eq}} f_{\mathrm{sw}}} \frac{(d-c)^2 k}{1+k} \,. \tag{3.31}$$

Notice that the power processed by the diode bridge is identical to that in the DCM region, $P_{3,\mathrm{DCM}} = P_{3,\mathrm{h1}}$. Moreover, when $c = 0$, the total power transfer of the converter depends on the relationship between d and m. When $d < m/2$, the total power corresponds to the DCM case, as described in (3.2). Conversely, when $d \geq m/2$, power transfer aligns with the (3.2) CCM case. In both scenarios, power is shared between the two partial-scale bridges according to (3.22). Furthermore, in this region, the extra pulse v_2 caused by the turn-on delay cT_{sw} leads to the pulse shift. The converter continues to operate in this region as long as the following boundary condition is satisfied:

$$\text{Hybrid 1:} \begin{cases} \dfrac{1}{4} - \dfrac{d}{2m} < c \leq d & \text{if } 0 \leq d \leq \dfrac{m}{2} \\ \dfrac{2d-m}{2-2m} < c \leq d & \text{if } \dfrac{m}{2} \leq d \leq 0.5 \end{cases} . \tag{3.32}$$

3.5.3 Hybrid 2 Region

Fig. 3.13 illustrates the Hybrid 2 region, with $d = 0.3$, and $c = 0.05$. As noticed, the turn-on delay cT_{sw} causes the diode bridge to continue operating in DCM, while the active bridge operates in CCM. The power processed by the diode bridge and the active bridge are different with respect to the hybrid 1 and DCM regions due to the different current waveform shape. The active bridge power $P_{2,\mathrm{h2}}$ is given in (3.33) while diode bridge power is:

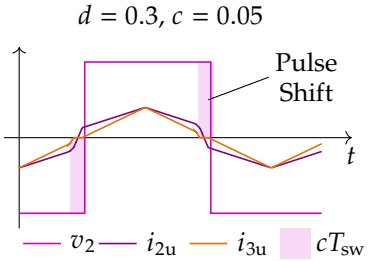


Figure 3.13: Voltage and current waveforms in Hybrid 2 region.

$$P_{3,\mathrm{h2}} = \frac{V_{\mathrm{dc}}^2}{L_{\mathrm{eq}} f_{\mathrm{sw}}} \frac{\{(d-c)^2 - x^2 - m[(d-c)^2 + x^2]\}k}{1+k} \,, \tag{3.34}$$

where x and t are defined as:

$$x = \frac{d - c + (c-0.5)m}{1+m} \,, \tag{3.35}$$

$$t = \frac{d + (2c-0.5)m - 2x(1+m)}{2(1+m)} \,. \tag{3.36}$$

When $c = 0$, the total power transfer aligns with the (3.2) (i.e., CCM case), and the power sharing among the partial scale bridges can be obtained by (3.22). The converter continues to operate in this region as long as the following boundary condition is satisfied:

$$\text{Hybrid 2:} \left\{ \frac{d}{2} - \frac{m}{4} \leq c \leq \frac{2d-m}{2-2m} \quad \text{if } \frac{m}{2} \leq d \leq 0.5 \,. \right. \tag{3.37}$$

$$P_{2,\mathrm{h2}} = \frac{V_{\mathrm{dc}}^2\{(d-c)^2 - x^2 - m[(d-c)^2 + x^2]\}}{L_{\mathrm{eq}} f_{\mathrm{sw}}(1+k)} + \frac{V_{\mathrm{dc}}^2(1+m)[(c-x-t)^2 - t^2 + 2(c-x-t)(d-c-x)]}{L_{12} f_{\mathrm{sw}}} \,. \tag{3.33}$$

3.5.4 Continuous Conduction Mode Region

For high values of d, delaying the passive bridge is not feasible. Consequently, the turn-on delay, cT_{sw}, has no effect on the diode bridge current i_{3u}, leading to no control over active power sharing. Thus, the converter operates in a conventional CCM mode, as shown in Fig. 3.14. The power transfer in this mode follows the equations provided below:

$$P_{2,\mathrm{CCM}} = \frac{mV_{dc}^2}{L_{eq}f_{sw}(1+k)}\left[\frac{d}{2}(1-d)-\frac{m^2}{8}\right], \tag{3.38}$$

$$P_{3,\mathrm{CCM}} = \frac{mV_{dc}^2 k}{L_{eq}f_{sw}(1+k)}\left[\frac{d}{2}(1-d)-\frac{m^2}{8}\right], \tag{3.39}$$

as long as:

$$\text{CCM: } \begin{cases} 0 \le c \le \dfrac{d}{2}-\dfrac{m}{4} & \text{if } \dfrac{m}{2} \le d \le 0.5 \end{cases}. \tag{3.40}$$

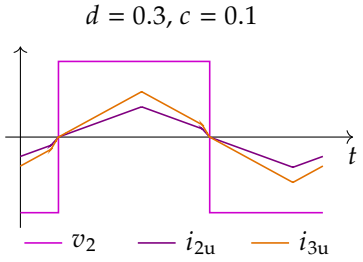


Figure 3.14: Voltage and current waveforms in CCM region.

3.5.5 Dual-Active-Bridge Region

As mentioned, when $c \ge d$, the diode bridge is completely shut down, and the converter transitions into DAB mode. The phase shift d is given between the legs of the primary bridge, while c represents the duty cycle applied to the secondary-side active bridge. In this configuration, the secondary-side active bridge is fully responsible for power transfer, while the diode-bridge current i_{3u} remains zero.

The resulting current waveform of the active bridge, i_{2u}, are shown in Figs. 3.15 and 3.16 for representative cases of $d = 0.15$, $d = 0.3$, and $c = 0.35$. Depending on the relative values of c and d, the converter can operate in either forward or reverse power flow, which are illustrated in the figure as DAB-FM (forward mode) and DAB-RM (reverse mode), respectively.

The power transferred in this mode is given by:

$$P_{2,\,\mathrm{DAB}} = \frac{V_{dc}^2(1+m)\left[(d-y)^2-y^2\right]}{L_{12}f_{sw}}, \tag{3.41}$$

where y is defined as:

$$y = \frac{d+m(2c-0.5)}{2(1+m)}. \tag{3.42}$$

This expression is valid for all values of $c \ge d$, where the diode bridge is inactive. However, the direction of power flow in the DAB mode depends on the relative values of c and d. Specifically, the power transfer can be characterized as:

$$\begin{cases} P_{2,\,\mathrm{DAB}} > 0, & \text{if } \dfrac{d}{2}+\dfrac{1}{4} > c \ge d \quad \text{(DAB-FM)}, \\ P_{2,\,\mathrm{DAB}} < 0, & \text{if } \dfrac{d}{2}+\dfrac{1}{4} < c < 0.5 \quad \text{(DAB-RM)}. \end{cases} \tag{3.43}$$

In DAB-FM, power flows from the primary to the secondary, while in DAB-RM, power reverses from the secondary to the primary. Both conditions remain valid within the DAB mode region defined by $c \ge d$.

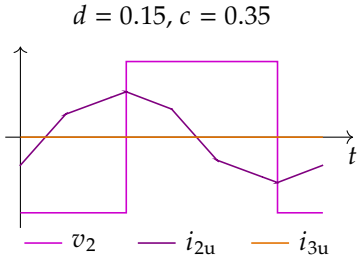


Figure 3.15: Voltage and current waveforms in DAB-RM region.

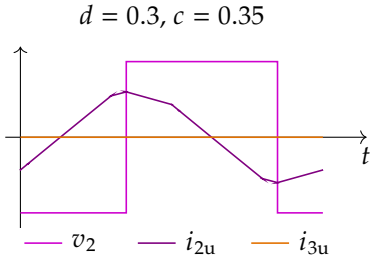


Figure 3.16: Voltage and current waveforms in DAB-FM region.

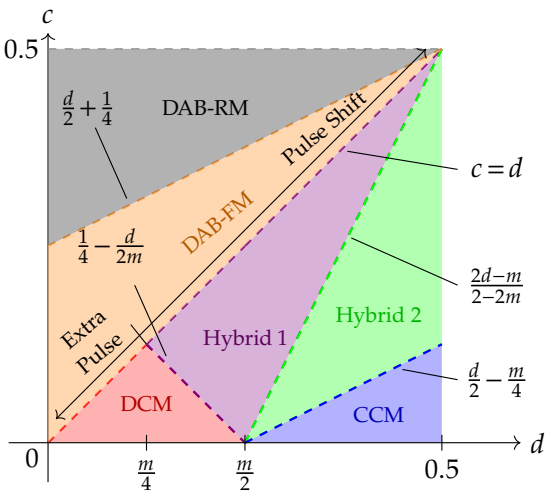


Figure 3.17: Operating conditions of the AB-DC/DC converter under active power-sharing control.

The complete boundary map of all operating regions is illustrated in Fig. 3.17 on the d–c plane. It outlines six distinct regions: DCM, hybrid 1, hybrid 2, CCM, DAB-FM, and DAB-RM, each governed by its respective boundary condition. The figure clearly highlights the occurrence of extra pulses in the DCM region, pulse shifts in the hybrid regions, and the diode bridge shutdown condition ($c \geq d$) in DAB mode. The transition from forward to reverse power flow within DAB mode is also indicated by the boundary $c = \frac{d}{2} + \frac{1}{4}$.

3.5.6 Numerical Validations

The converter shown in Fig. 3.4 is simulated in PLECS (Plexim GmbH) using the parameters listed in Table 3.4 to validate the proposed modulation strategy. The accuracy of the theoretical power formulations is verified through numerical simulations for both the active bridge power P_2 and the diode bridge power P_3. Fig. 3.18(a) illustrates the total input power. Whereas in Fig. 3.18(b), the comparison between the calculated and simulated values of P_2 demonstrates excellent agreement across all four operating regions. The data points align close to the bisecting line, indicating minimal deviation throughout the power range. To quantify this agreement, the coefficient of determination R^2 has been computed and is reported in Table 3.5. In all operating regions, R^2 exceeds 0.9, thereby validating the accuracy of the derived expressions. Similarly, Fig. 3.18(c) presents the comparison between

PLECS Script

The diode-bridge and active-bridge powers across all operating regions were obtained from simulations by sweeping the parameters c and d according to their respective boundary conditions. The complete MATLAB and PLECS simulation script is provided in Appendix A.2 for reference.

Table 3.4: Main parameters of the AB-DC/DC converter.

Parameters	Symbol	Value	Unit
Input voltage	V_{dc}	200	V
Switching frequency	f_{sw}	100	kHz
Voltage gain	m	0.5	-
Turn ratio	n	1	-
Leakage inductance	L_1	81.7	μH
Coupling inductance	$L_{2\text{u}}$	41.7	μH
	$L_{2\text{l}}$	41.2	μH
	$L_{3\text{u}}$	22.9	μH
	$L_{3\text{l}}$	25.8	μH
Coupling inductance Ratio	k	1.6 to 1.8	-

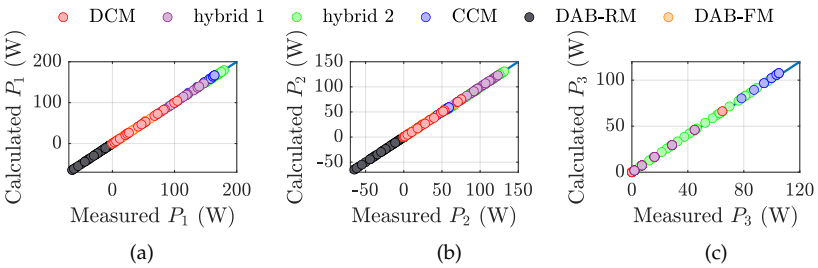


Figure 3.18: Comparison of measured and calculated powers: (a) input power P_1, (b) active bridge power P_2, and (c) diode bridge power P_3.

Table 3.5: Coefficient of determination of active and diode bridge powers in all the operating regions.

Region	R^2 - active bridge	R^2 - diode bridge
DCM	0.9995	0.9990
Hybrid 1	0.9981	0.9988
Hybrid 2	0.9964	0.9981
CCM	0.9754	0.9135
DAB-RM	0.9999	-
DAB-FM	0.9995	-

the theoretical and simulated results for the diode bridge power P_3. Once again, strong consistency is observed across all regions, with the predicted values closely matching the simulation data. In this case as well, R^2 values above 0.9 validate the proposed analytical model.

The parasitic components and magnetic tolerances discussed in [87] can lead to power imbalance between the parallel-connected bridges on the secondary side. However, the proposed modulation technique is specifically designed to compensate for these effects by adjusting the control parameter c, thereby maintaining balanced power sharing even in the presence of non-idealities.

3.5.7 Efficiency Analysis

The analytical efficiency of the proposed AB-DC/DC converter was evaluated in PLECS by incorporating detailed device models of the C3M0060075K1 SiC MOSFETs and C4D20120A Schottky diodes. The same modulation parameters (c, d) used for the analytical power calculations were employed for the efficiency analysis, ensuring a one-to-one correspondence between the operating points in the power and loss evaluations.

Fig. 3.19 presents the efficiency heatmap of the AB-DC/DC converter, where the efficiency is evaluated as a function of the control parameters c and d. The color distribution indicates the relative efficiency level, with warmer colors representing higher efficiency and cooler regions representing lower efficiency.

As observed, the converter achieves higher efficiency in the $c < d$ domain, which corresponds to the DCM, Hybrid 1, Hybrid 2, and CCM operating modes. In these regions, both the active and diode bridges participate in power transfer, and the switching transitions are predominantly low due to the lower c values, leading to minimized switching losses. Conversely, a noticeable reduction in efficiency is observed for $c \geq d$, which corresponds to the DAB operating region. Although this region allows complete diode-bridge shutdown and fully active power transfer, it is associated with higher circulating currents and increased switching losses, ultimately degrading the overall efficiency. Therefore, while operation in the $c \geq d$ region remains

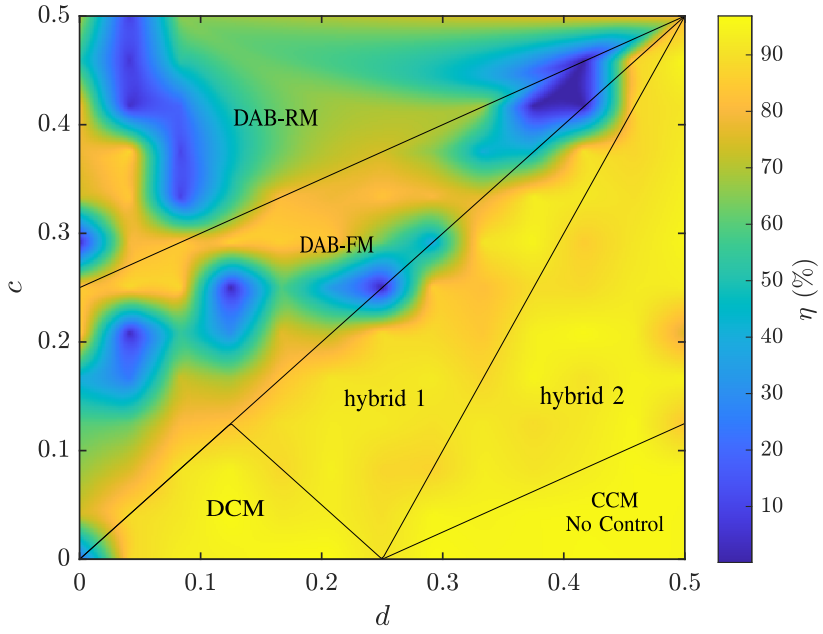


Figure 3.19: Thermal map showing converter efficiency (η) with respect to modulation parameters c and d.

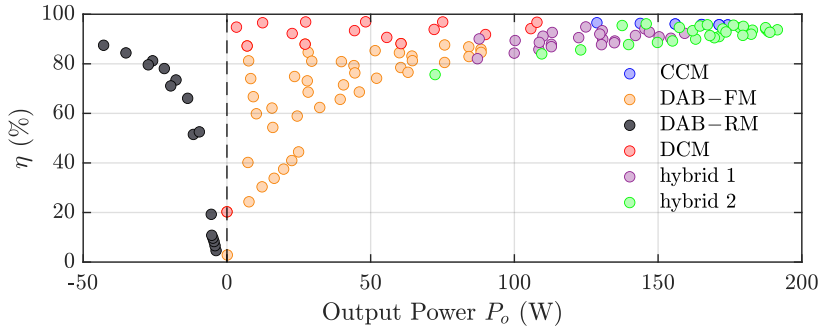


Figure 3.20: Scatter plot of converter efficiency (η) versus output power (P_o) across all operating regions.

feasible for bidirectional energy flow, it is not recommended for steady-state forward-mode operation where maximizing efficiency is the primary objective.

A clearer depiction of the converter performance across the operating power range is presented in Fig. 3.20. The two-dimensional plot shows the measured efficiency breakdown as a function of the output power P_o for each operating mode. It can be seen that the proposed active power-sharing control maintain consistently high efficiency, typically above 90%, over a wide range of output powers in DCM, Hybrid 1, Hybrid 2, and in CCM. In particular, the DCM region also demonstrates high efficiency at light load, primarily because of its reduced current conduction intervals, but is limited in its applicable power range. In contrast, the DAB regions (both forward and reverse modes) exhibit lower efficiency due to higher conduction and switching losses associated with simultaneous commutation of all MOSFETs.

From these results, it can be concluded that the proposed modulation strategy not only enables seamless power transfer from the diode bridge to the active bridge but also preserves the high-efficiency characteristics of the asymmetrical topology. The $c < d$ region is therefore the optimal operating domain for maximizing efficiency while ensuring balanced thermal loading between the active and diode bridges. The $c \geq d$ region, on the other hand, should be reserved for special operating cases, such as reverse power flow, where bidirectional energy transfer outweighs efficiency considerations.

Table 3.6: Selected operating conditions to validate voltage and current waveforms.

Region	c	d
DCM - conventional	0	0.20
CCM - conventional	0	0.35
DCM	0.05	0.15
Hybrid 1	0.35	0.40
Hybrid 2	0.35	0.45
CCM	0.10	0.46
DAB-RM	0.45	0.30
DAB-FM	0.35	0.30

3.5.8 Operation and Performance

The derived power expressions were validated over a wide range of c and d values across their respective boundary conditions. Whereas the current and voltage waveforms are provided for all regions based on c and d values summarized in Table 3.6.

Note that from Table 3.4, the designed coupling inductors result in a coupling inductance ratio k in the range of 1.6 to 1.8. As discussed in [87], under conventional operation, this ratio causes the secondary-side diode bridge to handle a greater portion of the power compared to the active bridge. Fig. 3.21 presents the simulated waveforms for all operating cases. In particular, Figs. 3.21(a) and 3.21(b), corresponding to conventional DCM and CCM, respectively, clearly show that the peak current of the diode bridge i_{3u} is higher than that of the active bridge i_{2u}. This confirms that the chosen coupling inductance ratio leads to greater power transfer through the diode bridge, thereby validating the passive power sharing mechanism.

Furthermore, in Fig. 3.21(a), both i_{2u} and i_{3u} are discontinuous, verifying operation in the DCM region. In contrast, Fig. 3.21(b) shows continuous currents for both branches, indicating CCM operation. These results further validate that the selected phase shifts $d = 0.2$ and $d = 0.35$, for a fixed voltage gain $m = 0.5$, satisfy the boundary conditions discussed in Section 3.5.

Figs. 3.21(c)–(h) illustrate the proposed modulation technique with active power sharing control, where the secondary-side active bridge MOSFETs are controlled using the diode turn-on delay parameter c. In Fig. 3.21(c), corresponding to the DCM region, the secondary-side voltage v_2 exhibits an extra pulse precisely within the shaded region defined by $c = 0.05$, as discussed in Section 3.5.1. Furthermore, the active bridge current i_{2u} exceeds the diode bridge current i_{3u}, confirming that active power sharing is achieved from the diode bridge to the active bridge.

In contrast, Fig. 3.21(d) represents the CCM region with $c = 0.10$ and $d = 0.46$. Here, the diode bridge current i_{3u} is higher than the active bridge current i_{2u}. Moreover, it can be observed that the waveforms in Fig. 3.21(b) and Fig. 3.21(d) are nearly identical, verifying that cT_{sw} has no effect on the diode bridge, leading to no control over active power sharing in this region, which is consistent with the developed modulation strategy.

Figs. 3.21(e) and 3.21(f) illustrate the Hybrid 1 and Hybrid 2 operating regions, respectively. In both cases, the active bridge current i_{2u} is higher than the diode bridge current i_{3u}, indicating effective active power sharing. Additionally, a pulse shift of duration cT_{sw} is clearly visible in both plots, highlighted as shaded regions, thereby verifying the functionality of the proposed modulation technique in these hybrid regions. Zoomed-in

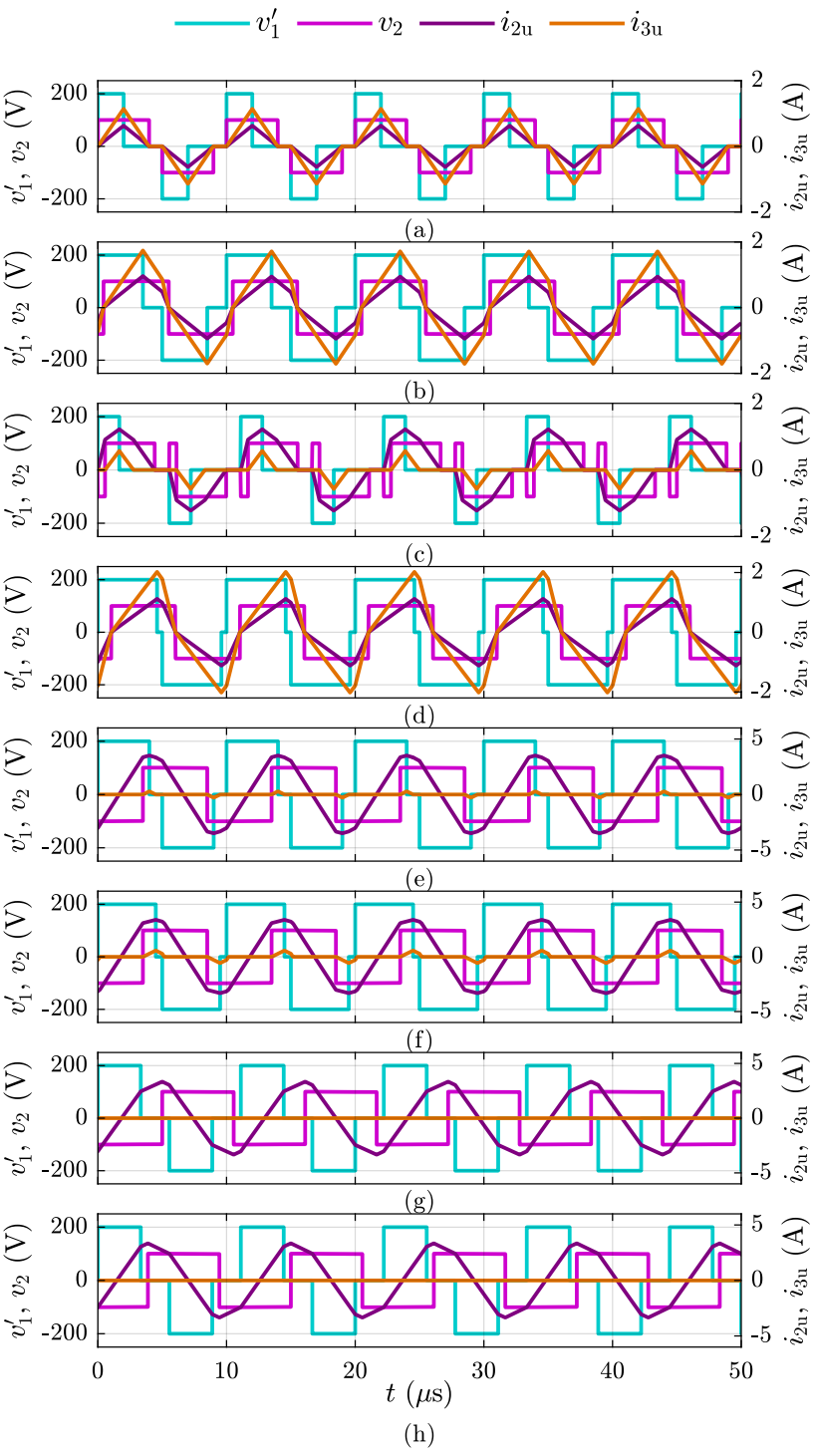


Figure 3.21: Simulated voltage and current waveforms for operating regions: (a) DCM-conventional; (b) CCM-conventional; (c) DCM; (d) CCM; (e) Hybrid 1; (f) Hybrid 2; (g) DAB-RM; (h) DAB-FM.

views of the diode bridge current i_{3u} waveforms are also included to emphasize the waveform shapes.

Finally, Figs. 3.21(g) and 3.21(h) correspond to the DAB-RM and DAB-FM regions, respectively. In both cases, since $c \geq d$, the diode bridge current i_{3u} is zero, confirming that the diode bridge is completely shut down and the converter operates as in DAB mode. Furthermore, closer observation of the active bridge current i_{2u} reveals different current slopes in Figs. 3.21(g) and 3.21(h), validating that the converter is operating in reverse and forward power flow modes, respectively.

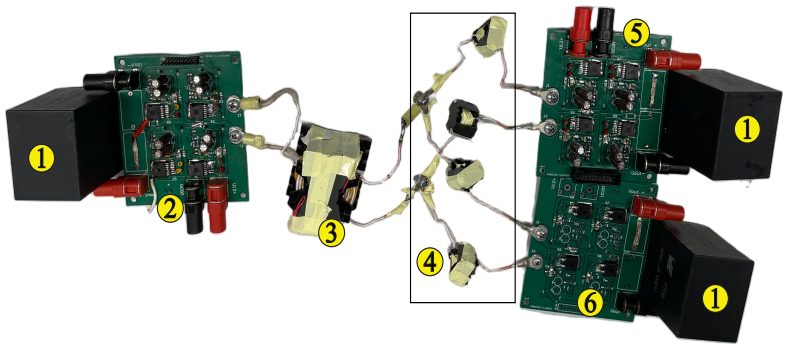


Figure 3.22: Experimental prototype: 1. DC-link capacitors; 2. primary-side active bridge; 3. high-frequency transformer; 4. coupling inductors; 5. secondary-side active bridge; 6. secondary-side diode bridge.

These simulation results confirm the feasibility of the proposed modulation approach. In the next section, experimental results are presented to validate the concept under real hardware conditions.

3.5.9 Experimental Validations

The experimental prototype of the converter, shown in Fig. 3.22, was implemented and operated using the system parameters summarized in Table 3.4 to validate the proposed modulation technique. The corresponding gate pulses were generated using the STM32G474RE microcontroller. All experimental results were obtained under open-loop control. The measured voltage and current waveforms for various operating regions are presented in Fig. 3.23. The results were recorded using an oscilloscope and exported in CSV format for post-processing, enabling a detailed comparison with the simulation waveforms.

Figs. 3.23(a) and 3.23(b) illustrate the conventional DCM and CCM operating regions, respectively. During these experiments, the MOSFETs of the secondary-side active bridge were disabled, allowing conduction through their body diodes. The measured voltage and current waveforms show good agreement with the simulation results. As expected, the secondary-side phase voltage v_2 exhibits oscillations during DCM operation due to the presence of parasitic elements. Furthermore, the diode bridge current i_{3u} is higher than the active bridge current i_{2u}, thereby confirming the passive power sharing behavior resulting from the selected coupling inductance ratio.

Figs. 3.23(c) and 3.23(d) correspond to the DCM and CCM operating regions under the proposed active power sharing modulation. In Fig. 3.23(c), the diode turn-on delay parameter is set to $c = 0.05$, which is relatively low and results in an unsuccessful or incomplete turn-on of the secondary-side MOSFETs. This effect is clearly visible in the form of an extra pulse on the secondary-side phase voltage v_2. As a result, the magnitude of the active bridge current i_{2u} appears lower than in the simulation, despite using identical operating parameters. Nevertheless, the diode bridge current i_{3u} remains lower than the active bridge current i_{2u}, confirming that active power sharing control is still effectively achieved in this DCM case.

In Fig. 3.23(d), which corresponds to the CCM region, the parameter cT_{sw} does not influence the diode bridge conduction, as discussed in Section 3.5.4. This leads to measured waveforms that closely resemble those in Fig. 3.23(b), further confirming that active power sharing is not engaged in this region, consistent with the intended behavior of the modulation strategy.

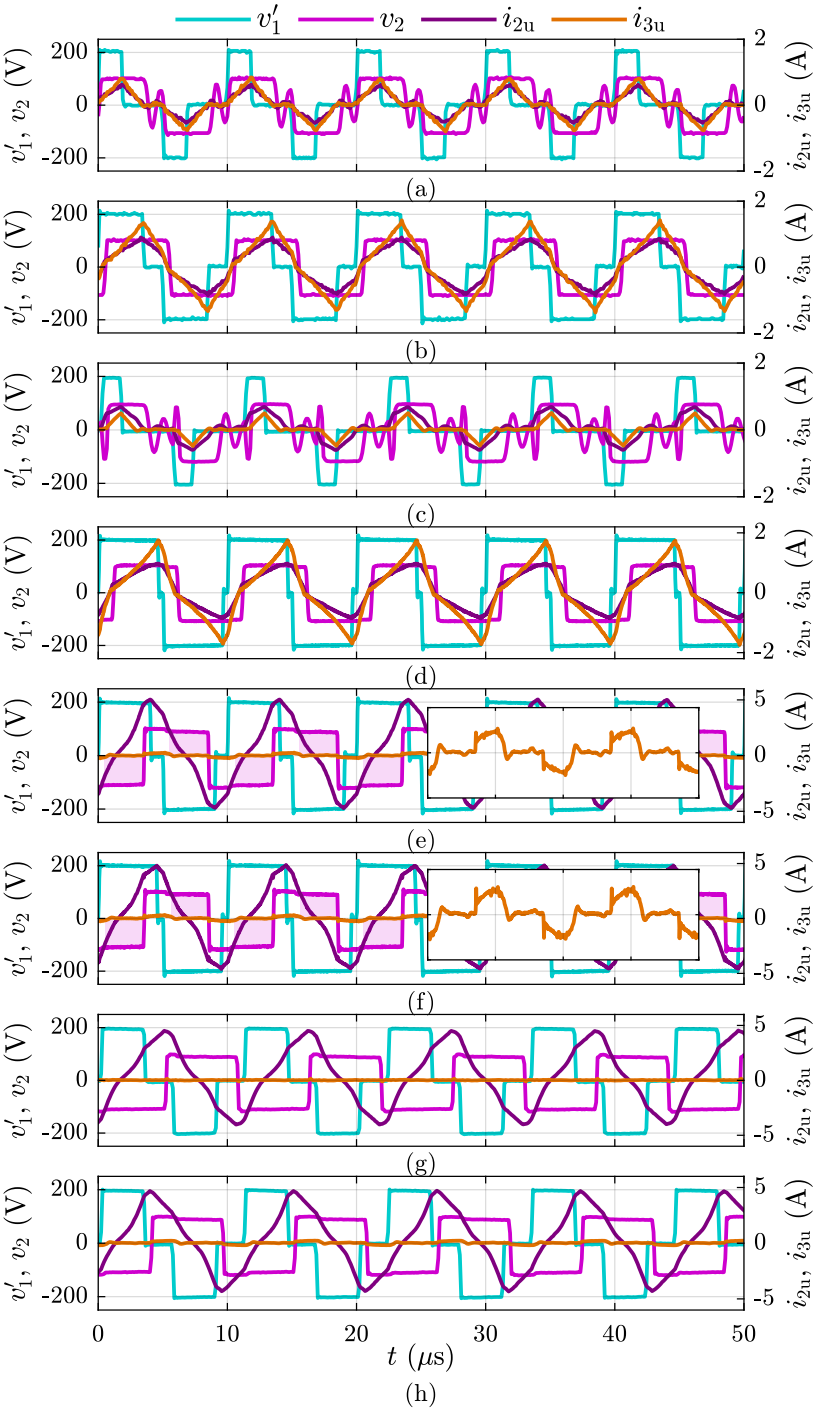


Figure 3.23: Experimental voltage and current waveforms for operating regions: (a) DCM-conventional; (b) CCM-conventional; (c) DCM; (d) CCM; (e) Hybrid 1; (f) Hybrid 2; (g) DAB-RM; (h) DAB-FM.

Figs. 3.23(e) and 3.23(f) show the experimental results for Hybrid 1 and Hybrid 2 regions, respectively. In both cases, active power sharing is evident, as the current through the active bridge i_{2u} is higher than that of the diode bridge i_{3u}. The pulse shift of duration cT_{sw} on the secondary-side voltage v_2 is clearly visible in both figures, validating the correct implementation of the proposed modulation scheme. Additionally, zoomed-in views highlight the diode bridge current waveforms. While Hybrid 1 and Hybrid 2 are theoretically distinguished by their respective combinations of c and d, the measured waveform shapes for i_{3u} appear similar across both cases. This is likely because the selected c and d values for the two modes are close in magnitude, $c = 0.40$ and $d = 0.35$

for Hybrid 1, and $c = 0.45$ and $d = 0.35$ for Hybrid 2, resulting in nearly identical current behavior in practice. Nonetheless, the experimental results confirm the validity of the modulation scheme.

Figs. 3.23(g) and 3.23(h) present the experimental waveforms corresponding to the DAB-RM and DAB-FM operating regions, respectively. As per the design condition $c \geq d$, the diode bridge remains completely inactive in both cases, and its current i_{3u} remains zero. This confirms that the diode bridge is effectively shut down and that the converter transitions into DAB mode.

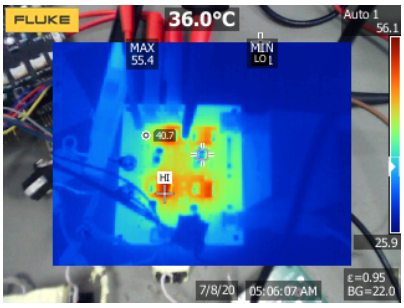
Furthermore, the active bridge current i_{2u} exhibits different slopes in the two modes. In Fig. 3.23(g), the slope indicates reverse power flow from the secondary to the primary. This reverse power flow was practically realized by reconfiguring the source and load connections such that the secondary side acted as the input and the primary side as the output. In contrast, Fig. 3.23(h) shows the opposite current slope, confirming forward power transfer from the primary to the secondary. It is also worth noting that a small current flows through the diode bridge, which can be attributed to circulating currents in the system.

The experimental waveforms across all operating regions, particularly the active bridge current i_{2u} and diode bridge current i_{3u}, confirm the effectiveness of the proposed active power sharing control, successfully enabling the power transfer from the diode bridge to the active bridge. While the open-loop implementation demonstrates consistent and reliable behavior, the adoption of closed-loop control can further enhance performance by compensating for hardware non-idealities.

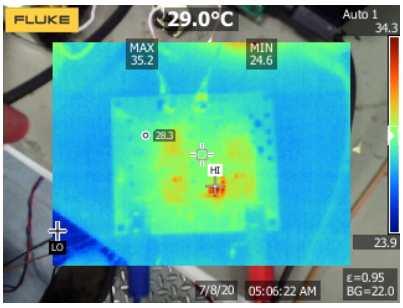
The proposed active power sharing control not only solves the power imbalance that arises in passive sharing due to the selected coupling inductance ratio, but also mitigates the overloading of the diode bridge by transferring part of its power to the active bridge. In passive sharing, the chosen ratio k fixes the power split as $P_3/P_2 = k$; with the adopted k, the diode bridge inherently processes a larger portion of the output power, which, over time, can lead to persistent thermal stress. In contrast, the active power sharing control deliberately reassigns a portion of this power from the diode bridge to the active bridge, thereby reducing the diode bridge's thermal loading.

This effect is evident in the thermal images obtained under active power sharing control. In Fig. 3.24 (DCM region), the active bridge reaches about 36.0°C [Fig. 3.24(a)], while the diode bridge runs cooler at about 29.0°C [Fig. 3.24(b)]. Similarly, in the CCM region (Fig. 3.25), the active bridge reaches 45.7°C [Fig. 3.25(a)], whereas the diode bridge remains at 35.1°C [Fig. 3.25(b)]. These results confirm that the proposed control reduces the thermal burden on the diode bridge relative to the passive power sharing case.

Moving to the hybrid operating regions, the behavior becomes more critical. In the Hybrid 1 case (Fig. 3.26), the active bridge temperature rises significantly to 55.5°C [Fig. 3.26(a)], while the diode bridge stays much cooler at 28.4°C [Fig. 3.26(b)]. The trend intensifies in the Hybrid 2 region (Fig. 3.27), where the active bridge reaches as high as 65.2°C [Fig. 3.27(a)], while the diode bridge remains at 29.1°C [Fig. 3.27(b)]. The elevated temperatures in the active bridge are consistent with the higher current stresses, as already evidenced in the experimental waveforms (see Fig. 3.23).

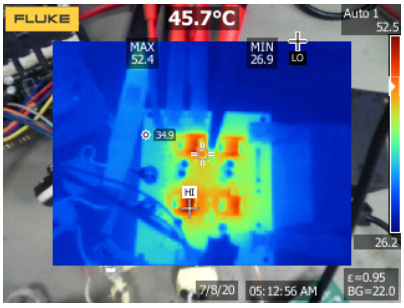


(a) active-bridge

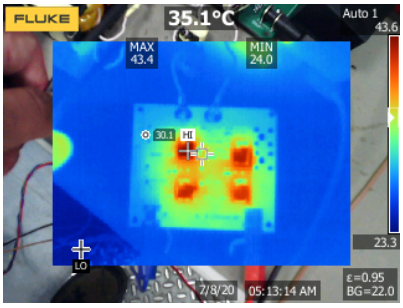


(b) diode-bridge

Figure 3.24: Secondary side thermal images of DCM region in active power sharing control.

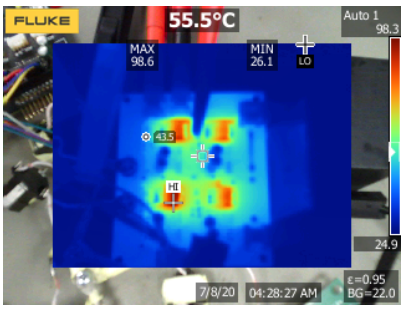


(a) active-bridge

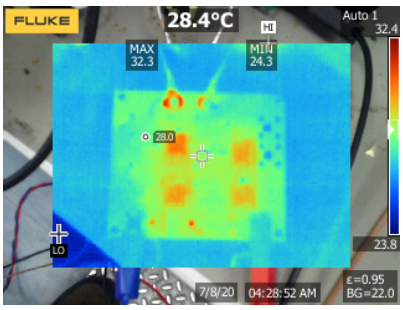


(b) diode-bridge

Figure 3.25: Secondary side thermal images of CCM region in active power sharing control.

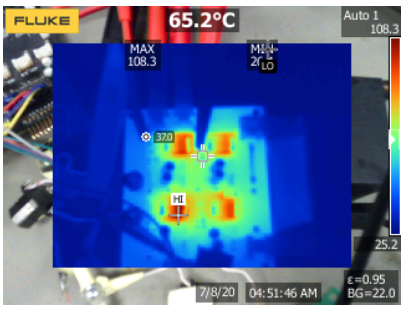


(a) active-bridge



(b) diode-bridge

Figure 3.26: Secondary side thermal images of Hybrid 1 region.



(a) active-bridge

(b) diode-bridge

Figure 3.27: Secondary side thermal images of Hybrid 2 region.

Overall, the thermal images clearly indicate that while active power sharing control alleviates the overloading effect on the diode bridge, the active bridge consistently operates at higher temperatures across all regions. This uneven distribution of thermal stress suggests that relying solely on the active power sharing control is not optimal, as it could lead to long-term reliability concerns. To mitigate this issue, the converter can be operated in an alternating ways, switching between the proposed active sharing technique and the conventional SAB modulation, i.e., passive power sharing. This approach provides a more balanced thermal profile between the bridges.

Observation

Active power sharing control reduces diode-bridge stress but shifts the thermal burden onto the active bridge.

3.6 Hybrid Modulation: Alternating Active Power Sharing and SAB Control

Taking advantage of the thermal inertia of the system, it is possible to mitigate long-term thermal stress by alternating conventional SAB operation (Fig. 3.2) with the proposed active power sharing control. In this way, the converter does not need to enforce power shifting within every switching period, but rather balances the stress over multiple cycles. This concept, hereafter referred to as hybrid power sharing modulation, is specifically discussed for the DCM region. To formalize the method, let G denote the ratio between the number of switching periods with power shift enabled and the number of switching periods operating under conventional SAB control. Using this definition, the average power processed by each bridge (defined in (3.22)) in the long term can be expressed as:

Note

Here, G denotes the ratio of active power-shift periods to conventional SAB periods. Note that this differs from the definition of G in the earlier chapter.

$$\begin{aligned} \overline{P}_2 &= GP_{2,\mathrm{DCM}} + (1-G)P_2 \\ \overline{P}_3 &= GP_{3,\mathrm{DCM}} + (1-G)P_3 \end{aligned} . \tag{3.44}$$

If $G = 1$, the delay time will happen in all the switching periods, while if $G = 0$, (3.44) reverts to (3.22) without any diode-bridge delay. In general, if $G = 1/N$, the proposed technique is enabled once every N switching periods. In this way, (3.25) and (3.28) can be updated to:

$$\begin{aligned} P_{2,\mathrm{DCM}} &= \frac{P_o}{G}\left[\frac{1}{1+k_p} - \frac{1-G}{1+k}\right] \\ P_{3,\mathrm{DCM}} &= \frac{P_o}{G}\left[\frac{k_p}{1+k_p} - \frac{(1-G)k}{1+k}\right] \end{aligned} , \tag{3.45}$$

restricting power-sharing ratio k_p within the diapason:

$$\frac{(1-G)k}{1+Gk} \le k_p \le k\,. \tag{3.46}$$

The possibility of employing the proposed technique in alternation with conventional SAB operation requires a redefinition of the modulation parameters c and d in order to achieve the desired power sharing. The procedure can be outlined as follows. Once the target output power P_o and the power sharing ratio k_p are specified, and the value of G is selected according to (3.46), the partial bridge powers $P_{2,\mathrm{DCM}}$ and $P_{3,\mathrm{DCM}}$ can be determined from (3.45).

From the diode-bridge power expression in (3.25), the difference $A = d - c$ can be directly calculated as:

$$\mathrm{A} = d - c = \sqrt{\frac{P_{3\mathrm{s}} L_{\mathrm{eq}} f_{\mathrm{sw}}}{V_{\mathrm{dc}}^2(1-m)}\frac{(1+k)}{k}}\,. \tag{3.47}$$

On the other hand, substituting (3.47) into the active-bridge power expression (3.28) yields the relationship:

$$\mathrm{B} = 2cd - c^2 = \frac{(kP_{2\mathrm{s}} - P_{3\mathrm{s}})L_{12} f_{\mathrm{sw}}}{kV_{\mathrm{dc}}^2(1+m)}\,. \tag{3.48}$$

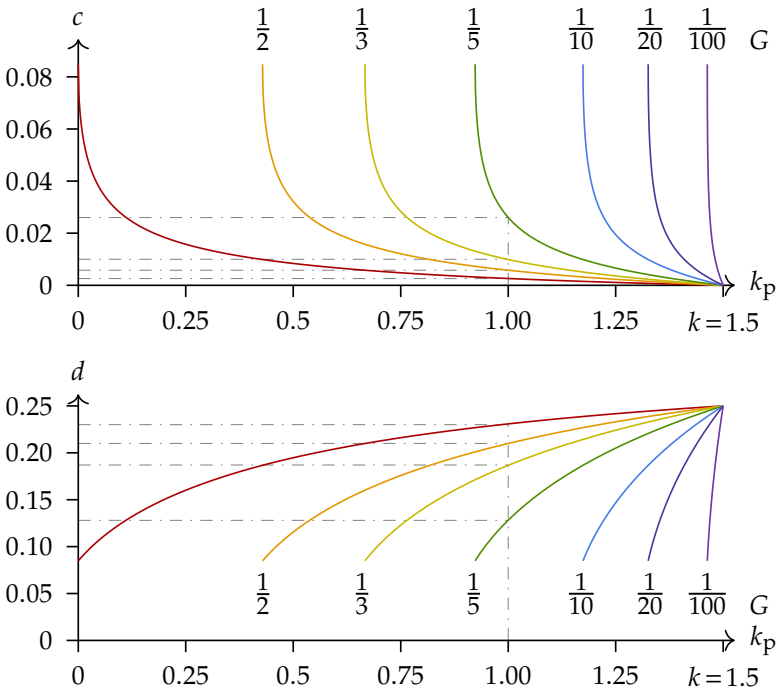


Figure 3.28: Values of c and d as a function of k_p under several values of G with references to the parameters listed in Table 3.7.

Finally, the parameters c and d can be explicitly obtained from (3.47) and (3.48) as

$$\begin{aligned} c &= -\mathrm{A} + \sqrt{\mathrm{A}^2 + B} \\ d &= \sqrt{\mathrm{A}^2 + B} \end{aligned} \quad . \tag{3.49}$$

Indeed, by examining Fig. 3.28, it can be observed that low values of G allow k_p to approach k while requiring comparatively larger c values. For example, referring to the parameters listed in Table 3.7, a power sharing ratio of $k_\mathrm{p} = 1$ can be obtained with $c = 0.0260$ when $G = 1/5$ (green trace in Fig. 3.28), compared to only $c = 0.0026$ when $G = 1$ (red trace in Fig. 3.28) [1].

1: Lower G makes it easier to reach the desired k_p, but requires larger c values.

Although the same methodology could, in principle, be extended to other operating regions, the approach becomes considerably more cumbersome and less tractable due to the lengthy and complex power expressions. Therefore, the hybrid modulation strategy is restricted to the DCM region, where the analytical formulation remains compact and practical.

3.6.1 Numerical Validation

The simulations has been carried out on PLECS (Plexim GmbH) with reference to the parameters listed in Table 3.7 to verify the proposed hybrid modulation technique.

As seen, the selected inductance values lead to the ratio $k = 1.5$. Therefore, under conventional SAB operations, the diode-bridge processes 60% of the rated power while active-bridge processes the remaining 40%. For $G = 1, 1/3$, and $1/5$, the power-sharing ratio k_p is reduced from the initial state $k_\mathrm{p} = k$ to $k_\mathrm{p} = (1 - G)k/(1 + Gk)$. Overall, 300 simulations validate the analytical developments discussed above.

Table 3.7: Numerical plant main parameters of the PSFB in forward mode.

Parameters	Symbol	Value	Unit
Input voltage	V_{dc}	400	V
Switching frequency	f_{sw}	20	kHz
Voltage gain	m	0.8	-
Turn ratio	n	1	-
Rated power at $d = 0.25$	P_o	2	kW
Leakage inductance	L_1	48.8	μH
Coupling inductance	L_{2u}, L_{2l}	1.5	μH
	L_{3u}, L_{3l}	1	μH
Coupling inductance Ratio	k	1.5	-
Equivalent inductance	L_{eq}	50	μH
Active-bridge inductance	L_{12}	51.8	μH

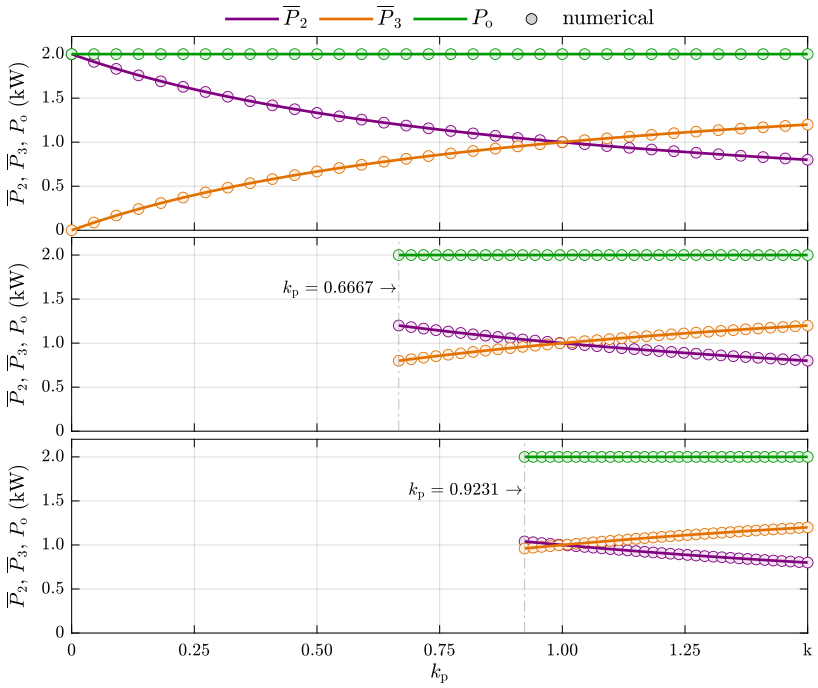


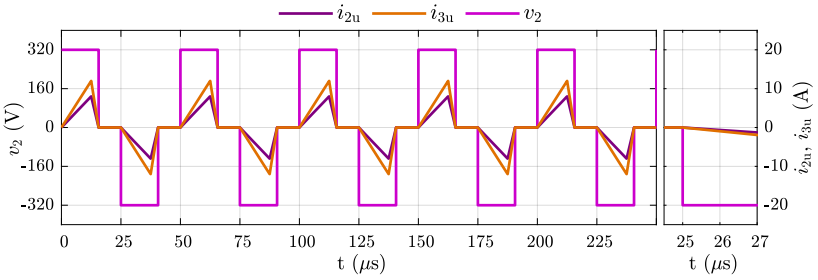
Figure 3.29: Active-bridge power $\overline{P}_2$, diode-bridge power $\overline{P}_3$, and total output power P_o with respect to the power ratio k_p, depicting both theoretical calculation and numerical results for $G = 1$, 1/3, and 1/5 (from top to bottom).

In Fig. 3.29, active-bridge power $\overline{P}_2$, diode-bridge power $\overline{P}_3$, and total output power P_o are depicted for different values of G. Initially, with $k_p = 1.5$, $c = 0$, and $d = 0.25$, the diode-bridge power surpasses the active-bridge power. As k_p decreases to 1, diode- and active-bridge powers match. Further reduction in k_p results in a gradual shift of power from the diode-bridge to the active-bridge, even though the total output power remains unchanged to the rated value 2 kW. The above considerations apply for each considered value of G, but it can be seen that the lower limit of k_p modifies according to (3.46) as G decreases. In particular, k_p is limited to 0, 0.6667, and 0.9231 for $G = 1$, 1/3, and 1/5, respectively. As is visible, numerical results (circles) fairly match the analytical predictions (solid traces). Moreover, the root mean square error (RMSE) between numerical evaluation and theoretical calculation of $\overline{P}_2$ and $\overline{P}_3$ is computed and listed in Table 3.8. The low RMSE values further confirm the capability of the proposed technique to shift power from diode- to active-bridge under heterogeneous working conditions.

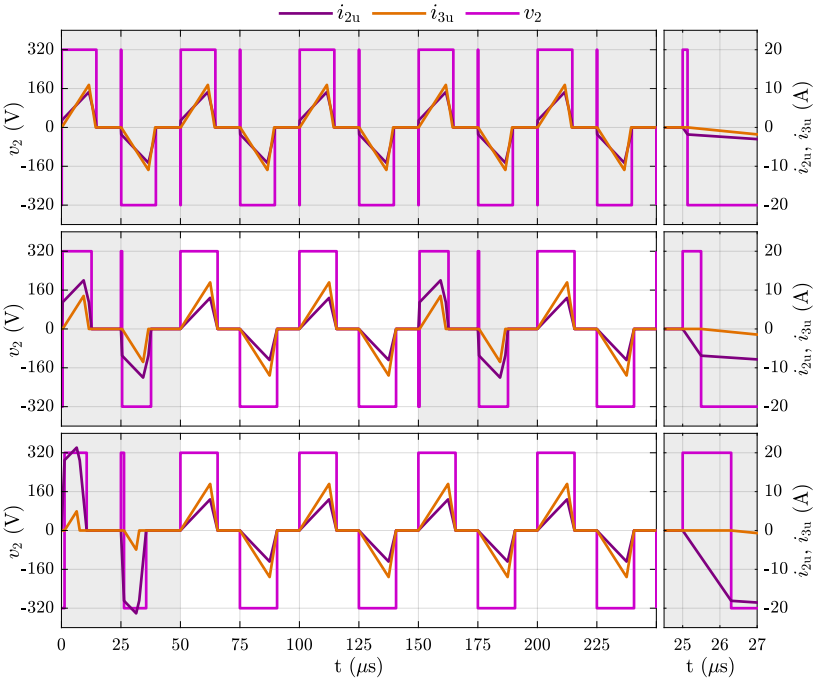
Fig. 3.30 shows the simulation waveforms of the output voltage v_2, active-bridge current i_{2u}, and diode-bridge current i_{3u}. Fig. 3.30(a) represents the

G	RMSE $\overline{P}_2$	RMSE $\overline{P}_3$	Unit
1	0.80	0.56	W
1/3	0.17	0.41	W
1/5	0.16	0.52	W

Table 3.8: Root Mean Squared Errors for $\overline{P}_2$ and $\overline{P}_3$ during power shift operation.



(a)



(b)

Figure 3.30: Waveforms of voltage and currents: (a) during conventional operation with $k_p = 1.5$; (b) during power shift operation with $k_p = 1$ considering $G = 1$, 1/3, and 1/5 (from top to bottom).

baseline scenario with $k_p = 1.5$ where no extra pulse (i.e., $c = 0$) is present. In this configuration, the converter operates as a conventional SAB converter with dual-output. Fig. 3.30(b) displays simulation waveforms for $k_p = 1$ in case of $G = 1$, 1/3 and 1/5, respectively. Periods with a gray background indicate that the proposed technique is enabled. Indeed, when $G = 1$, the additional pulse happens in every switching period. On the other hand, $G = 1/3$ and $G = 1/5$ showcase diode-bridge turn-on delay once every 3 and 5 switching periods, respectively.

Looking at the zoom frames on the right side of Fig. 3.30, it is apparent how decreasing the value of G leads to an increase of the diode-bridge turn-on delay cT_{sw}. Clearly, larger delay times cause higher active-bridge currents i_{2u} (limited at the involved switching period) if compared with the base scenario. These experimental results confirmed that the proposed hybrid modulation can effectively redistribute power, ensuring a more balanced thermal profile between the active and diode bridges.

3.7 Summary

This chapter investigated the AB-DC/DC converter by combining analytical derivations, statistical analysis, and validation through simulations and experiments. First, the SAB converter was studied to derive closed-form expressions of power transfer in both DCM and CCM, providing the foundation for the AB-DC/DC analysis. The passive power sharing mechanism was then examined, showing that coupling inductor tolerances strongly affect the expected power distribution between the diode and active bridges. Statistical and numerical analyses confirmed that even small magnetic variations compromise the inherent balance, resulting in unequal power allocation and additional thermal stress. To overcome this limitation, an active power-sharing modulation strategy was proposed, introducing controlled turn-on delays to shift power from the diode bridge to the active bridge. The converter was shown to operate in six distinct regions (DCM, CCM, Hybrid 1, Hybrid 2, DAB-FM, DAB-RM), each with analytically derived boundaries and closed-form power equations. The proposed approach was validated through extensive PLECS simulations and hardware experiments on a 200 V, 100 kHz prototype, confirming agreement between theoretical, numerical, and experimental results. Finally, a hybrid modulation scheme alternating between active power sharing and conventional SAB control was introduced to mitigate long-term thermal stress by balancing bridge utilization. Overall, this chapter demonstrated that while passive power sharing is insufficient under realistic component tolerances, active and hybrid modulation strategies provide reliable power distribution and improved converter robustness. The research outcomes from this chapter have led to the publications [87]–[90].

[87]: Pittala *et al.* (2024), 'Impact of Magnetics Tolerance on the Power Sharing of Parallel Dual-Output Phase-Shift Full-Bridge Converters'
[88]: Pittala *et al.* (2024), 'Software-Based Power Sharing Control in Parallel Dual-Output Phase-Shift Full-Bridge Converters'
[89]: Pittala *et al.* (2025), 'Active Power Sharing Control in Asymmetrical Bidirectional DC/DC for Smart Transformers'
[90]: Pittala *et al.* (2025), 'Active Power Sharing Control in Asymmetrical Bidirectional DC/DC Converter'

Series Resonant DC Transformer 4

Abstract

This chapter explores sigma–delta ($\Sigma\Delta$) based cycle-skipping modulation as a means to achieve power regulation and current sharing in series resonant converters operating as DC transformers (SRC-DCX). Unlike conventional burst-mode or frequency-modulation strategies, the $\Sigma\Delta$ approach distributes active and idle switching cycles in an optimized manner, reducing output voltage and current ripples while maintaining soft-switching. An analytical framework is developed to directly relate the pulse-density parameter to the average power transfer capability of the SRC-DCX.

Experimental validation is carried out on 1 kW prototypes. First, a single converter is tested to confirm the linear power regulation predicted by theory, with peak efficiency of 98.4% and efficiency above 96% even at light loads. Second, two converters are operated in an input-parallel output-parallel (IPOP) configuration to evaluate current balancing. Open-loop operation reveals significant imbalance due to parameter mismatches, whereas closed-loop $\Sigma\Delta$ pulse-skipping control ensures robust current sharing and balanced load distribution without requiring frequency or phase adjustments.

The results demonstrate that $\Sigma\Delta$-based cycle-skipping not only enables fine-grained power control of inherently unregulated DCX converters but also provides a simple and effective method for current sharing in modular systems, thereby enhancing their suitability for high-efficiency and scalable DC microgrid applications.

4.1 Introduction to Series Resonant Converters . . . 71
4.2 Series Resonant Converter Operating as a DC Transformer 73
4.3 Cycle-Skipping Modulation 75
4.3.1 ZVS Analysis in the Series Resonant Converter 76
4.3.2 Voltage Ripple Analysis in the Conventional CSM 78
4.4 Sigma-Delta Based Cycle-Skipping Modulation . . 78
4.4.1 Example: Conventional CSM and Sigma-Delta-based CSM 79
4.4.2 Implementation of Sigma-Delta-based CSM in STM32 microcontrollers 81
4.5 Hardware Design of a Series Resonant Converter 83
4.5.1 Power Regulation of an SRC-DCX 84
4.5.2 Experimental Validations 85
4.6 Current Sharing Control in Input Parallel and Output Parallel SRC-DCX 87
4.6.1 Experimental Validation 88
4.6.2 Parallel Operation of an SRC-DCX 88
4.6.3 Open-Loop Control Validation 89
4.6.4 Closed-Loop Control Validation 91
4.7 Summary 95

4.1 Introduction to Series Resonant Converters

In the previous chapters, the DAB converters and their derivatives were investigated to extend the ZVS region at light loads and address asymmetrical bidirectional power transfer by combining DAB and SAB converters. In practice, such topologies are highly suitable for applications like DC smart homes, where converters often operate under partial load conditions. Similarly, the AB-DC/DC converter finds relevance in electric vehicle charging or energy storage systems, where the asymmetrical nature of power flow must be effectively managed.

However, in DC microgrids, particularly for PV integration, full bidirectionality is not always required. In these cases, simpler unidirectional solutions such as SAB or resonant converters become attractive. While the SAB inherits the advanced controllability and ZVS capability of the DAB, its trapezoidal current waveform introduces significant harmonic components, leading to high electromagnetic interference (EMI). Resonant converters, by contrast, feature inherently sinusoidal currents with load-independent ZVS and ZCS, resulting in lower harmonic distortion and reduced EMI [95]. These benefits provide strong motivation to investigate resonant topologies, and in particular, this thesis focuses on

the analysis of the SRC as an alternative high-efficiency solution for DC microgrid applications. The SRC operating as a DCX has emerged as a particular promising candidate for the DC microgrid applications. As highlighted in [95], the SRC-DCX offers distinct advantages over conventional DAB-based solutions, making it a more suitable choice for high-efficiency and high-power-density SST designs.

The SRC-DCX is an inherently load-independent, uncontrolled power converter that operates with a fixed 50% duty cycle to match input and output voltages while providing galvanic isolation with high efficiency [52]. However, when output power regulation is required, conventional control methods such as frequency modulation or duty cycle/phase shift modulation may not be feasible or may introduce load dependency. This can result in unstable operation due to varying dc voltage gain under dynamic conditions and may compromise soft-switching and transient operation stability, leading to efficiency degradation [96]. Additional control techniques, such as conventional cycle-skipping, can also be implemented. However, this approach often results in increased current and voltage ripple at the input or output, adversely affecting performance and efficiency [97].

To overcome these limitations, the conventional cycle-skipping technique has been optimized by using the ΣΔ modulation. ΣΔ modulation was originally developed for telecommunications and digital signal processing [98]. However, recently it has demonstrated promising applications in power electronics due to its advantageous spectral characteristics [99], [100]. In prior research, ΣΔ modulation has been explored for natural power balancing in bipolar dc microgrids [101]. In [102], the authors implemented the ΣΔ technique to enable the variable switching frequency, which helps to reduce the switching losses in three-phase, four-wire active power filters. In this work, it is utilized as a cycle-skipping mechanism, where the average number of skipped cycles varies linearly with the modulator's input signal, generating an optimal cycle-skipping pattern. Such patterns maximize the equivalent frequency of pulses transferring energy to the output. This approach not only enhances efficiency but also enables effective power flow control in DCX-based modular SST systems.

Moreover, DCX-based modular architectures, such as input-parallel output-parallel (IPOP) or input-series output-series (ISOS), are limited by their unregulated nature. Even minor parameter mismatches between resonant tanks can cause significant current imbalance, with most of the current flowing through the path of least impedance. As noted in [52], [103], achieving effective power balancing in such configurations remains an open research challenge. However, the proposed ΣΔ modulation not only enables continuous power regulation across the full load range, but also facilitates balanced current sharing among modular DCX units.

The following sections are organized as follows. Section 4.2 introduces the operating principle of the series resonant converter as a DC transformer. Section 4.3 presents the cycle-skipping technique, which enables power regulation of the SRC-DCX without requiring additional converters. Section 4.4 details the ΣΔ modulation method, which optimizes conventional cycle-skipping and describes its implementation on an STM32 microcontroller. Section 4.5.2 reports the experimental validation of the proposed power regulation strategy. Section 4.6 extends the tech-

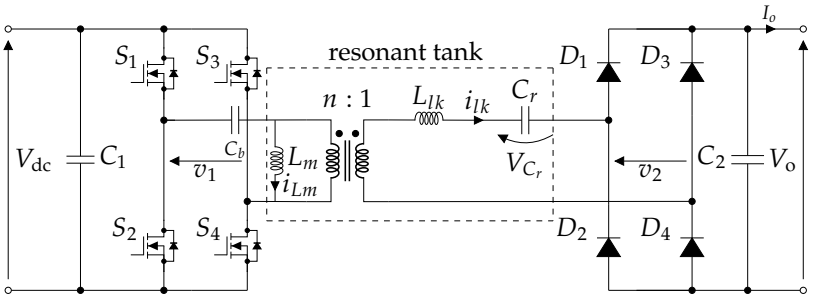


Figure 4.1: Series resonant converter operating as a DC transformer.

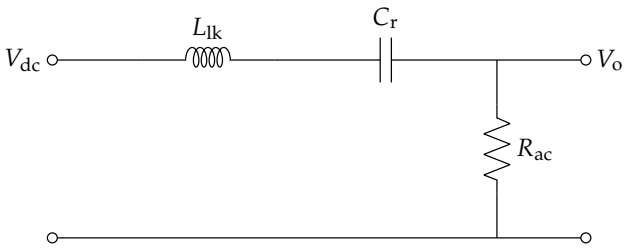


Figure 4.2: AC equivalent circuit of a series resonant converter.

nique to achieve current sharing in input-parallel and output-parallel modular configurations, while Section 4.6.1 provides the corresponding experimental verification.

4.2 Series Resonant Converter Operating as a DC Transformer

The SRC with an active bridge on the primary side and a diode bridge on the secondary side, as illustrated in Fig. 4.1, has been designed to maintain a constant conversion gain within the operating region. This mode of operation, characterized by a constant voltage gain, allows the SRC to function effectively as a DCX [104]. In the SRC with a capacitive output filter, the resonant tank drives the rectifier as a current source. The rectifier and its filter present a load to the AC tank that is not the DC load resistance R_L, but an equivalent AC resistance R_{ac} [1] obtained by retaining the fundamental component of the square-wave quantities at the rectifier interface. Following the AC–fundamental analysis in [105], the equivalent AC resistance seen by the tank in the series case is defined as:

1: Equivalent AC resistance seen by resonant tank from fundamental harmonic approximation.

$$R_{ac} = \frac{8}{n^2\pi^2} R_L \,, \tag{4.1}$$

which will be used in the subsequent tank calculations. Here, n is denoted as the transformer turns ratio. By employing the equivalent load resistance R_{ac} together with the AC fundamental analysis method outlined in [105], the characteristics of the SRC can be derived. The corresponding equivalent AC circuit is shown in Fig. 4.2. In this representation, the voltages denoted with uppercase symbols V correspond to the fundamental AC components of the applied square-wave excitation, which will be converted back to square-wave quantities at the end of the derivation. The impedance of each component is expressed as

$$Z_C = \frac{1}{j\omega C_r}, \qquad Z_L = j\omega L_{lk}, \qquad Z_R = R_{ac} \,. \tag{4.2}$$

The total impedance of the series tank is then calculated to be:

$$Z_{\text{tot}} = R_{\text{ac}} + j\omega L_{lk} + \frac{1}{j\omega C_r} \,. \tag{4.3}$$

By applying the voltage divider relationship, the AC gain across R_{ac} is given by:

$$G = \left|\frac{V_o}{V_{\text{dc}}}\right| = n \left| \frac{R_{\text{ac}}}{R_{\text{ac}} + j\left(\omega L_{lk} - \frac{1}{\omega C_r}\right)} \right| \,. \tag{4.4}$$

Normalizing with respect to the resonant frequency

$$\omega_0 = \frac{1}{\sqrt{L_{lk} C_r}} \,, \qquad N = \frac{\omega}{\omega_0} \,, \tag{4.5}$$

and defining the quality factor as:

$$Q = \frac{\omega_0 L_{lk}}{R_{\text{ac}}}, \tag{4.6}$$

the magnitude of the AC gain becomes:

$$G = \left|\frac{V_o}{V_{\text{dc}}}\right| = n \left| \frac{1}{\sqrt{1 + \left(\frac{Q}{N}\right)^2 (N^2 - 1)^2}} \right| \,. \tag{4.7}$$

Note

Here, G denotes the voltage gain ratio, consistent with the definition used in Chapter 2. Note, however, that this differs from the definition of G given in Chapter 3.

This expression represents the fundamental AC voltage transfer function of the SRC, valid for operation at and above resonance, and serves as the basis for analyzing its voltage gain and soft-switching characteristics. Fig. 4.3 illustrates the normalized gain as a function of the normalized frequency for different values of the quality factor Q. When the normalized frequency is unity ($N = 1$) [2], i.e., the switching frequency coincides with the resonant frequency, the voltage gain G equals the transformer turns ratio n, as given in (4.7). This operating point is indicated in the figure as DCX, where the turns ratio is selected as $n = 1$. At this condition, the SRC behaves as a DC transformer, achieving load-independent operation since the gain is unaffected by either the load resistance or the quality factor. This load independence implies that direct power regulation is not possible within the DCX operating point; however, it is possible to design the converter for its rated power, which can be calculated as follows: In general, the DC load resistance R_{L} can be expressed as:

2: At $N = 1$, SRC behaves as an ideal DC transformer (DCX).

$$R_{\text{L}} = \frac{V_o^2}{P_m} \,. \tag{4.8}$$

By substituting this into the definition of the equivalent AC resistance given in (4.1), the maximum power processed by the SRC-DCX can be obtained as:

$$P_m = \frac{8}{n^2 \pi^2} \frac{V_o^2}{R_{\text{ac}}} \,. \tag{4.9}$$

This substitution links the DC load resistance to the equivalent AC load, allowing direct calculation of the maximum transferable power. Using

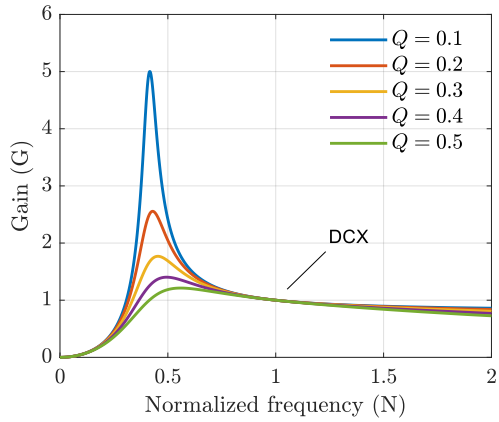


Figure 4.3: Gain characteristics of the series resonant converter.

the above equation, the converter can be designed for its maximum rated power and operated as a DCX according to the established design guidelines. In practice, a small phase difference between the transformer primary voltage v_1 and secondary voltage v_2 must be applied in order to enable power transfer. Even a slight variation in this phase shift can cause a significant change in the transferred power. Moreover, since the switching frequency is fixed at the resonant frequency, introducing a small frequency deviation allows for some degree of power control. Nevertheless, these two approaches are not suitable as practical regulation strategies, because they either lead to poor controllability or compromise the soft-switching condition. Moreover, modulation techniques based on frequency variation, phase shift, or duty-cycle control can drive the converter away from the DCX operating point, as shown in Fig. 4.3, thereby introducing load dependency and potentially compromising the soft-switching conditions. Therefore, many researchers employ an additional DC/DC converter cascaded with the DCX stage to achieve full-range power regulation [96], [106]–[110]. Nevertheless, introducing such an external stage adds extra losses to the system and increases the control complexity, which ultimately leads to a reduction in overall efficiency. To overcome this limitation, cycle-skipping (or pulse removal) techniques have been introduced, enabling power regulation without the need to alter the switching frequency or duty cycle of the converter [97].

4.3 Cycle-Skipping Modulation

The cycle-skipping modulation (CSM) technique, also referred to as pulse removal, pulse skipping, pulse-density modulation, or burst mode control, regulates the power transfer of the SRC-DCX by selectively suppressing switching cycles. In this method, the switches S_1, S_2, S_3, and S_4 of the full-bridge inverter in Fig. 4.1 are either driven sequentially at a constant switching frequency, producing active cycles N_{active}, with a fixed 50% duty cycle, or disabled for a number of switching periods, producing idle cycles N_{idle}. As a result, only a subset of cycles transfers energy, thereby reducing the average power delivered over time.

This principle is illustrated in Fig. 4.4, where the switches are disabled for certain intervals (shaded region) and re-enabled for others. The grouping of active and idle cycles into contiguous blocks is often referred to as burst mode. In the example shown, the interval from t_0 to t_3 spans

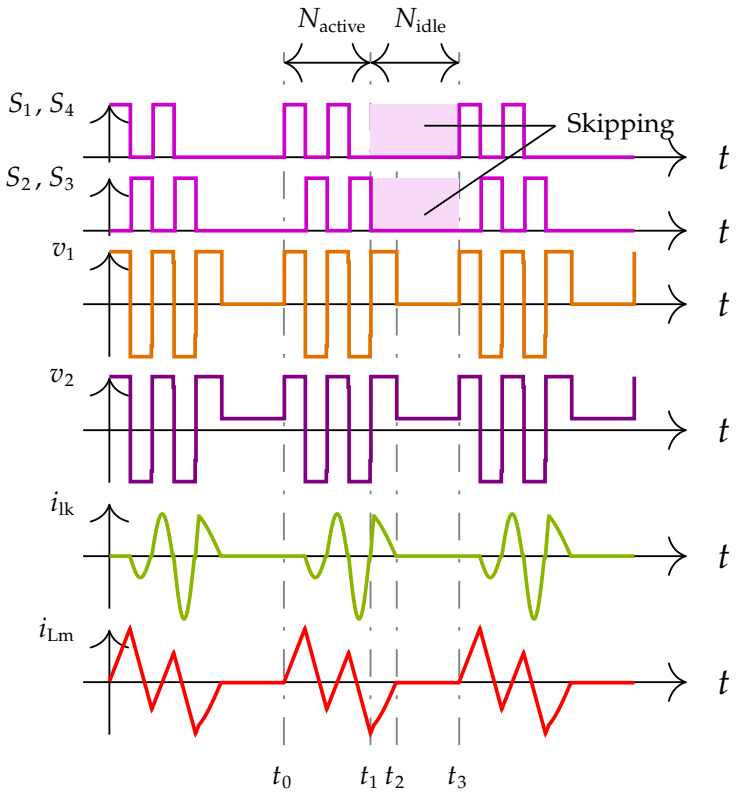


Figure 4.4: Ideal waveforms of SRC-DCX converter operating under conventional cycle skipping.

four switching periods T_{sw}, during which two cycles are skipped and two remain active. This interval can be regarded as burst period T_{burst}. The resulting pulse density or burst duty D is therefore defined as the ratio of active cycles (N_{active}), from t_0 to t_1, to the total number of cycles ($N_{\text{active}} + N_{\text{idle}} = T_{\text{burst}}$), i.e. $D = 2/4$ in this case. More generally, CSM can be realized by fractional pulse densities such as 1/2, 1/3, 6/11, 8/15, and so forth.

4.3.1 ZVS Analysis in the Series Resonant Converter

While CSM effectively reduces the average transferred power, its impact on soft-switching must also be examined. In particular, the turn-on of the primary switches after an idle interval N_{idle} can deviate significantly from the conventional ZVS condition [111]. In Fig. 4.4, the waveforms reveal that at t_0, when the converter resumes normal operation, the magnetizing current i_{Lm} is already reduced to zero. According to the ZVS condition, the energy stored in L_m must be sufficient to discharge the device output capacitances C_{s1} and C_{s2}, i.e.,

$$\frac{1}{2} L_m \left(\frac{\Delta i_m}{2} \right)^2 > C_s V_{\text{dc}}^2 , \tag{4.10}$$

where Δi_m denotes the peak-to-peak swing of the magnetizing current in one switching half-period, such that $\Delta i_m/2$ corresponds to the current available at a device turn-off and V_{dc} is the dc-link voltage [112]. Since $i_{Lm}(t_0) = 0$, this condition cannot be fulfilled, meaning that all the energy in the tank has been depleted during the skip interval. As a result, there

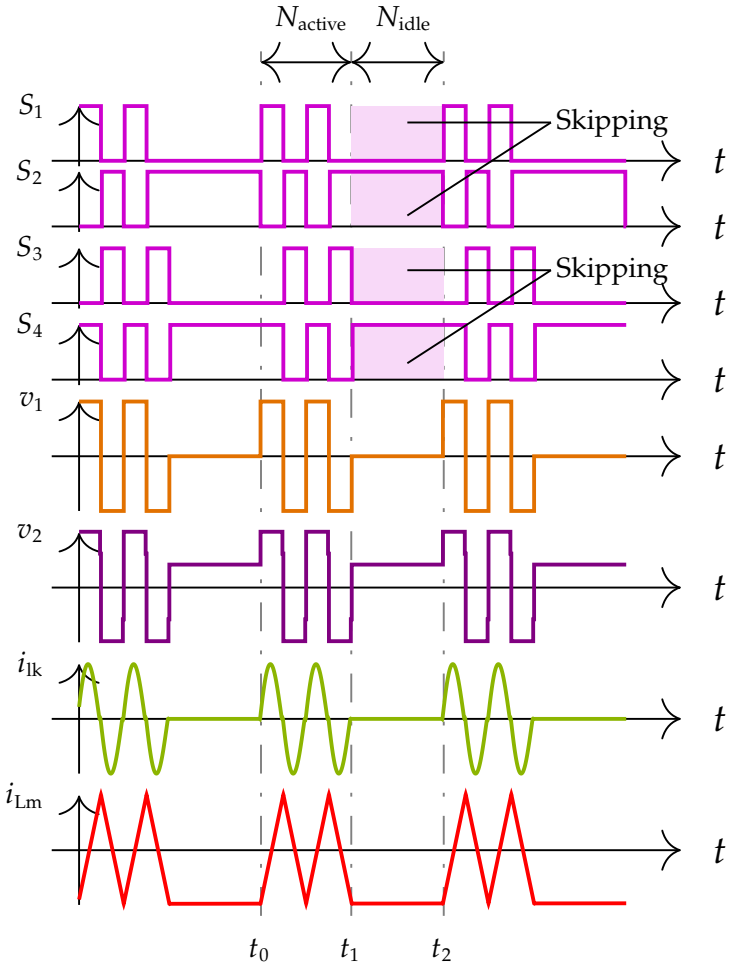


Figure 4.5: Ideal waveforms of SRC-DCX converter operating under modified cycle skipping technique.

is no current available to facilitate ZVS, and the subsequent turn-on occurs under hard-switching conditions. This behaviour has been noted in [111], [113], where the loss of ZVS is attributed to resonant tank energy depletion. To alleviate this, those works proposed a switching sequence in which the device turned on first is turned off last within the active cycles interval N_{active}, thereby reducing the commutation loss. However, this method can only achieve partial ZVS.

A different interpretation was given in [114], where it is stated that upon resuming operation, S_1 and S_4 turn on with ZCS. In practice, such a condition is not achievable: even if the current happens to be zero, the parasitic output capacitances remain charged, and without a magnetizing current to provide a discharge path, hard-switching losses inevitably occur.

Nevertheless, this issue can instead be mitigated by ensuring that a nonzero magnetizing current i_{Lm} is maintained even during the skipping interval. This can be accomplished by turning on either the top switches S_1, S_3 or the bottom switches S_2, S_4 during the skipping. In this way, a small dc bias is applied across the magnetizing inductor, sustaining a current flow with minimal conduction losses.

As illustrated in Fig. 4.5, the bottom switches S_2 and S_4 are turned on during the skipping region, highlighted in magenta shade. Consequently, when the converter resumes normal operation at t_0, the magnetizing current

i_{Lm} is nonzero and provides the required energy to discharge the device output capacitances charged to the dc-link voltage V_{dc}. In this way, the ZVS condition in (4.10) can still be satisfied after an idle interval, avoiding the hard-switching problem observed in the conventional CSM approach.

Furthermore, in the conventional CSM shown in Fig. 4.4, the magnetizing current decays exponentially during the normal operation. This decay leads to the loss of stored energy in L_m, which typically behaves as a transient dynamic response, and it is interrupted during the skipping intervals, leading to inrush or surge currents in the resonant tank. In contrast, the modified CSM shown in Fig. 4.5 maintains a continuous magnetizing current even during skipping, resulting in a steady waveform and eliminating inrush transients in the transformer.

4.3.2 Voltage Ripple Analysis in the Conventional CSM

Furthermore, the conventional method with fixed burst intervals can cause the higher ripple on the output voltage V_o [111]. During an active period, the resonant tank delivers energy to charge the output capacitor C_2, while during an idle block the capacitor must supply the load current I_{o} alone. A simplified estimate of the voltage ripple during the idle period can be defined as:

$$\Delta V \approx \frac{I_{\mathrm{o}}}{C_2} N_{\mathrm{idle}} T_{\mathrm{sw}} , \tag{4.11}$$

showing that longer fixed burst intervals cause larger voltage deviations, which appear as low-frequency ripple in the output waveforms. For example, with $D = 30/70$, a burst-mode implementation would deliver energy for 30 consecutive cycles and then remain idle for 40 cycles [3]. Such clustered transfer of energy forces the input and output capacitors to alternately charge and discharge over relatively long intervals, producing low-frequency oscillations that manifest as large voltage ripple.

3: Fixed burst intervals cause large low-frequency ripple.

As pointed out in [114], even with a two-pulse pattern the resulting voltage and current ripple can still be significant and often unacceptable for practical applications. To alleviate this, [113] introduced multi-pulse patterns (1-pulse, 2-pulse, and 3-pulse) within a fixed burst window. In the 3-pulse case, the energy packets are interleaved across the burst period, reducing the length of consecutive idle runs. While this approach remains deterministic, its effect is conceptually similar to that of ΣΔ cycle-skipping, where idle intervals are randomized and distributed in time to suppress low-frequency ripple.

Building on this idea, the present work introduces a sigma–delta based cycle-skipping modulation that not only suppresses the low-frequency ripple but also provides a direct mechanism for regulating the power transfer of the SRC-DCX. The dual benefit of ripple suppression and power regulation is demonstrated in the following sections.

4.4 Sigma-Delta Based Cycle-Skipping Modulation

The ΣΔ modulator transforms an analog or digital reference signal into a one-bit output sequence with noise-shaping properties. A first-order

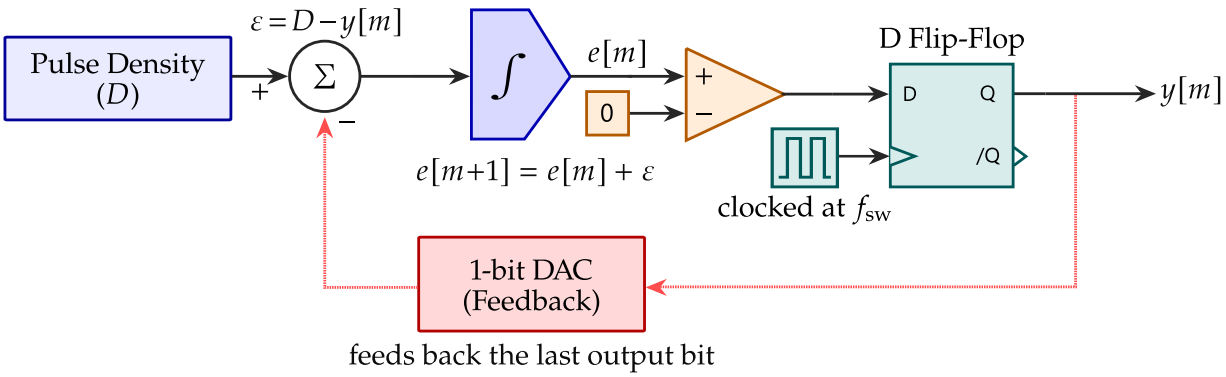


Figure 4.6: Basic idea of sigma-delta modulator.

implementation, shown in Fig. 4.6, consists of a summer, an integrator, a comparator, and a D flip-flop. The input reference is continuously compared with the accumulated quantization error, and the result determines whether the output bit for the next cycle is active or idle. In this way, the instantaneous error is fed back into the loop, preventing long runs of consecutive idle cycles.

The output sequence is therefore not strictly periodic but pseudo-random, with an average density corresponding to the input reference. The quantization noise is accumulated in the integrator and shaped by the loop, pushing most of its spectral content to higher frequencies. As a result, the one-bit stream exhibits the desired average duty while avoiding clustered gaps and spreading the error energy over a wider bandwidth.

When applied to cycle-skipping modulation, this property ensures that active and idle cycles are interleaved rather than grouped into bursts, thus reducing the total burst period T_{burst}. Consequently, the equation (4.11) shows that the capacitor voltage droop per burst segment is significantly reduced, suppressing the low-frequency envelope oscillations and shifting the residual ripple to higher frequencies where it is easier to filter.

4.4.1 Example: Conventional CSM and Sigma-Delta-based CSM

To illustrate the difference between conventional cycle-skipping and ΣΔ-based cycle-skipping, consider a pulse density of $D = 3/10$. In conventional CSM, the average duty is enforced by grouping three active cycles followed by seven idle cycles:

$$\underbrace{111}_{\text{active}}\,\underbrace{0000000}_{\text{idle}} \quad \Rightarrow \quad 1110000000 \mid 1110000000 \ \ldots$$

In this case, the N_{idle} is fixed to seven cycles, which produces a significantly low-frequency ripple according to (4.11).

Whereas in ΣΔ-based cycle-skipping: Let $m \in \mathbb{Z}_{\geq 0}$ be the switching-cycle index and $D \in [0, 1]$ be the desired pulse density (input signal reference to the ΣΔ modulator). Later defining few more parameters:

- $y[m] \in \{0, 1\}$ — the one-bit output at cycle m (1 = active cycle, 0 = skipped).

Note

Here, m denotes the switching-cycle index. Note that this differs from the definition of m in the earlier chapter.

4: $e[m]$ accumulates the density error

- $e[m] \in \mathbb{R}$ — the integrator state just before the decision at cycle m [4].

A minimal first-order loop is:

$$y[m] = \begin{cases} 1, & e[m] \geq 0, \\ 0, & e[m] < 0, \end{cases} \tag{4.12}$$

$$e[m+1] = e[m] + \varepsilon, \qquad e[0] = 0. \tag{4.13}$$

Equation (4.13) integrates the instantaneous density error $\varepsilon = D - y[m]$, and (4.12) quantizes the sign of the integrator state. This feedback prevents long runs of zeros/ones and yields an interleaved bitstream whose long-term average equals D. For $D = 0.3$, the resulting one-bit sequence is:

$$1000100100 \mid 1000100100 \mid \ \ldots$$

which repeats with a period of ten cycles. In this case, the maximum N_{idle} is reduced to three by considering the consecutive ones and zeros, which is much smaller than the conventional CSM case, thereby reducing the output capacitor voltage ripple and shifting ripple energy to higher frequencies. In this way, the capacitor size can be reduced while maintaining an acceptable voltage ripple, since the shortened burst length directly limits the maximum voltage that appears on C_2, as per (4.11).

It can be seen from Table 4.1 that the ΣΔ feedback loop inserts active cycles in such a way that the long-term density matches the desired $D = 0.3$, while avoiding long idle runs. As a result, the low-frequency oscillations associated with conventional CSM are strongly suppressed. However, it is difficult to find a microcontroller that directly provides the peripherals required to realize the theoretical ΣΔ loop, such as a summer, an integrator, a comparator, and a D flip-flop. In practice, these functions must be emulated in software or mapped onto existing hardware modules. As discussed in [115], the STM32 family of microcontrollers provides a high-resolution timer (HRTIM) with a burst mode controller (BMC), which can be configured to mimic the ΣΔ bitstream by appropriately updating the controller burst registers. The following section, therefore, describes how the ΣΔ-based cycle-skipping modulation can be implemented in an STM32 microcontroller using its built-in burst mode functionality.

Table 4.1: First ten cycles of a first-order ΣΔ modulator for $D = 3/10$.

Cycle (m)	$e[m]$ (before decision)	Output ($y[m]$)	Density error (ε)
1	+0.0	1	−0.7
2	−0.7	0	+0.3
3	−0.4	0	+0.3
4	−0.1	0	+0.3
5	+0.2	1	−0.7
6	−0.5	0	+0.3
7	−0.2	0	+0.3
8	+0.1	1	−0.7
9	−0.6	0	+0.3
10	−0.3	0	+0.3

4.4.2 Implementation of Sigma-Delta-based CSM in STM32 microcontrollers

In general, when the pulse density is expressed as a rational fraction $D = N_{\text{active}}/255$, the resulting bitstream has a period of at most 255 cycles. This 255-bit expansion corresponds to an 8-bit resolution of the pulse density, which is well suited for microcontroller implementation: this pattern is long enough to suppress low-frequency ripple, yet compact enough to be stored in the BMC registers as a sort of look-up tables.

In the STM32 implementation, the $\Sigma\Delta$ bitstream for a given $D = N_{\text{active}}/255$ is parsed into short bursts of consecutive active and idle cycles. A pair of register values describes each burst: HRTIM-BMPER (P_B), which sets the total burst length (active + idle), and HRTIM-BMCMP (I_B), which sets the number of idle periods within that burst. The timer hardware then outputs $P_B - I_B$ active cycles, followed by I_B idle cycles. At the end of each burst interval, the firmware loads the next pair of values. In this way, the $\Sigma\Delta$ bitstream is reproduced without per-cycle register updates, but only at burst boundaries.

To illustrate the procedure, consider the same density $D = 3/10$ discussed earlier. The corresponding $\Sigma\Delta$ sequence is:

$$1000100100 \mid 1000100100 \mid \ldots$$

which contains three active cycles in every ten. Parsing the sequence into maximal runs of consecutive ones and zeros gives the corresponding burst events:

$$(1\,000)\ (1\,00)\ (1\,00).$$

Hence one ten-cycle period is represented by three burst events with register values:

$$(P_B, I_B) = \{(4,3),\ (3,2),\ (3,2)\}.$$

The register programming can be organized into two tables: one for the burst period (BMPER) and one for the number of idle cycles (BMCMP).

Density D	Burst event j	1	2	3
3/10	P_B (cycles)	4	3	3
	I_B (idle cycles)	3	2	2

Table 4.2: Burst register values for $D = 3/10$.

Concatenating these three bursts reproduces the $\Sigma\Delta$ sequence exactly, while requiring only three register updates per 10 cycles rather than one update per cycle.

The same procedure extends naturally to the general case $D = N_{\text{active}}/255$,

N_{active}	ΣP_B	P_{B0}	P_{B1}	P_{B2}	P_{B3}	P_{B4}	P_{B5}	...	P_{B127}
0	1	255	–	–	–	–	–	...	–
1	1	127	–	–	–	–	–	...	–
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋱	⋮
5	5	42	42	41	42	41	–	...	–
6	6	36	35	36	35	36	35	...	–
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋱	⋮
255	1	255	–	–	–	–	–	...	–

Table 4.3: HRTIM-BMPER register – number and duration of the burst mode intervals used to emulate the $\Sigma\Delta$ modulator.

Table 4.4: HRTIM-BMCMP register – number of idle periods in the burst mode intervals used to emulate the ΣΔ modulator.

N_{active}	ΣI_B	I_{B0}	I_{B1}	I_{B2}	I_{B3}	I_{B4}	I_{B5}	...	I_{B127}
0	1	254	–	–	–	–	–	...	–
1	1	126	–	–	–	–	–	...	–
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋱	⋮
5	5	41	41	40	41	40	–	...	–
6	6	35	34	35	34	35	34	...	–
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋱	⋮
255	1	1	–	–	–	–	–	...	–

which is compatible with an 8-bit microcontroller. Parsing a 255-cycle period into maximal runs of ones and zeros yields the corresponding $\{P_B, I_B\}$ pairs, which can be precomputed and stored in lookup tables, as shown in Tables 4.3 and 4.4. Since 255 corresponds to an 8-bit resolution of the density, this method provides fine granularity while remaining computationally efficient for real-time STM32 firmware. The resulting resolution step is:

$$\Delta D = \frac{1}{255} \approx 0.00392 \text{ (i.e., } 0.392\%),$$

which defines the smallest achievable increment in the pulse density.

It can be observed from Tables 4.3 and 4.4 that the total burst length does not always span the full 255 cycles. For certain densities, the ΣΔ sequence becomes periodic with a much shorter repeating pattern. In such cases, the bitstream can be represented by fewer burst events and smaller P_B values, while still preserving the long-term density $D = N_{\text{active}}/255$.

At the extreme densities $N_{\text{active}} = 0$ and $N_{\text{active}} = 255$, the ΣΔ sequence ideally degenerates into all-idle or all-active cycles. In principle these would correspond to $(P_B, I_B) = (255, 255)$ and $(255, 0)$, respectively. However, in the STM32 HRTIM implementation the burst registers are defined such that at least one run and one idle slot are always reserved inside each burst. As a result, the tables report $(P_B, I_B) = (255, 254)$ for $N_{\text{active}} = 0$ and $(255, 1)$ for $N_{\text{active}} = 255$. Although this encoding appears shifted by one, the gating logic of the BMC ensures that the effective output still corresponds to fully idle or fully active operation.

For the case $N_{\text{active}} = 1$, the ideal sequence is one active cycle and 254 idle cycles. In principle, this could also be written as a single burst of length $P_B = 255$ with $I_B = 254$. However, in the STM32 implementation, the HRTIM counts half-cycles in center-aligned mode, so the same pattern is represented more compactly with $P_{B0} = 127$ and $I_{B0} = 126$. In both cases, the result is still preserved as a single burst event that reproduces the desired pulse density.

As a result, the effective table size is reduced: each table has dimensions 256×128, and the combined size of both tables is 32,768 bytes, which remains feasible for on-chip memory in STM32-class microcontrollers. In this way, the reduction in sequence length directly lowers the number of register updates and memory usage while still preserving the statistical properties of the modulation.

Since the implementation of the ΣΔ modulator in the STM32 microcontroller has been established, the next step is to focus on the hardware design of the SRC-DCX. This setup provides the experimental platform on which the proposed control can be validated. In the following section,

the design considerations of the SRC hardware are presented, followed by the results that demonstrate the capability of ΣΔ-based cycle-skipping modulation to regulate power while maintaining soft switching and suppressing low-frequency ripple.

4.5 Hardware Design of a Series Resonant Converter

During the design process, a resonant tank with a quality factor Q should not exceed 0.85 at the rated power P_m, offers a practical solution for minimizing component count and leveraging the transformer leakage inductance L_{lk} as the resonant inductance L_r, eliminating the need for an additional external inductor. Unlike high-Q designs ($Q > 1$), which necessitate external inductors and risk saturation, a lower Q enable using embedded inductor L_r and avoids the risk of saturation. Furthermore, the voltage gain of the SRC remains unaffected by high or low Q values when the switching frequency f_{sw} is equal to or near the resonant frequency f_r, making a high-Q design unjustified.

The lower Q-factor results in a sinusoidal half-cycle discontinuous current in the resonant tank [116]. By setting the switching frequency f_{sw} 5% lower than the resonant frequency f_r, as shown in Table 4.5, the magnetizing current is given sufficient time to charge and discharge the parasitic capacitances of the MOSFETs, ensuring a load-independent soft-switching of the primary-side semiconductors, during the dead-time [117]–[119].

The switching frequency f_{sw} of the designed converter is 100 kHz, as specified in Table 4.5. This high switching frequency allows for a smaller transformer design, specifically reducing the required core area product. Consequently, a PQ 50/50 ferrite core made of 3C95 material has been selected, along with a matching PQ 50/50 bobbin.

The minimum number of primary winding turns can be calculated using the following equation:

$$N_p = \frac{V_{\mathrm{dc}}}{4.44 A_e B_{max} f_{sw}}, \tag{4.14}$$

where A_e is the effective cross-sectional area of the core, and B_{max} is the maximum magnetic flux density. Due to the high switching frequency, B_{max} should be chosen well below the saturation point to minimize core losses and prevent overheating. In this design, a conservative value of 100 mT is selected for B_{max}. Based on the transformer core datasheet, the effective area A_e is 328 mm^2. Using (4.14), the number of primary turns is calculated to be 28. A similar approach is used to determine the number of secondary turns. For winding, a litz wire composed of 400 strands of 0.04 mm diameter (400×0.04) is used. The winding is arranged in a zigzag pattern across four layers to complete the required seven turns per layer, effectively accommodating the calculated total number of turns. As a result, a leakage inductance of 81.7 μH has been achieved. Additionally, an air gap is introduced in the transformer core to reduce the magnetizing inductance to a level suitable for ensuring zero-voltage switching (ZVS) in the SRC-DCX converter. The remaining hardware components required for the converter design are listed in Table 4.6. The

Table 4.5: Experimental setup parameters.

Parameters	Symbol	Value	Unit
Input voltage	V_{dc}	400	V
Output voltage	V_o	400	V
Switching frequency	f_{sw}	100	kHz
Resonant frequency	f_r	105	kHz
Leakage/Resonant inductor	L_{lk}	81.7	μH
Resonant capacitor	C_r	28	nF
Rated power	P_m	1	kW
DC link capacitor	C_1, C_2	50	μF
DC blocking capacitor	C_b	60	μF
Quality factor	Q	0.4	-
Transformer turns ratio	n	28:28	-

Table 4.6: Main Hardware components.

Components	Part number	Count
SiC MOSFETs	AIMBG75R090M1HXTMA1	4
SiC Diodes	IDK06G65C5XTMA2	4
Gate Drivers	ACPLP345500E	4
Isolated DC supplies	MGJ2D122005SC	4
Transformer core	PQ50/50-3C95	2
Transformer coil	B65982E0012D001	1
Resonant capacitors	R413F133050D0K	9
DC link capacitors	890494429005CS	2
DC blocking capacitor	B32778G8606K000	1

same experimental setup has been used in the Chapter 3 (Asymmetrical-Bidirectional DC/DC Converter) on page 39, for verifying the proposed active-power sharing control between the two parallel connected partially scaled active and diode bridges.

4.5.1 Power Regulation of an SRC-DCX

As mentioned in the previous sections, a ΣΔ modulation can be employed to implement optimized cycle-skipping and enables precise power flow control without altering the fixed 50% duty cycle of the switches. The power regulation can be achieved by varying the pulse density D, applied to the input of the ΣΔ modulator, which generates optimized cycle-skipping. Thus, the relation between the pulse density D and the converter's rated power defined in (4.9) can be achieved as:

$$P_{\text{in}} = DP_m. \tag{4.15}$$

Equation (4.15) highlights the linear relationship between the modulator input signal D and the converter's rated power P_m. By varying D from 0 to 1, the power transferred by the converter can be smoothly regulated, without requiring any additional regulators typically used for DCX converters. When $D = 1$, the converter switches continuously without skipping; when $D = 0$, all switching cycles are skipped, and no power is transferred. However, it is important to note that in [115], a similar analysis resulted in a nonlinear relationship between D and P_m. This discrepancy arises because the converter in [115] operates in boost mode, whereas the SRC-DCX considered here maintains a one-to-one voltage conversion ratio. Therefore, further studies are needed to verify the

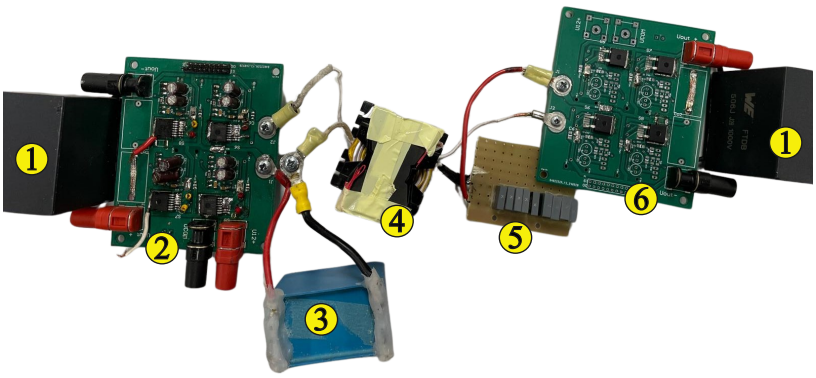


Figure 4.7: Experimental prototype, including: (1) DC link capacitors; (2) Primary bridge; (3) DC blocking capacitor; (4) High frequency transformer; (5) Resonant capacitors; (6) Secondary bridge

proposed modulation technique for all DCX modes discussed in [117] to gain a comprehensive understanding of the converter's power regulation across its operating range.

4.5.2 Experimental Validations

An experimental prototype of the converter, shown in Fig. 4.7, was developed based on the design methodology described in Section 4.5. The system parameters and key hardware components are summarized in Table 4.5 and Table 4.6, respectively.

The experimental results were obtained under open-loop control, and the corresponding waveforms are shown in Fig. 4.8. Each set includes the transformer primary and secondary voltages (V_1 and V_2), the resonant capacitor voltage (V_{C_r}), and the resonant current (i_{lk}). The results are presented for different numbers of active cycles N_{active} within a 255-cycle burst window. As previously discussed, the pulse density D is defined as $D = N_{\text{active}}/255$, and the corresponding values in Fig. 4.8 are: (a) 1; (b) 0.90; (c) 0.86; (d) 0.78; (e) 0.63; (f) 0.55; (g) 0.47; (h) 0.39.

For $D = 1$ [Fig. 4.8(a)], no skipping occurs, and the waveforms appear sinusoidal as expected. As D decreases, skipping intervals gradually emerge, as seen in Figs. 4.8(b)–(h). A noteworthy case is $D = 0.55$ [Fig. 4.8(f)], where the $\Sigma\Delta$ modulator introduces an additional active pulse after every few cycles. Such a pattern cannot be realized using conventional CSM, where only fixed burst intervals are possible (e.g., $D = 0.5$). This highlights a key advantage of the $\Sigma\Delta$ approach: fractional densities can be realized without long consecutive idle runs.

It is also important to note that the burst window length is fixed at 255 cycles. In conventional CSM, this would result in long contiguous idle periods at low D, leading to significant low-frequency ripple. In contrast, the proposed $\Sigma\Delta$ scheme distributes the skipped cycles more uniformly, so that only short idle segments are observed in Figs. 4.8(f)–(h). As a result, the output voltage ripple is substantially reduced compared to the conventional case.

Finally, during skipping intervals, the primary voltage V_1 collapses to zero while the secondary diode bridge voltage V_2 is clamped to the resonant capacitor voltage V_{C_r}. Since $V_{C_r} < V_o$, all diodes remain reverse-biased, preventing conduction and ensuring that no unintended current circulates during the idle phase.

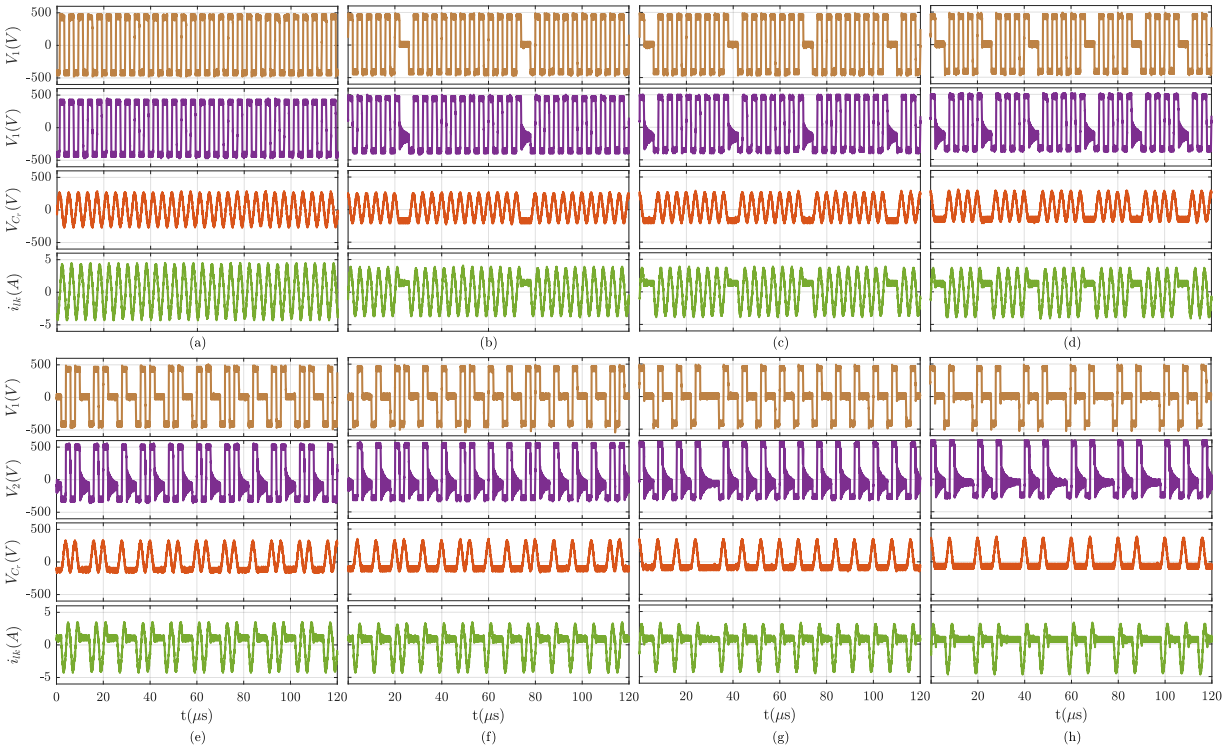


Figure 4.8: Experimental results for different N_{active}: (a) 255; (b) 230; (c) 220; (d) 200; (e) 160; (f) 140; (g) 120; (h) 100. Each scope consists of transformer primary V_1 and secondary V_2 voltages, voltage across resonant capacitor V_{C_r}, and resonant current i_{lk} from top to bottom, respectively.

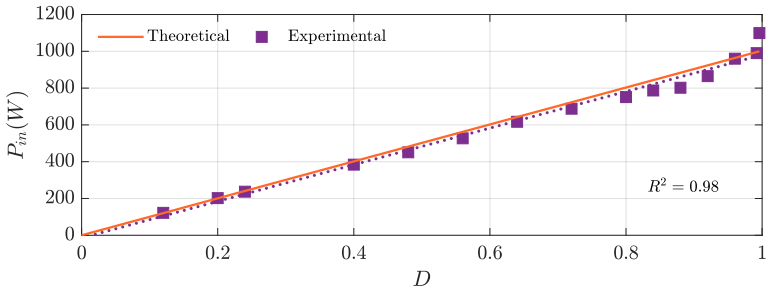


Figure 4.9: Experimental and theoretical verification of power flow control characteristic.

Fig. 4.9 illustrates the converter's power flow control capability, where the input power P_{in} is varied from 100% to 10% of the rated value as a function of the parameter D. The power regulation characteristic exhibits a linear dependence on D, consistent with the theoretical prediction given by (4.15). The experimental results closely match the theoretical values, with a root mean square error (RMSE) of 38 W, which is less than 4% of the rated power, thereby confirming the accuracy of the theoretical model. Furthermore, the coefficient of determination R^2 is calculated to be 0.98, indicating a strong agreement between the experimental data and the theoretical prediction.

Fig. 4.10 shows the efficiency of the converter, both with and without accounting for auxiliary losses, measured using the Yokogawa WT1800 power analyzer. The auxiliary losses, comprising the controller and gate driver consumption, were measured from the auxiliary power supply, and the corresponding power losses are approximated as 2.77 W. As observed from Fig. 4.10, the converter achieves a peak efficiency of approximately 98.4% without considering auxiliary losses, and a minimum efficiency

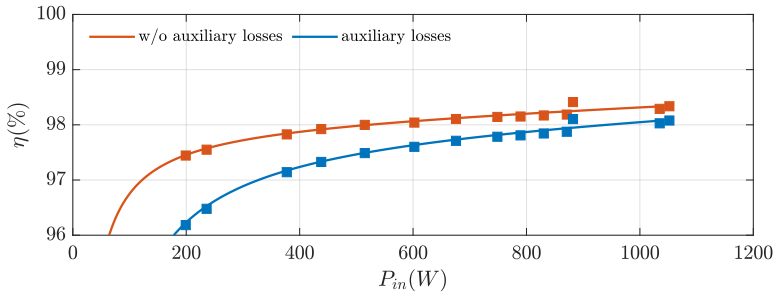


Figure 4.10: Efficiency of the designed converter with and without auxiliary power losses.

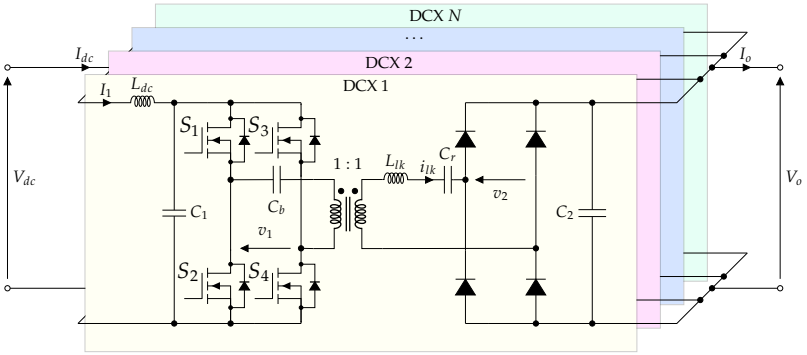


Figure 4.11: IPOP series resonant converter operating as a DC transformer.

of 97.44% down to a 200 W load. When auxiliary losses are included, the maximum and minimum efficiencies become 98.1% and 96.18%, respectively. Considering both cases, the converter maintains an efficiency well above 96% even under light load conditions.

Furthermore, to provide a standardized and application-relevant benchmark, the converter's efficiency was evaluated using the 4-point average method, which considers efficiency at 100%, 75%, 50%, and 25% of rated power. This metric is commonly used in the industry to reflect the typical operating profile of power converters across varying load conditions. Based on this method, the converter achieves an average efficiency of 97.47%, confirming its consistently high performance over a wide load range.

The proposed power regulation method has been validated both theoretically and experimentally. The same approach can also be extended to modular SRC-DCX configurations, such as Input-Parallel Output-Parallel (IPOP) or Input-Series Output-Series (ISOS), to achieve current balancing between modules, where natural parameter tolerances often cause imbalance. Thus, the following section provides a discussion on achieving current balancing in the IPOP configuration.

4.6 Current Sharing Control in Input Parallel and Output Parallel SRC-DCX

DCX-based modular architectures, such as IPOP or ISOS, are limited by their unregulated nature. Even minor parameter mismatches between resonant tanks can cause significant current imbalance, with most of the current flowing through the path of least impedance. As noted in [52], [103], achieving effective power balancing in such configurations remains an open research challenge.

In the context of this work, particular attention is given to the IPOP configuration, where the parallel connection makes the system especially sensitive to parametric tolerances. Several studies [120]–[126] have investigated current-sharing imbalances in modular DCX systems, employing active control, passive methods, or by tuning switching frequency and duty cycle. While these techniques can mitigate current imbalance, they typically require modifications to the topology or modulation scheme and do not provide true power regulation for unregulated DCX converters.

Since power regulation of the SRC-DCX has already been analyzed in the previous sections, the focus here is on demonstrating how the same ΣΔ-based cycle-skipping approach can be employed to achieve current balancing in modular configurations. This capability is experimentally validated with a closed loop control using two 1 kW SRC-DCX prototypes connected in an IPOP arrangement.

The IPOP SRC topology considered in this work is illustrated in Fig. 4.11. It comprises N parallel modules, each identical in terms of electrical parameters. Every module includes an active full-bridge on the primary side and a passive diode bridge on the secondary side, with galvanic isolation provided by a high-frequency transformer. A 1:1 turns ratio is chosen to match the input and output voltage levels. Each module features a series-connected resonant inductor, which is embedded in the transformer as a leakage inductance L_{lk} and a capacitor C_r, forming a resonant tank. A DC blocking capacitor C_b is included to prevent DC current flow, which could otherwise cause magnetic core saturation in the transformer. Moreover, with only an individual DC capacitor at the input, transients generated by one converter can influence the operation of the other. To mitigate this coupling effect, an inductor L_{dc} is added, forming an LC filter, which helps decouple the converters and suppresses high-frequency disturbances.

4.6.1 Experimental Validation

For the power regulation analysis, a single SRC-DCX converter was evaluated, whereas current-sharing verification was carried out using two converters, as shown in Fig. 4.12. Two STM32G474RE microcontrollers were employed to independently drive each converter, allowing separate control of the pulse density parameter D for each module. The following sections discuss the challenges associated with parallel operation of the two modules and present both open-loop and closed-loop results for current balancing.

4.6.2 Parallel Operation of an SRC-DCX

When SRC-DCX converters are connected in either series or parallel using different input and output configurations, they may exhibit unbalanced current sharing, despite being designed for identical rated power with nominally identical components. This current imbalance typically arises due to parameter mismatches in real-world implementations, such as variations in resonant tank elements, transformer coupling coefficients, and input-output voltage differences. These voltage discrepancies are commonly observed in practical converters, as documented in [116].

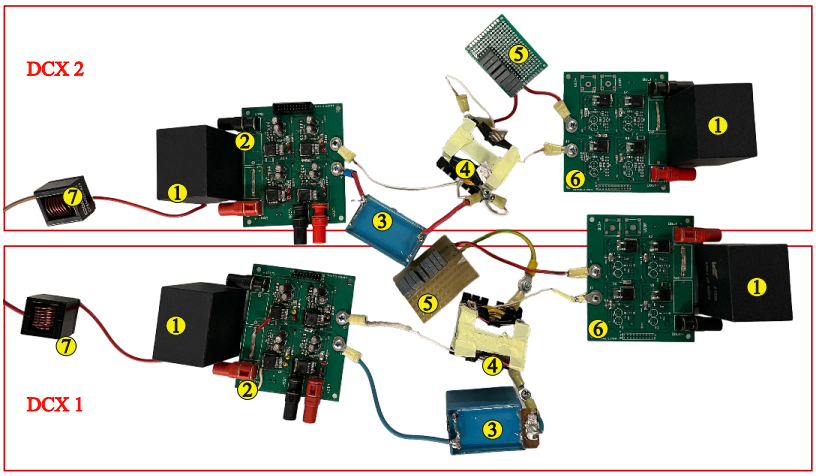


Figure 4.12: Experimental prototype, including: (1) DC link capacitor's; (2) Primary bridge; (3) DC blocking capacitor; (4) High frequency transformer; (5) Resonant capacitor; (6) Secondary bridge; (7) DC Inductors.

Table 4.7: Experimental Setup Parameters.

Parameters	Symbol	DCX 1	DCX 2	Unit
Input voltage	V_{dc}	400	400	V
Output voltage	V_o	400	400	V
Switching frequency	f_{sw}	100	100	kHz
Resonant frequency	f_r	102	105	kHz
Leakage/Resonant inductor	L_{lk}	81.2	82.1	μH
Resonant capacitor	C_r	29.8	27.6	nF
Rated power	P_m	1	1	kW
DC link capacitor	C_1, C_2	50	50	μF
DC inductor	L_{dc}	82	82	μH
DC blocking capacitor	C_b	60	60	μF
Quality factor	Q	0.40	0.41	-

To investigate this current sharing issue, specifically in IPOP, two converter prototypes, DCX 1 and DCX 2, shown in Fig. 4.12, were designed and fabricated, resulting in the specifications outlined in Table. 4.7. Individual testing of these converters at a fixed 400 V output voltage revealed significant performance differences. DCX 1 reached its rated power of 1 kW at an input voltage of 427 V, while DCX 2 required only 423 V to reach the same power level. This 4 V input difference creates challenges in parallel operation. At 427 V, DCX 2 becomes overloaded, while at 423 V, DCX 1 underutilizes its capacity. In addition to voltage variations, a finite mismatch in resonant tank parameters also exists, as summarized in Table 4.7. These discrepancies underscore the need for current sharing control strategies in parallel-connected DCX systems.

4.6.3 Open-Loop Control Validation

Given that DCX 2 reaches its rated power at 423 V, the combined system input voltage during open-loop testing is limited to 425 V. This constraint prevents DCX 2 from overloading while ensuring reasonable operation for both converters.

Fig. 4.13 illustrates the input currents I_1 and I_2 of DCX 1 and DCX 2, respectively, under open-loop conditions. With a fixed pulse density parameter of $D = 1$, DCX 1 draws approximately 2.0 A, delivering about 0.85 kW. In contrast, DCX 2 draws around 2.7 A, delivering approximately 1.15 kW, clearly indicating an imbalance in current sharing.

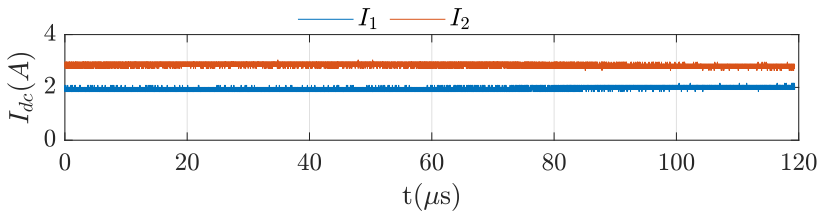


Figure 4.13: Experimental results of DCX's input currents in open-loop.

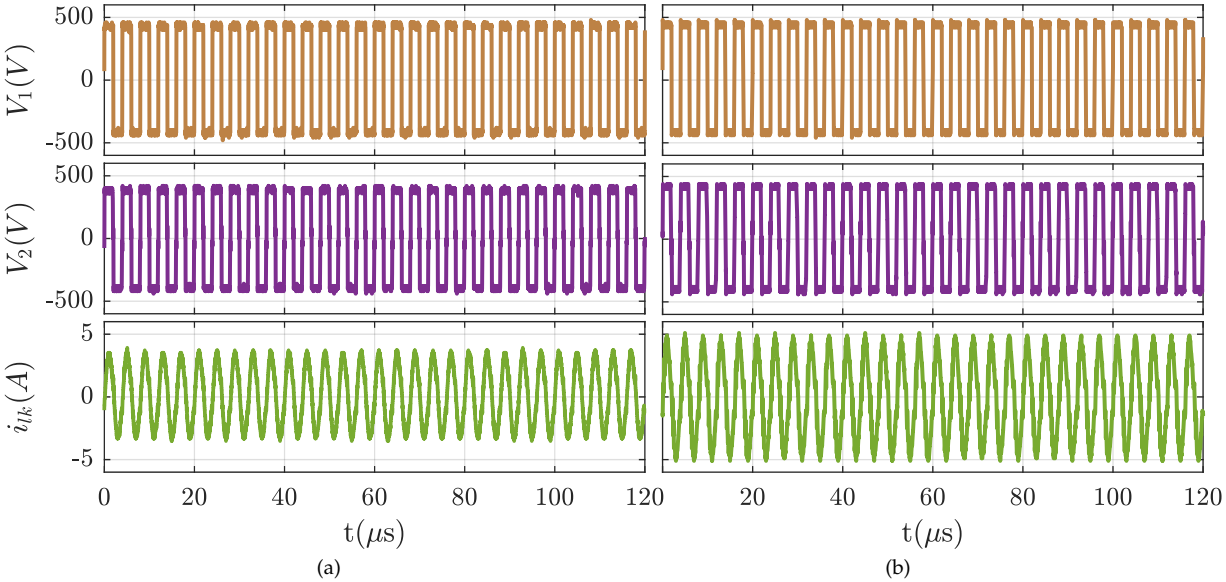


Figure 4.14: Experimental waveforms in open-loop operation; (a) DCX 1; (b) DCX 2.

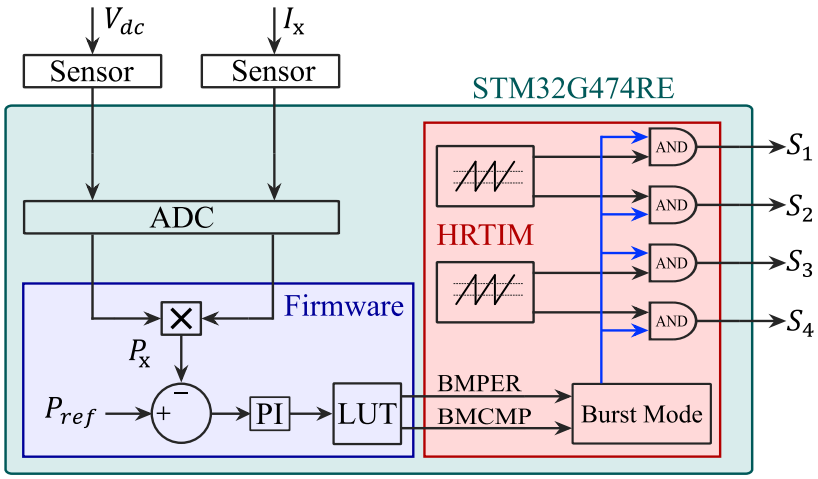


Figure 4.15: Closed-loop control with the proposed ΣΔ modulator for single DCX.

The experimental waveforms of both DCX 1 and DCX 2, specifically the primary and secondary transformer voltages (V_1 and V_2), and the resonant inductor current (i_{lk}), are shown in Fig. 4.14. As observed, with $D = 1$, the system operates without any pulse skipping, resulting in continuous switching for both converters.

To address the current unbalanced scenario, the power processed by DCX 2 can be manually reduced by changing the D value and introducing pulse skipping. This lowers the average current and achieves more balanced load sharing. Manual tuning is feasible for systems with a small number of modules, but for larger-scale parallel configurations, closed-loop control is preferred to ensure automatic current sharing and system stability. Accordingly, a simple PI controller is implemented as

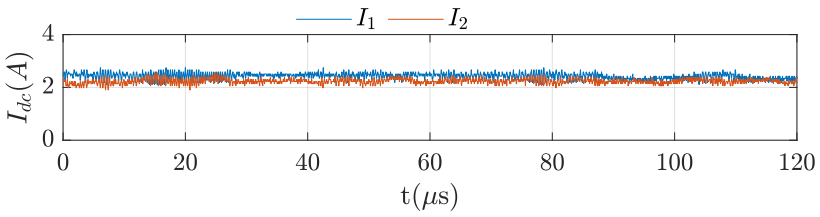


Figure 4.16: Experimental results of DCX's input currents in closed-loop for the 2 kW reference power.

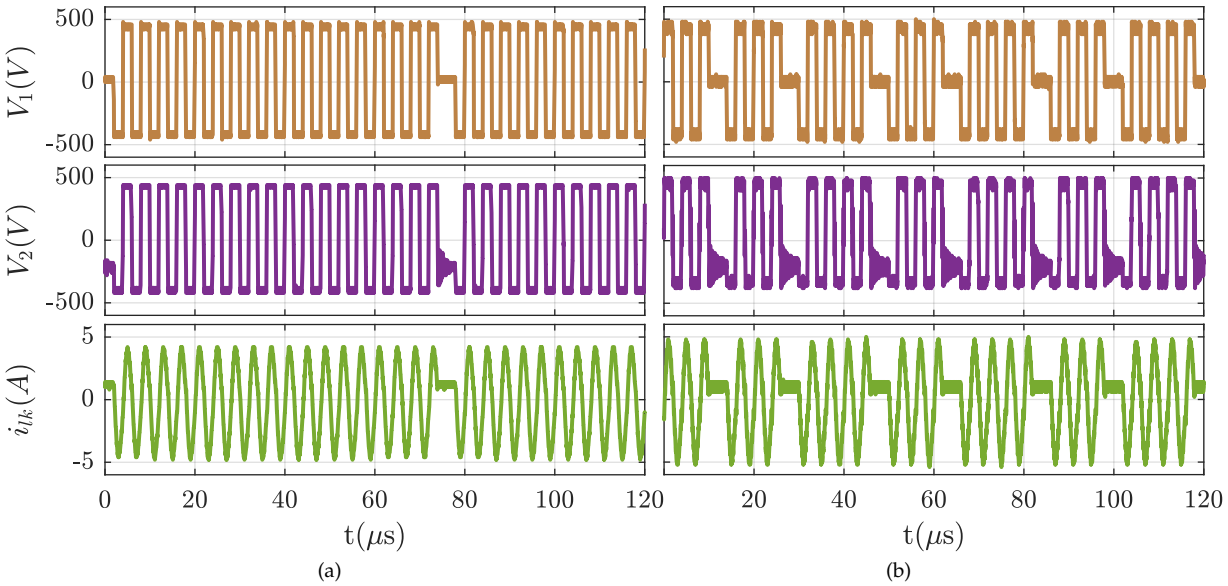


Figure 4.17: Experimental waveforms in closed-loop operation for the 2 kW reference power; (a) DCX 1; (b) DCX 2.

described in Fig. 4.15, depicting that each DCX comprises an individual PI controller. The control system employs two timers from the HRTIM peripheral, each generating two high-resolution PWM signals. Dead time insertion is handled directly by accounting for it when assigning the timer compare values. A PI controller processes the error between the reference power P_{ref} and the measured input power P_{x}. Its output is constrained to the integer range [0 255] and is used as an index for a look-up table (LUT). The corresponding LUT entry is then preloaded into the HRTIM-BMCMP and HRTIM-BMPER registers. It is important to note that the burst mode controller does not modify the compare values of the HRTIM timers directly; instead, it enables or disables the HRTIM outputs, effectively skipping switching cycles. This decentralized approach enables each module to independently regulate its output power, ensuring effective load sharing. Moreover, having individual controllers proves advantageous during phase shedding, as each PI can seamlessly reduce or halt the operation of its respective module without compromising overall system stability.

4.6.4 Closed-Loop Control Validation

The closed-loop performance of the IPOP SRC-DCX system was first evaluated at the maximum reference power of 2.0 kW. Fig. 4.16 shows the regulated input currents of the two converters, from which the input powers can be calculated using the operating voltage V_{dc} = 427.38 V. Under this condition, DCX 1 delivers approximately 1.03 kW and DCX 2 delivers 0.95 kW. The corresponding experimental waveforms in Fig. 4.17

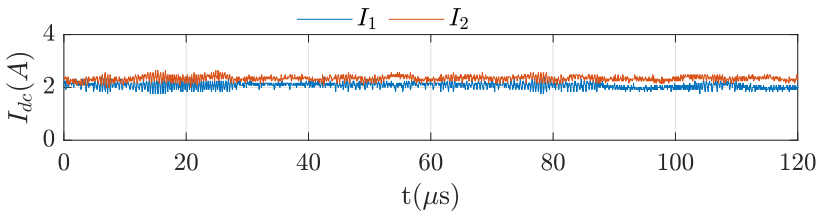


Figure 4.18: Experimental results of DCX's input currents in closed-loop for the 1.8 kW reference power.

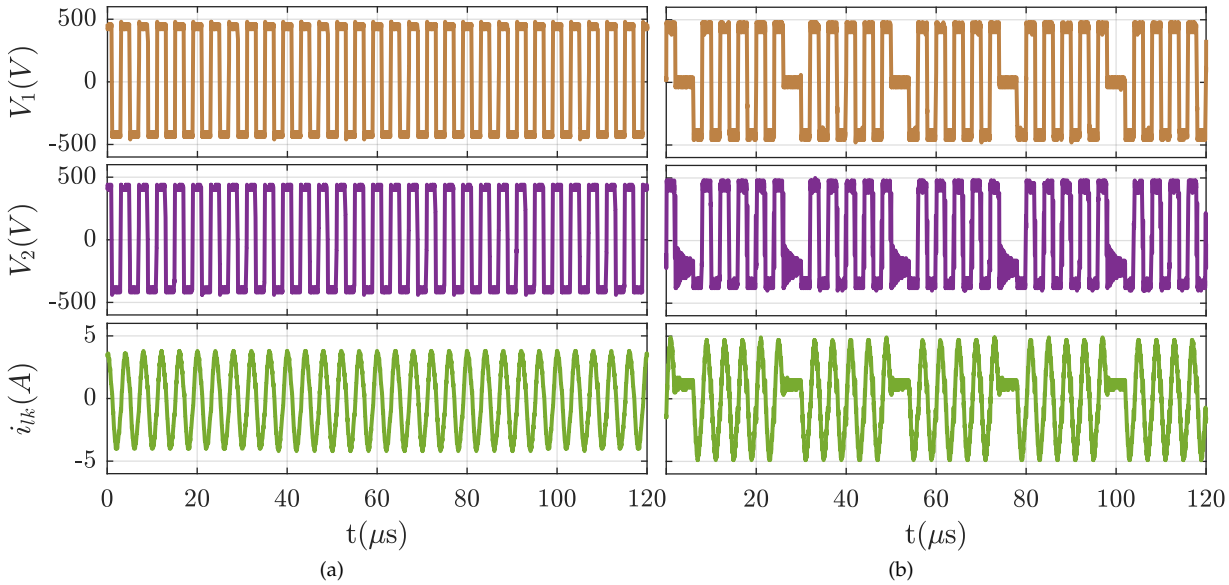


Figure 4.19: Experimental waveforms in closed-loop operation for the 1.8 kW reference power; (a) DCX 1; (b) DCX 2.

illustrate the transformer voltages and resonant current, where the observed skipping pattern corresponds to the pulse density values of $D = 0.88$ for DCX 1 and $D = 0.84$ for DCX 2.

When the total reference power was reduced to 1.8 kW, the operating voltage settled at $V_{\text{dc}} = 426.53$ V. The input currents in Fig. 4.18 show that DCX 1 and DCX 2 deliver 0.92 kW and 0.98 kW, respectively. The associated waveforms in Fig. 4.19 reveal that DCX 1 operates at $D = 1.00$ while DCX 2 regulates power transfer at $D = 0.78$. The small mismatch in delivered powers is attributed to component tolerances, wiring resistances, and PI controller offsets, but overall current sharing remains stable.

For the 1.0 kW case, the operating point was reached at $V_{\text{dc}} = 422.70$ V. From the input currents in Fig. 4.20, DCX 1 is seen to deliver 0.55 kW and DCX 2 about 0.47 kW. The waveforms in Fig. 4.21 confirm the corresponding pulse density values of $D = 0.92$ and $D = 0.78$.

Finally, at 600 W total load, the operating point was reached at $V_{\text{dc}} = 421.8$ V. The input currents in Fig. 4.22 indicate that DCX 1 and DCX 2 deliver 0.35 kW and 0.30 kW, respectively. The waveforms in Fig. 4.23 show reduced pulse densities, with $D = 0.74$ for DCX 1 and $D = 0.70$ for DCX 2. These results demonstrate that as P_{ref} decreases, the converters reach the required power at progressively lower input voltages, while the controllers adapt the pulse-density commands to maintain current sharing. It is important to note that the pulse density values D are only the outputs of the PI controllers. They do not directly represent the maximum capability of the converters. The actual operating point is determined together by the input voltage and the chosen reference power.

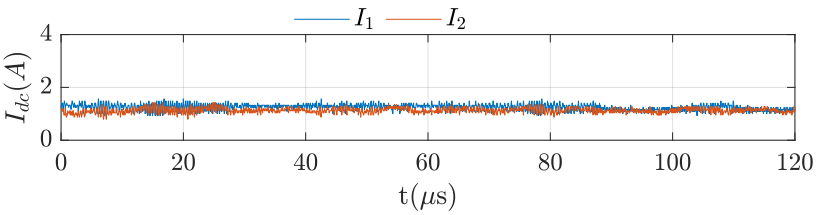


Figure 4.20: Experimental results of DCX's input currents in closed-loop for the 1 kW reference power.

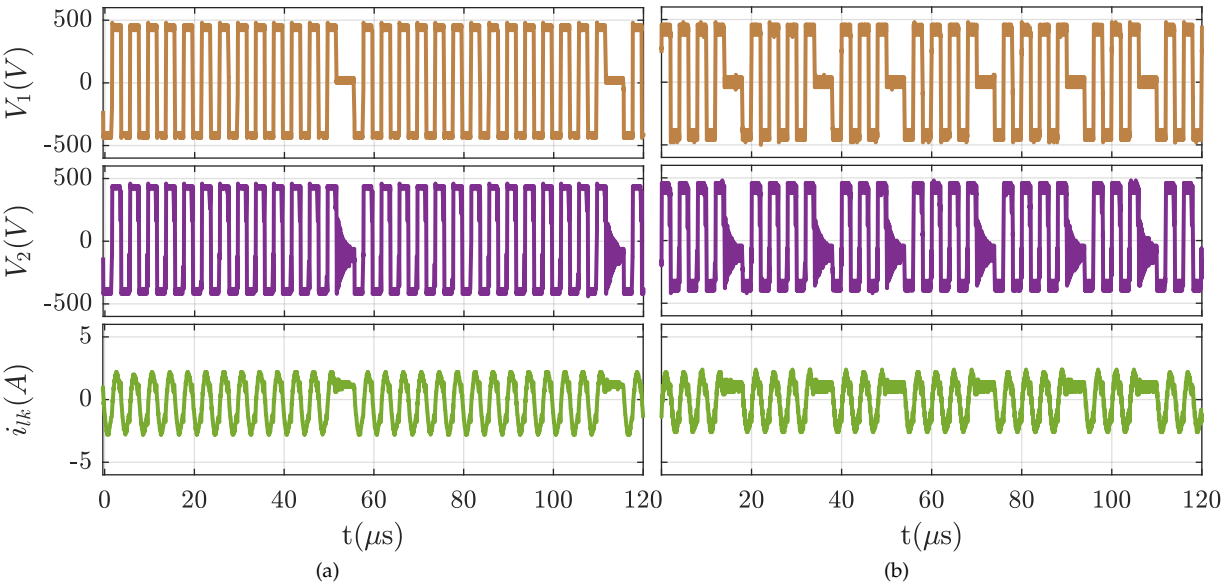


Figure 4.21: Experimental waveforms in closed-loop operation for the 1 kW reference power; (a) DCX 1; (b) DCX 2.

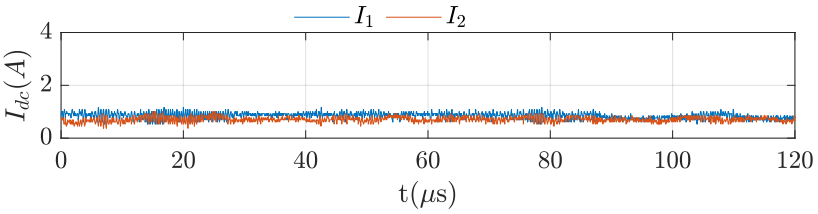


Figure 4.22: Experimental results of DCX's input currents in closed-loop for the 0.6 kW reference power.

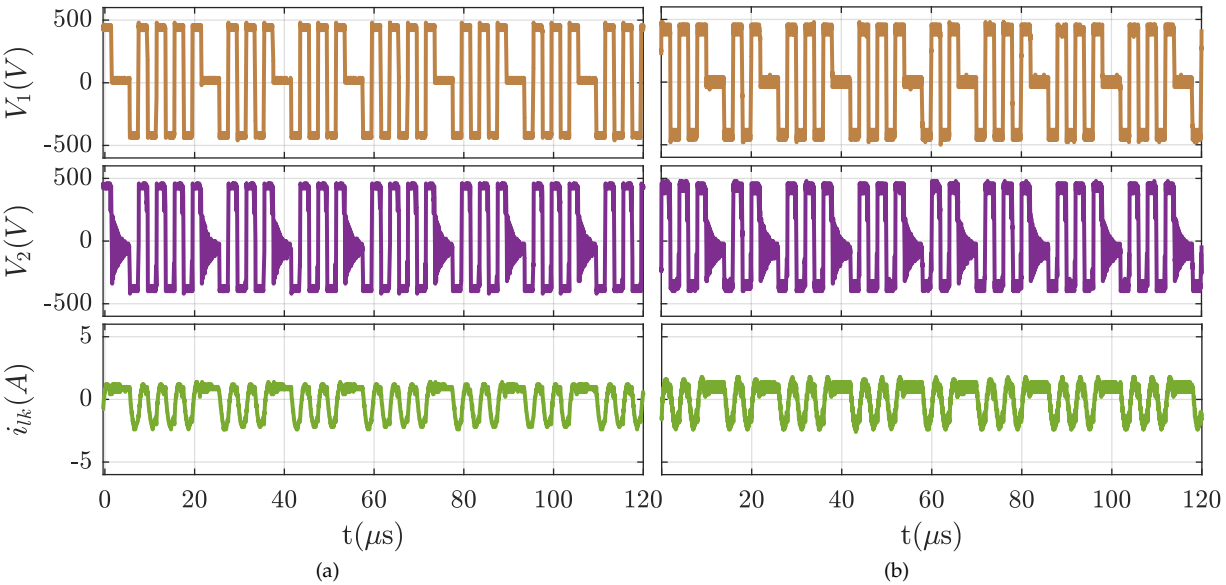


Figure 4.23: Experimental waveforms in closed-loop operation for the 0.6 kW reference power; (a) DCX 1; (b) DCX 2.

Table 4.8: Experimental data for different load conditions.

P_{ref} (kW)	V_{dc} (V)	I_1 (A)	I_2 (A)	P_1 (kW)	P_2 (kW)	P_{in} (kW)	DCX 1-D	DCX 2-D	ε_{ref} (%)	ε_{share} (%)
1.0	427.38	2.42	2.23	1.03	0.95	1.98	0.88	0.84	-1.00	4.04
0.9	426.53	2.15	2.30	0.92	0.98	1.89	1.00	0.78	+5.00	3.17
0.8	424.88	1.93	2.10	0.82	0.89	1.71	1.00	0.84	+6.87	4.09
0.7	423.62	1.75	1.76	0.74	0.75	1.48	1.00	0.82	+5.71	0.68
0.5	422.70	1.29	1.12	0.55	0.47	1.08	0.92	0.78	+8.00	7.41
0.4	421.75	1.07	0.85	0.45	0.36	0.80	0.92	0.78	0.00	11.25
0.3	421.79	0.84	0.70	0.35	0.30	0.65	0.74	0.70	+8.33	7.69
0.2	418.86	0.61	0.46	0.26	0.19	0.44	0.86	0.62	+10.00	15.91

The experimental results confirm the theoretical dependence of the maximum transferable power on the equivalent resistance, which can be expressed as:

$$P_{ref} = \frac{V_{dc}^2}{R_{ac}}, \tag{4.16}$$

where V_{dc} is the common input voltage and R_{ac} represents the equivalent resistance seen by each module. In practice, R_{ac} is never identical due to tolerances in transformer windings, PCB traces, and wiring resistances. As a result, even with the same input voltage, the two converters may exhibit slightly different power levels in open loop. The closed-loop controller compensates for these differences by regulating the pulse-density parameter D, ensuring that both converters share the load proportionally. The trend of lower V_{dc} being required as P_{ref} decreases is consistent with this relationship, as seen in the experimental results. Overall, the proposed control strategy achieves stable current sharing and reliable power regulation across a wide load range, with only minor deviations due to non-idealities.

Table 4.8 provides a summary of the closed-loop experimental results for different reference powers obtained using the Yokogawa WT1800 power analyzer. The table lists the operating input voltage V_{dc}, the average input current values of the two converters, the corresponding powers P_1 and P_2, the measured input power P_{in}, and the observed pulse-density values of DCX 1 and DCX 2. In addition, two error metrics are included:

$$\varepsilon_{ref} = \frac{P_{in} - 2P_{ref}}{2P_{ref}}, \qquad \varepsilon_{share} = \frac{|P_1 - P_2|}{P_{in}}, \tag{4.17}$$

where ε_{ref} indicates the tracking error with respect to the reference power, and ε_{share} quantifies the power imbalance between the two converters.

As observed, the tracking error ε_{ref} remains within ±10% across the full power range, while the sharing error ε_{share} is typically below 10% except at very light load (0.4 kW), where tolerances and controller offsets have a stronger influence. The results highlight that the strategy remains effective across the tested operating range, including challenging light-load conditions.

Fig. 4.24 illustrates the measured input voltage V_{dc} as a function of input current I_{dc} for both DCX 1 and DCX 2 under closed-loop operation. As observed, both converters maintain closely matched input currents throughout the operating range, demonstrating effective current balancing across the full power range, consistent with the values reported in Table 4.8. The zoomed plot highlights the region near the rated power

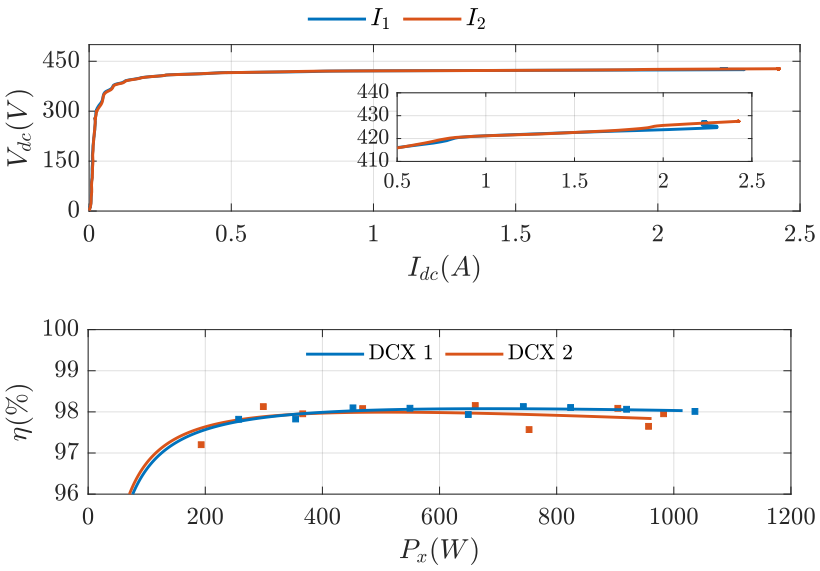


Figure 4.24: Experimental results of both converters depicting input voltage and input currents over the full power range.

Figure 4.25: Experimentally obtained efficiency of both converters.

point, clearly showing that both DCX 1 and DCX 2 reach their full rated output power of 2 kW when the input voltage approaches 427 V. It is also evident from the zoomed plot that as the total power reference is reduced, the corresponding operating voltage V_{dc} decreases slightly, consistent with the individual operating points summarized earlier.

Fig. 4.25 summarizes the measured efficiency profiles of both converters. As shown, both modules achieve nearly flat efficiency curves across the operating range, with a peak efficiency of approximately 98%. It should be noted that gate-driver losses are excluded from this evaluation. The smooth interpolation curves were generated following the methodology described in [66].

At light-load conditions, the combined efficiency of the two converters remains in the range of 96–98%. This can be further improved by employing phase-shedding techniques, since under such conditions it is not necessary to operate both converters simultaneously. Furthermore, the measured four-point efficiencies of DCX 1 and DCX 2 are 97.83% and 97.97%, respectively, confirming the consistent performance of the two modules.

It is also worth noting that small mismatches in power sharing between DCX 1 and DCX 2, as discussed in the Table 4.8, do not significantly affect the overall efficiency. The maximum observed efficiency difference between the two converters is only 0.14%, which is negligible in practice. This demonstrates that the proposed closed-loop strategy not only balances the power effectively but also maintains high efficiency across the full operating range.

4.7 Summary

This chapter focused on the SRC operated as a DCX, highlighting its potential as a unidirectional alternative to DAB-based topologies in DC microgrids. After introducing the fundamental AC analysis, the equivalent load resistance was derived and used to establish the maximum power capability of the SRC-DCX. The gain characteristics were analyzed,

showing that at resonance the converter behaves as a DC transformer with load-independent operation. While this property simplifies design and allows high efficiency, it also prevents straightforward power regulation using frequency or phase-shift control.

To address this limitation, the CSM was introduced as a method to regulate power without compromising soft-switching. The principle of active and idle cycles was explained, and the drawbacks of conventional burst-type CSM, particularly the large low-frequency ripple associated with clustered idle intervals, were highlighted. Building on this, ΣΔ–based CSM was proposed to distribute skipped cycles more evenly, thereby reducing ripple and improving regulation quality.

The experimental validation demonstrated the feasibility of ΣΔ CSM for SRC-DCX power regulation and further extended its application to parallel-connected configurations. In IPOP arrangements, the technique enabled current sharing between modules without requiring additional balancing circuits. Closed-loop tests confirmed robust power tracking and effective load sharing across a wide range of operating points, with only minor deviations due to tolerances and measurement offsets.

Finally, efficiency measurements showed that both modules achieved peak efficiencies close to 98%, with consistent performance across the load range. At light load, the possibility of applying phase-shedding techniques was noted as a way to further improve overall efficiency.

In summary, this chapter established the SRC-DCX with ΣΔ cycle-skipping control as a practical, efficient, and scalable solution in DC microgrids, complementing the DAB-based topologies studied in the earlier chapters. The research outcomes from this chapter have led to the publications [127], [128].

[127]: Pittala *et al.* (2025), 'Cycle-Skipping Technique Based on Sigma-Delta Modulation in Series Resonant DC Transformer'
[128]: Pittala *et al.* (2026), 'Cycle-Skipping Technique based on Sigma-Delta Modulation for Power Regulation in Modular SRC-DCX'

Conclusion and Future Research 5

Overview

This thesis has focused on the analysis and improvement of isolated DC/DC converters for DC microgrids. In particular, three representative converters were studied: the DAB converter, the AB-DC/DC converter, and the SRC-DCX. The main emphasis throughout the work was placed on developing a deep understanding of the operating principles of these converters, identifying their intrinsic limitations, and proposing novel solutions to overcome the associated challenges.

All original contributions and analyses were carried out with the aim of deriving elegant, simple, and closed-form formulations that remain valid across the full operating conditions of each converter. To this end, time-domain approaches were adopted in order to ensure analytical clarity and generality. Each proposed method was verified by numerical simulations and subsequently validated by experimental measurements, thereby demonstrating both theoretical soundness and practical feasibility.

5.1 Chapter Review and Contribution 97
5.2 Proposal for Future Research 99

5.1 Chapter Review and Contribution

The following section outlines the key analyses and achievements of this thesis. To facilitate straightforward navigation, the content is organised by chapter, with hyperlinks to relevant sections where appropriate.

- **Chapter 1 (Introduction) on page 1**

This chapter introduced the motivation for adopting isolated DC/DC converters in DC microgrids, particularly in applications such as electric vehicle charging, energy storage integration, and smart buildings. The state of the art in converter topologies was briefly outlined, highlighting the importance of isolation, bidirectional operation, efficiency, and modular scalability. The research objectives and the structure of the thesis were then presented.

- **Chapter 2 (Zero-Voltage Switching Analysis of Conventional and Current-Fed DAB Converters) on page 15**

This chapter analyzed the ZVS conditions of both the conventional DAB and the CF-DAB converters. The design guidelines are useful to support the systematic sizing of auxiliary components for improved ZVS performance in DAB converters.

- Section 2.2 derived the analytical formulation of the ZVS boundaries for the conventional DAB, providing closed-form conditions for both primary- and secondary-side switches.
- In Section 2.3, the use of auxiliary inductors was proposed to extend the ZVS region at light load, accompanied by a trade-off analysis between the enlarged ZVS range and the associated increase in current stress. Subsections 2.3.4 and 2.3.5 presented the numerical and experimental validation of the proposed ZVS analysis.

- Section 2.4 introduced the concept of the CF-DAB, where the use of interphase inductors enables an additional output port, suitable for both unipolar and bipolar DC microgrid configurations.
- The operating principle of the CF-DAB was described in Section 2.5, followed by the ZVS analysis under no-DC-offset and DC-offset conditions in Subsections 2.5.1 and 2.5.2, respectively.
- Subsection 2.5.3 reported the numerical validation of the CF-DAB ZVS analysis, while Subsection 2.5.4 provided the experimental validation of CF-DAB operation under both unipolar and bipolar load connections.

► **Chapter 3 (Asymmetrical-Bidirectional DC/DC Converter) on page 39**

This chapter focused on the limitations of the conventional DAB in handling asymmetrical bidirectional power flow, particularly in EV charging systems, and discussed the AB-DC/DC converter as a solution. The proposed active power sharing control is essential for this type of converter, as small parameter variations can lead to significant power imbalances when relying solely on passive power allocation.

- Section 3.2 presented the working principle of the SAB converter, along with closed-form analytical power formulations and the condition under which the converter transitions from DCM to CCM operation.
- Section 3.3 described the operating principle of the AB-DC/DC converter, developed on the basis of the SAB characteristics.
- Section 3.4 analyzed the passive power allocation between the partial-scale active bridge and the diode bridge connected in parallel on the secondary side of the AB-DC/DC converter. The following subsections provided a statistical evaluation of the effects of magnetic tolerances on passive power allocation. Numerical validation confirmed that even small parameter variations lead to a loss of the intended passive power distribution.
- Section 3.5 introduced a novel modulation strategy to overcome the limitations of passive allocation by enabling active power-sharing control, thereby regulating the distribution of power between the diode bridge and the active bridge. Subsections 3.5.1 to 3.5.5 detailed the converter operation across different boundary regions and derived closed-form power formulations for both bridges. The developed analysis was validated through numerical and experimental results in Subsections 3.5.6 and 3.5.9.
- Since the proposed modulation technique may cause uneven thermal loading of the active and diode bridges, Section 3.6 introduced a hybrid modulation approach that alternates between conventional SAB modulation and the proposed active power-sharing modulation. This technique was numerically validated, with particular focus on the DCM region in Subsection 3.6.1.

► **Chapter 4 (Series Resonant DC Transformer) on page 71**

This chapter investigated the SRC operated as a DCX, targeting unidirectional applications such as PV integration in DC microgrids. The proposed sigma-delta-based CSM can solve the various issues related to the conventional CSM and provides a better alternative for regulating the SRC-DCX, while simultaneously achieving power balancing in the modular configurations.

- Section 4.2 derived the AC equivalent circuit and discussed the general concept of first harmonic approximation. Using this, the maximum power capability and gain characteristics of the SRC were analyzed, showing its load-independent DCX operation at resonance.
- Section 4.3 introduced cycle-skipping modulation (CSM) as a means of regulating the SRC-DCX. The principle of active and idle cycles was described, and the drawbacks of conventional burst-mode CSM, especially low-frequency ripple, were identified.
- Section 4.4 presented sigma–delta–based CSM, which distributes skipped cycles more evenly to suppress ripple while maintaining ZVS. Implementation of the proposed $\Sigma\Delta$ modulation on an STM32 microcontroller was also described in Subsection 4.4.2.
- Section 4.5 experimentally validated the sigma–delta CSM for standalone SRC-DCX power regulation, confirming accurate tracking and providing the efficiency of the designed converter.
- Section 4.6 extended the technique to Input-Parallel Output-Parallel (IPOP) configurations for achieving power balancing. Subsection 4.6.1 reported the experimental validation providing both open-loop and closed-loop current sharing. The depicted results confirmed robust current balancing, stable regulation, and efficiencies of two modules close to 98%.

5.2 Proposal for Future Research

Future research could address the remaining gaps and extend the developments carried out in this thesis.

In the case of the auxiliary-inductor-based DAB, this work showed that efficiency is reduced at light load. However, with improved PCB layout practices and optimized auxiliary inductor core design, the light-load efficiency can be further enhanced.

For the CF-DAB, the ZVS analysis was numerically validated, and future work will focus on experimental validation. In addition, voltage balancing remains a challenge in bipolar DC grids. With appropriate hardware modifications or the adoption of novel modulation techniques, the CF-DAB topology could be adapted to address this issue effectively.

Regarding the AB-DC/DC converter, this thesis demonstrated active power distribution from the diode bridge to the active bridge. To improve thermal distribution, a hybrid modulation technique was introduced. Nevertheless, with the implementation of a closed-loop control scheme, it may be possible to achieve dynamic power sharing between the active and diode bridges directly, potentially eliminating the need for hybrid modulation.

Finally, for the SRC-DCX, this thesis presented a theoretical evaluation of ripple characteristics under cycle-skipping control. Future work should experimentally validate this analysis. Moreover, the proposed sigma–delta cycle-skipping approach was only applied to the SRC-DCX, whereas several other DCX topologies exist in the literature. Extending the study to different DCX structures would provide a broader understanding of the linear relationship between pulse density and regulated power, thereby establishing the generality of the proposed technique.

Appendix

A

PLECS Simulation Script

A.1 Parameter Sweep Analysis for Statistical Analysis

The following script corresponds to the statistical analysis of magnetic tolerances presented in Chapter 3 (Asymmetrical-Bidirectional DC/DC Converter) on page 39, Section 3.4.3. For illustration, the Case 1 script file is shown; Cases 2 and 3 can be reproduced by modifying the coupling inductor values according to Table 3.1.

```
t = [0.000999999 0.001];
L1 =  38e-6;
L2U = 15e-6;
L3U = 10e-6;
L2L = 15e-6;
L3L = 10e-6;
N = 10000;
Vin = 200;
m = 0.5;
f = 20e3;
p = 1475;

% Create an empty array to store inductance values
inductanceValues = zeros(N, 5);
powerData = zeros(N, 4);

for i = 1:N

    plecs('set','./counter','Value',num2str(i));

    % Generate random inductance values
    randL1  = [rand(1)*0.4+0.8]*L1;
    randL2U = [rand(1)*0.4+0.8]*L2U;
    randL3U = [rand(1)*0.4+0.8]*L3U;
    randL2L = [rand(1)*0.4+0.8]*L2L;
    randL3L = [rand(1)*0.4+0.8]*L3L;

    % Store the random values in the inductanceValues array
    inductanceValues(i, :) = [randL1, randL2U, randL3U, randL2L, randL3L]

        Leq = randL1+randL2U*randL3U/(randL2U+randL3U)+randL2L*randL3L/(randL2L+randL3L);
        k = Vin^2/(f*Leq);
        d = 0.5-0.5*sqrt(1-m^2-(8*p)/(k*m));

```

```
    % Set the inductance values for the model elements
    plecs('set', './L1', 'L', num2str(randL1));
    plecs('set', './L2A', 'L', num2str(randL2U));
    plecs('set', './L3A', 'L', num2str(randL3U));
    plecs('set', './L2B', 'L', num2str(randL2L));
    plecs('set', './L3B', 'L', num2str(randL3L));
        plecs('set', './Constant3', 'Value', num2str(d));

    % Run the simulation
    plecs('simulate');

    % Export power data from the scope at each time step
    plecs('scope', './Scope', 'ExportCSV', ['PLECS_TEMP.csv'], t);
    temp = dlmread('PLECS_TEMP.csv', ',', 3, 1);

    % Store the power data for this iteration
    powerData(i, :) = temp(1:4)
end

save -mat7-binary 'sweep_L_01.mat' 'inductanceValues' 'powerData'
```

A.2 Parameter Sweep Analysis for Active- and Diode Bridge Power Measurements

The following MATLAB script computes the diode turn-on delay c and the phase-shift d for all operating regions of the AB-DC/DC converter. The swept values are exported as separate `.csv` files, one per operating region.

```
m = 0.5;
step = 0.04;
c_vals = 0.001:step:0.5;
d_vals = 0.001:step:0.5;
% Containers for each condition
c1_c = []; c1_d = [];
c2_c = []; c2_d = [];
c3_c = []; c3_d = [];
c4_c = []; c4_d = [];
dab_fm_c = []; dab_fm_d = [];
dab_rm_c = []; dab_rm_d = [];
all_c = []; all_d = [];
for di = 1:length(d_vals)
    d = d_vals(di);
    for ci = 1:length(c_vals)
        c = c_vals(ci);
        % --- DCM ---
        cond1 = false;
        if d > m/4
            cond1 = (0 < c) && (c <= 0.25 - d);
        else
            cond1 = (0 < c) && (c <= d);
        end
```

```
        if cond1
            c1_c(end+1) = c;
            c1_d(end+1) = d;
        end
        % --- Hybrid-1 ---
        cond2 = false;
        if d < m/2
            cond2 = ((0.25 - d) < c) && (c < d);
        else
            cond2 = ((2*d - m) < c) && (c < d);
        end
        if cond2
            c2_c(end+1) = c;
            c2_d(end+1) = d;
        end
        % --- Hybrid-2 ---
        lower_bound = d/2 - m/4;
        upper_bound = (2*d - m)/(2 - 2*m);
        cond3 = (lower_bound <= c) && (c < upper_bound);
        if cond3
            c3_c(end+1) = c;
            c3_d(end+1) = d;
        end
        % --- CCM ---
        extra_bound = d/2 - m/4;
        cond4 = c < extra_bound;
        if cond4
            c4_c(end+1) = c;
            c4_d(end+1) = d;
        end
        % --- DAB-FM ---
        if ((d/2 + 0.25) > c) && (c >= d)
            dab_fm_c(end+1) = c;
            dab_fm_d(end+1) = d;
        end
        % --- DAB-RM ---
        if ((d/2 + 0.25) < c) && (c < 0.5)
            dab_rm_c(end+1) = c;
            dab_rm_d(end+1) = d;
        end
        % --- All conditions met ---
        if cond1 && cond2 && cond3 && cond4
            all_c(end+1) = c;
            all_d(end+1) = d;
        end
    end
end
```

The generated `.csv` files are imported into PLECS through the simulation script and assigned to their corresponding library blocks. For each pair of c and d values, the active bridge power P_2 and the diode bridge power P_3 are collected. The following script illustrates the procedure for importing the `.csv` file and exporting the power data in the DCM region. The same approach can be applied to the other operating regions.

```
model_path = 'E:\ICDCM\ICDCM power sharing.plecs';

% Choose the file that contains c and d
    filename = 'condition1_data.csv';

% Import the CSV file with c and d values
    raw_data = csvread(filename, 1, 0);
    c_values = raw_data(:, 1);
    d_values = raw_data(:, 2);

num_simulations = length(c_values);
f = 100000;

% Create arrays to store the results
power_results = zeros(num_simulations, 2);

% Create a waitbar to show progress
h = waitbar(0, 'Running PLECS simulations...');

% Loop through each pair of c and d values
for i = 1:num_simulations

    % Update the waitbar
    waitbar(i/num_simulations, h,
    sprintf('Running simulation %d of %d', i, num_simulations));

    phasedelay = d_values/f;

    plecs('set','./counter','Value',num2str(i));
    plecs('set', './counter1', 'Value', num2str(c_values(i)));
    plecs('set', './counter2', 'Value', num2str(d_values(i)));

    % Set the duty cycle (c) and phase shift (d)
    parameters in the PLECS model
    plecs('set', './PWM2', 'DutyCycle', num2str(c_values(i)));
    plecs('set', './PWM3', 'DutyCycle', num2str(c_values(i)));
    plecs('set', './PWM1', 'Delay', num2str(phasedelay(i)));

    % Run the simulation
    plecs('simulate');

    % Export power data from the scope at each time step
    csv_filename = sprintf('PLECS_TEMP_%d.csv', i);
    plecs('scope', './Scope8', 'ExportCSV',
    csv_filename, [0.01 0.011]);
    temp = dlmread(csv_filename, ',', 2, 1);

    % Store the power data for this iteration
    power_results(i, :) = temp(1:2)
end

% Close the waitbar
close(h);
```

List of Figures

1.1 Typical architecture of a DC microgrid with various loads and sources [5]. . . . 2
1.2 Unipolar configuration. . . . 3
1.3 Bipolar configuration. . . . 3
1.4 Basic topology of a flyback converter. . . . 6
1.5 Basic topology of a forward converter. . . . 7
1.6 Basic topology of a push–pull converter. . . . 7
1.7 Basic topology of an isolated Ćuk converter. . . . 8
1.8 Dual-active-bridge converter. . . . 10
1.9 Single-active-bridge converter. . . . 11
1.10 Asymmetrical bidirectional DC/DC converter. . . . 11
1.11 Series resonant converter operating as a DC transformer. . . . 12

2.1 Dual-active-bridge converter. . . . 17
2.2 Leakage inductor current over half of the switching period T_{sw}. . . . 17
2.3 ZVS region in the $G - d$ plane: (a) ideal case; (b) parasitic capacitance effect. . . . 19
2.4 Dual-active-bridge converter with auxiliary inductors. . . . 20
2.5 Voltage and current waveforms of an auxiliary inductor at the input side. . . . 20
2.6 Voltage and current waveforms of an auxiliary inductor at the output side. . . . 21
2.7 ZVS extension on the input and output sides of the DAB. . . . 21
2.8 Contour plots of the normalized switch current RMS of the input H-bridge for $\beta \to +\infty$. . . . 22
2.9 Isosurfaces of the normalized switch current RMS in auxiliary inductor case: (a) input bridge; (b) output bridge. . . . 23
2.10 Contour plots of the input side normalized switch current RMS: (a) $\beta = 5$; (b) $G = 1.2$. . . . 24
2.11 Contour plots of the output side normalized switch current RMS: (a) $\beta = 4$; (b) $G = 0.8$. . . . 24
2.12 Input bridge current and commutation trajectory for three β cases. . . . 26
2.13 Output bridge current and commutation trajectory for three β cases. . . . 26
2.14 Experimental setup of auxiliary inductor-based DAB: (1) input bridge; (2) output bridge; (3) high-frequency transformer; (4) auxiliary inductor; (5) input pins for gate signals. . . . 27
2.15 Primary and secondary side voltages (top) and the leakage current (bottom) of the transformer in case of conventional DAB. . . . 28
2.16 Drain-source voltage and gate source voltage: primary side switch S_1 (top) and secondary side switch S_5 (bottom) in case of conventional DAB. . . . 28
2.17 Primary and secondary side voltages (top), leakage current (middle) of the transformer, and auxiliary inductor current (bottom). . . . 29
2.18 Drain-source voltage and gate source voltage: primary side switch S_1 (top) and secondary side switch S_5 (bottom) in case of auxiliary inductor based DAB. . . . 29
2.19 Efficiency of the DAB converter operating without and with auxiliary inductor. . . . 29
2.20 Interleaved current-fed dual-active-bridge converter. . . . 30
2.21 Voltage and current waveforms of the interphase inductors without the DC offset case. . . . 31
2.22 Without DC offset case ZVS region in the G vs d plane for the CF-DAB. . . . 32
2.23 Voltage and current waveforms of the interphase inductors without the DC offset case. . . . 32
2.24 ZVS region in the G vs d plane for $\beta \to \infty$: (a) positive DC offset; (b) negative DC offset. . . . 33
2.25 ZVS region in the G vs d plane for $\beta = 1.5$: (a) positive DC offset; (b) negative DC offset. . . . 33
2.26 Instantaneous switch S_5 and S_6 currents in case of without DC offset: (a) Hard switching; (b) ZVS. 35
2.27 Instantaneous switch S_5 and S_6 currents in case of with DC offset: (a) Positive offset; (b) Negative offset . . . 35
2.28 Experimental setup of CF-DAB: (1) input bridge; (2) output bridge; (3) high-frequency transformer; (4) interphase inductors. . . . 36

2.29 (a) Main waveforms of CF-DAB; (b) Interphase inductor currents without the DC offset in Bipolar configuration. . . . 37
2.30 (a) Interphase inductor currents with the positive DC offset in Unipolar configuration; (b) Interphase inductor currents with the negative DC offset in Unipolar configuration. . . . 37

3.1 Single-active-bridge converter. . . . 42
3.2 Waveforms of SAB converter: (a) DCM; (b) CCM. . . . 42
3.3 Normalized output power P_o (p.u.) as a function of voltage gain m and phase shift d. . . . 43
3.4 Asymmetrical bidirectional DC/DC converter. . . . 44
3.5 Equivalent circuit of the AB-DC/DC converter from the transformer secondary side. . . . 44
3.6 Voltage and current waveforms in conventional DCM. . . . 44
3.7 Voltage and current waveforms in conventional CCM. . . . 44
3.8 Actual and approximated triangular PDF of the converter leg power with different k. . . . 46
3.9 Numerical power distribution together with actual and approximated triangular PDFs of the normalized leg power. Legs A, B, C, and D from left to right. Case 1, 2, and 3 from top to bottom. 49
3.10 Numerical power distribution together with approximated Irwin-Hall PDF of the normalized bridge power. Bridges 2 and 3 from left to right. Case 1, 2, and 3 from top to bottom. . . . 51
3.11 PSFB power shift operation in forward mode: (a) main voltage and current waveforms; (b) equivalent circuit from the transformer secondary side. . . . 53
3.12 Voltage and current waveforms in Hybrid 1 region. . . . 54
3.13 Voltage and current waveforms in Hybrid 2 region. . . . 55
3.14 Voltage and current waveforms in CCM region. . . . 56
3.15 Voltage and current waveforms in DAB-RM region. . . . 56
3.16 Voltage and current waveforms in DAB-FM region. . . . 56
3.17 Operating conditions of the AB-DC/DC converter under active power-sharing control. . . . 57
3.18 Comparison of measured and calculated powers: (a) input power P_1, (b) active bridge power P_2, and (c) diode bridge power P_3. . . . 58
3.19 Thermal map showing converter efficiency (η) with respect to modulation parameters c and d. 59
3.20 Scatter plot of converter efficiency (η) versus output power (P_o) across all operating regions. . . 59
3.21 Simulated voltage and current waveforms for operating regions: (a) DCM-conventional; (b) CCM-conventional; (c) DCM; (d) CCM; (e) Hybrid 1; (f) Hybrid 2; (g) DAB-RM; (h) DAB-FM. . 61
3.22 Experimental prototype: 1. DC-link capacitors; 2. primary-side active bridge; 3. high-frequency transformer; 4. coupling inductors; 5. secondary-side active bridge; 6. secondary-side diode bridge. 62
3.23 Experimental voltage and current waveforms for operating regions: (a) DCM-conventional; (b) CCM-conventional; (c) DCM; (d) CCM; (e) Hybrid 1; (f) Hybrid 2; (g) DAB-RM; (h) DAB-FM. . 63
3.24 Secondary side thermal images of DCM region in active power sharing control. . . . 65
3.25 Secondary side thermal images of CCM region in active power sharing control. . . . 65
3.26 Secondary side thermal images of Hybrid 1 region. . . . 65
3.27 Secondary side thermal images of Hybrid 2 region. . . . 65
3.28 Values of c and d as a function of k_p under several values of G with references to the parameters listed in Table 3.7. . . . 67
3.29 Active-bridge power $\overline{P}_2$, diode-bridge power $\overline{P}_3$, and total output power P_o with respect to the power ratio k_p, depicting both theoretical calculation and numerical results for $G = 1, 1/3$, and $1/5$ (from top to bottom). . . . 68
3.30 Waveforms of voltage and currents: (a) during conventional operation with $k_p = 1.5$; (b) during power shift operation with $k_p = 1$ considering $G = 1, 1/3$, and $1/5$ (from top to bottom). . . . 69

4.1 Series resonant converter operating as a DC transformer. . . . 73
4.2 AC equivalent circuit of a series resonant converter. . . . 73
4.3 Gain characteristics of the series resonant converter. . . . 75
4.4 Ideal waveforms of SRC-DCX converter operating under conventional cycle skipping. . . . 76
4.5 Ideal waveforms of SRC-DCX converter operating under modified cycle skipping technique. . . 77
4.6 Basic idea of sigma-delta modulator. . . . 79

4.7 Experimental prototype, including: (1) DC link capacitors; (2) Primary bridge; (3) DC blocking capacitor; (4) High frequency transformer; (5) Resonant capacitors; (6) Secondary bridge 85
4.8 Experimental results for different N_{active}: (a) 255; (b) 230; (c) 220; (d) 200; (e) 160; (f) 140; (g) 120; (h) 100. Each scope consists of transformer primary V_1 and secondary V_2 voltages, voltage across resonant capacitor V_{C_r}, and resonant current i_{lk} from top to bottom, respectively. 86
4.9 Experimental and theoretical verification of power flow control characteristic. 86
4.10 Efficiency of the designed converter with and without auxiliary power losses. 87
4.11 IPOP series resonant converter operating as a DC transformer. 87
4.12 Experimental prototype, including: (1) DC link capacitor's; (2) Primary bridge; (3) DC blocking capacitor; (4) High frequency transformer; (5) Resonant capacitor; (6) Secondary bridge; (7) DC Inductors. 89
4.13 Experimental results of DCX's input currents in open-loop. 90
4.14 Experimental waveforms in open-loop operation; (a) DCX 1; (b) DCX 2. 90
4.15 Closed-loop control with the proposed $\Sigma\Delta$ modulator for single DCX. 90
4.16 Experimental results of DCX's input currents in closed-loop for the 2 kW reference power. . . . 91
4.17 Experimental waveforms in closed-loop operation for the 2 kW reference power; (a) DCX 1; (b) DCX 2. 91
4.18 Experimental results of DCX's input currents in closed-loop for the 1.8 kW reference power. . . 92
4.19 Experimental waveforms in closed-loop operation for the 1.8 kW reference power; (a) DCX 1; (b) DCX 2. 92
4.20 Experimental results of DCX's input currents in closed-loop for the 1 kW reference power. . . . 93
4.21 Experimental waveforms in closed-loop operation for the 1 kW reference power; (a) DCX 1; (b) DCX 2. 93
4.22 Experimental results of DCX's input currents in closed-loop for the 0.6 kW reference power. . . 93
4.23 Experimental waveforms in closed-loop operation for the 0.6 kW reference power; (a) DCX 1; (b) DCX 2. 93
4.24 Experimental results of both converters depicting input voltage and input currents over the full power range. 95
4.25 Experimentally obtained efficiency of both converters. 95

List of Tables

1.1 Comparison of DC microgrid topologies and configurations. . . . 3
1.2 Proposed classification of the main DC buses for DC microgrids [24]. . . . 5
1.3 Comparison of basic isolated DC/DC converter topologies . . . 9
1.4 Comparison of bridge-based isolated DC/DC converter topologies . . . 12

2.1 Auxiliary inductor-based DAB numerical plant main system parameters. . . . 25
2.2 Analytical and numerical evaluation of switch current RMS. . . . 27
2.3 Auxiliary inductor-based DAB experimental setup parameters. . . . 27
2.4 CF-DAB numerical plant main system parameters. . . . 35
2.5 CF-DAB experimental setup parameters. . . . 36

3.1 Numerical plant main system parameters. . . . 48
3.2 Statistical analysis of measured and predicted powers in each leg. . . . 50
3.3 Statistical analysis of measured and predicted powers on the secondary-side bridges. . . . 50
3.4 Main parameters of the AB-DC/DC converter. . . . 57
3.5 Coefficient of determination of active and diode bridge powers in all the operating regions. . . . 58
3.6 Selected operating conditions to validate voltage and current waveforms. . . . 60
3.7 Numerical plant main parameters of the PSFB in forward mode. . . . 68
3.8 Root Mean Squared Errors for $\overline{P}_2$ and $\overline{P}_3$ during power shift operation. . . . 69

4.1 First ten cycles of a first-order $\Sigma\Delta$ modulator for $D = 3/10$. . . . 80
4.2 Burst register values for $D = 3/10$. . . . 81
4.3 HRTIM-BMPER register – number and duration of the burst mode intervals used to emulate the $\Sigma\Delta$ modulator. . . . 81
4.4 HRTIM-BMCMP register – number of idle periods in the burst mode intervals used to emulate the $\Sigma\Delta$ modulator. . . . 82
4.5 Experimental setup parameters. . . . 84
4.6 Main Hardware components. . . . 84
4.7 Experimental Setup Parameters. . . . 89
4.8 Experimental data for different load conditions. . . . 94

Bibliography

[1] T. Dragičević, X. Lu, J. C. Vasquez, and J. M. Guerrero, 'Dc microgrids—part i: A review of control strategies and stabilization techniques,' *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 4876–4891, 2016. DOI: 10.1109/TPEL.2015.2478859 (cited on pages 1, 2).

[2] V. F. Pires, A. Pires, and A. Cordeiro, 'Dc microgrids: Benefits, architectures, perspectives and challenges,' *Energies*, vol. 16, no. 3, 2023. DOI: 10.3390/en16031217 (cited on pages 1, 2).

[3] W. Tushar, T. K. Saha, C. Yuen, D. Smith, and H. V. Poor, 'Peer-to-peer trading in electricity networks: An overview,' *IEEE Transactions on Smart Grid*, vol. 11, no. 4, pp. 3185–3200, 2020. DOI: 10.1109/TSG.2020.2969657 (cited on page 1).

[4] A. W. Adegboyega, S. Sepasi, H. O. R. Howlader, B. Griswold, M. Matsuura, and L. R. Roose, 'Dc microgrid deployments and challenges: A comprehensive review of academic and corporate implementations,' *Energies*, vol. 18, no. 5, 2025. DOI: 10.3390/en18051064 (cited on page 1).

[5] M. Batool, W. Hassan, and D. D.-C. Lu, 'Review of advanced control strategies for isolated dc–dc converters in dc microgrids,' *IEEE Access*, vol. 13, pp. 103 137–103 154, 2025. DOI: 10.1109/ACCESS.2025.3578910 (cited on pages 2, 10).

[6] D. Kumar, F. Zare, and A. Ghosh, 'Dc microgrid technology: System architectures, ac grid interfaces, grounding schemes, power quality, communication networks, applications, and standardizations aspects,' *IEEE Access*, vol. 5, pp. 12 230–12 256, 2017. DOI: 10.1109/ACCESS.2017.2705914 (cited on pages 1, 3).

[7] K. M. Bhargavi, N. S. Jayalakshmi, D. N. Gaonkar, A. Shrivastava, and V. K. Jadoun, 'A comprehensive review on control techniques for power management of isolated dc microgrid system operation,' *IEEE Access*, vol. 9, pp. 32 196–32 228, 2021. DOI: 10.1109/ACCESS.2021.3060504 (cited on pages 1, 3).

[8] T. Dragičević, X. Lu, J. C. Vasquez, and J. M. Guerrero, 'Dc microgrids—part ii: A review of power architectures, applications, and standardization issues,' *IEEE Transactions on Power Electronics*, vol. 31, no. 5, pp. 3528–3549, 2016. DOI: 10.1109/TPEL.2015.2464277 (cited on page 2).

[9] 'Ieee draft standard for interconnection and interoperability of distributed energy resources with associated electric power systems interfaces,' *IEEE P1547/D6.7.2, May 2017*, pp. 1–116, 2017 (cited on page 2).

[10] 'Ieee draft standard for interconnection and interoperability of distributed energy resources with associated electric power systems interfaces,' *IEEE P1547/D7.3, December 2017*, pp. 1–148, 2017 (cited on page 2).

[11] V. F. Pires, A. Cordeiro, C. Roncero-Clemente, S. Rivera, and T. Dragičević, 'Dc–dc converters for bipolar microgrid voltage balancing: A comprehensive review of architectures and topologies,' *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 11, no. 1, pp. 981–998, 2023. DOI: 10.1109/JESTPE.2022.3208689 (cited on pages 2, 3).

[12] S. Rivera, R. Lizana F., S. Kouro, T. Dragičević, and B. Wu, 'Bipolar dc power conversion: State-of-the-art and emerging technologies,' *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 9, no. 2, pp. 1192–1204, 2021. DOI: 10.1109/JESTPE.2020.2980994 (cited on pages 2, 3).

[13] H. Kakigano, Y. Miura, and T. Ise, 'Low-voltage bipolar-type dc microgrid for super high quality distribution,' *IEEE Transactions on Power Electronics*, vol. 25, no. 12, pp. 3066–3075, 2010. DOI: 10.1109/TPEL.2010.2077682 (cited on pages 2, 3).

[14] T. Wang and A. Monti, 'Fault detection and isolation in dc microgrids based on singularity detection in the second derivative of local current measurement,' *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 3, pp. 2574–2588, 2021. DOI: 10.1109/JESTPE.2020.2976833 (cited on pages 2, 3).

[15] P. Prabhakaran and V. Agarwal, 'Novel four-port dc–dc converter for interfacing solar pv–fuel cell hybrid sources with low-voltage bipolar dc microgrids,' *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 2, pp. 1330–1340, 2020. DOI: 10.1109/JESTPE.2018.2885613 (cited on pages 2, 3).

[16] F. Wang, Z. Lei, X. Xu, and X. Shu, 'Topology deduction and analysis of voltage balancers for dc microgrid,' *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 2, pp. 672–680, 2017. DOI: 10.1109/JESTPE.2016.2638959 (cited on pages 2, 3).

[17] J.-O. Lee, Y.-S. Kim, and S.-I. Moon, 'Current injection power flow analysis and optimal generation dispatch for bipolar dc microgrids,' *IEEE Transactions on Smart Grid*, vol. 12, no. 3, pp. 1918–1928, 2021. DOI: 10.1109/TSG.2020.3046733 (cited on pages 2, 3).

[18] N. Bayati, H. R. Baghaee, A. Hajizadeh, and M. Soltani, 'Localized protection of radial dc microgrids with high penetration of constant power loads,' *IEEE Systems Journal*, vol. 15, no. 3, pp. 4145–4156, 2021. DOI: 10.1109/JSYST.2020.2998059 (cited on page 3).

[19] R. Asad and A. Kazemi, 'A novel distributed optimal power sharing method for radial dc microgrids with different distributed energy sources,' *Energy*, vol. 72, pp. 291–299, 2014. DOI: https://doi.org/10.1016/j.energy.2014.05.036 (cited on page 3).

[20] R. Mohanty and A. K. Pradhan, 'Protection of smart dc microgrid with ring configuration using parameter estimation approach,' *IEEE Transactions on Smart Grid*, vol. 9, no. 6, pp. 6328–6337, 2018. DOI: 10.1109/TSG.2017.2708743 (cited on page 3).

[21] S. A. Wakode, A. A. Sheikh, R. R. Deshmukh, and M. S. Ballal, 'Oscillation frequency based protection scheme for ring type dc microgrid,' in *2020 IEEE International Conference on Power Electronics, Smart Grid and Renewable Energy (PESGRE2020)*, 2020, pp. 1–5. DOI: 10.1109/PESGRE45664.2020.9070592 (cited on page 3).

[22] C. Chakraborty, H. Ho-Ching Iu, and D. Dah-Chuan Lu, 'Power converters, control, and energy management for distributed generation,' *IEEE Transactions on Industrial Electronics*, vol. 62, no. 7, pp. 4466–4470, 2015. DOI: 10.1109/TIE.2015.2412914 (cited on page 3).

[23] G.-Y. Lee, B.-S. Ko, J.-S. Lee, and R.-Y. Kim, 'An off-line design methodology of droop control for multiple bi-directional distributed energy resources based on voltage sensitivity analysis in dc microgrids,' *International Journal of Electrical Power and Energy Systems*, vol. 118, p. 105754, 2020. DOI: https://doi.org/10.1016/j.ijepes.2019.105754 (cited on page 3).

[24] E. L. Carvalho, A. Blinov, A. Chub, P. Emiliani, G. de Carne, and D. Vinnikov, 'Grid integration of dc buildings: Standards, requirements and power converter topologies,' *IEEE OJ. Power Electron.*, vol. 3, pp. 798–823, 2022. DOI: 10.1109/OJPEL.2022.3217741 (cited on pages 4, 5).

[25] LVDC, 'Electricity for the 21st century,' *IEC Technology Report, International Electrotechnical Commission, Geneva, Switzerland*, 2017. DOI: https://www.iec.ch/basecamp/lvdc-electricity-21st-century (cited on page 4).

[26] 'Ieee guide for batteries for uninterruptible power supply systems,' *IEEE Std 1184-2022 (Revision of IEEE Std 1184-2006)*, pp. 1–110, 2022. DOI: 10.1109/IEEESTD.2022.9774336 (cited on page 4).

[27] IEC, 'Iec tr 63282:2024 — low voltage direct current (lvdc) systems – assessment of standard voltages and power quality requirements,' *International Electrotechnical Commission (IEC)*, 2024, Available from the IEC Webstore (cited on page 4).

[28] 'Ieee standard for trip systems for low-voltage (1000 v and below) ac and general purpose (1500 v and below) dc power circuit breakers,' *IEEE Std C37.17-2022 (Revision of IEEE Std C37.17-2012)*, pp. 1–31, 2023. DOI: 10.1109/IEEESTD.2023.10045639 (cited on page 4).

[29] 'Ieee recommended practice for the design and application of power electronics in electrical power systems,' *IEEE Std 1662-2016 (Revision of IEEE Std 1662-2008)*, pp. 1–68, 2017. DOI: 10.1109/IEEESTD.2017.7874058 (cited on page 6).

[30] S. Sarani, H. Abootorabi Zarchi, and H. Delavaripour, 'Ripple-free input current flyback converter using a simple passive circuit,' *IEEE Transactions on Industrial Electronics*, vol. 69, no. 3, pp. 2557–2564, 2022. DOI: 10.1109/TIE.2021.3065624 (cited on page 7).

[31] J. Rodríguez, J. R. García-Meré, D. G. Lamar, M. M. Hernando, and J. Sebastián, 'High step-down isolated pwm dc–dc converter based on combining a forward converter with the series-capacitor structure,' *IEEE Access*, vol. 11, pp. 131 045–131 063, 2023. DOI: 10.1109/ACCESS.2023.3334794 (cited on page 7).

[32] R. R. Khorasani, E. Adib, and H. Farzanehfard, 'Zvt resonant core reset forward converter with a simple auxiliary circuit,' *IEEE Transactions on Industrial Electronics*, vol. 65, no. 1, pp. 242–250, 2018. DOI: 10.1109/TIE.2017.2716871 (cited on page 7).

[33] R. Mayer, L. S. de Oliveira, M. B. E. Kattel, L. C. Gili, and S. V. G. Oliveira, 'An interleaved forward/flyback dc–dc converter with bidirectional capability and wide voltage range characteristic,' *IEEE Transactions on Power Electronics*, vol. 40, no. 8, pp. 11 051–11 063, 2025. DOI: 10.1109/TPEL.2025.3553280 (cited on page 8).

[34] H. Tarzamni, E. Babaei, F. P. Esmaeelnia, P. Dehghanian, S. Tohidi, and M. B. B. Sharifian, 'Analysis and reliability evaluation of a high step-up soft switching push–pull dc–dc converter,' *IEEE Transactions on Reliability*, vol. 69, no. 4, pp. 1376–1386, 2020. DOI: 10.1109/TR.2019.2945413 (cited on page 8).

[35] P. Xuewei and A. K. Rathore, 'Naturally clamped zero-current commutated soft-switching current-fed push–pull dc/dc converter: Analysis, design, and experimental results,' *IEEE Transactions on Power Electronics*, vol. 30, no. 3, pp. 1318–1327, 2015. DOI: 10.1109/TPEL.2014.2315834 (cited on page 8).

[36] S. Bal, A. K. Rathore, and D. Srinivasan, 'Naturally clamped snubberless soft-switching bidirectional current-fed three-phase push–pull dc/dc converter for dc microgrid application,' *IEEE Transactions on Industry Applications*, vol. 52, no. 2, pp. 1577–1587, 2016. DOI: 10.1109/TIA.2015.2487444 (cited on page 8).

[37] N. Arish, M. Ardestani, and V. Teymoori, 'Comparison of dual stator consequent-pole linear permanent magnet vernier machine with toroidal and concentrated winding,' in *2020 11th Power Electronics, Drive Systems, and Technologies Conference (PEDSTC)*, 2020, pp. 1–5. DOI: 10.1109/PEDSTC49159.2020.9088384 (cited on page 8).

[38] E. Şehirli, 'Analysis of lcl filter topologies for dc-dc isolated cuk converter at ccm operation,' *IEEE Access*, vol. 10, pp. 113 741–113 755, 2022. DOI: 10.1109/ACCESS.2022.3218162 (cited on page 9).

[39] A. Alfares, B. Lehman, and M. Amirabadi, 'A ćuk-based modular dc–dc converter for medium voltage direct current (mvdc) applications,' *IEEE Open Journal of Power Electronics*, vol. 3, pp. 560–573, 2022. DOI: 10.1109/OJPEL.2022.3197545 (cited on page 9).

[40] G. A. Mudiyanselage, N. Keshmiri, and A. Emadi, 'A review of dc-dc resonant converter topologies and control techniques for electric vehicle applications,' *IEEE Open Journal of Power Electronics*, vol. 4, pp. 945–964, 2023. DOI: 10.1109/OJPEL.2023.3331180 (cited on page 10).

[41] J. Wu, K. Wang, Y. Yang, and W. Wu, 'A synchronous rectification method of cllc converters based on inner phase-shift modulation under light load conditions,' in *2024 IEEE 10th International Power Electronics and Motion Control Conference (IPEMC2024-ECCE Asia)*, 2024, pp. 988–993. DOI: 10.1109/IPEMC-ECCEAsia60879.2024.10567084 (cited on page 10).

[42] R. De Doncker, D. Divan, and M. Kheraluwala, 'A three-phase soft-switched high-power-density dc/dc converter for high-power applications,' *IEEE Trans. Ind. Appl.*, vol. 27, no. 1, pp. 63–73, 1991. DOI: 10.1109/28.67533 (cited on page 10).

[43] B. Zhao, Q. Song, W. Liu, and Y. Sun, 'Overview of dual-active-bridge isolated bidirectional dc–dc converter for high-frequency-link power-conversion system,' *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4091–4106, Aug. 2014. DOI: 10.1109/TPEL.2013.2289913 (cited on pages 10, 17).

[44] H. Bai and C. Mi, 'Eliminate reactive power and increase system efficiency of isolated bidirectional dual-active-bridge dc–dc converters using novel dual-phase-shift control,' *IEEE Transactions on Power Electronics*, vol. 23, no. 6, pp. 2905–2914, 2008. DOI: 10.1109/TPEL.2008.2005103 (cited on page 10).

[45] L. K. Pittala, R. Barbone, R. Mandrioli, V. Cirimele, M. Ricco, and G. Grandi, 'Insights on dab converter with auxiliary inductors,' in *Proc. Int. Conf. on Clean Electrical Power (ICCEP)*, 2023, pp. 458–463. DOI: 10.1109/ICCEP57914.2023.10247489 (cited on pages 11, 34, 38).

[46] A. Rodríguez, A. A. Gómez, M. M. Hernando, D. G. Lamar, and J. Sebastián, 'A dynamic study of the single active bridge converter,' *IEEE Transactions on Power Electronics*, vol. 40, no. 4, pp. 4805–4817, 2025. DOI: 10.1109/TPEL.2024.3426590 (cited on page 11).

[47] K. Wang, J. Xu, K. Xu, M. Huang, Z. Yao, and W. Wu, 'Hybrid resonant dc-dc converters for dc transformers in dc distribution networks with limited reverse power flow range,' *IEEE Access*, pp. 1–1, 2025. DOI: 10.1109/ACCESS.2025.3611385 (cited on page 11).

[48] C. Fan, K. Wang, S. Wu, Y. Yang, J. Li, and W. Wu, 'Analysis of switching characterization and power loss of bidirectional asymmetrical power flow dc/dc converters,' in *2024 IEEE 10th International Power Electronics and Motion Control Conference (IPEMC2024-ECCE Asia)*, 2024, pp. 1000–1005. DOI: 10.1109/IPEMC-ECCEAsia60879.2024.10567097 (cited on page 11).

[49] K. Wang, S. Wu, C. Fan, C. Yang, W. Wu, and M. Liserre, 'Peak current reduction of bidirectional-asymmetrical-power-flow dc-dc converters for low-penetration-renewable-energy power distribution networks,' *IEEE Jr. Emerg. Sel. Top. Power Electron.*, vol. 12, no. 5, pp. 4342–4351, 2024. DOI: 10.1109/JESTPE.2024.3406574 (cited on pages 11, 40).

[50] S. Tian, F. C. Lee, and Q. Li, 'A simplified equivalent circuit model of series resonant converter,' *IEEE Transactions on Power Electronics*, vol. 31, no. 5, pp. 3922–3931, 2016. DOI: 10.1109/TPEL.2015.2464351 (cited on page 12).

[51] J. Liang, L. Wang, J. Liang, M. Fu, T. Long, and H. Wang, 'A switched-capacitor and series-resonant hybrid mhz dcx in data center applications,' *IEEE Transactions on Power Electronics*, vol. 39, no. 10, pp. 13 389–13 400, 2024. DOI: 10.1109/TPEL.2024.3422672 (cited on page 12).

[52] F. Flores-Bahamonde, H. Renaudineau, A. M. Llor, A. Chub, and S. Kouro, 'The dc transformer power electronic building block: Powering next-generation converter design,' *IEEE Ind. Electron. Mag.*, vol. 17, no. 1, pp. 21–35, 2023. DOI: 10.1109/MIE.2022.3147168 (cited on pages 12, 72, 87).

[53] S. Cuoghi, R. Mandrioli, L. K. Pittala, V. Cirimele, and M. Ricco, 'Dual-active-bridge model and control for supporting fast synthetic inertial action,' *Energies*, vol. 15, no. 6, Mar. 2022. DOI: 10.3390/en15062295 (cited on page 15).

[54] Y. Yan, H. Gui, and H. Bai, 'Complete zvs analysis in dual active bridge,' *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1247–1252, Feb. 2021. DOI: 10.1109/TPEL.2020.3011470 (cited on page 15).

[55] J. Riedel, D. G. Holmes, B. P. McGrath, and C. Teixeira, 'Maintaining continuous zvs operation of a dual active bridge by reduced coupling transformers,' *IEEE Trans. Ind. Electron.*, vol. 65, no. 12, pp. 9438–9448, Dec. 2018. DOI: 10.1109/TIE.2018.2815993 (cited on page 16).

[56] S. Yin, S. Debnath, R. Wojda, P. Marthi, and M. Saeedifard, 'Impact of the transformer magnetizing inductance on the performance of the dual-active bridge converter,' in *Proc. IEEE 22nd Workshop Control Model. Power Electron.*, Nov. 2021, pp. 1–7. DOI: 10.1109/COMPEL52922.2021.9645978 (cited on page 16).

[57] X. Chen, G. Xu, H. Han, D. Liu, Y. Sun, and M. Su, 'Light-load efficiency enhancement of high-frequency dual-active-bridge converter under sps control,' *IEEE Trans. Ind. Electron.*, vol. 68, no. 12, pp. 12 941–12 946, Dec. 2021. DOI: 10.1109/TIE.2020.3044803 (cited on pages 16, 22).

[58] M. Kheraluwala, R. Gascoigne, D. Divan, and E. Baumann, 'Performance characterization of a high-power dual active bridge dc-to-dc converter,' *IEEE Trans. Ind. Appl.*, vol. 28, no. 6, pp. 1294–1301, Dec. 1992. DOI: 10.1109/28.175280 (cited on page 16).

[59] G. Xu, L. Li, X. Chen, W. Xiong, X. Liang, and M. Su, 'Decoupled eps control utilizing magnetizing current to achieve full load range zvs for dual active bridge converters,' *IEEE Trans. Ind. Electron.*, vol. 69, no. 5, pp. 4801–4813, May 2022. DOI: 10.1109/TIE.2021.3078351 (cited on page 16).

[60] Z. Guo and D. Sha, 'Dual-active-bridge converter with parallel-connected full bridges in low-voltage side for zvs by using auxiliary coupling inductor,' *IEEE Trans. Ind. Electron.*, vol. 66, no. 9, pp. 6856–6866, Sep. 2019. DOI: 10.1109/TIE.2018.2877145 (cited on page 16).

[61] K. Kojima, Y. Tsuruta, and A. Kawamura, 'Proposal of dual active bridge converter with auxiliary circuit for multiple pulse width modulation,' in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2016, pp. 1–8. DOI: 10.1109/ECCE.2016.7855367 (cited on pages 16, 25, 26).

[62] H. Higa and J.-i. Itoh, 'Extension of zero-voltage-switching range in dual active bridge converter by switched auxiliary inductance,' in *Proc. IEEE Energy Convers. Congr. Expo.*, Oct. 2017, pp. 5324–5331. DOI: 10.1109/ECCE.2017.8096893 (cited on pages 16, 25).

[63] R. Mandrioli, M. Ricco, G. Grandi, T. A. Pereira, and M. Liserre, 'Dab-based common-mode injection in three-phase four-wire inverters,' in *Proc. IEEE Int. Conf. Compat., Power Electron. Power Eng.*, Jul. 2022, pp. 1–6. DOI: 10.1109/CPE-POWERENG54966.2022.9880870 (cited on page 16).

[64] A. Rodríguez, A. Vázquez, D. G. Lamar, M. M. Hernando, and J. Sebastián, 'Different purpose design strategies and techniques to improve the performance of a dual active bridge with phase-shift control,' *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 790–804, Feb. 2015. DOI: 10.1109/TPEL.2014.2309853 (cited on page 18).

[65] S. Shao, H. Chen, X. Wu, J. Zhang, and K. Sheng, 'Circulating current and zvs-on of a dual active bridge dc-dc converter: A review,' *IEEE Access*, vol. 7, pp. 50 561–50 572, Apr. 2019. DOI: 10.1109/ACCESS.2019.2911009 (cited on page 19).

[66] J. W. Kolar, F. Krismer, Y. Lobsiger, J. Muhlethaler, T. Nussbaumer, and J. Minibock, 'Extreme efficiency power electronics,' in *Proc. 7th Int. Conf. Integrat. Power Electron. Sys. (CIPS)*, 2012, pp. 1–22 (cited on pages 29, 95).

[67] E. L. Carvalho, A. Blinov, A. Sidorova, A. Chub, and D. Vinnikov, 'Evaluation of dual-active bridge converter for dc energy buildings,' in *2023 IEEE 17th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG)*, 2023, pp. 1–6. DOI: 10.1109/CPE-POWERENG58103.2023.10227460 (cited on page 30).

[68] E. L. Carvalho, R. Mandrioli, L. K. Pittala, I. Bianchini, A. Blinov, A. Chub, and D. Vinnikov, 'Universal interlinking converter for prosumer dc buildings: Operation under normal and abnormal ac grid conditions,' in *2025 IEEE Seventh International Conference on DC Microgrids (ICDCM)*, 2025, pp. 1–5. DOI: 10.1109/ICDCM63994.2025.11144697 (cited on page 30).

[69] E. L. Carvalho, R. Mandrioli, L. K. Pittala, A. Blinov, A. Chub, and D. Vinnikov, 'Universal interlinking converter for prosumer dc buildings: Operation with different dc grid types,' in *2025 IEEE Seventh International Conference on DC Microgrids (ICDCM)*, 2025, pp. 1–6. DOI: 10.1109/ICDCM63994.2025.11144648 (cited on pages 30, 38).

[70] F. Peng, H. Li, G.-J. Su, and J. Lawler, 'A new zvs bidirectional dc-dc converter for fuel cell and battery application,' *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 54–65, 2004. DOI: 10.1109/TPEL.2003.820550 (cited on page 30).

[71] Y. Shi, R. Li, Y. Xue, and H. Li, 'Optimized operation of current-fed dual active bridge dc–dc converter for pv applications,' *IEEE Trans. Ind. Electron.*, vol. 62, no. 11, pp. 6986–6995, 2015. DOI: 10.1109/TIE.2015.2432093 (cited on page 30).

[72] Q. Gu, B. Xie, R. Li, Z. Zhu, and Y. Zhang, 'A zvs implementation method of a current-fed dual active bridge converter within the full load range,' in *Proc. IEEE Appl. Power Electron. Conf. Exp. (APEC)*, 2024, pp. 2059–2062. DOI: 10.1109/APEC48139.2024.10509164 (cited on page 30).

[73] G. Xu, M. Zhang, X. Chen, L. Li, Z. Lu, and M. Su, 'Dual-coupled-inductor-based dab dcx converter with full load range zvs,' *IEEE Trans. Ind. Electron.*, vol. 72, no. 1, pp. 525–535, 2025. DOI: 10.1109/TIE.2024.3406878 (cited on page 30).

[74] D. Sha, X. Wang, and D. Chen, 'High-efficiency current-fed dual active bridge dc–dc converter with zvs achievement throughout full range of load using optimized switching patterns,' *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1347–1357, 2018. DOI: 10.1109/TPEL.2017.2675945 (cited on page 30).

[75] L. K. Pittala, E. L. Carvalho, M. Ricco, G. Orfanoudakis, A. Kuperman, and R. Mandrioli, 'Zvs analysis of an interleaved current-fed dab for bipolar and unipolar dc grids,' in *Proc. IEEE Fourth Int. Conf. on Power Electron. Smart Grid and Ren. En. (PESGRE)*, 2025 (cited on page 38).

[76] G. De Carne, G. Buticchi, Z. Zou, and M. Liserre, 'Reverse power flow control in a st-fed distribution grid,' *Tran. Smart Grid*, vol. 9, no. 4, pp. 3811–3819, 2018. DOI: 10.1109/TSG.2017.2651147 (cited on page 39).

[77] V. N. Ferreira, N. Vazquez, B. Cardoso, and M. Liserre, 'Hybrid multiple-active bridge for unequal power flow in smart transformers,' in *Proc. En. Con. Cong. Expo. (ECCE)*, 2019, pp. 5016–5021. DOI: 10.1109/ECCE.2019.8913049 (cited on page 39).

[78] R. Zhu, F. Hoffmann, N. Vázquez, K. Wang, and M. Liserre, 'Asymmetrical bidirectional dc–dc converter with limited reverse power rating in smart transformer,' *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 6895–6905, 2020. DOI: 10.1109/TPEL.2019.2957407 (cited on pages 39, 40, 43).

[79] R. Zhang, Y. Lin, P. Zheng, J. Xue, F. Chi, R. Deng, D. Wen, and Z. Zou, 'Hybrid dc transformers and its active control method for dc power grids in low-carbon ports,' in *Proc. Int. Conf. Power En. Tech. (ICPET)*, 2024, pp. 287–292. DOI: 10.1109/ICPET62369.2024.10941071 (cited on page 40).

[80] N. L. Hinov and T. H. Hranov, 'Tolerance analysis of common transistor dc-dc converters,' in *Proceedings of 25th International Conference Electronics*, 2021, pp. 1–6. DOI: 10.1109/IEEECONF52705.2021.9467442 (cited on page 40).

[81] M. Rimondi, R. Mandrioli, V. Cirimele, L. K. Pittala, M. Ricco, and G. Grandi, 'Design of an integrated, six-phase, interleaved, synchronous dc/dc boost converter on a fuel-cell-powered sport catamaran,' *Designs*, vol. 6, no. 6, 2022. DOI: 10.3390/designs6060113 (cited on page 40).

[82] A. Cirillo, N. Femia, and G. Spagnuolo, 'An interval mathematics approach to tolerance analysis of switching converters,' in *Proceedings of 27th Annual IEEE Power Electronics Specialists Conference*, vol. 2, 1996, 1349–1355 vol.2. DOI: 10.1109/PESC.1996.548757 (cited on page 40).

[83] N. Hinov, T. Hranov, and V. Dimitrov, 'Tolerance analysis of resonant converters with parallel loaded capacitor,' in *Proceedings of XXIX International Scientific Conference Electronics (ET)*, 2020, pp. 1–5. DOI: 10.1109/ET50336.2020.9238188 (cited on page 40).

[84] B. M. H. Jassim, D. J. Atkinson, and B. Zahawi, 'Modular current sharing control scheme for parallel-connected converters,' *IEEE Transactions on Industrial Electronics*, vol. 62, no. 2, pp. 887–897, 2015. DOI: 10.1109/TIE.2014.2355813 (cited on page 40).

[85] K. Ma, M. Liserre, F. Blaabjerg, and T. Kerekes, 'Thermal loading and lifetime estimation for power device considering mission profiles in wind power converter,' *IEEE Transactions on Power Electronics*, vol. 30, no. 2, pp. 590–602, 2015. DOI: 10.1109/TPEL.2014.2312335 (cited on page 40).

[86] A. Diet, N. Couellan, X. Gendre, J. Martin, and J.-P. Navarro, 'A statistical approach for tolerancing from design stage to measurements analysis,' *Procedia CIRP*, vol. 92, pp. 33–38, 2020, 16th CIRP Conference on Computer Aided Tolerancing (CIRP CAT 2020). DOI: https://doi.org/10.1016/j.procir.2020.05.171 (cited on page 40).

[87] L. K. Pittala, R. Barbone, R. Mandrioli, V. Cirimele, and M. Ricco, 'Impact of magnetics tolerance on the power sharing of parallel dual-output phase-shift full-bridge converters,' in *PCIM Europe 2024; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2024, pp. 2571–2577. DOI: 10.30420/566262360 (cited on pages 40, 58, 60, 70).

[88] L. K. Pittala, J. Geng, S. Baldisserri, R. Mandrioli, M. Ricco, and G. Grandi, 'Software-based power sharing control in parallel dual-output phase-shift full-bridge converters,' in *2024 IEEE 18th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG)*, 2024, pp. 1–6. DOI: 10.1109/CPE-POWERENG60842.2024.10604390 (cited on pages 40, 52, 70).

[89] L. K. Pittala, M. Ricco, A. Chub, M. Sitbon, A. Kuperman, and R. Mandrioli, 'Active power sharing control in asymmetrical bidirectional dc/dc for smart transformers,' in *2025 IEEE Seventh International Conference on DC Microgrids (ICDCM)*, 2025, pp. 1–5. DOI: 10.1109/ICDCM63994.2025.11144708 (cited on pages 40, 70).

[90] L. K. Pittala, A. Chub, G. I. Orfanoudakis, A. Kuperman, M. Ricco, and R. Mandrioli, 'Active power sharing control in asymmetrical bidirectional dc/dc converter,' *IEEE Open Journal of Power Electronics*, vol. 6, pp. 1980–1990, 2025. DOI: 10.1109/OJPEL.2025.3630546 (cited on pages 40, 70).

[91] V. Cirimele, *et al.*, 'Uncertainty quantification for sae j2954 compliant static wireless charge components,' *IEEE Access*, vol. 8, pp. 171 489–171 501, 2020. DOI: 10.1109/ACCESS.2020.3025052 (cited on page 45).

[92] A. G. Glen, L. M. Leemis, and J. H. Drew, 'Computing the distribution of the product of two continuous random variables,' *Computational Statistics & Data Analysis*, vol. 44, no. 3, pp. 451–464, 2004. DOI: https://doi.org/10.1016/S0167-9473(02)00234-7 (cited on page 46).

[93] M. Linford, 'The gaussian-lorentzian sum, product, and convolution (voigt) functions used in peak fitting xps narrow scans, and an introduction to the impulse function.,' *Vacuum Technology and Coating*, Jul. 2014. DOI: 10.1016/j.apsusc.2018.03.190 (cited on page 47).

[94] J. E. Marengo, D. L. Farnsworth, and L. Stefanic, 'A geometric derivation of the irwin-hall distribution,' *Int. J. Math. Math. Sci.*, vol. 2017, 3571419:1–3571419:6, 2017. DOI: 10.1155/2017/3571419 (cited on page 48).

[95] S. Okutani, P.-Y. Huang, R. Nishiyama, and Y. Kado, 'Analysis and comparison of series resonant converter with embedded filters for high power density dcx of solid-state transformer,' *IEEE Access*, vol. 10, pp. 7716–7733, 2022. DOI: 10.1109/ACCESS.2022.3142028 (cited on pages 71, 72).

[96] D. Neumayr, M. Vöhringer, N. Chrysogelos, G. Deboy, and J. W. Kolar, 'P^3dct—partial-power pre-regulated dc transformer,' *IEEE Transactions on Power Electronics*, vol. 34, no. 7, pp. 6036–6047, 2019. DOI: 10.1109/TPEL.2018.2879064 (cited on pages 72, 75).

[97] S. Dalapati, S. Ray, S. Chaudhuri, and C. Chakraborty, 'Control of a series resonant converter by pulse density modulation,' in *Proceedings of the IEEE INDICON 2004. First India Annual Conference, 2004.*, 2004, pp. 601–604. DOI: 10.1109/INDICO.2004.1497831 (cited on pages 72, 75).

[98] B. Boser and B. Wooley, 'The design of sigma-delta modulation analog-to-digital converters,' *IEEE Journal of Solid-State Circuits*, vol. 23, no. 6, pp. 1298–1308, 1988. DOI: 10.1109/4.90025 (cited on page 72).

[99] C. H. Bae, J. Ryu, and K. W. Lee, 'Suppression of harmonic spikes in switching converter output using dithered sigma-delta modulation,' *IEEE Transactions on Industry Applications*, vol. 38, no. 1, pp. 159–166, 2002. DOI: 10.1109/28.980370 (cited on page 72).

[100] E. Dallago and G. Sassone, 'Advances in high-frequency power conversion by delta-sigma modulation,' *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 44, no. 8, pp. 712–721, 1997. DOI: 10.1109/81.611267 (cited on page 72).

[101] A. Chub, D. Zinchenko, D. Vinnikov, and A. Blinov, 'Three-port flyback converter for photovoltaic module integration in bipolar dc microgrids,' in *2020 IEEE International Conference on Industrial Technology (ICIT)*, 2020, pp. 909–914. DOI: 10.1109/ICIT45562.2020.9067237 (cited on page 72).

[102] D. Lumbreras, J. Zaragoza, M. Lamich, N. Berbel, and E. Romero-Cadaval, 'A novel three-dimensional sigma–delta modulation for high-switching-frequency three-phase four-wire active power filters,' *Electronics*, vol. 13, no. 3, 2024. DOI: 10.3390/electronics13030553 (cited on page 72).

[103] R. Ayyanar, R. Giri, and N. Mohan, 'Active input-voltage and load-current sharing in input-series and output-parallel connected modular dc-dc converters using dynamic input-voltage reference scheme,' *IEEE Trans. Power Electron.*, vol. 19, no. 6, pp. 1462–1473, 2004. DOI: 10.1109/TPEL.2004.836671 (cited on pages 72, 87).

[104] S. Okutani, P.-Y. Huang, R. Nishiyama, and Y. Kado, 'Series resonant converter with embedded filters for dcx of solid-state transformer,' in *IECON 2021 – 47th Annual Conference of the IEEE Industrial Electronics Society*, 2021, pp. 1–7. DOI: 10.1109/IECON48115.2021.9589304 (cited on page 73).

[105] R. Steigerwald, 'A comparison of half-bridge resonant converter topologies,' *IEEE Transactions on Power Electronics*, vol. 3, no. 2, pp. 174–182, 1988. DOI: 10.1109/63.4347 (cited on page 73).

[106] M. Fu, C. Fei, Y. Yang, Q. Li, and F. C. Lee, 'Optimal design of planar magnetic components for a two-stage gan-based dc–dc converter,' *IEEE Transactions on Power Electronics*, vol. 34, no. 4, pp. 3329–3338, 2019. DOI: 10.1109/TPEL.2018.2849741 (cited on page 75).

[107] Y. Jia, H. Wu, Y. Zhang, Y. Liu, and Y. Xing, 'Single-phase ac–dc converter with dual-output rectifier, dual-input dc transformer, and voltage-split/sigma principle,' *IEEE Transactions on Power Electronics*, vol. 35, no. 1, pp. 158–168, 2020. DOI: 10.1109/TPEL.2019.2914507 (cited on page 75).

[108] X. Zhou, J. Xu, S. Zhong, and Y.-F. Liu, 'Soft switching symmetric bipolar outputs dc-transformer (dcx) for eliminating power supply pumping of half-bridge class-d audio amplifier,' *IEEE Transactions on Power Electronics*, vol. 34, no. 7, pp. 6440–6455, 2019. DOI: 10.1109/TPEL.2018.2873234 (cited on page 75).

[109] J. Huang and X. Zhang, 'Three-step switching frequency selection criteria for symmetrical cllc-type dc transformer in hybrid ac/dc microgrid,' *IEEE Transactions on Power Electronics*, vol. 34, no. 10, pp. 9379–9385, 2019. DOI: 10.1109/TPEL.2019.2904045 (cited on page 75).

[110] T. Liu, X. Wu, and S. Yang, '1 mhz 48–12 v regulated dcx with single transformer,' *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 1, pp. 38–47, 2021. DOI: 10.1109/JESTPE.2019.2955607 (cited on page 75).

[111] B. Wang, X. Xin, S. Wu, H. Wu, and J. Ying, 'Analysis and implementation of llc burst mode for light load efficiency improvement,' in *2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition*, 2009, pp. 58–64. DOI: 10.1109/APEC.2009.4802633 (cited on pages 76–78).

[112] R. Karimi, E. Adib, and H. Farzanehfard, 'Resonance based zero-voltage zero-current switching full bridge converter,' *IET Power Electronics*, vol. 7, no. 7, pp. 1685–1690, 2014. DOI: https://doi.org/10.1049/iet-pel.2013.0301 (cited on page 76).

[113] W. Feng, F. C. Lee, P. Mattavelli, D. Huang, and C. Prasantanakorn, 'Llc resonant converter burst mode control with constant burst time and optimal switching pattern,' in *2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2011, pp. 6–12. DOI: 10.1109/APEC.2011.5744568 (cited on pages 77, 78).

[114] C.-S. Yeh, C.-W. Chen, M. Lee, and J.-S. Lai, 'A hybrid modulation method for single-stage soft-switching inverter based on series resonant converter,' *IEEE Transactions on Power Electronics*, vol. 35, no. 6, pp. 5785–5796, 2020. DOI: 10.1109/TPEL.2019.2948122 (cited on pages 77, 78).

[115] V. Sidorov, A. Chub, and D. Vinnikov, 'Implementation of burst control based on sigma-delta modulation in low-cost microcontroller,' in *2022 IEEE 23rd Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2022, pp. 1–6. DOI: 10.1109/COMPEL53829.2022.9830023 (cited on pages 80, 84).

[116] J. E. Huber, J. Miniböck, and J. W. Kolar, 'Generic derivation of dynamic model for half-cycle dcm series resonant converters,' *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 4–7, 2018. DOI: 10.1109/TPEL.2017.2703300 (cited on pages 83, 88).

[117] A. Chub, D. Vinnikov, and J.-S. Lai, 'Input voltage range extension methods in the series-resonant dc-dc converters,' in *2019 IEEE 15th Brazilian Power Electronics Conference and 5th IEEE Southern Power Electronics Conference (COBEP/SPEC)*, 2019, pp. 1–6. DOI: 10.1109/COBEP/SPEC44138.2019.9065291 (cited on pages 83, 85).

[118] D. Vinnikov, A. Chub, E. Liivik, and I. Roasto, 'High-performance quasi-z-source series resonant dc–dc converter for photovoltaic module-level power electronics applications,' *IEEE Transactions on Power Electronics*, vol. 32, no. 5, pp. 3634–3650, 2017. DOI: 10.1109/TPEL.2016.2591726 (cited on page 83).

[119] A. Campanini, M. Simonazzi, M. Bosi, and C. Rossi, 'Design and comparison between psfb and llc 400/48v dc/dc stage for on-board battery charger during total and partial cc-cv charging cycles,' in *2022 IEEE 21st Mediterranean Electrotechnical Conference (MELECON)*, 2022, pp. 1102–1106. DOI: 10.1109/MELECON53508.2022.9842914 (cited on page 83).

[120] R. Pillon Barcelos and D. Dujic, 'Parallel operation of direct current transformers,' in *Proc. Int. Exh. Conf. Power Electron., In. Motion, Ren. Ener. Ener. Manage.*, 2023, pp. 1–10. DOI: 10.30420/566091010 (cited on page 88).

[121] Y. Cao, K. Ngo, and D. Dong, 'Resonant commutation electronic-embedded dc transformer (rc-eet dcx) with quasi-trapezoidal current and natural current sharing,' *IEEE Trans. Power Electron.*, vol. 39, no. 8, pp. 9736–9751, 2024. DOI: 10.1109/TPEL.2024.3400606 (cited on page 88).

[122] Y. Cao, K. D. T. Ngo, and D. Dong, 'Hybrid electronic-embedded transformer-based dc transformer (eet-dcx): A new family of soft-switching dcxs,' *IEEE Trans. Power Electron.*, vol. 39, no. 8, pp. 9661–9679, 2024. DOI: 10.1109/TPEL.2024.3392579 (cited on page 88).

[123] R. Wei, X. Wu, R. Liu, L. Ding, W. Li, and Y. R. Li, 'An input-series-output-parallel connected four-switch buck-boost-integrated cllc dc transformer with bidirectional natural power-sharing property,' in *Proc. IEEE Ener. Conv. Cong. Exp. (ECCE)*, 2023, pp. 3224–3229. DOI: 10.1109/ECCE53617.2023.10361979 (cited on page 88).

[124] X. Chen, G. Xu, S. Xie, H. Han, M. Su, Y. Sun, H. Wang, Y. Liu, and W. Xiong, 'A natural bidirectional input-series–output-parallel llc-dcx converter with automatic power sharing and power limitation capability for li-ion battery formation and grading system,' *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 8, no. 4, pp. 3618–3632, 2020. DOI: 10.1109/JESTPE.2019.2941583 (cited on page 88).

[125] H. Wang, Y. Chen, Y. Qiu, P. Fang, Y. Zhang, L. Wang, Y.-F. Liu, J. Afsharian, and Z. Yang, 'Common capacitor multiphase llc converter with passive current sharing ability,' *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 370–387, 2018. DOI: 10.1109/TPEL.2017.2661066 (cited on page 88).

[126] H. Wang, Y. Chen, Y.-F. Liu, J. Afsharian, and Z. Yang, 'A passive current sharing method with common inductor multiphase llc resonant converter,' *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 6994–7010, 2017. DOI: 10.1109/TPEL.2016.2626312 (cited on page 88).

[127] L. K. Pittala, A. Chub, V. Sidorov, S. Khan, M. Ricco, and R. Mandrioli, 'Cycle-skipping technique based on sigma-delta modulation in series resonant dc transformer,' in *2025 IEEE Seventh International Conference on DC Microgrids (ICDCM)*, 2025, pp. 1–5. DOI: 10.1109/ICDCM63994.2025.11144699 (cited on page 96).

[128] L. K. Pittala, A. Chub, V. Sidorov, S. Khan, M. Ricco, and R. Mandrioli, 'Cycle-skipping technique based on sigma-delta modulation for power regulation in modular src-dcx,' *IEEE Open Journal of Power Electronics*, pp. 1–9, 2026. DOI: 10.1109/OJPEL.2026.3655068 (cited on page 96).

Nomenclature

ΔV	Voltage ripple.
$\hat{i}_{\mathrm{L}}$	Inductor ripple component in the DAB.
$\mathcal{N}$	Power PDF.
ω_0	Resonant frequency.
$\overline{P}_2, \overline{P}_3$	Averaged active- and diode-bridge power.
c	Diode-bridge turn-on delay parameter.
D	Pulse Density.
d	Phase-shift.
$i_1', i_{2\mathrm{u}}, i_{2\mathrm{l}}, i_{3\mathrm{u}}, i_{3\mathrm{l}}$	Leakage and coupling inductance currents.
i_{L}	Transformer leakage inductance in the DAB.
k	Coupling inductance ratio.
k_p	Power sharing ratio.
L_1	Leakage inductance in the AB-DC/DC converter.
L_1, L_2	Interphase inductors in the CF-DAB.
L_m	Magnetizing inductance.
$L_{2\mathrm{u}}, L_{2\mathrm{l}}, L_{3\mathrm{u}}, L_{3\mathrm{l}}$	Coupling inductance in AB-DC/DC converter.
L_{eq}, L_{12}	Equivalent and active-bridge inductance.
n	Transformer turns ratio in all converters.
P_2, P_3	Active- and diode-bridge power in passive power sharing control.
$P_{2,\mathrm{CCM}}, P_{3,\mathrm{CCM}}$	Active- and diode-bridge power in active power sharing control under CCM.
$P_{2,\mathrm{DCM}}, P_{3,\mathrm{DCM}}$	Active- and diode-bridge power in active power sharing control under DCM.
$P_{2,\mathrm{h1}}, P_{3,\mathrm{h1}}$	Active- and diode-bridge power in active power sharing control under hybrid 1.
$P_{2,\mathrm{h2}}, P_{3,\mathrm{h2}}$	Active- and diode-bridge power in active power sharing control under hybrid 2.
P_{o}	Total output power.
R_{ac}	Equivalent AC resistance of SRC.
R_{L}	Load resistance of SRC.
R_{sw}	Switch current RMS in the DAB.
S_{x}	MOSFETs in all converters, where $x \in 1, 2, 3, \ldots$.
$T_{\mathrm{sw}}, f_{\mathrm{sw}}$	Switching period and frequency.
$V_{\mathrm{dc}}, V_{\mathrm{o}}$	Input and output voltage.