ALMA MATER STUDIORUM
UNIVERSITÀ DI BOLOGNA

DOTTORATO DI RICERCA IN

INGEGNERIA ELETTRONICA, TELECOMUNICAZIONI E TECNOLOGIE DELL'INFORMAZIONE

Ciclo 37

Settore Concorsuale: 09/E3 - ELETTRONICA

Settore Scientifico Disciplinare: ING-INF/01 - ELETTRONICA

EFFICIENT SOLUTIONS FOR GAN POWER AMPLIFIERS

Presentata da: Simone Cangini

Coordinatore Dottorato

Davide Dardari

Supervisore

Alberto Santarelli

Co-supervisore

Corrado Florian

Esame finale anno 2025

Borsa di dottorato del Programma Operativo Nazionale Ricerca e Innovazione 2014-2020 (CCI 2014IT16M2OP005), risorse FSE REACT-EU, Azione IV.4 “Dottorati e contratti di ricerca su tematiche dell’innovazione” e Azione IV.5 “Dottorati su tematiche Green.” CUP J35F21003160006

Abstract

Over the past decade, wireless applications have grown exponentially, driven by demand across sectors like cellular networks, vehicular communication, and industrial systems. The affordability of sensors and improvements in energy efficiency have fueled the deployment of billions of connected devices. At the same time, the rise of smartphones and wireless internet has created challenges for higher data rates and broader coverage. The transition from 4G to 5G technology has addressed these needs, with 5G offering enhanced reliability, low latency, and cost-effective solutions. The introduction of millimeter-wave frequencies is mandatory to achieve the gigabit-level wireless traffic required. However, mm-wave signal attenuation requires increased power amplification, which adds to network power consumption.

RF power amplifiers (PAs), essential for boosting signals, face challenges with high peak-to-average-power-ratio (PAPR) signals common in modulated transmissions used to maximize spectral efficiency. This issue is particularly critical for 6G technology, which demands extreme linearity, power efficiency, and thermal management to operate in terahertz (THz) bands and deliver speeds up to 1 Tbps. New semiconductor technologies are expected to address these challenges, particularly Gallium Nitride (GaN), which offers an overall high power density, particularly promising when high integration is of interest. In combination with that, the ability to dynamically adjust the power amplifier performances or the possibility to let the PA operate at multiple bands is desirable for modern standards. Many topologies and clever solutions already address this objective but when more bandwidth or higher frequencies are employed, more challenges prevent these solutions from breaking through the market.

This Thesis addresses these challenges by investigating two key areas to improve the efficiency of GaN PAs. First, it delves into the impact of trapping effects, which can significantly degrade device performance, particularly with modern high-modulation schemes. A new characterization technique is developed, based on drain current transient (DCT) measurements, to assess figures of merit such as gate and drain lag, trap activation energy, cross-section, and carrier density reduction. This approach reduces

characterization time while providing valuable insights into the relationship between the physical structure of HEMTs and their susceptibility to trapping effects. This allows for more informed decisions when selecting GaN devices for specific applications.

The second area of focus is the integration of varactor devices into the output matching network of PAs to achieve reconfigurable amplifier architectures. To fulfill this goal, a preliminary characterization is required before new devices can be adopted. This study is conducted over existing diodes in GaN-on-SiC technology to assess the use of integrated solutions instead of discrete ones to reduce the impact of parasitics. After this preliminary research, the extraction of suitable models to allow CAD simulations is required. A novel automatic modeling procedure, employing vector network measurements, is developed to accurately characterize and model varactor device behavior. This procedure generates a lumped-element circuit representation, facilitating the simulation and optimization of the matching network for improved PA efficiency and adaptability. A matching network integrating varactors is also proposed and a preliminary evaluation of PAs with modified varactor devices is presented.

Acknowledgments

Pursuing my Ph.D. was a challenging yet profoundly enriching experience.

I had the opportunity to engage with many individuals who provided both professional guidance and meaningful conversations. Real gratitude goes to Prof. Alberto Santarelli and Prof. Corrado Florian for their patient supervision and constant motivation. Beyond the scientific advice, their support in navigating bureaucratic and financial matters was crucial throughout the entire period. I would also like to thank Prof. King and Prof. Martín-Guerrero for their valuable comments and feedback, which were instrumental in improving this thesis.

The Electronic Design and Measurement for RF and Industrial Applications (EDM) research group has been a great source of inspiration during my Ph.D., particularly thanks to the dedicated colleagues I had the pleasure of working with. I would like to mention Gian Piero and Alberto, who served as diligent and competent day-to-day mentors. Their experience and practical advice were essential in steering my work in the right direction. Other people were part of the everyday coffee-time, Maurizio, Rudi, Alessio and Alessandro, with a special mention to Mattia and Irene for making everyday moments more enjoyable with casual-talks and jokes.

Through my tutoring experience, I had the pleasure of meeting many students who, in turn, helped shape me both professionally and personally.

Collaborating with leading institutions in the microwave field was equally rewarding, offering valuable insight into the broader research and industry ecosystem. My time with the Ferdinand-Braun-Institut (FBH) in Berlin, Germany, and the Microwave Electronics for Communications (MEC) group in Bologna, Italy, led to productive collaborations and meaningful scientific growth. I am thankful to all colleagues from Berlin-Olof, Alessandro, and Domenico-as well as Francesco and Andrea from MEC.

A special mention goes to my family and my girlfriend, Francesca, for their constant support throughout this journey. Their patience, encouragement, and understanding, especially during the most intense periods, were paramount for achieving this goal.

Contents

List of Figures

List of Tables

Acronyms

5G Fifth Generation Mobile Communications Standard

CAD Circuit Aided Design

CMOS Complementary Metal-Oxide Semiconductor

CW Continuous Wave

DCT Drain Current Transients

GaN Gallium nitride

HEMT High Electron Mobility Transistor

IMN Input matching network

IoT Internet of Things

LTE Long Term Evolution

MEMS Microelectromechanical Systems

MIM Metal Insulator Metal

MMIC Microwave monolithic integrated circuit

MN Matching Network

MOS Metal Oxide Semiconductor

NVNA Nonlinear Vector Network Analyzer

OMN Output Matching Network

PA Power amplifier

PAE Power Added Efficiency

PDK product design kit

PIV Pulsed IV

RF Radio-frequency

SOLT Short Open Load Thru

TR Tuning Range

VNA Vector Network Analyzer

Chapter 1

Introduction

1.1 Telecommunication industry and technologies

1.1.1 Telecommunication trends

Over the last ten years, wireless applications have witnessed exponential growth due to increasing demand across various sectors such as cellular networks, vehicular communication, and industrial systems. Advances in semiconductor technology facilitate new paradigms that were unimaginable a few decades ago. These cutting-edge technologies have seamlessly integrated into daily life, proving their utility in diverse domains. For instance, the Internet of Things (IoT) has gained momentum in areas like agriculture, environmental monitoring, and smart metering, where it now plays a critical role [5]. The driving forces behind this widespread adoption are the affordability of connected sensors and consistent improvements in energy efficiency. These developments have enabled the deployment of many battery-powered, cable-free devices. Current estimates suggest that tens of billions of devices [6] are now connected to the network, prompting IoT standards to evolve to handle the increasing density of wireless connections. Simultaneously, the proliferation of smartphones and wireless internet connectivity has introduced new challenges. These include the need for higher data rates and better network coverage, both in rural areas and densely populated urban centers. The fourth-generation (4G) system, also known as Long-Term Evolution (LTE), has been the dominant standard for telecom data and voice traffic. By 2022, 4G surpassed the older third-generation (3G) standard, leading network operators to shut down 3G base stations in favor of the more advanced fifth-generation (5G) technology. 5G has now become a well-established commercial solution for wireless communication, designed to meet the diverse and demanding requirements of mod-

ern applications. These requirements include reliability, mobility, low latency, and cost-effectiveness. The versatility and superior performance of 5G are achieved by leveraging various advanced radio frequency (RF) techniques. These include Time Division Duplex (TDD) and Frequency Division Duplex (FDD), which were already employed in LTE, alongside a more sophisticated Orthogonal Frequency Division Multiplexing (OFDM) modulation scheme. Furthermore, novel approaches like Generalized Frequency Division Multiplexing (GFDM) [7] and Filtered-Orthogonal Frequency Division Multiplexing (f-OFDM) [8] have been explored to enhance spectral efficiency. These techniques reduce out-of-band emissions, thereby increasing the overall power spectral density and ensuring that 5G can meet the challenges of modern wireless communication.

5G network architecture relies on the deployment of femtocells, a new network structure scheme that makes use of multiple smaller base stations to address frequency reuse and denser layouts [9, 10]. These cells integrate massive MIMO antennas operating at millimeter-wave frequencies [11] to be able to deliver gigabit-level wireless traffic. The new frequency range 2 (FR2) makes available K- and Ka-bands for telecommunication with the advantage of more link capacity but lower range coverage, due to the degradation of millimeter-wave (mm-wave) signals with the propagation distance. To be able to maintain the same LTE signal strength, the transmitting power of the base station must be increased and multiplied for all concurrent amplifiers, which could be up to 64 [12]. This power consumption cannot be easily tolerated without adopting smart resource allocation based on network requirements and scheduling algorithms [9].

An important slice of the 5G network power consumption is drained by the RF power amplifiers driving the antennas. RF power amplifiers (PA) are vital components of telecommunication infrastructures, with the role of boosting signals to the levels needed for efficient long-distance transmission while maintaining signal quality and minimizing power losses. While the trend of the number of possible applications is increasing, the frequency bands available for new standards struggle to grow at the same rate. It is then of main importance to exploit at best the reserved bandwidth. In order to address these requirements, modulated signals are widely adopted for increasing data rates while exploiting the same spectral occupation. This usually comes with the generation of signals with high peak-to-average-power-ratio (PAPR), creating challenges for PAs. This is especially true with new sixth-generation (6G) technology that requires very advanced linearity performances to fulfill the requirements [13]. Looking at the future of telecommunication, the next 6G is expected to operate in the terahertz (THz) frequency bands and deliver speeds of up to 1 Tbps with ultra-low

latency. The shift to such high frequencies will demand unprecedented power efficiency, thermal management, and robustness from PAs to ensure reliable performance. New semiconductors aim to address the new requirements as will be explored in Sec. 1.1.2 and 1.1.3.

1.1.2 Semicondutor technologies for telecommunication

When looking at the state-of-the-art, several semiconductor technologies are available for the design and fabrication of telecommunication PAs and indeed the first step when target performances are provided is the technology selection. The output power required from the overall amplifier and the operation frequency are the two main drivers for the selection of the best solution optimizing the tradeoff between performances and costs. For low frequency applications, well-established technologies like CMOS and LDMOS offer good solutions and allow for low production costs and overall reliability [14]. On the other side, when high output power is required and the operation frequency enters the mm-wave domain, III-V semiconductors are usually adopted, as could be seen in Fig. 1.1 [1], thanks to the intrinsic advantages of the technology. From the late 20th century, Silicon Germanium (SiGe) became the most promising solution for telecommunication, offering the required processing maturity and yield, which makes it comparable with conventional Si solutions [15]. Gallium arsenide (GaAs) rapidly dominated the RF PA scenario because of its higher cut-off frequencies than silicon due to its high low-field mobility.

While the designers exploit all the performances of GaAs technology, the research industry started to look at Gallium Nitride (GaN) compound that theoretically can offer game-changing performances. Despite the promising results, the high production costs, due to a generally low yield, and the reliability problems arising with this new fabrication process, led to late optimization for the high-frequency operation and, instead, the high-power applications were privileged [16]. This is reasonable when considering that a PA operating at mm-wave frequencies needs a well-predictable manufacturing process, and large areas could be required to also implement all the passive structures, hence further reducing the yield of the process. In order to fully assess the advantages of GaN semiconductor and the current technological challenges, a deep analysis of the stack layer is presented in the following section.

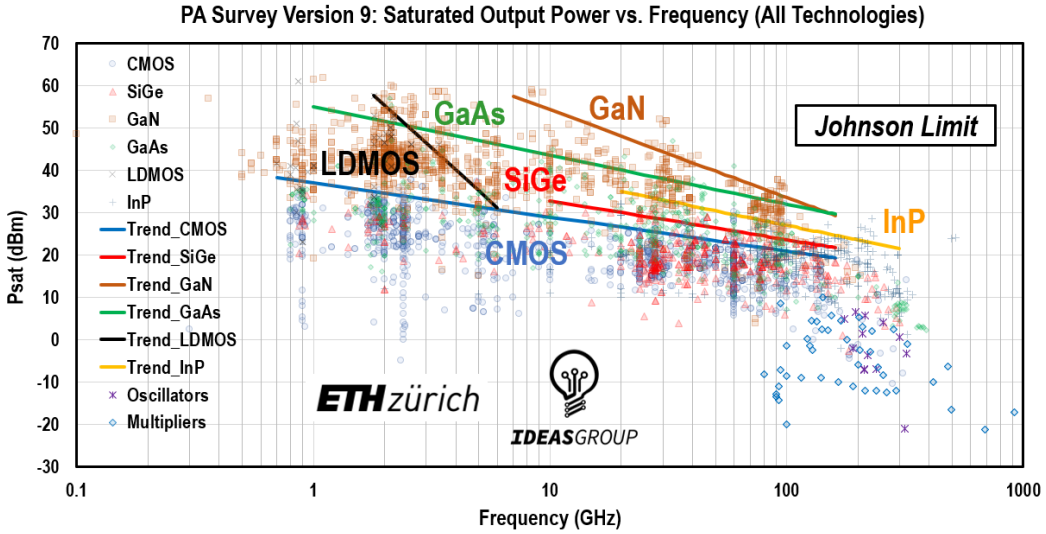

Figure 1.1: Survey of published works on PA per operational frequency and saturated power [1].

1.1.3 GaN technology

Many design strategies are investigated to improve the performance of GaN devices for specific applications. While GaN-on-Si vertical devices are widely adopted for low-frequency power applications, lateral heterojunction field-effect transistors (HFETs), also known as high electron mobility transistors (HEMTs), are usually adopted for high-frequency applications. The advantage of this structure lies in a reduced distance between drain and source contacts, lowering the resistance that electrons must counteract. The principal feature of this structure is the AlGaN/GaN heterojunction that creates a thin layer of electrons known as "two-dimensional electron gas" (2DEG). This layer is created as a result of the different crystal polarities, namely spontaneous and piezoelectric polarizations, and creates a conductive path between drain and source even when no voltage is applied to the device. Spontaneous polarization originates from the difference in the electronegativity of the group III and V elements, which creates polar Ga-N bonds. Piezoelectric polarization shows its impact by applying a stress to the material that, for the HEMT case, comes from the contact of two layers (AlGaN and GaN layers) with different lattice constants. Devices with this property are usually denoted as normally-ON devices because the HEMT is fully conductive when no bias is applied to the gate port. Therefore, no doping is required to create a fully functional device with this structure, and the threshold voltage (V_{th}) is only dictated by material properties.

The 2DEG electron density could be actively controlled by the gate terminal that

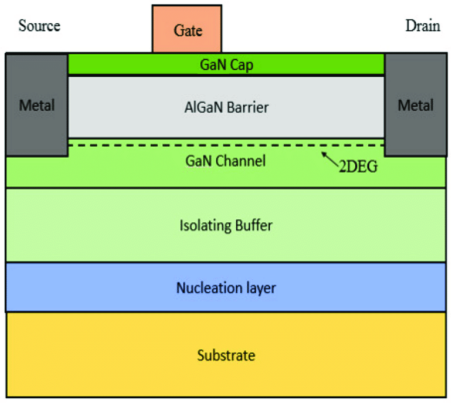

Figure 1.2: Cross section of common GaN HEMT.

acts like a Schottky junction. Applying a negative voltage with respect to source potential causes the electrons at the GaN-AlGaN interface to deplete, reducing the carrier concentration and hence the device conductivity. A thin cap layer, usually realized in silicon-nitride (SiN), could be added on top of AlGaN barrier to help reducing current collapse [17] and gate leakage current and avoiding the oxidation of the AlGaN, despite slightly reducing the 2DEG concentration.

A common layer stack for GaN HEMTs is depicted in Fig. 1.2, and a detailed description of layers is provided below.

Substrate

The substrate is the structural element of the whole chip, accommodating all layers composing the final device. In addition to physical strength properties, Traditionally, silicon (Si) is used as the main substrate material due to its low production costs while its physical strength allows the realization of wafers with a diameter of up to 200 mm. Despite these advantages, Si is not the preferred choice for GaN technology. Since the GaN layer should be deposited on top of the substrate to realize the HEMT channel, the lattice mismatch plays an important role. The difference in lattice constants of Si and GaN forces the latter to break the regular structure and adapt to the material below. Defects originating from this physical adaptation may induce vertical (drain to substrate) breakdown and reliability degradation. Moreover, Si has poor thermal performance, being a limitation for the high power density that GaN solutions address.

One no-brainer solution is to fabricate the entire wafer in GaN so that no defects are expected when the buffer layer is grown. Moreover, GaN material also offers good thermal conductivity, as expected from the substrate. Unfortunately, this alternative turns out to be prohibitively high in realization costs, and its physical properties are

not as good as the Si counterpart, as far as robustness is concerned. In order to obtain a compromise between the two alternatives, different materials are proposed, like sapphire, silicon carbide (SiC), and Al_2O_3. In particular, SiC offers a very low lattice mismatch compared to that of GaN and a reasonably low thermal mismatch, with a thermal conductivity higher than that of both GaN and Si substrates. Even if the realization cost is fairly high, it is a common adoption from foundries offering GaN-on-SiC technologies.

Buffer

The buffer layer is of great importance in reducing the number of physical defects in the GaN channel layer that affect the 2DEG conduction. Electrical properties are also affected, as the buffer should isolate the channel from the underlying substrate, preventing substrate current leakages and improving the off-state breakdown voltage [18]. It has been demonstrated that current-collapse effects can occur when hot-carriers are injected into the buffer and then trapped by the lower layers [19].

Intentionally introducing defects in the buffer helps improve its performance, particularly at RF frequencies. The undoped GaN deposited for the channel creation typically exhibits unintentional n-type doping characteristics, probably due to the deposition process and the influence of impurities like Si and oxygen (O) [20]. To compensate for this effect, acceptor-doping impurities like carbon (C) [21] or iron (Fe) could be used, demonstrating improvements in buffer charge confinement but worsening the trapping effects exhibited [22].

In addition to doping compensation, other strategies can be employed to enhance carrier confinement, like the introduction of buffer layers of different composition. One of these approaches consist in the introduction of an AlGaN back-barrier layer on top of the substrate. The additional potential barrier created helps to confine the 2DEG carriers [23], avoiding the need for a doped GaN buffer. Substantial improvements are observed at RF with this additional layer [24] despite other properties could be penalized, like thermal dissipation [25].

1.2 Radio-frequency power amplifiers

1.2.1 Overview

Since the introduction of the 4G standard, reconfigurable PAs have become key components of wireless front-ends. This reconfigurability was initially intended as

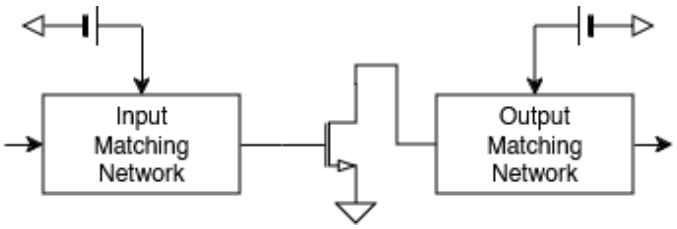

Figure 1.3: Schematic representation of a RF PA.

the ability to adapt the operative frequency of the amplifier, enabling the support of a variety of global services with multiple band licenses. Due to the required performance of the 4G standard, the ability to adapt the bandwidth of the amplifier in addition to the operational frequency was desirable. The number of available bands in the LTE technology makes it impossible to include many RF front-ends, each one devoted to a single carrier. Since designing wide-band circuits is increasingly hard as the frequency becomes higher [26], the inclusion of reconfigurable elements in the PA design is mandatory.

The typical block structure of an RF PA is reported in Fig. 1.3. The active element in the center is the main enabler of the overall structure, dictating the maximum performance we could expect from the amplifier and the technology to be used for the fabrication. The IMN and OMN blocks serve to adapt the input and output impedance, respectively, to the optimal impedance of the active element. In order to extract the values of those optimal impedances, measurements tailored to the specific selected device should be conducted. This is usually performed by the manufacturer, which provides a PDK that can be imported into the design software. If those data are not available, load- and source-pull setups can be exploited for the complete characterization [27].

The input and output matching networks usually contain a combination of passive elements, like resistors, capacitors, inductors, or microstrip lines, as well as active elements such as diodes or switches to achieve the required impedance adaptation. These last are exploited to achieve reconfigurable capabilities employing an external control signal (either current or voltage) directly affecting the circuit. In the next Section the topic of reconfigurable PAs is addressed, while in Sec. 1.2.3 state-of-the-art strategies to enhance the amplifier efficiency are presented.

1.2.2 Reconfigurable PAs

Reconfigurability for power amplifiers can be achieved in different ways, depending on the target application. Multiband operation is widely adopted in telecommuni-

cations and refers to the ability to operate at multiple central frequencies [28] in a non-concurrent manner, reducing the number of distinct amplifier circuits required to cover all operative bands. Since the number of transmitting elements is usually kept low due to space constraints and a single transmitting antenna is adopted, this solution allows for a reduction in the size of the switching matrix required for all amplifiers to operate on a single output connection. Although clever solutions can be adopted to achieve multiband operation [29], active elements are typically required to obtain the desired behavior.

In this context, many passive elements in the matching networks-such as resistors or inductors-are targeted for replacement in favor of reconfigurable implementations [30], exploiting the active elements available in the same technology. In this way, all PA components can be integrated on the same chip, reducing parasitics, which are particularly impactful at high frequencies. This approach is not always straightforward, as the selected technology may not support these circuit elements, or they may not be accurately modeled. In [31], RF diodes are integrated into the originally static output matching network to selectively include or exclude discrete components such as capacitors or resistors. Switches derived from transistor topologies can also be used to selectively isolate sections of the matching network, as seen in switched-capacitor topologies [32].

Frequently, difficulties in integrating diodes or switches in PAs arise from poor isolation or conduction performance, due to trade-offs made during the design phase. In particular, when the device is expected to be fully conductive, the lowest possible parasitic resistance is required, leading to design optimizations such as maximizing the number of fingers. Conversely, when the device is deactivated, it should behave as transparently as possible, approximating an open circuit. This requirement often leads to minimal device sizing to reduce leakage currents that would otherwise degrade performance. The insertion loss of the device should be critically evaluated, as it must remain controlled during both on- and off-states.

Reconfigurability in MIMO applications is essential, as the ability to control the beam steering of an antenna array is of increasing interest in telecommunications. Circuits such as phase shifters are extensively adopted in MIMO systems, where the phase of the input signal must be accurately controlled across the transmitting antennas. Reconfigurable phase shifters [33] can then be integrated before the PAs and controlled by an external signal to properly steer the transmitted beam.

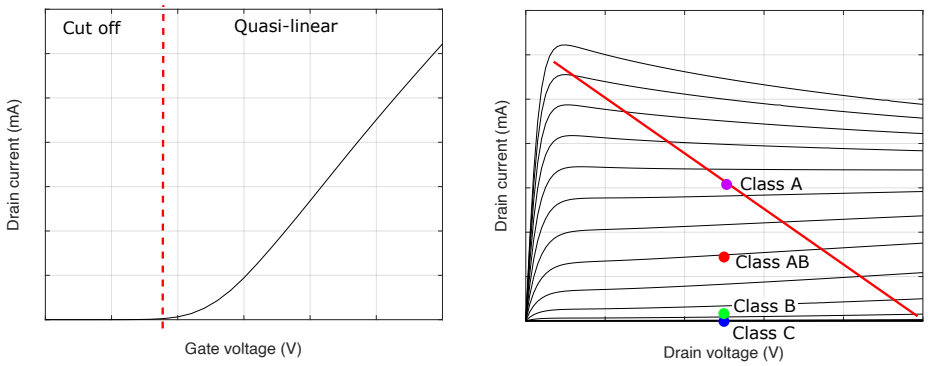

Figure 1.4: Visual representation of bias points for class A, B, AB.

1.2.3 High-efficiency PAs

In the last section, the reconfigurability of PAs is analyzed with the advantage of reducing the space occupation of the transmitter front-end when multiple bands should be supported. In addition to this aspect, the optimization of the amplifier efficiency should also be considered. Similarly to the results drawn in Sec. 1.1 for the network infrastructure, also in hand-held devices, the RF transmitter stage is the main energy-consuming element. Moreover, all the power not employed in wireless communication is converted to heat that needs to be extracted from the chip, usually drying out more space from the device.

Classical MMIC PA designs focus on achieving the best power-added efficiency (PAE) at the peak of the output power that the amplifier should provide. While this reduces the power loss where the maximum consumption is expected, with modern signal modulations, the peak output power is rarely achieved. This is particularly true when the amplifier is operated in class A, B, or AB. In these modes, the bias point provided to the amplifiers goes in the direction of achieving high linearity performances, penalizing the power efficiency. As visible in Fig. 1.4, class A bias point is selected in order to have a current conduction angle of $\theta = 2\pi$, therefore producing the maximum output voltage-current swing. In contrast, class B operation moves the bias point at a lower current, corresponding to a current conduction angle of $\theta = \pi$, slightly reducing linearity performances but with substantial power reduction. The ideal efficiencies expected from the two topologies are 50% and 78.5% for classes A and B, respectively, which are insufficient for modern PAs.

Several advancements have been made in PA technology to address these challenges, usually involving additional hardware to adapt the power amplifier to the input signal, dynamically changing its configuration. Among these, innovations in circuit design, such as Doherty amplifiers [34], Envelope Tracking [35], and Outphasing techniques,

have been explored to enhance the efficiency and linearity of RF PAs under dynamic operating conditions, usually linked to the instantaneous power of the input signal. Two techniques, in particular, are the object of study in this thesis; therefore, a detailed analysis is provided below.

Load modulation

At its core, load modulation refers to the dynamic variation of the load impedance seen by a power amplifier as a function of its output power or signal characteristics. In traditional fixed-load power amplifiers, the impedance of the load remains constant, tuned for delivering the optimal performance at the highest output power. While this approach simplifies design, it often results in inefficiencies, especially for signals with high peak-to-average power ratios (PAPR). For instance, when the output power is low, the load impedance can be increased, reducing the current through the device and thereby minimizing power dissipation. Conversely, at higher output powers, the impedance is lowered to allow maximum power transfer while maintaining efficiency. This adaptability enhances overall efficiency across the amplifier's operational range.

One of the most prominent implementations of load modulation is the Doherty power amplifier, originally presented in [36], which employs multiple active devices to modulate the load impedance. In a Doherty architecture, a main amplifier operates continuously, while one or more auxiliary amplifiers activate only at higher power levels. The interaction between these amplifiers adjusts the effective load impedance seen by the main amplifier, allowing efficient operation across a wide dynamic range.

Other techniques, such as outphasing PA [37] split the input signal in two paths, each one with its own amplifier, and exploit the phase difference of the output current of the two amplifiers. The combination of the two impacts the load exhibited to the two amplifiers, adapting the loadline to the desired output power. Despite outphasing PAs demonstrate better performances than Doherty counterparts, many implementation drawbacks prevent the diffusion of these solutions in wireless systems. Wide input signal bandwidth are required, necessitating wideband amplifiers for the two stages, and the mismatches on the circuit layout could impact heavily on the losses, particularly on the output combiner.

Supply modulation

Traditional PA design methodologies focus on impedance matching at the maximum power the amplifier can provide, targeting the worst-case scenario the amplifier might face. On one hand, this helps to limit the heat generated when maximum current

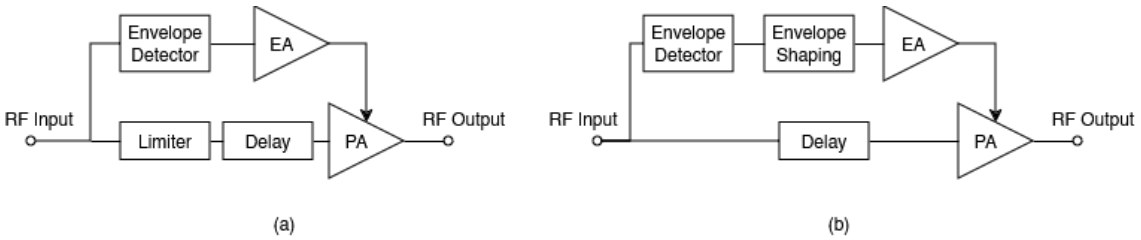

Figure 1.5: (a) Block diagram of EER amplifier; (b) block diagram of ET amplifier.

is drawn, but on the other, it reduces efficiency when lower power levels are required. Adaptively changing the power supply-thus limiting the maximum power the amplifier can deliver-improves performance, especially when modulated signals are involved. Two architectures are known to achieve this goal, namely Envelope Elimination and Restoration (EER) [38] and Envelope Tracking (ET). Both designs make use of two amplifiers, one of which feeds the supply input of the other.

In EER systems, the input signal is split into two separate paths: one carrying the phase information with a constant envelope, and the other containing only the amplitude (envelope) information [Fig. 1.5.(a)]. This separation allows the amplification process to be optimized for efficiency. The phase-modulated path is handled by a highly efficient non-linear power amplifier, such as a Class D or Class E amplifier, which excels at amplifying constant-envelope signals. Meanwhile, the envelope path is processed by a second amplifier, known as the supply modulator, which modulates the supply voltage or bias of the main amplifier. This process reintroduces the original amplitude variations into the amplified signal. While EER provides significant efficiency benefits, particularly at high output power levels, it does come with challenges. One major issue arises at low RF output power, where the envelope amplifier (EA) can suffer from reduced efficiency, depending on the specific implementation. EA performance is further constrained by the need for high switching frequencies and strict linearity requirements, as it must accurately reproduce the signal envelope. As signal bandwidth increases, the output filter design becomes more complex, often requiring higher-order filters that are sensitive to variations in load impedance. Moreover, the constant-envelope phase-modulated RF signal can exhibit a bandwidth up to ten times greater than that of the original input signal, demanding the main amplifier to operate at significantly higher performance levels. To mitigate these issues, the EA can be combined with a linear amplifier, which enhances low-power performance at the cost of increased complexity and reduced overall efficiency. Alternatively, hybrid operating modes have been developed in which the EER amplifier operates in its standard configuration for high-power signals but switches to linear behavior at low envelope lev-

els [39]. Digital control solutions for the EA have also been introduced [40], improving efficiency by dynamically adjusting the amplifier's operation. However, these digital approaches increase system complexity, requiring more silicon area and high-speed control circuitry. Additionally, the increased complexity can degrade synchronization between the EA and the main amplifier, introducing distortion in the output signal. This balance between efficiency, complexity, and performance highlights the trade-offs inherent in EER designs, particularly as modern communication systems demand higher bandwidths and more stringent performance requirements.

In ET architectures, the supply voltage of the main amplifier is dynamically adapted according to the instantaneous power of the input RF signal (Fig. 1.5(b)). For this technique, the main amplifier typically operates in linear classes, such as Class AB or Class B, in order to preserve the required linearity performance. The supply voltage is continuously adjusted following the envelope of the input signal, allowing the main amplifier to operate closer to its saturation region, thereby improving overall efficiency while maintaining acceptable linearity. Unlike EER, where the envelope and phase components of the signal are separated and handled by two different amplifier paths, ET maintains a single RF path and modulates only the supply voltage. This simplifies the signal reconstruction process and reduces the synchronization challenges commonly associated with EER.

Although ET introduces increased circuit complexity and design challenges, virtually all modern base stations implement power amplifiers composed of more than one basic amplifier [41]. In particular, ET is considered one of the most promising candidates due to its superior performance in covering large bandwidths, especially when compared to narrower-band solutions such as the Doherty amplifier. Moreover, ET proves advantageous in real-world scenarios where the output power can vary significantly over time, such as during different periods of the day.

1.3 Varactor devices

Variable capacitors, also referred to as varactors, represent a valuable choice for obtaining continuously tunable circuits to achieve PA adaptability. Varactors are designed to act as non-linear passive components used in replacement of fixed capacitors. They represent the main component in voltage-controlled oscillators (VCOs) [42] where an input voltage control is responsible for tuning the oscillator frequency. Other applications include patch antennas [43], filters [44] and phase-shifters [45].

Looking at the qualitative performance reported in Table 1.1, it is evident that

	Tunability	RF losses (Q)	Control voltage	Tuning speed	Power handling
GaAs	High	Moderate	< 20 V	Fast	Low
BST	Moderate	Moderate	10-20 V	Fast	High
MEMS	Low	Very good	50-100 V	Slow	High

Table 1.1: Qualitative performances for three varactor technologies.

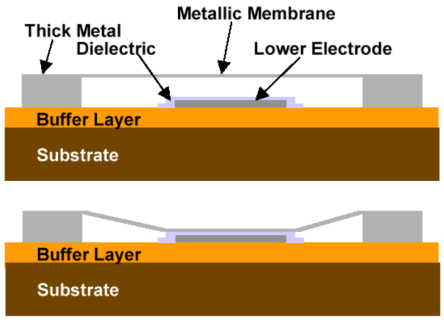

Figure 1.6: Cross-section representation of MEMS varactor from [2]. Two different states are highlighted, exhibiting different capacitance.

the best technology depends on the specific application. Among these technologies, MEMS [46] show promising results even at high frequencies. Their realization requires specialized techniques such as surface micromachining for the fabrication of thin, floating films capable of mechanical motion or actuation characteristics, as illustrated in Fig. 1.6 [2]. The microelectromechanical operation is used to adjust the position of the floating element, expressed as its distance from the substrate. This behavior results in a change in the capacitance exhibited between the device's ports, thus creating a varactor element. Due to the presence of mechanical parts, the dynamic response of the device, referred to as the switching time, can require several microseconds, which imposes limitations in applications requiring fast reconfiguration, such as those tracking the input signal envelope. Moreover, integration into MMIC designs is challenging for advanced technologies like GaN, necessitating the placement of the MEMS element outside of the RF circuit.

Other discrete solutions adopt Barium Strontium Titanate (BST) thin-film ferroelectrics [47], which offer low losses even at RF [48]. Depending on the fabrication process and material properties, the bias voltage required to control BST devices can reach up to 120 V [48], limiting their applicability in some target systems. The use of different electrode configurations has been reported to improve RF performance [49], with good results achieved at more manageable bias voltages around 30 V. However,

due to the materials and fabrication steps involved, these devices typically require a separate chip to be added to the amplifier [50], often using solder paste or gold wire bonding.

To design reconfigurable circuits operating in the mm-wave frequency range, integrating varactor devices becomes essential to minimize parasitic effects caused by bonding wires or packaging. Furthermore, as discussed in Sec. 1.1.2, it is preferable to implement these varactors using the same GaAs, GaN, or MOS technology as the rest of the circuit, ensuring seamless on-chip integration.

An MMIC varactor typically exploits a reverse-biased p-n junction, where the concentration of electrons and holes is modulated by the voltage difference across the N-type and P-type semiconductors. In this configuration, the capacitance of the depletion region, referred to as the junction capacitance C_j, dominates the overall device capacitance. The doping profiles of the N and P regions directly influence how C_j varies with the applied bias voltage. Abrupt junctions, while straightforward to fabricate, are less suitable for varactor applications because they do not provide an ideal relationship between capacitance and voltage. Instead, hyper-abrupt junctions are preferred, as they exhibit a more linear C-V characteristic and maintain this linearity across a wider voltage range. This reduces distortion under high-power operation, making them well-suited for demanding applications.

When scaling is considered, p-n junctions provide a reduced effect when the area is shrunk. Instead, metal-oxide-semiconductor (MOS) varactors can take advantage of the device scaling trend as the reduction of the oxide thickness reflects in an increased oxide capacitance [51]. MOS varactors operate by varying the gate voltage, which modulates the charge distribution in the semiconductor beneath the gate oxide [52]. This changes the depletion region width and, consequently, the capacitance. Despite many applications and optimization strategies being documented [53], the losses induced by the ohmic contacts and the resistance of the n-doped semiconductor are significant and pose limits on the addressable applications.

Schottky diodes appear to be among the most valuable solutions for high-performance applications. Devices realized with this technology can operate at higher frequencies and power levels, as the Schottky diode is a majority carrier device and, as such, provides increased performance compared to a conventional p-n junction. Moreover, their unipolar nature results in a negligible reverse recovery current during switching. The idea of using the Schottky junction for the realization of varactors is supported by its structural similarity to the GaN HEMT layer, where the gate contact effectively forms a Schottky junction.

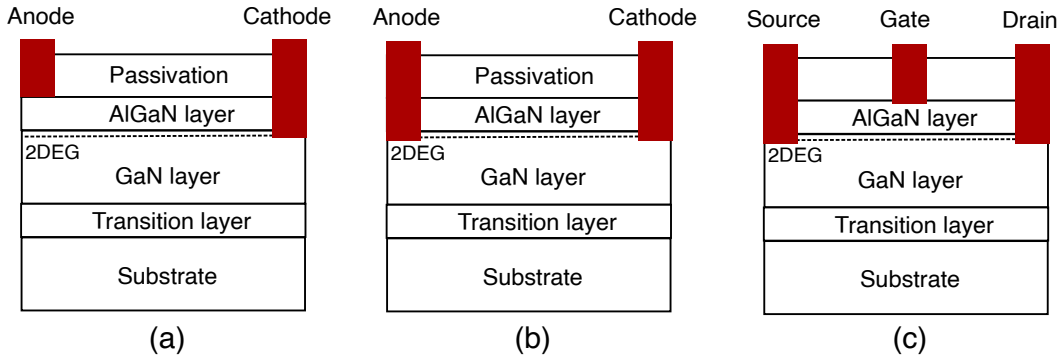

Figure 1.7: (a) Cross section of lateral Schottky diode; (b) lateral Schottky diode with recessed contact; (c) HEMT device exploited as Schottky diode.

In Fig. 1.7(a), the typical structure of a lateral AlGaN/GaN Schottky diode is shown. The cathode terminal is implemented as an ohmic contact, while the Schottky contact on the anode side enables the rectifying characteristics of the device. A forward bias voltage greater than the threshold, determined by the metal used and the device geometry, allows current to flow through the 2DEG channel to the cathode. A variation of this structure is illustrated in Fig. 1.7(b), known as the recessed diode. In this version, the AlGaN barrier is etched so that the anode metal is placed in direct contact with the 2DEG channel. This results in a lower turn-on voltage, reducing on-state losses, but also causes a higher leakage current in the off-state.

Fig. 1.7(c) presents a typical HEMT structure, which is very similar to that of Schottky diodes. The HEMT introduces a third metal contact-the gate-positioned over the 2DEG. This gate has the ability to control the charge density in the depletion region beneath it, thereby regulating the current flow through the device. As described in the previous section, the gate forms a Schottky junction, and if forward biased, current can flow from the gate to the source contact.

The influence of gate voltage on the 2DEG density can be exploited in the realization of a varactor device, commonly referred to as a high electron mobility varactor (HEMVAR) [54, 55, 3]. When the bias is above the pinch-off voltage, charges remain in the depletion region, and a high capacitance is observed. When a negative voltage is applied, the depletion region under the gate expands, reducing the charge density in the 2DEG and thus lowering the capacitance.

Following this concept, the gate metal can be replicated to form a combination of Schottky contacts, each exhibiting its own junction capacitance. This configuration is known as a metal-semiconductor-metal (MSM) varactor [56, 57].

1.4 On-wafer measurements

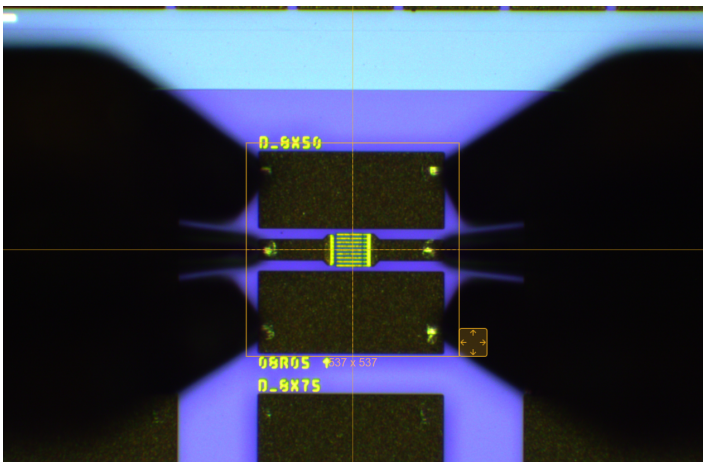

Figure 1.8: Microscope image of an MMIC diode with coplanar connections. The black shapes on both the left and right sides are ground-signal-ground (GSG) probes.

On-wafer measurements are a critical step in the characterization and validation of MMICs, offering a direct means to evaluate device performance without the interference of external packaging. These measurements enable testing as close as possible to the final device, eliminating parasitic effects introduced by elements such as bonding wires, which can significantly alter the behavior of high-frequency circuits. By directly probing the device on the wafer, it is possible to obtain a more accurate representation of the intrinsic performance of the MMIC, which is essential for both design validation and process development. Ground-signal-ground (GSG) probes are typically used, providing a matched 50 Ω condition up to the wafer surface. Figure 1.8 shows a typical MMIC device connected via two GSG probes. In the microscope image, the centrally located diode features coplanar connections that conveniently create a gold surface to accommodate the probes. The bright dots at the ends of the coplanar lines are the contact points of the probe tips. The distance between these contact points varies from 100 μm to 250 μm or more, depending on the selected probes, the minimum process clearance, and the required trace width. In this example, a pitch of 150 μm is used.

However, the precision of on-wafer measurements relies heavily on proper calibration of the probing system. Accurate calibration ensures the removal of systematic errors and parasitic contributions from the measurement setup, enabling the extraction of reliable data. Without meticulous calibration, the accuracy of the measurements can be compromised, potentially leading to incorrect conclusions about the device's capabilities. Multiple calibration methods are available to move the measurement reference plane up to the probe tips, including short-open-load-through (SOLT),

through-reflection-line (TRL), and other variations. All the measurement campaigns reported in this thesis make use of SOLT calibration due to the availability of standard substrates. Moreover, TRL calibration requires inclusion of the calibration structures on the same tile as the device under test and the use of the same RF pad geometries as the final structures. In some designs, space constraints make it impossible to accommodate such calibration patterns, but, depending on the layout of the structure, this is not always feasible. In contrast, SOLT calibration utilizes a dedicated calibration substrate that was readily available in the laboratory with the required frequency range capabilities.

In addition to proper calibration, de-embedding procedures play a crucial role in on-wafer measurements. During measurements, parasitics such as pad capacitances, resistances, and inductances associated with the probe-to-device interface can be observed. These parasitic effects are especially impactful in high-frequency applications, where even minor contributions can significantly affect performance metrics. Throughout this work, two main de-embedding techniques are adopted: one based on open-short structures [58, 59], and the other based on electromagnetic (EM) simulations.

The two-step open-short procedure extracts lumped components modeling the access structure that can then be removed with post-processing to obtain the intrinsic parameters. The fundamental assumption is that parallel parasitics originate from the signal pads while the interconnected lines have an influence on series parasitics. It is then required to have two separate structures devoted only to the procedure with the same structural properties as the ones adopted for the device. In Fig. 1.9(a), a coplanar structure for a 2-port diode is reported as an example. Access ports are located on the left and right side,s and the goal of the de-embedding is to move the calibrated reference plane from the contact points of the RF probes to the very end of the trans-

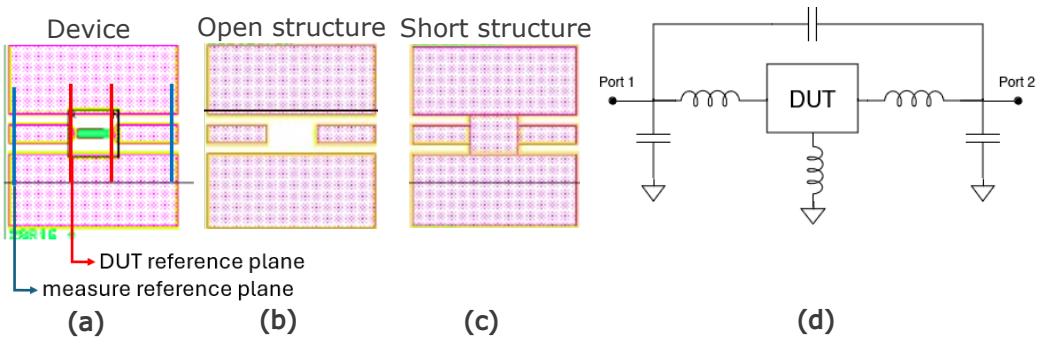

Figure 1.9: Structures for open-short de-embedding procedure. (a) Structure with device; (b) open structure; (c) short structure. (d) Parasitic elements extracted with the procedure.

mission lines. The open fixture in Fig. 1.9(b) is then derived from the device structure by removing the intrinsic device, therefore leaving an open space inside the structure while preserving the coplanar access. In contrast, the short fixture in Fig. 1.9(c) is realized by the introduction of a ground pad contacting the two signal lines. First, S-parameter measurements of the open fixture in Fig. 1.9(b) should be acquired and converted into Y-parameters in order to extract parasitic capacitances (Fig. 1.9(d)). The resulting Y-matrix could be subtracted from the measured Y-parameters of the device to remove the parasitics towards ground and between the two ports. Next, S-parameters of the short fixture could be converted to an impedance matrix to extract the parasitic inductances of the access lines and towards the ground (Fig. 1.9(d)). The combination of the two steps is summed up in the following equation

$$Y = \left((Y_{\mathrm{DUT}} - Y_{\mathrm{open}})^{-1} - \left(Z_{\mathrm{short}}^{-1} - Y_{\mathrm{open}} \right)^{-1} \right)^{-1} \tag{1.1}$$

where Y_{DUT} is the admittance matrix obtained from the measured S_{DUT}, Y_{open} is the measured admittance matrix of the open fixture, Z_{short} is the measured impedance matrix of the short fixture, and Y, with terms Y_{ij}, $i, j = 1, 2$, is the admittance matrix of the de-embedded device.

EM-based de-embedding is conducted using Keysight Momentum for the electromagnetic simulation of the RF pads, incorporating the full epitaxial stack of the process, as provided by the foundry. This approach accounts for all EM interaction between different metal layers and back-via-induced effects. Appropriate ports, i.e., a 50-Ω impedance for probe connections and multiple transmission-line terminations for the internal lines, are applied through simulations for obtaining two two-port S-parameter matrices (one for each pad). These are then converted into transmission T-parameter matrices in order to apply:

$$T = T_{\mathrm{pad,L}}^{-1} \cdot T_{\mathrm{DUT}} \cdot T_{\mathrm{pad,R}}^{-1} \tag{1.2}$$

where $T_{\mathrm{pad,L}}^{-1}$ and $T_{\mathrm{pad,R}}^{-1}$ represent the inverted T-parameters of left and right pads, respectively, T_{DUT} is obtained from the measured S_{DUT}, and T is the de-embedded T-matrix, which can then be converted into the de-embedded admittance matrix Y.

1.5 This work

1.5.1 Objective

This Ph.D. research is dedicated to enhancing PA performance for green telecommunication systems, focusing on two main areas of study. The first area explores the

degradation of performances due to the presence of defects in modern GaN devices. To address these challenges, a specialized experimental setup has been developed to accurately capture and analyze performance metrics associated with trapping effects. These effects can significantly impact device behavior, making it crucial to evaluate their influence within the context of specific technologies. By identifying and quantifying the impact of these trapping effects, the research enables informed comparisons of GaN devices for their suitability in targeted applications. Additionally, performing this detailed characterization on newly fabricated devices can help pinpoint production defects, potentially improving manufacturing processes. The second area of research focuses on leveraging varactor devices within the output matching network to design a reconfigurable amplifier architecture. For this approach to be effective, it is essential to thoroughly understand and model the behavior of the varactor device under various conditions. This is achieved by measuring the performance of diode devices, which serve as varactors, and subsequently extracting a nonlinear model. A key innovation of this research lies in the development of a novel automatic modeling procedure here applied to both single devices and more complex structures. This methodology efficiently generates a lumped-element circuit representation by analyzing vector measurements, providing a precise and reliable foundation for simulating and fine-tuning the target matching network.

A key aspect of this Ph.D. is the diversity of activities carried out, covering the RF designs in the simulator, the realization of custom fixtures to address RF measurements, and the development of experimental setups tailored to the specific measurement needs of each solution. As such, the effort put on the build and optimization of such automated setups constitutes an important part of this work. Most of the measurement campaigns have been carried out by the author in the RF laboratory of the University of Bologna, Bologna, Italy in the Electronic Design and Measurement (EDM) Laboratory research group. During the Ph.D. program, 3 months were spent at the Ferdinand Braun Institut (FBH), Berlin, Germany where access to the internal foundry resulted in an enriching opportunity for both the development and measurements of custom devices. Moreover, the collaboration of 6 months with Microwave Electronics for Communications (MEC), Bologna, Italy allowed the author to improve the RF design experience.

1.5.2 Organization of the text

The Thesis is organized as follows:

- Chapter 2 focuses on the characterization of state-of-the-art GaN HEMT pro-

cesses. This first assessment is particularly important when a new technology needs to be evaluated, since trapping effects could play a relevant role in active device performances. The extraction of multiple figures-of-merit from many device samples is addressed. The characterization is carried out with a new measurement approach, involving the realization of a custom automated setup capable of reducing the overall characterization time. First, the realized pulsed board is presented in addition to the custom setup developed. Then, measurement results obtained from many samples are reported, highlighting peculiar behavior observed from new-concept HEMTs.

- Chapter 3 presents the evaluation of Schottky diodes for the exploitation of their varactor properties. As explained in Sec. 1.3, despite being used in numerous circuits, not all fabrication processes include varactors in the design kit, making them available for designers. Therefore, the extraction of the main varactor metrics for suitable available devices, like diodes, provides information about the possibility to effectively exploit them as varactors. Two different GaN-on-SiC technologies are presented with characterization performed up to 50 GHz, targeting the use in mm-wave circuits. Many peripheries are analyzed to find the best trade-off between tuning range and losses.

- Chapter 4 addresses the next step in varactor characterization, namely the extraction of a circuit model from device measurements for use in the simulation environment. Despite many models do exist in literature for integrated varactors, the procedure usually relies on pre-determined networks, often derived from physical properties, and measurements targeted for specific network elements. Instead, a new modeling approach is being developed and presented with the advantage of being automatic in developing the required network and fully flexible with respect to the required dataset.

- Chapter 5 explores the power amplifier design strategies for the use of varactors as tunable elements to improve efficiency. Different approaches are evaluated, such as varactors employed in shunt or series configurations, as well as the introduction of complex topologies involving more varactors in series-parallel configurations. Custom amplifiers have been realized in different variants in GaN-on-SiC 150 nm technology and characterized. Moreover, a custom matching network in 120 nm GaN-on-SiC technology is proposed.

Finally, in Chapter 6 the main results achieved during the Ph.D. are summarized and future research goals are discussed.

Chapter 2

GaN HEMT characterization

2.1 Introduction

As discussed in Sec. 1.1.3, GaN technology is widely adopted for high-frequency applications. Its superior performances include high breakdown voltage and high electron mobility, both allowing for the reduction of the device size with the same expected performances. The potential to realize thinner drift regions also allows for the reduction of the ON-resistance, lowering the dissipated power, and increasing the overall efficiency of the amplifier. This reduction in size leads to a reduction in parasitic capacitances, especially on the gate side, enabling faster commutation and high-frequency operations. Reducing the gate length below 150 nm requires to properly scale epitaxial layers as well as avoiding undesired effects impacting the performances [60]. One prominent effect of scaling is the short-channel effect. This dynamic directly influences the channel surface potential by the drain voltage, referring to the drain-induced barrier lowering (DIBL) effect. Neglecting this underestimates the device's subthreshold current and its dependence on the drain voltage.

To mitigate these effects, iron (Fe) could be introduced in the GaN buffer [61, 62], with the advantage of obtaining a semi-insulating buffer layer increasing the blocking voltage. However, the introduction of dopants comes with the increased presence of defects that directly affect the current propagation. We usually refer to this effect as current collapse (CC) leading to decreased output power and PAE. While surface passivation [63] and/or the adoption of field plates [64] is effective in mitigating the impact of surface traps, electron trapping in the buffer is still a problem to be addressed [65]. Both the defects introduced during the layer deposition and the presence of dispersive effects due to iron doping can limit the performance and reliability of GaN HEMTs. Hence, accurate characterization of thermal and trapping effects is crucial

for the performance optimization of these solutions.

This chapter presents an extensive characterization of multiple device samples, focusing on the extraction of various figures-of-merit that quantify the influence of trapping effects on device performance. To streamline the process, a novel experimental framework based on drain current transient (DCT) measurements is introduced. This approach significantly reduces the number of required measurements, thereby accelerating the overall extraction process. By relying on a single type of measurement, the proposed framework simplifies the procedure and ensures consistency by utilizing a single configuration for the experimental setup. Additionally, a comparative analysis with traditional techniques, such as single-pulsed I-V (SPIV) measurements, is provided to demonstrate the accuracy and reliability of the proposed extraction method. The result of the work has been published in [66, 67]. This chapter is organized as follows: the trapping phenomena are deeply addressed in Sec. 2.2 where the state-of-the-art measurement approaches are presented. In Sec. 2.3 the new strategy for the complete characterization is discussed for each metric of interest. Sec. 2.4 describes the custom measurement setup adopted as well as the challenges faced. Measurement results are presented in Sec. 2.5 for classical structures and in Sec. 2.6 for a new type of buffer-free devices. Conclusions on the experimentally effects observed are drawn in Sec. 2.7.

2.2 Trapping phenomena

Trapping effects play a significant role in degrading the dynamic performance of GaN HEMTs, often manifesting as a reduction in maximum current or high-frequency gain. These effects can impose critical limitations on both high-frequency and high-power operations, constraining the overall potential of the device. By analyzing transient characteristics and pinpointing the location of trapping centers, it becomes possible to validate the production process and identify areas for optimization. Enhancements in growth techniques and adjustments to processing parameters can then be implemented to mitigate these adverse effects. The complex, layered structure of GaN HEMTs inherently allows for the formation of charge trapping centers at various locations within or between layers. Traps situated near the gate metal are referred to as surface traps and have a direct influence on the threshold voltage and current collapse. These traps lead to the accumulation of surface charges, which in turn expand the gate depletion region, forming a negatively charged virtual gate. This phenomenon significantly impacts device performance but can be mitigated through surface passivation

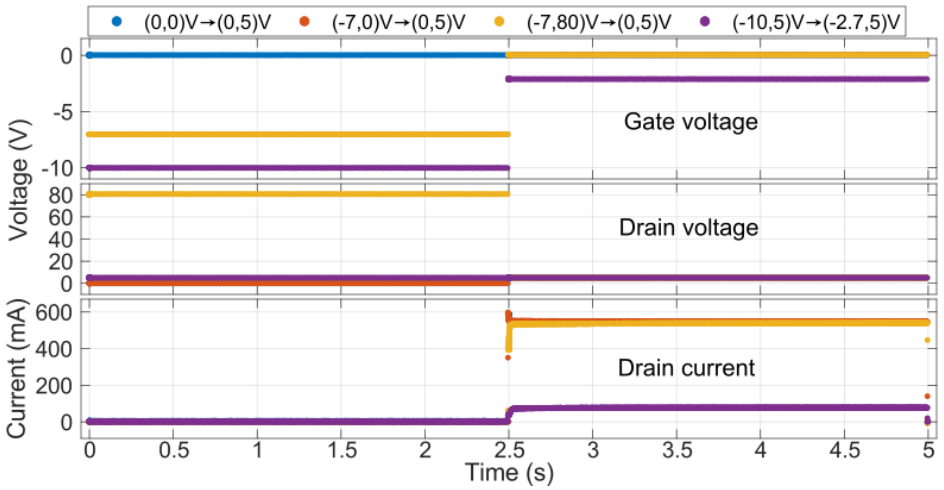

Figure 2.1: 50%-duty-cycle acquired waveforms for different configurations of gate/drain voltage and corresponding drain current (top to bottom). Full recovery of the drain current transient is guaranteed by adopting a period $T = 5$ s.

techniques, as discussed in [68]. Furthermore, electrons in the 2DEG may become injected into the buffer layer, where they are trapped in dislocations caused by lattice mismatches or impurities. Once trapped, these electrons disrupt the concentration of the 2DEG, resulting in a decrease in current density.

Various techniques have been explored for sensing the distribution and properties of the traps, each one with different capabilities [69]. Traditional SPIV characterization does not typically allow to study trapping dynamics, although modified PIV-based approaches like the double-pulse technique [70] in various implementations [71, 72, 73] have been used for the purpose as well as for nonlinear compact modeling [72, 73] and for design considerations [74]. Trapping dynamics have most often been studied by DCT measurements, and a range of DCT-based techniques have been applied to several types of GaN HEMT process technologies [75, 76, 77, 78, 79].

2.3 Extraction strategy

2.3.1 Overview

The strategy proposed aims to condense different approaches targeting the extraction of the principal trapping behaviors. The specific DCT-based framework makes use of square-wave excitations with 50% duty-cycle among different OFF and ON states. By ensuring that the waveform period (T) is sufficiently long to allow trapped charge levels to reach equilibrium, the framework effectively performs a step-response

characterization, as described in [80]. Under these conditions, the transient drain current profile observed during the ON state provides valuable insights into the trapping dynamics at play. A key advantage of this technique lies in its ability to capture the drain current response immediately after the square-wave transition, before any self-heating effects occur. This approach ensures that the measured current levels correspond precisely to those obtainable through SPIV measurements under identical ON- and OFF-state voltage conditions. Consequently, the method facilitates the extraction of all metrics typically derived from conventional SPIV procedures. Illustrative examples of the observed voltage and current transients for various ON/OFF state configurations are presented in Fig. 2.1, showcasing the versatility and reliability of this characterization approach in analyzing trapping dynamics and associated device behaviors. In the next Subsections all FoM of interest are described and the extraction from DCT waveforms is described.

2.3.2 Static IV

The first step to properly characterize active devices is mapping their capabilities in terms of current and power dissipated. This could also be the first step in the identification of faulty devices after the wafer manufacturing. It should be noted that RF transistors usually come in a common source configuration, meaning that the source contact is directly connected to ground terminal and these connections are optimized for stability and heat conduction. The extraction is performed by concurrently applying dc voltages to both the gate and drain ports that will be swept to realize all the possible combinations of voltages in a given range. Since the voltage is imposed to each port, the measurement target are the currents that flow through the device. The gate is expected to show a pure capacitive behavior and, as such, for dc stimuli the current flow is negligible. The drain current, in contrast, is the primary metric, from which the power dissipated from the device is also derived. This power performance, mathematically obtained by the multiplication of drain voltage and current at dc, limits the possible combinations of drain voltage and gate voltage the device could sustain without damage.

The maximum ratings of a device are known as safe-operatig-area (SOA) and declare the possible ranges the device can continuously tolerate without having any permanent damage. Ranges are usually expressed as voltage limitations for the two ports (gate and drain inputs) that account for different physical implications for the device. Gate allowed voltages are usually reported, which are usually related to the conduction of the metal-insulator interface when a positive voltage is applied. The

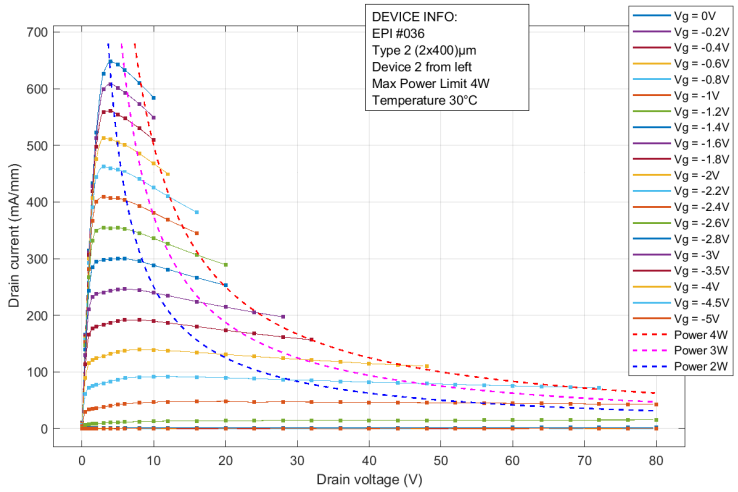

Figure 2.2: Static IV extraction for one sample performed at 30°C

negative voltage limit is also important since the thin insulation layer under the gate metal can only support few volts. The maximum voltage supported on the drain side is limited as well to avoid any breakdown effects. Breakdown consists in a rapid increase in drain current, which occurs - in the off-state - when the drain voltage reaches a critical value. Since usually devices are polarized in voltage-controlled mode, the current flow is not limited in magnitude, therefore the breakdown condition is usually destructive. Short-channel effects are sometimes responsible for drain-source leakages in OFF-state. Power dissipation is also included in SOA definitions and usually expressed as W/mm where watts represent the power computed from the drain voltage and current while the length represent the device finger overall length that can be computed multiplying the finger number and the length of each finger. This metric is tightly bonded to device technology and layer composition.

During the application of the described voltages and currents, the device will inevitably produce heat and the channel temperature will be different from the ambient temperature or the baseplate one. Each point in the IV characteristic feature a different dissipated power and a different temperature from the points nearby. This fact has direct implications on the extraction of device electrical characteristics that could not be properly distinguished from heat impact on the drain current.

The characterization procedure could be time-consuming depending on the number of points to which measurement will be performed. The steady state condition of the device must be granted for this metric, and this usually implies maintaining the polarization condition for some seconds. An example is provided in Fig. 2.2. The extraction is performed at 30°C baseplate temperature and for a power dissipation

of maximum of 4W. The effect of the heating is particularly strong on the curves for higher gate voltage, where high current is drawn.

2.3.3 Gate and drain lag

To address the limitation of static IV characterization, pulsed IV (PIV) is usually adopted to extract the IV characteristic. The static gate and drain voltages are replaced by periodic two-level waveforms.

Traditional SPIV measurements are widely adopted by foundries for performance evaluation of GaN HEMTs. They are implemented by applying different OFF-state bias conditions for most (e.g. $\geq 99\%$) of the waveform period, while ON-state conditions are briefly applied in a short pulse, avoiding self-heating. The drain current acquired during the pulse is used to extract trap-related FoMs of interest, such as gate/drain lag. The OFF-state points are selected as $(V_{GS}, V_{DS}) = (0, 0)$ V for reference waveform, as the 0 V bias for both gate and drain grants no charges are present in the device therefore no trapping is associated. The gate lag metric aims to assess the trap states in the vicinity of gate contact. Therefore only a gate voltage is applied and usually selected as the lowest voltage the device can sustain. For this technology the gate lag point selected is $(V_{GS}, V_{DS}) = (-7, 0)$ V. The gate-lag is computed as the relative variation (in %) with respect to reference current value. Drain lag metric, instead, targets the trapping effects related to buffer traps, therefore a large voltage between source and drain is applied. The bias point selected is $(V_{GS}, V_{DS}) = (-7, 80)$ V which of course requires a negative gate voltage for the device to stay in OFF-state. As the gate voltage also can influence the current dynamic response (as the gate lag metric assesses), the same voltage of -7 V is selected and the drain lag is extracted considering the gate lag waveform as its reference. The ON-state sensing point is taken on the device knee at $(V_{GS}, V_{DS}) = (0, 5)$ V. In particular, the sensing point is selected to draw the highest current while maintaining the device in the saturation region. While other definitions for the lag metrics can be found in the literature, the voltage points and extraction procedures here adopted are compatible to those commonly used by foundries. The whole extraction is carried out at the lowest user-controlled baseplate temperature available for this setup ($\theta_B = 21°\text{C}$).

Example drain current waveforms for both classical pulsed extraction and the proposed DCT methodology are reported in Fig. 2.3(a)-(b) respectively. Only the ON-state portion of the DCT waveform is visualized as in the OFF-state the current is negligible and no information is extracted. Considering the DCT case, the current is acquired across a time-window between 100 ns and 300 ns after the pulse edge,

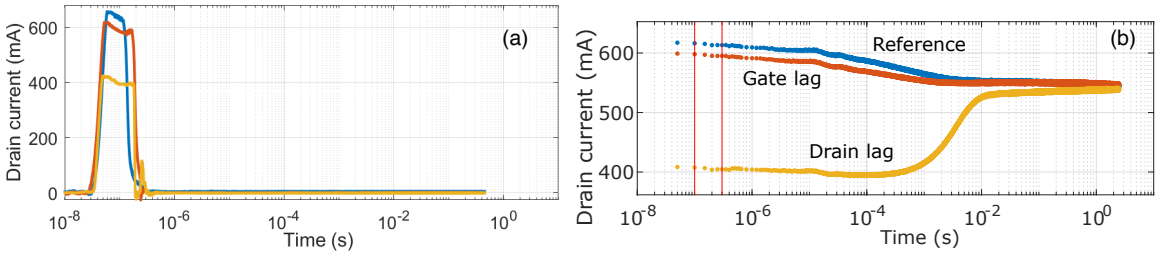

Figure 2.3: Example of current waveforms for the gate- and drain-lag extraction based on (a) classical pulsed characterization and (b) DCT extraction. With DCT only the first 200 ns are sampled and averaged.

obtaining a reference current of 615 mA, a gate-lag current of 592 mA (4%), and a drain-lag current of 404 mA (32%). From SPIVs, we obtain a reference current of 620 mA, a gate-lag current of 587 mA (5%), and a drain-lag current of 393 mA (33%), substantially in line with DCT.

2.3.4 Thermal resistance

Thermal resistance serves as a fundamental metric for quantifying the heat dissipation capabilities of GaN devices, thereby influencing their potential for operating at higher power levels. Accurate estimation of thermal resistance plays a pivotal role in device modeling, enabling a comprehensive understanding of the thermal-dependent trap behavior. As it will be described in Sec. 2.3.5, the accurate evaluation of channel temperature is a pivotal step for the correct identification of traps [65].

The methodologies described in the literature for determining thermal resistance can be broadly categorized as direct measurements, indirect deduction, usually through electrical measurements like currents, and simulation-based approach. Direct measurement techniques involve Raman scattering spectroscopy [81], infrared (IR) imaging, and more advanced atomic force microscope (AFM) coupled with thermal probe [82], which are among the most precise methods available, allowing direct measurement of the local temperature distribution. These approaches, however, come with significant practical limitations as they often require specialized equipment and dedicated sample preparation. On the other hand, 3-D finite-element simulations offer a powerful alternative by modeling the thermal behavior of the device. This method requires a highly accurate 3-D representation of the device, including precise geometries and thermal properties for all constituent materials. However, its implementation depends on having access to sensitive proprietary information from the device foundry, which is often restricted due to confidentiality agreements. As a result, designers may face challenges

in utilizing this approach unless such information is made available. Moreover, when the DUT comes over a metal carrier, the thermal properties of the glue and the carrier itself need to be considered in the simulation as well.

Electrical measurement techniques provide a more practical and noninvasive solution. These methods use an electrical parameter, such as threshold voltage, drain/collector current, output conductance, transconductance, or even S-parameters, to monitor the device's operating temperature. The temperature sensitivity of these parameters is typically characterized through measurements performed under static multi-temperature conditions or pulsed/transient regimes. While these techniques can be carried out relatively quickly with standard laboratory equipment, they have some limitations. Notably, the temperature estimation is inherently averaged over the active region of the device, potentially underestimating the peak temperature, depending on the specific measurement procedure employed. Despite these drawbacks, electrical methods are widely favored for their simplicity and accessibility.

Multiple thermal resistances could be identified in GaN transistors between the 2DEG, where current flows and heat is generated, and the thermal pad, usually the chip carrier. The procedure here adopted follows the one in [83] that results in being very suitable to the DCT pulses applied. As also suggested in [83], a periodic pulsed waveform is preferable instead of single-pulse type characterization as it will also allow to average the measurement over some periods. In doing so, some conditions need to be checked, as if a wrong configuration is provided, false outcomes are expected. Particularly, the period of the pulsed waveform has to be long enough to let the device channel cool down to the baseplate temperature during the T_{OFF}. The downside in the use of extremely large periods is the overall sweep duration, therefore the tradeoff should be searched for each device type.

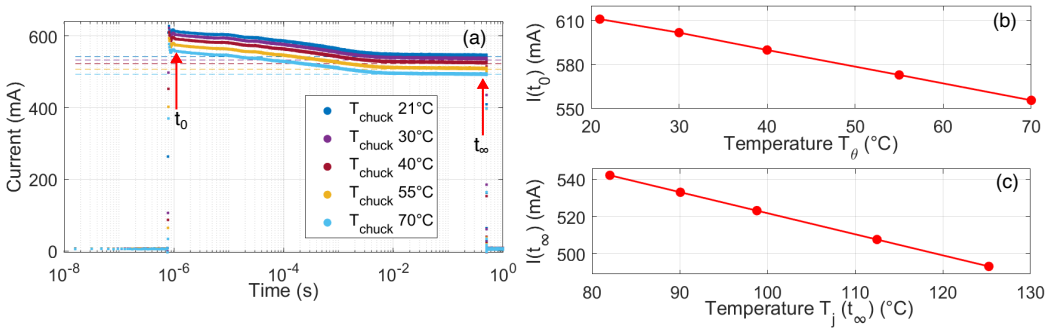

Figure 2.4: (a) Waveforms acquired at multiple baseplate temperatures for R_{th} extraction. (b) Sampling of drain current for each waveform at t_0. (c) Extrapolation of junction temperature θ_j based on interpolation in (b).

The thermal resistance R_{th} can be extracted from DCTs acquired at multiple baseplate temperatures θ_B. The transition selected is $(V_{GS}, V_{DS}) = (0, 0)$ V to $(V_{GS}, V_{DS}) = (0, 5)$ V. In particular, the drain current is sampled at $t_0 = 100$ ns just after the voltage edge and at t_∞ at the end of the transient, as indicated in Fig. 2.4(a). Fig. 2.4(b) reports $i(t_0)$ for each tested temperature. Then, the relationship $F(\theta_B)$ as defined in [83] can be interpolated by considering $i(t_0)$ for each θ_B. The quantity $\Delta\theta_j = F^{-1}(i_{t\infty}) - F^{-1}(i_{t0})$, i.e., the absolute variation of the junction temperature, can then be computed along with $P^{diss} = v_{DS}(t_\infty)i_{DS}(t_\infty)$, being v_{DS} and i_{DS} the time-domain waveforms of the drain voltage and current, respectively. The result is represented in Fig. 2.4(c). The thermal resistance is then obtained as $R_{th} = \Delta\theta_j / P_{diss}$ resulting, for the specific DUT, an $R_{th} \simeq 22.5$ °C/W.

As a comparison, the R_{th} was also extracted from SPIVs as done in [84] by exploiting the absence of self-heating. Firstly, the reference SPIV provides a mapping between the pulsed current and θ_j. Then, six SPIV acquisitions from different ON-state quiescent levels at different dissipated powers were used to extract R_{th}. Even if the waveforms for the extraction could have a low duty cycle and reduced time period, many additional waveforms need to be applied and sampled for the sole purpose of this extraction, requiring more measurement time.

2.3.5 Trap Activation Energy and Cross Section

While PIV characterization is a powerful tool to evaluate the impact of traps on the device current, the information that can be extracted is limited to the magnitude of the effects and few insights can be deduced for the traps themselves. Moreover, PIV parameters such as period or duty cycle are taken differently for each technology under test. This could lead to different effects observed for different characterizations, as the outcome is usually only a number and not the complete waveform acquired.

Many effects are demonstrated to be involved in the electron conduction and each effect takes time to manifest, usually an order of magnitude greater than the pulse time of PIV curves. Depending on the location of the defects and the device fabrication, detrapping effects can be observed to extinguish in many seconds [85].

One method consists of the analysis of current or capacitance [86] transients resulting from the response of the device to specific voltage steps and is referred to as deep level transient spectroscopy (DLTS). The current-based DLTS (I-DLTS) variant assesses the traps characterization by the observation of the drain current after the application of a voltage step. Since the drain current is dependent on both the gate and drain voltages, steps could be applied on the gate side, drain side, or both. The

dynamic current evolution in time can be exploited to gather valuable insights on the location and physical causes of the defects. In contrast to PIV measurements, where only the short pulse time needs to be acquired, in I-DLTS the evolution of the current during the complete ON-period should be considered. This justifies the required setup built for this purpose presented in Sec. 2.4. Limitations of this method arise when information on the traps behavior needs to be evaluated in configurations where the drain current is negligible. In such states, other methods must be used to complete the characterization.

Similarly to Current-Deep Level Transient Spectroscopy (I-DLTS) [87], the OFF-state bias in DCT acts as trap-filling pulse, while the observation of the drain current transient in the ON-state allows the extraction of de-trapping time constants of charge emission process. Various methods have been employed for this purpose, including multi-exponential fitting [75], analysis of the current transient derivative [88], and stretched exponential fitting. In this work, we apply the logarithmic time derivative of the current waveform, which yields a peak in the derivative curve corresponding to the emission process time constant.

The following procedure has been utilized in this work, starting from the device equations to obtain the final formulation. From [89], the detrapping time-constant for an electron trapped at a level E_T, such that $E_C - E_T = E_A$ where E_A is the activation energy, is:

$$\tau_n = \frac{1}{\sigma_n v_{th} N_c} e^{\frac{E_A}{kT}} \tag{2.1}$$

where N_c is the effective density of states in the conduction band, v_{th} is the thermal velocity of electrons and σ_n is the capture cross-section of the trap. This comes with the hypothesis that only thermal processes are in place and the degeneracy factor is one. The electron thermal velocity is found by equating the thermal energy ($\frac{1}{k}T$ per degree of freedom, and electrons have three as they can be treated as point particles) to their average kinetic energy. The value is:

$$v_{th} = \sqrt{\frac{3kT}{m_n}} \tag{2.2}$$

where $m_n = m_e m_n^*$ is the effective mass of the electron in the (bottom of) conduction band, m_e is the mass of a standard electron and m_n^* is the relative effective mass. Similarly, for the effective density of states in the conduction band:

$$N_c = 2\left(\frac{2\pi m_n kT}{h^2}\right)^{3/2} \tag{2.3}$$

Combining 2.2 and 2.3 in 2.1 it results:

$$\begin{aligned}\tau_n &= \frac{1}{\sigma_n \left(\frac{3kT}{m_n}\right)^{1/2} 2 \left(\frac{2\pi m_n kT}{h^2}\right)^{3/2}} e^{\frac{E_A}{kT}} \\ \tau_n &= \frac{h^3}{\sigma_n T^2 k^2 m_n 2^{5/2} 3^{1/2} \pi^{3/2}} e^{\frac{E_A}{kT}} \\ \tau_n T^2 &= \frac{h^3}{m_e k^2 2^{5/2} 3^{1/2} \pi^{3/2}} \frac{1}{m_n^*} \frac{1}{\sigma_n} e^{\frac{E_A}{kT}}\end{aligned} \tag{2.4}$$

in which the first term is only a constant value while the second term depends on the material. Taking the natural logarithm of both sides (assuming SI units):

$$\begin{aligned}\ln(\tau_n T^2) &= \ln(\frac{h^3}{m_e k^2 2^{5/2} 3^{1/2} \pi^{3/2}}) - \ln(m_n^*) - ln(\sigma_n) + E_A \cdot \frac{1}{kT} \\ \ln(\tau_n T^2) &\approx -58.7453 - ln(m_n^*) - ln(\sigma_n) + E_A \cdot \frac{1}{kT}\end{aligned} \tag{2.5}$$

For Gallium Nitride a value of $m_e^* = 0.2$ can be considered, finally resulting in:

$$\ln(\tau_n T^2) \approx -57.1358 - ln(\sigma_n) + E_A \cdot \frac{1}{kT}. \tag{2.6}$$

Therefore, the plot of extracted time constants τ_n could be used for the extraction of both the activation energy E_A and cross-section σ_n simply by extracting the slope and intercept of the linear interpolation of the time constants. In fact, if on the x-axis the quantity $\frac{1}{kT}$ is considered and on the y-axis the term $\ln(\tau_n T^2)$ is computed, E_A is directly mapped to the slope of the interpolation, while σ_n corresponds to the intercept once corrected from the constant factor. This type of plot is also known as Arrhenius plot. It should be considered that σ_n is expressed in m^2 with the given constant, therefore a multiplication by 10^4 is required to obtain a value in cm^2 as often is reported in literature.

An example extraction is provided in Fig. 2.5 where Fig. 2.5(a) reports the drain current waveforms for the the selected transition $(V_{GS}, V_{DS}) = (-7, 80)$ V to $(V_{GS}, V_{DS}) = (0, 5)$ V measured at multiple baseplate temperatures from 21°C to 70°C. The current recovery percentage with respect to static current for each bias-temperature couple is computed and reported to verify that the T_{ON} time of 2.5 s is sufficiently long. In Fig. 2.5(b) the log-time derivative is shown for each temperature. The peak in each waveform is identified with a star and the corresponding time instant is the de-trapping time τ_n of interest. The couple $(T, \tau_n(T))$ is derived for every tested θ_B and used for the Arrhenius plot in Fig. 2.5(c) to obtain the red non-compensated interpolation. The dissipation power P_{diss} at $t = \tau_n$ is employed in combination with R_{th} to extract a new $T_{comp} = \theta_B + P_{diss} * R_{th}$ used in the Arrhenius plot in place of θ_B to obtain the compensated interpolation [90]. From this interpolation, recalling Eq. 2.6, E_A and σ_n could be extracted.

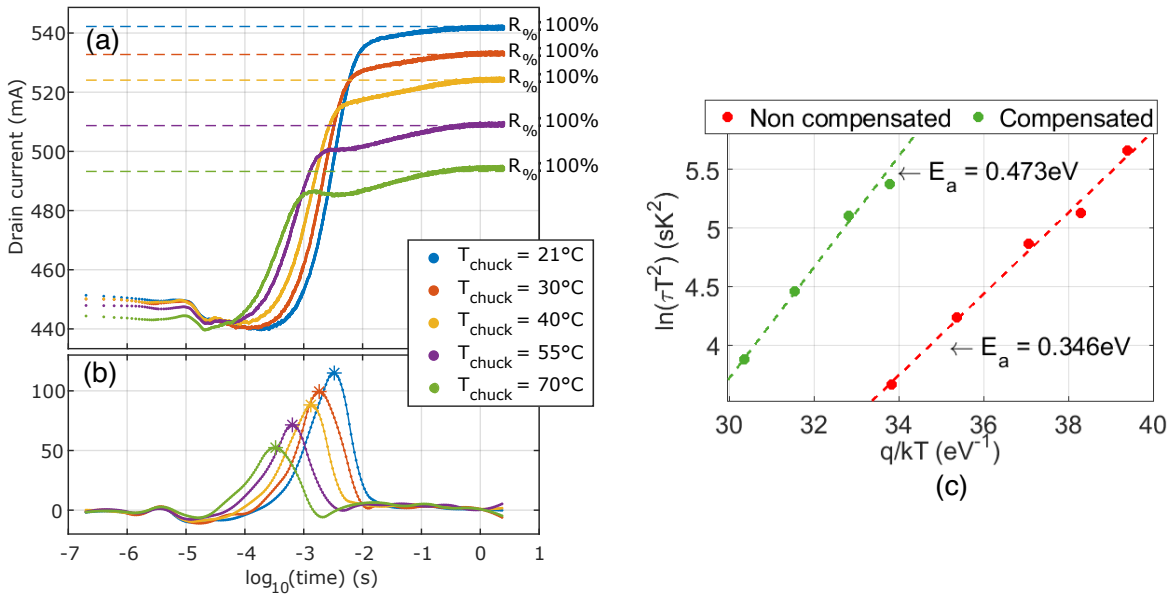

Figure 2.5: (a) Drain current waveforms acquired at multiple baseplate temperatures for transition $(V_{GS}, V_{DS}) = (-7, 80)$ V to $(V_{GS}, V_{DS}) = (0, 5)$ V and (b) the extracted time-derivative where selected de-trapping time constants are highlighted with a star. (c) Arrhenius plot with and without temperature compensation.

2.3.6 Density of Trapped Carriers

As reported in [91], DCT measurements also allow for the estimation of the dynamic reduction of the available charges in the two-dimensional electron gas (2DEG) due to the presence of ionized traps. This parameter is usually only derived from TCAD simulations and not always considered in the device characterization. For the extraction, the formulation of drain current can be exploited:

$$I_{DS}(t) = \frac{\omega_g v_{sat} \epsilon}{d + \Delta d} \left(V_{GS} - \Phi_B - \Delta E_C - \frac{q(n_s - n_T)(d + \Delta d)}{\epsilon} \right) \tag{2.7}$$

where E_C is the conduction band offset at the heterointerface, and n_s denotes the 2DEG density (in cm^{-2}) in the channel layer, Φ_B is the Schottky barrier height, d is the distance between the gate electrode and the 2DEG channel, and Δd is the effective depth of the 2DEG channel from the heterointerface. This expression could then be evaluated in two points: one located at the end of the pulse application (t_∞) and the second just after the pulse application t_1. At $t = t_\infty$ the reduction in 2DEG density caused by trapping (n_T) is considered extinguished, therefore a value of $n_T = 0$ is expected, simplifying the Eq. 2.7. The difference of current at the start and the end of the pulse can be computed and results in [91]

$$\Delta I_{DS} = I_{DS}(t_\infty) - I_{DS}(t_1) = -\omega_g v_{sat} q n_T (d + \Delta d) \tag{2.8}$$

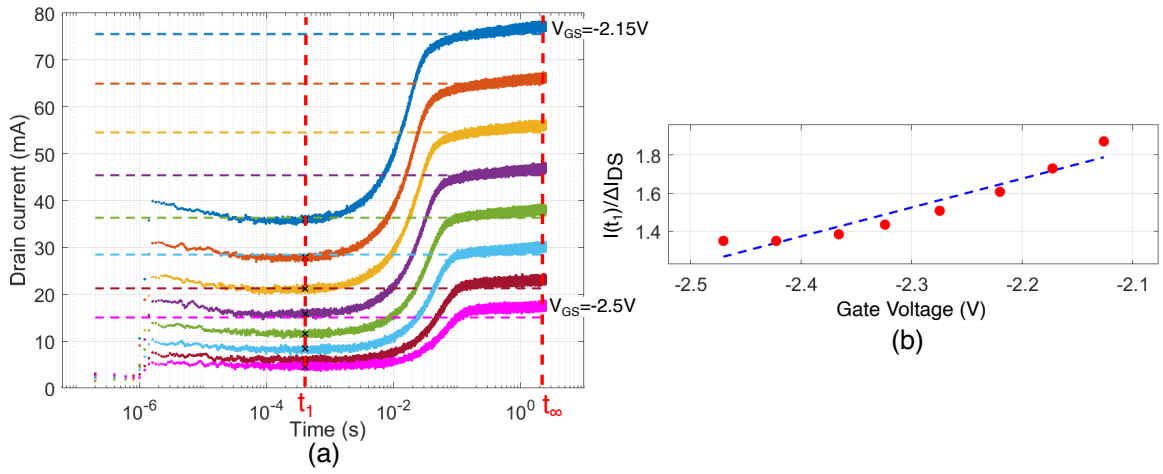

Figure 2.6: (a) Current waveforms for V_{GS} from -2.5 V to -2.15 V and $V_{DS} = 5$ V. The current is sampled at t_1 and t_∞. Dashed lines indicate the expected current from dc characterization. (b) Extracted current ratio as in Eq. 2.9 towards gate voltage for same range in (a).

and if the ratio $I_{DS}(t)|_{t=t_\infty}/\Delta I_{DS}$ is considered, it results in

$$\frac{I_{DS}(t)|_{t=t_\infty}}{\Delta I_{DS}} = \frac{\epsilon}{(d+\Delta d)qn_T}V_{GS} + \text{const.} \tag{2.9}$$

If replicated for many gate voltages V_{GS} and $\frac{I_{DS}(t)|_{t=t_\infty}}{\Delta I_{DS}}$ is plotted against V_{GS}, the slope of the linear interpolation can be tracked down to n_T.

The transient OFF-state serves as a filling pulse to let the electrons occupy all the available vacancies, therefore the lowest possible gate voltage is applied, selected as -10 V for this technology. In contrast, the effect of the drain voltage should be minimized, therefore a fixed voltage $V_{DS} = 5$ V is applied. The gate voltage in the ON-state is instead selected to achieve a semi-on condition, i.e. to have a low drain current so as to reduce the impact of self-heating. The extraction results are shown in Fig. 2.6.

2.4 Measurement setup

The setup required for the generation and acquisition of voltages and currents as described in last section has to be configured ad-hoc and many adjustments were needed to achieve the desired performances. A photo of the overall setup is shown in Fig. 2.7(a) while its schematic representation is provided in Fig. 2.7(c). On the drain side, both high-voltage and high-bandwidth acquisitions are necessary. The target voltage for the pulses is up to 100 V and some safety margins need to be taken into

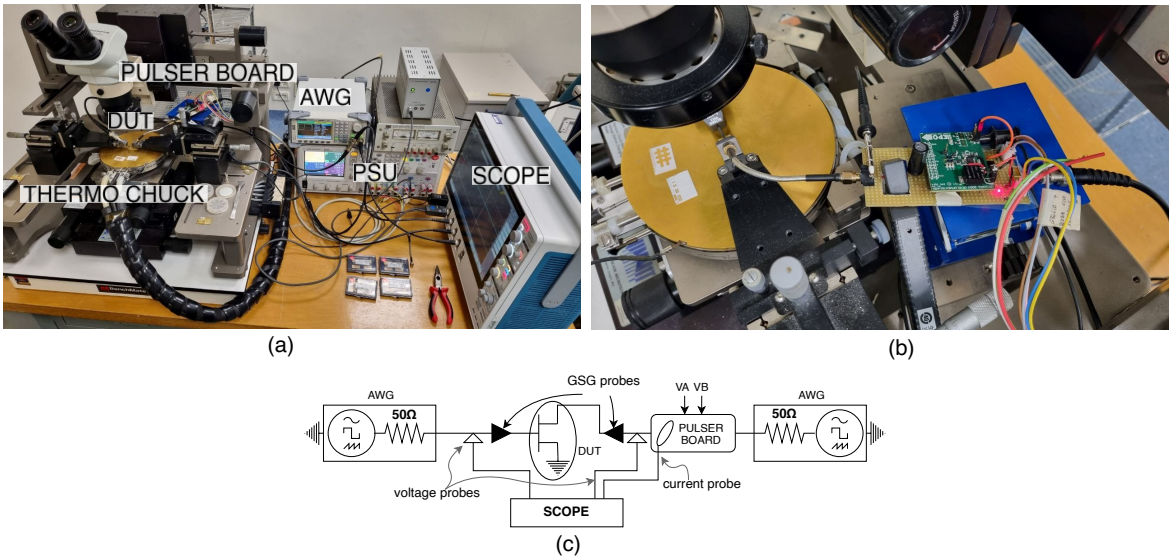

Figure 2.7: (a) Photo and (c) schematic representation of the measurement setup used for transient characterization. (b) Close up of the custom pulser board.

account due to spurious effects related to the very low switching time, while currents up to 1 A can be observed when the device is fully conductive. The high bandwidth requirement is motivated by the expected fast edges of the signal, in the order of nanoseconds, on both voltage and current waveforms. A standard high-impedance voltage probe and a clamp current probe (Keysight 1147A) are selected, offering adequate bandwidth and avoiding calibration procedures since the frequency behavior is already compensated by the manufacturers either by electronic compensation or by means of a dedicated internal circuit. On the gate side, due to the low voltages required, a direct connection to the scope input is in place. A Tektronix MSO56 real-time oscilloscope is responsible for all voltage and current measurements, offering 250 MHz of analog bandwidth and a maximum of 6.25 GSamples/s. An arbitrary signal generator from Siglent (SDG2122X) provides the voltage control for both drain and gate side, while an Agilent N6705B power supply is used for the required voltages on drain side. The probe station baseplate can be arbitrarily controlled in temperature by a thermo chuck from Temptronic TP03215A. The chuck can only heat up the baseplate so to achieve a control of θ_B across the 21°C - 100°C range.

The ability to generate waveforms with fast edges is particularly interesting for the characterization of trap effects as it allows for isolating the DUT response from the effects induced by the setup and allows for the identification of very-fast trapping effects in the order of nanoseconds. If this requirement is paired with the voltages and currents involved, the selection of adequate hardware is troublesome as custom, therefore costly, solutions need to be purchased. Moreover, some flexibility is desired,

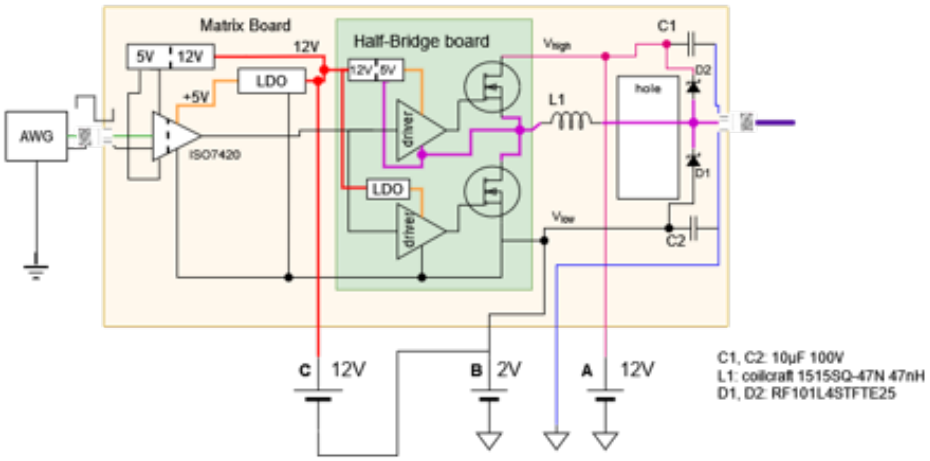

Figure 2.8: Schematic representation of the custom board visible in Fig. 2.7(b).

specifically when research is involved, to be able to adapt to peculiar device behaviors, as will be demonstrated later on in Sec. 2.6. Therefore, a custom two-level pulser board was developed in the lab. The board makes use of a commercial 5A/200V half-bridge board EPC9003 equipped with eGaN EPC2010. The adopted configuration, which is similar to the one recently shown in [92], makes use of fully-isolated gate drivers in order to provide floating control voltages with respect to the high/low power supply of the half-bridge. This additional circuitry required is mounted on a motherboard that includes also the coaxial connection for the GSG probe. In the very proximity of the connector, both voltage and current probes are accommodated to reduce to the minimum the influence of cables and parasitic. A schematic of the complete board is visible in Fig. 2.8. Regarding the half-bridge board, since the target application is power converters, the circuit is originally tuned to provide the maximum performance the technology can achieve, resulting in some non-ideal solutions. In order to mitigate voltage overshoots and ringing, gate-side series resistances need to be precisely tuned replacing the original ones. Custom solution makes use of an isolated DC/DC additional converter to properly power the upper driver of the bridge. Without the converter, a capacitor is responsible for accumulating the energy during the T_{OFF} of the waveform limiting the T_{ON} time to some milliseconds. This implementation allows for accurate two-level pulsed waveforms with arbitrary amplitudes up to 200 V, pulse widths down to 100 ns, and a slew-rate of up to 20 V/ns. The specific capability to apply sharp pulse edges accomplishes the goal of observing any transient effects in the immediate 100-ns to 1-μs range after the edge.

The acquisition of such waveforms also comes with non-straightforward solutions. The problem lies on the level of detail we are able to capture as the setup is particularly

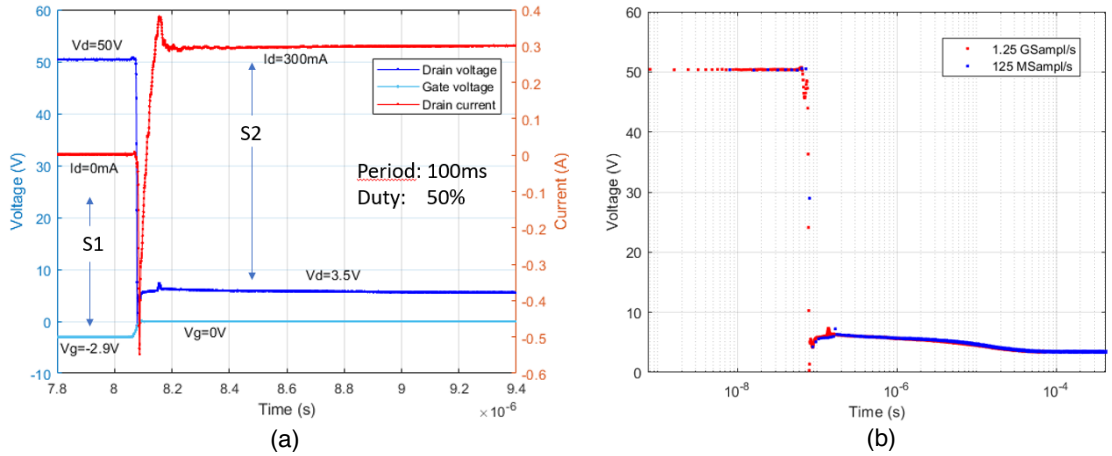

Figure 2.9: (a) Voltage and current waveforms for an excitation from $(-2.9, 50)$V to $(0, 3.5)$V. (b) Alignment of two acquisitions performed at different sampling rates for the accurate acquisition of the edge.

optimized for fast edges. As a first consideration, the maximum sampling rate should be considered in order to characterize the behavior of the device in this region accurately. At the same time, since the waveform duration could last as long as 10 s, the entire waveform should be acquired. If the highest sampling rate is then selected, the maximum number of points the instrument can collect limits the possible acquisition time to order of magnitude less than the one required. If opposite considerations are made, therefore selecting a relaxed sampling rate, less information is collected on the edge side and, in some cases, the entire edge could be absent from the collected waveform. In order to find an intermediate solution, multiple acquisitions are performed with different configurations for each pulse transition. The collected waveforms could then be glued one on top of the other as shown in Fig. 2.9(b)

2.5 Measurement results

The full characterization is conducted on multiple samples of GaN-on-SiC devices with different channel properties, barrier composition and thickness as reported in Fig. 2.10. The purpose of the investigation is to determine the impact that the different layers have on the trapping effect of the device. To reduce variability and identify effects, the layout is fixed between all devices and results in two fingers each 400-μm long, yielding a total gate width of 0.8 mm. A saturation current of 1.2 A/mm is expected from this type of HEMT and it is capable of providing about 10 W/mm RF power density at 50 V drain bias when operated in the S-band.

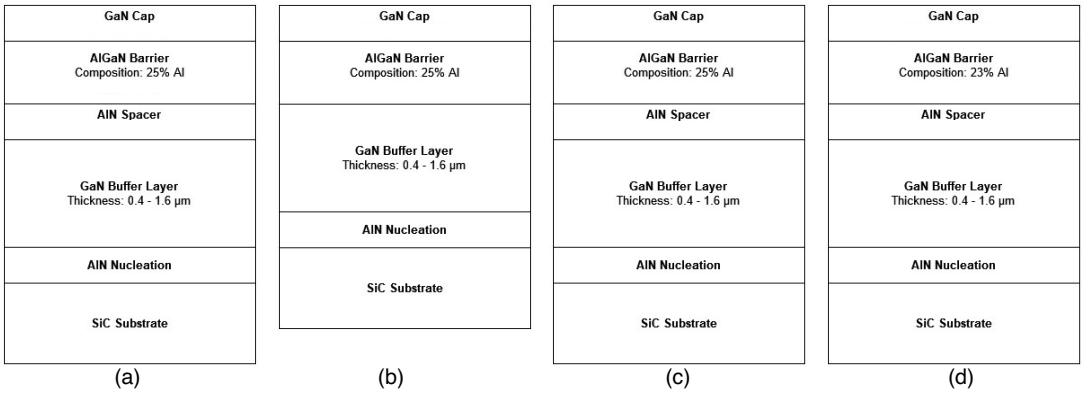

Figure 2.10: Cross sections of the available samples.

For the tests presented in this work, the drain voltage is pulsed across a minimum of 5 V (knee voltage) and a maximum of 80 V; the gate voltage is pulsed from a minimum of −10 V (sub-threshold conditions) to a maximum of 0 V. For all devices the DCT excitations are performed using $T_{ON} = T_{OFF} = 2.5$ s allowing full current recovery at the end of T_{ON} for all transitions and all temperatures. The total DCT period is therefore $T = 5$ s. As expected, the slowest recovery takes place at the coldest $\theta_B = 21°\text{C}$ for transition $(-7, 80)$ V $\rightarrow (0, 5)$ V.

As explained in Sec. 2.3.1, special care has been taken to optimize the number of acquisitions required for the complete characterization. In doing so, some pulse transitions are exploited for the extraction of multiple FoMs, taking full advantage of each waveform stored. A summary of the DCT transitions acquired at each temperature is reported in Table 2.1.

Transition	**Temperatures**				**Extraction**
	21°C	30°C	55°C	70°C	
(-10,5) → (V_G^{dens},5)	X				Trap density n_T
(0,0) → (0,5)	X	X	X	X	Reference R_{th}
(-7,0) → (0,5)	X				GL
(-7,80) → (0,5)	X	X	X	X	DL (only 21°C) E_A & σ_n

Table 2.1: Measurement plan for complete HEMT characterization. Voltage couples expressed as (V_{GS}, V_{DS}) V. V_G^{dens} indicates many gate voltages as described in Sec. 2.3.6.

Results for gate lag, drain lag and carrier density reduction n_T are summarized in Fig. 2.11. Device T1 could be considered as a reference device and the performances

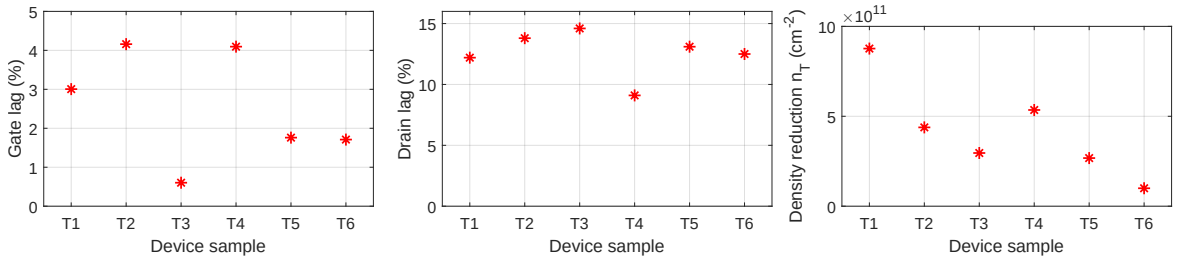

Figure 2.11: Gate lag, drain lag and carrier density reduction extracted for all samples available.

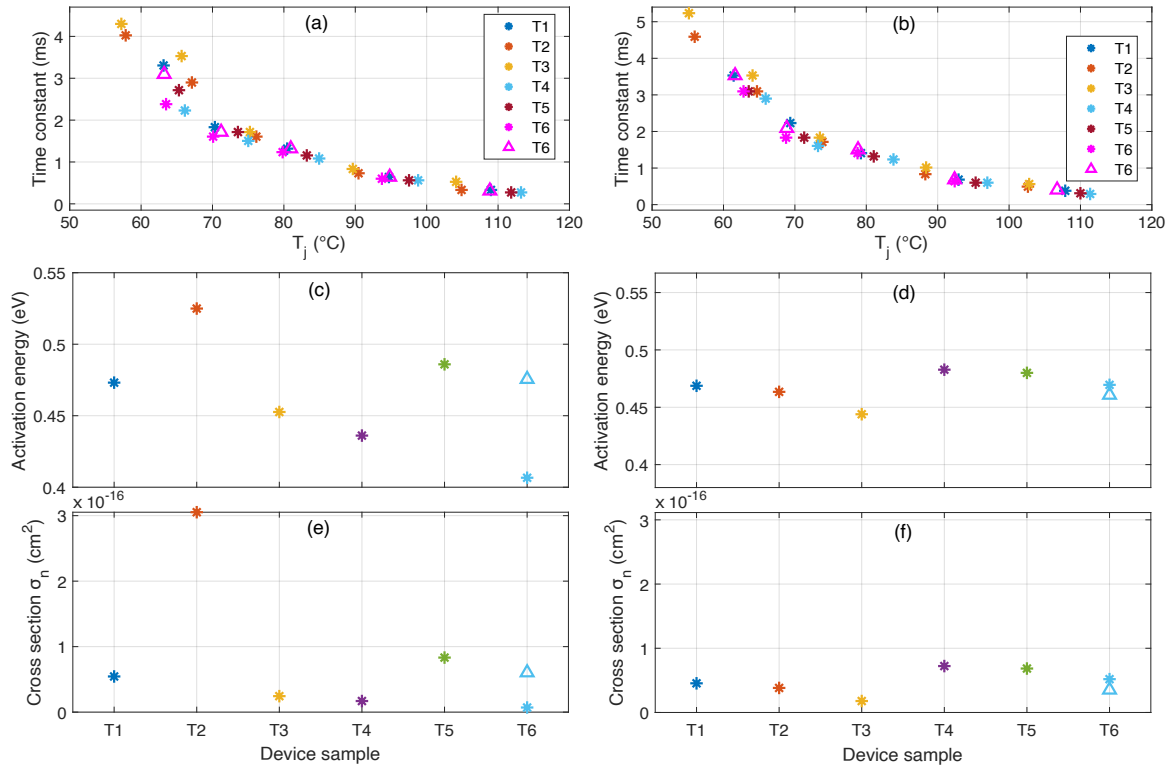

Figure 2.12: (a) Detrapping time, (c) activation energy E_A and (e) cross section σ_n for pulses with $V_{DS} = 50V$. (b) Detrapping time, (d) activation energy E_A and (f) cross section σ_n for pulses with $V_{DS} = 80V$.

for the other devices should then be compared to this one. Since pulses with filling voltage of 50 V were of interest for the characterization, the obtained results are presented alongside the 80 V characterization. As can be seen, some improvements are visible for gate and drain lag in some samples but the correlation with the physical structure, i.e. presence or absence of some layers or different AlGaN composition, is not straightforward. For n_T, a clear improvement is instead observed with respect to T1, obtaining values of approximately half of carrier reduction. Regarding Arrhenius extraction, a single trap signature is identified in all samples, and the corresponding activation energies and cross sections reported in Figs. 2.12(c)-(d) are in agreement with other Fe-doped buffer technologies [93]. Figs. 2.12(a)-(b) report the identified detrapping constants related to the junction temperature T_j corrected taking into account power dissipation and R_{th}. As expected, the increase in junction temperature allows for a faster detrapping, improving performances if only trap effects are considered. E_A and σ_n do not point out a clear winner technology, despite T3 shows promising results. Two identical samples for device T6 were measured and are included in this report, showing consistent results except for the 50 V activation energy in Figs. 2.12(c).

2.6 Buffer-free devices

2.6.1 Overview

As discussed in Sec. 1.1.3, conventional GaN HEMT structures grown on SiC or Si substrates require a thick GaN buffer to minimize structural defects caused by the lattice mismatch with the substrate, thus obtaining a crystal quality sufficient for device performance. Since the as-grown GaN buffer has a low resistivity, its doping with acceptor-like impurities, typically Fe or C, is required to suppress parasitic conduction and ensure buffer insulation. However, as demonstrated in the last section, the intentional acceptors act as electron traps, and therefore a trade-off between dispersion and insulation is usually made. An alternative approach, denoted as 'buffer-free' technology, has been proposed in [94] and [95]. The paradigm is to remove the doped channel and, instead, directly grow over the nucleation layer an unintentionally-doped GaN epitaxial layer of very-high structural quality, serving as the transistor channel layer. This technology was shown to have good performance in RF [96] with the potential to reduce the trapping effects associated with carbon or iron, as no thick Fe- or C-doped buffer is present, reducing leakage currents, and improving electron confinement now enforced by the nucleation layer.

The device, denoted as T2 in Fig. 2.13, is compared to a device with the same top

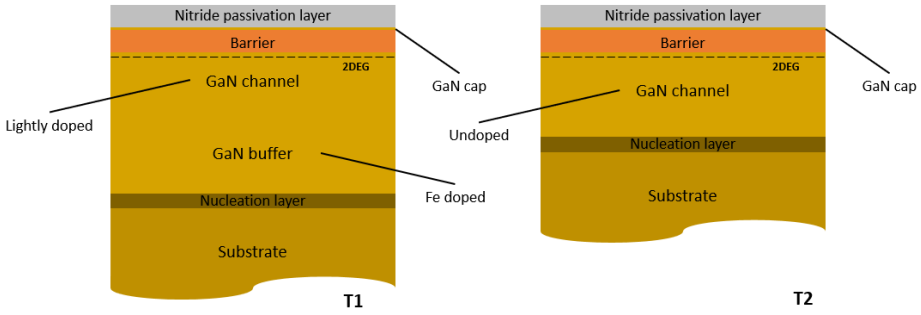

Figure 2.13: Cross section of the two technologies. T1 is the structure of GaN HEMT with Fe-doped buffer, while T2 is the structure of the 'buffer-free' device

layers (T1 in Fig. 2.13). These devices are 0.4-μm-gate-length transistors featuring two 400-μm-long fingers, yielding a total gate width of 0.8 mm. Both are equipped with source-connected field plates. T1 is manufactured on a conventional GaN structure featuring a Fe-doped thick buffer ($\sim$ 1.4 μm) already presented in previous Section. As typical, the iron concentration decreases when approaching the barrier, leaving a lowly-doped high-mobility GaN layer which defines the so-called channel region. The barrier thickness and composition is such to yield a saturation current of 1.2 A/mm. Such an HEMT is further capable of providing about 10 W/mm RF power density at 50 V drain bias when operated in the S-band.

2.6.2 Measurement results

First, a dc characterization is performed, exhibiting similar results obtained for the conventional devices and reported in Fig. 2.2. A small kink effect can be observed for a drain voltage of about 4 V.

The DCT measurements for gate/drain-lag, shown in Fig. 2.14(b), feature a substantially different transient behavior with respect to T1 and reported in Fig. 2.3(b). While the gate-lag transient is comparable to T1 (3% for T1 vs. 1% for T2), the drain-lag transient does not display a steady recovery. Drain lag current evolution, also visible in Fig. 2.15(a) for multiple temperatures, is instead characterized by a prompt current response immediately after the voltage transition, with current levels already comparable to - or higher than - the corresponding static ones (depicted with dashed lines in Fig. 2.15(a)). In the $\simeq 1-10$ μs interval, a slight current increase is measured, followed in the $10-100$ μs range by a subsequent dynamic reduction of the current in the order of 50 mA/mm. The final part of the transient features a recovery with a longer relaxation time with respect to T1. Such a recovery does not fully expire

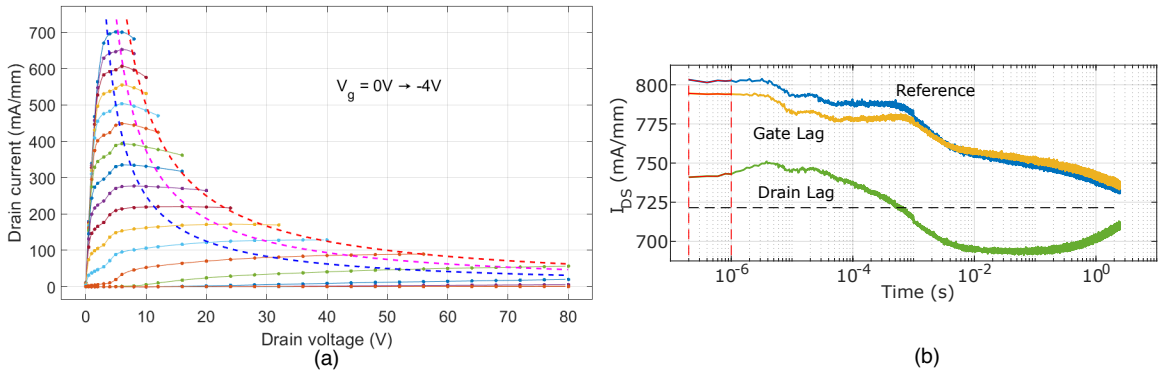

Figure 2.14: (a) DC characterization of buffer-free device. (b) Reference, gate lag and drain lag waveforms obtained from transitions $(V_{GS}, V_{DS}) = (0, 0)$ V $\rightarrow$ $(0, 5)$ V, $(V_{GS}, V_{DS}) = (-7, 0)$ V $\rightarrow$ $(0, 5)$ V and $(V_{GS}, V_{DS}) = (-7, 50)$ V $\rightarrow$ $(0, 5)$ V respectively.

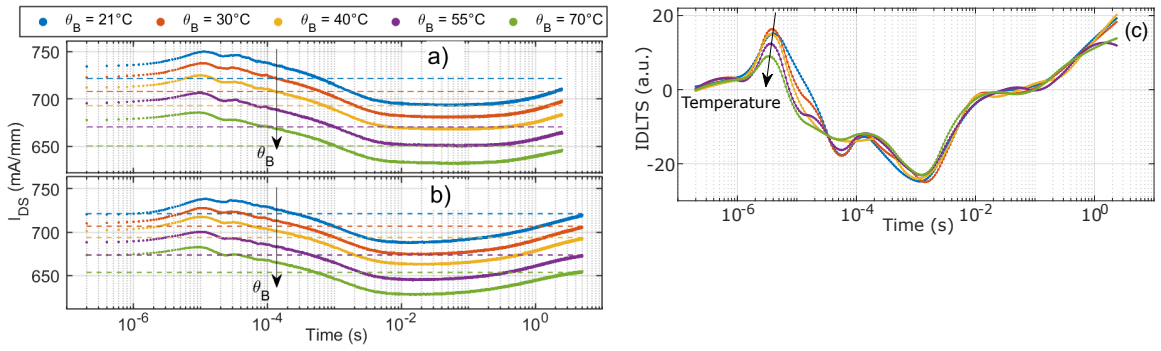

Figure 2.15: DCT measurements of (a) $T = 5$ s; (b) $T = 10$ s period of 'buffer-free' device acquired at baseplate temperatures $\theta_B = 21°\text{C} - 70°\text{C}$. The same voltage transition applied for all temperature is $(V_{GS}, V_{DS}) = (-7, 50)$ V $\rightarrow$ $(0, 5)$ V. Dashed lines indicate the corresponding static values from dc. (c) Extraction of time constants.

for the case with $T = 5$ s (Fig. 2.15(a)), while it is shown to reach the static value when using $T = 10$ s (Fig. 2.15(b)).

This specific behavior fundamentally impacts the nominal value of the drain-lag metric, which results in 7%, a much lower value than for T1. Nevertheless, considering the observed transient behavior, it is worth highlighting that the conventional drain-lag calculation provides rather incomplete information about the trapping behavior of T2. A similar transient behavior has been measured for all different θ_B tested, from $\theta_B = 21°\text{C}$ to $70°\text{C}$ (see Figs. 2.15(a)-(b)). As can be seen from Fig. 2.15(c), the transient relaxation time-constants do not depend on temperature, ruling out any temperature-assisted detrapping mechanisms.

Notably, the non-monotonic behavior of the measured DCT appears to be com-

patible with the dynamic threshold voltage characterization performed in [97] under analogous OFF/ON-state excitation for a thin HEMT featuring a similar ratio between gate-length and channel thickness. While no specific data or interpretation is shown for transient values in the immediate $\simeq 1-10$ μs range, a positive threshold shift is reported in [97] in the $10-100$ μs range for the ON-state transient, which can be linked to the drain current reduction shown here. In addition, [97] also reports a subsequent negative threshold shift in the $1-10$ ms, which can be linked to the slow current recovery shown here.

Since traps may still occur in T2 due to residual structural defects or non-intentional doping during the epitaxial growth, in [97] it is further argued that this non-monotonic transient behavior can be caused by a combination of two trap-related phenomena. The slower effect in the $1-10$ ms can be ascribed to the detrapping of hot electrons due to impact ionization between highly energetic hot electrons and filled levels. These levels are supposed to be slowly filled during the half-period where the device is in the OFF-state ($\frac{T}{2} = 2.5$ s). Conversely, the fast current reduction in the $10-100$ μs range can instead be caused by trapping of hot electrons.

2.7 Conclusion

This Chapter presents a unified experimental framework tailored to the extraction of multiple metrics useful for the characterization of GaN HEMT. Efforts have been made on both the software and hardware sides, tailored to the reduction of the characterization time for each device. About the hardware, the fabrication and optimization of the custom pulser board allowed for excellent results in terms of edge shape, avoiding unwanted overshoots or ringings, and edge rise and fall time, down to 10 ns. This solution can represent a cost-effective alternative to more sophisticated commercial systems, with the advantage of increased flexibility when other characterizations or integration with other systems need to be addressed. This solution comes with some limitations as well that will be addressed in future improvements. The introduction of some safety checks could be implemented to properly verify that the device is working inside its SOA. Erroneous gate/drain voltage configuration or misalignment of the waveforms could quickly kill the device and potentially damage the setup. Another useful feature is the ability to produce double-pulsed waveforms, which have the potential to further highlight trapping phenomena as described in [80].

On the software side, the algorithm was designed to automatically perform the complete characterization thanks to the possibility of remotely controlling all the in-

strumentation. Moreover, starting from the dc characteristic of the device, the extraction of interesting points is automatically performed and proposed to the operator. Since the variation of the baseplate temperature is usually the most time-consuming task, waveforms are organized so that a single temperature sweep is required and the same waveform is employed for the extraction of multiple features.

The method was shown to be robust and flexible for many use cases, as demonstrated from the characterization of new-concept devices with very different electrical characteristics. DCT period was extended up to 10 s and, despite no temperature-correlated trapping effects being observed, valuable information could be derived from the current waveforms themselves. Where possible, a comparison with traditional SPIV measurements has been performed, showing general agreement between the techniques.

Chapter 3

Varactor characterization

3.1 Introduction

The use of varactors in monolithic microwave integrated circuit (MMIC) designs is widespread, and some examples are here reported to highlight the state-of-the-art for this research area. In [98], a programmable gain amplifier is realized in Silicon Germanium (SiGe) bipolar complementary metal-oxide-semiconductor (BiCMOS) technology with multi-band switching capabilities. For this application, operation up to Ka-band has been demonstrated by exploiting an integrated varactor bank. Voltage-controlled oscillators usually make use of such devices, as demonstrated in [99], where a W-band VCO in Gallium Nitride (GaN) technology (60-nm process by OMMIC) is analyzed. In [100], MMIC GaN-on-Silicon Carbide (SiC) HEMTs (0.15-μm process by WIN Semiconductors) operated in a cold-FET topology are exploited as varactors to design variable delay lines for tunable bandstop filters, with demonstrated operation up to 4 GHz. Phase shifters usually take advantage of varactors to provide reconfigurability, as presented in [101] and [102]. For these works, HEMT-based varactors are investigated using GaN-on-SiC technologies, respectively in the Ka-band (0.1-μm process by Fraunhofer IAF) and in the W-band (40-nm process by HRL). Wideband applications, as reported in [103], are possible when the varactor layout can be freely optimized, leading to arrangements with improved linearity performances. What these solutions usually have in common is the reduced power these devices need to undergo due to their location inside the circuit. When the varactor instead targets the power section of an amplifier, all related losses start to heavily impact the efficiency performances.

To properly identify suitable varactor devices offering the required performance in terms of capacitance and parasitics, this Chapter details a comprehensive characteri-

zation procedure applied to multiple devices across different GaN technologies. Given that this Thesis focuses on radio-frequency (RF) power amplifiers (PAs), a detailed analysis in the K- and Ka-bands is also provided. Additionally, custom varactor designs are introduced in Sec. 3.4, aiming to address the limitations of traditional fingered layouts.

3.2 Figures of merit

As a new technology is considered for use as a varactor, three main figures of merit could be extracted from small-signal measurements. This characterization directly impacts the possible use of the device for the target circuit. A low capacitance value could restrict the implementation in load-modulated networks as well as a low quality factor.

Equivalent capacitance

$$C_{eq}(V_{\mathrm{B}}, f) = \frac{\Im\{Y_{21}(V_{\mathrm{B}}, f)\}}{2\pi f} \tag{3.1}$$

Quality factor

The quality factor Q expresses the losses that should be expected from the device when an RF signal is injected. It takes into consideration both the parasitic resistance and the equivalent capacitance. Therefore, when high capacitance is exhibited, i.e. when low absolute bias voltages are applied, the quality factor is expected to be low. Usually, this only quality factor is reported for a given device since it represents the worst performing region for the varactor.

Q value depends from both bias voltage and operative frequency. When a fixed bias is applied, the depletion region is established and does not depend heavily on the frequency. In this case, the parasitics acts in a predominant way, showing the effect on the overall Q. The expression used throughout this work is reported below:

$$Q(V_{\mathrm{B}}, f) = \frac{\Im\{Y_{21}(V_{\mathrm{B}}, f)\}}{\Re\{Y_{21}(V_{\mathrm{B}}, f)\}} \tag{3.2}$$

Tuning Range

As the main property of a varactor is its ability to change capacitance with bias voltage, it becomes important to express the amount of this variation over all bias voltage range. A simple way to express this quantity is by a ratio between the maximum

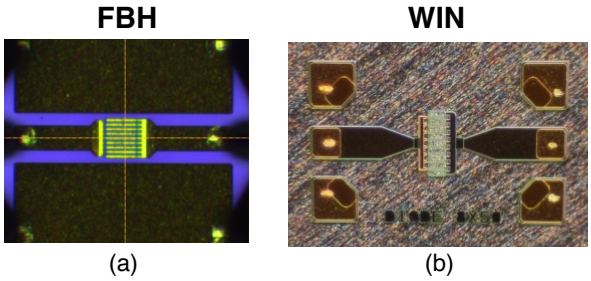

Figure 3.1: Microphotographs of varactor diodes by (a) FBH foundry, (b) WIN foundry.

exhibited capacitance and the minimum one, namely tuning range:

$$\mathrm{TR} = \frac{C_j|_{V_\mathrm{B}^{max}}}{C_j|_{V_\mathrm{B}^{min}}} = \frac{C_{max}}{C_{min}}. \tag{3.3}$$

This parameter can be controlled by changing the size of the overall depleted area of the varactor and is limited by the operating voltage of the device. When operated with large signals, the tuning range should consider the maximum voltage achieved by the bias and the RF voltage, therefore V_B^{min} and V_B^{max} should be carefully evaluated depending on the target application.

Alternative definitions can be provided, like the following [104]:

$$\mathrm{TR} = \frac{C_{max} - C_{min}}{C_{max} + C_{min}} \tag{3.4}$$

which results in a normalized parameter.

3.3 Experimental results

3.3.1 Experimental setup and devices

The diodes under study are realized in two modern GaN-on-SiC MMIC technologies targeting power diode applications up to the K-band. Notably, no optimization is performed in the layout, since the study specifically assess the use of already-available devices for the varactor use. The first one, reported in Fig. 3.1(a) is a planar diode technology with coplanar (CPW) connections in the 150 nm process by the Ferdinand Braun Institut (FBH), while the second one in Fig. 3.1(b) is the 120-nm process by WIN Semiconductors. Despite the technology capabilities, the anode of the diode from FBH is realized with a length of 250 nm, since this characteristic enables the device to support more power. The use of the FBH technology was enabled by a collaboration between the University of Bologna and FBH Institut in Berlin during the three-month

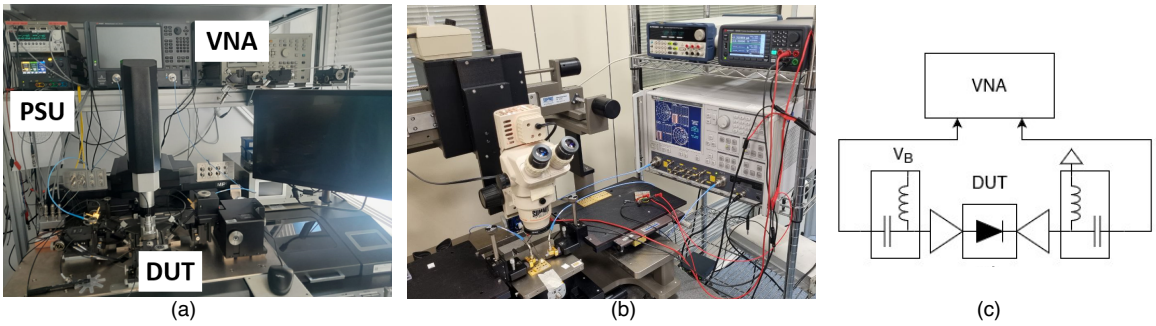

Figure 3.2: Photos of small-signal setups for varactor characterization at (a) FBH and (b) EDM Lab. (c) Schematic representation of the setup.

period abroad. Samples from WIN devices are instead realized custom for this study thanks to the Microwave Engineering Center for Space Applications (MECSA).

The experimental setup required for this characterization consists only of a vector network analyzer (VNA) and a power supply to provide the required bias voltage. Although the current flowing through the device should be negligible, in the order of μA, being able to accurately monitor its value could help to identify both the breakdown voltage and the conduction region. Different VNAs have been used during the Thesis work. Since both technologies comes in a plain wafer without any carrier or connectors, a probe station equipped with two GSG RF probes is also required. For the measurements conducted in the EDM laboratory, a manual probe station was used for the purpose. The data concerning FBH devices were instead acquired with a semi-automated probe station available in the RF Lab of FBH. Photos of laboratory equipment and a schematic representation of the setup are provided in Fig. 3.2.

The devices-under-test (DUTs) are both 2-port on-wafer structures as visible in Fig. 3.1(a)-(b). Port 2 is located between the cathode of the diode and ground and is forced to a 0 V potential through the bias-tee. Port 1, instead, located between the anode of the diode and ground, is used to apply the negative bias voltage V_B. Since V_B is defined as the voltage difference between the cathode and anode terminals, its value is negative to force the device to operate in the reverse-bias region. The small-signal data acquired, i.e. S-parameters, are de-embedded from the connection structures on both ports. Since the layout of the RF pads is different, and so are the de-embedding structures available, two different strategies have been adopted. In particular, the open-short methodology described in Sec. 1.4 is applied to samples from FBH foundry, while the EM de-embedding described in the same Section is exploited for the WIN technology. The intrinsic S-parameter data obtained after this procedure are processed for the extraction of the main FoMs described in Sec. 3.2. The results

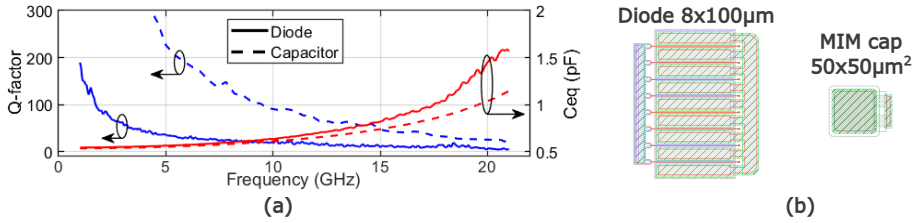

Figure 3.3: (a) Q-factor and capacitance extracted for a 50×50 μm^2 MIM capacitor and a 8×100 μm Shottky diode for bias $V_B = -5$ V in WIN technology. (b) Layouts of the diode (left) and capacitor (right).

are presented in the next Sections.

3.3.2 Comparison with MIM capacitor

As already discussed, minimizing losses is critical in achieving optimal performance in MMICs. Typically, integrated varactor solutions are compared against discrete alternatives; however, this approach is impractical for higher frequency bands, such as C and K bands, where discrete varactor solutions are unavailable. Consequently, this study evaluates the performance of a diode-based varactor by comparing its Q-factor to that of a metal-insulator-metal (MIM) capacitor fabricated within the same WIN MMIC process. The MIM capacitor in this process uses Silicon Nitride (SiN) as the insulating material, which has a dielectric constant of 6.5. Based on the design kit model, a theoretical capacitance of 0.53 pF is obtained for a MIM capacitor with dimensions of 50×50 μm^2. This value serves as the reference point for comparing the performance of the varactor diode. For this purpose, a diode varactor with dimensions of 50×100 μm was selected. It was biased at $V_B = -5$ V in order to exhibit the same capacitance value as the MIM capacitor at the lowest available frequency of 1 GHz.

Figure 3.3(a) illustrates the comparative performance of the MIM capacitor and the diode varactor, highlighting significant differences in their Q-factors across a range of frequencies. At lower frequencies, the capacitor exhibits a superior Q-factor, exceeding 200 for frequencies below 5 GHz, which underscores its efficiency in minimizing losses in this range. In contrast, the Q-factor of the diode varactor is considerably lower in the same frequency range, making it less advantageous for applications requiring minimal energy dissipation at lower operating frequencies. However, as the frequency increases, the gap in performance between the two devices narrows. Beginning at 18 GHz, the Q-factors of both components become more comparable, with the MIM capacitor achieving a value of 32 and the diode varactor reaching 16. This

convergence suggests that, for high-frequency applications, the diode varactor may present a viable alternative to the MIM capacitor, particularly when other design constraints or requirements favor its use. Both devices display a noticeable capacitance drift as the frequency increases, reflecting a deviation from their nominal capacitance values. This drift becomes especially pronounced at higher frequencies, where the capacitance for the diode varactor at 18 GHz doubles its nominal value, while for the MIM capacitor, the capacitance similarly doubles at 20 GHz. This behavior highlights a common limitation in high-frequency performance for both devices, necessitating careful consideration in frequency-sensitive MMIC designs.

In frequency ranges where the losses introduced by the MIM capacitor and the diode varactor are comparable, it can be reasonably concluded that the varactor is a viable candidate for integration into MMIC PA designs. In such cases, the varactor could be incorporated into the matching network, either in series with the RF path or grounded - similar to the typical application of a MIM capacitor - without incurring a significant efficiency penalty. This adaptability makes the varactor a practical choice, provided that its performance aligns with the specific requirements of the design. However, it is important to account for the differences in the RF current handling capabilities and voltage breakdown characteristics of these two devices. For the MIM capacitor, the maximum operating voltage is dictated by its breakdown voltage, which typically exceeds 100 V in these technologies. This high breakdown voltage allows the MIM capacitor to tolerate significant voltage levels without risk of damage, making it robust in high-power applications. In contrast, the diode varactor has inherent limitations due to its susceptibility to self-tuning effects at high input power levels. These effects, caused by the nonlinear characteristics of the varactor, can lead to a shift in its operating point, reducing its effective operating range to voltages well below the theoretical breakdown threshold. This makes the diode varactor less suitable for applications where high voltage handling is critical, as its performance can degrade under such conditions.

3.3.3 Layout considerations

The diode size, intended as the total active area computed as $n_F \cdot W$ where n_F is the number of fingers and W is the finger width, directly influences the performances. As expected, devices with larger size exhibit a higher equivalent capacitance as the area of the 2DEG is greater. At the same time, it is important to also evaluate n_F and W separately as the influence on the losses is different. Fig. 3.4 reports C_{eq} and Q values extracted for three FBH devices of different sizes across frequency. Peripheries

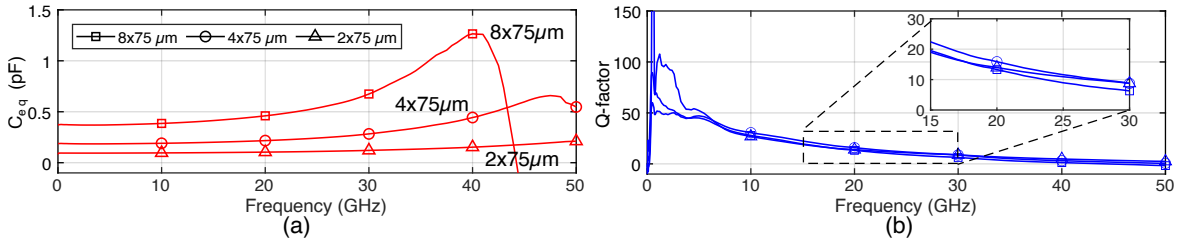

Figure 3.4: (a) Equivalent capacitance and (b) Q-factor extracted at $V_B = -30$ V for 3 devices from FBH with increasing finger number and fixed width of 75 μm

organized as N×75 μm are selected where N is the number of fingers. The lowest bias voltage allowed for the technology is applied, corresponding to $V_B = -30$ V, which also gives the lowest capacitance value that could be realized. As can be seen, a Q-factor lower than 10 is obtained for frequencies above 30 GHz, and further reduces at higher frequencies, reaching values below 5 when going above 40 GHz. Similar performances are observed for the three devices, indicating a weak dependence of losses when modifying the number of fingers. The inset in Fig. 3.4(b) provides a better representation of the performances in the K-band.

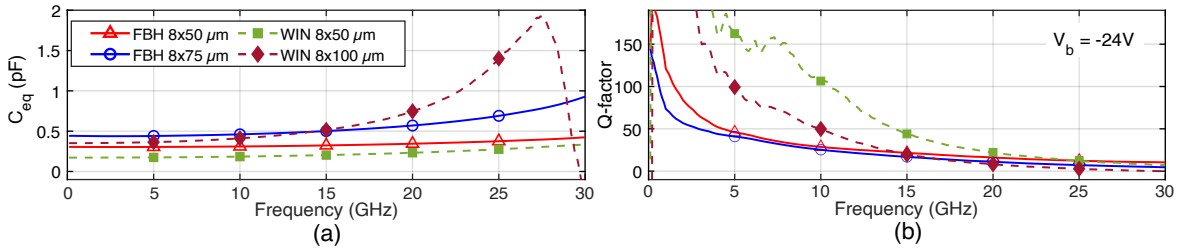

Figure 3.5: (a) Equivalent capacitance and (b) Q-factor extracted at $V_B = -24$ V for two Schottky diodes of size 8×50 μm and 8×75 μm in FBH technology (solid), and for two Schottky diodes of size 8×50 μm and 8×100 μm in WIN technology (dashed).

Fig. 3.5 shows the performance concerning the scaling of the finger length (8-finger devices considered) for both technologies. For the WIN technology, a reduction of 50 μm in finger length entails a reduction of a factor of 3 for the capacitance at 18 GHz, and a concurrent improvement of 17 points for the Q-factor. This is caused by series losses of the relatively thin gate (anode) metal of the GaN diodes, which have a greater impact on longer fingers. The improvement is more pronounced in the X-band, where the Q-factor reaches values of 106 and 50 for the 8×50 μm and 8×100 μm diodes, respectively.

It is worth noting that the larger-sized FBH 8×75 μm and WIN 8×100 μm devices display a larger capacitance variation over frequency, making them unsuitable for

wideband PA designs. Indeed, a capacitance value that is constant across the operating frequency would be preferable in this case. One should also avoid reaching the self-resonating condition, so that the use of, e.g., the FBH 8×75 μm device, could be intended just up to $30 - 35$ GHz. However, a design at these frequencies would result in being too lossy due to the low Q-factor. On the other hand, smaller devices with less active area exhibit lower capacitance values that may not be sufficient for the targeted application.

3.3.4 Evaluation at multiple frequency bands

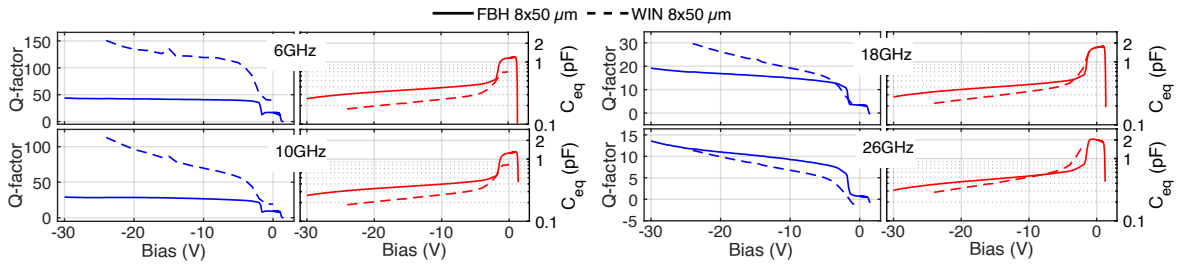

Figure 3.6: Equivalent capacitance and Q-factor extracted at $V_B = -24$ V for two Schottky diodes of size 8×50 μm and 8×75 μm in FBH technology (solid), and for two Schottky diodes of size 8×50 μm and 8×100 μm in WIN technology (dashed).

Fig. 3.6 shows the bias dependency of the varactor capacitance and the respective Q-factors in some relevant bands, from the C-band up to the K-band. FBH diodes are limited to the -30 to 2 V range, while the voltage range for WIN is -24 V and 0 V. All devices show a clear decrease of Q-factor with increasing frequency, but also a general yet slight increase in capacitance. The WIN devices show a superior Q-factor performance in the lower frequency bands (C- and X-band), but their degradation is substantial at 26 GHz, where FBH devices show a positive Q-factor up to 1.2 V.

A low bias voltage creates a narrow depletion region with high capacitance, whereas increasing the reverse bias increases the width of the depletion region, which in turn decreases the capacitance. Furthermore, a low reverse bias voltage is especially sensitive to bias variations because of the steep slope of the capacitance at around -2 V. Moreover, a considerable drop in the Q-factor takes place at low bias values, as shown in Fig. 3.6.

Considering these trends, one can identify two distinct regions of operation for the varactors. The first region corresponds to a bias voltage below -2 V, where the capacitance slowly decays with about a factor 2 with increasing negative bias. The second region lies above -2 V, where the capacitance abruptly changes by a factor of 4

to 6, and then reaches a plateau until the diode starts to conduct at around 2 V. For power applications featuring a large voltage swing over the varactor, the first region is the only feasible one. However, for small-signal operation, one could in principle consider exploiting the two distinct capacitance states, the first with low capacitance and high Q-factor, and the second with up to 3 times more capacitance but a poor Q-factor.

Table 3.1: Tuning range and Q-factor at multiple frequency ranges for FBH and WIN diode technologies, where $V_B = -24$ V for C_{min} and Q_{max} and $V_B = -5$ V for C_{max} and Q_{min}.

Frequency	**FBH**			**WIN**		
	TR	Q_{min}	Q_{max}	TR	Q_{min}	Q_{max}
6 GHz	17%	40	43	25%	109	151
10 GHz	17%	25	29	27%	57	113
18 GHz	19%	13	18	31%	16	30
26 GHz	22%	8	12	41%	5	11

The tuning range for the varactors under test, summarized in Tab. 3.1 for the different bands and technologies considered, can be computed as $TR = (C_{max} - C_{min})/(C_{max} + C_{min})$. For this evaluation, only the region with $V_B < -5$ V is considered, since it is the only feasible one for PAs.

3.3.5 Large signal evaluation

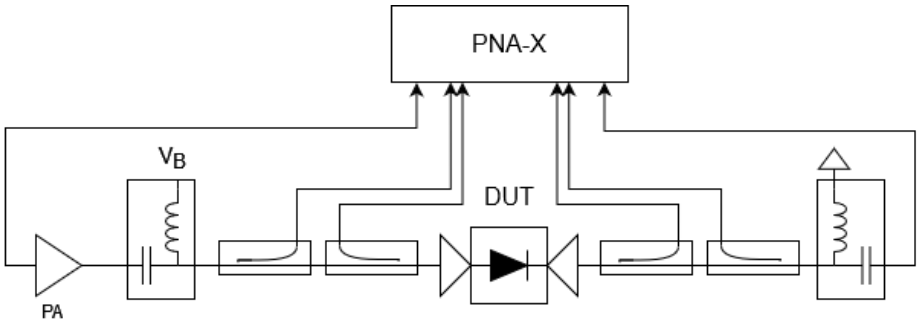

Figure 3.7: Setup adopted for the large-signal characterization.

The evaluation of the large-signal behavior allows assessing the impact of self-tuning at high power levels, which is of particular importance when the diode device is placed in series with the output signal [105, 106, 107]. For this characterization,

a VNA from Keysight (PNA-X) is adopted and the setup schematic is reported in Fig. 3.7. The RF power has been calibrated up to the probe input and the impact of the probe is considered by embedding its S-parameters. Both input and output impedances are therefore 50 ohm for every harmonic.

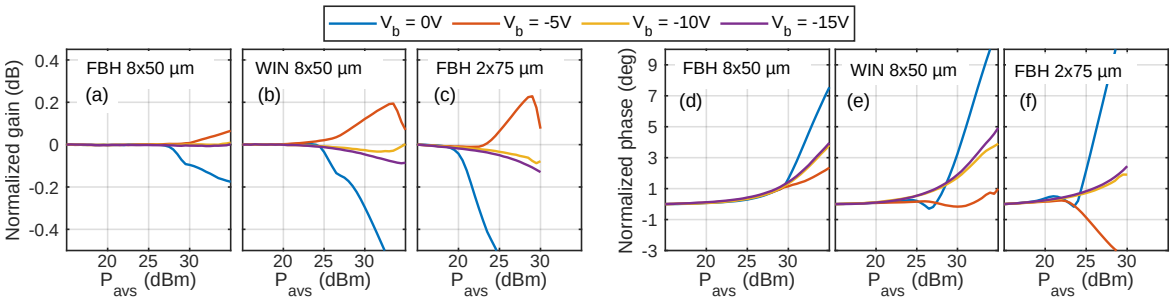

Figure 3.8: (a)-(c) AM/AM and (d)-(f) AM/PM normalized characteristics for three Schottky diode devices extracted at 18 GHz for multiple bias voltages.

The normalized gain (AM/AM) and phase (AM/PM) characteristics at 18 GHz are reported in Fig. 3.8 at multiple bias voltages for the 2×75 μm and 8×50 μm devices from FBH, as well as for the 8×50 μm device from WIN. Some level of compression effects are present, with up to 7 degrees phase deviation when the diodes are biased at 0 V. The impact of de-tuning at other bias voltages remains rather constant as the input power is increased, and only a small compression is observed.

3.4 Island varactors

In order to improve the varactor performances, the impact of parasitic resistances needs to be minimized. In traditional devices based on a fingered structure, this is usually achieved by reducing the finger length or increasing the finger number, as explored in the last Section. However, both methods present drawbacks that limit the amount of resistance reduction expected. Increasing the number of fingers creates challenges in controlling the path of the RF signal inside the device when the finger count is greater than 8. The middle fingers tend to be more stressed by the RF power, and the advantage of introducing more fingers becomes modest. Special layout optimization strategies should be employed. On the other hand, reducing the width of the fingers also reduces the power capabilities of the device, hence worsening the self-tuning effects.

A new Schottky diode design is presented here, aimed at mitigating the described limitations. The design is realized and fabricated in collaboration with FBH using their 250 nm GaN-on-SiC process. The new concept involves transitioning from the

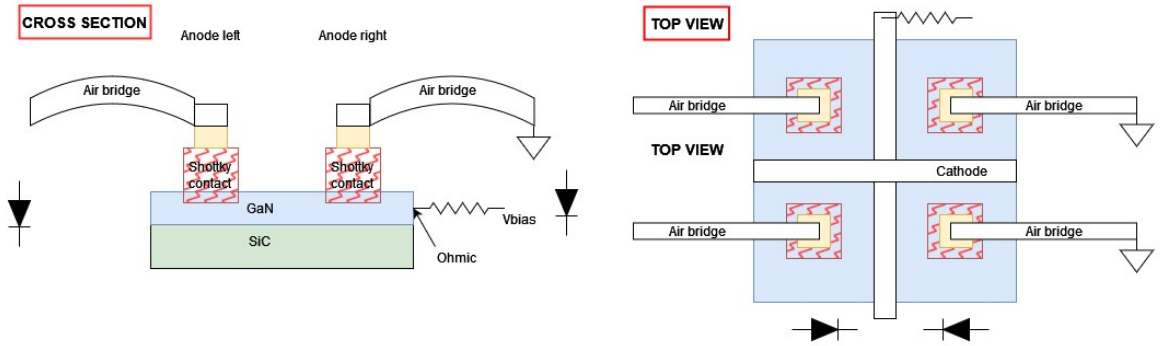

Figure 3.9: Schematic representation of 2x2 island varactor cell.

traditional fingered layout to island layouts, where the Schottky contact is square, and the GaN layer completely surrounds it. The proposed layout is illustrated in Fig. 3.9, which provides a schematic representation of both the cross-section and top view. Although the literature on similar devices is quite limited, some examples have been reported for MOS island varactors designed with the same objective of improving the Q-factor [108, 109]. Another study in [110] shows promising results for Schottky devices grown on SiC substrates, where a similar structure is proposed, utilizing multiple cells and bonding connections to the anode metal to improve overall capacitance.

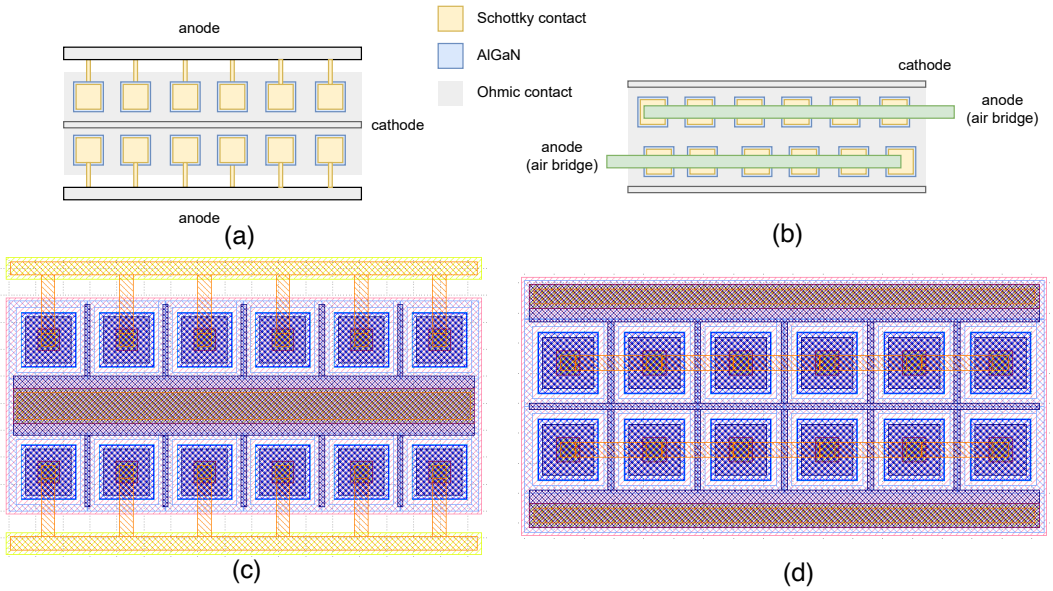

Figure 3.10: Schematic representation of island varactor structures connected in (a) parallel and (b) series. Layout of (c) parallel and (d) series structures.

With this configuration, the depletion region is distributed across four edges instead of only two, which, in principle, reduces the parasitic resistance introduced by each finger. Since diodes in anti-series configurations are commonly employed in PAs, im-

plementing a device that inherently provides this configuration allows for a reduction in both the occupied area and the associated parasitics derived from interconnections. This approach is combined with the implementation of multiple islands to increase the overall junction capacitance exhibited. However, since the overall area and the edge length scale differently, designing large islands does not necessarily contribute to size optimization. Instead, deploying multiple cells over the same GaN channel layer is preferable and can be addressed in various ways. One strategy involves contacting the center of the island element from the side, forming a small channel that connects all the anodes to a single external line. This solution is illustrated in Figs. 3.10(a) and (c). An alternative, shown in Figs. 3.10(b) and (d), entails creating two rows where each cell is connected to the next via metalization bonding. This latter approach could theoretically result in increased losses due to the series connection of islands, as opposed to the parallel configuration previously discussed. In both cases the limitation lies in the capability of the process to realize small areas of gate metal used to form the Schottky contact. For these devices, the internal area is a square with 20 μm edge with an additional 0.2 μm of recess on top surrounding AlGaN. Additionally, on the cathode connection, which is realized with ohmic contact, a resistor with a value of 2 kΩ is inserted to decouple the RF path. No current is expected to flow through this bias feed, as only a voltage potential is required to establish the depletion region. It should be noted that the conceptual sketch shown in Fig.3.10(a)-(b), which depicts the structure and dimensions of the cells, is translated into the final layout in Figs.3.10(c)-(d). This translation is performed by designers from FBH, who validate the required tolerances and ensure the minimal realizable area for each cell.

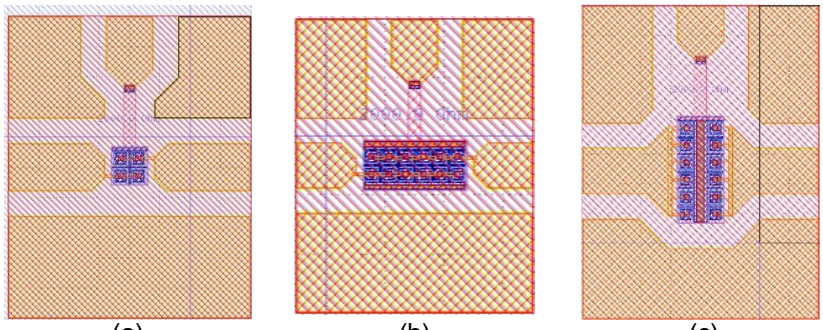

Figure 3.11: Complete island structures from layout with pads for measurement. (a) Basic 2x2 cell; (b) series structure; (c) parallel structure. The top connection is only meant for providing bias voltage and includes a series resistance of 2 kΩ.

The realized samples are shown in Fig. 3.10 and include a simple 2x2 structure (Fig. 3.10(a)), a 2x6 structure with the cells in each row connected in series

(Fig. 3.10(b)), and a 2x6 structure with parallel connections (Fig. 3.10(c)). Preliminary results have been extracted from some samples to initially verify data consistency between different devices with the same layout. Given that the layout implemented here differs significantly from standard diode designs, there is no guarantee that the manufacturing process will yield a fully functional device. Liftoff problems may arise when closed metal areas, such as those in this design, prevent the metalization from fully adhering to the underlying layer. DC characterization was also conducted initially, with no issues observed. Results are reported in Fig. 3.12 where very good

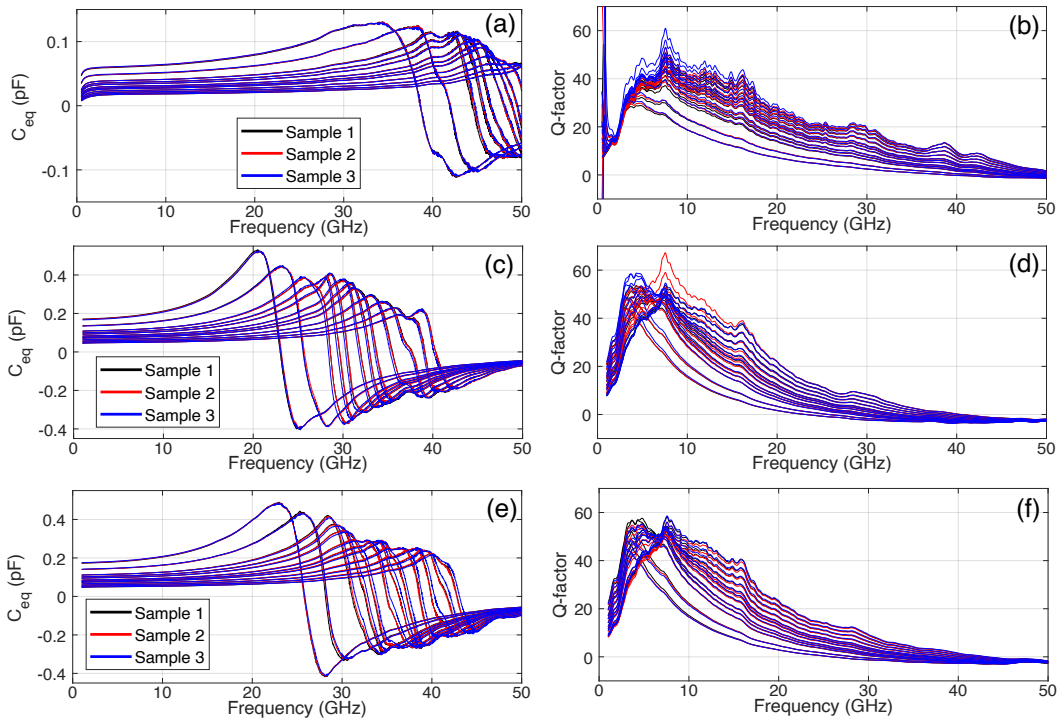

Figure 3.12: Equivalent capacitance and quality factor for multiple bias voltages of (a)-(b) 2x2 island structure; (c)-(d) 2x6 series structure; (e)-(f) 2x6 parallel structure.

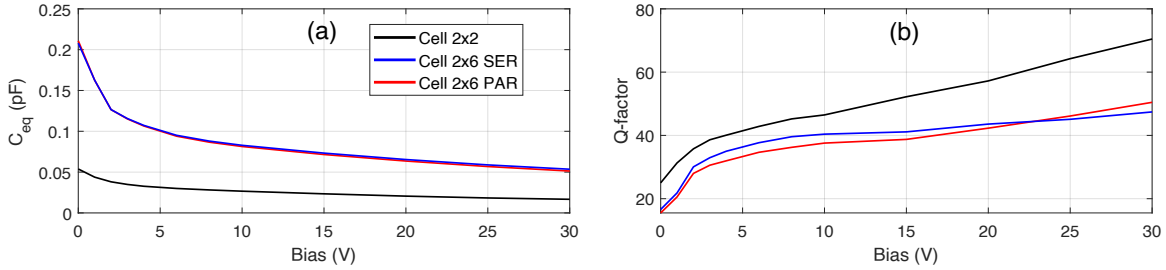

Figure 3.13: (a) Equivalent capacitance and (b) quality factor for all structures extracted at 10 GHz for full bias range.

agreement is demonstrated for all the samples. Clearly, the applied bias voltage V_B

spanning -30 V to 0 V has an impact on C_{eq} that demonstrates the effective tunability of the device. Despite the obtained TR is about 40% at 10 GHz, the absolute maximum capacitance obtained is 0.11 pF at the lowest useful bias of 2 V. In Fig. 3.13 a performance comparison for the three structures is reported, where very good agreement is observed for the 2x6 cells both for C_{eq} and Q. The smaller 2x2 cell exhibits a 3.3 times lower C_{eq} at 4 V, resulting in a slightly higher reduction if the theoretical value of 4 is considered. The 2x6 structures, involving 12 cells, should exhibit a 3-times higher junction capacitance with respect to the 4 cells present in the 2x2 structure. Parasitic capacitances due to connections could influence this ideal scaling adding a fixed contribute to the overall capacitance. Furthermore, no evident impact in Q value seems to be added by the bonding metalization as comparable values are observed at this frequency.

3.5 Conclusions

In this Chapter, a detailed analysis of multiple integrated Schottky diodes in GaN-on-SiC technology is presented. The characterization aims to evaluate the potential of these devices as tunable elements in MMICs, specifically in PAs operating at microwave frequencies. Their absolute performance is compared to measurements of an integrated MIM capacitor fabricated using the same technology. Since the study focuses on devices already available within a given technology, comparing them to a fixed capacitor commonly used in circuit designs can encourage designers to accept a certain level of increased losses in exchange for reconfigurability.

Since the PA topology and target application heavily affect the amount of capacitance required, particularly depending on the frequency application, the study is replicated on many devices with the same finger structure but different organization, and the effects of increasing the finger number or the finger width is discussed. Results highlight that different effects could be expected when different technologies are considered, despite the finger organization evaluated being similar. For some layouts, increasing the number of fingers or the finger width does not directly implies a degradation in performances, therefore the evaluation of bigger devices to provide more capacitance is an option.

Given the importance of self-tuning effects, large-signal characterizations of varactors are important. In this Chapter, a preliminary large-signal characterization is provided to display the deviations from the nominal behavior. Despite some insights could already be inferred, a more accurate measurement campaign is planned, possibly

including active load-pull setups and harmonic tuning.

New devices fabricated at the FBH Berlin foundry facility are also presented, designed with the objective of reducing the parasitic resistance of the diode and thereby increasing the Q-factor. Although the new layouts differ significantly from traditional fingered diodes, their effective operation and tunability properties are demonstrated, and characterization up to 50 GHz is performed. Since the devices are relatively new at the time of writing, only basic characterizations are presented here, with a more comprehensive analysis of both S-parameters and large-signal measurements to follow. After this initial technological assessment, further layout improvements may be proposed and implemented in a subsequent foundry run.

As a main outcome, this research suggests that this technology is sufficiently mature to be employed as a tunable element in reconfigurable MMIC PAs. Optimizations remain possible to further enhance performance, particularly for anti-series structures, where improvements could lead to reduced losses and increased linearity. Additionally, new layouts could be explored to address specific design challenges, such as minimizing parasitics or improving integration with existing MMIC processes. These advancements would not only extend the applicability of this technology in high-frequency applications but also provide valuable insights for extending its use in next-generation reconfigurable RF systems.

Chapter 4

Varactor Modeling

4.1 Introduction

A common challenge in microwave engineering is handling the complex frequency-dependent behaviors of circuits, often represented through scattering parameters (S-parameters), impedance, or admittance data. These behaviors can exhibit rapid variations over frequency, necessitating precise yet computationally efficient modeling techniques [111]. The first step in the characterization of new devices is the acquisition of S-parameters data sampled at discrete frequency points. These S-parameters are usually obtained through vector network analyzer (VNA) measurements. Nonlinear measurements obtained from nonlinear vector network analyzer (NVNA) could also be exploited for the extraction of voltage and current waveforms, mandatory for the validation of nonlinear models [112]. Once extracted, these network responses are integrated into the full PA simulation to properly tune the components and optimize the circuit through time-domain simulations due to the nonlinearities involved [113].

To carry out this type of simulations, two approaches could be adopted, namely convolution and macromodeling methods [114]. The first one requires the simulator to transform the time-domain waveform into the frequency-domain to evaluate S-parameter data and then back again to the time-domain with inverse Fourier transform. If a macromodeling-based method is used instead, S-parameters are first approximated by a rational function, which can be represented in forms such as polynomial ratios, pole-residue pairs, or state-space descriptions. In this form, the circuit simulator is more efficient in the convolution of the desired impedance. It is then preferable to adopt the latter representation to speed up the simulation time.

This chapter is focused on the modeling of Schottky diodes, already characterized in the reverse-bias region to target the use as varactors in Chapter 3. Conventional

methods utilize manufacturing data to characterize all the physical phenomena within the depletion region, contact/pad parasitics, and leakage effects [115, 3, 55, 4, 116]. These phenomena can be effectively modeled using equivalent-circuit models, which derive their topologies and components directly from the device's physical properties. This approach requires an accurate understanding of the manufacturing process as well as technical properties of the substrate like the sheet resistance value or, in some cases, carrier mobility. Moreover, parameter identification methods may utilize specialized experimental setups [3] or standard multibias S-parameter measurements coupled with optimization-driven extraction algorithms [4]. These methods could result in being time-consuming as multiple steps between different software could be required.

When commercially-available devices are evaluated, designers could have limited access to physical properties of the technology, limiting their ability to create a suitable varactor model if not provided by the foundry. This is also true for MMICs where, depending on the maturity of the process or the trade agreements, some physical parameters could only be implemented in the block modeling the component. Additionally, varactors might be implemented using different layout strategies or include multiple diodes connected in various topologies to improve performance [117], thereby complicating the description of the physical effects involved. Given these aspects, varactors and related models are not often available in MMIC process design kits (PDKs) and have to be developed on a case-by-case basis, e.g., starting from the model of the HEMT device [116].

Behavioral models, in contrast to physical models, do not require detailed knowledge of the device layout, offering a generalized approach that is inherently adaptable to any varactor topology. Despite their reliance solely on empirical data, these models can be effectively implemented as equivalent circuits, which demonstrate reliable convergence behavior in computer-aided design (CAD) tools. Additionally, they inherently support features such as scalability with layout parameters, making them particularly versatile for a wide range of applications.

Building on these principles, this Chapter introduces an innovative two-step methodology for automatically generating equivalent-circuit representations for various varactor diodes and structures. First, classical extraction methods are discussed in Sec. 4.3.1 where the basic building blocks of the model are analyzed. Conceptual steps are graphically represented in Fig. 4.1. The process begins with the extraction of a rational function from multibias S-parameter data as detailed in Sec. 4.3.1. Following this, the rational function is converted into a network representation through an automated synthesis process, as described in Sec. 4.3.2. Finally, the complete modeling

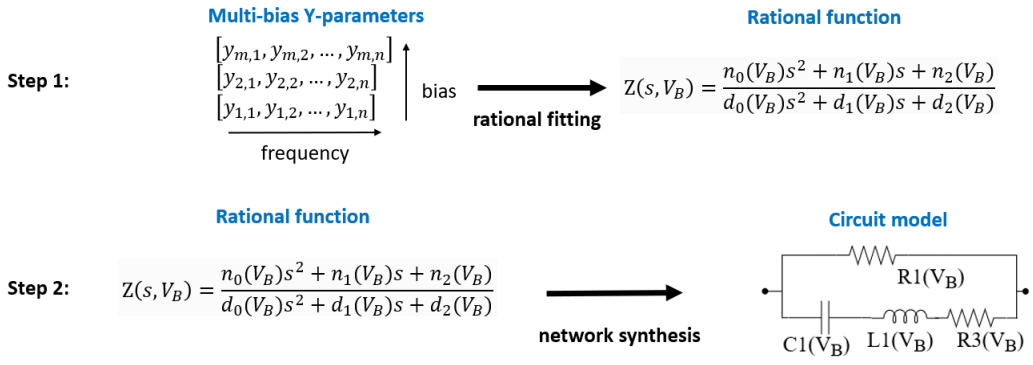

Figure 4.1: Conceptual steps of the proposed modeling procedure. Step 1 is summarized as the rational fitting procedure while step 2 consists on the network synthesis starting from the rational function extracted.

framework is validated by applying it to multiple GaN Schottky diodes and related structures fabricated using the same device technology, with the results and insights presented in Sec. 4.4. This work has been accepted for publication in the Transactions on Microwave Theory and Techniques (TMTT).

4.2 Traditional modeling approaches

This section provides an overview of the modeling techniques adopted for integrated varactors. This step is crucial to critically assess the outcome of the network synthesis in Sec.4.3.2 and to highlight possible strengths and weaknesses of the proposed method.

The invariant for all varactor models in the literature is a basic core constituted by a nonlinear capacitor and a nonlinear resistor in series, modeling the varactor exhibited capacitance and losses respectively. An additional resistor, usually with large values in the 100 kΩ - 1 GΩ range, is added in parallel to account for the parasitic losses observed at dc. Two varactor networks are reported in Fig. 4.2 from [3] (Fig. 4.2(a)) and [4] (Fig. 4.2(b)) where the fundamental core is visible along with elements that model the losses. Indeed, the networks are also similar for packaged solutions [115] where the parasitics from the package mainly influence the linear components that model the access structures. To better address components during the description of the extraction procedure, the simplified model in Fig. 4.3 will be used as a reference.

Multi-bias S-parameters are first considered for the extraction of parasitics, and the common assumption is that at low frequencies (around MHz) capacitances dominate the effect of inductances [115, 4], therefore L_{ser} is transparent during this step. Moreover, at very low bias voltages, the resistor in series with the junction capac-

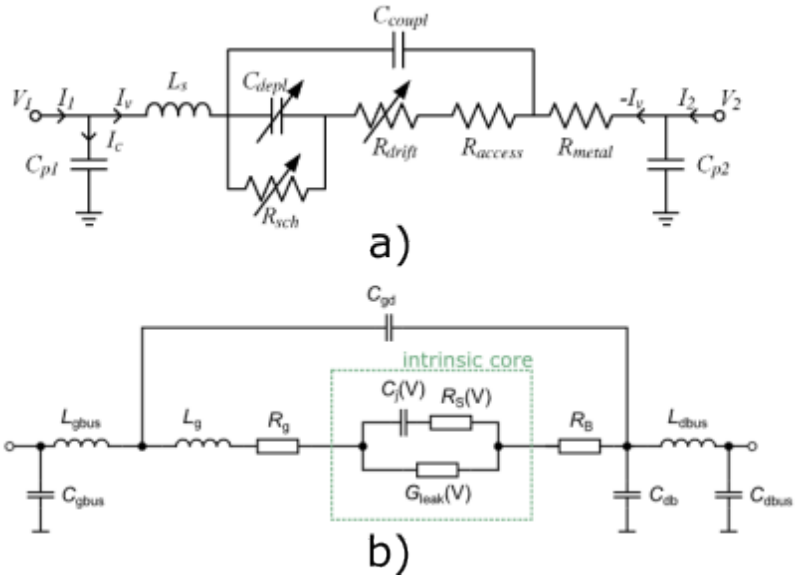

Figure 4.2: Equivalent-circuit topologies for Schottky diode varactors reported in a) [3] and b) [4].

itor $R_S(V)$ is considered negligible. Building on this, principal capacitors could be evaluated for each bias voltage tested. Since the model includes a series LC (realized with L_{ser} and $C_j(V)$), the resonant frequency of the structure can be exploited for the extraction of losses introduced by $R_S(V)$. Instead, the value of $R_{\text{leak}}(V)$ is usually obtained by dc measurements. In some cases, voltage and current sources can be inserted in the model, replacing $C_j(V)$ component to address large-signal operations [115, 4]. The presented extraction strategy makes use of wideband measurements to properly identify both low-frequency effects and the high-resonant frequency, restricting the possible applications to single devices or, at most, highly integrated anti-series structures. In addition, an optimization step could be required to properly identify the elements excluded from this extraction [4].

4.3 New Behavioral modeling approach

4.3.1 Rational fitting

Many rational fitting algorithms are available in the literature, being optimized for different application goals. RKFIT algorithm [118] makes use of Krylov-based approach for solving nonlinear rational least squares problems; AAA algorithm [119] was recently presented which makes use of rational barycentric representations for the extraction of the rational fitting; vector fitting (VF) [120] algorithm was first presented

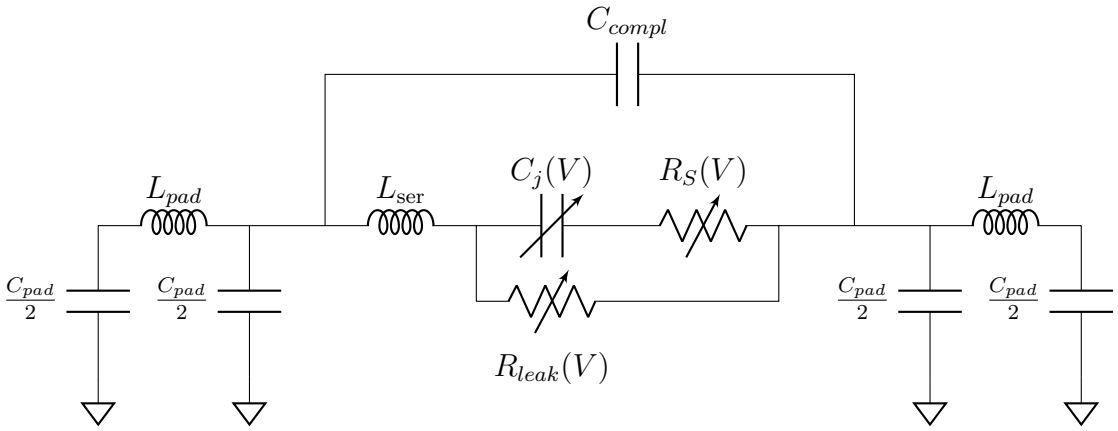

Figure 4.3: Example of minimal network for varactor diode extracted from literature.

in 1999 and it is widely documented in literature for the modeling of passive networks like filters [121, 122] or coplanar connections [123]. For the application considered in this work, VF extraction results in being sufficiently stable and flexible to be adapted to the varactor measurements. The other presented methods have also been tested on the available data obtaining similar results. The time required for the fitting to be performed does not result in any preferred algorithm since the very low number of poles required for varactor modeling.

VF generates a rational function of the form

$$W_{\text{VF}}(s) = \sum_{n=1}^{P} \frac{r_n}{s - p_n} + D + sE; \tag{4.1}$$

so that its restriction to the imaginary axis $W_{\text{VF}}(j\omega)$ closely approximates a given (measured or simulated) harmonic response function $W(\omega_k)$ at a discrete set of K positive frequencies $\omega_1 \ldots \omega_K$. The P complex values p_n and r_n are referred to as poles and residues, respectively. Residues in particular appear as either purely real numbers or as complex-conjugate pairs. D and E are instead purely real parameters. VF is particularly well-suited for approximating the transfer functions of electrical circuits as the elements of the immittance (i.e., either impedance or admittance) matrix of a passive linear lumped-component network, which are known to exhibit the functional form in (4.1) in the Laplace domain [124]. In these cases, the VF coefficients (p_n, r_n, D and E) are directly related to the values of the capacitance, inductance, and resistance of the network's lumped components. It is worth noting that D and E terms can be selectively excluded during the fitting process. Users have the flexibility to force both D and E to zero, to include only the constant D while setting $E = 0$, or to incorporate both constants into the fitting procedure. Since each term introduces additional network elements, this flexibility is important when the complexity of the

final network is considered.

Starting from the measured frequency response function, the VF algorithm can be used to fit models of variable complexity by changing the number of terms in (4.1), with higher fitting accuracy expected as the model order increases. In this work, the order of the VF model is described through the triplet of integers (P, Q, R), where P is the number of poles and $Q, R \in \{0, 1\}$ describe the absence or presence, in the fitted expression, of the terms D and E, respectively.

The rational fit in the form (4.1) is exploited for representing the varactor device as one-port element. Due to the nonlinear nature of varactors, the fitting procedure is applied at the small-signal frequency-domain measurements of the varactor at different dc bias voltages, resulting in the following impedance representation:

$$Z_{\mathrm{VF}}(s, V_{\mathrm{B}}) = \sum_{p=1}^{P} \frac{r_n(V_{\mathrm{B}})}{s - p_n(V_{\mathrm{B}})} + D(V_{\mathrm{B}}) + sE(V_{\mathrm{B}}); \tag{4.2}$$

where V_{B} is the dc voltage difference between the anode and the cathode. The fitting in (4.2) explicitly shows that nonlinear one-ports such as varactors, as opposed to the standard linear case in (4.1), require bias-dependent VF parameters describing the local behavior of the linearized circuit across frequency. Due to the focus on varactor applications, V_{B} is limited to the reverse-bias voltage region, here resulting in $V_{\mathrm{B}} \leq 0$, where negligible conduction current is observed.

In principle, the model complexity required to closely fit measured frequency-domain data could result in being different at the different bias voltage points. For example, impedance functions at different V_{B} could generally require a different number of poles for an accurate fit, making P dependent on V_{B}. Without loss of generality, this work instead assumes that the varactor small-signal data can be closely approximated with a VF of fixed complexity at all bias voltages. In turn, this fixed model order has to be selected by empirically evaluating the approximation error of VF at different bias voltages and complexities, choosing the (P, Q, R) set that provides a suitable fitting for the whole voltage range of interest.

After VF is applied to the measured small-signal data, the result is a bias-dependent rational function representing the impedance function in the Laplace domain. While it is possible to directly implement this type of behavior using bias-dependent poles and residues [125, 126], the resulting block-diagram implementation does not generally lead to a straightforward equivalent-circuit topology for the varactor. Instead, specific network synthesis techniques have to be adopted in order to realize a linear equivalent circuit that displays a one-port impedance equal to $Z_{\mathrm{VF}}(s, V_{\mathrm{B}})$ at the bias V_{B}.

4.3.2 Network Synthesis

A generic scalar rational function $Z(s)$ in the form of

$$Z(s) = \frac{b_0 s^m + b_1 s^{m-1} \dots b_{m-1} s + b_m}{a_0 s^n + a_1 s^{n-1} \dots a_{n-1} s + a_n}, \tag{4.3}$$

where a_i and b_i are real constants, can represent the impedance of a one-port linear passive network under certain conditions [124]. In order to have an implementation with only positive-value elements, the function should be rational and positive real (PR). For the latter to hold, some conditions need to be satisfied:

1. the function must be analytic in $\Re\{s\} > 0$, i.e. $Z(s)$ has no poles in the open right-half s-plane;
2. $\Re\{Z(s)\} > 0$ if $\Re\{s\} > 0$
3. $Z(s)$ is real for real s

If the rational function is derived from VF procedure, these constraints can be automatically imposed [127] so that any fitted impedance function resulting from VF is guaranteed to be realizable as a passive linear lumped component network. In the specific case of the bias-dependent impedance of the varactor in (4.2), the resulting synthesized network will be bias-dependent as well.

Classical passive network theory provides several well-established methods for synthesizing circuits from a given PR impedance function in rational form [124, 128, 129]. Initially, the term $sE(V_\mathrm{B})$ in (4.2), only present if a model order with complexity $R = 1$ is selected, can be realized directly as a series inductor with value $E(V_\mathrm{B})$. The remaining terms, representing a general impedance in series with the previously extracted inductor, can be arranged as the ratio of two polynomials of degree P:

$$Z_\mathrm{VF}(s, V_\mathrm{B}) = \prod_{n=1}^{P} \frac{s - z_n(V_\mathrm{B})}{s - p_n(V_\mathrm{B})} + sE(V_\mathrm{B}). \tag{4.4}$$

The product in (4.4) is known as a P-th order function (e.g., 2-nd order or biquadratic for $P = 2$, 3-rd order or bicubic with $P = 3$, etc.), with P poles p_n and P zeros z_n.

Brune was the first to demonstrate that any PR function can be realized as an RLC circuit and proposed a specific method for synthesizing an RLC impedance function, now known as Brune synthesis [130]. The process begins with some preliminary steps to transform the given PR function into a minimum-reactance and minimum-susceptance form. A function is considered minimum-reactance if it has no poles on the $j\omega$-axis and minimum-susceptance if it has no zeros on the $j\omega$-axis. Following this

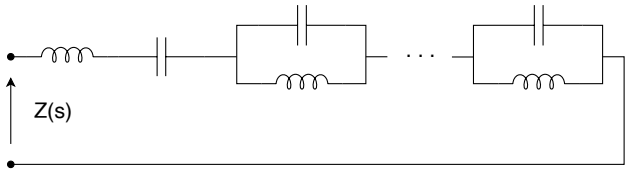

Figure 4.4: Network example of Brune synthesis.

preparation, the synthesis strategy involves systematically removing pairs of poles and zeros on the $j\omega$-axis, a step referred to as the Foster preamble. This process continues iteratively, reducing the degree of the function by two at each step, until a constant remainder is obtained. An example outcome of the resulting network is in Fig. 4.4. If this straightforward procedure fails to hold, a different approach must be applied resulting in negative-value elements, typically a negative inductor. One solution for dealing with such negative elements is to transform a T-topology of inductors into an equivalent ideal 2-port transformer. The total number of circuit elements generated through Brune synthesis corresponds to the number of coefficients in the PR function, i.e. Brune network extraction is canonical. The possibility of using transformers or negative RLC components in the equivalent circuit of the varactor can be tolerated in terms of a purely empirical description, as long as it guarantees good approximation performance, but it is certainly unsatisfactory from a physical adherence standpoint.

Since transformers are not desired when a PR function is synthesized, Raoul Bott and Richard Duffin propose a synthesis technique that does not require transformers or negative elements in the final network. The Bott-Duffin (BD) [124, 128] synthesis method allows to implement any P-th order impedance function as a lumped finite RLC-network, but typically results in an exceedingly large number of reactive elements, i.e. BD realization is not canonical. For example, for a general biquadratic function ($P = 2$), corresponding to a second order state-space model, the minimum number of energy storage and resistive elements deriving from the BD synthesis is respectively 5 and 2 [131]. The algorithm requires the function to be minimal, that is for a frequency ω_0 it hold that $\Re\{Z(j\omega_0)\} = 0$. If this is not the case, a resistor could be extracted with value $\mathrm{R}_0 = \Re\{Z(j\omega_0)\}$ resulting in a series resistance with the rest of the network. The extraction is then performed on the function $Z^{\min}(s) = Z(s) - \mathrm{R}_0$. The Richard's theorem is the applied considering a function $R(s)$ computed as:

$$R(s) = \frac{kZ(s) - sZ(k)}{kZ(k) - sZ(s)}. \tag{4.5}$$

It results that, for all real positive values k, $R(s)$ is PR if $Z(s)$ is PR. Extracting $Z(s)$

from the expression above results in:

$$Z(s) = \left(\frac{R(s)}{Z(k)} + \frac{k}{sZ(k)}\right)^{-1} + \left(\frac{1}{Z(k)R(s)} + \frac{s}{kZ(k)}\right)^{-1}. \tag{4.6}$$

As Eq. 4.6 represents an impedance, the sum indicates the two elements inside parenthesis can be placed in series to obtain the global expression $Z(s)$. Moreover, the terms $\frac{k}{sZ(k)}$ and $\frac{s}{kZ(k)}$ are indeed an inductor and a capacitor, respectively. The network can be configured as in Fig. 4.5 where $Z_1(s) = Z(k)R(s)$ and $Z_2(s) = \frac{Z(k)}{R(s)}$. A pair of

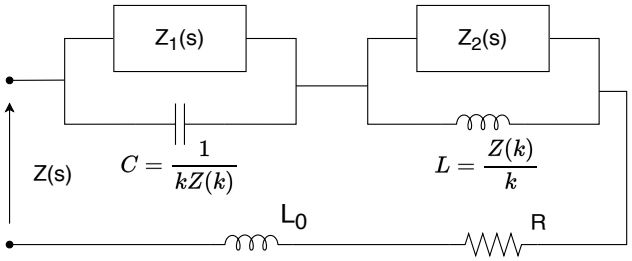

Figure 4.5: First step of the Bott-Duffin synthesis procedure. $Z_1(s)$ and $Z_2(s)$ denote two networks having lower complexity than $Z(s)$

critical frequencies on the $j\omega$ axis is then extracted from each of the two new PRFs $Z_1(s)$ and $Z_2(s)$ each realized as a resonant circuit. The procedure is repeated up to the point where $Z_1(s)$ and $Z_2(s)$ are constants, therefore implementable as dissipative elements, or have a degree less than 2.

Other classical synthesis techniques, such as Brune's [129] or Darlington's methods [128], require fewer elements (down to the theoretical minimum $2P$ for a P-order impedance), but make use of transformers in the resulting circuit.

The large number of elements required by the general BD synthesis of low-order impedance functions has driven recent research efforts to find specific compact circuit implementations for the cases of $P \leq 3$, under the hypothesis that the impedance functions display certain specific properties [132, 133, 134]. In particular, the work in [132] provides a minimal synthesis for all bicubic impedances containing three or less energy storage elements and displaying a series-parallel structure. These are generally a subset of the more general bicubic impedances and, as such, can provide a circuit realization for a reduced number of functions under determined conditions. Given their relatively simple structure, these compact networks will be directly used whenever possible. Some examples of such simplified network topologies are shown in Fig. 4.6. The experimental results in Sec. 4.4 clearly highlight that this simplified low-order synthesis is sufficient to achieve high-fitting accuracy for the varactors in this study.

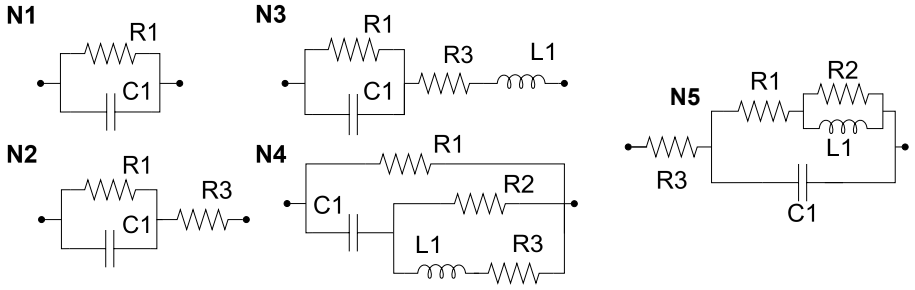

Figure 4.6: Synthesized networks for fitting complexities $(P, Q, R) = (1, 0, 0)$ (**N1**), $(P, Q, R) = (1, 1, 0)$ (**N2**), $(P, Q, R) = (1, 1, 1)$ (**N3**), and $(P, Q, R) = (2, 1, 0)$ (**N4** and **N5**).

However, in the general case, the proposed method can provide an equivalent circuit even for high-order impedances with $P \geq 4$ by systematically using the general BD procedure, as employed in Sec. 4.7.

4.3.3 Complete modeling application

The specific procedure adopted for synthesizing the multibias small-signal equivalent-circuit model is shown in Fig. 4.7. The first step consists of applying VF at a given (P, Q, R) complexity to the set of small-signal data points, separately at each bias. Subsequently, a global fitting error at each bias is evaluated by adopting the following normalized mean-squared-error (NMSE):

$$\mathrm{NMSE}_Z(V_\mathrm{B}) = 10\log_{10}\left(\frac{\sum_{k=1}^{K}\left|Z(\omega_k, V_\mathrm{B}) - Z_\mathrm{VF}(s, V_\mathrm{B})|_{s=j\omega_k}\right|^2}{\sum_{i=1}^{K}|Z(\omega_k, V_\mathrm{B})|^2}\right); \tag{4.7}$$

where K is the number of data points collected at the angular frequencies ω_k, Z represents the impedance data to be modeled, and Z_VF is the vector-fitted impedance.

If such an error is found to be above a certain user-defined threshold for any of the V_B values of interest, the VF procedure is repeated with an increased model complexity. This ensures that the chosen (P, Q, R) values are sufficient to reproduce the data points at a given V_B. As varactor technologies might display largely different physical effects occurring sharply across the bias voltage range, the user might decide to accept higher fitting errors at given bias voltage or, conversely, enforce a uniform threshold for the maximum NMSE_Z across all bias values. Once a satisfactory fitting error is achieved, either the minimal circuit synthesis approach [131] or a complete BD synthesis is performed on the impedance function in (4.2). As a result, a complete RLC network is obtained as a small-signal equivalent circuit of the varactor at each fixed bias V_B.

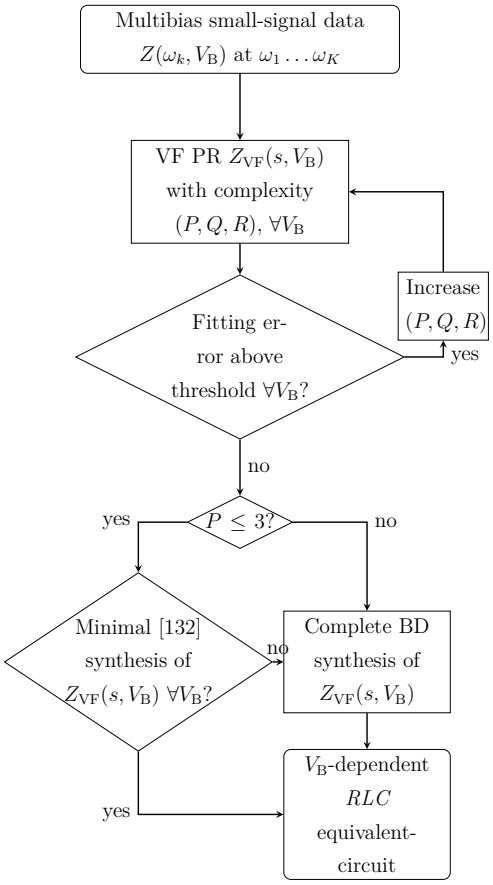

Figure 4.7: Flow chart for the proposed equivalent-circuit model extraction from small-signal data.

Given that each bias condition is treated separately, there is no guarantee that the synthesis procedure will result in the same circuit topology for all bias voltages, even when using VF with the same complexity (P, Q, R). However, the relative simplicity of varactor models adopted in the literature [3, 55, 4], along with basic physical insights, suggests that a relatively low complexity order is sufficient to achieve satisfactory model accuracy. This avoids component overfitting and ensures that the same RLC-network topology can be adopted for all bias values. In this case, the effect of V_B is realized through bias-dependent network values.

Moreover, it has to be noted that each component value in the synthesized network is not necessarily controlled by the voltage difference or current at its terminals, but depends on the external one-port voltage V_B. In other words, it is not guaranteed that the resulting empirical circuit can be represented as an interconnection of simpler one-port components that are current/voltage controlled with their own intrinsic variables. However, this aspect is not critical, as the dependence on the external voltage V_B is common in many other modeling works [4, 116]. In any case, all possible realizations

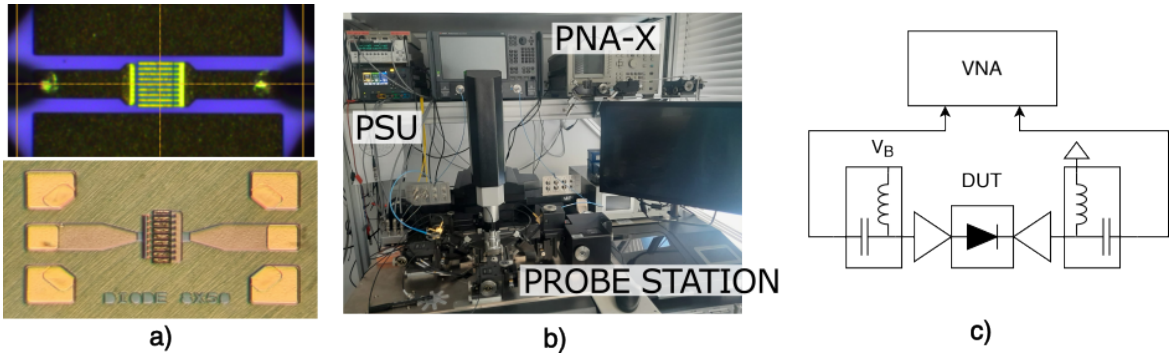

Figure 4.8: (a) Microphotographs of 8×50 μm Shottky diode by FBH (top); 8×50 μm Shottky diode by WIN semiconductors (bottom). (b) Photo and (c) block diagram of the measurement setup for performing S-parameter characterization.

of the empirical V_{B}-dependent lumped component network in CAD, e.g., in terms of look-up-tables or fitted parametric functions, results in a complete nonlinear model implementation that is fully compatible with both small- and large-signal simulations.

4.4 Experimental results

The synthesis methodology described in Sec. 4.3.1 has been applied to two GaN-on-SiC MMIC Schottky diodes, with target applications up to Ka-band, already described in Sec. 3.3.1. Both devices are derived from planar HEMT structures in which drain and source terminals are short-circuited (hence $V_{DS} = 0$, known as a "cold-FET" condition). In this way, the stack of materials between the gate metal contact, the $\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{N}$ barrier layer, the GaN channel and the joint source/drain contact are used to provide a variable capacitance effect [56, 55]. In this configuration, the controlling voltage V_{B} is taken as $V_{GS} = V_{GD} < 0$ in order to operate the diode in the reverse region with negligible current. This type of approach is commonly adopted in high-frequency GaN processes Product Design Kits (PDKs), in which HEMTs are typically available [4, 116], while standard varactors are not.

The same initial S-parameter data presented in Sec. 3.3.1 are exploited for the model extraction. Therefore, the same setup is shown in Figs. 4.8(b)-(c) where a vector network analyzer (VNA, Keysight PNA-X 5247B) is used to acquire the on-wafer two-port S-parameters at multiple bias points. The bias voltage V_{B} is applied through two bias-tees and it is defined as the difference between the voltage applied on the dc path of the anode and the voltage at the dc path of the cathode, the latter being always connected to ground. The measured S-parameters for the two-port DUTs (S_{DUT}) are then postprocessed to deembed the access pads as described in Sec. 1.4.

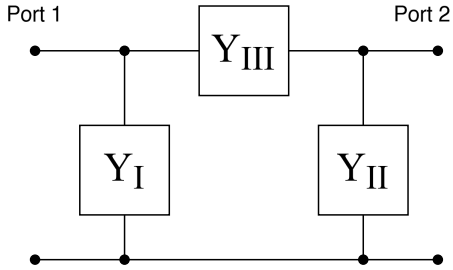

Figure 4.9: Partitioning of varactor device in three bipoles. The decomposition is valid if Y-parameters are considered.

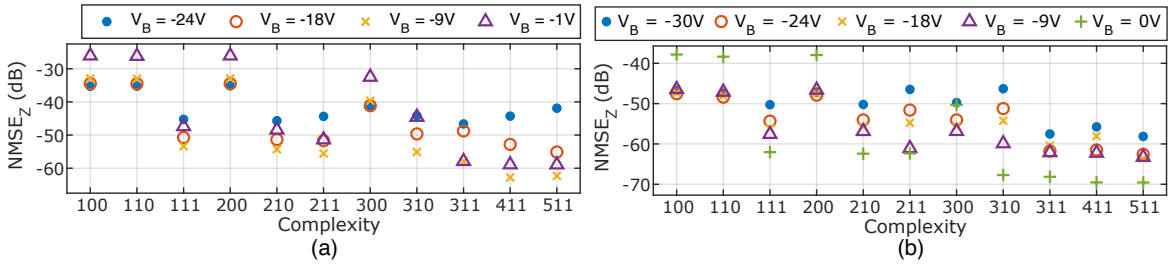

Figure 4.10: Error computed as in Eq. 4.7 for (a) WIN device and (b) FBH device for multiple bias voltages at increasing complexity.

Since both technologies come in a two-port configuration a 2×2 Y-parameters matrix with terms Y_{ij}, $i, j = 1, 2$ could be derived from measured S-parameter matrix. Y-parameters can then be decomposed into the equivalent π-network shown in Fig. 4.9, where $\mathrm{Y_I} = Y_{11} + Y_{21}$, $\mathrm{Y_{II}} = Y_{22} + Y_{21}$, and $\mathrm{Y_{III}} = -Y_{21}$. This partitioning allows the three one-port devices to be considered independently, eventually resulting in three separate networks.

By looking at the physical configurations in Fig. 4.8(c), it is reasonable to assume that the one-port devices $\mathrm{Y_I}$ and $\mathrm{Y_{II}}$ can only represent parasitic effects towards ground, without involving any bias dependency. As expected from layout considerations, each of them simply requires fitting a capacitance in the fF range, without involving any application of the proposed bias-dependent procedure.

Instead, the full procedure in Fig. 4.7 was applied, at increasing complexity levels, for the measured equivalent impedance function $Z_{\mathrm{III}} \stackrel{\mathrm{def}}{=} \frac{1}{\mathrm{Y_{III}}}$.

Fig. 4.10 reports the resulting NMSE_Z for both the $8{\times}50$ μm WIN diode (Fig. 4.10(a)) and $8{\times}50$ μm FBH sample (Fig. 4.10(b)) at different complexities at five bias voltages. The complexity levels range from $(P, Q, R) = (1, 0, 0)$, which corresponds to a single capacitance with parallel resistance, to $(P, Q, R) = (5, 1, 1)$, corresponding to 5 poles/residues as well as the D and E terms. From this analysis, complexities $(1, 1, 1)$, $(2, 1, 0)$, and $(3, 1, 1)$ result in good fitting accuracy across all bias voltages.

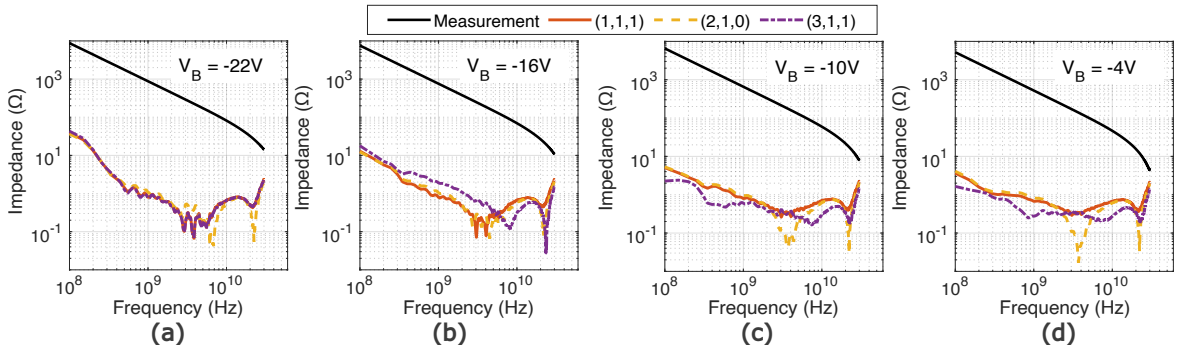

Figure 4.11: Measured $|Z_{\mathrm{III}}|$ impedance (black line) and absolute error across frequency between Z_{III} and its vector-fitted version Z_{VF} for the 8x50 μm diode by WIN. The extraction is performed at three different complexities for V_{B} = -22V (a), -16V (b), -10V (c), -4V (d).

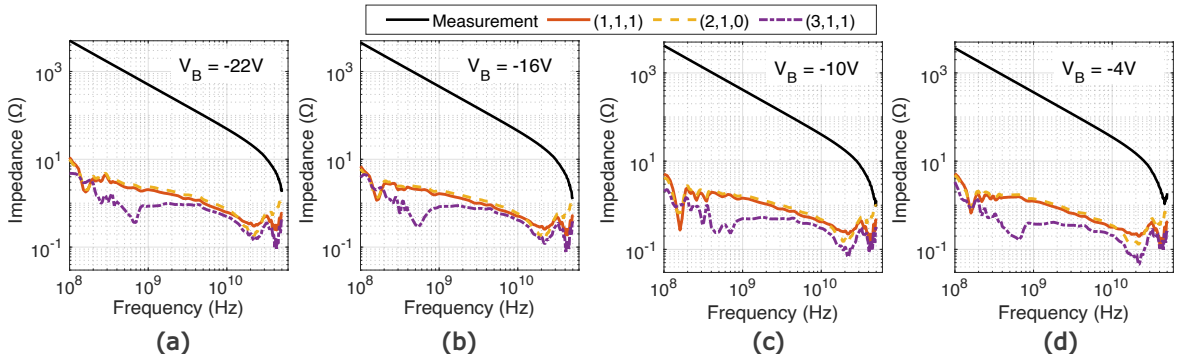

Figure 4.12: Measured $|Z_{\mathrm{III}}|$ impedance (black line) and absolute error across frequency between Z_{III} and its vector-fitted version Z_{VF} for the 8x50 μm diode by FBH. The extraction is performed at three different complexities for V_{B} = -22V (a), -16V (b), -10V (c), -4V (d).

As the NMSE_Z is computed as an average across frequency, it is worth evaluating the deviation across frequency by the following absolute error:

$$E_{\mathrm{Z}}(\omega_k, V_{\mathrm{B}}) = \left| Z_{\mathrm{III}}(\omega_k, V_{\mathrm{B}}) - Z_{\mathrm{VF}}(s, V_{\mathrm{B}})|_{s=j\omega_k} \right|, \ \forall k; \tag{4.8}$$

where Z_{VF} is the fitting with a given complexity (P, Q, R). Fig. 4.11 reports measured impedance and the computed error for WIN device for the configurations (1,1,1), (2,1,0), and (3,1,1). In Fig. 4.12 the same results are presented for the FBH device. The absolute error ranges from a few Ωs when the measured impedance is several kΩs, and it goes down to the mΩs as the measured impedance is in the Ω-range, thus displaying consistently small error values across the entire frequency range.

The simplified network synthesis in [132] was applied to a subset of the cases shown in Fig. 4.11. By using the network labeling in Fig. 4.6, $(1, 0, 0)$ corresponds to **N1**,

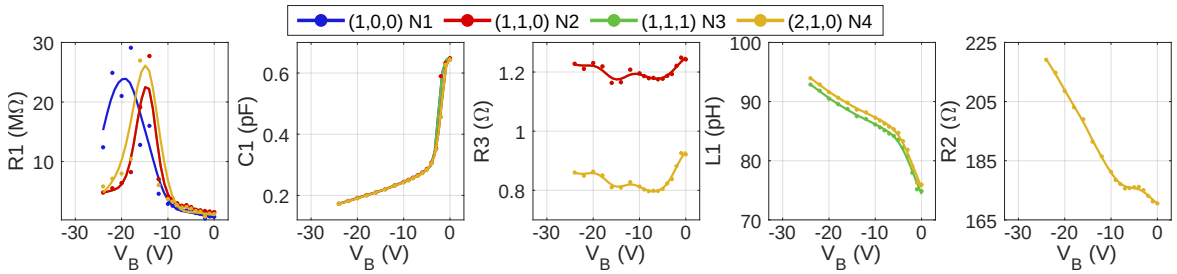

Figure 4.13: Network elements for the 8×50 μm varactor by WIN, with component names referring to Fig. 4.6 (not all components are present for every network). Each dot corresponds to a given bias value, whereas solid lines are spline approximations across all bias values.

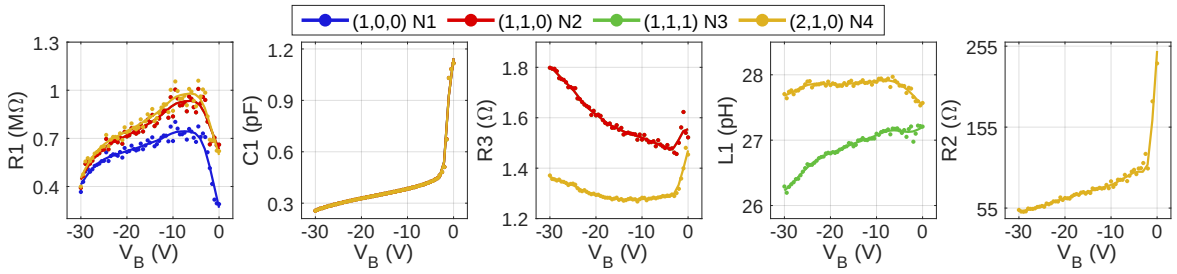

Figure 4.14: Network elements for the 8×50 μm varactor by FBH, with component names referring to Fig. 4.6 (not all components are present for every network). Each dot corresponds to a given bias value, whereas solid lines are spline approximations across all bias values.

$(1,1,0)$ to **N2**, $(1,1,1)$ to **N3**, and $(2,1,0)$ to **N4**. The values for the components for each of these networks are reported in Fig. 4.13 for WIN device, where each point corresponds to a single-bias VF, while solid lines are the result of spline approximations across the whole bias voltage range. In Fig. 4.14, similar patterns to those observed for the WIN varactor can be noticed, such as the sharp change in the C1 value, and the R1 value in the MΩ range. However, despite the same periphery and similar layout as the WIN varactor, the FBH device exhibits a higher nonlinear capacitance value, a higher R3 series resistance, and a lower parasitic inductance.

4.5 CAD implementation and validation

In Sec. 4.4 the model adherence to measured data was evaluated only for the one-port Y_{III} element in the impedance domain. In order to implement the model in CAD environment for simulation, the complete π-network should be implemented, including Y_{I} and Y_{II}, so as to evaluate the modeling performance for the two-port DUTs. As

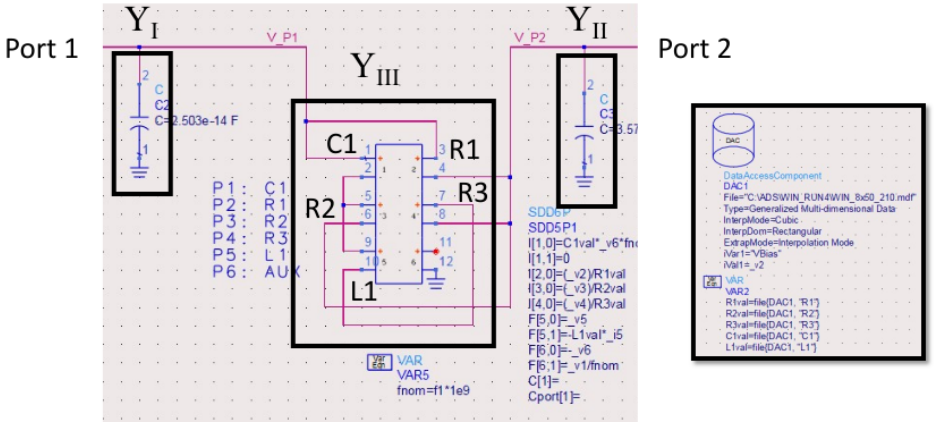

Figure 4.15: Implementation of varactor model for complexity $(2, 1, 0)$ in ADS environment.

already discussed, the capacitor elements This is achieved by considering the two-port S-parameter matrix S with terms S_{ij}, $i, j = 1, 2$ as obtained by converting from the two-port de-embedded admittance matrix Y.

The nonlinear network implemented in Advanced Design System (ADS) environment is reported in Fig. 4.15. The core circuit is implemented in a symbollically defined device (SDD) block which has the ability to define the voltage-current equations for each port evaluated at runtime. In this way, the voltage between port 1 and port 2 is used to interpolate the value of each element (R1, R2, C1, ...) from a lookup table. The table contains the value for each element depending on the extraction bias voltage and ADS performs a cubic interpolation when extracting the values. Y_{I} and Y_{II} are instead implemented as linear capacitors directly facing the two connection ports. This methodology has the flexibility to adapt to the device simply considering a different data file, therefore the same component is adopted for both FBH and WIN solutions. Moreover, SDD component, being defined by voltage-current equations, fully support nonlinear simulations, which is desirable for such model.

Fig. 4.16 reports the comparison in terms of S_{11} and S_{21} between measurement and modeling across the whole measured frequency range for the implemented network **N4** at $V_{\mathrm{B}} = -20$ V, showing accurate model prediction for both DUTs. To allow a quantitative evaluation of the model accuracy across frequency, the following error metric is adopted:

$$E_S(\omega_k, V_{\mathrm{B}}) = \frac{1}{4}\sum_{j=1}^{2}\sum_{i=1}^{2}\left|S_{ij}(\omega_k, V_{\mathrm{B}}) - S_{ij}^{\mathrm{model}}(s, V_{\mathrm{B}})|_{s=j\omega_k}\right|^2; \tag{4.9}$$

where S_{ij}^{model} are the terms of the two-port S-matrix obtained from modeling. Fig. 4.17(a) reports the error profile across frequency at multiple bias voltages for FBH device,

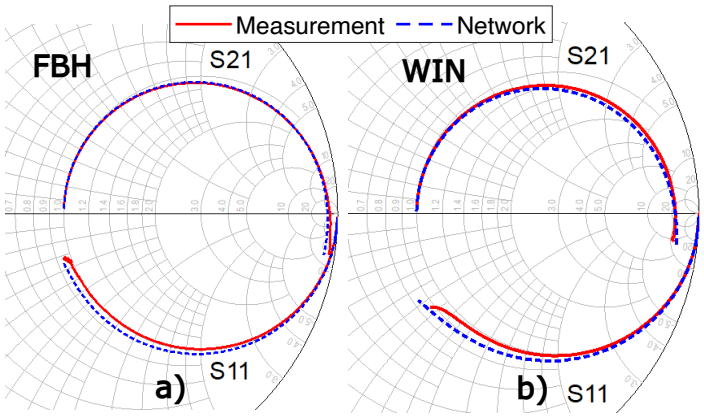

Figure 4.16: Comparison between modeled and measured S-parameters at $V_{\mathrm{B}} = -20\mathrm{V}$ for 8×50 μm by (a) FBH and (b) WIN.

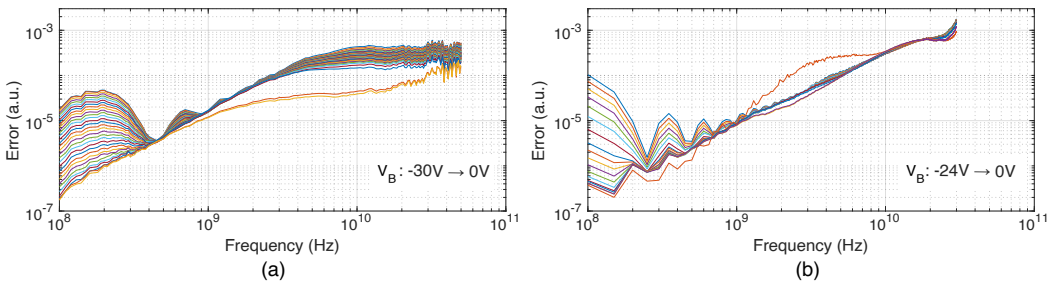

Figure 4.17: Modeling error E_S on the two-port S-parameters for (a) FBH 8×50 μm device and (b) WIN 8×50 μm device across frequency for all available bias voltages.

Table 4.1: $\bar{E}_S(V_B)$ in dB as from (4.10) at two selected bias voltages.

$\bar{E}_S(V_B)$ **(dB)**	**FBH 8 × 50μm**		**WIN 8 × 50μm**	
Complexity	V_B **= -20 V**	V_B **= -2 V**	V_B **= -20 V**	V_B **= -2 V**
(1,0,0)	-27.6	-27.9	-22.3	-23.2
(1,1,0)	-27.9	-28.3	-22.3	-23.2
(1,1,1)	-37.2	-33.2	-32.4	-30.7
(2,1,0)	-36.9	-33.3	-32.8	-31.1

showing a slight increase proportional to the frequency, yet remaining below 10^{-3} for all bias voltages. Similar results are observed for WIN device in Fig. 4.17(b), for which the error is lower than $2 \cdot 10^{-3}$. Table 4.1 reports the average error across frequency calculated as:

$$\bar{E}_S(V_B) = \frac{1}{K} \sum_{k=1}^{K} e(\omega_k, V_B) \tag{4.10}$$

for $V_B = -20$ V and $V_B = -2$ V at different complexities, generally demonstrating good model accuracy and increased prediction up to the $(2, 1, 0)$ case.

4.6 Model scaling

One of the desired properties of a device model is its ability to adapt to different device sizes and, eventually, being able to predict the performances of smaller or bigger devices with respect to the ones available for testing. If the prediction is accurate, a complete PA design could be carried out exploiting the varactor model instead of fabricating the target device. To assess the robustness of the proposed behavioral modeling approach and explore its correlation with the physical properties of the devices, the model fitting procedure was applied to a number of varactor devices fabricated using the FBH process. Despite all samples sharing a similar layout, finger configurations are mostly different thought to provide an accurate understanding of the impact of geometric scaling on device behavior. Specifically, the investigation focused on two scaling scenarios: one involving variations in the number of gate fingers, n_F, while maintaining a constant gate finger width of $W_F = 75$ μm; and the other examining changes in the gate finger width, W_F, for a fixed number of gate fingers, $n_F = 8$ [4]. For this investigation, initially a fixed complexity of $(1, 1, 0)$ was employed, corresponding to the **N3** topology, as it is the first complexity exhibiting good fitting results.

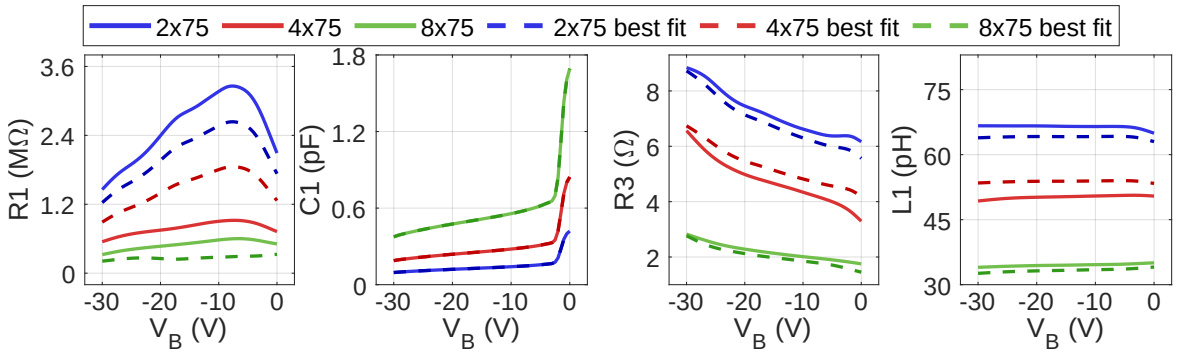

Figure 4.18: Network elements fitting (solid lines) for complexity $(1, 1, 0)$ for varactors in FBH technology with different finger numbers but fixed width (75 μm). Values are linearly interpolated for each bias and the evaluation of the best fitting function is reported in dashed lines. Element names are referred to network **N3** in Fig. 4.6.

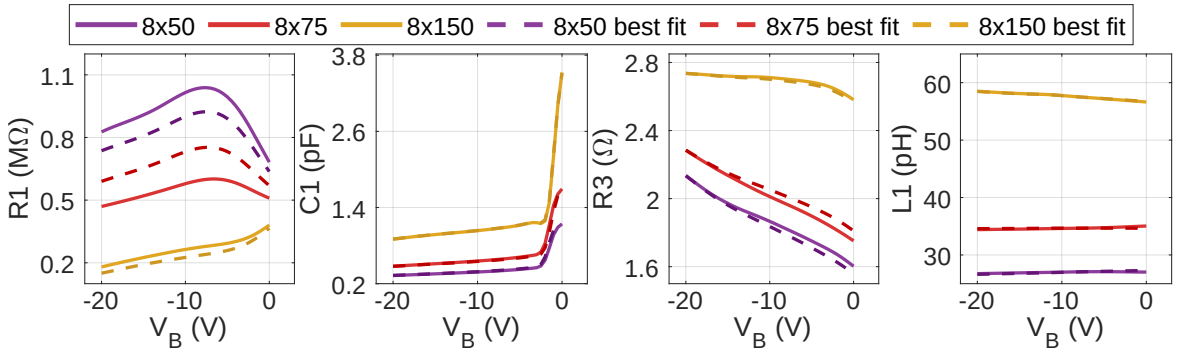

Figure 4.19: Network elements fitting (solid lines) for complexity $(1, 1, 0)$ for varactors in FBH technology with 8 fingers and multiple finger widths. Values are linearly interpolated for each bias and the evaluation of the best fitting function is reported in dashed lines. Element names are referred to network **N3** in Fig. 4.6.

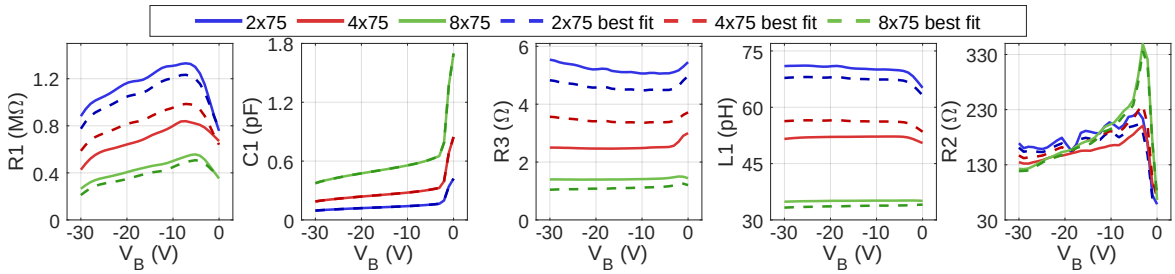

Figure 4.20: Network elements fitting (solid lines) for complexity $(1, 1, 0)$ for varactors in FBH technology with different finger numbers but fixed width (75 μm). Values are linearly interpolated for each bias and the evaluation of the best fitting function is reported in dashed lines. Element names are referred to network **N3** in Fig. 4.6.

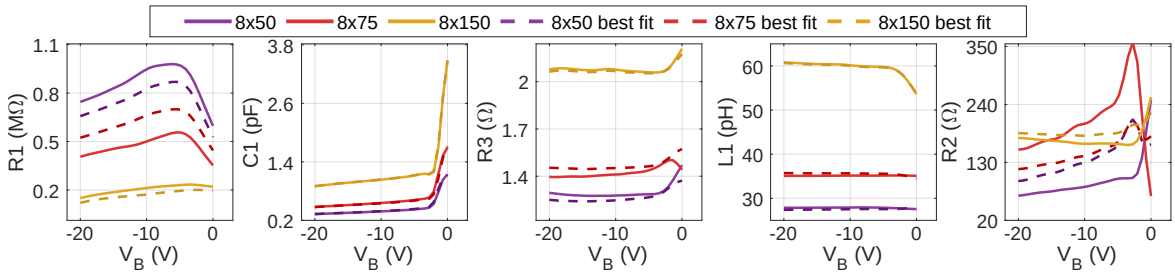

Figure 4.21: Network elements fitting (solid lines) for complexity (2,1,0) for varactors in FBH technology with 8 fingers and multiple finger widths. Values are linearly interpolated for each bias and the evaluation of the best fitting function is reported in dashed lines. Element names are referred to network **N4** in Fig. 4.6.

Fig. 4.18 displays the values of the network elements at increasing number of fingers for layouts 2×75 μm, 4×75 μm, and 8×75 μm, whereas Fig. 4.19 reports the effect of finger-width scaling, reporting 8×50 μm, 8×75 μm, and 8×150 μm peripheries. In general, C1 exhibits a clear increase as the overall periphery ($\propto n_F \times W_F$) is larger, consistent with the fact that the capacitance originates from the depletion area of the diode. The intrinsic series resistance R3, which directly impacts the quality factor of the varactor, reduces as n_F is increased, whereas it is slightly proportional to W_F. As expected, the parasitic inductance L1 reduces as n_F is increased, whereas it is proportional to W_F. The leakage resistor R1, expectedly, decreases its value both for larger W_F and larger n_F. The same study was performed adopting the $(2, 1, 0)$ complexity. This particular topology has previously been shown to be sufficiently accurate for capturing the multibias S-parameter behavior of similar devices. Moreover, slightly better modeling performances are expected if compared to $(1, 1, 1)$ complexity. Results are consistent with the ones already commented for complexity $(1, 1, 1)$. The only addition here is the parasitic resistance R2 that barely depends on the layout,

thus does not show a clear trend.

In order to better quantify these effects, a linear regression was applied for each RLC component value with respect to n_F and W_F, for the corresponding datasets. The best fit values by this ideal linear scaling law are shown as dashed lines in Figs. 4.18-4.21. Capacitance C1 displays a linear proportionality with respect to both n_F and W_F, that is, with respect to the device total anode area. The intrinsic series resistance R3 and the parasitic L1 inductance show very accurate linear scaling with W_F, while the trend is only slightly less accurate with respect to n_F. The scaling properties for R1 are slightly less ideal, but this behavior can be tolerated considering that its value in the MΩ range only influences the parasitic conduction and the impact on S-parameters is negligible.

Although the use of an empirical equivalent circuit may result in the identification of RLC components that do not always correspond directly to intrinsic physical phenomena in the varactors - potentially complicating their interpretation (e.g., the case of R2) - the findings nonetheless suggest a notable degree of alignment with intuitive scaling rules for most equivalent elements. This alignment indicates that the modeling approach captures meaningful physical insights, even though the models themselves are derived purely through behavioral analysis based on measured data, without any prior assumptions or detailed knowledge of the device's internal structure. This ability to infer physically relevant trends from a data-driven model highlights the robustness of the approach and its potential utility in guiding design decisions.

4.7 Modeling of complex structures

As explained in Sec. 4.3, the advantages of the proposed modeling strategy lie in the possibility of applying the same modeling procedure to non-conventional devices or more complex structures globally acting as varactors. When multiple devices are involved, the effects extracted for a single structure can mix up with interconnections or parasitics provided by the bias line, resulting in complex interactions between components, as will be demonstrated later. Influences due to short physical distances can worsen the simulation outcomes when considering the single-device model instead of a complete electromagnetic simulation. Moreover, wide-band frequency data could be useless outside a declared bandwidth, being limited by the design of the structure and not by the setup involved. This is the case of bias feeds realized with $\lambda/4$ lines or narrowband inductors coupled with bypass capacitors. In this Section, an equivalent circuit will be extracted for such structures and compared with electromagnetic

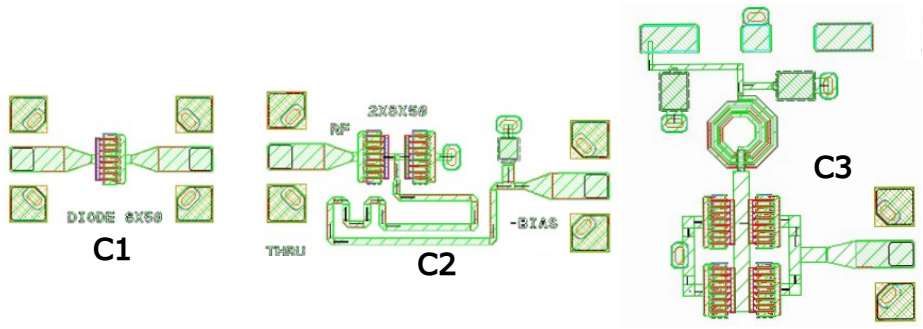

Figure 4.22: Varactor cells under test. **C1** Single diode; **C2** two diodes in antiseries configuration; **C3** 2x2 island configuration.

simulation results.

The varactor cells under consideration (Fig. 4.22) are designed in the commercial 120-nm GaN-on-SiC technology from WIN Semiconductors already presented. The first cell (**C1**) is the Schottky power diode with 8×50 μm periphery already employed in this Chapter. The second cell (**C2**) is realized by connecting two **C1** cells in an anti-series configuration; the third cell (**C3**) is designed by placing two anti-series structures in parallel referred to as *island* configuration (not to be confused with island design presented in Sec. 3.4). All these designs are custom realizations targeting the evaluation of varactor elements in configurations more suited for the use in PA designs. This is mostly due by the fact that since a bias is required for the varactor, anti-series structures allow to handle the RF input without any bias, influencing as little as possible classical PA design. Given the novelty of the layouts realized in this technology, and provided that no measurements were a-priori available for the varactor region of the diode, a complete characterization is worth carrying out for each fabricated device.

A preliminary evaluation is conducted as described in Chapter 3 to extract the equivalent capacitance (C_{eq}) and quality (Q) factor across V_b for any given frequency. Multi-bias S-parameters are acquired with a Vector Network Analyzer (Keysight) as 2-port data for the single element **C1** in Fig. 4.22 and as 1-port data for the cells **C2** and **C3** in Fig. 4.22. In the last two structures, the second connection is only meant for the application of the bias voltage and works as an open connection at the diode level between 16 GHz and 22 GHz. In all cases, the access pad is de-embedded by EM simulations as described in Sec. 1.4. The results are reported in Fig. 4.23 for the operation in the reverse bias region as varactors. For this characterization, the bias voltage V_b ranges from -20 V to -2 V.

C3 is expected to provide a C_{eq} approximately equal to that of **C1** as it is configured

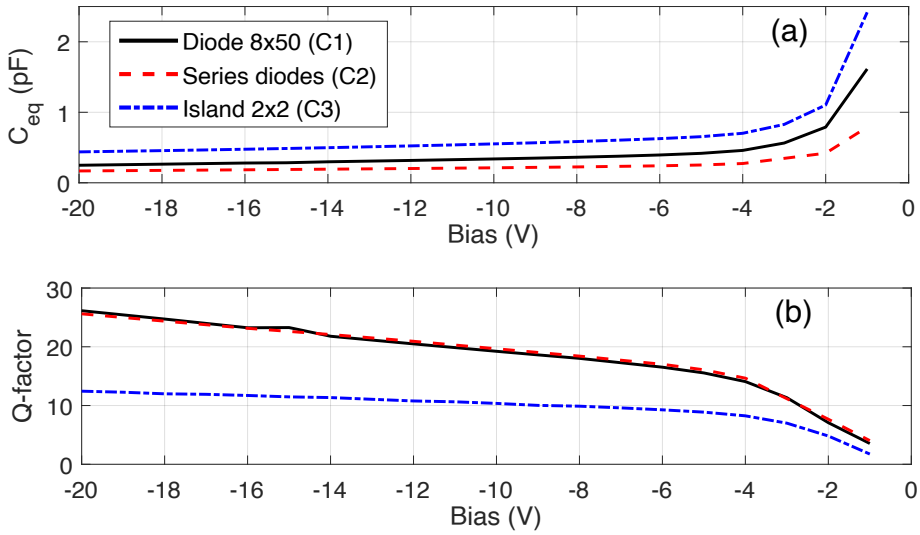

Figure 4.23: (a) Equivalent capacitance and (b) quality factor of the three cells in Fig. 4.22 at 18 GHz.

as two diodes in parallel connected in series. Instead, the resulting capacitance is higher than the one of **C1** (Fig. 4.23(a)), probably caused by the additional structures required by this configuration. The increased parasitics provided by both the bias connection and the interconnection metal clearly impact the quality factor, resulting in the worst performances. Instead, **C2** is realized as a single anti-series structure, thereby creating a varactor device that nominally has half the capacitance of **C1**. This is visible in Fig. 4.23(a) as a red dashed line exhibiting values slightly higher than expected. Q values are close to the ones of **C1** and this is particularly good, as it indicates that such a structure does not add much parasitics.

The modeling procedure described in Sec. 4.3 has been applied to all three cells, limiting the frequency range from 16 GHz to 22 GHz. Fig. 4.24 reports the NMSE computed as in Eq. 4.7 for the three cells. Since **C2** and **C3** are one-port devices, the decomposition in a π-network is not needed in this case, therefore the error will be referred to as NMSE without any subscript. As expected, a reduced error is observed when the complexity is increased, reaching a plateau from complexity (3,1,0) and beyond. From this analysis, the complexity (2,1,1) is selected as a trade-off between accuracy and number of network elements.

BD synthesis applied to the three cells for complexity (2,1,1) results in the network topology reported in Fig. 4.25. This time, the data resulting from measurements do not allow for the extraction of a minimal network, therefore the full BD algorithm is applied. In particular, element L_0 corresponds to term E in Eq. 4.2 and is therefore

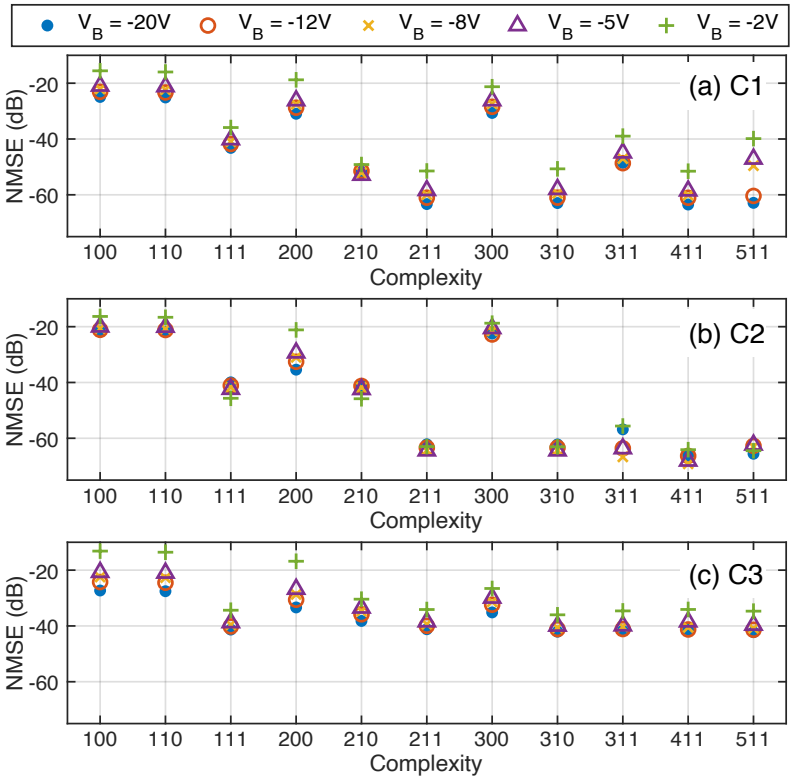

Figure 4.24: Fitting errors for five bias voltages at increasing complexities for (a) **C1**, (b) **C2** and (c) **C3** cells in Fig. 4.22 over the available frequency range of 16 GHz - 22 GHz.

excluded from the BD algorithm. Values for each element are reported in Fig. 4.26. Similar results could be observed for all cells and similar trend observable in other varactor models could be identified in C element, probably the main responsible for the capacitive effect of the varactors. Notably, the two diodes in series exhibit very low L values, in the order of fF, resolving in a reduced impact of the right part of the network on the overall S-parameters.

The bias-dependent network was implemented in CAD software as described in Sec. 4.5 and the error on the S-parameters is evaluated with the following equation:

$$E_S(\omega_k, V_\mathrm{B}) = \left| S_{11}(\omega_k, V_\mathrm{B}) - S_{11}^{\mathrm{model}}(s, V_\mathrm{B})|_{s=j\omega_k} \right|^2; \tag{4.11}$$

As visible in Fig. 4.27, a maximum value of around $1 \cdot 10^{-4}$ is observed in the worst case represented by structure **C3** for all bias voltages and in the full frequency span available. Error drops down to $1 \cdot 10^{-6}$ for structures **C1** and **C2**. Since these errors are evaluated by comparing the model performances extracted from measurements with measured data themselves, good agreement is expected. Instead, it could be interesting to compare this error with that obtained by simulating **C2** and **C3** structures with data available for the diode. The results combine the S-parameters of the single

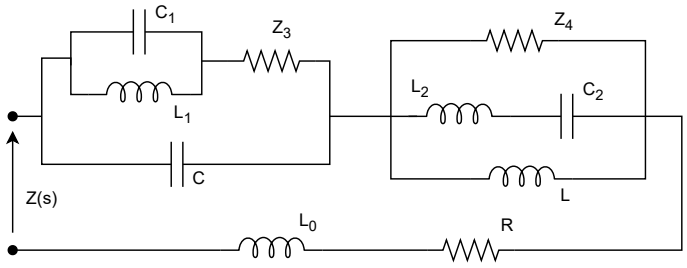

Figure 4.25: Network resulting after the application of BD network synthesis for complexity $(2, 1, 1)$.

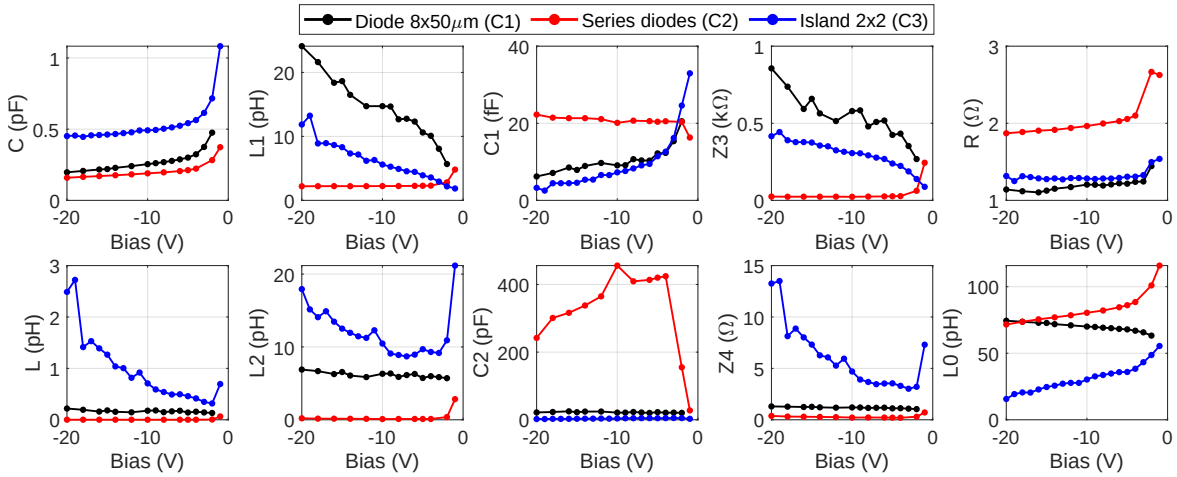

Figure 4.26: Elements value for BD extraction performed on the three cells. Network element names refer to components in Fig. 4.25.

diode with EM simulations of the interconnections and bias lines to derive a possible implementation of the structures if the fabrication of test elements is not feasible. Figure 4.28 shows the model error, resulting from the average of multiple biases, and the error computed from the simulation results over the complete frequency span. As visible, the error obtained from the simulator is order of magnitudes greater than the one achieved with direct structure modeling. This result further supports the advantages related to the new modeling procedure here proposed as traditional modeling approaches could not easily be adapted for the goal.

4.8 Conclusions

This Chapter presented the implementation of an innovative automated network synthesis method for equivalent-circuit modeling of integrated varactor diodes operating in the millimeter-wave frequency range. The proposed model is derived from empir-

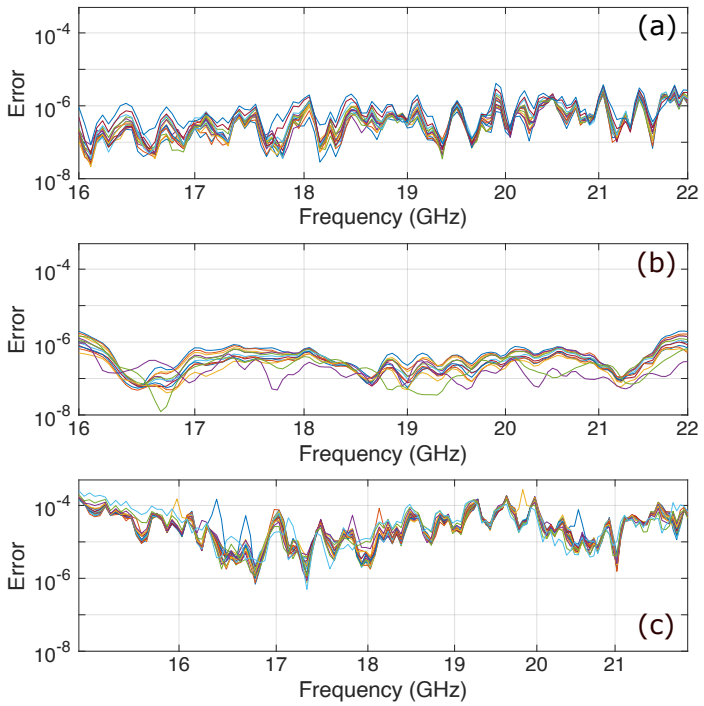

Figure 4.27: Error on S-parameters for (a) single diode, (b) series diodes, (c) island diodes.

ical multi-bias S-parameter measurements of the device under test (DUT), without imposing any predefined circuit topology. This flexibility allows for seamless adaptation to diverse design requirements. The procedure incorporates a user-defined complexity level, enabling designers to balance model accuracy with simplicity. By leveraging the VF algorithm, a rational function representation of the device is extracted with a specified tolerance, ensuring accurate characterization of its high-frequency behavior while maintaining control over computational and modeling complexity.

Although behavioral in nature, the model preserves a connection to the physical properties of the DUT, demonstrating robustness across different device scales and technologies. Its direct implementation as a bias-dependent lumped-element network facilitates both linear and nonlinear simulations in any CAD environment. Although component values are generally bias-dependent, the approach can identify components that are independent of bias V_{B} without requiring any prior assumptions. Users can then decide whether to approximate certain RLC elements as bias-independent, tailoring the model to specific application requirements.

The proposed approach overcomes the limitations of traditional layout-dependent modeling methodologies, which often rely on low-frequency measurements or the determination of the DUT's self-resonant frequency. Being entirely data-driven, the proposed models can be fitted with increasingly higher approximation orders to meet spe-

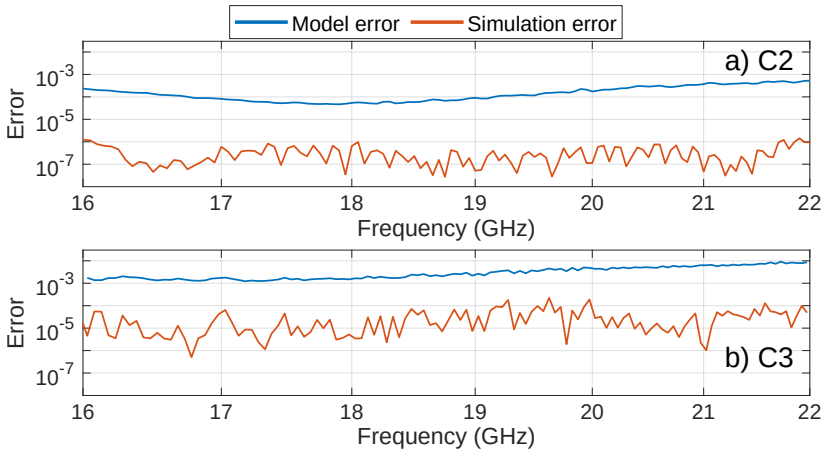

Figure 4.28: Error on S-parameters computed for model and simulation for a) series diodes, b) island diodes.

cific accuracy requirements. Independent of the device's layout details, this approach is not theoretically confined to single-diode devices. It can be seamlessly extended to more complex bias-dependent configurations, such as varactors with anti-series diode structures, or to other bias-dependent devices, such as microwave switches. Moreover, the dataset used for model extraction can be flexibly constrained in the voltage or frequency domain, enabling the creation of accurate models tailored to the specific ranges required by the application. These capabilities are demonstrated by applying the modeling procedure to two structures designed for PA applications, yielding superior results compared to pure EM simulations.

This modeling approach, at this stage, lacks a proper large-signal verification which was not possible to carry out given the instrumentation available in the laboratory. In fact, NVNA measurements are required to properly extract the voltage and current waveforms for a detailed comparison with the CAD results [111, 115]. This experimental validation will be addressed in a future development.

Chapter 5

RF Power Amplifier design techniques

5.1 Introduction

As mentioned in Sec. 1.2, power amplifiers are the main energy-consuming systems of base stations or wireless devices, and stand-alone applications powered by batteries adopt clever ways to reduce the impact of the wireless communication. Depending on the target application, multiple classes of operation are possible [135]. Traditionally, operating a PA in class A provide the best performances for linearity, with the drawback of forcing the circuit to constantly draw power to maintain the set bias point. On the contrary, class F operation relies on performance optimization, reducing the overall linearity FoM.

During the conversion process of a generic power amplifier, not all the input power is provided to the load. Some metrics could be introduced to properly quantify the quality of the amplifier, defined as the conversion efficiency. Power-added efficiency (PAE) is usually employed and is defined as:

$$\mathrm{PAE} = \frac{P_{\mathrm{OUT}} - P_{\mathrm{IN}}}{P_{\mathrm{DC}}} \tag{5.1}$$

where P_{DC} is the power drawn from the supply, P_{IN} and P_{OUT} are the RF input and output power, respectively. If the efficiency of the amplifier is low, more P_{DC} is required, hence reducing the PAE FoM.

Solutions to improve the performances of PAs are presented in Sec. 1.2.3 where load and supply modulations are discussed in detail. This work focuses on the improvement of single amplifiers, therefore no secondary amplifiers will be introduced to modulate the main one. Instead, the goal is to act on load and supply voltage of the single

main amplifier with varactors and switches, respectively. At the actual state of the research, no proper solutions are evaluated for the control of the supply voltage that will be addressed in future developments. When hardware amplifiers are tested, the voltage is then imposed by the controllable power supply, while in simulation, a voltage source is used to provide the proper bias on the drain side. The effect introduced by varactors is instead considered, first targeting the static control, i.e. adapting the synthesized impedance independently of the input signal.

As mentioned in Sec. 1.2, power amplifiers (PAs) are the primary energy-consuming components in base stations and wireless devices. In battery-powered stand-alone applications, energy constraints drive the adoption of strategies to reduce the impact of wireless communication. Depending on the target application, various classes of PA operation are available [135]. Traditionally, Class A operation offers the best linearity performance. However, this comes at the cost of low efficiency, as the circuit continuously draws current to maintain its bias point, regardless of the signal level. Between the extremes of Class A and Class F, other amplifier classes – such as Class AB, B, and C – strike various trade-offs between linearity and efficiency, and are often selected based on the specific system requirements. In contrast, Class F amplifiers are optimized for efficiency by shaping harmonic content through output network design, but they typically sacrifice linearity as a trade-off.

In a generic PA, not all the input power is delivered to the load. To evaluate how effectively a PA converts input and supply power into useful output power, we can introduce the concept of efficiency. A commonly used figure of merit is the *Power-Added Efficiency* (PAE), defined as:

$$\mathrm{PAE} = \frac{P_{\mathrm{OUT}} - P_{\mathrm{IN}}}{P_{\mathrm{DC}}}, \tag{5.2}$$

where P_{DC} is the power drawn from the DC supply, and P_{IN} and P_{OUT} are the RF input and output powers, respectively. A high PAE indicates that the amplifier effectively boosts the signal while minimizing energy losses. Conversely, if the amplifier's efficiency is poor, a larger amount of supply power (P_{DC}) is required to achieve a given output. This excess power, not converted into useful RF output, is dissipated as heat, requiring careful thermal management to prevent performance degradation or damage.

Strategies for enhancing PA performance are discussed in Sec. 1.2.3, focusing on load and supply modulation techniques. This work emphasizes improving the efficiency of a single amplifier stage, without relying on additional amplifiers for envelope tracking or load modulation. Instead, the dynamic control of the load and supply voltage of the main amplifier is proposed, using varactor elements.

At the current stage of this research, a dedicated control solution for the supply voltage has not yet been implemented and will be addressed in future work. During hardware testing, the supply voltage is externally controlled via a programmable power supply. In simulation, voltage sources provide the appropriate drain-side and varactor biases. The influence of varactor-based load modulation is considered, starting with static control, i.e., adapting the synthesized impedance independently of the instantaneous input signal.

Other works demonstrate the efficiency improvement due to the integration of varactors in the OMN at lower frequencies [136, 137, 138, 139]. For this work, Ka-band is selected with a center frequency of 16.5 GHz, and the goal is the realization of a completely integrated solution, therefore the use of devices realizable in the same process is mandatory.

5.2 Design experience at MEC

The required design knowledge for the design of the PAs with varactors has been gained during the internship period of six months at Microwave Electronics for Communications (MEC) in Bologna. The company specializes in the design and testing of MMIC in GaN and GaAs processes for a number of applications, including RF front-ends, low-noise amplifiers, frequency multipliers, and more.

During this industry period, the work focused on the design and optimization of a PA operating at microwave frequencies and targeting space applications. Since the design was intended for military purposes, only limited information can be disclosed in this Thesis. Initial specifications provided included target parameters such as PAE, gain, output power, and minimal bandwidth, while leaving the selection of appropriate stages to the discretion of the designer. The expertise gained during this period primarily focused on the design of static matching networks, both for the output stage and interstages, and their subsequent optimization using EM simulations. These simulations were critical in refining the matching networks to ensure optimal impedance performance across the specified operating conditions. Particular attention was devoted to ensuring the amplifier met stringent linearity requirements while achieving the requested PAE. This balance is often challenging in space applications due to the need for high efficiency without compromising signal integrity. Respecting specific temperature constraints is also of paramount importance in this field as conservative limits are usually in place. Another significant challenge came from layout constraints, which frequently require the designer to reconfigure certain networks to minimize space

consumption. In many cases, microstrip lines had to be folded or reshaped to fit within the compact layout. This necessitated an iterative design process involving EM simulations to verify that the realized impedance matched the amplifier's demands.

The design experience gained and optimization results are crucial for the designs presented in the next Section, and this experience turns out to be very tailored to this Ph.D. work since a similar GaN process was available for custom test designs.

5.3 Output matching network design with varactors

The output matching network (OMN) of the varactor has the role of providing the proper impedance to the transistor drain port while realizing a 50 Ω impedance on the second port for the external connection. This condition enables to obtain the ideal maximum power from the active device providing a standard impedance for the following elements. The optimal impedance is dependent on multiple factors. First, the technology heavily impacts the approximate location of the target impedance in the Smith Chart, mostly related to the physical characteristics of the substrate and metallization, but also to the geometry of the active element. For this work, GaN-on-SiC technology from WIN Semiconductors was used. Specifically, an initial study with the 150 nm technology (NP15-00) is conducted, followed by 120 nm technology already presented in Chapters 3-4. Other factors affecting the best impedance include the operating frequency, supply voltage, and output power. Since all these factors vary during the amplifier's operation, a trade-off should be considered, targeting the maximization of one performance in particular.

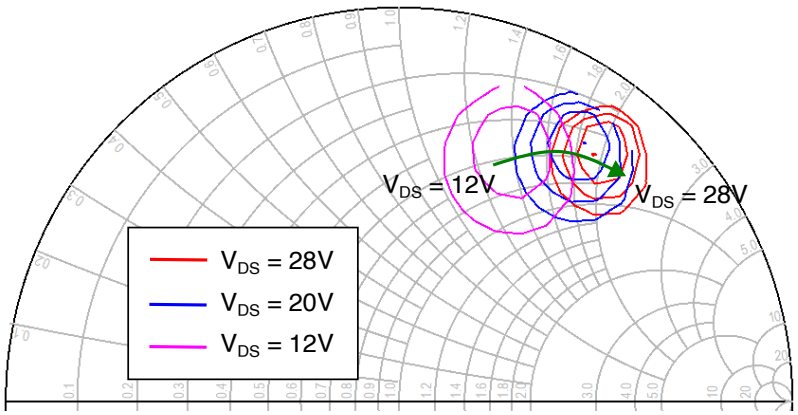

Figure 5.1: PAE contours for 4×50 μm device at 16.5 GHz for three bias voltages.

When the foundry provides a product design kit (PDK), the optimum impedance

can be found by load-pull simulations of the target device, where multiple loads are applied and the resulting performances in terms of power balance are acquired. Usually, since many output loads are tested, the results are conveniently plotted as contours, highlighting in the Smith Chart the regions of best operating conditions. Concentric circles represent the reduction of the selected performance, usually output power or efficiency, while the center point is located at the impedance that provides the maximum performance. An example is reported in Fig. 5.1 where red lines refer to PAE contours for 16.5 GHz and a target bias drain voltage V_{DS} of 28 V with bias voltage adapted to achieve a 100 mA/mm drain current. Blue and pink curves express the same metric obtained from V_{DS} = 20 V and 12 V, respectively. As visible, when the drain voltage is reduced, the optimum loads move to the left, following a constant resistance circle for the case under analysis. Therefore, one should expect a performance degradation due to the mismatch between the OMN load and the optimal one when the drain voltage differs from the target one. The goal of a reconfigurable OMN is to follow this variation and track the impedance as the supply voltage varies. In this sense, the amplifier achieves static reconfigurability, i.e., when the operation requires a low output power to be delivered, the supply voltage is varied accordingly and the varactor control signal is selected for the target impedance. The reduced voltage on the drain side will reduce dc power dissipation, and the losses are minimized by tuning the impedance to the optimal one for the specific configuration.

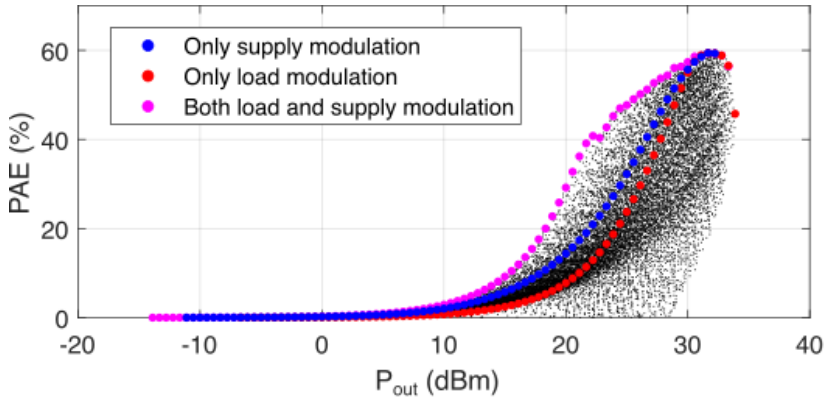

Figure 5.2: PAE performance extracted at 16.5 GHz for HEMT stage in common-source configuration. Efficiency envelope obtained with a fixed load but multiple V_{DS} is represented with blue dots; red dots are obtained with a fixed V_{DS} = 28 V but different loads; pink dots highlight the ideal condition achieved by selecting the best load for each tested V_{DS}.

To better assess the expected performances derived from this combination of effects, a simulation-driven load-pull analysis was conducted. This study involved sweeping

the load reflection coefficient across the entire Smith chart, in conjunction with a combined sweep of the drain-source supply voltage V_{DS} (ranging from $V_{\mathrm{DS}} = 18$ V up to the nominal $V_{\mathrm{DS}} = 28$ V) and the available RF input power, extending from small-signal levels to values sufficient to reach and exceed the peak power-added efficiency (PAE). Figure 5.2 presents the resulting PAE values, where each black dot corresponds to a unique operating condition. From this dataset, it is possible to extract the maximum attainable PAE profile as a function of output power under various optimization strategies. For instance, the blue dots represent the PAE profile achieved by varying the supply voltage while maintaining a fixed load, specifically chosen to yield the best PAE at the maximum V_{DS} and obtainable through a conventional matching network. Conversely, the red dots show the performance attained by optimizing the load at each power level while keeping the supply voltage fixed at its nominal value of $V_{DS} = 28$ V. The highest PAE performance is achieved through a joint optimization of both the load and the supply voltage, indicated by the pink dots. This dual optimization defines target profiles for both the supply voltage and load impedance as functions of output power. It must be remembered that these performances are achieved by the only reconfiguration of the OMN with a reduced impact on the starting design due to the introduction of varactors in the network. This preliminary study motivates the subsequent realization of test structures and simple amplifiers in this direction.

Varactors can be integrated into the OMN design in two primary configurations: either in series with the RF path or shunted to ground. Additionally, multiple varactors or varactor cells may be combined to expand the achievable impedance coverage of the target network [136]. The choice of topology should consider the characteristics of the available devices, particularly their tuning range and quality factor. The former determines the extent of impedance variation each varactor can contribute, while the latter becomes especially critical when large capacitance values are needed for a specific impedance. In fact, at low bias voltages, varactor capacitance becomes highly sensitive to bias variations (see Sec. 3.3), making the self-tuning effect under large-signal excitation more pronounced.

Given these considerations, it becomes evident that although multiple network configurations may theoretically achieve the desired impedance coverage, certain topologies are preferable as they help mitigate non-ideal effects. Due to the preliminary and investigative nature of this research on integrated varactors, both configurations were explored to assess the differing impacts that shunt and series arrangements may have on overall performance. Although a direct and coherent comparison was not feasible, since different foundry processes were available at different time, several alternative

approaches, involving various configurations and test structures, were analyzed to gain as comprehensive an understanding of the technology as possible.

5.3.1 Implementation with shunt varactor

In this Section, the implementation of a shunt varactor topology is addressed, similar to solutions presented in other works, although at lower frequencies [140, 137, 138, 141, 142]. In Fig. 5.3, a schematic representation of the contribution provided by

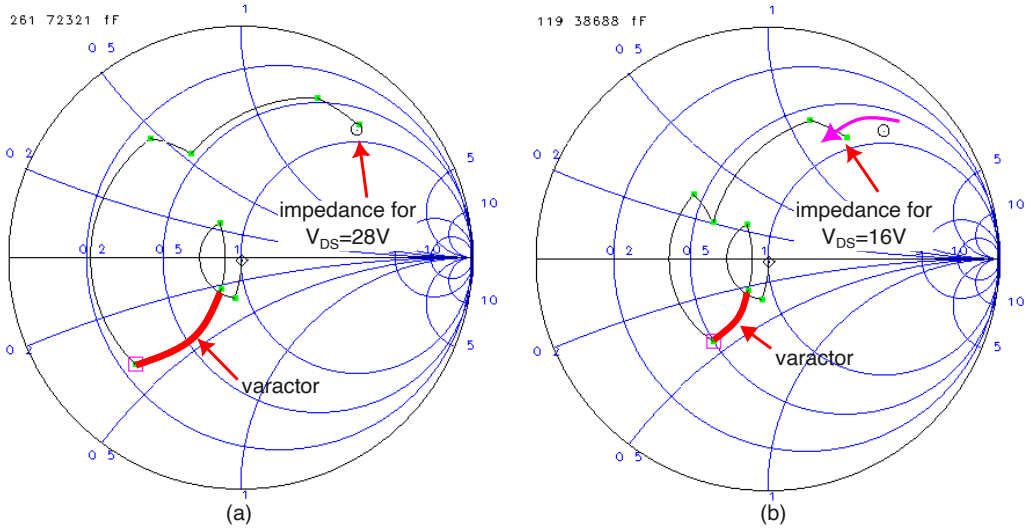

Figure 5.3: Impedance synthesized with the matching network and impact of capacitance variation of the varactor element for (a) maximum capacitance and (b) minimum capacitance.

each component to the MN impedance is shown. Particularly, the impedance trajectory obtained is visible when the capacitance value of the varactor element is modified. The movement should mimic the variation observed in load-pull simulations in Fig. 5.1.

When replacing a single capacitor with a varactor, certain considerations regarding the bias feed must be addressed. The varactor device should have one terminal connected to ground, while the second terminal must accommodate both dc and RF components. If the varactor is directly connected to the matching network, as shown in Fig. 5.4(a), the varactor bias must already be integrated within the network. This necessitates the presence of a dc feed elsewhere, on the MMIC or outside the chip, and requires a series capacitor to decouple the dc feed of the transistor from that of the varactor. Alternatively, a fixed capacitor can be inserted between the varactor and the network to properly isolate the dc path. This configuration is depicted in Fig. 5.4(b). In principle, the fixed capacitor could be replaced with a second varactor

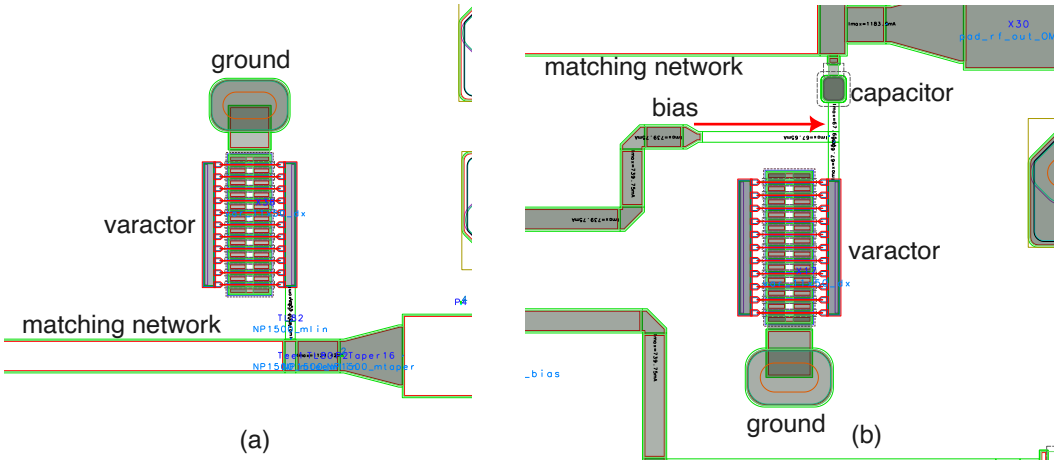

Figure 5.4: Possible implementation of varactor in the matching network: (a) direct connection providing both dc and RF signals; (b) decoupling capacitor and independent bias connection.

element, forming an anti-series structure where both devices are tuned by an external bias. Such a configuration eliminates the need for bias on the network but still requires a series capacitor to isolate the drain voltage, similar to the first solution. For the variant in Fig.5.4(b), a bias line provides the necessary dc connection via a dedicated pad. For this solution, the line is designed to present an open impedance at the central frequency of 16.5 GHz. This design uses a fixed capacitor that exhibits a short impedance at 16.5 GHz, combined with a line of the appropriate length to transform the short impedance into an open. Since the required length is typically quite long at this frequency, the line is folded to minimize area usage. Alternative solutions can include the use of a large resistor, typically in the order of kΩs [143, 103], or large inductors [136, 140].

Since no varactor device was available in the technology, an RF switch is used for the purpose. The switch is designed with source and drain contacts on opposite sides and a gate metal that crosses two bond metallizations. The layout is visible in Fig. 5.5(a) where both source and drain are connected to ground through backvia access. It should be noted that the switch design, being realized with the same metal layer as the HEMT gate, could be placed only with the fingers aligned from left to right. This is a common limitation of foundry processes that are particularly optimized in one direction. Although this design could work as a varactor, some issues prevent its use “as it is” and instead some modifications are required. In the first place, each backvia has a non-negligible occupation area and comes with design limitations like minimum distance from other elements and metal layers. This will prevent placing the varactor close to the network, reducing its effective tuning capabilities. The modified

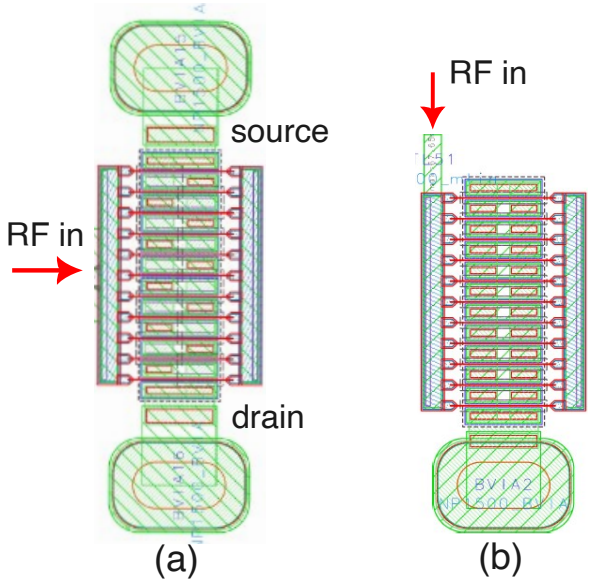

Figure 5.5: (a) Original layout of the switch device with source and drain grounded through backvias. (b) Switch layout modified to allow for only one backvia connection.

version, shown in Fig. 5.5(b), is obtained by connecting source and drain together with internal vias. In this way, only one backvia is required and the gate connection, now the input RF port, is directly available with a metal connection. The capacitance of this new structure should be close to that of the original switch, being affected only by the missing backvia.

The newly designed varactor was implemented in two different PAs designed and realized in 150 nm GaN-on-SiC technology. The complete tile is shown in Fig. 5.6, where a total of four PAs are present along with single varactors for characterization. The amplifiers are organized in the following way: **PA1** and **PA2** share the same layout, both for the IMN and the OMN. The only difference is the varactor element that in **PA1** is substituted with a fixed capacitor optimized for best PAE performances at 28 V of drain bias. The varactor bias is provided through the output RF pad, while a dedicated dc pad provides the bias for the drain. In this way, the PAs effectively implement the solution with varactor directly connected to the matching network (see Fig. 5.4(a)) and the isolation between drain and varactor bias is provided by a series capacitor also used for obtaining the appropriate matching. In contrast, **PB1** and **PB2** implement the variant with decoupled varactors (see Fig. 5.4(b)) and, as such, the varactor bias is externally provided by two dc pads, one for each varactor, while the RF output pad is used for the drain bias. Similarly with **PA1** and **PA2**, also **PB1** and **PB2** share the same layout, although different from **PA1** and **PA2** since in this case the series capacitor must be avoided to correctly provide the drain bias.

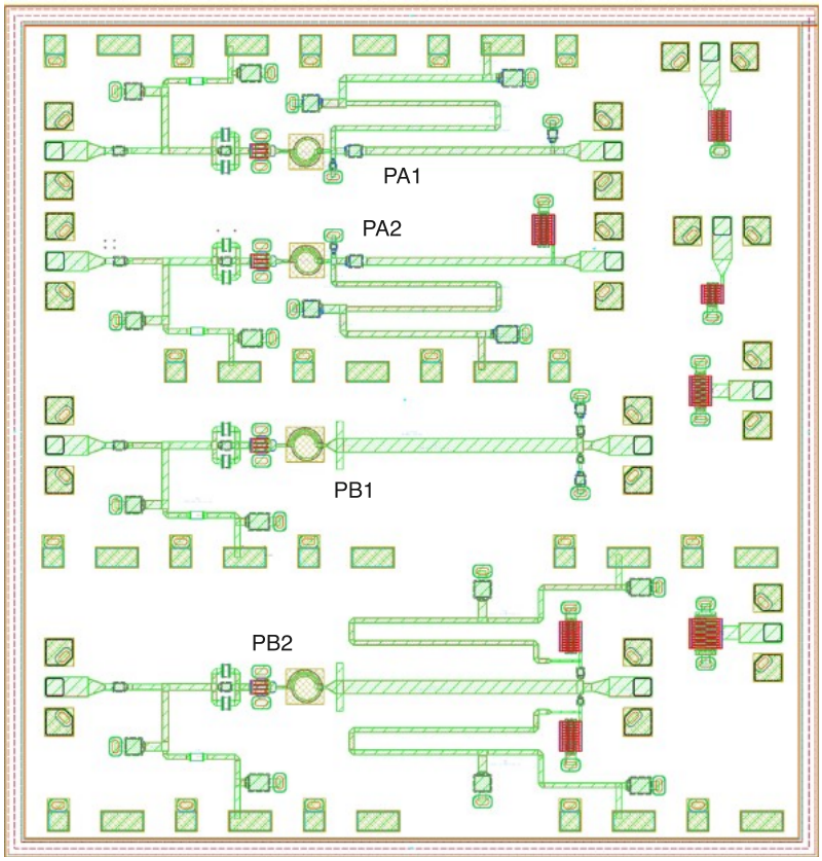

Figure 5.6: Layout of the complete manufactured chip containing the four amplifiers implementing varactors in the OMN.

Although the layout was designed to be tested with dc probe cards, where a total of six connections are provided interleaved with ground connections, adequate probes were not available at the time of characterization. Therefore, the development of a copper fixture with a custom printed circuit board (PCB) for providing appropriate dc connections was required. A schematic of the realized PCB is visible in Fig. 5.7(a) where all the wire connections are represented in blue at the bottom and the bonding wires are highlighted in yellow in the center hole. Since the PCB is thicker than the GaN chip, a first realization presented issues when contacting the external RF pads with the probes. Limitations are due to the clearance between the tip of the probe contacting the chip and the body of the probe; touching the PCB with the probe body prevents the tip from correctly touching the metalization. Therefore, a second revision included the milling of the copper block under the two PCBs, only leaving a raised square area for the chip. In this way, the surface of the chip and the one of the surrounding PCB are at the same height, increasing the spacing for the probe. The problem arises since the PCB needs to surround all the chip for all the bondings to be

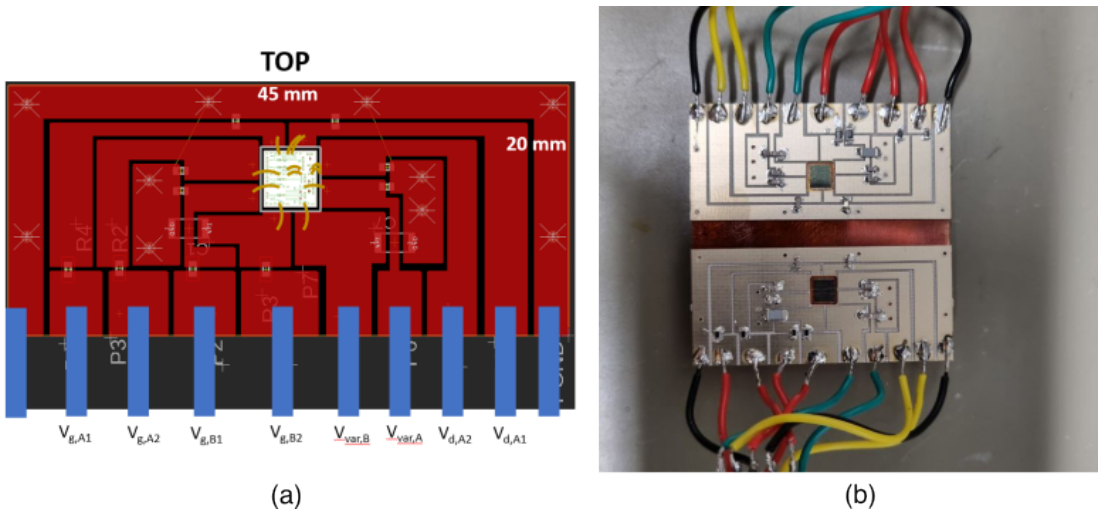

Figure 5.7: (a) Schematic representation of PCB fixture for delivering bias voltage up to the dc pads. (b) Photo of the complete fixture with two PCB boards and amplifier chip accommodated on a copper block.

in place. The length of the bonding wire is, in fact, limited, and the inner amplifiers (**PA2** and **PB1**) have contacts too far away from the top and bottom edges.

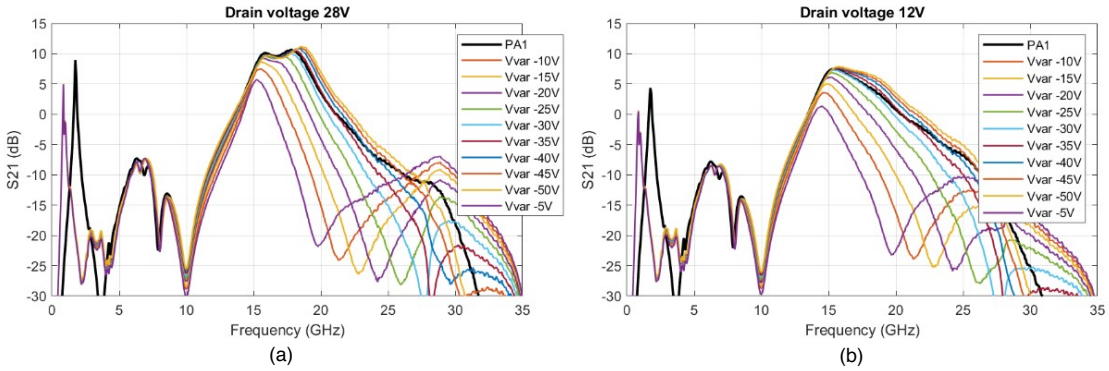

Figure 5.8: S_{21} performances of **PA1** and **PA2** as in Fig. 5.6 for two drain bias voltages of (a) $V_{DS} = 28$ V and (b) $V_{DS} = 12$ V and multiple varactor biases.

Small-signal performances measured for the four sample PAs are reported in Figs.5.8-5.9. Specifically, Fig.5.8 shows the S_{21} parameter, with the black line representing the amplifier with a fixed capacitor and the colored lines corresponding to the varactor-based counterpart for two drain bias voltages V_{DS}. The impact of different varactor biases is clearly visible, and the performance of the varactor version surpasses that of the fixed-capacitor counterpart when a low varactor bias is applied. This trend is also observed for the lower $V_{DS} = 12$ V, indicating that the capacitance value of the varactor is slightly detuned from the optimal value for this amplifier. A similar behavior

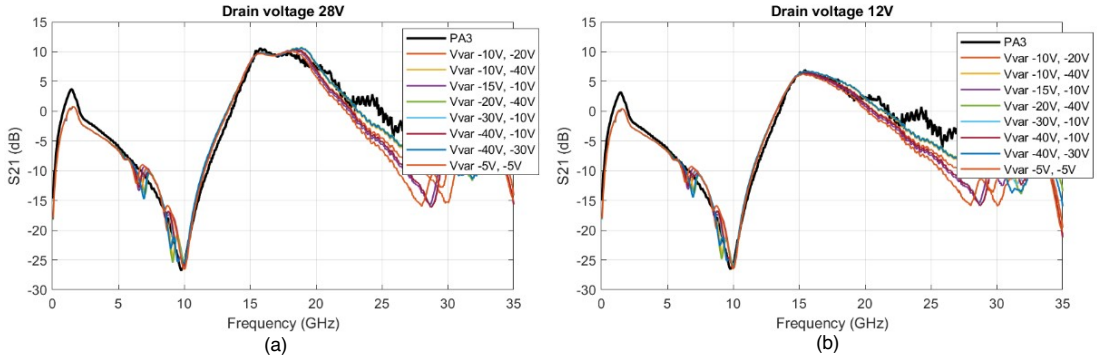

Figure 5.9: S_{21} performances of **PB1** and **PB2** as in Fig. 5.6 for two drain bias voltages of (a) $V_{\mathrm{DS}} = 28$ V and (b) $V_{\mathrm{DS}} = 12$ V and multiple varactor biases.

is observed for amplifiers **PB1** and **PB2** in Fig.5.9, although the absolute variation of S_{21} with respect to the varactor bias is smaller. This outcome was expected, as the additional capacitor introduced for decoupling the dc bias mitigates the effect of the varactor tuning. The second varactor was included in this case to enhance the overall capacitance.

Since the improvement is expected to be mainly on the PAE of the amplifier, S_{21} performance is not fully indicative of the effectiveness of varactors for improving efficiency. Large-signal measurements are required, but unfortunately, the needed hardware was not available.

5.3.2 Implementation with series varactor

As demonstrated in [136], varactors in an anti-series configuration can be inserted into the OMN as an alternative to a shunt solution. This Section proposes a matching network based on this implementation variant. The design and fabrication, differing from Sec. 5.3.1, were carried out using a 120 nm GaN-on-SiC process by WIN Semiconductors. In this process, a dedicated device optimized for switching applications was not available. Instead, a power diode is used, providing an alternative approach for implementing the varactor. The performance of this component is thoroughly discussed in Chapters 3–4; here, only the behavior of the matching network (MN) is addressed. It is important to note that only S-parameter measurements of the diode under reverse bias were available at the time of design, and the model developed in Chapter 4 was not applied in this case.

Two test structures were designed and are presented in Fig. 5.10. Both Figs. 5.10(a)–(b) are block elements used within the complete MN and were included on-chip for more granular characterization. These blocks consist of cells of four varactors arranged

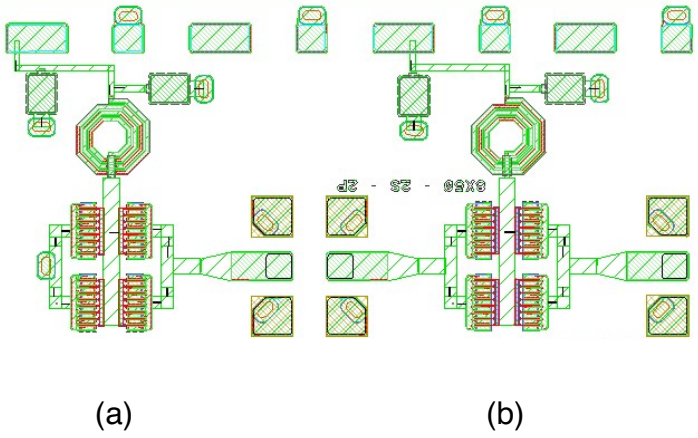

Figure 5.10: Test structures for the realization of MN with series varactors. Cell with configuration of 2x2 varactors is realized in (a) shunt version and (b) 2-port version.

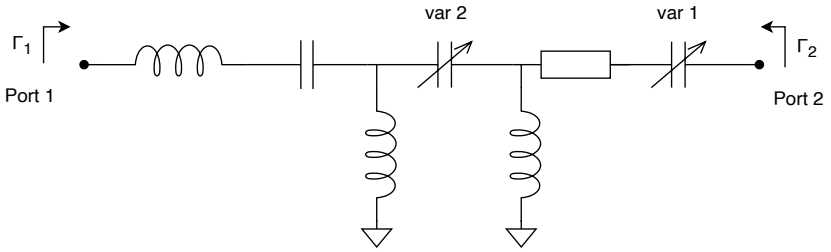

Figure 5.11: Schematic representation of the realized matching network including the varactor cells.

in a series-parallel configuration. This layout meets specific requirements related to biasing, as the DC bias voltage is applied internally within the cell, necessitating a 0 V potential on the exterior. Proper RF isolation for biasing is achieved using a large inductor and capacitor, which offer high attenuation around 16.5 GHz. Due to this limitation, MN measurements are considered reliable only within the 9–30 GHz frequency range, beyond which the impact of the DC connection becomes non-negligible. The difference among the cells lies in the presence of a second RF port in Fig. 5.10(b) replaced with a ground connection in the cell in Fig. 5.10(a). The two implementations should enable a fine characterization even for using the cell in shunt configuration and offer a direct comparison with the anti-series structures described in Sec. 4.7. Two instances of the cell were used in a series configuration to enable bi-dimensional coverage of impedances, as discussed in Sec. 5.3 [136], ultimately resulting in the circuit topology shown in Fig. 5.11. Figure 5.12 graphically illustrates the resulting load tunability range enabled by the two island varactor cells across the Smith Chart. The complete layout of the tunable matching network, including two bias networks that

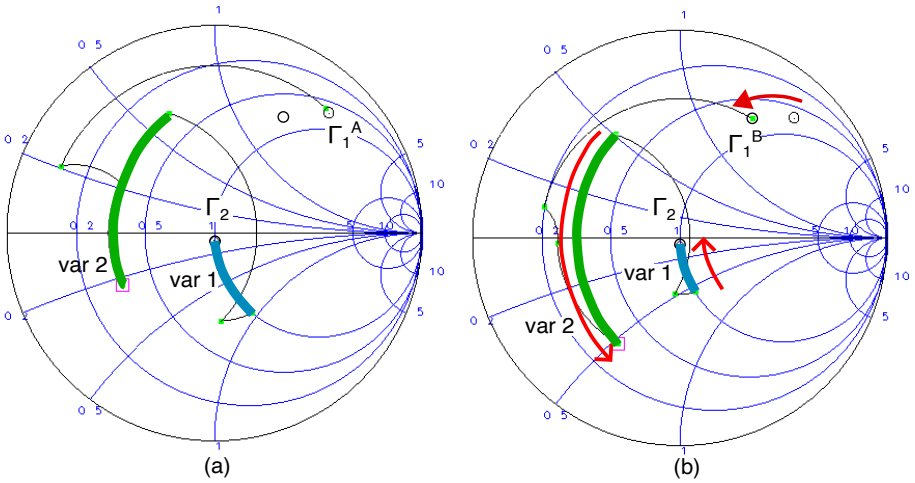

Figure 5.12: Reflection coefficient Γ_1 synthesized by the matching network at port 1 with the topology in Fig. 5.11. The effect of the two varactor cells (var1 and var2) is highlighted by reporting two extremal tuning configurations in (a) and (b), respectively.

allow independent voltage control of the two island varactor cells, is shown in Fig. 5.13. This network was fabricated without any HEMT device to evaluate its standalone performance. The complete matching network is designed to present a 50 Ω impedance at the output port (port 2, on the right) and the ideal impedance for the transistor at the second port (port 1, on the left). Varactor biases are provided independently through dc pads (V_{B1} and V_{B2}).

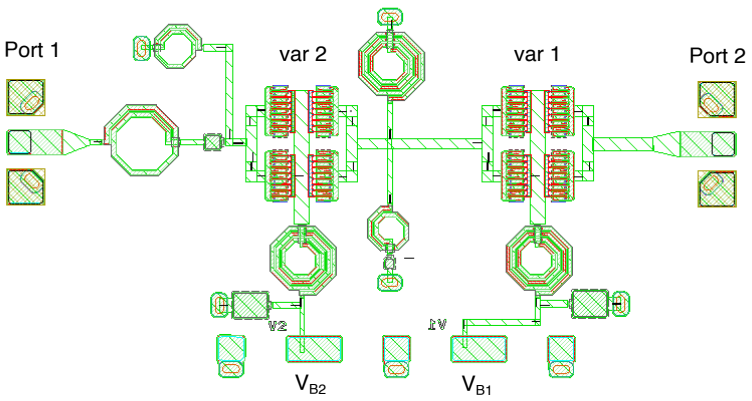

Figure 5.13: Layout of the designed tunable matching network. The target impedance is realized at port 1, while port 2 is to be terminated to the 50 Ω load. The two pads at the bottom allow to provide independent bias voltages to the two varactor cells.

An S-parameter measurement campaign was conducted by sweeping the two bias control voltages, $V_{B1}, V_{B2} \in \{-4, -30\}$, to characterize the full practical tunability

range. The resulting area covered in terms of load impedances is shown in the Smith Chart plot in Fig. 5.14, and is found to be sufficient to reasonably cover the target load profile required for optimal matching of the PA stage under consideration. The set of control voltages capable of tracking the wanted impedance profile as a function of power are reported in Fig. 5.15.

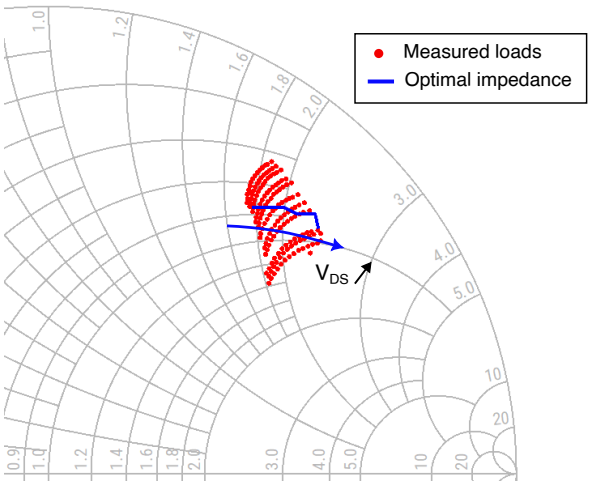

Figure 5.14: Loads extracted for all combination of varactor biases (red dots) extracted at 16.5 GHz and best impedance trajectory (blue line) extracted from load-pull simulations with V_{DS} swept from 18 V to 28 V.

Finally, Fig. 5.16 shows the insertion loss of the matching network across the selected control voltages for a 1 GHz bandwidth centered at 16.5 GHz. In this case study, substantial losses are observed across the operating band due to the introduction of multiple varactors, whereas the variation in loss across the different values of the control bias voltages V_{B1}–V_{B2} at the center frequency of 16.5 GHz is approximately 0.5 dB. Overall, the lower performance that a tunable matching network generally yields compared to a conventional matching network requires a trade-off evaluation against the efficiency improvement resulting from load adaptation.

5.4 Conclusion

This work on the implementation of varactors in OMN is in its early stages and many efforts are required to achieve a fully working PA. The necessity of first including discrete devices as standalone test structures for the characterization, results in an increase in the time required for the design phase. The creation of a varactor model is of main importance for large-signal simulations, required for extracting the PAE performances for the amplifier. Unfortunately, device models were not available at the

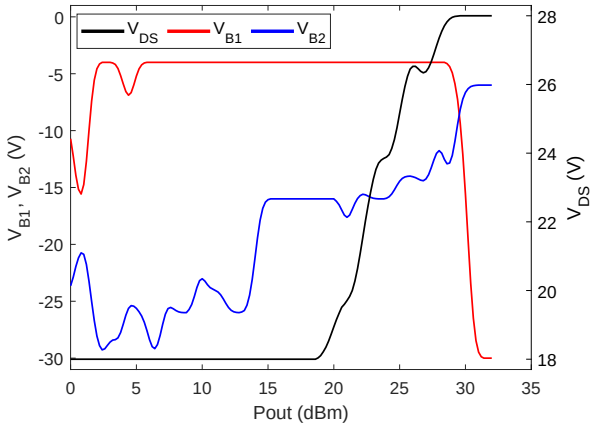

Figure 5.15: Control voltages for V_{DS}, V_{B1} and V_{B2} across output power P_{out}.

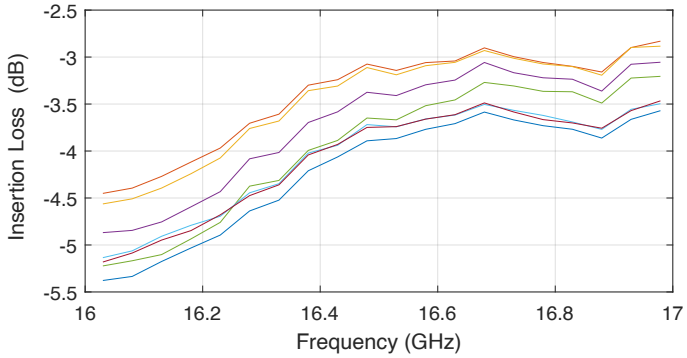

Figure 5.16: Insertion loss of the designed tunable matching network extracted from small-signal measurements at selected varactor bias voltages.

time of design due to the strict deadline for the submission of the successive foundry tape-out.

Despite poor models being used for the design, both complete amplifiers and test network structures are available for further studies. In particular, large-signal measurements will be conducted on the complete amplifiers to evaluate if the simulation results respect the observed performances on both variants. The networks realized in 120 nm technology can be fully characterized and used to simulate a complete PA to properly assess the impact of the losses introduced by series devices.

Overall, for small-signal excitations, an impact on the gain of the amplifier is visible and for some designs, the performance variation is substantial. If the losses introduced by the varactors are of modest impact, an improvement in efficiency performance could be expected. Despite the variant with decoupled varactor demonstrated reduced effects, a solution with anti-series devices could be tested as better linearity performances are also expected [144].

Chapter 6

Conclusions

6.1 Main achievements

The aim of this thesis was to introduce new approaches to address the challenges posed by emerging technologies such as 5G and 6G. These standards demand highly efficient power amplifiers capable of operating over wide bandwidths and, potentially, across multiple frequency bands. GaN technology was selected for this work, as it is one of the leading contenders in current research for applications at microwave frequencies. Thanks to the collaboration between the University of Bologna and the Microwave Engineering Center for Space Applications (MECSA), the author gained access to the NP12-00 120-nm GaN-on-SiC process and the NP15-00 150-nm GaN-on-SiC process provided by WIN Semiconductors. This advanced technology enabled the design and fabrication of multiple tiles incorporating test structures specifically tailored to the research objectives. The necessary design competencies were acquired during a six-month industrial internship at Microwave Electronics for Communications (MEC) in Bologna, Italy, a leading MMIC design center. Another key opportunity was the collaboration with the Ferdinand-Braun-Institut (FBH) during a three-month research period spent at the FBH Power Lab in Berlin. During this time, both the measurement capabilities and access to the foundry facilities proved to be highly beneficial. As a result of this collaboration, custom varactor designs were fabricated and evaluated. The whole Ph.D. work is supported by the European Union's FSE REACT-EU initiative through the Italian Ministry of University and Research under D.M. 1061/2021 - PON 'RICERCA E INNOVAZIONE' 2014-2020.

These collaborations lead to the improvement of GaN amplifiers for telecommunication, working on different fronts:

- First, a comprehensive characterization of GaN high-electron mobility transis-

tors (HEMTs) is conducted to identify the key figures-of-merit (FoMs) associated with trapping effects. In this context, a complete measurement framework is proposed with the objective of streamlining the performance evaluation process for multiple devices. Significant efforts were dedicated to the development of the pulser board, which, in combination with the measurement setup - including an oscilloscope, arbitrary signal generator, and power supply - facilitates the generation of voltage waveforms with fast edges and long periods.
When assessing the impact of the layer composition and the fabrication quality on the amount of device defects, a robust experimental evaluation is essential in conjunction with simulations based on device physics. This is particularly critical for the proposed 'buffer-free' devices, whose behavior differs significantly from that of 'classical' devices. Nevertheless, the proposed setup and extraction strategy proved to be both flexible and well-suited for identifying the main signatures of these devices. The results are published in [66, 67].

- A complete evaluation of integrated diode devices targeting their use as varactors was proposed. The evaluation objective is to assess whether these devices can be adopted in power amplifiers to provide some reconfigurability, usually unachievable due to the impact of losses and parasitics. The evaluation includes the study of integrated capacitors and multiple layout arrangements, showing the impact of both the equivalent capacitance and the quality factor obtained. A new varactor device is proposed, exploiting island structures instead of fingers, and realized in the FBH GaN-on-SiC process. Preliminary results are presented, indicating that promising performances can be achieved with further optimizations. The results are published in [145].

- A novel modeling approach targeting varactor devices has been presented. This procedure enables the generation of a lumped equivalent circuit for a varactor device or structure based on multi-bias S-parameter measurements. The process begins with the derivation of a rational function from the available data, followed by network synthesis using either the Bott-Duffin approach or minimal network synthesis. The successful modeling of multiple Schottky diodes is demonstrated, with considerations on the model's scaling properties and adherence to physical characteristics. Additionally, the modeling of more complex structures is explored, focusing on anti-series diodes and a 2x2 structure designed for implementation in a matching network. The method showed significant improvements in automating model extraction and provides greater flexibility, par-

ticularly in its ability to work with constrained frequency data. The results are detailed in a paper published in the IEEE Transactions on Microwave Theory and Techniques (TMTT). Furthermore, the application of the method to more complex structures is discussed in a conference paper presented at the International Workshop on Integrated Nonlinear Microwave and Millimetre-wave Circuits (INMMiC) 2025 in Turin.

- The impact of varactors on the PA gain metric is demonstrated and the comparison with the fixed-capacitor version shows that comparable performances are achieved. Despite sub-optimal tuning apparently worsening the increment of performances at lower drain biases, varactor bias still has some margins for trying to tune the impedance properly. The stand-alone matching network has also demonstrated good adherence with simulations. These preliminary results could be exploited for establishing the effective PAE improvement relying on measurement data and proper device models.

6.2 Future work

Many further developments could follow from the results obtained during the Ph.D. period. Some key improvements will be discussed in this section along with next research goals.

- Regarding the HEMT characterization, the measurement setup could be further extended in its capabilities by adding more half-bridges to develop a double-pulsed setup. This would allow for other types of characterizations [146, 147] to possibly be added to the current ones. From the extracted signatures, the improvements of existing models could be addressed [148], including the impact of traps. In the current state, no bias tees are present in the setup, therefore no vector measurements could be performed. The extraction of S-parameters after the pulse application can provide additional insight on the trapping behavior and location [149, 150]. From the preliminary characterization conducted, it is clear that 'buffer-free' devices need a proper model to replicate the peculiar behavior and more considerations on trap effects and identification must be made.

- On the characterization of varactors, particularly on the custom island varactors, a more extensive evaluation is worth conducting. The application of the described modeling procedure could lead to insights about the impact on the performances of different elements, like the losses introduced by the bonding

metalization. Comparison with classical fingered designs with similar active area in the same technology can be pivotal to evaluate improvements on losses, area occupation or large signal performances. Regarding the latter, a proper large-signal measurement campaign is already scheduled and it should provide better description of self-tuning effects when high RF power is injected in the device. If good results are obtained, possibly with the help of TCAD physical simulations, further adjustments could be made in the layout and more samples could be fabricated.

- The modeling procedure, at this stage, lacks a proper large-signal validation of the model with NVNA measurements. This step was not implemented due to the unavailability of the proper hardware, but is of key importance to obtain accurate simulations. The development of proper scalable model could also be considered in order to streamline the CAD simulation and let the model automatically adapt to the target varactor size.

- The PA design is in its early stage and many issues must be addressed. First, large-signal continuous wave (CW) measurements are required to fully evaluate the improvement due to the introduction of varactors. The characterization of losses is of main importance, and it also applies to the standalone matching network. The available results could be used in simulation to extract the real impact of the network on PAE performances and, if necessary, the network could be tuned and re-designed. Since the layout footprint of this first solution is relatively high, a new version could optimize the cell design by realizing a more compact anti-series structure. The impact of varactors on the linearity of the amplifier is also of interest as the PAE performances are not the only driver for modern RF amplifiers. Linearity characterization will also be tested for the independent 2x2 cell structure to better correlate the observed distortions to the self-tuning effects or parasitics of the varactors.

Bibliography

[1] H. Wang *et al.* "Power Amplifiers Performance Survey 2000-Present". [Online]. Available: https://ideas.ethz.ch/Surveys/pa-survey.html

[2] J. J. Yao, "Rf mems from a device perspective," *Journal of micromechanics and microengineering*, vol. 10, no. 4, p. R9, 2000.

[3] C. M. Andersson, M. Thorsell, and N. Rorsman, "Nonlinear characterization of varactors for tunable networks by active source–pull and load–pull," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 7, pp. 1753–1760, 2011.

[4] R. Amirpour, D. Schwantuschke, F. Van Raay, P. Brueckner, R. Quay, and O. Ambacher, "Large-Signal Modeling of a Scalable High-Q AlGaN/GaN High Electron-Mobility Varactor," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 3, pp. 922–927, 2019.

[5] L. Mainetti, L. Patrono, and A. Vilei, "Evolution of wireless sensor networks towards the internet of things: A survey," in *SoftCOM 2011, 19th international conference on software, telecommunications and computer networks.* IEEE, 2011, pp. 1–6.

[6] . "Infographic: The Growth Of The Internet Of Things". [Online]. Available: https://www.ncta.com/whats-new/infographic-the-growth-of-the-internet-of-things

[7] G. Fettweis, M. Krondorf, and S. Bittner, "Gfdm-generalized frequency division multiplexing," in *VTC Spring 2009-IEEE 69th Vehicular Technology Conference.* IEEE, 2009, pp. 1–4.

[8] J. Abdoli, M. Jia, and J. Ma, "Filtered ofdm: A new waveform for future wireless systems," in *2015 IEEE 16th international workshop on signal processing advances in wireless communications (SPAWC).* IEEE, 2015, pp. 66–70.

[9] K.-C. Chang, K.-C. Chu, H.-C. Wang, Y.-C. Lin, and J.-S. Pan, "Energy saving technology of 5g base station based on internet of things collaborative control," *IEEE Access*, vol. 8, pp. 32 935–32 946, 2020.

[10] M. H. Alsharif and R. Nordin, "Evolution towards fifth generation (5g) wireless networks: Current trends and challenges in the deployment of millimetre wave, massive mimo, and small cells," *Telecommunication Systems*, vol. 64, pp. 617–637, 2017.

[11] S. Hur, T. Kim, D. J. Love, J. V. Krogmeier, T. A. Thomas, and A. Ghosh, "Millimeter wave beamforming for wireless backhaul and access in small cell networks," *IEEE transactions on communications*, vol. 61, no. 10, pp. 4391–4403, 2013.

[12] S. Han, S. Bian *et al.*, "Energy-efficient 5g for a greener future," *Nature Electronics*, vol. 3, no. 4, pp. 182–184, 2020.

[13] H. Shin, S. Park, L. Kim, J. Kim, T. Kim, Y. Song, and S. Lee, "The future service scenarios of 6g telecommunications technology," *Telecommunications Policy*, vol. 48, no. 2, p. 102678, 2024.

[14] H. S. Bennett, R. Brederlow, J. C. Costa, P. E. Cottrell, W. M. Huang, A. A. Immorlica, J.-E. Mueller, M. Racanelli, H. Shichijo, C. E. Weitzel *et al.*, "Device and technology evolution for si-based rf integrated circuits," *IEEE Transactions on Electron Devices*, vol. 52, no. 7, pp. 1235–1258, 2005.

[15] J. D. Cressler, "Sige hbt technology: A new contender for si-based rf and microwave circuit applications," *IEEE Transactions on Microwave Theory and techniques*, vol. 46, no. 5, pp. 572–589, 1998.

[16] K. Hoo Teo, Y. Zhang, N. Chowdhury, S. Rakheja, R. Ma, Q. Xie, E. Yagyu, K. Yamanaka, K. Li, and T. Palacios, "Emerging gan technologies for power, rf, digital, and quantum computing applications: Recent advances and prospects," *Journal of Applied Physics*, vol. 130, no. 16, 2021.

[17] T. Kikkawa, M. Nagahara, N. Okamoto, Y. Tateno, Y. Yamaguchi, N. Hara, K. Joshin, and P. Asbeck, "Surface-charge controlled algan/gan-power hfet without current collapse and gm dispersion," in *International Electron Devices Meeting. Technical Digest (Cat. No. 01CH37224)*. IEEE, 2001, pp. 25–4.

[18] Y. C. Choi, M. Pophristic, H.-Y. Cha, B. Peres, M. G. Spencer, and L. F. Eastman, "The effect of an fe-doped gan buffer on off-state breakdown characteristics in algan/gan hemts on si substrate," *IEEE transactions on Electron devices*, vol. 53, no. 12, pp. 2926–2931, 2006.

[19] M. Uren, K. Nash, R. S. Balmer, T. Martin, E. Morvan, N. Caillas, S. L. Delage, D. Ducatteau, B. Grimbert, and J. C. De Jaeger, "Punch-through in short-channel algan/gan hfets," *IEEE Transactions on Electron Devices*, vol. 53, no. 2, pp. 395–398, 2006.

[20] C. Wetzel, T. Suski, J. Ager Iii, E. Weber, E. Haller, S. Fischer, B. K. Meyer, R. Molnar, and P. Perlin, "Pressure induced deep gap state of oxygen in gan," *Physical review letters*, vol. 78, no. 20, p. 3923, 1997.

[21] G. Verzellesi, L. Morassi, G. Meneghesso, M. Meneghini, E. Zanoni, G. Pozzovivo, S. Lavanga, T. Detzel, O. Häberlen, and G. Curatola, "Influence of buffer carbon doping on pulse and ac behavior of insulated-gate field-plated power algan/gan hemts," *IEEE Electron Device Letters*, vol. 35, no. 4, pp. 443–445, 2014.

[22] P. Klein, S. Binari, K. Ikossi, A. Wickenden, D. Koleske, and R. Henry, "Current collapse and the role of carbon in algan/gan high electron mobility transistors grown by metalorganic vapor-phase epitaxy," *Applied Physics Letters*, vol. 79, no. 21, pp. 3527–3529, 2001.

[23] D. Nirmal, L. Arivazhagan *et al.*, "Impact of algan back barrier in algan/gan hemt on gan substrate," in *2020 5th International Conference on Devices, Circuits and Systems (ICDCS)*. IEEE, 2020, pp. 290–293.

[24] V. Desmaris, M. Rudzinski, N. Rorsman, P. Hageman, P. Larsen, H. Zirath, T. Rodle, and H. Jos, "Comparison of the dc and microwave performance of algan/gan hemts grown on sic by mocvd with fe-doped or unintentionally doped gan buffer layers," *IEEE Transactions on electron devices*, vol. 53, no. 9, pp. 2413–2417, 2006.

[25] R. Pécheux, R. Kabouche, E. Dogmus, A. Linge, E. Okada, M. Zegaoui, and F. Medjdoub, "Importance of buffer configuration in gan hemts for high microwave performance and robustness," in *2017 47th European Solid-State Device Research Conference (ESSDERC)*. IEEE, 2017, pp. 228–231.

[26] B. Razavi, "Challenges in portable rf transceiver design," *IEEE circuits and devices magazine*, vol. 12, no. 5, pp. 12–25, 1996.

[27] A. M. Angelotti, G. P. Gibiino, T. S. Nielsen, D. Schreurs, and A. Santarelli, "Enhanced wideband active load-pull with a vector network analyzer using modulated excitations and device output match compensation," in *2020 IEEE/MTT-S International Microwave Symposium (IMS)*. IEEE, 2020, pp. 763–766.

[28] A. M. M. Mohamed, S. Boumaiza, and R. R. Mansour, "Electronically tunable doherty power amplifier for multi-mode multi-band base stations," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 4, pp. 1229–1240, 2013.

[29] R. Fagotti, A. Cidronali, and G. Manes, "Concurrent hex-band gan power amplifier for wireless communication systems," *IEEE Microwave and Wireless Components Letters*, vol. 21, no. 2, pp. 89–91, 2011.

[30] R. Mukhopadhyay, Y. Park, P. Sen, N. Srirattana, J. Lee, C.-H. Lee, S. Nuttinck, A. Joseph, J. D. Cressler, and J. Laskar, "Reconfigurable rfics in si-based technologies for a compact intelligent rf front-end," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 1, pp. 81–93, 2005.

[31] U. Kim, S. Kang, J. Woo, Y. Kwon, and J. Kim, "A multiband reconfigurable power amplifier for umts handset applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 8, pp. 2532–2542, 2012.

[32] S.-M. Yoo, J. S. Walling, E. C. Woo, B. Jann, and D. J. Allstot, "A switched-capacitor rf power amplifier," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 12, pp. 2977–2987, 2011.

[33] M. Unlu, S. Demir, and T. Akin, "A 15–40-ghz frequency reconfigurable rf mems phase shifter," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 8, pp. 2865–2877, 2013.

[34] R. Giofre, A. Del Gaudio, and E. Limiti, "A 28 ghz mmic doherty power amplifier in gan on si technology for 5g applications," in *2019 IEEE MTT-S International Microwave Symposium (IMS)*. IEEE, 2019, pp. 611–613.

[35] A. Rifi, C. Hallepee, M. Ayad, G. Neveux, and D. Barataud, "An envelope tracking oriented, 17-20ghz, average 64qam modulated 2w, pae¿ 37%, obo 8db gan

mmic power amplifier," in *2023 International Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits (INMMIC)*. IEEE, 2023, pp. 1–4.

[36] W. H. Doherty, "A new high efficiency power amplifier for modulated waves," *Proceedings of the Institute of radio engineers*, vol. 24, no. 9, pp. 1163–1182, 1936.

[37] H. Chireix, "High power outphasing modulation," *Proceedings of the Institute of Radio Engineers*, vol. 23, no. 11, pp. 1370–1392, 1935.

[38] L. R. Kahn, "Single-sideband transmission by envelope elimination and restoration," *Proceedings of the IRE*, vol. 40, no. 7, pp. 803–806, 1952.

[39] D. Tena-Ramos, F. J. Ortega-González, and M. Patiño-Gómez, "Hybrid envelope elimination and restoration technique for enhancing the linearity of switchmode envelope amplifiers," *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 2, pp. 186–188, 2017.

[40] S.-M. Yoo, J. S. Walling, O. Degani, B. Jann, R. Sadhwani, J. C. Rudell, and D. J. Allstot, "A class-g switched-capacitor rf power amplifier," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 5, pp. 1212–1224, 2013.

[41] P. Asbeck and Z. Popovic, "Et comes of age: Envelope tracking for higher-efficiency power amplifiers," *IEEE Microwave Magazine*, vol. 17, no. 3, pp. 16–25, 2016.

[42] C. Rauscher, "Large-signal technique for designing single-frequency and voltage-controlled gaas fet oscillators," *IEEE Transactions on Microwave Theory and Techniques*, vol. 29, no. 4, pp. 293–304, 1981.

[43] H. Gu, J. Wang, and L. Ge, "Circularly polarized patch antenna with frequency reconfiguration," *IEEE Antennas and Wireless Propagation Letters*, vol. 14, pp. 1770–1773, 2015.

[44] P. C. Chen, P. M. Asbeck, and S. A. Dayeh, "Freestanding high-power gan multi-fin camel diode varactors for wideband telecom tunable filters," *IEEE Transactions on Electron Devices*, vol. 70, no. 3, pp. 963–970, 2023.

[45] A. Singh and M. K. Mandal, "Electronically tunable reflection type phase shifters," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 3, pp. 425–429, 2019.

[46] E. R. Brown, "Rf-mems switches for reconfigurable integrated circuits," *IEEE Transactions on microwave theory and techniques*, vol. 46, no. 11, pp. 1868–1880, 1998.

[47] J. Nath, D. Ghosh, J.-P. Maria, A. I. Kingon, W. Fathelbab, P. D. Franzon, and M. B. Steer, "An electronically tunable microstrip bandpass filter using thin-film barium-strontium-titanate (bst) varactors," *IEEE transactions on microwave theory and techniques*, vol. 53, no. 9, pp. 2707–2712, 2005.

[48] O. Bengtsson, H. Maune, F. Gölden, S. Chevtchenko, M. Sazegar, P. Kurpas, A. Wiens, R. Jakoby, and W. Heinrich, "Discrete tunable rf-power gan-bst transistors," in *2012 42nd European Microwave Conference*. IEEE, 2012, pp. 703–706.

[49] A. Vorobiev, P. Rundqvist, K. Khamchane, and S. Gevorgian, "Silicon substrate integrated high q-factor parallel-plate ferroelectric varactors for microwave/millimeterwave applications," *Applied Physics Letters*, vol. 83, no. 15, pp. 3144–3146, 2003.

[50] A. Victor, J. Nath, D. Ghosh, S. Aygun, W. Nagy, J.-p. Maria, A. I. Kingon, and M. B. Steer, "Voltage controlled gan-on-si hfet power oscillator using thin-film ferroelectric varactor tuning," in *2006 European Microwave Conference*. IEEE, 2006, pp. 87–90.

[51] F. Svelto, S. Manzini, and R. Castello, "A three terminal varactor for rf ic's in standard cmos technology," *IEEE Transactions on Electron Devices*, vol. 47, no. 4, pp. 893–895, 2000.

[52] R. L. Bunch and S. Raman, "Large-signal analysis of mos varactors in cmos-g/sub m/lc vcos," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 8, pp. 1325–1332, 2003.

[53] A.-S. Porret, T. Melly, C. C. Enz, and E. A. Vittoz, "Design of high-q varactors for low-power wireless applications using a standard cmos process," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 3, pp. 337–345, 2000.

[54] R. Amirpour, D. Schwantuschke, P. Brueckner, R. Quay, and O. Ambacher, "AlGaN/GaN High Electron-mobility Varactors on Silicon Substrate," in *Proc. German Microwave Conf.*, 2019, pp. 244–247.

[55] A. Hamdoun, L. Roy, M. Himdi, and O. Lafond, "Characterisation and analytical modelling of GaN HEMT-based varactor diodes," *Electronics Lett.*, vol. 51, no. 23, pp. 1930–1932, 2015.

[56] C. San Chu, Y. Zhou, K. J. Chen, and K. M. Lau, "Q-factor characterization of RF GaN-based metal-semiconductor-metal planar interdigitated varactor," *IEEE electron device letters*, vol. 26, no. 7, pp. 432–434, 2005.

[57] W. Wang, Q. Li, N. An, and J. Zeng, "A novel gan-based metal-2deg-metal varactor with cutoff frequency of 3.13 thz," *IEEE Transactions on Electron Devices*, vol. 69, no. 5, pp. 2270–2274, 2022.

[58] L. F. Tiemeijer and R. J. Havens, "A calibrated lumped-element de-embedding technique for on-wafer rf characterization of high-quality inductors and high-speed transistors," *IEEE Transactions on electron devices*, vol. 50, no. 3, pp. 822–829, 2003.

[59] M. Koolen, J. Geelen, and M. Versleijen, "An improved de-embedding technique for on-wafer high-frequency characterization," in *Proc. Bipolar Circuits Technol. Meeting*. Minneapolis, MN, 1991, pp. 188–191.

[60] K. Shinohara, D. C. Regan, Y. Tang, A. L. Corrion, D. F. Brown, J. C. Wong, J. F. Robinson, H. H. Fung, A. Schmitz, T. C. Oh *et al.*, "Scaling of gan hemts and schottky diodes for submillimeter-wave mmic applications," *IEEE Transactions on Electron Devices*, vol. 60, no. 10, pp. 2982–2996, 2013.

[61] F. Jia, X. Ma, L. Yang, B. Hou, M. Zhang, Q. Zhu, M. Wu, M. Mi, J. Zhu, S. Liu *et al.*, "The influence of fe doping tail in unintentionally doped gan layer on dc and rf performance of algan/gan hemts," *IEEE Transactions on Electron Devices*, vol. 68, no. 12, pp. 6069–6075, 2021.

[62] R. P. Vaudo, X. Xu, A. Salant, J. Malcarne, and G. R. Brandes, "Characteristics of semi-insulating, fe-doped gan substrates," *physica status solidi (a)*, vol. 200, no. 1, pp. 18–21, 2003.

[63] B. M. Green, K. K. Chu, E. M. Chumbes, J. A. Smart, J. R. Shealy, and L. F. Eastman, "The effect of surface passivation on the microwave characteristics of undoped algan/gan hemts," *IEEE Electron Device Lett.*, vol. 21, no. 6, pp. 268–270, 2000.

[64] Y. Ando, Y. Okamoto, H. Miyamoto, T. Nakayama, T. Inoue, and M. Kuzuhara, "10-w/mm algan-gan hfet with a field modulating plate," *IEEE Electron Device Lett.*, vol. 24, no. 5, pp. 289–291, 2003.

[65] M. Cioni, N. Zagni, L. Selmi, G. Meneghesso, M. Meneghini, E. Zanoni, and A. Chini, "Electric field and self-heating effects on the emission time of iron traps in gan hemts," *IEEE Transactions on Electron Devices*, vol. 68, no. 7, pp. 3325–3332, 2021.

[66] S. Cangini, G. P. Gibiino, A. M. Angelotti, C. Florian, A. Santarelli, and M. Lorenzini, "Rf gan-hemt technology evaluation framework based on drain current transient measurements," in *2023 International Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits (INMMIC)*. IEEE, 2023, pp. 1–4.

[67] ——, "Experimental characterization of drain current transient effects in 'buffer-free' rf gan hemts," in *2024 15th German Microwave Conference (GeMiC)*. IEEE, 2024, pp. 33–36.

[68] T. Hashizume, S. Ootomo, T. Inagaki, and H. Hasegawa, "Surface passivation of gan and gan/algan heterostructures by dielectric films and its application to insulated-gate heterostructure transistors," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena*, vol. 21, no. 4, pp. 1828–1838, 2003.

[69] X. Zou, J. Yang, Q. Qiao, X. Zou, J. Chen, Y. Shi, and K. Ren, "Trap characterization techniques for gan-based hemts: A critical review," *Micromachines*, vol. 14, no. 11, p. 2044, 2023.

[70] A. Santarelli *et al.*, "A double-pulse technique for the dynamic i/v characterization of gan fets," *IEEE Microw. Wirel. Compon. Lett.*, vol. 24, no. 2, pp. 132–134, 2013.

[71] J. L. Gomes, L. C. Nunes, C. F. GonÃ§alves, and J. C. Pedro, "An accurate characterization of capture time constants in gan hemts," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 7, pp. 2465–2474, 2019.

[72] G. P. Gibiino, A. Santarelli, and F. Filicori, "A gan hemt global large-signal model including charge trapping for multibias operation," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 11, pp. 4684–4697, 2018.

[73] J. Pedro, J. Gomes, and L. Nunes, "Electro-thermal and trapping characterization of algan/gan rf power hemts," in *Proc. IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symp.*, 2021, pp. 1–6.

[74] G. P. Gibiino, C. Florian, A. Santarelli, T. Cappello, and Z. Popović, "Isotrap pulsed *iv* characterization of gan hemts for pa design," *IEEE Microw. Wirel. Compon. Lett.*, vol. 28, no. 8, pp. 672–674, 2018.

[75] J. Joh and J. A. Del Alamo, "A current-transient methodology for trap analysis for gan high electron mobility transistors," *IEEE Trans. Electron Devices*, vol. 58, no. 1, pp. 132–140, 2010.

[76] S. A. Albahrani and A. E. Parker, "Characterization of trapping and thermal dispersion in gan hemts," in *IEEE/MTT-S Int. Microw. Symp. Dig.*, 2010, pp. 413–416.

[77] S. A. Albahrani, A. E. Parker, and M. Heimlich, "Identifying a double-energy-level trap center in a gan hemt by performing three-stage pulse measurements," *IEEE Trans. Electron Devices*, vol. 63, no. 9, pp. 3693–3699, 2016.

[78] J. Couvidat *et al.*, "Investigation of fast and slow charge trapping mechanisms of gan/a1gan hemts through pulsed iv measurements and the associated new trap model," in *IEEE/MTT-S Int. Microw. Symp. Dig.*, 2018, pp. 720–723.

[79] A. M. Angelotti, G. P. Gibiino, A. Santarelli, and C. Florian, "Experimental characterization of charge trapping dynamics in 100-nm aln/gan/algan-on-si hemts by wideband transient measurements," *IEEE Trans. Electron Devices*, vol. 67, no. 8, pp. 3069–3074, 2020.

[80] A. M. Angelotti *et al.*, "Trapping dynamics in GaN HEMTs for millimeter-wave applications: Measurement-based characterization and technology comparison," *Electronics*, vol. 10, no. 2, p. 137, 2021.

[81] S. Rajasingam, J. Pomeroy, M. Kuball, M. Uren, T. Martin, D. Herbert, K. Hilton, and R. Balmer, "Micro-raman temperature measurements for electric field assessment in active algan-gan hfets," *IEEE Electron Device Letters*, vol. 25, no. 7, pp. 456–458, 2004.

[82] R. Aubry, J.-C. Jacquet, J. Weaver, O. Durand, P. Dobson, G. Mills, M.-A. di Forte-Poisson, S. Cassette, and S.-L. Delage, "Sthm temperature mapping

and nonlinear thermal resistance evolution with bias on algan/gan hemt devices," *IEEE transactions on electron devices*, vol. 54, no. 3, pp. 385–390, 2007.

[83] C. Florian *et al.*, "Characterization of the nonlinear thermal resistance and pulsed thermal dynamic behavior of AlGaN–GaN HEMTs on SiC," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 5, pp. 1879–1891, 2013.

[84] J. Joh, J. A. Del Alamo, U. Chowdhury, T.-M. Chou, H.-Q. Tserng, and J. L. Jimenez, "Measurement of channel temperature in gan high-electron mobility transistors," *IEEE Trans. Electron Devices*, vol. 56, no. 12, pp. 2895–2901, 2009.

[85] D. Bisi, M. Meneghini, C. De Santi, A. Chini, M. Dammann, P. Brueckner, M. Mikulla, G. Meneghesso, and E. Zanoni, "Deep-level characterization in gan hemts - part i: Advantages and limitations of drain current transient measurements," *IEEE Transactions on electron devices*, vol. 60, no. 10, pp. 3166–3175, 2013.

[86] D. Lang, "Deep-level transient spectroscopy: A new method to characterize traps in semiconductors," *Journal of applied physics*, vol. 45, no. 7, pp. 3023–3032, 1974.

[87] T. Mizutani, T. Okino, K. Kawada, Y. Ohno, S. Kishimoto, and K. Maezawa, "Drain current dlts of algan/gan hemts," *physica status solidi (a)*, vol. 200, no. 1, pp. 195–198, 2003.

[88] M. Ťapajna, R. J. Simms, Y. Pei, U. K. Mishra, and M. Kuball, "Integrated optical and electrical analysis: Identifying location and properties of traps in algan/gan hemts during electrical stress," *IEEE Electron Device Letters*, vol. 31, no. 7, pp. 662–664, 2010.

[89] D. K. Schroder, *Semiconductor material and device characterization.* John Wiley & Sons, 2015.

[90] A. Chini, F. Soci, M. Meneghini, G. Meneghesso, and E. Zanoni, "Deep levels characterization in gan hemts - part ii: Experimental and numerical evaluation of self-heating effects on the extraction of traps activation energy," *IEEE transactions on electron devices*, vol. 60, no. 10, pp. 3176–3182, 2013.

[91] P. V. Raja *et al.*, "Estimation of Trapping Induced Dynamic Reduction in 2DEG Density of GaN-Based HEMTs by Gate-Lag DCT Technique," *IEEE Trans. Electron Devices*, vol. 69, no. 9, pp. 4864–4869, 2022.

[92] A. Alemanno, A. M. Angelotti, G. P. Gibiino, A. Santarelli, E. Sangiorgi, and C. Florian, "A reconfigurable setup for the on-wafer characterization of the dynamic r on of 600 v gan switches at variable operating regimes," *Electronics*, vol. 12, no. 4, p. 1063, 2023.

[93] A. Chini *et al.*, "Deep Levels Characterization in GaN HEMTs - Part II: Experimental and Numerical Evaluation of Self-Heating Effects on the Extraction of Traps Activation Energy," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3176–3182, 2013.

[94] J.-T. Chen *et al.*, "A gan–sic hybrid material for high-frequency and power electronics," *Applied Physics Lett.*, vol. 113, no. 4, 2018.

[95] B. Hult, M. Thorsell, J.-T. Chen, and N. Rorsman, "High voltage and low leakage gan-on-sic mishemts on a "buffer-free" heterostructure," *IEEE Electron Device Letters*, vol. 43, no. 5, pp. 781–784, 2022.

[96] D.-Y. Chen, A. Malmros, M. Thorsell, H. Hjelmgren, O. Kordina, J.-T. Chen, and N. Rorsman, "Microwave performance of 'buffer-free' gan-on-sic high electron mobility transistors," *IEEE Electron Device Letters*, vol. 41, no. 6, pp. 828–831, 2020.

[97] G. Zhan *et al.*, "Transconductance overshoot, a new trap-related effect in algan/gan hemts," *IEEE Trans. Electron Devices*, 2023.

[98] K. Ma, T. B. Kumar, and K. S. Yeo, "A Reconfigurable K-/Ka-Band Power Amplifier With High PAE in 0.18-*mu*m SiGe BiCMOS for Multi-Band Applications," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 12, pp. 4395–4405, 2015.

[99] D. Kim and S. Jeon, "W-and G-band GaN voltage-controlled oscillators with high output power and high efficiency," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 8, pp. 3908–3916, 2021.

[100] M. C. Robinson, Z. Popović, and G. Lasser, "Linear broadband interference suppression circuit based on GaN monolithic microwave integrated circuits," *IET Circuits Devices Syst.*, vol. 17, no. 4, pp. 213–224, 2023.

[101] P. Neininger, R. Amirpour, L. John, C. Friesicke, R. Quay, and T. Zwick, "A phase shifter with integrated PA MMIC for Ka-band frequencies," in *Proc. German Microwave Conf.*, 2020, pp. 13–16.

[102] A. Romano, T. Sonnenberg, and Z. Popović, "50–110-GHz Continuous GaN MMIC Reflective Phase Shifters," *IEEE Trans. Microw. Theory Techn.*, vol. 72, no. 3, pp. 1634–1642, 2024.

[103] P. Neininger, P. Brückner, and R. Quay, "mm-wave gan varactors and e/w-band phase shifter," in *2024 19th European Microwave Integrated Circuits Conference (EuMIC)*. IEEE, 2024, pp. 239–242.

[104] W. M. Y. Wong, P. S. Hui, Z. Chen, K. Shen, J. Lau, P. C. Chan, and P.-K. Ko, "A wide tuning range gated varactor," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 5, pp. 773–779, 2000.

[105] E. Arabi, C. Gamlath, K. Morris, and M. Beach, "A comparison of lumped-based tunable matching networks for dynamically-load-modulated power amplifiers," in *Proc. IEEE Asia-Pacific Microw. Conf.*, 2017, pp. 33–36.

[106] W. Hallberg, D. Gustafsson, M. Özen, C. M. Andersson, D. Kuylenstierna, and C. Fager, "A class-J power amplifier with varactor-based dynamic load modulation across a large bandwidth," in *IEEE MTT-S Int. Microw. Symp. Dig*, 2015, pp. 1–4.

[107] H. Maune, M. Sazegar, and R. Jakoby, "Tunable impedance matching networks for agile rf power amplifiers," in *IEEE MTT-S Int. Microw. Symp. Dig.*, 2011, pp. 1–4.

[108] Y. Oh and J.-S. Rieh, "A comprehensive study of high-q island-gate varactors (igvs) for cmos millimeter-wave applications," *IEEE transactions on microwave theory and techniques*, vol. 59, no. 6, pp. 1520–1528, 2011.

[109] Y. Oh, S. Kim, S. Lee, and J.-S. Rieh, "The island-gate varactor - a high-q mos varactor for millimeter-wave applications," *IEEE microwave and wireless components letters*, vol. 19, no. 4, pp. 215–217, 2009.

[110] C. M. Andersson, B. Magnusson, N. Henelius, and N. Rorsman, "Epitaxial and layout optimization of sic microwave power varactors," in *Asia-Pacific Microwave Conference 2011*. IEEE, 2011, pp. 1642–1645.

[111] D. E. Root, "Future device modeling trends," *IEEE Microwave Magazine*, vol. 13, no. 7, pp. 45–59, 2012.

[112] A. García-Luque, T. M. Martín-Guerrero, and F. J. Mata-Contreras, "Relaxation-time modeling for nqs phenomena characterization in high-frequency diodes," in *2023 International Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits (INMMIC)*. IEEE, 2023, pp. 1–3.

[113] A. García-Luque, T. Martín-Guerrero, A. Santarelli, and C. Camacho-Peñalosa, "Automatic nonlinear nonquasi-static diode model extraction from large-signal measurements," in *2021 16th European Microwave Integrated Circuits Conference (EuMIC)*. IEEE, 2022, pp. 374–377.

[114] C.-C. Chou and J. E. Schutt-Ainé, "Equivalent circuit synthesis of multiport s parameters in pole–residue form," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 11, no. 11, pp. 1971–1979, 2021.

[115] A. García-Luque, T. Martín-Guerrero, and F. Mata-Contreras, "Varactor characterization procedure for large-signal high-frequency applications," in *2023 18th European Microwave Integrated Circuits Conference (EuMIC)*. IEEE, 2023, pp. 105–108.

[116] A. Hamdoun, M. Himdi, R. Langis, and O. Lafond, "Large signal and analytic non-linear modelling of GaN HEMT-based varactors," in *Proc. IEEE Int. Conf. Electron Devices and Solid-State Circ.*, 2019, pp. 1–3.

[117] C. Florian, S. D'Angelo, D. Resca, and F. Scappaviva, "A chip set of low phase noise MMIC VCOs at C, X and Ku band in InGaP-GaAs HBT technology for satellite telecommunications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, 2017, pp. 1148–1151.

[118] M. Berljafa and S. Guttel, "The rkfit algorithm for nonlinear rational approximation," *SIAM Journal on Scientific Computing*, vol. 39, no. 5, pp. A2049–A2071, 2017.

[119] Y. Nakatsukasa, O. Sète, and L. N. Trefethen, "The aaa algorithm for rational approximation," *SIAM Journal on Scientific Computing*, vol. 40, no. 3, pp. A1494–A1522, 2018.

[120] B. Gustavsen and A. Semlyen, "Rational approximation of frequency domain responses by vector fitting," *IEEE Transactions on power delivery*, vol. 14, no. 3, pp. 1052–1061, 1999.

[121] C.-K. Liao, C.-Y. Chang, and J. Lin, "A vector-fitting formulation for parameter extraction of lossy microwave filters," *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 4, pp. 277–279, 2007.

[122] P. Zhao and M. Rao, "Design and tuning of extracted-pole filters with non-resonant nodes by circuit model extraction," *IEEE Transactions on Microwave Theory and Techniques*, vol. 70, no. 4, pp. 2174–2184, 2022.

[123] F. Solgun and D. P. DiVincenzo, "Multiport impedance quantization," *Annals of physics*, vol. 361, pp. 605–669, 2015.

[124] D. C. Youla, *Theory and synthesis of linear passive time-invariant networks*. Cambridge University Press, 2015.

[125] A. M. Angelotti, G. P. Gibiino, and A. Santarelli, "Efficient implementation of a modified-Volterra radio-frequency power amplifier nonlinear dynamic model by global rational functions approximation," *Int. J. of RF and Microwave Computer-Aided Engineering*, vol. 30, no. 11, p. e22392, 2020.

[126] E. Ngoya, C. Quindroit, and J. M. Nebus, "On the continuous-time model for nonlinear-memory modeling of RF power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 12, pp. 3278–3292, 2009.

[127] B. Gustavsen and A. Semlyen, "Enforcing passivity for admittance matrices approximated by rational functions," *IEEE Trans. Power Systems*, vol. 16, no. 1, pp. 97–104, 2001.

[128] O. Wing, *Classical circuit theory*. Springer Science & Business Media, 2008, vol. 773.

[129] F. Mukhtar and P. Russer, "Brune's algorithm for lumped element equivalent circuit synthesis of linear lossy multiports," *AEU-International J. of Electronics and Communications*, vol. 76, pp. 175–187, 2017.

[130] O. Brune, "Synthesis of a finite two-terminal network whose driving-point impedance is a prescribed function of frequency," Ph.D. dissertation, Massachusetts Institute of Technology, 1931.

[131] T. H. Hughes and M. C. Smith, "On the minimality and uniqueness of the Bott–Duffin realization procedure," *IEEE Trans. Automatic Control*, vol. 59, no. 7, pp. 1858–1873, 2014.

[132] T. H. Hughes, "Minimal series–parallel network realizations of bicubic impedances," *IEEE Trans. Automatic Control*, vol. 65, no. 12, pp. 4997–5011, 2020.

[133] S. Y. Zhang, J. Z. Jiang, H. L. Wang, and S. Neild, "Synthesis of essential-regular bicubic impedances," *Int. J. Circuit Theory and Applications*, vol. 45, no. 11, pp. 1482–1496, 2017.

[134] J. Z. Jiang and M. C. Smith, "Regular positive-real functions and five-element network synthesis for electrical and mechanical networks," *IEEE Trans. Automatic Control*, vol. 56, no. 6, pp. 1275–1290, 2010.

[135] S. C. Cripps, *Advanced techniques in RF power amplifier design*. Artech House, 2002.

[136] E. Arabi, C. Gamlath, K. Morris, and M. Beach, "A comparison of lumped-based tunable matching networks for dynamically-load-modulated power amplifiers," in *2017 IEEE Asia Pacific Microwave Conference (APMC)*. IEEE, 2017, pp. 33–36.

[137] H. M. Nemati, C. Fager, U. Gustavsson, R. Jos, and H. Zirath, "Design of varactor-based tunable matching networks for dynamic load modulation of high power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 5, pp. 1110–1118, 2009.

[138] W. E. Neo, Y. Lin, X.-D. Liu, L. C. De Vreede, L. E. Larson, M. Spirito, M. J. Pelk, K. Buisman, A. Akhnoukh, A. De Graauw *et al.*, "Adaptive multi-band multi-mode power amplifier using integrated varactor-based tunable matching networks," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 9, pp. 2166–2176, 2006.

[139] C. Hoarau, N. Corrao, J.-D. Arnould, P. Ferrari, and P. Xavier, "Complete design and measurement methodology for a tunable rf impedance-matching network," *IEEE transactions on microwave theory and techniques*, vol. 56, no. 11, pp. 2620–2627, 2008.

[140] R. Amirpour, R. Darraji, F. Ghannouchi, and R. Quay, "Enhancement of the broadband efficiency of a class-j power amplifier with varactor-based dynamic load modulation," *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 2, pp. 180–182, 2017.

[141] W. Lu, L. Wang, S. Gu, P. M. Asbeck, and P. K. Yu, "Critical design considerations for gan-based microwave power varactors," in *2012 IEEE International Conference on Electron Devices and Solid State Circuit (EDSSC)*. IEEE, 2012, pp. 1–4.

[142] K. Buisman, C. Huang, A. Akhnoukh, M. Marchetti, L. De Vreede, L. Larson, and L. Nanver, "Varactor topologies for rf adaptivity with improved power handling and linearity," in *2007 IEEE/MTT-S International Microwave Symposium*. IEEE, 2007, pp. 319–322.

[143] R. Amirpour, D. Schwantuschke, P. Brueckner, R. Quay, and O. Ambacher, "High-q anti-series algan/gan high electron-mobility varactor," in *2019 IEEE MTT-S International Microwave Symposium (IMS)*. IEEE, 2019, pp. 599–602.

[144] D. Berthiaume, J.-J. Laurin, and N. G. Constantin, "Anti-series varactor network with improved linearity performances in the presence of inductive and capacitive parasitics," *IEEE Access*, vol. 9, pp. 48 325–48 340, 2021.

[145] S. Cangini *et al.*, "Evaluation of integrated gan diodes as varactors for tunable mmic pas from c-to k-band," in *2024 19th European Microw. Integrated Circuits Conf. (EuMIC)*. IEEE, 2024, pp. 14–17.

[146] D. Bisi, A. Stocco, M. Meneghini, F. Rampazzo, A. Cester, G. Meneghesso, and E. Zanoni, "High-voltage double-pulsed measurement system for gan-based power hemts," in *2014 IEEE International Reliability Physics Symposium*. IEEE, 2014, pp. CD–11.

[147] A. Santarelli, R. Cignani, D. Niessen, P. A. Traverso, and F. Filicori, "New pulsed measurement setup for gan and gaas fets characterization," *International Journal of Microwave and Wireless Technologies*, vol. 4, no. 3, pp. 387–397, 2012.

[148] C. Florian, G. P. Gibiino, and A. Santarelli, "Characterization and modeling of rf gan switches accounting for trap-induced degradation under operating regimes," *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 12, pp. 5491–5500, 2018.

[149] J. L. Gomes, L. C. Nunes, and J. C. Pedro, "Transient pulsed s-parameters for trapping characterization," in *2020 International Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits (INMMiC)*. IEEE, 2020, pp. 1–3.

[150] P. Luo, O. Bengtsson, and M. Rudolph, "A drain lag model for gan hemt based on chalmers model and pulsed s-parameter measurements," in *2017 IEEE MTT-S International Microwave Symposium (IMS)*. IEEE, 2017, pp. 240–243.