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DESIGN OF HIGH-PERFORMANCE ELECTRONIC POWER CONVERTERS BASED ON GAN-ON-SI SEMICONDUCTORS DEVICES

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Abstract

In recent times, automotive world has been witnessing a paradigm change: hybrid, plug-in hybrid and battery electric vehicles (HEVs, PHEVs, BEVs) are progressively replacing the internal combustion engine vehicles (ICEVs) in circulation. A strong motivation derives from the carbon dioxide (CO_2) emission performance standards that have been set by several legislative institutions aiming to tackle climate change challenges, as in the case of Regulation EU 2019/631 of the European Parliament.

Consequently, electric vehicles have experienced a significant growth in sales reaching over 250 000 new registrations per week worldwide in 2023, which exceeds the annual total that has been recorded in 2013. Although the market is spreading globally, there is still a concentration in a few major markets (such as China, Europe and United States). Given the growing interest among the population, the electrification of the global vehicle fleet is expected to continue to grow at a high rate of speed also in the coming future, and not limited to passenger light-duty vehicles, but also extended to light commercial vehicles, 2/3-wheelers, buses and trucks, significantly reducing in this way the gap with the Net Zero Emissions (NZE) targets.

In this context, power electronics is assuming a pivotal role in automotive industry. In fact, an increase of just few percentage points in terms of efficiency or power density can make a huge difference for the driving range, since they have a direct influence on size, weight, charging time and cost of the EV major components (batteries, electric motors, and power electronic converters). Considering also the concerns related to the low profit margins, the development of top-performing and cost-effective power converters (AC/DC, DC/DC, DC/AC) is of crucial importance for automotive players.

In this framework, semiconductor companies and foundries, as well as passive components manufacturers and research institutions, are continuously engaged in research and innovation in order to propose technology refinements or breakthroughs. In the last decades, the Wide Band Gap (WBG) technology, based on Gallium Nitride and Silicon Carbide semiconductors, has had a disruptive impact on power electronics, paving the way for a new generation of power components, targeting not only the automotive market but also other applications such as home appliances, mobile charges, datacenters, railways, robotics and industrial motor drives.

The objective of this thesis is to explain the design approach that has been followed to pursue the development of a top notch GaN-based Bi-directional OBC (On-Board Charger) prototype for automotive application, also emphasizing the challenges posed by the adoption of such technology. By partnering with a specialized company, the final product, after being fully tested and certified, will enter mass production exhibiting state-of-the-art performance.

Acknowledgements

I want to thank professor Corrado Florian for his incredible support during my whole PhD journey. A special mention goes to Arca Tecnologie and its fantastic team of engineers. I learned a lot.

To my family.

Chapter 1

Introduction

Recently, the heritage Silicon-based technology is facing difficulties to meet the high demanding requirements imposed by the power electronic market trends: having reached its theoretical performance limit, designers are progressively moving towards Gallium Nitride (GaN) and Silicon Carbide (SiC) solutions. Despite the lower heritage in the wafer manufacturing process and the higher cost of the device, the adoption of WBG semiconductors relies on some notable and clear advantages in terms of design FOMs (Figure of Merits). In fact, the high power density targets (currently up to 4 kW/L for the OBCs in the medium power range) are leading to the implementation of an increasingly high switching frequency [1], which can ensure greater compactness, due to the shrinking of passive components (transformers and LC/CL filters), and superior dynamics because of the corresponding wider bandwidth. On the other hand, since in hard-switching topologies the switching losses are proportional to the switching frequency, the exploitation of power switches that exhibit a strong reduction both in capacitive and inductive parasitics is of fundamental importance in order to minimize the losses and achieve high efficiency (> 96 %) converters. For OBCs in the medium-voltage/medium-power class, 650 V-25 mΩ GaN HEMTs (High Electron Mobility transistors) can represent an excellent choice. Further enhancements in efficiency (> 98 %) can be reached by means of soft-switching topologies (with Zero Voltage Switching and Zero Current Switching behaviour) which can ensure practically negligible switching losses [2].

Looking at the physical properties of semiconductors [3,4] in Figure 1.1, GaN appears particularly suited for high switching frequency applications benefiting from its excellent electron mobility and saturation velocity, which also guarantee a low channel resistance.

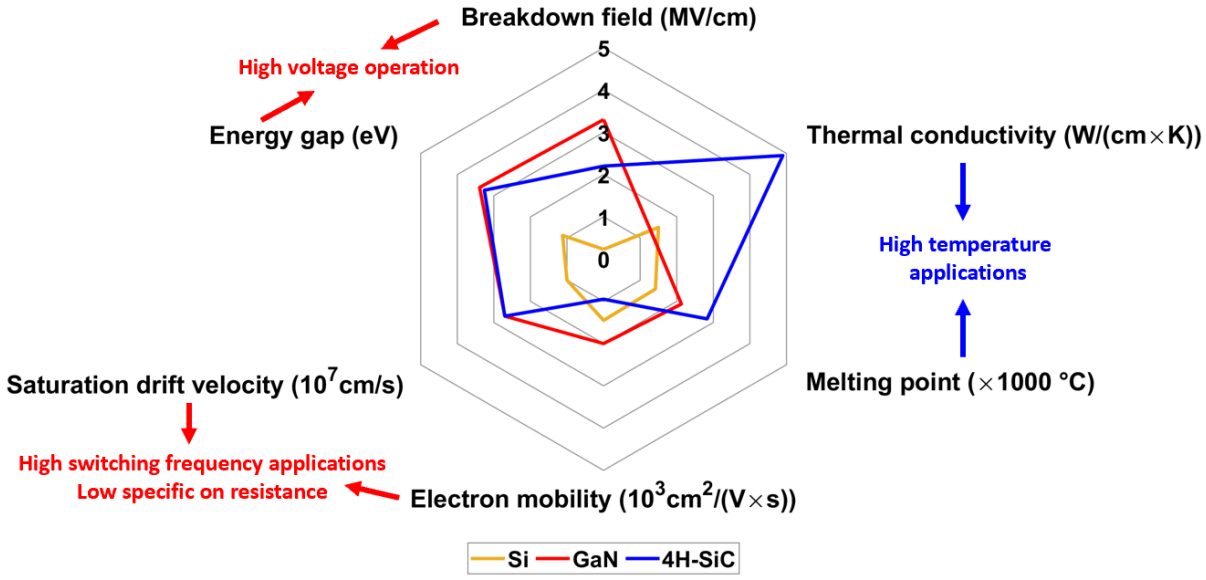


Figure 1.1 Physical properties of Si, GaN and SiC.

From the first release of E-mode GaN-on-Silicon in 2009, GaN power switches have come across almost two decades of innovations [5]. At the present time, automotive-grade 650 V-25 mΩ devices represent the best technology in the market for medium-voltage class applications. In the last few years, several semiconductor companies have released or announced GaN power ICs which also feature monolithic integration of the gate driver [6] and further R&D activities are exploring the development of two-gate monolithic bidirectional switches with bipolar blocking voltage capability and bidirectional current control, which are expected to be the next breakthrough in power electronics [7,8]. However, at the moment GaN HEMT discrete devices are the most mature and available technology provided by several semiconductor suppliers in the market.

Nevertheless, GaN adoption comes along with some specific design challenges: the very high slew rates of voltage and current (dv/dt and di/dt) at commutations – up to hundreds of volts per nanosecond and ten amps per nanosecond – make it necessary to assess, minimize and compensate any parasitics of the circuit during the design phase, at any level: PCB layout, stray inductance of active/passive components, transistor-to-heatsink capacitance, transformer interwinding capacitance, as well as busbars and others mechanical connections – otherwise several issues may arise in terms of reliability (gate/drain overvoltages and current spikes), electromagnetic interference (ringing, oscillation, common-mode conductive paths) and performance degradation (higher losses, higher distortion and lower dynamics) [9-11].

Furthermore, as depicted in Figure 1.2, also device cost can be a limiting factor, although GaN is believed to become less expensive in the next future benefiting from economies of scale.

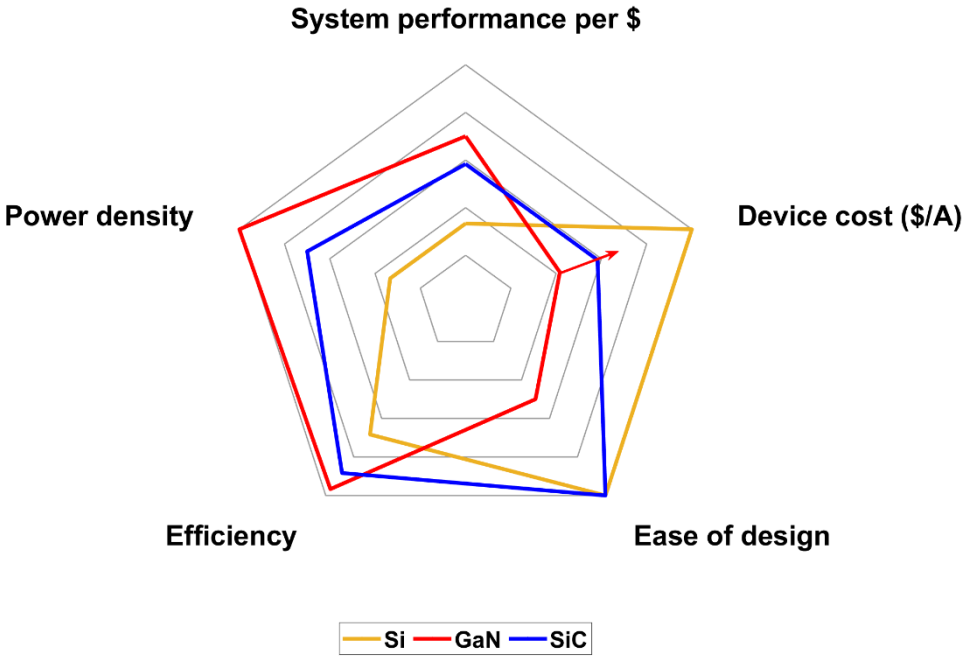


Figure 1.2 Converter design FOMs exploiting Si, GaN and SiC devices [12].

In addition, GaN commercial devices are actually restricted to a maximum blocking voltage of 650 V: as lateral devices, foundries are facing difficulties to develop 1200 V GaN power switches that exhibit a low channel resistance, since the trade-off between breakdown and channel conductivity is very tough. Multilevel topologies can overcome this limitation but cost and design complexity (in terms of control scheme, containment of parameters spread and balancing of layout parasitics) are significantly increased.

Taking into consideration all these characteristics, as shown in Figure 1.3, Gallium Nitride can be considered the optimum solution for medium voltage and medium power applications, especially if high switching frequency is required to achieve superior dynamics and power densities. On the other hand, Silicon Carbide is particularly suitable for high voltage, high power and high temperature application fields.

Not least, Silicon will remain the baseline technology especially in case of converters in low and medium power classes due to its long heritage in manufacturing process, as well as the wider availability and lower cost.

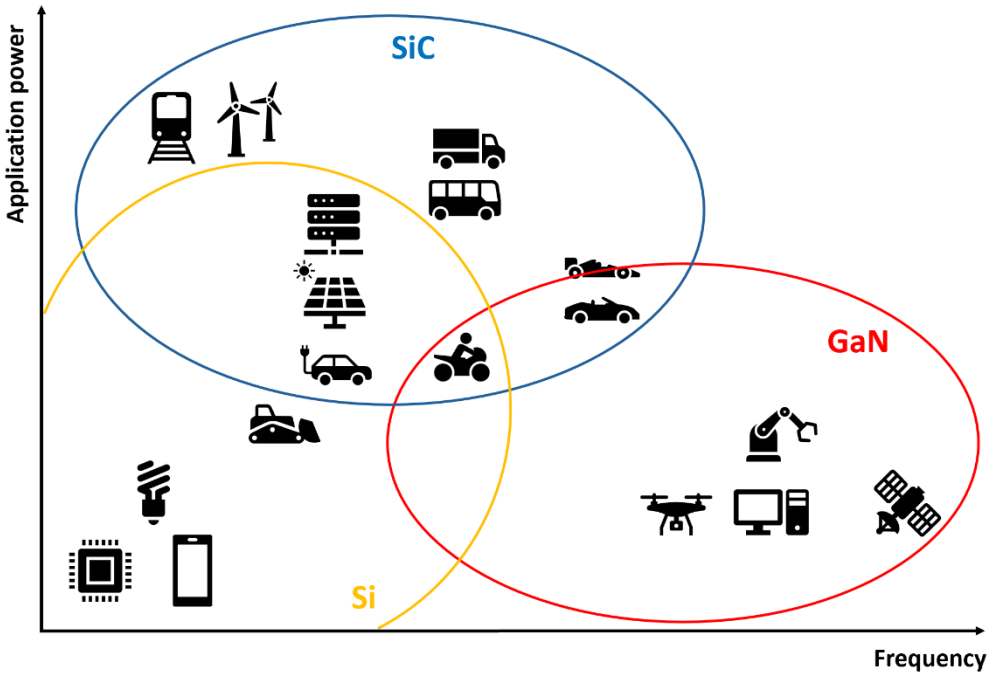


Figure 1.3 Typical application areas of Si, GaN and SiC technologies.

Going into the details of the automotive field, electric vehicles (EVs) were introduced into the market in 2010s with a nominal battery voltage of around 400 V because of the wider availability of automotive-qualified components for that voltage range [13]. Nowadays, despite the increasing interest to move towards higher DC-link voltages, 400-V powertrain represents the most mature and suited technology not only for small and medium cars but also for electric sport motorcycles. In fact, as depicted in Figure 1.4, higher voltage batteries enable superior performances in terms of charging speed and global weight reduction but this is at the expense of higher cost, bulkier housing and more complex BMS (Battery Management System) [5,6].

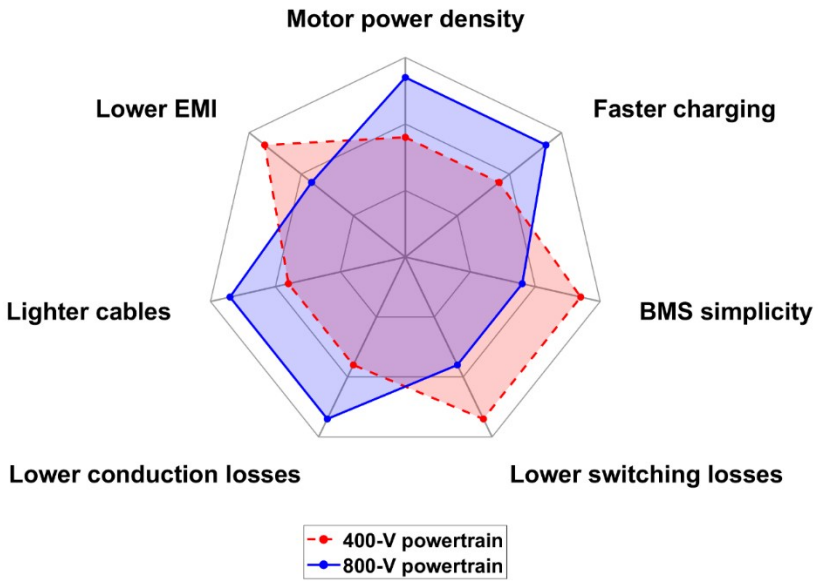


Figure 1.4 Comparison of 400/800-V powertrains based on system FOMs [5,6].

At the present time, a large part – around 80 % – of BEVs (Battery Electric Vehicles) is equipped with 400-V batteries, even if 800-V share is believed to increase up to 40 % in the next ten years. As a result, the development of top-notch power converters for 400-V powertrains is highly motivated by the EV market demand and is propelled by a continuous technology innovation in power electronics.

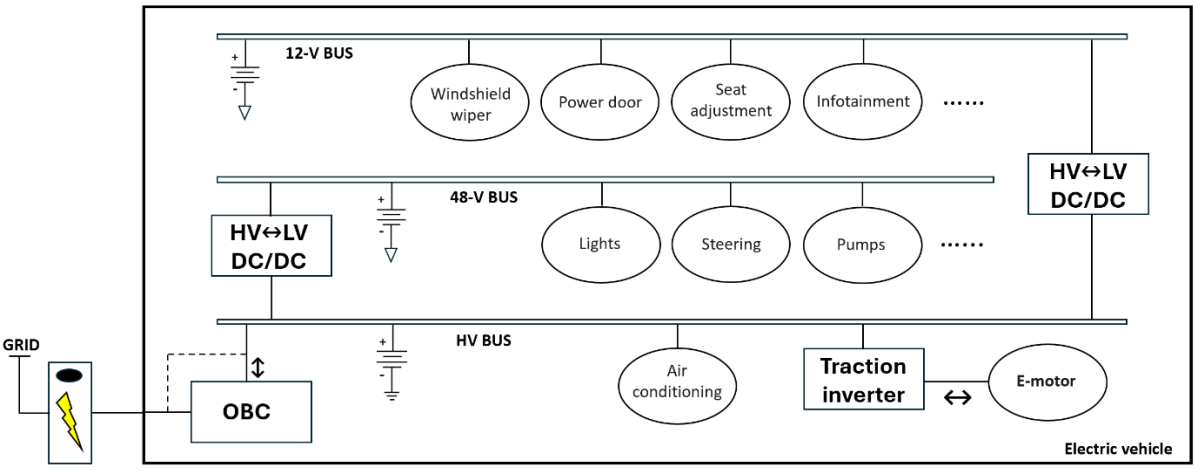


Figure 1.5 EV powertrain system.

As can be seen from Figure 1.5, an EV powertrain system typically includes several voltage buses, each one with specific load characteristics and function. It is evident that multiple semiconductor technologies can be integrated in such miscellaneous and complex architecture, with cost and performance targets playing an essential role in design choices.

One increasingly demanded feature is the bidirectional power flow capability of the power converters. The exploitation of bidirectional devices and suitable control algorithms enable to implement operation modes such as the V2G/V2L (Vehicle to Grid/Vehicle to Load) and the limp-home feature with regard to the On-Board Charger, and the energy recuperation (or regenerative braking) as far as the traction inverter.

In this thesis, the design and realization of a GaN-based high-power density 450-V, 6.6 kW OBC with bidirectional power flow capability and integration of an auxiliary DC-DC converter (for interconnection to the 12-V service battery) are described. After presenting the main requirements to be satisfied, topology choices, design challenges and trade-offs are detailed in Chapter 2, supported by electrical and thermal simulations performed through PSIM software package. In Chapter 3, the optimization process of the On-Board Charger PCB layout that has been carried out by means of several electrical and electromagnetic (EM) simulations in Keysight Advanced Design System (ADS) is explained with particular reference to the HV DC-DC converter stage. To this aim, the Pspice non-linear dynamic model of the transistor has been exploited and the layout parasitics have been extracted and taken into consideration through a multi-port S-parameters matrix representation. Also, some interesting peculiarities of

GaN devices at commutations are deeply discussed. One for all, a Miller voltage below the threshold in case of a strong driver at turn-off is reported.

Chapter 2

Design of a High Power Density GaN-based, 6.6-kW, 450-V, Bi-directional On-Board Charger with Integrated 1-kW, 12-V Auxiliary DC-DC Converter

Automotive-grade GaN power switches have been made recently available in the market from a growing number of semiconductor suppliers. The exploitation of this technology enables the development of very efficient power converters operating at much higher switching frequency with respect to components implemented with silicon power devices. Therefore, a new generation of automotive power components with an increased power density is expected to replace the silicon-based counterparts, especially in case of high performance electric and hybrid vehicles. 650 V GaN-on-Silicon power switches are particularly suitable for the development of 3-7 kW OBCs for electric cars and motorcycles equipped with a 400 V voltage battery pack. In this Chapter the design and implementation of a 6.6 kW OBC for electric vehicles using automotive-grade 650 V, 25 mΩ discrete GaN switches are described. The OBC allows bi-directional power flow, since it is composed by a bridgeless interleaved totem-pole PFC AC/DC active front end, followed by a Dual Active Bridge (DAB) DC-DC converter. The prototype can operate from a single phase 90-264 Vrms AC grid to a 200-450 V high-voltage (HV) battery with 96% overall efficiency at the maximum ambient temperature of 60 °C. It also provides the integration of an auxiliary 1 kW DC-DC converter to connect the HV battery to the 12 V battery of the vehicle. The auxiliary DC-DC converter is realized in a center-tapped phase shifted full bridge (PSFB) topology with synchronous rectification. The entire OBC is liquid cooled.

With regard to the specifications of the AC/DC active front end, it is required to comply with several AC charging markets (above all EU, USA, China and Japan). Hence, the PFC (Power Factor Correction) AC/DC stage is capable of handling a wide range (90-264 Vrms, 50/60 Hz) of AC mains supply.

A second stage (the DC-DC HV converter) is used to regulate the battery voltage and current, both in G2V and V2G/V2L operation modes with a battery voltage range between 200 V and 450 V. An auxiliary DC-DC LV (low-voltage) stage is used to connect the 12-V service battery with bidirectional capability, charging the low-voltage battery from the HV DC-rail as well as providing features such as limp-home and inverter DC-link capacitor's precharge from the low-voltage battery. Table 2.1 lists the OBC main specifications while Figure 2.1 displays the designed system topology.

Table 2.1 OBC main specifications.

PFC stage					
AC grid range		**$V_{out,nominal}$**		**$P_{out,\ nominal}$**	
90-264 Vrms		400 V		6.6 kW	
DC-DC HV stage					
$V_{in,nominal}$	**$V_{out,range}$**	**$V_{out,nominal}$**	**$I_{out,nominal}$**	**$P_{out,nominal}$**	**$P_{out,max}$**
400 V	200-450 V	400 V	16.5 A	6.6 kW	7 kW
DC-DC LV stage					
$V_{in,range}$	**$V_{in,nominal}$**	**$V_{out,range}$**	**$V_{out,nominal}$**	**$P_{out,nominal}$**	**$P_{out,max}$**
240-450 V	360 V	10-16 V	12 V	800 W	1 kW
Additional requirements					
Bidirectional power flow CISPR 32/EN 55022/32 Class B compliance					

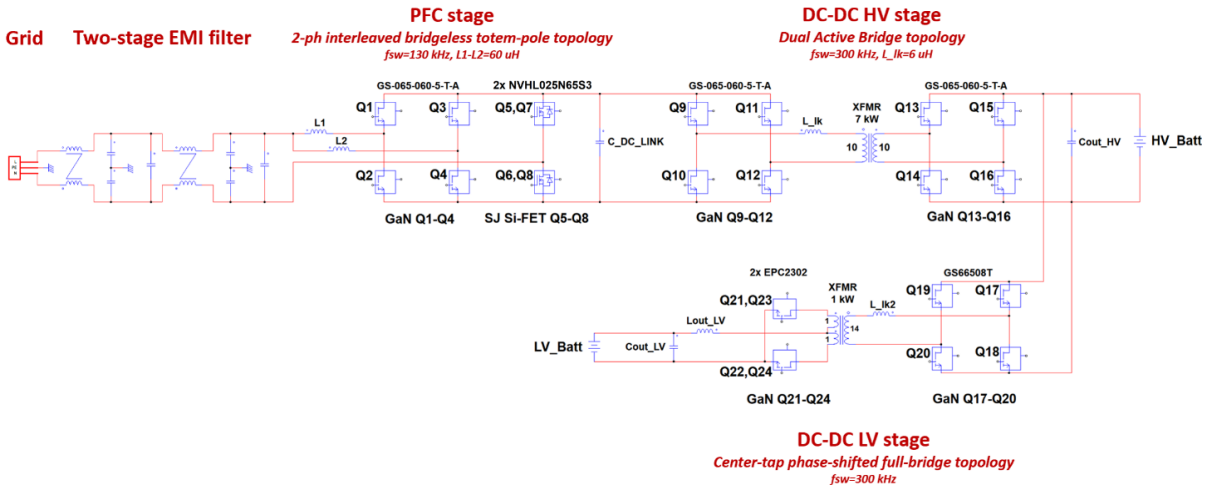


Figure 2.1 OBC designed system topology.

In the following, the development of the OBC prototype is detailed addressing the PFC (Section 2.1), DAB (Section 2.2) and PSFB (Section 2.3) design choices that has been validated exploiting the PSIM simulator. Furthermore, in Section 2.4, the simplified control architecture is briefly explained and finally, in Section 2.5, the OBC implementation and preliminary validation measurements are presented.

2.1. PFC converter design

The PFC converter is realized in a 2-ph interleaved bridgeless totem-pole topology, which offers notable advantages over the conventional boost or the 2-ph bridgeless circuits [14]. First of all, the elimination of diode bridge losses allows to improve the efficiency from 97-98 % to 99 % or higher, ensuring bidirectional capability as well. Furthermore, it benefits from lower part counts enabling higher power density and lower BOM cost. Not least, when GaN devices are used in the half bridge configuration, the inherently absence of a parasitic body-diode guarantees zero reverse recovery loss at turn-on (Q_{rr} = 0) making it possible to operate in CCM (Continuous Conduction Mode) even at high power levels with lower harmonics (higher PF quality) and lower rms current (higher efficiency) as opposed to DCM/CrCM (Discontinuous Conduction Mode/Critical Conduction Mode) which are implemented to avoid body-diode conduction when Si mosfets are used instead [14,15].

The automotive grade top-side cooled 650 V-25 mΩ GS-065-060-5-T-A GaN HEMT device from GaN Systems (now part of Infineon Technologies) has been selected to be used in the two HF (high-frequency) half-bridges of the PFC, as well as in the DC-DC HV converter. Its main datasheet parameters are listed in Table 2.2.

Table 2.2 Datasheet parameters of GaN HEMT GS-065-060-5-T-A.

V_{DS}	I_{DS} @Tc = 25 °C; @Tc = 100 °C		$R_{DS,on}$ @Tj = 25 °C; @Tj = 150 °C	
650 V	60 A; 41 A		25 mΩ; 65 mΩ	
C_{iss} (@400 V)	**C_{oss} (@400 V)**	**C_{gd} (@400 V)**	**Q_{gd} (@400 V)**	**Q_g (@400 V)**
516 pF	127 pF	2.4 pF	4.1 nC	14 nC
E_{on}, E_{off}, E_{oss} (@ 400 V, 20 A, R_G = 10/2 Ω, V_{GS} = 6/-3 V, Tj=25 °C)				
117 μJ		17.2 μJ		17 μJ
Package inductances L_g, L_d, L_s (from Pspice level 3 model)				
4 nH		0.2 nH		0.3 nH

Super-junction (SJ) Si mosfets (650 V, 19.9 mΩ) are used in the LF leg ensuring bidirectional capability and synchronous rectification with higher efficiency with respect to IGBTs or FRDs (fast recovery diodes). Operating at line frequency, they exhibit negligible switching losses. The usage of two Si mosfets in parallel per switch

enables similar conduction losses compared to the GaN HEMTs in the two-phase interleaved HF legs.

Regarding the boost power inductors, the combination of 2-phase interleaving, CCM operation and high switching frequency (f_{sw} = 130 kHz) enables the best compromise between distortion and power density using significantly reduced inductance value (L1, L2 = 60 μH) with respect to traditional Silicon-based PFC circuits that typically use PFC inductors in the range of 300-500 μH. The inductance value of each PFC channel can be determined as [6]:

$$L = \frac{V_{out} \,/\, 2}{k_{ripple} \cdot \sqrt{2} \cdot I_{L,rms} \cdot 2 \cdot f_{sw}} \tag{2.1}$$

where $k_{ripple} < 1$ is the ripple coefficient and $I_{L,rms}$ is the rms current of the PFC channel.

PSIM simulator exploits the so-called thermal module model [16] in order to calculate conduction and switching losses on the basis of several look-up table datasets (first and third quadrant characteristics, as well as E_{on} and E_{off} values as functions of V_{GS}, V_{DS}, I_{DS}, R_G and T_j of the device). This approach enables to avoid the large computational effort of Spice-like simulators which calculate the power dissipation basing on the integration of V_{DS} and I_{DS} waveforms. Moreover, the thermal model allows to retrieve junction and case temperature delta due to the power dissipation by means of the junction-case thermal impedance and the thermal resistance of the connection between the TIM (thermal interface material) and the liquid cold plate. Furthermore, PSIM simulations take into account also the accurate models of the passive components (in Table 2.3 for the PFC converter).

Table 2.3 PFC passive components.

Passive component	PN	Quantity	Parameters
PFC inductor	Bourns custom design	2x	L = 60 μH (@ 1 V, 100 kHz) R_{DC} = 22 mΩ Saturation Current: 20 % Roll off
Electrolytic capacitor	Kemet ALA7DA391CF500	3x	V_{DC} = 500 V C = 390 μF ESR = 481.2 mΩ (@ 20 °C, 10 kHz) ESL = 20 nH I_{crms} = 4.12 Arms (@ 85 °C, 10 kHz)
Ceramic capacitor	TDK B58031U5105M062	2x for each GaN leg	V_{DC} = 500 V C = 1 μF ESR = 12 mΩ (@ 0 V_{DC}, 0.5 Vrms, 25 °C, 1 MHz) ESL = 3 nH I_{crms} = 11 Arms (@ 85 °C, 100 kHz)

Custom-designed PFC inductors exploit a gapped ferrite core, ensuring 5 A of margin between peak current and the saturation point. Moreover, windings in Litz wire guarantee an AC resistance which is close to the DC resistance value. A really compact size has been achieved: each PFC inductor is encapsulated in a 46.1 (L) x 38.6 (W) x 46 (H) [mm] potting box.

PFC simulation results are reported hereafter. The following operating conditions are assumed: V_{in} = 240 Vrms, f_{line} = 50 Hz, L1 = L2 = 60 μH, V_{out} = 400 V, P_{out} = 6.6 kW, f_{sw} = 130 kHz, dead-time = 100 ns, T_{amb} = 60 °C (that is the maximum temperature of the cooling plate). GaN devices are driven with V_{GS} = 6/-3 V and R_G = 10/2 Ω, whereas Si mosfets are driven with V_{GS} = 10/0 V and R_G = 2 Ω.

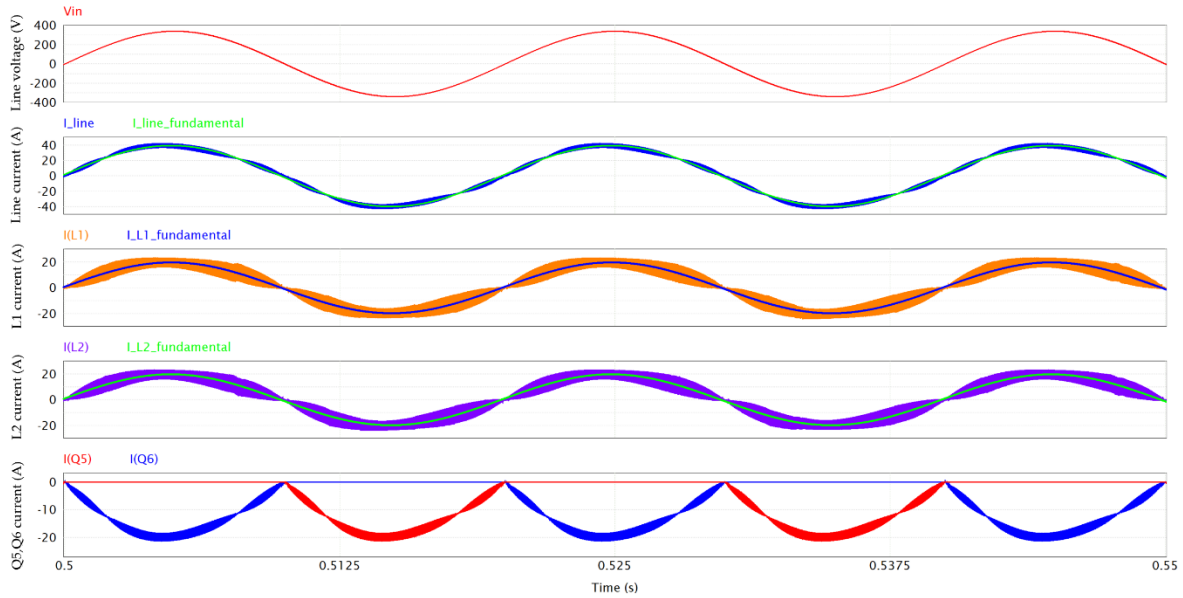


Figure 2.2 PFC waveforms, from top to bottom: line voltage, line current and its fundamental component (50 Hz), inductor L1 current and its fundamental component (50 Hz), inductor L2 current and its fundamental component (50 Hz), Q5 and Q6 (LF leg) currents.

Figure 2.3 provides a magnification of inductors ripple and line current ripple, that is enhanced by the interleaved operation. Despite the very low value of inductance (60 µH), the combination of high switching frequency and interleaving results in a computed THD of 6 %. From simulation results, the PF (Power Factor) turns out to be 0.996.

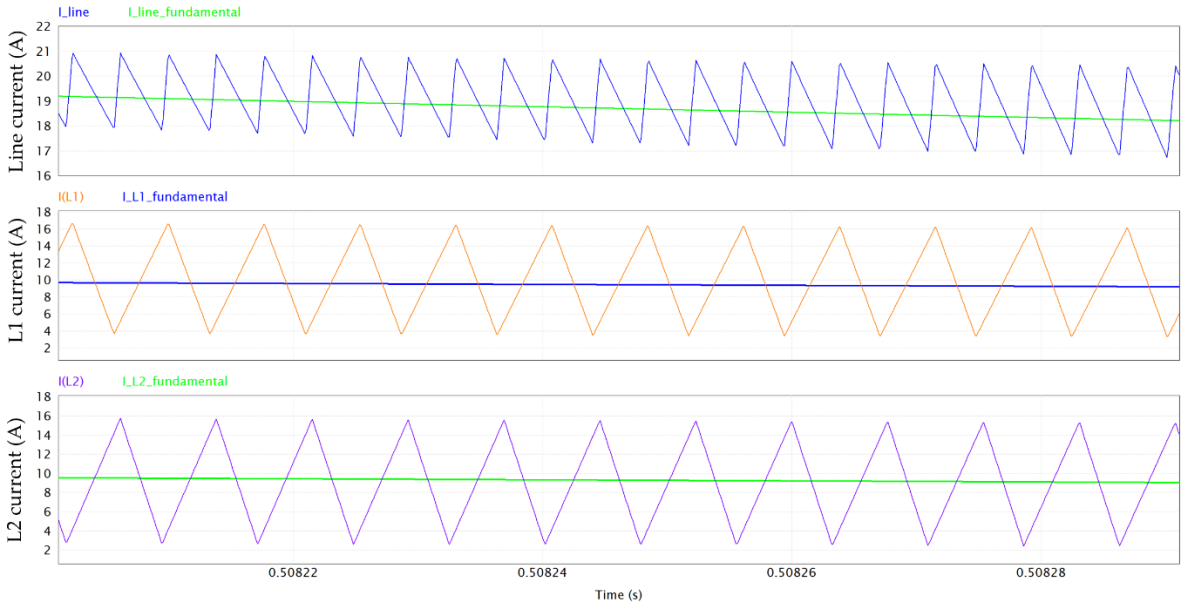


Figure 2.3 Magnification of the ripple of line current (at 260 kHz) and of L1/L2 current (at 130 kHz).

Figure 2.4 shows the HF currents conducted by the first GaN half-bridge Q1-Q2.

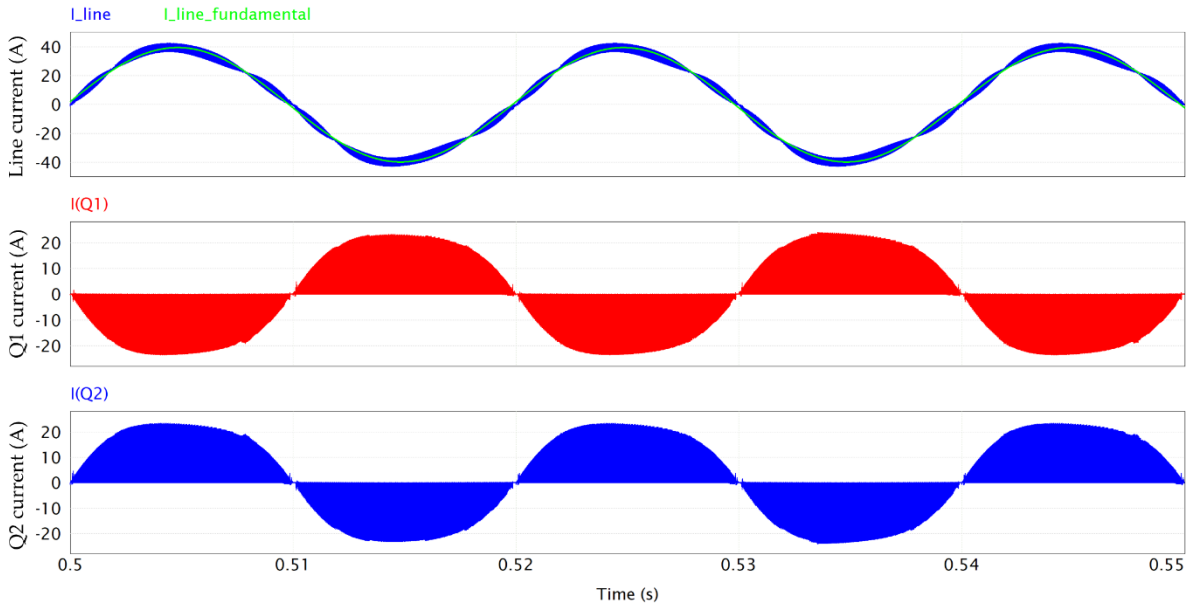


Figure 2.4 Q1-Q2 HF current conduction.

As observed before, the exploitation of PSIM thermal models enables the accurate computation of transistor losses and their different contributions. Power losses contributions for Q1 are displayed in Figure 2.5 along with case and junction temperatures. The waveforms of Figure 2.5 are at a stable thermal regime. Nonetheless, the variation of the junction temperature and the power dissipation within the slow 50 Hz period can be appreciated. It can be observed that in this nominal full power condition (P_{out} = 6.6 kW) at the maximum cooling plate temperature (T_{amb} = 60 °C), the GaN HEMT channel temperature (T_j) is still safely far from its maximum rating of 150 °C. By computing the average values of dissipated power, the pie chart in Figure 2.6 can be obtained, showing the power losses distribution. Third quadrant losses occur during dead time, when the GaN HEMT has a diode-equivalent behavior with a forward voltage equals to $-V_{GS(th)} - |V_{GS,off}| - R_{ds,rev} \cdot I_{SD} \approx -5$ V [17]. It is possible to consider also these losses as conduction losses. It is worthy of note that there is an almost even distribution between conduction and switching losses, meaning that the selected switching frequency represents a very good compromise between the switching losses and the shrinking of inductor size.

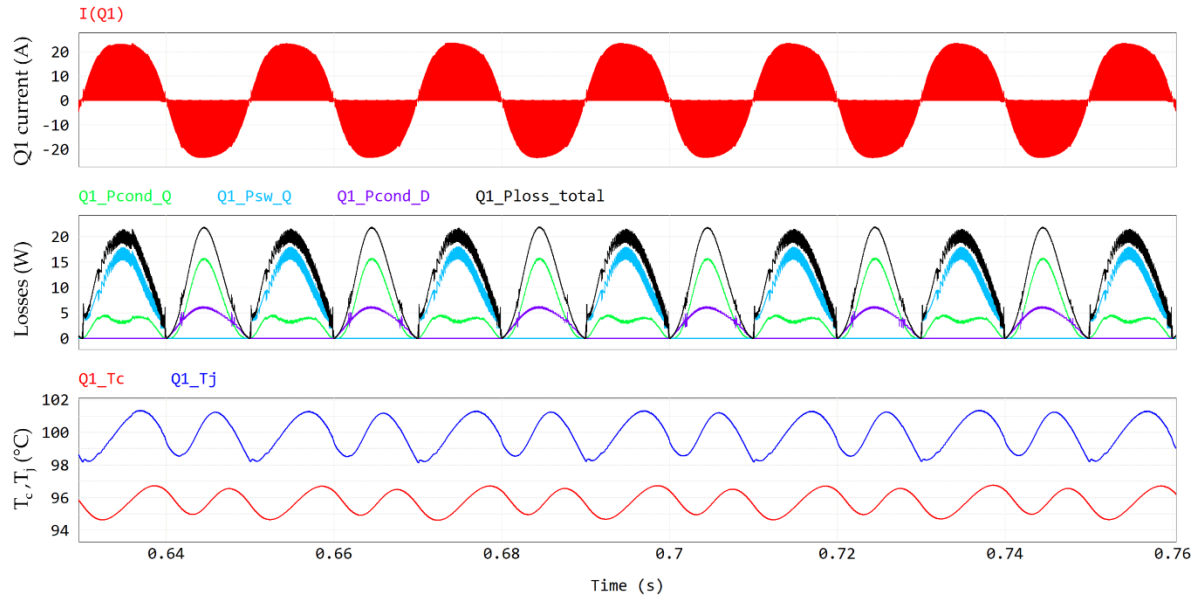


Figure 2.5 Q1 losses, from top to bottom: Q1 current, conduction losses (in green), switching losses (in cyan), third-quadrant losses (in violet), total losses (in black), case (Tc) and junction (Tj) temperatures.

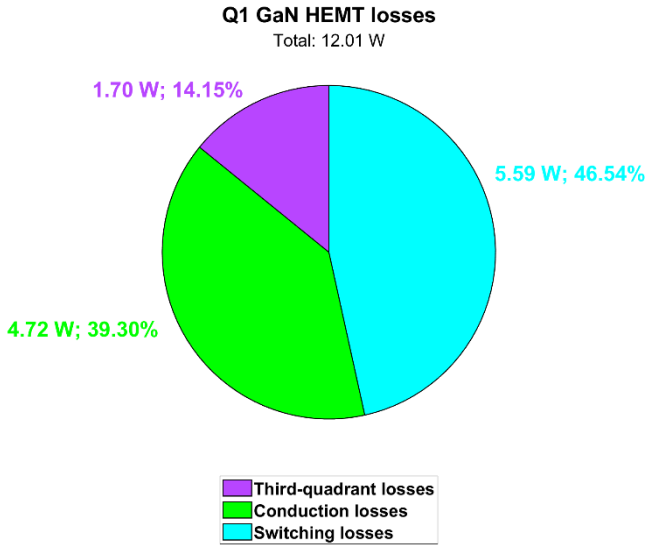


Figure 2.6 Contributions of Q1 power losses (@T_{amb} = 60 °C).

Similarly to CCM boost PFC, the capacitance value of the DC-link capacitor is determined by voltage ripple and hold-up time requirements [18]:

$$C_{DC-link} \geq \frac{P_{out}}{V_{out} \cdot 2 \cdot \pi \cdot f_{line} \cdot \Delta V_{pk-pk}} \tag{2.2}$$

$$C_{DC-link} \geq \frac{2 \cdot P_{out} \cdot t_{hold-up}}{V_{out}^2 - V_{out,min}^2} \tag{2.3}$$

Based on equations (2.2) and (2.3), at least 1.2 mF are necessary to guarantee a voltage ripple of 44 $V_{pk\text{-}pk}$ when P_{out} = 6.6 kW and V_{out} = 400 V, as well as an hold-up time of 10 ms with a minimum acceptable output voltage $V_{out,min} \approx$ 220 V.

The total current through the output capacitance $C_{DC\text{-}LINK}$ has two main components: a dominant low-frequency (LF) component at twice the line frequency and a high-frequency component at the switching frequency and its harmonics. As observed in [18,19], the low-frequency rms component can be calculated as:

$$I_{LF,rms} = \frac{P_{out}}{V_{out} \cdot \sqrt{2}} = \frac{I_{out}}{\sqrt{2}} = \frac{16.5\ Arms}{\sqrt{2}} = 11.67\ Arms \tag{2.4}$$

while the high-frequency rms component in case of 2-ph interleaving can be approximated as [19]:

$$I_{HF,rms,2-ph} = \sqrt{mt\left(\frac{3}{2}\cdot\frac{P_{in}^2}{V_{out}^2} - \frac{64}{15\pi}\cdot\frac{P_{in}^2\cdot V_{in\_pk}}{V_{out}^3}\right) + ct\left(\frac{16}{3\pi}\cdot\frac{P_{in}^2}{V_{in\_pk}\cdot V_{out}} - \frac{3}{2}\cdot\frac{P_{in}^2}{V_{out}^2}\right)} \tag{2.5}$$

where *mt* and *ct* are the coefficients for linearization of the correction factor $K_{MS}(t)$

$$K_{MS}(t) = mt\ \frac{V_{in\_pk}}{V_{out}}\sin(\omega t) + ct \tag{2.6}$$

with *mt* = -1.2 and *ct* = 0.6 when the on time duty cycle $d_{on}(t) = 1-(V_{in\_pk}/V_{out})\cdot\sin(\omega t)$ is greater than 0.5, whereas *mt* = 1.2 and *ct* = -0.6 when $d_{on}(t) < 0.5$. In our case, under the mentioned operating conditions, from (2.5) the DC-link HF component turns out to be equal to

$$I_{HF,rms,2-ph} = 5.70\ Arms \tag{2.7}$$

The total rms current through the DC-link capacitors can be then calculated as

$$I_{C,DC-link} = \sqrt{I_{LF,rms}^2 + I_{HF,rms,2-ph}^2} = \sqrt{11.67^2 Arms^2 + 5.70^2 Arms^2} = 12.99\ Arms \tag{2.8}$$

which is consistent with the simulation result reported in Table 2.4.

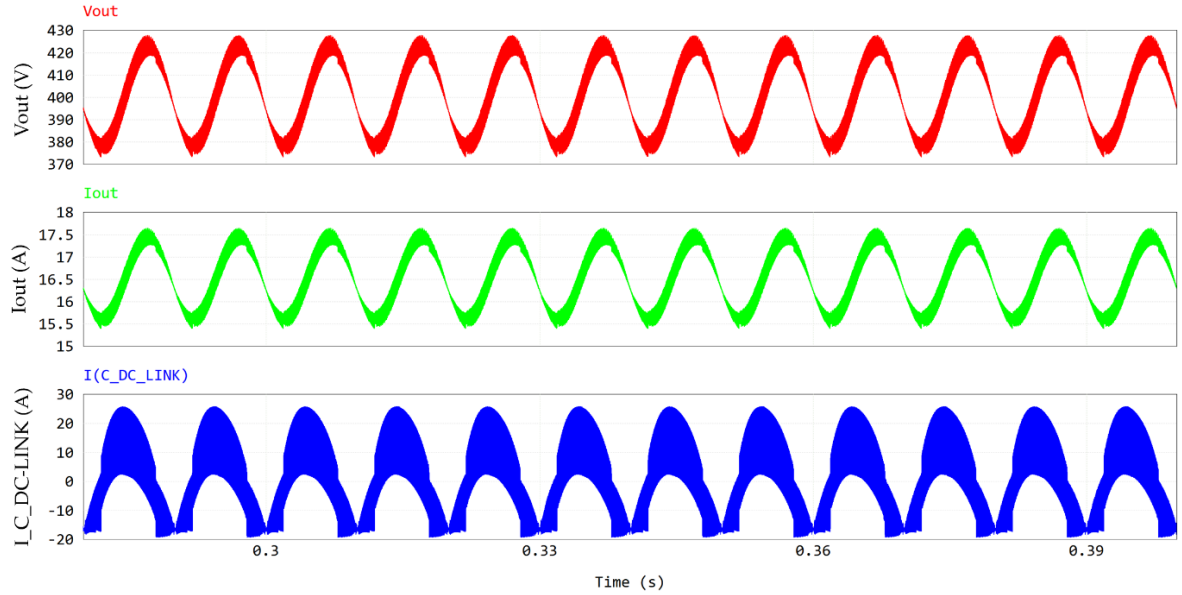


Figure 2.7 PFC waveforms at the output section: V_{out}, I_{out}, $I_{C\_DC\text{-}LINK}$.

Table 2.4 RMS and mean values of the PFC waveforms at the output section.

Quantity	RMS value	Mean value
V_{out}	400.37 Vrms	400.06 V
I_{out}	16.52 Arms	16.50 A
$I_{C,DC\text{-}link}$	13.32 Arms	≈ 0 A

Figures 2.8 and 2.9 show the frequency spectrum of V_{out}, I_{out} and $I_{C\_DC\text{-}LINK}$ allowing to evaluate their harmonic content (see Table 2.5).

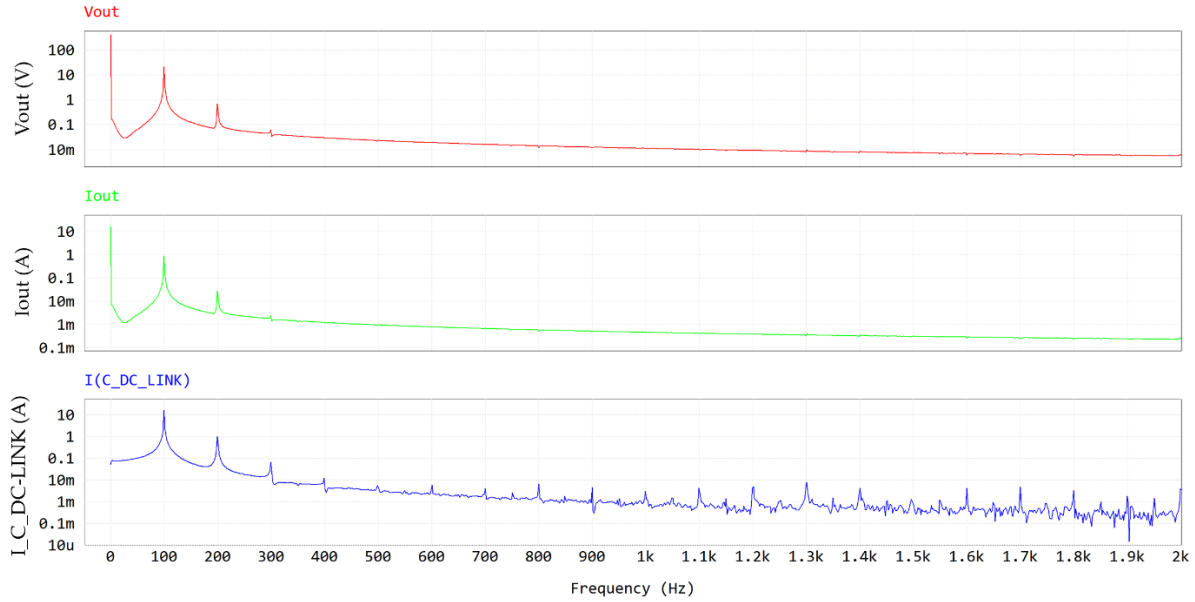


Figure 2.8 FFT (0-2 kHz) of the PFC waveforms at the output section. Y-axis is in log scale.

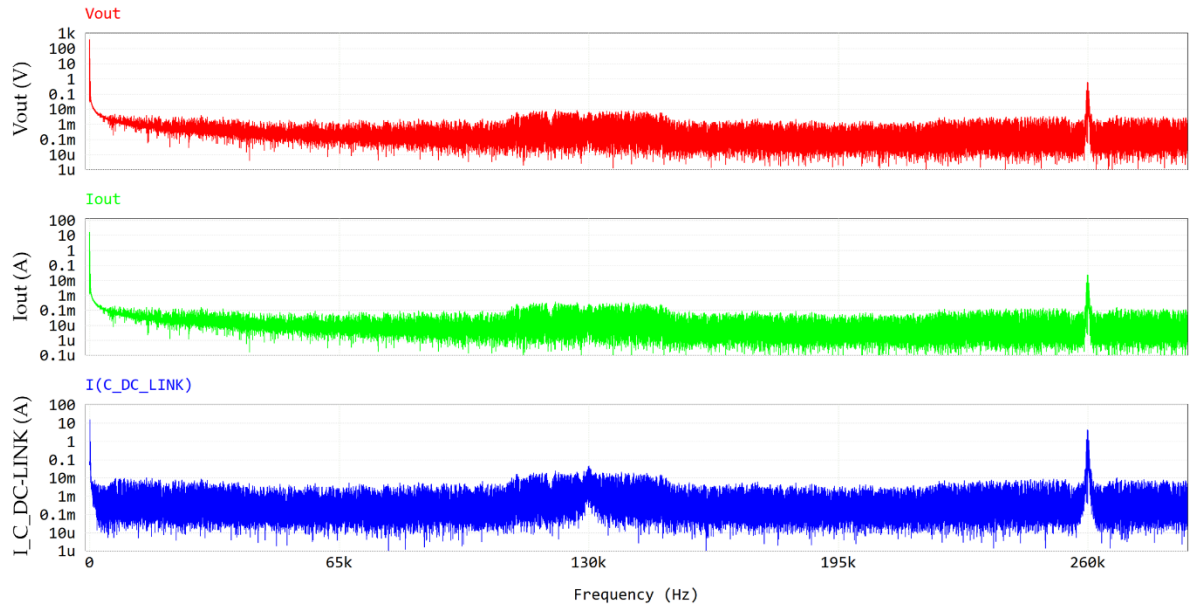


Figure 2.9 FFT (0-280 kHz) of the PFC waveforms at the output section. Y-axis is in log scale.

Table 2.5 Main frequency components of the PFC waveforms at the output section.

Quantity	Amplitude (0 Hz)	Amplitude (100 Hz)	Amplitude (260 kHz)
V_{out}	400 Vpk	22.04 Vpk	0.55 Vpk
I_{out}	16.50 Apk	0.91 Apk	0.023 Apk
$I_{C,DC\text{-}link}$	≈ 0 Apk	16 Apk	4.41 Apk

DC-link capacitor bank has been realized with three electrolytic capacitors in parallel (Kemet ALA7DA391CF500, 500 V, 390 µF). Figure 2.7 shows an output voltage ripple of 45 $V_{pk\text{-}pk}$. Table 2.5 reports an amplitude of LF component of the DC-link current (16 Apk = 11.31 Arms) which is close to the DC-component of the output current (16.5 Apk ≈ 16.5 Arms), justifying equation (2.4). The HF component at twice the switching frequency is displayed in Figure 2.9.

The ESR of electrolytic capacitors decreases with temperature, for ALA7DA391CF500 can be estimated in 250 mΩ at 70 °C. Then, losses of DC-link capacitor bank can be calculated as

$$P_{DC-link\ cap\ bank} = \frac{ESR}{3} \cdot I_{C,DC-LINK}^2 = \frac{250\ m\Omega}{3} \cdot 13.32^2 Arms^2 = 14.79\ W \qquad (2.9)$$

where $I_{C,DC\text{-}LINK}$ is the total ripple current of DC-link capacitors from Table 2.4.
DC-resistance of power inductors is equal to 22 mΩ. The inductor copper losses related to the DCR can be computed as

$$P_{L.DCR} = DCR \cdot I_{L,rms}^2 = 22\ m\Omega \cdot 14.27^2 Arms^2 = 4.48\ W \qquad (2.10)$$

Simulation performed through ANSYS software results in total winding losses of 6 W, taking also into account the contribution of eddy currents (i.e., the AC-resistance). Table 2.6 and Figure 2.10 summarize the PFC simulation results. Average temperatures and power losses at regime are considered. The total dissipated power is quantified in 86.79 W and PFC efficiency turns out to be 98.70 %. This performance is in the worst-case condition of 60 °C coolant temperature.

Table 2.6 PFC simulation results at T_{amb} = 60 °C, V_{in} = 240 Vrms, V_{out} = 400 V, P_{out} = 6.6 kW.

Quantity	Value
Line current	28 Arms
Boost inductor current	14.27 Arms 23.17 A – peak value 12.94 A_{pk-pk} – ΔI_{max}
GaN HEMT current	10.07 Arms
Si mosfet current	9.90 Arms
DC-link capacitor bank current	13.32 Arms
GaN HEMTs temperature	T_c = 96 °C, T_j = 100 °C
Si mosfets temperature	T_c = 68 °C, T_j = 69 °C
Inductor copper losses	(2x) 6 W
GaN HEMTs losses	(4x) 12 W
Si mosfets losses	(4x) 3 W
DC-link capacitor bank losses	14.79 W
Total losses	86.79 W
V_{out}	400 V
V_{out} voltage ripple	45 V_{pk-pk}
I_{out}	16.5 Arms
P_{out}	6600 W
P_{in}	6686.79 W
Efficiency	98.70 %
THD	6 %
PF	0.996

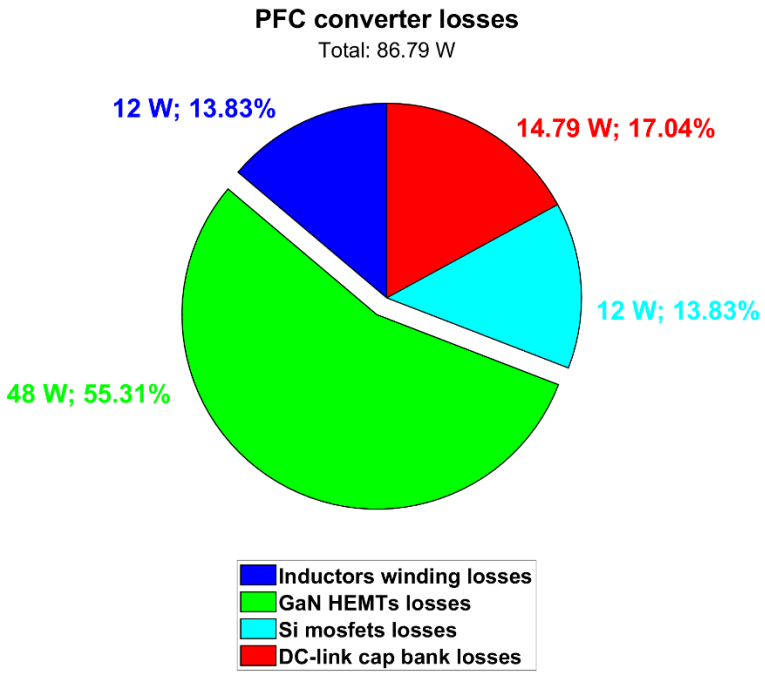


Figure 2.10 PFC converter power loss contributions (@T_{amb} = 60 °C).

These computed performances can be achieved by the actual implementation of the converter provided that optimal layout of the PCB is designed. Indeed, the fast switching behaviour of GaN devices imposes very high slew rates of voltage and current at commutations (up to hundreds of volts per nanosecond and ten amps per nanosecond). Therefore, it is fundamental to precisely assess, minimize and compensate any inductive or capacitive parasitics of the circuit. One of the major concern is related to driver and power loops, i.e. gate-source and drain-source loops of the device. GS-065-060-5-T-A embedded package ensures ultra-low stray inductances with respect to the traditional wire-bonded QFNL (Quad Flat No-Lead) or TO (Transistor Outline) packages, at the expense of higher cost. Furthermore, an optimal PCB layout – with a wise driver loop and power/ground planes arrangement along with an accurate selection of passive components and mechanical connectors – plays an essential role. To this aim, a very compact layout of the GaN switching leg has been designed by implementing a very compact driving loop, also exploiting magnetic flux cancellation in the power loop, with top-side cooled GaN HEMTs on the bottom layer (to be directly connected to the cold plate) while drivers and low-parasitic, high-current decoupling capacitors are placed on the top layer (see Figure 2.11). Top-side cooled GS-065-060-5-T-A GaN HEMT does not provide a separate Source Sense pin (as opposed to the bottom-side cooled counterpart GS-065-060-5-B-A). However, for the same purpose, a Kelvin connection at the side of Source pad has been routed, separating the drive return and the power ground, minimizing the common source inductance and thus the noise coupling between the two loops [17]. Also, Allegro AHV85110 isolated single-channel drivers that feature in-package micro transformer and 2A/4A of source/sink current are used to provide an optimal GaN HEMTs driving

in a very compact form factor. The optimization of the layout of the GaN switching leg was also supported by EM simulations as detailed later in Chapter 3.

The low-frequency switching leg (with super-junction Silicon mosfets) is not critical and is implemented with a traditional PCB layout exploiting through hole connection of TO-247 package devices, driven by Texas Instruments UCC21530BQDWKRQ1 4A/6A isolated dual-channel driver.

Some pictures of the OBC will be shown later in Section 2.5.

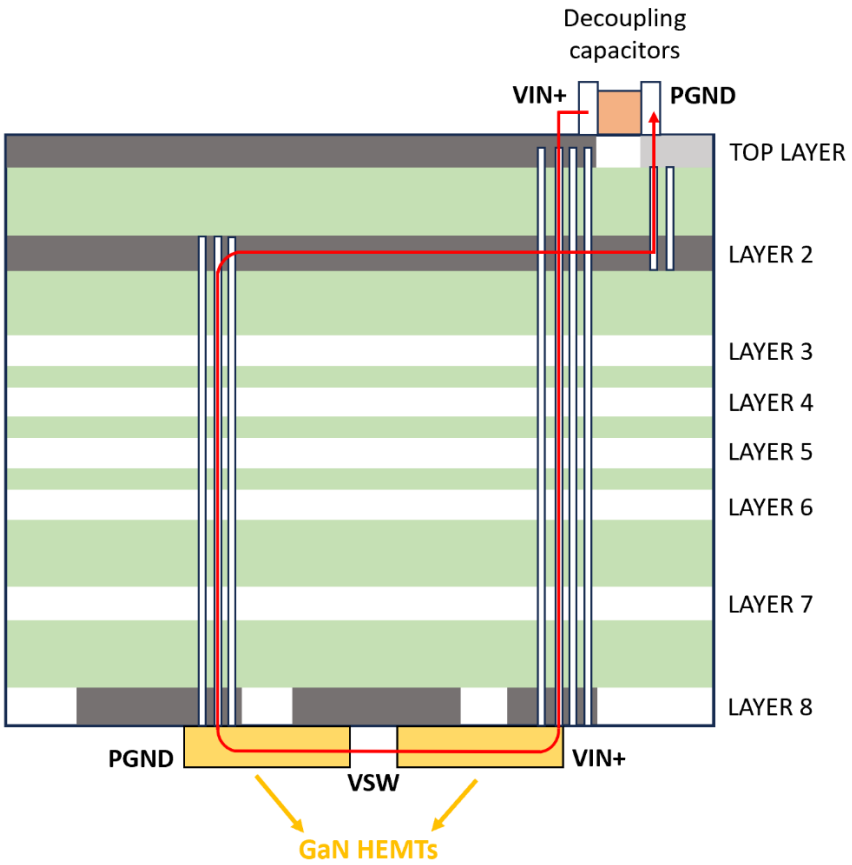


Figure 2.11 Flux-cancelling traces with top-side cooled devices in a 8-layers PCB: layer 2 is used as ground return. The thickness of the entire layer stack-up is 2060 µm in our case (further details are presented in Chapter 3).

2.2. DAB converter design

In two-stage OBC designs, the PFC converter is followed by a DC-DC HV stage to regulate the battery charging process. The exploitation of bidirectional devices and suitable control algorithms enables V2G and V2L operation modes as well.

High-voltage DC-DC converter specifications (in Table 2.1) include a wide output voltage range (200-450 V). Galvanic isolation is also required. The most promising topologies to realize this stage are the resonant CLLC and the Dual Active Bridge. This latter has been preferred due to the simplicity of design and control scheme: in a SPS (single phase-shift) modulation the power flow is controlled by regulating the voltage applied to the primary series inductor by simply adjusting the time displacement (phase shift) among the gate signals of the two full bridges, avoiding the non-linear relationship between the gain and the load condition that exists in a CLLC circuit, where the operating switching frequency at small Q (quality factor) can reach very high values [20,21].

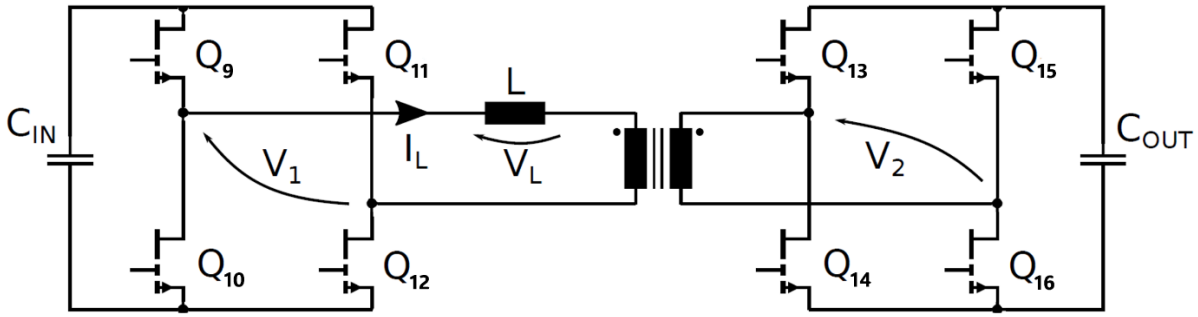


Figure 2.12 DAB DC-DC converter schematic.

With reference to the schematic in Figure 2.12, the relationship between the output power and the phase shift ϕ is equal to [22]:

$$P = \frac{nV_1V_2}{2\pi^2 f_{sw}L}\,\phi\,(\pi - |\phi|) \tag{2.11}$$

where $n = N_2 / N_1$ is the transformer turns ratio and $-\pi/2 < \phi < \pi/2$. The absolute maximum power is obtained for $\phi = \pi / 2$:

$$|P_{max}| = \frac{nV_1V_2}{8f_{sw}L} \tag{2.12}$$

The designed DAB converter is composed of two full bridges of GS-065-060-5-T-A GaN HEMTs driven by Allegro single-channel isolated driver AHV85110, which features Power-Thru Integrated Isolated Bias Supply. The PCB layout of each switching leg is the same as described for the PFC section, that guarantees optimal performances by minimizing parasitics.

The selected switching frequency is 300 kHz which allows the development of a very compact custom transformer. DAB ZVS boundaries depends on the total energy stored in the series inductor and can be calculated as reported in [20,22]. A series inductance of 6 μH has been selected to ensure a wide ZVS region and provide an output power of 6.6 kW when $V_{in} = V_{out} = 400$ V, $f_{sw} = 300$ kHz, $n = 1$ and phase shift = 33°.

The series inductance is represented by the leakage inductance (6 μH) of the custom-designed DAB transformer (n=1) without the need of an external shim inductor. This is crucial to minimize the dimensions of the converter: DAB transformer has been encapsulated in a 65.19 (L) x 47.51 (W) x 46.90 (H) [mm] potting box. Regarding the mixed-type capacitor bank formed by electrolytic low-frequency capacitor C_{LF} and ceramic high-frequency capacitor C_{HF}, it is paramount important in WBG applications to minimize the involved parasitic inductance, especially ESL of LF capacitor and inductance of connection structure, otherwise antiresonance issues at high frequencies may arise. A maximum overall inductance of two digits of nH should be met.

DAB passive components are listed in Table 2.7.

Table 2.7 DAB passive components.

Passive component	PN	Quantity	Parameters
DAB XFMR	Bourns custom design	1	L_{lk} = 6 μH L_{mag} = 301.6 μH $C_{p,s}$ = 27.2 pF C_{ww} = 43.3 pF $R_{DCp,s}$ = 9.4 mΩ Turns ratio = 10:10
Electrolytic capacitor	Kemet ALA7DA391CF500	3x in the DC-link section; 1x in the output section	V_{DC} = 500 V C = 390 μF ESR = 481.2 mΩ (@ 20 °C, 10 kHz) ESL = 20 nH Icrms = 4.12 Arms (@ 85 °C, 10 kHz)
Ceramic capacitor	TDK B58031U5105M062	2x for each GaN leg	V_{DC} = 500 V C = 1 μF ESR = 12 mΩ (@ 0 V_{DC}, 0.5 Vrms, 25 °C, 1 MHz) ESL = 3 nH I_{crms} = 11 Arms (@ 85 °C, 100 kHz)

DAB waveforms (400V/400V, 6.6 kW, 300 kHz, V_{GS} = 6/-3 V, R_G = 10/2 Ω, dead time = 100 ns, T_{amb} = 60 °C) simulated through PSIM are reported in Figures 2.13 and 2.14. The names of the electrical quantities correspond to the labels in Figure 2.12. In a SPS modulation, switches on the same diagonal (Q9-Q12, Q10-Q11, Q13-Q16, Q14-Q15) are ON/OFF for half a period and share the same gate signal with 50 % duty cycle. Figures 2.13 and 2.14 show that when Q10-Q11 are turned off, the negative inductive current I_L charges the C_{oss} of Q10-Q11 to 400V+V_f and discharges the C_{oss} of Q9-Q12 to -V_f, where $V_f \approx 5$ V is the diode-equivalent forward voltage of GaN in reverse conduction. Then V1 commutes to 400V+2V_f, VL to 800V+2V_f and series inductor is being charged. Similarly, when Q14-Q15 are turned off, V2 commutes to 400V+2V_f, VL to -2V_f (since in the meantime Q9-Q12 have stopped reverse conduction) and series inductor is slowly discharged. In the second half of the period, Q9-Q12 are turned off (V1 toggles to -400V-2V_f and VL to -800V-2V_f) followed by Q13-Q16 (V2 toggles to -400V-2V_f and VL to +2V_f).

It is noteworthy that GaN HEMTs experience a ZVS turn-on: for instance, during the dead-time that follows Q10-11 turn-off, the negative inductive current I_L discharges the C_{oss} of Q9-12 to -V_f. Hence, Q9-Q12 are in reverse conduction in third quadrant, acting as equivalent free-wheeling diodes (the gate is OFF). Then, when the PWM signal of Q9-Q12 goes ON, they are forward-biased with an almost null drain-source voltage, which further decreases, in absolute term, from -V_f to -$V_{DS,ON}$, leading to negligible turn-on losses. The negative sign of V_{DS} is due to the fact that Q9-Q12 have opposite polarity when I_L is negative (see Figure 2.12).

Looking at Figures 2.13 and 2.14, all the DAB switches experience a ZVS turn-on at V_{out} = 400 V and P_{out} = 6.6 kW. Since they are piloted per diagonal lines, Figure 2.14 is representative for all eight switches.

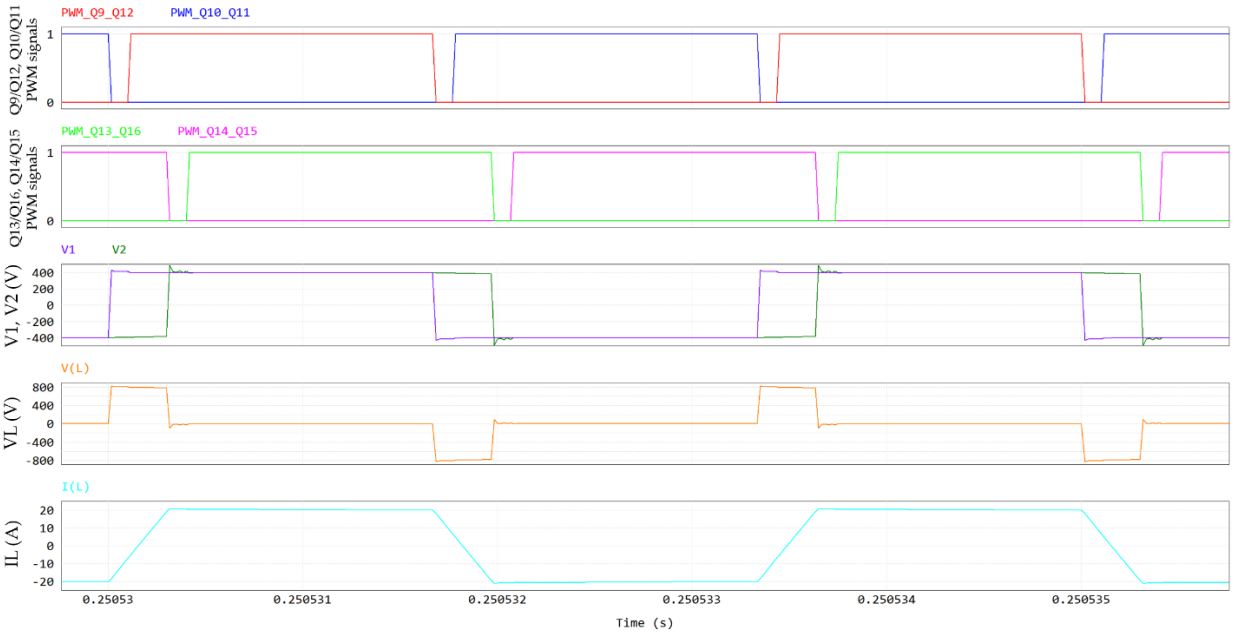


Figure 2.13 DAB waveforms, from top to bottom: PWM signals of Q9-Q12 and Q10-Q11, PWM signals of Q13-Q16 and Q14-Q15, primary (V1) and secondary (V2) voltages, series inductor voltage V_L, series inductor current I_L.

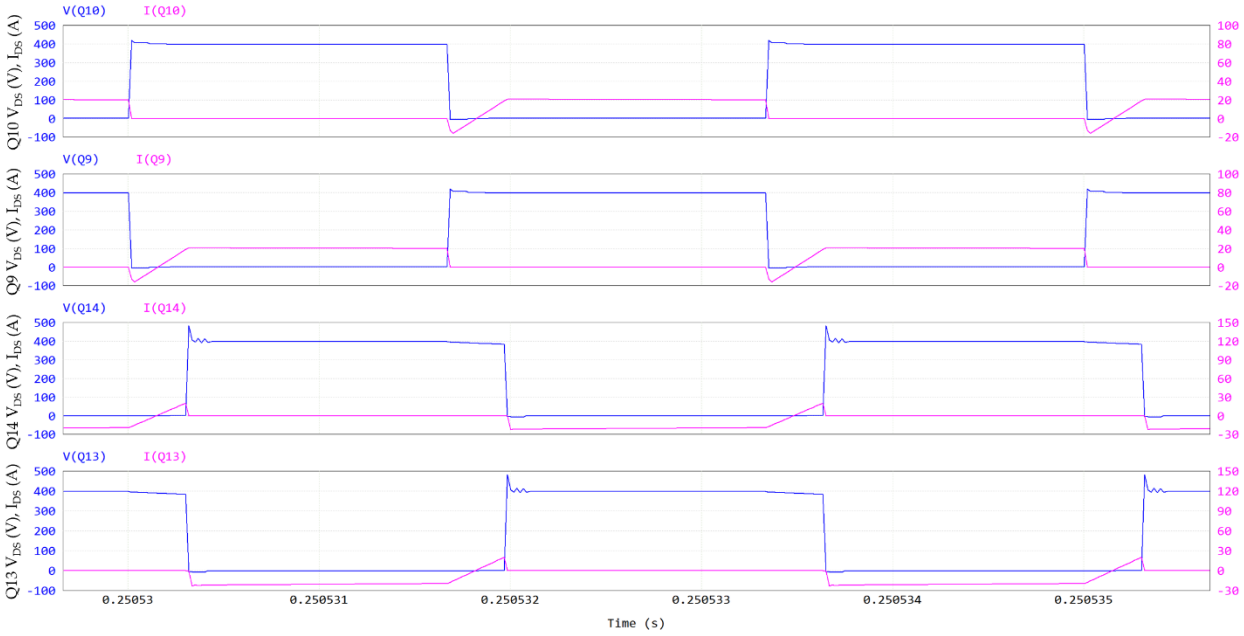


Figure 2.14 DAB ZVS turn-on: V_{DS} and I_{DS} of Q10, V_{DS} and I_{DS} of Q9, V_{DS} and I_{DS} of Q14, V_{DS} and I_{DS} of Q13. Y-axis of drain-source voltage is on the left, Y-axis of drain-source current is on the right.

Power losses contributions at steady-state for Q9 are displayed in Figure 2.15 along with case and junction temperatures. It can be noted that at full power condition (P_{out} = 6.6 kW) and at the maximum cooling plate temperature T_{amb} = 60 °C, the GaN HEMT channel temperature (T_j) reaches 116 °C, which is still safely far from its maximum rating of 150 °C. The pie chart in Figure 2.16 shows the weights of the different contributions to DAB power losses.

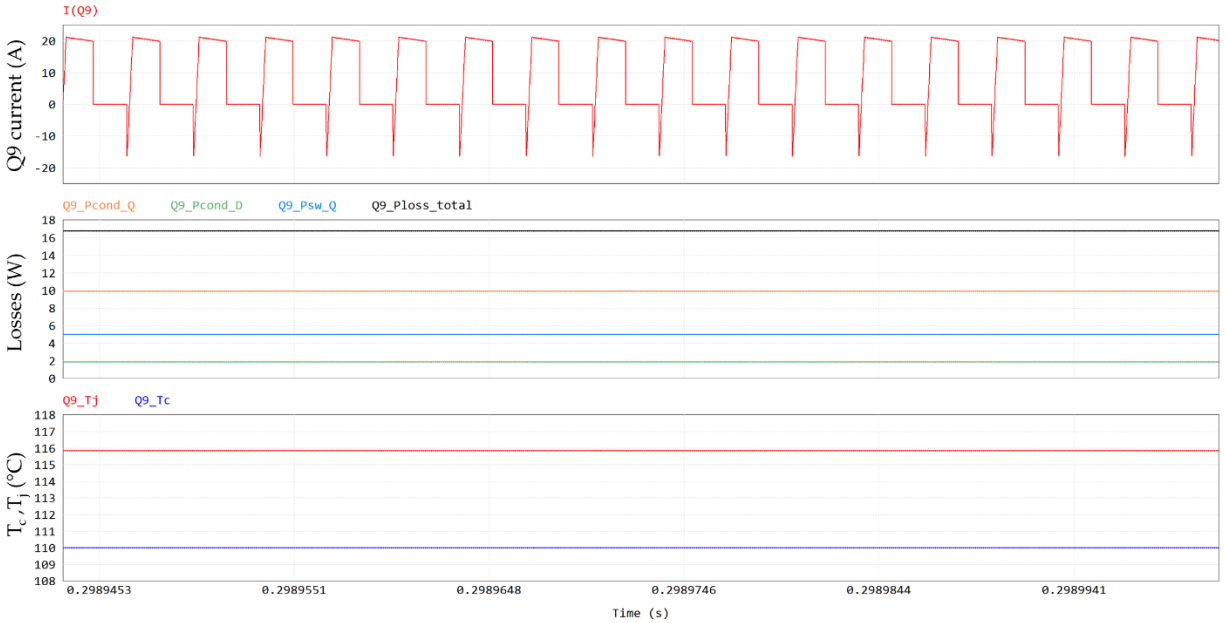


Figure 2.15 Q9 losses, from top to bottom: Q9 current, conduction losses (in orange), third-quadrant losses (in green), switching losses (in light blue), total losses (in black), case and junction temperatures.

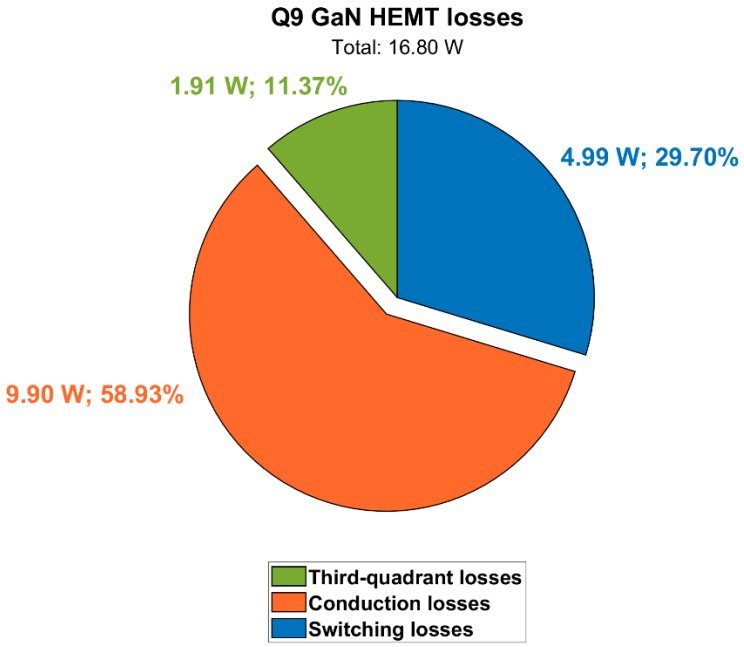


Figure 2.16 Contributions of Q9 power losses (@ V_{out} = 400 V, P_{out} = 6.6 kW, T_{amb} = 60 °C).

In Chapter 3, the details of ZVS turn-on and almost ZVS turn-off commutations of GS-065-060-5-T-A GaN devices in the described DAB converter prototype will be extensively discussed, exploiting the Pspice non-linear dynamic model of the transistor and distinguishing between channel current and parasitic capacitance C_{gs}, C_{gd}, C_{ds} currents, also taking into account the parasitics of the designed PCB. It is noteworthy to anticipate that it will be possible to observe the absence of Miller plateau both at turn-on and turn-off commutation [23], as well as a Miller voltage below the threshold in case of a strong driver at turn-off [2], when GaN devices experience also an almost

ZVS turn-off with nearly negligible turn-off losses [24]. This denotes that PSIM simulator overestimates the switching losses of the device in case of a ZVS behaviour, since the thermal model computes the power dissipations basing on the pre-commutation values of V_{DS} and I_{DS} waveforms. This underlines the need of accurate analyses of the non-linear dynamic behaviour of GaN devices in order to achieve precise assessments of power losses and of corresponding thermal design. In this second Chapter, we take the PSIM thermal model losses as valid, considering them as a worst case scenario for the thermal budget of the cooling system design.

Other main losses are related to the DAB transformer. Primary/secondary DC resistances are equal to 9.4 mΩ, leading to about (3.85 + 3.85) W of copper losses. Core losses (PQ60-42Z Ferrite - DMR95 - with gap of 0.1 mm) can be estimated in 10 W.

Taking into consideration only the OBC DC-DC stage under exam, the rms current of electrolytic capacitors are quantified in 3.54 Arms for the DC-link section and 1.47 Arms for the output section. Then, losses of electrolytic capacitors can be calculated as:

$$P_{DC-link\ cap\ bank} = \frac{ESR}{3} \cdot I_{C,DC-LINK}^2 = \frac{250\ m\Omega}{3} \cdot 3.54^2 Arms^2 = 1.04\ W \tag{2.13}$$

$$P_{output\ cap} = ESR \cdot I_{C,out}^2 = 250\ m\Omega \cdot 1.47^2 Arms^2 = 0.54\ W \tag{2.14}$$

Taking all these loss contributions into account, total dissipated power is quantified in 163.28 W and DAB efficiency turns out to be 97.59 %. Table 2.8 and Figure 2.17 summarize the DAB simulation results at V_{out} = 400 V, P_{out} = 6.6 kW.

Table 2.8 DAB simulation results at T_{amb} = 60 °C, V_{in} = 400 V, V_{out} = 400 V, P_{out} = 6.6 kW, f_{sw} = 300 kHz.

Quantity	Value
XFMR current at primary	19.21 Arms 21.21 A – peak value
XFMR current at secondary	19.43 Arms 21.77 A – peak value
Current of GaN HEMT at primary	13.54 Arms 21.21 A – peak value
Current of GaN HEMT at secondary	13.68 Arms 21.77 A – peak value
DC-link capacitor bank current	3.54 Arms
Output capacitor current	1.47 Arms
Temperature of GaN HEMTs at primary	T_c = 110 °C, T_j = 116 °C
Temperature of GaN HEMTs at secondary	T_c = 117 °C, T_j = 123 °C
DAB XFMR losses	17.7 W
Losses of GaN HEMTs at primary	(4x) 17 W
Losses of GaN HEMTs at secondary	(4x) 19 W
DC-link capacitor bank losses	1.04 W
Output capacitor losses	0.54 W
Total losses	163.28 W
V_{out}	400 V
V_{out} voltage ripple	1.58 V_{pk-pk}
I_{out}	16.5 Arms
P_{out}	6600 W
P_{in}	6763.28 W
Efficiency	97.59 %

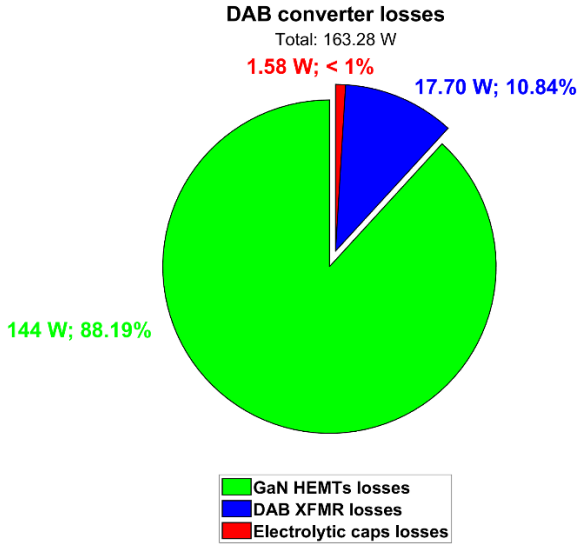


Figure 2.17 Contributions of DAB converter losses (@ V_{out} = 400 V, P_{out} = 6.6 kW, T_{amb} = 60 °C).

In the following, simulation results at V_{out} = 250 V, I_{out} = 16.5 Arms and P_{out} = 4.125 kW are provided as further evidence of design success: a high efficiency value (> 96 %) is achieved under these operating conditions as well (the coolant temperature is always at the worst-case condition of 60 °C), proving high performance also at low battery voltage values with respect to the nominal condition (400 V).

Looking at Figures 2.18 and 2.19, Q9 and Q10 experience a ZVS turn-on also at V_{out} = 250 V and P_{out} = 4.125 kW. Power losses contributions for Q9 are displayed in Figure 2.20 along with case and junction temperatures. A pie chart of Q9 power losses is shown in Figure 2.21, while Table 2.9 and Figure 2.22 summarize the DAB simulation results at V_{out} = 250 V, P_{out} = 4.125 kW.

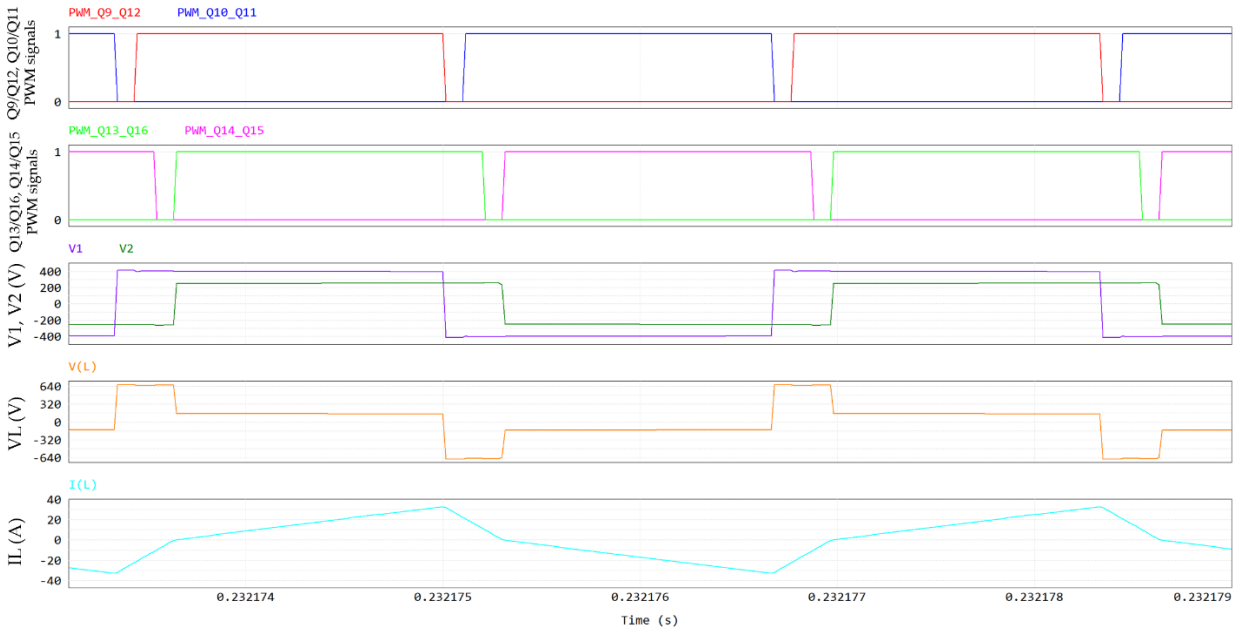


Figure 2.18 DAB waveforms at V_{out} = 250 V and P_{out} = 4.125 kW, from top to bottom: PWM signals of Q9-Q12 and Q10-Q11, PWM signals of Q13-Q16 and Q14-Q15, primary (V1) and secondary (V2) voltages, series inductor voltage V_L, series inductor current I_L.

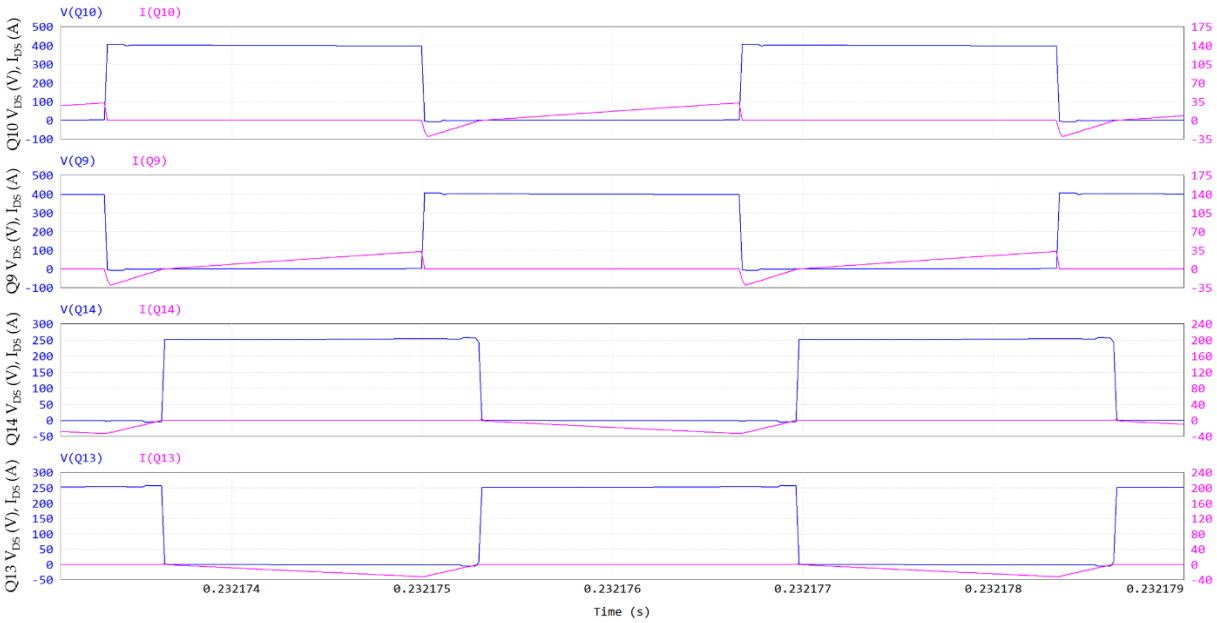


Figure 2.19 DAB Q9 and Q10 ZVS turn-on (@ V_{out} = 250 V and P_{out} = 4.125 kW): V_{DS} and I_{DS} of Q10, V_{DS} and I_{DS} of Q9, V_{DS} and I_{DS} of Q14, V_{DS} and I_{DS} of Q13. Y-axis of drain-source voltage is on the left, Y-axis of drain-source current is on the right.

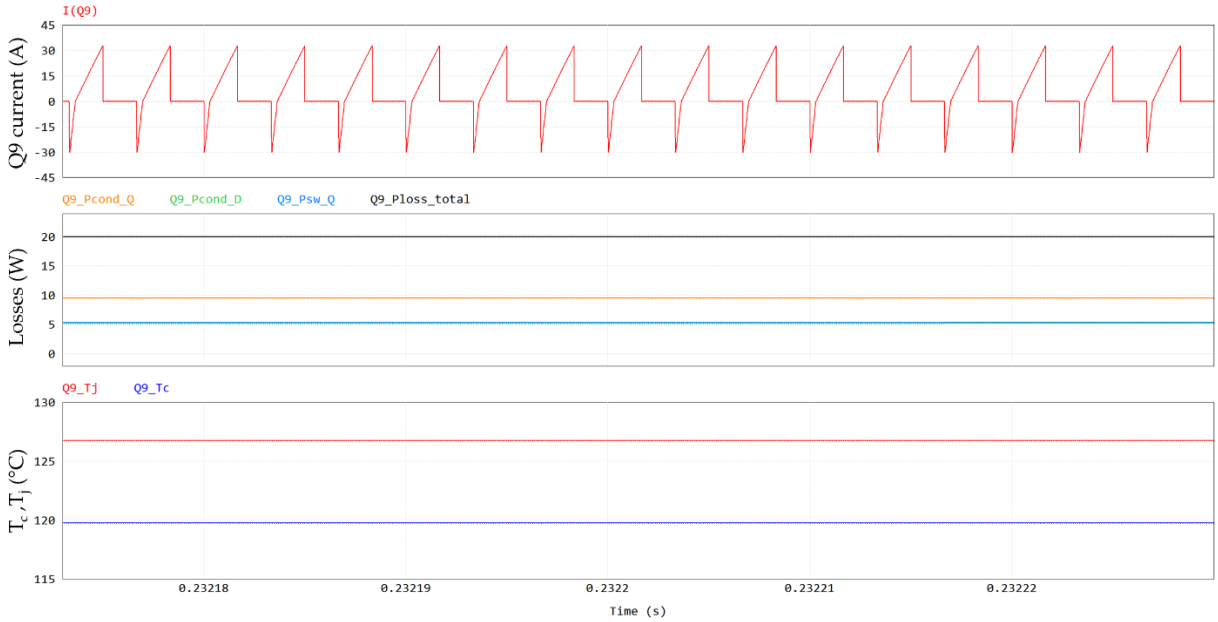


Figure 2.20 Q9 losses at V_{out} = 250 V and P_{out} = 4.125 kW: Q9 current, conduction losses (in orange), third-quadrant losses (in green), switching losses (in light blue), total losses (in black), case and junction temperatures.

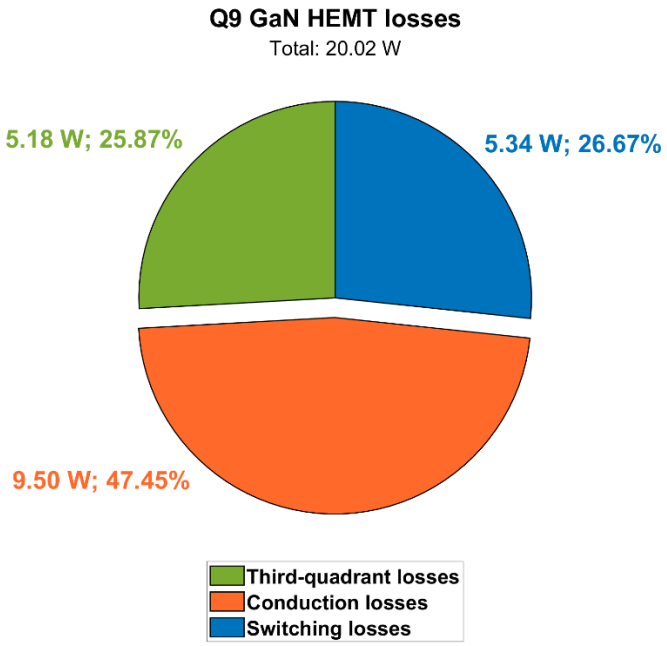


Figure 2.21 Contributions of Q9 power losses (@ V_{out} = 250 V, P_{out} = 4.125 kW, T_{amb} = 60 °C).

Table 2.9 DAB simulation results at T_{amb} = 60 °C, V_{in} = 400 V, V_{out} = 250 V, P_{out} = 4.125 kW, f_{sw} = 300 kHz.

Quantity	Value
XFMR current at primary	19.17 Arms 33.63 A – peak value
XFMR current at secondary	19.06 Arms -33.44 – negative peak value
Current of GaN HEMT at primary	13.45 Arms 33.63 A – peak value
Current of GaN HEMT at secondary	13.77 Arms -34.44 A – negative peak value
DC-link capacitor bank current	7.38 Arms
Output capacitor current	2.10 Arms
Temperature of GaN HEMTs at primary	T_c = 120 °C, T_j = 127 °C
Temperature of GaN HEMTs at secondary	T_c = 107 °C, T_j = 113 °C
DAB XFMR losses	13.91 W
Losses of GaN HEMTs at primary	(4x) 20 W
Losses of GaN HEMTs at secondary	(4x) 16.5 W
DC-link capacitor bank losses	4.54 W
Output capacitor losses	1.10 W
Total losses	165.55 W
V_{out}	250 V
V_{out} voltage ripple	1.75 V_{pk-pk}
I_{out}	16.5 Arms
P_{out}	4125 W
P_{in}	4290.55 W
Efficiency	96.14 %

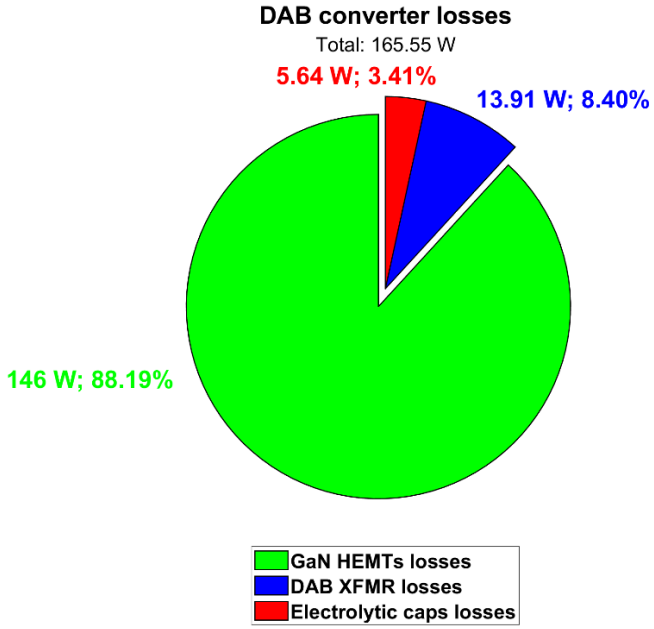


Figure 2.22 Contributions of DAB converter losses (@ V_{out} = 250 V, P_{out} = 4.125 kW, T_{amb} = 60 °C).

2.3. Auxiliary PSFB converter design

The proposed OBC design provides the integration of a third conversion stage in order to supply the 12-V service battery from the HV-rail. Moreover, the exploitation of bidirectional devices and suitable control algorithms enables to implement features such as limp-home and inverter HV DC-link capacitor's precharge from the LV battery.

The most promising topologies to realize this high step-down DC/DC converter are [12,25,26,27]:

- The Phase Shift Full Bridge (PSFB) with center-tapped synchronous rectification;
- The Phase Shift Full Bridge with full bridge synchronous rectification;
- The Current Doubler Phase Shift Full Bridge;
- The Active Clamp Forward with synchronous rectification;
- The Resonant LLC.

A one-fits-all solution does not exist and topology choice depends on current and power levels as well as on voltage ratio, part counts, complexity and cost. As anticipated in Figure 2.1, the center-tapped PSFB with synchronous rectification has been selected for our design. In fact, it is a popular scheme for an EV DC-DC converter benefiting from lower cost and lower complexity. In boost operating mode, i.e. from the LV (low-voltage) to the HV (high-voltage) side, it appears as a current-fed push-pull DC-DC converter [28,29].

From Table 2.1, we recall the auxiliary DC-DC converter main specifications:

Table 2.10. DC-DC LV converter main specifications.

DC-DC LV stage					
$V_{in,range}$	$V_{in,nominal}$	$V_{out,range}$	$V_{out,nominal}$	$P_{out,nominal}$	$P_{out,max}$
240-450 V	360 V	10-16 V	12 V	800 W	1 kW

At primary side the designed PSFB makes use of a full bridge of top-side cooled GS66508T GaN HEMTs (650 V, 30 A, 50 mΩ), driven by Allegro AHV85110 single-channel isolated drivers. At secondary side, two EPC2302 eGaN FETs (100 V, 101 A, 1.4 mΩ) in parallel per switch are used, driven by Texas Instruments UCC27611 single-channel drivers.

High switching frequency (300 kHz) has been selected to obtain very compact magnetic components. The required transformer ratio can be calculated as [30]:

$$n = \frac{N_1}{N_2} \leq \frac{V_{in,min}}{V_{out,nom}} \cdot D_{max} = \frac{240\ V}{12\ V} \cdot 0.7 = 14 \tag{2.15}$$

The breaking voltage of secondary side devices is then decided on the basis of:

$$V_{blocking\ max,sec} = \frac{2 \cdot V_{in,max}}{n} = \frac{2 \cdot 450\ V}{14} \approx 64\ V \tag{2.16}$$

It has been chosen to use 100 V power switches to have a sufficient safety margin with respect to the well-known V_{DS} overvoltage spike issue of this topology due to the resonance between the output rectifier parasitic capacitance and transformer leakage inductors [35]. A RCD snubber solution is adopted to minimize overvoltages on the synchronous rectifier devices.

In order to implement the peak-current mode control (PCMC), the magnetizing inductance of the transformer has to fulfill the condition [30]:

$$L_{mag} \geq \frac{V_{in} \cdot \left(1 - D_{typ}\right) \cdot n}{\Delta I_{Lout} \cdot 0.5 \cdot 2f_{sw}} = \frac{360\ V \cdot (1 - 0.47) \cdot 14}{13.3\ A \cdot 0.5 \cdot 600\ kHz} \approx 670\ \mu H \tag{2.17}$$

where $2f_{sw}$ is the switching frequency of the output inductor and ΔI_{Lout} is the inductor ripple current (20 % of the output current which is equal to $P_{out}/V_{out} \approx 67$ Arms). PCMC guarantees a cycle-by-cycle check on the primary current of PSFB transformer preventing core saturation without the need of a bulky DC-blocking capacitor enhancing the power density. The output inductance can be computed as:

$$L_{out} = \frac{V_{out} \cdot \left(1 - D_{typ}\right)}{\Delta I_{Lout} \cdot 2 f_{sw}} = \frac{12\ V \cdot (1 - 0.47)}{13.3\ A \cdot 600\ kHz} \approx 0.8\ \mu H \tag{2.18}$$

In Table 2.11, PSFB passive components are listed. A really compact size of the PSFB transformer has been achieved: the potting box size is 50 (L) x 34 (W) x 42 (H) [mm].

Table 2.11 PSFB passive components.

Passive component	PN	Quantity	Parameters
PSFB XFMR	Bourns custom design	1	L_{mag} = 838.6 µH (@100 kHz) L_{lk} = 9.3 µH (@100 kHz) $R_{DC,p}$ = 23.6 mΩ $R_{DC,s1,s2}$ = 1.2 mΩ $C_{p,s}$ = 14 pF C_{ww} = 87 pF Turns ratio = 14:1:1
Electrolytic input capacitor	Kemet ALA7DA391CF500	1	V_{DC} = 500 V C = 390 µF ESR = 481.2 mΩ (@ 20 °C, 10 kHz) ESL = 20 nH I_{crms} = 4.12 Arms (@ 85 °C, 10 kHz)
Ceramic capacitor	TDK B58031U5105M062	2x for each GaN leg at primary	V_{DC} = 500 V C = 1 µF ESR = 12 mΩ (@ 0 V_{DC}, 0.5 Vrms, 25 °C, 1 MHz) ESL = 3 nH I_{crms} = 11 Arms (@ 85 °C, 100 kHz)
Output inductor	Vishay IHDM1107BBEV1R1M20	1	L = 1.1 µH (@ 100 kHz, 0.25 V, 0 A) DCR = 0.30 mΩ (@25 °C) Saturation current = 301 A (@ 30% of L drop)
Electrolytic output capacitor	Panasonic EEEFT1H331AV	2x	V_{DC} = 50 V C = 330 µF ESR = 120 mΩ (@ 20 °C, 100 kHz) I_{crms} = 0.9 Arms (@ 105 °C, 100 kHz)
Ceramic output capacitor	Murata GRM32ER7YA106KA12K	5x	V_{DC} = 35 V C = 10 µF ESR = 2 mΩ (@ 0 V_{DC}, 25 °C, 1 MHz)

In Figure 2.23, the PSFB waveforms (360V/12V, 800 W, 300 kHz, dead time = 80 ns, T_{amb} = 60 °C) simulated through PSIM are shown. 650 V GaN HEMTs at primary are

driven with V_{GS} = 6/-3 V and R_G = 10/2 Ω, whereas 100 V eGaN FETs at secondary are driven with V_{GS} = 5/0 V and R_G = 1.6 Ω. PSFB ZVS conditions can be calculated as reported in [26,27]. An external shim inductor is not used in our case, enchancing the power density. Figures 2.24 and 2.25 display a ZVS turn-on for all the switches at primary side.

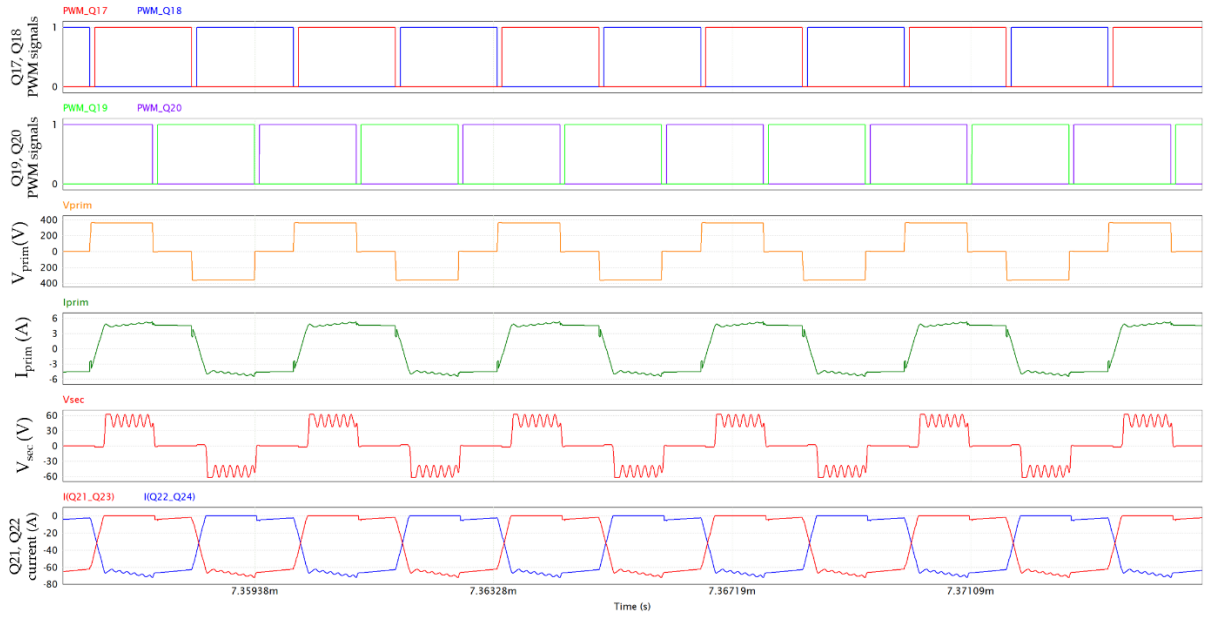


Figure 2.23 PSFB waveforms, from top to bottom: PWM signals of Q17 and Q18, PWM signals of Q19 and Q20, primary voltage, primary current, secondary voltage, Q21-Q23 and Q22-Q24 currents.

The secondary voltage (V_{sec} in the fifth plot of Figure 2.23) corresponds to the V_{DS} of Q21-Q23 when Q22-Q24 are conducting and to -V_{DS} of Q22-Q24 when Q21-Q23 are conducting. The impact of the snubber is visible, maintaining the device drain-source voltages below 62 V, along with the typical ringing effect. The nominal blocking voltage of secondary side devices under the mentioned operating conditions is about 51 V.

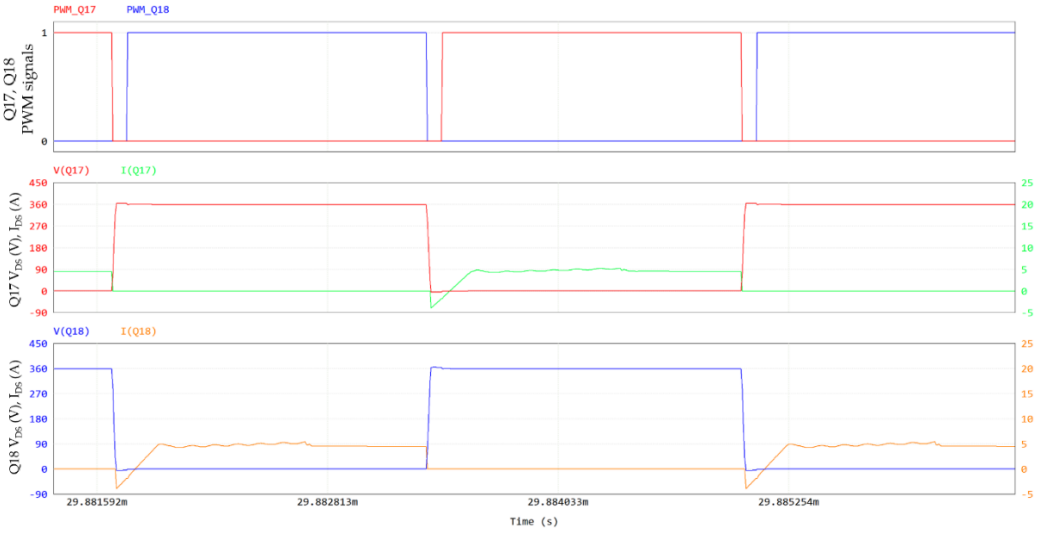


Figure 2.24 PSFB Q17 and Q18 ZVS turn-on: PWM signals of Q17 and Q18, V_{DS} and I_{DS} of Q17, V_{DS} and I_{DS} of Q18. Y-axis of drain-source voltage is on the left, Y-axis of drain-source current is on the right.

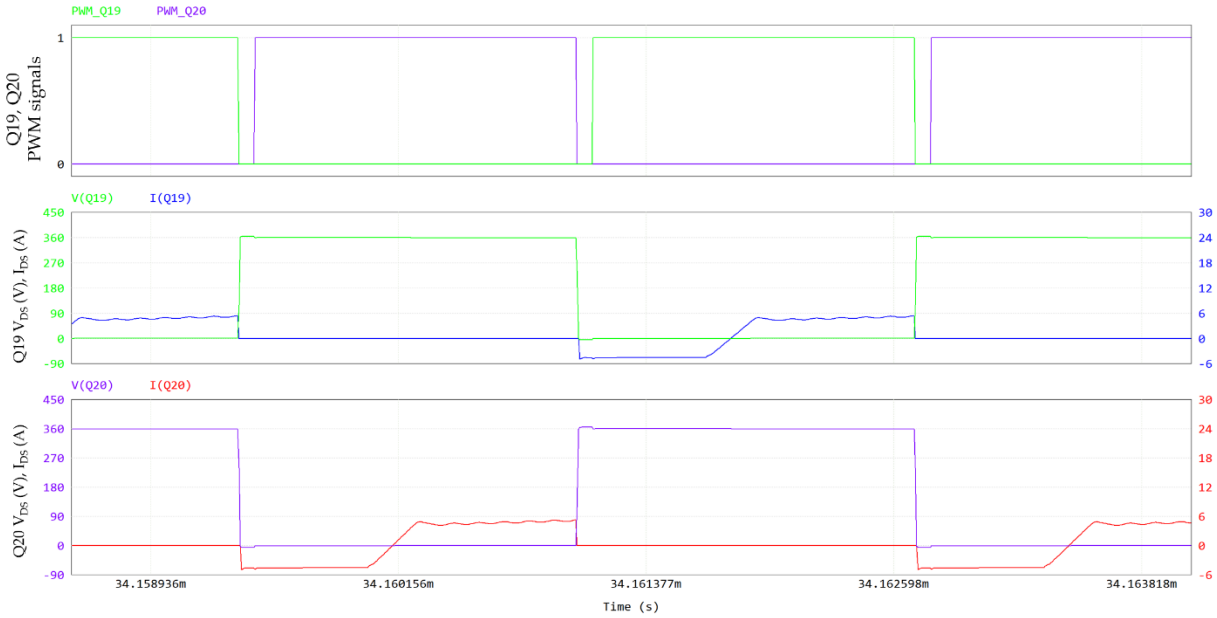


Figure 2.25 PSFB Q19 and Q20 ZVS turn-on: PWM signals of Q19 and Q20, V_{DS} and I_{DS} of Q19, V_{DS} and I_{DS} of Q20. Y-axis of drain-source voltage is on the left, Y-axis of drain-source current is on the right.

Q17 (primary side) and Q21/Q23 (secondary side) currents, temperatures and power losses are shown in Figure 2.26 and 2.27, respectively.

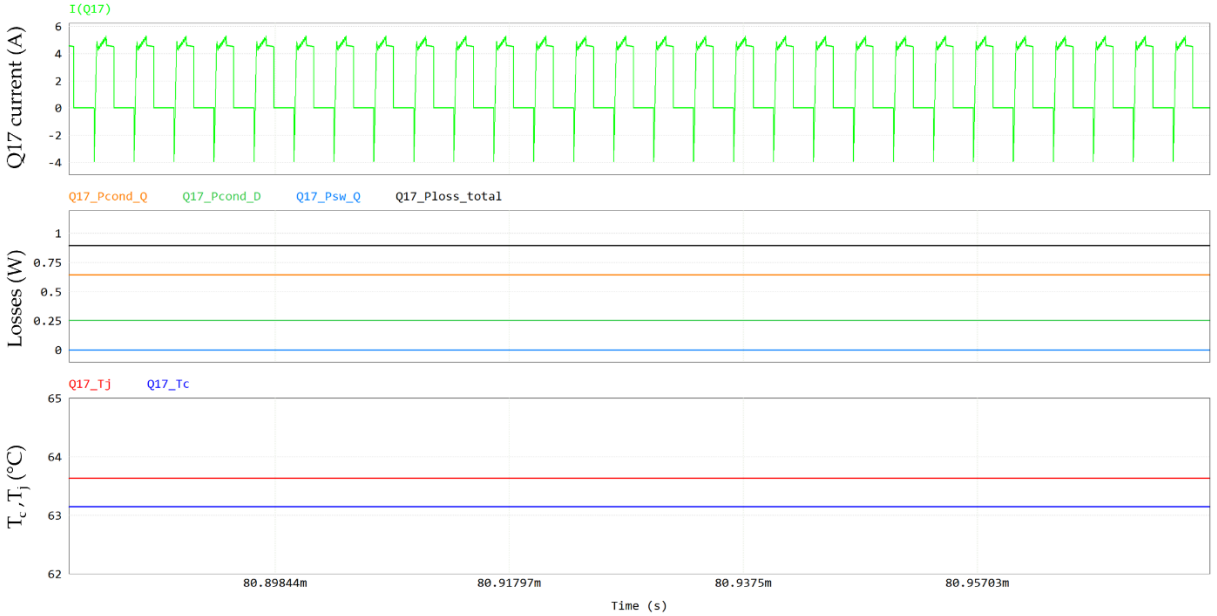


Figure 2.26 Q17 losses, from top to bottom: Q17 current, conduction losses (in orange), third-quadrant losses (in green), switching losses (in light blue), total losses (in black), case (T_c) and junction temperatures (T_j).

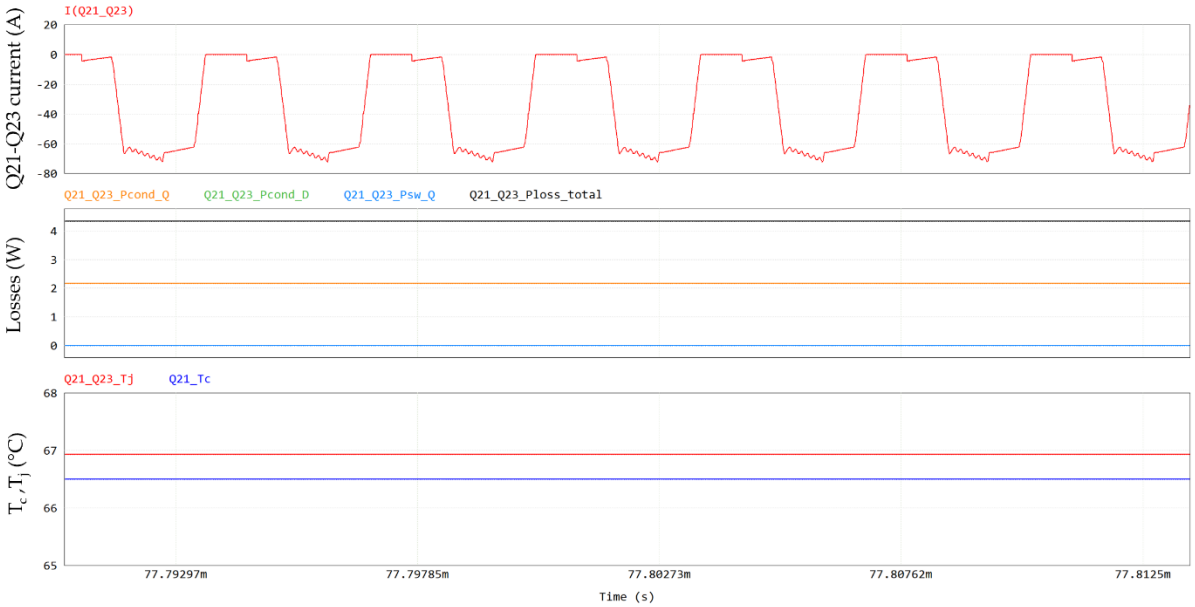


Figure 2.27 Q21/Q23 losses, from top to bottom: Q21-Q23 current, conduction losses (in orange), third-quadrant losses (in green), switching losses (in light blue), total losses (in black), case and junction temperatures. Current in the first plot and losses in the second plot refer to the power switch formed by the parallel of Q21-Q23, whereas temperatures refer to the individual device.

The custom-designed transformer (UI core) exploits Litz wire to reduce the skin effect. Simulation of power losses performed through ANSYS software results in 1.5 W for the core, 2.25 W and 6 W for winding losses at primary and secondary side, respectively. Power dissipation of output inductor can be estimated in 1.33 W. RCD snubber losses (two capacitors 100V-220nF, two resistors 1kΩ-2W) are computed in 4.83 W. Losses of electrolytic capacitors can be quantified in 0.1 W, leading to negligible losses in terms of the total thermal budget.

Table 2.12 and Figure 2.28 summarize the PSFB simulation results. The total dissipated power is quantified in 29.87 W and PSFB efficiency turns out to be 96.40 % (at 60 °C coolant temperature).

Table 2.12 PSFB simulation results at T_{amb} = 60 °C, V_{in} = 360 V, V_{out} = 12 V, P_{out} = 800 W, f_{sw} = 300 kHz.

Quantity	Value
XFMR current at primary	4.47 Arms 5.40 A – peak value
XFMR current at secondaries	45.54 Arms -72.40 A – negative peak value
Current of GaN HEMT at primary	3.15 Arms 5.40 A – peak value
Current of GaN switch at secondary	45.54 Arms -72.40 A – negative peak value
Input electrolytic capacitor current	0.56 Arms
Output capacitor bank current	2 Arms
Output inductor current	66.67 Arms 71.15 A – peak value 9.45 A_{pk-pk} – ΔI_{max}
Temperature of GaN HEMTs at primary	T_c = 63.1 °C, T_j = 63.6 °C
Temperature of eGaN FETs at secondary	T_c = 66.3 °C, T_j = 66.9 °C
PSFB XFMR losses	9.75 W
Losses of GaN HEMTs at primary	(4x) 1.3 W
Losses of eGaN FETs at secondary	(4x) 2.19 W
Output inductor losses	1.33 W
RCD snubber losses	4.83 W
Total losses	29.87 W
V_{out}	12 V
V_{out} voltage ripple	0.43 V_{pk-pk}
I_{out}	66.67 Arms
P_{out}	800 W
P_{in}	829.87 W
Efficiency	96.40 %

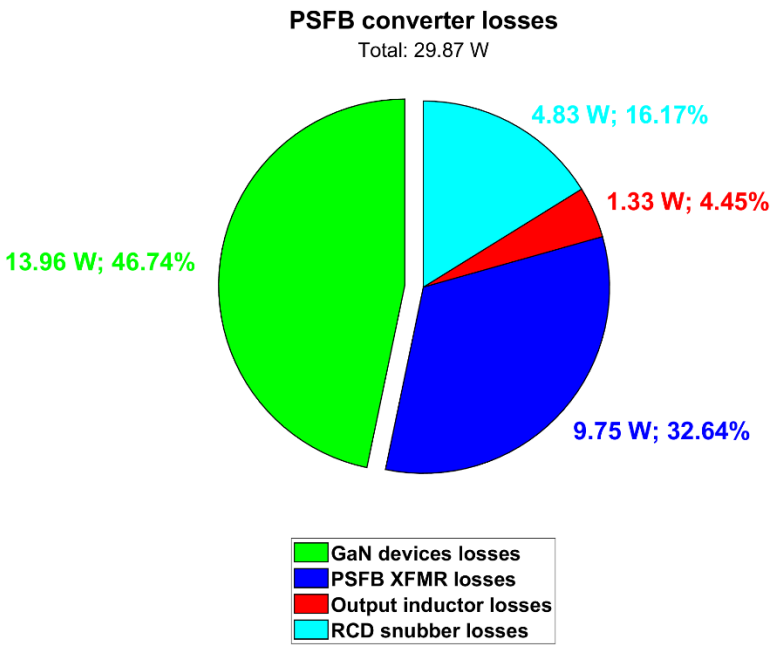


Figure 2.28 Contributions of PSFB converter losses (@T_{amb} = 60 °C).

2.4. Converter control

Figure 2.29, that recalls for convenience the overall system topology anticipated in Figure 2.1, describes at high level the OBC control architecture. Seven different currents and four different voltages are sensed by means of isolated Hall-effect current sensors (Allegro ACS733KLATR-40AB-T) and reinforced isolated amplifiers (TI AMC3330DWER). The 32-bit 200 MHz real-time microcontroller TMS320F28P659D from C2000 family of Texas Instruments is exploited to implement the control algorithms, along with CAN communications and other service tasks. Internal 12 and 16 bit ADCs are used for the digitalization of sensed signals. The µC generates 20 different gate PWM signals (since devices in parallel share the same PWM signal). Gate signal buffering and isolation is implemented by the gate drivers mentioned in the previous sections.

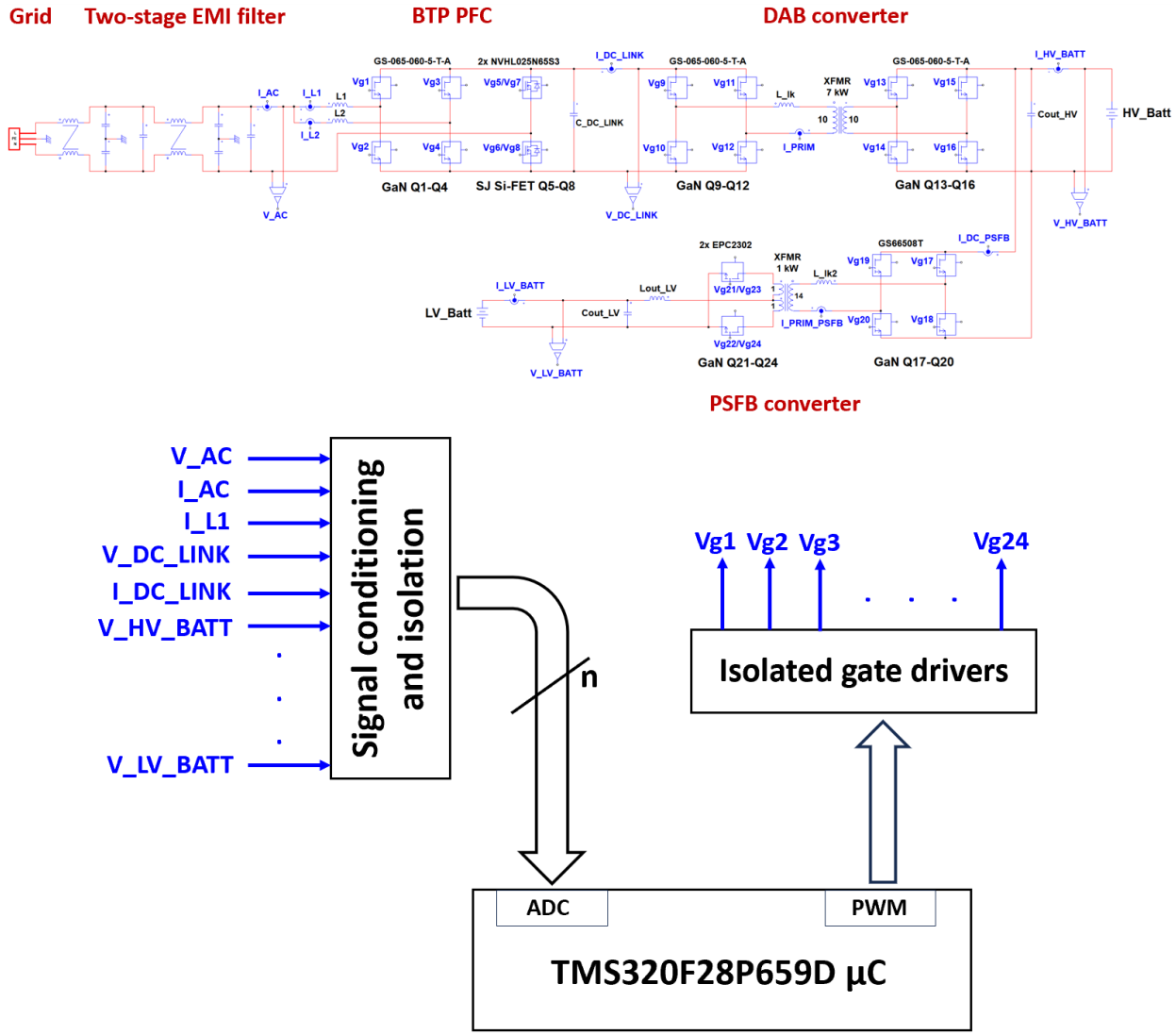


Figure 2.29 OBC simplified control architecture.

The BTP PFC control technique consists of two main feedback loops that regulates the output voltage (outer and slower loop) and the two input currents (inner and faster loops) where sinusoidal shape is superimposed by sensing L-N voltage for PFC purposes [16,36]. The bandwidth of the voltage and current regulators are set respectively to five time less the grid frequency to avoid distortion, and a range between a decade above the voltage bandwidth and a decade under the antiresonance frequency of the input EMI filter.
In order to improve the harmonic distortion and the power factor three main techniques have been implemented:

- Reduction of current spikes during the zero-crossing, caused by the charge/discharge of the C_{oss} of HF and LF devices, is obtained implementing a soft-start procedure every half period [33-35];
- A PLL-SOGI filter is applied to the AC-voltage measured signal;
- An internal model compensator is applied to the input currents up to the 9th harmonic of the grid frequency.

Finally, a start-up procedure is designed to minimize the occurrence of conduction of the diode-rectifier (placed parallel to the BTP to pre-charge the output capacitors) when PWM are triggered on and output voltage is tied to the voltage grid peak. Basically, the converter begins to be piloted few moments after the peak value of the grid in order to boost the output voltage for almost an entire grid period avoiding any diode being positively forward.

With regard to the DAB converter, it is piloted in SPS modulation and controlled by a single feedback loop on the output voltage, (similarly to [36]), where the reference power is retrieved, and phase-shift angle is forced to the converter. Since the load is a HV-battery, the regulator manages the amount of power by saturating to the maximum current on the level required by the battery or handled by the system. Given the slow dynamic of charging procedure compared to control bandwidth, no feedforward terms are employed avoiding regulator overshoot.

For the PSFB converter, the peak current mode control (PCMC) has been implemented as described in [37,38]. This choice guarantees a cycle-by-cycle check on the primary current of the transformer preventing consequently the core saturation without the need of a bulky DC-blocking capacitor enhancing power density. The outer voltage control is implemented by software and compensates the plant (output capacitor) by a PI regulator, while the inner current control is entirely managed by dedicated hardware due to the bandwidth required (twice the switching frequency). The hardware resources have been made available by the F28P65x that integrates a Comparator Subsystem (CMPSS) Type-6 and Enhanced PWM (ePWM) Type-5 specifically designed for such control mode.

In terms of software, the entire system is managed by a TMS320F28P659D μC consisting of two separated cores. Given the different switching frequencies of BTP

(130 kHz) and DAB/PSFB (300 kHz), the first converter relies on the first core, while the last two converters on the second. Concerning the execution timing, the code is organized in two main tasks: a fast task (30 kHz), where the control algorithms are executed, and a slow task (1 kHz) in charge of handling context conditions such as presence of HV plugs, enabling internal supplies, etc.

2.5. OBC implementation and validation measurements

The OBC has been implemented on a 8-layers PCB, optimizing the power density and wisely exploiting layers as shielding ground planes for EMI minimization. All the high-frequency commutating GaN devices are placed on the bottom layer. The thermal pad of their top-side cooled package is connected through a very high-performance TIM (thermal interface material) to a custom-designed cold plate that spans beneath the entire PCB. The PCB is properly shaped with internal and lateral slots so that, all the custom magnetic components (i.e., DAB transformer, PSFB transformer and PFC choke inductors) are encapsulated in an aluminum box and screwed directly to the cold plate to optimize the power dissipation.

In Figures 2.30, 2.31 and 2.32 the pictures of the different sections of the OBC are shown with some dimensional references. The dimensions of the different sections are also indicated. The space occupancy of the circuits is very limited, due to compact magnetics and capacitors enabled by the operation at high switching frequency and the fast control. Moreover, the OBC size can be further reduced in successive iteration of the PCB, since this first prototype is designed for accessibility of probing for verification and debugging. The entire OBC PCB will be enclosed in an aluminum box integrating the cold plate and all the connectors to the grid and the batteries.

At this stage the first PCB prototype has been partially tested at room temperature. The PFC section has been tested at full power (6.6 kW) with 230 Vrms, 50 Hz grid voltage and nominal 400 V output voltage (16.5 A output current). Also, the DAB converter has been tested at room temperature up to 4.5 kW with V_{in} = 400 V = V_{out} and an output current of 11.25 A.

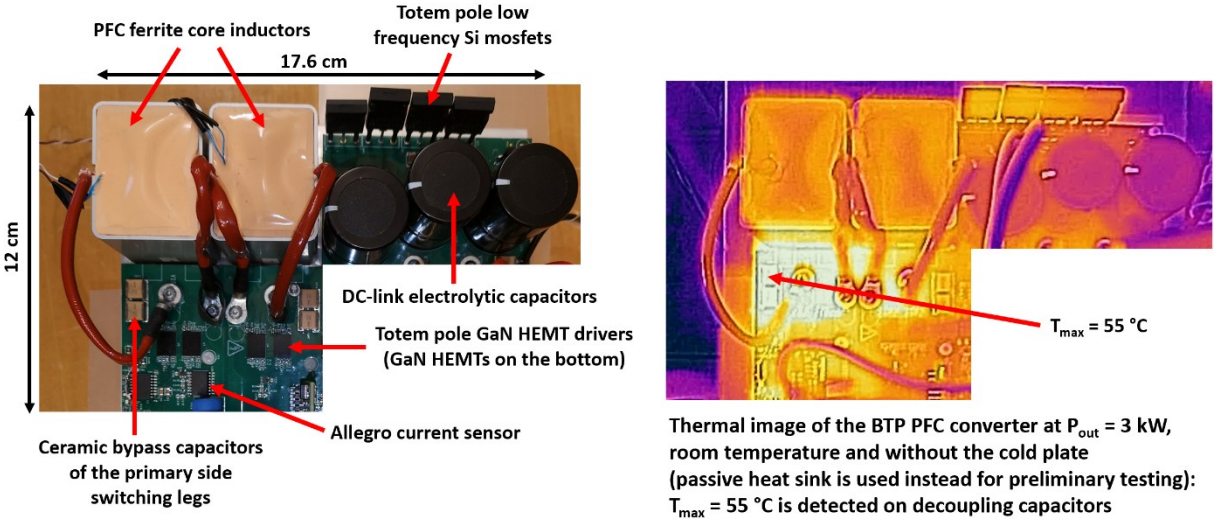


Figure 2.30 OBC prototype: BTP PFC converter and thermal image.

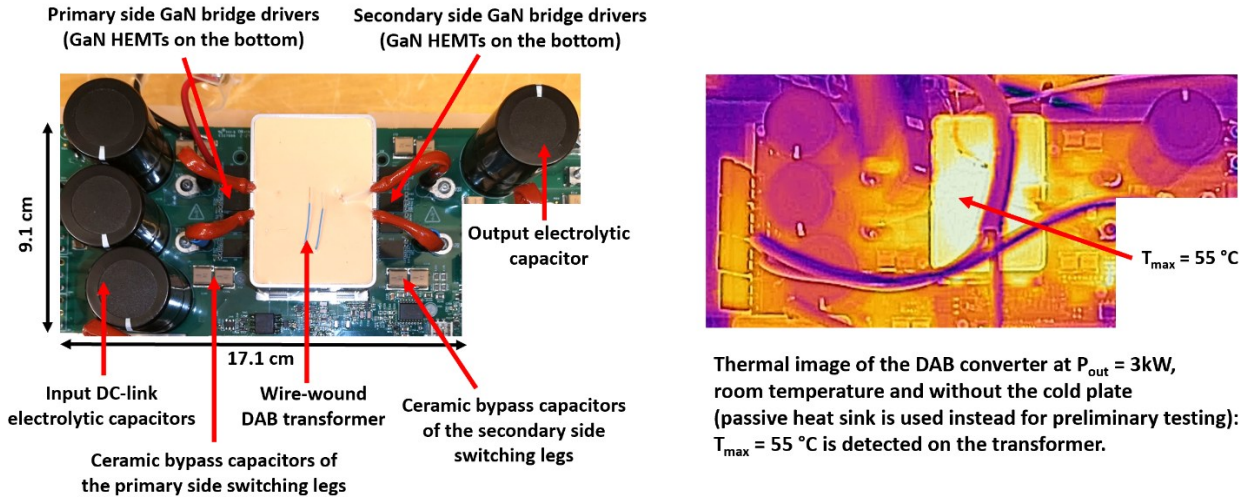


Figure 2.31 OBC prototype: DAB converter and thermal image.

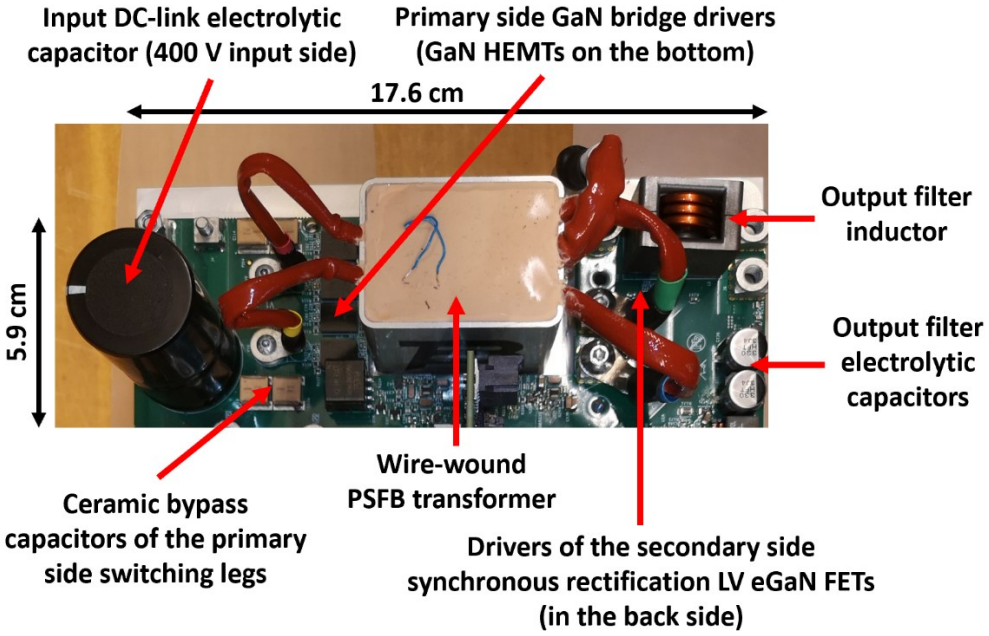


Figure 2.32 OBC prototype: PSFB converter.

The converter efficiency computed by preliminary measurement characterization is very close to simulated values. Also, thermal images of the converters confirmed the expected case temperatures of visible components such as magnetics, capacitors and gate drivers: some examples of thermal images are shown in Figures 2.30 and 2.31. Some measured waveforms at 3.3 kW such as the DAB converter primary current I_L, V_{DS} and V_{GS} voltages of DAB Q10 GaN HEMT, are shown in Figures 2.33, 2.34 and 2.35 along with simulations. The waveforms are measured exploiting wideband sensors (20 MHz Rogoski current probe and 100 MHz active differential voltage probe) and digital oscilloscope (500 MHz MSO-56 Tektronix at 6.25 GS/s) that can capture without filtering/attenuating any eventual high frequency component (e.g., ringing) of the waveforms. The very clean waveforms without overshoots or ringing reveal an effective low-parasitic PCB design and the quality of magnetics that exhibit extremely low parasitic capacitances. Simulation waveforms derive from the post-layout simulation of the DAB converter, i.e. taking into account also the S-parameters matrix which is the result of the EM simulation of the board, performed through Keysight Advanced Design System (ADS), that made it possible to find a better trade-off between third-quadrant and switching losses [2] for our design case if $V_{GS,off}$ = -1 V is implemented (as opposed to $V_{GS,off}$ = -3 V). Details on device commutation behaviour is presented in the next Chapter.

The converter prototype will be further tested at different operative and temperature conditions and then will be encapsulated in the final metal box with integrated cold plate for EMI pre-compliance characterization.

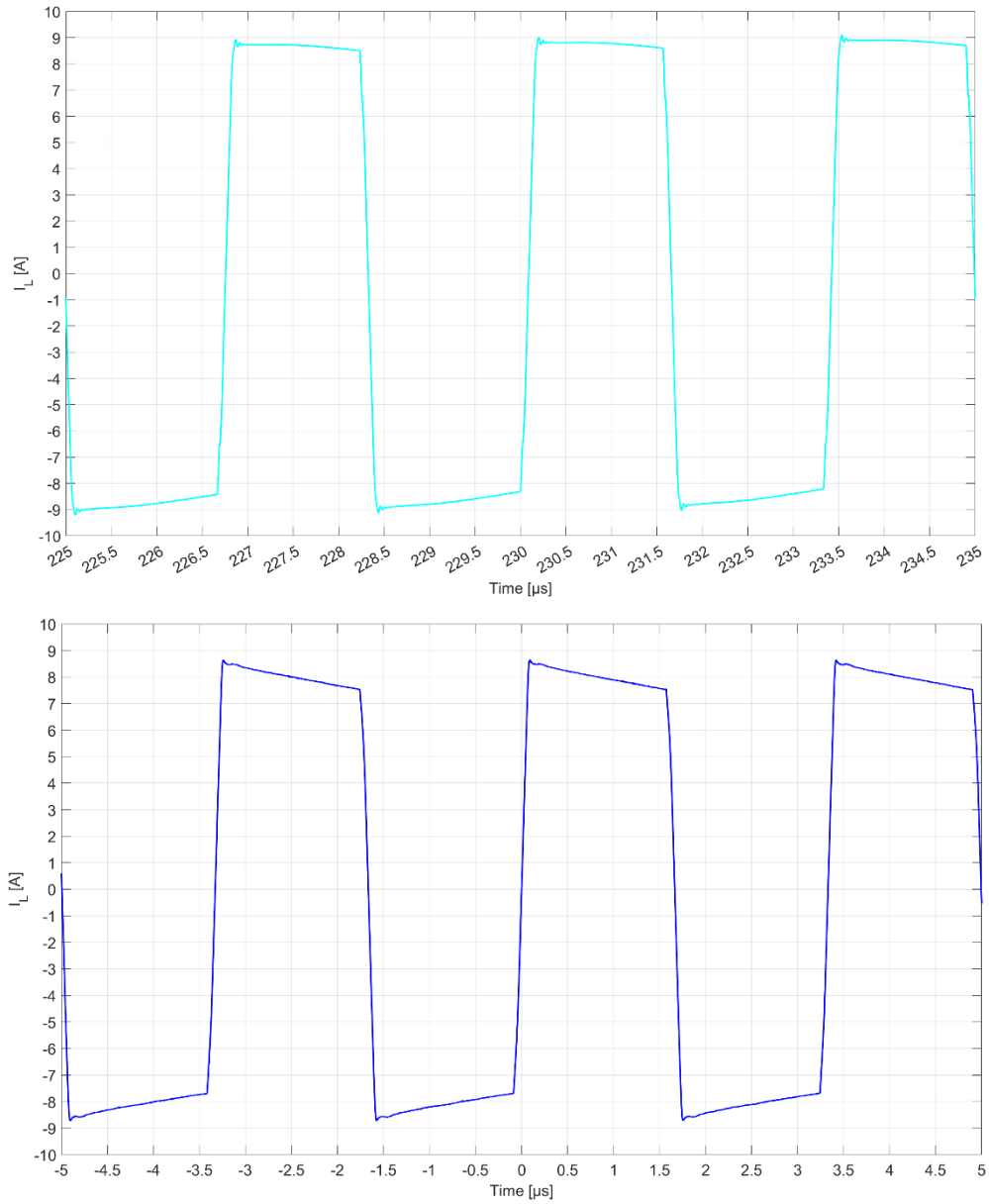


Figure 2.33 Comparison between the series inductor current I_L from post-layout simulation (first plot) and I_L from scope acquisition (second plot).

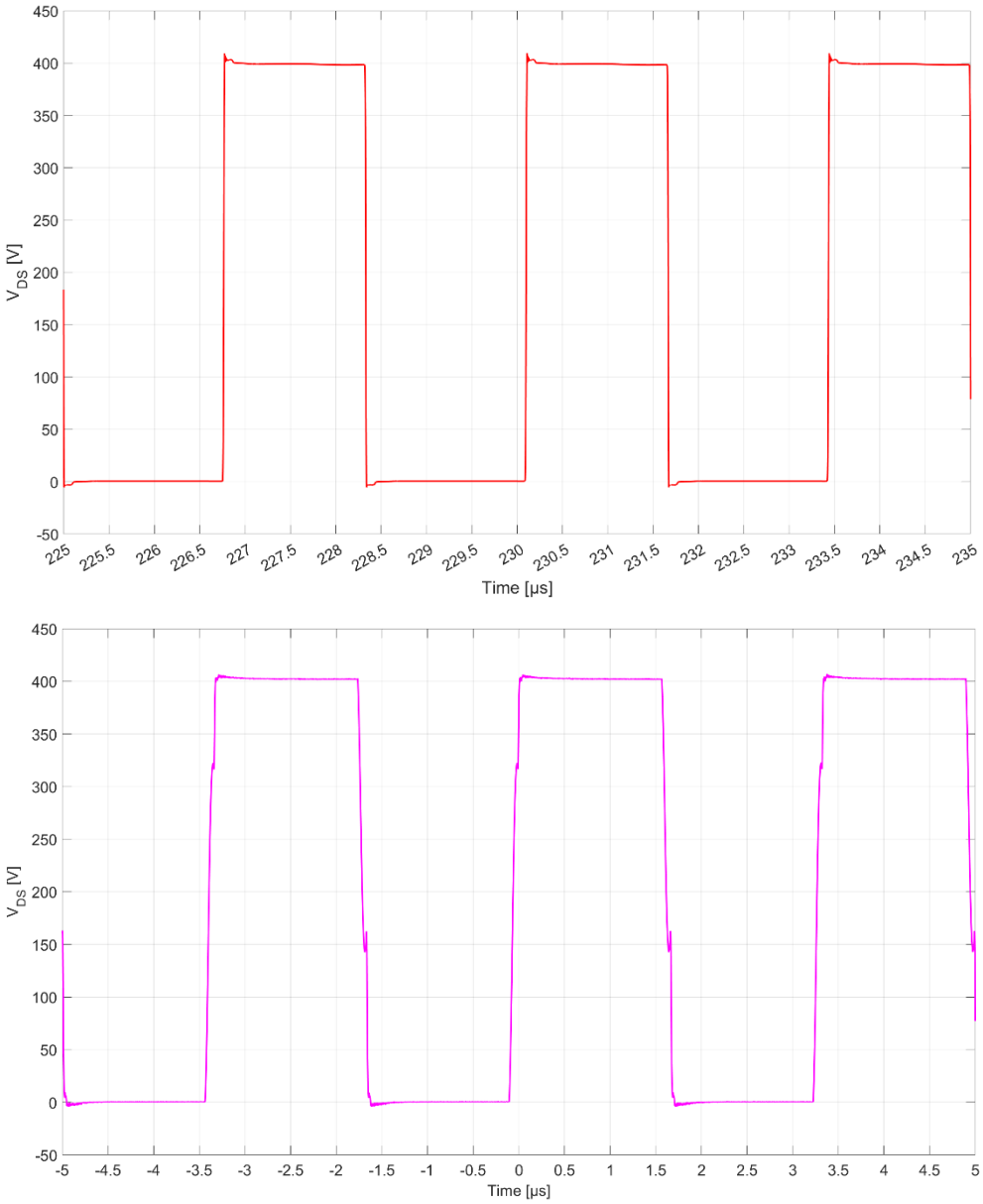


Figure 2.34 Comparison between V_{DS} of Q10 from post-layout simulation (first plot) and V_{DS} of Q2 from scope acquisition (second plot).

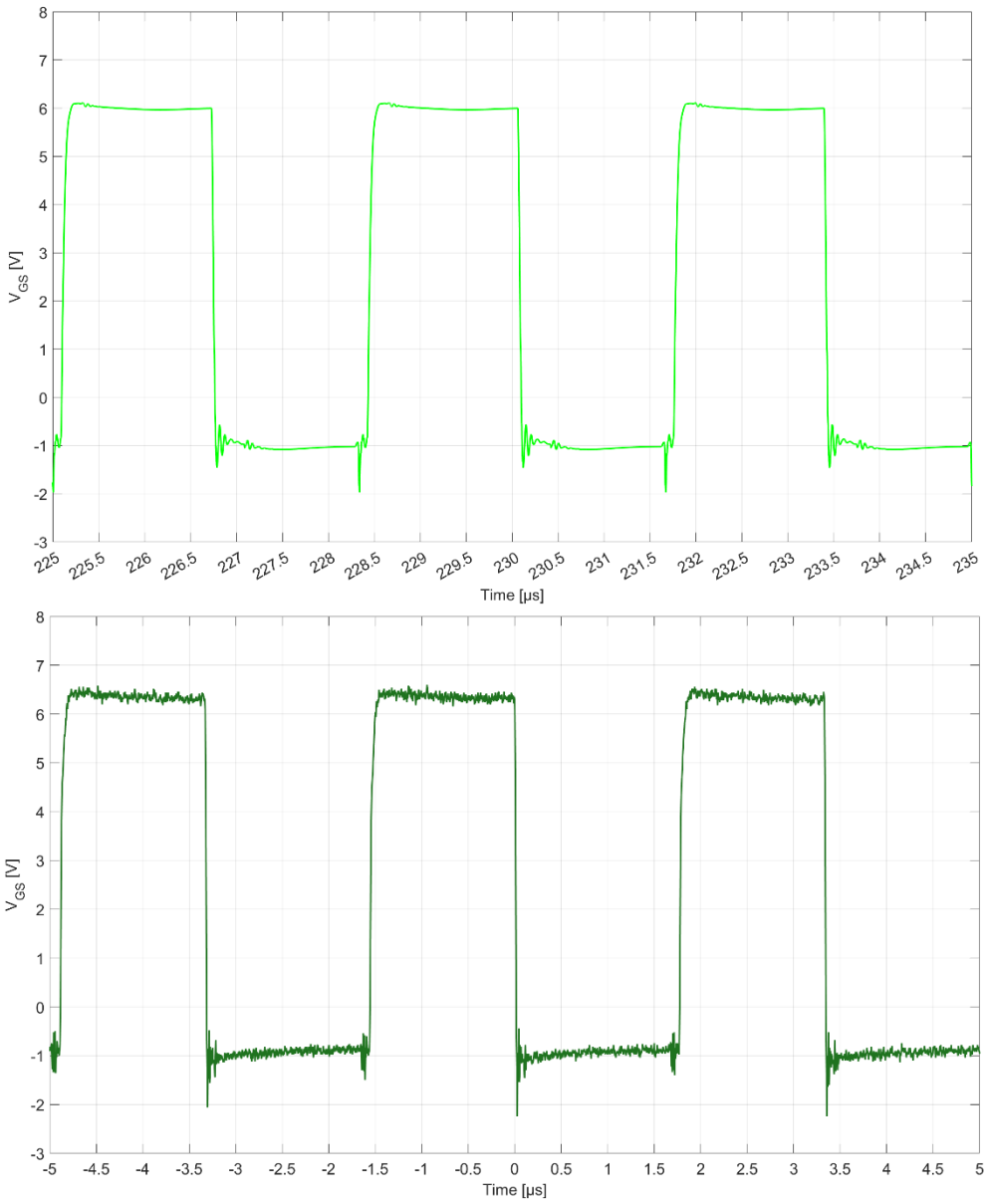


Figure 2.35 Comparison between V_{GS} of Q10 from post-layout simulation (first plot) and V_{GS} of Q2 from scope acquisition (second plot).

2.6. Conclusions

The comprehensive design of a GaN-based OBC for automotive application has been described. Detailed simulations enabled to estimate power loss distributions and overall performances by means of accurate models of the components. The simulated performances at the maximum operative temperature of 60 °C are at the state-of-the-art. Preliminary characterization measurements on the first prototype are in line with simulation results, indicating the effectiveness of the design and simulation approach.

Chapter 3

Accurate Evaluation of commutations of 650-V GaN Power Switches in a 6.6-kW Dual Active Bridge DC-DC converter

State-of-the-art On-Board Chargers in the medium-power range, are currently represented by 4 kW/L, 98%-efficient bidirectional On-Board chargers (OBCs) with integration of an auxiliary DC-DC converter for interconnection to the 12-V service battery [6,39]. These top notch features are made possible by the exploitation of Gallium Nitride, which benefits from some exceptional properties with respect to the heritage Silicon-based technology, such as wider band gap, higher breakdown field and thermal conductivity, superior electron mobility and carrier drift velocity [3,40]. This implies that a better trade-off between efficiency and power density can be achieved due to the reduced losses at high switching frequency, enabling also the shrinking of passive components (transformers and LC/CL filters).

However, fast commutations of WBG devices with very high dv/dt and di/dt require to precisely assess, minimize and compensate any parasitics of the circuit, otherwise several issues may arise in terms of reliability, electromagnetic interference (EMI) and performance degradation [9,23,41]. The accurate evaluation of device commutations is necessary for a correct estimation of losses and of the corresponding thermal design. As a consequence, during the design phase it is paramount important to analyze the device switching behaviour combined with a precise assessment of passive components' parasitics and electromagnetic simulations of the PCB layout.

In the following, a deep insight into the switching waveforms of a 6.6 kW DAB (Dual Active Bridge) DC-DC converter in GaN technology is carried out, explaining details of the ZVS turn-on and almost ZVS turn-off commutations at the intrinsic device by means of the non-linear dynamic model of the transistor, distinguishing between channel current and parasitic capacitance Cgs, Cgd, Cds currents. The influence of the driver characteristics and PCB parasitics on converter performances is accurately reproduced in Keysight Advanced Design System (ADS) through electrical

and electromagnetic simulations, i.e. the post-layout simulation takes into account the PCB parasitics represented by the S-parameters matrix which is the result of the EM simulation of the PCB.

Hence, the design has been validated prior to the board production, saving cost and accelerating the product time to market, avoiding vicissitudes and redesign due to the lack of an analysis tool capable of a precise estimation of the design requirements in terms of parasitics. This approach is modus operandi in RF (Radio Frequency) electronics, but becomes also very valuable in power electronics, where very fast commutations at high switching frequency occur when exploiting WBG semiconductors at their best potential. The DAB converter under examination is part of the high power density 400-V GaN OBC that has been descripted so far.

In Section 3.1, the Pspice non-linear dynamic model of the GaN HEMT (GS-065-060-5-T-A) is exploited to extract static and dynamic characteristics of the transistor; in Section 3.2, details of device turn-on and turn-off commutations in the DAB converter prototype are discussed taking into account device and passive components' parasitics. Finally, in Section 3.3 also the PCB role is investigated by means of electromagnetic (EM) simulations.

3.1 Assessment of GaN HEMT GS-065-060-5-T-A characteristics and non-linear dynamic model validation

For convenience, Table 3.1 recalls the datasheet parameters of the GaN HEMT used in the Dual Active Bridge HV (high-voltage) DC-DC converter.

Table 3.1 Datasheet parameters of GaN HEMT GS-065-060-5-T-A.

V_{DS}	I_{DS} @Tc = 25 °C; @Tc = 100 °C		$R_{DS,on}$ @Tj = 25 °C; @Tj = 150 °C	
650 V	60 A; 41 A		25 mΩ; 65 mΩ	
C_{iss} (@400 V)	**C_{oss} (@400 V)**	**C_{gd} (@400 V)**	**Q_{gd} (@400 V)**	**Q_g (@400 V)**
516 pF	127 pF	2.4 pF	4.1 nC	14 nC
E_{on}, E_{off}, E_{oss} (@ 400 V, 20 A, R_G = 10/2 Ω, V_{GS} = 6/-3 V, Tj=25 °C)				
117 μJ		17.2 μJ		17 μJ
Package inductances L_g, L_d, L_s (from Pspice level 3 model)				
4 nH		0.2 nH		0.3 nH

As it is clear from the previous Table, GS-065-060-5-T-A embedded package [42] contributes to ensure ultra-low device stray inductances and parasitic capacitances with respect to the traditional wire-bonded QFNL (Quad Flat No-Lead) or TO (Transistor Outline) packages.

The Pspice non-linear dynamic model is provided by the manufacturer and has been imported in ADS to be used for the detailed study of commutation behaviour. Several simulations have been performed to assess the capability of the model to properly reproduce the measured static and dynamic electrical quantities reported in the device datasheet. Figures 3.1-3.5 report transcharacteristic, transconductance and output characteristic of the transistor at different channel temperatures Tj, obtained through DC (i.e. static) ADS simulations.

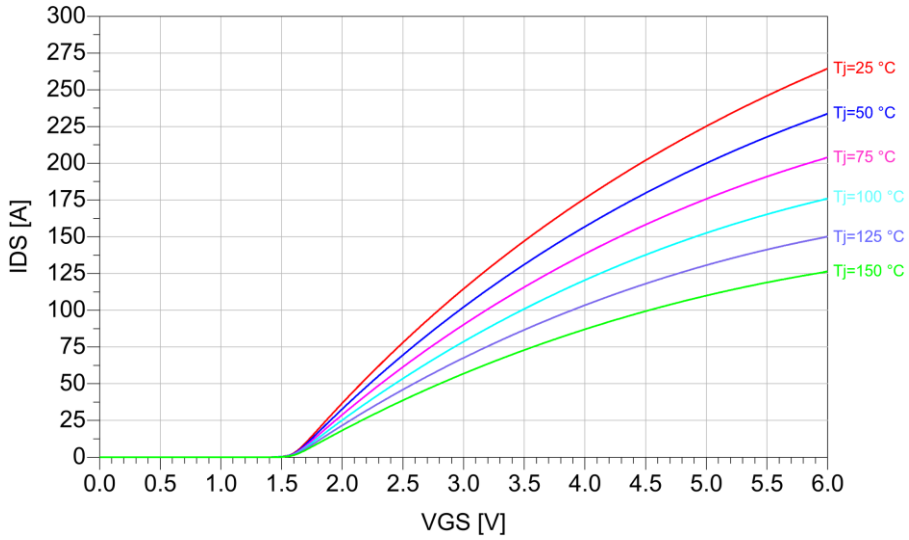


Figure 3.1 GS-065-060-5-T-A transcharacteristic, @V_{DS} = 10 V.

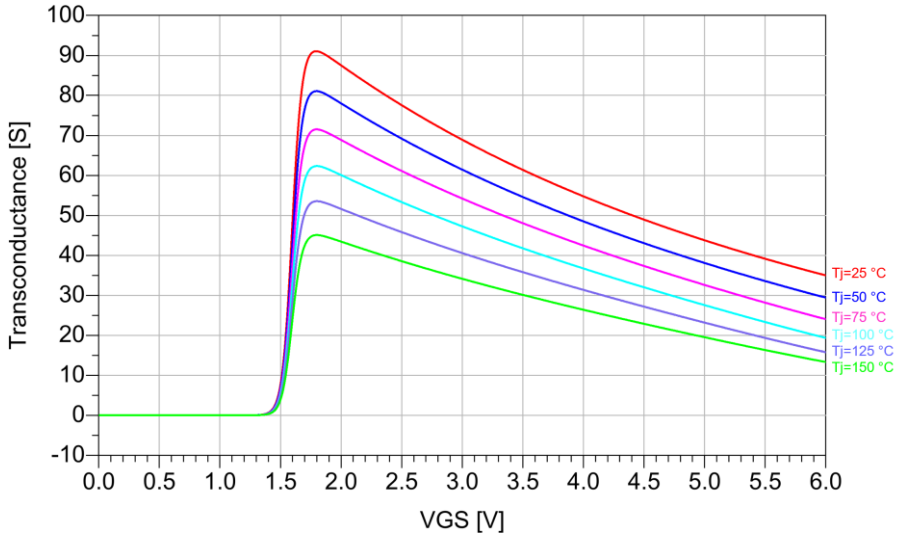


Figure 3.2 GS-065-060-5-T-A transconductance vs V_{GS}, @V_{DS} = 10 V.

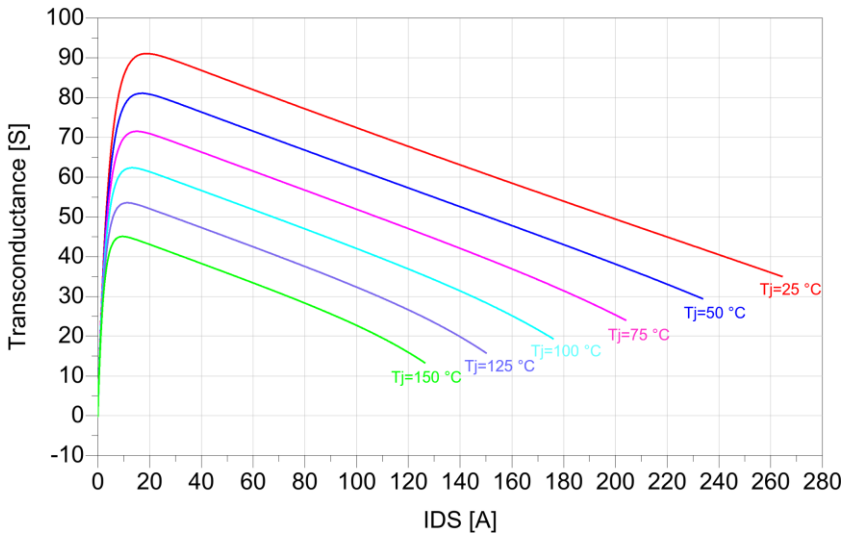


Figure 3.3 GS-065-060-5-T-A transconductance vs I_{DS}, @V_{DS} = 10 V.

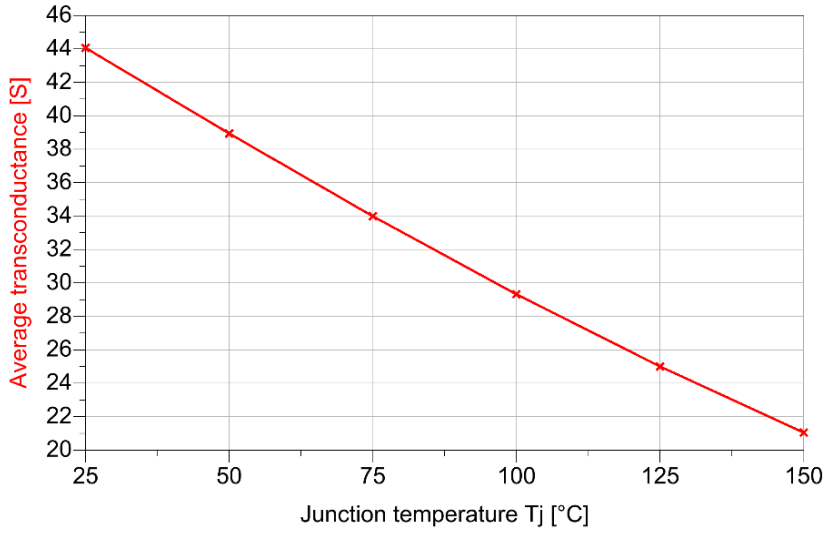


Figure 3.4 GS-065-060-5-T-A average transconductance vs junction temperature, @V_{DS} = 10 V.

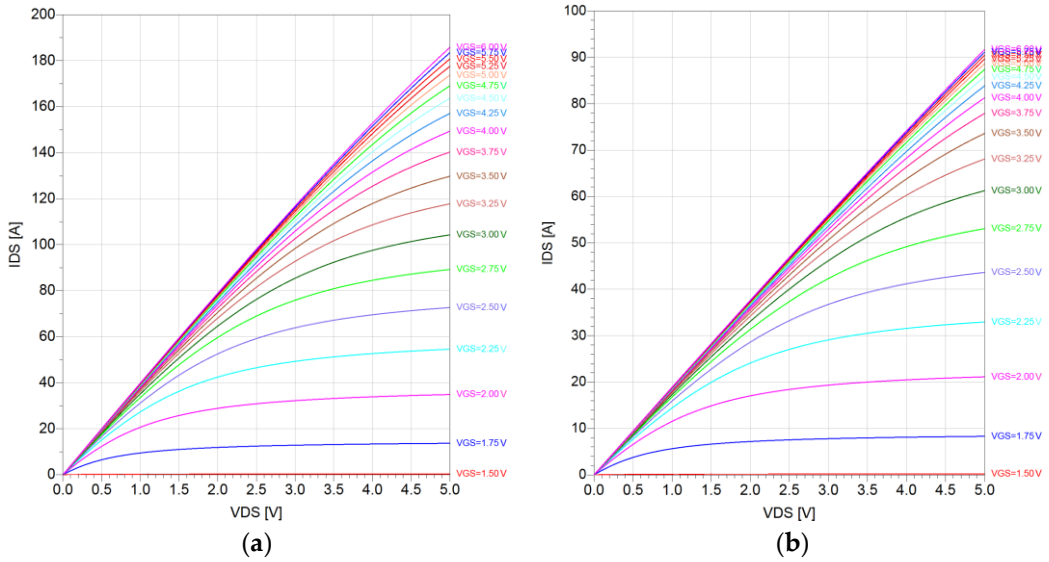


Figure 3.5 GS-065-060-5-T-A a) Output characteristic @25 °C; b) Output characteristic @120 °C.

GaN devices exhibit a stable gate-source threshold voltage $V_{GS(th)}$ over temperature and a negative temperature coefficient of the transconductance (Figures 3.1-3.5), in addition to a positive temperature coefficient of the $R_{DS,on}$ (as depicted in the simulation result shown in Figure 3.6). This implies easier thermal balance and superior paralleling capability with respect to SiC and Si devices, making GaN particularly suitable in applications where multiple devices in parallel are required, e.g. high-frequency and high-current multilevel topologies [39,43,44] in which GaN is used to overcome its reduced blocking voltage (up to 650 V for commercial devices) with respect to SiC and Si. At the same time, GaN can benefit from its excellent transconductance, ensuring low rise/fall times during switching transitions and enabling exceptional dynamic performances due to the combination of reduced parasitics and high switching frequency regime.

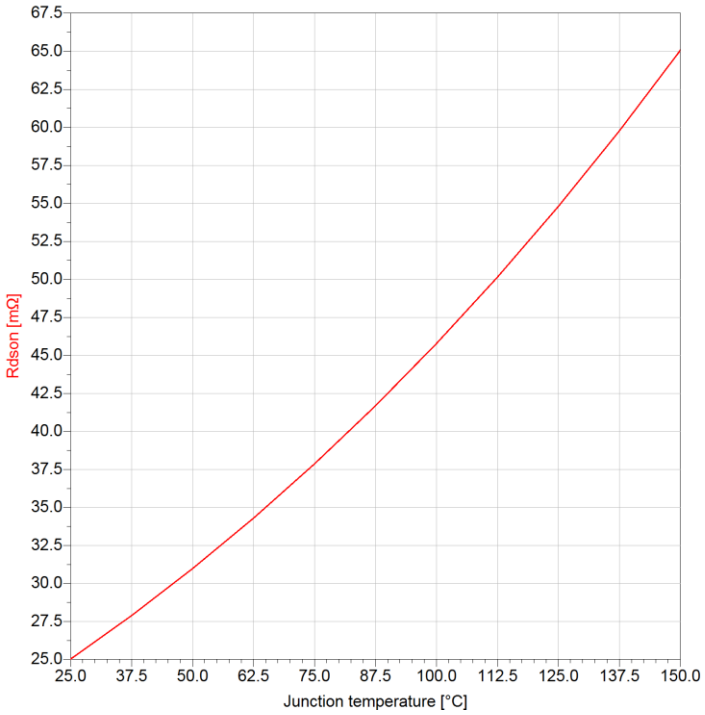


Figure 3.6 GS-065-060-5-T-A $R_{DS,on}$ vs junction temperature (@ V_{GS} = 6 V, I_{DS} = 18 A).

Another notable feature of GaN HEMTs is the absence of a parasitic body-diode: since the two-dimensional electron gas (2DEG) channel can conduct in the third quadrant, they are inherently capable of reverse conduction [17]. The lack of reverse recovery loss (Q_{rr} = 0) and uncontrolled high dI_{rr}/dt enables higher efficiency (lower E_{on}) and cleaner waveforms (lower EMI). Hence, in a GaN phase leg hard-switching transition, the voltage commutation immediately follows the current commutation.

The output non-linear capacitance C_{oss} is being charged/discharged during voltage commutations leading to E_{qoss} (for high-side device) and E_{oss} (for low-side device) energy dissipations, which can be quantified according to [46] as:

$$E_{qoss} = \int_0^{V_{DC}} (V_{DC} - V_{DS}) \cdot C_{oss\,(V_{DS})}\, dV_{DS} \tag{3.1}$$

$$E_{oss} = \int_0^{V_{DC}} V_{DS} \cdot C_{oss\,(V_{DS})}\, dV_{DS} \tag{3.2}$$

These loss contributions are inevitable in hard-switching applications and are particularly relevant under light-load operating conditions. Instead, in soft switching regimes with ZVS turn-on, these energies are recycled back to the circuit and do not contribute to power dissipation (unless second-order non-idealities are considered [47,48]).

As observed in [45,49,50], the turn-on and turn-off losses reported in the datasheet are the external measurable quantities, i.e. they take into consideration the total drain-source current I_{DS}:

$$E_{on\_external} = E_{VI\_on} + E_{qoss} \tag{3.3}$$

$$E_{off\_external} = E_{VI\_off} + E_{oss} \tag{3.4}$$

while the intrinsic energies taking into account the channel current ($I_{channel}$) are equal to:

$$E_{on\_intrinsic} = E_{VI\_on} + E_{qoss} + E_{oss} \tag{3.5}$$

$$E_{off\_intrinsic} = E_{VI\_off} \tag{3.6}$$

where E_{VI} is the switching energy related to the overlap of drain-source voltage and channel current during commutations.

Typically E_{qoss} is not listed in the datasheet, instead it is part of $E_{on\_external}$. E_{qoss} and E_{oss} of GS-065-060-5-T-A GaN HEMT device have been calculated from (3.1) and (3.2) through a Matlab script by making use of the $C_{oss(VDS)}$ curve of the datasheet. As observed in [46], these informations can be conveniently displayed in a plot of E_{qoss}/E_{oss} energies Vs the actual V_{DS} swing across the device: Figure 3.7 reports this plot for the GS-065-060-5-T-A GaN HEMT. For the E_{qoss}, each value of the rail-voltage V_{DC} identifies a different curve. The following results are obtained from the plot for the case V_{DC} = 400 V:

$$E_{qoss}\,(@400\text{ V}) = 37.52\ \mu\text{J} \tag{3.7}$$

$$E_{oss}\,(@400\text{ V}) = 17.30\ \mu\text{J} \tag{3.8}$$

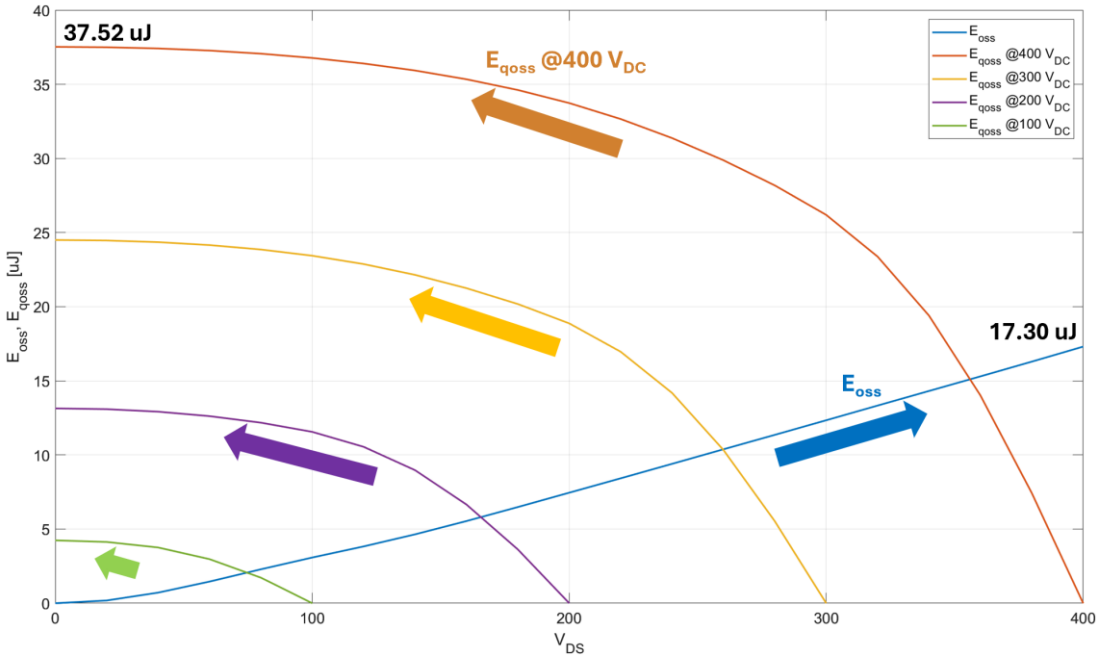


Figure 3.7 E_{oss} and E_{qoss} loss of GS-065-060-5-T-A at different operating voltage.

A Double Pulse Test (DPT) simulation (i.e. time domain dynamic simulation, in Figure 3.8) has been performed in Advanced Design System, under the same conditions at which the switching losses are reported in the datasheet: V_{DC} = 400 V, I_{DS} = 20 A, R_G = 10/2 Ω, V_{GS} = 6/-3 V, Tj = 25 °C. As suggested by GaN Systems [51], a gate inductance of 3 nH due to the driver component is considered in addition to the level 3 model of the GaN HEMT, and rise/fall times of driver switches are set to 1 ns. Under these conditions, the impact of the overall gate inductance (7 nH) is quite significant. In Figure 3.8 the extrinsic V_{GS} at device terminals (in green), and the intrinsic V_{GS} devoided of device stray inductances (in red) are displayed. Package drain and source inductances, instead, are such extremely low (hundreds of pH) that there is practically no difference between intrinsic and extrinsic V_{DS} voltages.

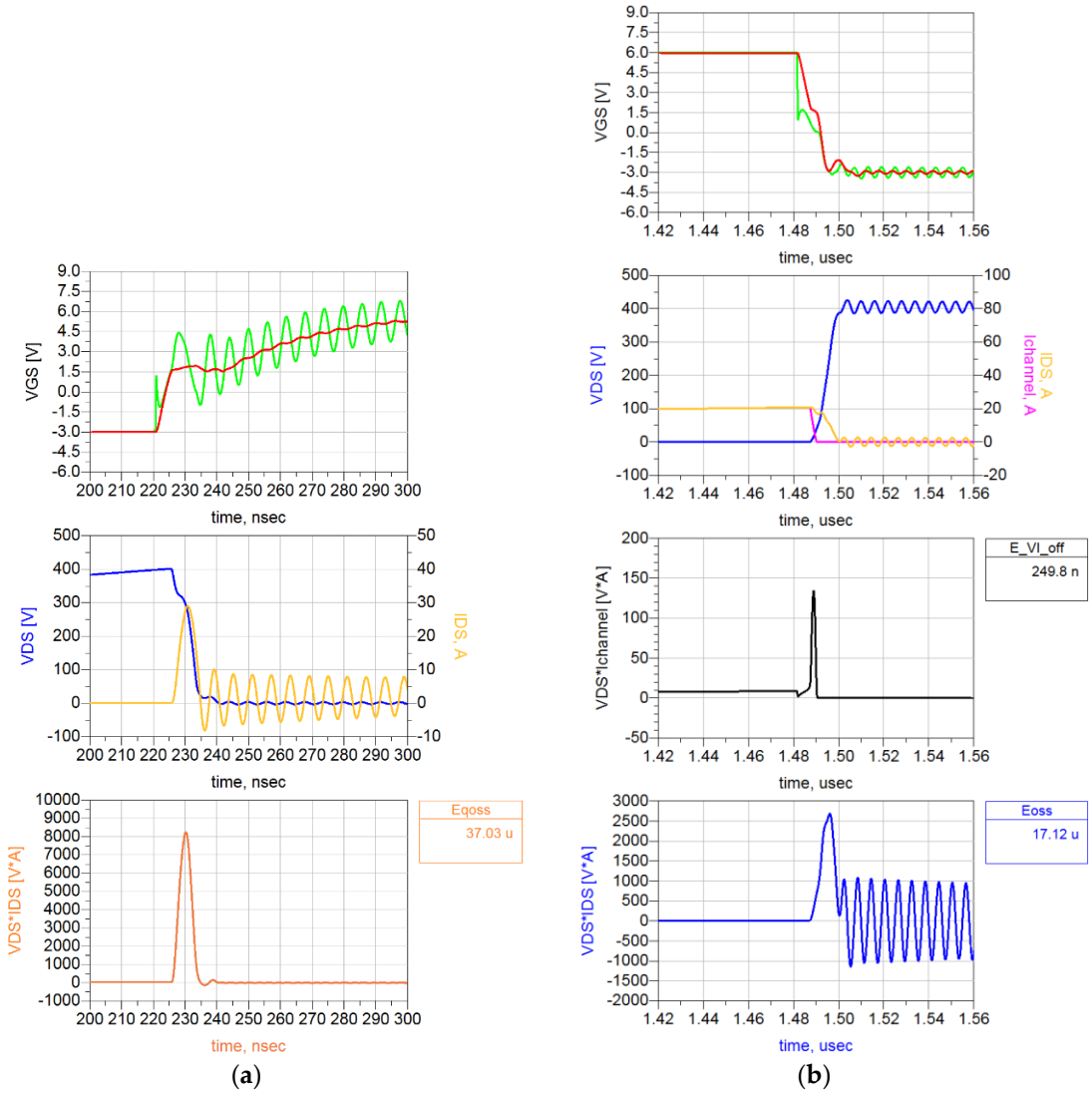


Figure 3.8 DPT of GS-065-060-5-T-A: a) At turn-on of the first pulse: extrinsic V_{GS} (in green) and intrinsic V_{GS} (in red), V_{DS} and I_{DS}, the product of V_{DS} and I_{DS} (the instantaneous dissipated power) and the corresponding calculated E_{qoss}; b) At first turn-off: extrinsic V_{GS} (in green) and intrinsic V_{GS} (in red), V_{DS}, I_{DS} and $I_{channel}$, the instantaneous dissipated power through the channel and the corresponding calculated E_{VI_off}, the instantaneous dissipated power and the corresponding calculated E_{oss}.

E_{qoss} can be conveniently obtained from the turn-on of the first pulse which has $E_{VI\_on} = 0$. The computed value of E_{qoss} from the simulation waveforms in Figure 3.8a is consistent with the previous calculated value (3.7). The E_{oss} energy resulting from the waveforms at the first turn-off of the DPT is shown in Figure 3.8b: also this parameter is in good agreement with the previous calculation (3.8) and the datasheet value in Table 3.1. E_{VI_off} can be derived from the datasheet through equation (3.4) as

$$E_{VI\_off} = E_{off\_intrinsic} = E_{off\_external} - E_{oss} = 17.2\ \mu J - 17\ \mu J = 0.2\ \mu J \qquad (3.9)$$

This value is consistent with 250 nJ that has been calculated from DPT turn-off waveforms in Figure 3.8b.

It is worthy of note that GaN devices exhibit extremely low E_{VI_off} losses, i.e. a negligible power is dissipated through the channel at turn-off. In fact, as can been seen from the waveforms in Figure 3.8b, the 2DEG channel ($I_{channel}$) is switched off when the drain-source voltage is low, since it is at the beginning of its transition and thus an almost ZVS turn-off is achieved. This is the reason why turn-off of GaN devices can be classified as natural soft-switching [24]. This is particularly true when a strong driver is implemented at turn-off by means of low value of gate resistance and even more if a negative gate-source voltage is used, as in our case ($R_{G,off} = 2\ \Omega$, $V_{GS,off} = -3$ V).

It is interesting to highlight that the implementation of the Pspice model in ADS allows the decomposition of the different contributions of I_{DS} current. As depicted in Figure 3.9, applying Kirchhoff's Current Law (KCL), the total I_{DS} at the drain node is composed of three contributions: $I_{channel}$, C_{ds} current and C_{dg} current. By convention, C_{dg} current is the current through the Miller capacitance C_{gd} with positive direction of the current probe from the drain to the gate.

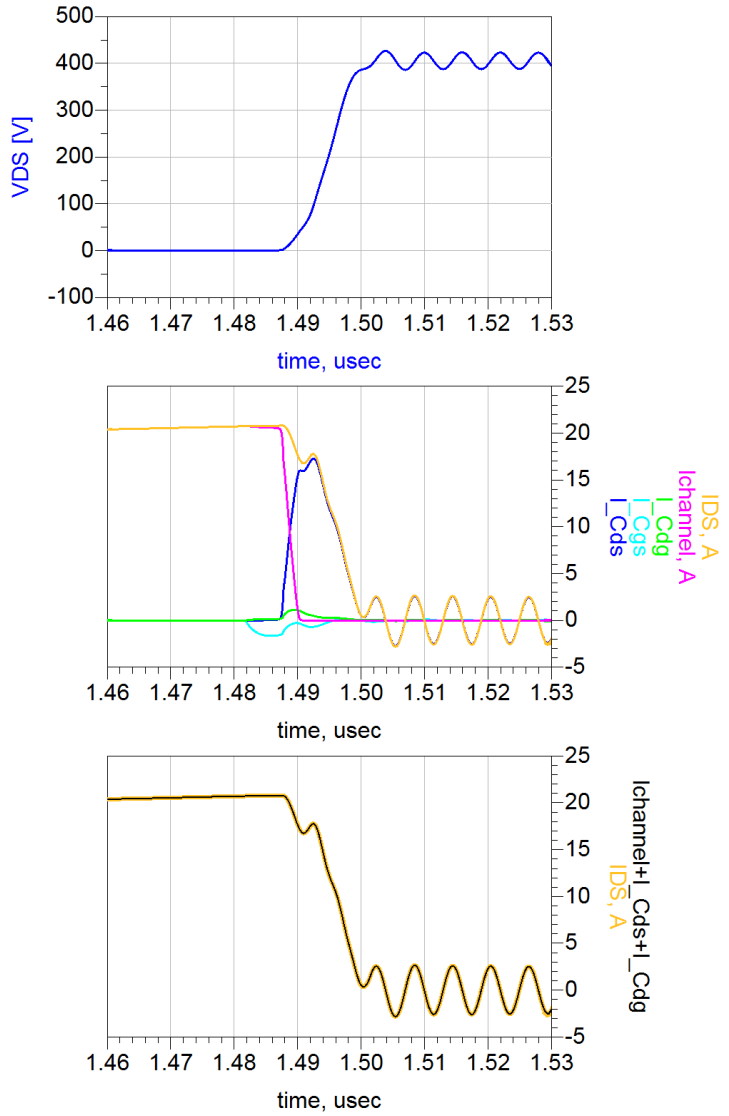


Figure 3.9 DPT of GS-065-060-5-T-A at first turn-off: contributions of the I_{DS} current at the drain node. In the third plot the I_{DS} waveform (in orange) has twice the thickness of the sum of its contributions (in black).

With the proposed ADS simulations that have been performed exploiting the device non-linear dynamic model, it has been verified that the model is capable to precisely reproduce the measured static and dynamic parameters of the transistor, while giving a total insight on the loss mechanism involved. This is essential to pursue loss minimization during the design stage. This simulation tool is used in the next sections for detailed analyses of commutations in a real converter.

3.2 DAB DC-DC converter

In this Section, we deeper discuss turn-on and turn-off transitions of GaN HEMTs in the 6.6 kW Dual Active Bridge DC-DC converter. In particular, the positive consequence of strong turn-off on the Miller voltage will be shown.

Table 3.2 recalls the HV DC-DC converter specifications.

Table 3.2 DC-DC converter specifications

V_{in}	$V_{out,range}$	$V_{out,nominal}$	$I_{out,nominal}$	$P_{out,nominal}$	$P_{out,max}$	f_{sw}
400 V	200-450 V	400 V	16.5 A	6.6 kW	7 kW	300 kHz

DC-DC converter requirements in Table 3.2 can be typically satisfied by means of resonant CLLC or DAB topologies in GaN technology. As anticipated, Dual Active Bridge has been chosen due to the much lower design and control complexity [20,21]. In fact, in DAB circuits, gains are linearly proportional to the loads: the two full-bridges (FBs) typically operate at fixed switching frequency and 50% duty cycle, and, in case of a single phase-shift modulation (SPS), the power flow is controlled by regulating the voltage applied to the series inductor by simply adjusting the time displacement (phase shift) among the gate signals of the two FBs.

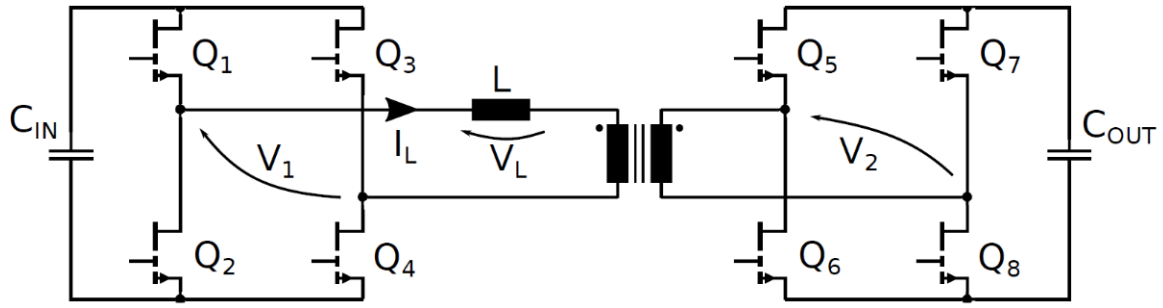


Figure 3.10 DAB DC-DC converter schematic.

With reference to the schematic in Figure 3.10, the relationship between the output power and the phase shift ϕ is equal to [22]:

$$P = \frac{nV_1V_2}{2\pi^2 f_{sw}L}\,\phi\,(\pi - |\phi|) \tag{3.10}$$

where $n = N_2 / N_1$ is the transformer turns ratio and $-\pi/2 < \phi < \pi/2$. The absolute maximum power is obtained for $\phi = \pi / 2$:

$$|P_{max}| = \frac{nV_1V_2}{8f_{sw}L} \tag{3.11}$$

The designed DAB converter is composed of two full bridges of GS-065-060-5-T-A GaN HEMTs driven by Allegro single-channel isolated driver AHV85110, which features Power-Thru Integrated Isolated Bias Supply. The ADS simulations discussed in this Section take into consideration the parasitics of the involved passive components (for convenience reported in Table 3.3). In Section 3.3 also the role of PCB parasitics is investigated by means of electromagnetic simulations, aiming to demonstrate that the PCB layout has been designed and optimized to have no significant detrimental impact on converter performances.

Table 3.3 DAB passive components.

Passive component	PN	Quantity	Parameters
DAB XFMR	Bourns custom design	1	L_{lk} = 6 μH L_{mag} = 301.6 μH $C_{p,s}$ = 27.2 pF C_{ww} = 43.3 pF $R_{DCp,s}$ = 9.4 mΩ Turns ratio = 10:10
Electrolytic capacitor	Kemet ALA7DA391CF500	3x in the DC-link section; 1x in the output section	V_{DC} = 500 V C = 390 μF ESR = 481.2 mΩ (@ 20 °C, 10 kHz) ESL = 20 nH Icrms = 4.12 Arms (@ 85 °C, 10 kHz)
Ceramic capacitor	TDK B58031U5105M062	2x for each GaN leg	V_{DC} = 500 V C = 1 μF ESR = 12 mΩ (@ 0 V_{DC}, 0.5 Vrms, 25 °C, 1 MHz) ESL = 3 nH I_{crms} = 11 Arms (@ 85 °C, 100 kHz)

DAB waveforms (400V/400V, 6.6 kW, 300 kHz, 25 °C, V_{GS} = 6/-3 V, R_G = 10/2 Ω) simulated through ADS are displayed in Figure 3.11. Allegro driver AHV85110 rise/fall times (0-100 %) are quantified in 30 ns. Dead-time is equal to 100 ns. The names of the electrical quantities in the waveforms of Figure 3.11 correspond to the labels in Figure 3.10.

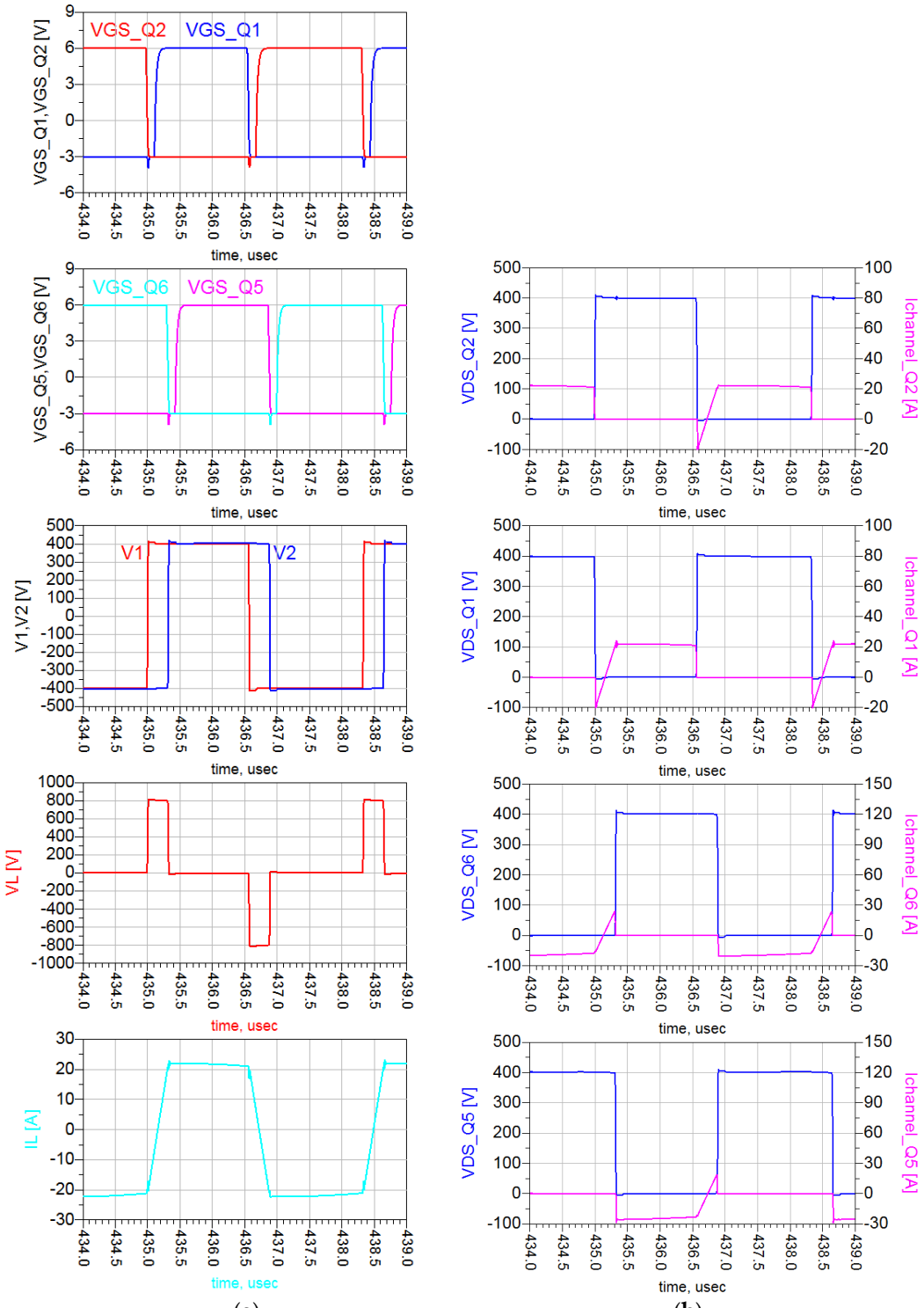


Figure 3.11 DAB waveforms: a) V_{GS} of Q1 and Q2, V_{GS} of Q5 and Q6, primary (V1) and secondary (V2) voltages, series inductor voltage V_L, series inductor current I_L; b) V_{DS} and Ichannel of Q2, V_{DS} and Ichannel of Q1, V_{DS} and Ichannel of Q6, V_{DS} and Ichannel of Q5.

In a SPS modulation, switches on the same diagonal (Q1-Q4, Q2-Q3, Q5-Q8, Q6-Q7 in Figure 3.10) are ON/OFF for half a period and share the same gate signal. Figure 3.11 shows that when Q2-Q3 are turned off, the negative inductive current I_L charges the C_{oss} of Q2-Q3 to 400V+V_f and discharges the C_{oss} of Q1-Q4 to -V_f,

where $V_f = V_{GS(th)} + |V_{GS,off}|$ is the diode-equivalent forward voltage of GaN in reverse conduction, in our case $-V_f \approx -4.6$ V. Then V1 commutes to $400V+2V_f$, VL to $800V+2V_f$ and series inductor is being charged. Similarly, when Q6-Q7 are turned off, V2 commutes to $400V+2V_f$, VL to $-2V_f$ (since in the meantime Q1-Q4 have stopped reverse conduction) and series inductor is slowly discharged. In the second half of the period, Q1-Q4 are turned off (V1 toggles to $-400V-2V_f$ and VL to $-800V-2V_f$) followed by Q5-Q8 (V2 toggles to $-400V-2V_f$ and VL to $+2V_f$).

Let us now look in detail the DAB ZVS turn-on, for instance for the pair Q2-Q3. ZVS boundaries depends on the total energy stored in the series inductor and can be calculated as reported in [20,22,51,52]. At nominal full-power, as in our case, ZVS condition is assured by design (selection of a suitable series inductance, with respect to V_{DC} voltage, device C_{oss}, switching frequency and dead time). Figure 3.12 shows that when Q1-Q4 are switched off, during dead-time the positive inductive current I_L charges the C_{oss} of Q1-Q4 to $400V+V_f$ and discharges the C_{oss} of Q2-Q3 to $-V_f$. Hence, Q2-Q3 are in reverse conduction in third quadrant, acting as equivalent free-wheeling diodes (the gate is OFF). Then, when the gate-source voltage of Q2-Q3 goes above the threshold (which is equal to 1.6 V in the Pspice model) they are forward-biased with an almost null drain-source voltage, which further decrease, in absolute term, from $-V_f$ to $-V_{DS,ON}$. The negative sign of V_{DS} is due to the fact that Q2-Q3 have opposite polarity when I_L is positive (see Figure 3.10). As is clear from Figure 3.12, the switching transient of the drain-source voltage (400 V swing) exhibits very short time duration (17 ns): the high commutation speed of GaN devices enables to implement very short dead-time (typically between 50 and 100 ns) minimizing third quadrant losses.

It is worthy of note the absence of a Miller plateau. For turn-on the reason is two-fold: typically GaN devices do not exhibit a Miller plateau when relatively low gate resistance are used ($R_{g,on} = 10\ \Omega$ in our case) because of the small parasitic capacitances (*Cgs* and *Cgd*) to be charged [23] and, secondly, in a ZVS turn-on when the gate goes ON there is no drain-source voltage to commute since C_{oss} has already been discharged during dead-time.

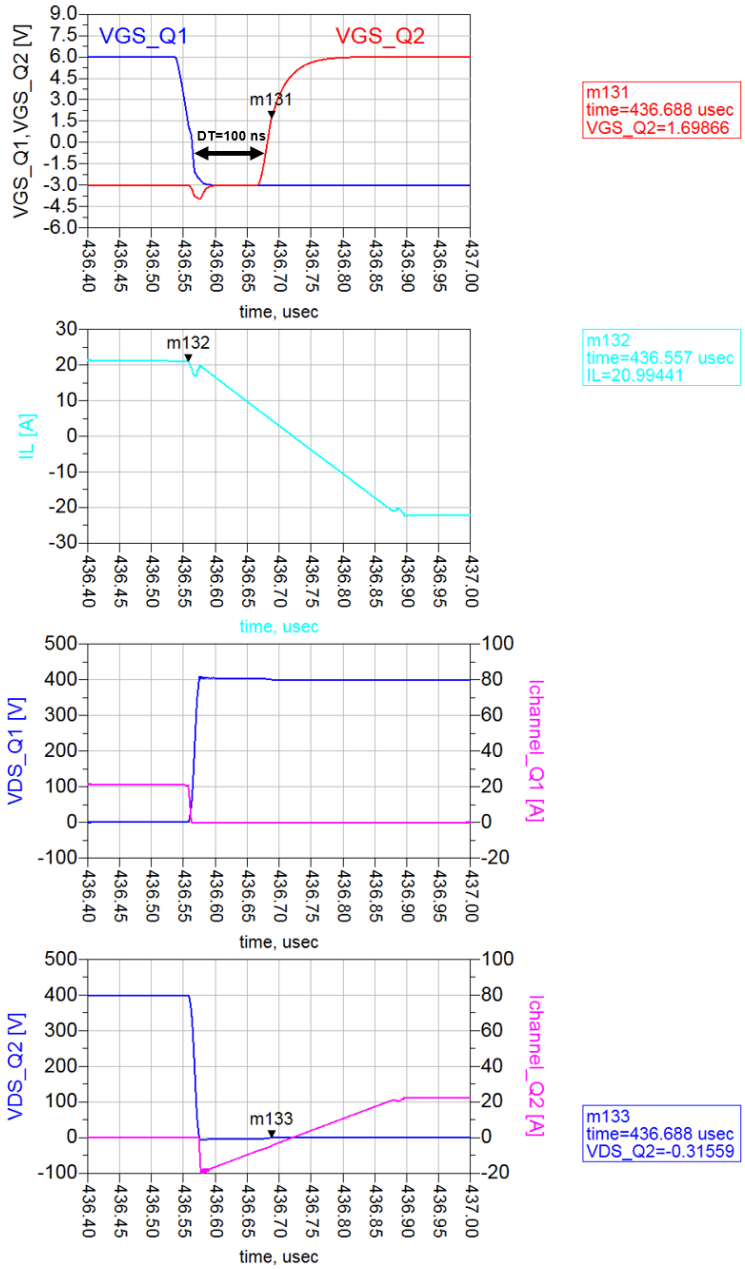


Figure 3.12 Detail of DAB Q2 ZVS turn-on, from top to bottom: V_{GS} of Q1 and Q2, series inductor current I_L, V_{DS} and Ichannel of Q1, V_{DS} and Ichannel of Q2. Time grid in the plot is 50 ns.

Figure 3.13 depicts a schematic view of Q2-Q3 ZVS turn-on mechanism.

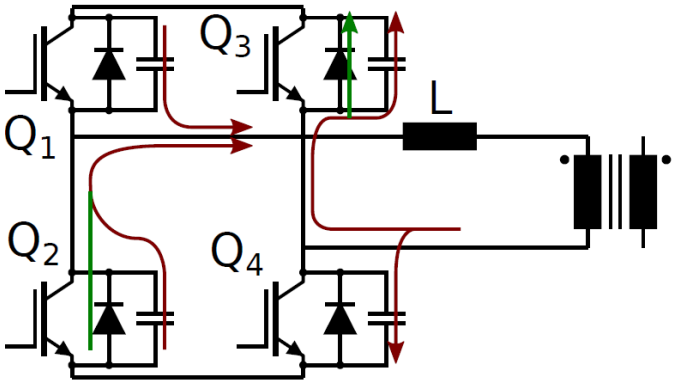


Figure 3.13 DAB schematic view of Q2-Q3 ZVS turn-on mechanism. Brown arrows indicate capacitive displacement currents, green arrows indicate reverse conductive currents in third quadrant operation.

A deep insight into the strong ($V_{GS,off}$ = -3 V, $R_{G,off}$ = 2 Ω) and very low-loss turn-off of a GaN HEMT is provided hereafter. In particular, Q1 of the DAB converter is under exam, but similar conclusions can be reached through a DPT simulation as well. Looking at Figure 3.14, the first part of turn-off is characterized by C_{gs} discharge (C_{gs} current is in green line in the second plot) with V_{GS} of Q1 decreasing from 6 V to 1.26 V. At this point, also C_{gd} (in cyan color) starts to be deeply discharged and voltage/current commutations begin. Hence, strong driver has enough current to discharge C_{gd} and C_{gs} at the same time during this second phase. This implies the absence of a Miller plateau also at turn-off for GaN HEMTs [23]. Channel current (in magenta in the third plot) rapidly goes to 0 A (in 5 ns) while V_{DS} is at the beginning of its transition, reaching only 50 V on a total 400 V swing. Therefore an almost ZVS turn-off is achieved and the power dissipation through the channel can be almost neglected.

C_{gd} deep discharge begins at V_{GS} = 1.26 V causing device voltage/current transitions, meaning that a strong driver and low values of C_{gd} can pull the Miller voltage below the threshold [2]. In fact, this latter is equal to 1.6 V. This denotes that the voltage transient is not controlled by the gate driver but rather by the C_{oss} and the load current [48,53]. 2DEG channel is pinched-off during voltage commutation [2], which starts when V_{GD} = 0 V.

When the channel current of Q1 is equal to 0 A, its drain-source current I_{DS} at the drain node becomes equal to the C_{oss} current (= I_C_{dg}_Q1+I_C_{ds}_Q1, in red in the third plot). At the same time, applying Kirchhoff's Current Law (KCL) at the source node of Q1, the series inductor current I_L (in brown color in the second plot) becomes equal to I_C_{gs}_Q1+I_C_{ds}_Q1+I_C_{gd}_Q2-I_C_{ds}_Q2-Igate_Q1 (in purple line in the second plot). Finally, this latter starts to decrease when the transient of V_{DS}_Q1 is over and Q2 begins reverse conduction in third quadrant (Q2 channel current is in black line in the second plot) equalling the inductor current in the end.

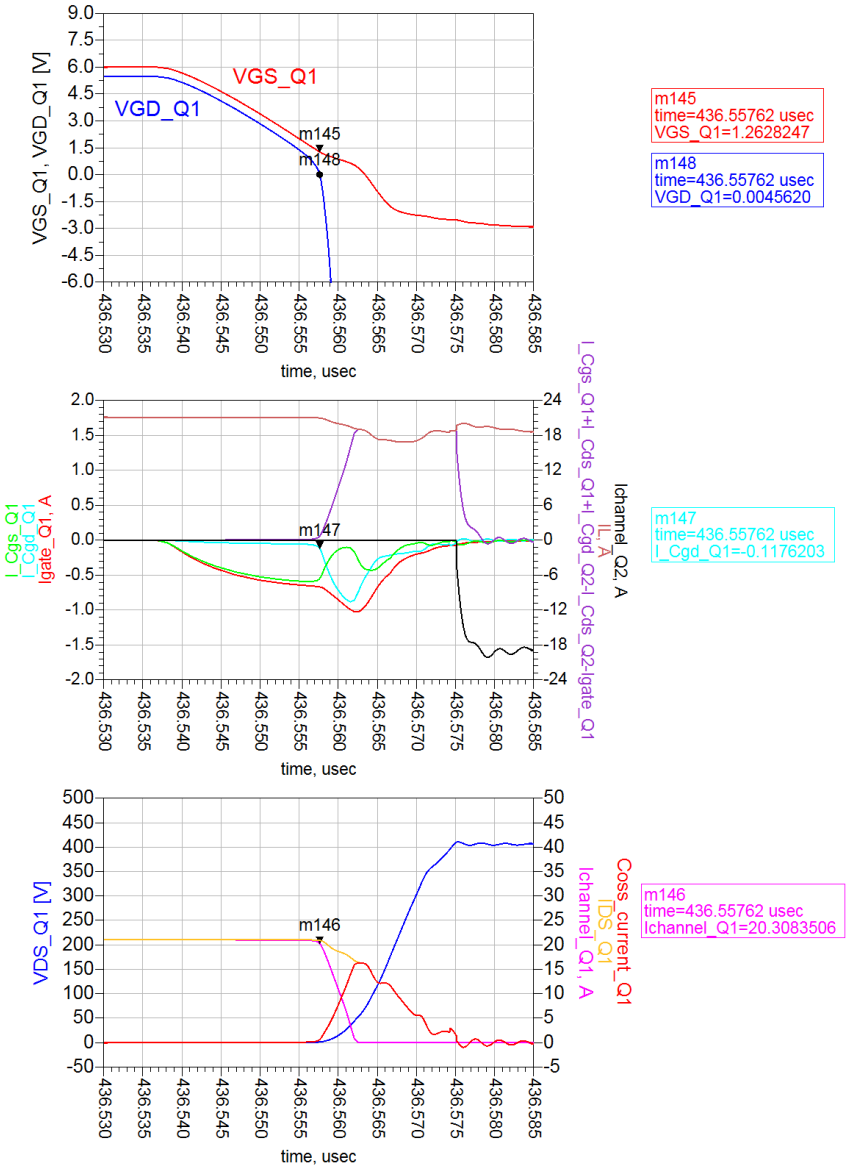
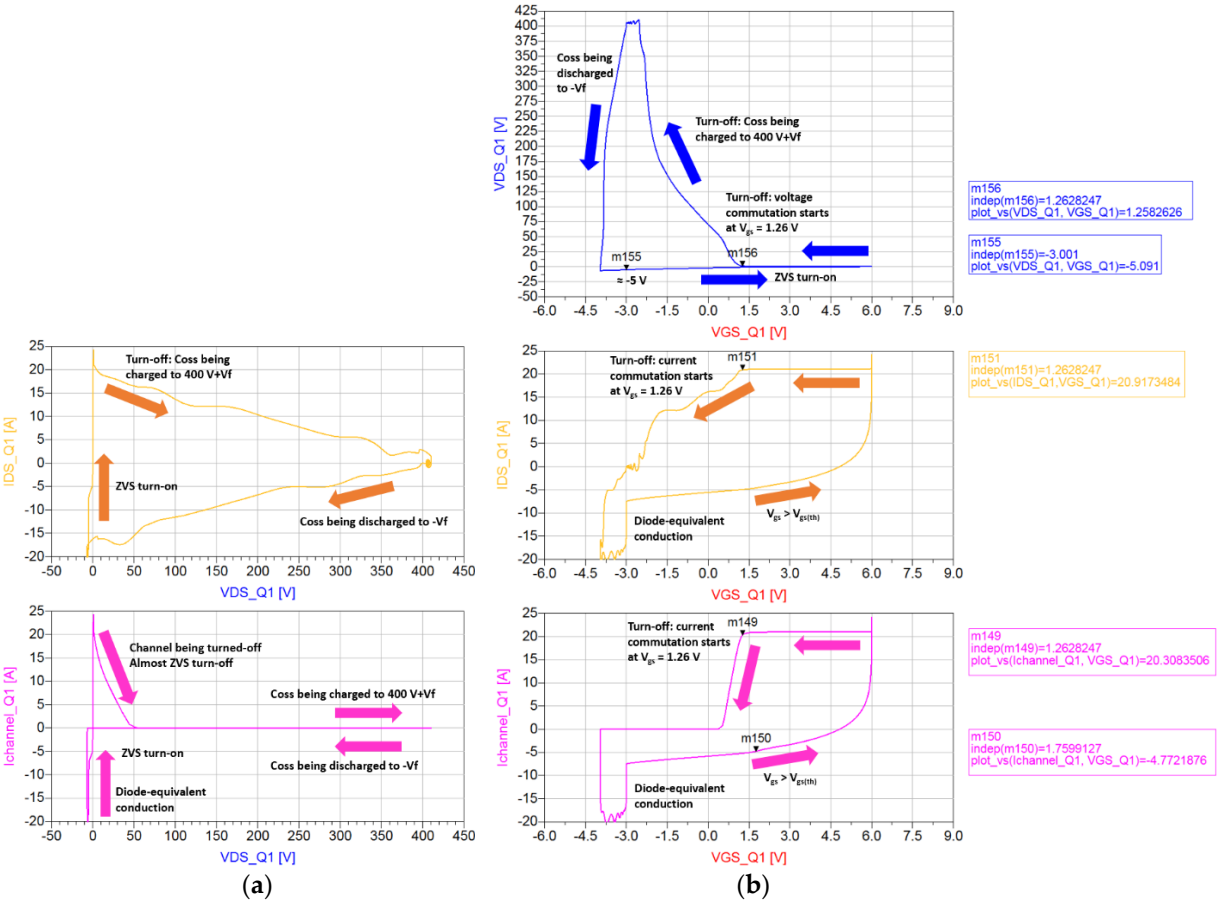


Figure 3.14 Q1 strong turn-off, from top to bottom: V_{GS} and V_{GD} of Q1; C_{gs}, C_{gd} and gate current of Q1 (on the left), I_C_{gs}_Q1+I_C_{ds}_Q1+I_C_{gd}_Q2-I_C_{ds}_Q2-Igate_Q1, I_L, and $I_{channel}$ of Q2 (on the right); V_{DS} of Q1 (on the left), $I_{channel}$, I_{DS} and C_{oss} current of Q1 (on the right). Major time grid in the plots is 5 ns, minor time grid is 1 ns.

For a full and intuitive picture of the device commutation behavior within an entire switching period, it is useful to plot I_{DS} and $I_{channel}$ currents versus V_{DS} and V_{GS} voltages. Figure 3.15 reports these waveforms for Q1. Also, V_{DS} versus V_{GS} is displayed. Plots in Figure 3.15a are clockwise, while plots in Figure 3.15b are counter clockwise. ZVS turn-on and almost ZVS turn-off are highlighted. Also, the beginning of voltage and current transitions in correspondence of $V_{GS} = 1.26\ V < V_{GS(th)} = 1.6\ V$ at turn-off is clearly shown. V_{DS} overvoltage and V_{GS} dip at commutations are visible. Moreover, the full voltage across the device in third-quadrant operation ($-V_{GS(th)} - |V_{GS,off}| - R_{ds,rev} \cdot I_{SD} \approx -5\ V$) [17] is marked in the first plot of Figure 3.15b.



(**a**) (**b**)

Figure 3.15 Q1 waveforms over an entire switching period: a) I_{DS} vs V_{DS} and $I_{channel}$ vs V_{DS}; b) V_{DS} vs V_{GS}, I_{DS} vs V_{GS} and $I_{channel}$ vs V_{GS}.

Figure 3.16 displays the turn-off trajectories of channel current (in magenta) and drain-source current (in orange) with respect to the drain-source voltage, mapped on the output characteristic of the device (@Tj = 25 °C, in black). X-axis is in log scale. This plot clearly shows the very low-loss nature of these turn-off commutations: in particular, the channel current trajectory is almost the one of an ideal switch, indicating almost null power dissipation of this event in the channel.

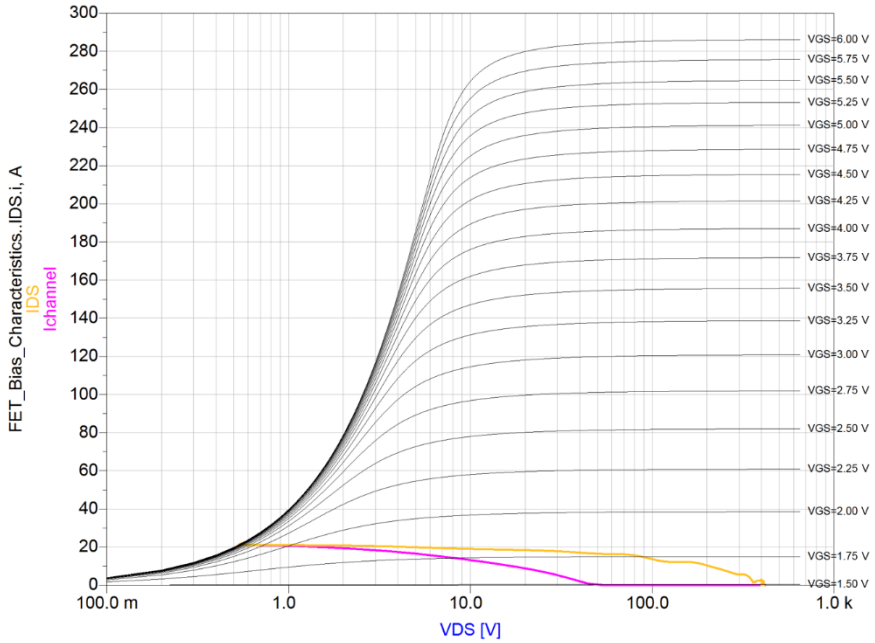


Figure 3.16 Turn-off trajectories of $I_{channel}$ and I_{DS} mapped on the output characteristic.

The detailed description of the device voltages and currents during commutations can be suitably exploited for the calculation of power dissipation in the DAB converter and the identification of the different contributions. The following operating conditions are assumed: V_{in} = 400 V, V_{out} = 400 V, P_{out} = 6.6 kW, f_{sw} = 300 kHz, V_{GS} = 6/-3 V, R_G = 10/2 Ω, dead time = 100 ns, Tj = 120 °C. This latter can be considered the maximum acceptable junction temperature of GaN HEMTs at full-power working regime to have a sufficient safety margin with respect to the component maximum rating of Tj = 150 °C.

Figure 3.17 shows the waveforms for the calculation of power dissipation for Q1. Three phases can be clearly detected. First contribution is due to the diode-equivalent conduction in third quadrant, which starts when drain-source voltage of Q1 reaches $-V_f$ following Q2 turn-off. Then Q1 is set ON when $V_{gs} \geq V_{GS(th)}$. And finally, after a half switching period, Q1 channel is switched off. Leakage current losses in OFF state are negligible.

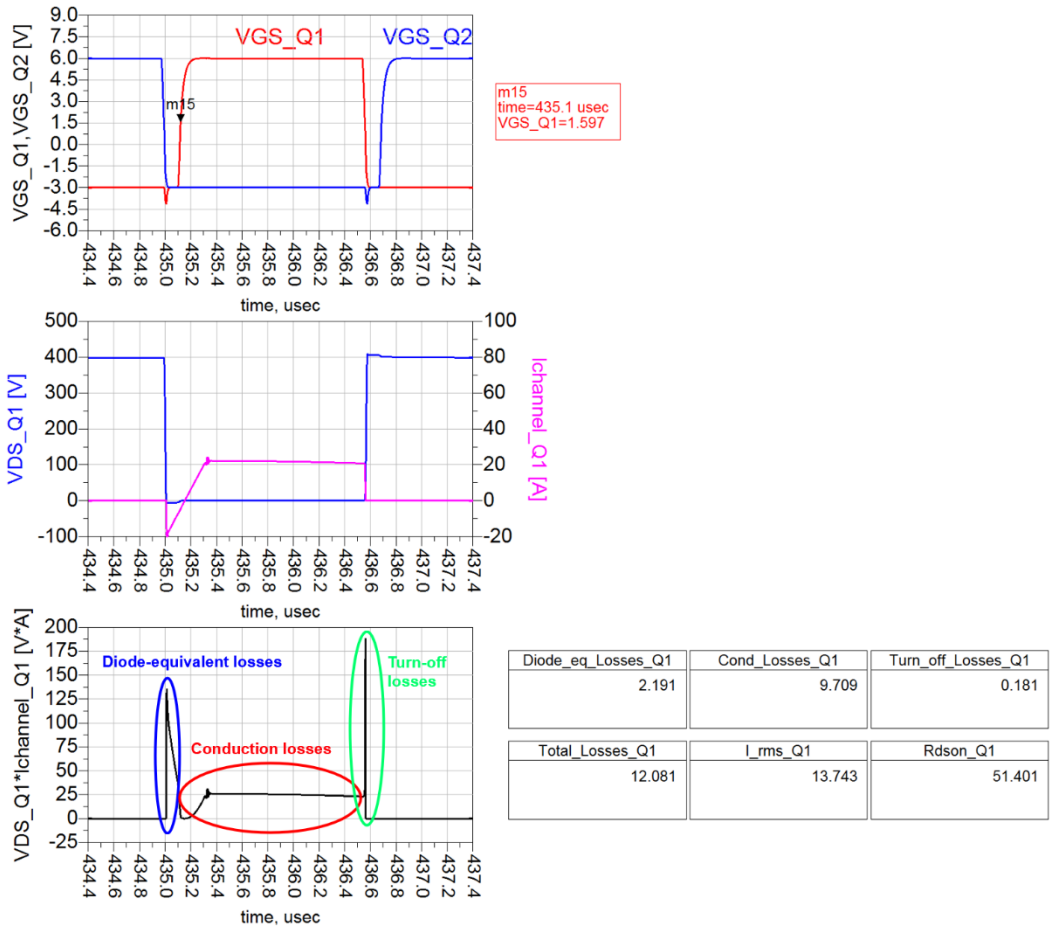


Figure 3.17 Power dissipation of Q1 over an entire switching period, from top to bottom: V_{GS} of Q1 and Q2, V_{DS} and Ichannel of Q1, the instantaneous dissipated power through the channel and calculation of losses (in W), rms current (in Arms) and equivalent $R_{DS,on}$ (in mΩ).

Power losses shown in the table of Figure 3.17 have been computed through integration of the instantaneous dissipated power waveform (third plot of Figure 3.17). It is also useful to calculate the device RMS current (from its integral definition) and $R_{DS,on}$, which has been computed as

$$R_{DS,on} = \frac{Conduction\ losses}{I_{rms}^2} \tag{3.12}$$

The resulting $R_{DS,on}$ for the GS-065-060-5-T-A device in these operating conditions (i.e. Tj = 120 °C, and the described driving conditions) is 51.40 mΩ, whereas its nominal $R_{DS,on}$ at 25 °C is 25 mΩ. As indicated in Figure 3.17, the overall device losses are equal to 12.081 W: the pie chart in Figure 3.18 shows the weights of the different contributions to Q1 losses.

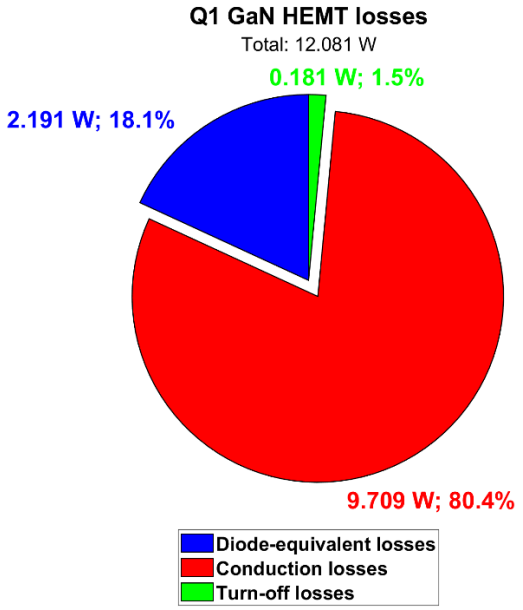


Figure 3.18 Contributions of Q1 power losses. Turn-on losses are null since device experiences a ZVS turn-on at nominal power converter regime.

It is evident that conduction losses are dominant. These losses can be maintained at their minimum possible level by minimizing the $R_{DS,on}$: this is achieved by maximizing $V_{GS,on}$ and optimizing the thermal management of the device by using a proper TIM (thermal interface material) and the best possible heatsink or liquid cooling system. Diode-equivalent losses (i.e. third quadrant conduction losses) can be reduced by implementing -3 V < $V_{gs,off}$ ≤ 0 V (with a compromise between dead-time and turn-off losses [2,52]) or decreasing the duration of dead time. This latter is pursued by selecting a strong driver (high gate commutating current available) and minimizing the gate and power loop parasitics so that minimum commutation time is obtained. It is then very interesting to highlight that under the conditions described for this design, commutation losses are practically negligeable. In the end, when exploiting GaN devices at their best potential and even more if soft switching conditions are attained, the upper bound on the switching frequency of the power converter is not determined by semiconductor devices but rather by magnetics design in terms of cost-effective solution, since the trade-off between power density and losses can be very critical at high switching frequency.

Total losses for Q1-Q8 are reported in Table 3.4.

Table 3.4 DAB GaN HEMTs losses (@ V_{in} = 400 V, V_{out} = 400 V, P_{out} = 6.6 kW, f_{sw} = 300 kHz, V_{GS} = 6/-3 V, R_G = 10/2 Ω, dead time = 100 ns, Tj = 120 °C).

Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Total
12.08 W	13.77 W	13.82 W	12.13 W	17.11 W	12.83 W	12.89 W	17.16 W	111.79 W

Other main losses are related to the DAB transformer. Primary/secondary DC resistances are equal to 9.4 mΩ, leading to about (3.85 + 3.85) W of copper losses. Core losses (PQ60-42Z Ferrite - DMR95 - with gap of 0.1 mm) can be estimated in 10 W.

Taking into consideration only the OBC DC-DC stage under exam, DAB contributions to the rms current of electrolytic capacitors are quantified in 3.785 Arms for the DC-link section and 2.021 Arms for the output section. The ESR of electrolytic capacitors decreases with temperature: for ALA7DA391CF500 can be estimated in 250 mΩ at 70 °C. Then, losses of electrolytic capacitors can be calculated as:

$$P_{DC-link\ cap\ bank} = \frac{ESR}{3} \cdot I_{C,DC-LINK}^2 = \frac{250\ m\Omega}{3} \cdot 3.785^2 Arms^2 = 1.19\ W \tag{3.13}$$

$$P_{output\ cap} = ESR \cdot I_{C,out}^2 = 250\ m\Omega \cdot 2.021^2 Arms^2 = 1.02\ W \tag{3.14}$$

Taking all these loss contributions into account, total dissipated power is quantified in 131.70 W and DAB efficiency turns out to be 98.04 %. A pie chart of DAB converter losses is shown in Figure 3.19.

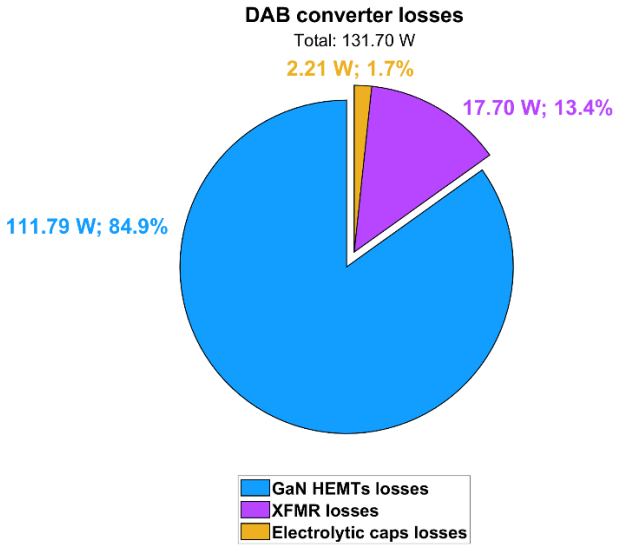


Figure 3.19 Contributions of DAB converter losses.

All the DAB converter simulations hitherto reported in Section 3.2 exploit the GaN HEMT Pspice level 1 model, i.e. without considering the device stray inductances: beforehand, it has been verified that under the described driving conditions, these parasitics have no significant impact on converter performances or device commutations (as depicted in Figure 3.20), demonstrating that GS-065-060-5-T-A

embedded package is highly optimized for fast switching behaviour in a real converter. Nonetheless, ADS computational time is five times larger when the Pspice level 3 model is used.

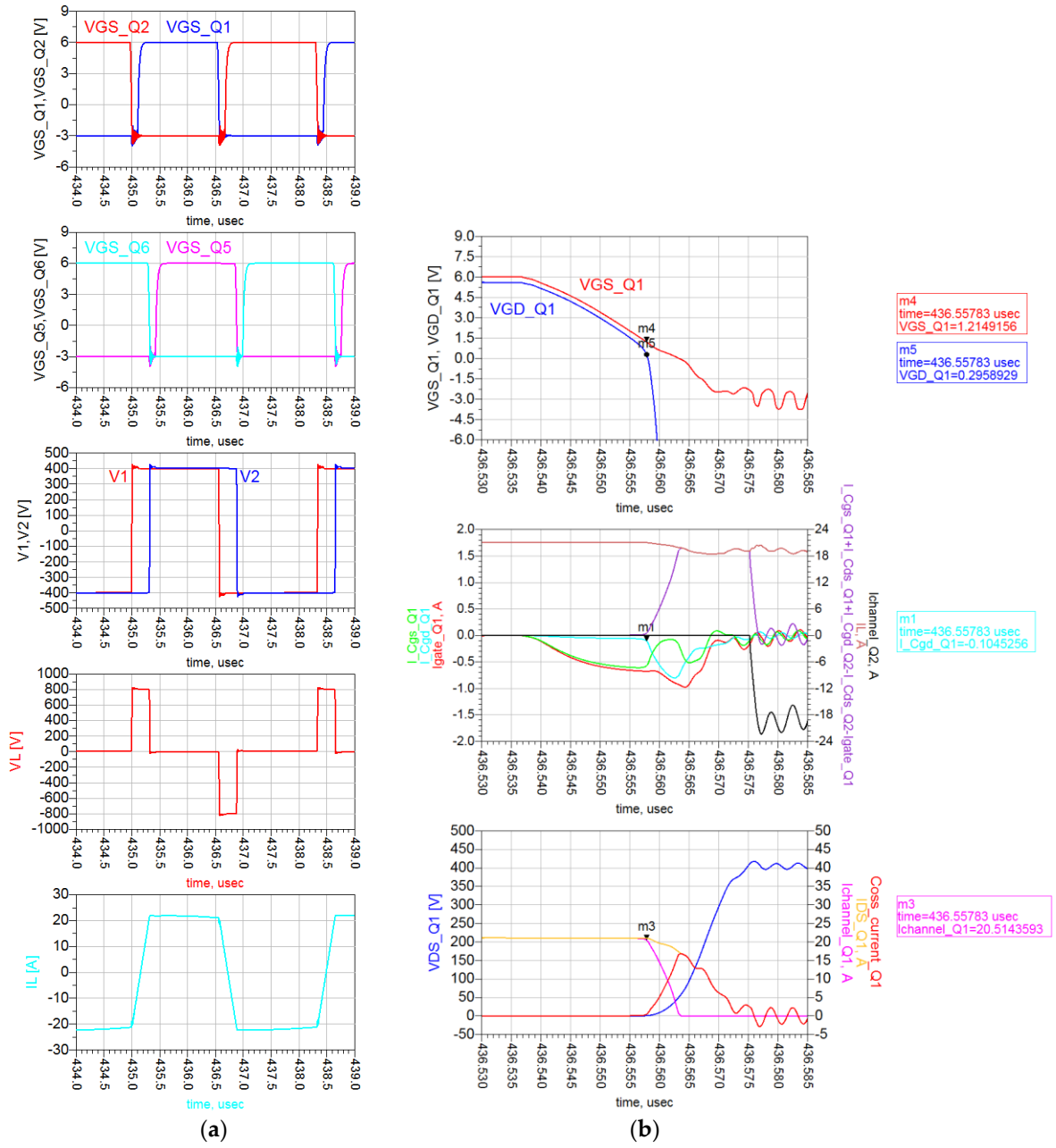


Figure 3.20 Simulation results using the Pspice level 3 model: a) DAB waveforms; b) Q1 almost ZVS turn-off.

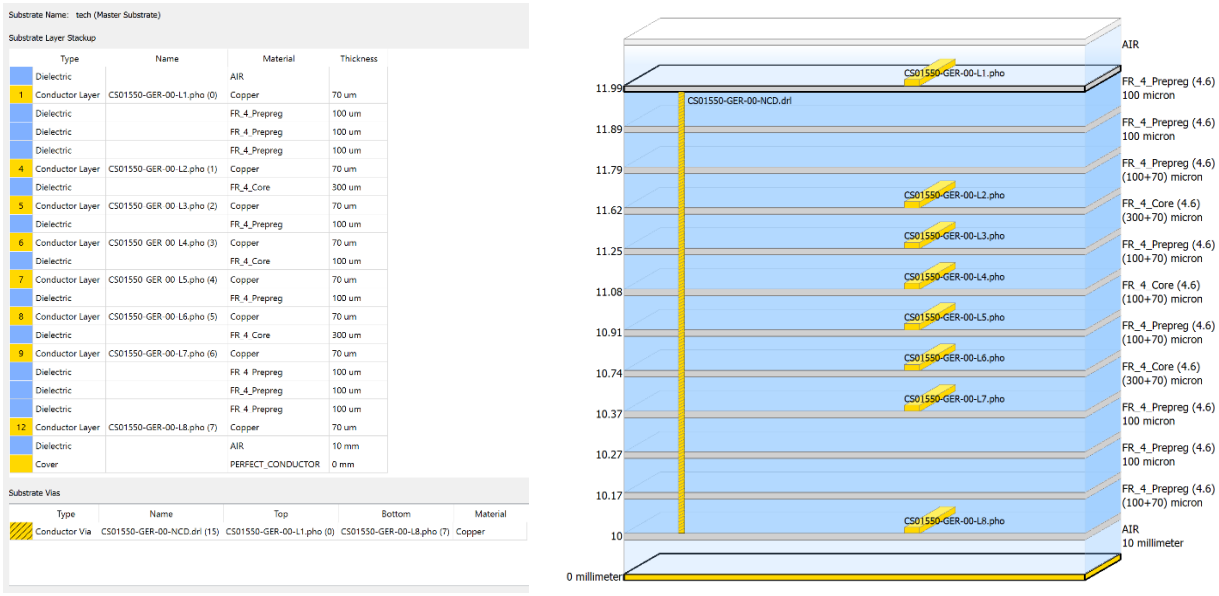
The described performances – achieved by means of very low-loss commutations, enabling to switch with high efficiency at high switching frequency and reduce the converter volumetric dimensions – can be obtained in the actual implementation of the converter only through of a detailed optimization of the PCB layout. A tool and a design procedure for the accurate assessment of layout parasitics and their influence on converter performances are then needed. This is the topic discussed in Section 3.3.

3.3. EM simulation of the DAB PCB layout

Several electromagnetic simulations of the PCB layout of the Dual Active Bridge converter have been performed aiming to optimize the PCB design in a step-by-step process avoiding vicissitudes and rework following the board production. In fact, as previously seen, the fast switching behaviour of GaN devices causes very high slew rates of voltage and current during commutations. Therefore, it is fundamental to precisely evaluate, minimize and compensate any parasitics of the circuit in order to fully exploit GaN potential and avoid issues such as worse reliability, lower efficiency and EMI generation. One of the major concern is related to driver and power loops, i.e. gate-source and drain-source loops of the device. GS-065-060-5-T-A embedded package ensures extremely low stray inductances with respect to the traditional wire-bonded QFNL (Quad Flat No-Lead) or TO (Transistor Outline) packages, at the expense of higher cost. Furthermore, an optimal PCB layout (e.g. exploiting flux cancellation technique) along with an accurate selection of passive components and mechanical connectors – plays a crucial role.

In order to investigate these parasitics loops, the electromagnetic simulator called Momentum Microwave [54] has been used in Advanced Design System. This simulator is based on a numerical discretization technique named Method of Moments (MoM), which is employed to solve Maxwell's equations for planar structures embedded in a multilayered dielectric substrate. By means of full-wave Green functions, the substrate is fully characterized without introducing any simplification to the Maxwell's equations. The result is a multi-port S-parameters matrix which represents the complex and frequency-dependent L and C parasitics of the board.

In particular, the final EM simulation of the optimized PCB is reported and discussed hereafter. The OBC layout substrate (8-layers) has been defined in ADS as shown in Figure 3.21. Total layers thickness is equal to 2060 μm.



(**a**) (**b**)

Figure 3.21 OBC layout model: a) Substrate layer stackup; b) Substrate illustration.

EM simulator settings are reported in Table 3.5.

Table 3.5 EM simulator settings.

Simulator engine	Frequency plan	f_{sw}	Mesh density	Thick conductor model	Via conductor model
Momentum Microwave	SMPS	300 kHz	20 cpw	Sheet	Lumped

Figure 3.22 shows the On Board Charger PCB layout with DAB bridges and magnetics positioning highlighted, while Figure 3.23 displays the ports that have been placed for gate-source and drain-source PCB loops in order to execute the EM simulation, in particular with reference to the primary GaN bridge. Top-side cooled GaN HEMTs are placed on the bottom layer of the board, while drivers and capacitors are placed on the top layer. The layout has been designed to exploit flux cancellation technique to minimize the parasitic inductance. The board of the OBC prototype is illustrated in Figure 3.24.

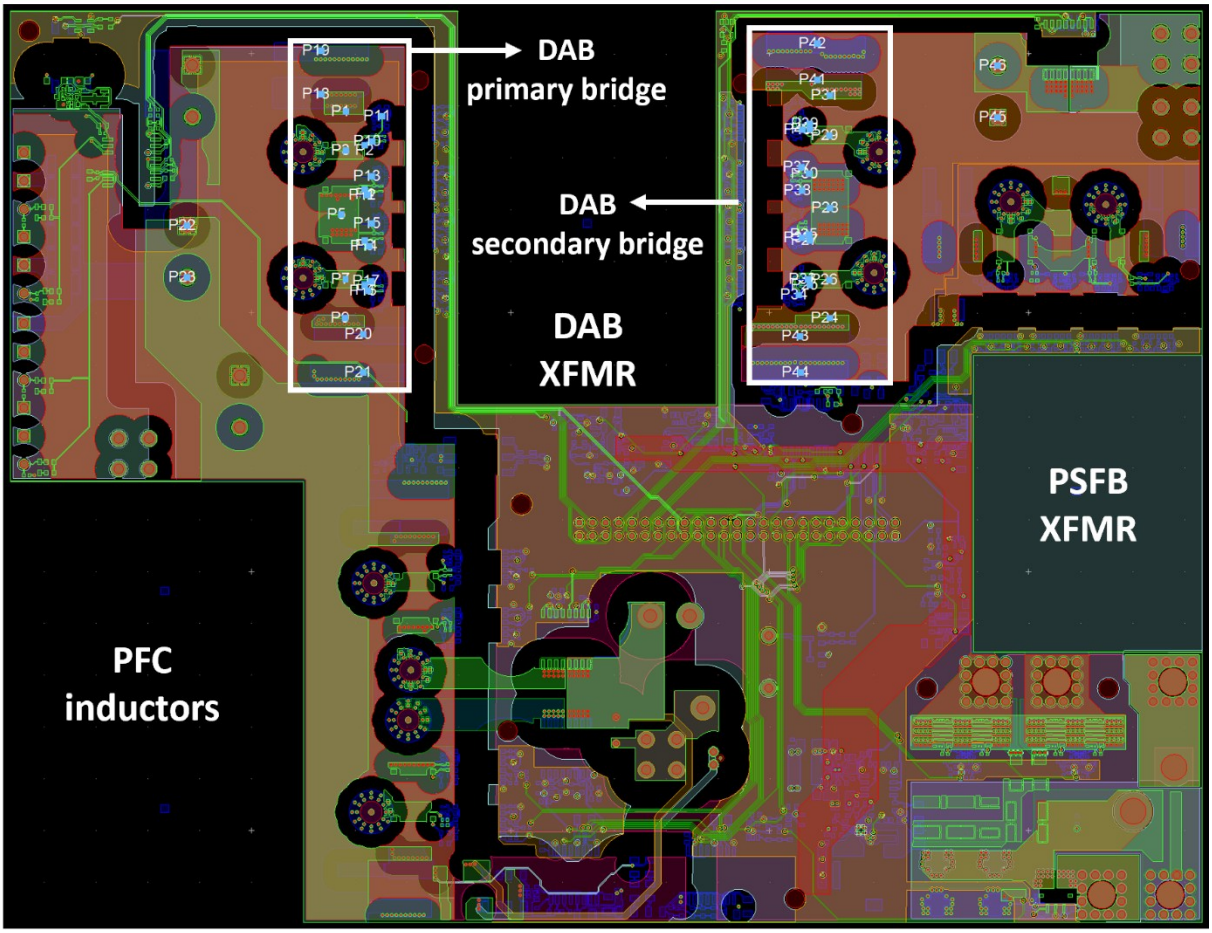
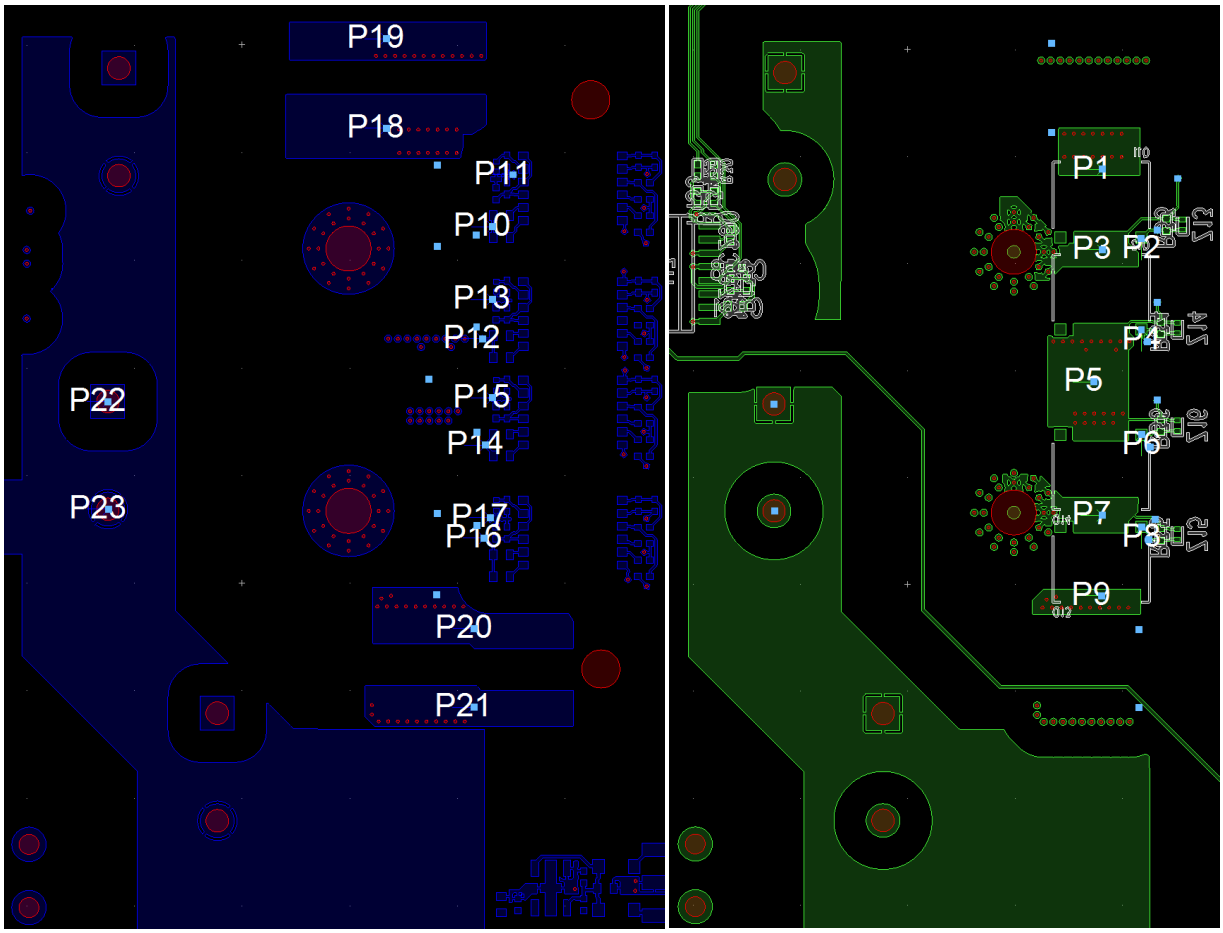
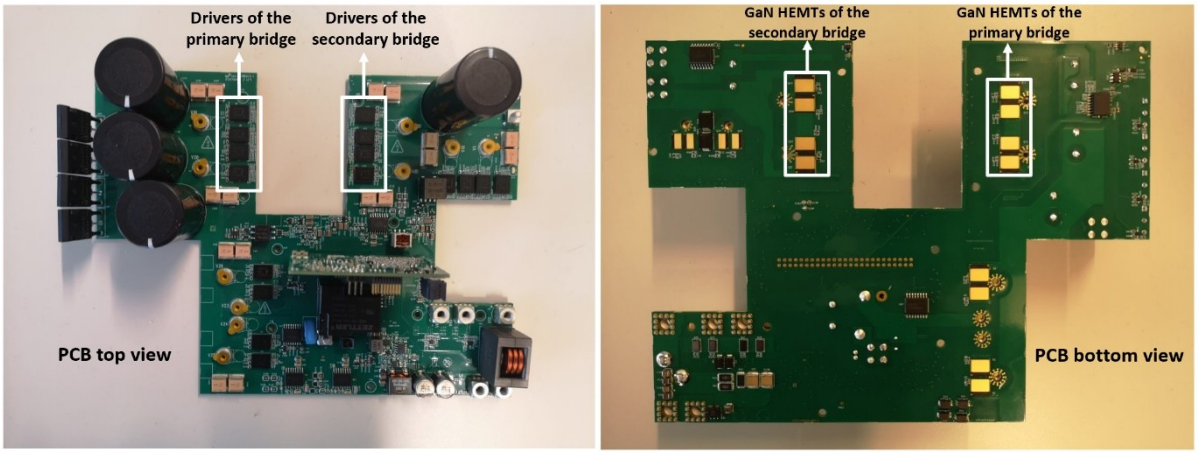


Figure 3.22 Designed OBC layout.



(a) (b)

Figure 3.23 Port placement (PXX) in the primary GaN bridge: a) For drivers, ceramic and electrolytic capacitors on top layer; b) For GaN HEMTs on bottom layer.



(a) (b)

Figure 3.24 OBC prototype: a) Top view; b) Bottom view. EMI filter card and magnetics are not shown.

The ADS schematic used for post-layout simulation, i.e. taking into consideration the S-parameters matrix which represents the result of Momentum Microwave EM simulation, is reported in Figure 3.25. As a result, in this simulation the board connections are not assumed as ideal anymore, but considered on the basis of the

involved R, L and C parasitics whose values can also be extracted from the S-parameters matrix [55].

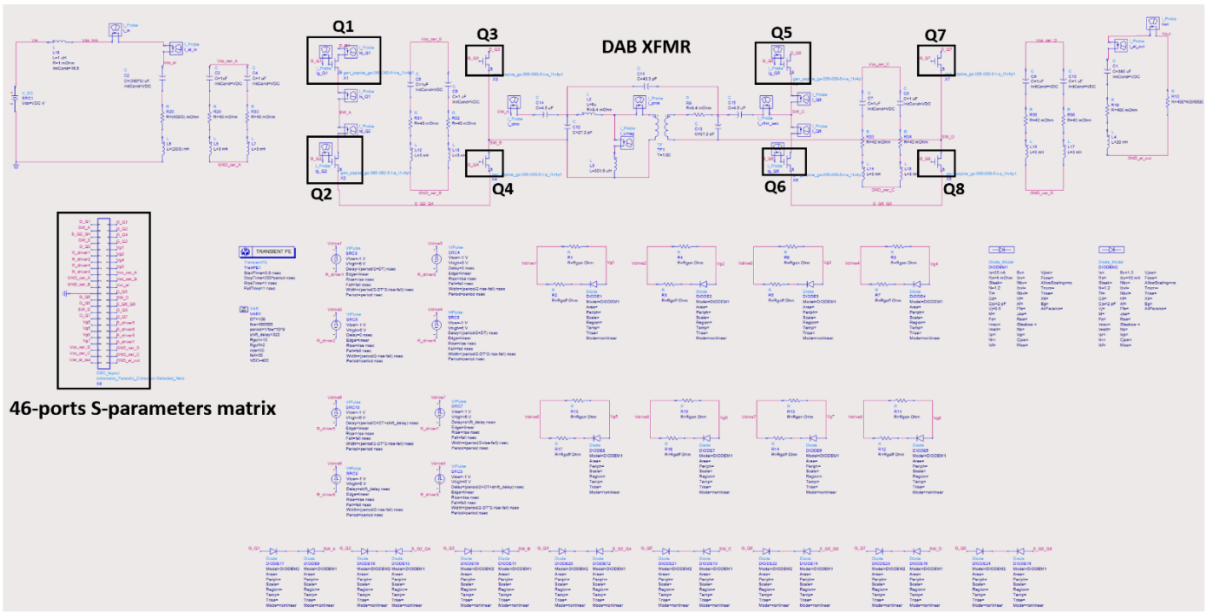


Figure 3.25 ADS schematic for post-layout simulation.

Figure 3.26 provides the detail of the S-parameter matrix element.

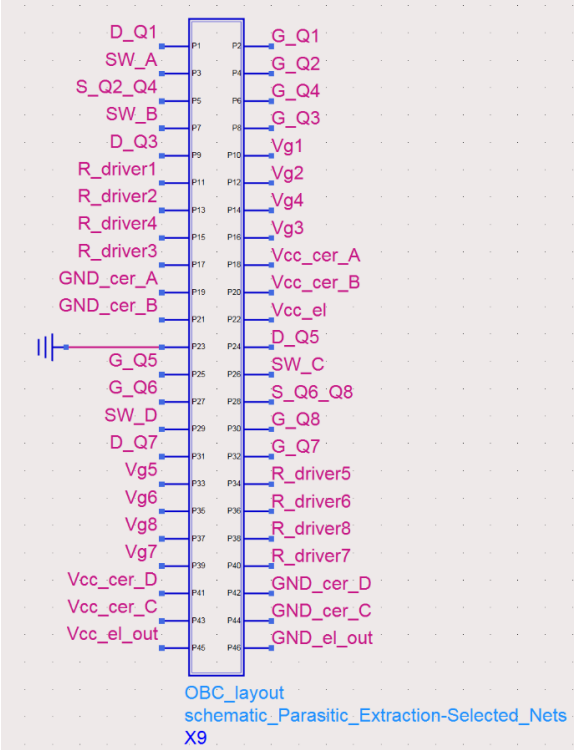


Figure 3.26 Detail of the 46-ports S-parameters matrix.

The parasitics of gate-source and drain-source loops for the first GaN leg Q1-Q2 are reported in Table 3.6.

Table 3.6 Parasitics values of gate-source and drain-source loops for the first GaN leg Q1-Q2.

Pins	Ports	L	R	C
D_Q1-Vcc_cer_A	P1-P18	0.6 nH	0.5 mΩ	
Vg1-G_Q1	P10-P2	2 nH	2 mΩ	
Vcc_cer_A-Vcc_el	P18-P22	12 nH	0.5 mΩ	
R_driver1-SW_A	P11-P3	10 nH	47 mΩ	
Vg2-G_Q2	P12-P4	1.8 nH	1.8 mΩ	
S_Q2_Q4-GND_cer_A	P5-P19	14 nH	0.6 mΩ	
GND_cer_A-GND_el	P19-P23	10.5 nH	1.7 mΩ	
R_driver2-S_Q2_Q4	P13-P5	0.3 nH	0.2 mΩ	
D_Q1-SW_A	P1-P3			0.39 pF
G_Q1-SW_A	P2-P3			0.38 pF
G_Q1-D_Q1	P2-P1			0.40 pF
SW_A-S_Q2_Q4	P3-P5			3.70 pF
G_Q2-S_Q2_Q4	P4-P5			0.60 pF
G_Q2-SW_A	P4-P3			0.50 pF

Figures 3.27-3.30 display the results of the post-layout simulation of the DAB converter. The following operating conditions are assumed: V_{in} = 400 V, V_{out} = 400 V, P_{out} = 6.6 kW, f_{sw} = 300 kHz, V_{GS} = 6/-1 V, R_G = 10/2 Ω, dead time = 100 ns, Tj = 25 °C (except for Figure 3.30 where Tj = 120 °C). As depicted in Figures 3.27 and 3.28, the parasitics of the designed PCB layout have no significant detrimental impact in terms of over/under voltages, ringing or oscillations related to the gate-source and drain-source voltages of the GaN HEMTs.

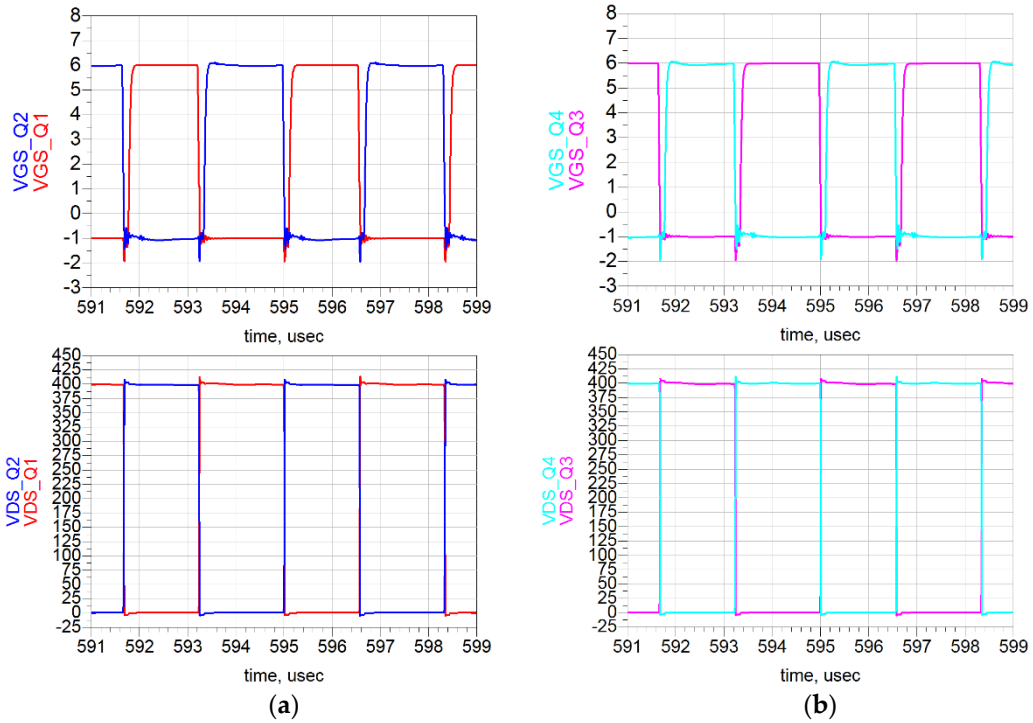


Figure 3.27 Post-layout simulation results: a) V_{GS} and V_{DS} of Q1-Q2; b) V_{GS} and V_{DS} of Q3-Q4.

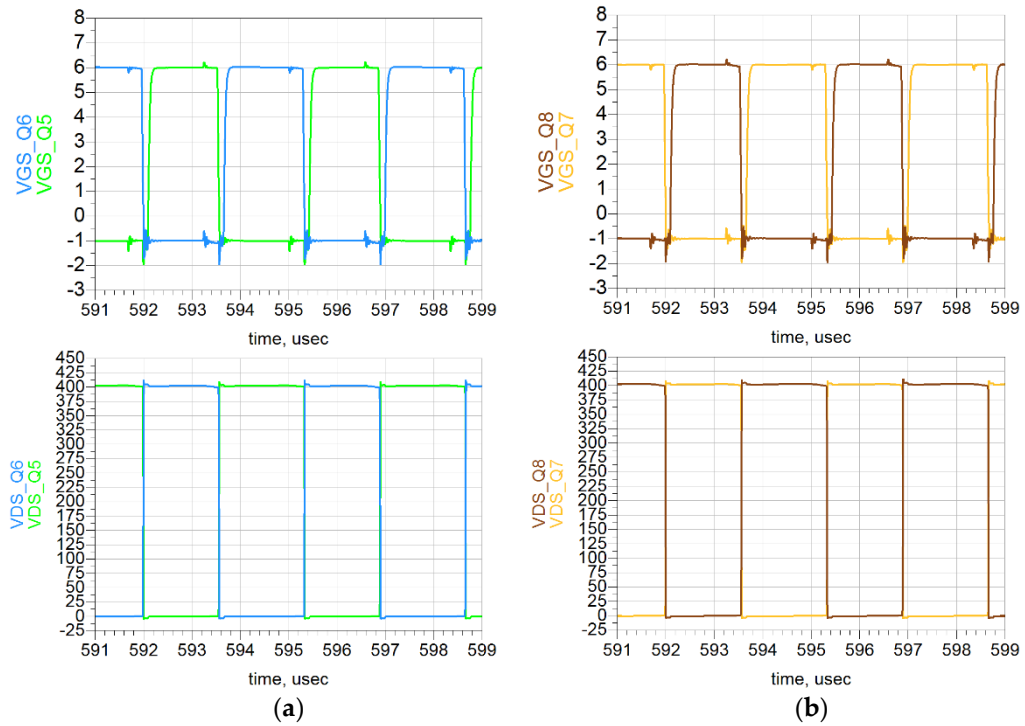


Figure 3.28 Post-layout simulation results: a) V_{GS} and V_{DS} of Q5-Q6; b) V_{GS} and V_{DS} of Q7-Q8.

The success of design efforts is further evidenced by the details of Q2 ZVS turn-on and Q1 almost ZVS turn-off in Figure 3.29. In fact, only minor differences can be appreciated with respect to the electrical simulations discussed in Section 3.2.

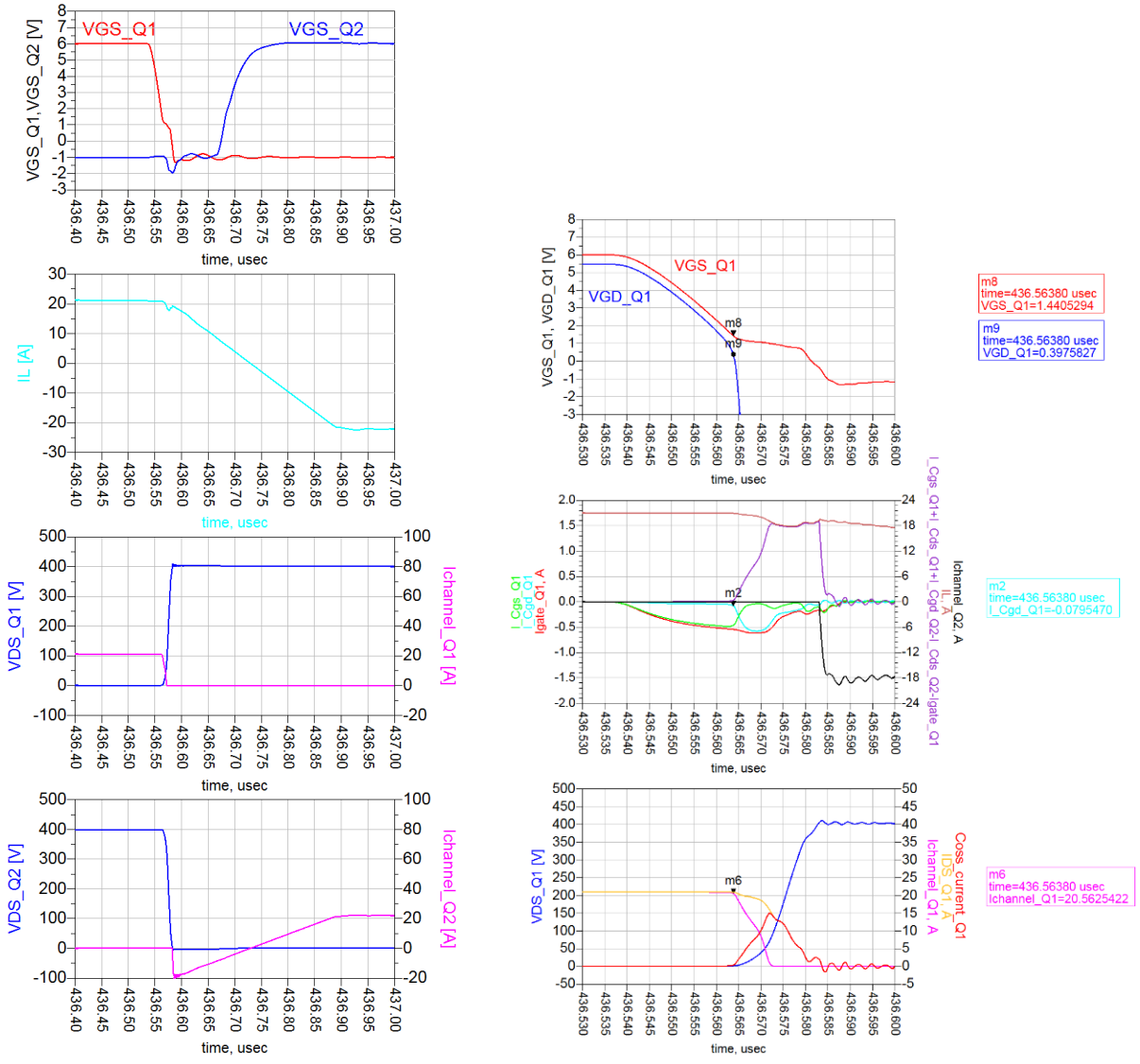


Figure 3.29 Post-layout simulation results: a) Q2 ZVS turn-on; b) Q1 almost ZVS turn-off.

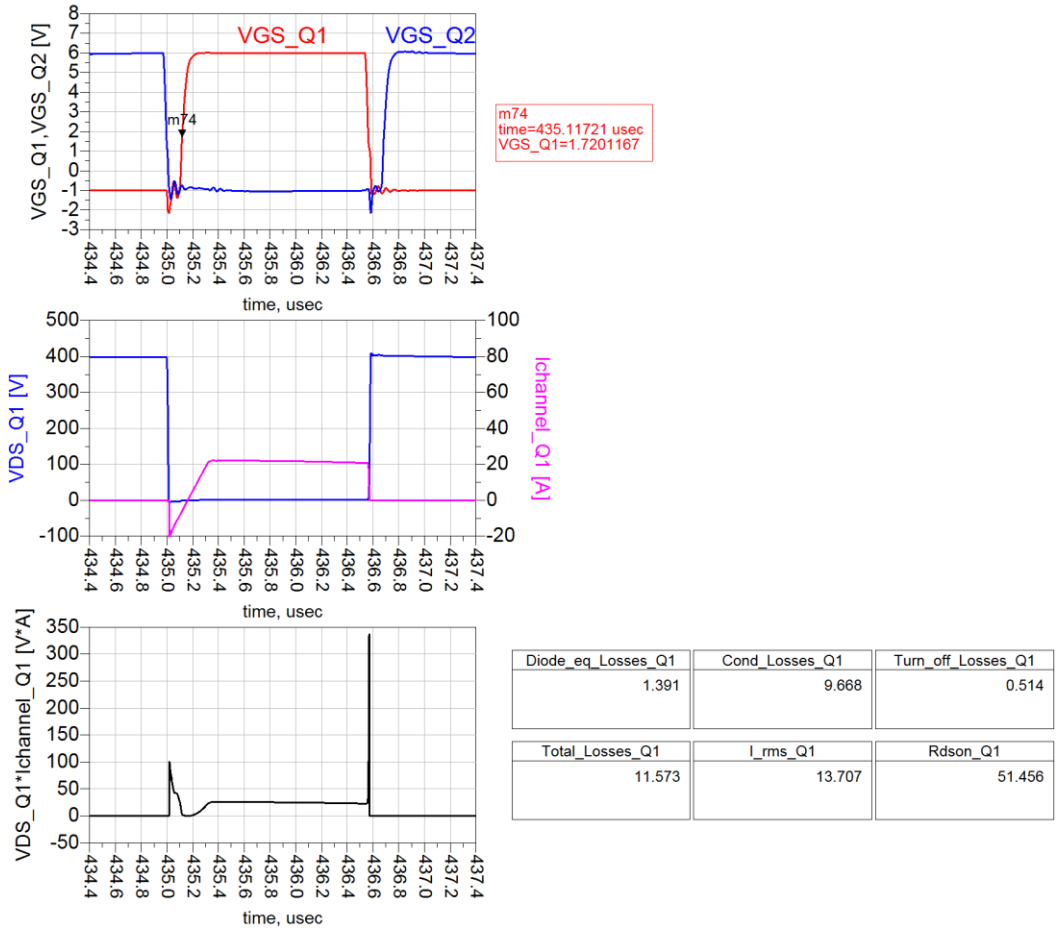


Figure 3.30 Post-layout simulation results: Q1 power losses (@ Tj = 120 °C, $V_{GS,off}$ = -1 V).

For the final implementation of the DAB converter it has been decided to exploit $V_{GS,off}$ = -1 V, which enables a better trade-off between dead-time (i.e. third-quadrant) and turn-off losses for this design case, as it is clear from Figures 3.30 and 3.31. In fact, when $V_{gs,off}$ = -1 V, the full drain-source voltage across the device in third-quadrant operation (@ 25 °C) is equal to

$$V_{DS} = -V_{GS(th)} - |V_{GS,off}| - R_{ds,rev} \cdot I_{SD} \approx -3.02\ V \tag{3.15}$$

and thus diode-equivalent losses show a reduction. On the other hand, the turn-off strength is lowered leading to increased turn-off losses, but still a Miller voltage (1.44 V) below the threshold can be seen in Figure 3.29b.

The overall losses of Q1 GaN HEMT are reduced by about 0.51 W with respect to the electrical simulation reported in Section 3.2 (Figures 3.17 and 3.18) which exploits $V_{gs,off}$ = -3 V. The pie chart in Figure 3.31 displays the weights of the different contributions to Q1 losses.

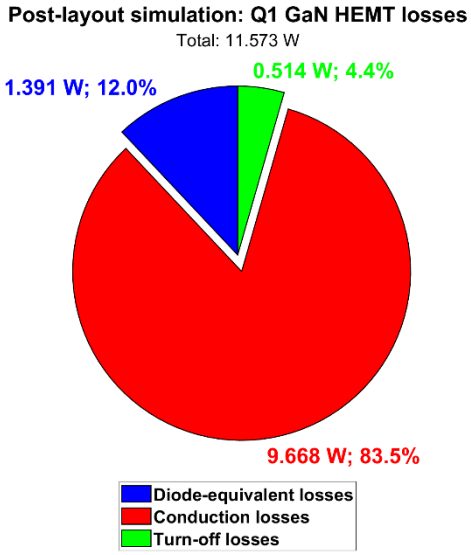


Figure 3.31 Post-layout simulation: contributions of Q1 power losses (@$V_{GS,off}$ = -1 V).

Total losses for Q1-Q8 are reported in Table 3.7.

Table 3.7 Post layout simulation: GaN HEMTs losses (@ V_{in} = 400 V, V_{out} = 400 V, P_{out} = 6.6 kW, f_{sw} = 300 kHz, V_{GS} = 6/-1 V, R_G = 10/2 Ω, dead time = 100 ns, Tj = 120 °C).

Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Total
11.57 W	13.14 W	13.27 W	11.44 W	15.54 W	11.76 W	11.92 W	15.42 W	104.06 W

The total losses of DAB converter can be then quantified in 123.97 W with a reduction of about 8 W with respect to the electrical simulation reported in Section 3.2 (Figure 3.19), and its efficiency turns out to be 98.16 %. Pie chart of DAB converter losses is shown in Figure 3.32.

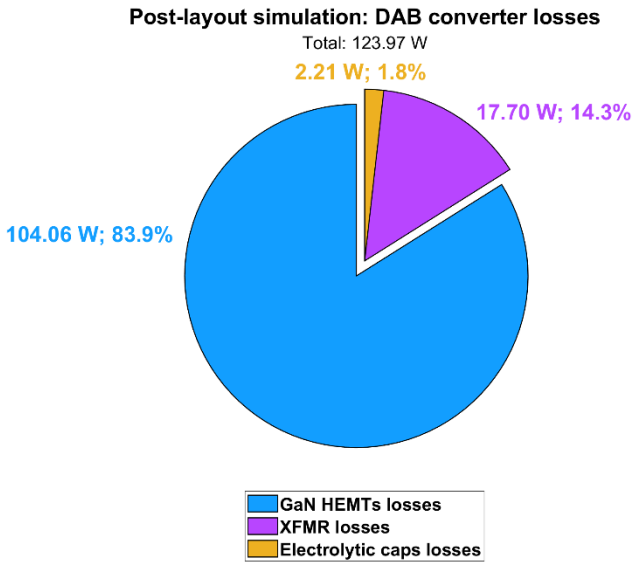


Figure 3.32 Post-layout simulation: contributions of DAB converter losses (@$V_{GS,off}$ = -1 V).

This discussion on the need of layout optimization ends by simulating a worse PCB design. Extra inductances have been added on the gate (15 nH) and on the source (30 nH) of GaN devices, between GaN devices and ceramic capacitors (20 nH) and between ceramic and electrolytic capacitors (20 nH). As a comparison, it is interesting to highlight that 10-15 nH can be a typical range value of the package inductances of a TO-247 transistor. Figure 3.33 reports the simulation results of the mentioned non-optimized layout. High-frequency ringing and oscillations due to the resonance effect of the parasitics can be noted both on the V_{GS} and V_{DS} voltages. These latter also exhibit an overvoltage of 100 V. The consequences are worse reliability and EMI performance, which can prevent the certification of the product according to the strict requirements of CISPR 32/EN 55022/32 Class B regulation. On the other hand, under the described operating conditions, there is not a major impact on the switching losses since the device experiences in any case a ZVS turn-on and an almost ZVS turn-off.

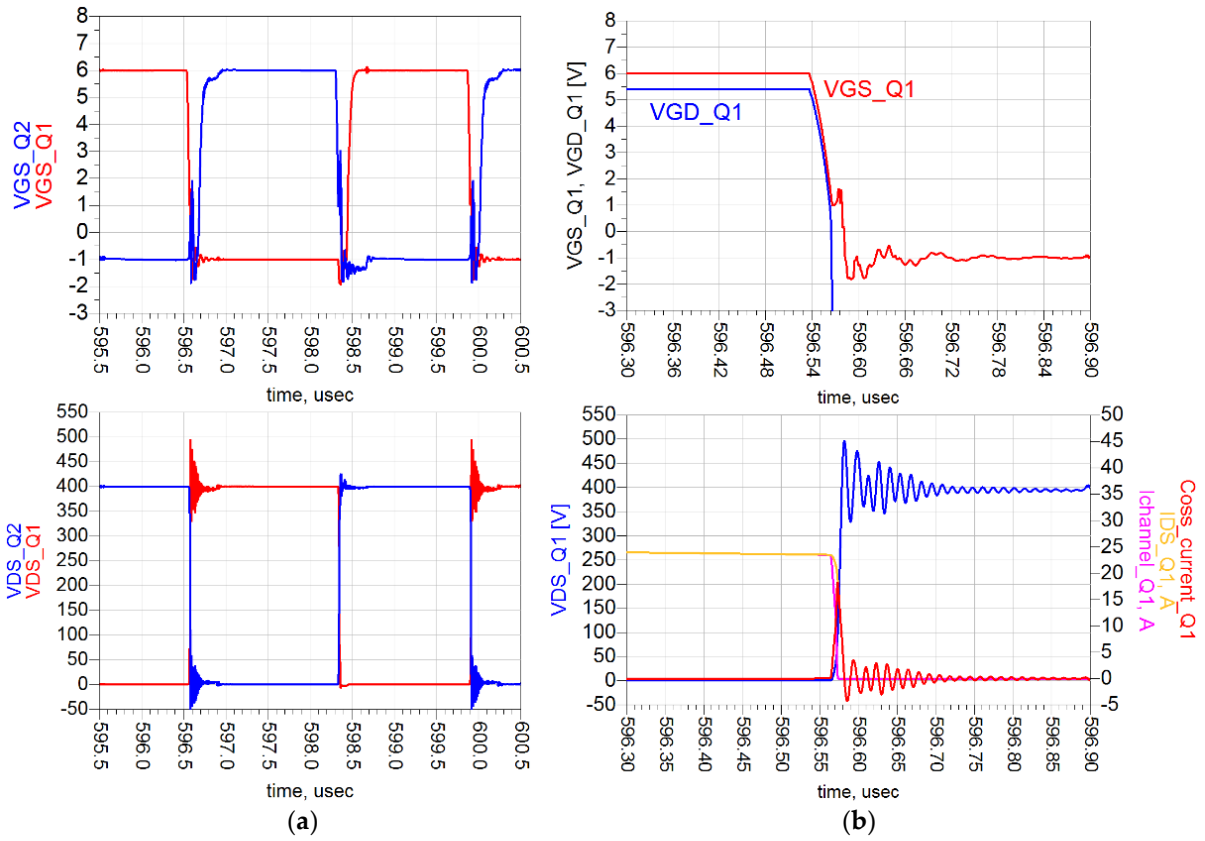


Figure 3.33 Worse design simulation results: a) V_{GS} of Q1, Q2 and V_{DS} of Q1, Q2; b) Q1 almost ZVS turn-off.

At present, the developed DAB converter prototype has been tested up to 4.5 kW. Since it is not possible to probe the current of the individual GaN device, simulation results can be only verified on the basis of the global performances of the converter and by comparing the measurable waveforms. The temperature of the components acquired through the thermal camera and the global efficiency of the DAB converter are

consistent with simulation results. Moreover, as reported in Figures 3.34-3.36 and anticipated in Section 2.5, the comparison between simulated and measured waveforms (series inductor current I_L, V_{DS} and V_{GS} of Q2 at 3.3 kW power level) exhibits an optimal fitting and the absence of the typical ringing effect due to excessive parasitics. It is worth noticing that measurements have been performed exploiting wideband sensors (20 MHz Rogoski current probe and 100 MHz active differential voltage probe) and digital oscilloscope (500 MHz MSO-56 Tektronix at 6.25 GS/s) that can capture without filtering/attenuating any eventual high frequency component (e.g., ringing) of the waveforms.

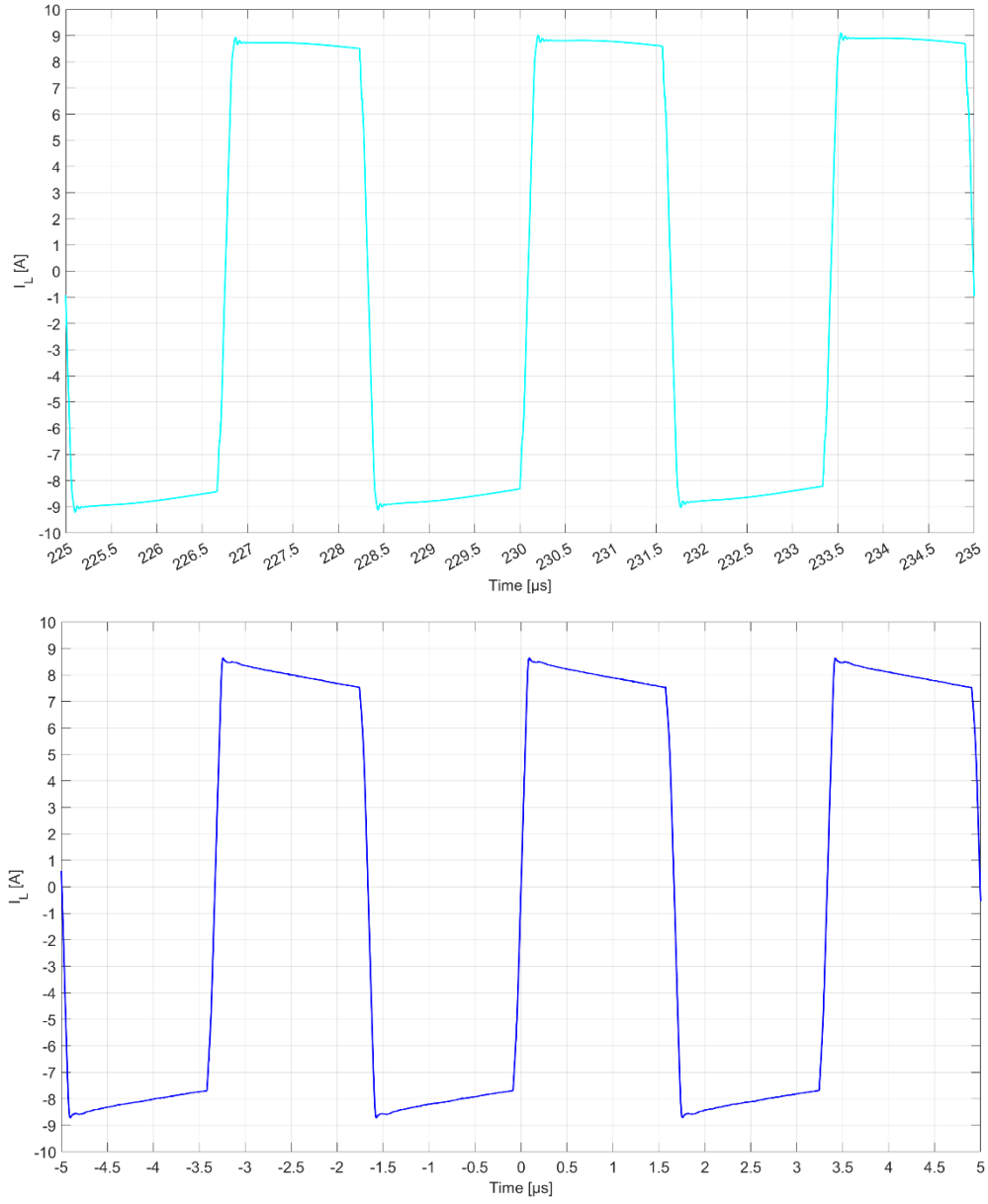


Figure 3.34 Comparison between the series inductor current I_L from post-layout simulation (first plot) and I_L from scope acquisition (second plot).

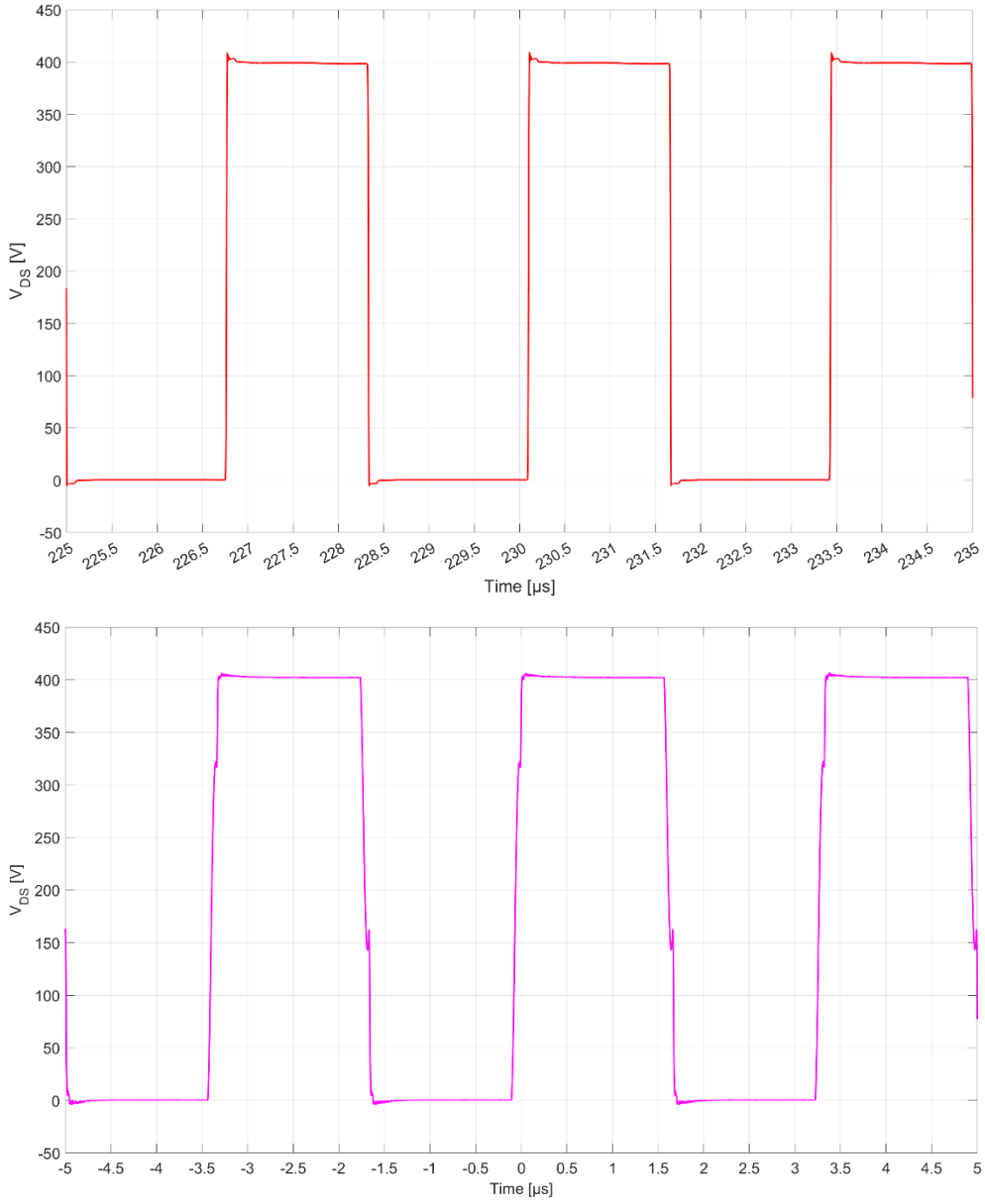


Figure 3.35 Comparison between V_{DS} of Q2 from post-layout simulation (first plot) and V_{DS} of Q2 from scope acquisition (second plot). Q2 refers to the schematic in Figure 3.10.

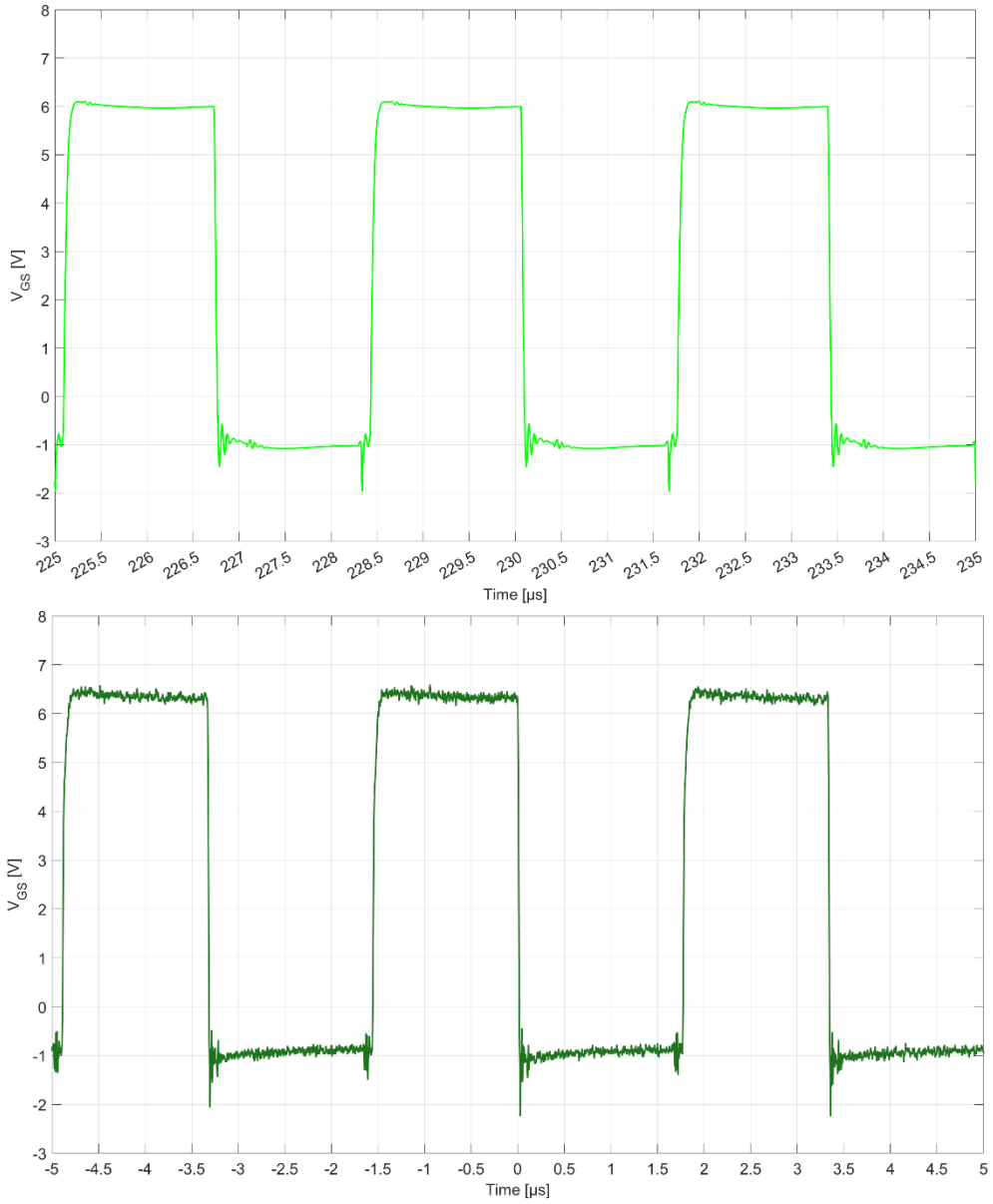


Figure 3.36 Comparison between V_{GS} of Q2 from post-layout simulation (first plot) and V_{GS} of Q2 from scope acquisition (second plot). Q2 refers to the schematic in Figure 3.10.

Chapter 4

Conclusions

In the presented work, the design procedure and implementation of a high power-density GaN-based On-Board Charger has been carried out exploiting automotive-grade GaN HEMT discrete devices. In Chapter 2 the overall design flow in PSIM simulation software has been discussed, also retrieving all the power loss contributions of PFC, DAB and PSFB converters composing the OBC. Top-notch results in terms of efficiency and power density have been achieved due to the implementation of a high switching frequency, combined with wise topology choices. Dimensional reference and thermal results of the OBC have been provided, along with some experimental measurements of the waveforms.

In Chapter 3, details of GaN power devices have been deeply analyzed, highlighting some peculiar characteristics of such technology. In fact, the high speed commutation behaviour of GaN transistor associated with the implementation of an increasingly high switching frequency, are leading designers to adopt an approach that is typical in RF (Radio Frequency) electronics: the electromagnetic simulation of the PCB layout. The aim is to assess the design requirements in terms of parasitics, avoiding rework after board production (which can be a typical step of product development if low switching speed Silicon-based devices are used). As a result, in Advanced Design System, a step-by-step process has been adopted with the ultimate goal of developing a high reliability OBC, which also exhibits excellent EMI performance denoted by the absence of high-frequency ringing or oscillation at commutations, as well by the practically negligible drain-source and gate-source under/overshoots. This has been possible only through a correct estimation and a meticulous minimization of the PCB layout parasitics. Also, it is noteworthy that distinguishing between the channel current and the currents of parasitic capacitances, the switching behaviour has been analyzed both at the intrinsic and extrinsic device level. A Miller voltage below the threshold in case of a strong driver at turn-off has been reported.

Thanks to the collaboration with a specialized company that has a notable experience also in control algorithm and software design, the OBC prototype that has been developed is capable of entering mass production exhibiting state-of-the-art performance.

References

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