ALMA MATER STUDIORUM
UNIVERSITÀ DI BOLOGNA

DOTTORATO DI RICERCA IN

INGEGNERIA BIOMEDICA, ELETTRICA E DEI SISTEMI

Ciclo 37

Settore Concorsuale: 09/E2 - INGEGNERIA DELL'ENERGIA ELETTRICA

Settore Scientifico Disciplinare: IIND-08/A - CONVERTITORI, MACCHINE E AZIONAMENTI ELETTRICI

POWER ELECTRONICS SOLUTIONS AND ARCHITECTURES FOR INDUSTRIAL AND HIGH-POWER APPLICATIONS

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Esame finale anno 2025

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Abstract

This PhD thesis is part of a high-level apprenticeship (Dottorato in Apprendistato di Alta Formazione e Ricerca) conducted in collaboration between OCEM Power Electronics and the University of Bologna. The research focuses on the development of power electronics solutions and architectures for industrial and high-power applications, addressing the growing need for more efficient, scalable, and flexible systems in these sectors. The thesis combines both practical industrial applications and theoretical advancements, demonstrating the importance of power electronics in managing complex, high-demand energy environments.

The thesis is structured into five chapters, with the first three detailing the work carried out at OCEM Power Electronics and the last two chapters covering research conducted at the University of Bologna.

In the first chapter it is introduced the Poseidon Project, an EU-funded initiative that addresses energy storage for marine environments through the development of a Fast-Response Energy Storage System. This system integrates advanced technologies to provide reliable, efficient power delivery while significantly reducing fuel consumption and emissions in maritime operations. This chapter highlights how hybrid energy storage solutions can meet dynamic power demands while contributing to sustainable maritime practices.

The second chapter presents a collaborative study on Poloidal Field (PF) coils conducted with ENEA Frascati, which focuses on optimizing the power supply systems for poloidal field coils used in tokamak fusion reactors. Supercapacitors were used to enhance the rapid energy release needed for plasma stabilization, reducing the system's physical and energy footprint. The results demonstrate how power electronics can provide responsive and efficient solutions for the high-power demands of fusion reactors.

The third chapter deals with the design and testing of a high-voltage pulse generator prototype. While the prototype achieved the required technical specifications, delivering 25 kV pulses with fast rise times, further refinements are suggested to enhance the reliability and performance of the system.

The second part of the thesis focuses on theoretical advancements in power electronics, with research conducted at the University of Bologna. Chapter four explores Modular Multilevel Converters, which are increasingly used in many different fields due to their modularity and scalability. The research introduces novel theoretical framework based on two-time scale analysis, improving the performance of the converter.

Chapter five investigates matrix rectifiers as an alternative to conventional rectifiers, providing direct AC-to-DC conversion with greater efficiency due to a tailored control strategy for losses reduction. This work highlights the potential of matrix rectifiers in industrial applications.

Preface

The field of power electronics has become a cornerstone of modern technology, playing a pivotal role in a wide range of applications that demand efficient, reliable, and scalable solutions for energy conversion and management. As industries continue to evolve and the demand for electrical power grows, power electronics solutions are increasingly required to handle not only high power levels but also the complex operational dynamics of large-scale systems. The need for effective power electronics architectures is particularly acute in industrial and high-power applications, where operational efficiency, system flexibility, and sustainability are critical to maintaining competitiveness and meeting environmental regulations.

Power electronics involves the conversion and control of electrical energy using semiconductor devices to manage power flow between sources and loads. Its applications are diverse, ranging from energy distribution in industrial settings to renewable energy integration, transportation, and scientific research. The ability to precisely manage power at various levels, whether converting AC to DC, managing voltage levels, or improving energy efficiency, makes power electronics essential to the performance and reliability of modern energy systems.

In industrial and high-power applications, the challenges are amplified. Systems often operate at very high power levels, requiring robust and scalable solutions that can withstand demanding operational conditions. These applications include large manufacturing plants, electrical grids, transportation systems, and specialized research facilities that rely on advanced power conversion systems. The focus in these environments is on delivering consistent, reliable performance while minimizing energy losses, improving overall system efficiency, and reducing environmental impact.

As the demand for energy continues to grow, there is also an increasing emphasis on sustainable energy solutions. This has led to the exploration of new energy storage technologies, renewable energy integration, and the development of more efficient power conversion systems that can support the shift towards cleaner energy. In high-power applications, such as those found in industrial environments or large-scale infrastructure, the role of power electronics is not only to improve efficiency but also to ensure that systems can

adapt to changing operational conditions, manage peak power demands, and integrate with renewable energy sources.

In this context, power electronics architectures are developed to optimize the interaction between energy sources, conversion systems, and storage technologies. These architectures must be flexible enough to support a wide range of operating conditions, from steady-state energy conversion to handling transient peaks in power demand. Additionally, they must be scalable, allowing for expansion as systems grow or as energy demands increase. The development of innovative architectures that integrate new energy storage systems and efficient converter designs is crucial to meeting these challenges.

This PhD thesis, titled *"Power Electronics Solutions and Architectures for Industrial and High Power Applications",* investigates these challenges. It is the culmination of a high-level apprenticeship (*Dottorato in Apprendistato di Alta Formazione e Ricerca*) conducted in collaboration between OCEM Power Electronics (a division of Energy Technology S.r.l.) and the Alma Mater Studiorum University of Bologna. This thesis explores these challenges and presents solutions aimed at addressing the increasing complexity of power systems in industrial and high-power environments.

This work is divided into two primary sections, focusing first more on the practical applications of power electronics within OCEM Power Electronics, while dealing more later with theoretical aspects and control strategies developed at the Department of Electrical, Electronic, and Information Engineering (DEI) at the University of Bologna. Each section presents distinct but interconnected contributions to the overall theme of optimizing power electronics solutions for high-demand environments.

At OCEM Power Electronics, the focus was on developing solutions that could meet the immediate challenges of industrial applications. One of the major projects undertaken during this research was the Poseidon project, a project that is part of the Horizon EU research & innovation framework programme, which aimed to create a Fast-Response Energy Storage System for marine applications. In marine environments, power demands can fluctuate rapidly, particularly during critical operations such as port maneuvers or dynamic positioning. The Poseidon Project addressed these challenges by integrating three advanced energy storage technologies: Kinetic Energy Storage Systems, Superconducting Magnetic Energy Storage, and Electrostatic Energy Storage Systems. These systems, when combined, provide the ability to deliver high bursts of power instantly, while also storing energy

efficiently for extended periods. The research demonstrated how these integrated systems could significantly reduce fuel consumption and emissions in maritime operations, aligning with global efforts toward decarbonization.

Another key area of research conducted at OCEM was the collaborative study with ENEA Frascati, which focused on the power supply systems for poloidal field coils used in tokamak fusion reactors. PF coils are responsible for shaping and stabilizing the plasma within the reactor, and their power systems must be highly responsive to the dynamic power requirements of the fusion process. This study explored the use of supercapacitors to optimize energy storage for these systems, providing rapid power delivery while reducing the physical footprint of the energy storage units. The ability to manage power peaks and reduce strain on the external power grid was a central challenge addressed in this work.

A further project focused on the development of a high-voltage pulse generator for industrial applications. High-voltage pulse generators are widely used in research facilities for processes like particle acceleration, which require precise and powerful pulses. The pulse generator designed in this project was a compact, high-performance prototype capable of delivering 25 kV pulses with a fast rise time, addressing the need for efficient and reliable pulse generation in space-constrained environments. The research highlighted the importance of optimizing the generator's design to minimize parasitic inductance and ensure reliable performance under high-voltage conditions.

The second part of the thesis transitions to the theoretical work conducted at the University of Bologna. Here, the focus shifted toward the development of advanced power conversion systems that could meet the future demands of high-power applications. One of the key areas of research was on Modular Multilevel Converters, a technology that has gained prominence for its use in high-voltage direct current transmission systems. MMCs offer distinct advantages in terms of scalability and efficiency, making them ideal for large-scale energy transmission. The research in this area introduced new control strategies, particularly through the development of two-time scale analysis methods, which enhance the performance of MMCs in dynamic environments. These strategies allow the converters to handle varying loads more effectively, maintaining stability and efficiency even under rapidly changing conditions.

Finally, the thesis examines the potential of matrix rectifiers as an alternative to conventional rectifiers. Matrix rectifiers provide direct AC-to-DC conversion, offering

higher efficiency than traditional systems. The research explored the theoretical foundations of matrix rectifiers, as well as their practical applications in industrial settings, demonstrating their ability to improve power quality and reliability in high-power environments.

Chapter 1

ENERGY STORAGE FOR MARINE APPLICATIONS

1.1 Introduction

The maritime industry is the backbone of global trade, responsible for transporting around 90% of the world's goods. However, this sector also contributes significantly to greenhouse gas (GHG) emissions, accounting for nearly 2.5% of global CO_2 emissions [1]. As the urgency to address climate change grows, decarbonizing maritime transport has become a priority for policymakers, industry leaders, and researchers.

1.1.1 Current State of Decarbonization Efforts

CO2 emissions remain significantly high, highlighting the urgent need for effective reduction strategies. Despite fluctuations in recent years due to events like the COVID-19 pandemic and changes in EU regulations. Looking at Figure 1.1 the rebound visible in 2022 shows that emissions are far from being under control. Proactive measures are essential to achieve meaningful and sustained reductions. Efforts to decarbonize maritime transport include exploring alternative fuels, enhancing energy efficiency, integrating renewable energy, and advancing digital technologies to optimize operations.

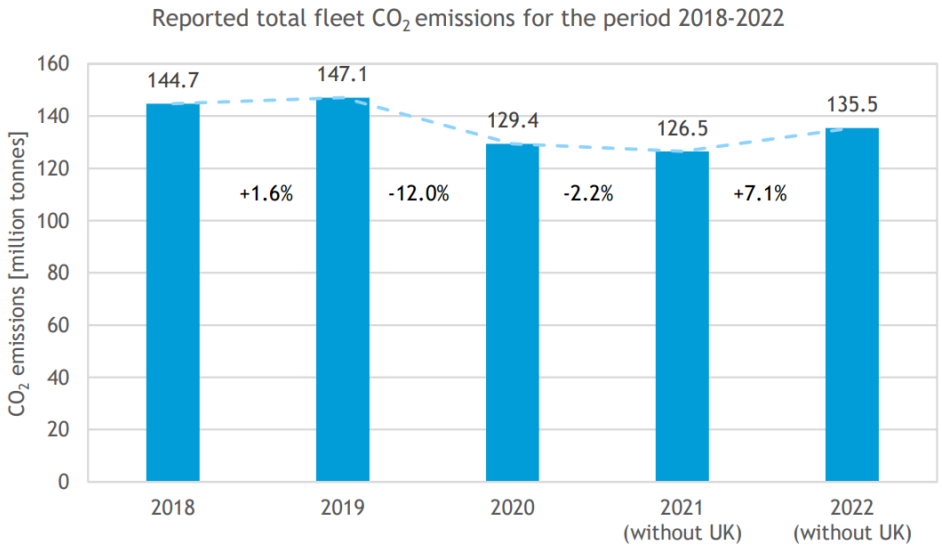


Figure 1.1 – Reported total EU fleet CO2 emissions; 2018-2022 [2].

A key strategy is the transition from heavy fuel oil to low or zero-carbon fuels. Alternatives like Liquefied Natural Gas (LNG), biofuels, hydrogen, ammonia, and methanol are considered, but each comes with its own challenges, such as availability, energy density, storage needs, and the requirement for new infrastructure. For instance, while LNG reduces some emissions, it is still a fossil fuel and may not meet long-term decarbonization targets [3].

Improving energy efficiency is another important step toward reducing emissions. New ship designs, including advanced hull forms and propulsion systems, help lower fuel consumption. Technologies like air lubrication systems reduce friction between the hull and water, and waste heat recovery systems capture excess energy for additional power [4]. The IMO's Energy Efficiency Design Index (EEDI) sets mandatory standards for new ships, pushing for more sustainable designs.

Renewable energy also plays a role. Wind-assisted propulsion technologies, such as rotor sails and kites, harness wind power to reduce fuel usage, while solar panels provide energy for onboard electrical systems. These technologies, though supplementary, contribute to lowering emissions [5].

Digitalization enhances operational efficiency through data analytics, real-time monitoring, and artificial intelligence. Efficient route planning and speed optimization allow ships to minimize fuel consumption by arriving at ports "just in time", cutting emissions without affecting delivery schedules [6].

Regulatory and market-based measures, like carbon pricing mechanisms and emissions trading systems, are also pushing the industry toward greener technologies. These approaches internalize the environmental costs of emissions, encouraging investment in low-carbon solutions [7].

1.1.2 Challenges Faced

Despite progress, significant challenges remain in decarbonizing the maritime industry. Economic viability is a major concern, as the costs of developing and deploying new technologies and fuels are often high. Without adequate financial incentives or regulations, shipowners may hesitate to invest in unproven or expensive solutions.

Infrastructure limitations also pose a challenge. The global infrastructure for alternative fuels is underdeveloped, requiring significant investments in bunkering facilities and supply chains. Building this infrastructure demands international coordination and cooperation.

Many low or zero-carbon technologies are still in the early stages of development. Scaling these solutions to meet the demands of global shipping presents technical challenges, including ensuring safety, reliability, and compatibility with existing systems.

The regulatory complexity of international shipping makes enforcing uniform standards difficult. Harmonizing policies across nations and ensuring compliance require international collaboration, which is often challenging due to differing national priorities and interests [8]-[9].

1.2 Legislative Framework

Energy storage systems on ferries to reduce GHG emissions are governed by a complex legislative framework that includes international, regional, and national regulations. Central to this framework is the International Maritime Organization (IMO), a United Nations agency responsible for regulating shipping. The IMO has developed several conventions and regulations to minimize the environmental impact of maritime transport.

One key instrument is the International Convention for the Prevention of Pollution from Ships (MARPOL), particularly Annex VI, which addresses air pollution from ships. Annex VI sets limits on nitrogen oxides (NO_x) and sulfur oxides (SO_x) emissions and introduces the Energy Efficiency Design Index (EEDI) and the Ship Energy Efficiency Management Plan (SEEMP) [10]. The EEDI sets energy efficiency standards for new ships, and the SEEMP requires all ships to have plans for improving energy efficiency. These regulations encourage the adoption of energy storage systems, as they promote technologies that enhance efficiency and reduce emissions.

The IMO's 2018 Initial Strategy on reducing GHG emissions aims to cut CO_2 emissions per transport work by at least 40% by 2030 and to pursue efforts toward a 70% reduction by 2050, compared to 2008 levels. Additionally, it aims to reduce total annual GHG emissions by at least 50% by 2050, while ultimately phasing them out entirely. This strategy highlights the importance of innovative solutions, such as energy storage systems, to help meet these goals.

At the regional level, the European Union has taken further steps through the EU MRV (Monitoring, Reporting, Verification) Regulation, which requires ships over 5,000 gross tons visiting EU ports to monitor and report CO_2 emissions. The EU is also incorporating maritime shipping into its Emissions Trading System (ETS), incentivizing GHG reductions and promoting clean technologies [11].

National regulations can also impact energy storage systems on ferries. Coastal states can implement stricter environmental regulations within their territorial waters and Exclusive Economic Zones (EEZs). Some nations offer incentives for green technologies, including energy storage, or impose stricter emission limits in designated Emission Control Areas (ECAs).

Safety regulations are another crucial aspect of the legislative framework. The International Convention for the Safety of Life at Sea (SOLAS) sets minimum safety standards for ships, and energy storage systems must comply with SOLAS requirements, as well as guidelines from the International Electrotechnical Commission (IEC) and classification societies, to ensure that they do not compromise vessel safety.

1.3 The Role of Energy Storage Systems in Marine Applications

Energy Storage Systems (ESSs) play a crucial role in the marine sector due to the operational demands of modern ships. Vessels often face sudden changes in power needs, especially during activities like dynamic positioning, port entry, and emergency maneuvers. In these situations, a quick response from the ESS is essential to deliver power without waiting for traditional engines to adjust. ESSs are designed to supply high power for short periods with immediate response, making them ideal for maintaining stability and performance in fast-changing scenarios. For instance, in dynamic positioning, ESSs can instantly provide the power needed for thrusters, reducing the strain on diesel engines and cutting fuel consumption. Similarly, during peak loads, ESSs offer supplementary power, preventing engines from operating inefficiently at fluctuating levels.

One of the key benefits of ESSs in marine applications is their ability to improve fuel efficiency. By reducing the reliance on engines during peak loads or transient events, ESSs allow the main engines to function closer to their optimal efficiency, cutting fuel consumption and emissions. This is especially beneficial in hybrid vessels, where ESSs and traditional engines work together to extend operational range while reducing environmental impact.

ESSs also enhance the safety and reliability of marine operations. In emergency situations, such as equipment failure, the ability to instantly provide power can be critical, ensuring that vital systems like navigation and steering controls remain operational.

ESSs bridge the gap between slow-reacting traditional power sources and the fast-changing energy needs of modern marine operations, ensuring both efficiency and reliability.

1.3.1 Types of Energy Storage Technologies

Marine applications require ESSs that are reliable, scalable, durable, and efficient. This section explores four major ESS technologies currently used or under development in the maritime industry: batteries, supercapacitors, flywheels, and superconducting magnets.

Each energy storage technology exhibits different performance characteristics in terms of power density and energy density. The Ragone diagram shown in Figure 1.2 summarizes the main technologies used for energy storing.

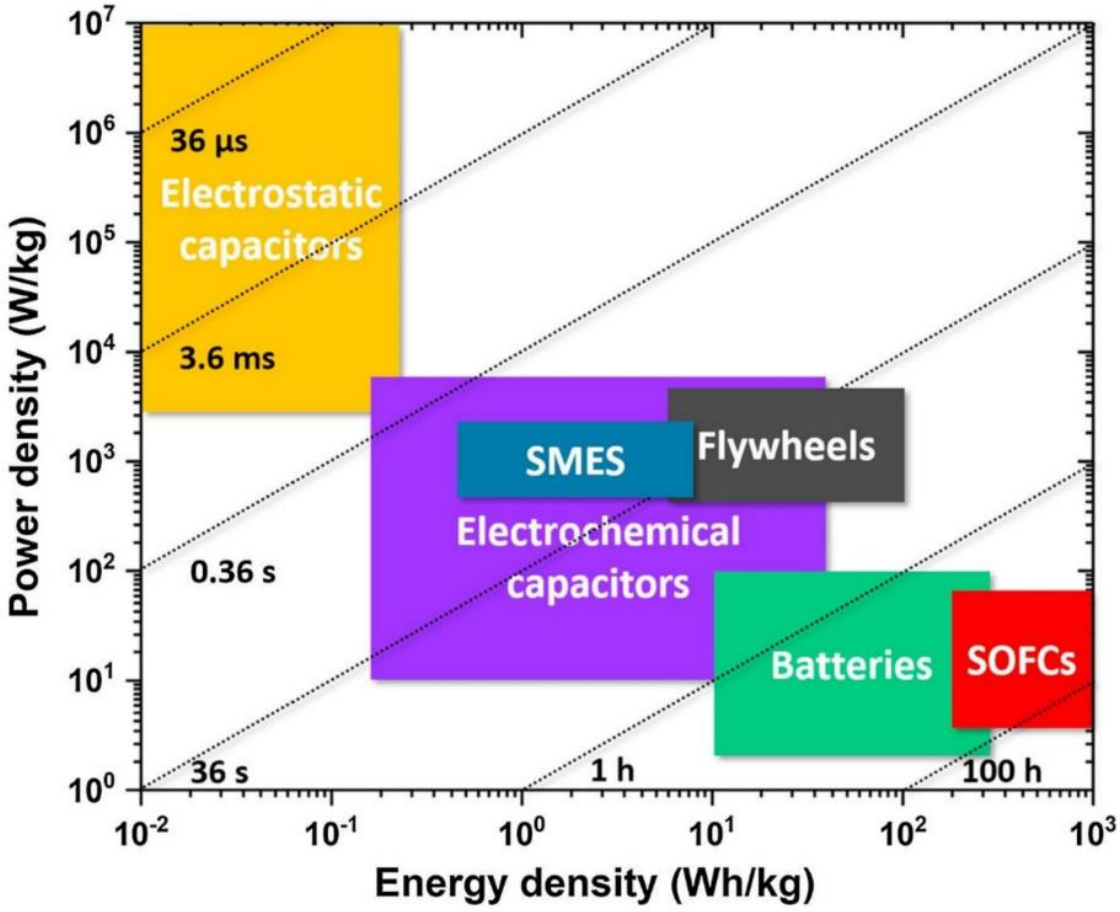


Figure 1.2 – Ragone diagram of ESS technologies [12].

1.3.1.1 Batteries

Batteries have been the most common form of energy storage in marine applications due to their reliability [13]-[14]. However, despite their widespread use, batteries like lithium-ion, lead-acid, and sodium-sulfur each come with challenges.

Lithium-ion batteries are considered the most suitable for marine use because of their high energy density, efficiency, and long-life cycle. They deliver sustained power over long periods, making them ideal for hybrid propulsion and electric ships. Their fast charging times are essential for vessels like ferries that require quick turnarounds. However, they are sensitive to extreme temperatures and can pose safety risks, such as thermal runaway. Advanced thermal management systems are required to mitigate these risks, and their high cost and space requirements remain barriers for some vessels.

Lead-acid batteries are still used due to their low cost and availability, often in auxiliary systems for backup power. However, they suffer from low energy density, short life cycles, and slow charging times. Corrosion from saltwater exposure can also degrade performance over time, making them less suitable for demanding applications.

Sodium-sulfur batteries offer high energy density and deep discharge capabilities but require high operating temperatures, which adds complexity and takes up valuable space. For smaller vessels, the added cost and operational difficulty outweigh the benefits, making them less practical for widespread use.

Batteries remain the primary energy storage solution for providing stable power over long periods, making them a cornerstone in marine applications like hybrid propulsion and electric ships. Among the various battery technologies, lithium-ion batteries are often favored due to their high energy density, efficiency, and relatively long-life cycle. Other battery types, such as lead-acid and sodium-sulfur, are still in use but come with limitations like lower energy density, slower charging times, or higher operational complexity.

However, while batteries excel at delivering steady power over extended durations, they are not the optimal choice for handling high power peaks over short periods. During transient operations, such as port maneuvers or emergency power demands, the rapid response required can place considerable stress on batteries, leading to faster degradation and reduced lifespan. In these scenarios, fast-response energy storage technologies are better suited to meet the high-power, short-duration demands without compromising the long-term health of the battery system.

1.3.1.2 Supercapacitors

Supercapacitors, also known as ultracapacitors, complement batteries in marine ESSs. Unlike batteries, which store energy chemically, supercapacitors store it electrostatically, allowing for rapid charge and discharge. This makes them ideal for applications requiring short bursts of high power, such as dynamic positioning, load leveling, or emergency power.

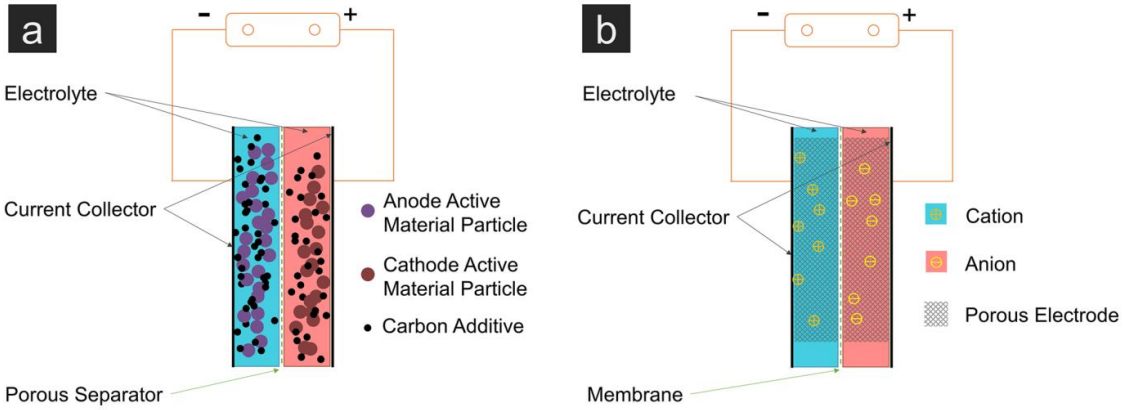


Figure 1.3 - Li-ion battery vs Supercap [15].

Their long life cycle, often exceeding a million cycles, makes supercapacitors particularly useful in continuous operations. However, their lower energy density means they are more suitable for high-power, short-duration tasks rather than long-term energy storage.

1.3.1.3 Flywheels

Flywheels store energy in the form of rotational kinetic energy. In marine applications, they are useful for stabilizing power supplies or providing backup power during peak demand. A rotating mass is accelerated using surplus energy, which is then converted back into electricity during high demand periods [16].

Flywheels are valuable in situations requiring quick response and high-power output, such as ship maneuvers. They are also employed in regenerative braking systems to recover and reuse kinetic energy. While they require minimal maintenance, careful integration into the ship's energy management system is needed to ensure efficiency.

1.3.1.4 Superconducting Magnets

Superconducting magnets store energy in a magnetic field generated by a current through a superconducting coil. Their ability to deliver near-instantaneous power makes them highly effective for marine applications that require fast-response energy.

While superconducting magnets systems offer great potential for stabilizing voltage and frequency, they come with challenges, including high costs and the complexity of cryogenic cooling systems. As technology advances, superconducting magnets could become more viable for large-scale marine energy storage.

1.4 Poseidon project

The Poseidon Project is an EU-funded initiative aimed at advancing energy storage solutions for marine applications [17]. Launched on January 1st, 2023, and running until December 31st, 2025, the project's primary goal is to demonstrate the feasibility of a Fast-Response Energy Storage System (FRESS) specifically designed for maritime vessels. This system integrates three advanced technologies: Kinetic Energy Storage System (KESS), Superconducting Magnetic Energy Storage (SMES), and Electrostatic Energy Storage System (EESS). These technologies will be tested on marine vessels to enhance operational efficiency and reduce reliance on traditional fossil fuel engines.

The Poseidon Project aims to address key challenges faced by the maritime industry, such as improving fuel efficiency, reducing emissions, and meeting the growing need for operational flexibility. By leveraging cutting-edge energy storage technologies, Poseidon seeks to optimize vessel performance in critical scenarios, such as docking and dynamic positioning, while contributing to international environmental goals.

In addition to technological development, Poseidon will focus on creating assessment tools like the Levelized Cost of Storage (LCOS) to evaluate the cost-effectiveness of these solutions and conduct Life Cycle Assessments (LCA) to quantify their environmental benefits. The project will also work on establishing safety standards and regulatory frameworks to facilitate the adoption of energy storage systems in the maritime sector.

The early findings of this project have been presented at the ELECTRIMACS'24 held in Castellò (Spain) from the 26th to the 30th of May 2024, and will be available in the proceedings of the conference once they will be published.

1.4.1 Context

The maritime industry plays a pivotal role in global trade but also faces increasing pressure to reduce its environmental impact. The International Maritime Organization (IMO) has set ambitious targets to reduce greenhouse gas (GHG) emissions from maritime transport by

50% by 2050 compared to 2008 levels. Achieving these goals requires the adoption of cleaner, more efficient technologies.

While energy storage systems (ESS) have been explored as a means of reducing emissions and improving operational efficiency, the Poseidon Project aims to push this further by integrating FRESS into large vessels. This system will provide stable and reliable energy during high-demand operations, such as port maneuvering and dynamic positioning, reducing reliance on diesel engines and cutting fuel consumption.

Current propulsion systems often struggle with fluctuating power demands, leading to inefficiencies and increased emissions. By incorporating the advanced energy storage systems developed under Poseidon, vessels can operate more efficiently, with lower emissions and better fuel economy, particularly during peak load periods.

1.4.2 Main Goals

The Poseidon Project's main goals are:

1. **Develop and demonstrate advanced ESS**: The project aims to develop and test three key energy storage technologies: Electrostatic Energy Storage Systems (EESS) based on supercapacitors, Kinetic Energy Storage Systems (KESS) using flywheels, and Superconducting Magnetic Energy Storage (SMES). These systems will be integrated into marine vessels and evaluated for their ability to meet the operational needs of modern shipping.

2. **Assess cost-effectiveness**: Poseidon will develop the Levelized Cost of Storage (LCOS) tool to help maritime operators evaluate the long-term financial benefits of adopting ESS technologies. This tool will provide a comprehensive framework that considers installation, maintenance, operational costs, and fuel savings.

3. **Lifecycle analysis (LCA)**: The project will conduct detailed lifecycle assessments to measure the environmental impact of each energy storage system. These LCAs will focus on quantifying emissions reductions, energy savings, and the overall environmental footprint of the ESS technologies developed under Poseidon.

4. **Ensure safety and regulatory compliance**: As with any emerging technology, safety and regulatory standards are crucial. Poseidon will work closely with international regulatory bodies to ensure that the ESS technologies comply with safety standards

and maritime regulations. This effort includes identifying potential safety risks and contributing to the creation of guidelines for the safe integration of ESS into marine environments.

1.4.3 Fast-Response Energy Storage System (FRESS)

The FRESS is a hybrid solution designed to manage the fluctuating power demands of marine vessels efficiently.

Figure 1.4 - Balearia's ferry.

Developed under the Poseidon project, FRESS integrates three different energy storage technologies: Kinetic Energy Storage System (KESS), Superconducting Magnetic Energy Storage (SMES), and Electrostatic Energy Storage System (EESS)**.** These systems store energy in different ways, allowing for a flexible and reliable energy management solution that can deliver both immediate and sustained power. A significant component of the FRESS development process involved collaboration with Balearia, a leading ferry operator. Balearia not only provided the vessel (a typical vessel is shown in Figure 1.4) that will be equipped with the FRESS, but also supplied the power profiles required during the ferry's port operations.

These power profiles, which outline the energy demand peaks during docking and departure maneuvers, were critical for designing and sizing the FRESS. The power demand during these phases is typically much higher due to the heavy use of thrusters and other high-

power equipment, and the ability to respond to these spikes is crucial for improving operational efficiency.

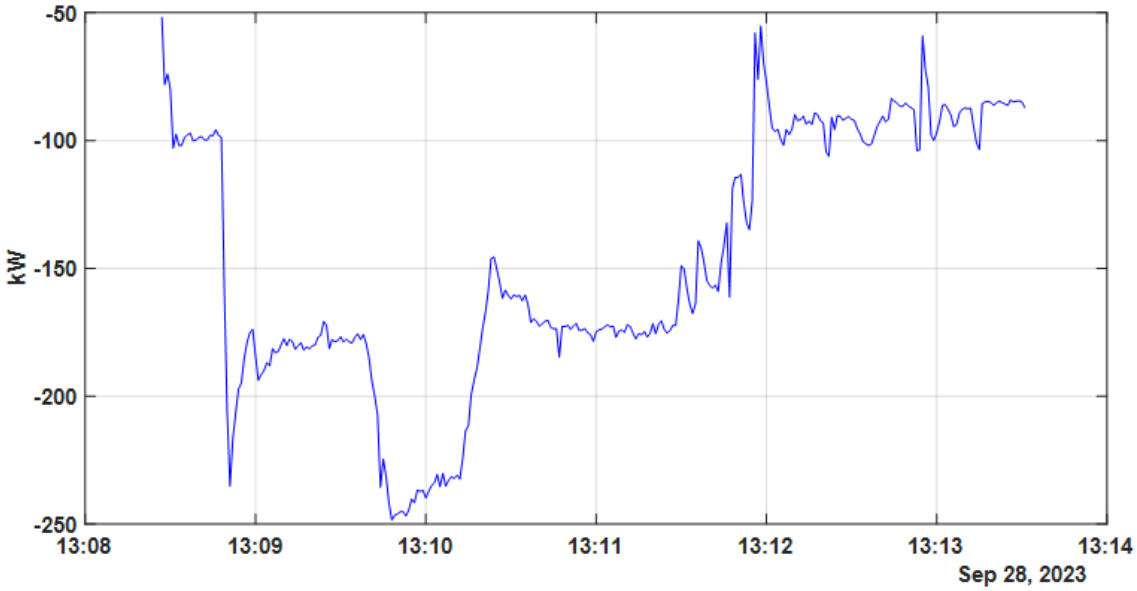


Figure 1.5 - Power demand during port approach.

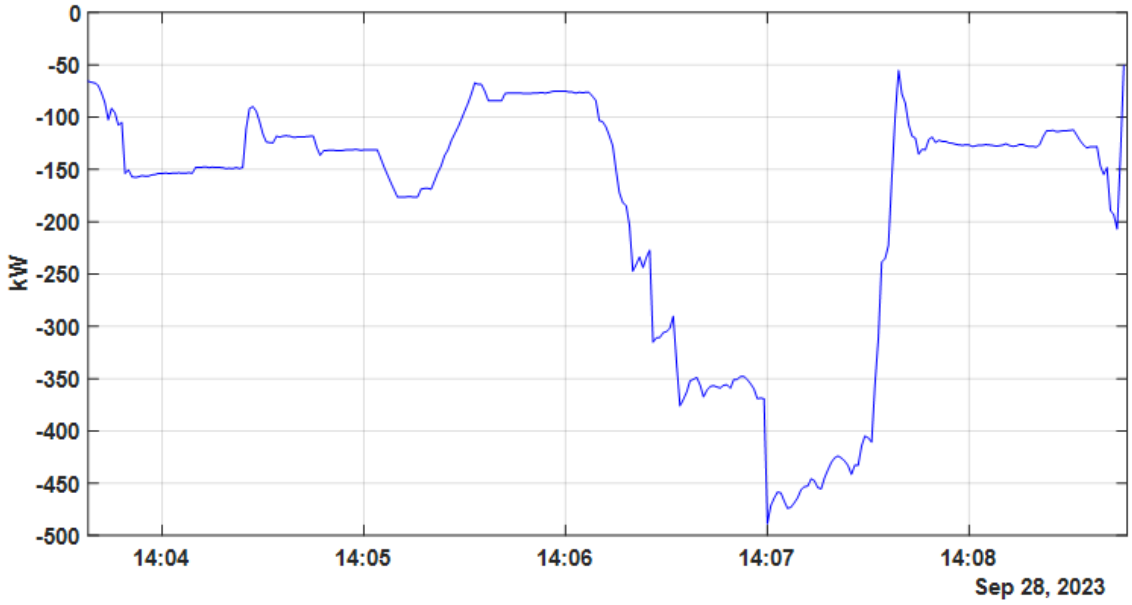


Figure 1.6 - Power demand during port departure.

The FRESS is designed to handle these high-demand periods by using the KESS to absorb and store energy during low-demand phases and release it during peak loads. Meanwhile, SMES provides instantaneous power for stability, and EESS responds to short, sharp power bursts, ensuring that the diesel engines can operate at optimal loads without being overstressed.

This system not only reduces fuel consumption and emissions but also enhances the overall reliability of the ferry's energy management system, making it a crucial step toward more sustainable maritime operations. The ability to combine multiple energy storage technologies in a single integrated system allows FRESS to meet the varying power demands of the vessel while supporting the global push toward cleaner and more efficient marine transport.

1.4.3.1 Kinetic Energy Storage System (KESS)

The KESS relies on the principle of storing energy in a rotating mass, following the equation $E = \frac{1}{2}J\omega^2$, where J represents the moment of inertia and ω the angular velocity. Energy is stored by accelerating the mass using an electric machine coupled to the flywheel. When energy is needed, the machine decelerates the flywheel to extract power. The decoupling of energy and power allows for flexible operation: energy is related to rotational speed, while the power capability is determined by the electric machine's capacity.

In this case, the design target power for KESS is 20 kW, a value chosen based on CIEMAT's expertise in machine design for high-speed applications. This power level was considered suitable for unitary modules and aligns with the power profiles provided by Balearia, which outlined the vessel's peak power requirements during port maneuvers, specifically docking and departure phases. These are periods of high power demand, and the KESS ensures that the energy demands are met without over-relying on diesel engines, thus improving fuel efficiency and reducing emissions.

Among the electrical machines suitable for this system, the Switched Reluctance Machine (SRM) was selected due to its superior performance characteristics. SRMs have lower losses in no-load conditions, no demagnetization issues at high temperatures (as found in permanent magnet machines), and are more cost-effective, avoiding the use of rare earth materials. A 6/4 configuration of the SRM was chosen, as it minimizes torque ripple and is suitable for high-speed operations, making it an ideal candidate for kinetic energy storage in the KESS.

The SRM requires the use of power electronics to manage the sequential switching of its phases. The machine operates by energizing coils in each phase, generating magnetic forces that rotate the rotor to a position of maximum alignment. Once alignment is achieved, the system de-energizes the current phase and energizes the next, creating continuous rotation

and allowing for efficient energy transfer between the rotating flywheel and the vessel's power grid.

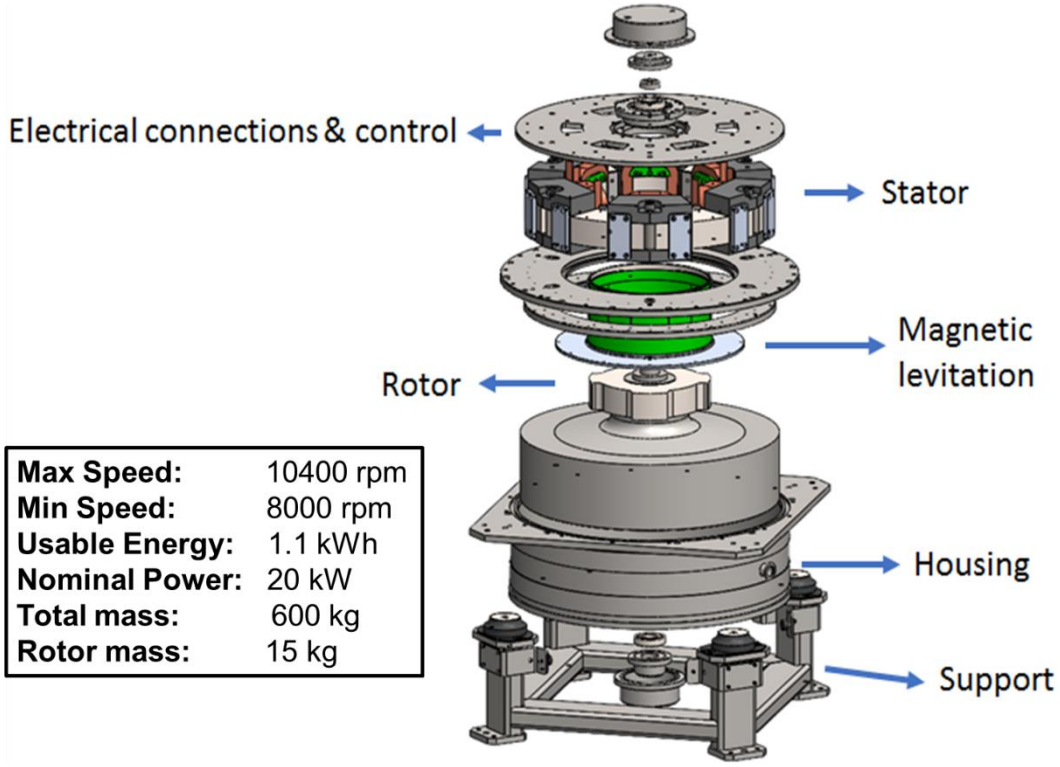


Figure 1.7 - KESS 3D.

The energy stored in the KESS flywheel is based on the inertia of the rotating mass and the square of its rotational speed. For this project, a solid high-strength steel cylinder was selected as the flywheel, capable of operating at speeds ranging from 8000 to 10,400 rpm. This rotational speed range provides a total energy storage capacity of approximately 1.1 kWh, ensuring that the system can meet the vessel's short-term power demands during critical operations.

1.4.3.2 Superconducting Magnetic Energy Storage (SMES)

The SMES system is a critical part of the FRESS, designed to store energy in the magnetic field generated by a direct current (DC) flowing through a superconducting coil according to the expression $E = \frac{1}{2}LI^2$, where L is the inductive value of the coil and I is the RMS value of the current flowing through it. The system includes three main components: the superconducting magnet, the cooling system, and the power conditioning system (PCS). The superconducting coil is made of Second Generation High-Temperature Superconductor, better known through its acronym 2G HTS, tape and operates at extremely low temperatures,

facilitated by a cryogenic cooling system, typically between 4.2K and 20K. This enables the coil to achieve zero resistance, allowing it to store energy with minimal losses.

The coil's geometry, particularly the number of turns and the separation between them, significantly affects the SMES's energy storage capability. The solenoidal coil configuration chosen for the Poseidon project consists of 12 double pancakes with a total of 144 turns per coil, yielding an inductance of 1.68 H and a nominal current of 457 A at 4.2K. This design results in an energy storage capacity of 275 kJ. The system optimization involved fine-tuning the separation between coils to maximize energy density while keeping the overall size within the physical constraints of marine applications.

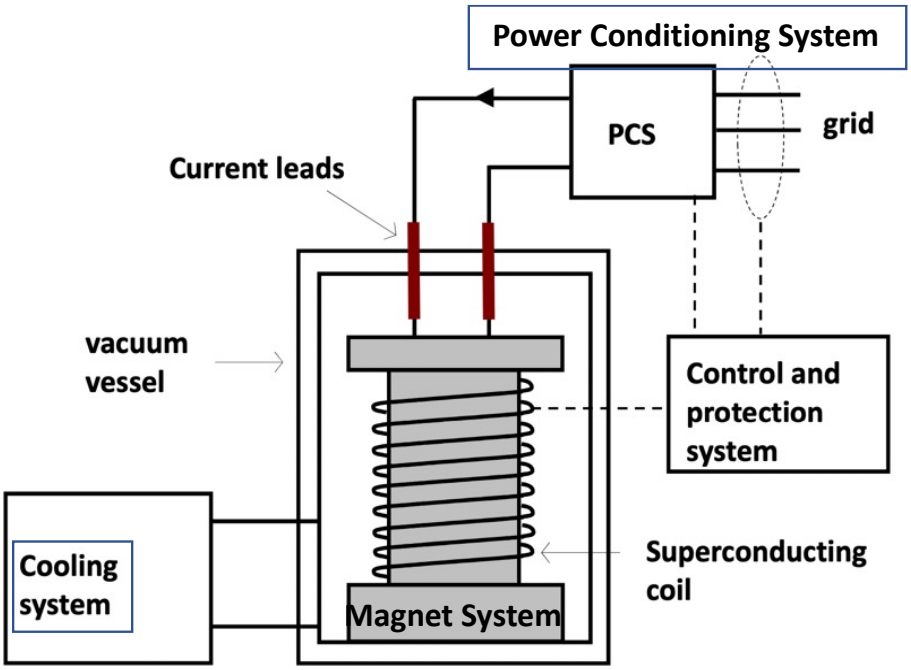


Figure 1.8 - SMES block scheme.

For cooling, a flow refrigeration system using forced helium gas was selected, as it offers cost-effectiveness, compactness, and reliable performance over a broad range of operating temperatures. This cooling system, referred to as the Cryogenic Supply System (CSS), ensures the superconducting coil maintains its critical low temperature, thereby enabling efficient energy storage.

The Power Conditioning System (PCS), which connects the SMES to the vessel's power grid, is based on a Voltage Source Converter (VSC) topology. This allows for the exchange of power between the grid and the SMES in all four quadrants. The PCS features a grid-side inverter and a DC-DC chopper, controlling the voltage across the DC-link capacitor to

regulate energy flow. This configuration helps maintain moderate AC losses and Total Harmonic Distortion (THD), ensuring the system operates efficiently and safely within the vessel's power grid.

1.4.3.3 Electrostatic Energy Storage System (EESS)

The EESS, based on supercapacitors, plays a crucial role in the FRESS by delivering rapid energy bursts for short-duration power demands. The design and manufacturing of this system will be described more in detail in the next chapter since this activity has been my main contribution to the Poseidon project.

1.4.4 EESS Design

The EESS for the Poseidon project was designed based on a simulation model developed using PLECS software by Plexim. The general schematic of the system, highlighting the main components, is shown in Figure 1.9.

1.4.4.1 Simulation model

Starting from the left of the diagram shown in Figure 1.9 , the ferry's common DC bus is represented by an ideal DC voltage source with a resistor in series (depicted in brown). Connected directly to this DC bus is the bidirectional DC/DC converter (in blue). Downstream of the converter is a filtering stage comprising three inductors, one for each leg of the converter (highlighted in red). This is followed by a filter capacitor with a parallel damping branch (in orange) and a second filter inductor (in purple). Finally, downstream of the filtering stage is the supercapacitor (SC) bank (in green).

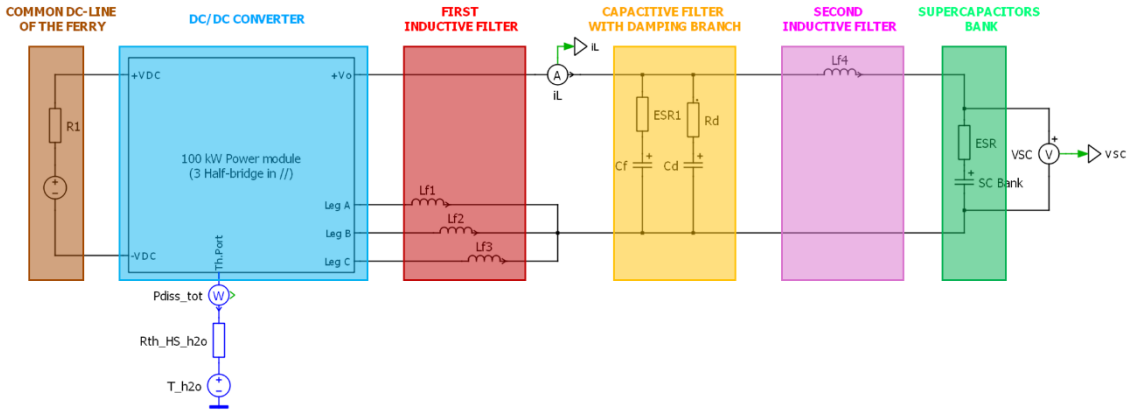


Figure 1.9 – General scheme of the model.

The initial step in the design was to size the SC bank appropriately. The minimum goal for the EESS was to design an SC bank that, at its End of Life (EOL), is capable of providing 2.5 MJ of energy to the common DC bus, with a maximum peak power of 100 kW.

The fundamental equation relating the energy delivered $E_{delivered}$ to the capacitance C of the bank is:

$$E_{delivered} = \frac{1}{2}\, C\, (V_{top}^2 - V_{bottom}^2). \tag{1.1}$$

To determine the total capacitance required, it is necessary first to define the maximum voltage V_{top} at which the bank is fully charged and the minimum residual voltage V_{bottom} at the end of the energy transfer.

Considering that the SC bank's voltage can be either the input or output voltage of the bidirectional DC/DC converter, and that the common DC bus voltage is 850 V, it is advantageous to set V_{top} lower than 850 V. This ensures that the bidirectional converter will always operate as a boost converter during the discharge of the bank towards the DC bus and as a buck converter during the recharge stage. Setting V_{top} higher than 850 V would necessitate the converter to switch modes during charging or discharging, complicating the control strategy.

Therefore, V_{top} for the SC bank was set to 750 V.

For V_{bottom}, it is important to note that supercapacitors release approximately 75% of their total stored energy when discharging from 100% to 50% of their State of Charge (SoC). Discharging the SCs below 40% of their nominal peak voltage is not practical and can be risky, considering that the lower the voltage the higher is the current needed to satisfy the power demand, jeopardizing the life of the semiconductors. Thus, V_{bottom} should not be lower than 300 V.

With V_{top} = 750 V and V_{bottom} = 300 V, the total capacitance of the SC bank can be calculated by rearranging (1.1):

$$C = \frac{2 \cdot E_{delivered}}{(V_{top}^2 - V_{bottom}^2)} = \frac{2 \cdot 3 \cdot 10^6}{(750^2 - 300^2)} = \ 12.7\ [F]. \tag{1.2}$$

This value represents the minimum EOL capacitance required for the SC bank.

The DC/DC converter features three IGBT legs and is configured as a chopper. All legs are driven synchronously to ensure proper current sharing among them. Since the peak

voltage of the SC bank is always lower than that of the DC bus, the DC/DC converter operates as a buck converter during the charging stage and as a boost converter when transferring energy from the SC bank to the DC bus.

The filtering stage is critical because supercapacitors are sensitive to frequencies above 100 Hz. The three inductors placed at the output of the converter provide initial filtering by smoothing the high-frequency components of the current resulting from the converter's switching actions. Downstream of the common point of these inductors, there are three parallel branches:

1. The filter capacitor C_{filter}
2. The damping branch
3. A series combination of the second filter inductor L_{filter} and the SC bank

In Figure 1.10, the damping branch is neglected for simplification, as its impedance is typically one or two orders of magnitude higher than the other two branches. The design goal is to size these two branches such that, for frequencies above approximately 100 Hz, the impedance of the filtering branch $Z_{filterbranch}$ is much lower than that of the SC bank branch $Z_{SCbranch}$, while the opposite holds true at low frequencies.

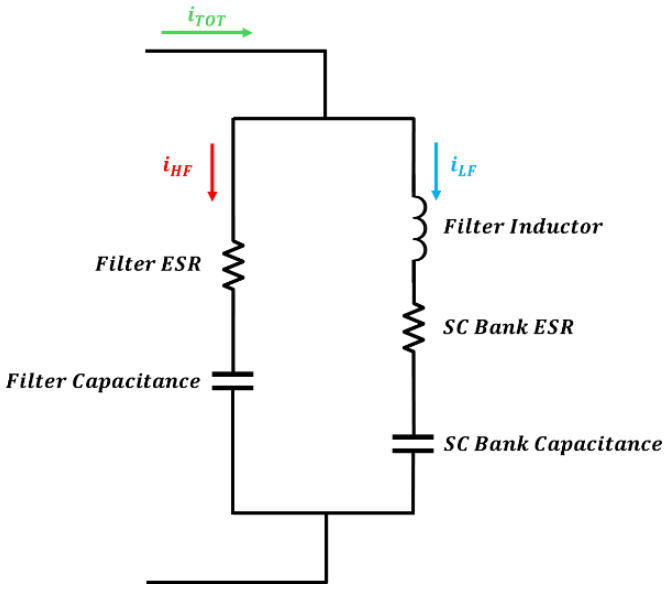


Figure 1.10 – Filter diagram.

The equivalent impedances of the two branches can be computed as:

- Filter branch impedance:

$$Z_{filterbranch} = \frac{1}{j\omega C_{filter}} + R_{ESRfilter} \tag{1.3}$$

- SC bank branch impedance:

$$Z_{SCbranch} = j\omega L_{filter} + \frac{1}{j\omega C_{SCbank}} + R_{ESRbank} \tag{1.4}$$

where:

$\omega = 2\pi f$;

f is the frequency;

R_{ESR} is the Equivalent Series Resistance (intrinsic resistance of each component).

Then, the dimensional constraint becomes:

$$Z_{filterbranch} \leq Z_{SCbranch} \qquad for \quad f \geq 100\ Hz\,. \tag{1.5}$$

This ensures that high-frequency ripple currents predominantly flow through the filter capacitor rather than the SC bank, thus reducing stress on the supercapacitors.

Figure 1.11 illustrates the control logic blocks used in the system. The control implemented takes in input a Power profile reference, the SC voltage measurement and the total current measured on the DC/DC converter.

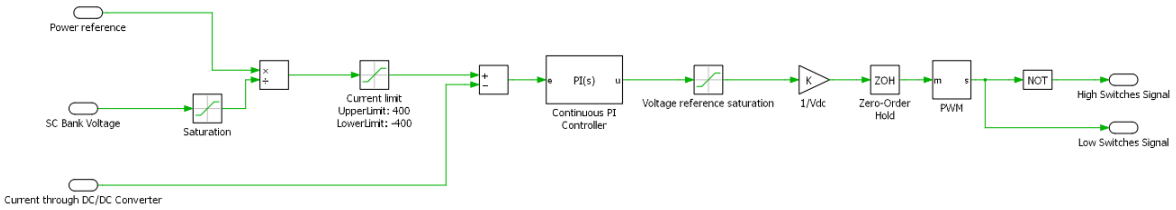


Figure 1.11 – Control blocks.

The current converter reference is generated through the power reference and the measured SC voltage, then it is compared to the measured converter current, and the error is regulated through a PI regulator, the output of the regulator, scaled, is used as modulating signal for the PWM block with switching frequency of 5kHz, that will generate the proper driving signals for the converter's IGBTs.

The main outcomes of the simulation are presented in Figure 1.12. The top plot shows the comparison between the converter current and the current flowing in the SC Bank. As

highlighted in Figure 1.13, the current in the SC branch is much smoother, thanks to the action of the filters. The middle plot shows the common DC line voltage (in green), the voltage across the SC bank (in red), the higher voltage threshold (in blue), the lower voltage threshold (in yellow) and the SoC of the SC bank (in purple). The bottom plot displays the power reference (in red) and the actual power delivered (in green).

In the simulated scenario, a conservative approach was taken by assuming that the power demand is always at the peak value. The peak power was set to 120 kW, which is 20% higher than the minimum design goal of 100 kW. During the initial few seconds, the actual power increases linearly due to a current limitation imposed to protect the IGBTs. Once the current stabilizes below the limit of 400 A, the converter accurately tracks the power reference.

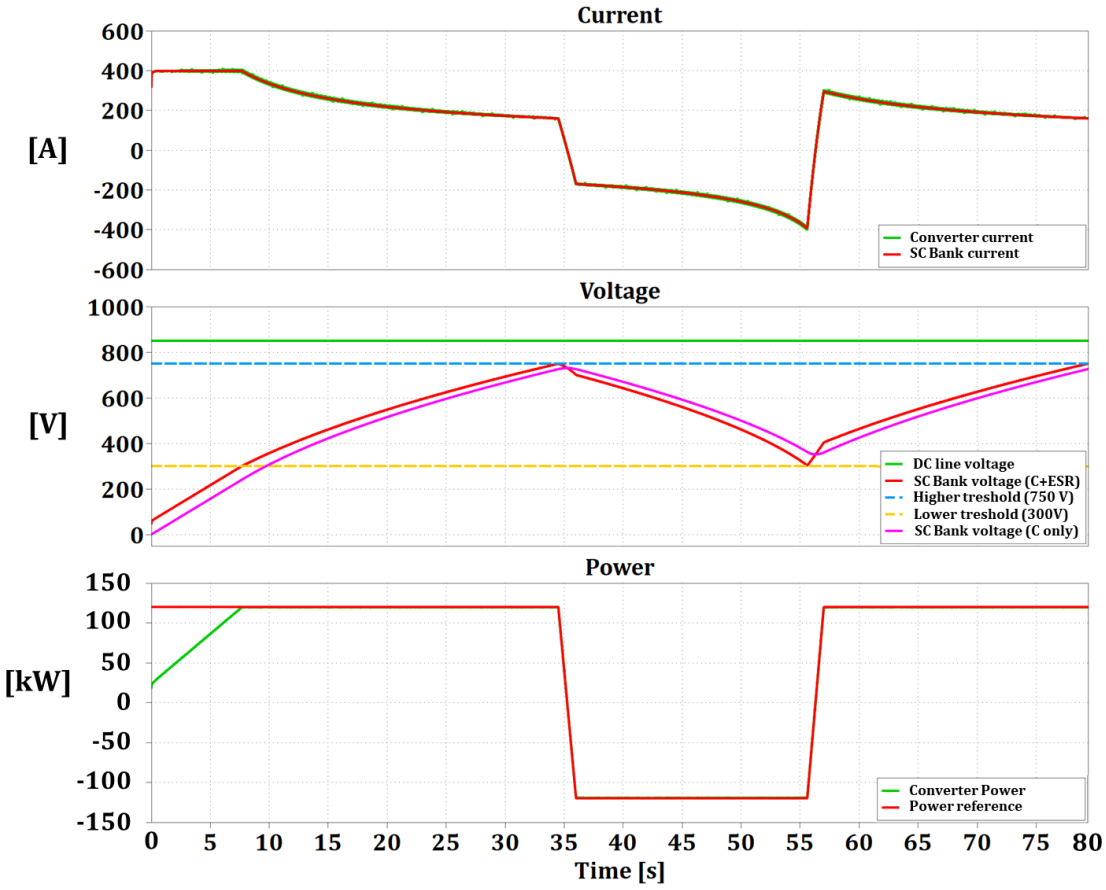


Figure 1.12 – Main Outcomes.

Figure 1.13 shows in detail the comparison between the current flowing through the converter and the one through the SC bank. It is evident that a high-frequency ripple current with a peak-to-peak amplitude up to 25 A is present in the converter current (the cumulative current flowing through the three filter inductors at the output of the converter) while it is absent on

the SC bank, this is due to the action of the filters. This effectively reduces the stress on the supercapacitors, enhancing their lifespan.

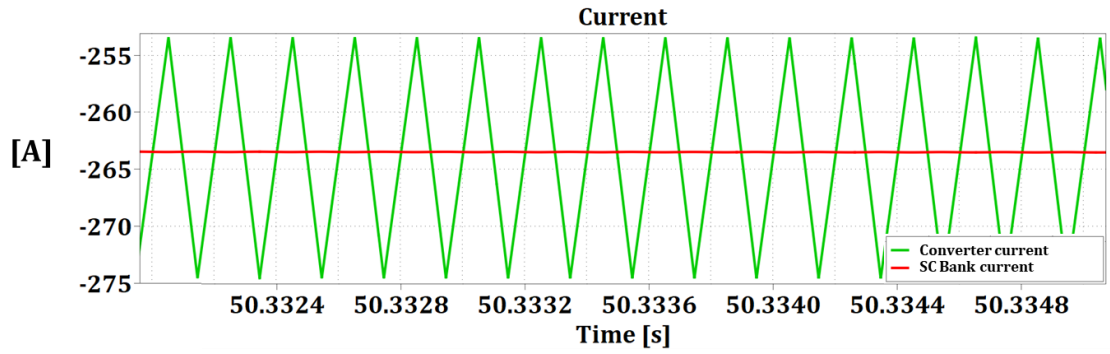


Figure 1.13 – Comparison between converter current and SC Bank current.

Finally, Figure 1.14 depicts the energy stored in the SC bank. Starting from 0 MJ (fully discharged) it reaches 3.6 MJ once the charge is completed, then, during the discharge, 3 MJ are released from 750 V to 300 V.

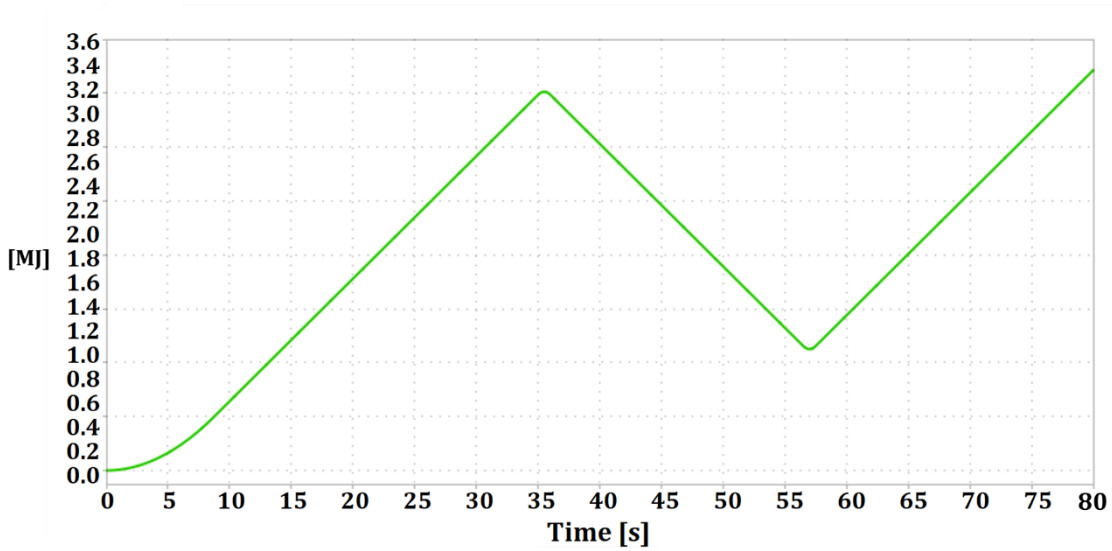


Figure 1.14 – Energy stored in the EESS.

1.4.4.2 Selected Components

The component selection started with a proper IGBT model. Considering the voltage level of the common DC line (850 V), the selected IGBT module was the MITSUBISHI CM600DX-34T. This component has a voltage rating of 1700 V that makes it suitable for this application. Furthermore, the current rating (600 A continuous current) ensures a good safety margin since it should carry current not higher than 133 A at 5kHz.

DX

Collector current I_C ..... **600** A
Collector-emitter voltage V_{CES} ..... **1700** V
Maximum junction temperature T_{vjmax} ..... **175** °C

- Flat base type
- Copper base plate (Nickel-plating)
- RoHS Directive compliant
- Tin-plating pin terminals

Figure 1.15 – Main data of Mitsubishi CM600DX-34T.

In order to validate this choice, the thermal model of the component has been built on PLECS and has been used to run thermal simulations.

Figure 1.16 and Figure 1.17 show the pictures of the thermal models built for IGBTs and diodes. All curves have been retrieved from the datasheet of the MITSUBISHI CM600DX-34T.

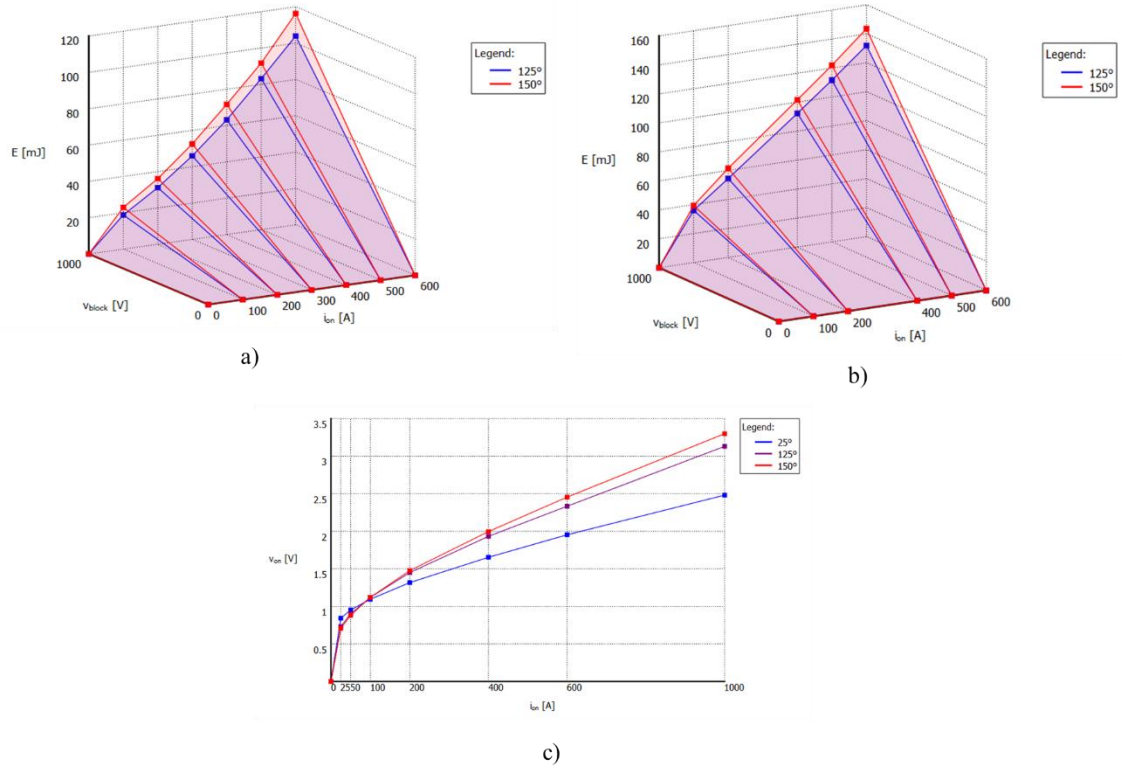
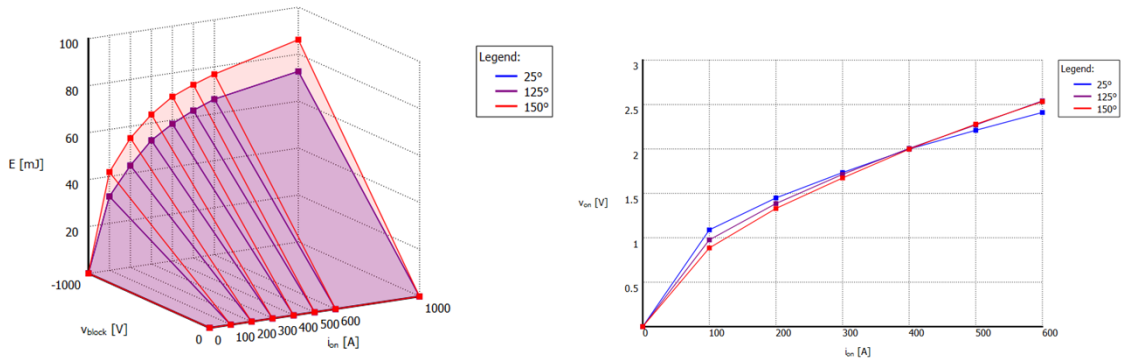


Figure 1.16 – IGBT thermal model CM600DX-34T: a) Turn on Losses; b) Turn off Losses; c) Conduction Losses.



a) b)

Figure 1.17 - Diode thermal model CM600DX-34T: a) turn off losses; b) conduction losses.

Figure 1.18 shows the PLECS thermal network for the thermal simulations.

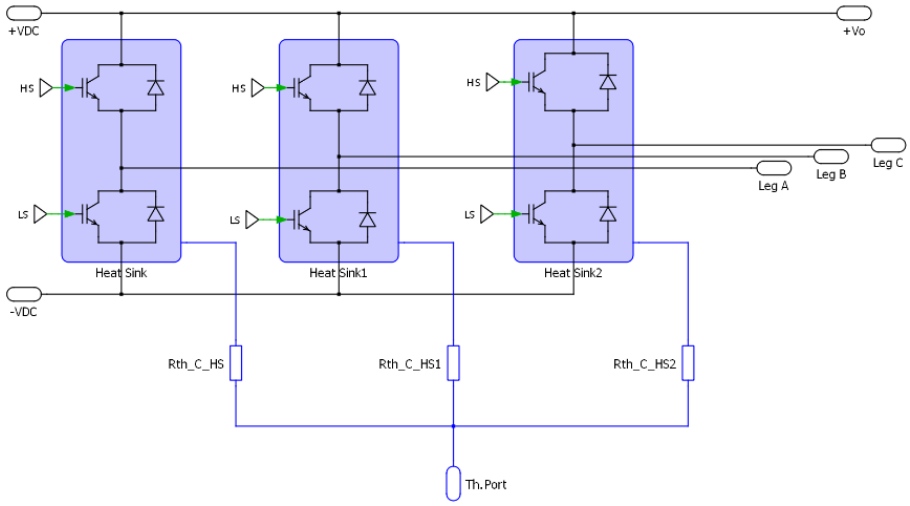


Figure 1.18 – Thermal network built in the simulation model.

The results of the thermal simulations are summarized in Figure 1.19, which shows that the application is safe from the point of view of the temperatures, considering that the maximum temperature reached is 85 °C and it is reached during the interval in which the converter is operating at the maximum current (400 A).

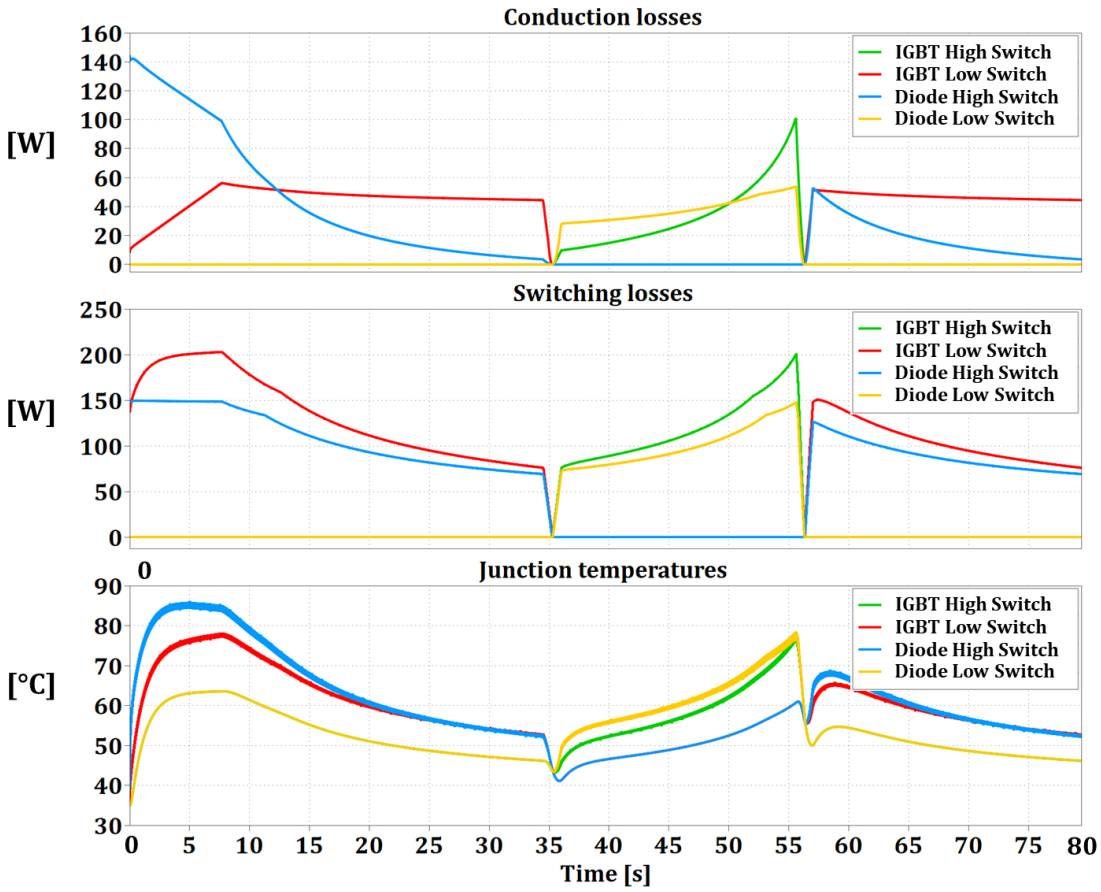


Figure 1.19 – Main outcomes from thermal simulations.

The individual power module (shown in Figure 1.20) is a water-cooled unit provided with IGBTs in the standard 150 x 62 x 17 mm package and completed with IGBT drivers, diagnostic board, bus-bar and local DC-bus film capacitors.

The use of film capacitors also gives a strong contribution to the overall reliability of each module. Moreover, if the module is used as a spare part and is stocked for several years, it does not lose its electrical properties during the stockage period.

The cooling plate of IGBT is realized with copper and stainless steel in contact with water. The capacitors are sized to withstand the ripple current of the IGBT. The power module can be configured to realize different converter topologies and can be equipped with different IGBT and capacitors voltage ratings. For the application presented in this document, the module is configured as half-bridge chopper with three 1700V IGBTs modules in parallel.

The connection between capacitors and semiconductors is made of low inductance laminated busbars.

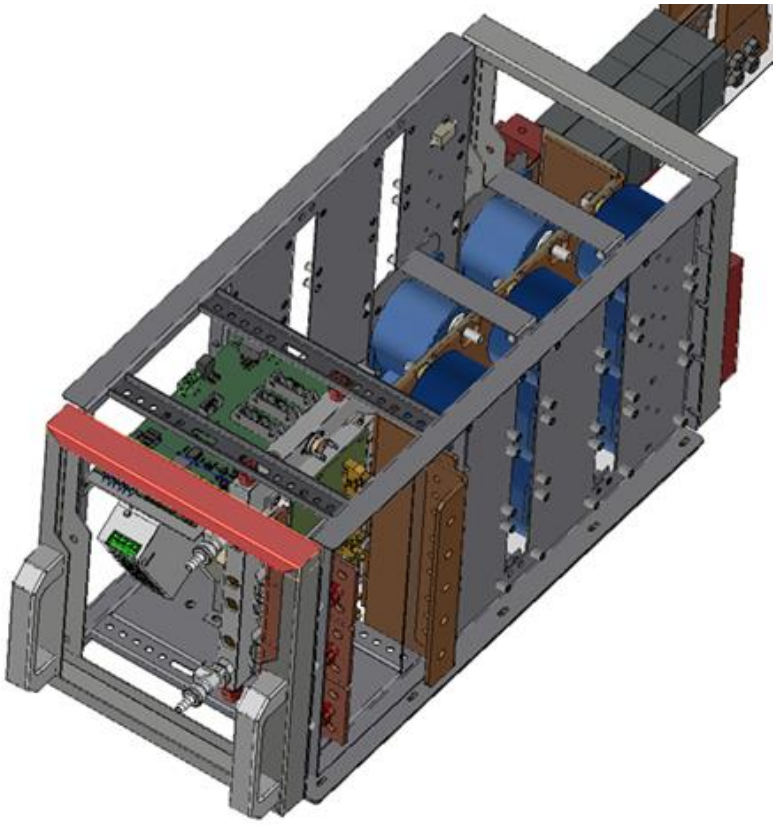


Figure 1.20 – Triumf Generation Power Module (TGPS), designed for a power supply at the TRIUMF Canada's Particle Accelerator Centre.

The IGBT drivers used are the Power Integrations 2SP0115T2A0-17, which are directly soldered to the IGBT. The IGBT switching signals and status feedback signals are provided through optic fibre for improved disturbance immunity.

For the SC module, the selected component was the module CapTop CTM 00165C0 0054V0 NN00, depicted in Figure 1.21. This module is rated at 54 V and 165 F, with the capability to handle peak currents of up to 2000 A for short durations. Each module is built through a series connection of 18 SC cells rated 3V 3000F and has its own Dynamic Cells Balancing (DCB) system, reporting to the String Management Unit (SMU) that exposes the ModbusRTU interface for monitoring. Each string will therefore have one or more Modbus addresses.

The suitable voltage and capacitance ratings of the CapTop SC module, along with its high current handling capacity, align well with the requirements of the application.

To arrange the SC Bank, two paralleled stacks of 15 SC modules each will be placed into a cabinet, giving to the SC bank a total capacitance at the Beginning Of Life (BOL) of 22 F

(that at the EOL will be around 17 F). This gives a considerable margin respect to the minimum capacitance needed computed in (2), allowing the system to transfer the required amount of energy with a reduced voltage jump, that implies reduced peak currents and stress on the components.

Figure 1.21 – CapTop CTM 00165C0 0054V0 NN00 Power Brick.

For what concerns the passive components, the three inductors to be placed one at the output of each converter leg have been sized to have an inductance of 6 mH, a nominal current of 130 A with a ripple superimposed of 13 $A_{pk\text{-}pk}$ at 4 kHz. The second filtering inductor has been sized with an inductance of 540 μH, a nominal current of 350 A and a superimposed ripple of 35 $A_{pk\text{-}pk}$ at 4 kHz. In both cases, the manufacturer is Trasfoproject. Finally, the filter capacitors chosen are the Ducati DCH 85C series, model 416.85.V. 195.x rated 900 V and 4.5 mF. Figure 1.22 shows the picture of the family DCH 85 C. The same component is used for the damping branch, where four capacitors in parallel are in series to a 0.5 Ω resistor.

Figure 1.22 - Ducati DCH 85C series.

1.4.4.3 Control Architecture

The control system is based on CompactRIO (cRIO) architecture made by National Instruments. The model selected for this project is the *cRIO 9036,* a high-performance control system with several industrial I/O modules, extreme ruggedness, and compliance with the majority of industry-standard certifications.

In general, the control system is divided into two main parts:

- *Fast Controller* - managing the control loops and the interfacing with the external control network;
- *Slow Controller* - monitoring the status of the whole system.

Fast controller and slow controller are included in the same system and connected by an Ethernet communication.

In the following paragraphs, the main parts of software and control electronics are presented:

- Fast Controller
- Current sensors & voltage transducers
- Slow control
- Interface with Personnel Protection Interlock System
- Local/Remote Operation
- Operator Interface

The architecture of the cRIO is shown in Figure 1.23. The main software used is LabVIEW, which allows for real-time deployment and distribution of user interface applications for monitoring and controlling the entire system.

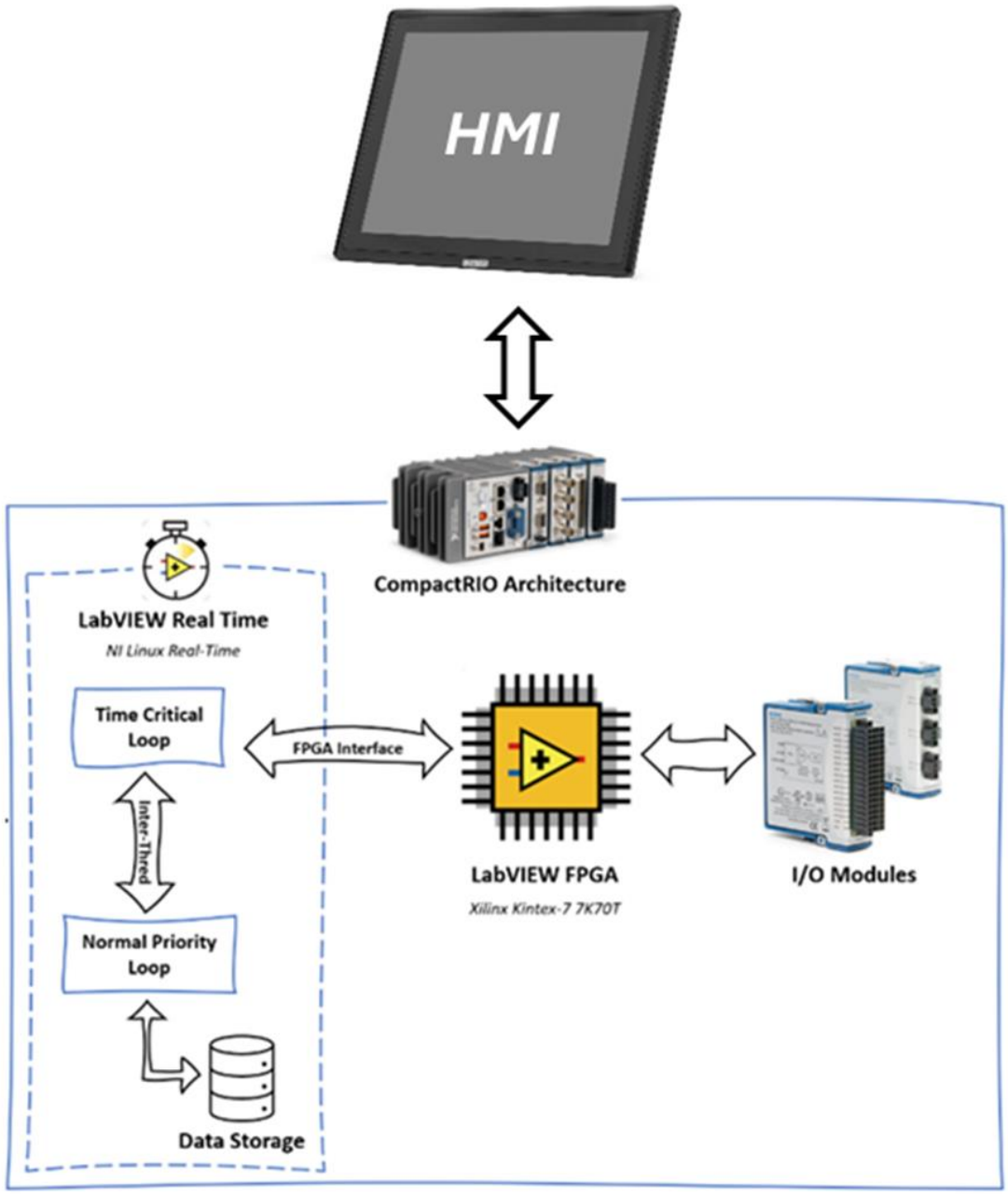


Figure 1.23 – Control architecture based on CompactRIO.

The cRIO is based on two separate units: one for real-time tasks; and the other is the FPGA module for smaller tasks that require high-speed logic and precise timing.

Controller CompactRIO cRIO-9036, 1,33 GHz dual core, 8 slot, FPGA Kintex-7 70T, from -40 °C to 70 °C. The components of the control system are indicated below in the next list.

Controller cRIO 9036: It is a real-time controller with high-performance.

CPU	*Intel Atom E3825*
Cores	*2*
CPU Frequency	*1.33 GHz*
OS	*NI Linux Real-Time (64-bit)*
Ethernet Ports	*2*
RS-232	*1*
RS-485	*1*
USB	*1 Standard B and 2 Standard A*
SSD	*4 GB*
FPGA	*Xilinx Kintex-7 7K70T*

- **Chassis x8**: The chassis contains the FPGA, and each I/O module is connected directly rather than through a bus; this architecture allows for no control latency for system response.
- **I/O Modules**: Several modules have been chosen to fulfil the MEST control requirements; the details are listed below.

1x NI 9201 with Screw Terminals

Voltage range	*+/-10 V*
Sampling rate freq.	*500 kS/s*
Resolution	*12-Bit*
Terminal type	*8-Ch AI Module*

1x NI 9375 with Spring Terminals

Number of Inputs	*16-Ch sinking DI*
Number of Outputs	*16-Ch sourcing DO*
Voltage range	*0 V to 30 V*

Terminal Type	*Screw*

1x NI-9862 C Series CAN Interface Module

Transceiver	*NXP TJA1041AT*
Max baud rate	*1 Mbps*
CAN_H, CAN_L bus lines voltage	*-27 to +40 VDC*
CAN Supply voltage range (V_{SUP})	*+9 to +30 VDC*

1x IRS Optical Interface 2-fold Tx/Rx 10 Mbit/s

Fibre Connection	*Versatile Link*
Data rate	*10 Mbit/s typ.*
Transmitters	*3*
Receivers	*3*

1x TSM-1012 Touch Screen Monitor

LCD Display	305 mm (12 in.) (4:3)
Maximum Resolution	1024 × 768
Brightness (cd/m^2)	600
Contrast Ratio	700:1
LCD Color	16.2 M
Pixel Pitch	0.24 mm × 0.24 mm
Viewing Angle (H-V)	160°/140°
Backlight MTBF	50,000 hours

1.4.4.4 Mechanical Layout

Figure 1.24 shows the layout of the EESS. The storage system is composed of two cabinets (each having dimensions W x D x H 1200 x 800 x 2000 mm). One cabinet houses the SC modules, while inside the other cabinet there are all the other components, including the

TGPS (visible on the bottom of the cabinet), the first filter inductors (depicted as three green parallelepipeds), the second filter inductor (red parallelepiped) the filter capacitors with damping branch (capacitors in orange, and damping resistor in black), the discharge resistor (grey cube on top right) and water chiller (grey parallelepiped mounted on the side panel).

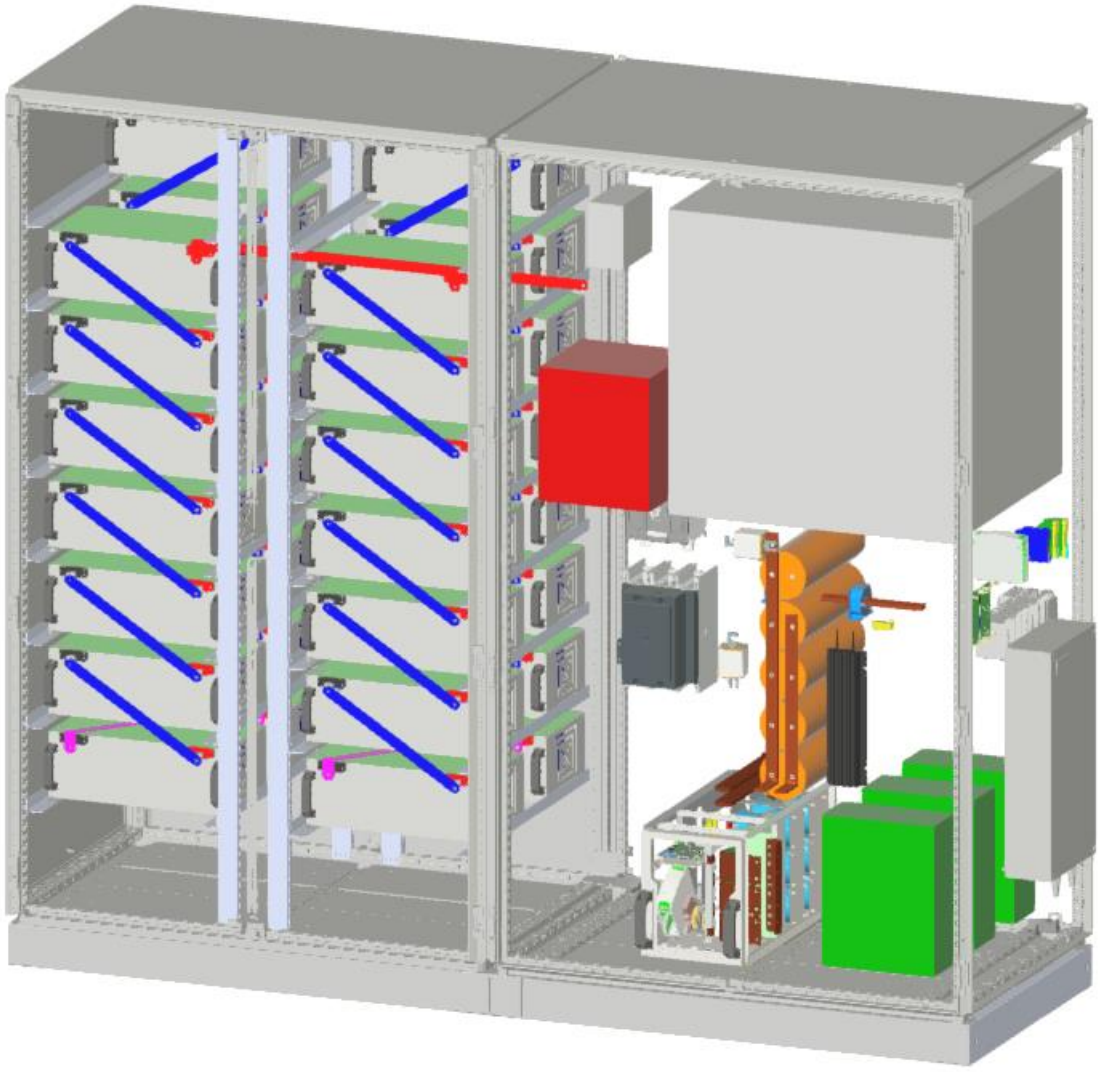


Figure 1.24 – CAD 3D model of the EESS for Poseidon.

1.4.4.5 Summary of the design of the EESS

The system is composed of multiple supercapacitor (SC) modules connected in series, interfaced with an 850V DC line via a bidirectional DC/DC converter. The converter manages the charge and discharge of the SC bank, ensuring voltage oscillations between 750V (fully charged) and 300V (minimum operational voltage), with the system providing a maximum power output of 120 kW when fully charged and a net usable energy of 3 MJ.

The supercapacitors are organized into two paralleled stacks, each containing 15 modules. Every module is composed of several supercapacitor cells connected in series, designed to store and discharge energy efficiently under fluctuating load conditions. The DC/DC converter charges the SC bank up to 750V before operation, while during operation, it modulates the charge/discharge cycle based on the Energy Dispatcher system's power or current reference signals. This ensures that the SC voltage remains within the operational range, preventing excessive discharge that could damage the supercapacitor cells.

a) b) c)

Figure 1.25 - EESS a) Cell b) Module c) Cabinet.

The control system for the EESS is responsible for regulating the current, monitoring the performance of the DC/DC converter, and protecting the SC bank from faults such as voltage inversion. Should the voltage drop too close to zero, a resistor-based dissipation system prevents a sudden voltage drop, protecting the individual SC cells from damage.

Overall, the EESS provides an effective and reliable energy storage solution that supports high-power demands during critical vessel operations such as docking and maneuvering, where rapid energy deployment is essential.

1.4.5 Global thermal simulation model

In the Poseidon project, the company Techno Pro Hispania (TPH) is tasked with developing a unified thermal model that incorporates the simulation models of KESS, SMES, and EESS, which are housed within a 20-foot container. This integrated thermal model,

designed in Modelica (an object-oriented modeling language used for simulating complex multi-domain physical systems), is essential for accurately simulating the thermal dynamics within the container and optimizing the management of heat generated by these systems.

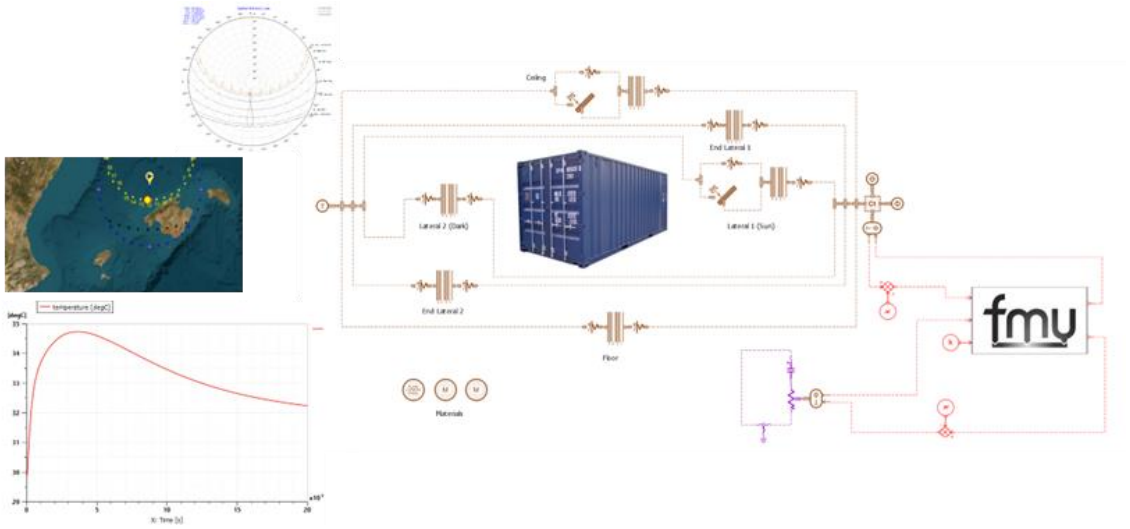


Figure 1.26 – Thermal model of the FRESS.

TPH's process begins by exporting detailed simulation models of the individual ESS units and incorporating them into a global thermal framework using AMESIM. The approach focuses on simplifying model complexity through reduced-order models (ROM), while still maintaining essential physical behaviors. The thermal model accounts for multiple factors, including heat transfer mechanisms (convection and radiation), ship movement-induced mechanical stresses, and the container's HVAC system.

A key aspect of this work involves validating newly developed components such as a ceramic disk resistor, which simulates heat absorption via the Joule effect. This resistor model demonstrates how the thermal load behaves under various conditions, such as peak power discharge, and how it influences the cooling requirements within the container. The model ensures that the heat transfer coefficients and temperature profiles are accurate for real-world applications, providing reliable insights into the performance and safety of the ESS.

Through this integrated thermal model, TPH is able to predict temperature distribution and identify potential thermal hotspots, ensuring that all ESS operate within safe temperature limits. This model aids in optimizing cooling strategies, enhancing the overall efficiency and reliability of the containerized ESS in the maritime environment.

1.4.6 Containerized Solution

After the completion and individual testing of all systems, the next step involves integrating them into a unified infrastructure. This integration is planned to be housed within a 20-foot maritime container. The containerized solution serves multiple purposes: it protects the equipment from the harsh sea environment and provides a structural platform that ensures quick and easy embarkation and connection to the ship's systems.

The primary objective of incorporating a set of fast-response energy storage devices is to align more effectively the power and energy requirements of the onboard electrical load with the capabilities of the energy storage system. By distributing the power demand across multiple storage devices, the system aims to reduce battery aging and enhance the overall efficiency of power delivery on the vessel.

The power contribution from each subsystem is managed by a control optimization algorithm. This algorithm considers real-time measurements of operational variables from the different storage systems, including temperature, current, and state of charge (SoC) of the three fast-response devices. Testing and validating this control algorithm is a core mission of the integration phase, ensuring that the energy distribution among the storage devices optimizes performance and longevity.

In this specific implementation, directly connecting the containerized solution to the ship's main electrical system presents challenges. Modifying the ship's electrical infrastructure is beyond the scope of this project. To circumvent this, the container will draw power from a dedicated diesel generator onboard the ship to charge the FRESS. The discharge of the FRESS is managed via a heater installed within the container. This heater dissipates power in a controlled manner, allowing the system to simulate real-world power consumption profiles as regulated by the control system.

Figure 1.27 presents a CAD model of the FRESS system within the containerized solution. The illustration showcases the layout and integration of the components, highlighting how the systems are organized to function cohesively within the confined space of the container.

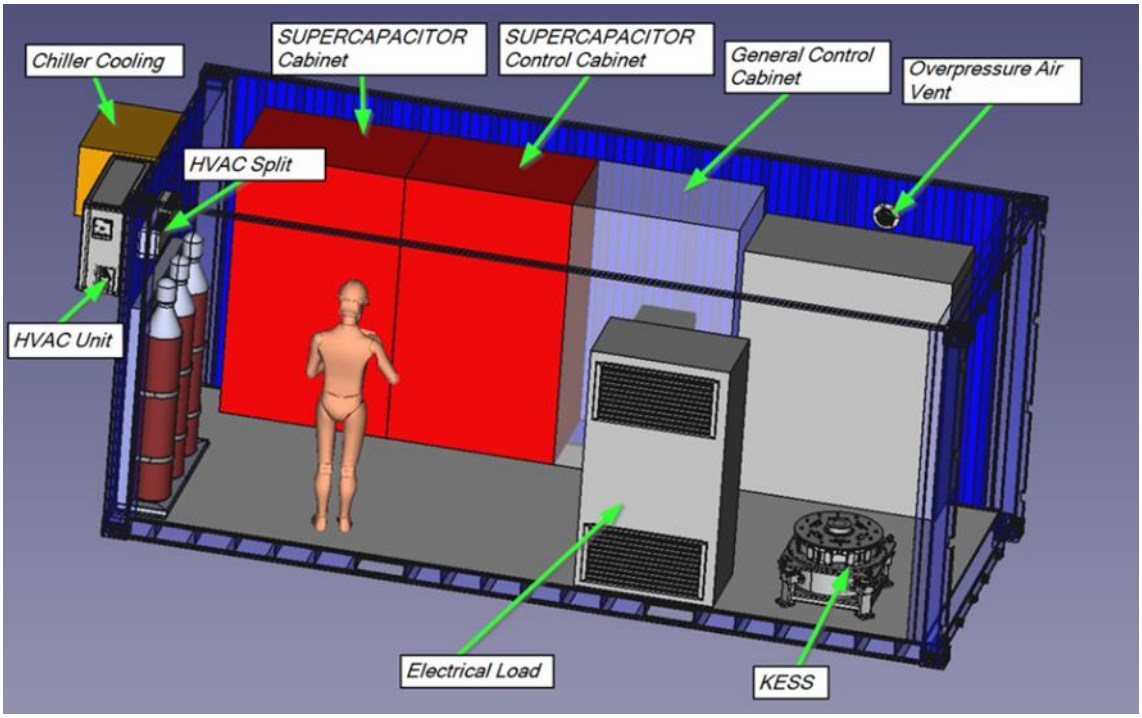


Figure 1.27 - Arrangement of the various ESS inside the container.

This integrated approach not only facilitates testing in a controlled environment but also demonstrates the feasibility of deploying advanced energy storage solutions on maritime vessels without necessitating extensive modifications to existing ship infrastructure. The containerized system can be seen as a modular and scalable solution, potentially applicable to a wide range of ships seeking to reduce greenhouse gas emissions through improved energy management.

1.5 Conclusions

This chapter has outlined the design and development of a Fast-Response Energy Storage System (FRESS) for marine applications, focusing on reducing greenhouse gas emissions and enhancing operational efficiency in the maritime industry. The Poseidon project integrates three distinct energy storage technologies, KESS, SMES, and EESS, each selected for their ability to meet the fast-response and high-power demands typically encountered during critical maritime operations, such as port maneuvers and dynamic positioning.

The project's ambition is to facilitate the cost-effective deployment of ESSs in the maritime sector, enabling a swift transition to more efficient and sustainable modes of transport. By investigating the applicability of FRESS across various waterborne segments and developing an onboard demonstrator, the Poseidon project plays a crucial role in

validating these technologies in a relevant marine environment. This validation process includes a series of scheduled tests, starting with individual functional testing, followed by integrated system testing at CIEMAT laboratories in Madrid. By the end of 2025, the final phase will involve testing the fully integrated FRESS on a Balearia ferry, marking a key milestone in the project.

The primary objective of FRESS is to minimize or eliminate the use of diesel power units during frequent but short-duration operations, such as docking and undocking maneuvers. These storage systems, designed for fast response, high power output, and short energy bursts, are ideally suited to cover these specific energy demands. The power profiles previously analyzed show that KESS, SMES, and EESS can effectively handle the high peak power required during these operations. However, to ensure comprehensive coverage of the energy profile, an additional higher-energy storage system, such as batteries, may be necessary. Batteries could provide a more stable and sustained power output, while the fast-response technologies would manage the peak power demands, thereby extending battery life and optimizing overall system efficiency.

As the project progresses, economic evaluations are conducted to assess the viability of different storage configurations, considering factors such as cost, performance, and the impact on battery degradation over time. These analyses will be crucial for selecting the most suitable combination of energy storage technologies, ensuring a balance between technical performance and economic feasibility.

The containerized solution developed for the ESS not only protects the systems from harsh marine environments but also offers a modular, scalable platform for integration into various types of vessels. This flexible approach is key to achieving widespread adoption of FRESS and similar technologies in the maritime sector, ultimately supporting the industry's broader goals of reducing emissions and improving fuel efficiency. By the conclusion of the Poseidon project, the aim is to demonstrate the effectiveness of these integrated systems in real-world maritime operations, paving the way for more sustainable and resilient energy practices across the industry.

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Chapter 2

OPTIMIZING POWER SUPPLIES FOR PF COILS

2.1 Introduction

One of the main areas in which OCEM Power Electronics is active is the plasma physics, especially in connection with the field of controlled nuclear fusion; in this context, it emerged the possibility to join a collaboration with the ENEA Research Center in Frascati and the University of Rome Tor Vergata, regarding the study for a preliminary optimized design for some power supplies needed in the Divertor Tokamak Test (DTT) facility, under construction in Frascati, Italy.

This study eventually led to the publication of a paper [18], and this section of the thesis will be entirely dedicated to this study.

Controlled nuclear fusion is increasingly gaining importance as is widely considered to be one of the most promising options for generating clean, safe, and programmable energy on a large scale, as evidenced by increasing investments from both public institutions and private companies [19],[18],[20],[21]. Among the various approaches to achieve this goal, tokamaks stand out as one of the most promising solutions for leveraging nuclear fusion to produce controllable and safe energy. A significant challenge in the practical application of tokamaks lies in managing the power flow required to initiate and sustain the fusion process.

One area of considerable interest in this field is the optimization of power supplies, which are essential for the reliable and efficient operation of the many subsystems within a tokamak [22]. Power supply optimization focuses on enhancing the performance and reducing the size of energy storage and conversion systems, which are critical for managing the variable and high power demands of nuclear fusion processes. Given the complex dynamics involved in controlling the magnetic fields and plasma behavior, achieving a balance between power supply efficiency and physical footprint is particularly challenging. This makes the development of new strategies to manage energy storage an important area of ongoing research.

In the specific case of tokamaks, the Poloidal Field (PF) coils play a crucial role in shaping and stabilizing the plasma [23]. These coils generate the poloidal component of the magnetic field, which circulates in planes perpendicular to the central axis of the tokamak, ensuring

precise control of the plasma configuration. Optimizing the power supplies for the PF coils, which must accommodate high power peaks and variable demands, is the key focus of this study.

The proposed approach involves sharing the DC storage among different coil circuits, supported by new analytical formulas and a specialized circuit model developed for this purpose. The results demonstrate that this method and the associated algorithms can significantly reduce the overall size of the storage system and the power exchange with the grid, thereby contributing practically to the feasibility and efficiency of nuclear fusion systems.

A tokamak confines extremely hot plasma, where fusion reactions occur, using strong magnetic fields generated by controlled currents flowing through coils. These coils are oriented and supplied independently to control the main components of the magnetic field, classified in tokamak reference coordinates as toroidal (TF) or poloidal (PF) fields [23].

A trend in current and proposed tokamaks is the use of superconducting materials in TF and PF coils, operating at increasingly higher currents. A critical issue for the practical use of tokamaks as energy sources is the optimization of the power and energy required in the coils to initiate and maintain the desired plasma configurations. While the TF remains practically constant in a tokamak, the PF must vary according to a predefined "scenario", resulting in a variable power flow between each coil and its power supply. Traditional power supply systems, implemented using thyristor-based AC/DC converters, introduce significant reactive power into external grids, leading to power demands in the order of 1 GVA from the grid. Although the total energy produced by the tokamak could offset these demands, sustaining the technical and economic effectiveness of the process is challenging. Moreover, the massive and variable power flow at the interconnection nodes can pose problems for the external electrical grid.

The voltage levels and the limited number of variations required in TF coils allow for some power supply optimizations. For instance, traditional power supplies could be replaced by contactless systems, known as flux pumps, which minimize losses in superconducting circuits under steady-state conditions [24]. For PF power supplies, an identified improvement is the introduction of an energy buffer to limit power exchange between the coils and the external grid. Various topologies and technologies are possible in principle, however, the

most promising solution is to incorporate the energy storage in the DC link of the PF power supplies, and sometimes other coils.

The challenges described here are commonly encountered across diverse energy sources and power conversion applications, where energy storage is vital to maintaining system stability and performance, and its importance is continuously growing. However, PF power supplies possess distinct characteristics: despite the average energy and duty cycles often being relatively low (especially in current experimental setups), they involve extremely high power peaks and require numerous rapid charge and discharge operations daily. This combination of factors points to supercapacitors (SCs), known for their high power density and swift charging and discharging abilities, as potentially optimal energy storage solutions [25]. Consequently, SC banks have been incorporated to support tokamak power supplies, specifically within the DC links connecting the AC/DC and DC/DC converter stages.

Once this reference solution is determined, the primary design challenge is to reduce the physical footprint of these DC storage systems without compromising their functional integrity and reliability. Given that SC banks represent the largest and most costly components of a new power supply system, oversizing them could negate their intended benefits.

It is crucial to recognize that effective optimization requires a departure from the standard operation of DC links in power electronics, where a relatively constant voltage is typically maintained. In this case, the voltage across SC banks must fluctuate between minimum values necessary for intended operational scenarios and safe thresholds for the hardware.

Due to the complex, time-variable interactions among circuit parameters and their interdependence with other tokamak elements, an entirely analytical approach to design and optimization is unfeasible. Nonetheless, models and equations have been developed to establish an initial range for the process and to incorporate all tokamak components in a circuit model to validate the design. Since DC link optimization is the primary focus, the power supply circuits rely on a single H-bridge converter.

This chapter demonstrates that for superconducting inductive loads, SCs offer more benefits than might be inferred from a conventional analysis using the Ragone plot. The optimization strategy can capitalize on the specific characteristics and operational principles of PF coils. Although the explicit optimization of other coil types, such as those inducing poloidal fields but serving different functions, including the Vertical Stabilization (VS),

Central Solenoid (CS), fast Radial Control (RC), and Divertor (DIV) coils, falls outside the chapter's scope.

Thus, although the proposed approach has broad applicability to various tokamaks and other nuclear fusion facilities, this analysis uses real-world examples. The focus is on the DTT facility 189[27]. The DTT features six superconducting PF coils, a standard element in tokamaks, alongside all other coil types mentioned (CS, VS/RC, DIV).

This study examines novel approaches to minimizing the volume of the DC storage system in PF power supply converters by utilizing SCs configured in both series and parallel arrangements. For the first time, the proposed solution involves sharing the DC storage stage across pairs of power supplies. This strategy, validated through simulation, leverages complementary energy demand profiles in certain coil pairs, enabling a more efficient and compact design. Findings suggest that this approach not only reduces the overall size of the DC storage stage but also improves performance, efficiency, and cost-effectiveness. Optimizing power exchange with the grid can help alleviate other power quality challenges faced by tokamaks, including reactive power, harmonics, flicker, and oscillations. Specifically, the substantial power flow variations that could impact the viability of tokamaks as energy sources may be managed internally[22].

On the other hand, this chapter will address some limitations and challenges inherent to this approach, such as the difficulties in optimizing available power, energy, and voltage.

The implications of this research are significant for various applications in energy storage and conversion technologies, underscoring the role of innovative design in addressing the complex demands of advanced energy systems.

2.2 Role and Operation of Poloidal Field Coils in Tokamaks

2.2.1 Overview of Tokamak Magnetic Systems

A tokamak is a complex apparatus engineered to confine and regulate high-temperature plasma through magnetic fields, with the goal of sustaining nuclear fusion reactions[23]. The magnetic system of a tokamak is illustrated schematically in Figure 2.1. Within this system, PF coils are essential for shaping and controlling the plasma, necessitating highly responsive and precise power supply systems [26].

At the heart of the tokamak lies a toroidal (doughnut-shaped) chamber where fusion reactions occur. Magnetic coils positioned around this chamber help establish the stable magnetic field configuration required for plasma confinement. The TF coils generate a continuous magnetic field around the torus, serving as the primary confinement force. Meanwhile, the stability and specific shape of the plasma are primarily governed by the PF coils. These coils, arranged in vertical and horizontal loops around the torus, allow for control over the cross-sectional shape and positioning of the plasma.

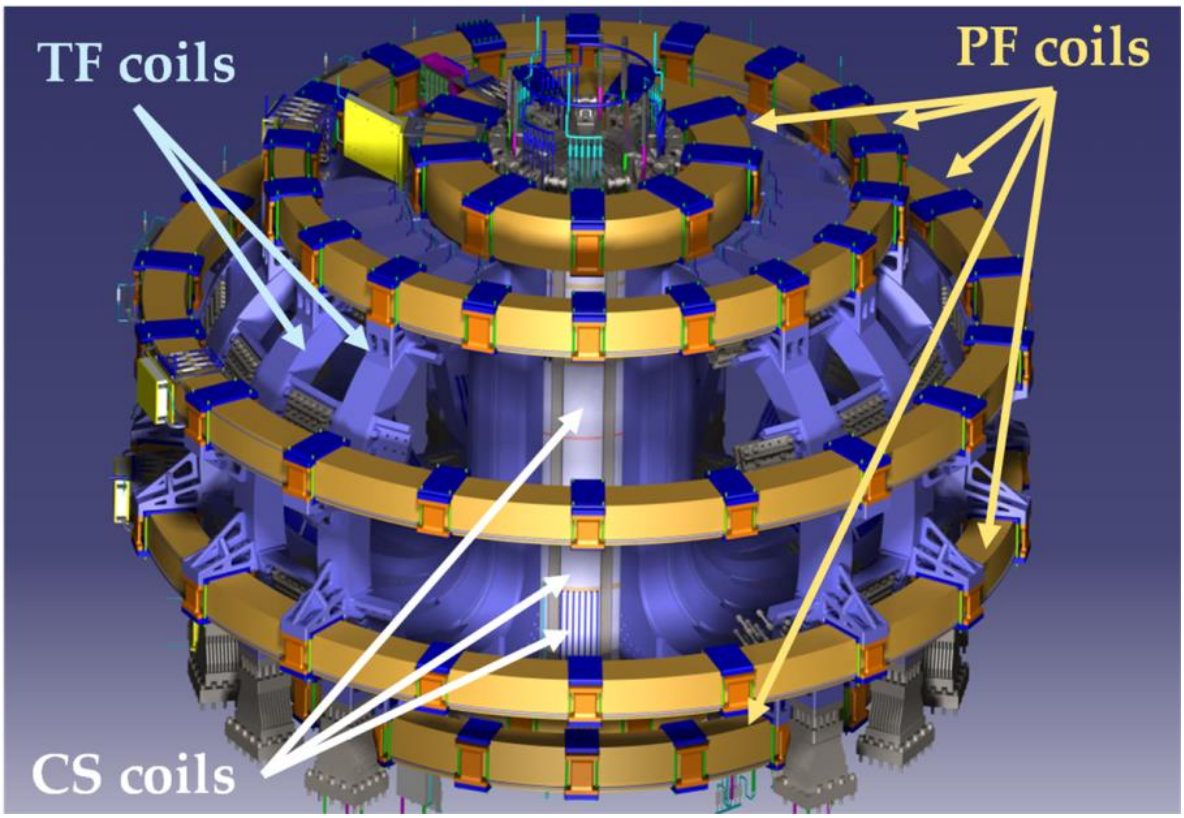

Figure 2.1 - Basic structure of a tokamak (DTT) emphasizing the magnetic systems.

PF coils are fundamental for tokamak operation, as they dynamically adjust the plasma's shape and stability. To achieve this, the PF coils must produce highly variable current profiles, reaching peaks of tens of kiloamperes, and manage voltage profiles that span several kilovolts. The ability to quickly and accurately modulate these high current and voltage levels is crucial for maintaining the desired plasma configuration and ensuring the fusion process remains stable overall [23].

2.2.2 Current and Voltage Profiles for PF Coils

Forecasting tokamak operations is a complex, multidisciplinary task that involves magnetohydrodynamic (MHD) modeling [23]. In terms of power supply design, these operations are comprehensively defined by a "scenario", which includes:

- Current profiles corresponding to each actively powered coil.
- A plasma behavior model, represented as equivalent electrical current filaments.
- Parasitic currents arising in passive tokamak components, represented by equivalent circuits with internal resistance and inductance.

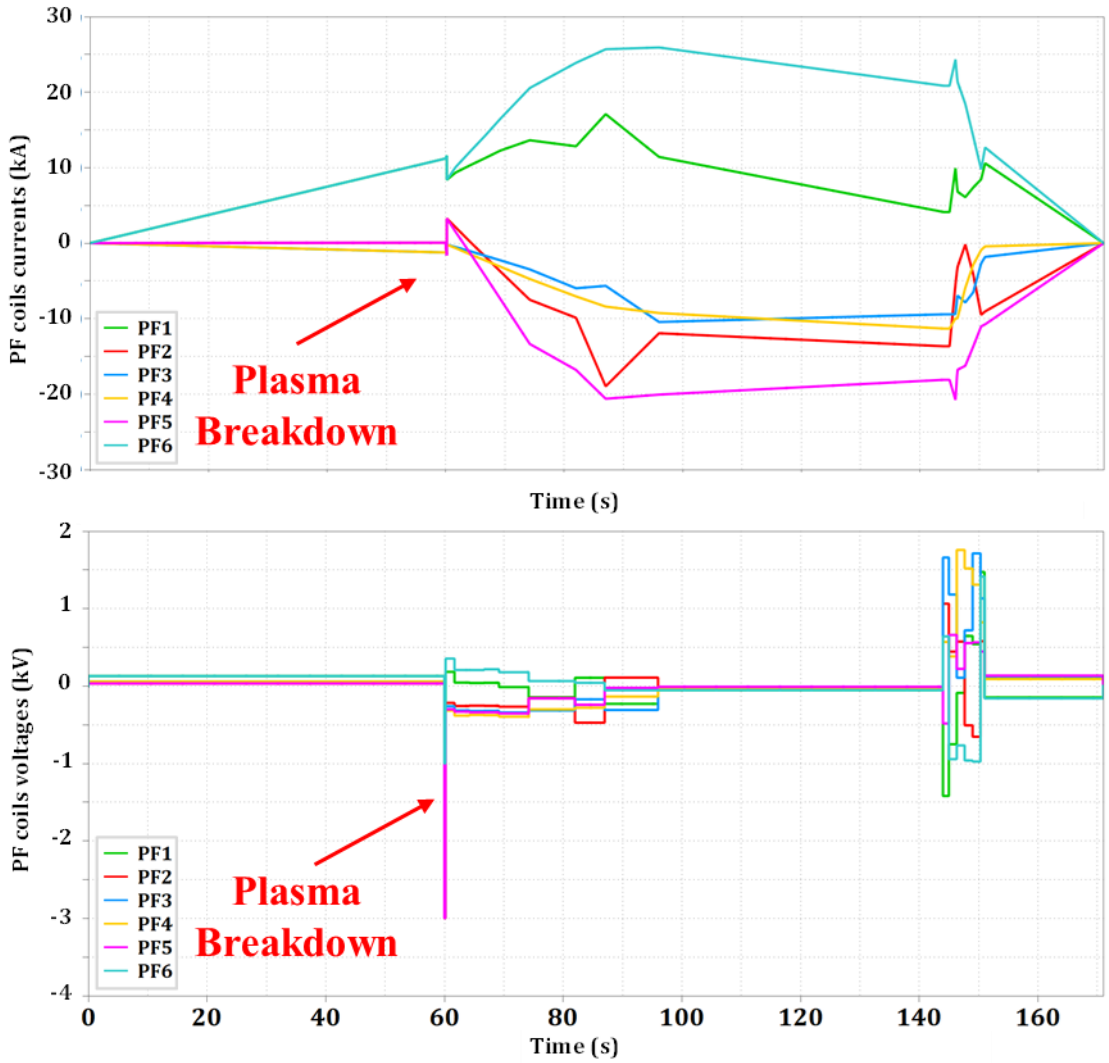

Figure 2.2 - Currents and voltages of PF coils in the DTT reference scenario, detailing transient phenomena and stages such as plasma breakdown, plasma ramp-up, the L-H mode transition, and the H-L mode transition.

Practically, a scenario is defined by a time-dependent vector containing current samples at specified time instants. The corresponding voltage evolutions can be derived by modeling the geometric structure of the tokamak's poloidal cross-sections and the magnetic interactions among them. All flowing currents are magnetically coupled through a square matrix M that contains the mutual inductances among active coils, plasma currents, and passive elements. For the active coils, the voltage required from the power supply systems can be determined by subtracting the voltage drops in the circuit (including DC bus bars, cryogenic transitions, connections, joints, and parasitic effects) from the voltage across the coil terminals.

The waveforms shown in Figure 2.2 were calculated using this procedure for the DTT's operations. To provide a comprehensive reference scenario for power supply design, these waveforms include more phenomena than standard scenarios that consider only equilibrium states. They encompass transient phases such as plasma breakdown, plasma ramp-up, low-to-high (L-H) mode transition, and high-to-low (H-L) mode transition. These analyses were conducted by the CREATE (Consorzio di Ricerca per l' Energia, l' Automazione e le Tecnologie dell' Elettromagnetismo) team and reprocessed for this study [28],[29],[30]. The calculations also involved other active and passive currents, particularly those in the central solenoid (CS) coils, which are not depicted in the plots.

While other experimental scenarios are possible in the DTT, the scenario presented in Figure 2.2 is the most demanding from an electrical standpoint and serves as a benchmark for design and optimization efforts.

The waveforms in Figure 2.2 establish the initial specifications for designing each PF power supply, specifically the minimum rated current and voltage. It is important to note that in many cases, plasma breakdown (which occurs at 60 seconds in Figure 2.2) is facilitated by additional components in series within the power supply circuit, such as a Switching Network Unit (SNU) [31]. However, for the DTT PF coils, all phases are implemented directly by the power supply converters.

2.3 Integrating Energy Storage into PF Coil Systems

In the PF power supplies, as illustrated in Figure 2.3, despite the occurrence of very high power peaks, the overall average power requirement remains relatively low. Additionally, the system operates within a restricted duty cycle, especially notable in current experimental setups like the DTT, where it is approximately 100 seconds out of every 3600 seconds [30].

To address the stringent demands of PF coils, a robust and efficient energy storage system is critical, as these coils represent only a portion of the electrical load necessary for operating an experimental tokamak like DTT or a fusion-based power plant. Such a system needs the capacity to store significant energy amounts and deliver it precisely as required.

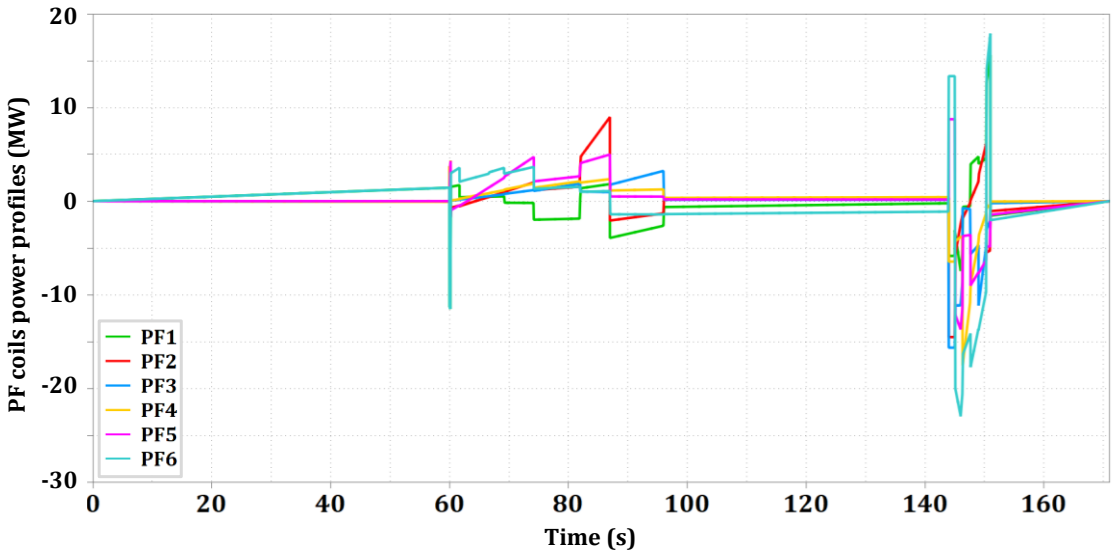

Figure 2.3 - Powers delivered to the PF coils in the DTT reference scenario.

In past fusion experiments, a common approach to support medium-to-high voltage transmission lines involved the use of flywheel generators, which could supply substantial power over short durations without impacting grid stability . This solution is less prevalent today, partly due to the limited availability of such devices on the market [32] (even though in some cases older flywheel generators are being reused in newer installations [33]). Additionally, as fusion operations are extended in duration for energy production, more adaptable technologies are required.

A promising alternative under investigation for fusion reactors involves a DC storage system that uses supercapacitor banks or other high-capacity storage devices, capable of rapid discharge and recharge to meet the dynamic requirements of PF coils. Here, the AC/DC converter stage functions as a “charger”, which can be rated for much lower power than the peak load delivery.

The development of such a DC storage system involves several important factors. Primarily, the storage must provide ample energy reserves to meet peak current and voltage needs, ensuring sufficient power output during the most demanding plasma confinement phases. Additionally, the system must respond swiftly to demand fluctuations, allowing

precise magnetic field adjustments necessary for plasma stability. Reliability and efficiency are also essential in the design, as any malfunction or inefficiency in power delivery could destabilize the plasma, risking disruptions or damage to the tokamak. Thus, advanced power conversion and energy storage technologies are integrated to meet these rigorous performance standards.

2.3.1 Benefits and Features of Supercapacitors

Supercapacitors (SCs) have gained recognition as a promising energy storage solution, particularly well-suited for applications that demand rapid charging and discharging cycles [34]. SCs offer distinct advantages such as high power density, extended cycle life, broad temperature tolerance, and minimal maintenance needs. Their capability to deliver and absorb power rapidly makes them ideal for managing short-term power demands, and unlike conventional batteries, they withstand millions of charge-discharge cycles with little degradation. Additionally, SCs operate effectively over a wide temperature range, which enhances their adaptability to diverse environmental conditions and reduces operational costs due to low maintenance requirements. While initially considered for mobility and renewable applications at much lower power and energy levels, SCs are now being evaluated for the higher demands of DTT PF power supplies.

Integrating SCs into the DC storage stage, positioned between the AC/DC and DC/DC converters, has the potential to enhance the performance and reliability of PF coil power supplies significantly. SCs could also be beneficial in other power systems within tokamaks and fusion devices.

However, SCs have limitations as well. One significant drawback is the frequency-dependent decay of their equivalent capacitance, which diminishes to nearly negligible levels at around 100 Hz, coupled with an increase in internal losses [35]. This constraint requires the implementation of additional filters to interface SCs efficiently with power electronics, allowing them to meet system requirements without adding unwanted harmonics or instabilities. Such filters are essential to uphold the overall performance and reliability of the power supply by mitigating the impact of SC frequency-dependent behavior.

Accurately modeling SCs in simulations is complex due to their intricate properties, which involve multiple parameters and dynamic behaviors [36]. Although ongoing experimental and theoretical work is further characterizing these aspects, a simplified model is adopted

here to focus on energy balance analysis rather than on component-specific transients. For this study, the entire SC bank is represented in simulations as a single capacitance with an equivalent series resistance (ESR) to capture the bank's overall characteristics while simplifying the simulation process.

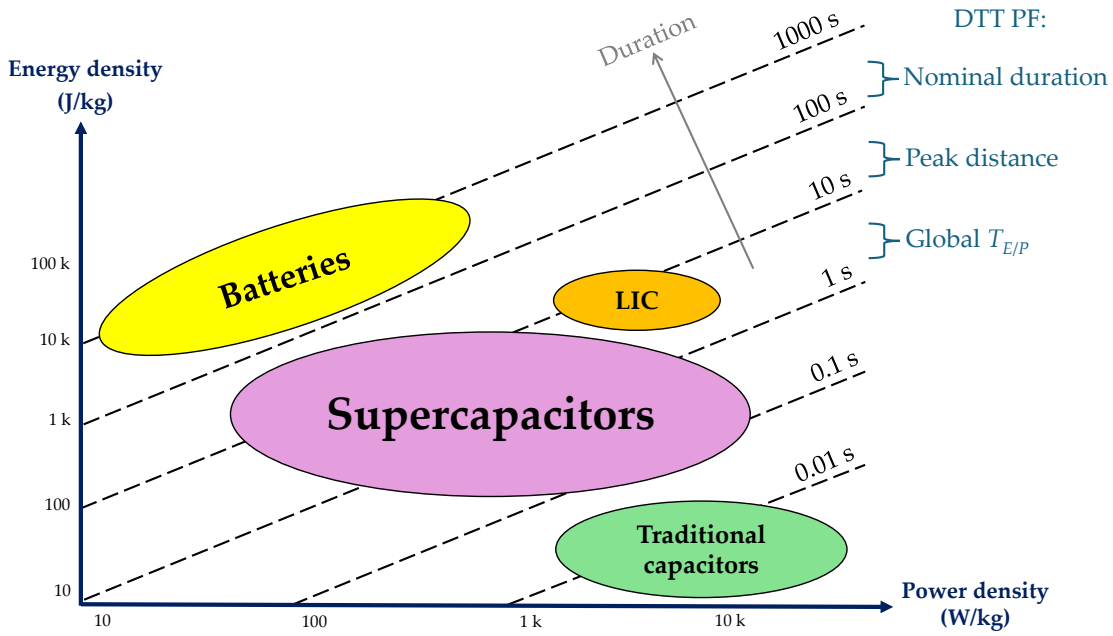

Figure 2.4 - Ragone plot comparing the main energy storage technologies and some typical durations of their operations. To support the analysis of this study, some characteristic times of the DTT PF power supply system are also reported for discussion.

A Ragone Plot, shown in Figure 2.4, serves as a common method for comparing energy storage technologies based on their power and energy densities [37],[38]. The ellipses in Figure 2.4 represent key groups of storage technologies, indicating that SCs occupy a complementary area relative to other solutions, providing a middle ground between the high energy density of batteries and the high power density of conventional capacitors. Lithium-ion capacitors (LICs), a type of SC with battery-like electrodes, extend the energy storage range, covering a broader area in the plot.

The dotted lines in Figure 2.4 summarize the typical operational durations for various power and energy levels. According to this plot, SC applications are most effective within timeframes of a few tens of seconds.

2.3.2 Applying the Ragone Plot to Tokamak Energy Needs

The Ragone Plot, however, is often subject to misinterpretation. For a clearer understanding of the analysis, it is essential to emphasize that an energy storage system can operate outside its designated region on the plot, though doing so would result in an oversized configuration—either in terms of power or energy. Such an approach might still be feasible depending on factors like cycle life, costs, or other specific requirements.

The duration considered for storage capacity should not be limited to the scenario duration alone. Instead, a shorter equivalent duration may be adopted, influenced by factors such as load type (dissipative or inductive) and the system's ability to recover energy from the load and charger, thereby supporting rapid charge-discharge cycles [39]. In such cases, the equivalent duration is roughly the interval between two consecutive positive power peaks.

Additionally, the SC voltage cannot be assumed to remain constant during operation, which affects both coordinates on the Ragone Plot. This variability must be factored into optimization, despite introducing complexity due to fluctuating voltage requirements (see Figure 2.2).

Consequently, while the nominal scenario duration for the DTT plasma is around 100 seconds, with approximately 160 seconds for the DTT PF coils, the actual maximum interval between positive power peaks falls within the range of 100–140 seconds as depicted in Figure 2.3, resulting in an effective duration of about 40 seconds. An input charger rated at a few megawatts can further decrease this interval by supplementing the scenario’s power needs and thus limiting SC voltage discharge.

These considerations suggest that employing DC storage and SCs is well-suited for tokamak PF systems. A forthcoming paper will expand this discussion to include TF, CS, VS, RC, DIV and EFC coils and their operational requirements.

2.4 Optimization Parameters and Their Limitations

Having established that PF power supplies would benefit from an SC-based energy storage system, the design challenge becomes optimizing its size and cost while managing its power demand from the grid. Since SC banks can be the most expensive and largest components of the power supply system, designing them based solely on peak requirements could negate any potential advantages in terms of cost and performance. Therefore, it is necessary to solve an optimization problem under highly variable and complex load conditions.

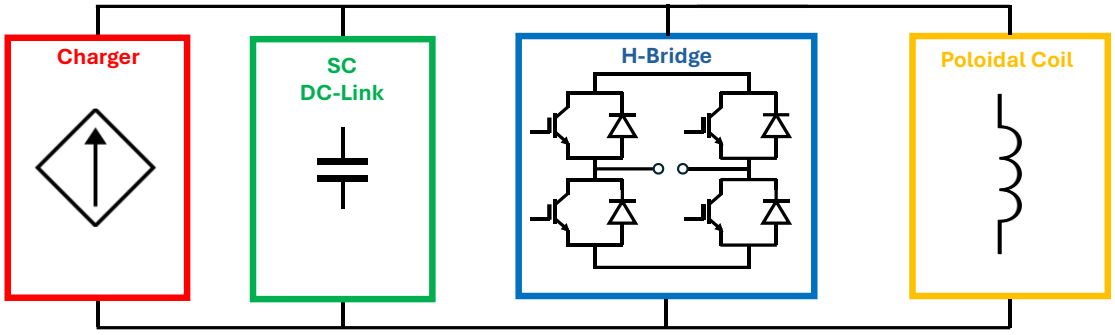

Figure 2.5 - General topology of the PF coil PS used for the design and optimization.

In common commercial technologies for energy storage applications, an individual SC cell possesses a capacitance value on the order of thousands of farads but can sustain a voltage of only about 2–3 V. As a result, practical implementations always involve connecting multiple cells in series (and parallel). Manufacturers usually provide assembled modules with voltages in the tens or hundreds of volts (e.g., 16 V, 48 V, 54 V, 64 V, 160 V). For PF power supplies, these voltages are still insufficient, and the required current (power) and energy levels necessitate using packs or banks of SC cells or modules. Some manufacturers offer racks of modules that include management, control, and cooling systems. While racks are useful for specific applications like grid storage, their fixed voltage levels limit flexible design optimization.

The first step in designing the power supply is selecting a suitable topology. For this study, a single H-bridge converter based on insulated-gate bipolar transistors (IGBTs) with a single SC DC link is considered. Figure 2.5 shows a block diagram of the power supply topology for a single PF coil, which will be used for optimization and circuit simulations.

In the final design, adding more IGBTs or bridges in series or parallel, or splitting the DC link into multiple SC banks connected to portions of the necessary H-bridges, could offer practical benefits [40]. However, these details do not significantly affect the dimensions of the SC DC link being optimized in this analysis. A slightly different scenario arises when an SC module and a small converter are combined into a basic unit that can be connected in series or parallel to achieve any desired voltage and current values. This approach focuses on designing a single unit but is constrained to discrete values, resulting in fewer degrees of freedom for optimization. Therefore, adopting a large DC link not tied to any specific SC model is preferred for this analysis.

To ensure balance, the banks must consist of cells or modules from the same family and encompass the same amount of SCs in series (N_s) for each parallel branch (N_p is the total number of parallel branches), fully defining the configuration by the pair $N_s \times N_p$.

It is commonly accepted that the model of a group of series and parallel cells can be extended from the model of a single cell. While this is not strictly accurate for complex models according to circuit theory, it is applicable for a simplified model consisting of an equivalent capacitance plus an equivalent series resistance (ESR), especially if all assembled cells or modules are identical. In reality, component tolerances mean they are not perfectly identical. Additionally, standard formulas for linear circuits may not apply due to non-idealities introduced by phenomena observed in SCs. Manufacturers typically include balancing systems in commercial modules or cabinets to compensate for tolerances, supporting the simplification but slightly modifying the SC equivalent circuit. These tolerances are expected to be accounted for in the estimation of the bank size and covered by safety margins. The difficulty in directly characterizing modules and packs likely stems from the challenge of finding specific instruments to perform such tests. Nonetheless, some studies have verified models for small numbers of SC cells with balancing.

Parameters for Optimization:

- Base SC Cell or module: identifies the unit voltage and capacitance, as well as intrinsic ESR.
- Number of series N_s and parallel N_p cells or modules: defines the configuration of the SC bank.
- Maximum current I_{Lmax} required for the load coils: although SC cells can handle extremely high peak currents (around 1000 A), this parameter is usually satisfied when other parameters are optimized.
- Maximum voltage V_{max} across the DC link: the voltage of the DC link can vary during operations to fully utilize stored energy, but it must always stay below the rated voltage of the SC cells and other hardware components, such as IGBTs. Choosing V_{max} involves deciding between the maximum value required by the load coils during the scenario and the maximum value allowed by the hardware.

- Minimum Voltage $V_{\min}$ across the DC link: $V_{\min}$ must be sufficient to drive the currents required by the scenario and is a critical parameter in fully exploiting stored energy.
- Peak Power Required for the Load Coils: Due to the properties of the Ragone plot, this parameter is generally satisfied when other parameters are optimized.
- Maximum Energy Stored E_{DC} in the DC Link: While it might seem straightforward, calculated by integrating the power over time during the scenario, it is not optimal for pulses longer than a few seconds. The actual value must comply with the maximum input power demand from the grid.
- Maximum Input Power Demand from the Grid P_{gridmax}: Although theoretically this can be zero if the scenario is entirely driven by the energy in the DC storage, in practice, a charger must be present. Therefore, it is sensible to utilize its contribution.

These parameters are interdependent. The most significant relationship is between $V_{\max}$ and E_{DC}, given by the well-known formula:

$$E_{\mathrm{DC}} = \frac{1}{2} C {V_{\max}}^2. \tag{2.1}$$

Enhanced optimization could be achieved by loosening or adjusting constraints among parameters. Using LICs for DC storage or hybridizing with batteries can increase energy density [41] [42]. Additionally, a separate charger could enable a higher $V_{\max}$ specifically for brief ramp-up periods. A deeper SC discharge might be realized by adding a boost converter stage between the SC bank and the H-bridge. An independent offset to $V_{\max}$ could be introduced by using an H-bridge powered by standard capacitors in series with the SC-fed H-bridge. While further strategies for reducing parameter interdependence are discussed in the following sections, none of these options seem universally beneficial enough to warrant the added costs or complexities in typical applications.

2.5 Optimization Approaches and Criteria

Assessing all these parameters analytically is impractical due to the complex interactions and variable conditions involved, then the problem will be tackled through simulations [43].

However, some formulas can be derived to provide guidelines for approaching the optimization problem.

2.5.1 Analytical Formulas for Optimizing PF Coils

Assuming ideal conditions for the SC and converters, the simplest energy balance involves transferring all stored energy from the SC to the load. Thus, the DC energy E_{DC} must exceed the energy E_L that the load can store, this means having the following expression:

$$E_{\mathrm{DC}} \gg E_L. \tag{2.2}$$

The energy stored in the SC is derived from $V_{\max}$ using (2.1).

However, it is important to note that SC capacitance depends on voltage, generally exhibiting a linear behavior [44] [45]:

$$C(V) = C(V_{\mathrm{ref}}) + k_v[V - V_{\mathrm{ref}}]. \tag{2.3}$$

This voltage dependency is not typically reported in manufacturers' datasheets but is observed in experimental characterizations [44] [45]. For design purposes, the standard formula can be used while considering this effect as a safety margin.

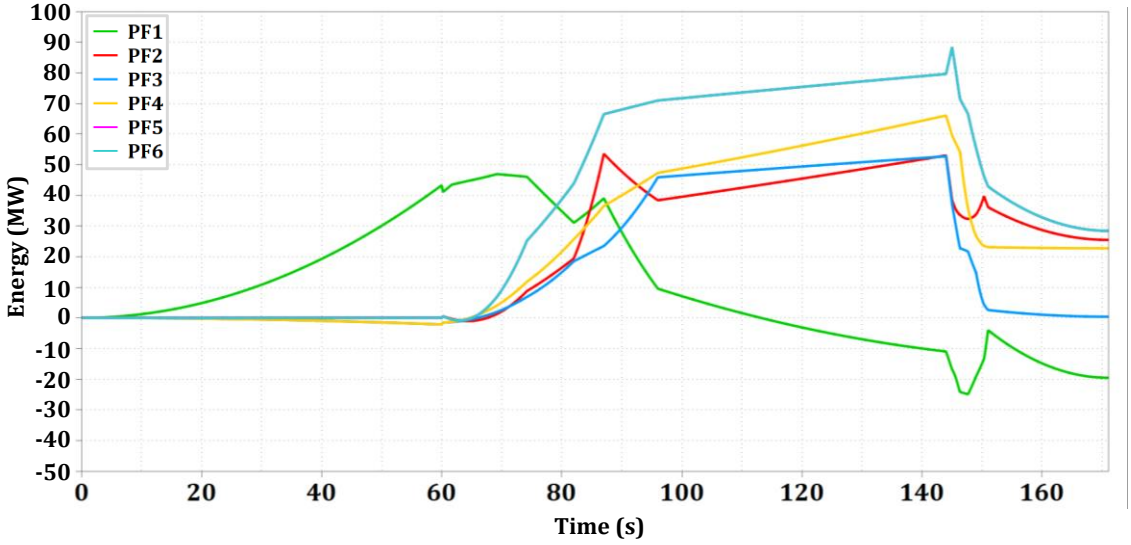

Figure 2.6 - Energies delivered to the PF coils in the DTT reference scenario.

If the load were limited to the coil itself, the magnetic energy would be solely determined by its self-inductance L:

$$E_L = \frac{1}{2} L I_{\max}{}^2. \tag{2.4}$$

Table 2.1 lists the self-inductance values for the DTT PF coils, corresponding to the diagonal entries of the inductance matrix.

Table 2.1 - Self-inductance and energy values for DTT PF coils.

PF Coil	L	E_L	E_s
PF1	454 mH	80 MJ	47 MJ
PF2	298 mH	65 MJ	54 MJ
PF3	690 mH	46 MJ	53 MJ
PF4	690 mH	269 MJ	66 MJ
PF5	298 mH	77 MJ	88 MJ
PF6	454 mH	185 MJ	100 MJ

However, the actual energy involves additional contributions, which can be calculated by integrating the power curves in Figure 2.3, resulting in a time-varying energy $e(t)$:

$$e(t) = \int_0^t p(\tau) d\tau. \tag{2.5}$$

The negative energies at the end of operations are neglected in Figure 2.6 as these arise from the approach of discharging all coils within the same time interval, potentially returning more energy to certain coils than others. This aspect will be adjusted when scenarios are optimized with respect to DC storage requirements.

An important parameter characterizing the scenario's energy demand is the maximum energy over time:

$$E_s \overset{\text{def}}{=} \max_t \{e(t)\}. \tag{2.6}$$

For a single coil without mutual interactions, E_s and E_L are equivalent.

Introducing E_s allows to define the efficiency of the DC storage:

$$\eta_{DC} \overset{\text{def}}{=} \frac{E_s}{E_{DC}}. \tag{2.7}$$

A higher η_{DC} indicates better utilization of the SC bank, while a lower value provides a safety margin to account for unforeseen losses or voltage drops in semiconductors.

Comparing the energy values estimated by different approaches reveals that using E_{s} derived from the complete MHD model significantly reduces the estimated energy flowing in the power supply circuits, potentially increasing efficiency.

2.5.2 Establishing Minimum Voltage for DC Link Design

A more detailed approach includes a minimum voltage V_{min} for the SC bank model, leading to the condition:

$$\frac{1}{2}C{V_{\mathrm{max}}}^2 - E_{\mathrm{s}} > \frac{1}{2}C{V_{\mathrm{min}}}^2. \tag{2.8}$$

Introducing V_{min}, the efficiency η_{DC} can be expressed as function of this parameter:

$$\eta_{\mathrm{DC}} \cong 1 - \left(\frac{V_{\mathrm{min}}}{V_{\mathrm{max}}}\right)^2. \tag{2.9}$$

This underscores the importance of maximizing the voltage range from V_{min} to V_{max} to enhance efficiency.

The value of V_{min} must satisfy two conditions:

- It must be higher than the voltage required to power the load, considering both the scenario's voltage requirements and the voltage necessary to maintain the IGBTs conducting.
- It should be above a threshold considered safe or optimal for the SC bank, although this value is not precisely defined.

Given the ambiguity of the second condition, a simplified approach is often employed.

2.5.3 Simplified Method Using Half-Voltage Cycles

A practical method involves setting $V_{\mathrm{min}} = \frac{V_{\mathrm{max}}}{2}$. This choice aligns with the operating range commonly used to define SC specifications and is critical for LICs, which can be damaged if discharged below a threshold near $\frac{V_{\mathrm{max}}}{2}$ [47].

This approach simplifies calculations, resulting in an clear requirement for the SC bank's capacitance:

$$C > \frac{4}{3} L \frac{{I_{\max}}^2}{{V_{\max}}^2}. \tag{2.10}$$

With the capacitance determined, the bank's energy can be calculated using (2.1). While the ability to generate $I_{\max}$ should be confirmed, it is usually not an issue. This method does not account for voltage-dependent capacitance, which can serve as an additional safety margin.

In this framework, η_{DC} is fixed at 75%, reflecting the proportion of stored energy utilized. However, this formula does not automatically ensure compliance with (2.9), so this condition must be independently verified.

2.5.4 Scenario-Based Optimization in the Time Domain

To potentially achieve higher efficiency, it could be allowed for SC discharge beyond 50%, accepting a possible reduction in lifecycle. The optimal energy balance, without involving the grid, is achieved when the energy delivered does not reduce the SC bank's voltage below what's required by the scenario:

$$\frac{1}{2} C {V_{\max}}^2 - e(t) > \frac{1}{2} C v(t)^2. \tag{2.11}$$

Here, $e(t)$ is the energy demanded by the scenario, as shown in Figure 2.6. This model can be readily implemented in simulations:

$$C > \max_t \left\{ \frac{2e(t)}{{V_{\max}}^2 - v(t)^2} \right\}. \tag{2.12}$$

Table 2.2 presents the capacitance values for each PF coil derived using this method. This represents an optimistic estimate that does not factor in losses.

Once the capacitance is established, the required energy storage is calculated as:

$$E_{\mathrm{DC}} > \max_t \left\{ \frac{e(t)}{1 - \left[\frac{v(t)}{V_{\max}}\right]^2} \right\}. \tag{2.13}$$

Again, confirming the ability to generate $I_{\max}$ is necessary but typically not problematic.

If the time of maximum energy demand E_{s} coincides with the minimum $V_{\min}$, the efficiency approximates the value given by the earlier formula. This is common, but if the

scenario's voltage requirements dictate a higher $V_{\min}$, it could lead to a larger required capacitance. In such cases, the efficiency satisfies:

$$\eta_{\mathrm{DC}} < 1 - \left(\frac{V_{\min}}{V_{\max}}\right)^2 . \tag{2.14}$$

This method can result in smaller SC banks with higher efficiency, although efficiency may not be the primary design criterion. For the DTT PF coils, this situation did not occur.

Table 2.2 - SC bank design results from time-domain optimization.

PF Coil	Minimum *C* from (2.12)	Minimum E_{DC} from (2.13)	Related η_{DC}
PF1	39 F	63 MJ	75%
PF2	10 F	58 MJ	92%
PF3	11 F	68 MJ	78%
PF4	12 F	72 MJ	91%
PF5	16 F	92 MJ	96%
PF6	62 F	100 MJ	100%

2.5.5 Compensating for System Losses

The previous formulas are true for an ideal system, neglecting all the losses. In reality, several factors contribute to losses: SC ESRs; parasitic elements on AC or DC sides (cables, bus bars, connections); voltage drops in converter semiconductors; passive elements like the vessel, walls, and plasma equivalent resistance.

Modeling all these losses is impractical due to their dependence on variables like time, frequency, current, and voltage. While the complete scenario model (as in Figure 2.2) can account for some effects, other losses must be estimated.

A practical approach is to set a value of input power P_{gridmax} sufficient for compensating the maximum power or energy demands during operations. These estimates, derived from Figure 2.3 and Figure 2.6, considering that short-duration high power peaks can be managed effectively. Based on this approach, a value for P_{gridmax} in the range of 1 to 3 MW was chosen as the starting point for the case of study treated in this section.

2.6 Leveraging Complementary Power Demands of PF Coils

While the previous sections primarily addressed PF systems, the principles discussed are largely applicable to other types of coils. Here, the specific feature of PF systems is highlighted. In tokamak operations, PF coils exhibit energy demand profiles that are often complementary between two coils. This implies that while some coils draw high power, others may have lower demands or even return energy to the system. This behavior is evident in the DTT case shown in Figure 2.2. By analyzing these profiles, a shared DC storage system can be designed to optimally distribute energy needs across multiple coils.

Figure 2.7 illustrates the total power delivered to the load coils by all the PF power supply systems.

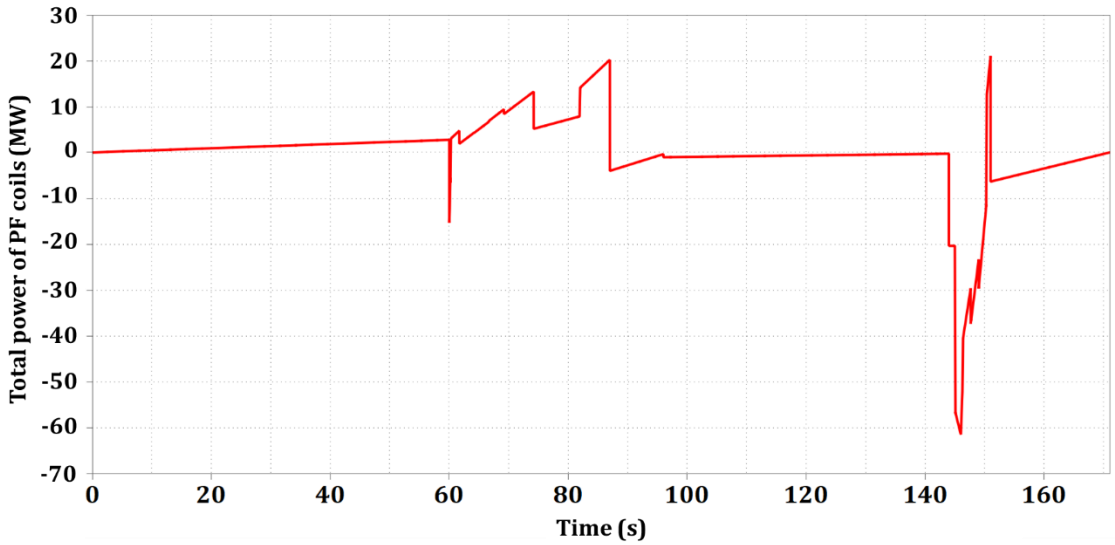

Figure 2.7 - Sum of the instantaneous powers of the six PF coils shown in Figure 2.3.

By integrating this power over time, Figure 2.8 shows that it is possible to recover a significant amount of energy.

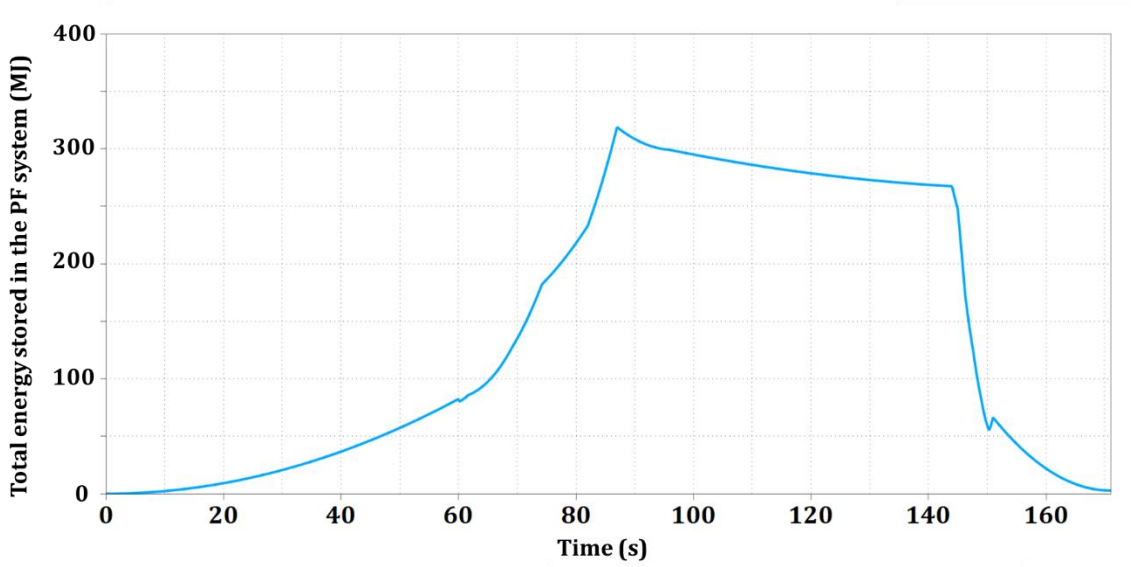

Figure 2.8 - Total energy stored in the load coils, including equivalent mutual couplings.

This is because the actual losses in the process are minimal, especially when compared to the peak power levels. It should be noted, however, that some power flows to the plasma and passive components, with additional input from the CS coils. Likely, only the early DTT experiments will quantify these losses accurately, but even partial recovery of energy required for tokamak operations represents a significant accomplishment.

The insights from Figure 2.7 and Figure 2.8 clarify that the total power demand is less than the combined rated power of each supply shown in Figure 2.3. This observation suggests that implementing a single storage system shared among several coils could reduce the total power demand from the grid. This reduction results from the complementary nature of PF coil power demands. One innovative aspect of this work is to leverage this complementary demand for optimization purposes.

This feature is particularly noticeable in the DTT. While gathering data for every case is challenging, the current profiles retrieved for other tokamaks indicate that the considerations made so far for the DTT could be applicable elsewhere. Figure 2.9 shows a valuable example: the power profiles of the equilibrium field coils (different name, but analogue to PF coils) of JT-60SA [48], the largest superconducting tokamak currently in operation globally. In Figure 2.9, the coil names have been adjusted to match those used in the DTT. The JT-60SA coils currently do not have DC storage stages, they are supplied from the grid through thyristor bridges.

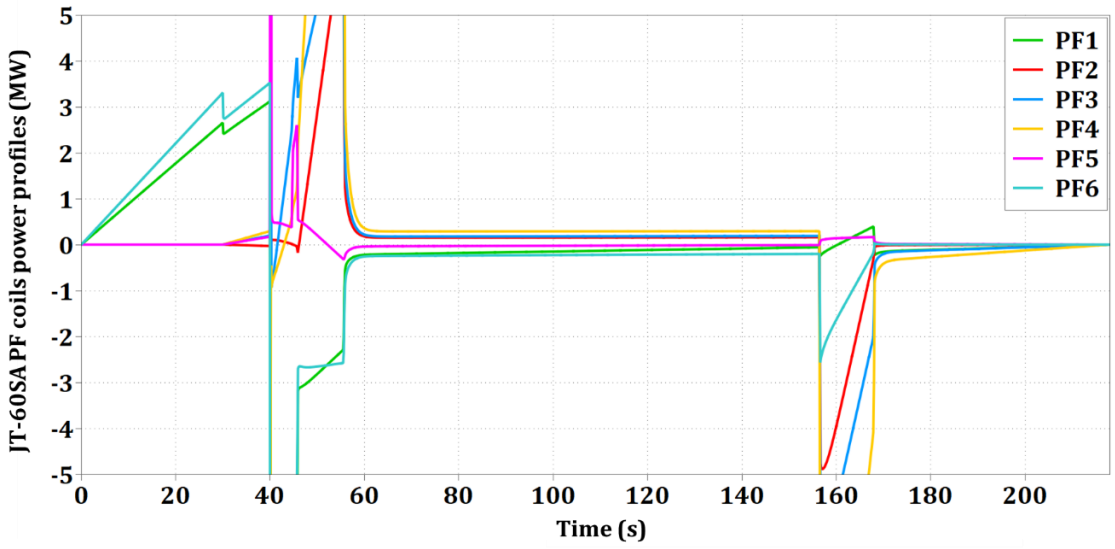

Figure 2.9 - Example of complementarity in the powers delivered to the PF coils in the JT-60SA reference scenario [48] (coil names adjusted to match those of the DTT).

It is worth emphasizing that the optimization process is based on scenarios, like those shown in Figure 2.2 and Figure 2.9, which were originally developed by plasma physicists without regard for potential electrical power or energy optimization. This suggests that future results could be even more impactful if these aspects are integrated from the outset.

The concept of complementary power and energy profiles plays a key role in optimizing DC storage system design. By utilizing these complementary profiles, the footprint of the DC storage can be minimized while still meeting performance requirements.

2.6.1 Determining Equivalent Parameters for Shared DC Links

Observing the peaks in Figure 2.7 and Figure 2.8 allows to introduce a new global equivalent time $T_{E/P}$ based on these peaks:

$$T_{E/P} \stackrel{\text{def}}{=} \frac{\max_t\{\sum_{n=1}^{6} e_{sn}(t)\}}{\max_t\{\sum_{n=1}^{6} p_n(t)\}} \cong 5\ \text{s}\,. \tag{2.15}$$

This time can be compared to durations on the Ragone plot, as shown in Figure 2.4, further demonstrating that supercapacitors are an ideal solution for optimizing the DTT PF system.

Equations (2.12) and (2.13) from the previous section can be extended to a shared DC link with capacitance C among multiple coil power supply circuits. Each circuit has its own voltage $v_n(t)$ and energy $e_n(t)$, but they share the same maximum voltage $V_{\max}$:

$$C > \max_t \left\{ \frac{2 \sum_n e_n(t)}{{V_{\max}}^2 - \max_n \{v_n(t)^2\}} \right\} \tag{2.16}$$

$$E_{\mathrm{DC}} > \max_t \left\{ \frac{\sum_n e_n(t)}{1 - \max_n \left\{ \left[\frac{v_n(t)}{V_{\max}} \right]^2 \right\}} \right\}. \tag{2.17}$$

While these formulas may appear complex, they can be readily implemented using software simulations.

The performance of a shared DC link with total energy E_{DC} can be evaluated by introducing new definitions of efficiency. The first extends (2.7) to the global efficiency of the shared DC link by comparing it to the total energy of all shared circuits:

$$\eta_{\mathrm{DC}} \stackrel{\mathrm{def}}{=} \frac{\sum_n E_{sn}}{E_{\mathrm{DC}}}. \tag{2.18}$$

Alternatively, the effectiveness of sharing between the power supplies of different coils, each originally designed with its own bank energy $E_{\mathrm{DC}n}$, can be assessed using the ratio:

$$\eta_{\mathrm{sharing}} \stackrel{\mathrm{def}}{=} 1 - \frac{E_{\mathrm{DC}}}{\sum_n E_{\mathrm{DC}n}}. \tag{2.19}$$

In both definitions, the efficiencies can exceed 100%, indicating that the shared system is more efficient than the sum of the individual systems.

2.7 Simulations

2.7.1 Circuital Models

To determine the optimal balance between the size of the DC energy storage system and the peak power drawn from the electrical grid, it is essential to develop an electrical model within a power electronics simulation software. In this study, the tool PLECS has been used to simulate the block diagram shown in Figure 2.5 for each PF coil. This simulation includes all necessary components for operation, even those not explicitly depicted in Figure 2.5. This section outlines the key principles of the developed model.

Implementing the scheme from Figure 2.5 in a circuit simulation software requires a method to accurately represent the effects of mutual couplings among the coils. Without accounting for these mutual inductances, component ratings could appear higher than

necessary, leading to an oversized and inefficient design. However, most circuit simulation software does not natively support an inductance matrix $\underline{\underline{M}}$ with any number *N* of rows and columns. Moreover, simulating even six coupled power supply circuits becomes computationally intensive, making it impractical for an optimization process that requires numerous simulations. Therefore, it is crucial to introduce a simplified method to emulate all the mutual coupling effects efficiently.

In the most general scenario, the vector $\underline{v}(t)$ representing the voltages across all PF coils and other poloidal cross-section elements can be expressed in terms of the vector $\underline{i}(t)$ of impressed currents using the following relationship:

$$\underline{v}(t) = \frac{d\left[\underline{\underline{M}}(t) \times \underline{i}(t)\right]}{dt}. \tag{2.20}$$

In (2.20), the mutual inductance matrix $\underline{\underline{M}}$ is time-dependent, which poses challenges for circuit simulators that typically handle time-invariant parameters.

If the voltage and current profiles for the coil under analysis are known, the system can be modeled using a standard approach with constant mutual inductance values. Specifically, the voltage across the k^{th} PF coil can be written as:

$$v_k(t) = \sum_{n=1}^{N} M_{kn} \frac{di_n(t)}{dt}. \tag{2.21}$$

Here, M_{kn} represents the mutual inductance between the k^{th} PF coil and the n^{th} element (where n = 1 to 6 for PF coils and n = 7 to N for passive elements), and $i_n(t)$ are the corresponding currents. The self-inductance and current of the coil under consideration are denoted as L_k and $i_k(t)$, respectively.

To simplify the model and reduce computational complexity, instead of considering all *N* elements, each coil is magnetically coupled to a single fictitious auxiliary coil with a controlled current source $i_A(t)$ in series. Under this simplification, the voltage across the k^{th} coil becomes:

$$v_{k\mathrm{A}}(t) = L_k \frac{di_k(t)}{dt} + M_{k\mathrm{A}} \frac{di_A(t)}{dt}. \tag{2.22}$$

The two expressions for the coil voltage will be equivalent if $v_{k\mathrm{A}}(t) = v_k(t)$ at every instant in time. This condition allows to dynamically determine the controlled current $i_A(t)$

through a simple control loop that enforces the equality. By integrating and solving for $i_A(t)$, one obtains:

$$i_{\mathrm{A}}(t) = \frac{1}{M_{\mathrm{k}A}}\left(\int_0^t v_k(\tau)d\tau - L_k i_k(t)\right). \tag{2.23}$$

Since $v_k(t)$, L_k, and $i_k(t)$ are always known, all mutual coupling effects can be emulated by controlling the current in the auxiliary inductor using (2.23). The value of $M_{\mathrm{k}A}$ (and similarly the self-inductance L_A of the auxiliary coil) can be chosen arbitrarily, provided it is consistent with other circuit parameters. Figure 2.10 illustrates the block diagram implementing this algorithm for the mutual coupling contribution.

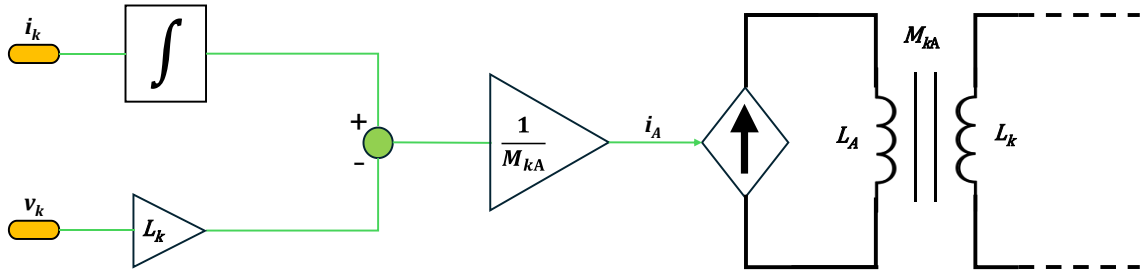

Figure 2.10 - Block diagram of the control algorithm used to emulate the mutual coupling effect.

For simulating the charger's behavior, Figure 2.11 presents the logic of a controlled current source. The charger supplies current whenever the DC-link voltage drops below a specified reference threshold but does not exceed the imposed limit on the maximum grid power P_{gridmax}. The threshold control includes a hysteresis band between V_{max} and $V_{\mathrm{max}} - 10V$. When activated, the charger provides the maximum current allowed based on the fixed P_{gridmax} and V_{max}. A more sophisticated control strategy could involve limiting the charger current based on anticipated (feedforward) needs of the scenario.

As previously mentioned, a simplified model for the supercapacitor (SC) bank, comprising only capacitance and equivalent series resistance (ESR), is sufficient to focus on the energy balance analysis in the simulations.

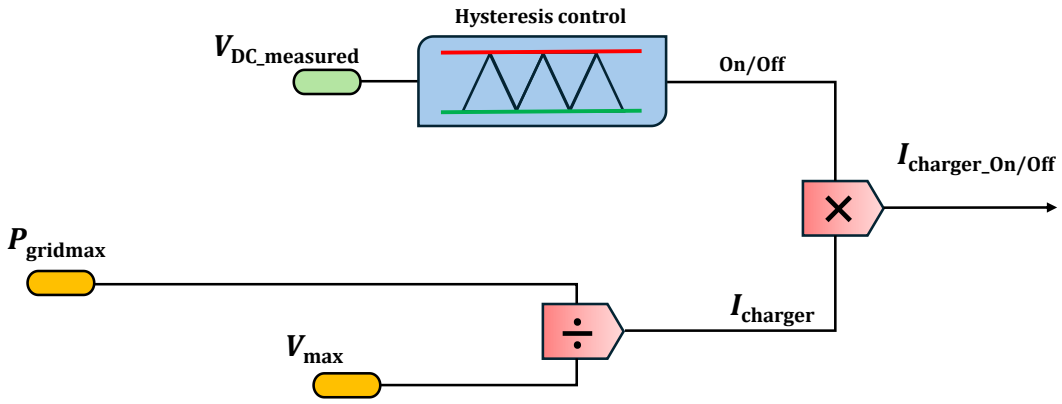

Figure 2.11 - Logic diagram of the controlled current source representing the charger in circuit simulations.

The control algorithm for the H-bridge converter is depicted in Figure 2.12. Starting from the error between the reference load current and the actual current, a proportional-integral (PI) regulator generates a modulation signal. This signal is then compared with a triangular carrier waveform at the switching frequency. The direct output of the comparator provides the gating signals for one diagonal of the H-bridge, while its inverse controls the other diagonal.

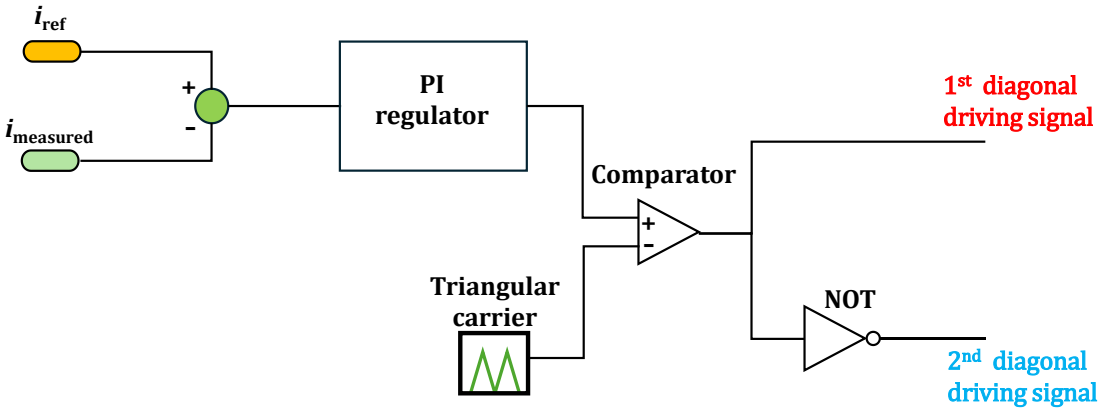

Figure 2.12 - Block diagram of the H-bridge control algorithm.

By incorporating these models and control strategies, the simulation can accurately reproduce the behavior of the tokamak power supply system, allowing for effective evaluation and optimization of the DC energy storage size and grid power requirements.

2.7.2 Simulation Campaign

Although preliminary indications of optimal trade-offs were derived using (2.16) and (2.17), practical optimization requires validation through detailed simulations. These

simulations are essential to verify the theoretical findings and to ensure that the proposed configurations perform as expected under realistic operating conditions.

For the simulation studies, maximum DC-link voltages $V_{\max}$ of 1.8 kV and 3.5 kV were chosen. These voltage levels are compatible with commercially available insulated-gate bipolar transistors (IGBTs) that offer suitable switching frequencies for the application. For instance, a 3.5 kV DC-link voltage can be managed by a single 6 kV IGBT used in railway applications or by connecting three widely used 1.7 kV IGBTs in series.

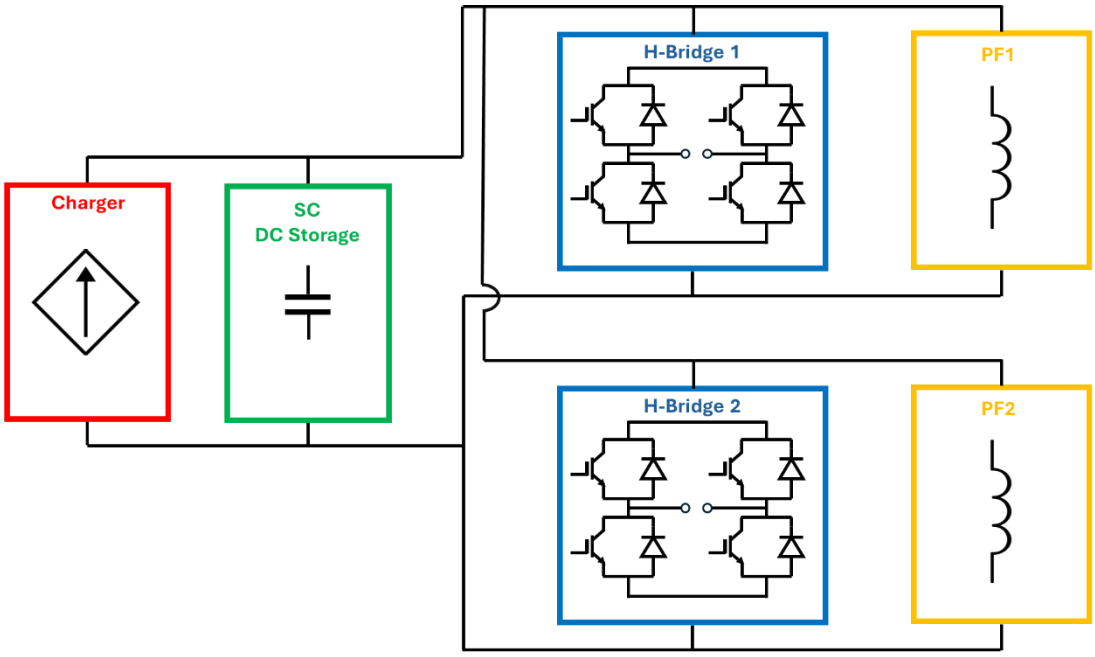

Figure 2.13 - Basic circuit configuration for a shared DC link (using the PF1 and PF2 pair as an example).

The PF power supplies, each with an installed capacity of up to 90 MW, can operate while drawing less than 3 MW of input power from the grid. In this optimization study, three different limits for the maximum grid power (P_{gridmax}) were considered, with the input power factors being negligible for this analysis:

1. Maximum of 1 MW
2. Maximum of 2 MW
3. Maximum of 3 MW

Under each of these three power limits, two contrasting conceptual topologies were compared:

1. Independent DC Links
2. Shared DC Links

In the independent DC links configuration, each PF power supply operates with its own dedicated DC link (DC storage bank). This setup serves as the baseline for comparison.

In the shared DC links configuration, depicted schematically in Figure 2.13, the benefits of sharing a DC link among power supplies feeding different PF coils are exploited. This approach leverages the complementary power demands of certain PF coils to optimize the size and utilization of the DC energy storage system.

2.7.2.1 Selecting Optimal Coil Pairs for DC Link Sharing

Considering that significant power and energy demands occur at specific time instants (as shown in Figure 2.7 and Figure 2.8), sharing a large energy storage system among all PF coils would yield limited efficiency improvements. Preliminary simulations demonstrated that while sharing a DC link among all PF power supplies is theoretically possible, the advantages are minimal compared to the engineering complexities it introduces.

On the other hand, connecting two power supplies to opposite ends of a common DC link presents clear benefits in terms of system layout, feasibility, and performance. Therefore, the analysis focused on combining pairs of PF coils to share the DC storage bank effectively.

By analyzing the power demand profiles of the six PF coils shown in Figure 2.3, possible pairings were evaluated to identify the most advantageous combinations. The objective was to combine the dynamic power profiles in such a way as to minimize both the average power drawn from the DC storage and the power variations.

The most logical and beneficial pairs for sharing the DC storage bank, based on the complementarity of their power profiles, are:

1. PF1 and PF2 (PF1 & PF2)
2. PF3 and PF4 (PF3 & PF4)
3. PF5 and PF6 (PF5 & PF6)

These pairings were selected because their power demand profiles are complementary, when one coil has a high power demand, the other typically has a lower demand or may even be returning energy to the system. By sharing the DC storage between these coils, it is possible to reduce the overall size of the energy storage system and optimize the power drawn from the grid.

The choice of these specific pairs also offers practical advantages in terms of system design and implementation. Connecting two power supplies at opposite ends of a shared DC

link simplifies the physical layout and reduces the complexity of the connections, making the system more manageable and cost-effective.

By focusing on these pairings and analyzing them under different grid power limits, the simulation campaign aims to validate the benefits of shared DC links and determine the optimal configurations for the PF power supplies in the tokamak system.

2.7.3 Main Simulation Outcomes

The benefits of pairing PF coils are vividly illustrated in Figure 2.14, which compares the DC-link voltage of the PF2 power supply with a capacitance of 17 F at 3.5 kV in two scenarios: when it operates individually connected to PF2 and when it shares the DC-link with PF1. In the individual case, the DC-link voltage of PF2 drops to zero rapidly due to its high power demand, making it impossible to maintain the required voltage levels. However, when PF2 shares the DC-link with PF1, this rapid voltage decay does not occur because PF1 compensates for the power demand far more effectively than the distribution grid could.

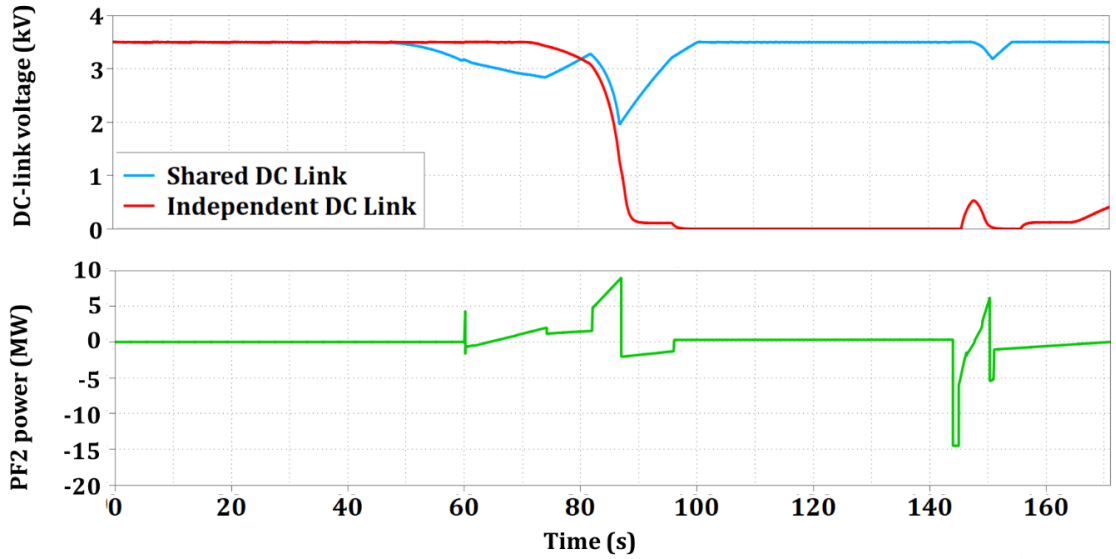

Figure 2.14 - Comparison between the scenarios where the PF1 and PF2 power supplies share the DC storage and where the same DC storage feeds only the PF2 power supply.

The main findings from the simulation campaign are summarized in Table 2.3. For each configuration, the table specifies:

1. Capacitance Value of the Storage: The total capacitance required for the DC-link.
2. Nominal Peak Voltage of the DC-Link: The maximum voltage level the DC-link is designed to handle.

3. Total Energy Stored in the Bank: The total energy capacity of the supercapacitor (SC) bank.

Some PF coils, when operated individually, require a peak voltage of 1.8 kV. However, in the shared DC-link configuration, the bank must be sized according to the highest peak voltage needed by any of the PF coils in the pair, which is 3.5 kV in this case. Notably, pairing PF6 with PF1 did not demonstrate benefits in terms of energy savings or size reduction; therefore, it is more advantageous to design them independently, leveraging economies of scale and providing a safety margin for operations.

Table 2.3 offers significant insights into the advantages and limitations of sharing DC-links:

- PF1 & PF2 Pair: Sharing the storage between PF1 and PF2 could potentially reduce the required size of the storage bank by half.
- PF5 & PF6 Pair: The reduction is even more pronounced, with storage requirements potentially decreasing by about two-thirds.
- PF3 & PF4 Pair: No significant advantages were observed when transitioning to a shared DC storage configuration for this pair. Therefore, there is no compelling reason to alter the simpler, independent layout for these coils.

Table 2.4 presents these results in terms of efficiency, utilizing the definitions provided in (2.18) and (2.19). As anticipated, in some cases, the efficiencies exceed 100%, indicating that the shared configuration is more efficient than the sum of the individual systems.

2.7.4 Impact on Physical Layout and Size

Beyond the numerical values of the electrical parameters, it is crucial to consider the practical aspects of implementing the SC bank, including its physical layout and dimensions. To this end, the CapTop CTM 00165C0 0054V0 NN00 SC module (depicted in Figure 2.15) was used as a reference. This module is rated at 54 V and 165 F, with a peak current capability (limited to short durations) of up to 2000 A. Other manufacturers offer similar modules with comparable footprints and performance characteristics.

These SC modules can be assembled into standard cabinets with physical dimensions of 600 mm × 1200 mm × 2000 mm (height). Thus, the size of the SC bank can be quantified in terms of the number of these standard cabinets required.

Table 2.5 translates the electrical requirements from Table 2.3 into practical terms of layout and dimensions, considering the reference SC modules and cabinets.

Figure 2.15 - CapTop CTM 00165C0 0054V0 NN00 supercapacitor module, rated at 54 V and 165 F.

2.7.5 Optimizing Input Power from the Grid

Another significant aspect of the study was analyzing the effect of the peak power drawn from the grid, which is critical for designing the input charger and the distribution grid infrastructure. The key findings are:

- Increasing the peak power limit from 1 MW to 2 MW results in a substantial reduction in the required energy for DC storage. Specifically, considering the reference SC modules and cabinets, this could save approximately 18 cabinets.
- Increasing Peak Power Limit from 2 MW to 3 MW produces less pronounced effects, resulting in a savings of only about 6 cabinets.

These results suggest that setting a peak power limit of 2 MW offers the best compromise between efficiency and practical feasibility. Detailed data supporting these conclusions can be found in Table 2.3 and Table 2.5.

Table 2.3 - Summary of differences in voltage, capacitance, and energy of SC banks for independent and shared DC-links under various grid power limits.

	$P_{gridmax}$=1 MW for each coil		$P_{gridmax}$=2 MW for each coil		$P_{gridmax}$=3 MW for each coil	
	Independent DC-links	**Shared DC-links**	**Independent DC-links**	**Shared DC-links**	**Independent DC-links**	**Shared DC-links**
PF1	1.8 kV 68 F 110 MJ	3.5 kV 30 F 184 MJ	1.8 kV 58 F 92 MJ	3.5 kV 17 F 104 MJ	1.8 kV 44 F 70 MJ	3.5 kV 15 F 92 MJ
PF2	3.5 kV 35 F 215 MJ		3.5 kV 34 F 209 MJ		3.5 kV 30 F 184 MJ	
PF3	3.5 kV 28 F 172 MJ	3.5 kV 60 F 368 MJ	3.5 kV 25 F 154 MJ	3.5 kV 55 F 337 MJ	3.5 kV 18 F 110 MJ	3.5 kV 40 F 245 MJ
PF4	3.5 kV 32 F 196 MJ		3.5 kV 28 F 172 MJ		3.5 kV 22 F 135 MJ	
PF5	3.5 kV 55 F 337 MJ	3.5 kV 38 F 233 MJ	3.5 kV 55 F 337 MJ	3.5 kV 30 F 184 MJ	3.5 kV 25 F 154 MJ	3.5 kV 25 F 154 MJ
PF6	1.8 kV 155 F 233 MJ		1.8 kV 120 F 260 MJ		1.8 kV 105 F 176 MJ	

Table 2.4 - Achieved efficiencies for PF pairs, assessed using the two different proposed definitions.

	1 MW		2 MW		3 MW	
	η_{DC}	$\eta_{sharing}$	η_{DC}	$\eta_{sharing}$	η_{DC}	$\eta_{sharing}$
PF1&PF2	55%	42%	97%	65%	109%	64%
PF3&PF4	32%	0%	35%	0%	49%	0%
PF5&PF6	81%	61%	102%	66%	122%	68%

Table 2.5 - Comparison of SC bank sizes, expressed as the number of reference cabinets and configurations, for shared and independent dc storage under various grid power limits.

	1 MW		2 MW		3 MW	
	Independent DC-links	**Shared DC-links**	**Independent DC-links**	**Shared DC-links**	**Independent DC-links**	**Shared DC-links**
PF1	14 cabinets (1 × 14)	24 cabinets (2 × 12)	12 cabinets (1 × 12)	14 cabinets (2 × 7)	9 cabinets (1 × 9)	12 cabinets (2 × 6)
PF2	28 cabinets (2 × 14)		28 cabinets (2 × 14)		24 cabinets (2 × 12)	
PF3	22 cabinets (2 × 11)	48 cabinets (2 × 24)	20 cabinets (2 × 10)	44 cabinets (2 × 22)	14 cabinets (2 × 7)	32 cabinets (2 × 16)
PF4	26 cabinets (2 × 13)		22 cabinets (2 × 11)		18 cabinets (2 × 9)	
PF5	44 cabinets (2 × 22)	32 cabinets (2 × 16)	44 cabinets (2 × 22)	24 cabinets (2 × 12)	40 cabinets (2 × 20)	20 cabinets (2 × 10)
PF6	32 cabinets (1 × 32)		25 cabinets (1 × 25)		22 cabinets (1 × 22)	

Moreover, the average power drawn from the grid does not necessarily reach the fixed peak limit.

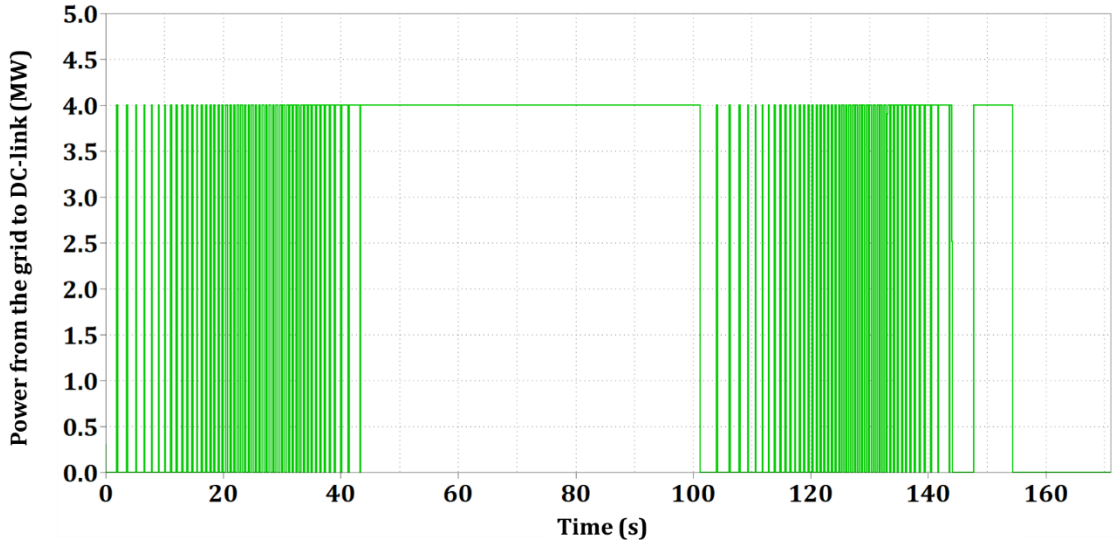

Figure 2.16 - Instantaneous power drawn from the grid by the PF1 & PF2 pair.

For example, Figure 2.16 illustrates the instantaneous power drawn by the PF1 & PF2 power supply pair with a P_{gridmax} of 2 MW per coil. It shows that the peak power is not constantly required, resulting in an average power of approximately 2.2 MW, half of the

allowed peak value. This observation indicates potential for further optimization in distributing the tokamak's electrical loads.

As a result of these findings, the DC storage system for the entire DTT PF power supply could be composed as follows:

- For P_{gridmax}= 2 MW: The system would consist of 14 (PF1) + 42 (PF3 & PF4) + 24 (PF5 & PF6) = 80 cabinets, occupying approximately 58 m², with an input power around 10 MW (6 coils at 2 MW peak each).
- For P_{gridmax}= 3 MW: The system would consist of 12 (PF1) + 32 (PF3 & PF4) + 20 (PF5 & PF6) = 64 cabinets, occupying approximately 46 m², with an input power around 15 MW (6 coils at 3 MW peak each).

These results are quite remarkable considering that the installed power capacity can exceed 500 MW.

2.8 Conclusions

This study focused on the design and optimization of a power supply system for the PF coils of a tokamak, using the DTT facility as a primary example. Although the analysis centered on DTT, the methodologies and conclusions are broadly applicable to all tokamaks and other nuclear fusion reactors.

The problem has been approached through both theoretical analysis and circuit simulations, which was made possible by establishing several foundational steps developed for the first time in this research:

1. Defining a Comprehensive Scenario: a voltage and current reference scenario that includes all plasma phases have been established, providing a realistic framework for the analysis.
2. Developing Analytical Formulas and Parameters: key analytical expressions and parameters necessary to set up and evaluate the optimization process effectively have been identified.
3. Creating a Circuit Simulation Model: a circuit model that incorporates all relevant tokamak phenomena has been designed, enabling accurate simulations of the PS system.

The models and algorithms developed, implemented in the PLECS software, are now available for future studies that may incorporate more detailed component behaviors and transient analyses. Notably, these models are planned to be integrated into a hardware-in-the-loop (HIL) setup, combining supercapacitor (SC) and H-bridge models with a real control board operating under the desired scenario.

Our findings highlighted the significant benefits of utilizing DC energy storage based on SC technology. With these advantages established, the focus shifted to finding the optimal balance between the size of SC banks and the power demand from the electrical grid. A novel concept introduced was the complementarity among the power and energy profiles of different PF coils, which proved crucial for optimization. By exploiting this complementarity through shared DC storage, grid power peaks can be limited via temporal shifts (compensating for demand fluctuations over time) and load balancing (distributing energy storage requirements across multiple PS units). This strategic use of available energy reduces the physical footprint of the DC storage and lowers both capital and operational costs, all without compromising performance, reliability, or stability standards.

A comprehensive simulation campaign revealed substantial benefits when sharing the DC storage bank between specific coil pairs, namely: PF1 & PF2 and PF5 & PF6. For the PF1 & PF2 pair, the shared storage configuration could potentially halve the size of the required storage bank. For PF5 & PF6, the reduction could be as much as two-thirds.

Additionally, analyzing the power demand from the grid showed that increasing the peak power limit from 1 MW to 2 MW leads to a more significant reduction in the required DC storage energy than increasing it from 2 MW to 3 MW. This finding suggests that a peak power limit of 2 MW offers the best balance between system dimensions and efficiency. In practical terms, using standard SC modules and cabinets, this translates to saving 18 cabinets for the PF system. The entire DC storage could then consist of either 80 cabinets occupying approximately 58 m² or 64 cabinets occupying about 46 m², depending on the configuration.

Looking ahead, trends in SC technology, independent of nuclear fusion applications, indicate that storage dimensions and costs are likely to decrease in the future. Batteries are expected to improve even more rapidly due to massive investments and the construction of gigafactories. Superconducting magnetic energy storage (SMES) is another promising technology that may be particularly suitable for fusion applications, facing optimization challenges similar to those of SC banks.

While the results of this study provide clear guidance for optimizing the DC storage and PS system, several practical considerations need to be addressed for real-world implementation. Future work should focus on detailed implementation plans, including validation tests. Additionally, exploring alternative topologies, such as boost converters or hybrid storage systems that combine SCs and batteries, could help overcome some intrinsic limitations identified in this study.

A significant practical issue is the layout of the DC link for connections to different PS units. This could introduce parasitic resistive and inductive effects that might negate the benefits of pairing the DC links. However, it is important to note that PS units in a pair can be divided into parallel units connected to smaller DC links, mitigating this concern.

Another practical aspect involves selecting the appropriate technology, such as insulated-gate bipolar transistors (IGBTs) or integrated gate-commutated thyristors (IGCTs), and deciding on the topology to use, like H-bridges or neutral-point-clamped (NPC) converters. The simulations in this study were based on a single H-bridge converter, focusing primarily on the DC storage rather than converter control. However, using parallel H-bridges may be necessary to handle higher power levels and provide redundancy. In such cases, interphase inductors play a crucial role in ensuring proper operation, balancing currents between parallel H-bridges, and preventing circulating currents that could lead to inefficiencies or potential damage.

Safety considerations are also paramount. The large amount of energy stored in the coils must be managed carefully. A braking system (chopper) should always operate in parallel with the SC banks to prevent overvoltages or overcharging. Clear detection of full discharge is required for maintenance and settings, which are frequent in fusion experiments. It is worth noting that while LICs offer advantages in specific energy, they present greater safety challenges.

Despite these considerations, this study presented viable strategies for addressing a critical issue, almost a showstopper, in the utilization of tokamaks as energy sources. The total power demand for the entire PF system was around 10 MW. Optimizing power exchange in this way can also mitigate other power quality issues affecting tokamaks, such as reactive power, harmonics, flicker, and oscillations.

Finally, it is important to emphasize that the analysis conducted was based on scenarios developed by plasma physicists without considering electrical power or energy optimization,

nor the option of a shared DC storage. Therefore, the results could be even more significant with an integrated approach that incorporates power and energy optimization requirements from the outset.

Based on the guidelines and results of this study, a call for tender for the realization of the DTT PF PS system is expected to be launched in 2025.

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Chapter 3

HIGH VOLTAGE PULSE GENERATORS

3.1 Introduction

Pulsed power technology is an essential field of study within engineering and physics, particularly in applications requiring the generation of extremely high voltages and large currents over very short durations. From its origins in flash radiography and X-ray generation, pulsed power has evolved significantly, finding uses in military, industrial, and medical domains [49],[50]. Modern pulsed power systems encompass a vast range of applications, from nuclear electromagnetic pulse (EMP) simulations and direct energy weapons to emerging techniques in biological and medical applications such as electroporation and plasma generation [49].

At its core, pulsed power technology relies on the principle of energy accumulation over relatively long periods, followed by rapid compression into high-power pulses. The energy can be stored over minutes and released in microseconds, or even shorter intervals, down to tens of nanoseconds or picoseconds [50]. This approach enables extremely high peak power outputs, with instantaneous power far exceeding the average power consumed during the charging phase. For example, pulsed power systems are capable of delivering pulse energies from 1 to 10^7 joules, peak powers of up to 10^{14} watts, and voltages ranging from 10^3 to 10^7 volts [49].

3.1.1 Historical Development of Pulsed Power

The development of pulsed power systems is deeply rooted in the exploration of electrical breakdown phenomena in insulating materials, such as gases, liquids, and solids. The fundamental observation that insulators can withstand higher electric fields when subjected to shorter pulse durations was well known before pulsed power formally emerged in the 1950s. Early work by Townsend, for example, elucidated the mechanisms of ionization and current growth in low-pressure gases. These early discoveries laid the foundation for the creation of devices such as the Marx generator, patented in 1923, which was instrumental in producing much higher voltages and shorter pulse durations than previously possible.

The subsequent development of pulsed power technology accelerated during the mid-20th century, particularly with the advent of the high-voltage accelerators. This shift enabled the development of machines capable of delivering pulses of up to 50 kA at 6 MV, significantly improving the resolution of radiographic systems and demonstrating the cost-effectiveness of pulsed power techniques.

Figure 3.1 – Marx generator built in 1961, currently at the High Voltage laboratory of the Technische Universität Darmstadt [51]

3.1.2 Core Principles of Pulsed Power Systems

The essential components of a pulsed power system include: a source of constant power, an input interface that transfers the energy from the source to a storage system under the shape of constant power, an energy storage system, an output interface that transfers the energy to the load under the shape of pulsed power, and a load [49],[50]. The output interface is the most critical block, because it has to handle high currents and voltages.

In Figure 3.2 it is depicted the generic block scheme of a pulsed power generating system.

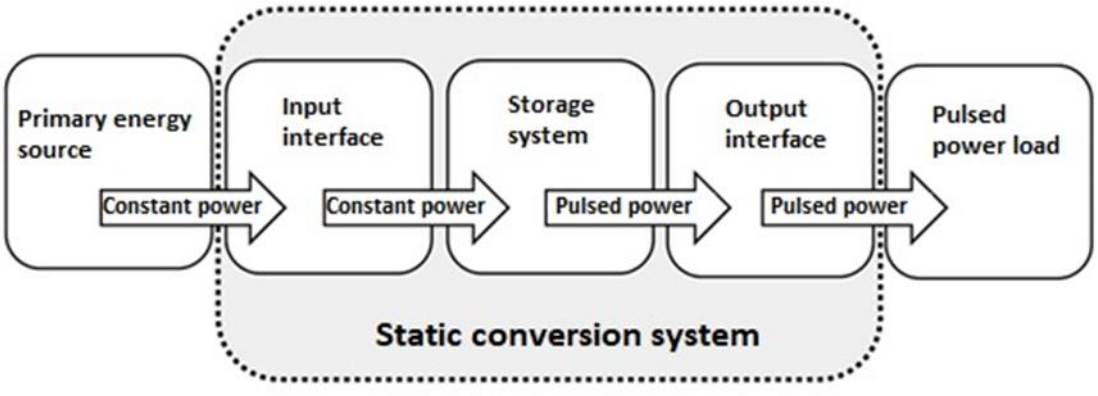


Figure 3.2 – Block scheme of generic pulsed power generating system.

The key to understanding pulsed power lies in its ability to exploit the time-dependence of electrical breakdown. The higher electric fields achievable with short-duration pulses allow pulsed power systems to be orders of magnitude smaller than continuous high-voltage systems, while still delivering immense power outputs [49]. For example, Marx generators, which remain one of the most widely used types of high-voltage pulse generators, can generate pulses with voltages as high as 18 MV [52], making them suitable for use in applications such as lightning simulators and multigigawatt pulsed power systems.

3.1.3 Advancements in HVPG Technology

Recent advancements in High Voltage Pulse Generators (HVPGs) have transformed the field of pulsed power. One of the most significant developments is the shift from traditional gas-discharge switches, such as thyratrons and spark gaps, to solid-state devices like Insulated Gate Bipolar Transistors (IGBTs) and Silicon Carbide (SiC) MOSFETs [53]. Solid-state technology offers superior reliability, efficiency, and precision in pulse generation, allowing for the production of arbitrary waveform pulses with sub-nanosecond rise times [53]. These advances have made HVPGs indispensable in fields requiring highly controlled pulses, such as plasma generation, biomedical treatments, and material processing.

Another key development is the increased use of pulse compression techniques, which allow energy to be stored over longer periods and then rapidly discharged to produce high-power pulses [54]. This method has enabled the design of more compact and efficient HVPG systems. Additionally, modern HVPGs are capable of operating at higher repetition rates, with some systems delivering up to 10,000 pulses per second [53].

3.1.4 Applications of HVPGs

The range of applications for HVPGs is vast and continues to expand as new technologies emerge. In the medical field, HVPGs are used in electroporation, where short, high-voltage pulses are applied to cells to temporarily permeabilize their membranes [55]. In industrial settings, HVPGs are employed in processes such as water purification [53], surface modification of materials, and the generation of non-thermal plasmas [56],[57]. These systems are also critical in defense applications, particularly in the development of directed energy weapons and EMP simulation [58].

Furthermore, HVPGs are central to scientific research, particularly in the study of high-energy physics. Machines capable of delivering millions of volts and passing hundreds of thousands of amperes for durations as short as nanoseconds are crucial for experiments involving particle accelerators, X-ray generation, and nuclear physics [59],[60].

3.2 Design of a 20 MW Peak Power Generator Prototype

The design and development of a high-voltage pulse generator (HVPG) capable of delivering 20 MW of peak power at 25 kV emerged as part of an ongoing OCEM initiative to create a versatile and compact pulse generation system. The demand for such systems is driven by the need for adaptable solutions that can meet the requirements of various applications without significant redesigns. Flexibility and the ability to repurpose the system across different fields with only minor modifications were key considerations in the project.

The primary challenge was to produce a pulse generator that could be efficiently adapted for use in multiple contexts, while maintaining a small form factor. Research and development efforts were aimed at ensuring that the generator would be compact enough to fit within the space-constrained environments typical of many research and industrial settings. This focus on compactness was particularly relevant for applications such as kicker magnets, which require fast, high-energy pulses but in some cases are limited by the available space within their operating environments.

Kicker magnets, commonly used in particle accelerators, represent one of the most demanding applications for high-voltage pulse generators [61]. These systems require precise and reliable pulses with rapid rise times to control beam steering [62]. The flexibility to reuse the generator in different scenarios, whether in research labs, medical applications, or defense technologies, was an important driver behind the project's direction.

Additionally, the ability to recycle the core design of the HVPG with only minimal adjustments for different applications further supports the long-term value of the system. This versatility offers the potential for expanded usage across various industries, ensuring that the system remains relevant and cost-effective over time.

For the prototype, the technical specifications for the pulse were internally defined based on previous experience with kicker magnets. These values were considered significant for ensuring the necessary performance, particularly in achieving fast, stable pulses suitable for beam steering applications and other similar high-voltage needs.

Table 3.1 – Main pulse parameters.

Pulse specifications	
Peak Power	20 MW
Peak Voltage	25 kV
Rise time	< 50 ns
Flat top duration	>100 ns
Fall time	< 150 ns

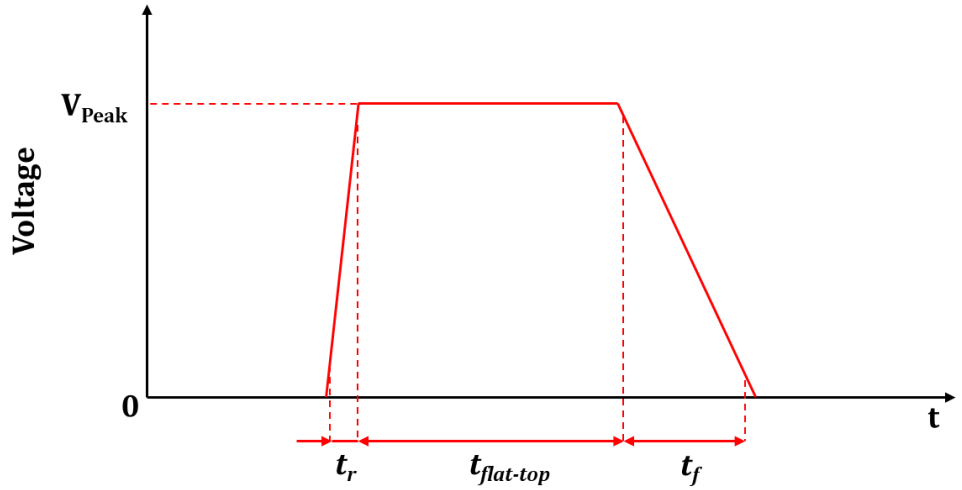


Figure 3.3 – Pulse waveform.

3.2.1 Selection of the Architecture

The selection of the architecture for the 20 MW peak power generator is influenced by several technical, logistical, and procurement challenges. The first step in the development of the generator is to select the most suitable architecture. This is accomplished through an evaluation of various designs based on key parameters such as space requirements, costs,

lead time for components, and procurement constraints. The goal is to find an architecture that can meet the performance requirements while complying with the logistical and practical limitations.

Several potential architectures are considered. The most relevant three solutions are the Marx architecture, the Blumlein architecture and an architecture based on a single HV switch.

Each of these architectures has been evaluated not only for its ability to meet the technical specifications, namely, 20 MW peak power, 25 kV peak voltage, and a rise time of less than 50 ns, but also for its feasibility in terms of space, cost, and component availability.

3.2.1.1 Marx Generator

The first architecture studied consists of a 25-stage Marx generator, powered by a 1 kV DC supply.

The Marx generator is an electrical apparatus designed to produce high-voltage pulses using low-voltage components. Conceived in 1924 by German physicist Erwin Otto Marx, this device leverages a specific arrangement of capacitors and switches to accumulate energy and subsequently release it in the form of a high-voltage pulse [49]. The Marx generator finds extensive application in fields that require brief, high-voltage pulses, such as insulation testing, particle acceleration, and plasma physics research.

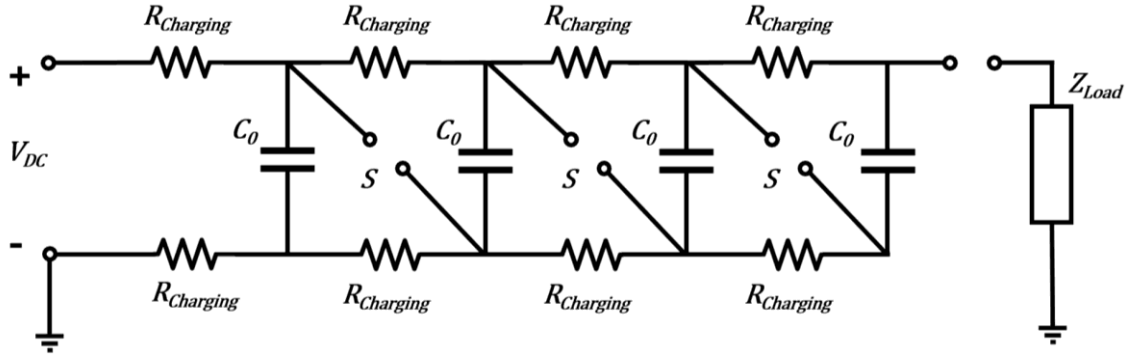


Figure 3.4 – General scheme of Marx generator.

Figure 3.4 shows the conceptual scheme of a 4-stage Marx generator. The Marx generator comprises some essential components:

- **Capacitors**: These devices store energy. For effective operation, the capacitors must have an adequate voltage rating to withstand the charging voltage and a low inductance to ensure rapid discharge with minimal energy loss.

- **Charging Resistors**: Serving as current-limiting components during the charging phase, these resistors also isolate the capacitors during the discharge phase.
- **Spark Gaps**: Acting as voltage-controlled switches, spark gaps are crucial for the rapid reconfiguration of the circuit during the discharging phase. They trigger when the voltage across them surpasses a predefined threshold, allowing for swift connection of the capacitors in series.

The operation of the Marx generator is founded on a two-phase process: the parallel charging of capacitors and their subsequent series discharging. This methodology enables the multiplication of the initial supply voltage, thereby generating a voltage pulse significantly higher than the input voltage.

During the charging phase, the capacitors in each stage (all with the same value of capacitance C_0) are charged in parallel through the charging resistors ($R_{charging}$) from the high-voltage DC source (V_{DC}). The resistors limit the charging current to prevent damage to the capacitors and ensure a controlled charging process. In this configuration, each capacitor charges up to the voltage level of V_{DC}, while the spark gaps (S) remain open due to the insufficient voltage to trigger a breakdown.

Once the capacitors are fully charged, the discharge phase begins. A trigger is applied to initiate the breakdown of the first spark gap, which creates a path for current to flow. As the spark gap closes, it connects the charged capacitors in series, causing their voltages to sum. This results in a high-voltage pulse across the load (Z_{load}). The total voltage across the load is ideally N × V_{DC}, where N is the number of stages (in this example, four). The capacitors discharge rapidly, transferring their stored energy to the load, generating the high-voltage pulse necessary for the application.

The swift switching action results in the generation of a high-voltage pulse of short duration. This pulse can be directed toward a specific load or utilized to produce intense electric fields necessary for various applications. The characteristics of the pulse, including its duration and waveform, are influenced by the properties of the circuit components, such as the capacitance of the capacitors and the inductance of the connections. Typically, the Marx generator achieves pulses in the microsecond to nanosecond range, which are suitable for the intended high-voltage applications.

The Marx generator offers several benefits that make it a preferred choice for generating high-voltage pulses. Its structural simplicity is notable, as the design utilizes standard components arranged in a modular architecture. This modularity facilitates scalability and customization based on specific requirements, making it adaptable to a wide range of applications.

Another significant advantage is its efficient voltage multiplication capability. The Marx generator achieves high voltages without the need for expensive or complex transformers, rendering it a cost-effective solution for high-voltage pulse generation. Additionally, its flexibility allows for the generation of various voltage levels and pulse durations by adjusting the number of stages and the characteristics of the components. This adaptability is particularly valuable in research and industrial settings where different parameters may be required.

For the application presented in this chapter, the Marx solution has been discarded due to the following major drawbacks:

- **Large Footprint**: The multi-stage design required significant space, which made it impractical given the size constraints of the system. The 25 stages needed a proper distance to avoid undesired discharges between them. This drawback could be avoided if other dielectric means were used instead of air, but this choice would have increased costs and complexity in manufacturing.

- **Synchronization**: The inclusion of 25 stages would have implied the need for precise synchronization of the switches, but a delay of some nanoseconds in the risetimes of the switches could have significant impact in slowing the rise time of the output pulse. Considering that two switches having the same part number still have some small differences, synchronizing the driving signals would have meant to shape a custom control signal for each switch. This would have caused the costs to increase significantly [53].

3.2.1.2 Blumlein line

The second architecture studied consisted of a Blumlein pulse forming network, encompassing 25 lines, powered by a 1 kV DC supply.

The Blumlein pulse-forming line, named after its inventor Alan Blumlein, is a circuit configuration utilized for generating high-voltage pulses with precise duration and amplitude [63]. Developed in the 1930s, the Blumlein line has become a fundamental component in

high-power microwave systems, radar transmitters, and pulsed power applications. Its ability to produce rectangular voltage pulses with sharp rise and fall times makes it particularly suitable in scenarios where pulse fidelity and timing are critical.

The operation of the Blumlein line is grounded in transmission line theory and the principles of electromagnetic wave propagation. Essentially, it consists of one or more transmission lines that are charged to a specific voltage and then rapidly discharged into a load, producing a pulse whose characteristics are determined by the properties of the lines and the load [49].

In its simplest form, a Blumlein line comprises two identical transmission lines connected in parallel and charged to a voltage V_{DC}. Upon triggering, a switch at one end of the lines closes, causing electromagnetic waves to propagate along the lines. Due to the specific configuration, the voltage across the load becomes two times the initial charging voltage V_{DC} during the pulse duration, effectively doubling the initial charging voltage.

The key to the Blumlein line's operation lies in the reflection and superposition of voltage waves within the transmission lines. When the switch closes, a voltage wave propagates down each line. At the end of the lines, these waves reflect back due to impedance mismatches, and their interaction results in a voltage pulse across the load with a duration equal to twice the transit time of the line. This mechanism allows for precise control over the pulse width and amplitude, making the Blumlein line an effective pulse-forming network.

The performance of the Blumlein line is dictated by its fundamental components, which include transmission lines, a high-voltage charging system, and a fast-switching mechanism.

The transmission lines are typically coaxial cables or parallel-plate structures designed to support high voltages and handle rapid voltage transitions. The characteristic impedance, length, and dielectric properties of the lines determine the pulse width, amplitude, and shape. High-quality dielectric materials are employed to minimize losses and ensure consistent pulse characteristics. The physical length of the lines is particularly crucial, as it directly influences the pulse duration; longer lines result in longer pulse widths.

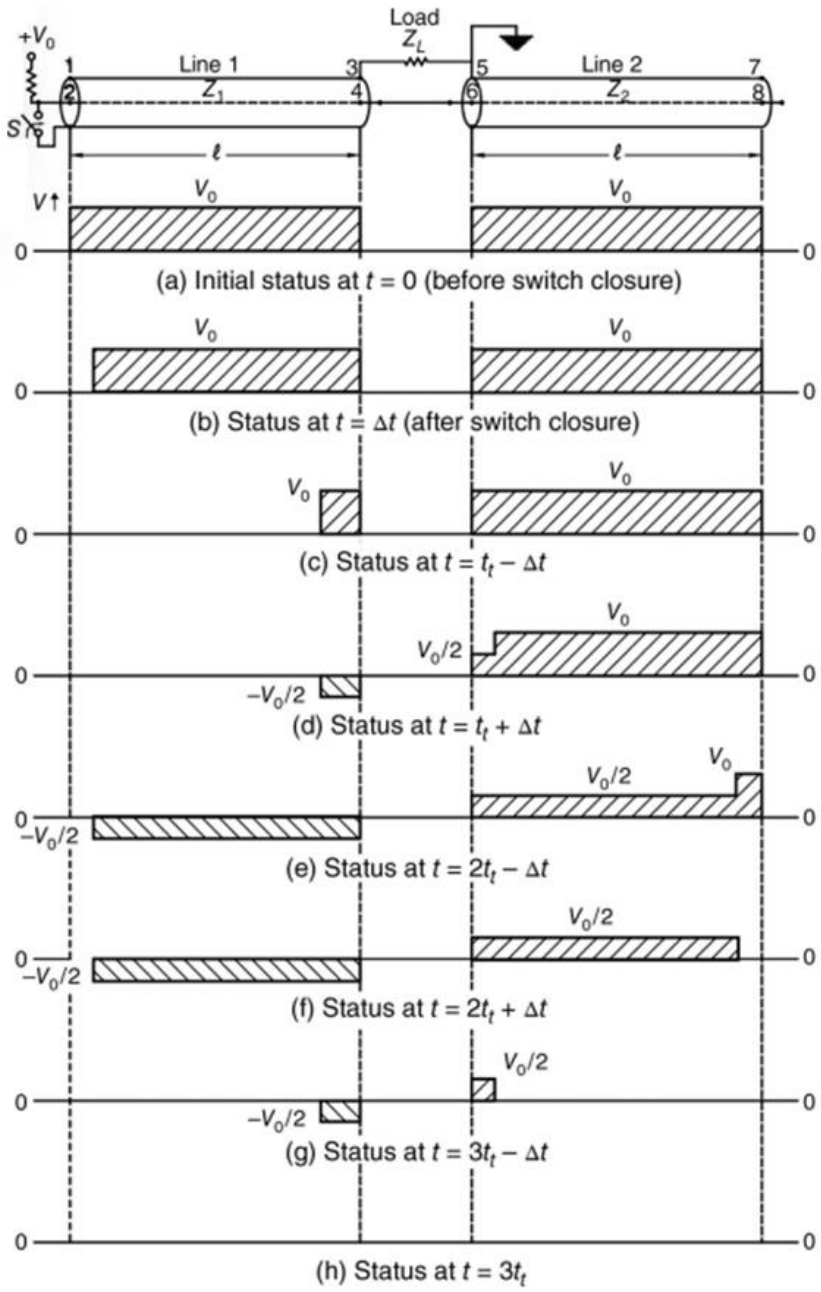


Figure 3.5 – Voltage wave dynamics across a Blumlein transmission line with matched impedance [49].

A critical component of the Blumlein line is the switch that initiates the pulse. This switch must close rapidly and withstand high voltages and currents. Common types of switches used include spark gaps, thyratrons, and solid-state devices like semiconductor switches. The performance of the switch directly affects the pulse rise time and overall fidelity. Fast switching ensures that the voltage wave propagates with minimal distortion, which is essential for maintaining the integrity of the pulse.

The charging system supplies the initial voltage V_{DC} to the transmission lines. It must provide a stable and precise voltage to ensure repeatable pulse characteristics. The charging circuit often includes resistive or inductive elements to control the charging rate and prevent overvoltage conditions. Adequate insulation and safety measures are essential in the charging system to handle the high voltages involved.

One of the primary advantages of the Blumlein line is its ability to produce high-voltage pulses with extremely fast rise and fall times and well-defined durations. The pulse shape is inherently rectangular, which is beneficial in applications requiring precise timing and amplitude control.

The Blumlein configuration effectively multiplies the charging voltage across the load during the pulse, allowing for higher output voltages without increasing the charging voltage. This voltage multiplication is achieved through the superposition of waves within the transmission lines, making it an efficient method for high-voltage pulse generation. Additionally, the Blumlein line provides excellent impedance matching with the load, reducing reflections and power losses. This efficient energy transfer enhances the overall performance of the system.

Furthermore, the predictable behavior based on transmission line theory facilitates precise control over the pulse parameters through careful selection of line characteristics. Adjustments to the line length, impedance, and dielectric properties allow engineers to tailor the pulse to specific application requirements. This level of control is advantageous in research and industrial environments where customized pulse profiles are often necessary.

The Blumlein solution was deemed unsuitable for the specific application due to several significant drawbacks:

- **Large Footprint**: The multi-stage design required an extensive amount of physical space, making it impractical given the system's size constraints. Specifically, the total length of the transmission lines necessary to produce the required pulse would have been several tens of meters.

- **Limited Flexibility**: A Blumlein pulse-forming network is custom-tailored to the load impedance and the specific pulse shape it needs to deliver. This specialization poses a risk if, during the project, the load parameters or the required pulse characteristics

were to change. Adapting the network to accommodate such changes would be challenging and could jeopardize the system's performance.

3.2.1.3 Single Stage Switching

The last architecture studied is based on a single stage, with a bank of capacitors acting as energy storage system and a high voltage power switch rated 50kV and 2400A.

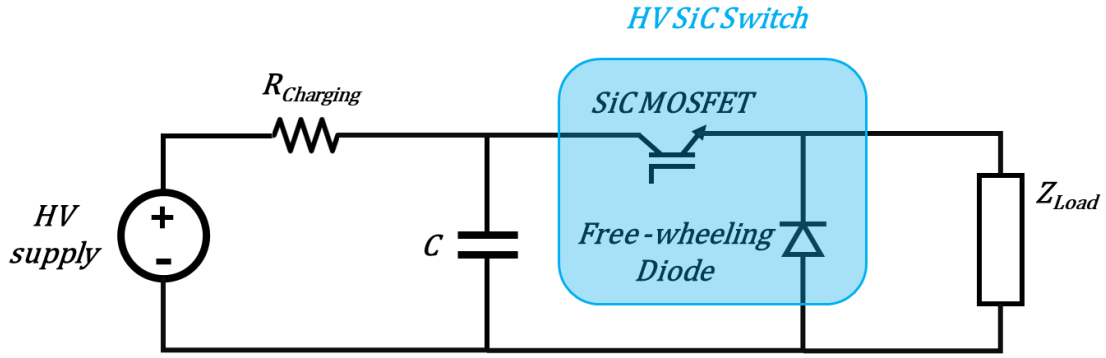


Figure 3.6 – Conceptual scheme of the single stage architecture with HV SiC Switch.

The advancement of power electronics has led to the development of HV power switches capable of handling extreme voltage and current levels. Silicon Carbide (SiC) MOSFETs have emerged as a promising technology for such applications due to their superior electrical and thermal properties compared to traditional silicon-based devices.

The HV power switch in question is designed to handle a blocking voltage of up to 50 kV and conduct currents up to 2400 A. This performance is achieved by arranging multiple SiC MOSFETs in series and parallel configurations (see Figure 3.7). Series connection is employed to withstand the high blocking voltage, while parallel connection allows for the distribution of current among multiple devices to handle the high current rating.

SiC MOSFETs are chosen for their wide bandgap, high critical electric field, and excellent thermal conductivity. These characteristics enable the devices to operate at higher voltages, temperatures, and switching frequencies than their silicon counterparts. The high critical electric field allows for a thinner drift layer, reducing on-resistance and conduction losses. The superior thermal properties facilitate better heat dissipation, which is crucial in high-current applications.

Designing an HV power switch rated at 50 kV and 2400 A using SiC MOSFETs involves significant complexity. The series and parallel connection of multiple devices require careful voltage and current balancing to prevent uneven stress distribution, which can lead to device

failure. Implementing proper gate drive circuitry and ensuring synchronized switching across all devices add to the design challenges.

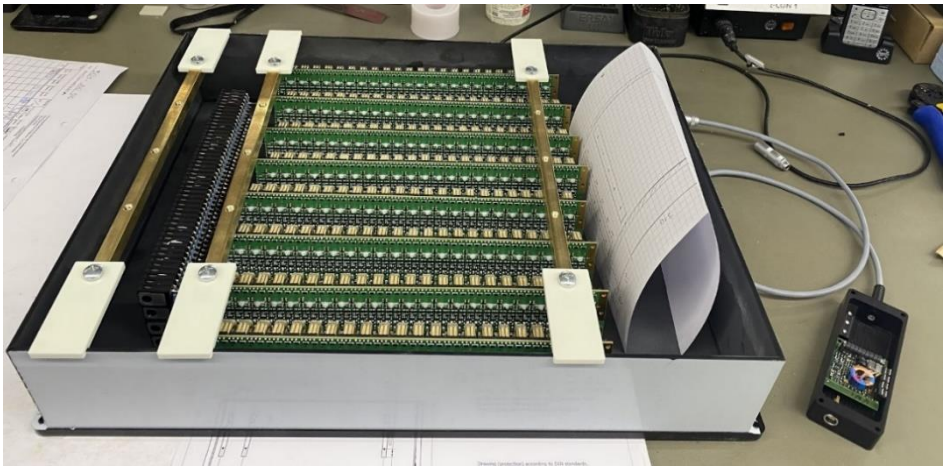


Figure 3.7 – Example of HV Switch during the manufacturing.

This architecture has the same flexibility of the Marx, but it is way more compact. Furthermore, the synchronization issue (still present, since the HV switch is made of several smaller switches arranged in series and parallel) is completely demanded to the external control unit purchased with the HV switch which does not require a specific trimming of the signals for each switch.

However, the decision to use a single stage architecture comes with certain trade-offs, particularly in terms of reliability. With respect to what has been said for the Marx Generator, the use of multiple smaller switches not only introduces a possible delay in the rising edge of the pulse but also increases the potential for failure, particularly under high-voltage conditions: if one switch fails, the entire array could become inoperable, leading to system downtime and the need for repairs.

The selection of the single-switch architecture for the 20 MW peak power generator is driven by practical considerations, including procurement challenges and the need for lower system complexity. Although this design introduces certain limitations in terms of reliability and performance, it provides a compact and feasible solution for generating high-voltage pulses under constrained conditions.

3.2.2 Core components

3.2.2.1 Capacitor Bank Design

Due to its prototype nature, the HVPG has been designed to be charged by an external low power HVDC generator, which is then decoupled from the HVPG during the discharge. Hence, the capacitive energy storage has been sized in such a way to provide the required amount of energy for three consecutive pulses with the constraint that the final voltage after the last pulse should not be lower than 20 kV, as follows:

$$E \approx N_p \times \frac{V_{peak}^2}{R} \times T_{pulse} = \frac{1}{2} C \left(V_{peak}^2 - V_{min}^2\right) \tag{3.1}$$

$$C \approx \frac{N_p \times \frac{V_{peak}^2}{R} \times T_{pulse}}{\frac{1}{2}\left(V_{peak}^2 - V_{min}^2\right)} \approx 250\, nF \tag{3.2}$$

where $\boldsymbol{E}$ is the energy stored, $\boldsymbol{N_p}$ the number of pulses, $\boldsymbol{V_{peak}}$ is the peak voltage of the first pulse, $\boldsymbol{V_{min}}$ is the voltage of the energy storage after the last pulse, $\boldsymbol{R}$ is the load resistance, and $\boldsymbol{T_{pulse}}$ is the period of the pulse.

To achieve a capacitance close to the one calculated in (3.2), 42 capacitors WIMA FKP1Y012205H, each rated at 220 nF and 6 kV, were arranged in a configuration of 6 capacitors in series to form a string rated for 36 kV, with 7 such strings connected in parallel.

In parallel to each capacitor, a 18 MΩ resistor has been placed for ensuring a proper voltage sharing in each string.

Figure 3.8 – Storage Bank made of 42 capacitors each with a paralleled resistor.

3.2.2.2 Switch Configuration

At the core of the system is the HV SiC switch, which controls the release of energy from the capacitor bank into the load. Although described as a “single-switch” system, the actual implementation consists of multiple smaller switches connected in series and parallel to handle the high voltage and current levels.

The HV switch is accompanied by a separate control unit, which is responsible for coordinating the switching signals of all the individual switches within the HV switch.

Figure 3.9 – HV SiC switch with its separated control unit

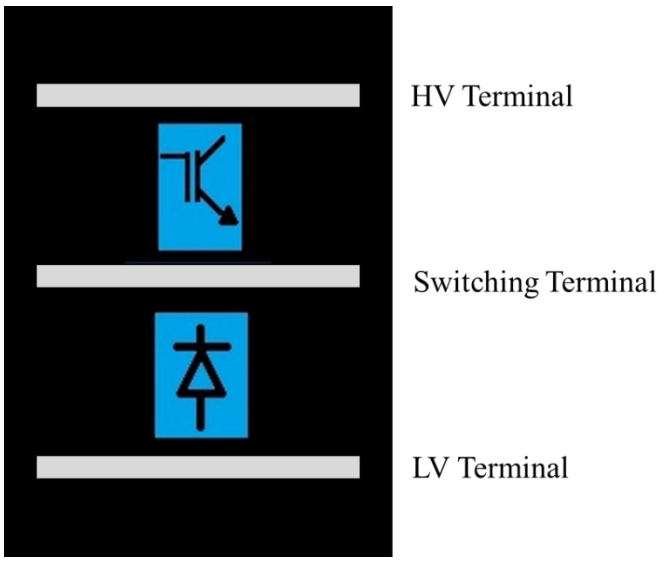


Figure 3.10 - Conceptual diagram of the HV SiC Switch

3.2.2.3 Energy Source

The system is powered by an high voltage DC supply model SPELLMAN SL70P1200/FG/ESL/230 capable of delivering up to 60 kV. This generator is limited in current, with a power rating of only 1.2 kW. Given these limitations, the HVDC supply is used just to charge the capacitor bank, ensuring that enough energy is available for the desired number of pulses, but it has not to be considered part of the prototype generator.

Figure 3.11 - Spellman SL70P1200/FG/ESL/230.

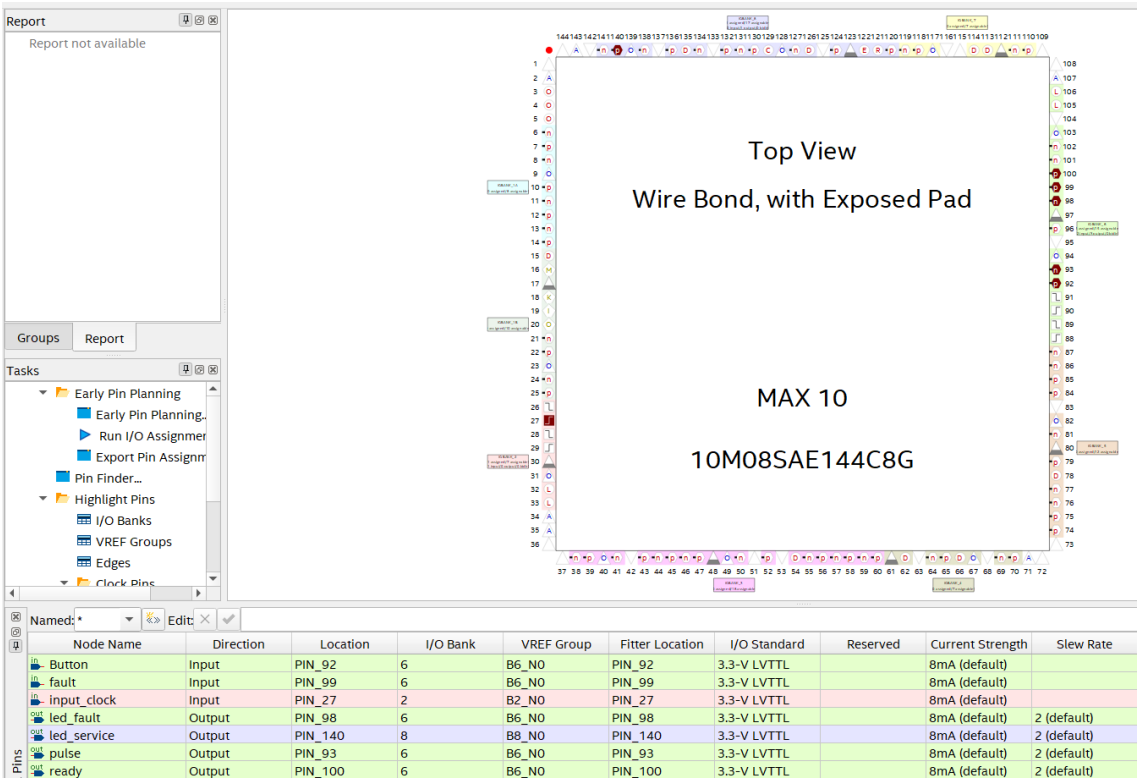
3.2.3 Signal generation

For the control system, specifically the generation of the pulse train using programmed logic, an Intel MAX 10 FPGA board, based on 55 nm integrated NOR flash technology, was selected (Figure 3.12). This board offers a range of configurable I/O banks, which are well-suited to this application. In particular, the development tool's pin planner screen shows that the I/O pin dedicated to generating the PWM signal is Pin 93, located on Bank 6.

Figure 3.12 – FPGA board Intel MAX 10 Aku Aku.

As shown in the Quartus development environment (Intel FPGA programming software) in Figure 3.13, additional pins are configured, such as the Button, which initiates the pulse

train generation with a period of 1 ms and an on-time (T_{On}) of 450 ns. After verifying the absence of faults (Pin 99), the green "ready" LED (Pin 100) is turned on. Once the pulse train is initiated, the "ready" LED is turned off. If a fault occurs during operation, the pulse generation is halted, and the red "fault" LED (Pin 98) is activated.



Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Slew Rate
Button	Input	PIN_92	6	B6_N0	PIN_92	3.3-V LVTTL		8mA (default)	
fault	Input	PIN_99	6	B6_N0	PIN_99	3.3-V LVTTL		8mA (default)	
input_clock	Input	PIN_27	2	B2_N0	PIN_27	3.3-V LVTTL		8mA (default)	
led_fault	Output	PIN_98	6	B6_N0	PIN_98	3.3-V LVTTL		8mA (default)	2 (default)
led_service	Output	PIN_140	8	B8_N0	PIN_140	3.3-V LVTTL		8mA (default)	2 (default)
pulse	Output	PIN_93	6	B6_N0	PIN_93	3.3-V LVTTL		8mA (default)	2 (default)
ready	Output	PIN_100	6	B6_N0	PIN_100	3.3-V LVTTL		8mA (default)	2 (default)

Figure 3.13 – Quartus screenshot.

To generate the appropriate switching signals, as well as the additional signals required for the correct operation of the system (such as fault indicators, LED control signals, etc.), two additional boards have been designed (see Figure 3.14).

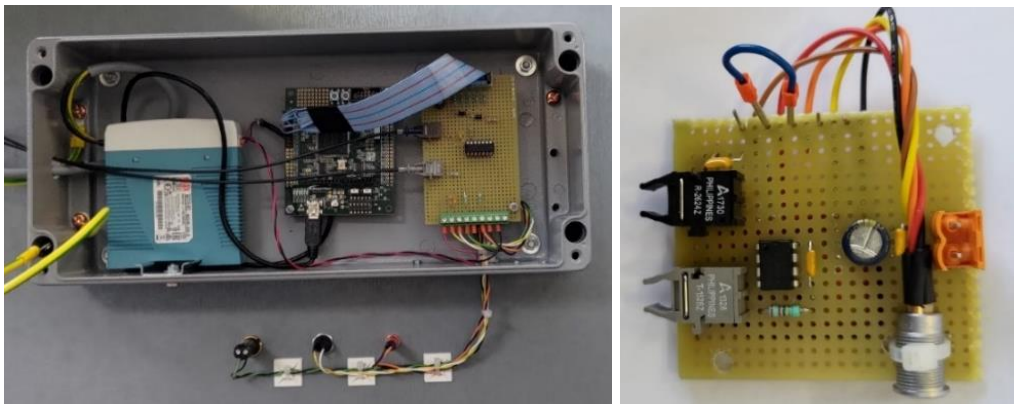


Figure 3.14 – Control architecture: on the left the crate encompassing a 24V supply, the FPGA board and the internal buffer board; on the right the external buffer board.

The first buffer board (from now on called Internal buffer board) is placed inside the crate and has the task of putting in communication the trigger button and the LEDs with the FPGA Board, the other buffer board (from now on called External buffer board) is placed outside the crate and has the task of putting in communication the separated control unit with the FPGA board.

This architecture is based on the Intel FPGA board, and additional buffer boards are integrated to interface between the FPGA and the control unit of the SiC device.

3.2.4 Layout optimization

In this application, the impact of parasitic inductance is particularly significant, and its minimization is crucial to achieve the desired performance.

Figure 3.15 – HV Switch with DC storage frame.

Parasitic inductance, if not properly controlled, can lead to slower rise times and distorted pulses, which directly affect the efficiency and reliability of the system. Due to the experimental nature of the generator, many improvements were implemented during the development process, with their effectiveness determined empirically through testing and iteration.

One of the most critical steps taken to minimize inductance was optimizing the physical layout of the components. Specifically, the terminals of the storage bank were positioned as close as possible to the terminals of the switch. This adjustment reduced the length of the conductive paths and, as a result, the parasitic inductance within the circuit. To facilitate this

improvement, a custom frame for the capacitor bank was designed and constructed, ensuring that the components were securely mounted in close proximity to the switch.

Another measure that contributed to reducing parasitic effects was the implementation of a distributed load. Instead of using a single 30-ohm resistor, the load was distributed across five 150-ohm resistors connected in parallel. This configuration not only improved current distribution but also minimized the inductance associated with the load, resulting in more stable pulse performance.

Figure 3.16 – HV SiC Switch with snubber and Distributed load at its terminals.

In addition, an aluminum ground plane was installed as part of the layout optimization. This ground plane helped facilitate the closure of the current loop, which further minimized inductive effects by providing a low-impedance path for the return current. These modifications, though incremental, significantly improved the overall performance of the generator, highlighting the importance of careful layout design in minimizing parasitic inductance.

Figure 3.17 – Aluminum ground plane.

3.2.5 Operation

The operation of the generator follows a series of steps. Initially, the auxiliary systems powered by 230V are turned on, after which the HV supply is activated. The voltage is gradually increased to the desired level, allowing the capacitors to charge through decoupling resistors that limit the charging current. Once the storage bank has reached the target voltage, the pulse is triggered. Following the pulse, the power supply recharges the storage bank to the designated voltage level. At the end of the operation, the high-voltage power supply is switched off, and the storage bank is safely discharged.

3.3 Experimental Tests

This section presents the most significant results from the experimental test campaign conducted on the prototype generator. Given the experimental nature of the generator and the complexity of the system, the testing process was essential not only for evaluating the generator's performance but also for identifying areas where layout improvements could be made. The challenge of constructing reliable simulation models for such high-speed pulse applications, particularly those with extremely fast rise times, meant that many of the tests were performed to empirically determine the effectiveness of design modifications.

The generator's rapid rise times and high voltage necessitated a cautious approach to testing. It was considered unsafe to begin testing at the full target voltage of 25 kV. Therefore,

the tests were carried out incrementally, starting at a lower voltage of 5 kV and increasing in 5 kV steps. This gradual testing approach allowed for careful monitoring of system performance at each stage, reducing the risk of damage and ensuring that any issues could be addressed before reaching higher voltage levels.

3.3.1 Setup

In the experimental setup, the configuration was adjusted to accommodate the prototype nature of the system. Specifically, the control crate, which houses the electronics and control systems, was positioned outside the main cabinet to allow easier access for monitoring and adjustments during the tests. Additionally, the high-voltage generator, responsible for charging the storage bank, was placed behind the HVPG cabinet. However, as one can see in Figure 3.19, there is enough space inside the cabinet to fit the control crate and a HV supply, so, when the prototype is validated in terms of performance, the next step is to fit the devices inside the cabinet.

Figure 3.18 – Test setup.

Figure 3.19 – HVPG cabinet.

Figure 3.20 represents the principal blocks and their respective connections in the experimental setup. The control crate, powered by a 230V supply, generates a drive signal and is connected to the external buffer board via a pair of optical fibers—one fiber transmits the drive signal, while the other receives a fault signal, if present. The external buffer board then communicates with the separated control unit of the HV SiC switch through a LEMO 4-pin cable. The separated control unit is responsible for managing communication with the HV SiC switch itself.

In the upper-right portion of the figure, the HV supply block is shown, connected to a group of four charging resistors with an equivalent resistance of 10 MΩ via a high-voltage power cable rated for up to 100 kV DC. These resistors are included to limit the charging current, ensuring that the HV power supply does not reach its power limit, which would

trigger its protection mechanism. The other terminal of the charging resistors is connected, also via an appropriately insulated cable, to the HV terminal of the HV SiC switch.

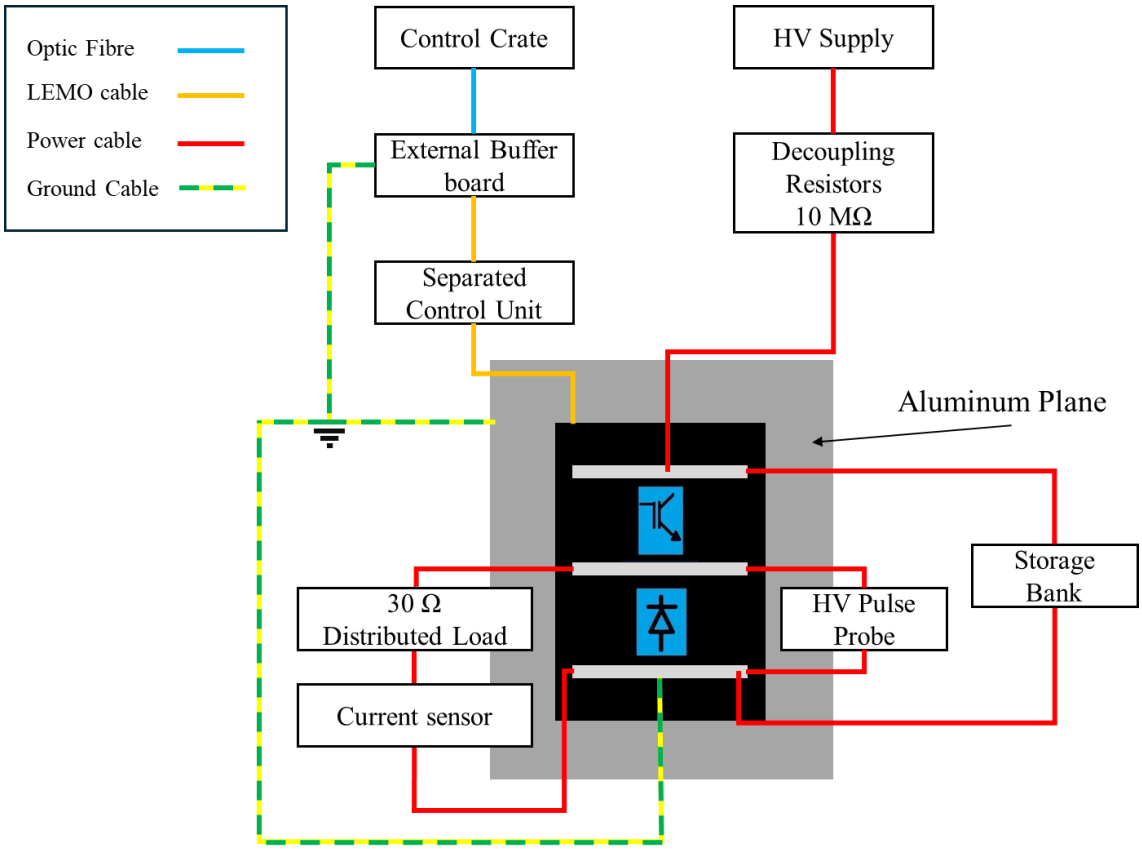


Figure 3.20 – Block scheme of testing layout.

Looking at the terminals of the HV SiC switch, it can be observed that the capacitor bank is connected between the HV terminal and ground, while the load is positioned between the middle terminal and ground. In parallel with the load, a high-voltage pulse probe is placed, while a current sensor is connected in series with the load. More specifically, given the distributed load across five branches, the current sensor is placed on one of the five branches, so the measured current represents one-fifth of the total current.

Finally, an aluminum plate, serving as the ground plane, is positioned behind the HV SiC switch to facilitate the closure of the return current loop.

3.3.2 Test at 5kV

The pulse shape obtained in the 5 kV test is reported in Figure 3.21. The results were positive. The rise time of the pulse was approximately 25 ns, and the pulse maintained a stable flat top with only a slight oscillation. The fall time was also relatively fast, 40 ns.

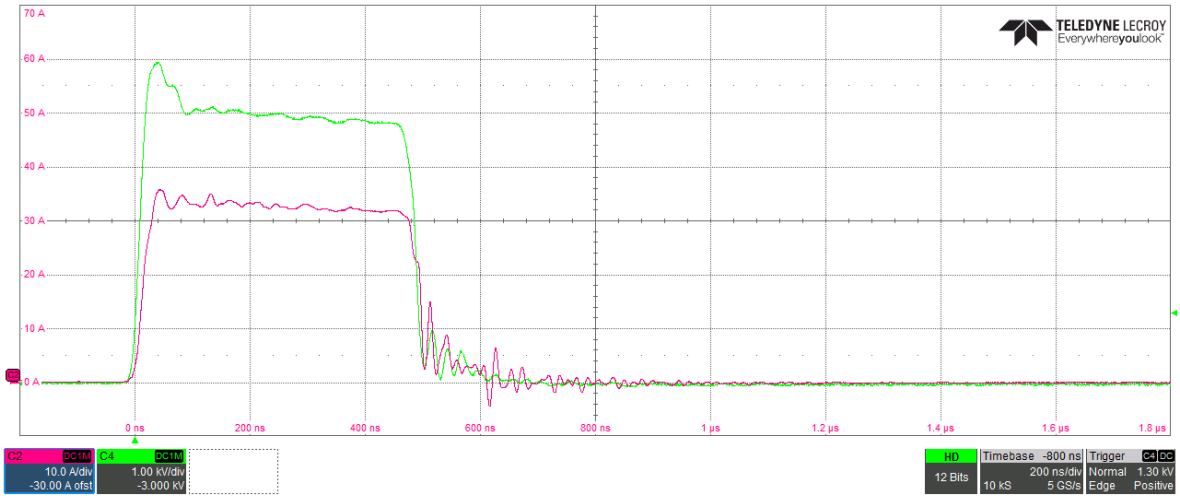


Figure 3.21 – 5kV pulse voltage (green) and current (red). 200 ns/div.

Given the satisfactory performance of this test, the decision was made to proceed to the next voltage level, 10 kV.

3.3.3 Test at 10kV

The 10 kV test also yielded positive results. The rise time of the pulse was approximately 30 ns, and the fall time was around 45 ns.

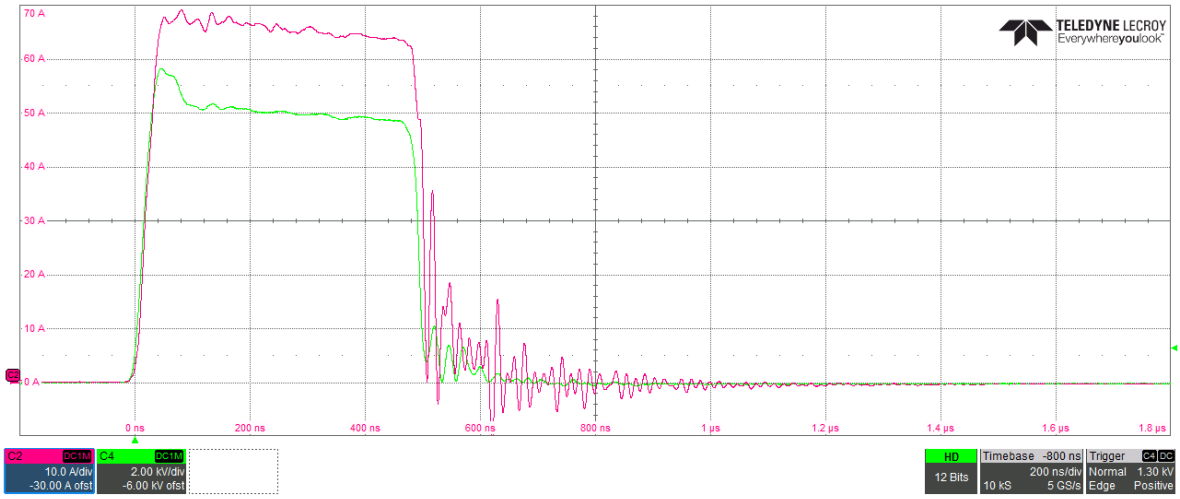


Figure 3.22 – 10kV pulse voltage (green) and current (red). 200 ns/div.

Given the successful outcome of this test, the decision was made to continue testing at the next voltage level.

3.3.4 Test at 15kV

The 15 kV test also yielded positive results. The rise time and the fall time were comparable to the ones obtained during the 10 kV test (around 30 ns for rising and 45 for falling). As in the previous test, the pulse maintained a stable flat top.

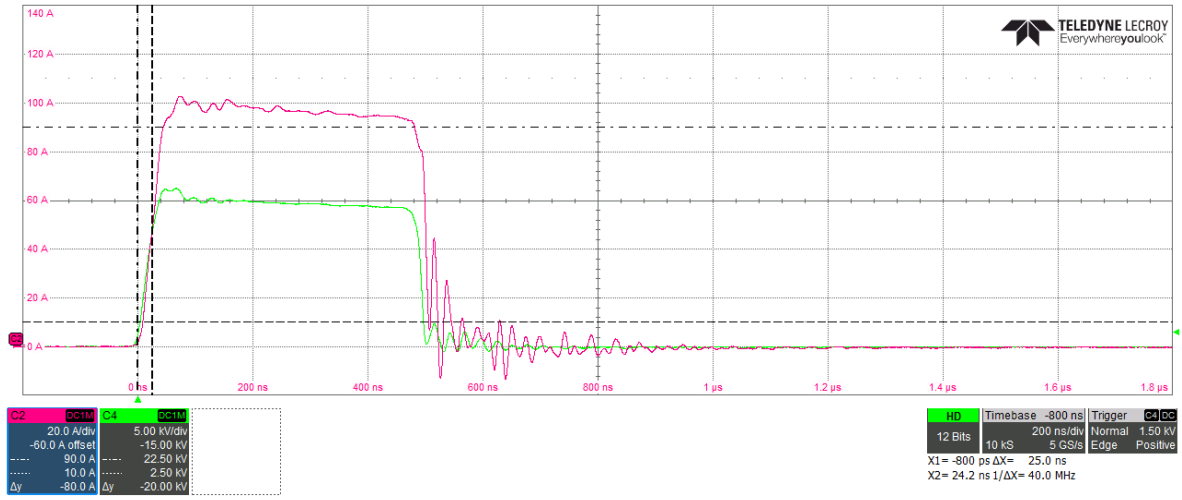


Figure 3.23 – 15kV pulse voltage (green) and current (red). 200 ns/div

Given the successful outcome of this test, the decision was made to continue testing at the next voltage level.

3.3.5 Test at 20kV

The 20 kV test proceeded well, with a rise time of approximately 40 ns, a stable flat top, and a fall time of 80 ns. Although the fall time was acceptable, it was noticeably slower than in previous tests.

Figure 3.24 – 20kV pulse voltage (green) and current (red). 200 ns/div.

The slower falling time underlines an increased difficulty in turning off for the HV switch. It was then decided to measure the voltage overshoot between the HV terminal of the switch and the ground during the switch opening. The voltage overshoot during the opening is a common occurrence in power switches. This happens due to the parasitic inductance reacting to the sudden change in current. In this case, the measured overshoot did not cause any concern.

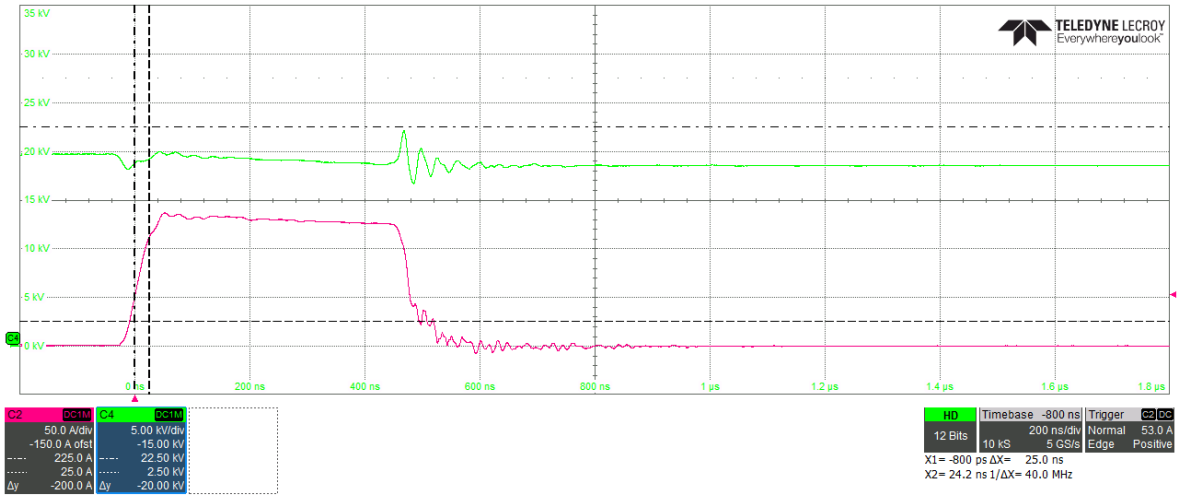


Figure 3.25 - 20kV pulse switch opening voltage (green) and current (red). 200 ns/div.

Given the successful outcome of this test, the decision was made to continue testing at the next voltage level.

3.3.6 Test at 25 kV

The final test at 25 kV, which represented the target voltage for the system, demonstrated the generator's ability to meet its design specifications under full operating conditions. The rise time of the pulse was measured at less than 50 ns, indicating that the system could achieve the required fast pulse initiation. The flat top remained stable throughout the pulse, confirming the generator’s ability to maintain the necessary voltage levels without significant fluctuation.

However, the fall time extended to approximately 100 ns, which marked a further increase compared to previous tests, while still within acceptable limits.

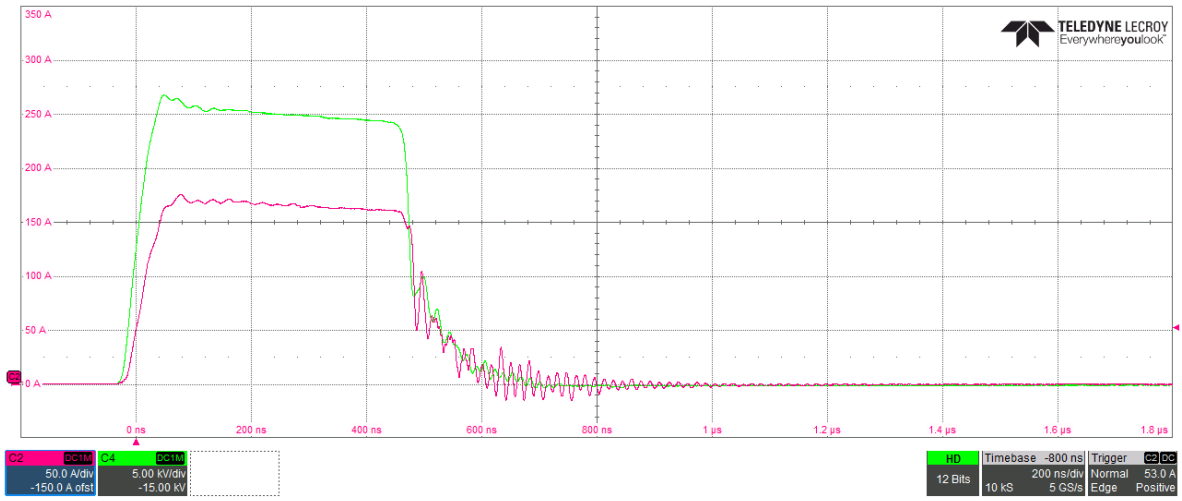


Figure 3.26 – 25kV pulse voltage (green) and current (red). 200 ns/div.

This prompted a closer examination of the switching behavior, particularly during the opening phase of the switch. For this reason, the voltage overshoot at the HV terminal was measured again during the switch opening, as it had been during the 20 kV test. As expected, the overshoot remained minimal and posed no risk to the system's operation.

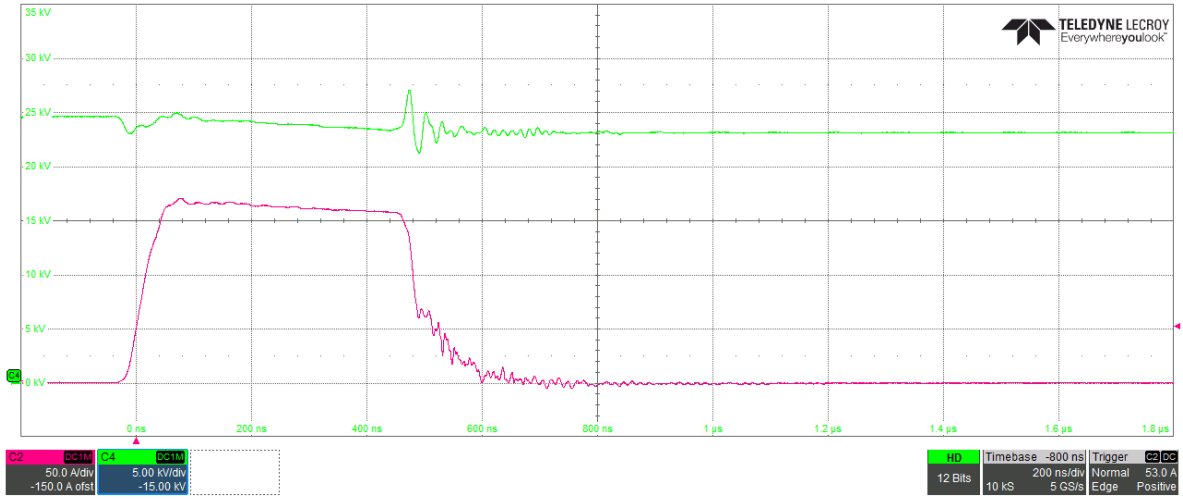


Figure 3.27 - 25kV pulse switch opening voltage (green) and current (red). 200 ns/div

3.4 Analysis of Test Results and Future Paths

The HVPG developed for this project successfully met its performance targets, delivering the required 25 kV peak voltage, 20 MW peak power, and maintaining the compact design essential for the intended applications. However, during the test campaign, a critical reliability issue was encountered when the HV SiC switches failed. The fault of this switch

halted testing temporarily. The testing could be completed only after purchasing a replacement. While the overall results of the tests were positive, this incident highlighted the need for a more reliable architecture moving forward.

Looking to the future, the focus will shift towards developing a compact Marx generator. This design has the potential to offer improved reliability but will require a significant increase in resources to achieve the desired performance. Specifically, perfect synchronization between stages will be essential to ensure proper functionality. Additionally, replacing air with higher-performing dielectrics will be necessary to compress the stages into a smaller footprint, allowing for both the compactness and robustness required by the application. This next phase of development will be a more resource-intensive endeavor, but it is a critical step towards overcoming the limitations encountered with the current HVPG design.

Chapter 4

NEW THEORETICAL FRAMEWORK FOR MODULAR MULTILEVEL CONVERTERS

4.1 Introduction

The Modular Multilevel Converter (MMC) has become a widely adopted technology in power electronics, particularly for applications requiring high efficiency, flexibility, and scalability. Introduced by Professor Marquardt in the early 2000s, the MMC uses a modular architecture where numerous submodules (SMs) are connected in series to form the converter's arms [66]. This configuration allows for precise power conversion and handling of large voltages and currents, making it well-suited for modern power systems[67]. Each SM can be independently controlled, providing the MMC with the capability to generate high-quality output waveforms, which is essential in many energy applications.

As power systems evolve with the integration of renewable energy sources, electric vehicles, and distributed generation, there is an increasing need for converters that can manage energy flows efficiently while ensuring high power quality. The MMC's modularity and scalability position it as a key technology to meet these demands. Its application spans areas such as high-voltage direct current (HVDC) transmission[68],[69], motor drives[70], and renewable energy integration, with a focus on providing reliable and efficient power conversion [71],[72],[73],[74].

4.1.1 MMC Applications

MMC technology is particularly valuable in HVDC transmission systems, which are essential for long-distance power transfer and grid interconnection [75],[76],[77]. HVDC systems allow for the transmission of significant amounts of power over long distances with minimal losses. Traditionally, line-commutated converters (LCCs) were used in these systems, but LCCs faced challenges related to limited control flexibility, harmonic distortion, and power quality[78]. MMCs address these challenges by producing higher-quality voltage waveforms with reduced harmonic content, improving overall system efficiency [78].

Several HVDC projects around the world have adopted MMC technology to enhance grid stability and enable the integration of renewable energy sources [79].

In medium-voltage motor drives, MMC technology has become increasingly valuable for enhancing motor performance [70]. MMC-based drives provide precise control over motor speed and torque by improving output waveform quality, which is critical for medium- and large-sized motors [80]. Traditional two-level or three-level converters often exhibit limitations such as high switching losses and poor waveform fidelity, leading to increased stress on motor windings. In contrast, MMCs minimize these issues by producing cleaner, more sinusoidal waveforms, reducing harmonic distortion and allowing the motor to operate more efficiently. This leads to extended motor lifespans, lower maintenance needs, and better overall system performance, especially in applications requiring continuous or high-power operation, such as in pump, compressor, and conveyor motor drives.

The role of MMCs in renewable energy systems is also significant. In wind energy systems, turbines generate variable AC power that must be converted into a stable form for transmission or storage [73]. The MMC's ability to handle fluctuating input conditions while maintaining high power quality makes it an important component in wind energy conversion systems. Similarly, in photovoltaic (PV) systems, the MMC efficiently manages the power output from solar panels, ensuring compliance with grid requirements[72].

Beyond these established applications, MMCs are also being explored for use in electric vehicle (EV) charging infrastructure, energy storage systems, and solid-state transformers [71]. The growing adoption of electric vehicles has led to increased demand for fast-charging stations, where MMCs provide efficient and high-power charging solutions [74]. In energy storage systems, MMCs manage large power flows, particularly in systems utilizing supercapacitors or batteries, and offer modularity that improves the integration of storage with renewable energy. For solid-state transformers, MMCs are being investigated for their potential to provide efficient power conversion across different voltage levels.

4.1.2 Challenges in MMC Operation

Despite their advantages, MMCs face operational challenges, with circulating current management being one of the most critical. A circulating current flows within the converter's internal structure, particularly between the upper and lower arms, but it does not contribute

to the output power. This current can affect the converter's efficiency and stability, and controlling it is essential for optimal performance [81],[82],[83].

In the early stages of MMC development, circulating current was seen as an undesirable effect that needed to be minimized to reduce losses and prevent voltage imbalances across the SMs [84]. Methods such as increasing the arm inductance were employed to limit circulating current, but this approach increased the converter's size and cost. Proportional-integral (PI) controllers were also used to suppress circulating current, providing effective control during steady-state operation. However, PI controllers can struggle with dynamic performance when operating conditions change rapidly, leading to inefficiencies in certain scenarios.

4.1.3 Advancements in MMC Control Strategies

Recent advancements in MMC control strategies have focused on actively managing circulating current to enhance converter performance [85]. An approach is model predictive control (MPC), which uses a system model to predict future behavior and optimize control inputs [86],[87]. In MMC applications, MPC can predict the behavior of circulating current and adjust the switching states of the SMs to minimize losses and improve efficiency. MPC is more suited to dynamic conditions compared to traditional PI controllers, as it can handle multiple variables and constraints [88].

Direct power control (DPC) is another approach that focuses on controlling the active and reactive power output of the MMC [89]. By managing the power flow, DPC reduces circulating current and improves the converter's response to changes in power demand. This method is particularly useful in applications that require fast and accurate power control, such as renewable energy integration and grid support.

In addition, adaptive control techniques have been developed to improve the converter's response to varying operating conditions. Adaptive control continuously adjusts control parameters based on real-time measurements, enabling the converter to respond effectively to changes in load or input conditions [90],[91]. This approach is beneficial in maintaining system stability and performance in complex power systems.

4.1.4 Focus of the Chapter

This chapter introduces a theoretical framework for controlling MMCs using time-scale analysis [92] and orthogonal functions [93]. Time-scale analysis separates fast and slow dynamics within the converter, allowing for optimized control strategies that address both short-term fluctuations and long-term stability. By decoupling these dynamics, the proposed control approach aims to improve the overall performance and reliability of MMCs.

The chapter first outlines the basic topology of the MMC and develops the mathematical model that underpins the control strategy. It then discusses the control objectives and introduces the two-time scale analysis method used to decouple the control of the upper and lower arms. Simulation and experimental results are also presented to demonstrate the effectiveness of the proposed strategy. Finally, the chapter concludes with a summary of key findings and potential future research directions.

4.2 MMC Topologies

Two of the main strengths of MMCs are modularity and flexibility. The architecture of an MMC allows for various SM topologies [94], each suited to specific applications and operational requirements. The selection of an appropriate topology directly influences the performance, efficiency, and complexity of the converter. This chapter discusses the most widely used MMC topologies, examining their structures, benefits, and typical areas of application.

The half-bridge SM is one of the simplest and most commonly utilized topologies in MMC designs. Each half-bridge SM consists of two power semiconductor switches, typically IGBTs, along with associated diodes arranged in a half-bridge configuration. This configuration also includes a capacitor that stores energy and regulates voltage. The half-bridge topology functions by inserting or bypassing each SM depending on the state of its switches, which simplifies control and operational processes. The ability of the half-bridge topology to generate multilevel output voltage through the series connection of SMs results in high-quality waveforms. The number of voltage levels produced depends on the number of SMs per arm, directly impacting the quality of the converter's output.

Applications of the half-bridge topology are widespread in areas where fault-blocking capability is not critical, such as medium-voltage motor drives and renewable energy systems where DC fault conditions can be managed by other means [96]. The simplicity of the half-

bridge design, along with its reduced component count, contributes to lower losses and ease of implementation. The control schemes for half-bridge MMCs are well-established and generally less complex than those required for other topologies. However, a key limitation of the half-bridge topology is its inability to generate negative voltages and block DC fault currents, which restricts its use in applications requiring fault-tolerant operation, such as HVDC transmission systems without additional protection measures [88],[96].

In contrast, the full-bridge SM topology provides greater control over voltage output by including four power semiconductor switches. This enables each SM to produce both positive and negative voltage levels, offering more flexibility in voltage control. The full-bridge topology is particularly valuable in applications that demand the ability to block DC fault currents, such as offshore HVDC systems or high-reliability grids. By controlling current during fault conditions, the full-bridge topology enhances system stability and safety. The use of full-bridge SMs allows converters to manage positive and negative voltage outputs, offering improved fault tolerance and operational reliability. Despite these advantages, the full-bridge topology comes with increased complexity, as it requires more switching components, which can lead to higher costs and greater power losses. The control strategies for full-bridge MMCs are also more sophisticated, adding to the design challenges. Nevertheless, the ability to block DC fault currents makes the full-bridge topology a preferred choice for demanding applications where system protection is critical.

Beyond the half-bridge and full-bridge configurations, several alternative SM topologies have been proposed to fulfill different objectives in MMC applications [97],[98],[99]. One such topology is the Modified Active-Neutral-Point-Clamped (ANPC) SM, which acts as a lower-loss option in applications where unipolar voltage output is sufficient. The ANPC SM combines features of both half-bridge and neutral-point-clamped topologies to achieve improved efficiency and reduced semiconductor losses, making it suitable for medium-voltage applications where efficiency is a priority.

Bipolar SMs like the Cross-Connected SM (CCSM) and the Clamped Double SM (CDSM) provide general fault-blocking capabilities and controllable negative voltages similar to the full-bridge topology but with a reduced component count. The CCSM achieves this by cross-connecting two half-bridge circuits, allowing it to generate both positive and negative voltage levels while using fewer components than a traditional full-bridge SM. Similarly, the CDSM uses a clamping diode arrangement to enable negative voltage

generation and DC fault blocking, offering a compromise between the complexity of full-bridge and the simplicity of half-bridge topologies.

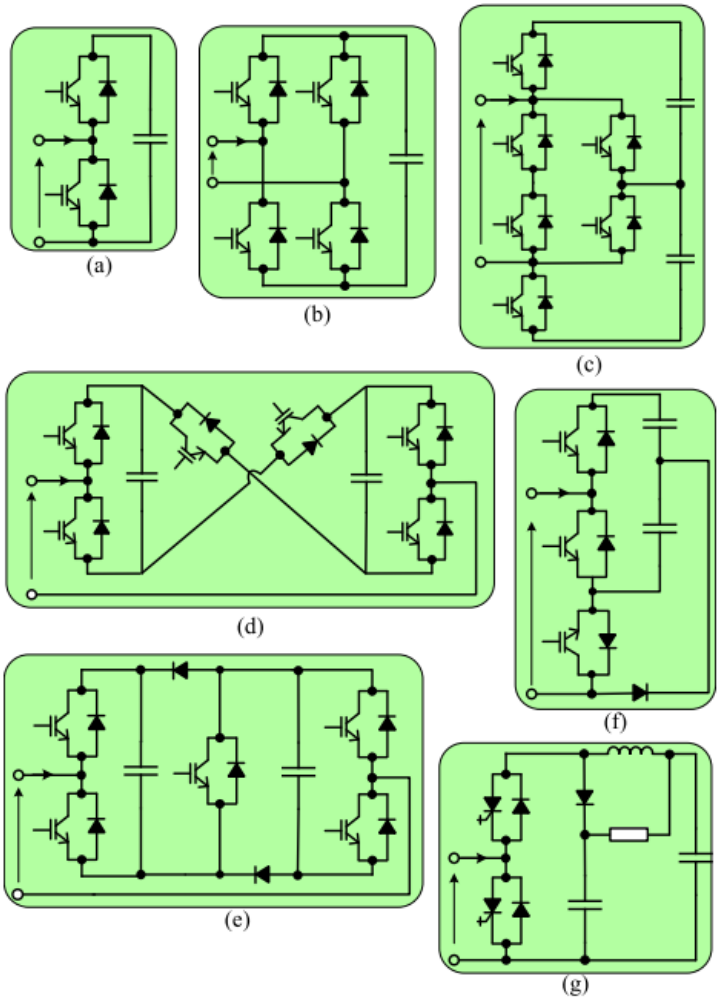


Figure 4.1 - MMC submodules: (a) half-bridge submodule, (b) full-bridge submodule, (c) modified ANPC submodule, (d) cross-connected submodule (CCSM), (e) clamped double submodule (CDSM), (f) single-clamped submodule (SCSM), and (g) IGCT submodule [88].

The Single-Clamped SM (SCSM) defines a family of SMs equipped with bypass clamping diodes that facilitate fault clearing in MMCs. The inclusion of clamping diodes allows the SCSM to handle DC fault conditions more effectively than the standard half-bridge SM, providing an additional layer of protection without significantly increasing complexity or cost. This makes the SCSM an attractive option for applications where enhanced fault management is desired without the full overhead of a full-bridge design.

Additionally, SMs based on Integrated Gate-Commutated Thyristors (IGCTs) offer higher efficiency, voltage ratings, and reliability. IGCT-based SMs are characterized by their low

on-state voltage drop and high current-carrying capability, which result in reduced conduction losses and improved overall converter efficiency. Their robustness and reliability make them suitable for high-power applications where long-term operational stability is crucial.

Mixed SM topologies, which incorporate combinations of these various SM types, offer a balanced approach to meeting specific application requirements [88]. By selectively integrating different SM topologies within the same converter, designers can optimize for cost, efficiency, fault tolerance, and complexity. For example, a converter might use a majority of half-bridge SMs for efficiency and simplicity, supplemented by a smaller number of full-bridge or clamped SMs in strategic locations to provide fault-blocking capabilities.

In typical mixed topologies, a portion of the SMs in each arm consists of advanced units like full-bridge, CCSM, or CDSM SMs, with the majority being half-bridge units. This arrangement reduces the number of components required while still providing enhanced fault tolerance when necessary. Mixed topologies are frequently used in systems where DC faults are infrequent but must still be addressed if they occur. HVDC transmission systems are a prime example where mixed SM topologies may be employed, allowing for high efficiency during normal operation while retaining the ability to manage faults effectively. While these topologies reduce costs compared to full-bridge designs, they still require more sophisticated control schemes to balance the differing SM configurations and ensure efficient operation under varying conditions.

The choice of MMC topology depends largely on the specific requirements of the application. The half-bridge topology is widely used in scenarios where simplicity and efficiency are prioritized, particularly in systems that do not require fault-blocking capabilities. The full-bridge topology is suited to applications where fault tolerance is crucial, despite its higher complexity and cost. Alternative SM topologies like ANPC, CCSM, CDSM, and SCSM offer intermediate options that balance performance and complexity for specific needs. Mixed SM topologies provide a compromise by combining the benefits of multiple SM types. The selection of an appropriate topology is thus determined by a combination of factors, including cost, complexity, fault tolerance, efficiency, and specific operational requirements, all of which must be carefully considered in the design and deployment of MMC-based systems [88].

4.3 Mathematical Model of the MMC

Although various MMC topologies exist [94], they share several core characteristics. Each topology consists of identical SMs, and a series of these SMs forms an arm. Each arm within the converter includes the same number of SMs. When two arms, commonly referred to as the upper and lower arms, are connected, they form a leg, and an MMC may have one or more legs.

The basic structure of an MMC, shown in Figure 4.2, consists of a single leg. The input voltage source is the DC-link voltage E_{DC} , while i_o and v_o represent the output current and voltage, respectively. As illustrated in Figure 4.3, the SMs are arranged as half-bridge legs containing two IGBTs and two antiparallel diodes, with a capacitor placed in parallel with the half-bridge leg.

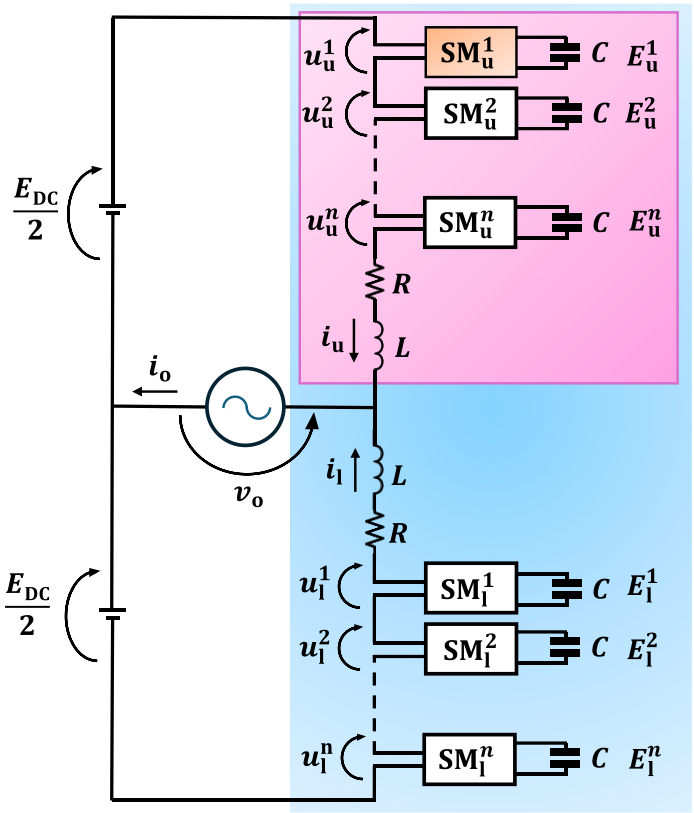


Figure 4.2 – Basic topology of one phase MMC.

To address voltage imbalances that arise during switching between the two arms, an inductor is placed before the connection point with the other SMs. The voltage generated by each leg is a result of the combined SM voltages, enabling the desired output voltage to be synthesized through the appropriate switching configuration. However, it is crucial to

maintain voltage balance across the SM capacitors. To achieve this, a sorting algorithm within the control system determines which SMs should be inserted or bypassed during each sampling period to ensure balanced voltage across all SMs [95].

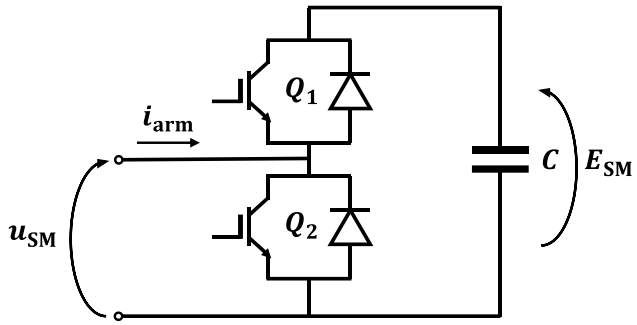


Figure 4.3 - Sub-module topology with a half bridge connected in parallel to a capacitor.

Certain assumptions are made to develop a simplified yet accurate mathematical model of the converter. For a single-phase half-bridge MMC topology, the first assumption is that the SMs within the same arm operate in perfect synchronization, maintaining a precise voltage balance at all times. This assumption allows the SMs within an arm to be represented by a single equivalent SM. Additionally, it is assumed that the fundamental output frequency is at least two orders of magnitude lower than the switching frequency and that the output voltage resolution is significantly smaller than the voltage amplitude due to the large number of SMs.

The schematics shown in Figure 4.4a provide a foundation for deriving the equations governing the two arms of the MMC:

$$\frac{E_{\mathrm{DC}}}{2} - m_{\mathrm{u}}E_{\mathrm{u}} - Ri_{\mathrm{u}} - L\frac{di_{\mathrm{u}}}{dt} = v_{\mathrm{o}} \tag{4.1}$$

$$-\frac{E_{\mathrm{DC}}}{2} + m_{\mathrm{l}}E_{\mathrm{l}} - Ri_{\mathrm{l}} - L\frac{di_{\mathrm{l}}}{dt} = v_{\mathrm{o}}. \tag{4.2}$$

In (4.1) and (4.2), L and R represent the arm inductance and resistance, respectively. The currents in the upper and lower arms are denoted by i_u and i_l, where the subscripts 'u' and 'l' correspond to “upper” and “lower” arms. The voltages of the equivalent SMs in these arms are represented by E_{u} and E_{l}, while m_{u} and m_{l} are the modulation indexes generated by the control logic to drive the SMs. The DC voltage is denoted as E_{DC}, and the output voltage is v_o. If the converter is connected to the grid, as shown in Figure 4.4 (a), the output voltage is a known quantity. Otherwise, as depicted in Figure 4.4 (b), it may depend on the load.

For the upper and lower equivalent SMs, the relationships between the capacitor currents ($m_{\mathrm{u}}i_{\mathrm{u}} - m_{\mathrm{l}}i_{\mathrm{l}}$) and the capacitor voltages (E_{u} and E_{l}) are described by the following equations:

$$C_{eq}\frac{dE_{\mathrm{u}}}{dt} = m_{\mathrm{u}}i_{\mathrm{u}} \tag{4.3}$$

$$C_{eq}\frac{dE_{\mathrm{l}}}{dt} = -m_{\mathrm{l}}i_{\mathrm{l}} \tag{4.4}$$

where C_{eq} is the equivalent capacitance of each arm, calculated as the series combination of all the arm capacitances.

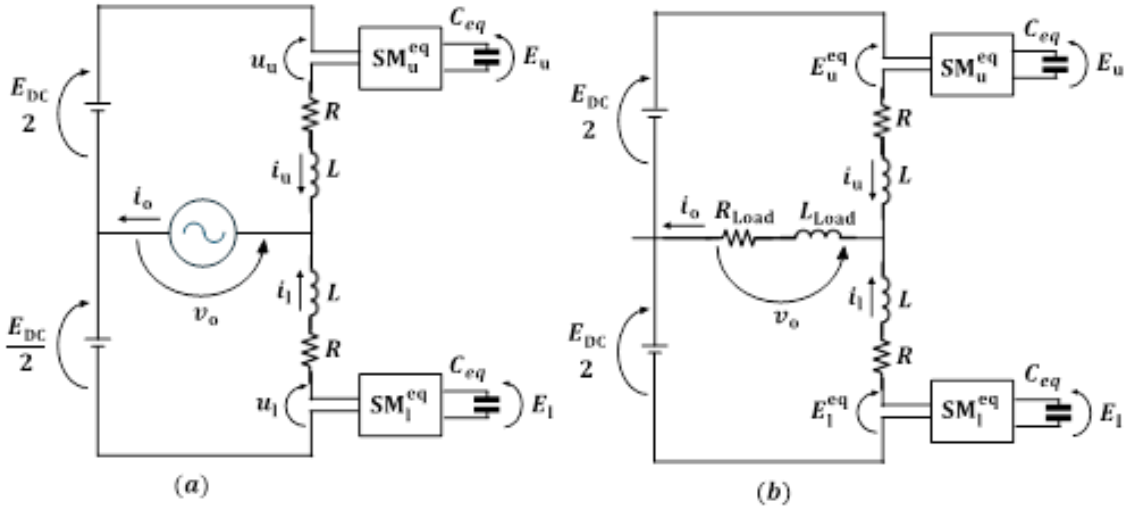


Figure 4.4 - Simplified scheme of an MMC. (a) The converter is connected to a sinusoidal voltage source. (b) The converter is connected to a passive load.

The resulting output current, denoted by i_{o}, is the sum of the current contributions from both arms, and can be expressed as:

$$i_{\mathrm{o}} = i_{\mathrm{u}} + i_{\mathrm{l}}. \tag{4.5}$$

Another important current in an MMC is the differential current, defined as the difference between the currents of the two arms within the same leg:

$$i_{\mathrm{diff}} = i_{\mathrm{u}} - i_{\mathrm{l}}. \tag{4.6}$$

The path of the differential current i_{diff} flows through its corresponding leg and the DC source, which means it does not impact the output variables. By manipulating (4.5) and (4.6), the currents i_{u} and i_{l} can be expressed in terms of i_{o} and i_{diff}, resulting in:

$$i_{\mathrm{u}} = \frac{i_{\mathrm{o}} + i_{\mathrm{diff}}}{2} \tag{4.7}$$

$$i_{\mathrm{l}} = \frac{i_{\mathrm{o}} - i_{\mathrm{diff}}}{2}. \tag{4.8}$$

The dynamic equations for i_{o} and i_{diff} can be derived by summing and subtracting (4.1) and (4.2), while considering the relationships in (4.5) and (4.6):

$$\frac{L}{2}\frac{di_{\mathrm{o}}}{dt} + \frac{R}{2}i_{\mathrm{o}} = u_{\mathrm{o}} - v_{\mathrm{o}} \tag{4.9}$$

$$L\frac{di_{\mathrm{diff}}}{dt} + Ri_{\mathrm{diff}} = u_{\mathrm{diff}} \tag{4.10}$$

where:

$$u_{\mathrm{o}} = \frac{m_{\mathrm{l}}E_{\mathrm{l}} - m_{\mathrm{u}}E_{\mathrm{u}}}{2} \tag{4.11}$$

$$u_{\mathrm{diff}} = \frac{E_{\mathrm{DC}} - m_{\mathrm{u}}E_{\mathrm{u}} - m_{\mathrm{l}}E_{\mathrm{l}}}{2}. \tag{4.12}$$

These equations express the voltages u_{o} and u_{diff} as functions of the SM duty cycles, showing the relationship between these variables. Once the expressions for u_{o} and u_{diff} are known, the modulation signals can be determined by inverting the equations:

$$m_{\mathrm{u}}E_{\mathrm{u}} = \frac{E_{\mathrm{DC}}}{2} - \frac{u_{\mathrm{o}} - u_{\mathrm{diff}}}{2} \tag{4.13}$$

$$m_{\mathrm{l}}E_{\mathrm{l}} = \frac{E_{\mathrm{DC}}}{2} + \frac{u_{\mathrm{o}} - u_{\mathrm{diff}}}{2}. \tag{4.14}$$

In the case of a passive load, as shown in Figure 4.4 (b), the equation for the load must also be included in the system model:

$$L_{load}\frac{di_{\mathrm{o}}}{dt} + R_{load}i_{\mathrm{o}} = v_{\mathrm{o}}. \tag{4.15}$$

By combining (4.9) and (4.15), the control equation for the load current is obtained, which depends on both the load and converter parameters:

$$\left(\frac{L}{2} + L_{load}\right)\frac{di_{\mathrm{o}}}{dt} + \left(\frac{R}{2} + R_{load}\right)i_{\mathrm{o}} = u_{\mathrm{o}}. \tag{4.16}$$

The control of the load current can be based on (4.9) or (4.16), depending on whether v_{o} is a known quantity. If this is not, v_{o} can be estimated using (4.15).

4.4 Decoupled control

The control of an MMC is typically designed to achieve two primary objectives. The first goal is to provide the desired output quantities for i_o and v_o, while the second is to regulate the SM voltages so that they remain below a predefined safety threshold with minimal voltage ripple. To meet these objectives, three variables need to be controlled, i.e., E_u, E_l, and i_o.

However, since the system only has two control variables, the modulation indexes m_u and m_l, the control strategy is complex. As shown in (4.9) and (4.10), i_o and i_{diff} can be controlled by the voltages u_o and u_{diff}, which are defined in (4.11) and (4.12). It is important to recognize that there is a key difference between the currents i_o and i_{diff}. This difference lies in how their references are generated: while $i_{o,ref}$ is a known quantity, $i_{diff,ref}$ must be selected. The following sections will explain how the circulating current i_{diff} influences the total energy stored in the SM capacitors and how it can be used to reduce voltage imbalances.

4.4.1 Control of the Capacitor Voltages

The total electromagnetic energy stored in the upper and lower arms, denoted as W_u and W_l, can be expressed as the sum of the electrostatic energy in the equivalent capacitors and the electromagnetic energy in the arm inductors:

$$W_u = \frac{1}{2}Li_u^2 + \frac{1}{2}C_{eq}E_u^2 \tag{4.17}$$

$$W_l = \frac{1}{2}Li_l^2 + \frac{1}{2}C_{eq}E_l^2. \tag{4.18}$$

Neglecting the intrinsic resistances of the arm inductors, the time derivatives of W_u and W_l can be written as:

$$\frac{dW_u}{dt} = \left(\frac{E_{DC}}{2} - v_o\right)i_u - Ri_u^2 \cong \left(\frac{E_{DC}}{2} - v_o\right)i_u \tag{4.19}$$

$$\frac{dW_l}{dt} = -\left(\frac{E_{DC}}{2} + v_o\right)i_l - Ri_l^2 \cong -\left(\frac{E_{DC}}{2} + v_o\right)i_l. \tag{4.20}$$

By substituting i_u and i_l from (4.7) and (4.8), one obtains:

$$\frac{dW_u}{dt} = v_1 i_o + v_1 i_{diff} \tag{4.21}$$

$$\frac{dW_{\mathrm{l}}}{dt} = -v_2 i_{\mathrm{o}} + v_2 i_{\mathrm{diff}} \tag{4.22}$$

where:

$$v_1 = \frac{1}{2}\left(\frac{E_{\mathrm{DC}}}{2} - v_{\mathrm{o}}\right) \tag{4.23}$$

$$v_2 = \frac{1}{2}\left(\frac{E_{\mathrm{DC}}}{2} + v_{\mathrm{o}}\right). \tag{4.24}$$

Equations (4.21) and (4.22) express the time derivatives of the energy stored in the two arms as the sum of two contributions, one proportional to the output current i_{o} and one proportional to the differential current i_{diff}. The distinction between these contributions lies in the fact that the former is not controllable, as it directly depends on i_{o}, which follows a predefined reference, while the latter can be controlled through i_{diff} using (4.10). Thus, i_{diff} becomes the control variable for regulating the capacitor voltages.

4.4.2 Two Time-Scale Analysis

As indicated in (4.19) and (4.20), the arm energies W_{u} and W_{l} contain harmonics with frequencies that are multiple of the output frequency ω. This is because they depend on i_{o} and v_{o}, which have sinusoidal waveforms. Additionally, the arm energies exhibit a secular variation, defined as a long-term, non-periodic trend. Multiple time-scale analysis, a technique used to approximate the solutions to perturbation problems, can distinguish between periodic variations and secular terms.

For simplicity, only W_{u} will be considered here, as the same reasoning applies to W_{l}. According to multiple-scale analysis, W_{u} can be expressed as a function of two angular variables, τ and θ, which operate on different time scales and are treated as independent:

$$W_{\mathrm{u}} = W_{\mathrm{u}}(\tau, \theta) \tag{4.25}$$

where τ is the slow variable and θ is the fast variable.

If the frequency band of the slow-varying part is [0, ω_c] with $\omega_c << \omega$, and ε is a small number defined as the ratio of ω_c and ω, θ and τ are related to time t as follows:

$$\tau = \omega_{\mathrm{c}} t \tag{4.26}$$

$$\theta = \omega t = \frac{\omega_c}{\varepsilon} t. \tag{4.27}$$

Furthermore, W_u is periodic with respect to θ:

$$W_u(\theta, \tau) = W_u(\theta + 2\pi, \tau). \tag{4.28}$$

Figure 4.5 illustrates the meaning of θ and τ.

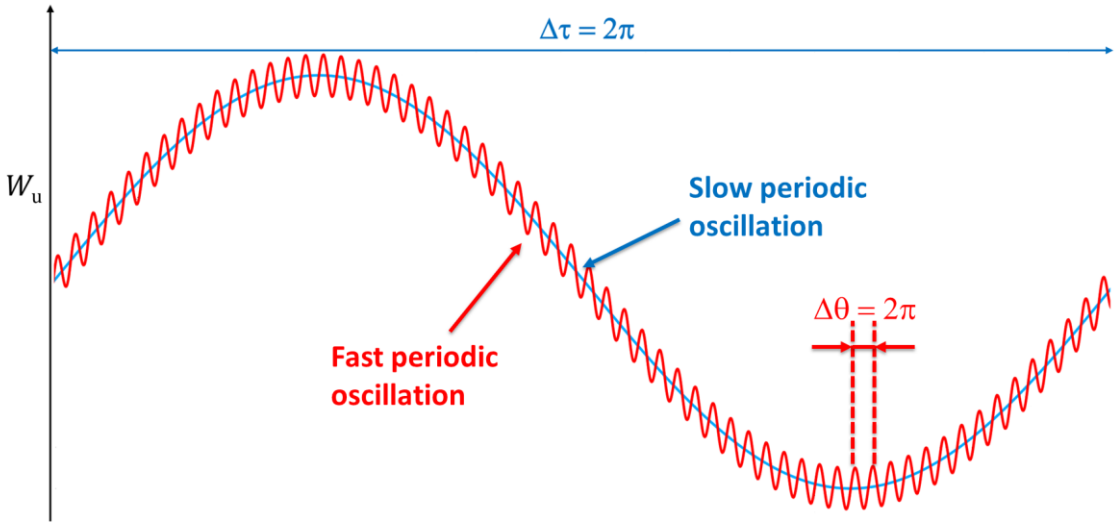


Figure 4.5 - Fast and slow time scales.

Using the chain rule, the time derivative of W_u becomes:

$$\frac{dW_u}{dt} = \frac{\partial W_u}{\partial \tau}\omega_c + \frac{\partial W_u}{\partial \theta}\omega. \tag{4.29}$$

After expressing ω as $\frac{\omega_c}{\varepsilon}$, multiplying both sides of (4.21) by ε, and considering (4.29), one obtains:

$$\frac{\partial W_u}{\partial \tau}\varepsilon\omega_c + \frac{\partial W_u}{\partial \theta}\omega_c = \varepsilon(v_1 i_o + v_1 i_{diff}). \tag{4.30}$$

When ε is small, according to standard perturbation theory, W_u can be expanded into a power series of ε under the assumption that the $(n+1)^{th}$ term becomes arbitrarily small compared to the n^{th} term as $\varepsilon \to 0$:

$$W_u = W_{u0}(\tau, \theta) + W_{u1}(\tau, \theta)\varepsilon + \ \ldots \tag{4.31}$$

Since W_u is periodic with respect to θ, both W_{u0} and W_{u1} must be periodic functions as well.

Substituting (4.31) into (4.30) and equating the coefficients of the same powers of ε yields the following set of equations for the first two orders of ε:

$$\frac{\partial W_{\mathrm{u0}}}{\partial \theta} = 0 \tag{4.32}$$

$$\frac{\partial W_{\mathrm{u0}}}{\partial \tau}\omega_c + \frac{\partial W_{\mathrm{u1}}}{\partial \theta}\omega_c = v_1 i_{\mathrm{o}} + v_1 i_{\mathrm{diff}}. \tag{4.33}$$

Equation (4.32) indicates that W_{u0} does not depend on the fast variable θ, representing the slow-varying part of the arm energy (secular term). The contribution from the fast oscillation can be neglected, as its period is insignificant compared to the slow transients. Therefore, the time derivative of W_{u0} can be expressed as:

$$\frac{dW_{\mathrm{u0}}}{dt} = \frac{\partial W_{\mathrm{u0}}}{\partial \tau}\omega_{\mathrm{c}}. \tag{4.34}$$

The right-hand side of equation (4.34) can be calculated by integrating each side of (4.33) with respect to θ over the interval [0,2π]. Since W_{u1} is a periodic function of θ, the integral of $\frac{\partial W_{\mathrm{u1}}}{\partial \theta}\omega_c$ is zero, and (4.34) simplifies to:

$$\frac{dW_{\mathrm{u0}}}{dt} = \frac{1}{2\pi}\int_0^{2\pi} v_1 i_{\mathrm{o}}\, d\theta + \frac{1}{2\pi}\int_0^{2\pi} v_1 i_{\mathrm{diff}}\, d\theta. \tag{4.35}$$

A similar expression can be derived for W_{l}:

$$\frac{dW_{\mathrm{l0}}}{dt} = \frac{1}{2\pi}\int_0^{2\pi} (-v_2 i_{\mathrm{o}}) d\theta + \frac{1}{2\pi}\int_0^{2\pi} v_2 i_{\mathrm{diff}}\, d\theta. \tag{4.36}$$

Finally, (4.35) and (4.36) can be rewritten using time as the integration variable, based on (4.27):

$$\frac{dW_{\mathrm{u0}}}{dt} = \frac{1}{T}\int_0^{T} v_1 i_{\mathrm{o}}\, dt + \frac{1}{T}\int_0^{T} v_1 i_{\mathrm{diff}}\, dt \tag{36}$$

$$\frac{dW_{\mathrm{l0}}}{dt} = \frac{1}{T}\int_0^{T} -v_2 i_{\mathrm{o}}\, dt + \frac{1}{T}\int_0^{T} v_2 i_{\mathrm{diff}}\, dt \tag{37}$$

where T is equal to $2\pi/\omega$.

Equations (4.36) and (4.37) explicitly describe the time derivatives of the slowly varying components of the arm energies and show their dependence on the average power exchanged

by the SMs over the period T. These equations can replace (4.18) and (4.19) in synthesizing a stable control system.

4.4.3 Orthogonal Functions

Two functions, f and g, belonging to a vector space V with an inner product $\langle\cdot,\cdot\rangle$, are considered orthogonal if their inner product is zero. The integral operator in (4.39) satisfies the properties of symmetry, linearity, and positive definiteness. Therefore, it acts as an inner product for real periodic functions defined in the interval $[0,2\pi]$:

$$\langle f, g\rangle = \frac{1}{2\pi}\int_0^{2\pi} f(\theta)g(\theta)d\theta. \tag{4.39}$$

Equations (4.34) and (4.35) can be rewritten using equation (38) as follows:

$$\frac{dW_{\mathrm{u0}}}{dt} = \langle v_1, i_{\mathrm{o}}\rangle + \langle v_1, i_{\mathrm{diff}}\rangle \tag{4.40}$$

$$\frac{dW_{\mathrm{l0}}}{dt} = -\langle v_2, i_{\mathrm{o}}\rangle + \langle v_2, i_{\mathrm{diff}}\rangle. \tag{4.41}$$

The only independent variable in (4.40) and (4.41) that can be used to control the arm energies is i_{diff}. This means that the two arm energies are coupled and cannot be controlled independently.

To decouple the control of the two arms, i_{diff} can be expressed as a linear combination of two independent functions, $w_1(\tau,\theta)$ and $w_2(\tau,\theta)$. While $w_1(\tau,\theta)$ influences the energy of the upper arm, $w_2(\tau,\theta)$ only affects the energy of the lower arm:

$$i_{\mathrm{diff}} = \lambda_1(\tau)w_1(\tau,\theta) + \lambda_2(\tau)w_2(\tau,\theta) \tag{4.42}$$

where λ_1 and λ_2 are parameters that depend on the slow time variable τ. The unit for w_1 and w_2 is volts [V], while λ_1 and λ_2 are measured in ohms-inverse [Ω^{-1}].

It is beneficial to select w_1 and w_2, which can be arbitrarily chosen, such that they are mutually orthogonal to the voltage functions v_1 and v_2, as follows:

$$\langle v_{\mathrm{h}}, w_{\mathrm{k}}\rangle = \begin{cases} P_{\mathrm{n}} & if\ \ h = k \\ 0 & if\ \ h \neq k \end{cases} \qquad h,k = 1,2 \tag{4.43}$$

where P_{n} is an arbitrary non-zero constant with the dimension of power [W].

By combining (4.40)-(4.42), one obtains a system of two decoupled equations:

$$\frac{dW_{\mathrm{u0}}}{dt} = \langle v_1, i_{\mathrm{o}}\rangle + \lambda_1 P_{\mathrm{n}} \tag{4.44}$$

$$\frac{dW_{\mathrm{l0}}}{dt} = -\langle v_2, i_{\mathrm{o}} \rangle + \lambda_2 P_{\mathrm{n}}. \tag{4.45}$$

Equations (4.44) and (4.45) show that λ_1 and λ_2 can be treated as independent variables, allowing for separate control of the arm energies with slow dynamics.

4.4.4 Reciprocal Functions

To ensure decoupled control of the arm energies, (4.42) indicates that i_{diff} should be chosen from the linear span of w_1 and w_2. The basis (w_1, w_2) is reciprocal to the basis $(v_1\ v_2)$ since (4.43) ensures that v_1 and v_2 are orthogonal to w_2 and w_1, respectively.

The functions λ_1 and λ_2 in (4.42) are referred to as the covariant components of i_{diff}.

The explicit expressions for w_1 and w_2 can be determined by assuming they can both be written as combinations of v_1 and v_2:

$$w_{\mathrm{k}} = \mu_{\mathrm{k},1} v_1 + \mu_{\mathrm{k},2} v_2 \qquad k = 1, 2 \tag{4.46}$$

The coefficients $\mu_{\mathrm{k},1}$ and $\mu_{\mathrm{k},2}$ in (4.46) are known as the contravariant components of w_{k} .

To find the explicit values of the coefficients $\mu_{\mathrm{k,h}}$, it is necessary to solve the matrix equation obtained by combining (4.46) with (4.43) for $k, h = 1, 2$:

$$\begin{bmatrix} \mu_{1,1} & \mu_{1,2} \\ \mu_{2,1} & \mu_{2,2} \end{bmatrix} \begin{bmatrix} \langle v_1, v_1 \rangle & \langle v_1, v_2 \rangle \\ \langle v_2, v_1 \rangle & \langle v_2, v_2 \rangle \end{bmatrix} = P_{\mathrm{n}} \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}. \tag{4.47}$$

The solution to (4.47) is:

$$\begin{bmatrix} \mu_{1,1} & \mu_{1,2} \\ \mu_{2,1} & \mu_{2,2} \end{bmatrix} = P_{\mathrm{n}} \begin{bmatrix} \langle v_1, v_1 \rangle & \langle v_1, v_2 \rangle \\ \langle v_2, v_1 \rangle & \langle v_2, v_2 \rangle \end{bmatrix}^{-1}. \tag{4.48}$$

Since E_{DC} is constant and v_{o} is sinusoidal at steady state, the explicit values of the coefficients $\mu_{h,k}$ can be found by substituting (4.23) and (4.24) into (4.48):

$$\mu_{1,1} = \mu_{2,2} = \frac{4P_{\mathrm{n}}}{E_{\mathrm{DC}}^2}\left(1 + \frac{E_{\mathrm{DC}}^2}{V_{\mathrm{o,RMS}}^2}\right) \tag{4.49}$$

$$\mu_{1,2} = \mu_{2,1} = \frac{4P_{\mathrm{n}}}{E_{\mathrm{DC}}^2}\left(1 - \frac{E_{\mathrm{DC}}^2}{V_{\mathrm{o,RMS}}^2}\right) \tag{4.50}$$

where $V_{\mathrm{o,RMS}}$ is the RMS value of the output voltage.

Then, w_1 and w_2 can be rewritten by combining (4.23), (4.24), (4.49), (4.50), and (4.46) as follows:

$$w_1 = \frac{2P_\mathrm{n}}{E_\mathrm{DC}}\left(1 - \frac{E_\mathrm{DC}}{2}\frac{v_\mathrm{o}}{V_\mathrm{o,RMS}^2}\right) \tag{4.51}$$

$$w_2 = \frac{2P_\mathrm{n}}{E_\mathrm{DC}}\left(1 + \frac{E_\mathrm{DC}}{2}\frac{v_\mathrm{o}}{V_\mathrm{o,RMS}^2}\right). \tag{4.52}$$

In conclusion, the desired reference value for i_diff can be generated using (4.42), where λ_1 and λ_2 are independent functions selected to control the arm energies according to (4.44) and (4.45), and w_1 and w_2 are given by (4.51) and (4.52).

4.4.5 Differential Current and Total Energy Ripple

Equation (4.42) does not provide the complete expression for i_diff, but only the components that influence the arm energies. This raises the question of whether additional components of i_diff can be included to improve converter performance without affecting the control of the arm energies.

More generally, i_diff in (4.42) can be redefined as follows:

$$i_\mathrm{diff} = \lambda_1(\tau)w_1(\theta,\tau) + \lambda_2(\tau)w_2(\theta,\tau) + i_\mathrm{f} \tag{4.53}$$

where i_f is a new current component that must not contribute to the variations in W_u0 and W_l0. Therefore, i_f must be orthogonal to w_1 and w_2.

The fast-varying part of the arm energy W_u can be found by combining (4.33) and (4.34):

$$\omega_\mathrm{c}\frac{\partial W_\mathrm{u1}}{\partial\theta} = \frac{dW_\mathrm{u0}(\tau)}{dt} - (v_1 i_\mathrm{o} + v_1 i_\mathrm{diff}). \tag{4.54}$$

If the slow-varying component of arm energy W_u is assumed to be steady, its derivative becomes zero. The expression for the fast-varying component of W_u then simplifies to:

$$\omega_\mathrm{c}\frac{\partial W_\mathrm{u1}}{\partial\theta} = -v_1(i_\mathrm{o} + i_\mathrm{diff}). \tag{4.55}$$

The same reasoning applies to the energy W_l1 of the lower arm:

$$\omega_\mathrm{c}\frac{\partial W_\mathrm{l1}}{\partial\theta} = -v_2(-i_\mathrm{o} + i_\mathrm{diff}). \tag{4.56}$$

The derivative of the fast-varying component of the total leg energy, obtained by summing (4.55) and (4.56), is:

$$\omega_{\mathrm{c}} \frac{\partial W_{1,\mathrm{tot}}}{\partial \theta} = v_{\mathrm{o}} i_{\mathrm{o}} - \frac{1}{2} E_{\mathrm{DC}} i_{\mathrm{diff}}. \tag{4.57}$$

The term i_{f} in (4.53) can be used to reduce fluctuations in $W_{1,\mathrm{tot}}$, which are caused by the oscillating component of the output power $v_{\mathrm{o}} i_{\mathrm{o}}$. Assuming a sinusoidal output voltage and current, the output power contains a harmonic component with a frequency of 2ω:

$$v_{\mathrm{o}} i_{\mathrm{o}} = V_{\mathrm{o,RMS}} I_{\mathrm{o,RMS}} \left(\cos(2\theta - \varphi) + \cos\varphi\right) \tag{4.58}$$

where φ is the output phase angle, and $I_{\mathrm{o,RMS}}$ is the root mean square value of the output current.

Substituting (4.53) and (4.58) into (4.57), one obtains:

$$\begin{aligned} \omega_{\mathrm{c}} \frac{\partial W_{1,\mathrm{tot}}}{\partial \theta} = {} & V_{\mathrm{o,RMS}} I_{\mathrm{o,RMS}} \cos\varphi + V_{\mathrm{o,RMS}} I_{\mathrm{o,RMS}} \cos(2\theta - \varphi) \\ & + \frac{1}{2}(-\lambda_1 w_1 E_{\mathrm{DC}} - \lambda_2 w_2 E_{\mathrm{DC}} - i_{\mathrm{f}} E_{\mathrm{DC}}). \end{aligned} \tag{4.59}$$

The quantities λ_1 and λ_2 are slow-varying functions of τ, and their steady-state values can be obtained from (4.44) and (4.45):

$$\lambda_1 = -\frac{\langle v_1, i_{\mathrm{o}} \rangle}{P_{\mathrm{n}}} = \frac{1}{2P_{\mathrm{n}}} V_{\mathrm{o,RMS}} I_{\mathrm{o,RMS}} \cos\varphi \tag{4.60}$$

$$\lambda_2 = \frac{\langle v_2, i_{\mathrm{o}} \rangle}{P_{\mathrm{n}}} = \frac{1}{2P_{\mathrm{n}}} V_{\mathrm{o,RMS}} I_{\mathrm{o,RMS}} \cos\varphi. \tag{4.61}$$

Considering (4.23), (4.24), (4.60), and (4.61), when the slow-time component of leg energy is at a steady state, (4.59) becomes:

$$\omega_{\mathrm{c}} \frac{\partial W_{1,\mathrm{tot}}}{\partial \theta} = V_{\mathrm{o,RMS}} I_{\mathrm{o,RMS}} \cos(2\theta - \varphi) - \frac{1}{2} i_{\mathrm{f}} E_{\mathrm{DC}}. \tag{4.62}$$

To reduce the fluctuations in total energy, the current i_{f} should be:

$$i_{\mathrm{f}} = 2 \frac{V_{\mathrm{o,RMS}}}{E_{\mathrm{DC}}} I_{\mathrm{o,RMS}} \cos(2\theta - \varphi). \tag{4.63}$$

It can be verified that the expression for i_{f} in (4.63) is orthogonal to w_1 and w_2 and, therefore, does not affect the slow-time components of the arm energies.

4.5 Control Structure

Figure 4.6 presents a detailed flow diagram of the control logic derived from the theoretical framework discussed in the previous section. The control system's primary objective is to regulate the energy in the upper and lower arms, represented by $W_{u,ref}$ and $W_{l,ref}$, while also ensuring optimal differential and output current control. This section outlines the step-by-step functionality of the control scheme and explains how various system components interact.

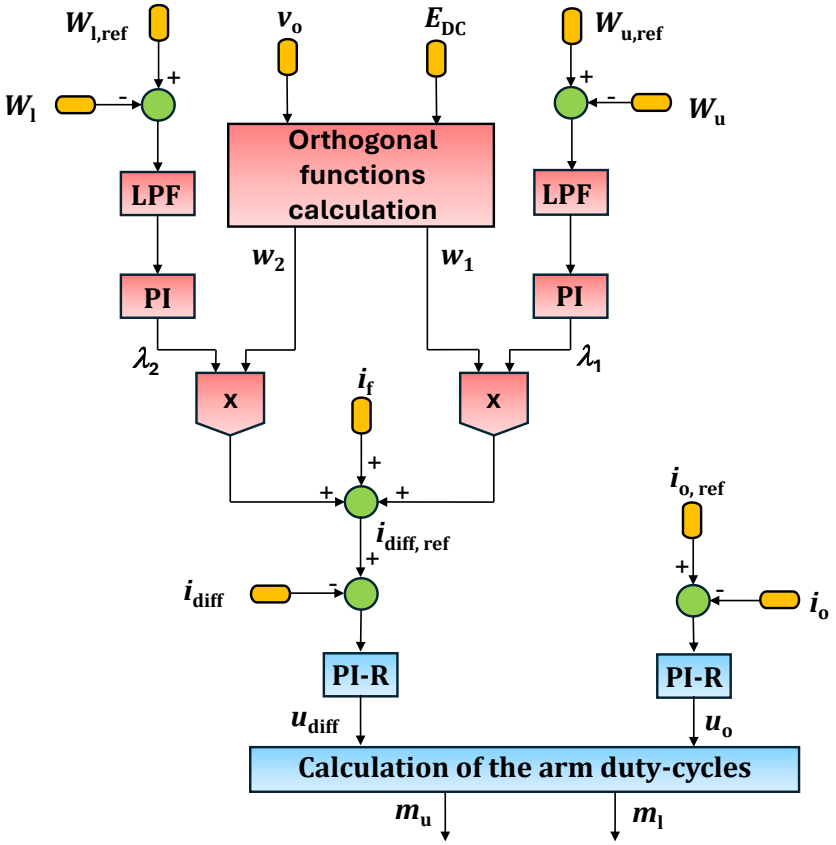


Figure 4.6 - MMC control block diagram.

The control scheme begins by receiving the reference signals $W_{u,ref}$ and $W_{l,ref}$, which serve as inputs. These reference signals are derived from the desired performance of the MMC and are compared to the actual energy values W_u and W_l. The actual arm energy values are calculated based on the real-time measurements of the arm currents and capacitor voltages, using (4.17) and (4.18). Simultaneously, the system takes measurements of the output voltage v_o and the DC-link voltage E_{DC}, which are essential for computing the

orthogonal functions w_1 and w_2. These functions play a pivotal role in ensuring independent control over the upper and lower arm energies.

Once the comparison between the reference and actual arm energy values is completed, the resulting tracking errors pass through a Low Pass Filter (LPF). The LPF extracts the slow-varying content of the arm energy differences, ensuring that the control system focuses on the low-frequency components, which correspond to the desired secular variation of the system. Following this, the filtered signals are fed into two Proportional-Integral (PI) controllers, which generate the signals λ_1 and λ_2. These signals represent the control variables that regulate the energy in the upper and lower arms independently, as discussed in the earlier sections.

To regulate the differential current, the component i_{f}, which accounts for the oscillating part of the differential current, must first be calculated. This component can either be determined through (4.63) or by extracting the oscillating portion of the output power and dividing it by $\frac{E_{\mathrm{DC}}}{2}$. With i_{f} known, the reference value for the differential current $i_{\mathrm{diff,ref}}$ can be computed using (4.53). This step is crucial because it ensures that the control system can properly manage the circulating current within the converter and minimize voltage imbalances between the SMs.

Next, the reference values for the differential current $i_{\mathrm{diff,ref}}$ and the output current $i_{\mathrm{o,ref}}$ are compared to the actual measured values of i_{diff} and i_{o}. The control system tracks these values using two multi-resonant PI regulators (PIR controllers). These controllers are designed to provide accurate tracking by generating the voltages u_{diff} and u_{o}, which are used to control the modulation indexes m_{u} and m_{l}. Equations (4.11) and (4.12) are employed to convert u_{diff} and u_{o} into modulation indexes that control the switching states of the SMs, thus managing the output voltage and the balance of the differential current.

The use of multi-resonant PI controllers, tuned to resonant frequencies ω and 2ω, ensures that the control system can eliminate tracking errors in steady state. This is particularly important because the reference signals for the differential and output currents contain harmonics at these frequencies. Without the inclusion of these resonant components, the control system would be unable to compensate for the periodic fluctuations in the current, leading to persistent errors in the system's performance.

In summary, the control flow diagram highlights the coordinated approach used to regulate the arm energies, differential current, and output current in an MMC. By leveraging orthogonal functions, PI controllers, and multi-resonant regulators, the system ensures stable and efficient operation under varying load conditions.

4.6 Simulations

To validate the effectiveness of the proposed control strategy and demonstrate that the differential current reference generation based on orthogonal functions successfully decouples the control of the two arms, a detailed simulation model was developed in MATLAB Simulink. This simulation replicates the behavior of a single-leg MMC with three SMs per arm, where each SM is configured as a half-bridge circuit with a parallel capacitor. The converter is designed to supply an L-R load. The parameters used in the simulation match those of the physical prototype employed for experimental testing, as outlined in Table 4.1.

Table 4.1 – Main simulation parameters.

Parameter	Value	Unit
Nominal DC arm voltage ($E_{\mathrm{u,ref}} = E_{\mathrm{l,ref}}$)	100	[V]
Output current peak	10	[A]
Fundamental output frequency	50	[Hz]
SM capacitance (all identical)	2.85	[mF]
Arm inductance (for both arms)	1.75	[mH]
Load inductance	0.81	[mH]
Load resistance	3.2	[Ω]

The simulation begins under balanced conditions, meaning that the reference voltages for the upper and lower arm capacitors are equal ($E_{\mathrm{u,ref}} = E_{\mathrm{l,ref}}$), and no differential current component i_{f} is injected at the initial stage, i.e., $i_{\mathrm{f}} = 0$. Once the system reaches steady-state operation, the injection of i_{f} is enabled. This step mimics the real-world scenario where the control system stabilizes before fine-tuning the differential current. In addition to this, a step change is applied to the voltage reference $E_{\mathrm{u,ref}}$ for the upper arm capacitors after the transient phase has ended, further testing the system's response to sudden variations.

Figure 4.7 present the key outcomes of the simulations. Introducing a component with a frequency twice that of the fundamental frequency and the correct phase angle into the differential current can mitigate oscillations in the total energy. This effect is highlighted in Figure 4.7, where the injection of i_f successfully reduces the total energy ripple by 64%. This result showcases the effectiveness of the proposed strategy in stabilizing the system's energy without compromising the overall performance.

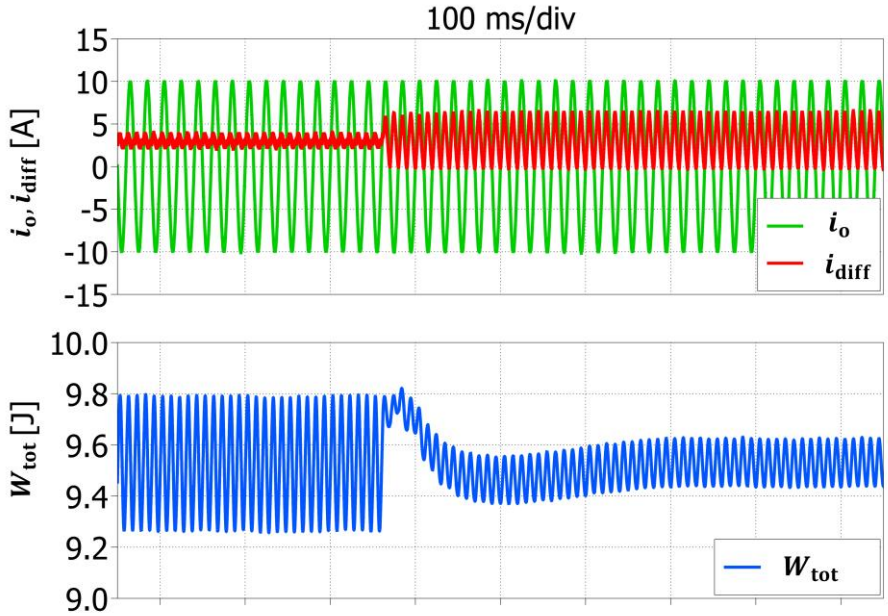


Figure 4.7 – Reduction of the total energy ripple in response to the injection of the component $\boldsymbol{i_f}$.

Although the reduction in total energy ripple is quite significant, the impact on the voltages across the arm capacitors is less pronounced, but still notable. As shown in Figure 4.8, the peak-to-peak voltage ripple of the arm capacitors decreases by approximately 13%, from 14.4 V to 12.9 V. While this improvement may seem modest compared to the reduction in total energy ripple, it demonstrates that the control strategy effectively minimizes voltage fluctuations, further contributing to the stability of the system.

Figure 4.9 illustrates the converter's behavior when the DC voltage reference for the upper arm capacitors, $E_{u,ref}$, is reduced by 10% of its nominal value, dropping from 100 V to 90 V. This adjustment impacts only the parameter λ_1, which is associated with the upper arm. The corresponding control variable undergoes a significant change, while λ_2, which governs the lower arm, remains unaffected. This result confirms the decoupling effect of the proposed control strategy, as changes in one arm do not influence the other. The ability to control the

arms independently is a crucial feature for achieving efficient and reliable performance in MMC systems.

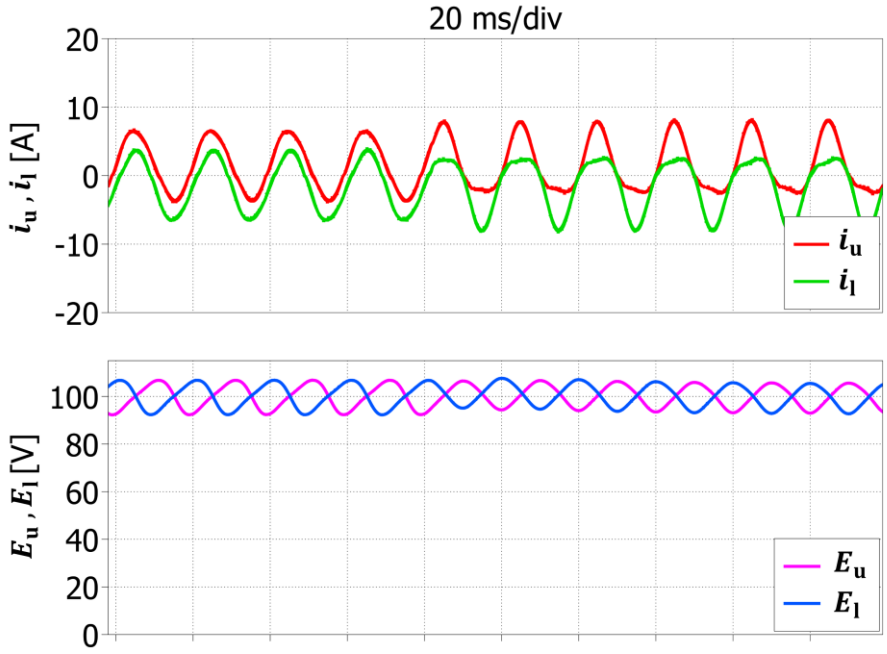


Figure 4.8 – Response of arms currents and voltages to the injection of the component i_f.

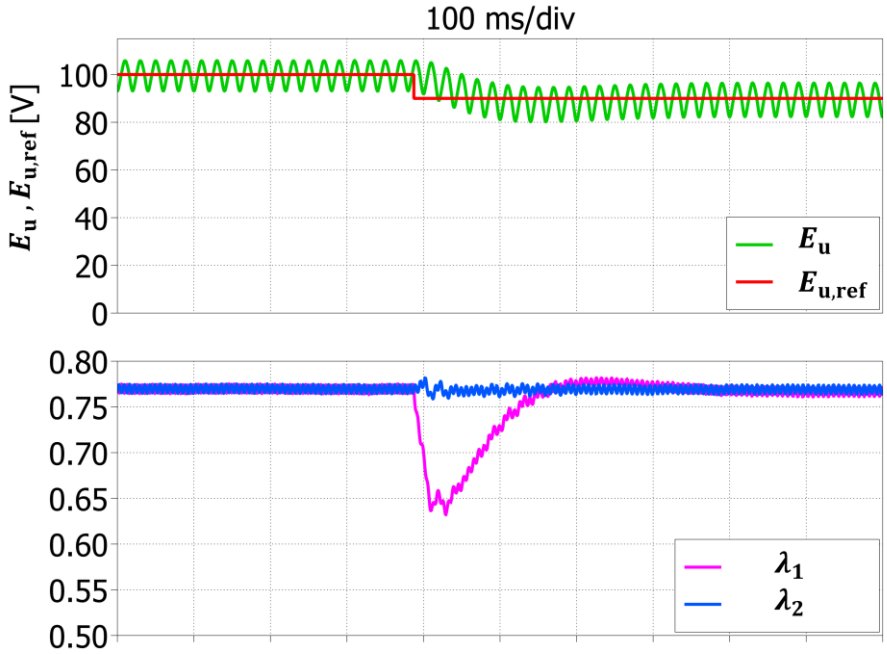


Figure 4.9 – Response of the converter to a step decrease in the setpoint $E_{u,ref}$ by 10%. Waveforms of $E_{u,ref}$, $E_{u,ref}$ (upper traces) and λ_1, λ_2 (lower traces).

Finally, Figure 4.10 presents the output quantities in steady-state balanced conditions, where $E_{\mathrm{u,ref}} = E_{\mathrm{l,ref}}$, after the injection of i_{f} is enabled. It can be observed that the circulating current exhibits an oscillation with a frequency twice that of the output frequency, as expected from the theoretical analysis. Despite the presence of this oscillation in the circulating current, the output current and voltage remain almost perfectly sinusoidal, indicating that the system effectively filters out the high-frequency components in the output signal. This result highlights the robustness of the control system in maintaining high-quality output waveforms, even under dynamic operating conditions.

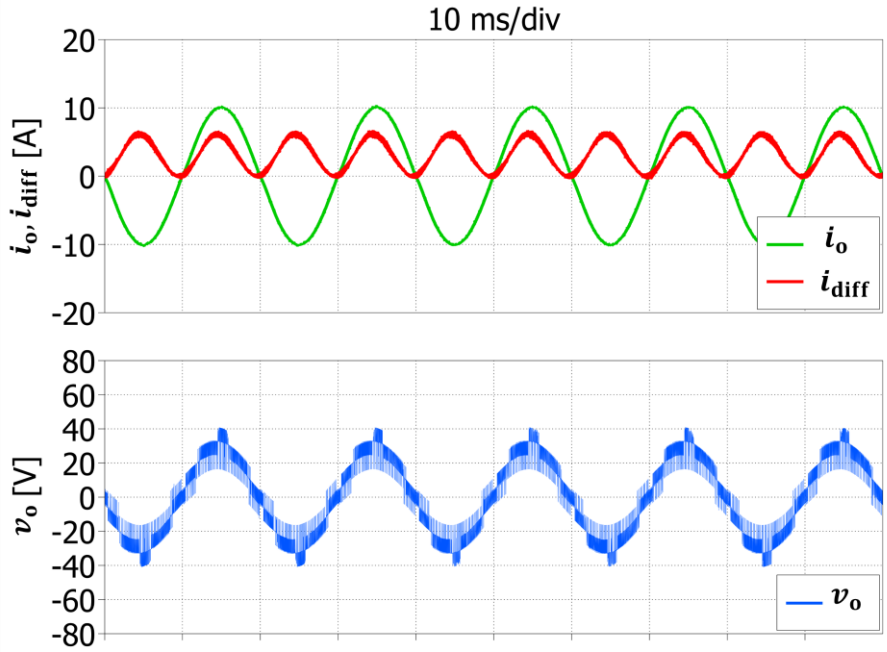


Figure 4.10 – Waveforms of $\boldsymbol{i_o}$, $\boldsymbol{i_{diff}}$ (upper traces) and $\boldsymbol{v_o}$ (lower trace) at a steady state.

The simulation results confirm that the control strategy, based on orthogonal functions, successfully decouples the control of the upper and lower arms of the MMC. The injection of a differential current component with twice the fundamental frequency significantly reduces the energy ripple and stabilizes the system, while ensuring that the output current and voltage remain sinusoidal. These findings validate the effectiveness of the control approach and demonstrate its potential for practical implementation in real-world MMC systems.

4.7 Experimental tests

To validate the proposed control strategy, a physical prototype of a single-leg MMC, as shown in Figure 4.11, was constructed. This prototype was designed to replicate the conditions of the simulations discussed earlier. The SM capacitances, arm inductances, and arm resistances were carefully sized to match the corresponding values used in the simulation model. Additionally, the control parameters and reference values were set identical to those employed in the simulations, ensuring that the experimental tests provided a direct comparison to the simulated behavior.

Figure 4.11 - MMC prototype, encompassing six SMs, used for experimental tests.

Figure 4.12 – Individual SM board.

The initial experiment tested the system's performance in steady-state balanced conditions, where the reference voltages for both the upper and lower arms were equal ($E_{\mathrm{u,ref}} = E_{\mathrm{l,ref}}$). The results are depicted in Figure 4.13. In this case, the differential current

component i_f was initially set to zero, and under these conditions, the differential current remained almost constant. However, once the injection of i_f was enabled, the differential current began to oscillate at a frequency twice that of the fundamental, as predicted by the control strategy. This injection significantly reduced the total energy ripple, demonstrating the practical effectiveness of the proposed control mechanism.

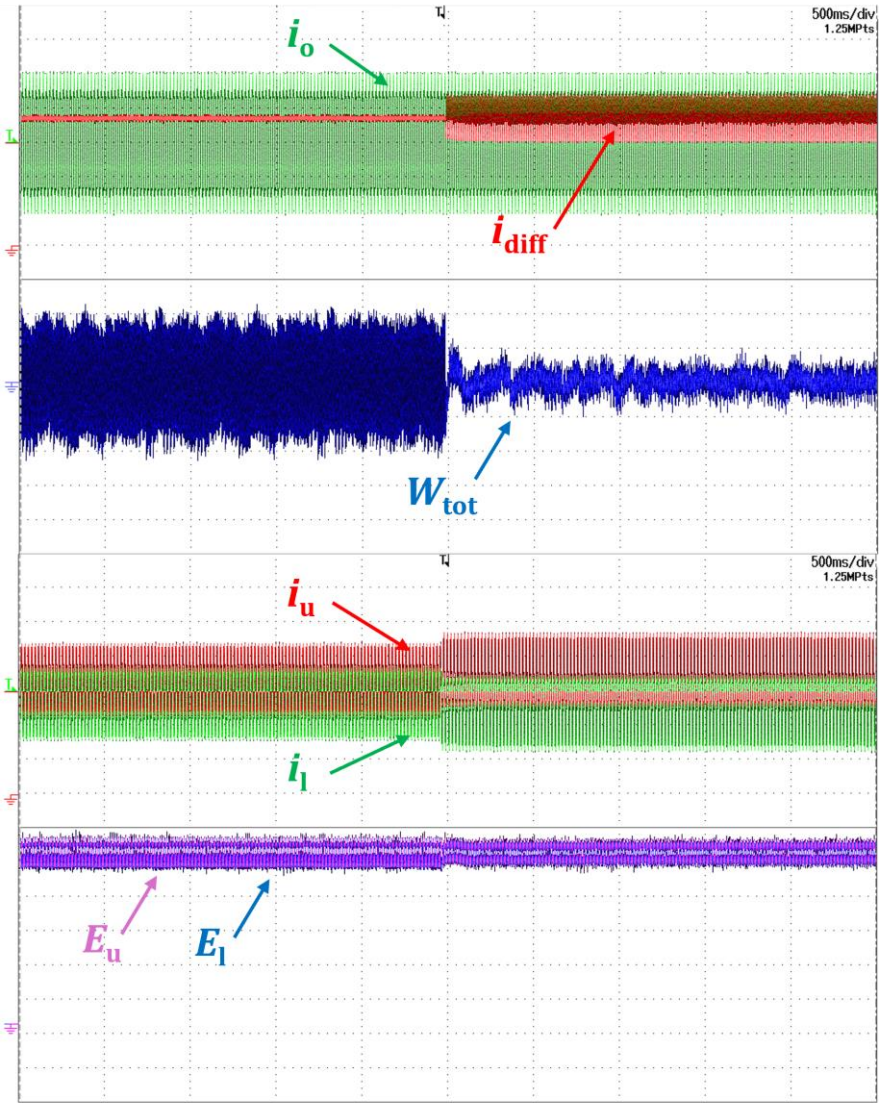


Figure 4.13 - System response to i_f injection. From top to bottom: output current i_o(in green, 5 A/div); differential current i_{diff} (in red, 5 A/div); total energy W_{tot} (in blue, 200 mJ/div, AC coupling); upper arm current i_u (in red, 5 A/div); lower arm current i_l (in green, 5 A/div); upper arm voltage E_u (in purple, 20 V/div); lower arm voltage E_l (in blue, 20 V/div).

To enhance the readability and clarify the finer details of the response, Figure 4.14 illustrates the same test as Figure 4.13, but with a shorter time scale of 20 ms/div as opposed

to 500 ms/div. This time scale adjustment allows for better visualization of the differential current oscillations and their impact on the energy ripple. The results in Figure 4.14 closely align with those seen in the simulations presented earlier in Figure 4.8, reinforcing the conclusion that the control strategy performs consistently in both simulated and experimental environments.

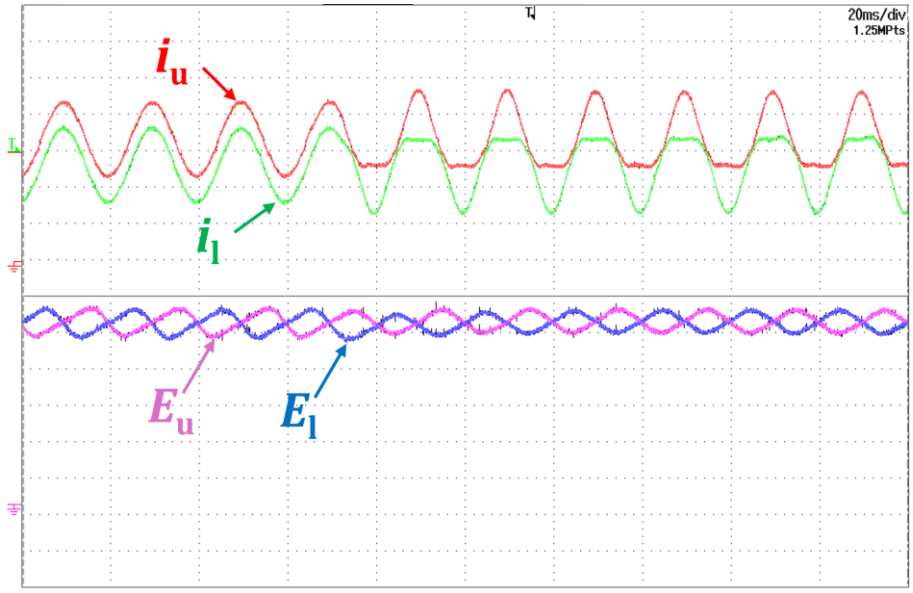


Figure 4.14 - Detail of system response to $\boldsymbol{i_f}$ injection, from top to bottom: upper arm current $\boldsymbol{i_u}$ (in red, 5 A/div); lower arm current $\boldsymbol{i_l}$ (in green, 5 A/div); upper arm voltage $\boldsymbol{E_u}$ (in purple, 20 V/div); lower arm voltage $\boldsymbol{E_l}$ (in blue, 20 V/div).

The second phase of the experiment involved introducing a 10% step reduction in the upper arm voltage reference $E_{\mathrm{u,ref}}$, which decreases from 100 V to 90 V, once the system had stabilized in a new steady state. The results are shown in Figure 4.15. As expected, the control variable λ_1, associated with the upper arm, exhibited a rapid drop in response to the change, accurately tracking the new reference voltage. On the other hand, λ_2, which controls the lower arm, remained unaffected by the variation in $E_{\mathrm{u,ref}}$. This outcome is consistent with the simulation results and further validates the decoupling of control between the two arms. The fact that the change in the upper arm reference had no effect on the lower arm confirms that the control strategy effectively decouples the control loops, allowing each arm to be regulated independently.

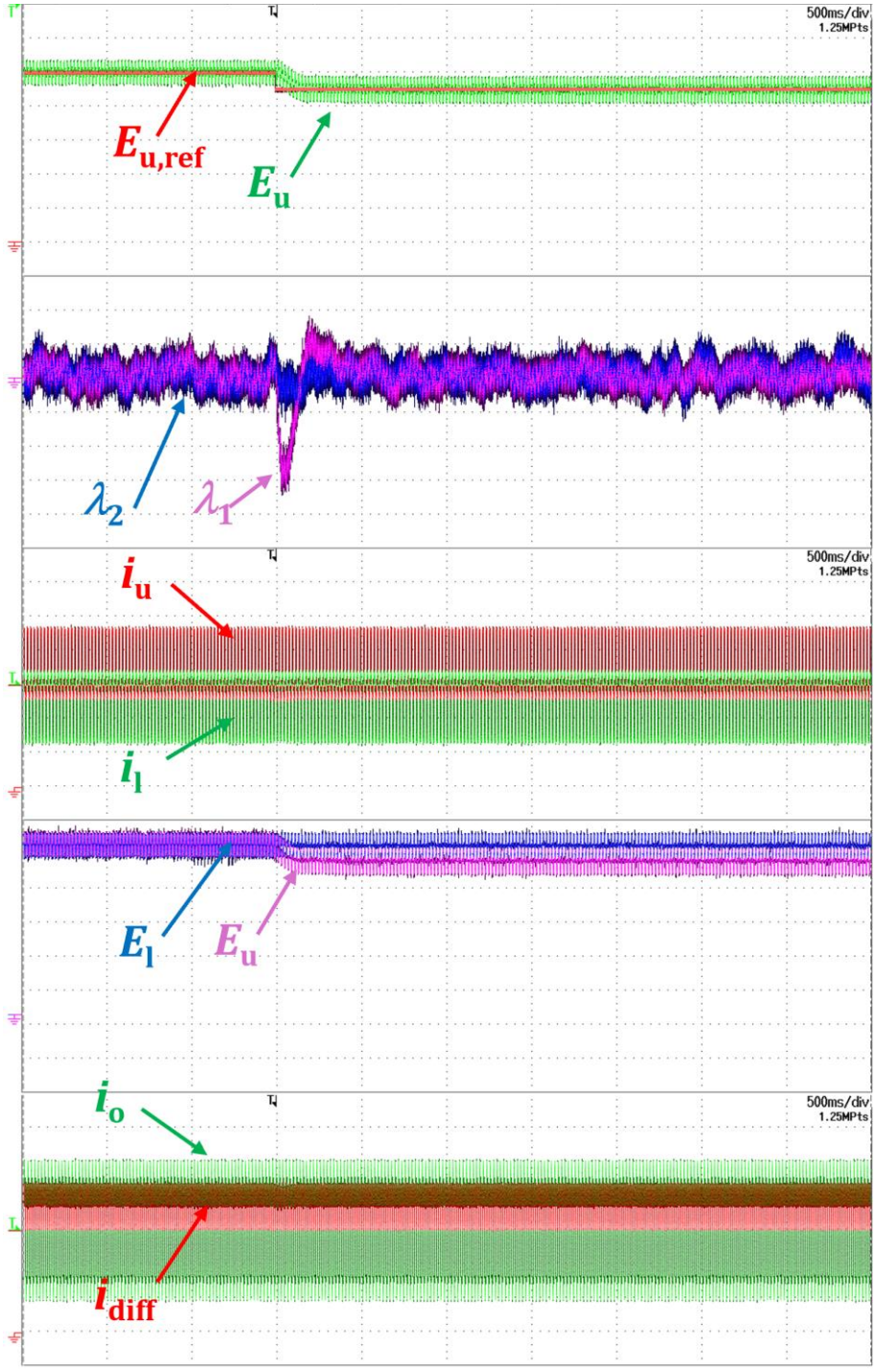


Figure 4.15 - Response of the system to a step variation in $E_{u,ref}$, from top to bottom: upper arm voltage reference $E_{u,ref}$ (in red, 20 V/div); upper arm voltage E_u (in purple, 20 V/div); λ_1 (in purple, 0,05/div, AC coupling); λ_2(in blue, 0,05/div, AC coupling); upper arm current i_u (in red, 5 A/div); lower arm current i_l (in green, 5 A/div); upper arm voltage E_u (in purple, 20 V/div); lower arm voltage E_l (in blue, 20 V/div); output current i_o (in green, 5 A/div); differential current i_{diff} (in red, 5 A/div).

Finally, Figure 4.16 presents the system's performance in steady-state balanced conditions, where both $E_{\mathrm{u,ref}}$ and $E_{\mathrm{l,ref}}$ are set at 100% of their rated values. In this scenario, the injection of the differential current component i_{f} was enabled, and the figure displays the output current, the differential current, and the output voltage of the MMC. The differential current again shows the characteristic oscillation at twice the fundamental frequency, while the output current and voltage remain nearly sinusoidal, indicating that the control strategy not only manages the differential current effectively but also maintains high-quality output waveforms. These results confirm that the injection of i_{f} enhances the stability of the system without degrading the overall output performance.

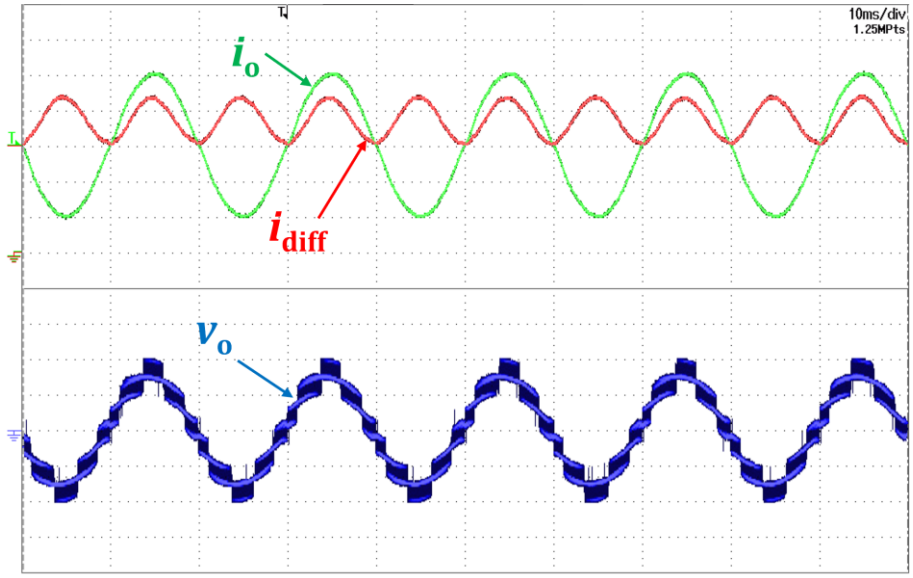


Figure 4.16 - Steady-state condition, from top to bottom: output current $\boldsymbol{i_o}$ (in green, 5 A/div); differential current $\boldsymbol{i_{diff}}$ (in red, 5 A/div); output voltage $\boldsymbol{v_o}$ (in blue, 20 V/div).

The experimental results corroborate the findings of the simulation studies. The injection of the differential current component i_{f} reduces the total energy ripple and provides improved control over the arm voltages. The decoupling of the control loops between the two arms, as demonstrated by the step change in $E_{\mathrm{u,ref}}$, ensures that each arm can be regulated independently, providing greater flexibility and stability in the overall system. These findings reinforce the viability of the proposed control strategy for practical MMC applications, showing that the control logic performs robustly both in simulations and real-world implementations.

4.8 Conclusions

The theoretical framework developed in this thesis offers a robust alternative to the conventional control strategies for MMCs, which typically focus on managing the total and differential arm energies. By introducing a novel technique grounded in the use of orthogonal functions, this approach enables precise generation of the circulating current reference and allows for direct control over the energy in each arm of the MMC. This framework not only simplifies the control structure but also enhances flexibility in energy regulation, leading to improved system performance.

The results from both simulations and experimental testing consistently demonstrate the reliability and stability of this control strategy. By aligning experimental outcomes with simulated predictions, this methodology has been validated across various operating conditions, proving its effectiveness in practical applications. The injection of a differential current component with twice the fundamental frequency, as developed in the control strategy, significantly reduces the energy ripple while maintaining high-quality output waveforms. The decoupling of control between the upper and lower arms further enhances the system's stability, enabling independent regulation of the arms and improving overall system efficiency.

In terms of performance, the MMC controlled via this innovative strategy achieves results comparable to traditional control methods, with the added advantage of introducing a new perspective for MMC analysis and control. The ability to manage each arm's energy independently and with precision, coupled with the reduction of energy ripple, makes this approach a promising alternative for a wide range of applications, including HVDC transmission and renewable energy systems.

In conclusion, the work presented in this chapter demonstrates the effectiveness and practicality of a novel MMC control strategy. The successful validation of this method, through both simulations and experimental implementation, underscores its viability for real-world applications.

Chapter 5

MODULATION STRATEGIES FOR LOSSES MINIMIZATION IN MATRIX RECTIFIERS

5.1 Introduction

The evolution of modern power systems has introduced increasingly complex requirements, particularly in applications involving energy management and the interfacing between electrical systems and various energy storage solutions. Power converters, acting as a bridge between alternating current (AC) and direct current (DC) domains, play a pivotal role in such systems. Among the many challenges these converters must address, the ability to manage bidirectional power flow and maintain high power quality is paramount, particularly in sectors such as renewable energy, electric vehicle (EV) infrastructure, and smart grids [100],[101].

Traditional passive rectifiers have been used for long time due to their simplicity, robustness, and relatively low costs. These rectifiers, typically composed of diodes and filters, are known for their ability to provide efficient power conversion under certain conditions. However, their drawbacks are becoming more apparent in modern applications, particularly when dealing with variable loads and dynamic power flows. One significant issue with passive rectifiers is their inherently high Total Harmonic Distortion (THD) in the input current [100],[101]. THD is a critical metric in power systems, as high levels of harmonic distortion can lead to inefficiencies, increased losses, and even damage to sensitive equipment. Passive rectifiers, even when supplemented with inductive filters, often fail to meet the stringent THD requirements of today's power systems. Furthermore, when thyristor-based rectifiers are used, the input power factor decreases as the output voltage decreases, introducing an additional layer of inefficiency.

In applications where the direction of power flow can reverse, such as vehicle-to-grid (V2G) or other smart grid interactions, passive rectifiers are generally unsuitable. These applications require bidirectional power flow, which passive rectifiers cannot accommodate without significantly more complex circuitry[100],[101]. This inability to reverse the

direction of power flow means that alternative converter topologies must be explored for such modern requirements.

Active rectifiers have emerged as a potential solution to overcome these limitations. Among them, three-phase pulse-width modulated (PWM) voltage-source and current-source rectifiers have shown superior performance, particularly in terms of controlling input current harmonics and power factor [102],[103]. Voltage-source rectifiers, for instance, are commonly employed as active front ends to the grid. These rectifiers use active switching devices such as IGBTs or MOSFETs to control the voltage and current waveforms, thereby reducing THD and enabling better power factor correction. However, while voltage-source rectifiers offer improved performance in many respects, they come with their own set of challenges. One notable limitation is that the DC-link voltage they produce is typically higher than the input phase-to-phase voltage. This characteristic makes them less suitable for applications requiring low DC output voltages, such as battery charging or other low-voltage loads. To address this mismatch, additional step-down converters or bulky transformers are often required, adding complexity, cost, and space requirements to the system.

On the other hand, current-source rectifiers have found their niche in applications where the output voltage is lower than the input voltage. These rectifiers are typically used in high-power applications, such as industrial motor drives or off-board fast chargers for electric vehicles,[104] where efficiency and performance are prioritized over size and simplicity. In lower power applications, voltage-source rectifiers tend to be favored due to their simpler control mechanisms, lower conduction losses, and wider availability of components. Nevertheless, current-source rectifiers remain a valuable option in certain high-power systems, especially where step-down operation and the lack of a need for bidirectional power flow are acceptable trade-offs [104].

A more versatile topology that has gained attention in recent years is the three-phase AC-DC matrix converter [105]. This converter offers several advantages over both passive and active rectifiers, including the ability to adjust the input power factor dynamically, reverse power flow, and reduce the harmonic content of both input and output currents. The AC-DC matrix converter is inherently a step-down converter, which makes it especially suitable for applications requiring low DC voltages, such as battery charging systems, renewable energy interfaces, or certain industrial processes. Additionally, because matrix converters eliminate the need for bulky energy storage components like capacitors and inductors, they enable more

compact designs, which are highly desirable in space-constrained applications such as electric vehicles or marine systems.

Despite the many advantages of the AC-DC matrix converter, the existing literature on this topology remains limited, particularly in comparison to the extensive research on AC-AC matrix converters. While several studies have explored various modulation strategies for improving the efficiency of AC-AC matrix converters [106],[107],[108], far less attention has been given to AC-DC matrix conversion. In recent years, however, a growing body of research has focused on optimizing the performance of AC-DC matrix converters, particularly in terms of minimizing switching losses and controlling harmonic distortion [109],[110],[111],[112],[113].

This chapter aims to contribute to this ongoing research by presenting a comprehensive analysis of a novel modulation strategy designed to minimize switching losses in three-phase AC-DC matrix converters. The proposed strategy is compared with seven space vector modulation (SVM) techniques, which have been widely used in the control of power converters. The comparative analysis presented in this chapter focuses on key performance metrics such as efficiency, harmonic distortion of input and output currents, and overall system reliability. All results are experimentally validated using a prototype matrix converter, and the performance improvements achieved by the proposed modulation strategy are demonstrated through a series of tests and measurements.

5.2 Modulation Techniques for Performance Optimization

Matrix converters, due to their ability to connect input and output phases directly through bidirectional switches, require precise control of their switching operations to achieve optimal performance. The absence of energy storage elements, such as inductors or capacitors, means that the input and output are directly linked, which presents both opportunities and challenges. On the one hand, the lack of intermediate energy storage reduces the physical size of the converter and allows for faster dynamic response. On the other hand, this configuration places greater demands on the modulation strategy to ensure that switching losses are minimized and that the desired output voltage and current characteristics are maintained.

The modulation strategy developed for this study is based on the space vector representation of the switch states. This approach has been widely adopted in the control of

matrix converters due to its ability to efficiently exploit the available input voltage while minimizing the RMS value of the current ripple. The core idea behind the space vector modulation (SVM) approach is to represent the various possible states of the converter as vectors in a complex plane. By appropriately selecting the sequence of vectors, it is possible to approximate the desired output voltage and current waveforms over each switching period.

In the case of AC-DC matrix converters, the challenge lies in managing the switch states to ensure that switching losses are minimized. Switching losses occur whenever a switch transitions between its on and off states, and they are proportional to both the voltage difference across the switch and the current flowing through it at the time of transition. To minimize these losses, the modulation strategy must carefully control the sequence of switch commutations to reduce the number of transitions and ensure that transitions occur under favorable conditions (i.e., when the voltage difference and current are minimized).

This study proposes a new modulation technique specifically tailored for AC-DC matrix converters. Drawing from established methods traditionally applied to AC-AC matrix converters, the proposed approach extends these techniques to the AC-DC domain, ensuring compatibility with the unique characteristics of this type of conversion. The performance of matrix converters is inherently dependent on the modulation strategy employed, and various strategies based on different mathematical frameworks have been developed in the past for direct three-phase matrix converters. Each of these strategies presents distinct advantages and limitations, such as differences in the number of switch commutations per switching period and the level of input voltage utilization.

SVM has been widely explored in the context of matrix converters due to its suitability for digital implementation, effective utilization of input voltage, and its ability to reduce the RMS value of the load current ripple. Extensive research has been dedicated to optimizing SVM for traditional direct AC-AC matrix converters, as demonstrated in the literature, where comprehensive solutions based on the representation of switch states as space vectors have been developed. This method highlights the various parameters that influence the performance of the modulation strategy, allowing them to be adjusted for optimal converter operation.

To achieve this, the states of the matrix converter switches are represented by two complex numbers, $\bar{m}_1$ and $\bar{m}_2$, which correspond to the two output phases of the converter. This strategy allows the input-output relationships of the converter to be expressed in terms of

space vectors, simplifying the control problem and providing greater flexibility in designing the modulation strategy.

Moreover, the modulation strategy proposed achieves the theoretical minimum in switching losses, demonstrating a significant improvement in efficiency compared to conventional methods. This optimization is particularly relevant in applications where minimizing energy loss and improving overall system efficiency are critical objectives.

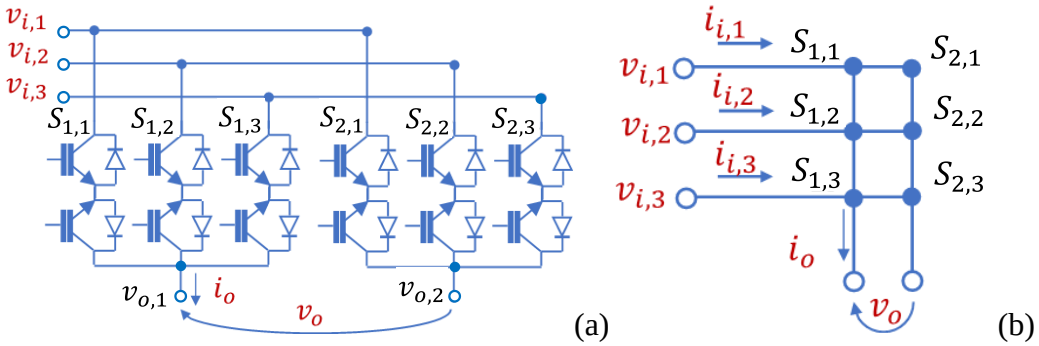


Figure 5.1 - Basic layout of a three-phase AC-DC matrix converter. (a) Converter architecture. (b) Matrix representation in simplified form.

In the following subsections, the mathematical formulation of the modulation strategy is presented in detail, and its impact on switching losses is analyzed.

5.2.1 Mathematical Modeling of Input-Output Dynamics

The operation of an AC-DC matrix converter can be understood through the relationships between its input and output voltages and currents. Matrix converters, by their design, directly connect the input to the output using bidirectional switches, making their control both complex and highly dependent on the modulation strategy. One of the key challenges in controlling these converters is ensuring that the desired output voltage is achieved while maintaining efficient power transfer and minimizing losses.

Matrix converters do not include passive components like inductors or capacitors to store energy, unlike traditional rectifiers. As a result, the instantaneous power at the input must equal the instantaneous power at the output, assuming ideal conditions with negligible converter losses. This characteristic introduces specific constraints on the converter's operation and requires a precise modulation scheme to manage the instantaneous input-output relationship.

With reference to Figure 5.1,the general expression for the output voltage v_o of a three-phase AC-DC matrix converter is given as:

$$v_o = v_{o1} - v_{o2} = \sum_{k=1}^{3} (m_{1,k} - m_{2,k}) v_{i,k} \tag{5.1}$$

where $v_{i,k}$ (with k=1,2,3) are the input voltages, and $m_{1,k}$ and $m_{2,k}$ represent the duty cycles associated with the bidirectional switches connecting the input and output phases. The duty cycles $m_{1,k}$ and $m_{2,k}$ control the fraction of time during which each input voltage is applied to the output.

As previously stated, the total power delivered to the load must match the power drawn from the input, this leads to the following power balance equation:

$$\sum_{k=1}^{3} i_{i,k} v_{i,k} = v_o i_o = \sum_{k=1}^{3} (m_{1,k} - m_{2,k}) v_{i,k}\, i_o \tag{5.2}$$

where i_o is the output current, and $i_{i,k}$ (for k=1,2,3) are the input currents. From (5.2), it holds:

$$i_{i,k} = (m_{1,k} - m_{2,k}) i_o \qquad k=1,2,3. \tag{5.3}$$

The modulation strategy must ensure that the duty cycles $m_{1,k}$ and $m_{2,k}$ are chosen in such a way as to avoid short-circuits between the input phases. To prevent over-voltage conditions and short circuits, the duty cycles must satisfy the following constraint:

$$\sum_{k=1}^{3} m_{h,k} = 1 \qquad h = 1,2 \tag{5.4}$$

This constraint ensures that at every instant, the sum of the duty cycles applied to the input voltages equals one, thereby preventing any discontinuity or imbalance in the converter's operation.

5.2.2 Space Vector Representation of Input-Output Equations

The space vector representation is particularly useful for power converters because it reduces the number of variables needed to describe the system. Instead of working with three separate phase voltages or currents, these quantities are combined into a single vector that captures the essential characteristics of the system. This approach is not only more efficient

but also provides greater insight into the converter's operation, especially when it comes to optimizing the switching sequences and reducing losses.

In the case of the AC-DC matrix converter, the input voltages $v_{i,k}$ and currents $i_{i,k}$ can be written as space vectors $\bar{v}_i$ and $\bar{\imath}_i$. These space vectors are defined as follows:

$$v_{i,k} = \bar{v}_i \cdot \bar{\alpha}_k \tag{5.5}$$

$$i_{i,k} = \bar{\imath}_i \cdot \bar{\alpha}_k \tag{5.6}$$

where $\bar{\alpha}_k$ is a complex exponential function that represents the phase relationships between the three input phases. Specifically, $\bar{\alpha}_k$ is given by:

$$\bar{\alpha}_k = e^{j\frac{2\pi}{3}(k-1)}. \tag{5.7}$$

This exponential function accounts for the phase shift of 120° between each phase in the three-phase system. By using space vectors, the control and analysis of the system are simplified, as the behavior of the three-phase converter can be represented by a single complex number rather than three separate quantities. Similarly, the states of the converter's switches can be described using two complex numbers, $\bar{m}_1$ and $\bar{m}_2$, which correspond to the two output phases of the converter. These complex numbers are defined as:

$$\bar{m}_h = \frac{2}{3}\sum_{k=1}^{3} m_{h,k}\bar{\alpha}_k\,, \quad h = 1, 2. \tag{5.8}$$

Here, $m_{h,k}$ are the duty cycles associated with the switches, and $\bar{\alpha}_k$ represents the phase angles. These space vector representations of the switch states simplify the description of the converter's behavior, making it easier to analyze and control.

Considering (5.8) and replacing (5.5) and (5.6) into (5.1) and (5.3), the input-output relationships for the three-phase AC-DC matrix converter can be expressed in terms of the space vectors $\bar{m}_1$ and $\bar{m}_2$. The equations for the output voltage and input current in terms of these space vectors are as follows:

$$v_o = \frac{3}{2}\bar{v}_i \cdot (\bar{m}_1 - \bar{m}_2) \tag{5.9}$$

$$\bar{\imath}_i = i_o(\bar{m}_1 - \bar{m}_2). \tag{5.10}$$

These equations indicate that the difference between the two space vectors $\bar{m}_1$ and $\bar{m}_2$ plays a crucial role in determining the output voltage and input current of the converter. The value of this difference is referred to as the direct component $\bar{m}_d$, and it is the primary factor influencing the performance of the converter.

$$\bar{m}_d = \bar{m}_1 - \bar{m}_2 \tag{5.11}$$

In addition to the direct component $\bar{m}_d$, another important variable is the zero-sequence component $\bar{m}_0$, this component does not affect the output voltage or input current directly, but it provides additional flexibility in the modulation strategy.

$$\bar{m}_0 = \frac{1}{2}(\bar{m}_1 + \bar{m}_2). \tag{5.12}$$

With these definitions, the input-output relationships of the converter can now be rewritten as:

$$v_o = \frac{3}{2}\bar{v}_i \cdot \bar{m}_d \tag{5.13}$$

$$\bar{\imath}_i = i_o \bar{m}_d \tag{5.14}$$

As can be observed from (5.13) and (5.14), both the output voltage and the input current depend only on the direct component $\bar{m}_d$, and not on the zero-sequence component $\bar{m}_0$. This behavior is similar to that observed in Pulse-Width Modulated (PWM) three-phase inverters, where the output voltage is independent of the zero-sequence component of the modulating signals. In AC-DC matrix converters, this role is played by the complex quantity $\bar{m}_0$ due to the increased complexity of the converter's structure.

If the desired direction of the input current space vector is denoted by the unit vector $\bar{\psi}_{ref}$, and the desired output voltage is denoted as $v_{o,ref}$, the direct component $\bar{m}_d$ can be derived by solving (5.13) and (5.14). The result is the following expression for $\bar{m}_d$:

$$\bar{m}_d = \frac{2}{3}\frac{v_{o,ref}\,\bar{\psi}_{ref}}{\bar{v}_i \cdot \bar{\psi}_{ref}} \tag{5.15}$$

Equation (5.15) provides a direct relationship between the desired output voltage, the input voltage space vector, and the input current direction. The zero-sequence component $\bar{m}_0$, can

be chosen freely to optimize the performance of the modulation strategy, providing additional flexibility in designing the control scheme.

Substituting (5.15) into (5.11) and (5.12), the values of $\bar{m}_1$ and $\bar{m}_2$ can be determined:

$$\bar{m}_h = (-1)^{h-1}\frac{\bar{m}_d}{2} + \bar{m}_0, \quad h = 1,2. \tag{5.16}$$

The quantity $\bar{m}_0$ represents two degrees of freedom that can be exploited to define any desired modulation strategy. The complex numbers $\bar{m}_1$ and $\bar{m}_2$ are essential for calculating the switch duty cycles, as they determine the switching behavior of the converter.

Finally, the duty cycles $m_{h,k}$, which control the state of the converter's switches, can be derived by solving (5.4) and (5.8). The solution is given by the following expression:

$$m_{h,k} = \frac{1}{3} + \bar{m}_h \cdot \bar{\alpha}_k, \quad h = 1,2, \;\; k = 1,2,3. \tag{5.17}$$

This general solution provides the foundation for all modulation strategies used in AC-DC matrix converters. By adjusting the values of $\bar{m}_d$ and $\bar{m}_0$, different modulation strategies can be implemented, each tailored to the specific performance requirements of the system.

By carefully selecting the value of $\bar{m}_0$, it is possible to optimize the switching sequences, reduce losses, and improve the overall efficiency of the converter.

The space vector formulation simplifies the control problem and provides a more intuitive understanding of the converter's behavior. By manipulating the direct and zero-sequence components, the modulation strategy can be optimized to achieve the desired output characteristics while minimizing switching losses.

5.3 Output Voltage Control Boundaries

The relationship between the input and output voltages is influenced by the duty cycles $m_{1,k}$ and $m_{2,k}$. These duty cycles control the amount of time for which each input phase is connected to the output, effectively shaping the output voltage. For the converter to function correctly, these duty cycles must remain within specific bounds, fulfilling the following constraint:

$$0 \leq m_{h,k} \leq 1, \quad h = 1,2; \quad k = 1,2,3. \tag{5.18}$$

This condition ensures that the converter's switches operate within their safe limits, preventing short-circuits between phases and avoiding overvoltages that could damage the components or reduce the reliability of the system. The sum of the duty cycles for each phase must always equal one, as established in the previous sections.

By considering the expressions (5.16) and (5.17) for $\bar{m}_d$ and $\bar{m}_0$, the constraint in (5.18) can be rewritten to reflect the relationship between the duty cycles and the space vector quantities. Specifically, (5.18) becomes:

$$0 \leq \frac{(-1)^{h-1}}{2} \bar{m}_d \cdot \bar{\alpha}_k + m_{0,k} \leq 1, \quad h = 1,2. \tag{5.19}$$

The term $m_{0,k}$ is defined as:

$$m_{0,k} = \frac{1}{3} + \bar{m}_0 \cdot \bar{\alpha}_k, \quad k = 1,2,3. \tag{5.20}$$

These equations show that the quantities $m_{0,k}$ (for k=1,2,3) are the components of the zero-sequence vector $\bar{m}_0$. The vector $\bar{m}_0$, which plays a key role in the modulation strategy, can be expressed as a linear combination of its components:

$$\bar{m}_0 = \frac{2}{3} \sum_{k=1}^{3} m_{0,k} \bar{\alpha}_k \tag{5.21}$$

Moreover, the sum of the components $m_{0,k}$ (for k=1,2,3) is equal to 1. This property ensures that the modulation strategy remains balanced and that the output voltage is properly controlled.

The inequalities in (5.19) can be further rewritten to emphasize the upper and lower bounds of the zero-sequence component $m_{0,k}$. The result is the following expression:

$$\frac{(-1)^{h-1}}{2} \bar{m}_d \cdot \bar{\alpha}_k \leq m_{0,k} \leq 1 - \frac{(-1)^{h-1}}{2} \bar{m}_d \cdot \bar{\alpha}_k \tag{5.22}$$

A closer examination of these bounds reveals that, under the worst-case scenario, the upper and lower limits of $m_{0,k}$ can be expressed as follows:

$$m_{0,k}^{min} \leq m_{0,k} \leq m_{0,k}^{max} \tag{5.23}$$

where:

$$m_{0,k}^{min} = \frac{1}{2}|\bar{m}_d \cdot \bar{\alpha}_k|, \quad k = 1,2,3. \tag{5.24}$$

$$m_{0,k}^{max} = 1 - \frac{1}{2}|\bar{m}_d \cdot \bar{\alpha}_k|, \quad k = 1,2,3. \tag{5.25}$$

The constraints in (5.24) and (5.25) ensure that the zero-sequence component remains within the permissible range, preventing the duty cycles from exceeding their operational limits. Since the upper bound of $m_{0,k}$ must always be greater than or equal to the lower bound, these equations imply the following constraint on the direct component $\bar{m}_d$:

$$|\bar{m}_d \cdot \bar{\alpha}_k| \leq 1. \tag{5.26}$$

This condition is critical for ensuring that the modulation strategy is feasible, and that the converter operates within its linear modulation range. Inserting (5.15) into (5.26) leads to the following expression:

$$\frac{2}{3}\left|v_{o,ref}\frac{\bar{\psi}_{ref} \cdot \bar{\alpha}_k}{\bar{v}_i \cdot \bar{\psi}_{ref}}\right| \leq 1 \qquad k = 1,2,3. \tag{5.27}$$

Equation (5.27) shows that the maximum voltage transfer ratio depends on the alignment of the input voltage space vector $\bar{v}_i$ and the input current direction $\bar{\psi}_{ref}$. Specifically, the voltage transfer ratio is maximized when $\bar{\psi}_{ref}$ is aligned with one of the space vectors $\bar{\alpha}_k$ (for *k*=1,2,3). Under this condition, the maximum voltage transfer ratio is given by:

$$\frac{|v_{o,ref}|}{|\bar{v}_i|} \leq \frac{3}{2}|cos\,\varphi_i| \tag{5.28}$$

where φ_i represents the input power factor angle, which is positive when the input current lags behind the input voltage vector. This angle plays a significant role in determining the efficiency of the power conversion process.

If (5.28) is satisfied, the AC-DC matrix converter operates within the linear modulation range, meaning that the modulation problem has feasible solutions. In other words, there exists at least one value of the zero-sequence component $\bar{m}_0$ that ensures all the duty cycles

remain within the allowed interval [0, 1]. This is crucial for maintaining the stability and reliability of the converter.

However, the optimal choice of $\bar{m}_0$ is not straightforward and depends on the specific operating conditions and performance criteria of the converter.

5.4 Space Vector Modulation

The application of SVM to matrix converters introduces additional complexities, as the converter must manage both the input and output voltages simultaneously. This requires careful coordination between the switching of the input and output phases, ensuring that the desired output voltage is achieved while maintaining proper control of the input current. The zero-sequence component, $\bar{m}_0$, plays an important role in this process, as it provides additional degrees of freedom that can be used to optimize the switching sequences.

There are several variations of the SVM technique, depending on how the zero vectors are employed. The most common strategies include SVM with three zero vectors (SVM 3Z), SVM with two zero vectors (SVM 2Z), and SVM with one zero vector (SVM 1Z). Each of these strategies offers different trade-offs between switching losses, harmonic distortion, and control complexity. For instance, using more zero vectors can reduce the number of switch commutations, thereby lowering switching losses, but it may also increase the harmonic distortion in the output current.

The set of possible configurations for an AC-DC matrix converter is illustrated in Table 5.1. Each configuration corresponds to a unique combination of switches being activated, and the resulting values for the space vector variables $\bar{m}_1$, $\bar{m}_2$, $\bar{m}_d$, and $\bar{m}_0$ are computed based on (5.8) and (5.14).

This table outlines the nine possible configurations of the matrix converter. The first six are active configurations that produce a non-zero output voltage, while the last three are zero configurations that produce no voltage output. The third and fourth columns show the instantaneous values of $\bar{m}_1$ and $\bar{m}_2$, while the fifth and sixth columns present the corresponding values for $\bar{m}_d$ and $\bar{m}_0$.

Table 5.1 - Configurations of the AC-DC Matrix Converter.

Conf. #	Switches	$\bar{m}_1$	$\bar{m}_2$	$\bar{m}_d$	$\bar{m}_0$
1	$S_{1,1}$ ON $S_{2,2}$ ON	$\frac{2}{3}\bar{\alpha}_1$	$\frac{2}{3}\bar{\alpha}_2$	$\frac{2}{3}(\bar{\alpha}_1 - \bar{\alpha}_2)$	$\frac{1}{3}(\bar{\alpha}_1 + \bar{\alpha}_2)$
2	$S_{1,1}$ ON $S_{2,3}$ ON	$\frac{2}{3}\bar{\alpha}_1$	$\frac{2}{3}\bar{\alpha}_3$	$\frac{2}{3}(\bar{\alpha}_1 - \bar{\alpha}_3)$	$\frac{1}{3}(\bar{\alpha}_1 + \bar{\alpha}_3)$
3	$S_{1,2}$ ON $S_{2,3}$ ON	$\frac{2}{3}\bar{\alpha}_2$	$\frac{2}{3}\bar{\alpha}_3$	$\frac{2}{3}(\bar{\alpha}_2 - \bar{\alpha}_3)$	$\frac{1}{3}(\bar{\alpha}_2 + \bar{\alpha}_3)$
4	$S_{1,2}$ ON $S_{2,1}$ ON	$\frac{2}{3}\bar{\alpha}_2$	$\frac{2}{3}\bar{\alpha}_1$	$\frac{2}{3}(\bar{\alpha}_2 - \bar{\alpha}_1)$	$\frac{1}{3}(\bar{\alpha}_1 + \bar{\alpha}_2)$
5	$S_{1,3}$ ON $S_{2,1}$ ON	$\frac{2}{3}\bar{\alpha}_3$	$\frac{2}{3}\bar{\alpha}_1$	$\frac{2}{3}(\bar{\alpha}_3 - \bar{\alpha}_1)$	$\frac{1}{3}(\bar{\alpha}_1 + \bar{\alpha}_3)$
6	$S_{1,3}$ ON $S_{2,2}$ ON	$\frac{2}{3}\bar{\alpha}_3$	$\frac{2}{3}\bar{\alpha}_2$	$\frac{2}{3}(\bar{\alpha}_3 - \bar{\alpha}_2)$	$\frac{1}{3}(\bar{\alpha}_2 + \bar{\alpha}_3)$
0_1	$S_{1,1}$ ON $S_{2,1}$ ON	$\frac{2}{3}\bar{\alpha}_1$	$\frac{2}{3}\bar{\alpha}_1$	0	$\frac{2}{3}\bar{\alpha}_1$
0_2	$S_{1,2}$ ON $S_{2,2}$ ON	$\frac{2}{3}\bar{\alpha}_2$	$\frac{2}{3}\bar{\alpha}_2$	0	$\frac{2}{3}\bar{\alpha}_2$
0_3	$S_{1,3}$ ON $S_{2,3}$ ON	$\frac{2}{3}\bar{\alpha}_3$	$\frac{2}{3}\bar{\alpha}_3$	0	$\frac{2}{3}\bar{\alpha}_3$

Figure 5.2 illustrates the admissible values of $\bar{m}_d$, which divide the complex plane into six distinct sectors. These sectors are used to determine the switching strategy, as the desired value of $\bar{m}_d$ (denoted as $\bar{m}_{d,ref}$) will always lie within one of these sectors. Knowing the reference value $\bar{m}_{d,ref}$, two vectors can be identified, $\bar{m}_d^L$ and $\bar{m}_d^R$, which define the boundaries of the sector. The vector $\bar{m}_d^L$ leads $\bar{m}_d^R$, with an example being sector 1, where $\bar{m}_d^L = \frac{2}{3}(\bar{\alpha}_1 - \bar{\alpha}_2)$ and $\bar{m}_d^R = \frac{2}{3}(\bar{\alpha}_1 - \bar{\alpha}_3)$.

The reference value $\bar{m}_{d,ref}$ over a switching period can be approximated as a linear combination of $\bar{m}_d^L$ and $\bar{m}_d^R$:

$$\bar{m}_{d,ref} = \delta^L \bar{m}_d^L + \delta^R \bar{m}_d^R \tag{5.29}$$

In (5.29), δ^L and δ^R represent duty cycles, which are numbers within the interval [0, 1]. Solving (5.29) for these duty cycles gives:

$$\delta^L = -\frac{\sqrt{3}}{2}\bar{m}_{d,ref} \cdot j\bar{m}_d^R \tag{5.30}$$

$$\delta^R = \frac{\sqrt{3}}{2}\bar{m}_{d,ref} \cdot j\bar{m}_d^L. \tag{5.31}$$

Once the application times for $\bar{m}_d^L$ and $\bar{m}_d^R$ have been determined, the remainder of the switching period is filled with the three zero vectors, thus introducing additional degrees of freedom. The duty cycles for the zero vectors, $\delta_{0,1}$, $\delta_{0,2}$ and $\delta_{0,3}$, must satisfy the following condition:

$$\delta_{0,1} + \delta_{0,2} + \delta_{0,3} + \delta^L + \delta^R = 1. \tag{5.32}$$

The switching sequence of the converter states for SVM is determined by the sector number in which $\bar{m}_{d,ref}$ resides.

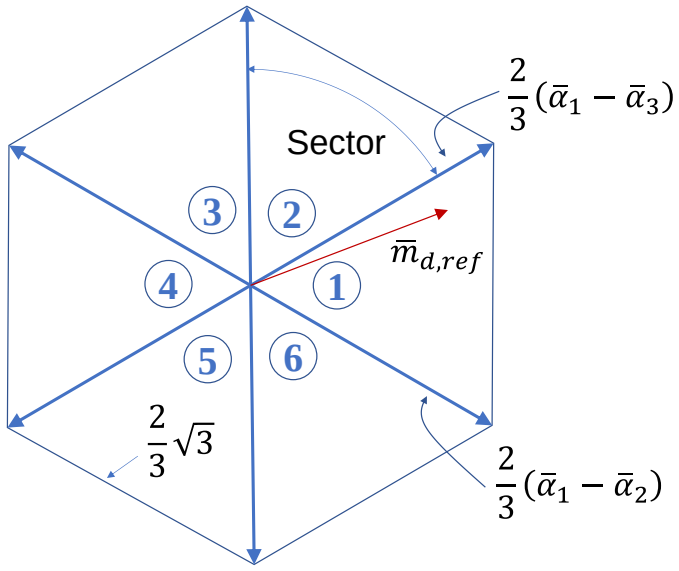


Figure 5.2 - Admissible instantaneous values of $\bar{\boldsymbol{m}}_{\boldsymbol{d}}$ and repartition of the plane into six sectors.

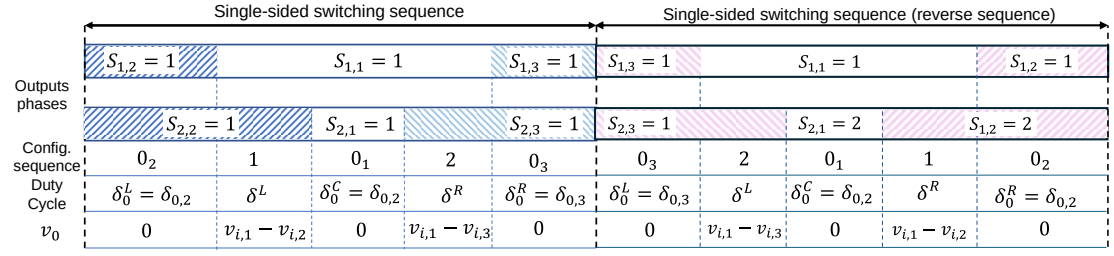
Table 5.2 outlines the sequence of vectors for each sector, highlighting the minimal number of switch commutations needed. Only two distinct sequences are possible, one being the reverse of the other, to minimize the total number of switch transitions.

These sequences represent the most efficient switching patterns for the matrix converter, with each sequence composed of three zero configurations and two active configurations. Configuration c_3, identical in both sequences, depends on the sector in which $\bar{m}_{d,ref}$ lies. The vector configuration c_3 corresponds to the phase with the highest instantaneous current. For instance, when the input current space vector resides in sector 1, the largest current flows through phase 1, meaning that configuration c_3 in Table 5.2 would be 0_1.

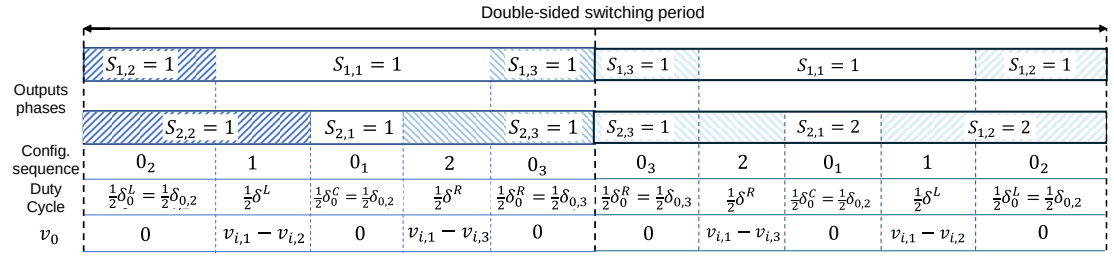
Table 5.2 - Sequence of Vectors for SVM (with reverse order possible).

	Vector sequence				
$\bar{m}_d$	0	$\bar{m}_d^L$	0	$\bar{m}_d^R$	0
Duty-cycles	δ_0^L	δ^L	δ_0^C	δ^R	δ_0^R
	Configurations $c_1 - c_5$ of the vector sequence				
Sector number	c_1	c_2	c_3	c_4	c_5
1	0_2	1	0_1	2	0_3
2	0_1	2	0_3	3	0_2
3	0_3	3	0_2	4	0_1
4	0_2	4	0_1	5	0_3
5	0_1	5	0_3	6	0_2
6	0_3	6	0_2	1	0_1

For completeness, Figure 5.3 illustrates the typical single-sided and double-sided switching patterns of the converter when $\bar{m}_{d,ref}$ is located in sector 1. In the double-sided switching pattern, the configuration sequence in the second half of the period mirrors that of the first half but in reverse order. In this example, all three zero configurations are utilized. When the duty cycles of the zero vectors are equal, the modulation strategy is referred to as SVM 3Z.



(a)



(b)

Figure 5.3 - Switching patterns with three zero-voltage configurations when the vector $\bar{m}_d$ lies in sector 1. Single-sided (a) or double-sided (b).

Other strategies, such as SVM 2Z and SVM 1Z, use fewer zero configurations, as indicated in Table 5.3. The letters "L", "C" and "R" correspond to the placement of the zero vectors within the switching period, standing for "Left", "Center" and "Right" respectively.

Table 5.3 - Modulation Strategies Based on Zero Configurations.

Modulation Strategy	Constraints	Zero configurations used in the sequence
SVM 3Z	$\delta_0^L = \delta_0^C = \delta_0^R$	c_1, c_3, c_5
SVM 2Zlc	$\delta_0^L = \delta_0^C, \delta_0^R = 0$	c_1, c_3
SVM 2Zlr	$\delta_0^L = \delta_0^R, \delta_0^C = 0$	c_1, c_5
SVM 2Zrc	$\delta_0^C = \delta_0^R, \delta_0^L = 0$	c_3, c_5
SVM 1Zl	$\delta_0^C = \delta_0^R = 0$	c_1
SVM 1Zc	$\delta_0^L = \delta_0^R = 0$	c_3
SVM 1Zr	$\delta_0^L = \delta_0^C = 0$	c_5

The choice of SVM strategy depends on the specific requirements of the application. For applications where efficiency is critical, minimizing switching losses may take precedence, leading to the selection of a modulation strategy that uses more zero vectors. In contrast, applications that require high power quality may prioritize minimizing harmonic distortion, even if this leads to slightly higher switching losses.

SVM 3Z, which uses three zero configurations, minimizes switching losses by reducing the number of active transitions. However, SVM 2Z and SVM 1Z may provide better harmonic performance under certain conditions by using fewer zero configurations.

5.5 Improvement in Switching Losses

5.5.1 General Expression of the Switching Losses

The determination of the duty cycles, as expressed in (5.17), does not fully specify a unique modulation strategy, as it is still possible to define different switching sequences, meaning different turn-on and turn-off orders for the switches.

In this context, the assumption is made that the same switching pattern is applied to both output phases. During the first half of the switching period, each output phase is connected to the input phases in a predefined order, based on the magnitude of the input voltages.

Specifically, each output phase is first connected to the input phase with the highest voltage, followed by the one with the intermediate voltage, and finally to the one with the lowest voltage. During the second half of the switching period, the sequence is reversed.

This switching pattern is known to minimize the switching losses of the converter, although it may slightly increase the harmonic content of both input and output currents. A simplified analysis is presented below for the first converter leg, under the assumption that a four-step commutation process is adopted. Considering the first half of the switching period, where the output pole voltage v_{o1} is sequentially connected to the input voltages $v_{i,a}$, $v_{i,b}$ and $v_{i,c}$. During the second half of the switching period, the sequence is reversed, forming a double-sided switching pattern.

The switching losses $P_{SW,1}$ for the first leg during the first half of the cycle can be expressed as follows [114]:

$$P_{SW,1} = f_{SW}\tau_{tot}|i_o|\left(\left|v_{i,a} - v_{i,b}\right| + \left|v_{i,b} - v_{i,c}\right|\right) \tag{5.33}$$

In this expression, f_{SW} represents the switching frequency, and τ_{tot} is a time constant that describes the energy loss per unit of voltage and current due to the switching actions. τ_{tot} can be decomposed into three components:

$$\tau_{tot} = \tau_{on} + \tau_{off} + \tau_{rec} \tag{5.34}$$

Here, τ_{on} and τ_{off} are the coefficients related to the energy loss during the turn-on and turn-off transitions of the IGBTs, while τ_{rec} accounts for the energy loss in the diodes due to reverse recovery currents.

Applying the triangular inequality, the switching losses for the first leg are bounded as follows:

$$P_{SW,1} \geq f_{SW}\tau_{tot}|i_o|\left(\left|v_{i,a} - v_{i,c}\right|\right). \tag{5.35}$$

Equality in (5.35) is achieved only when the input voltages are ordered such that $v_{i,a} \geq v_{i,b} \geq v_{i,c}$, or $v_{i,c} \geq v_{i,b} \geq v_{i,a}$. Therefore, the switching losses are minimized only if the input voltages follow a descending or ascending order.

As indicated by (5.35), under the assumption of an ordered switching pattern, the minimum power loss is independent of the intermediate voltage. Consequently, the switching losses do not change if the intermediate voltage is excluded from the switching pattern. Furthermore, if the switching pattern excludes either the maximum or minimum voltage, the

switching losses can be further reduced, as the voltage gap $|v_{i,a} - v_{i,c}|$ is decreased to either $|v_{i,b} - v_{i,c}|$ or $|v_{i,a} - v_{i,b}|$, respectively.

In general terms, if the indices of the input voltages in descending order (top, medium, and bottom voltages) are represented by the triplet (*t*,*m*,*b*), such that:

$$v_{i,t} \geq v_{i,m} \geq v_{i,b} \tag{5.36}$$

Then, the total switching losses for the entire converter can be expressed as:

$$P_{SW,tot} = P_{SW,1} + P_{SW,2} = f_{sw}\tau_{tot}\ |i_o| \sum_{h=1}^{2} \left(|v_{i,t} - v_{i,m}|\varepsilon_{top,h} + |v_{i,m} - v_{i,b}|\varepsilon_{bot,h} \right) \tag{5.37}$$

where $\varepsilon_{top,h}$ is a coefficient that equals 1 if the *h*th output pole voltage transitions from the maximum input voltage to another lower voltage level during the switching period, and 0 if this transition does not occur. Similarly, $\varepsilon_{bot,h}$ is 1 if the *h*th output pole voltage transitions to the minimum input voltage from another higher voltage level during the switching period.

Typically, all four coefficients $\varepsilon_{top,h}$ and $\varepsilon_{bot,h}$ (for h = 1, 2) are equal to 1. However, with a suitable choice of $\overline{m}_0$, up to two of these coefficients can be reduced to zero, further minimizing switching losses. If all coefficients remain equal to 1, (5.37) simplifies to:

$$P_{SW,tot} = 2f_{sw}\tau_{tot}|i_o|\left(v_{i,t} - v_{i,b}\right). \tag{5.38}$$

If the output pole voltages are synthesized without using all input voltages, the switching losses decrease compared to (5.37), as long as the intermediate voltage is not excluded from the switching pattern, since its absence does not affect the switching losses.

5.5.2 Optimal Zero-Sequence Component for Minimizing Switching Losses

The reduction of switching losses is achievable when an output pole voltage is synthesized without using the maximum or minimum input voltages, denoted as $v_{i,t}$ (the highest voltage) and $v_{i,b}$ (the lowest voltage). This condition occurs only when the zero-sequence components $m_{0,t}$ and $m_{0,b}$ take on their extreme values ($m_{0,t}^{min}$ and $m_{0,b}^{min}$ respectively), which lie at the lower and upper bounds of the admissible intervals, as defined by (5.23). Table 5.4

summarizes the four possible combinations of $m_{0,t}$ and $m_{0,b}$, which will be examined in detail below.

Table 5.4 - Values of the Zero-Sequence Components.

	$m_{0,t}$	$m_{0,b}$
Case 1	$m_{0,t}^{min} = 0.5\lvert\bar{m}_d \cdot \bar{\alpha}_t\rvert$	$m_{0,b}^{min} = 0.5\lvert\bar{m}_d \cdot \bar{\alpha}_b\rvert$
Case 2-A	$m_{0,t}^{max} = 1 - 0.5\lvert\bar{m}_d \cdot \bar{\alpha}_t\rvert$	$m_{0,b}^{min} = 0.5\lvert\bar{m}_d \cdot \bar{\alpha}_b\rvert$
Case 2-B	$m_{0,t}^{min} = 0.5\lvert\bar{m}_d \cdot \bar{\alpha}_t\rvert$	$m_{0,b}^{max} = 1 - 0.5\lvert\bar{m}_d \cdot \bar{\alpha}_b\rvert$
Not applicable	$m_{0,t}^{max} = 1 - 0.5\lvert\bar{m}_d \cdot \bar{\alpha}_t\rvert$	$m_{0,b}^{max} = 1 - 0.5\lvert\bar{m}_d \cdot \bar{\alpha}_b\rvert$

In Case 1, $m_{0,t}$ and $m_{0,b}$ are both set to their minimum values. Under this condition, two of the duty cycles, denoted as $m_{h^I,t}$ and $m_{h^{II},b}$, become zero, and the corresponding coefficients ε_{top,h^I} and $\varepsilon_{bot,h^{II}}$ also become zero. The indices h^I and h^{II} can be determined from (5.23) with $k = t$ and $k = b$, as indicated in Table 5.5.

Table 5.5 - Coefficients for Case 1, 2-A and 2-B.

Case 1	
$h^I = \begin{cases} 2 \; if \;\; sgn(\bar{m}_d \cdot \bar{\alpha}_t) \geq 0 \\ 1 \; otherwise \end{cases}$	$h^{II} = \begin{cases} 2 \; if \;\; sgn(\bar{m}_d \cdot \bar{\alpha}_b) \geq 0 \\ 1 \; otherwise \end{cases}$
Case 2-A	Case 2-B
$h^{III} = \begin{cases} 1 \; if \;\; sgn(\bar{m}_d \cdot \bar{\alpha}_t) \geq 0 \\ 2 \; otherwise \end{cases}$	$h^{IV} = \begin{cases} 1 \; if \;\; sgn(\bar{m}_d \cdot \bar{\alpha}_b) \geq 0 \\ 2 \; otherwise \end{cases}$

In Case 2-A, $m_{0,t}$ reaches its maximum value $m_{0,t}^{max}$, causing one of the duty cycles, $m_{h^{III},t}$, to equal 1. The index h^{III} is determined from (5.23) with $k = t$. Since $m_{h^{III},t} = 1$, the remaining duty cycles of the same output leg must be zero, thereby satisfying the condition $m_{0,b} = m_{0,b}^{min}$ in Table 5.4 for Case 2-A. This case corresponds to $\varepsilon_{top,h^{III}} = \varepsilon_{bot,h^{III}} = 0$.

Similarly, in Case 2-B, $m_{0,b}$ reaches its maximum value $m_{0,b}^{max}$, causing $m_{h^{IV},b}$ to equal 1, with h^{IV} determined by the same process. This case leads to $\varepsilon_{top,h^{IV}} = \varepsilon_{bot,h^{IV}} = 0$.

The case where both $m_{0,t}$ and $m_{0,b}$ reach their maximum values simultaneously is generally not considered because these conditions are usually incompatible with each other.

Once the values of $m_{0,t}$ and $m_{0,b}$ are determined, the zero-sequence component $m_{0,m}$ (corresponding to the intermediate voltage) can be calculated using the following equation:

$$m_{0,m} = 1 - m_{0,t} - m_{0,b}. \tag{5.39}$$

The value of $m_{0,m}$ from (5.39) must satisfy the constraints in (5.23). Using (5.21), the zero-sequence vector $\bar{m}_0$ can be expressed as:

$$\bar{m}_0 = \frac{2}{3}\left(m_{0,t}\bar{\alpha}_t + m_{0,m}\bar{\alpha}_m + m_{0,b}\bar{\alpha}_b\right). \tag{5.40}$$

It is important to note that Cases 2-A and 2-B are mutually exclusive. For Case 2-A, the zero-sequence component $m_{0,m}$ is given by:

$$m_{0,m} = \frac{1}{2}\left(|\bar{m}_d \cdot \bar{\alpha}_t| - |\bar{m}_d \cdot \bar{\alpha}_b|\right) \tag{5.41}$$

In Case 2-B, $m_{0,m}$ is expressed as:

$$m_{0,m} = \frac{1}{2}\left(|\bar{m}_d \cdot \bar{\alpha}_b| - |\bar{m}_d \cdot \bar{\alpha}_t|\right). \tag{5.42}$$

Since (5.41) and (5.42) are opposites, one of them will always be negative, which violates the positivity requirement imposed by (5.23). Thus, only one of these cases will yield a feasible solution.

Additionally, it can be verified that solutions for Case 2 exist only when the input power factor angle φ_i lies within the range $[-\frac{\pi}{6}, \frac{\pi}{6}]$. In the following subchapter a more detailed analysis is provided.

In summary, only two modulation strategies from Table 5.4 result in reduced switching losses. The first corresponds to Case 1, which is valid for any value of the input power factor, while the second corresponds to either Case 2-A or Case 2-B, but these exist only when $|\varphi_i| \leq \frac{\pi}{6}$.

5.5.3 Graphical Representation of the Switch States

Plotting $\bar{m}_1$ (or $\bar{m}_2$) on the complex plane reveals that these vectors lie inside a triangular region, as shown in Figure 5.4. The admissible values of $\bar{m}_1$ can be determined by

considering all possible duty cycles. Equation (5.17) indicates that the distances between $\bar{m}_1$ and the sides of the triangle are numerically equal to the duty cycles $m_{1,1}$, $m_{1,2}$ and $m_{1,3}$. Figure 5.4 (a) provides a visual representation of this concept. Similarly, the distances between $\bar{m}_2$ and the triangle sides correspond to the duty cycles $m_{2,1}$, $m_{2,2}$ and $m_{2,3}$.

When $\bar{m}_1$ or $\bar{m}_2$ lies on one of the triangle's sides, at least one duty cycle is zero, reducing the number of switch transitions per period. If $\bar{m}_1$ or $\bar{m}_2$ coincides with a vertex of the triangle, one of the duty cycles equals 1, while the remaining duty cycles are zero.

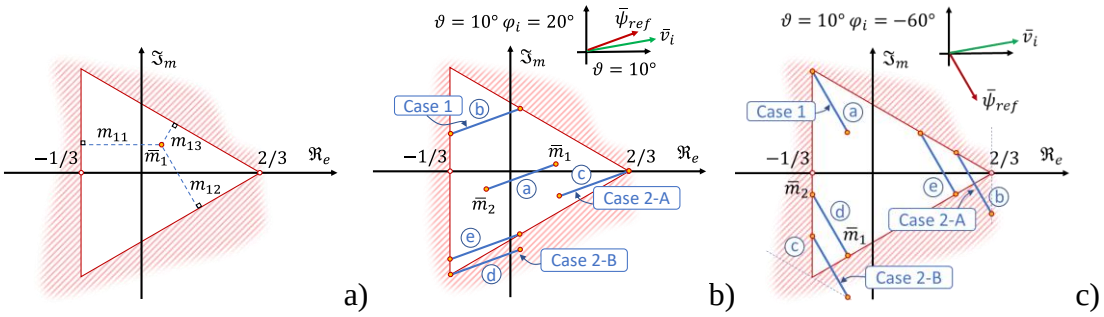


Figure 5.4 - Geometrical representation of $\bar{m}_1$ and $\bar{m}_2$. a) Graphical meaning of $\bar{m}_1$. b) Typical positions of the segment connecting $\bar{m}_1$ and $\bar{m}_2$ with an input power factor greater than 0.866 c) Typical positions of the segment connecting $\bar{m}_1$ and $\bar{m}_2$ with an input power factor lower than 0.866.

According to (5.16), $\bar{m}_1$ and $\bar{m}_2$ represent the endpoints of a segment that can be shifted by changing $\bar{m}_0$, which corresponds to the midpoint of the segment. Figure 5.4 (b) shows this segment in five different positions (a) through (e), assuming input current and voltage phase angles $\varphi_i = 20°$ and $\vartheta = 10°$, respectively. The maximum, intermediate, and minimum voltages are denoted by $v_{i,1}$, $v_{i,2}$ and $v_{i,3}$, i.e, (t, m, b) = (1, 2, 3).

In position (a), the segment does not touch the triangle's sides, so no commutations are avoided. Position (b) corresponds to Case 1 in Table 5.4, where both $m_{1,3}$ and $m_{2,1}$ are zero. In position (c), $\bar{m}_1$ coincides with a vertex, making $m_{1,1} = 1$ and both $m_{1,2}$ and $m_{1,3}$ zero. This condition falls under Case 2-A in Table 5.4. Position (d) corresponds to Case 2-B, where $m_{2,1} = 0$ $m_{2,2} = 0$ and $m_{2,3} = 1$. However, this configuration is invalid, as $\bar{m}_1$ lies outside the triangle.

Finally, position (e) offers a feasible solution to the modulation problem, with both $m_{2,1}$ and $m_{1,2}$ equal to zero. However, this condition is not included in Table 5.4 because it is

suboptimal, as excluding the intermediate input voltage does not lead to further reductions in switching losses.

Figure 5.4 (c) analyzes the possible segment positions when the input power factor angle φ_i is $-60°$. While Case 1 still leads to a valid configuration in position (a), Case 2-A and Case 2-B, corresponding to positions (b) and (c), produce invalid configurations. Positions (d) and (e) offer reduced switching losses, but to a lesser extent than Case 1.

5.5.4 Optimal Expression of the Switching Losses

By selecting the zero-sequence component according to Cases 1, 2-A, or 2-B in Table 5.4, the total switching losses can be simplified, as some of the coefficients $\varepsilon_{top,h}$ and $\varepsilon_{bot,h}$ (h=1, 2) become zero. Specifically, in Case 1, ε_{top,h^I} and $\varepsilon_{bot,h^{II}}$ are zero; in Case 2-A, $\varepsilon_{top,h^{III}}$ and $\varepsilon_{bot,h^{III}}$ are zero; in Case 2-B, $\varepsilon_{top,h^{IV}}$ and $\varepsilon_{bot,h^{IV}}$ are zero.

In all cases, the simplified expression for total switching losses is:

$$\begin{aligned} P_{sw,tot} &= f_{sw}\tau_{tot}|i_o|\left(\left|v_{i,t}-v_{i,m}\right|+\left|v_{i,m}-v_{i,b}\right|\right)= \\ &= f_{sw}\tau_{tot}|i_o|\left(v_{i,t}-v_{i,b}\right) \end{aligned} \tag{5.43}$$

This indicates that all cases theoretically produce the same amount of switching losses. The average switching losses, calculated over a full fundamental period of the input voltage, are:

$$P_{sw,avg} = \frac{3\sqrt{3}}{\pi}\tau_{tot}f_{sw}|\bar{v}_i||i_o|. \tag{5.44}$$

Thus, there is not a single optimal modulation strategy among Cases 1, 2-A, and 2-B in terms of switching losses. However, Case 1 is the preferred strategy, as it is valid for any value of the input power factor, while Case 2 produces feasible solutions only when the input power factor exceeds 0.866. Consequently, Case 1 is considered the optimal solution in the experimental validation.

5.6 Experimental Results

A series of experimental tests was conducted to assess the performance of the proposed modulation strategy. Figure 5.5 provides a schematic representation of the experimental setup.

The converter used for experimental validation features IGBT modules Infineon FM35E12KR3, while the control algorithm is implemented on a fixed-point digital signal processor (DSP) from Texas Instruments, model TMS320F2812. Key system parameters are listed in Table 5.6, and the converter operates using a four-step commutation process.

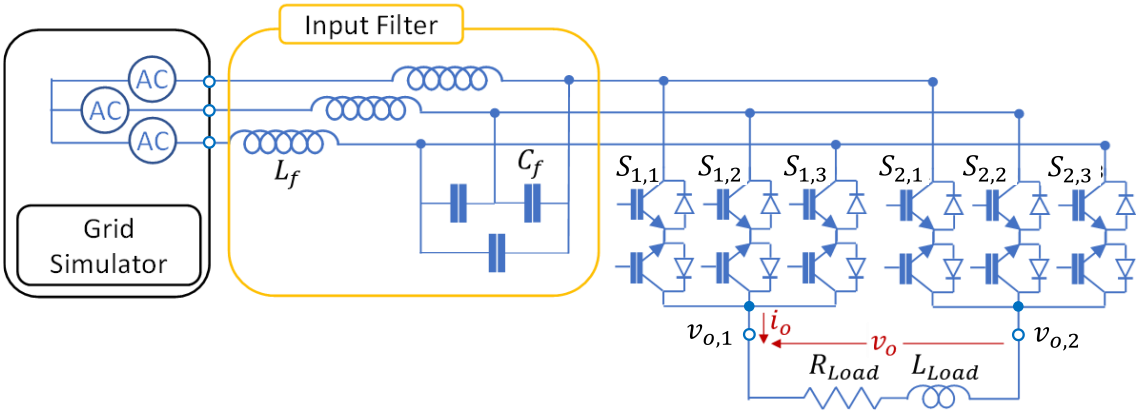


Figure 5.5 - Basic diagram of the AC-DC conversion system.

Figure 5.6 illustrates the switching losses of the IGBTs and diodes as function of the direct current, given a blocking voltage of 600 V and a junction temperature of 25°C. Although the prototype has a nominal power rating of around 12 kW, it currently operates at roughly 20% of its capacity (2.5 kW) since the power module has not yet been commercialized. The commutation process naturally introduces switching noise into the output voltage, which generally requires an LC filter to mitigate the ripple in the output current. However, in this study, the load is represented by a simple ohmic inductive impedance. Using a first-order low-pass filter allows for an accurate assessment of how the modulation strategies affect output current distortion, without the complexity introduced by more sophisticated filters.

Figure 5.7 illustrates the path traced by $\bar{m}_0$ and $\bar{m}_1$ in the complex plane under **Case 1**.

When the voltage transfer ratio reaches its maximum value (1.5), the limits of the linear modulation range become clearly defined. The vector $\bar{m}_1$ traces a path that aligns with the edges of an equilateral triangle. Under these conditions, $\bar{m}_d$ attains the highest amplitude allowed for linear modulation. As the voltage transfer ratio decreases, $\bar{m}_1$ continues to follow the sides of the triangle, albeit only partially. The exact position of $\bar{m}_1$ is influenced by the switching sequence and the input voltages, while $\bar{m}_0$ follows a trajectory determined by the rules outlined in Table 5.5.

Table 5.6 - Experimental Parameters.

Supply	Input Filter	Converter	Load
v_i = 150 V	L_f = 0.2 mH	f_{SW} = 10 kHz,	R_{Load}= 22.6 Ω
ω_G = 2π 60 rad/s,	C_f = 25 μF (Δ)	T_{dead} = 2 μs	L_{Load} = 2.36 mH
DC collector current		$I_{C,nom} = 35\ A\ @\ T_{CASE} = 80\ °C$	
Repetitive peak collector current		$I_{CRM} = 70\ A\ @\ T_{CASE} = 80\ °C, t_{PULSE} = 1\ ms$	
Collector emitter saturation voltage		$V_{CEsat} = 1.70\ V\ @\ T_{VJ} = 25\ °C$ $I_C = I_{C,nom}, V_{GE} = 15V$	
Diode forward voltage		$V_F = 1.65\ V\ @\ T_{VJ} = 25\ °C,$ $I_C = I_{C,nom}, V_{GE} = 15V$	
Collector-emitter voltages		$V_{CES} = 1200\ V$	
Thermal resistance junction-to-case		$R_{th,JC,trans} = 0.60\ K/W$ $R_{th,JC,diode} = 0.95\ K/W$	

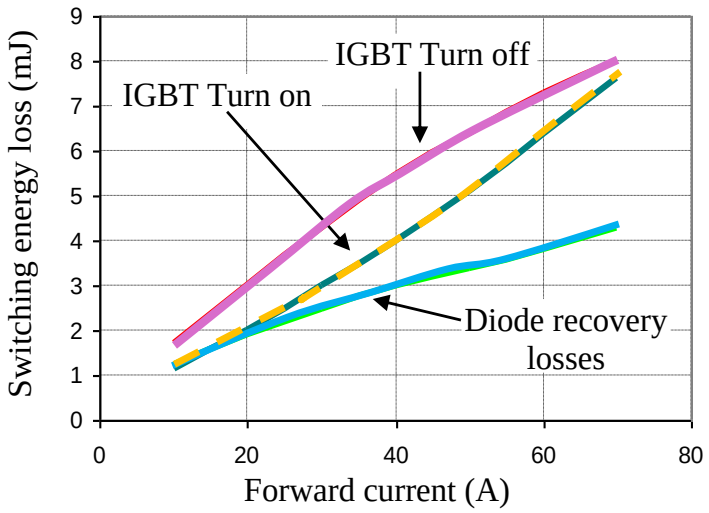


Figure 5.6 - Switching losses of the converter's IGBTs and diodes at a test voltage of 600 V and a junction temperature of 25°C.

Figure 5.8 illustrates the converter's behavior when operating with eight different modulation strategies, using a voltage transfer ratio of 0.9 and a power factor of 1. The proposed modulation technique is compared with seven space vector modulation strategies that reduce the number of commutations, as outlined in Table 5.3. The figure displays the waveforms for input current i_{i1}, input voltage v_{i1}, output current i_o, output voltage v_o, and the modulating signals for the first output leg $m_{1,1}, m_{1,2}, m_{1,3}$. It is evident that the input

voltage is almost perfectly in phase with the input current. The presence of the input filter capacitor causes a slight phase lead in the line current, which is influenced by the voltage transfer ratio. The line current is, in fact, the sum of the current flowing through the capacitor C_f (as shown in Figure 5.5), given by $j\omega_G C_f \bar{v}_i$ in steady state, and the converter's input current $\bar{\imath}_i$. As the voltage transfer ratio decreases, the converter's input current also decreases, while the current through the capacitor remains constant. This results in an increasing phase lead in the line current, which theoretically reaches 90 degrees when the converter's input current $\bar{\imath}_i$ is zero.

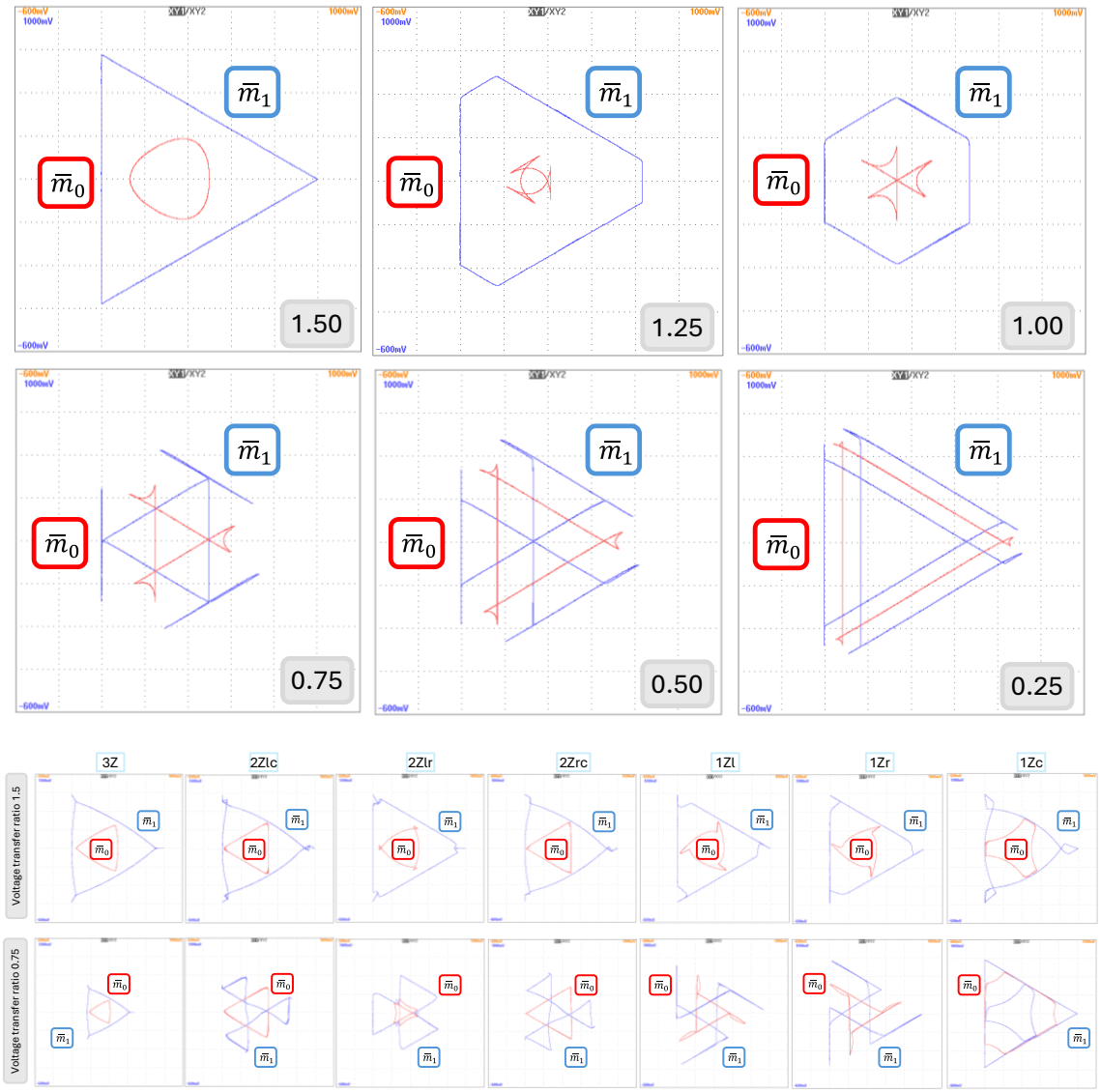


Figure 5.7 - Trajectories in the complex plane of $\bar{\boldsymbol{m}}_1$ and $\bar{\boldsymbol{m}}_0$ for Case 1 (a) and for conventional SVM strategies (b). The numbers inside the grey boxes are the voltage transfer ratios.

Based on the data in Figure 5.8, the power delivered to the load is approximately 2400 W, while the total power consumption is around 2500 W. The phase voltage at the input filter measures roughly 150 V peak, with a corresponding current of about 11 A peak. The capacitive current reaches 4.5 A peak, while the inductive current is around 12 A peak. The reactive power consumed by the filter is approximately -1000 VAR, causing the current to lead the voltage and resulting in a source power factor of approximately 0.9. The phase displacement of the input line current could be corrected by adjusting the reference phase angle $\bar{\psi}_{ref}$ directly or by implementing a dedicated control loop for managing the input power factor. However, this method was not applied in the current analysis to maintain simplicity in evaluating the modulation strategy.

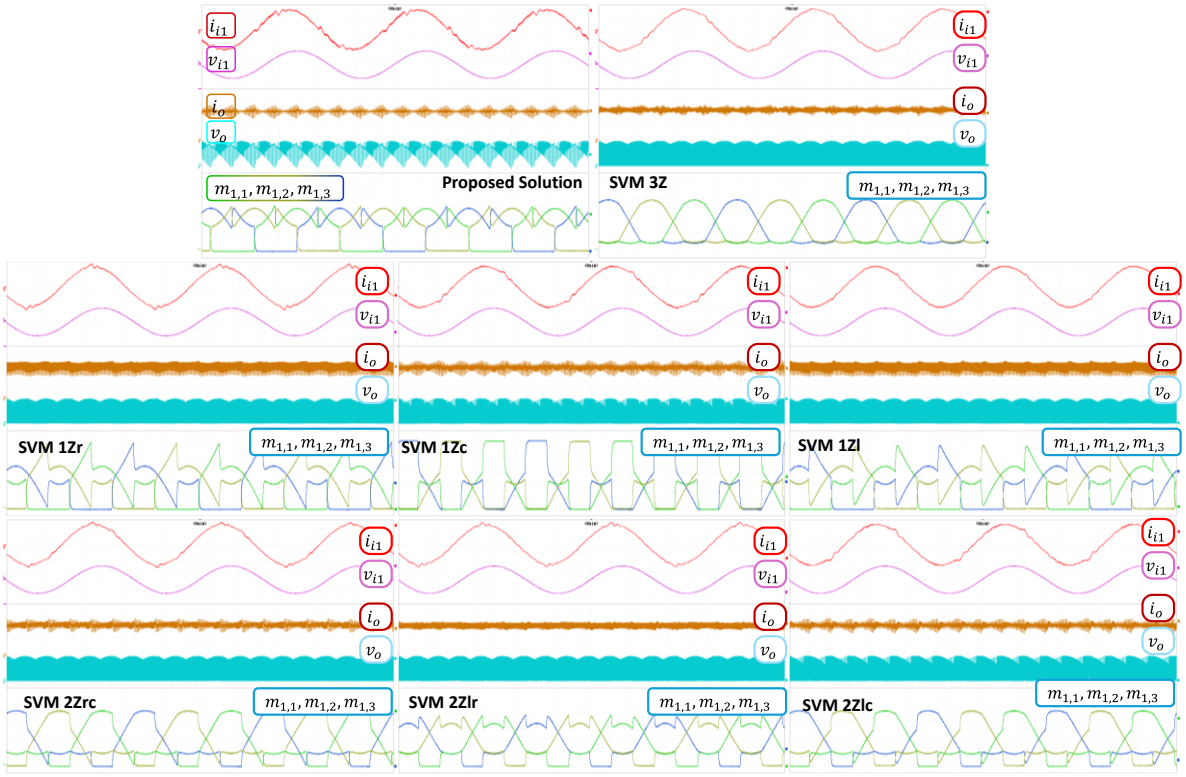
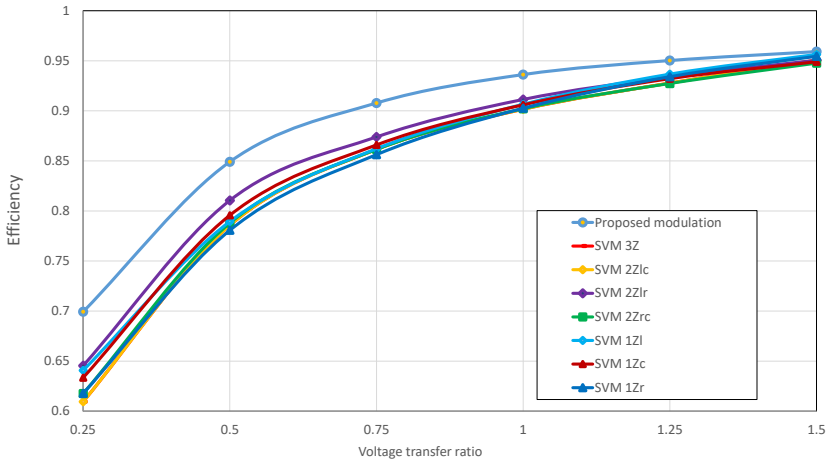


Figure 5.8 - Experimental performance of the AC-DC matrix converter with various modulation strategies at an input power factor of 1 and a voltage transfer ratio of 0.9. Input current i_{i1} (5 A/div), input voltage v_{i1} (100 V/div), load current i_o (2 A/div), output voltage v_o (50 V/div), modulating signals $m_{1,1}$, $m_{1,2}$, $m_{1,3}$ (0.2/div). Time scale: 5 ms/div.

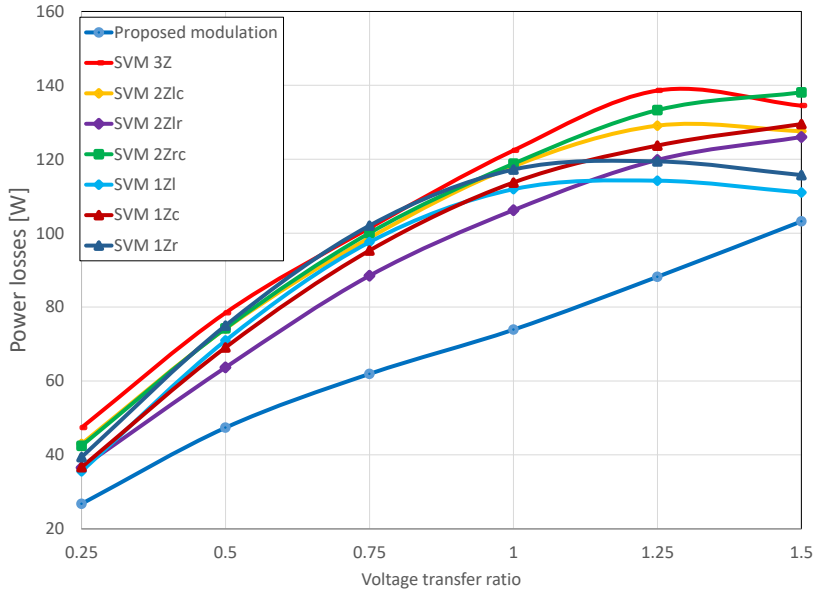
As shown in Figure 5.8, the modulation strategy associated with Case 1 consistently sets two modulating signals to zero. For high power factors, these zeroed signals correspond to two different output phases, as depicted in Figure 5.4 (b). Unlike the other modulation strategies, the symmetrical space vector modulation (SVM3Z) does not eliminate any

commutations. The remaining techniques reduce the number of commutations by selectively clamping some duty cycles to either 0 or 1.

The efficiency of the AC-DC matrix converter, when controlled using the eight different modulation strategies, was experimentally measured using a Yokogawa WT2030 power meter. Figure 5.9 presents the converter's efficiency and corresponding losses as a function of the voltage transfer ratio, with load conditions identical to those described in Figure 5.8.



(a)



(b)

Figure 5.9 - Performance of the AC-DC matrix converter under eight different modulation strategies with an input power factor of 1. (a) Efficiency. (b) Power losses.

As observed, the efficiency of the modulation strategy derived from Case 1 is significantly higher than that of the other SVM strategies, particularly at lower voltage transfer ratios, which aligns with the theoretical analysis. The efficiencies of the SVM 1Zr and SVM 1Zl

techniques are nearly equivalent due to the symmetrical nature of these modulation methods. While the commutation losses are not identical at any given moment, the average losses over the period of the input voltage are almost the same. Similarly, the losses associated with SVM 2Zlc and SVM 2Zrc are nearly identical, with only minor differences attributed to input filter losses and the varying effects of dead time in each case.

An approximate calculation of the converter losses can be made by comparing the input power with the efficiency values. When the proposed modulation strategy is compared to SVM3Z, a reduction in losses of approximately 24% is observed at the maximum voltage transfer ratio, and nearly 44% when the voltage transfer ratio is reduced to 0.25. These losses account for switching and conduction losses within the converter, as well as losses in the input filter and the clamp circuit.

The efficiency of the converter is influenced by both the switching and conduction losses of its components. To minimize switching losses, the modulation technique must ensure that each output terminal is connected to input terminals arranged in either ascending or descending order of input voltages. Traditional methods do not always follow this principle, leading to higher switching losses. The proposed theoretical approach, however, calculates the duty cycles for the bidirectional switches while identifying available degrees of freedom. For each output terminal, either the switch connected to the highest or the lowest input voltage remains unchanged, further reducing the switching losses.

Figure 5.10 presents the converter efficiencies for the modulation strategies outlined in Table 5.4, under different input power factor values. These results were obtained at the maximum possible voltage transfer ratio, as defined by (5.28). The improvement in efficiency achieved by the proposed modulation strategy remains consistent across all input power factor values.

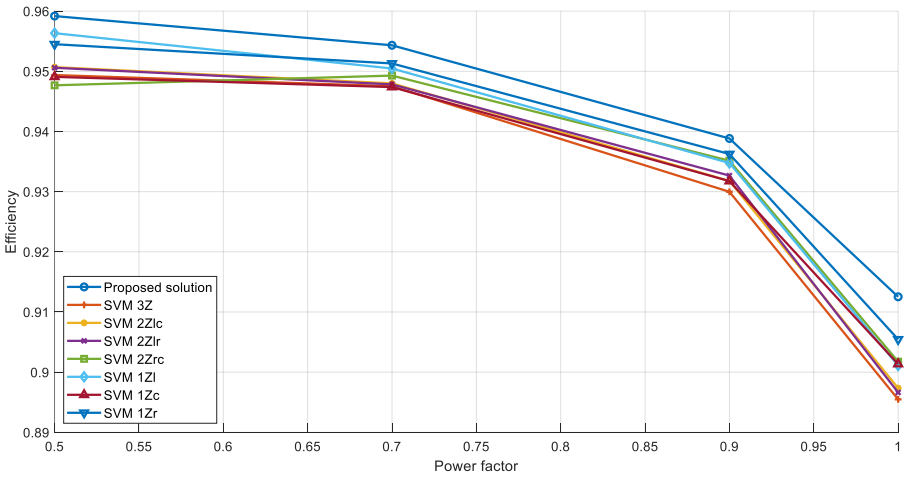


Figure 5.10 - Efficiency of the AC-DC matrix converter for eight different modulation strategies at the maximum voltage transfer ratio (1.5).

Figure 5.11 and Figure 5.12 illustrate the total harmonic distortion (THD) of both the load current and the input current as functions of the voltage transfer ratio, with the input power factor set to 1. The THD of the output current is defined by the following equation:

$$THD(i_o) = \sqrt{\frac{I_{o,RMS}}{I_{o,AVR}} - 1} \tag{5.45}$$

where $I_{o,RMS}$ and $I_{o,AVR}$ represent the RMS and average values of the output current, respectively.

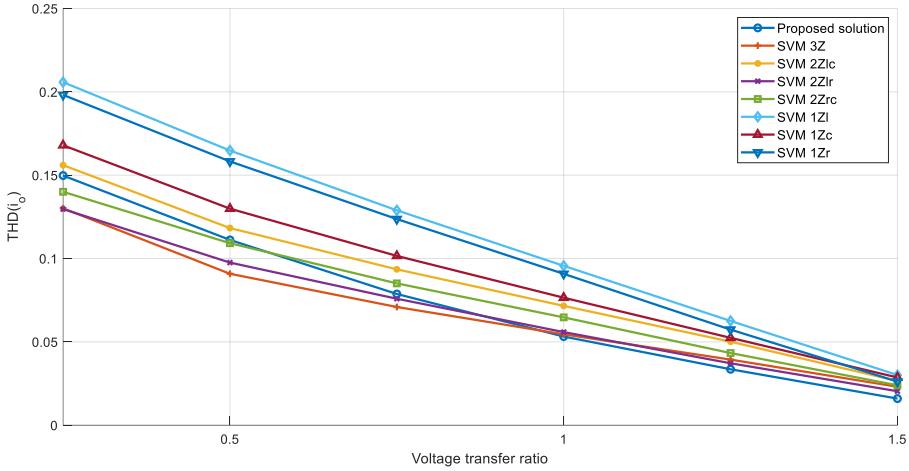


Figure 5.11 - Measured THD of the output current as a function of the voltage transfer ratio when the input power factor is 1.

The proposed modulation strategy exhibits the lowest distortion in both output and input currents at higher voltage transfer ratios. However, for voltage transfer ratios between 0.5

and 1.25, the input current distortion increases significantly, which can be attributed to the reordering of the switching pattern. The experimentally observed trend in the output current THD, as seen in Figure 5.11, lacks a clear theoretical explanation. The THD provides an overall measure of current quality over a complete cycle, making it difficult to pinpoint the exact factors that contribute to its reduction. Nonetheless, it is worth noting that the proposed technique tends to limit the variations in the potentials of the output terminals, which may positively influence the ripple of the load current.

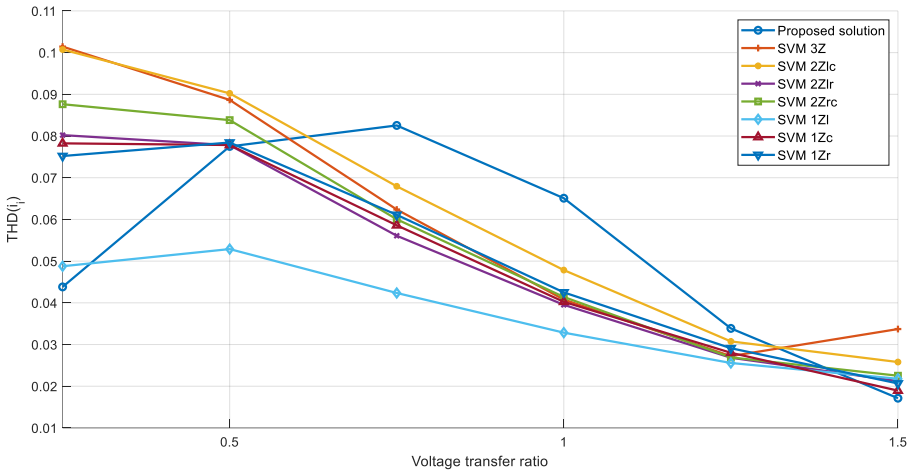


Figure 5.12 - Measured THD of the input current as a function of the voltage transfer ratio when the input power factor is 1.

Lastly, the converter's performance under transient conditions was tested. Figure 5.13 shows the waveforms of input and output voltages and currents following three step changes in the reference voltage transfer ratio, ranging from 0.75 to 1.5 in increments of 0.25. The figure also provides a closer look at two transients in the output voltage and current. After each step, the current stabilizes within 1 ms. It is important to note that the output current is not regulated in these tests, as a control loop was intentionally excluded to prevent adjustments to the voltage transfer ratio that could account for noise and nonlinearities, potentially affecting the evaluation of the modulation strategies.

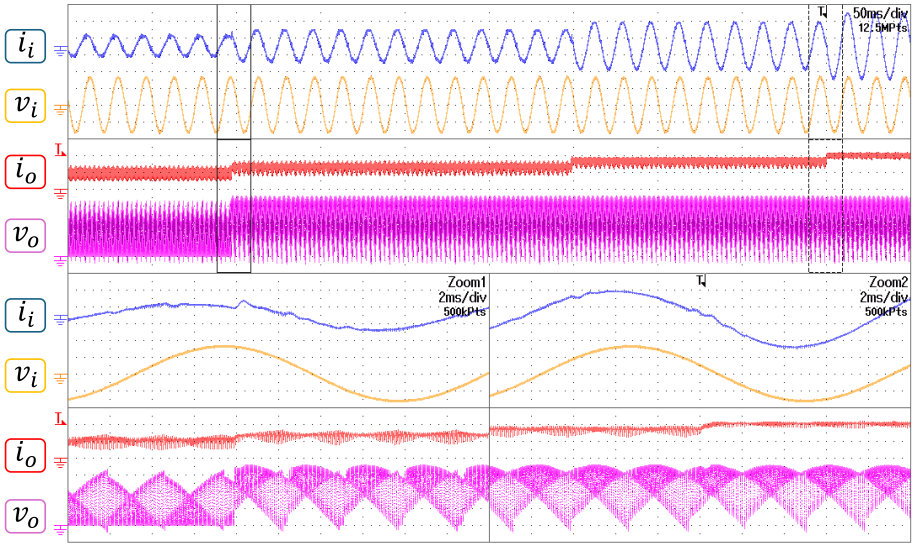


Figure 5.13 - Transient response of the converter during three step changes in the voltage transfer ratio (0.75, 1, 1.25, 1.5). From top to bottom: input current (5 A/div), input voltage (100 V/div), output current (5 A/div), output voltage (80 V/div).

5.7 Conclusions

The study presented in this chapter introduces a comprehensive methodology for analyzing the performance of three-phase AC-DC matrix converters, with a specific focus on minimizing switching losses through optimized modulation strategies. The proposed approach identifies a modulation technique that significantly reduces switching losses by tailoring the switching sequence and the zero-sequence component of the converter. This methodology not only achieves a systematic reduction in losses but also ensures that the converter operates within its safe and efficient boundaries across a wide range of voltage transfer ratios and input power factors.

The modulation strategy derived from Case 1, as examined in the experimental section, has been shown to outperform conventional SVM techniques, particularly in terms of switching losses. The experimental results demonstrate that, at the maximum voltage transfer ratio, the proposed strategy reduces switching losses by approximately 24% compared to the traditional SVM that uses three equally spaced zero vectors. This reduction becomes even more pronounced as the voltage transfer ratio decreases, with a nearly 44% reduction in losses observed at a transfer ratio of 0.25. Such a substantial improvement is of great importance for high-efficiency applications, where minimizing energy dissipation is a critical factor.

The experiments conducted validate the effectiveness and feasibility of the proposed modulation strategy. By examining multiple modulation techniques under identical conditions, it is evident that the proposed strategy not only reduces switching losses but also maintains the operational stability and performance of the converter. The consistent improvement in efficiency across a range of operating conditions, as well as the reduction in harmonic distortion, further reinforces the suitability of this strategy for practical applications. Moreover, the strategy's ability to adapt to different input power factors without compromising efficiency highlights its robustness in real-world scenarios, where input conditions may vary.

The results presented also underscore the versatility of the proposed methodology, which can be adapted to different converter configurations and operational requirements. The flexibility of the zero-sequence component allows for the fine-tuning of the modulation strategy, enabling further optimization based on specific performance criteria, such as minimizing harmonic distortion or reducing commutation losses. This adaptability makes the approach particularly relevant for applications in fields where power quality and efficiency are paramount, such as renewable energy systems, industrial drives, and electric vehicle charging stations.

In conclusion, the research conducted provides a solid foundation for further development of modulation techniques aimed at improving the performance of matrix converters. The significant reduction in switching losses achieved by the proposed strategy offers a clear advantage over traditional methods, while experimental validation ensures that the technique is both practical and reliable. Future work may focus on expanding the methodology to include fault tolerance and further reductions in harmonic distortion, ensuring that the next generation of matrix converters can meet even more stringent efficiency and performance requirements.

Conclusions

This PhD thesis has investigated power electronics solutions and architectures for industrial and high-power applications, addressing key challenges in the field through both practical and theoretical work. By focusing on energy efficiency, system flexibility, and scalability, the research aims to improve the performance of power systems in demanding environments.

The Poseidon Project demonstrated the potential of a hybrid Fast-Response Energy Storage System (FRESS), integrating KESS, SMES, and EESS to provide efficient power management in marine applications. The project highlighted the significant benefits of combining diverse energy storage systems to reduce fuel consumption and emissions, proving the feasibility of such solutions in dynamic power environments.

The study on PF coils, conducted in collaboration with ENEA Frascati, optimized the power supply systems of tokamak fusion reactors. By using supercapacitors, the research minimized the physical footprint while ensuring rapid energy release, crucial for stabilizing plasma in fusion energy applications.

The HVPG prototype addressed the need for compact, high-voltage pulse generators, achieving key performance metrics with fast rise times at 25 kV. The project revealed areas for further improvement in system reliability and optimization.

Theoretical work on MMC introduced new control strategies, improving performance in HVDC applications. Two-time scale analysis enhanced system stability under dynamic conditions, making MMCs more efficient in large-scale power transmission.

Finally, research on matrix rectifiers provided a high-efficiency alternative to traditional rectifiers, with the potential to improve AC-to-DC conversion in space-constrained, high-power environments.

This thesis offers practical insights and theoretical developments in power electronics, addressing both industrial needs and future research directions. The solutions discussed are relevant to current challenges in energy management and provide a foundation for further exploration in power electronics architectures and control strategies.

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