ALMA MATER STUDIORUM
UNIVERSITÀ DI BOLOGNA

ARCES – ADVANCED RESEARCH CENTER ON ELECTRONIC SYSTEMS
FOR INFORMATION AND COMMUNICATION TECHNOLOGIES E. DE CASTRO

SPECTRUM SHAPING AND ITS APPLICATION: SPREAD-SPECTRUM CLOCK GENERATOR AND CIRCUITS FOR ULTRA WIDE BAND

Luca Antonio De Michele

TUTORS

Professor
Riccardo Rovatti

Professor
Gianluca Setti

COORDINATOR

Professor
Riccardo Rovatti

PHD. THESIS
January, 2005 – December, 2007

PHD PROGRAM IN INFORMATION TECHNOLOGY
CYCLE XX – ING-INF/01

"Killing a fox with a hatchet has been a difficult task at any time, particularly when there was a phase error of as much as 180^o *between hunter and fox. Apparently both fox and peasant crossed the wall with exactly the same frequency, but the peasant wasn't able to obtain phase tracking."*

From Roland E. Best, "Phase-Locked Loops: theory, design and applications", New York, Mc Graw-Hill, 1984. Picture from Wilhelm Busch, Der Fuchs (The Fox)*, Rascher-Verlag, Zurich, Switzerland, 1881.*

Contents

Preface

A *spectrum*, as spoken of in this thesis, is a frequency domain representation of a signal. Any signal can be described in the time or frequency domain, and transforms (mathematical operators, e.g. the Fourier transform) are available for conversion of descriptive functions from one domain to the other and back again. Even as an oscilloscope window in the time domain for observing signal waveforms, so is a spectrum analyzer a window in the frequency domain. The spectra presented in this work are almost all spectrum analyzer representations, generated by sweeping a filter across the band of interest and detecting the power falling within the filter as it is swept. This power level is then plotted on an oscilloscope. All spectra referred to are power spectra.

The effort in using available spectrum in a way as more productively as possible, by studying new techniques, have started long time ago, since when its importance was recognized. Already in 1959 J. P. Costas [7] concluded that "for congested-band operation, broad-band systems appear to offer a more orderly approach to the problem and a potentially higher average traffic volume than narrow-band systems."

The spectrum can be identified as a *resource* for the designer then, as well as for the manufacturer, from two complementary points of view: first, because it is a good in great demand by many different kind of applications; second, because despite its scarce availability, it may be advantageous to use more spectrum than necessary.

This is the case of Spread-Spectrum Systems, those systems in which the transmitted signal is spread over a wide frequency band, much wider, in fact, than the minimum bandwidth required to transmit the information being sent. Spread spectrum applications started with the first communicator who set up a scheduled time to send and receive messages. This scheduling may have come about through a desire to avoid heavy traffic or a desire to avoid interception by surprising the would-be interceptor. The same technique of time was adapted by radio operators, but they added a new dimension: *frequency*. The

radio operator not only could schedule his transmission for a time unknown to an interceptor but could transmit at one of many frequencies, which forced the interceptor to "find" his transmission in addition to guessing its schedule. Encoding of messages for error correction and improved time and frequency selection naturally followed.

Beside their application to telecommunications, recently spread spectrum systems have received attention by other fields of electronics, in which signal processing such as *spectrum shaping* could signify an additional degree of freedom in the performance of the systems.

This thesis is organized in two parts. In part I, it is shown how it is possible to reduce the electromagnetic interference (EMI) of a clock signal in integrated circuits (ICs) design, through a spread spectrum technique. In part II, two applications of the emerging ultra-wide band (UWB) technology are presented, both dealing with the advantages as well as with the challenges of a wide-band system.

Part I

Spread Spectrum Clock Generator.

Chapter 1

Introduction

Electromagnetic interference (EMI) is a serious and increasing form of environmental pollution, whose effects range from minor annoyances, like the crackles on broadcast reception, to potentially fatal accidents, like the corruption of safety-critical control systems. Various forms of EMI may cause electrical and electronic malfunctions, can prevent the proper use of the radio frequency spectrum, can ignite flammable or other hazardous atmospheres, and may even have a direct effect on human tissue. As electronic systems penetrate more deeply into all aspects of society, both the potential for interference effects and the potential for serious EMI-induced incidents will increase.

Starting from the first experiments in radiocommunication, it has been observed that spark gaps generate electromagnetic waves which are very rich in spectral components and which are therefore likely to cause interference in electronic systems. Nowadays, several other sources of electromagnetic emission exist, ranging from radio transmitters and radars to relays and dc electric motors, as well as digital electronic devices. As an example, mobile cellular telephones are rapidly establishing themselves, through their sheer proliferation, as a serious EMI threat: passengers boarding civil airliners, for instance, have become familiar with the announcement that the use of such devices is not permitted on board.

The task of designing systems that may be considered *compatible* from the electromagnetic point of view, has so become of great practical concern. Electromagnetic compatibility (EMC) is defined [8] as "*the ability of a device, unit of equipment or system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbances to anything in that environment*".

A basic situation of interest for electromagnetic interference (EMI) analysis

can be schematically represented as electromagnetic energy emitted by a given *source*, which is transferred though a *coupling path* to an electronic device, or *victim*, where it is processed, potentially giving rise to undesired behaviors. This transfer of energy may be further broken into four subgroups, with regard to the prevention of interference: *radiated* emissions from the source and *radiated* susceptibility of the victim, as well as *conducted* emissions from the source and *conducted* susceptibility of the victim. To summarize, undesired signals may be either radiated or picked up by the power cord, interconnection cables, metallic cabinets or internal circuitry of the subsystems, even though these structures or wires are not intended to carry the signals. From these considerations, three ways to prevent interference follow:

1. Suppress the emission at its source;

2. Make the coupling path as inefficient as possible;

3. Make the receptor less susceptible to the emission.

EMI effects were first analyzed with reference to military applications, especially in avionic and aerospace fields, but currently, due to the generalized adoption of electronic equipments, they are experimentally evaluated and carefully studied to find possible prevention methodologies for practically all electronic systems. Additionally, both the USA and the EU have dictated specific rules [9] for the maximum allowed radiation of devices in order to reduce electromagnetic pollution and the possibility of causing faults in nearby apparatuses. Since the regulations affect *any single* civil consumer electronic device and since producers need to be compliant to enter the market, EMI issues are obviously of great practical concern.

An interesting and important type of EMI is due to rapidly switching timing signals. In the following, two significant examples will be analyzed, such as pulse width modulated (PWM) control signals of switched-mode power converters, and synchronization signals in integrated circuits (ICs) design.

Switched-mode power converters are fundamental components in every modern electronic equipment. Being commonly controlled by a fixed frequency timing signal, switching converters result in impulsive, periodic currents and voltages components either in the circuits or in the power lines. Depending on the deployed power, such currents and voltages are typically relatively large so that they can be considered responsible for the largest part of the EMI produced by the system. The emitted and conducted EMI spectra is clearly tightly related to the spectrum of such signals, and, thanks to periodicity is

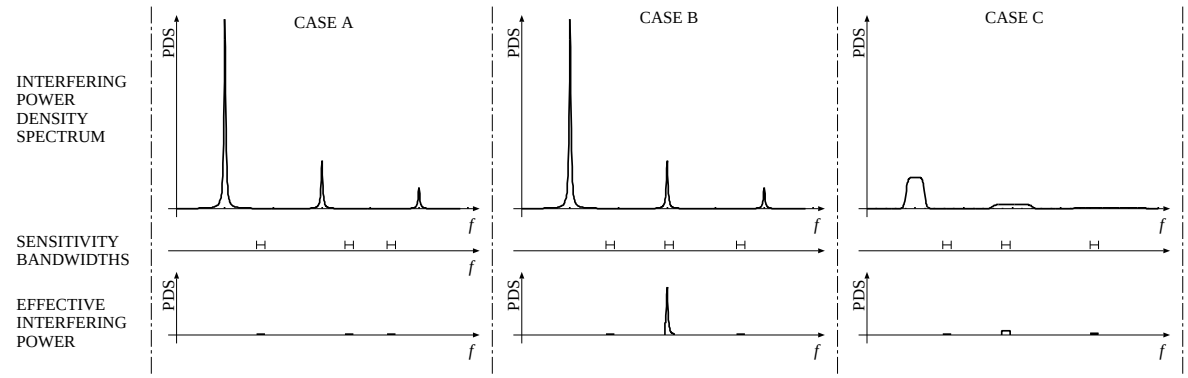


Figure 1.1: Relating the EMI which can effectively disturb a victim operation to the EMI PDS and the victim sensitivity bandwidths. Case A - the EMI PDS is concentrated and not overlapped with the victim sensitivity bandwidth: the victim is unaffected; case B - the EMI PDS is concentrated and overlaps the victim sensitivity bandwidth: the victim receives a large portion of the emitted power and fails; case C - the EMI PDS is spread: the victim cannot receive more than a small fraction of the emitted power and survives

composed by clusters of δ-like terms concentrated at the master timing signal and its harmonics [10][11][12](fig. 1.1, top plot of cases A and B). On the receiver side, victims are generally sensitive to electromagnetic noise due for instance to internal resonance phenomena and ringing. In other words, most potential victims are actually quite resistant to EMI and risk failure only if the interference falls in some narrow frequency windows where they are particularly good at absorbing electromagnetic energy from the environment. Hence it is common to model potential victims assuming that they have *narrow* sensitivity bandwidths, as also shown in fig. 1.1 (middle plots). The number and position of such bandwidths cannot generally be known but the information that they must be narrow is already very useful. In fact, the interference that can *interact* with a victim is approximately the product of the source EMI power density spectrum (PDS) by the characteristic functions of the sensitivity bandwidths. If the emitted spectrum is impulsive, it is quite unlikely that its non-null regions can intersect with the sensitivity bandwidth of a victim (case A in fig. 1.1), but if they do (case B) the victim receives a significantly large fraction of the emitted power, with a high risk of failure.

Power-supply filters, shielded cables and filtered connectors are common solutions to increase system EMC by *minimizing the coupling* between the source and the victim. The price of these solutions is both direct (packaging, wiring, manufacturability, etc.) and indirect (bulkiness, weight, marketability, product development schedule, etc.). Additionally, since the sensitivity bandwidth of the victim is unknown, there is no a-priori guarantee that their use may effectively increase EMI immunity.

As a consequence, increasing attention has recently been focused on alternative means to improve the EMC of switching power converters mixed signal circuits and boards [13], [14]. A possible alternative way to improve the EMC is the adoption of *signal processing methodologies* in order to *shape* the emitted PDS and to make it as spread as possible, thus *tuning* emissions at its source. With this (case C in fig. 1.1), the total emitted power remains unchanged and the probability of an intersection between the emitted PDS and a victim sensitivity bandwidth is actually increased. However, the amount of interference power which, in the worst case, can effectively disturb the victim is sensibly decreased. Note that the approach is coherent with EMC regulations [9][14]. In fact, the latter introduce masks under which the EMI PDS of a source (evaluated at a prescribed resolution and using prescribed methodologies) must fall. Typically masks are frequency-dependent, meaning that all the emitted harmonics are potentially dangerous. Obviously, sources which distribute their EMI power evenly over continuous ranges of frequencies have a much better chance of staying in-mask than sources which distribute their EMI in a localized fashion.

Also in the case of integrated circuits (ICs) design, signal processing based EMC enhancement techniques offer several advantages. To increase reliability and decrease system cost and size, a great effort is nowadays devoted to the implementation of ICs containing both the digital and the analog circuitry. This has a twofold consequence on the EMC design of these circuits. On one hand, the coupling path between digital and analog parts makes the latter more susceptible to interference from the digital clock signal. On the other hand, the typical solutions for increasing EMC by means of filtering and screening cannot be employed, so that the use of alternative method for interference reduction is obviously needed [15],[16],[17].

To achieve the desired result of spectrum spreading, one has to slightly modify the circuit generating the control timing signals by adding an additional modulation layer which operates by slightly anticipating or delaying its rising and falling edges, as in [13], [18] for power conversion, or in [15],[16],[17] for clock signals. Clearly, a trade-off exists in that one might want to perturb the PWM or clock signal, as much as possible to spread its spectrum, and as little as possible not to affect the system operation.

Let us also briefly comment on the characteristics of the external excitation which is needed to drive any possible additional modulation of the timing signal. It is intuitive that to break the periodicity of the timing waveform the excitation should be very irregular or noise-like. Random signals have been

proposed for this task [19][20], as well as *chaos-based* signals, i.e. excitations produced by discrete-time dynamical systems showing chaotic behavior. The advantages offered by the latter, for reducing the EMI due to timing signals, over other modulation techniques, have already been discussed [21] and supported by theoretical hints from the statistical approach to dynamical system theory [21][22].

Aim of this contribution is to present a validation of such theoretical results. Part I of this dissertation deals with a signal processing-based technique of EMI reduction for clock signals in IC design, named spread-spectrum clock generation (SSCG). Three different prototypes of chaos-based SSCG are presented in all their aspects: design, simulation, and post-fabrication measurements. For all three prototypes, the author has focused on the design and realization of the *modulator*, whereas the chaos-based modulating signal, still part of the monolithic implementation of the clock generator, has been studied and designed in the context of another PhD work. The interested reader is referred to Appendix A and references therein for an in-depth examination.

Part I of this work is structured as follows:

- Generation of low-EMI clock signals for digital circuits and boards is presented in chapter 2. Here the features of frequency-modulated (FM) clock signals are discussed: performance obtained by periodic and random, as well as chaotic, profiles of the modulating signals are compared. Some theorems are reported allowing to compute the PDS of chaos-based random FM clock signal, which link the statistical features of the modulating signal with the final spectrum; some measurement results confirming the superiority of chaotic techniques are also presented. Finally, a distinction between *slow* and *fast* modulation is introduced, and some results are addressed showing the best performance of the latter in terms of EMI.

- The design of a FM clock generator can be conveniently based on a phase-locked loop (PLL). PLLs are feedback systems that, if properly modified, can perform the additional function of frequency modulation, and consequently of SSCG. A brief description of such systems, as well as a mathematical linear model, is discussed in chapter 3. Some guidelines for the design of SSCG implementing either *fast* or *slow* modulation are derived in the conclusion.

- In chapter 4 the design of a PLL-based SSCG prototype aiming at reduc-

ing EMI through chaos-based fast random modulation is presented. The modulating signal is in turn given by the output of an ADC-based random number generator, obtained through a chaotic map. An established technology, such as AMS 0.35 μm CMOS, as well as a low frequency, $f_0 = 100$ MHz have been chosen because considered suitable for proving the theoretical results discussed in chapter 2. Measurements are presented, showing that the expected modulation is performed, and the desired spread of the clock power spectrum is achieved.

- The design of a second SSCG prototype, aiming at reducing EMI through the same chaos-based fast random modulation, is also presented in chapter 4. This SSCG has been obtained through a *scaling* to 180 nm of the first prototype, in order to operate at a higher frequency, namely $f_0 = 3$ GHz. Adopted values for f_0, as well as for frequency deviation, are suggested by Serial Advanced Technology Attachment II (SATA-II) protocol, and discussed in chapter 5. Serial ATA specifications [23] do suggest that a spread spectrum technique should conveniently be applied to its synchronization signal, in order to perform an on-chip EMI reduction. Since the modulation requested by the same protocol should be *slow* though, this implementation only aims at proving the benefits of fast modulation at high frequency. Measurements show that the desired modulation is performed, as well as clock power spectrum is shaped as expected. Regrettably, the measured working frequency is lower than expected, probably due to design-time mischaracterization of parasitic effects.

- Finally in chapter 5 a third SSCG prototype is presented, which aims at being possibly applied to standard Serial ATA-II. In the realized prototype, the spreading of the clock spectrum is achieved through a chaos-based random *slow* frequency modulation, as requested by the standard, which also sets the main frequency to $f_0 = 3$ GHz, along with the value of frequency deviation. The random modulating signal is given by the output of an ADC-based Random Number Generator, based on a chaotic map. Measurements are presented, showing as the expected modulation is performed, and the desired spread of the clock power spectrum is achieved.

The main innovative points developed by the author are here summarized:

- Two prototypes of a spread spectrum clock generator for EMI reduction which use a chaos-based fast random modulation have been implemented. They are described in chapter 4, and use an ADC-based RNG as source of randomness. These prototypes are the first that implements a frequency *binary fast* modulation (see chapter 2), which allows a maximum EMI reduction with respect to all other known modulations. See [3, 4, 5, 6].

- One prototype of a spread spectrum clock generator for EMI reduction which uses a chaos-based slow random modulation has been implemented. It is described in chapter 5, and uses an ADC-based RNG as source of randomness. This prototype is the first implementing a frequency *random* modulation to be proposed as a possible application to standard Serial ATA-II.

Chapter 2

Generation of low-EMI clock signals

Among the different strategies for generating high-EMC clock signals, increasing attention has recently been paid to simple frequency modulation (FM), rather than on *period modulation* for example used in [18].

This is particularly due to its rather intuitive effect on the shape of the power density spectrum (PDS) of the modulated signal. Roughly speaking, the resulting effect of the FM is to scatter the power of each harmonic over a wider bandwidth, which increases linearly with frequency, so that the spreading provided by the modulation method is also linearly increasing. Obviously, the effect obtained on the spectrum strongly depends on the modulating signal characteristics, ranging from pure sinusoids [14] to optimized frequency deviation profiles based on cubic polynomials [15], and, more recently, to random signals generated by one-dimensional chaotic maps [16][17].

More formally, consider first the simple case of a pure sinusoidal signal with frequency f_0:

$$s(t) = A\sin(2\pi f_0 t)$$

modulated by one with frequency f_m, and indicate with Δf the amplitude of the frequency change, or *frequency deviation*. As well known from basic modulation theory [24], the spectrum of the modulated signal

$$s(t) = A\sin(2\pi f_0 t + \Delta f/f_m \sin(2\pi f_m t))$$

presents side-band harmonics at frequency $f_0 \pm k f_m$, $k = 0, 1, \ldots$, whose amplitudes A_k satisfy the signal power conservation constraint $A^2 = A_0^2 + 2(A_1^2 + A_2^2 + \ldots)$. Moreover, according to Carson's rule, the total power of a FM signal

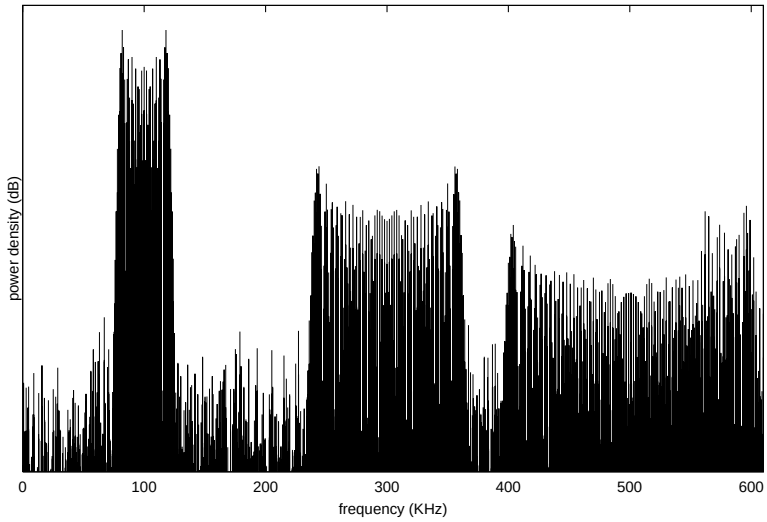


Figure 2.1: Power density spectrum of square waveform with $f_0 = 100$kHz frequency modulated by a sinusoidal signal with $f_m = 1$kHz and modulation index $m = 20$

is approximately contained inside a bandwidth of amplitude $B_P = 2(m+1)f_m$, where $m = \Delta f / f_m$ is the frequency *modulation index*. Therefore, the effect of the FM is to spread the power associated to the unmodulated signal over (approximatively) the bandwidth $[f_0 - B_P/2, f_0 + B_P/2]$, thus reducing the harmonics magnitude at frequency f_0.

If the unmodulated signal is a square wave, then it contains harmonics itself. Similarly to the previous case, the effect of the frequency modulation is still to scatter each harmonic component into side-band harmonics. However, according to Carson's rule, and since the modulation index of the n-th harmonics is n times the modulation index of the first harmonic, the amplitude of these band is $B_P^n = 2(nm+1)f_m \approx nB_P$ for $m \gg 1$. In rough terms, the general effect of FM is to spread out the power of each harmonic and the higher the harmonic number, the greater is the spread-out power. This effect is clearly identifiable in fig. 2.1 which represents the power density spectrum of a square wave with $f_0 = 100$kHz, frequency modulated by a sinusoidal signal with $f_m = 1$kHz and $m = 20$. Note how the critical contribution to EMI is given by the power in a neighborhood of the first harmonic.

Obviously, the FM carrier frequency f_0 and the frequency deviation Δf must be properly chosen so that $\phi(t) = \text{sgn}(s(t))$ can be seamlessly used for the timing of a digital apparatus. In other terms, neither f_0 nor Δf can be regarded as tunable parameters for achieving maximal EMC improvement; in fact, f_0 is fixed at the nominal clock rate, and Δf is superiorly bounded at ~ 5–$10\ \%$ of f_0

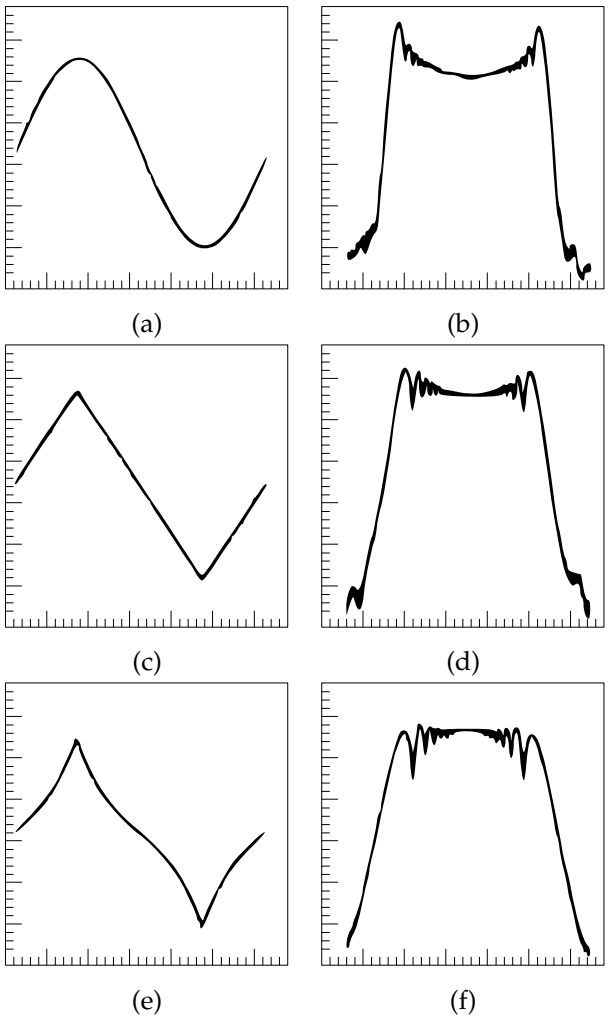


Figure 2.2: Comparison between *sinusoidal* (a) *triangular* (c) and *cubic* (e) modulating signals, in terms of resulting spectra, respectively (b), (d) and (f).

not to have a too irregular wave. Therefore only the features of the modulating signals can be exploited to optimize the power spectrum spreading.

A first step along this direction is reported in [15], where it is first noticed that a sinusoidal modulating waveform is not optimal for obtaining maximum attenuation of clock harmonics. This is due to the fact that the power in the spectrum of the modulated signal concentrates at those frequencies corresponding to points in the modulating waveform where the time derivative is small [24]. This effect can be clearly identifiable in fig. 2.1 where peaks are present, corresponding to frequencies where the time derivative of the sine wave is zero. On the contrary, at frequencies corresponding to the zero-

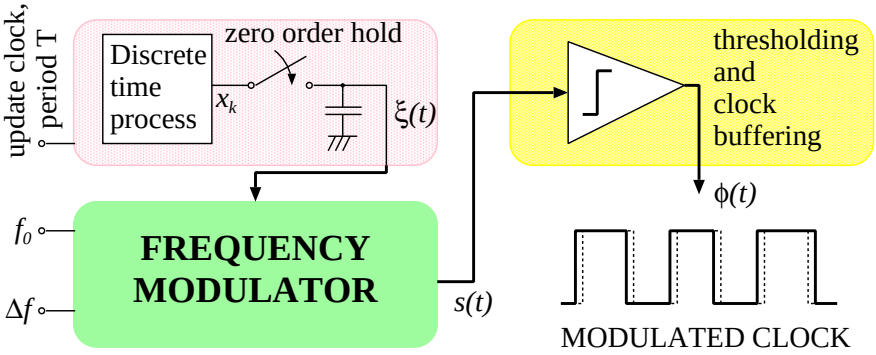


Figure 2.3: Architecture of the high-EMC clock synthesizer which needs to be optimized by a proper design of the signal source

crossing of the sinusoid, the amplitude of the harmonics is reduced since the time derivative of the modulating waveform is the largest. These effects can be appreciably reduced by using a properly chosen modulating signal resulting in a instantaneous frequency deviation generated by means of a suitable family of cubic polynomials, which has been optimized in order to increase the time derivative at the peaks of the modulating waveform and to reduce it at the zero crossing. With this, one can obtain a reduction of the PDS peak value of several dB with respect to sinusoidal modulating signal [15]. The comparison between the different profiles, in terms of resulting spectra, taken from [15], is shown in fig.2.2.

2.1 Random FM Clock Modulation

As long as the frequency deviation laws are periodic, the power is densely concentrated around specific frequencies (see also fig. 2.1) and thus the peak interference remains quite high. A way to achieve lower power densities relies on the availability of non-periodic modulating signals such as those coming from a random source or a discrete time chaotic system.

More precisely, let us refer to the block diagram of an high-EMC clock generator shown in fig. 2.3, where $s(t)$ is the continuous-valued output of an FM modulator whose driving signal is indicated as $\xi(t)$, and where $\phi(t) = \text{sgn}(s(t))$ is the candidate clock with edges which are slightly delayed or anticipated to avoid perfect periodicity.

To tackle the problem from a general point of view, let us express the mod-

ulating signal as

$$\xi(t) = \sum_{k=0}^{\infty} x_k g_{T_m}(t - kT_m),$$

where $g_{T_m}(t)$ is the rectangular pulse which is 1 within $[0, T_m]$ and vanishes elsewhere and $x_k \in [-1, 1]$ is the sample generated by a suitable source at time step k. In other word, we assume that $\xi(t)$ is produced by a discrete-time process and a zero order hold operation. Let us notice that the degrees of freedom in the modulating signal are limited to the update time T_m and to the samples $\{x_k\}$ themselves. In order to take advantage of them for EMI reduction, one needs to know how they relate to the PDS of $\phi(t)$.

To obtain such an analytical relationship, it is convenient to derive first the PDS of the baseband equivalent signal $\tilde{s}(t)$ of $s(t)$ [25]. If we indicate it as $\Phi_{\tilde{s}\tilde{s}}(\Delta f, T_m, \{x_k\}; f)$– to show that it is a function of the system parameters, of the statistical features of the source generating the samples $\{x_k\}$ and of f– then it can be proven that the spectrum $\Phi_{\phi\phi}$ of $\phi(t)$ is built of *replicas* of $\Phi_{\tilde{s}\tilde{s}}$, namely

$$\Phi_{\phi\phi}(f_0, \Delta f, T_m, \{x_k\}; f) = \sum_{i=0}^{\infty} \frac{8}{(2i+1)\pi} \Big[\Phi_{\tilde{s}\tilde{s}}\big((2i+1)\Delta f, T_m, \{x_k\}; f - (2i+1)f_0\big) + \Phi_{\tilde{s}\tilde{s}}\big((2i+1)\Delta f, T_m, \{x_k\}; -f - (2i+1)f_0\big) \Big] \quad (2.1)$$

Intuitively, this expression comes from the series expansion of a square wave into sinusoidal terms although the derivation is not completely straightforward [26].

Following consolidated methodologies [27], the computation of $\Phi_{\tilde{s}\tilde{s}}$ can be practiced by evaluating the Fourier transform of the average autocorrelation of $\tilde{s}(t)$. Through a non trivial derivation, for time-shifts $\tau > 0$ the latter can be cast as

$$\phi_{\tilde{s}\tilde{s}}(\tau) = \frac{1}{2T_m} \big(\mathbf{E}\big[w^{x_0 \tau / T_m}\big](T_m - \tau) g(\tau) + \int_0^{T_m} \sum_{n=1}^{\infty} g(t) g(t + \tau - nT_m) E_n(t, \tau) dt \big) \quad (2.2)$$

where $w = e^{\imath 2\pi \Delta f T_m}$ and $E_n(t, \tau)$ is defined as

$$E_n(t, \tau) = \mathbf{E}\big[w^{x_0(1 - t/T_m) + \sum_{j=1}^{n-1} x_j + x_n(t+\tau)/T_m - n)}\big] \quad (2.3)$$

from which one gets that PDS calculation passes through the computation of the expected values $\mathbf{E}[\cdot]$ of a complex observable of the samples $\{x_k\}$. Although it is not yet possible to deal with (2.3) in the most general terms, we

report here some analytical results for the case of samples $\{x_k\}$ generated by an i.i.d. random source (i.e. a source of independent and identically distributed symbols) or by a discrete time chaotic map. We will state the theorems without proof and the interested reader is referred to [28] and reference therein.

Our knowledge about the spectrum of random FM signals can be summarized with the following theorems.

Theorem 1 (Random-FM spectrum)**.** *If $s(t)$ is the output of an FM modulator with frequency deviation Δf, driven by a sequence $\{x_k\}$ having a pulse period T_m and made of i.i.d. samples whose probability density function is $\bar{\rho}(x)$, then:*

$$\Phi_{\tilde{s}\tilde{s}}(f) = \mathbf{E}_x\left[K_1(x,f)\right] + Re\left(\frac{\mathbf{E}_x^2\left[K_2(x,f)\right]}{1-\mathbf{E}_x\left[K_3(x,f)\right]}\right) \tag{2.4}$$

where

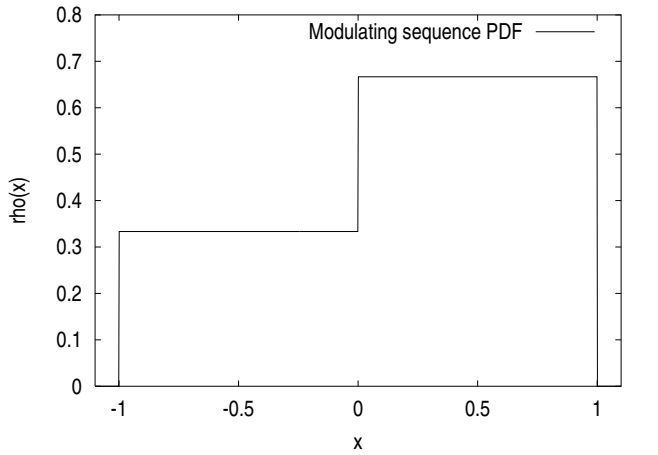
$$\begin{aligned} K_1(x,f) &= \frac{1}{2}T_m sinc^2(\pi T_m(f-\Delta f\, x)) \\ K_2(x,f) &= j\frac{e^{-j2\pi T(f-\Delta f x)}-1}{2\pi\sqrt{T_m}(f-\Delta f x)} \\ K_3(x,f) &= e^{-j2\pi T(f-\Delta f x)} \end{aligned} \tag{2.5}$$

Theorem 1 is a general analysis tool where equation (2.4) can conveniently take an integral form reminding that the statistical independence of $\{x_k\}$ implies that $\mathbf{E}_x[f(x)] = \int f(x)\bar{\rho}(x)\,dx$. The excellent conformance to numerical results can be remarked by an example. Suppose that a random modulating sequence, whose probability density function is as depicted in fig. 2.4 (a), is fed to an FM modulator with $f_0 = 100\,\mathrm{MHz}$ and $\Delta f = 8.5\,\mathrm{MHz}$ at a sample rate of 8.5 Msample/s. Figure 2.4 (b) shows the predicted spectrum and the one obtained by numerical simulations, almost completely superimposed.

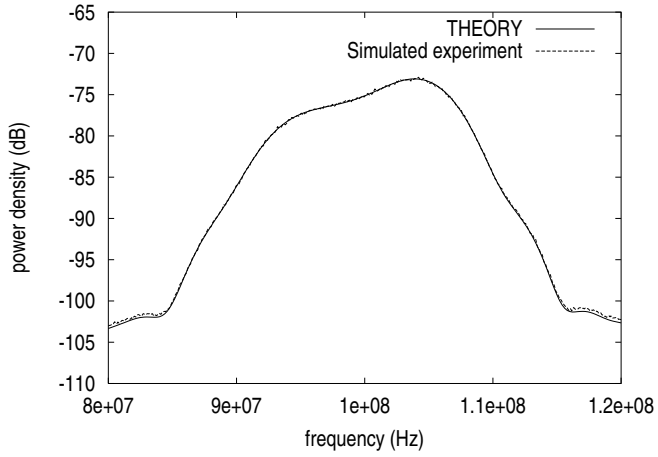
As shown in the next subsection, a further analytical result can be obtained under the assumption $T_m \to \infty$. Following an established approach [29], one shall refer to the large-T_m case as *slow* modulation, and to the opposite, small-T_m, as *fast* modulation. In the following, the two cases will be studied separately. Notice that in fact it would be more proper to distinguish among large and small modulation index. The confusion arises from the fact already observed that both f_0 and Δf are usually set by applications, thus making the two parameters T_m and m inter-independent.

2.1.1 Case of *slow* modulation

Theorem 2 (Slow-modulation Random-FM spectrum)**.** *If $s(t)$ is the output of an FM modulator with frequency deviation Δf, driven by a sequence $\{x_k\}$ having a pulse*



(a)



(b)

Figure 2.4: Application example for theorem 1. (a) modulating sequence PDF; (b) correspondent modulated signal spectrum.

period T_m, made of samples which are now not necessarily i.i.d.*, with a probability density function $\bar{\rho}(x)$, then:*

$$\lim_{T_m \to \infty} \Phi_{\tilde{s}\tilde{s}}(f) = \frac{1}{2\Delta f}\, \bar{\rho}\left(\frac{f}{\Delta f}\right) \tag{2.6}$$

Theorem 2 is a specialized analysis tool, for the slow modulation case. The advantage of specialization is twofold:

1. The much easier formulation of $\Phi_{\tilde{s}\tilde{s}}(f)$ as a function of $\bar{\rho}$. Note how a slow modulation implies that the modulated signal PDS is *shaped* as $\bar{\rho}$. This result can also be intuitively accepted: if T_m tends to infinity in fact,

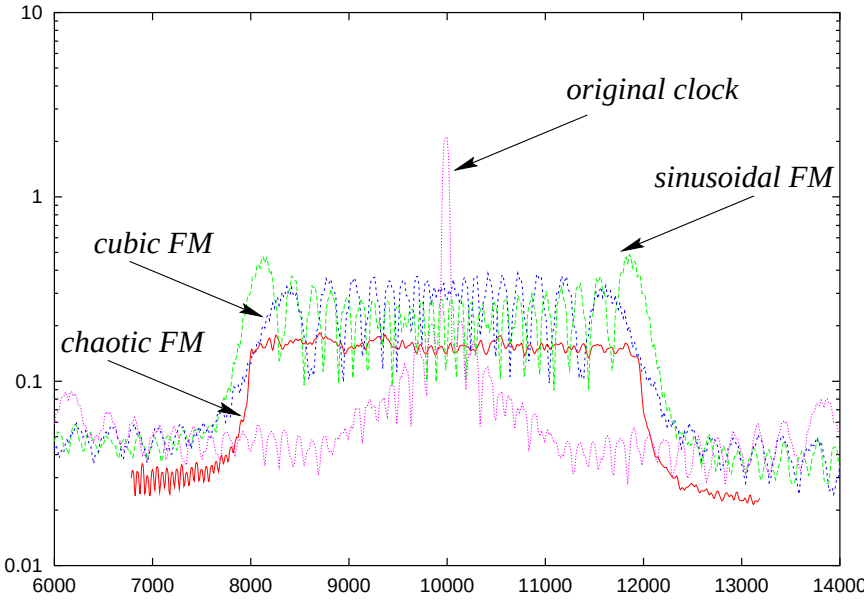


Figure 2.5: Experimental comparison between different clock spreading methods. $f_0 = 10\,\mathrm{kHz}$, $\Delta f = 2\,\mathrm{kHz}$ and $f_m = 50\,\mathrm{Hz}$. The resolution bandwidth of the 35670A digital spectrum analyzer has been set to $8\,\mathrm{Hz}$.

each instantaneous frequency of the modulated signal is hold for a time t, which in turn tends to infinity; this in the PDS is represented as a line. The contribution of each line to the whole PDS then, shall be weighted by the *continuous* probability associated to the symbol $\{x_k\}$ corresponding to the line itself.

It is worth noticing that this formulation is easily reversible, permitting to determine $\bar{\rho}$ in order to deliver a modulated signal conforming to a given spectrum. In other words, this theorem is also a synthesis tool [28]: if $\bar{\rho}$ is in fact shaped *uniformly*, then the modulated signal PDS will be *flat*, as can be observed in fig. 2.5.

2. The hypothesis that the source of symbols is "not necessarily" i.i.d. allows to choose as source of randomness a *chaotic* system [28] with proper characteristics, as described in Appendix A.

Figure 2.5 plots the measured PDS of the clock signals (in the neighborhood of the fundamental harmonic) modulated using the chaos-based technique compared with a non-modulated clock, one modulated using a sinusoidal signal, or an optimal periodic profile [15]. In all cases, $f_0 = 10\,\mathrm{kHz}$, $\Delta f = 2\,\mathrm{kHz}$ and $f_m = 50\,\mathrm{Hz}$ have been assumed and a tent map implemented with off-the-shelf components has been used as simple chaos generator. Mea-

surement have been performed using a digital spectrum analyzer, whose resolution bandwidth was set to $8\,\mathrm{Hz}$. From direct visual inspection one gets that a non-negligible improvement can be obtained with the chaos-based modulation technique. More quantitatively, the achieved attenuation, i.e. the difference between the peak of the unperturbed spectrum and the peak of the spread spectrum, is of ≈ 5dB for a sinusoidal modulating signal, ≈ 8dB for the method considered in [15] and of ≈ 15dB when chaos-based FM is employed.

2.1.2 Case of *fast* modulation

There is no theorem specialized for the case of fast modulation. As already observed, though, the modulating signal has got two degrees of freedom, namely the update time T_m and the samples $\{x_k\}$ themselves: the case of *slow* random modulation fixes the first one to infinity, and gets a result for the PDS of $\phi(t)$ depending on the statistic of the samples $\{x_k\}$.

A *fast* random modulation has been proposed in [30], wherein the fixed degree of freedom is on the contrary $\{x_k\}$, thus expecting the PDS of $\phi(t)$ to be dependent on T_m, or equivalently m. In particular, we get:

$$\bar{\rho}(x) = \frac{1}{2}\delta(x+1) + \frac{1}{2}\delta(x-1) \tag{2.7}$$

that is, the symbols $\{x_k\}$ can only assume two discrete values (-1 and +1), each one with identical probability $p = 1/2$. This kind of modulation is called *binary fast* random modulation.

As a consequence, also the instantaneous output frequency can only assume the two values $f_0 - \Delta f$ and $f_0 + \Delta f$. Now, if T_m was large, one would expect a corresponding PDS of $\phi(t)$ shaped as two peaks on the edge of the spread spectrum. On the contrary, being T_m a free degree of freedom, it is possible to obtain, by means of numerical optimization, a value of m that optimizes the shape of the PDS [30].

This is obtained, given the exact expression for $\Phi_{\bar{s}\bar{s}}(f)$, substituting equation 2.7 in 2.4 and looking for a numerical optimum for m: as a result, peaks in the PDS are minimized for the value:

$$m = \Delta f\, T_m = m_{\mathrm{opt}} \simeq 0.318;$$

whereas lower values of m cause the PDS to increase around 0, and higher values increase it around $f = \pm\Delta f$ (Figure 2.6) (this last result according to slow modulation case).

As already mentioned, each harmonic is described by a different modulation index: as a consequence, this optimization can be achieved *only* on one

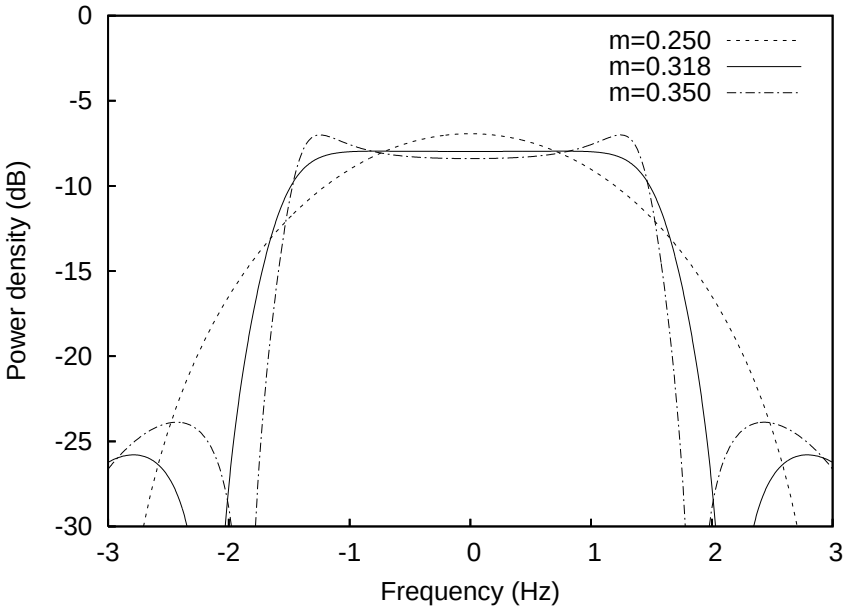


Figure 2.6: Normalized ($\Delta f = 1$) low-pass equivalent for PDS in the binary frequency modulation for value of the modulation index around m_{opt}

single harmonic; in particular, the optimum modulation index is:

$$\begin{aligned} m_{1_{\text{opt}}} &= m_{\text{opt}} = 0.318, && 1^{st} \text{ harmonic} \\ m_{3_{\text{opt}}} &= 3m_{1_{\text{opt}}} = 0.954, && 3^{rd} \text{ harmonic} \\ m_{5_{\text{opt}}} &= 5m_{1_{\text{opt}}} = 1.59, && 5^{th} \text{ harmonic} \\ &\ldots && \ldots \end{aligned}$$

Since the power content of the fundamental tone is much higher than that of all the other harmonics, and so are the corresponding peaks, the best result in overall peak reduction is achieved when the modulation index is optimized for the fundamental tone, i.e. $m = m_{\text{opt}}$.

Since *fast* modulation allows to gain 3 further dB on the fundamental tone, with respect to *slow* modulation, it can be considered the best choice for EMI reduction among all known modulation techniques [30].

It is worth noticing that in this case the condition that the source outputs binary symbols are i.i.d. is fundamental, descending from Theorem 1: on the another hand, symbols outputted by chaotic systems are not i.i.d, because *not independent* by definition. It has been proven, though, that by a proper quantization of the output of a chaotic system with certain characteristics, as described in Appendix A, it is still possible to obtain a source of i.i.d random symbols.

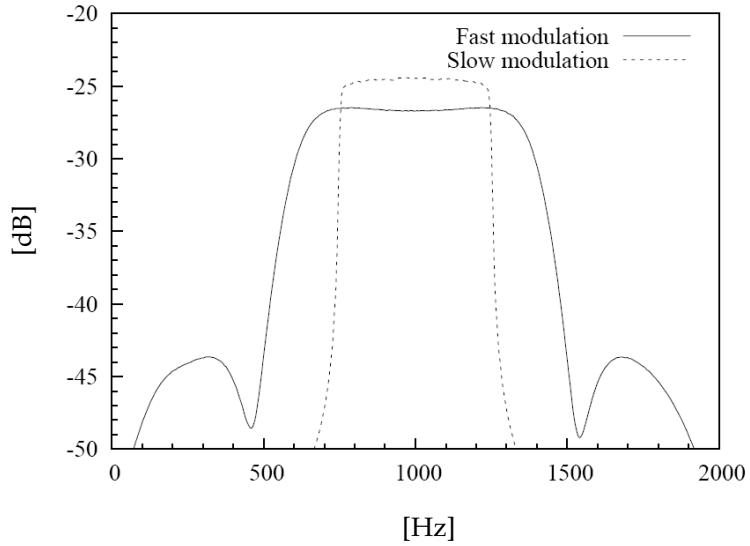


Figure 2.7: Comparison between fast and slow modulation; center-spread frequency $f_0 = 1$ kHz, $\Delta f = 250$ Hz and $m = 454$ for the slow modulation, $m = 0.318$ for the fast modulation.

2.2 Conclusion

Contrarily to conventional methodologies, signal processing methods are not about reducing the emitter energy of an interferer, but their aim is to affect the *way* in which the energy is emitted, to try to make it less dangerous for potential victims.

Clearly, signal processing has its greatest potential on those systems where the EMI is initially very much localized in frequency, so that the spreading action can make a big difference. On the case of digital clocked devices, where a timing waveform with a periodic structure is the dominant cause of the EMI issues, the signal processing approach is practiced by slightly altering the timing waveforms, through the addition of suitable modulation layers, in particular a frequency modulation.

The choice of modulating waveforms is fundamental; aperiodic waveforms have been proven to be superior to periodic ones. Since aperiodic waveforms are best described through their statistical features, their statistics have been related to the final emission spectrum and viceversa. In all cases there is evidence that the use of chaos-based random-FM modulations can reduce the peak values in the emitted PDS more than other published or patented signal processing methods, with a gain of 3 dB in the case of fast modulation with respect to the case of slow modulation [30] (fig.2.7).

It is worth noticing that when the modulating signal is slowly varying with

respect to the modulated one (slow modulation), a EMC norm compliant signal may still cause victim system to fail. Its output frequency in fact is maintained unaltered for a considerable period of time, thus an amount of energy sufficient to cause victim system failure may be transferred. If this happens, since FM spreads the signal frequency over a wider bandwidth, slow modulation may even cause an *increase* of interference, by enlarging the range of potential victims.

To conclude, fast modulation has to be considered preferable from the EMI point of view; it also provides the best peak reduction for the 1^{st} harmonic with respect to all other known modulations.

Chapter 3

Generation of a FM clock through a PLL

THE DESIGN of a frequency modulated (FM) clock generator can be conveniently based on a phase-locked loop (PLL). PLLs are feedback systems that were introduced to allow operations such as jitter reduction and frequency multiplication: if they are properly modified, they can perform the additional function of frequency modulation, and consequently its special case, that is spread-spectrum clock generation (SSCG). After a brief description of such systems, a mathematical linear model is discussed in this chapter; for an in-depth analysis of phase-locked systems the reader is referred to [31]. Some guidelines for the design of SSCG implementing either *slow* or *fast* modulation are derived in the conclusion.

3.1 Phase-Locked Loop

As every feedback system, the phase-locked loop (PLL) is a circuit that causes a particular system to track with another one. More precisely, the PLL is a circuit synchronizing an output signal (generated by an oscillator) with a reference or input signal, in frequency as well as in phase. In the synchronized state the phase error between the oscillator's output signal and the reference signal is zero, or remains constant. If a phase error builds up, a control mechanism acts on the oscillator in such a way that the phase error is again reduced to a minimum. In such a control system the phase of the output signal is actually *locked* to the phase of the reference signal: this is why it is referred to as a *phase-locked loop*. Every PLL consists of three main blocks: a *phase detector (PD), a*

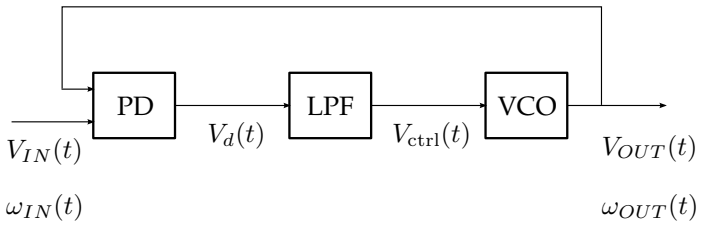


Figure 3.1: Phase-locked Loop.

low-pass filter (LPF) and a *voltage controlled oscillator (VCO)*. Referring to fig. 3.1, the operating principle of the PLL is described mathematically in the following.

The VCO oscillates at an angular frequency ω_{OUT} which is determined by the output signal $V_{\mathrm{ctrl}}(t)$ of the low-pass filter, so that:

$$\omega_{OUT}(t) = \omega_0 + K_{VCO} V_{\mathrm{ctrl}}(t)$$

where ω_0 is the center angular frequency of the VCO and K_{VCO} is the VCO gain in $rad\ s^{-1}V^{-1}$. The PD compares the phase of the output signal with the phase of the reference signal and develops an output signal $V_d(t)$ that is approximately proportional to the phase error $\Delta\phi$, at least within a limited range of the latter:

$$V_d(t) = K_d \Delta\phi$$

where K_d represents the gain of the PD. The output signal $V_d(t)$ of the PD consists of a dc component and a superimposed ac component: the latter is undesired, hence it is canceled by the low-pass filter.

Assume now that the frequency of the input signal is changed by the amount $\Delta\omega$. The phase of the input signal then starts leading the phase of the output signal: a phase error is built up and increases with time. The PD develops a signal $V_d(t)$, which also increases with time. With a delay given by the loop filter, $V_{\mathrm{ctrl}}(t)$ will also rise. This causes the VCO to increase its frequency. The phase error becomes smaller, and after some settling time the VCO will oscillate at a frequency that is exactly the frequency of the input signal, thus $\omega_{OUT} = \omega_{IN}$. Depending on the type of circuits used, the final phase error will have been reduced to zero or to a finite value. In most applications, a *divider* block is added in the feedback loop (fig. 3.2). Assuming that it divides the number of oscillations in a given time interval by a factor N, the frequency of the VCO output signal is forced to be N times the reference frequency, thus $\omega_{OUT} = N\omega_{IN}$. It is worth noticing that if the divider ratio N is made programmable, it is possible to synthesize the output frequency of the VCO, given one input frequency.

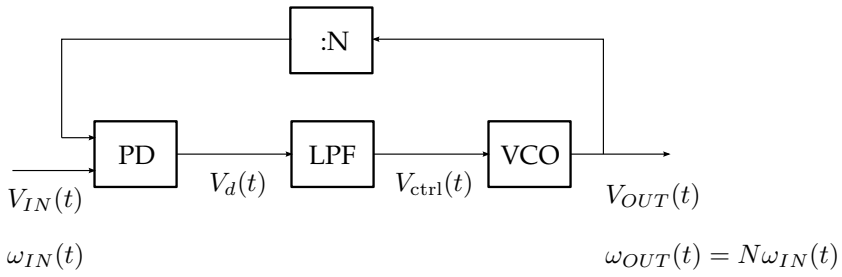


Figure 3.2: Phase-locked Loop with a divider.

One of the most important characteristics of the PLL is its ability to suppress noise superimposed on its input signal. If the input signal of the PLL is corrupted by noise, in fact, the PD tries to measure the phase error between input and output signals. The noise at the input causes the zero crossings of the input signal to be advanced or delayed in a stochastic manner: this causes the PD output signal to jitter around an average value. If the corner frequency of the loop filter is low enough, almost *no noise* will be noticeable in the signal V_{ctrl}, and the VCO will operate in such a way that the phase of the output signal is equal to the *average* phase of the input signal. Phase-locked systems have many possible applications, ranging from jitter reduction, skew suppression, clock recovery, etc. to frequency synthesis in wireless and RF applications, high-precision clock generation and the application of interest in this thesis, that is frequency-modulated clock generation.

Referring to fig. 3.2, a high precision clock generator can be obtained if the square-wave input signal is given by a low-frequency quartz, with constant frequency ω_{IN}. The PLL then multiplies by N the frequency of the input signal, and also suppresses the jitter introduced by the high-frequency VCO: thus originates a high-frequency square-wave which carries the same characteristics of accuracy and stability of the quartz.

Moreover, a FM clock generator can be obtained from a standard clock generator by properly adding a modulating signal in the scheme; the PLL will continue to perform its operation as described so far, plus the output frequency will somehow also depend on the modulating signal.

In order to study the possible realization of a SSCG through a PLL, in the following a mathematical model of the PLL will be analyzed.

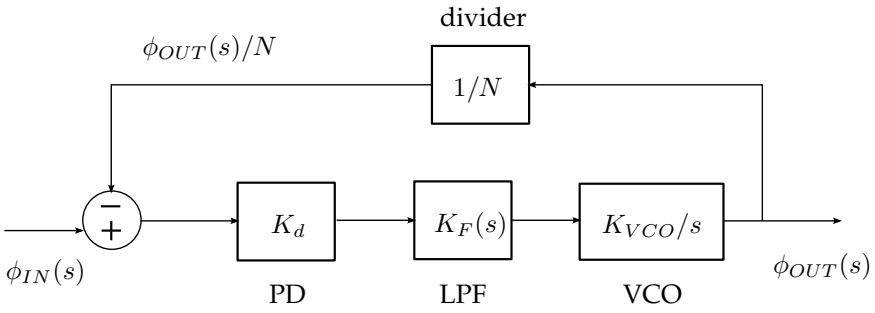


Figure 3.3: Mathematical model for the locked state of the PLL.

3.2 Linear model of the PLL

Phase-locked systems exhibit nonlinear behavior at least during part of their operation (e.g. transients), thus requiring time-domain analysis in almost all applications. However, in the steady state and during slow transients, it's extremely helpful to study its response in the frequency domain as well. This is especially true if the application imposes certain constraints on the output spectrum. In this work, frequency analysis has been considered sufficient to provide guidelines for the design of a SSCG.

So, if we assume that the PLL has locked and stays locked for the near future, we can develop a *linear* mathematical model for the system [31] in the Laplace domain, which is used to calculate a frequency-transfer function $H(s)$ that relates the frequency of the input signal to the frequency of the output signal (fig. 3.3).

To get an expression for $H(s)$ we must know the transfer functions of the individual building blocks.

In the following, analysis will limit to the case of interest of a *mixed-signal* PLL, i.e. composed of both analog and digital circuits, which deals with clock signals, thus *square-waves*. The PD, shown in fig. 3.4, is of the type that delivers a current output instead of a voltage output: it is said to have a *charge pump (CP)* output. The loop filter considered, shown in fig 3.5, is a passive second-order filter.

Let us proceed then, to derive the transfer function of the system.

- From fig. 3.4, PD and CP can be modeled as a single component, which senses the phase difference $\Delta\phi$ between the two inputs of the PD, and outputs a series of high frequency pulses of intensity $\pm I_{\text{pump}}$ and duty-cycle proportional to $\Delta\phi$; a phase difference of $\Delta\phi = 2\pi$ results in an average output current $\hat{I} = I_{\text{pump}}$, while a phase difference of $\Delta\phi = -2\pi$

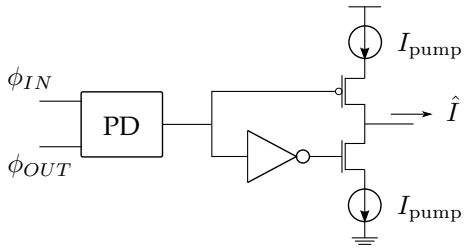


Figure 3.4: Phase detector with charge pump output.

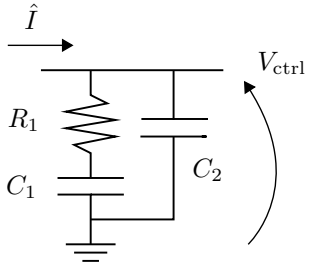


Figure 3.5: Second-order passive low-pass filter.

results in $\hat{I} = -I_{\text{pump}}$. Analytically:

$$\hat{I} = \frac{I_{\text{pump}}}{2\pi}\Delta\phi = K_d\Delta\phi$$

Obviously, the phase difference is bounded in the interval $[-2\pi, 2\pi]$.

- For proper operation, LPF cut-off frequency must be much lower (typically two or more order of magnitude) than the frequency of the pulses coming from the CP (i.e. the input frequency); as a consequence, one can consider that at the input of the filter only the average value of $\hat{I}$ is present, that is:

  $$\hat{I}(s) = K_d\Delta\phi(s)$$

  Referring to Figure 3.5, the filter output voltage is:

  $$V_{\text{ctrl}}(s) = \frac{1+sT_2}{sT_1(1+sT_3)}\hat{I}(s) = K_F(s)\hat{I}(s)$$

  where

  $$\begin{aligned} T_1 &= \text{C1} + \text{C2} \\ T_2 &= \text{R1}\,\text{C1} \\ T_3 &= \text{R1}\,\frac{\text{C1}\,\text{C2}}{\text{C1}+\text{C2}} \end{aligned}$$

- The VCO in turn converts this voltage into an output angular frequency:

  $$\omega_{\text{OUT}}(s) = K_{\text{VCO}}V_{\text{ctrl}}(s)$$

Observing that the phase $\phi(t)$ of a signal is just the integral of the instantaneous frequency $\omega(t)$ in time domain, it holds:

$$\phi_{\mathrm{OUT}}(s) = \frac{\omega_{\mathrm{OUT}}(s)}{s} = \frac{K_{\mathrm{VCO}}}{s} V_{\mathrm{ctrl}}(s)$$

- If we now consider the *open-loop transfer function* $H_0(s)$, from $\Delta\phi$ to ϕ_{OUT}, we get:

$$H_0(s) = \frac{\phi_{OUT}(s)}{\Delta\phi(s)} = K_d K_F(s) \frac{K_{VCO}}{s} = \frac{I_{\mathrm{pump}}}{2\pi} \frac{1+sT_2}{sT_1(1+sT_3)} \frac{K_{\mathrm{VCO}}}{s}$$

Observing that $\Delta\phi = \phi_{IN} - \phi_{OUT}/N$, N being the divider ratio, the correspondent *closed-loop transfer function* from ω_{IN} to ω_{OUT} is:

$$H_1(s) = \frac{\omega_{\mathrm{OUT}}(s)}{\omega_{\mathrm{IN}}(s)} = \frac{\phi_{\mathrm{OUT}}(s)}{\phi_{\mathrm{IN}}(s)} = \frac{H_0(s)}{1 + \frac{H_0(s)}{N}} \tag{3.1}$$

- It is very common to consider $\mathrm{C2} \ll \mathrm{C1}$, thus $T_3 \simeq 0$ and

$$K_F(s) \approx \frac{1+sT_2}{sT_1}$$

Under this assumption, equation (3.1) can be recast as

$$H_1(s) = N \frac{\omega_n^2(1+sT_2)}{s^2 + 2\omega_n\zeta s + \omega_n^2} \tag{3.2}$$

with

$$\omega_n = \sqrt{\frac{I_{\mathrm{pump}} K_{VCO}}{2\pi N T_1}}$$
$$\zeta = \frac{\omega_n T_2}{2}$$

which is the standard form used in control theory [32] for a two poles transfer function, where ω_n is the natural frequency and ζ the dumping factor.

$H_1(s)$ presents a double pole in ω_n and a zero in $1/T_2$. For proper values of its parameters, the system is designed to be *stable* [31] and exhibits a low-pass behavior, with cut-off frequency ω_n and base-band gain N, as expected. This means that the second-order PLL is able to track for phase and frequency variations of the reference signal, as long as this variations remain within an angular frequency band roughly between zero and ω_n. Equivalently, it is able to track for variations of the output signal, in case the reference signal is kept constant.

The time the PLL takes to track for a slow variation is defined as *lock-in* time, and can be in general calculated as: $T_L \simeq 2\pi/\omega_n$.

3.3 Frequency Modulator based on the PLL

The PLL-based SSCGs that appear in Literature can be roughly divided into three categories: those which directly add a signal at the input of the VCO [33][34], those which varies the divider ratio N [35][36][37][38], and those which combine the multi-phase outputs of the clock source and the special digital processing circuits to achieve the spread spectrum function [39][40][41]. Among these different techniques, in the following we will focus on the first two cases:

1. modulation obtained by adding a signal to the input of the VCO;
2. modulation obtained by varying the divider ratio N.

3.3.1 Modulated signal added at the input of the VCO

Let us indicate with $\xi(t)$ a driving signal added at the input of the VCO, and with $\xi(s)$ its Laplace transform. The VCO converts the sum of this driving signal and $V_{\mathrm{ctrl}}(s)$ into an output angular frequency:

$$\omega_{\mathrm{OUT}}(s) = K_{\mathrm{VCO}}\left(V_{\mathrm{ctrl}}(s) + \xi(s)\right)$$

and it follows:

$$\phi_{\mathrm{OUT}}(s) = \frac{\omega_{\mathrm{OUT}}(s)}{s} = \frac{K_{\mathrm{VCO}}}{s}\left(V_{\mathrm{ctrl}}(s) + \xi(s)\right)$$

For the *closed-loop transfer function* between $\omega_{\mathrm{OUT}}(s)$ and $\xi(s)$, one gets:

$$H_2(s) = \frac{\omega_{\mathrm{OUT}}(s)}{\xi(s)} = \frac{1}{s}\frac{\phi_{\mathrm{OUT}}(s)}{\xi(s)} = s\frac{1}{1+\dfrac{H_0(s)}{N}}\frac{K_{\mathrm{VCO}}}{s}$$

thus, similarly to what observed for equation 3.1:

$$H_2(s) = \frac{s^2/\omega_n^2}{s^2 + 2\omega_n\zeta s + \omega_n^2}$$

This transfer function presents a double zero in the origin, and a double pole at ω_n; this is a high-pass transfer function, with cut-off frequency equal to ω_n: it is indeed the transfer function "seen" from the driving signal at the input of the VCO.
Let us consider two significant cases.

1. If the (angular) frequency of the driving signal $\xi(t)$ is much lower than the cut-off frequency of the PLL, that is:

$$2\pi f_m \ll \omega_n$$

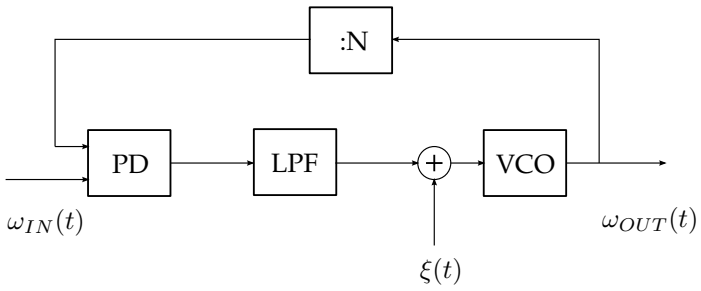


Figure 3.6: PLL-based SSCG with fast modulation.

then the PLL loop is able to *track* this $\xi(t)$, thus minimizing phase and frequency errors between this signal and the reference clock. This case is very similar to the one of clock generator without any modulation, wherein some low-frequency jitter is introduced by the VCO and the PLL loop takes charge of reducing it to a minimum. To conclude, under this condition, no modulation is performed.

2. On the contrary, if the (angular) frequency of the driving signal $\xi(t)$ is much higher than the cut-off frequency of the PLL, that is:

$$2\pi f_m \gg \omega_n$$

then $\xi(t)$ cannot be *tracked* by the PLL loop, due to the low-pass nature of the loop. The high-frequency "perturbation" $\xi(t)$, in fact, enters the PD, where it is compared with the low-frequency reference, thus originating a high-frequency error, which does not pass through the filter. As a consequence, as in an open-loop system, the modulating signal ends up driving the VCO *directly*, leaving to the feedback loop the mere function of tracking the *average* output frequency, thus setting the center-spread frequency equal to N times the input reference clock.

In time-domain, it means that the PLL lock-in time T_L is much longer than the period T_m of $\xi(t)$: then, every time $\xi(t)$ varies, the PLL starts the process of tracking, but it is not able to finish it before a new variation occurs. To conclude, under this condition, a *fast* modulation is performed, as defined in chapter 2.

From both these considerations, a SSCG with fast modulation, using the scheme shown in fig.3.6, has been implemented; its output frequency can be expressed as $\omega_{OUT}(t) = N\omega_{IN}(t) + K_{VCO}\xi(s)$. Circuital description, along with simulations and post-fabrication measurements of the SSCG can be found in chapter 4.

3.3.2 Modulated signal driving the input of the programmable divider

Consider now the case of a driving signal which acts on the value of the divider ratio N, at a rate f_m. Let us indicate with $N(t)$ the varying divider ratio and with $N(s)$ its Laplace transform. The *closed-loop transfer function* between $\omega_{\mathrm{OUT}}(s)$ and $N(s)$ can be calculated from equation 3.2 as:

$$H_3(s) = \frac{\omega_{\mathrm{OUT}}(s)}{N(s)} = \omega_{\mathrm{IN}}(s) \frac{\omega_n^2 (1 + sT_2)}{s^2 + 2\omega_n \zeta s + \omega_n^2}$$

$H_3(s)$ is the product of two terms of which:

- the first one can be simply considered as the Laplace transform of the frequency of a constant frequency square-wave, (the one given by the reference clock), that is equal to a constant value.
- the second one is the same as in $H_1(s)$, thus mainly characterized by a low-pass nature with a double pole in ω_n.

It follows that $H_3(s)$, similarly to $H_1(s)$, is a transfer function with a low-pass nature, with a cut-off frequency equal to ω_n.
Again, two significant cases will be considered.

1. If the (angular) frequency of the driving signal $\xi(t)$ is much lower than the cut-off frequency of the PLL, that is:

   $$2\pi f_m \ll \omega_n$$

   then the PLL loop can *track* the varying value of the divider ratio. Then, since the period of change T_m of N results much longer than the lock-in time, every time the value of N is changed, the output frequency in turn switches to a different value in a negligible time. To conclude, under this condition, a *slow* modulation is performed, as defined in chapter 2.

2. On the contrary, if the (angular) frequency of the driving signal $\xi(t)$ is much higher than the cut-off frequency of the PLL, that is:

   $$2\pi f_m \gg \omega_n$$

   then $\xi(t)$ cannot be *tracked* by the PLL loop, due to the low-pass nature of the loop. As a consequence, the feedback loop can only track the *average* division ratio.

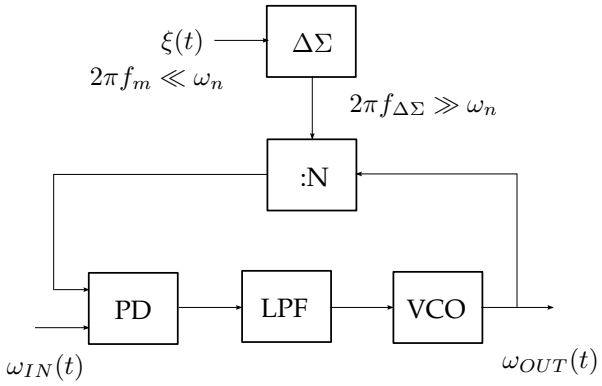


Figure 3.7: PLL-based SSCG with slow modulation.

From both these considerations, a SSCG with slow modulation, using the scheme shown in fig. 3.7, has been implemented. Its circuital description, along with simulations and post-fabrication measurements can be found in chapter 5; in the following the principles of its operation will be discussed. As indicated in fig. 3.7, the frequency f_m of the modulating signal $\xi(t)$ is such that $2\pi f_m \ll \omega_n$: consequently, the performed modulation is *slow*. One can notice, though, that $\xi(t)$ does not drive directly the divider ratio N: it drives instead the input of a $\Delta\Sigma$ converter. The $\Delta\Sigma$ circuit is an over-sampling A/D converter that transforms each analog value at its input in a sequence of "1s" and "0s"; the length of such a sequence depends on the $\Delta\Sigma$ Over-Sampling Ratio (OSR), that is:

$$\text{OSR} = \frac{f_{\Delta\Sigma}}{f_m}$$

If this OSR is sufficiently high, i.e. if the sequence of "1s" and "0s" in turn drives the division ratio N with a frequency $f_{\Delta\Sigma}$ such that $2\pi f_{\Delta\Sigma} \gg \omega_n$, then the feedback loop can only track the *average* division ratio.

The SSCG shown in fig. 3.7 is said to implement a (slow) modulation that is based on "fractional synthesis" [31]: the divider can provide only two possible ratios, N_{min} and N_{max}, but the whole range of frequency within $\omega_{OUT} = N_{min}\omega_{IN}$ and $\omega_{OUT} = N_{max}\omega_{IN}$ can be generated by inputting into the divider a sequence which originates a proper *average* value for N. Let us explain this mechanism through some examples; the values for N_{min} and N_{max} will be set to 199 and 200, respectively.

Imagine to input the periodic sequence of bits "10101010..." to the programming input of the divider, and say input "1" corresponds to $N = 200$, and input "0" corresponds to $N = 199$. Let us assume as well that the initial value for the output frequency is $\omega_{\text{OUT}} = 199\omega_{\text{IN}}$. Then, at the occurrence of

the first "'1", the feedback loop starts the process of tracking, trying to adapt the output frequency to the value $\omega_{\mathrm{OUT}} = 200\omega_{\mathrm{IN}}$; before it is able to finish it, though, a "0" occurs, thus setting N back to 199. Again the feedback loop tries to adapt the output frequency to $\omega_{\mathrm{OUT}} = 199\omega_{\mathrm{IN}}$, but it cannot get to this value because interrupted by a further variation. It is easy to conclude that the mentioned sequence of bits at the input of the divider will originate an actual output frequency of

$$\omega_{\mathrm{OUT}} = \frac{N_{min} + N_{max}}{2}\omega_{\mathrm{IN}} = \frac{200 + 199}{2}\omega_{\mathrm{IN}} = 199.5\omega_{\mathrm{IN}}$$

This concept can be extended to get any other value of N within the interval $[N_{min}, N_{max}]$, by simply inputting a different sequence of bits into the divider, which corresponds to a sequence of division ratios whose average value is the one desired. For instance, the periodic sequence "100100100..." will result in a division ratio of

$$N = \frac{200 + 199 + 199}{3} = 199.333$$

More in general, for *any* sequence, even *non-periodic*, the actual value of N depends:

- in first approximation, on the ratio between occurrences of "1s" and occurrences of "0s", i.e. the value of N is the weighted sum of "1s" and "0s" occurring in the sequence. For instance, the sequence with period "11000" and the one with period "01010" give rise to the same average value of N;
- due to the low-pass nature of the system, though, also on the *position* of the bits in the sequence: the higher the rate of switch from a value to a different one, the best the value of N is *averaged* by the loop; thus, the example sequence with period "01010" gives better results than the one with period "11000".

3.4 Conclusion

PLLs-based frequency modulation have been analyzed, and significant guidelines have been derived and used to implement two different types of SSCGs. In chapter 4, two prototypes of SSCG with *fast* modulation, whereas in chapter 5 one prototype of SSCG with *slow* modulation, will be presented.

Chapter 4

Hardware implementation of a SSCG with fast modulation

IN THIS CHAPTER two prototypes of Spread-Spectrum Clock Generators (SSCGs), designed to implement a *fast* binary modulation are described. For both prototypes:

- the modulation parameters have been chosen so that the modulation index m is equal to its optimum value $m = 0.318$: this means that a *flat* shape for the first harmonic of the clock is expected (see chapter 2);
- the modulating signal is a PAM random signal, as expected by random modulation (see chapter 2), whose time-symbol is T_m.
- the modulator is based on a standard Phase-Locked Loop (PLL), wherein the modulation is obtained by adding a signal to the input of the VCO; (see chapter 3);

In both implementations, the symbols of the modulating signal comes from the output of an embedded ADC-based Random Number Generator. This circuit is based on a *chaotic map*, whose implementation has been part of another PhD work; a brief description of its working principles and hardware realization can be found in Appendix A. Remember that fast modulation requires a PAM driving signal with i.i.d. binary values, which can be obtained by the quantization of the output of a chaotic map (chapter 2).

Furthermore, since the power density spectrum of a PAM signal is composed of adjacent lobes, the first of which ranging from 0 to f_m, it can be intuitively accepted that the consideration derived in chapter 3 about the conditions to obtain a fast or a slow modulation can be extended to this case. For this

Center-Spread Frequency, f_0	100 MHz
Spread-Spectrum Modulation frequency, f_m	10 Mbit/s
Spread-Spectrum Modulation Deviation ,Δf	3.18 MHz

Table 4.1: Specifications of 0.35 μm SSCG.

reason, in the following we will continue to refer to $f_m = 1/T_m$ as the *frequency* of the modulating signal.

4.1 Description of the 0.35 μm SSCG prototype

The first SSCG prototype here described has been designed in an established technology, to perform at low frequency: these characteristics have been considered suitable for getting a first practical proof of the theoretical results discussed in chapter 2.

- The technology is 0.35 μm C35B3C1. Provided by Austria Micro System (AMS) AG, it is a n-well CMOS technology with a minimum MOS width of 0.35 μm and a minimum resolution of 0.05 μm. Also a double poly-silicon layer is provided (with a poly-poly capacitor module and a high resistive poly-silicon module) as well as three levels of metallization. A power supply voltage of 3.3 V is required.

- The mean working frequency is $f_0 = 100$ MHz.

The modulation parameters are summarized in table 4.1. It is worth noticing that the value of frequency deviation Δf in table 4.1 corresponds to about 3% f_0, which is a standard value for frequency deviation of a clock.

From table 4.1 one gets for the modulation index:

$$m = \frac{\Delta f}{f_m} = 0.318$$

that is exactly the optimum value derived in chapter 2.

4.1.1 Implementation of the PLL

The block diagram of the PLL-based modulator is shown in fig. 4.1. It is composed of a phase-frequency detector (PFD) with a charge pump (CP), a second-order passive low-pass filter (LPF), a voltage-controlled oscillator (VCO) and a divider by N on the feedback path.

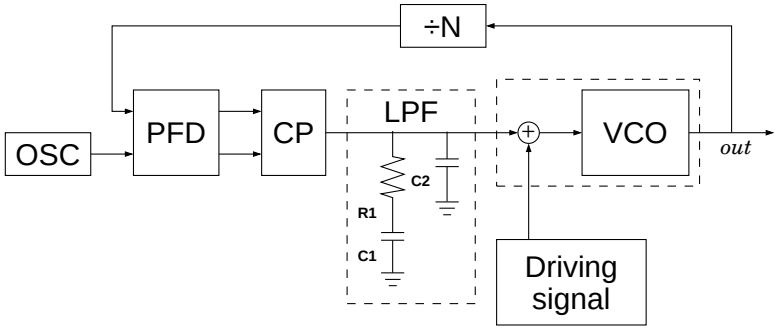


Figure 4.1: Block diagram of the PLL modified to achieve a frequency modulator.

In this scheme, a *phase-frequency* detector (PFD) has been used in place of a simple *phase* detector (PD) as in chapter 3. The PFD is a circuit whose output depends on phase error in the locked state of the PLL, and also on frequency error in the unlocked state [31], which guarantees that a PLL using a PFD will lock under any condition. Its schematic, taken from [42], is shown in fig. 4.2. Dynamic logic gates are used instead of conventional static logic circuitry: as a result, the number of transistors is reduced, which reflects in a shortened feedback path delay, thus increasing circuit precision. The PFD asserts two outputs, here named UP and DOWN: if there is a phase difference between EXT_CLK and VCO_CLK, the width of UP and DOWN pulse will be proportional to the phase difference of the inputs.

The aim of the CP, whose schematic is shown in fig. 4.3, is to convert the UP and DOWN signals into one current signal:

$$I_{\text{out}} = \begin{cases} I_{\text{pump}} & \text{UP} = 1 \\ 0 & \text{UP} = 0, \text{DOWN} = 0 \\ -I_{\text{pump}} & \text{DOWN} = 1 \end{cases}$$

Although the value of I_{pump} is not explicitly indicated in fig. 4.3, it is set through I_{ref} and the ratio between the form factors of the current mirror branches. I_{out} is then filtered by the second-order LPF, which re-converts it into a voltage signal and generates the control voltage V_{ctrl} needed by the VCO.

In the project design, it has been set $I_{\text{pump}} = 400\mu A$ and $N = 64$. To ensure stability, the (external) filter has been designed with:

$$C_1 = 58 \text{ nF}$$
$$C_2 = 5.8 \text{ nF}$$
$$R_1 = 370\ \Omega$$

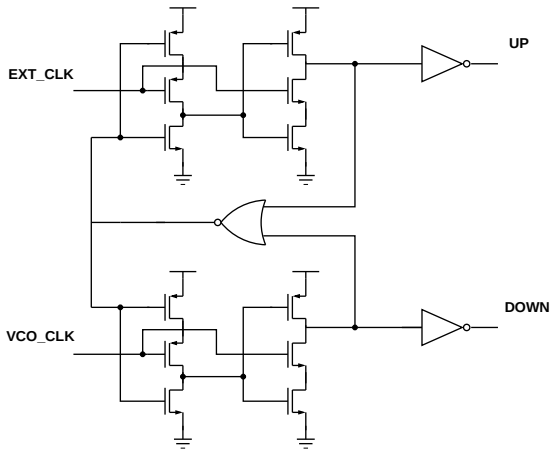


Figure 4.2: Phase Frequency Detector.

The resulting closed-loop PLL bandwidth and dumping factor are equal to:

$$\omega_n = \sqrt{\frac{I_{\text{pump}} K_{\text{VCO}}}{2\pi N C_1}} = 94.25\text{krad/s}$$
$$\zeta \simeq 1$$

thus meaning a cut-off frequency of about 15 KHz, while the zero of $H_1(s)$ is at $1/T_2 = 46.6\text{krad/s}$, i.e. 7.4 KHz. Also, the PLL lock-in time can be estimated as $T_L = 2\pi/\omega_n \simeq 66\ \mu s$.

Figure 4.4 shows a simulation of the VCO control voltage during the pull-in process (that is the process to enter the *locked* state, [31]) for the PLL without any driving signal. It is possible to notice that the PLL eventually reaches stability; also the time between entering the locked state (i.e. when major oscillations end) and reaching a complete settlement, is almost equal to the estimated lock-in time T_L.

4.1.2 Implementation of the modulation

The core block of the PLL is the VCO, whose base-design shown in fig. 4.5 (a) is taken from [33]. It is essentially composed of a seven-stage ring oscillator (c), which is followed by a wave-shaping buffer (d), in order to obtain proper values of logic levels and slew-rate for the output, and is controlled by an input stage (b), whose purpose is mainly to supply the correct operating current to the ring oscillator, and to decouple it from the other parts of the circuit.

As already mentioned, the modulation is obtained by adding a signal to the input of the VCO. Due to the discrete (i.e. binary, then digital) nature of

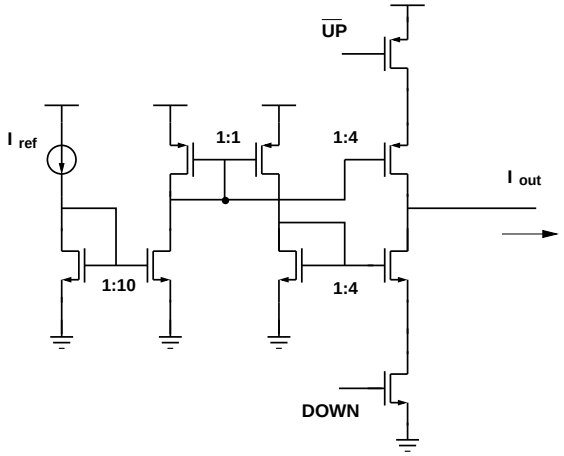


Figure 4.3: Charge Pump.

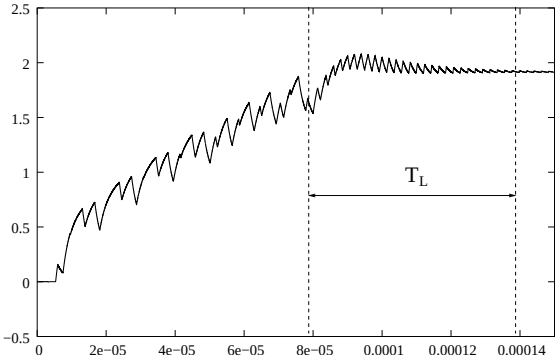


Figure 4.4: Simulation of the *pull-in* and *lock-in* process of the PLL.

the modulating signal, no full analog adders have been realized: the additive function is instead performed by the input stage of the VCO. Figure 4.5 (b) shows how this is obtained through the two pass-transistors driven by Φ_1 and Φ_2, along with the two current sources I_{bias}. This circuit is designed to work with $\Phi_1 = \overline{\Phi_2} = \Phi$, where Φ is the digital representation of the modulating signal $\xi(t)$, which comes from the random number generator. However its behavior is more evident considering Φ_1 and Φ_2 separately. Supposing $\Phi_1 = \Phi_2 = 0$, the circuit acts as a linear voltage amplifier, where V_{ddL} is proportional to V_{ctrl}; the obtained VCO $f_{\mathrm{OUT}}/V_{\mathrm{ctrl}}$ characteristic is represented by the solid line in fig 4.6; the voltage/frequency ratio is set to:

$$K_{\mathrm{VCO}} = 518\mathrm{Mrad/s/V}$$

corresponding to $K_{\mathrm{VCO}} = 82.5\mathrm{MHz/V}$. When $\Phi_1 = 1$, the current I_{bias} is subtracted from the current mirror, thus shifting up the $f_{\mathrm{OUT}}/V_{\mathrm{ctrl}}$ characteristic.

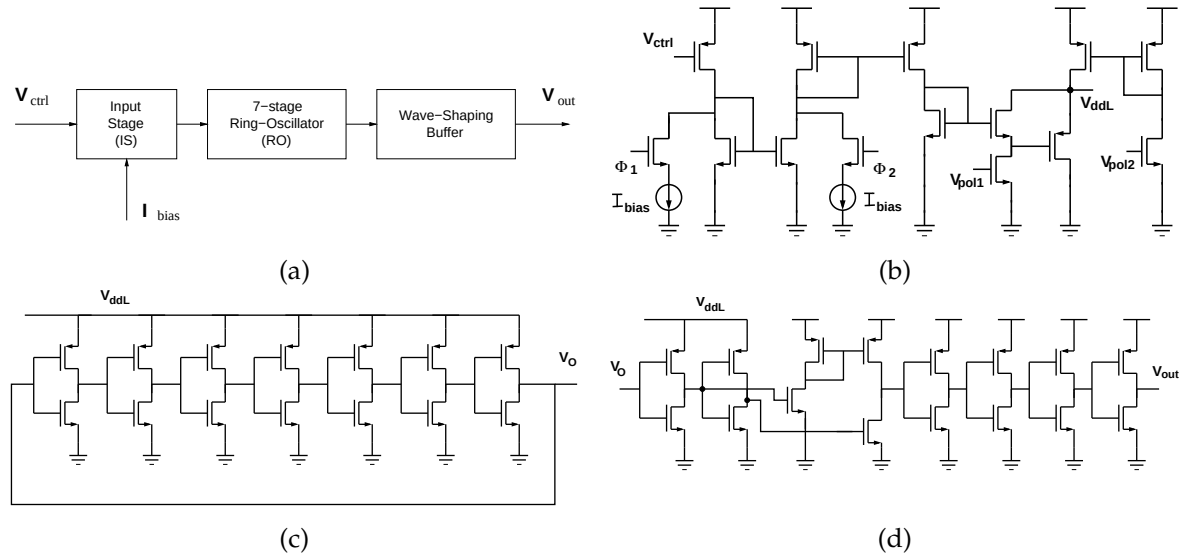


Figure 4.5: (a) Block diagram of the VCO. (b) Modified Input Stage. (c) Ring-Oscillator. (d) Wave-shaping Buffer.

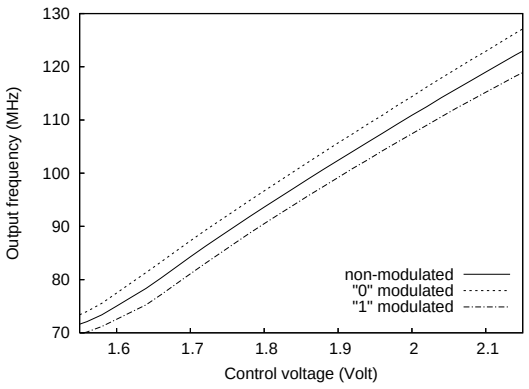
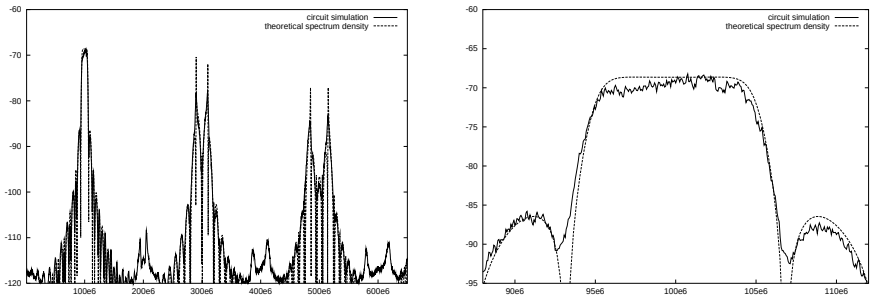


Figure 4.6: Voltage/Frequency characteristic of the VCO in non spread spectrum mode (solid line) and spread spectrum mode (dashed lines).

On the contrary, $\Phi_2 = 1$ adds $I_{\rm bias}$ to the current mirror and shifts down the characteristic. The two shifted characteristics are represented by dashed lines in fig. 4.6. The distance between the curves is approximately constant in the range of interest and represents the PLL Δf. Its value depends on $I_{\rm bias}$; furthermore there is an almost linear relationship between Δf and $I_{\rm bias}$, that is:

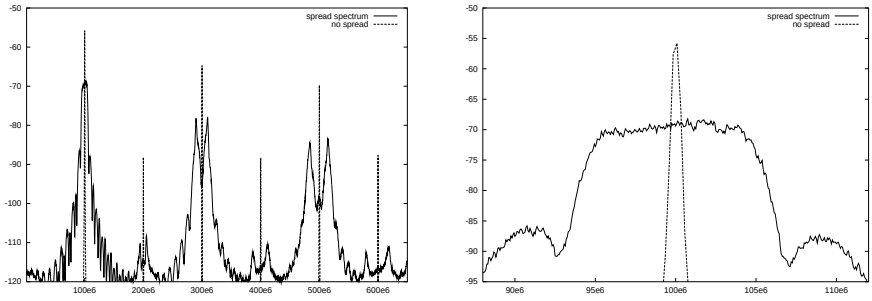
$$K_{\Delta f} = 1.106\,\mathrm{Mrad/s/\mu A}$$

corresponding to $K_{\Delta f} = 0.176\,\mathrm{MHz/\mu A}$.



(a) (b)

Figure 4.7: Comparison between power spectrum density of the output clock obtained from the simulated circuit and the theoretical power spectrum density of the binary modulation, for (a) a wide set of harmonics; and (b) only for the fundamental tone.



(a) (b)

Figure 4.8: Comparison between power spectra density of the modulated and non modulated output clock for (a) a wide set of harmonics; and (b) only for the fundamental tone.

4.1.3 Simulation results and post-fabrication measurements

The simulated power spectrum density of the output clock signal can be seen in fig. 4.7 (a) and (b). The figures have been obtained from a 1.2 ms simulations and discarding the first 200 μs data, which is a sufficient time, according to PLL bandwidth, to consider extinguished all circuit transients . The simulated spectrum is also compared with the theoretical one from chapter 2. As can be seen, the simulated spectrum is very close to the theoretical one.

Figures 4.8 (a) and (b) show a comparison between the simulated power spectrum density of the output clock signal and the same spectrum obtained from the circuit without any driving signal, i.e. working as a standard PLL-based clock generator. The resolution bandwidth is set to 120 kHz, as indicated by CISPR regulations [43] [44]. The comparison shows a peak reduction on the fundamental tone of about 13 dB.

All the simulation results are confirmed by measurements on the proto-

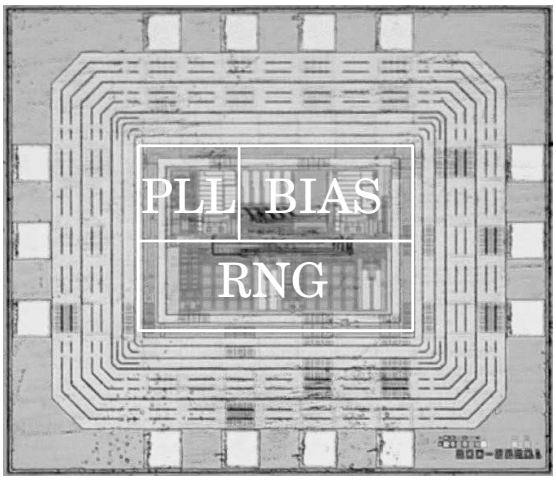


Figure 4.9: Microphotograph of the 0.35 μm SSCG prototype.

Output frequency	100 MHz
Modulation type	Binary Random
Modulation frequency	10 MHz
Frequency Deviation	3.18 MHz
Lock-range	63–108 MHz
Chip area	1.38×1.20mm^2
Power consumption	20.5mW
Closed loop Bandwidth	15 KHz $C_1 = 58$nF, $C_2 = 5.8$nF $R_1 = 370\Omega$

Table 4.2: Performance summary of the 0.35 μm SSCG prototype

type. The chip microphotograph is shown in fig. 4.9, while table 4.2 gives a performance summary of the integrated SSCG. The active area occupies 0.38×0.65 mm^2 and the total area including pads is 1.38×1.20 mm^2. The low-pass filter is off-chip. Figure 4.10 shows the measured spectrum of the 100 MHz output signal without any modulation (a) and modulated with the optimum index value $m = 0.318$ (b). The measured peak reduction is about 18 dB. Figure 4.11 shows the comparison between the spectrum from fig. 4.10 (a) and the theoretical one; the matching is very good, confirming the effectiveness of the proposed circuital approach.

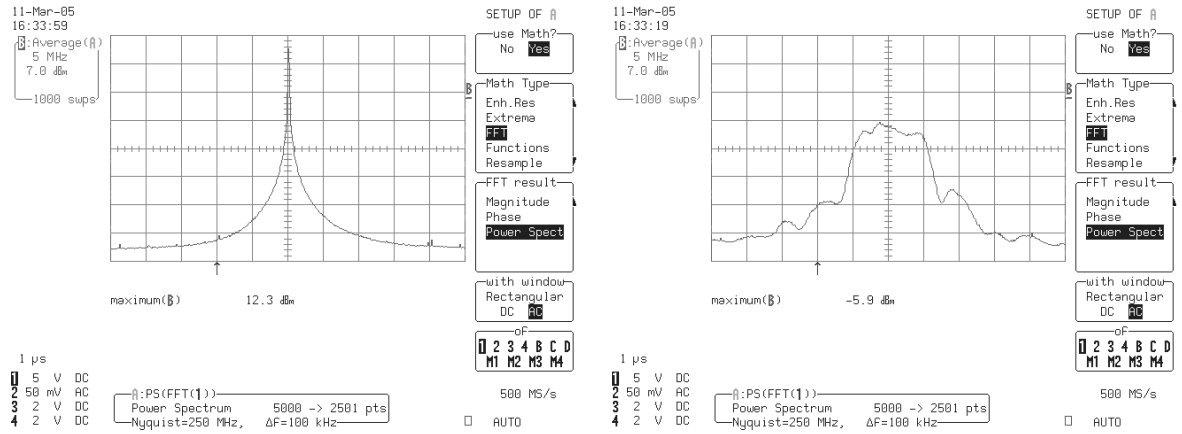


Figure 4.10: (a) Measurements from the prototype in non spread spectrum mode; and (b) in spread spectrum mode.

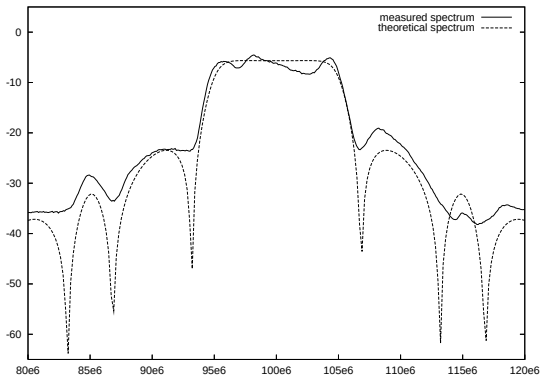


Figure 4.11: Comparison between the measured spectrum of Figure 5.17(b) and the theoretical one.

4.2 Description of the 180 nm SSCG prototype

The second SSCG prototype here described has been scaled in technology, to perform at high frequency: the parameters of the modulation, such as center frequency and frequency deviation, have been suggested by Serial Advanced Technology Attachment (SATA) protocol [23]. This standard, though, requires that the performed modulation applied to its synchronization signal is of *slow* type. For this reason, this implementation does not aim at being suitable for the standard, but only at proving the benefits of fast modulation at high frequency.

The technology used is UMC 180 nm: a standard n-well CMOS technology, optimized for digital applications. It has a single poly-silicon layer, up to six metal layers, and a metal/metal capacitor options between the two top metal layers. The core power supply voltage is reduced to 1.8 volts, but 3.3 volts

Center-Spread Frequency, f_0	3 GHz
Spread-Spectrum Modulation frequency, f_m	47.17 Mbit/s
Spread-Spectrum Modulation Deviation, Δf	15 MHz

Table 4.3: Specifications of 180 nm SSCG.

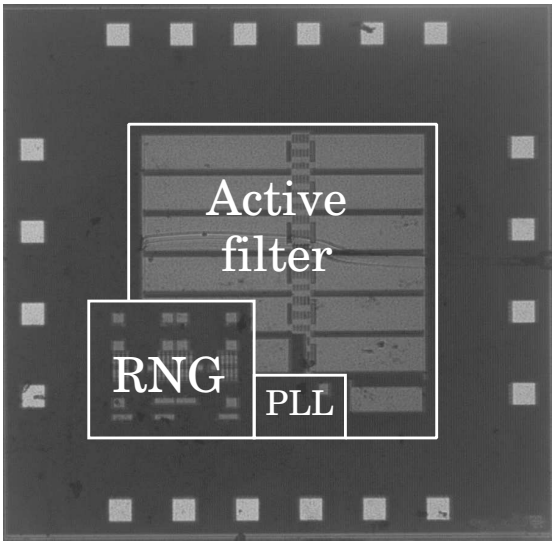


Figure 4.12: Microphotograph of the 180 nm SSCG prototype.

transistors are available as I/O devices.

The modulation parameters are summarized in table 4.3. From the table, one gets for the modulation index:

$$m = \frac{\Delta f}{f_m} = 0.318$$

that is exactly the optimum value derived in chapter 2.

Hardware implementation of the PLL as well of the modulation function is the same as in section 4.1, and will not be described in the following.

4.2.1 Simulation results and post-fabrication measurements

The microphotograph of the circuit is shown in fig.4.12. The unmodulated and modulated $f_{\mathrm{OUT}}/V_{\mathrm{ctrl}}$ characteristics of the VCO for this implementation are represented in fig. 4.13; the voltage/frequency ratio is set to:

$$K_{\mathrm{VCO}} = 248\,\mathrm{MHz/V}.$$

The power density spectrum (PDS) of the output clock signal can be observed in fig.4.14 (a), where simulated and theoretical spectra are also com-

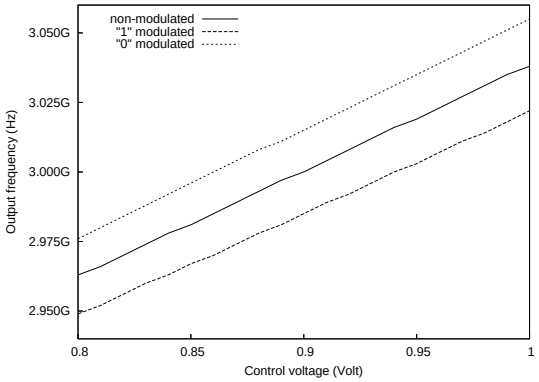
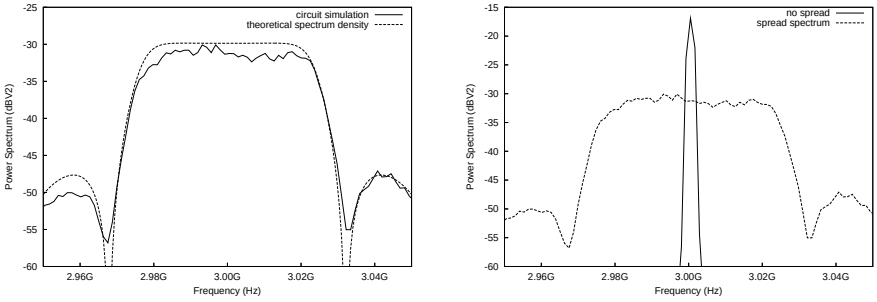


Figure 4.13: Voltage/Frequency characteristic of the VCO in non spread spectrum mode (solid line) and spread spectrum mode (dashed lines).

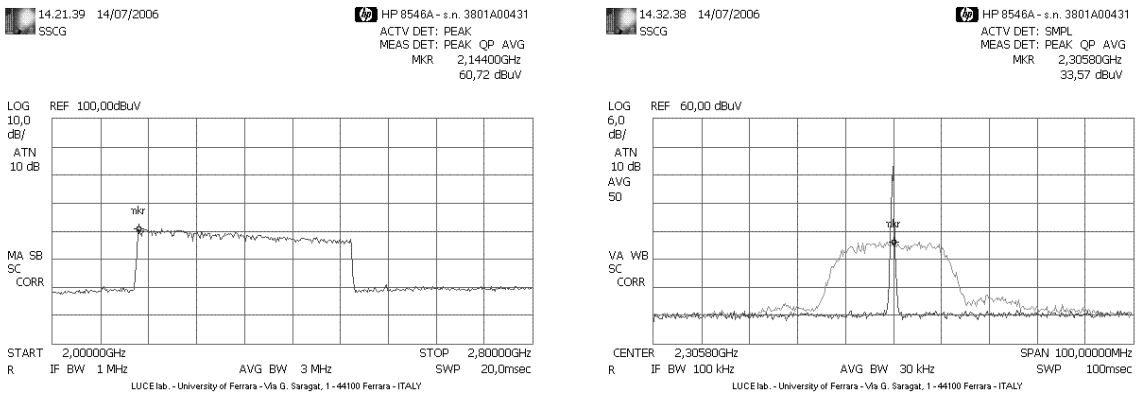


(a) (b)

Figure 4.14: (a) Comparison between power spectrum density of the output clock obtained from the simulated circuit and the theoretical power spectrum density of the binary modulation; and (b) comparison between power spectra density of the modulated and non modulated output clock. The spectra are measured in dBV^2, with RBW = 120KHz.

pared. As in the previous prototype, simulation results support the theoretical ones. Figure 4.14 (b) shows a comparison between the simulated PDS of the output clock signal in case it is unmodulated and in case it is modulated. The resolution bandwidth is set to 120 kHz, as indicated by CISPR regulations [43][44]. The comparison shows a peak reduction on the fundamental tone of about 13 dB.

Regrettably, measurements indicate that the circuit works in a range of frequencies that is sensibly lower than expected. In fact, the lock range of the PLL, in fig. 4.15 (a), goes from 2.2 GHz to 2.5 GHz, that is far from the 3 GHz expected. This is probably due to a design-time underestimation of the the parasitic effects in the VCO. However, as can be noticed in fig. 4.15 (b), the binary modulation is properly applied, and the frequency spectrum is exactly the expected one. The peak reduction is measured in about 16 dB. A summary of the



(a) (b)

Figure 4.15: (a) Measured lock-range of the PLL; and (b) comparison between modulated and unmodulated power spectra.

Output nominal frequency	3000 MHz
Lock range *(designed)*	2700-3150 MHz
(measured)	2200-2500 MHz
Modulation type	Binary Random
Modulation frequency	47.17 MHz
Frequency Deviation	0.5%
Chip area	$1.48 \times 1.48\text{mm}^2$
(without pads)	$0.95 \times 0.95\text{mm}^2$
Power consumption	35.5mW
(PLL only)	13.5 mW
Closed loop Bandwidth	45 KHz

Table 4.4: Performance summary of the 180 nm SSCG prototype

prototype characteristics can be found in table 4.4.

4.3 Conclusion

In this chapter, the design of a SSCG aiming at reducing EMI is presented. Its architecture is based on a PLL, wherein the modulating signal is added at the input of the VCO. The spreading of the clock spectrum is achieved through a fast frequency modulation, whose modulating signal is a random binary PAM.

Two prototypes have been designed, the first one in CMOS 0.35 μm technology to operate at a clock of $f_0 = 100$ MHz, and the second one in CMOS 180 nm technology to operate at a frequency $f_0 = 3$ GHz. Both prototype perform

the requested modulation achieving the desired clock power spectrum; however for the 180 nm prototype a maximum working frequency lower than the expected one, and approximately equal to $f_0 = 2.5$ GHz, has been measured.

Chapter 5

A SSCG with slow modulation for application to Serial ATA-II

SERIAL ADVANCED TECHNOLOGY ATTACHMENT (SATA) is a computer bus technology designed in 2003 for fast data transmission to and from Hard Disk Drives, through a simple serial cable, in opposition to the previous ATA standard that relied on *parallel* data transmission. This technology concentrates all transmission-related problems into a single high–speed line, making the system simpler and more reliable. Recently this protocol has raised its clock rate to 3.0 GHz, with the release of SATA–II, in order to increase transmission speed. The drawback to higher transmission rate is an increase in EMI. To this regard, Serial ATA specifications suggest that a spread spectrum clock can conveniently be applied to perform an on-chip EMI reduction, without any need for heavy shielding materials, thus reducing the overall cost of the equipment.

Standard Specifications of Serial ATA [23] read, about spread-spectrum: "*Serial ATA allows the use of spread spectrum clocking (SSC), or intentional low frequency modulation of the transmitter clock. The purpose of this modulation is to spread the spectral energy to mitigate the unintentional interference to radio services. [...] The modulation frequency of SSC, as well as the modulation frequency deviation shall be in the prescribed ranges. [...] The SSC modulation only moves the frequency below the nominal frequency: this technique is often called down-spreading.*" The two ranges for modulation frequency and modulation frequency deviation are shown in table 5.1, along with channel speed. As stated in the specifications, modulation shall be *slow*. An example triangular frequency modulation profile is shown

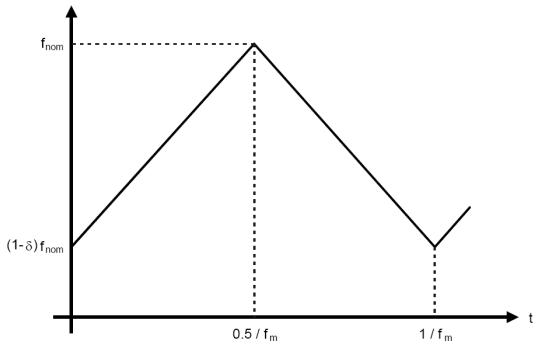


Figure 5.1: Serial ATA-II SSC profile example: Triangular

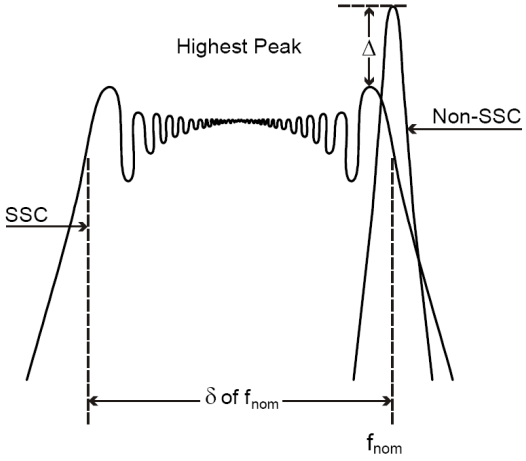


Figure 5.2: Serial ATA-II: Spectral fundamental frequency comparison, in case of Triangular profile.

in Figure 5.1, where f_{nom} is the nominal frequency in the *non Spread Spectrum Clock* mode, f_m is the modulation frequency, δ is the modulation amount, and t is time. As an example, for triangular modulation, the absolute spread amount at the fundamental frequency is shown in fig. 5.2, as the width of its spectral distribution.

Most of SSCGs proposed in Literature as suitable for SATA system employ periodic modulation profiles, in particular the *triangular* profile as in [37][38],

Channel Speed	1.5 or 3 GHz
Spread-Spectrum Modulation frequency	30 to 33 kHz
Spread-Spectrum Modulation Deviation	[-5000,+0] ppm

Table 5.1: Specifications of Serial ATA-II.

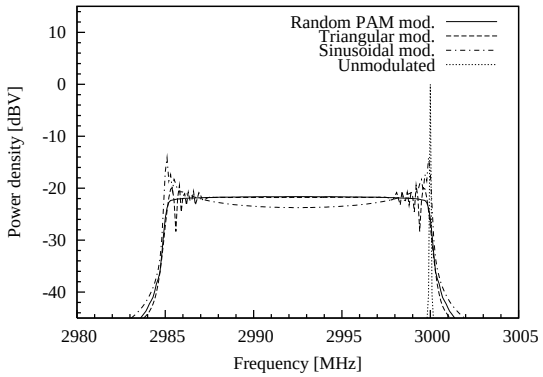


Figure 5.3: Comparison between different modulation profiles.

since it is considered the simplest to implement. Nevertheless, as already discussed in chapter 2, using a *random* modulation profile may be advantageous from the point of view of EMI reduction. Fig. 5.3 shows a comparison, in the frequency range of interest for SATA, between different modulation waveforms: as can be noticed, the *random* profile is the one offering the best results in terms of peak reduction. In this chapter a prototype of SSCG, designed to implement a *slow* random modulation for application to standard Serial ATA-II is described.

For this prototype:

- the modulator is based on a standard Phase-Locked Loop (PLL), wherein the modulation is obtained by driving the division ratio N of the divider; (see chapter 3);
- the modulating signal is a PAM random signal, as expected by random modulation (see chapter 2), whose time-symbol is T_m.

The symbols of the modulating signal comes from the output of an embedded ADC-based Random Number Generator. This circuit is based on a *chaotic map*, whose implementation has been part of another PhD work; a brief description of its working principles and hardware realization can be found in Appendix A. Remember that slow modulation requires a PAM driving signal with *uniformly* distributed continuous values, in order to shape *flat* the spread spectrum.

Furthermore, since the power density spectrum of a PAM signal is composed of adjacent lobes, the first of which ranging from 0 to f_m, it can be intuitively accepted that the consideration derived in chapter 3 about the conditions to obtain a fast or a slow modulation can be extended to this case. For

Center-Spread Frequency, f_0	3 GHz
Spread-Spectrum Modulation frequency, f_m	33 kbit/s
Spread-Spectrum Modulation Deviation	[-5000,+0] ppm

Table 5.2: Specifications of 0.13 μm SSCG.

this reason, in the following we will continue to refer to $f_m = 1/T_m$ as the frequency of the modulating signal.

5.1 Description of the SSCG prototype

This SSCG prototype has been implemented in UMC 130 nm technology, a standard n-well CMOS technology optimized for digital applications. It has a single poly-silicon layer, up to eight metal layers, and a metal/metal capacitor options between the two top metal layers. The core power supply voltage is 1.2 volts, but 3.3 volts transistors are available as I/O devices.

The modulation parameters have been set according to the values in table 5.1, and are summarized in table 5.2.

It is worth noticing that the value of frequency deviation in table 5.2 corresponds to 0.5% f_0, that is $\Delta f = 15$ Mhz. Observe that since the modulation, according to the specifics, only moves the frequency *below* the nominal frequency, the output frequency only spans from $f_0 - \Delta f$ to f_0. From table 5.2 one gets for the modulation index:

$$m = \frac{\Delta f}{f_m} \simeq 454$$

thus the modulation can actually be considered *slow*.

5.1.1 Implementation of the modulator

The block diagram of the SSCG is shown in fig. 5.4: its structure is based on a standard PLL, wherein the modulation is obtained by using a programmable integer divider in the feedback loop. The standard blocks of the PLL have already been described in chapter 4: the phase frequency detector (PFD), the charge pump (CP), and the 2-nd order low-pass filter (LPF). The programmable divider ratio N can here be set to the value 199 or 200; additionally, a $\Delta\Sigma$ converter is interposed between the RNG and the programming input of the divider, as anticipated in chapter 3.

Each value coming from the low-frequency RNG is *over-sampled* by the $\Delta\Sigma$ converter, thus transformed in a sequence of "1s" and "0s", whose length de-

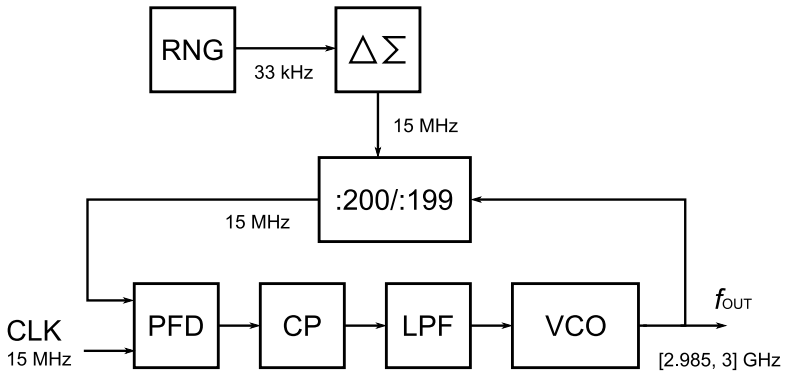


Figure 5.4: Block diagram of the SSCG.

pends on the $\Delta\Sigma$ Over-Sampling Ratio (OSR), that is:

$$\text{OSR} = \frac{f_{\Delta\Sigma}}{f_{\text{RNG}}} = \frac{15\text{MHz}}{33\text{kHz}} = 454$$

The output of the $\Delta\Sigma$ then drives the division ratio N with a frequency that is made higher than the PLL loop frequency, that is:

$$2\pi f_{\Delta\Sigma} \gg \omega_n$$

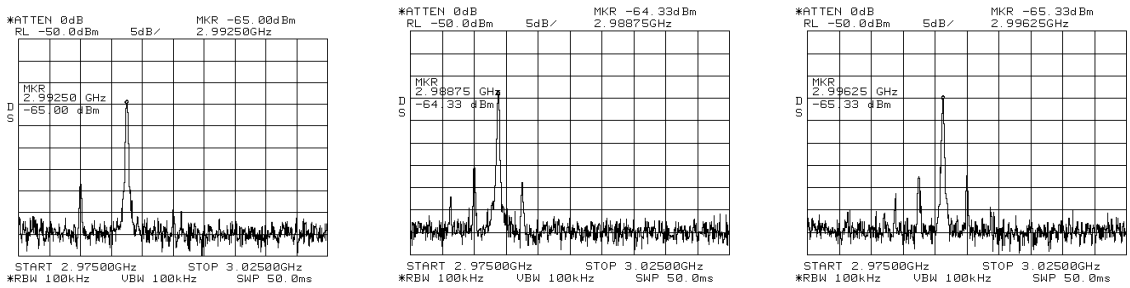
Consequently, for each input sequence, the divider will actually divide by 200 a number of times corresponding to the number of "1s" therein occurring, and by 199 the remaining number of times. This way, the actual ratio of division will be a value between 199 and 200, with a step correlated to the inverse of the OSR, that is $1/454$. Observing that f_{IN} is set to 15 MHz, it results for the output frequency:

$$\begin{aligned} f_{\text{OUT}_{\text{max}}} &= 3\text{GHz}, && \text{if } N = 200 \\ f_{\text{OUT}_{\text{min}}} &= 2.985\text{GHz}, && \text{if } N = 199 \end{aligned}$$

The actual output frequency then will span from $f_{\text{OUT}_{\text{min}}}$ to $f_{\text{OUT}_{\text{max}}}$ in a discrete way, that can be considered a *continuous* way from the point of view of slow modulation, due to the large value of OSR.

Actually, the values of $f_{\Delta\Sigma}$, f_{IN} and N have been chosen, in the design, according to the following reasoning:

- Δf is set to 15 MHz by the application;
- $f_{\Delta\Sigma}$ must be much greater than ω_n, then its value shall be as large as possible;
- the divider completes each counting at a rate equal to f_{OUT}/N: this value limits the upper bound of $f_{\Delta\Sigma}$, that must be chosen then $\leq f_{OUT}/N$;



(a) (b) (c)

Figure 5.5: Measured output frequency for three different values of N, in case no modulation is performed: $N = 199.5$ (a), $N = 199.25$ (b), $N = 199.75$ (c).

- as a consequence f_{IN}, which coincides with f_{OUT}/N, becomes the frequency to be maximized;
- it has been chosen to set $f_{IN} = \Delta f = 15$ MHz: this way, with an integer divider, $f_{OUT_{min}}$ and $f_{OUT_{max}}$ can be obtained with the two adjacent values $N = 199/200$;
- to maximize $f_{\Delta\Sigma}$, it has been set in turn equal to f_{OUT}/N, that is 15 MHz: this way, every count of the divider a new value from the $\Delta\Sigma$ is available at its input.

In chapter 3 it has been shown how for *any* sequence, even *non-periodic*, the actual value of N depends not only on the *ratio* between occurrences of "1s" and occurrences of "0s", but also on the *position* of the bits in the sequence: the higher the rate of switch from a value to a different one, the best the value of N is *averaged* by the loop. Fig. 5.5 shows the measured output frequency for three different values of N, in case no modulation is performed, but only the frequency multiplication. The values of N have been obtained by feeding the divider with an external sequence; respectively:

- a 7.5 MHz square-wave with duty-cycle=50% has originated a value of $N = 199.5$, with a corresponding $f_{OUT} = 2.9925$ GHz, as in fig. 5.5 (a);
- a 3.75 MHz square-wave with duty-cycle=25% has originated a value of $N = 199.25$, with a corresponding $f_{OUT} = 2.98875$ GHz, as in fig. 5.5 (b);
- a 3.75 MHz square-wave with duty-cycle=75% has originated a value of $N = 199.75$, with a corresponding $f_{OUT} = 2.99625$ GHz, as in fig. 5.5 (c).

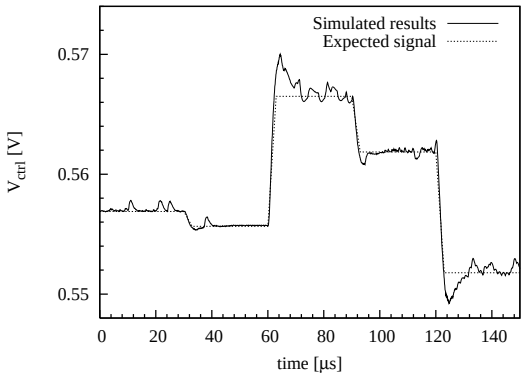


Figure 5.6: Output of the LPF.

LOAD=1	at the occurrence of clock edge, the input data is loaded.
DOWN=1	at the occurrence of clock edge, the counter decreases of 1 its current value.
HOLD=1	the counter holds without counting

Table 5.3: Operation of the divider.

The performed slow modulation transfers the PAM signal, originated by the analog values outputted by the RNG, to the output filter voltage V_{ctrl}, in turn driving the VCO. Fig. 5.6 shows the measured values for V_{ctrl}, compared with its expected values: the *ripple* which is superimposed to every analog value is originated (other than by the lock-in process of the PLL) by the mechanism of *average* so far discussed. The lower the ripple, the better the value of N is averaged.

The block-diagram of the programmable divider is shown in fig. 5.7. It is a 8-bit down counter, composed in turn of two 4-bit down counters, namely $DIV0$ and $DIV1$. Its operation is based on the value of the bits LOAD, DOWN, HOLD, as described in table 5.3. After the external value (for this application, 199 or 200) is loaded in the INPUT DATA bits, DIV0 starts counting down to 0 while DIV1 holds. When DIV0 gets to 0, the carry bit CY0 switches to 1; the next cycle DIV1 decreases of 1 its current value (DOWN state) and DIV0 loads the binary value "1111". This process goes on until also DIV1 has counted down to 0; at that point, all the eight outputs are 0. Then, DIV0 and DIV1 enter the LOAD state again and a new count begins. Since every stage is fed with a high-frequency signal (the frequency that is divided comes directly from the output of the VCO) the divider has been realized with the dynamic true single phase clock architecture TSPC-2. In fig. 5.8 the elementary TSPC-2 nMOS latch

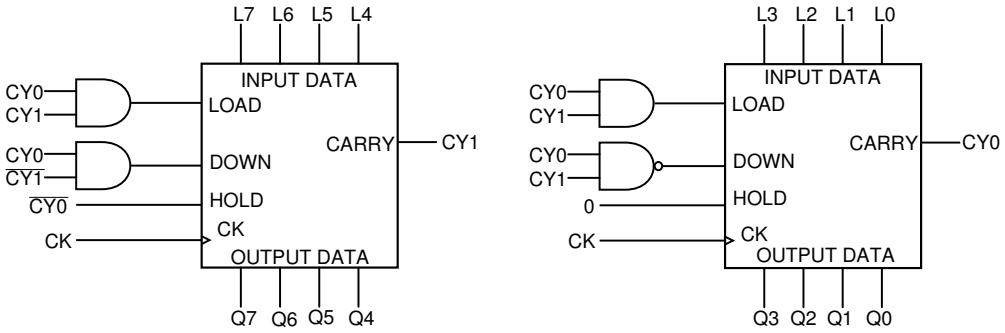


Figure 5.7: Block diagram of the 8-bit programmable divider.

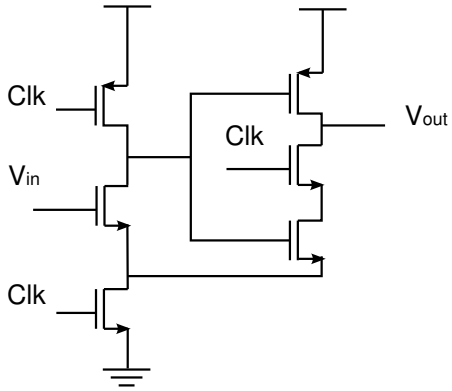


Figure 5.8: TSPC-2 nMOS latch.

is shown.

The VCO is composed of a standard input-stage, a six-stage ring oscillator, and a wave-shaping buffer. The elementary stage along with the architecture of the ring-oscillator, taken from [45], are shown in fig. 5.9 and 5.10. The four transistors M1, M2, M3 and M4 constitutes a CMOS latch delay-cell, whose dif-

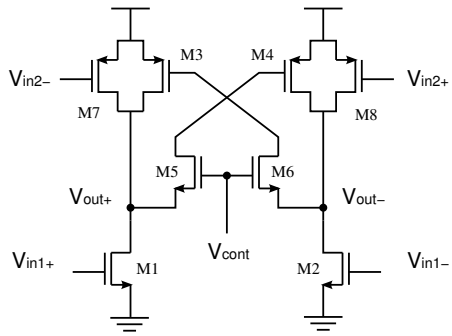


Figure 5.9: Ring-Oscillator: elementary stage.

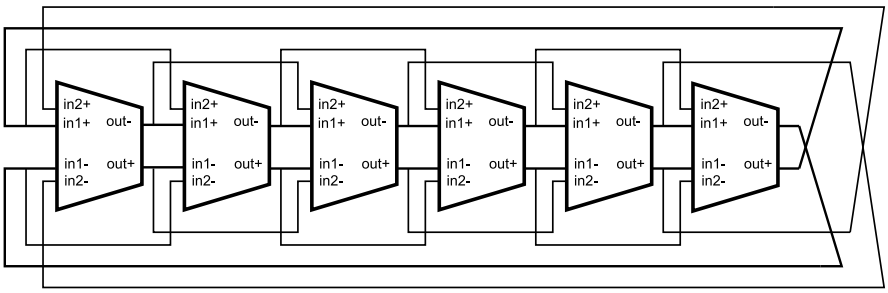


Figure 5.10: Ring-Oscillator: architecture.

ferential structure reduces the power-supply-injected phase noise. The cross-coupled transistors, M5 and M6, control the maximum gate voltage of the PMOS load transistors and limit the strength of the latch. When V_{ctrl} is low, the latch becomes weaker, and the output driving current of the PMOS load increases, and vice-versa. With the help of the positive feedback of the latch, the transition edges of the output waveform are sharp: this delay cell is able to perform *complete* switching thus further reducing the overall phase-noise.

In addition, by using a dual-delay scheme (fig. 5.10) to implement the VCO, through the introduction of transistors M7 and M8, higher operation frequency is achieved. In the differential stage, in fact, the couple of inputs V_{in2+} and V_{in2-} are taken from two stages *before* the current stage: these signals turn on in advance PMOS transistors during the output transitions and compensate for the performance of PMOS, which are usually slower than that of the NMOS. This operation then enhances the rise time of the output.

As it can be noticed in the microphotograph of the chip, shown in fig. 5.11, the prototype is composed of four separate circuits: the low-frequency part originating the modulating signal, which will be described in subsection 5.1.2, and three high-frequency PLLs, identical in all aspects but in the main output frequency. They are centered respectively on 2.7, 3.3 and 3 GHz; this solution has been adopted to ensure that in presence of errors in the computation of parasitic effects, at least one of the three PLLs locks at the desired frequency: parasitic effects, in fact, strongly influence the oscillating frequency of the ring-oscillator. Figure 5.12 shows the three VCO $f_{\mathrm{OUT}}/V_{\mathrm{ctrl}}$ characteristics obtained from simulations; for all three the voltage/frequency ratio is set to:

$$K_{\mathrm{VCO}} = 937.5\mathrm{MHz/V}.$$

The procedure followed for sizing the PLL band-loop and get stability is the same as in chapter 4. In this project design, the current delivered by the CP

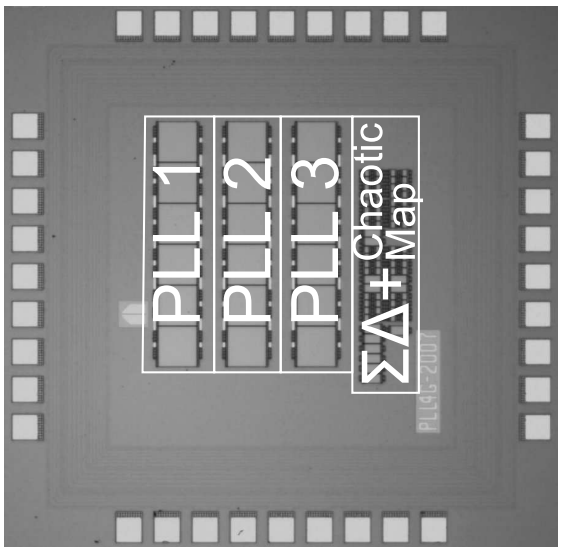


Figure 5.11: Microphotograph of the 0.13 μm SSCG prototype.

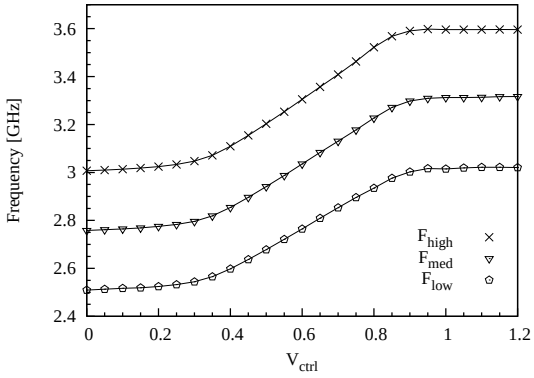


Figure 5.12: $f_{\mathrm{OUT}}/V_{\mathrm{ctrl}}$ simulated characteristics of the three VCO.

has been set to $I_{\mathrm{pump}} = 20\mu A$, while the division ratio of the divider, which in this case is programmable, can assume the two values $N = 199/200$. To ensure stability, the internal filter has been designed with:

$$C_1 = 600 \text{ pF}$$
$$C_2 = 60 \text{ pF}$$
$$R_1 = 6.8 \text{ k}\Omega$$

plus an additional low-pass filter, with $R = 100\text{k}\Omega$, $C = 710\text{fF}$, has been inserted between the LPF and the VCO. The additional pole introduced by this filter is positioned at a frequency that is sufficiently high to allow that the analysis of stability is conducted without taking into consideration its presence.

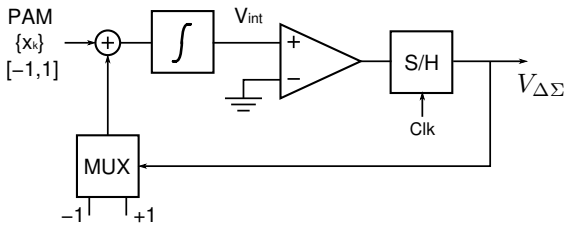


Figure 5.13: Block diagram of the $\Delta\Sigma$ converter.

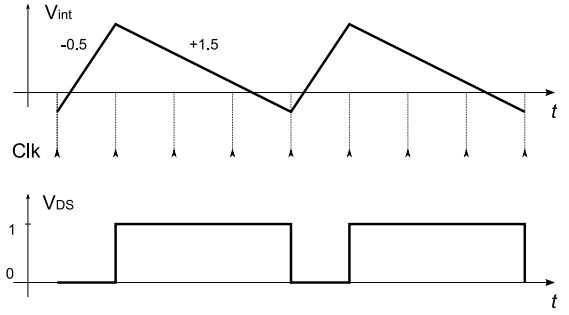


Figure 5.14: $\Delta\Sigma$ converter: output waveforms of integrator and sample/hold.

The closed-loop PLL bandwidth of the VCO results equal to:

$$\omega_n = \sqrt{\frac{I_{\mathrm{pump}} K_{\mathrm{VCO}}}{2\pi N C_1}} = 395\mathrm{krad/s}$$

thus meaning a cut-off frequency of about 63 KHz. Also, the PLL lock-in time can be estimated to $T_L = 2\pi/\omega_n \simeq 16\ \mu s$.

5.1.2 Implementation of the modulating signal

The block diagram of the *first order* $\Delta\Sigma$ is shown in fig. 5.13: it is composed of a loop including an integrator, a comparator, a sample/hold (S/H) and a multiplexer (MUX). The MUX is programmed to output "1" when the comparator outputs "-1", and viceversa: fig. 5.14 depicts the behavior of the output V_{int} of the integrator, along with the output $V_{\Delta\Sigma}$ of the S/H, in response to an analog value of "0.5" at the input. The input is summed to the feedback value, and the sum is fed to the integrator, which originates a ramp whose slope is proportional to it. The output of the integrator is then compared to zero and latched by the S/H. As a result, the output $V_{\Delta\Sigma}$ is a *periodic* waveform whose duty cycle is proportional to the normalized input: "0.5" considered over the interval [-1,1] corresponds to a duty cycle equal to 3/4.

More in general, the length of the period of the sequence depends on how much easily the input analog value can be represented in a digital format; "0.5"

Output frequency	3 GHz
Modulation type	Continuous-values Random
Modulation frequency	33 kHz
Frequency Deviation	15 MHz
Lock-range	2.562–3.012 GHz
Chip area	$650 \times 830 \mu\text{m}^2$
Power consumption	37mW
Closed loop Bandwidth	63 KHz $C_1 = 600\text{pF}, C_2 = 60\text{pF}$ $R_1 = 6.8\text{k}\Omega$

Table 5.4: Performance summary of the 0.13 μm SSCG prototype

is very easily representable with a couple of bits, but a different value, say "0.754" may require a number of bits that could be larger than the available 454. If the data is irrational (e.g. π) the sequence can not be periodic at all.

5.1.3 Post-fabrication measurements

Table 5.4 gives a performance summary of the integrated SSCG, referring to the PLL centered on 3 GHz. The active area occupies $650 \times 830 \mu\text{m}^2$ and the total area including pads is $1400 \times 1400 \mu\text{m}^2$. The measured power consumption amounts to 37mW, whereas the simulated power consumed by each PLL is around 14.8mW. Figure 5.15 shows the measurement of the $\Delta\Sigma$ output. From the bottom: 33 kHz clock, 15 MHz $\Delta\Sigma$ output and demodulated $\Delta\Sigma$ output, through an external filter. Figure 5.16 shows the measured lock-range of (a) the PLL centered on 2.7 GHz and (b) the PLL centered on 3 GHz. In the first case the lock-range spans from 2.328 GHz to 2.735 GHz; in the second case from 2.562 GHz to 3.012 GHz. Again referring to the PLL centered on 3 GHz, fig. 5.17 shows the measured spectrum of its output signal in case it is not modulated (a) and in case it is (b). The measured peak reduction is about 18 dB.

5.2 Conclusion

In this chapter the design of a SSCG that aims at reducing EMI emissions for application to standard Serial ATA-II is presented. The spreading of the clock spectrum is achieved through a slow frequency modulation involving a random continuous-values PAM signal as driving signal. One prototype has been designed, in CMOS 0.13 μm technology to operate at a clock of $f_0 = 3$ GHz.

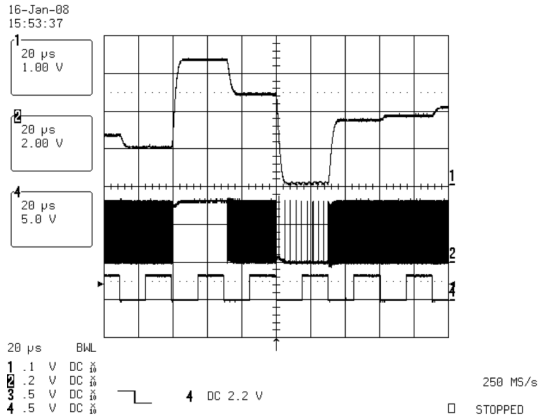
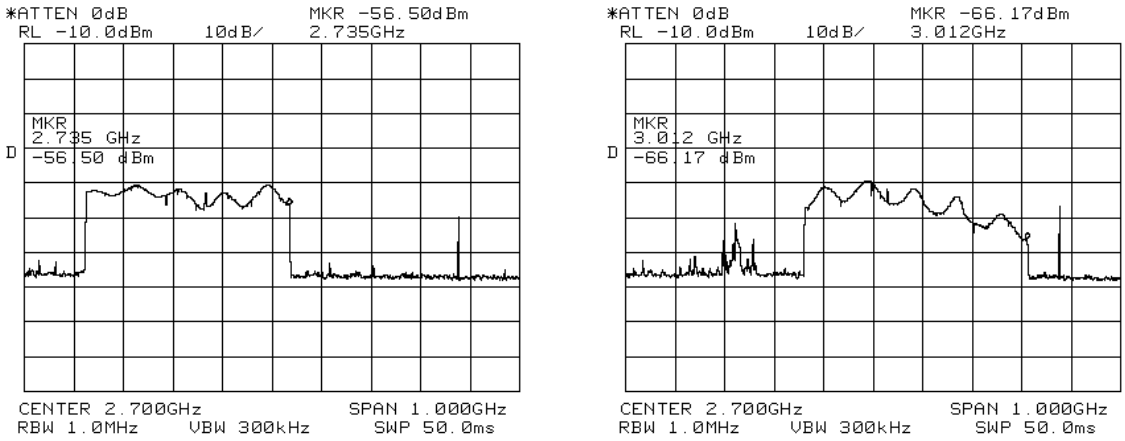


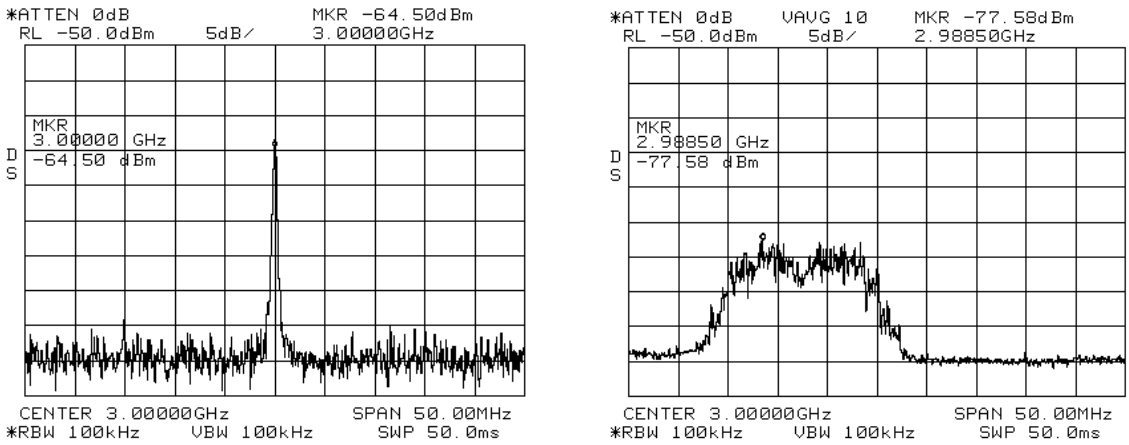
Figure 5.15: Measurement of the $\Delta\Sigma$ output. From the bottom: 33 kHz clock, 15 MHz $\Delta\Sigma$ output and demodulated $\Delta\Sigma$ output, through an external filter.



(a) (b)

Figure 5.16: Measured lock-range of (a) the PLL centered on 2.7 GHz and (b) the PLL centered on 3 GHz.

The prototype performs the expected modulation, achieving the desired clock power spectrum.



(a) (b)

Figure 5.17: (a) Measurements from the prototype in non spread spectrum mode; and (b) in spread spectrum mode.

Part II

Circuits for UWB.

Chapter 6

Introduction

ULTRA-WIDE BAND (UWB) radio[1] is a fast emerging technology with uniquely attractive features inviting major advances in wireless communications, networking, radar, imaging, and positioning systems. By its rule-making proposal in 2002, the Federal Communications Commission (FCC) in the United States essentially unleashed huge "new bandwidth" (3.6-10.1 GHz) at the noise floor, where UWB radios overlaying coexistent RF systems can operate using low-power ultra-short information bearing pulses. With similar regulatory processes currently under way in many countries worldwide, industry, government agencies, and academic institutions responded to this FCC ruling with rapidly growing research efforts targeting a host of exciting UWB applications: short-range very high-speed broadband access to the Internet, covert communication links, localization at centimeter-level accuracy, high-resolution ground-penetrating radar, through-wall imaging, precision navigation and asset tracking, just to name a few.

UWB characterizes transmission systems with instantaneous spectral occupancy in excess of 500 MHz or a fractional bandwidth of more than 20%. The fractional bandwidth is defined as B/f_c , where:

$$B := f_H - f_L$$

denotes the -10 dB bandwidth and center-frequency

$$f_c := (f_H + f_L)/2$$

with f_H being the upper frequency of the -10 dB emission point, and f_L the lower frequency of the -10 dB emission point.

[1]The following introduction to UWB systems is mainly drawn from the article [46], which the reader is referred to for a more detailed analysis of such systems in all their aspects.

Such systems rely on ultra-short (nanosecond scale) waveforms that can be free of sine-wave carriers and do not require IF processing because they can operate at *baseband* (since this is not true for all existing UWB systems, the ones operating at baseband are referred to as impulse-radio (IR) UWB, as opposed as *multiband* or *multi-carrier* UWB, discussed later in this chapter).

As information-bearing pulses with ultra-short duration have UWB spectral occupancy, UWB radios come with unique advantages that have long been appreciated by the radar and communications communities:

1. enhanced capability to penetrate through obstacles;
2. ultra high precision ranging at the centimeter level;
3. potential for very high data rates along with a commensurate increase in user capacity;
4. potentially small size and processing power.

Despite these attractive features, interest in UWB devices prior to 2001 was primarily limited to radar systems, mainly for military applications. But things changed drastically in the spring of 2002, when the FCC released a spectral mask allowing (even commercial) operation of UWB radios at the noise floor, but over an enormous bandwidth (up to 7.5 GHz). This huge "new bandwidth" opens the door for an unprecedented number of bandwidth-demanding position-critical low-power applications in wireless communications, networking, radar imaging, and localization systems [47]. It also explains the rapidly increasing efforts undertaken by several research institutions, industry, and government agencies to assess and exploit the potential of UWB radios in various areas. These include short-range, high-speed access to the Internet, accurate personnel and asset tracking for increased safety and security, precision navigation, imaging of steel reinforcement bars in concrete or pipes hidden inside walls, surveillance, and medical monitoring of the heart's actual contractions.

For wireless communications in particular, the FCC regulated power levels are very low (below -41.3 dBm), which allows UWB technology to overlay already available services such as the global positioning system (GPS) and the IEEE 802.11 wireless local area networks (WLANs) that coexist in the 3.6-10.1 GHz band. Although UWB signals can propagate greater distances at higher power levels, current FCC regulations enable high-rate (above 110 MB/s) data transmissions over a short range (10-15 m) at very low power. Similar to the frequency reuse principle exploited by wireless cellular architectures, low-power,

short-range UWB communications are also potentially capable of providing high spatial capacity, in terms of bits per second per square meter. In addition, UWB connectivity is expected to offer a rich set of software-controllable parameters that can be used to design location-aware communication networks flexible to scale in rates and power requirements.

To fulfill these expectations, however, UWB research and development has to cope with formidable challenges that limit their bit error rate (BER) performance, capacity, throughput, and network flexibility. Those include high sensitivity to synchronizing the reception of ultra-short pulses, optimal exploitation of fading propagation effects with pronounced frequency-selectivity, low-complexity constraints in decoding high-performance multiple access protocols, and strict power limitations imposed by the desire to minimize interference among UWB communicators, and with coexisting legacy systems, particularly GPS, unmanned air vehicles (UAVs), aircraft radar, and WLANs. These challenges call for advanced digital signal processing (DSP) expertise to accomplish tasks such as synchronization, channel estimation and equalization, multiuser detection, high-rate high-precision low-power analog/digital conversion (ADC), and suppression of aggregate interference arising from coexisting legacy systems.

Despite its renewed interest during the past decade, UWB has a history as long as radio. When invented by Guglielmo Marconi more than a century ago, radio communications utilized enormous bandwidth as information was conveyed using spark-gap transmitters. The next milestone of UWB technology came in the late 1960s, when the high sensitivity to scatterers and low power consumption motivated the introduction of UWB radar systems [48], [49], [50]. Ross' patent in 1973 set up the foundation for UWB communications. Readers are referred to [48] for a review of pioneer works in UWB radar and communications. In 1989, the U.S. Department of Defense (DoD) coined the term "ultra wideband" for devices occupying at least 1.5 GHz, or a -20 dB fractional bandwidth exceeding 25% [51]. Similar definitions were also adopted by the FCC notice of proposed rule making that regulated UWB recently. The rule making of UWB was opened by FCC in 1998. The resulting First Report and Order (R&O) that permitted deployment of UWB devices was announced on 14 February and released in April 2002 [52]. Three types of UWB systems are defined in this R&O: imaging systems, communication and measurement systems, and vehicular radar systems. Among the spectral masks assigned to these applications, the one for indoor communications is illustrated in fig. 6.1, as taken from [46].

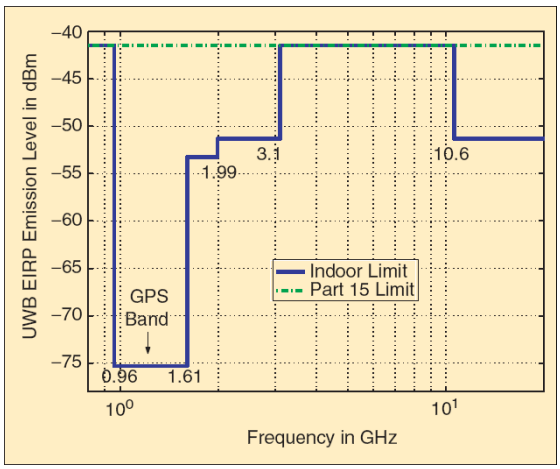


Figure 6.1: FCC indoor mask.

Foremost application trends in UWB system development are outlined in the following.

- *Wireless personal area networks (WPANs).* Also known as in-home networks, WPANs address short-range (generally within 10-20 m) ad hoc connectivity among portable consumer electronic and communication devices. They are envisioned to provide high-quality real-time video and audio distribution, file exchange among storage systems, and cable replacement for home entertainment systems. UWB technology emerges as a promising physical layer candidate for WPANs, because it offers high-rates over short range, with low cost, high power efficiency, and low duty cycle.

- *Imaging systems.* Different from conventional radar systems where targets are typically considered as point scatterers, UWB radar pulses are shorter than the target dimensions. UWB reflections off the target exhibit not only changes in amplitude and time shift but also changes in the pulse shape. As a result, UWB waveforms exhibit pronounced sensitivity to scattering relative to conventional radar signals. This property has been readily adopted by radar systems (see e.g., [48] and references therein) and can be extended to additional applications, such as underground, through-wall and ocean imaging, as well as medical diagnostics and border surveillance devices [55], [56].

- *Vehicular radar systems.* UWB-based sensing has the potential to improve the resolution of conventional proximity and motion sensors. Relying on

the high ranging accuracy and target differentiation capability enabled by UWB, intelligent collision-avoidance and cruise-control systems can be envisioned. These systems can also improve airbag deployment and adapt suspension/braking systems depending on road conditions. UWB technology can also be integrated into vehicular entertainment and navigation systems by downloading high-rate data from airport off ramp, road-side, or gas station UWB transmitters.

- *Wireless Sensor networks*. Wireless Sensor Networks (WSNs) consist of a large collection of small battery-powered devices called nodes which integrate computing, sensing and communication capabilities. WSNs promise to be a solution to all those pervasive and geographic problems of sensing, automatic surveillance, intelligent unmanned monitoring that are out of the scope of less flexible approaches heavily relying on rigid or semi-rigid communication infrastructures. The nodes can be static, if deployed for, e.g., avalanche monitoring and pollution tracking, or mobile, if equipped on soldiers, firemen, or robots in military and emergency response situations. Key requirements for sensor networks operating in challenging environments include low cost, low power, and multi functionality. High data-rate UWB communication systems are well motivated for gathering and disseminating or exchanging a vast quantity of sensory data in a timely manner. WSNs have been attracting increasing research interest since they pose unique design challenges in network organization and routing-algorithms, collaborative processing tasks and communication techniques. In the most promising applications, nodes are randomly and densely deployed either inside the phenomenon or very close to it and their functionality depends on the existence of a communication network capable of transferring information from one node to another and, possibly, to a central collecting unit. Typically, energy is more limited in sensor networks than in WPANs because of the nature of the sensing devices and the difficulty in recharging their batteries. Studies have shown that current commercial Bluetooth devices are less suitable for sensor network applications because of their energy requirements [53] and higher expected cost [54]. In addition, exploiting the precise localization capability of UWB promises wireless sensor networks with improved positioning accuracy. This is especially useful when GPSs are not available, e.g., due to obstruction.

Baseband pulses can also be modulated onto carrier(s) to higher frequency band(s). Recently, there has been an increasing interest in transmissions with multiple subbands, which we henceforth term multiband UWB (see e.g., [57], [58], [59]). In multiband UWB radios, pulses are modulated by several analog carriers to subbands 500-800 MHz wide. Multiband UWB can make more efficient use of the FCC mask, minimize interference to existing narrowband systems by flexible band selection, and facilitate future scalability of the spectrum use. Moreover, since each band occupies only a fraction of the bandwidth of a singleband transmission, the pulse shaper employed in multiband UWB can have much longer duration in time, which in turn eases implementation of the ADC, and enables implementation with off-the-shelf (OTS) components capitalizing on existing mature technology for wideband communications.

As in single-band UWB, challenges facing multiband UWB systems include timing acquisition and channel estimation. However, due to the introduction of multiple carrier frequencies, new challenges arise.

Multiband UWB radios rely on analog carriers, and thus have to deal with multiple carrier frequency offsets (CFO) arising from the mismatch of multiple transmit-receive oscillators. Unless compensated for, CFO is known to degrade performance severely, especially in carrier-modulated MC-UWB transmissions. For multiband UWB, carrier frequency synchronization is more challenging because there are more than one carrier frequencies, especially when OFDM or fast frequency-hopping is employed across multiple bands. For this reason, multiband UWB calls for CFO sensitivity studies, low complexity CFO estimators, and per-subcarrier based channel estimation modules.

Multiband UWB multiple access schemes also have to be designed by taking all bands into consideration. In particular, they require several mixers or digital fast Fourier (FFT) transform techniques to place the different signal components in the required bands.

To summarize, multiband based UWB-MA scheme must account for the following issues:

- flexibility to accommodate various schemes for multiple access,
- capability to collect full multipath diversity,
- scalability in spectral efficiency (from low, to medium, and high data rates).

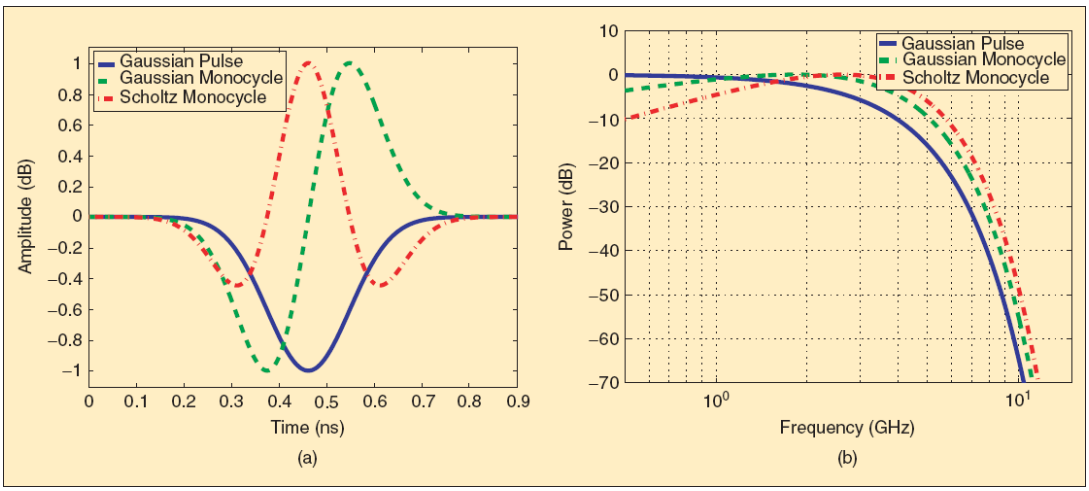


Figure 6.2: (a) Generally adopted pulse shapes in UWB communications; (b) Fourier transform of several pulse shapes. Pulse width: 0.7 ns.

Generally adopted spectrum shapers $p(t)$ for UWB communications include the Gaussian pulse, the Gaussian monocycle (first derivative of Gaussian pulse), and the second derivative of the Gaussian pulse, as depicted in fig. 6.2, along with their Fourier transforms (FTs). The reason behind the popularity of these pulses is twofold:

- Gaussian pulses come with the smallest possible time-bandwidth product of 0.5, which maximizes range-rate resolution and
- the Gaussian pulses are readily available from the antenna pattern [60].

With T_p at the sub-nanosecond scale, $p(t)$ occupies UWB with bandwidth $B \approx 1/Tp$. Such an ultra-short $p(t)$ also gives rise to multiple resolvable copies, and thus enables rich multipath diversity.

In a typical UWB system, each information-conveying symbol is represented by a number of N_f pulses, each transmitted per frame of duration $Tf \gg Tp$. Having N_f frames, over which a single symbol is spread, reverses the commonly used terminology where a frame consists of multiple symbols (here multiple frames comprise a symbol). With M-ary modulation, $\log_2 M$ message bits are transmitted during a signaling interval of duration $T_s = N_f T_f$ that corresponds to a bit rate $BR = (\log_2 M)/T_s$.

As bandwidth efficiency drops with increasing modulation size M, PPM is suitable for power-limited applications. In fact, PPM was almost exclusively adopted in the early development of UWB radios because negating ultrashort pulses were difficult to implement. As pulse negation became easier to imple-

ment, pulse amplitude modulation (PAM) attracted more attention. In particular, when $M = 2$, antipodal pulses are used to represent binary symbols, as in binary phase shift keying (BPSK) or bipolar signaling.

To allow for multi-user access (MA) to the UWB channel, time hopping (TH) was introduced early in [61]. With TH, each pulse is positioned within each frame duration T_f according to a user-specific TH sequence. With TH codes, MA is achieved by altering the pulse position from frame to frame, according to the sequence.

MA can also be enabled by modifying the pulse *amplitude* from frame to frame. Depending on the spreading codes employed, the UWB systems are termed TH-UWB [61], direct-sequence (DS)-UWB [62], or baseband single-carrier /multicarrier (SC/MC)-UWB [63], [64], just to name a few.

In addition to facilitating multiple access, spreading codes also shape the transmit spectrum. In fact, continuous pulse generation leads to strong spectral lines in the transmitted signal at multiples of the pulse repetition frequency: the transmit PSD in case of no spreading thus presents pronounced spectral lines. To cope with this problem and thus smooth the transmit power spectrum density, traditionally *random* sequences are used, typically originated for UWB systems by a pseudo-random generator.

Part II of this work is structured as follows:

- in chapter 7 a *chaos-based* sequence generation method for reducing Multiple Access Interference (MAI) in Direct Sequence UWB Wireless-Sensor-Networks (WSNs) is presented, along with the schematic design of a modulator scheme. Chaos-based spreading is numerically optimized to combine with the pulse profile (as obtained by extensive simulations) and maximizing the Bit-Rate (BR) at which each user may transmit given a certain link quality, measured as the Signal-to-Interference Ratio (SIR); when compared with traditional random sequences, the BR increase is up to 30%.

- in chapter 8 design and simulations of a Low-Noise Amplifier for impulse radio UWB are presented. This topic was studied during a study-abroad period in collaboration with Delft University of Technology, Delft, Netherlands. UWB communication poses big challenges for low-noise amplifier: since the LNA is the first active component close to the antenna, it must provide sufficient low noise behavior not only at one frequency but over the whole UWB frequency band from 3.1 to 10.6GHz.

Compared to competitive solutions, this chip will be much smaller and cheaper; it will use standard CMOS technology, and achieve very low noise, high gain and wide band matching at reasonable power consumption.

Chapter 7

A DS-UWB modulator for WSN chaos-based spreading

A TYPICAL CONFIGURATION of Wireless Sensor Network (WSN) is shown in Figure 7.1. Nodes are randomly and densely deployed, and their functionality depends on the existence of a communication network capable of transferring information from one node to another and, possibly, to a central collecting unit. Due to its structure, the physical wireless interface of such a network must cope with the presence of a potentially large number of competitors for the communication channel as well as with the absence of a central authority managing the diversity needed to distinguish competing logical links.

A way to address this problem is to employ Direct Sequence Code Division Multiple Access (DS-CDMA) that distinguishes nodes by means of binary antipodal spreading codes that act as node signatures. Due to stringent resource constraint in terms of energy and memory, typically short spreading factors are

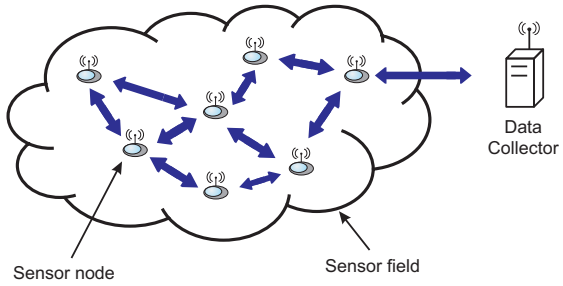


Figure 7.1: Typical WSN configuration. Sensor nodes are scattered in a sensor field.

used [65].

Though the design of the dedicated signaling channel and protocol is out of the scope of this work, it can be easily envisioned that each node generates its spreading code which is saved in its internal memory and then exchanged once with all the neighboring nodes before communication begins.

Since no global structure or authority is assumed, spreading codes cannot be made orthogonal unless a very complex negotiation is initiated that risks to involve the whole network and thus must be avoided [66].

Yet, since in many applications nodes are scattered in unknown but fixed positions, the communication environment can be considered bit-synchronous as receivers will be able, through standard DS-CDMA algorithm [67], to eventually compensate delays that do not change in time.

To avoid frequency allocation problems, and thus cope with uncontrolled and unsupervised environments, DS-CDMA modulation may be Ultra Wide Band (UWB). As already mentioned, to achieve UWB transmission, very short pulses (< 1ns) are employed whose shape is mainly dictated by spectrum shaping problems as well as implementation constraints rather than Inter Chip Interference (ICI) considerations.

In the light of the above discussion, the system under investigation is an UWB bit-synchronous interface exploiting code diversity to allow multiple access, for which codes cannot be orthogonal but must be generated and propagated locally without any global knowledge of the system, and in which ICI is non-negligible.

As far as the receiver is concerned, due to the stringent energy limitations of the nodes, it must be kept in the simplest form, i.e. that of a correlate-and-dump receiver matching the spreading sequence of the nodes whose signal must be decoded. Such a simple structure paired with the lack of orthogonality of spreading codes immediately hints at the presence of Multiple Access Interference (MAI) that actually becomes the main cause of quality degradation when the number of nodes increases.

As for the transmitted pulses, the most commonly adopted shapes for UWB systems are the Gaussian pulse and its derivatives as proposed by Win and Scholtz [68] and in [69] [70] [71] respectively.

The approach we pursue is that of designing a pulse-shaper whose pulses have spectral characteristics similar to the 2-nd derivative of a Gaussian pulse, and fitting within the spectral mask for UWB transmission. Then, we propose a chaos-based generator [72] of spreading sequences that may be easily triggered independently for each node (i.e. that does not require any central authority

for code assignment) and that effectively copes with ICI and in general with the pulse profile either by increasing the quality of transmission or allowing an higher ICI – and thus a higher bit rate (BR) when quality is fixed. To do so we start from the wide Literature on the exploitation of (quantized) chaotic dynamics to generate spreading sequences that improve the performance of DS-CDMA systems in various environments and operating conditions.

The key idea is that chaos-based generators control the statistical features of the sequences that, in turn, interact with the pulse shape in determining the final performance figure.

The results of this approach are extremely promising since intensive Monte-Carlo simulations allow to tune sequences to the pulse shape and obtain an increase in BR of 30% when compared with the pseudo-noise (PN) generation that would be the classical choice for these systems.

In the following:

- the system model is stated, starting from the signal transmitted from each user up to the derivation of the expression of the received signal. Particular emphasis are on the definition of the main performance figures. Standard Gaussian Assumption (SGA) is adopted to identify a unique significant quantity called Signal-to-Interference Ratio (SIR) accounting for the relative strength of the useful signal and of the disturbances. In our scheme SGA is well suited to estimate actual performance as the disturbing quantity can be expressed as a weighted sum of many independent variables. Its validity is confirmed in [72] through numerical results;

- then, the generation of spreading sequences by means of the quantization and periodical repetition of chunks of chaotic trajectories is briefly recalled. The statistical properties of the generated sequences are also described in detail;

- subsequently, the scheme of a modulator is proposed and described in detail. It entails a pulse-shaper, controlled by both the spreading symbols and the bits to be transmitted, along with an equivalent circuit for both transmitter and receiver antennas. An *average* impulse computed from simulations is then considered and compared with a classical 2-nd derivative Gaussian pulse fitting the spectral mask set for UWB transmissions;

- the path followed for the optimization of the sequence generator is briefly sketched and some results are given.

7.1 System model and performance figures

Given a set of U nodes, the signal generated by the u-th transmitter can be taken from [73]:

$$s^{(u)}(t) = \sqrt{P^{(u)}} \sum_{h=-\infty}^{\infty} b_h^{(u)} \sum_{k=0}^{N-1} y_k^{(u)} g\left(t - hT_{\mathrm{b}} - kT_{\mathrm{c}}\right), \tag{7.1}$$

where $b_h^{(u)} \in \{-1, 1\}$ are the transmitted bits, $y_j^{(u)} \in \{-1, 1\}$ represent the spreading symbols, T_{b} is the bit period, T_{c} is the chip period, the integer $N = T_{\mathrm{b}}/T_{\mathrm{c}}$ is the spread spectrum processing gain or *spreading factor*, $g\left(t\right)$ is the chip pulse and $\sqrt{P}$ a power control factor. Note that $\sqrt{P}$ depends on N, on the pulse profile, on the spreading sequence and sets the energy $\mathcal{E}_{\mathrm{b}}$ that the transmitter puts in each bit.

The signal generated at the transmitter is sent through the channel by means of an antenna that can be effectively modeled by an attenuation A_{tx} (assumed equal for all the nodes) and a time-derivative [74]. Along the channel the signal suffers from an attenuation $A_{\mathrm{ch}}^{(u)}$ and a delay $\tau^{(u)}$ that depends on the traveled path, and finally arrives to the receiver antenna that imposes a further attenuation A_{rx} and a time-derivative.

Hence, the signal due to the u-th transmitter that is received can be written in terms of the second derivative of the chip original pulse [69] $g_{\mathrm{rx}}\left(t\right) = (d^2/dt^2)g\left(t\right)$ as

$$\begin{aligned} s_{\mathrm{rx}}^{(u)}(t) &= A_{\mathrm{tx}} A_{\mathrm{ch}}^{(u)} A_{\mathrm{rx}} \sqrt{P^{(u)}} \times \\ &\qquad \sum_{h=-\infty}^{\infty} b_h^{(u)} \sum_{k=0}^{N-1} y_k^{(u)} g_{\mathrm{rx}}\left(t - hT_{\mathrm{b}} - kT_{\mathrm{c}}\right). \end{aligned}$$

Since we assume that the receivers can eventually compensate delays that do not change in time, we are legitimate to set $\tau^{(u)} = 0$ for every u. On the contrary, we cannot assume straightforwardly that $P^{(u)}$ can be set to ensure power equalization $A_{\mathrm{rx}} A_{\mathrm{ch}}^{(u)} A_{\mathrm{tx}} \sqrt{P^{(u)}} =$const. In fact, in a general WSN scenario (i.e., when no central node is assumed), more than one receiver may be active at the same time, each one potentially interested in the signal coming from a different transmitter.

It is reasonable to assume that all the nodes have identical air interfaces and thus that, when transmitting in the same conditions, deliver the same energy per bit $\mathcal{E}_{\mathrm{b}}$ to the receiver. More in detail we may concentrate on the reception of the 0-th bit, choose $A_{\mathrm{rx}} A_{\mathrm{ch}}^{(u)} A_{\mathrm{tx}} = 1$ as a reference ideal conditions and get

$$\begin{aligned}\mathcal{E}_{\mathrm{b}} &= \int_{-\infty}^{\infty} \left| \sqrt{P^{(u)}} \sum_{k=0}^{N-1} y_k^{(u)} g_{\mathrm{rx}}\left(t - kT_{\mathrm{c}}\right) \right|^2 dt \\ &= P^{(u)} \sum_{j=0}^{N-1} \sum_{k=0}^{N-1} y_k^{(u)} y_j^{(u)} \int_{-\infty}^{\infty} g_{\mathrm{rx}}\left(t - jT_{\mathrm{c}}\right) g_{\mathrm{rx}}\left(t - kT_{\mathrm{c}}\right) dt \\ &= P^{(u)} \sum_{j=0}^{N-1} \sum_{k=0}^{N-1} y_k^{(u)} y_j^{(u)} G_{\mathrm{rx}}\left((j-k)T_{\mathrm{c}}\right),\end{aligned}$$

where we assumed $g\left(-t\right) = g\left(t\right)$ (and thus $g_{\mathrm{rx}}\left(-t\right) = g_{\mathrm{rx}}\left(t\right)$) to define $G_{\mathrm{rx}}\left(x\right) = \int_{-\infty}^{\infty} g_{\mathrm{rx}}\left(t\right) g_{\mathrm{rx}}\left(x - t\right) dt$ as the convolution of the chip pulse with itself. From the above equality we get

$$P^{(u)} = \frac{\mathcal{E}_{\mathrm{b}}}{\sum_{j=0}^{N-1} \sum_{k=0}^{N-1} y_k^{(u)} y_j^{(u)} G_{\mathrm{rx}}\left((j-k)T_{\mathrm{c}}\right)}. \tag{7.2}$$

Note that when received pulses do not produce inter-chip interference (ICI) we have $G_{\mathrm{rx}}\left(mT_{\mathrm{c}}\right) = 0$ for every integer $m \neq 0$ and $G_{\mathrm{rx}}\left(0\right) = \int_{-\infty}^{\infty} g_{\mathrm{rx}}\left(t\right)^2 dt$ that is the pulse energy. In this case

$$P^{(u)} = \frac{\mathcal{E}_{\mathrm{b}}}{N G_{\mathrm{rx}}\left(0\right)}$$

i.e., $P^{(u)}$ is the ratio between the bit energy and N times the received chip pulse energy. Yet, received UWB pulses are, in general, non ICI-free and P takes into account the whole bit signal. In the following we will assume that $P^{(u)}$ is such that $\mathcal{E}_{\mathrm{b}} = 1$, that is, $P^{(u)}$ is set to make the waveform corresponding to the unmodulated spreading sequence, defined as

$$y_{\mathrm{rx}}^{(u)}(t) = \sqrt{P^{(u)}} \sum_{k=0}^{N-1} y_k^{(u)} g_{\mathrm{rx}}\left(t - kT_{\mathrm{c}}\right),$$

a unit energy waveform.

The decoding part of the receiver is fed with the sum of all the incoming signals plus the thermal noise $n(t)$, i.e. with:

$$\begin{aligned}z(t) &= n(t) + A_{\mathrm{rx}} A_{\mathrm{tx}} \sum_{u=0}^{U-1} A_{\mathrm{ch}}^{(u)} \sqrt{P^{(u)}} \sum_{h=-\infty}^{\infty} b_h^{(u)} \times \\ &\qquad \sum_{k=0}^{N-1} y_k^{(u)} g_{\mathrm{rx}}\left(t - hT_{\mathrm{b}} - kT_{\mathrm{c}}\right) \\ &= n(t) + A_{\mathrm{rx}} A_{\mathrm{tx}} \sum_{u=0}^{U-1} A_{\mathrm{ch}}^{(u)} \sum_{h=-\infty}^{\infty} b_h^{(u)} y_{\mathrm{rx}}^{(u)}(t - hT_{\mathrm{b}}),\end{aligned} \tag{7.3}$$

is the waveform corresponding to the unmodulated spreading sequences at the receiver.

We assume to use the simplest possible decoding, i.e. a correlate and dump receiver matched with the useful transmitter. Within this scheme we focus, without loss of generality, on the decoding of the 0-th bit of the 0-th transmitter and first compute

$$X = C \int_{-\infty}^{\infty} z(t) y_{\mathrm{rx}}^{(0)}(t) dt$$

for some positive constant C and estimate $b_0^{(0)} = 1$ if $X > 0$ or $b_0^{(0)} = -1$ if $X < 0$.

Going back to (7.3) one gets:

$$\begin{aligned} X &= C A_{\mathrm{rx}} A_{\mathrm{tx}} \sum_{u=0}^{U-1} A_{\mathrm{ch}}^{(u)} \sum_{h=-\infty}^{\infty} b_h^{(u)} \int_{-\infty}^{\infty} y_{\mathrm{rx}}^{(u)}(t - hT_{\mathrm{b}}) y_{\mathrm{rx}}^{(0)}(t) dt + \\ & \quad C \int_{-\infty}^{\infty} n(t) y_{\mathrm{rx}}^{(0)}(t) dt. \end{aligned}$$

Since correlation with $y_{\mathrm{rx}}^{(0)}$ is a key component of the decision signal X, we define $X_h^{(u)} = \int_{-\infty}^{\infty} y_{\mathrm{rx}}^{(u)}(t - hT_{\mathrm{b}}) y_{\mathrm{rx}}^{(0)}(t) dt$ to rewrite:

$$\begin{aligned} X &= C A_{\mathrm{rx}} A_{\mathrm{tx}} \Bigg[A_{\mathrm{ch}}^{(0)} X_0^{(0)} b_0^{(0)} + A_{\mathrm{ch}}^{(0)} \sum_{\substack{h=-\infty \\ h \neq 0}}^{\infty} X_h^{(0)} b_h^{(0)} + \\ & \quad \sum_{u=1}^{U-1} A_{\mathrm{ch}}^{(u)} \sum_{h=-\infty}^{\infty} X_h^{(u)} b_h^{(u)} \Bigg] + C \int_{-\infty}^{\infty} n(t) y_{\mathrm{rx}}^{(0)}(t) dt. \end{aligned}$$

Note now that $X_0^{(0)} = \mathcal{E}_{\mathrm{b}}$ that, by means of the factors $P^{(u)}$ is made independent of u and, in our assumptions, equal to 1. With this we may finally set $C = \left(A_{\mathrm{rx}} A_{\mathrm{tx}} A_{\mathrm{ch}}^{(0)} \right)^{-1}$ to obtain:

$$\begin{aligned} X = b_0^{(0)} + & \\ \underbrace{\sum_{\substack{h=-\infty \\ h \neq 0}}^{\infty} X_h^{(0)} b_h^{(0)}}_{\mathrm{I_s}} + & \underbrace{\sum_{u=1}^{U-1} \frac{A_{\mathrm{ch}}^{(u)}}{A_{\mathrm{ch}}^{(0)}} \sum_{h=-\infty}^{\infty} X_h^{(u)} b_h^{(u)}}_{\mathrm{I_c}} + \underbrace{C \int_{-\infty}^{\infty} n(t) y_{\mathrm{rx}}^{(0)}(t) dt}_{\mathrm{I_n}}, \end{aligned}$$

where we have highlighted the useful component $b_0^{(0)}$, the self-interference $\mathrm{I_s}$ due to the other bits of the useful stream, the cross-interference $\mathrm{I_c}$ due to the other transmitters, and the thermal noise contribution $\mathrm{I_n}$.

Each of the non-useful components in the expression of X may be assumed to be a zero-mean Gaussian random-variable (this is called standard gaussian

assumption). This is straightforward for the thermal-noise component but is also a sensible assumption for the self- and cross-interference that are weighted sums of the independent antipodal random variables $b_h^{(u)}$.

In the light of this, the performance of the elementary decoder is uniquely determined by the variances σ_{s}^2, σ_{c}^2, and σ_{n}^2. In fact, its bit error probability [75] is

$$P_{\mathrm{err}} = \frac{1}{2}\operatorname{erfc}\sqrt{\frac{1}{2(\sigma_{\mathrm{s}}^2+\sigma_{\mathrm{c}}^2+\sigma_{\mathrm{n}}^2)}} \quad .$$

In the following we will assume that the system is dominated by interference, i.e., that $\sigma_{\mathrm{s}}^2+\sigma_{\mathrm{c}}^2 \gg \sigma_{\mathrm{n}}^2$, so that the signal-to-interference (SIR)

$$\rho = \frac{1}{\sigma_{\mathrm{s}}^2+\sigma_{\mathrm{c}}^2} \tag{7.4}$$

becomes *the main performance figure*.

The variances involved in the definition of SIR will be computed by averaging both on the transmitted bits ($\mathbf{E}_b$) and on the possible spreading sequences ($\mathbf{E}_y$) that affect the $X_h^{(u)}$ terms. Since the bits are independent and zero-mean we have $\mathbf{E}_b\left[b_{h'}^{(u')}b_{h''}^{(u'')}\right] = 0$ whenever $u' \neq u''$ or $h' \neq h''$, while $\mathbf{E}_b\left[\left(b_h^{(u)}\right)^2\right] = 1$. This helps writing

$$\sigma_{\mathrm{s}}^2 = \sum_{\substack{h=-\infty \\ h\neq 0}}^{\infty} \mathbf{E}_y\left[\left(X_h^{(0)}\right)^2\right] \tag{7.5}$$

$$\sigma_{\mathrm{c}}^2 = \sum_{u=1}^{U-1}\left(\frac{A_{\mathrm{ch}}^{(u)}}{A_{\mathrm{ch}}^{(0)}}\right)^2 \sum_{h=-\infty}^{\infty} \mathbf{E}_y\left[\left(X_h^{(u)}\right)^2\right] \tag{7.6}$$

$$= \sum_{u=1}^{U-1}\left(\frac{A_{\mathrm{ch}}^{(u)}}{A_{\mathrm{ch}}^{(0)}}\right)^2 \sum_{h=-\infty}^{\infty} \mathbf{E}_y\left[\left(X_h^{(1)}\right)^2\right] \tag{7.7}$$

in the last of which we have realized that, if we agree to use independent instances of the same sequence generator for each transmitter, the expectation in σ_{c}^2 is actually independent of u as long as $u \neq 0$. Hence, the cross-interference power can be factored in two terms the first of which

$$Z = \sum_{u=1}^{U-1}\left(\frac{A_{\mathrm{ch}}^{(u)}}{A_{\mathrm{ch}}^{(0)}}\right)^2$$

takes into account the ratios between the attenuations of the interfering component and the attenuation of the useful component and is dependent on the channel and on the node deployment models. Since, for a given scenario, Z

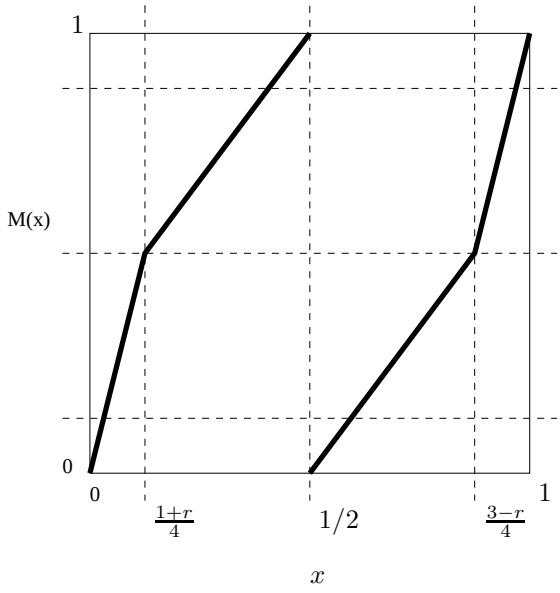


Figure 7.2: The family of maps used for the generation of spreading sequences whose statistical features depend on parameter r.

indicates the number of nodes that can be used to obtain a desired link quality, in the follow we will call Z as load factor. The second term takes into account the correlation of the waveforms corresponding to the unmodulated spreading sequences with different delays.

7.2 Chaos-based generation of spreading sequences

As far as y_k^u are concerned, they are taken from the quantization of the trajectory of a discrete time chaotic dynamical system $x_{k+1} = M(x_k)$, where $M : [0,1] \mapsto [0,1]$ is assumed to be at least a mixing chaotic map [21]. The spreading sequence is selected considering a chunk of length N $x_k, x_{k+1}, \ldots, x_{k+N-1}$ of the map trajectory and getting binary values by quantizing so that $y_k = +1$ if $x_k < 1/2$ and $y_k = -1$ if $x_k \geq 1/2$.

The family of maps we will use is shown in Fig. 7.2 where $r \in]-1, 1[$ is the parameter defining the breakpoints between adjacent segments.

It has been shown that for such a map [21], being $i \leq j \leq k \leq l$:

$$\begin{aligned} \mathbf{E}_y[y_i^u y_j^u] &= r^{j-i} \\ \mathbf{E}_y[y_i^u y_j^u y_k^u y_l^u] &= r^{j-i+l-k} \end{aligned} \tag{7.8}$$

This property is used to compute the $\mathbf{E}_y[\cdot]$ terms contained in the expression of σ_{s}^2 and σ_{c}^2. Summarizing, the family of maps here considered is able to produce antipodal sequences with exponentially decaying second- and fourth-order correlations with the rate of decay r that may be arbitrarily set to any number in $]-1,1[$.

7.3 Design of the Modulator

The proposed modulator, designed in CMOS UMC130 1.2V technology, is meant to generate a sequence of 2-nd derivative Gaussian-shaped pulses, controlled by both the spreading sequence and the bits to be transmitted. It is based on the classical scheme used to obtain a glitch from a NAND gate [76] (Fig. 7.3). As one can see, a rising edge at the input In produces a glitch at the NAND output, subsequently amplified by a buffer, due to the fact that the two inputs of the NAND carry a phase difference depending on the delay τ introduced by the inverter. The width τ_1 of the glitch, in turn, depends both on the delay τ and on the load C_{tune}.

In order to obtain the proper shape for the final pulse, and at the same time to ensure that the sequence is composed of equidistant pulses, a second block is introduced, whose function is that of a *delay selector*, whose schematic is shown in Fig. 7.4. If $\mathrm{Sel} = 1$, then transistor $\mathrm{M1}$ is on, while $\mathrm{M2}$ is off, so that the CMOS pass transistor PT is open: the signal In then gets to the output after passing through the inverters $\mathrm{I1}$ and $\mathrm{I2}$, thus carrying a delay here defined as τ_2. On the contrary, if $\mathrm{Sel} = 0$, then transistor $\mathrm{M1}$ is off while $\mathrm{M2}$ is on, so that the CMOS pass transistor PT is close, whereas the output of $\mathrm{I2}$ is three-state: the signal In then gets to the output after passing through PT, that is almost immediately, carrying a negligible delay (here considered vanishing).

The whole modulator scheme, shown in Fig. 7.5, is composed of two branches, each one entailing a pulse generator, a delay selector and some additional logic; the simulated circuit includes also an equivalent model of the transmitting antenna, as well as an equivalent circuit of the receiving one; both of them have been taken from [77] and their components (including resistors $R1$ and $R2$) have been sized so to obtain the desired derivative behavior.

Given an input clock Clk, the two outputs of the pulse generators P_1 and P_2 respond to a rising edge with a glitch, as already seen. Then the transmitting antenna performs their difference, $\mathrm{P}_1 - \mathrm{P}_2$, whose waveform is shown in Fig. 7.5 too. As one can see, depending on the value of the controlling signal Sel, the signal that gets delayed is either P_1 or $\mathrm{P2}$, so that two shapes are possible

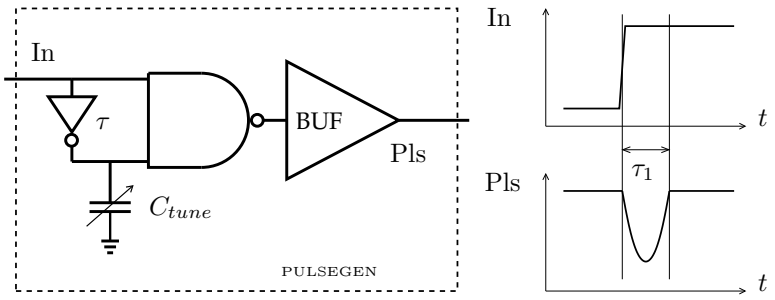


Figure 7.3: Pulse Generator based on the glitch produced by a NAND gate when one input get delayed with respect to the other one.

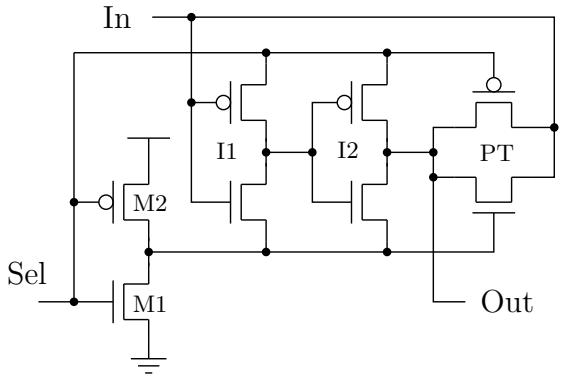


Figure 7.4: Delay Selector: its output is equal to the input either after a negligible delay or after the delay τ_2.

for the pulse generated by the modulator, one being the other after changing sign of its values. Note that these pulses are similar to the 1-st derivative of the Gaussian pulse; after the further derivative performed by the transmitting antenna, transmitted pulses get to be 2-nd derivative Gaussian shaped.

The additional logic present at the input of the two delay selectors, composed of an EX-OR gate whose inputs are the spreading sequence bits (Seq) and the bits to be transmitted (Bit), determines the final operation of the modulator: starting from a given value for Bit and some given values for the chips Seq of the spreading sequence, pulses $\mathrm{P}_1 - \mathrm{P}_2$ are generated as can be seen in Fig. 7.6, where a factor spreading $N = 3$ is used as a simple example; note as this operation corresponds to what is described by Equation 7.1.

The transmitted pulse $g_{\mathrm{c}}(t)$ at the output of the transmitting antenna obtained from circuit level simulations is shown in Fig. 7.7 and it is compared with the 2-nd derivative gaussian pulse $g_{\mathrm{i}}(t)$ whose value of standard deviation has been taken from [78] and corresponds to the one that ensures to optimize the fitting of the FCC power spectrum UWB mask. To verify suitability in

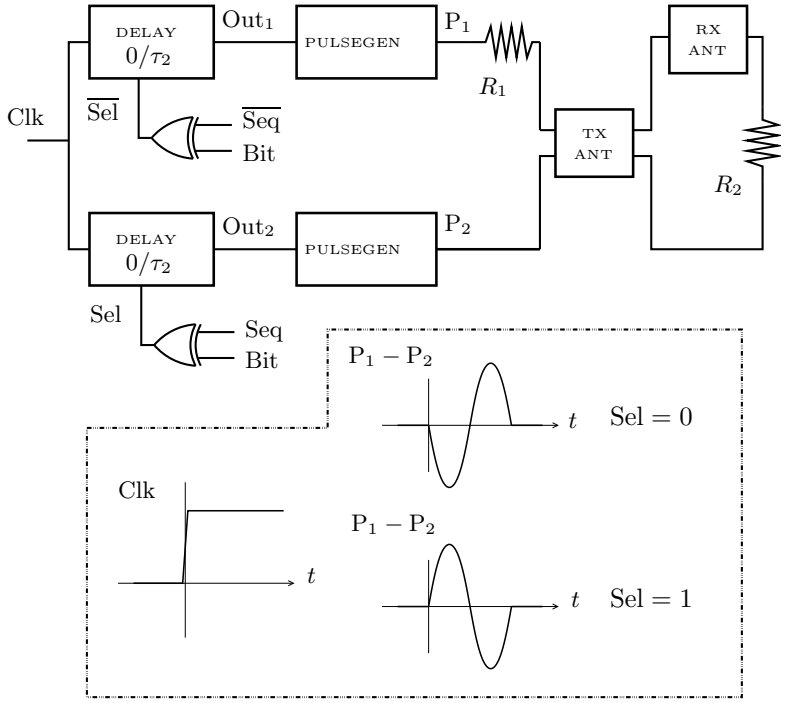


Figure 7.5: Simulated circuit: block scheme of the Modulator, transmitting and receiving antenna.

terms of spectrum occupation, fig. 7.8 shows a comparison between the spectra of a theoretical Gaussian 2-nd derivative $g_{\text{i}}(t)$ and the simulated pulse $g_{\text{c}}(t)$. As can be noted, the spectra are almost identical and far below the FCC mask.

7.4 Numerical Results

In this section we illustrate the simulation strategy and analyze the performance of the system using pulses coming from circuit-level simulations of the described modulator. We also determine, by numerical simulation, the optimum spreading and the corresponding maximum achievable SIR.

To obtain specific results and allow comparison between the maximum value of BR obtained using i.i.d. and chaos-based sequences, we have computed σ_{s}^2 and σ_{c}^2 numerically for $r \in [-1, 1]$, $N = 31, 63, 127, 255$ and for different values of T_{c}. If we set the minimum value of link quality $\rho_{\min}$, the spreading factor N and the load factor Z, we need to choose the values of r and T_{c} such that BR is maximized.

Here three different values of $\rho_{\min}$ are considered, corresponding to the values of P_{err} 10^{-2}, 10^{-3}, 10^{-4}, in a scenario where SGA is adopted, thermal

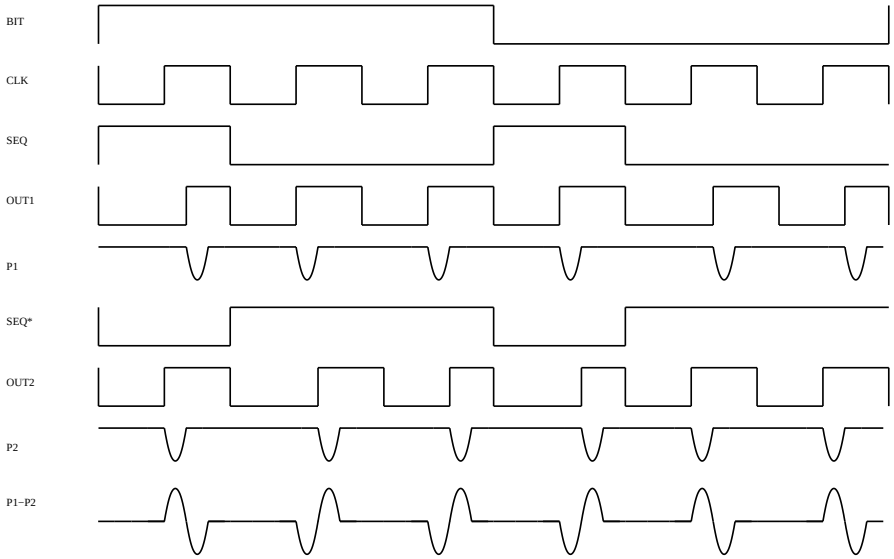


Figure 7.6: Modulator: waveforms.

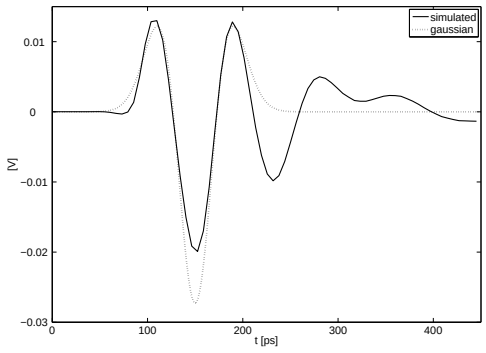


Figure 7.7: Generated pulse compared with 2-nd derivative Gaussian pulse.

noise is neglected and signal power is normalized (see (7.4)); Z has been set to a value called Z_{max}, equal to 90% of the maximum value of Z which allows to obtain $\rho = \rho_{\min}$, in case T_{c} is such that 99% of the pulse energy is contained in the time-interval $[0, T_{\mathrm{c}}]$. This values are used to obtain the maximum Bit-Rate both for i.i.d. and chaos-based spreading policy.

Table 7.1 reports the results of this optimization. As one can see, chaos-based spreading sequence strategy always outperforms i.i.d. sequence generation method. Note that the value r, here called r_{opt}, corresponds to the parameter used to compute second- and fourth-order moment of the spreading sequences in Equation (7.5,7.7), in turn corresponding to the value of the

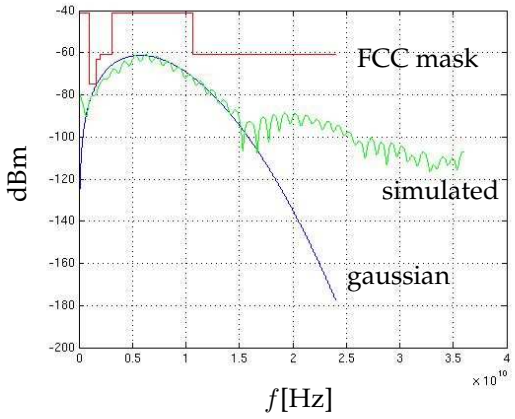


Figure 7.8: Comparison between the spectra of 2-nd derivative of a Gaussian waveform of the pulse obtained from simulation of the designed circuit.

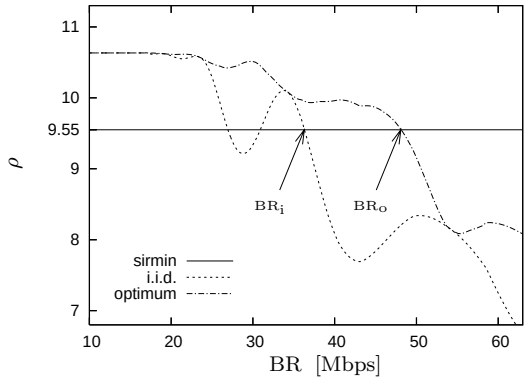


Figure 7.9: SIR obtained using i.i.d. sequences vs optimum correlated sequences for a system with pulses from simulations, $N = 255$ and $Z = 24.03$.

breaking points of the map branches, defined in Fig. (7.2).

As a reference example, we can consider a scenario with a spreading factor $N = 255$ and a minimum value of link quality $\rho_{\min} = 9.55$ which corresponds to $\mathrm{P_{err}} = 10^{-3}$.

Figure 7.9 compares the SIR that is achieved using i.i.d. and chaos-based spreading respectively for different values of BR. The maximum achievable BR is evaluated intersecting the SIR curve with the horizontal line corresponding to $\rho_{\min}$. In the case of i.i.d. sequences, we will indicate such a BR as $\mathrm{BR_i}$, whereas in the case of chaos-based spreading policy we have to use the dashed trend, looking for the value of r which minimizes BR once that ρ is set equal to $\rho_{\min}$. We indicate this value as $\mathrm{BR_o}$ and, as one can see, we have $\mathrm{BR_o} \geq \mathrm{BR_i}$ We quantify the performance provided by chaos-based spreading policy

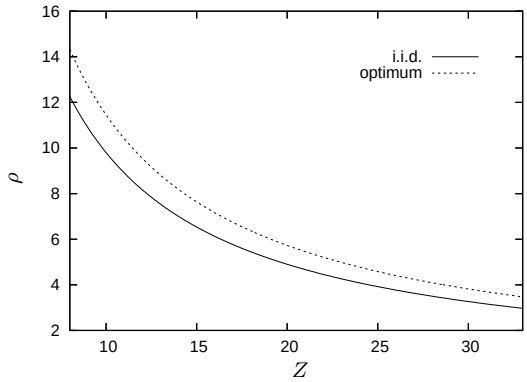


Figure 7.10: BR as a function of the load factor obtained using i.i.d. sequences and chaos-based sequences for a system with pulses from simulations, $N = 127$ and $\rho_{\min} = 13.83$.

over i.i.d. sequences using $\mathrm{SU}\,\% = 100\,(\mathrm{BR_o}\,/\,\mathrm{BR_i}\,-1)$ where $\mathrm{BR_i}$ and $\mathrm{BR_o}$ are the maximum value of Bit Rate we can achieve using i.i.d. and chaos-based sequences respectively.

Note that, in Table 7.1, inequality yields independently of the link quality $\rho_{\min}$ we have chosen.

N	$Z^{\max}$	$\mathrm{BR_i}$ [Mbps]	$\mathrm{BR_o}$ [Mbps]	r_{opt}	SU %	$\rho_{\min}$	$\mathrm{P_{err}}$
31	5.13	296.48	391.55	-0.43	32.06	5.41	10^{-2}
63	10.44	145.81	193.39	-0.44	32.63		
127	21.15	72.11	95.49	-0.44	32.42		
255	42.48	35.91	47.55	-0.44	32.44		
31	2.88	300.80	397.58	-0.43	32.18	9.54	10^{-3}
63	5.94	146.75	193.94	-0.44	32.15		
127	11.97	72.83	96.48	-0.44	32.48		
255	24.03	36.28	48.09	-0.44	32.57		
31	1.98	301.72	397.85	-0.43	31.86	13.83	10^{-4}
63	4.05	148.03	196.74	-0.43	32.91		
127	8.28	72.80	96.31	-0.44	32.29		
255	16.56	36.35	48.23	-0.44	32.69		

Table 7.1: Bit Rate performance using simulated average pulse for different values of N and $\rho_{\min}$.

As a further example, in Fig. 7.10 we show the trend of ρ when $N = 127$ and Z sweeps from 8 to 33. As one can see, chaos-based spreading sequence ρ always outperforms i.i.d. sequence ρ, independently of the number of active nodes.

7.5 Conclusion

A DS-UWB modulator taking into account both the transmitter and receiver antenna has been designed and simulated in CMOS UMC130 1.2V technology, and here presented along with a chaos-based sequence generation method for synchronous WSN. The modulator is able to generate sequences of 2-nd derivative Gaussian shaped pulses, whose spectrum fits FCC mask for UWB. The sequence generation method, then, allows the reduction of MAI increasing the Bit-Rate. Numerical simulations, using different system parameters values, has evidenced better performances of chaos-based spreading policy over traditional i.i.d. sequences. Over a bandwidth compliant with current regulations, a BR increase up to 30% can be achieved for a given communication quality.

Chapter 8

A UWB CMOS 0.13μm LNA with Dual-Loop Negative Feedback

ULTRA WIDE BAND UWB communication poses big challenges for low-noise amplifier (LNA) design. Since the LNA is the first active component close to the antenna, it must provide sufficient low noise behavior not only at one frequency but over the whole UWB frequency band from 3.1 to 10.6GHz. The targeted noise figure is around 3dB, which is quite a challenging value compared to previously reported works. Power gain is another important parameter; S_{21} should be larger than 15dB[1].

Wide-band impedance matching is another critical issue: the LNA has to be matched to 100Ω, the characteristic impedance of the antenna [79], so S_{11} should be below -10dB over the entire frequency band. At the same time, we need to ensure that the matching network will not destroy the noise performance and waste chip area. Some LNA designs by other UWB groups in the world [80] employ LC ladder networks. However, an inductor is a costly component since it consumes most of the chip area and also introduces large parasitic resistances that will increase noise. Power consumption is another consideration: our goal is to limit the current consumption to less than 15mA. The IC technology we target is UMC (United Microelectronic Corporation) 0.13μm CMOS.

Since our design is based on negative feedback, it will benefit from technol-

[1] In a usually matched system, the transducer power gain equals $|S_{21}|^2$

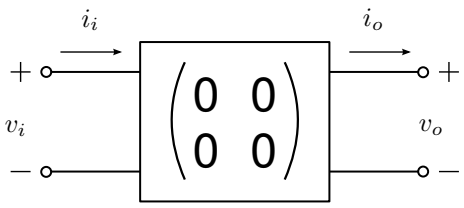


Figure 8.1: The nullor.

ogy advancements, leading to a larger loop gain and hence a larger bandwidth and a lower power consumption.

In the following, we will discuss the dual-loop feedback topology chosen for the LNA and will define the feedback network according to our specifications. Subsequently, a nullor implementation with optimized performance and relevant simulation results will be presented. Finally, a comparison between our work and previously reported wide-band amplifiers will be given.

8.1 LNA Topology

The amplifier-design methodology described in the following is based on the negative-feedback topology, consisting of an active circuit combined with a feedback network.

The active circuit in turn is in first approximation schematized with a *nullor*, that is an *ideal* two-port (fig. 8.1) whose chain matrix contains only zeros, that is:

$$\begin{pmatrix} v_i \\ i_i \end{pmatrix} = \begin{pmatrix} 0 & 0 \\ 0 & 0 \end{pmatrix} \begin{pmatrix} v_o \\ i_o \end{pmatrix}$$

Subsequently, in the next section the design of an active circuit will be presented, whose properties approach the ones of the nullor, as much as required by the application.

To achieve accurate input impedance matching, two feedback loops are used: a voltage-to-current (V-I) feedback loop and an indirect current-to-current (I-I) feedback loop, as shown in Fig. 8.2.

The reason why this topology is called "indirect feedback" is because the I-I feedback does not sense the output directly, but in an indirect way, by means of a replica of the output current: the final circuit has got two inputs and four current outputs. Of the two negative outputs, one is fed back to the input, while the other is fed to the load; the two positive outputs are put in parallel and fed back to the input after being converted to a voltage.

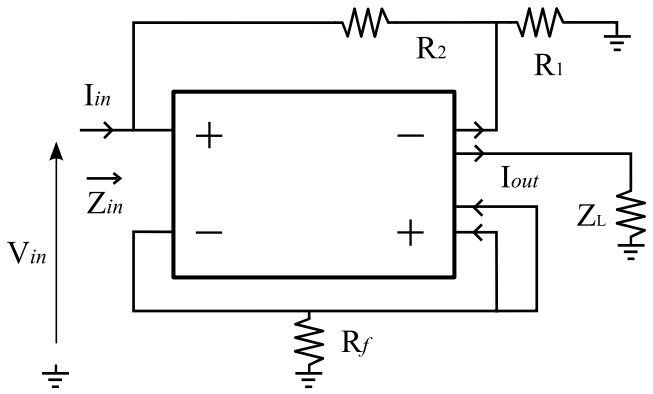


Figure 8.2: Dual loop indirect negative feedback power-to-current amplifier (basic configuration).

For the V-I loop, it holds:

$$\frac{I_{out}}{V_{in}} = -\frac{1}{2R_f} \tag{8.1}$$

For the I-I loop, the current gain can be expressed as:

$$\frac{I_{out}}{I_{in}} = -\frac{R_1 + R_2}{R_1 + 2R_f} \tag{8.2}$$

where R_f represents the V-I feedback resistor and R_1, R_2 are the current divider resistors. Hence, the input impedance can be defined as:

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{I_{out}}{I_{in}}\frac{V_{in}}{I_{out}} = \frac{R_1 + R_2}{R_1 + 2R_f} \cdot 2R_f \tag{8.3}$$

By proper selection of the feedback resistors, appropriate values for input impedance, power gain and noise figure can be designed. In fact, under the condition of sufficient input impedance match, it can be derived:

$$|S_{21}|^2 = \frac{P_{out}}{P_{in}} = \frac{I_{out}}{I_{in}}\frac{I_{out}}{V_{in}}Z_L = \frac{R_1 + R_2}{R_1 + 2R_f}\frac{1}{2R_f}Z_L \tag{8.4}$$

Z_L being the load impedance, usually equal to 50Ω. The resistors in the two feedback loops will contribute noise and have influence on the noise transfer. After shifting and combining all the noise sources, we arrive at the following expression for the total noise voltage power spectral density:

$$\begin{aligned} S_{v_n,eq} &= 4kTR_{n,s} + |R_s + R_f|^2 S_{i_n} + |1 + \frac{R_s}{R_2}|^2 S_{v_n} \\ &\quad +4kT\frac{R_s^2}{R_2} + 4kTR_f \end{aligned} \tag{8.5}$$

where S_{v_n} and S_{i_n} are the equivalent power of the voltage and current noise sources of the first stage of the nullor; $R_{n,s}$ is the noise resistance of the UWB antenna, approximately equal to antenna resistance R_s, 100Ω in our case, instead of the usual value of 50Ω. As it can be seen from Equation 8.5, if the value of R_f is decreased and the value of R_2 increased, the total noise power spectral density will be reduced. So in order to achieve low noise, R_f must be chosen as small as possible and R_2 as large as possible. However, some practical limitations arise. For instance, if R_f is too small, for the same input signal, more current needs to be delivered, which is likely to cause clipping distortion as the available current from the supply is limited. Based on simulation results $R_f = 5\Omega$, $R_2 = 910\Omega$ and $R_1 = 90\Omega$ have been found to offer a good compromise. The resulting values for power gain and noise figure will be shown in Section IV.

8.2 Nullor Design

The nullor is the critical part in our design, since parameters such as bandwidth, noise figure, distortion, will all depend on how good the nullor implementation is. For proper design of the first stage of the nullor, its noise performance is of prime importance. Furthermore, a high gain is required to suppress noise from other stages. Generally, a nullor comprises at least two stages (an input stage and an output stage), but in order to increase the loop gain and bandwidth, we can add more intermediate stages. Each stage will add gain and a dominant pole, so if more than three stages are used, frequency compensation will become very difficult, compromising the stability of the circuit.

Fig. 8.3 shows the circuit diagram of the nullor, which is composed by three stages, described in subsections *A* and *B*: the input stage realized by transistor M_1, the intermediate stage (transistor M_2) and the double output stage (transistors M_3 and M_4). In order to get a large gain, all stages are realized through common-source (CS) transistors. Additional stages used to obtain frequency compensation will be described later in the chapter.

8.2.1 Input Stage

The noise contribution of the active part of the LNA is minimized by optimizing the input stage of the nullor, i.e. defining geometry and bias current of its input transistor. Since the noise figure of the LNA reduces when the drain bias

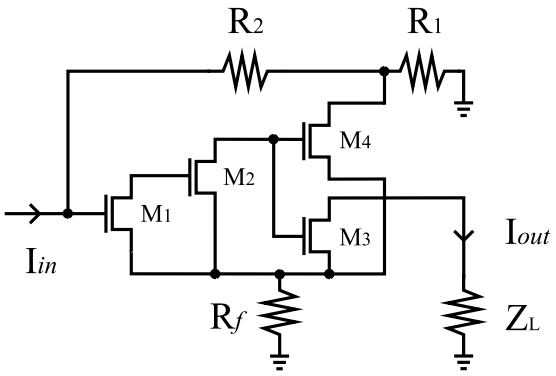


Figure 8.3: Dual loop indirect negative feedback power-to-current amplifier (circuit diagram, biasing not included).

current I_d of the first stage increases, in order to minimize the noise, I_d should be chosen as large as possible. Trading off noise figure for power consumption, we choose 4mA for the drain current of the first stage (transistor M_1). Since the gain of a transistor is proportional to its g_m, which, in strong inversion, in turn is proportional to W/L, W being the width of the transistor and L its length, we choose the minimum feature size 0.12μm for L. In weak inversion, the g_m of the transistor no longer depends on its width and as the parasitic capacitances still do, the gain of the transistor reduces again for increasing widths. As a consequence, the NF increases again. As a compromise, we choose W=100μm.

8.2.2 Intermediate and Output Stage

For the two indirect output stages (transistor M_3 and M_4), like for the input stage, in order to have a large gain, we use CS stages. The width of each transistor equals $W = 100\mu$m; their bias current equals 3.5mA. To increase the loop gain, we add one intermediate CS stage, transistor M_2, whose width W is equal to 100μm and bias current equal to 3mA.

8.2.3 Frequency Compensation

Employing phantom zeros is an efficient way to do frequency compensation [81]: their characteristic property is that, though implementing a zero in the loop gain, they are not present in the system transfer function. Phantom zeros are mostly placed near the band edge. Hence, their influence on noise and distortion is only noticeable beyond the band of interest. The zero is either realized in the feedback network, or at the input or at the output. For three stages, in order to do proper frequency compensation, two phantoms zero are

required or one phantom zero and an additional frequency compensation measure. From hand calculations and circuit simulations, employing a phantom zero at the input or at the output proves to be ineffective. Since the LNA has two feedback loops, we thus have to implement any phantom zero in both loops. As the feedback element of the V-I loop is a resistor (R_f), we can only implement one phantom zero in the feedback path, by means of a series inductor. For the other (current) feedback loop, we implement the (same) phantom zero by means of a capacitor in parallel with R_2. Final values for these two components are set from simulations to: C_{comp}=50fF, L_{comp}=65pH.

8.2.4 Multipath Structure

Since, in general, two frequency compensation measures are required to compensate a third-order feedback system, next to the phantom zero, we need an additional measure. To this end, pole splitting, pole-zero cancelation or resistive broad-banding can be used [81]. Another technique, which turned to be very adequate for the proposed double-loop negative feedback power-to-current amplifier, is by adding an additional transistor connected between input and output, as in Fig. 8.4 (transistors M_5 and M_6, one transistor each feedback loop). We now obtain a *multipath* structure, composed by the parallel connection of the three-stage path discussed so far, and the additional common-gate stages, whose frequency responses have a dominant pole which lies at a much higher frequency than the dominant poles of the three stage path.

The parallel of the two signal paths operates as follows. At low frequencies the loop gain is delivered by the parallel of the two paths: as the gain of the three stage path is much larger, the loop gain is still mainly determined by this one. On the contrary, the additional stage is effective at higher frequencies, where the multipath transistor takes over, increasing the phase margin, thus ensuring stability.

8.3 Simulation Results

The final circuit diagram including biasing scheme, first-order models for the bondpad (bp), bondwires (bw) and antenna, is shown in Fig. 8.5. Biasing is realized employing three additional coupling capacitors, C_c, a biasing shunt resistor R_{sh}, a voltage source V_b and a simple current mirror with multiple current outputs, fed to the four transistors in the third-order path; the two multipath transistors are biased at $I_{\rm out1} - I_{\rm interm}$ each. The total bias current

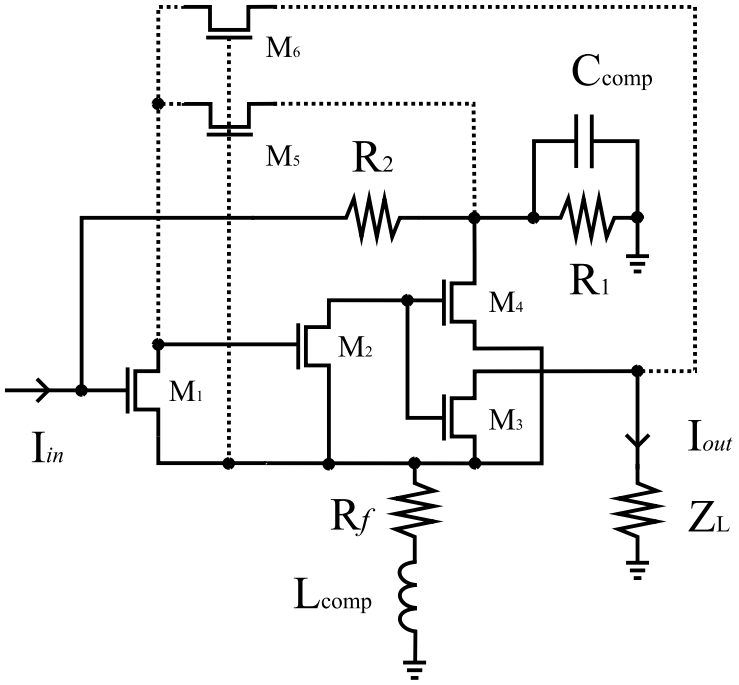


Figure 8.4: Amplifier signal diagram employing phantom zeros and multipath structure.

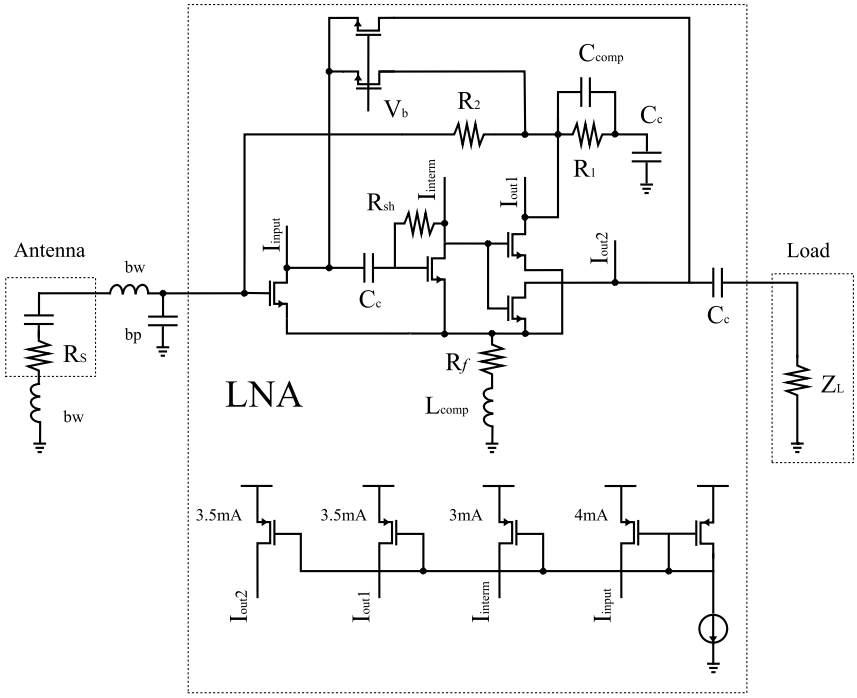


Figure 8.5: Final circuit with biasing.

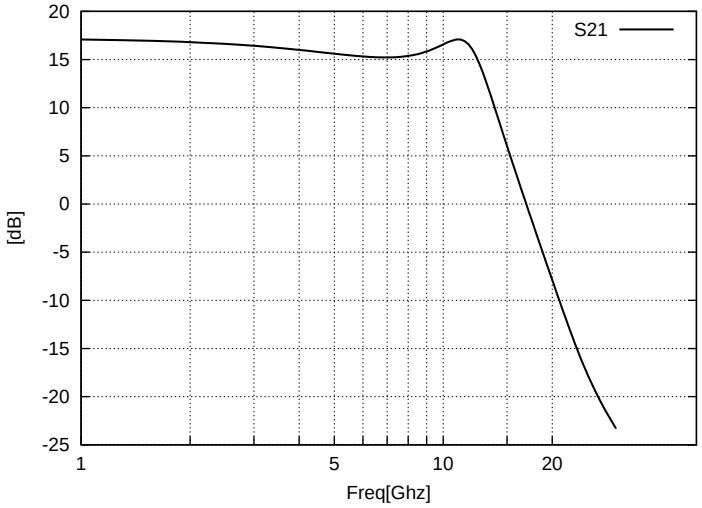


Figure 8.6: Forward transmission coefficient S_{21}.

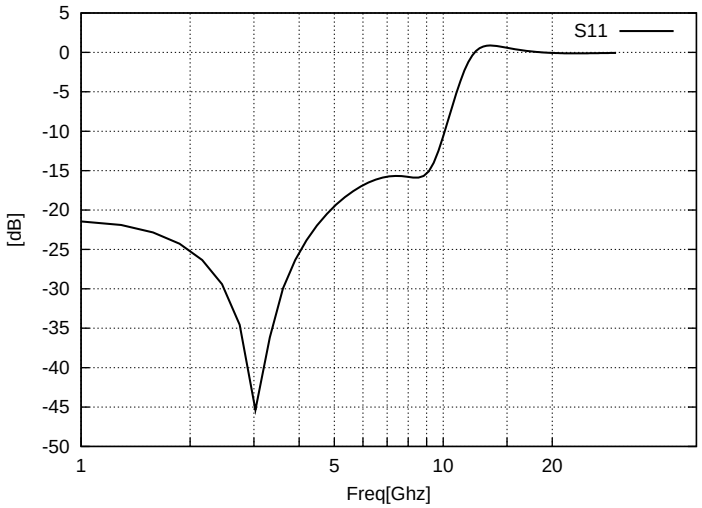


Figure 8.7: Input reflection coefficient S_{11}.

through the input stage equals $I_{\mathrm{input}} + 2(I_{\mathrm{out1}} - I_{\mathrm{interm}})$.

From circuit simulations, the following results are obtained: the bandwidth spans up to 12GHz, $S_{21} = 17$dB, $S_{11} < -10$dB up to 10GHz, NF<3dB up to 8GHz and NF<4dB at 10GHz and IIP3=-15.6dBm . Figures 8.6, 8.7 and 8.8 show the forward transmission coefficient, S_{21}, the input reflection coefficient, S_{11} and the noise figure, NF, as a function of frequency. In Tab. 8.1, a comparison with previous UWB LNA designs is made. We can state that our work is one of the most advanced LNA solutions for UWB applications due to its

Table 8.1: Comparison with recently reported state-of-the-art UWB LNA

	Tech.	S_{11}[dB]	S_{21}[dB]	B[GHz]	NF_{min}[dB]	Power[mW]	$IIP3$[dBm]
This work	0.13 CMOS	< -10	17	3-12	2@5GHz	16.8	-15.6@7GHz
[80]	0.18 SiGe	< 9.6	21	2.2-8	2.5@5GHz	30	-1@5GHz
[82]	0.13 CMOS	-	16.5	2.2-10.6	2@5GHz	9	-5.1@8GHz
[83]	0.18 SiGe	< -9.9	9.3	2.6-11.7	4@6GHz	9	-15@6GHz
[84]	0.25 SiGe	-	10	4-6	4.5@5GHz	3.5	-10@5GHz
[85]	0.18 SiGe	-	20.3	0.1-13.6	1.8@6GHz	26	2.1@6GHz
[86],[87]	0.18 CMOS	-	8.5	2.8-10.8	4.4@10GHz	4.5	8.3@10GHz

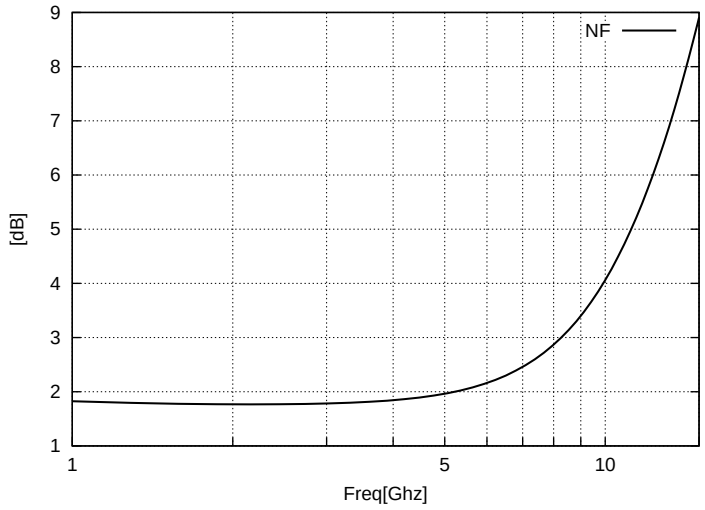


Figure 8.8: Noise Figure.

wide-band features.

8.4 Conclusion

An UWB dual-loop negative-feedback low-noise amplifier to be implemented in UMC 0.13μm CMOS technology has been presented. The use of a dual-loop negative feedback topology is advantageous, since it allows to achieve both impedance matching and a very low noise figure, as well as the possibility of saving a lot of chip area as no bulky inductors are needed.

A nullor and a resistive feedback network are employed, and the values of the feedback elements involved are defined in order to fulfill the noise-figure, input impedance and power-gain requirements for an UWB receiver. To ensure circuit stability, frequency compensation is done by means of a phantom zero and the addition of a transistor connected between input and output, thus realizing a *multipath* structure.

The design targets UMC 0.13μm CMOS IC technology and operation from a 1.2-volt supply. From circuit simulations, the power gain equals 17dB over a bandwidth up to 12GHz with a noise figure smaller than 4dB. S_{11} is below -10dB from very low frequencies up to 10GHz. Since the supply voltage is 1.2V and the total current consumption is 14mA, the power consumption equals 16.8mW.

Compared to competitive solutions, using resonating load stages or LC ladder networks, this chip will be much smaller and cheaper; it will use standard CMOS technology, and achieve very low noise, high gain and wide band matching at reasonable power consumption.

Appendix A

Hardware Implementation of a Chaos-Based RNG

THIS APPENDIX starts from a general overview of discrete-time chaos theory, in particular focusing on the aspects under which a chaotic circuit can be analyzed as a Markov chain. Subsequently, it describes the hardware implementation of the Random Number Generator used in the prototypes described in chapters 4 and 5: to do so it overviews pipeline A/D converters, recognizing the similarity between a pipeline A/D converter stage and a chaotic map. For a detailed description of hardware implementation, along with the guidelines used in the design, the reader is referred to [88]. At the end of the chapter, it will be shown how the implemented chaotic map is suitable for playing the role of modulating signal both for slow and fast modulation in spread-spectrum clock generator.

A.1 Chaotic maps

Systems referred to as *chaotic maps* are 1-D discrete-time autonomous chaotic dynamical systems [89, 90, 91]. Consider the domain X and a nonlinear, non-invertible function $M : X \rightarrow X$. These system are dynamical since they have memory of the past; the domain X of M is called the *state space* of the transformation.

Starting from an initial point $x_0 \in X$, the successive states at times $1, 2, 3, \ldots$, are given by the trajectory $x_1, x_2, x_3, \ldots$, where

$$x_{k+1} = M(x_k) \tag{A.1}$$

for $k = 0, 1, 2, \ldots$.

In these systems, like in any chaotic systems, the observation of chaotic trajectories is difficult and brings very little information, because a slight change in the initial state gives rise to a substantially different evolution of the system. Typically, few iterations are sufficient to make the new trajectory almost uncorrelated from the previous one so that any error in the knowledge of the state results in the impossibility to predict the position in the state space.

To cope with this problem, it is usual to consider a different approach, i.e. a probabilistic approach. However, before introducing the main operators used in the classical analysis, it is necessary to remind some definitions.

Denote with M^k the k-th iterate of M, so that for any set $Y \subseteq X$, $M^k(Y)$ is the set $\left\{y \in X \,|\, y = M^k(x) \wedge x \in Y\right\}$ and $M^{-k}(Y)$ is the set $\left\{x \in X \,|\, y = M^k(x) \wedge y \in Y\right\}$. Indicate with $\mathcal{A}$ a σ-algebra of subsets of X and with μ a measure on $\mathcal{A}$. The triple $(X, \mathcal{A}, \mu)$ is called a measure space. Moreover, if $\mu(X) = 1$, then $(X, \mathcal{A}, \mu)$ will be named a *probability space*. With regard to a measure space $(X, \mathcal{A}, \mu)$, a map $M : X \to X$ is said to be

1. *nonsingular*, if $\mu\left(M^{-1}(Y)\right) = 0$ for all sets $Y \in \mathcal{A}$ such that $\mu(Y) = 0$;
2. *measure-preserving*, if $\mu\left(M^{-1}(Y)\right) = \mu(Y)$ for any set $Y \in \mathcal{A}$.

A measure-preserving transformation is necessarily nonsingular.

A.1.1 The Perron-Frobenius Operator

Assume that the initial state x_0 is a random variable drawn according to a (probability) density $\rho_0 : X \to \mathbb{R}^+$. If the map is iterated, a new random variable $x_1 = M(x_0)$ is obtained and a link exists between ρ_0 and the (probability) density ρ_1 associated to it

$$\rho_1(x) = \frac{d}{dx} \int_{M^{-1}([0,x])} \rho_0(\xi)\, d\xi$$

Indicate with $\mathbb{L}_1$ the space of all the Lebesgue integrable functions $\phi : X \to \mathbb{C}$ and with $\|\cdot\|_1 = \int_X |\cdot|$ the associated $\mathbb{L}_1$ norm, and consider a measure space $(X, \mathcal{A}, \mu)$, where μ is the Lebesgue measure.

DEFINITION 1. If M is a nonsingular map, the unique operator $\mathbf{P} : \mathbb{L}_1 \to \mathbb{L}_1$ defined by

$$[\mathbf{P}\phi](x) = \frac{d}{dx} \int_{M^{-1}([0,x])} \phi(\xi)\, d\xi = \int_X \phi(\xi)\, \delta(M(\xi) - x)\, d\xi$$

is called the *Perron-Frobenius Operator* (PFO) corresponding to M.

The PFO **P** is a functional linear operator characterized by the following properties [90, 92]:

$$\mathbf{P} \text{ is positive, i.e. } \mathbf{P}\phi \geq 0, \text{ if } \phi \geq 0 \tag{A.2}$$

$$\mathbf{P} \text{ conserves } \|\cdot\|_1, \text{ i.e } \int_X |[\mathbf{P}\phi](x)|\, dx = \int_X |\phi(x)|\, dx \tag{A.3}$$

$$\text{The PFO corresponding to } M^k \text{ is } \mathbf{P}_k = \mathbf{P}^k \tag{A.4}$$

Properties (A.2) and (A.3) assure that the PFO maps density functions into density functions so that the restriction of the PFO to the set $\mathbb{D}(X)$ of probability densities defined on X can be considered. Property (A.4) assures that the PFO associated with the k-th iterate of the map is the k-th successive application of the PFO associated to M. If the initial condition x_0 of the map is drawn according to ρ_0, its state after k iterations is regulated by the density

$$\rho_k = \mathbf{P}\rho_{k-1} = \mathbf{P}^k\rho_0$$

For all the maps considered here, and for k large enough, the density $\rho_k = \mathbf{P}^k\rho_0$ converges to a final density $\overline{\rho}$ independently of ρ_0. Such a final density must be a *fixed point* of the PFO associated to it, i.e.

$$\mathbf{P}\overline{\rho} = \overline{\rho}.$$

This is usually expressed by saying that $\overline{\rho}$ is the *invariant density* of the map. Moreover, $\mathbf{P}\overline{\rho} = \overline{\rho}$ if and only if the measure $d\overline{\mu} = \overline{\rho}dx$ is invariant under M [90, 92] and $\overline{\mu}$ is referred as the *invariant measure* of the map.

A.1.2 Ergodic, Mixing and Exact Maps

The existence of a unique invariant density $\overline{\rho}$ is linked to particular properties of M.

DEFINITION 2. Consider a measure space $(X, \mathcal{A}, \mu)$. A nonsingular map $M : X \to X$ is said to be *ergodic* if every invariant set $Y \in \mathcal{A}$ is a trivial subset of X, i.e., if either $\mu(Y) = 0$ or $\mu(X \backslash Y) = 0$.

A set Y is an *invariant set* if $M(Y) = Y$. The above definition states that in an ergodic map, no invariant sets other than X can exist; X is also called *principal invariant set*. The following theorem links ergodicity with the existence of $\overline{\rho}$.

THEOREM 1. *Let $(X, \mathcal{A}, \mu)$ be a measure space, M a nonsingular transformation, and **P** the PFO associated to M. If M is ergodic, then there is at most one invariant density $\overline{\rho}$ for **P**. Furthermore, if there is a unique invariant density $\overline{\rho}$ of **P** and if $\overline{\rho}(x) > 0$ almost everywhere, then M is ergodic.*

DEFINITION 3. A map $M : X \to X$ is called piecewise C^2 if it exists a sequence of points $0 = y_0 < y_1 < \cdots < y_n = 1$ in X such that for any $j = 1, \ldots, n$ the restriction of M to the open interval $]y_{j-1}, y_j[$ is a C^2 function which can be extended to the corresponding closed interval $[y_{j-1}, y_j]$ remaining of class C^2. M does not need be continuous at the points y_j.

DEFINITION 4. Consider a probability space $(X, \mathcal{A}, \mu)$ and a measure preserving transformation M. M is called *mixing* if for any $Y_1, Y_2 \in \mathcal{A}$ one has that $\lim_{n\to\infty} \mu(Y_1 \cap M^{-n}(Y_2)) = \mu(Y_1)\mu(Y_2)$.

For a mixing map $\mu\left(Y_1 \cap M^{-n}\left(Y_2\right)\right)/\mu\left(Y_2\right) \to \mu\left(Y_1\right)$ as $n \to \infty$. The first term is the probability (according to μ) that a typical system trajectory arrives in Y_1 after n time steps, given that it starts in Y_2 while the second term simply represents the probability that a typical trajectory is in Y_1. It follows that for large n the two events $\{x \in Y_2\}$ and $\{M^n\left(x\right) \in Y_1\}$ become statistically independent.

A mixing map is also ergodic but has a much more complicated behavior; in fact it is common to indicate as chaotic only those maps which are at least mixing. Additionally, for a mixing map, it can be proven that

$$\left\|\mathbf{P}^k \rho_0 - \overline{\rho}\right\|_{BV} \leq H \left\|\rho_0\right\|_{BV} r_{\mathrm{mix}}^k$$

for a suitable constant $H > 0$ [93] and a suitable defined bounded variation norm $\|\cdot\|_{BV}$ [90] so that if the initial condition of a mixing map is randomly chosen according to a bounded variation density ρ_0, then the state x_k distributes according to a density $\mathbf{P}^k\rho_0$ which converges to the invariant one at an exponential rate r_{mix} (called *rate of mixing*) in the bounded variation norm.

Finally, some noninvertible transformations may possess a stronger form of mixing, which is called exactness [90].

DEFINITION 5. Consider a probability space $(X, \mathcal{A}, \mu)$ and a measure preserving transformation $M : X \to X$. M is called *exact* if $\lim_{n\to\infty} \mu\left(M^n\left(Y\right)\right) = 1$ for any $Y \in \mathcal{A}$ with $\mu\left(Y\right) > 0$.

It can be proven that exact maps are also mixing; the chaotic maps that found practical applications usually are exact maps.

A.1.3 Markov Chains and PWAM Maps

In mathematics, a Markov chain, named after the Russian mathematician Andreyevich Markov, is a discrete-time stochastic process with the Markov property, that is, briefly speaking, the property of a process to keep memory only of the last realization (i.e. memory-1 property).

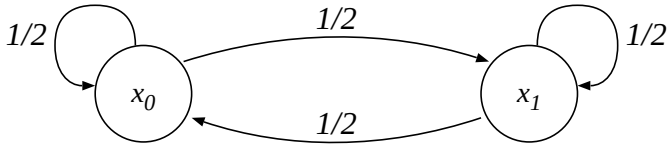


Figure A.1: Example of Markov chain.

For the scope of this chapter, it is enough to consider a finite Markov chain, that is a finite-state machine, where transition from one state to another, as well as the possibility to rest in the same state, is regulated by a stochastic process.

The Markov property ensure that the conditional probability distribution of a state in the future can be deduced using only the current state; no additional information is given by the knowledge of the past evolution. In other words, the past states does not carry any information about future states.

A Markov chain is usually depicted as in Figure A.1, where two states x_0 and x_1 are present, and all the possible transitions between the states are indicated with an arrow, and by the probability associated to this transition. This is the Markov chain that describes the fair coin toss, where, for example, being in the state x_0 correspond to the outcome "head" of the toss, while the state x_1 is associated to the outcome "tail". Every time we toss the coin, i.e. every time the finite-state machine may change the state, the probability to stay in the same state, i.e. to get the same outcome of the previous coin toss, or the probability to change state, i.e. to have an outcome different from the previous one, are both equal to $p = 1/2$.

Note that every Markov chain can be expressed as a stochastic matrix which is a square matrix each of whose rows consists of nonnegative real numbers and sums to 1. Each state of the Markov chain is associated to a row of the matrix; each element of the row is the conditioned probability to be in the state associated to the row, and have a transition towards one of all the possible states. The stochastic matrix associated to the Markov chain of the example is

$$\boldsymbol{P} = \begin{pmatrix} \frac{1}{2} & \frac{1}{2} \\ \frac{1}{2} & \frac{1}{2} \end{pmatrix}$$

The goal of this subsection is to introduce a particular class of chaotic maps whose behavior can be described as a Markov chain.

DEFINITION 6. A map $M : X \to X$ is said to be a Piece-Wise Affine Markov (PWAM) map with respect to a given partition $\mathcal{X}_n = \{X_1, X_2, \ldots, X_n\}$ if the intervals X_j are such that M is affine on each X_j and that for any couple of indices j and k, either $X_k \subseteq M(X_j)$ or $X_k \cap M(X_j) = \emptyset$.

Under the assumption of an exact PWAM map, if one limits himself to initial probability densities ρ_0 which are stepwise in $\mathcal{X}$, all subsequent probability ρ_k densities are then compelled to be stepwise on the interval partition. Note that this analysis is not restrictive, since also $\overline{\rho}$ is compelled to be stepwise, and for ergodic maps the existence of a unique invariant density has been proved.

Consider a partition $\mathcal{X}_n$ and indicate as Σ_n the n-dimensional subspace of $\mathbb{L}_1$ generated by χ_{X_j}. Any function φ step-wise in $\mathcal{X}$ is belonging to Σ_n, and can be expressed as a n-dimensional vector $\boldsymbol{\varphi} = (\varphi_1, \ldots, \varphi_n)$ with respect to the basis $\left\{\chi_{X_j}, X_j \in \mathcal{X}_n\right\}$. Then, define the $x \times n$ matrix $\boldsymbol{\mathcal{K}}$ as

$$\boldsymbol{\mathcal{K}}_{j_1,j_2} = \frac{\mu\left(X_{j_2} \cap M^{-1}(X_{j_1})\right)}{\mu\left(X_{j_2}\right)}$$

This is often referred to as the *kneading matrix* since its entry in the j_1-th row and j_2-th column records the fraction of X_{j_2} that is mapped into X_{j_1}. It follows that $\boldsymbol{\mathcal{K}}$ is a stochastic matrix that can be used to express the evolution of density step-wise in $\mathcal{X}_n$ starting from an arbitrary $\boldsymbol{\varphi}_0$:

$$\boldsymbol{\varphi}_{k+1} = \boldsymbol{\mathcal{K}}\boldsymbol{\varphi}_k$$

In other words, $\boldsymbol{\mathcal{K}}$ can be interpreted as the restriction of $\mathbf{P}$ into the finite-dimensional subspace Σ_n. The invariant density $\overline{\boldsymbol{\varphi}}$ can be simply computed as $\overline{\boldsymbol{\varphi}} = \boldsymbol{\mathcal{K}}\overline{\boldsymbol{\varphi}}$, i.e. it is given by the right eigenvector $\mathbf{e} = (e_1, \ldots, e_n)$ of $\boldsymbol{\mathcal{K}}$ with unit eigenvalue.

Note that, supposing that the state x_k at the time step k is in X_j, and neglecting the exact knowledge of x_k, the j-th row of $\boldsymbol{\mathcal{K}}$, by definition, represents the probability that the following state x_{k+1} belongs to any intervals of $\mathcal{X}_n$. This means that the evolution of the map, when considering only the interval of $\mathcal{X}_n$ where the state is, i.e. the evolution of the system in Σ_n, can be modeled by the Markov chain associated to the stochastic matrix $\boldsymbol{\mathcal{K}}$. Note also that this is not an approximation of the evolution of the map, but comes from the exact analysis of the restriction of the evolution of the system in Σ_n.

Finally, the method to determine the exactness of PWAM maps relies on the following theorem [94].

THEOREM 2. *If M is a PWAM map and its kneading matrix is* primitive, *i.e., an integer l exists such that $\overline{\boldsymbol{\mathcal{K}}}^l$ has no null entries, then M is exact.*

A.2 ADC-based Chaotic Map

A pipeline A/D converter belongs to the category of successive approximation converters, in which the mapping between the analog input and the digital

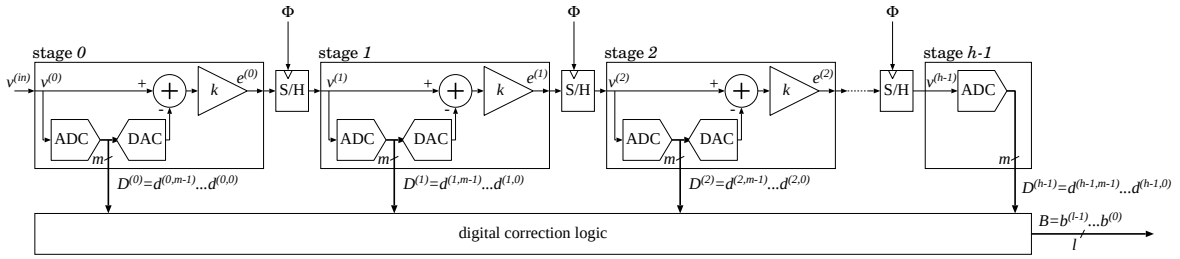


Figure A.2: Basic structure of a pipeline ADC.

output is completed in more than one step, exploiting a binary search of the digital value closer to the input analog quantity. In particular, in pipeline converters this is done by performing a series of h coarse intermediate conversions over different hardware blocks at different time steps [95].

The typical structure of these converters is presented in Figure A.2, depicting a h-stages converter which provides a representation of an input variable $v^{(in)}$ defined on an interval X into a l-bits numerical notation. Note that, even if this is supposed in this dissertation, it is not strictly necessary that all stages are identical; in particular the last stage, having nothing downhill, always presents a simpler structure and it is usually composed by a simple flash converter.

The i-th stage computes, usually with a small and fast flash converter, a *coarse* m-bit representation $D^{(i)} = d^{(i,m-1)} \dots d^{(i,0)}$, of its input $v^{(i)}$ sampled at the time step n, and then calculates (and rescales) an analog *error conversion* $e^{(i)}$ to be passed at the time step $n+1$ to the following stage $(i+1)$-th as its input $v^{(i+1)}$.

In this design, only the first stage provides a direct conversion of the input $v^{(in)} \equiv v^{(0)}$; all other stages provide a representation of the intermediate conversion errors. Since the conversion error $e^{(i)}$ of the stage i is bounded in an interval smaller than X, it is sensible to rescale it before passing it to the next stage as $v^{(i+1)}$ in order to let every $v^{(i)}$ span the whole available range X. Note that this is a necessary condition for having identical stages; otherwise no additional information about the conversion can be retrieved from all stages beyond the first. Then, a *digital correction logic* processes the digital outputs of all the h stages in order to retrieve the l bits $b^{(l-1)} \dots b^{(0)}$ of the conversion, with $l \leq h \cdot m$.

It is easy to see that if $k = 2^m$ (e.g. $m = 2$ bits, $k = 4$), then the conversion is done exactly as in a SAR *(Successive Approximation Register)* converter, and the conversion word is obtained just by collecting in the right order all the intermediate conversion bits, with $l = h \cdot m$. However in the general case, $k < 2^m$

and the number of significative bits l in the conversion is smaller then the total number of computed bits $h \cdot m$; this means that there is a sort of *redundancy*. This redundancy, associated to a proper correction logic (hence, the name "digital correction logic") can be used to relax some constraints about the accuracy in the circuital implementation.

For this reason, the maximum number of stages in the pipeline (the higher the number of stages used, the higher the resolution of the converter) is not limited by the accuracy of the implementation but by the noise. In particular the noise introduced by the first stage, that passes through and is amplified by all stages, is the main factor in the determination of the maximum number of stages. In practical cases, the number of stages is limited to 8–10.

One major advantage of this approach is that the flow of information can be synchronized exactly as in a digital pipeline. Since the various stages are separated by *sample and hold* blocks (S/Hs), every stage is free to start operating on the next piece of data as soon as the following S/H has stored the rescaled conversion error. This permits to increase the throughput of the system up to the inverse of the latency of a *single* stage, which is much larger than the inverse of the time needed by the *whole* conversion, at the cost of an increasing complexity of the digital correction logic, which has to process data coming from different time instants.

One of the most used configuration for pipeline A/D converters is the so-called *one bit and a half* per stage [96, 97]. In this arrangements, supposing X the normalized interval $X = [-1, 1]$, the A/D conversion function $Q(x)$ employed at each stage is:

$$Q(x) = \begin{cases} -1, & \text{for} \quad x < -\frac{1}{2} \\ 0, & \text{for} \quad -\frac{1}{2} \leq x < \frac{1}{2} \\ +1, & \text{for} \quad x \geq \frac{1}{2} \end{cases}$$

Obviously, to represent this three-level quantization function, at least two bits are required. Usually the conversion is obtained by confronting $v^{(i)}$ with the two values $\pm 1/2$ by means of two comparators; it is common to take a thermometric coding for $D^{(i)}$, so that each $d^{(i,j)}$ is the output of a comparator:

$$D^{(i)} = d^{(i,1)} d^{(i,0)} = \begin{cases} 00, & \text{for} \quad v^{(i)} < -1/2 \\ 01, & \text{for} \quad -1/2 \leq v^{(i)} < 1/2 \\ 11, & \text{for} \quad v^{(i)} \geq 1/2 \end{cases} \tag{A.5}$$

Hence, $e^{(i)} = k\left(v^{(i)} - Q\left(v^{(i)}\right)\right)$, so if $v^{(i)}$ spans in $X = [-1, 1]$, then $e^{(i)}$ spans in $[-k/2, k/2]$. To take full advantage from this architecture, the rescaler has to be set with a gain equal to $k = 2$, so all the $v^{(i)}$ take values in the same range as

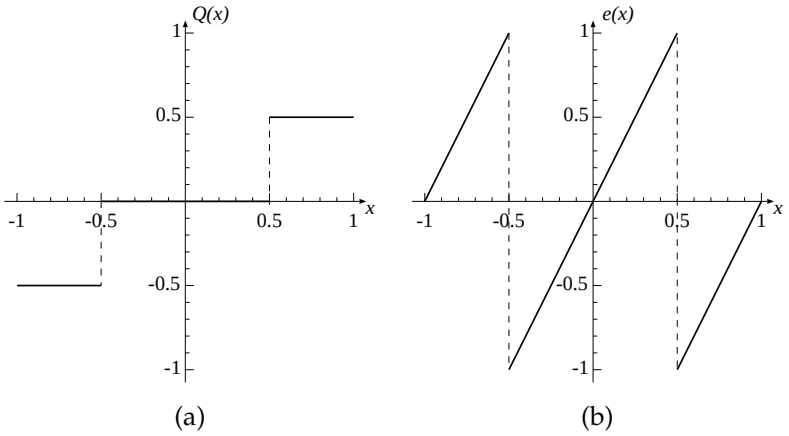


Figure A.3: (a) Quantization function $Q\left(x\right)$; and (b) error function $e\left(x\right)$ of the 1.5 bits A/D converter.

$v^{(in)}$:

$$e\left(x\right)=\begin{cases}2x+2, & \text{for} \quad x<-\frac{1}{2}\\ 2x, & \text{for} \quad -\frac{1}{2}\leq x<\frac{1}{2}\\ 2x-2, & \text{for} \quad x\geq\frac{1}{2}\end{cases} \tag{A.6}$$

The conversion function $Q\left(x\right)$ and the error function $e\left(x\right)$ are reported in Figure A.3.

Actually, the error function $e\left(x\right)$ of Figure A.3b fulfills all the requisites for being used in the implementation of a PWAM map, with $M\left(x\right)=e\left(x\right)$ [98], assuming a Markov partition $\mathcal{X}=\{X_0,X_1,X_2,X_3\}$ equal to

$$\mathcal{X}=\left\{\left[-1,-\frac{1}{2}\right),\left[-\frac{1}{2},0\right),\left[0,\frac{1}{2}\right),\left[\frac{1}{2},1\right]\right\}.$$

The kneading matrix $\mathcal{K}$ and the four-state Markov chain associated to this map (referring to state x_0 if $x\in X_0$, x_1 if $x\in X_1$ and so on) are shown in Figure A.5a and b, respectively.

A.2.1 Chaos-based random number generator (RNG) suitable for FM-slow modulation

The right eigenvector $\overline{\varphi}$ of $\mathcal{K}$ can be computed as:

$$\overline{\varphi}=\left(\frac{1}{4},\frac{1}{4},\frac{1}{4},\frac{1}{4}\right)$$

that means that the probability for x_k to be in each of the intervals of $\mathcal{X}$ is the same. It follows that the stepwise invariant density $\overline{p}$ of the map is *uniform* over

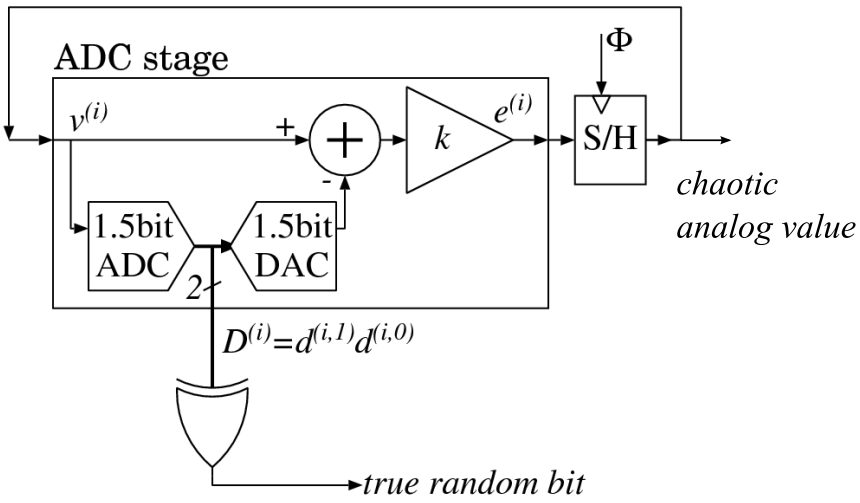


Figure A.4: Complete arrangement for achieving a random bit generator from a 1,5 bit A/D stage.

the whole definition set X, i.e.:

$$\overline{\rho} = \begin{cases} 1/2, & \text{if } -1 \leq x \leq 1 \\ 0, & \text{otherwise} \end{cases}$$

Now, it is intuitive how a single 1.5 bits ADC stage can be used as a chaotic number generator; it is sufficient to directly close the output in a loop onto the input including a unity-delay block (that can be the S/H stage present in-between every stage of the pipeline) to achieve the dynamic behavior:

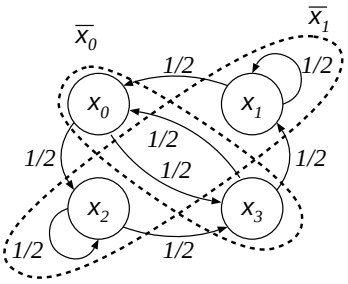
$$v^{(i)}\left((k+1)\,T\right) = e\left(v^{(i)}\left(kT\right)\right)$$

that is the same behavior as (A.1), where the time steps $k, k+1, \ldots$ are substituted by the sampling instants $kT, (k+1)\,T, \ldots$.

Notice how the chaotic analog output in fig. A.4 is constituted by analog values that are uniformly distributed in the interval [-1,1] but not *independent*: that is, it is not a truly i.i.d. true-random signal.

Anyway, the same signal, which in chapter 2 has been referred to as $\xi(t)$, is still suitable for playing the role of *modulating signal* of a spread spectrum clock generator implementing a *slow* modulation. In the case of *slow* modulation, in fact, analytical results have been presented showing how an optimum peak reduction can be obtained with a chaos-based modulating signal, only depending on the probability density function (PDF) $\overline{\rho}$ of the modulating signal: being this PDF uniform, the correspondent spread spectrum will be flat.

$$\mathcal{K} = \begin{pmatrix} 0 & 0 & \frac{1}{2} & \frac{1}{2} \\ \frac{1}{2} & \frac{1}{2} & 0 & 0 \\ 0 & 0 & \frac{1}{2} & \frac{1}{2} \\ \frac{1}{2} & \frac{1}{2} & 0 & 0 \end{pmatrix}$$



(a) (b)

Figure A.5: (a) Kneading matrix associated to the ADC-based chaotic map; and (b) associated Markov chain.

A.2.2 Chaos-based digital random number generator suitable for FM-fast modulation

A digital RNG can easily be obtained from the quantization of the output of an analog RNG. In the following we will show a quantization method to get a digital random output starting from the analog RNG described in the previous subsection: even if it is not the most intuitive, it gives the advantage to generate symbols which are *independent*.

Due to the particular structure of the Markov chain associated to the map, it is possible to *aggregate* the states of the graph two by two, as shown in dotted lines in fig. A.5b. If we introduce the two macro-states $\overline{x_0}$ and $\overline{x_1}$, respectively $\overline{x_0}$ corresponding to the system being either in x_0 or x_3, while $\overline{x_1}$ corresponding to the system being either in x_1 or x_2, the resulting diagram is identical to the ideal coin toss diagram.

In order to evaluate whether the system is in macro-state $\overline{x_0}$ or $\overline{x_1}$, it is sufficient to look at the digital outputs of the converter stage. In fact, the partition $\mathcal{X}$ is partially coincident with the quantization intervals of (A.5). For determining the macro-state, it is sufficient to take the exclusive-or between $d^{(i,1)}$ and $d^{(i,0)}$, as summarized by Table A.1. The complete arrangement is illustrated in Figure A.4.

Notice how the true random bit in fig. A.4 is constituted by digital values that are independent and identically distributed (i.i.d.): that is, it is a true-random signal.

The same signal, which in chapter 2 has been referred to as $\xi(t)$, is then suitable for playing the role of *modulating signal* of a spread spectrum clock generator implementing a *fast* modulation. In the case of *fast* modulation, in fact, numerical optimization has been presented showing how an optimum peak

$d^{(i,1)}, d^{(i,0)}$	partition interval	state	macro-state
00	X_0	x_0	$\overline{\mathsf{x}_0}$
01	X_1 or X_2	x_1 or x_2	$\overline{\mathsf{x}_1}$
11	X_3	x_3	$\overline{\mathsf{x}_0}$

Table A.1: Markov interval for the ADC based map and corresponding associated states and macro-states.

reduction can be obtained with a digital modulating signal whose symbols are i.i.d.

Publications

International Conference Publications

[1] LUCA ANTONIO DE MICHELE, Wouter A. Serdijn and Sumit Bagga, Gianluca Setti and Riccardo Rovatti "An UWB CMOS 0.13um Low-Noise Amplifier with Dual Loop Negative Feedback", to appear in *Proceedings of 2008 IEEE International Symposium on Circuits and Systems* (ISCAS2008). Seattle, Washington, (USA), May 18–21 2008.

[2] LUCA ANTONIO DE MICHELE and Giampaolo Cimatti, Riccardo Rovatti, Gianluca Setti "Joint Design of a DS-UWB Modulator and Chaos-Based Spreading Sequences for Sensor Networks", in *Proceedings of 2007 IEEE International Symposium on Circuits and Systems* (ISCAS2007), pp. 1441–1444. New Orleans (USA), May 27–30, 2007.

[3] LUCA ANTONIO DE MICHELE, Fabio Pareschi, Riccardo Rovatti, and Gianluca Setti "3 GHz Spread Spectrum Clock Generator for Serial ATA-II using Random Frequency Modulation", in *Proceedings of 2006 International Symposium on Nonlinear Theory and its Applications* (NOLTA2006), pp. 635–638. Bologna (Italy), September 11–14, 2006.

[4] LUCA ANTONIO DE MICHELE, Fabio Pareschi, Riccardo Rovatti, and Gianluca Setti, "Chaos-based High-EMC Spread-Spectrum Clock Generator", in *Proceedings of 17th IEEE European Conference on Circuit Theory and Design* (ECCTD 2005), pp. 165–168. Cork (Ireland), August 29 – September 2, 2005. ***Winner of the best paper award.***

[5] Fabio Pareschi, LUCA ANTONIO DE MICHELE, Riccardo Rovatti, and Gianluca Setti, "A PLL-based clock generator with improved EMC", in *Proceedings of 16th IEEE International Zurich Symposium on Electromagnetic Compatibility* (EMCZurich2005), pp. 367–372. Zurich (Swiss), February 13–18, 2005. ***Winner of the best student paper award.***

[6] LUCA ANTONIO DE MICHELE, Fabio Pareschi, Riccardo Rovatti, and Gianluca Setti, "A chaos-driven PLL based spread spectrum clock generator", in *Proceedings of 2004 International Symposium on Nonlinear Theory and its Applications* (NOLTA2004), pp. 251–254. Fukuoka (Japan), November 29 – December 3, 2004.

Bibliography

References are organized in sections clustering them into homogeneous topics. Within each section, references are sorted in order of citation.

EMI Reduction Related References

[7] J.P. Costas, "Poisson, Shannon, and the Radio Amateur" *Proc. of the IRE*, vol. 47, iss. 12, pp. 2058-2068, Dec. 1959.

[8] IEC50 (161): (BS4727 : Pt 1 : Group 09) Glossary of electrotechnical, power, telecommunication, electronics, lighting and colour terms: Electromagnetic compatibility; IEC 61000: Electromagnetic compatibility.

[9] National Archives and Records Administration's Office, Code of Federal Regulations. 47 (47CFR), part 15, subpart B: "Unintentional Radiators"

[10] H. S. Black, *Modulation Theory*, Van Nostrand, 1953.

[11] C. Christopoulos, "Electromagnetic Compatibility – Part I: General Principles," IEE Power Enginnering Journal., vol. 6, pp. 89-94, 1992

[12] C. Christopoulos, "Electromagnetic Compatibility – Part II: Design Principles," IEE Power Engineering Journal, vol. 6, pp. 239-247, 1992

[13] M. M. Bech, J. K. Pedersen, F. Blaabjerg, "Random modulation techniques for power conversion — an update," Proceedings of the 7th International Power Electronics and Motion Control Conference, vol. 3, (Budapest), pp. 357–365, 1996

[14] F. Lin, D. Y. Chen, "Reduction of Power Supply EMI Emission by Switching Frequency Modulation," IEEE Trans. on Power Electronics, vol. 9, pp. 132-137, 1994

[15] K. B. Hardin, J. H. Fessler, D. R. Bush, J. J. Booth, "Spread Spectrum Clock Generator and Associated Method," U.S. Patent n. 5,488,627, 1996

[16] R. Rovatti, G. Setti, S. Graffi, "Chaos based FM of clock signals for EMI reduction", Proceedings of ECCTD99, vol. 1, (Stresa), pp. 373–376, Sept. 1999

[17] G. Setti, M. Balestra, R. Rovatti, "Experimental verification of enhanced electromagnetic compatibility in chaotic FM clock signals", Proceedings of IEEE ISCAS'00, vol. 3, (Lousanne), pp. 229–232, 2000

[18] A. M. Stankovic, G. C. Verghese, D. J. Perrault, "Analysis and synthesis of random modulation schemes for power converters", IEEE Transactions on Power Electronics, vol. 10, pp. 680–693, Nov. 1995

[19] A. Stankovic, H. Lev-Hari, "Randomized Modulation in Power Electronic Converters," Proceedings of the IEEE, pp. 782-799, 2002

[20] A.M. Stankovic, "Random Pulse Modulation with application to Power Electronic Converters," Ph.D. Thesis, MIT 1993

[21] G. Setti, G. Mazzini, R. Rovatti, S. Callegari, "Statistical Modeling of Discrete-Time Chaotic Processes: Basic Finite-Dimensional Tools and Applications", Proceedings of the IEEE, pp. 662–690, 2002

[22] A. Lasota, M.C. Mackey, *Chaos, Fractals, and Noise*, Springer-Verlag, 1994

[23] Serial ATA International Organization, "Serial ATA Revision 2.6", February 2007.

[24] J. D. Gibson (Ed.), "The Mobile Communications Handbook," IEEE Press, 1996

[25] J.G. Proakis, *Digital Communications*, McGraw-Hill, Singapore, 1983

[26] R. Rovatti, G. Setti, S. Callegari, "Limit Properties of Folded Sums of Chaotic Trajectories," IEEE Transactions on Circuits and Systems - Part I, 2003.

[27] S. Callegari, R. Rovatti, G. Setti, "Chaos based improvement of EMI compliance in switching loudspeaker drivers", Proceedings of ECCTD2001, vol. III, (Helsinki), pp. 421–424, 2001

[28] S. Callegari, R. Rovatti, G. Setti, "Spectral Properties of Chaos-Based FM Signals," IEEE Transactions on Circuits and Systems - Part I, pp. 1584-1597, 2003.

[29] G. Kolumban, P. K. Kennedy, and G. Kis, "Performance Evaluation of FMDCSK", *Chaotic Electronics in Telecommunications*, Boca Raton, FL: CRC, ch. 7, 2000.

[30] S. Santi, R. Rovatti, G. Setti, "Advanced chaos based frequency modulations for clock signal tuning" in *Proceedings of 2003 IEEE International Symposium on Circuits and Systems* (ISCAS2003), vol 3, pp 116–119. Bangkok (Thailand), May 25–28, 2003.

Hardware Implementation Related References

[31] R. E. Best, *Phase-locked Loops: Design, Simulation and Applications*, McGraw-Hill, 1999.

[32] K. Izawa, *Introduction to Automatic Control*, Elsevier, New York, 1963.

[33] Hsiang-Hui Chang, I-Hui Hua, Shen-Iuan Liu, "A Spread-Spectrum Clock Generator With Triangular Modulation", *IEEE J.Solid-State Circuits*, vol.38, no.4, April 2003

[34] H. S. Li, Y. C. Cheng, and D. Puar, "Dual-loop spread-spectrum clock generator", *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 184-185, 1999.

[35] J. Y. Michel and C. Neron, "A frequency modulated PLL for EMI reduction in embedded application", *Proc. IEEE Int. ASIC/SOC Conf.*, pp. 362–365, 1999.

[36] M. Sugawara *et al.*, "1.5-Gb/s 5150-ppm spread-spectrum SerDes PHY with a 0.3-mW 1.5-Gb/s level detector for serial ATA", *Symp. VLSI Circuits Dig. Tech. Papers*, pp. 60-63, June 2002.

[37] M. Kokubo, T. Kawamoto, T. Oshima *et al.*, "Spread-Spectrum Clock Generator for Serial ATA using Fractional PLL Controlled by $\Delta\Sigma$ Modulator with Level Shifter" *IEEE Intern. Solid-State Circuits Conf.*, pp. 160-161, 2005.

[38] H. Lee, O. Kim, G. Ahn, and D. Jeong, "A Low-Jitter 5000ppm Spread Spectrum Clock Generator for Multi-channel SATA Transceiver in 0.18 μm CMOS", *IEEE Intern. Solid-State Circuits Conf.*, pp. 162-163, 2005.

[39] Y. Moon, D. K. Jeong, and G. Kim, "Clock dithering for electromagnetic compliance using spread-spectrum phase modulation" *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 186-187, 1999.

[40] H. Mair and L. Xiu, "An architecture of high-performance frequency and phase synthesis" *IEEE Journal of Solid-State Circuits*, vol.35, no.6, pp. 835-846, June 2000.

[41] H. W. Chen and J. C. Wu, "A spread-spectrum clock generator for EMI reduction" *IEICE Trans. Electron.*, pp. 1959–1966, Dec. 2001.

[42] S. Kim *et al.*, "A 960-Mb/s/pin interface for skew-tolerant bus using low-jitter PLL", *IEEE J.Solid-State Circuits*, vol.32, pp. 691–700, May 1997

[43] Federal Communication Commission "FCC methods of measurement of radio noise emission from computing devices", *FCC/OST MP-4*, July 1987.

[44] International Special Committee on Radio Interference (CISPR), Publication 16-1, 2002.

[45] C. Park, B. Kim, "A Low-Noise, 900-MHz VCO in 0.6-μm CMOS", *IEEE Journal of Solid-State Circuits*, vol.34, no.5, pp. 573-579, May 1999.

UWB Related References

[46] L. Yang and G. B. Giannakis, "Ultra-Wideband Communication: An Idea Whose Time Has Come" *IEEE Sig. Proc. Mag.*, Nov. 2004

[47] S. Verdu, "Wireless bandwidth in the making", *IEEE Commun. Mag.*, vol. 38, no. 7, pp. 53-58, 2000.

[48] T.W. Barrett, "History of ultra wideband (UWB) radar and communications: Pioneers and innovators" *Proc. Progress in Electromagnetics Symposium*, Cambridge, MA, 2000.

[49] G.F. Ross, "The transient analysis of multiple beam feed networks for array systems" Ph.D. dissertation, Polytechnic Institute of Brooklyn, Brooklyn, NY, 1963.

[50] G.F. Ross and K.W. Robbins, "Base-band radiation and reception system", U.S. Patent 3,739,392, June 12, 1973.

[51] "Assessment of Ultra-Wideband (UWB) Technology", OSD/DARPA, Ultra-Wideband Radar Review Panel, R-6280, July 13, 1990.

[52] FCC First Report and Order: In the matter of Revision of Part 15 of the Commission's Rules Regarding Ultra-Wideband Transmission Systems, FCC 02-48, April 2002.

[53] S. Tilak, N.B. Abu-Ghazaleh, and W. Heinzelman, "A taxonomy of wireless micro-sensor network models", *Mobile Computing Commun. Rev.*, vol. 6, no. 2, pp. 28-36, 2002.

[54] I.F. Akyildiz, W. Su, Y. Sankarasubramaniam, and E. Cayirci, "A survey on sensor networks" *IEEE Commun. Mag.*, vol. 40, no. 8, pp. 102-114, 2002.

[55] E.M. Staderini, "UWB radars in medicine", *IEEE Aerosp. Electron. Syst. Mag.*, vol. 17, no. 1, pp. 13-18, 2002.

[56] J.D. Taylor, "Ultra Wideband Radar Technology", New York: CRC Press, 2001.

[57] G.R. Aiello and G.D. Rogerson, "Ultra-wideband wireless systems", *IEEE Microwave Mag.*, vol. 4, no. 2, pp. 36-47, 2003.

[58] J. Balakrishnan, A. Batra, and A. Dabak, "A multi-band OFDM system for UWB communication", *Proc. Conf. Ultra-Wideband Systems and Technologies*, Reston, VA, 2003, pp. 354-358.

[59] E. Saberinia and A.H. Tewfik, "Pulsed and non-pulsed OFDM Ultra Wideband wireless personal area networks", *Proc. Conf. Ultra-Wideband Systems and Technologies*, Reston, VA, 2003, pp. 275-279.

[60] H.G. Schantz and L. Fullerton, "The diamond dipole: A Gaussian impulse antenna", *in Proc. IEEE Int. Symp. Antennas and Propagation Society*, vol. 4, Boston, MA, 2001, pp. 100-103.

[61] R.A. Scholtz, "Multiple access with time-hopping impulse modulation", *Proc. MILCOM Conf.*, Boston, MA, 1993, pp. 447-450.

[62] J.R. Foerster, "The performance of a direct-sequence spread ultra wideband system in the presence of multipath, narrowband interference, and multiuser interference", *Proc. Conf. Ultra-Wideband Systems and Technologies*, Baltimore, MD, 2002, pp. 87-92.

[63] Z. Wang, "Multi-carrier ultra-wideband multiple-access with good resilience against multiuser interference", *Proc. Conf. Info. Sciences and Systems*, Baltimore, MD, 2003.

[64] L. Yang and G.B. Giannakis, "Digital-carrier multi-band user codes for baseband UWB multiple access". *J. Commun. Networks*, vol. 5, no. 4, pp. 374-385, 2003.

[65] Jason Lester Hill, "System Architecture for Wireless Sensor Networks", Ph.D. Thesys, University of California, Berkeley, 2003.

[66] Chun-Hung, Liu and Harry Asada, "A Source Coding and Modulation Method for Power Saving and Interference Reduction in DS-CDMA Sensor Network Systems", Proceedings of the American Control Conference, Anchorage, AK May 8-10, 2002.

[67] Y.H. Lee and S. Tantaratana, "Sequential Acquisition of PN sequences for DS/SS communications: design and performance", IEEE JSAC, vol. 10, no. 4, pp. 750-759, May 1992.

[68] Win M.Z., Scholtz R. A., "Ultra Wide Bandwidth Time-Hopping Spread-Spectrum Impulse Radio for Wireless Multiple-Access Communications", IEEE Trans. Communications, vol. 58, no. 4, pp. 171-175, April 2000.

[69] H. Sheng, P. Orlik, A. M. Haimovich, L.J. Cimini, Jr. J. Zhang, "On the Spectral and Power Requirements for Ultra-Wideband Transmission" , IEEE International Conference on Communications (ICC), Dec. 2003.

[70] Hämäläinen M., Hovinen V., Iinatti J., Latva-aho M., "In-band Interference Power Caused by Different Kinds of UWB Signals at UMTS/WCDMA Frequency Bands", IEEE Radio and Wireless Conference, RAWCON2001. Waltham-Boston, Massachusetts, USA, pp. 97-100, Aug 19-22, 2001.

[71] Conroy J.T., LoCicero J.L. and Ucci D.R., "Communication techniques using monopulse waveforms", Proceeding of IEEE MILCOM'99, vol. 2, pp. 1181-1185, 1999.

[72] G. Cimatti, R. Rovatti and G. Setti, "Chaos-Based Spreading in DS-UWB Sensor Networks Increases Available Bit-Rate", *IEEE Trans. Circuits Syst I, Reg. Papers*, 2007, (accepted for publication).

[73] Foerster J. R., "The Performance of a Direct-Sequence Spread Ultra-Wideband System in the Presence of Multipath, Narrowband Interference, and Multiuser Interference", IEEE Conference on Ultra Wideband Systems and Technologies, 2002.

[74] H.F. Hangler, Jr. "Technical Issues in Ultra-Wideband Radar Systems", Introduction to Ultra-Wideband Radar Systems, ch. 2, pp. 33-34, Edited by J.D. Taylor, CRC Press, 1994.

[75] M. B. Pursley, "Performance evaluation for phase-coded spread-spectrum multiple access communication-Part I: System analysis", IEEE Trans. Communications, vol. 25, pp. 795-799, 1997.

[76] L. Stoica, A. Rabbachin, H. O. Repo, T. S. Tiuraniemi, and I. Oppermann, "An ultrawideband system architecture for tag based wireless sensor networks", *IEEE Trans. on Vehicular Technology*, Vol. 54. No. 5, Sept. 2005, pp. 1632-1645.

[77] S. B. T. Wang, A. M. Niknejad, and R. W. Brodersen, "Circuit modeling methodology for UWB omnidirectional small antennas" *IEEE Jour. on Selected Areas in Communications*, Vol. 24, No. 4, April 2006, pp. 871-877.

[78] H. Sheng, P. Orlik, A. M. Haimovich, L. J. Cimini, and Z. Jinyun, "On the spectral and power requirements for ultra-wideband transmission", *IEEE ICC03 Anchorage*, US, 11-15 May 2003, pp 738- 742.

[79] S. Bagga, A.V. Vorobyov, S.A.P. Haddad, W.A. Serdijn, A.G. Yarovoy and J.R. Long, "Codesign of an Impulse Generator and Miniaturized Antennas for IR-UWB", *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 4, part 2, pp. 1656-1666, Apr. 2006.

[80] A. Ismail and A.A. Abidi, "A 3-10-GHz low-noise amplifier with wideband LC-ladder matching network", *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2269-2277, Dec. 2004.

[81] C.J.M Verhoeven et al, "Structured Electronic Design - Negative Feedback Amplifiers", Kluwer Academic Publishers, 2003.

[82] M.T. Reiha, J.R. Long and J.J. Pekarik, "A 1.2 V Reactive-feedback 3.1-10.6 GHz ultrawideband low-noise amplifier in 0.13 μm CMOS", in IEEE Radio Freq. Integrated Circuits Symp., pp. 41-44, Jun. 2006.

[83] A. Bevilacqua and A.M. Niknejad, "An ultrawideband CMOS lownoise amplifier for 3.1-10.6 GHz wireless receivers", *IEEE J. Solid- State Circuits*, vol. 39, no. 12, pp. 2259-2268, Dec. 2004.

[84] D. Barras, F. Ellinger, H. Jackel, and W. Hirt, "A low supply voltage SiGe LNA for ultra-wideband frontends", *IEEE Microw. Wireless Compon. Lett.*, vol. 14, no. 10, pp. 469-471, Oct. 2004.

[85] Y. Lu, R. Krithivasan, W.M.L. Kuo, and J.D. Cressler,"A 1.8-3.1 dB noise figure (3-10 GHz) SiGe HBT LNA for UWB applications", in *IEEE Radio Freq. Integrated Circuits Symp.*, Jun. 2006, pp. 45-48.

[86] S. Shekhar, X. Li, and D.J. Allstot, "A CMOS 3.1-10.6 GHz UWB LNA employing stagger-compensated series peaking", in *IEEE Radio Freq. Integrated Circuits Symp.*, Jun. 2006, pp. 49-52.

[87] S. Shekhar, J.S. Walling, and D.J. Allstot, "Bandwidth extension techniques for CMOS amplifiers", *IEEE J. Solid-State Circuits*, vol. 41, no.11, pp. 2424-2439, Nov. 2006.

Chaos and Random Number Related References

[88] F. Pareschi, "Chaos-based random number generators: monolithic implmentation, testing and applications", PhD thesis, University of Bologna, 2007.

[89] R. Devaney, *An introduction to Chaotic Dynamical System*, Addison-Wesley, (Second Edition) 1989.

[90] A. Lasota, and M. C. Mackey, *Chaos, Fractals, and Noise. Stochastic Aspects of Dynamics*, Springer-Verlag, 1994.

[91] E. Ott, *Chaos in Dynamical Systems*, Cambridge University Press, 1993.

[92] A. Lasota, J. A. Yorke, "On the Existence of Invariant Measure for Piecewise Monotonic Transformations", in *Transactions of the American Mathematical Society*, vol. 186, pp 481-488, December 1973.

[93] F. Hofbauer, G. Keller, *Ergodic Properties of Invariant Measures for Piecewise Monotonic Transformations*, Mathematische Zeitschrift, Springer-Verlag, vol. 180, no. 1, pp. 119–140, March 1982.

[94] R. Rovatti, G. Setti, G. Mazzini, "Chaotic Complex Spreading Sequences for Asynchronous CDMA - Part II: Some Theoretical Performance Bounds", *IEEE Transaction on Circuit and Systems I: Fundamental Theory and Applications*, vol. 45, no. 4, pp. 496-505, April 1998.

[95] B. Razavi, *Principles of Data Conversion System Design*, Wiley-IEEE Press, November 1994.

[96] A. M. Abo, P. R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter", in *IEEE Journal of Solid-State Circuits*, vol. 34, no. 5, pp. 599–606, May 1999.

[97] T. B. Cho, and P. R. Gray, "A 10 b, 20 Msample/s, 35mW Pipeline A/D Converter", in *IEEE Journal of Solid-State Circuits*, vol. 30, no. 3, pp. 166–172, March 1995.

[98] S. Callegari, R. Rovatti, and G. Setti, "Embeddable ADC-Based True Random Number Generator for Cryptographic Applications Exploiting Nonlinear Signal Processing and Chaos", in *IEEE Transaction on Signal Processing*, vol. 53, no. 2, pp. 793–805, February 2005.