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Power Converters in WBG Device Technology for Automotive Applications and Characterization Setups for GaN Power Transistors

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Abstract

The strong push towards the electrification is a key factor for the ambitious targets on the progressive dismiss of fossil energy and greenhouse gases emission reduction. Power electronics systems have a huge impact on this process providing the capacity to handle the electric energy flow accordingly to the application requirements. One of the main sectors involved in such transition is the automotive field, where the restricted cost margin forces to continuously pursue more efficient and compact solutions in order to fully exploit the traction battery energy and obtain a competitive product. In fact, so far Silicon has represented the preferable choice of automotive OEMs for the design of power converters forming the electric power-train due to its long heritage, high reliability, low manufacturing costs of large size wafers of well assessed semiconductor processes. However, at this time, technological processes have been able to reach the physical limits of the material, making extremely arduous to achieve additional performance step-ups. The employment of WBG technologies overcomes the issue through the superior characteristics of the materials, as GaN and SiC, providing higher breakdown level per unit-volume and more thermally stable lattices. This allows the realization of electronic devices with smaller footprints and parasitics compared to Si counterparts enabling higher switching frequencies, reduction of the passive and magnetics values and simpler thermal management for the development of more compact and efficient power converters. On the other hand, the relative young technological processes, the very fast commutations, elevated di/dt, dv/dt and reduced form-factors represent the main challenging aspects for the designer, since an incorrect assessment during the design stage can lead to strong EMI generation, drastical efficiency reduction, increase of distortion and reliability issues that jeopardize WBG benefits.

This PhD dissertation envisages the design of innovative power converters exploiting WBG devices to get state-of-the-art performance in products intended for industrial applications of automotive field. The collaborations with different specialized companies, provided the opportunity to access commercially-available state-of-the-art SiC and GaN technologies and the possibility to realize innovative converter prototypes. Concerning SiC technology, the complete design of a $350kW$ Battery Emulator instrument in collaboration with a company leader in the automotive testing sector, was carried out from scratch exploiting state-of-the-art SiC power-modules, planar magnetics and top-notch MCU technologies. Discrete high-voltage GaN switches were exploited in the Power Supplies design for automotive charger application to target improved performances compared to the market state-of-the-art. Specifically, two high-efficiency prototypes, an AC/DC converter and a DC/DC converter of $7.5kW$, have been realized for this purpose. To further investigate the characteristics of state-of-the-art GaN power devices

two measurement set-ups have been designed. In particular, the trapping phenomenon causing the collapse of drain current during ON-state with a consequent degradation of ON-resistance has been analyzed.

Contents

Chapter 1

Introduction

The compelling necessity to fulfill sustainable, climate-preservative and environmental friendly goals by industrial players and maintaining, or even rising, production levels without affecting the social fabric is leading to a deep transformation of the industrial processes. The path is marked by strict and audacious targets fixed by international government institutions through the allocation of resources for pivotal goals, one for all the decarbonization. In this direction, the European Green Deal (EGD) [1] aspires to obtain climate neutrality by 2050 of EU members by means of several regulamentations like the Fit for 55 plan [2] in which the greenhouse gas emissions must be decreased at least of 55% by 2030 compared to 1990. Concerning the industrial sector, this translates in the progressive abandonment of fossil fuel as energy propellant of power-hungry processes in favor of electric alternatives. Among the various fields involved by the electrification trend as buildings' energy management, renewable energy systems, furnaces-related industries [3], etc..., the automotive sector, in charge of the 15% of total EU CO_2 emissions [4], is showing the fastest transition driven by the possibility to partially or fully electrify the automotive power-train, process that deeply relies on applications of power electronics, with a strong boosting effect on vehicle efficiency.

1.1 Power Electronics in Automotive Field

In contrast to Internal Combustion Engine (ICE) vehicles, the powertrain of Hybrid and full-electric Electric Vehicles (HEV/EV) gets rid of a large amount of moving parts as transmission, gear tank, driveshaft, etc.. depending on the hybridization level, making the whole system more reliable and efficient. Several variants of powertrains are possible for HEV/EV according to the presence of mechanical differentials [5], number of e-motors, parallel or series working operation of ICE in HEV [6], implying an accurate design process in terms of performance, size, power level and cost. An overview of a generic EV powertrain is depicted in Figure 1.1.

Up to three voltage buses are present, supplied by a high-voltage traction battery and two $48V$, $12V$ low-voltage batteries. The first is set typically to $400V$, but reaches $800V$ in high-range performance cars, and is made by several cells in series-parallel configuration constituting a battery pack usually placed at the bottom of the vehicle forming a skateboard-shaped structure. The main function

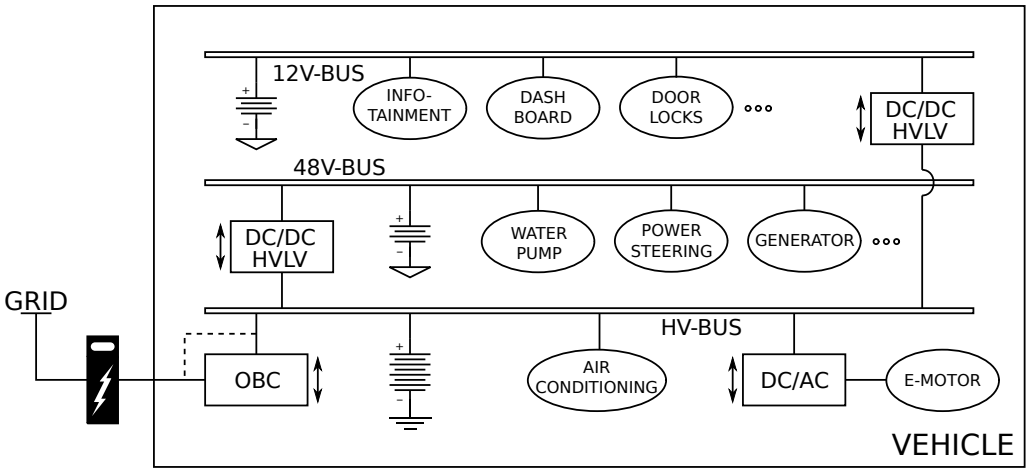

Figure 1.1: schematic of a generic EV powertrain

is to provide the demanded energy by the e-motor and high-voltage auxiliary components as air-conditioning compressor. The battery pack capacity goes from $20kWh$ to more than $100kWh$ [7] to fulfill the wide choice of automotive market by means of cylindrical or punch cells of Lithium-Ion that guarantees high energy efficiency, high specific power and long life cycle, compared to other materials [8]. The $12V$ battery performs the same role that has in an ICE vehicle, supplying the low-power systems as infotainment, dashboard, door locks, power windows, etc..., while the $48V$ battery is dedicated to systems in the range of hundreds and a thousand of Watt as water pump and power steering. The low-voltage batteries are supported by the traction battery through isolated DC/DC converters due to the lack of an alternator. Unidirectionability feature is sufficient to keep the low-voltages battery charged, however bidirectional converters are usually employed for safety and emergency conditions. Indeed, the jump-starting procedure through the low voltage bus is extremely simpler than connecting directly to the battery pack, moreover, in case of simultaneous discharged traction battery and dangerous situation, the vehicle can be moved by the low-voltage battery for a limited, but potentially vital, distance [9]. In modern HEV/EV the e-motor is made of an AC machine, mainly induction or permanent-magnet synchronous machine [10], thanks to higher efficiency, power density, reliability and lower maintenance costs than DC motor, which on the other hand can achieve higher torque at low speeds with a simpler control. Therefore a DC/AC converter is placed between the high-voltage battery and the e-motor. The traction inverter regulates the amplitude, frequency and phase of the three-phase voltage set when the e-motor requires power, while acts as AC/DC during breaking situations, regenerating the high-voltage battery by means of bidirectional energy flow. In order to properly charge the battery pack, a charging system is set up where the grid energy is provided to the battery through an isolated AC/DC converter. The battery chargers are crucial in the EV, since interacts with the most valuable component of the vehicle, and can be categorized depending on where the AC-to-DC conversion takes place and on the power level. When the AC voltage of the grid is directly provided to the charging connector, the DC voltage for the high-voltage battery is generated within the vehicle by means of an On-Board Charger (OBC), on the other hand a DC voltage, externally generated by an Off-Board Charger, can be directly applied to the connector and the OBC bypassed. The first solution

gives more flexibility in terms of charging locations, while the second manages higher power levels for a reduction of charging time. It is noteworthy how the OBC can transfer energy in conductive or inductive way, however the second is still seldom employed in current commercially available cars. Concerning the distinction by power levels, the IEC 61851 [11] regulates the charging modes in terms of power limits in addition to data transfer for battery monitoring, cables and socket to be used within European borders. Table 1.1 summarizes the mode features and indicates the typical corresponding charger system.
Given the power at stake, Mode I is generally used in domestic locations for charging time that lasts $6 - 8$ hours while the others are available in public spots and guarantee fast charging up to few tens of minutes [12]. As for the DC/DC between high-voltage and low-voltage buses, an unidirectional charger would be sufficient to achieve the goal, however bidirectionality feature is broadly implemented to perform Vehicle-to-Grid (V2G) power transfer. The main benefit is the possibility to use charged car as an energy storage system to maintain grid balancing in case of grid strongly dependent on inconstant renewable energy sources or in case of temporary high power demand [13].
As appears clearly, bidirectional characteristic is shared among all the main power converters tied to automotive applications together with the following aspects. To make HEV/EV competitive compared to ICE vehicles in terms of cost and mileage per full-charge, the design of power converters is deeply focused on obtaining the maximum efficiency targets and highest power density by means of light and compact systems requiring reduced efforts in thermal management. Such goals are unfeasible without the exploitation of advanced topologies and innovative technologies as Wide Band-Gap (WBG) materials.

Table 1.1: Charging mode features

Charging Mode	**Max Power**	**Max Voltage**	**Max Current**	**Data Transfer**	**Battery Charger**
I	$3.7kW$	$230V_{AC}$ Single-phase	$16A$	No	On-Board
II	$7.2 - 22kW$[1]	$480V_{AC}$ Single/Three-phase	$32A$	Yes	On/Off-Board
III	$> 22kW$	$480V_{AC}$ Three-phase	$63A$	Yes	Off-Board
IV	$> 22kW$[2]	$> 200V_{DC}$	$> 63A$	Yes	Off-Board

[1] $7.2kW$ for On-board case, $22kW$ for Off-board case [14]
[2] Fast DC charging is usually in the $50 - 100kW$ range with Ultrafast charging up to $400kW$ ($800V$) [14]

1.2 Wide Bandgap Techonology

A semiconductor material is conventionally denominated wide bandgap when the energy gap E_g, i.e. the energy needed by an electron to pass from the valence band to the conduction band, is greater than a threshold of usually $2eV$. Elevated E_g physically translates in stronger crystalline bonds which require an higher critical electric field E_c to be broken when reverse biased triggering the impact ionization responsible of the avalanche effect in a PN junction [15]. Still, given the proportionality of E_c on the Drain to Source (or Collector to Emitter) distance in the electronic device, the breakdown voltage of WBG material is shifted to higher values for the same form-factors. Moreover, the intrinsic carrier concentration n_i is inversely proportional to E_g providing lower leakage currents. Such properties are crucial in the development of new generation power devices, migrating from the largely used Silicon (Si), with $E_g < 2eV$, to other technologies as Silicon Carbide (SiC) and Gallium Nitride (GaN) which are emerging in the power electronic market. The main physical characteristics of these material are plotted in Figure 1.2.

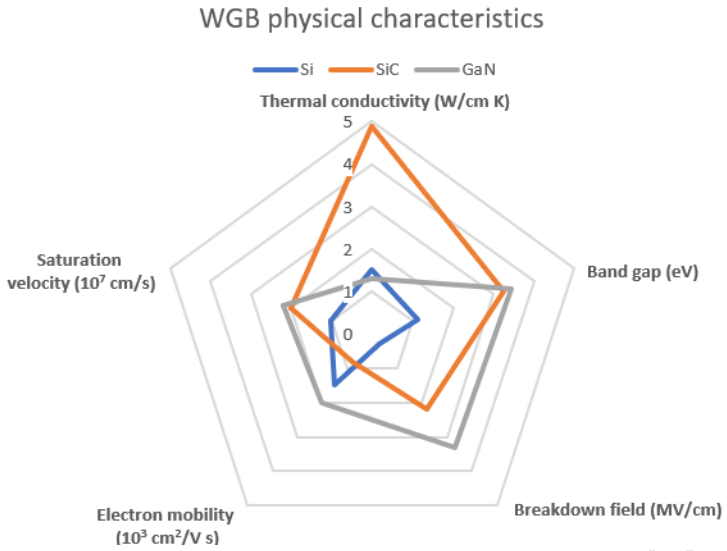

Figure 1.2: WBG physical characteristics values [16]

Here it can be noted how the superior thermal conductivity of SiC makes it suitable for very high power level systems, while the GaN electron mobility addresses this material to high speed applications as indicated also by the Johnson's FOM [17], that is the product of E_c and saturation velocity. Nevertheless, both SiC and GaN highlight superior physical features than Si. In order to estimate the technological limit of a semiconductor, the specific ON-resistance versus the breakdown voltage figure of merit is often considered since a trade-off between the two parameters are usually implied in the design stage [18]. As expected, in [19] Si reveals lower performances, however the reported devices are closer or even beyond the limit curve, while SiC and, most of all, GaN devices are quite far from their respective limits. This means Si represents a mature technology with little margin of new developments, whilst the others have larger room of improvement. The fairly notable number of manufacturing companies that furnish SiC products is symptom of a good technology maturity level, nevertheless important

challenges remain to cope with as gate-oxide growth, density of defects and chiefly the high manufacturing cost (10x compared to Si), which is still unclear if can be decreased considerably [20]. On the other hand, GaN technology is affected by more demanding issues which don't allow its employment extensively. The high costs of implementing material substrates with favorable crystalline lattice where the GaN can grow, force the use of Si bulks, negatively impacting on the device thermal conductivity and leading to heterogeneous structures realized in lateral devices. The latter is a suitable solution for high frequency operation at the expense of breakdown voltage levels which currently reach 600-650V. Cascode configuration have been designed to address such issue obtaining devices able to withstand up to 900V, however the GaN benefits are further reduced in terms of complexity and conductive losses. Moreover, additional process stages are required to shift the gate threshold toward positive values (normally-OFF devices), and to limit the current collapse effect [21]. In spite of that, early generation devices already provide better performances than more consolidated Si solutions.

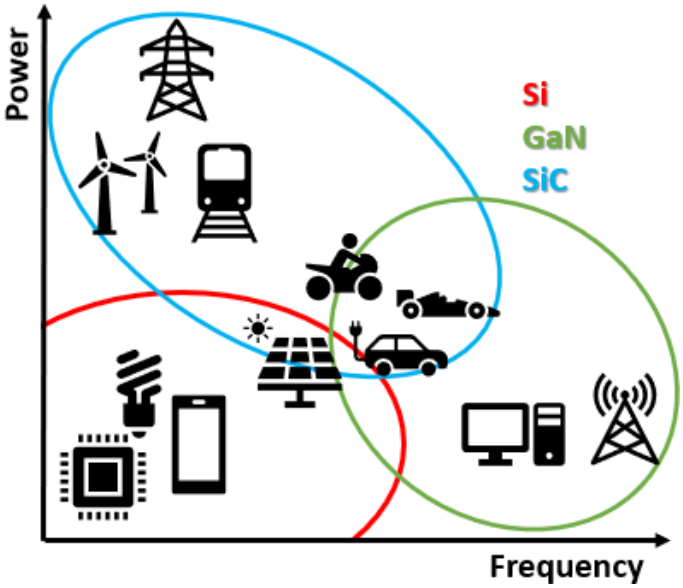

Figure 1.3: Application fields of Si, SiC and GaN technology in function of power and working frequency

As consequence of the previous considerations, three main application areas can be identified in Figure 1.3 on the employment of the different materials. SiC technology is well suited for high voltage and mid-to-high power ($>\sim 10kW$) sectors as heavy transportation and wind turbine, while GaN is indicated for high speed and mid-to-low power ($<\sim 10kW$) fields as telecommunication power amplifier and charger for portable devices, then Si remains the most valid option when low power and low frequency levels are needed as in lighting and digital applications. Nowadays, Si devices still dominate the automotive sector, however the increasing power demand and the necessity of compactness, as described in Section 1.1, make WBG materials the most promising alternatives.

On system level, the exploitation of SiC and GaN devices have multiple advantages, leading to an efficiency boost of switching power converters up to 98% and even beyond. The possibility to obtain smaller devices than Si counterparts for the same voltage/current rating reduces considerably the parasitics, as gate

charge and output capacitance, enabling faster commutations. By consequence, the dimensions of capacitance and magnetics (inductance and transformer), typically the bulkiest components in a switching converter, shrink down with an immediate benefit in terms of occupied volume, weight and power density. Afterwards, in addition to lower commutation losses, the combination of high thermal conductivity (SiC) and low ON-resistance (high electron mobility - GaN) with the more thermally stable bonds due to wide bandgap bring to a more relaxed cooling system design. However such improvements come at the price of more expensive electronic devices, which are nevertheless dumped by cheaper passives, and more careful layout design. Elevated di/dt, dv/dt can cause large spikes and EMI generation if traces and components arrangement are not finely addressed, chiefly in parallelized transistors or power modules. On the other hand, an optimized layout of the area between driver and gate is crucial to minimize and effectively decouple the power loop and gate loop through the ground to avoid degradation at gate level or unwanted turn-on.
In the thesis, the design and realization of three different power converter prototypes employing WBG devices are described. The first two prototypes are intended for automotive applications and represent a $7.5kW$ unit cell for a high efficiency battery charger exploiting GaN technology. In particular, a bridgeless single-phase AC/DC converter and an isolated DC/DC converter are realized where the employment of commercial $650V$ GaN HEMT transistors allow high frequency operations and smart topology thanks to the reduced commutation losses. The component procurement, the PCBs realization the assembly procedure have been sponsored by OCEM Power Electronics, a leading company in power electronics for scientific and industrial research. The last prototypes is a bidirectional isolated $350kW$ DC/DC converter capable of handling steep voltage and current transitions in order to mimic the behavior of a traction battery in different conditions. Given the power levels at stake and the fast dynamic requirements to perform battery emulation tests, commercial $1200V$ SiC power modules are employed along with state-of-the-art components to obtain a system compliant with most of the structures to be tested as HEV/EV power-trains. The activity has been carried out in collaboration with LOCCIONI, a leader company in the automotive testing solutions, which commissioned the project and provided the indispensable facilities for the system realization and ARCA Tecnologie, providing the know-how needed to properly design and implement the control algorithm.
In addition, given the more promising features of GaN technology, either in terms of performance and manufacturing process, but more prone to defect due to the minor heritage by the foundries, two measurement setups have been implemented for the characterization of ON-Resistance degradation on experimental version of GaN devices from a research foundry. The first allows to perform tests at on-wafer level accessing the device by a probe station and varying the blocking voltage, the commutation period and temperature, while the second embeds the device in a typical power electronic application, providing insight of the behavior during realistic working operations. Both strategies aim to yield valuable information for GaN transistor foundries by means of dynamic, large signal tests.
The arrangement of the dissertation is the following: in Chapter 2 the design of the converters for charging applications are presented, in Chapter 3 the battery emulator converter design is shown, while the implementation of the two mea-

surement setups is located in Chapter 4.
The entire PhD course have been carried out during the recent pandemic emergency and the worldwide chip shortage which heavily hit the electronic sector causing extremely severe inconvenients in term of production delay and component replacement. In fact, a big effort has been made for the actual implementation of the aforementioned designs, which nevertheless have been successful. The results of these activities have been summarized in four scientific papers [22], [23], [24], [25].

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Chapter 2

Design of a 7.5kW Power supply for charger applications

The trend in automotive power-trains electrification drastically sped up in the recent years pushed by enormous industrial investments consequent to demanding environmental requirements imposed by legislators and the growing appeal of electric and hybrid vehicles among the population [1]. One of the most thriving topic concerns the charging framework of automotive electric energy storage (EES), typically Ion-Lithium battery-packs, in which OFF/ON Board Chargers play the chief role. These are usually two-stage systems, with an AC/DC grid-tied converter and a DC-DC converter to regulate the battery voltage and current, where elevate efficiency and bidirectionality are required respectively to reduce the system size and for vehicle-to-grid (V2G) power flow. Among a wide variety of classification depending on the housing, power size and charging technique [2], [3], the single-phase LEVEL2 [4] 2-stage battery charger represents the standard implementation since can be used either as ON-Board Charger (OBC) and OFF-Board charger in private facilities or as base cell in fast charging stations.
Wide Band-Gap (WBG) technology, as SiC and GaN, is gaining considerably share market to the detriment of Si devices. If for LEVEL3 chargers[5] only SiC transistors can be exploited for the higher breakdown voltages and longer heritage, in LEVEL2 range ($1.8 - 19.2kW$) $650V$ GaN technology commercial solutions are available for power electronic applications thanks to normally-OFF HEMT devices. The superior characteristics in terms of low channel resistance for current capability, small capacitive parasitics and absence of reverse recovery charge are crucial to increase efficiency, power density and switching frequency, enabling the shrinking of the magnetic components as the high-frequency transformer, typically one of the bulkiest device in DAB topology. However, such benefits come along with new challenges from the design point of view: elevated $\frac{di}{dt}$, $\frac{dv}{dt}$ must be handled in terms of layout, minimizing inductive loops with wise signal and ground plane arrangement, and adopting suitable components for the high frequency regime with reduced stray inductances. In this context, two $7.5kW$ converters using $650V$ commercial HEMT GaN transistors suitable for charging applications has been designed and implemented exploiting PSIM [6] simulation environment for electrical and thermal simulations, while Eagle CAD tool [7] by Autodesk has been employed for power and control PCB boards. In this chapter the design of the two stages forming a $7.5kW$ base cell are described in detail, in particular Section 2.1 is

dedicated to the AC/DC converter and Section 2.2 to the DC/DC converter.

2.1 PFC

The first stage of a power supply for automotive charging application is made of an AC/DC converter in charge of extracting the demanded power from the grid maximizing the Power Factor (PF) and minimizing the Total Harmonic Distortion (THD). In this way the system is not oversized for the exceeding apparent power and doesn't contribute to source distortion. A bridgeless, boost-like PFC converter allows to fulfill the requirements with enhanced efficiency and bidirectionality, due to the elimination of the input diode bridge. Several bridgeless PFC converters are present in literature; [8] compares different PFC topologies (with or without input diode bridge) to the well-known PFC boost converter, while [9] focuses only on bridgeless ones. Among the bridgeless boost, bridgeless dual boost, bridgeless boost interleaved, bridgeless totem-pole boost (BTTP) and bridgeless totem-pole boost interleaved, the most promising turns out to be the BTTP. Indeed, it is able to reach the highest efficiency ($> 99\%$ theoretically) with the shortest component list. Nevertheless, BTTP struggles to prevail over other topologies since the switching losses on silicon IGBTs or silicon power transistors compel to adopt Critcial or Discontinuous Conduction Mode (CrCM, DCM), making control more complex and deteriorating the THD. Therefore, the exploitation of WBG devices becomes crucial to overcome silicon limits. In particular, GaN technology is the ideal candidate thanks to zero reverse recovery Q_{rr} enabling the employment Continuous Conduction Mode (CCM) for BTTP control. This section describes the detailed design, simulation and implementation of an air-cooled, $7.5kW$ Bridgeless Totem Pole PFC Boost Converter exploiting commercial $650V$ GaN switches. The single-phase bidirectional converter operates at $100kHz$ switching frequency with and output DC link voltage of $400V$ and an overall efficiency at full power of 98.4%. In Section 2.1.1 the BTTP topology is illustrated, in Section 2.1.2 the converter design is developed in terms of active and passive components' sizing and system architecture. Then the proposed control algorithm and efficiency assessment by simulations are illustrated in Section 2.1.3 and Section 2.1.4, respectively.

2.1.1 Topology

In Table 2.1 the specifications of the PFC AC/DC converter are expressed. Here it is evident how PF and efficiency (η) targets address to a BTTP PFC boost converter.

Table 2.1: AC/DC converter specifications.

Vin	**Iin**	**Switching Freq.**	**PF**	**THD**	η	**Pout**	**Vout**
$240V_{AC}$, $50Hz$	$32A_{RMS}$	$100kHz$	$> 98\%$	$< 5\%$	$> 98\%$	$7.5kW$	$400V$

In Figure 2.1 is depicted the basic schematic of a BTTP: two half-bridges are placed between an input inductor and an output capacitance where the respec-

tively input current and output voltage are controlled in boost-like fashion. Q1 and Q2 form the low frequency (LF) leg, while Q3 and Q4 form the high frequency (HF) leg. Basically, the 3-4 leg acts as a synchronous boost converter that works alternately on the positive and negative part of the input voltage sine wave to obtain power factor correction. This should be more clear looking at the working principle in Figure 2.2. When $V_{in} > 0$, Q2 is ON and connects the output low potential to the neutral potential of the grid. Hence, L-Q4-Q3 triplet forms a boost converter where Q4 is the leading switch (T) and its modulation scheme is the duty cycle ρ, whereas Q3 acts as diode (D) conducting for the remaining percentage of the period $1 - \rho$. This is shown in a-b quadrants, where the current path is highlighted in case of activation of T and D. When $V_{in} < 0$, Q1 is ON and connects the output high potential to the neutral potential of the single-phase grid. Now the leading switch becomes Q3 and Q4 works as the diode (c-d quadrants). It is evident how LF leg shares the same frequency of main voltage ($50Hz$), while HF leg work at switching frequency. For this reason LF can be made of conventional silicon transistors because switching losses are not critical, while HF leg must use WBG devices. It is noteworthy the possibility to replace LF switches with power diodes, however it would imply worse performances, chiefly in terms of efficiency and THD, and loosing bidirectionality.
The main disadvantage of the BTTP converter is the possibility of current spikes generation during the polarity change of the main voltage. Indeed, the output charge of transistors and the recovery charge of silicon body diodes could discharge abruptly if the zero-crossing is not well detected [10], [11]. To avoid this behavior, all the devices are turned OFF when the main voltage is near $0V$ ceding a bit of PF performance.

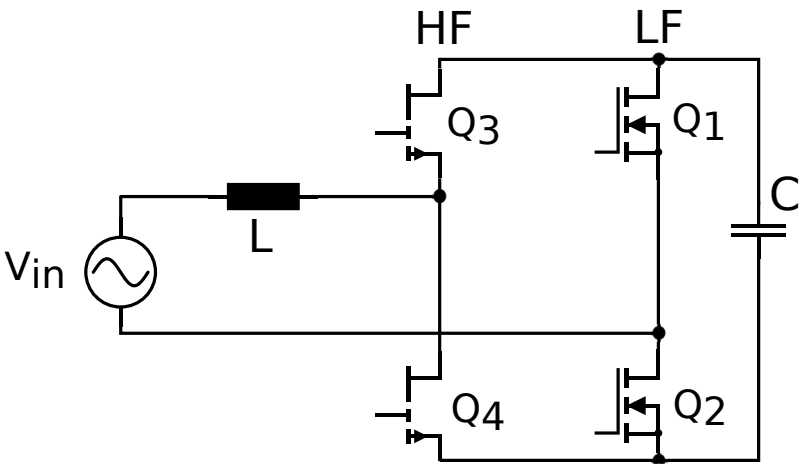


Figure 2.1: BTTP schematic

2.1.2 Design Implementation

2.1.2.1 Component sizing

As said previously, the two BTTP legs should use different semiconductor technologies due to their function in the working principle. The tied efficiency constraint of Table 2.1 helps in the choice in both cases. In Table 2.2 a list of possible commercial switches is shown. Since the conductive power loss is predominant,

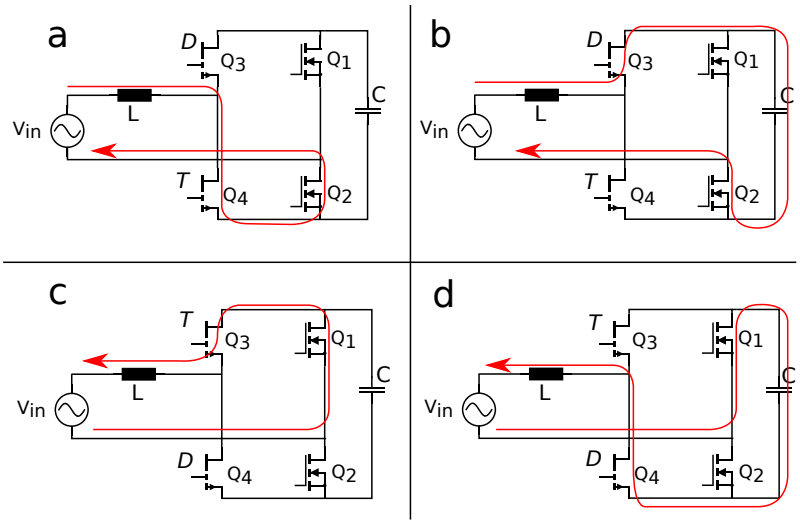


Figure 2.2: BTTP working principle

the IPW60R017C7 [12] was chosen for its low channel resistance thanks to CoolMos technology. Concerning HF leg, the range of WBG commercial devices for voltages and currents of Table 2.1 is still not as wide as for the silicon technology. Few possibilities are shown in Table 2.3 and the GS66516B [13] was chosen in order to minimize as much as possible switching losses. For GaN technology, only HEMTs devices (with positive threshold) were been considered, while cascade versions were omitted due to the exploit of embedded input silicon transistor that sightly degrades switching performance allowing though higher blocking voltages [14].

Table 2.2: LF leg possible devices.

Product	**Manufacturer**	**Technology**	V_{DS}
IPW60R045CP	Infineon	Si	$650V$
STY105NM50N	ST	Si	$550V$
IPW60R017C7	Infineon	Si	$650V$
FCH023N65S3	ON	Si	$650V$
IPZ65R019C7	Infineon	Si	$700V$
I_{DS}@100°C	R_{DS}	C_{oss}	
$38A$	$45m\Omega$	$320pF$	
$88A$	$22m\Omega$	$500pF$	
$69A$	$17m\Omega$	$200pF$	
$66A$	$23m\Omega$	$298pF$	
$62A$	$19m\Omega$	$160pF$	

In agreement to the previous BTTP converter description, the inductor and output capacitor are sized in the same way of a typical PFC boost converter. Equations follow [15], [16]:

$$L_{min} = \frac{V_{out}}{4 f_{sw} \Delta I} = 74uH, \quad \text{with} \quad \Delta I = 3\% \frac{P_{out}}{V_{in,RMS,min}\sqrt{2}} \tag{2.1}$$

Table 2.3: WBG power devices.

Product	**Manufacturer**	**Technology**	V_{DS}	I_{DS}@100°C
IMW65R027M1H	Infineon	SiC	$650V$	$39A$
IMZA65R027M1H	Infineon	SiC	$650V$	$41A$
GS66516B	GaN System	GaN HEMT	$650V$	$47A$
R_{DS}	C_{oss}	Q_r	C_{iss}	
$27m\Omega$	$244pF$	$239nC$	$2131pF$	
$27m\Omega$	$244pF$	$239nC$	$2131pF$	
$25m\Omega$	$130pF$	$0nC$	$520pF$	

$$C_{out,min} = max \begin{cases} \frac{P_{out}}{V_{out} 2\pi f_{line} \Delta V_{out}} = 2.98mF, & \text{with} \quad \Delta V_{out} = 5\% V_{out} \\ \frac{2P_{out} t_{hu}}{V_{out}^2 - V_{lim}^2} = 2.5mF \end{cases} \tag{2.2}$$

where t_{hu} is the holdup time and corresponds to a line cycle ($20ms$), while $V_{lim} = 200V$ is the output voltage threshold in case of a line interruption of t_{hu} duration. A value of $4mF$ is chosen for the output capacitance. Concerning the inductor, an initial a value of $100uH$ has been considered, however circuital simulation shown a THD value beyond the specification limit, therefore a $200uH$ input inductance was chosen. At the output stage, the voltage spikes generated by high current derivative of GaN devices on bulk capacitor ESL must be carefully accounted. ESL can be decreased placing multiple capacitors in parallel and using low-ESL capacitor. Capacitor with film technology can assure low ESL but the poor capacity density leads to an unfeasible number of parallel component. Hence, both electrolytic (high capacity density, medium-high ESL) and film capacitor are used to flatten ESL and redistribute the current harmonics [17].

2.1.2.2 Architecture

The converter is built following a modular approach and with a sparse component distribution in the main board in order to increase the prototype testability and eventual tweaking. This choice for the first development of the prototype obviously decrements the overall power density, that can be highly increased in a successive design iteration. The three modules constituting the system are the Mother Board, the Control Board and GaN Daughter Module. The schematic of the entire converter, comprehensive of sensed signals, is shown in Figure 2.3.

The GaN Daughter Module consists of two separated boards, a driver board and an IMS board. This solution is implemented to satisfy the necessity of an enhanced thermal management together with minimal parasitics [18]. Figure 2.4 depicts the 3-D version the module consisting of two distinct boards, the brown one (IMS Board) and the green one (Driver Board). The Driver Board is implemented in a 4-layer $43x69mm$ FR4 PCB and is populated by the isolated gate drivers, the isolated DC-DC converters for their power supply and the ceramic capacitors for the local DC decoupling of the DC-link for the minimization of the power-loop stray inductance. Two isolated single-channel ADUM4121 [19] gate drivers by Analog Devices boost the digital PWM signals from the microcontroller in two

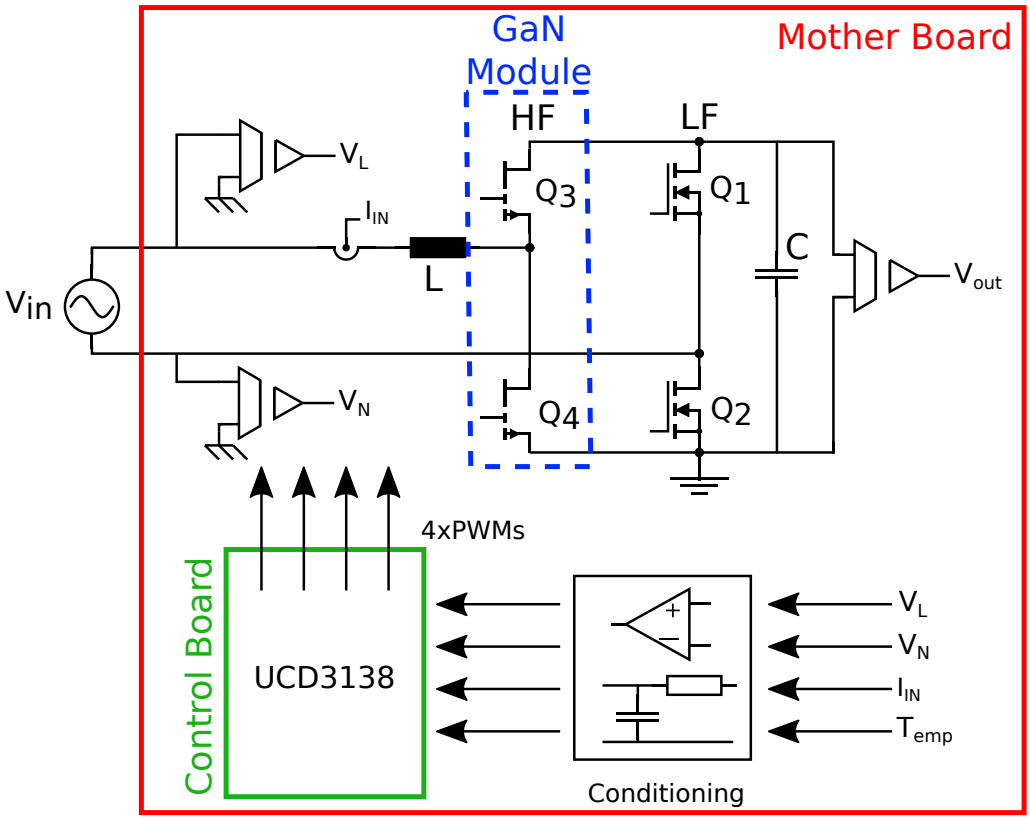


Figure 2.3: Schematic of the whole converter comprehensive of sensing characteristics

$+6/-3V$ gate signals with fast transitions and high peak/sink current capabilities, fundamental characteristics when driving WBG devices. Given a maximum skew of the delay time among two different ADUM4121 of $22ns$, and the very fast commutation of the switches (delay time + rise/fall time <$40ns$), a $70ns$ nominal dead-time value was selected and implemented in the PWM command generation. The placement of drivers in the board was optimized to reduce as much as possible the distance between their output and the gate ports of transistors to minimize the inductance of the gate driving loop: to this aim, a short $2.54mm$ connector toward the IMS board is used and the connection is made with the transistor Kelvin-source. The IMS board is a $45x45mm$ PCB where two GS66516B transistors are placed forming, an half-bridge, while the insulated metal substrate is in charge to convoy the heat produced to the heat sink minimizing the thermal resistance. Indeed, IMS board is basically made of a thin FR-4 layer attached to a thick thermal conductive substrate, typically aluminum, for enhanced thermal management performances (in combination with heatsink) in comparison to a single FR4 board with thermal vias. It is noteworthy that GS66516B has the thermal pad at the bottom of its case, hence oriented to the IMS metal substrate, allowing to not overheat driving circuits. These boards are described in the pictures of Figure 2.5 and Figure 2.6.

The Control Board is a 4-layer $46.2x38.1mm$ FR4 PCB specifically designed to implement the control law of the converter. The employment of a detached board allows to upload the firmware more easily and perform tests on digital signals without being necessarily connected to power devices, other than being more immune to possible conductive EMI thanks to a single joint point of the ground reference with the Mother Board. Among the wide variety of microcontrollers that are commercially available, a trade off in terms of computational resources,

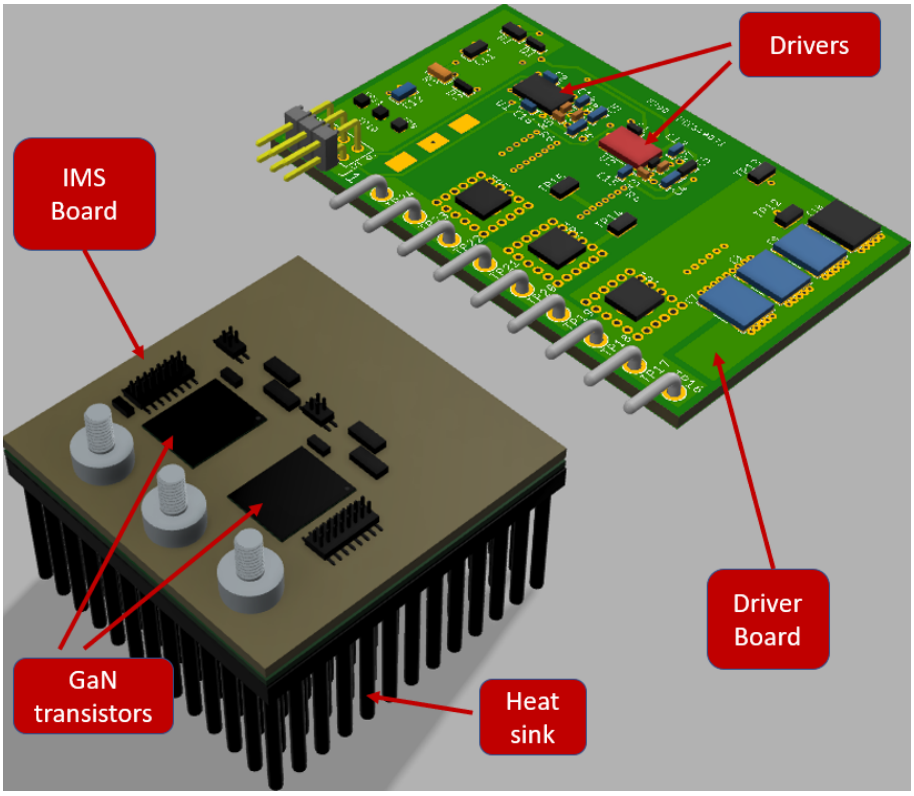


Figure 2.4: GaN Daughter Board Module (3-D version)

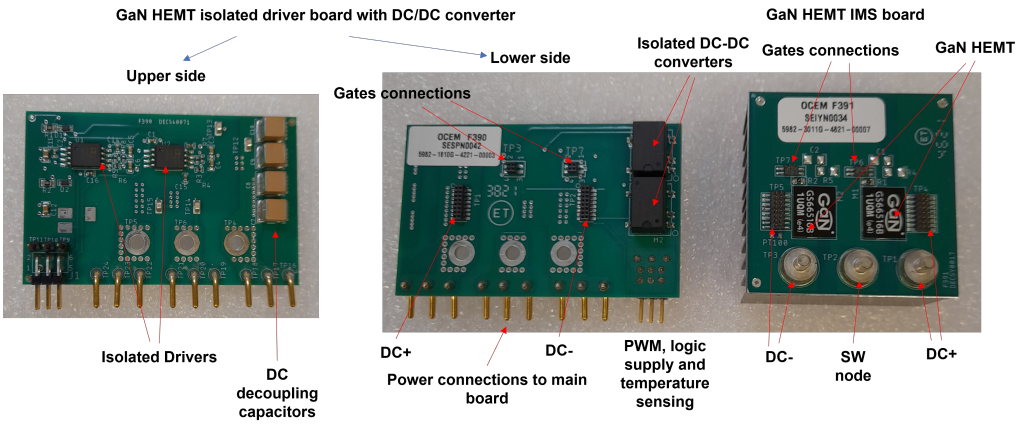


Figure 2.5: GaN IMS board and driver board

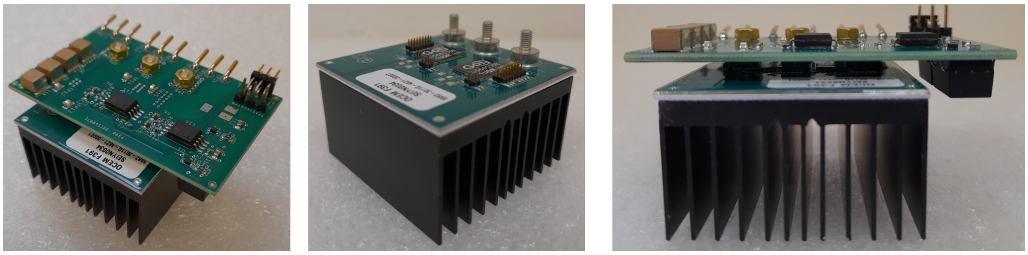


Figure 2.6: GaN Daughter Module assembly: driver board + IMS board + heat sink

speed, compactness and price lead to the selection of the UCD3138 by Texas Instruments. The UCD3138 [20] is a digital controller specifically designed for power supply purposes with tailored resources to be interfaced with AC/DC and DC/DC converters. This allows to deal with a more application-dependent device, avoiding the more general-purpose and power-hungry microcontrollers of C2000 family. The main characteristics of UCD3138 are the 8 digital PWM with 250ps resolution, 3 feedback loops, 14 single-ended ADCs and a dedicated hardware state machine following a mixed-signal approach. The last feature enables the possibility to implement a very fast control loop in combination with 2 differential error ADC (EADC) with a sampling frequency up to 16MHz. The realized control board (50x38mm) is shown in Figure 2.7 The proposed control algorithm will be discussed later

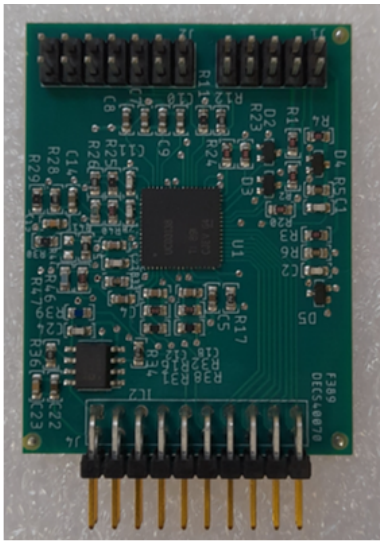


Figure 2.7: Control Board realization

The Mother board is a 223x265mm 4 layers FR-4 board where the previous modules are connected to the rest of high voltage section (LF leg, PFC choke, bulk capacitors, etc) and to the low voltage section. In addition the mother board provides input and output accesses to the system. The input stage (depicted in Figure 2.8) is made of a 250V/60A fast-acting SMD fuse, an EMI filter EN55022 Class B compliant, a relay with in-rush current protection thermistors and a diode bridge. The function of diode bridge is to pre-charge the output bulk capacitors during start-up, indeed it stops to conduct when the output voltage is above $240\sqrt{2}$, i.e. when BTTP starts to boosts the input main voltage. The low voltage section basically carries out the sensing operations and deals with PWM signals up to the drivers. This entire section is galvanically isolated from the high voltage for additional protection by means of the 12V/15W AE15-EW-S12 CUI auxiliary power supply [21] which is supplied by the output voltage of BTTP. This auxiliary supply is largely over-sized for this application and was mainly selected for its availability: the dimensions of this functional block can be widely reduced with a custom design. The quantities to be sensed are input and output voltages, input current and GaN module temperature. The three voltages (V_L, V_N, V_{out}) are

acquired with resistor voltage dividers together with an optical isolated amplifier (ACPL-C87A by Broadcom Inc. [22]) whose output is scaled and filtered by an Op-Amp in differential configuration. Concerning the current, the automotive-grade ACS724LMATR-65AB-T [23] hall-effect sensor of Allegro microsystem is used, which assures the acquisition of a bidirectional current within $\pm 65A$ in SOIC16 SMD package. The GaN temperature is measured by a PT100 resistor combined with a Wheatstone bridge. The PT100 is located directly on the IMS board, because the heat of transistors is easily spread by the aluminum substrate of IMS board. In the end, a polarity check circuit is implemented to give an auxiliary feedback to the controller on the zero-crossing event. This is made by a comparator and a switch as in [24].

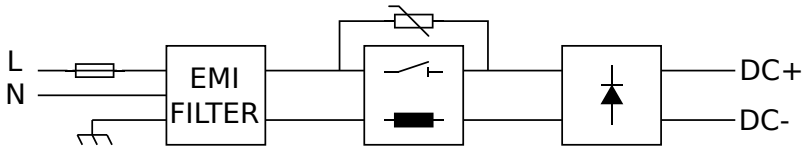


Figure 2.8: Input stage

The GaN Module and the Control Board are plugged into the Mother Board shaping the $223mmx265mmx107mm$ system depicted in Figure 2.9.

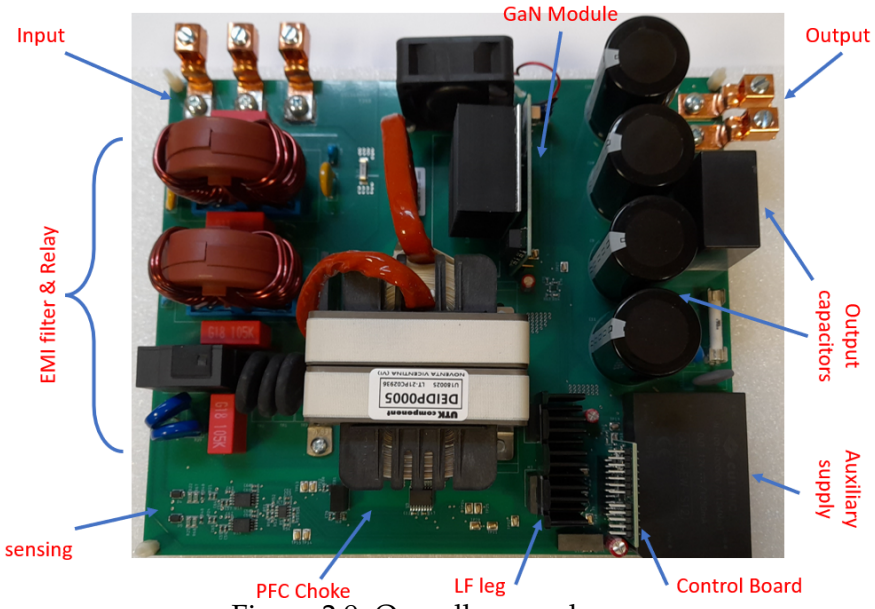


Figure 2.9: Overall power losses

2.1.3 Control

Simulations of the converter are carried out by means of PSIM [6], an electronic circuit simulation software developed by Powersim, designed for power electronics and motor drive simulations. PFC system cannot be fully evaluated in open-loop condition due to the mandatory sinusoidal-shape of the input current, therefore a feedback control strategy must be accounted from the first simulation step. Two feedback loops are in charge to regulate the output voltage and the input current in average mode. The control scheme is shown in Figure 2.10. The slow voltage loop generates a power reference which is multiplied by an appropriate

feed-forward term to scale its magnitude and give the shape of the input voltage to the current reference. It can be noted that the main difference with the typical PFC boost control is rectification of the current measurement in order to account the duty cycle swap during positive and negative line cycle.

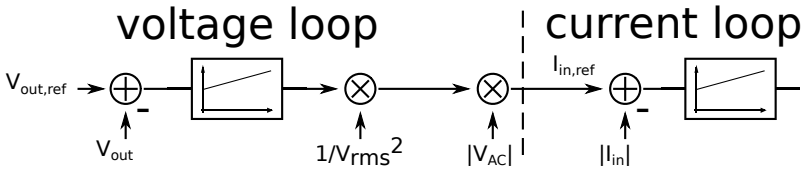


Figure 2.10: Control scheme

The coefficients of the two PI blocks can be obtained following the common strategy used in PFC boost converter [15], [25]:

$$PI_V : K_{p,V} = \omega_V C_{out} V_{out}\ K_{i,V} = K_{p,V}\frac{\omega}{h} \quad with \quad \omega_V = 2\pi f_V,\ f_V < \frac{f_I}{10},\ 0.7 < h < 3 \tag{2.3}$$

$$PI_I : K_{p,I} = \omega_I \frac{L}{V_{out}}\ K_{i,I} = K_{p,I}\frac{\omega_I}{h} \quad with \quad \omega_I = 2\pi f_I,\ 10 f_V < f_I < \frac{f_{PWM}}{10},\ 0.7 < h < 3 \tag{2.4}$$

where f_V, f_I are the bandwidth of the voltage and current loops, respectively. In Figure 2.11, the schematic of the topology and control blocks are depicted in PSIM environment with resistive load. Here, the converter is assessed in its functional behavior considering a limited number of parasitics (as channel resistance, C_{oss}, forward voltage of transistors during reverse conduction). The simulation results in Figure 2.12 provide encouraging PF and THD values ($> 99\%, < 4\%$) with a $\pm 10V$ low frequency ripple in the output voltage which can be easily tolerated by a DC/DC second stage.

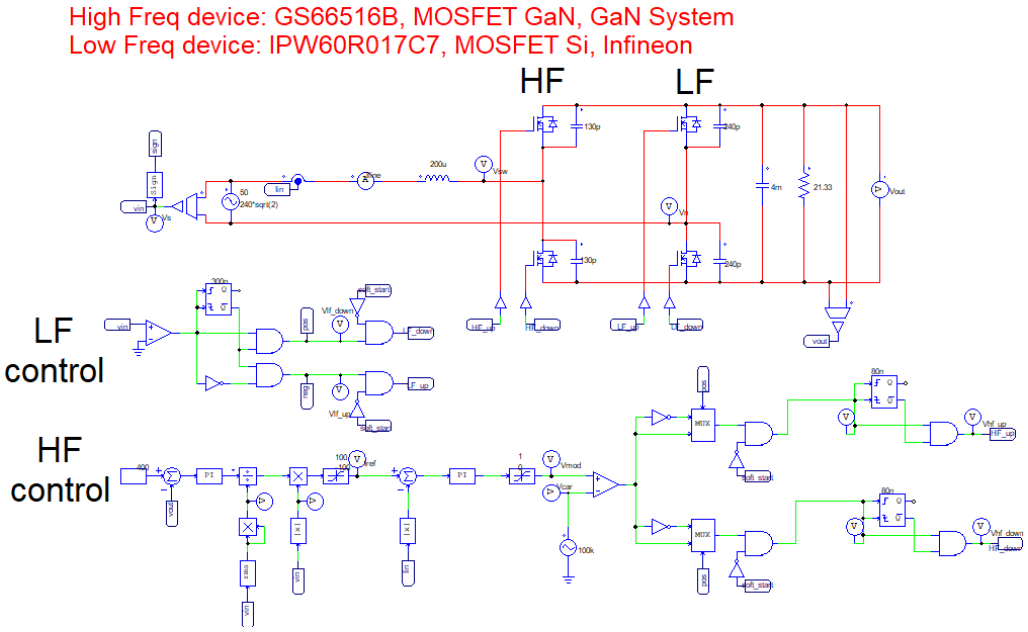
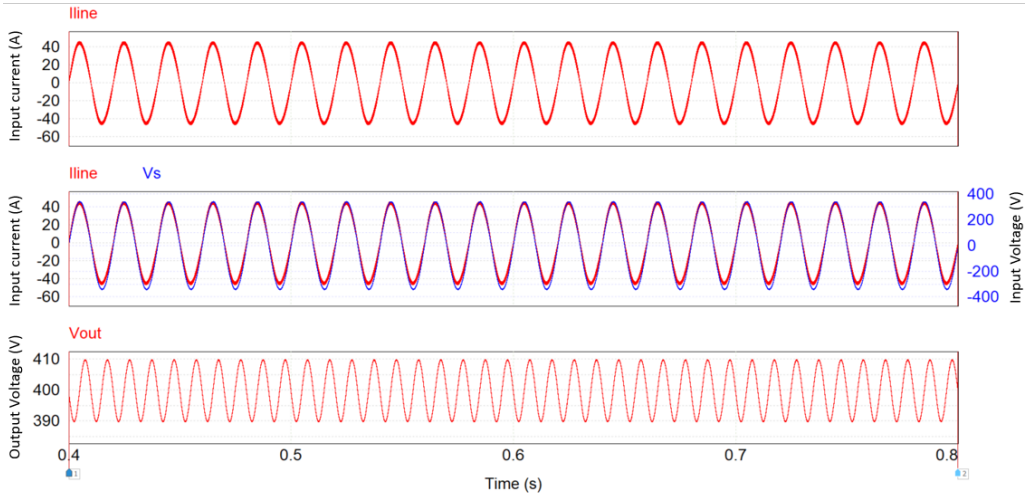


Figure 2.11: PSIM scheme



	X1	X2	Δ	P	PF	THD
Time	4.00000e-01	8.00000e-01	4.00000e-01			freq=50
Iline	-3.01031e-02	-3.36542e-02	-3.55106e-03	Only 2 curves ...	Only 2 curves ...	3.88276e-02
Iline	-3.01031e-02	-3.36542e-02	-3.55106e-03	7.55390e+03	9.98996e-01	3.88276e-02
Vs	-1.59944e-02	-2.13345e-02	-5.34009e-03			0.00000e+00
Vout	3.99346e+02	3.99344e+02	-2.48158e-03	Only 2 curves ...	Only 2 curves ...	2.89658e+06

Figure 2.12: Simulation results of functional and almost ideal converter

Concerning the EMI noise, the converter requires an EMI filter to fulfill the Class B standard. Following [26], [27], [28], a Differential Mode (DM) CLCL filter is inserted in the PSIM schematic along with a LISN network to evaluate the differential noise and chose the value of the filter components. Considering two X-capacitors of $0.5uF$ and a $0.5mH$ strongly coupled inductor, the DM voltage [29] captured by the LISN is depicted in Figure 2.13. The red and green traces are the DM noise, the blue trace is the Common Mode (CM) while the pink one is the FCC Class B limit. The system fulfills the standard for DM noise, while the CM noise is under estimated due to the perfect ground implemented in the simulation and the lack of realistic value to be inserted into the circuit. Nevertheless, a double CLCL filter of $1uF$ and a $0.57mH$ values is considered with a conservative approach, accounting also $1nF$ Y-capacitors for CM noise.

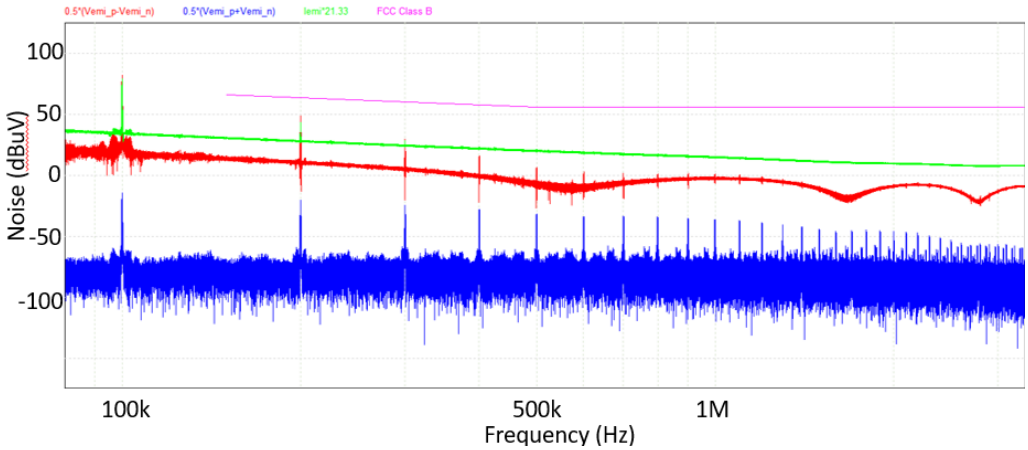


Figure 2.13: Simulation results of EMI noise

For the boost inductor, a custom wounded choke by UTK Component has been realized with an average $200uH$ inductance and $13m\Omega$ DCR, while at the output port a bulk capacitance with heterogeneous technology is exploited [30] for ESL reduction and a better current management. Four $1mF, 450V$ electrolytic capaci-

tors provide the needed capacitance, while a $12uF, 575V$ film capacitor handles the high frequency current spikes generated by steep di/dt characteristic of GaN devices. Moreover, some ceramic capacitor of few uF are deployed close to the GaN Module for bypass purposes.
Now that the main elements of the power system are known, the PSIM schematic is updated with all the principal parasitics (ESR and ESL). Moreover, the sensing conditioning and the digital delay are considered to obtain more realistic simulation results and PI coefficients values for the source code. For this purpose, the SmartCtrl tool is used to close the two feedback loops overcoming the generic Equation 2.3, 2.4. Once AC simulations are performed in PSIM environment to obtain the plant transfer function, SmartCtrl provides compensators solutions by means of open loop and closed loop transfer functions tunable by different corner frequency and phase margin. Figure 2.14 shows how the plant behavior is affected by the compensator in the current and voltage loop. On the left can be seen how the EMI filter doesn't allow to go beyond a $8kHz$ bandwidth and how the digital delay have small impact. Here it is crucial to have a flat phase response at $50Hz$ to compensate the slow oscillation of current reference. A corner frequency of $1kHz$ and 45° phase margin is obtained. For the voltage loop the main requirement is to obtain an open loop transfer function with a negative value (attenuation) in the amplitude bode diagram at $50Hz$. Here the compensator gives out a corner frequency of $23Hz$ and a phase margin of 50°. In Figure 2.15 can be noted how the system is well regulated and offers good results in term of PF (98%) and ripple of output voltage ($\pm 10V$@$50Hz$, $\pm 3V$@$100kHz$). The input current has still a good sinusoidal shape, but the discontinuity on the zero crossing rises up the THD at 8%. In order to reduce this value and to be compliant with the specification in Table 2.1 an improvement on the control algorithm must be achieved. [10] proposes an advanced technique consisting in reducing the time period where the PWM signals are kept in OFF state and implementing a soft-start sequence of the device which turns ON after the zero crossing event.

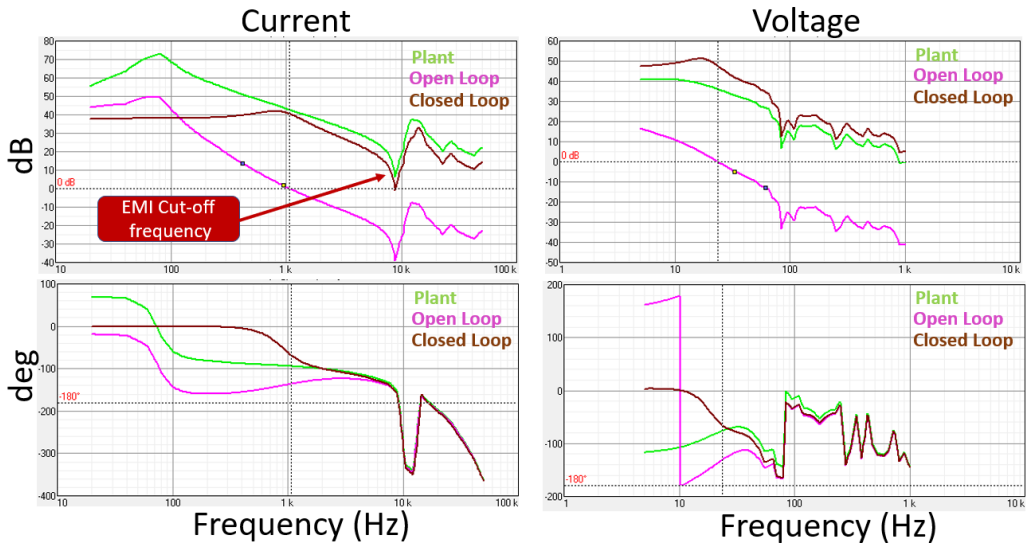
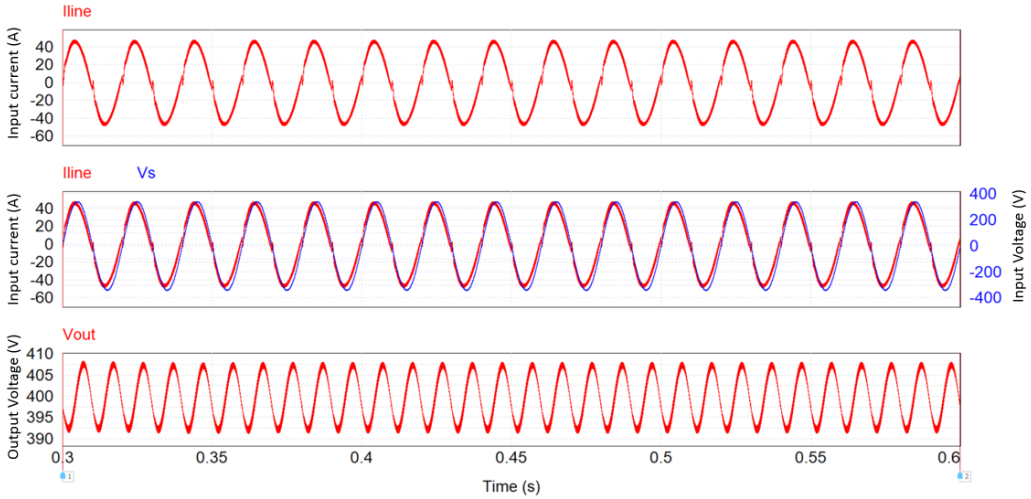


Figure 2.14: System transfer functions

The control strategy is implemented in the UCD3138 microcontroller handling the two feedback loops differently. Given the low bandwidth of the voltage loop, it



	X1	X2	Δ	P	PF	THD
Time	3.00000e-01	6.00000e-01	3.00000e-01			freq=50
Iline	8.27990e+00	8.29652e+00	1.66248e-02	Only 2 curves ...	Only 2 curves ...	8.39492e-02
Iline	8.27990e+00	8.29652e+00	1.66248e-02	7.57688e+03	9.79666e-01	8.39492e-02
Vs	2.65374e-03	-2.68272e-03	-5.33646e-03			0.00000e+00
Vout	3.97709e+02	3.97440e+02	-2.68748e-01	Only 2 curves ...	Only 2 curves ...	1.25617e+06

Figure 2.15: Simulation results of functional converter with parasitics terms

is fully handled by firmware, while the current loop is managed by the hardware state machine made of an Error-ADC (EADC), a PID filter and PWM peripheral. This forces to compensate the offset and the conditioning of current hall sensor directly in the calculation of reference current as depicted in Figure 2.16. The sign of the current error must be adjusted accordingly the input voltage polarity acting on the EADC setting, while the swap of ρ control law is done in the DPWM peripheral setting.

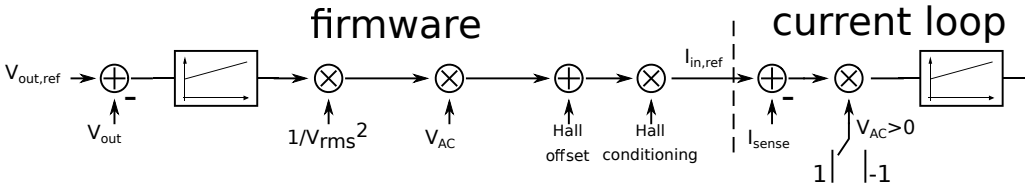


Figure 2.16: Control scheme with Hall sensor compensation (conditioning not shown)

These operations are executed by means of the software state machine shown in Figure 2.17. When the input voltage is close to zero, the zero-crossing states keep all the PWMs off until a stable polarity change is happened, on the other hand, in the high-voltage states the LF and HF legs are properly piloted as long as the input voltage is above a certain threshold, which cannot be too low to avoid current spikes but neither too high to lose control and decrease PF. A second state machine (Figure 2.18) is implemented to deal with the start-up and in the normal operative conditions. If the RMS value of the input voltage is above $100V$ for at least $100ms$ the system is initializes and enter in Ramp-Up state where the output voltage reference is slowly increased up to $400V$. The system is the nominal condition in PFC-ON state and under/over voltages are managed by Hiccup and Shutdown states. The temperature and over current protection are handled by fast analog comparators which acts directly to DPWM peripheral.

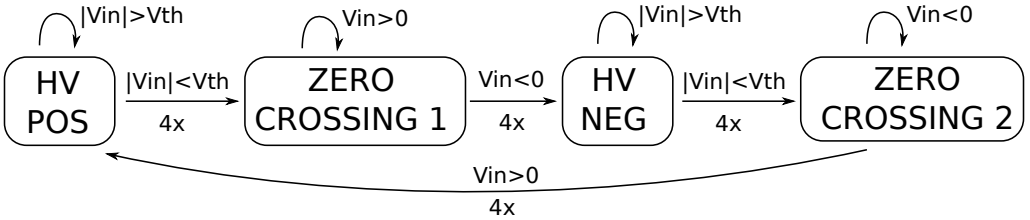


Figure 2.17: PWM state machine

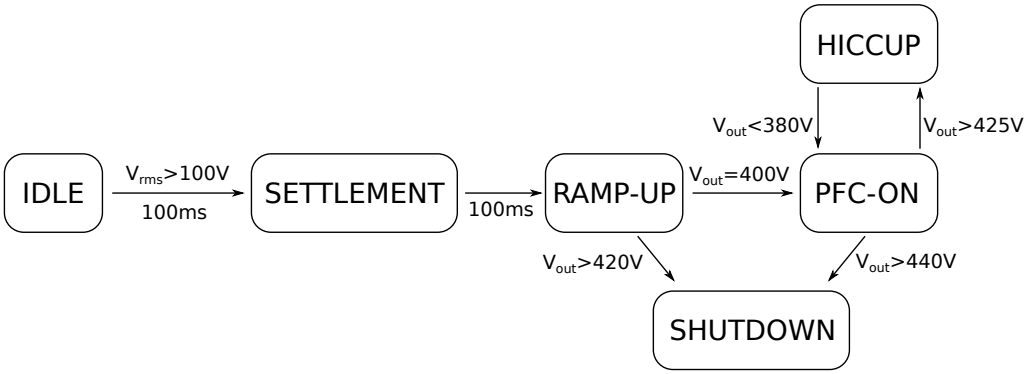


Figure 2.18: System state machine

2.1.4 Efficiency and Thermal assessment

The efficiency assessment and the validation of the cooling strategy is carried out through the Thermal Module add-on provided in PSIM. These models allow to evaluate both the conduction and switching losses of the switches, exploiting a look-up-table approach, thus avoiding long waveform integration during switching event as in Spice-like simulators. Conduction losses are calculated using the I_{DS}vsV_{DS} characteristics referred to 1^{st} and 3^{rd} quadrant at different temperatures, while switching losses are retrieved by inserting E_{ON}, E_{OFF} values for different I_{DS}, V_{DS} switching conditions and the adopted gate resistance. The junction temperature of the switches is computed since the models account also for temperature increase due to power dissipation and the thermal impedance of the switch in the actual set up. Nevertheless, it is important to consider the right thermal case-ambient thermal resistance. For the Silicon transistors of LF leg, the $3°C/W$ PA-T22-38E heat sink is employed in condition of natural convection. In the simulation this value is doubled since both transistor are on the same heat sink. In the same manner, the $0.49°C/W$ thermal resistance at $3.5m/s$ air speed of the 3-181808U heat sink by Cool Innovation used on the IMS board must counted twice. Moreover, since the heat of the GaN devices flows from the bottom part of the case, the contribution of the IMS insulation layer must be accounted. Considering the surface occupied by the GaN and a $3W/mK$ thermal conductivity of the insulation, a $0.31°C/W$ value is considered for each transistor. This value should not be doubled because the heat in the insulation remain confined in the surface subtended by the GaN case.
The simulation aided by thermal modules with $40°C$ ambient temperature shares the same configuration employed for Figure 2.15 in terms of parasitics and control scheme. In Figure 2.19 the conduction and switching power dissipations are shown in steady-state conditions of a single GaN transistor (Q5) and a single Silicon transistor (Q3) along with the devices' junction temperatures. Since Q3

and Q5 operate at very different frequencies, the evaluation of the characteristics at every cycle outputs steady value for Q5 and periodic for Q3. The spikes on Q5 switching losses are due to the C_{oss} discharge in hard switching regime, however the peaks values don't represent faithfully the real situation because the simulation doesn't employ non-linear and dynamic models capable to properly investigate such behavior. The junction temperatures, evaluated in the average form due to the slow time constants, provide a confident safety margin compared to the maximum rating. Figure 2.20 gives an outlook on the distribution of the losses in the system, where the HF leg is accountable for the 50%, with a majority of conduction losses, while the total efficiency estimated in the order of 98%. It is noteworthy also the non-negligible losses of the passive component, specifically the boost inductor, in spite of the benefits introduced by GaN devices.

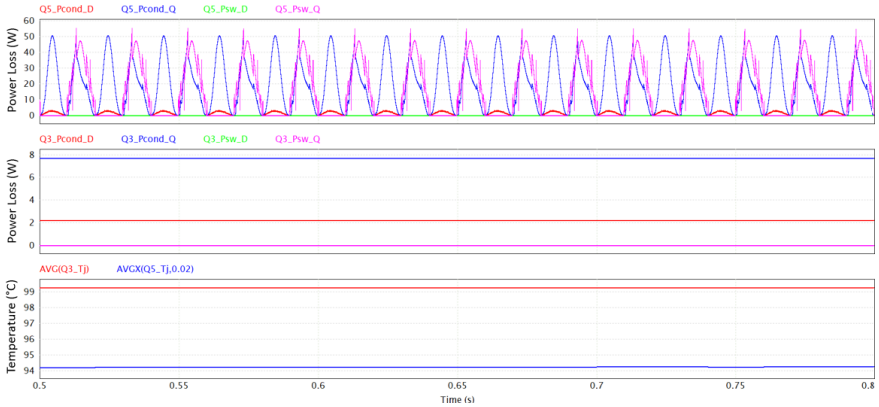


Figure 2.19: Simulation results with thermal modules

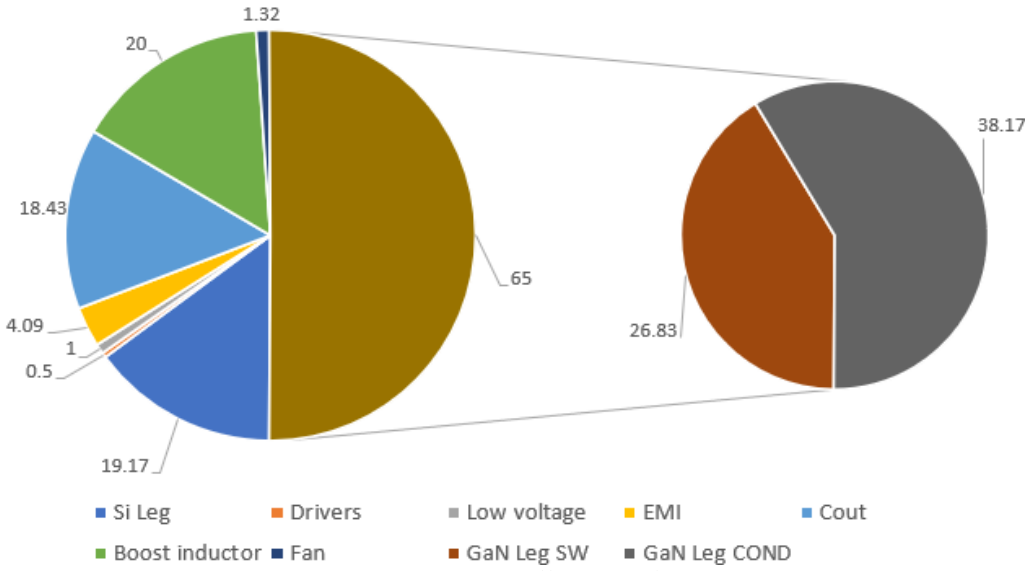


Figure 2.20: Overall power losses

2.2 DAB

Concerning the DC section of a typical dual-stage battery charger, among the different topologies investigated in [31], [32], the most promising are the CLLC [33] and Dual Active Bridge (DAB) [34] isolated converters. Despite CLLC converter guarantees a slightly higher efficiency level and a better light-load management than DAB, the latter still provides excellent performance with a shorter component list, a simpler control mechanism thanks to fixed switching frequency and a wider output voltage range to cope with different battery types. This section describes the detailed design, simulation and implementation of an air-cooled, $7.5kW$ Dual Active Bridge converter exploiting commercial $650V$ GaN switches, compact planar transformer and low ESL/ESR metal film capacitors. The isolated bidirectional converter operates at 200 kHz switching frequency, with an output voltage range of $200 - 500V$ at nominal $400V$ input voltage and a maximum output current of $28A$, with wide full-power ZVS region. The overall efficiency at full power is 98.2%. This converter is developed in particular for battery charging applications when bidirectional power flow is required. In Section 2.2.1 the DAB converter working principles are explained; in Section 2.2.2 the design procedure of the prototype is described, while in Section 2.2.3 the realized converter is shown along with results of experimental tests.

2.2.1 Topology

A schematic of a DAB converter is shown in Figure 2.21: two Full-Bridges (FB) are connected at the primary and secondary side a high-frequency transformer with a series input inductor that provides energy storage. The two FB operate typically at fixed switching frequency and 50% duty cycle and the power flow is controlled regulating the voltage applied to the series inductor by adjusting the time displacement (phase-shift) among the gate signals of the two FBs. The symmetrical structure allows to achieve bidirectionality, whereas the wide voltage range generation (either in buck and boost mode) is guaranteed by the possibility to impose alternatively the sum and the difference of input/output voltages across the inductor. The fundamental law of DAB converter is retrievable analyzing the waveforms in Figure 2.22. For the sake of clarity, steady-state operations, constant input and output voltages, the absence of a transformer, and single phase-shift (SPS) modulation are assumed. SPS means that the devices within the same FB are ON for half a period at fixed diagonals (for instance, Q1-Q4 share the same gate signal as well as Q2-Q3), while the useful phase-shift lies on the gate signals of devices of different FBs.

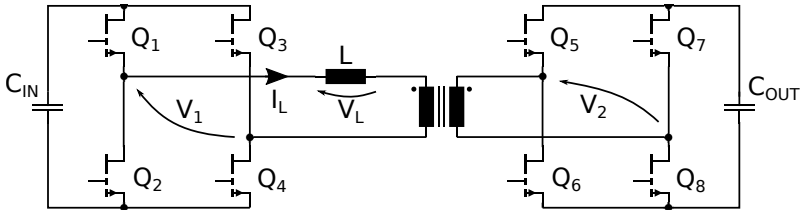


Figure 2.21: DAB converter schematic

Looking at Figure 2.22 from top to bottom the following waveforms can be

observed: gate signals of Q1 and Q5, the high-frequency voltage waveforms V_1, V_2, the inductor voltage and current V_L, I_L. The time period T_s is divided in 4 slots. Focusing on the inductor current, the equations for the first two time slots follow [35]:

$$\textcircled{1} \begin{cases} i_L(\phi) = i_L(0) + \Delta I_1 \\ \Delta I_1 = \frac{V_1+V_2}{L}\phi\frac{T_s}{2\pi} = \frac{V_1+V_2}{2\pi f_s L}\phi \end{cases} \tag{2.5}$$

$$\textcircled{2} \begin{cases} i_L(\pi) = i_L(\phi) + \Delta I_2 \\ \Delta I_2 = \frac{V_1-V_2}{L}\frac{(\pi-\phi)T_s}{2\pi} = \frac{V_1-V_2}{2\pi f_s L}(\pi-\phi) \end{cases} \tag{2.6}$$

where ϕ is the phase-shift between gate signals Q1 and Q5.

Since in steady state the average inductor current over the period is null and thanks to the symmetrical FB mode of operation, every inductor current value is repeated after half period with opposite sign, in particular:

$$i_L(\pi) = i_L(0) + \Delta I_1 + \Delta I_2 = -i_L(\pi) + \Delta I_1 + \Delta I_2 \tag{2.7}$$

Substituting and rearranging Equations 2.5, 2.6, 2.7 the results are:

$$i_L(\pi) = \frac{V_1\pi + V_2(2\phi - \pi)}{4\pi f_s L} \tag{2.8}$$

$$i_L(\phi) = \frac{V_2\pi + V_1(2\phi - \pi)}{4\pi f_s L} \tag{2.9}$$

where Equation 2.8 and Equation 2.9 are respectively the peak of I_L in buck and boost mode. At the input and output ports of the converter, the inductor current is rectified by FBs every half period, therefore the main harmonic component is at $2f_s$ and the power can be computed taking into account just half period.

$$\begin{aligned} P = P_{out} = P_{in} &= V_1\frac{1}{\pi}\int_0^\pi i_L(\theta)\,d\theta \\ &= \frac{V_1}{\pi}\left(\int_0^\phi i_L(\theta)\,d\theta + \int_\phi^\pi i_L(\theta)\,d\theta\right) \\ &= \frac{V_1}{\pi}\left[\frac{\phi(i_L(\phi) - i_L(0))}{2} + \frac{(\pi-\phi)(i_L(\pi) - i_L(\phi))}{2}\right] \\ &= \frac{V_1V_2}{2\pi^2 f_s L}\phi(\pi-\phi) \end{aligned} \tag{2.10}$$

Considering finally the turn ratio $n = N_2/N_1$ and the possibility to have negative ϕ (i.e. the gate signal of Q_5 precedes the one of Q_1), Equation 2.10 becomes

$$P = \frac{nV_1V_2}{2\pi^2 f_s L}\phi(\pi - |\phi|) \tag{2.11}$$

where $-\pi/2 < \phi < \pi/2$ because the maximum power in absolute term is obtained for $\phi = \pi/2$:

$$|P_{max}| = \frac{nV_1V_2}{8f_s L} \tag{2.12}$$

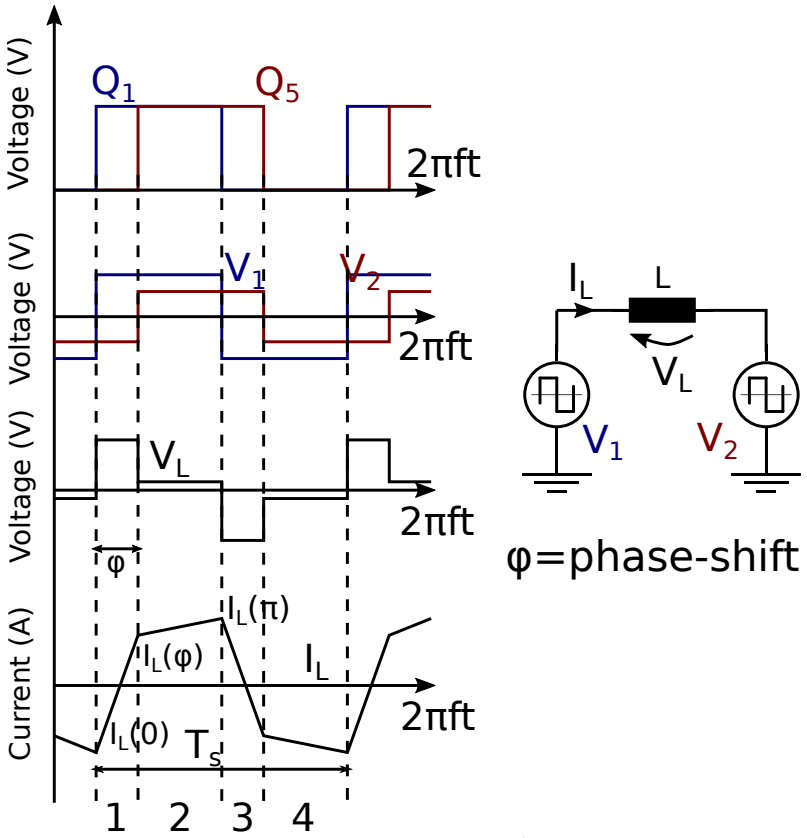


Figure 2.22: DAB waveforms

The DAB converter allows to obtain ZVS thanks to the inductance L that acts like a current generator charging and discharging the devices' output capacitances during the dead-time. Figure 2.23 shows what happens during dead-time when Q1-Q4 are set OFF and Q2-Q3 are going to be set ON on the FB at the primary side. The inductor forces a current that discharges C_{oss} of Q2 and Q3 while charges Q1 and Q4. When the energy of output capacitances is over, the devices go in reverse conduction acting as free-wheeling diode enabling the activation of Q2 and Q3 with an almost null drain-source voltage. This practically eliminates switching losses at turn ON. ZVS operation is assured when Equations 2.8,2.9 are both positive [36] and when the power balance

$$\frac{1}{2}Li_L^2 > 4\frac{1}{2}C_{oss}V^2 \tag{2.13}$$

is fulfilled. Equation 2.13 is valid in most of the conditions, in particular with WBG decives with low parasitics, while the condition on $I_L(\pi)$ and $I_L(\phi)$ are used to delimit the ZVS region.
Looking at Equation 2.11, there are three main components that determine the power delivery: the switching frequency f_S, the phase-shift ϕ and the inductance L. The major effect of ϕ and L reflexes on the current level [37]: an increasing phase-shift reflects on higher current when voltages are fixed, the same result can be obtained with larger inductance due to more energy storage capability. Such behavior leads to a wider ZVS region but also to higher RMS currents. Indeed, one disadvantage of DAB converter in SPS mode is the high level of RMS current on DC-link capacitors, because of the lack of an inductive filtering in the input and output sections. This can be mitigated exploiting different modulation techniques

like the Dual Phase-Shift (DPS)[38] that acts also to the duty cycle of transistor diagonals within the same FB, but this is beyond the aim of this chapter. The f_S has a huge impact on size of magnetic components, in particular on the high frequency transformer. Nonetheless, at high switching frequencies, accurate selection of core and winding technology and techniques is fundamental to avoid performance degradation due to excessive losses and large/uncontrolled parasitic effects. In this context, planar transformer technology is a very attractive solution for its potentiality to obtain small form factor, better power dissipation and accurate prediction and repeatability of parasitics. The latter is a significant advantage, since at high frequency parasitics play a fundamental role in the actual operation of the converter, as for example in the ZVS mechanism described before, where the leakage inductance of the transformer is a key parameter and then must be known with accuracy and must be highly repeatable in the transformer construction.

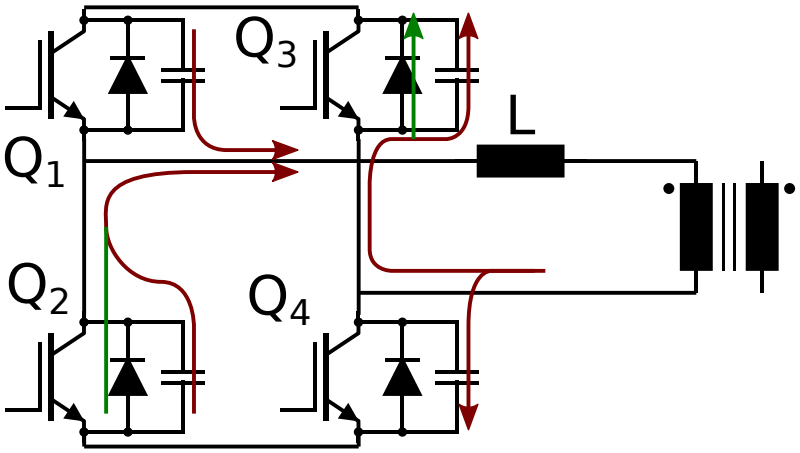


Figure 2.23: DAB ZVS mechanism

2.2.2 Converter Design

2.2.2.1 Dimensioning

In Table 2.4, the proposed specifications for the DAB converter are illustrated. The indicated high target value for the switching frequency $f_s = 200kHz$ that would enable high power density as discussed, can be addressed for these voltage and current ratings only by exploiting WBG semiconductor technologies to limit the switching losses and to enable higher operating temperature. The Table 2.3 displays a short list of commercially available WBG devices, potentially compliant for the design goals of Table 2.4. The GS66516B [13] provides the best performances in terms of parasistics and maximum current level, in particular the null reverse recovery charge of GaN devices, due to the absence of a body diode, typically allows to work at higher frequencies in comparison to SiC transistors. GaN switching time is smaller due to much lower input capacitance. Moreover the high-frequency design of the GS66516B lead-less package guarantees minimal stray inductance, facilitating the minimization of the switching times. The device GS66516B was adopted to implement the two full bridges of the converter. With the following calculations and simulations it will be demonstrated that 4 switches for every FB are enough to meet the specifications (no need of switch paralleling).

Table 2.4: DC/DC converter proposed specifications.

Vin	Iout max	Switching Freq.	Pout	Vout nom	Vout min/max
$400V$	$18A$	$200kHz$	$7.5kW$	$400V$	$200V/500V$

Considering Equation 2.11, the parameters to be identified for the converter operation according to its specification and the device maximum ratings are L and ϕ. In addition to what discussed in the previous section regarding power transfer and ZVS conditions, [37] shows how the selection of ϕ and L deeply impacts the control characteristic and the converter efficiency performance. Indeed, in SPS control technique, lower ϕ values in nominal condition allow to reduce RMS current on devices, transformers and DC-link capacitors, but makes the control too sensitive to small variation of ϕ, requiring very high resolution on the phase shift control. On the contrary, for higher values (close to 90°) the control is smoother, but losses increase, due to higher RMS currents. Considering the inductor, from Equation 2.11 the higher is the value of L, the higher the value of ϕ for a target power transfer [37]. Based on these considerations, a value between $20° - 50°$ is suggested for nominal operative full power condition, without exceeding the $15° - 75°$ range for the rest working cases. Imposing a $\phi = 20°$ in the nominal condition ($V_{in} = V_{out} = 400V, P_{out} = 7.5kW, f_{sw} = 200kHz, n = 1$) into Equation 2.11, the corresponding inductance value results $L = 5.3uH$. Once L is know, Table 2.5 can be computed, where I_{max} represents the peak value of I_L and is computed exploiting Equation 2.8 and Equation 2.9.

Table 2.5: ϕ and I_{max} values for $L = 5.3uH$ and $Pout = 7.5kW$

Vout	L	Phase Shift	Imax
$200V$	$5.3uH$	$48.8°$	$73.2A$
$400V$	$5.3uH$	$20°$	$21.1A$
$500V$	$5.3uH$	$15.6°$	40.1

Some other considerations can be carried out for the final choice of the value of the inductance. The maximum continuous current for GS66516B is $60A$ at $T_{case} = 25°C$ and $47A$ at $T_{case} = 100°C$. Since the converter is air-cooled, a maximum case temperature of $Tcase = 80°C$ can be envisaged. It must be noted that I_{max} of Table 2.5 is a peak value and thus should be compared with the maximum pulsed current of GS66516B, that from the data sheet is $120A$ (for a maximum pulse width of $50us$). Nonetheless, the very conservative approach to consider the continuous current limit also for I_{max} was taken for this prototype design, so I_{max} shouldn't exceed $50A$. With this requirements, the $Vout = 200V$ case of Table 2.5 is not acceptable. To investigate the feasibility to deliver $7.5kW$ at $Vout = 200V$, the $50A$ current limit value is forced into Equation 2.9 (peak current in buck-mode) and the obtained ϕ is substituted in Equation 2.11, getting the new inductance value $L = 1.8uH$. Such value is not a good choice for a couple of reason: 1) it is a value that may be smaller than the leakage inductance of the planar transformers [39], making the design unfeasible; 2) such low inductance value leads to a decrement of ZVS region [37] and bad exploitation of useful phase-shift range. This considerations ruled out the possibility to maintain full power

delivery at minimum output voltage (at least with the described conservative approach on maximum current rating of devices). Accepting a power de-rating at the lowest output voltages, some other considerations can be made for the selection of the inductance value. Figure 2.24, computed from Equations 2.8, 2.9 shows how a larger leakage inductance allows to meet the maximum current limit for a wider phase-shift range, increasing the converter controllability range, whereas for low inductance values the phase-shift range is heavily limited by the maximum peak current on devices. Thus, from this observations, it is decided to move from an inductance value of $5uH$ towards a value close to $8uH$. The final selection was $\phi = 35°$ for the nominal phase-shift and the corresponding inductance $L = 8.35uH$: the results for this final choice are listed in Table 2.6. It can be noted that $50A$ peak current on the switches is reached when $V_{out} = 267V$: this represent the minimum output voltage for full power delivery. At $V_{out} = 200V$ the row is empty because the phase-shift value required to obtain $7.5kW$ would be greater than $90°$. At $200V$ the maximum output power is $5.2kW$.

Table 2.6: ϕ and I_{max} values for $L = 8.35uH$ at $P_{out} = 7.5kW$

Vout	L	Phase Shift	Imax
$200V$	$8.35uH$	$--°$	$--A$
$267V$	$8.35uH$	$67°$	$50A$
$400V$	$8.35uH$	$35°$	$23.3A$
$500V$	$8.35uH$	$26.4°$	$32.5A$

Figure 2.25a depicts the computed trend of output power and peak current on switches for the entire output voltage span, highlighting the separation between constant power and constant-current regions.
In such configuration, Figure 2.25b shows the ZVS limits for the input and output FB, where ZVS operation is guaranteed in the region within the two boundaries, that is when $i_L(\phi) > 0$ for output full-bridge and $i_L(\pi) > 0$ for input full-bridge, plus a contribution obtained from Equation 2.13. Nevertheless, the latter has a negligible effect on the boundaries above $P_{out} = 1200W$, due to the low value of C_{oss}: therefore, the nominal condition $V_{in} = V_{out}$ provides always soft switching beyond such threshold. For $P_{out} = 7.5kW$, ZVS condition is above a phase-shift of $25°$; since such value is lower than the phase-shift value for $V_{out} = 500V$ (Table 2.6), this means that soft switching is always verified in the actual design for nominal power. Moreover, also for $V_{out} = 200V$, $I_{max} = 50A$ ($60°$ phase-shift value), ZVS condition is possible, since the output power is $5.33kW$. In Figure 2.26 the output power is related to the phase-shift and output voltage with threshold plane at $7.5kW$.

Once these parameters have been selected, the converted has been modeled and simulated in PSIM simulation environment. These simulations were also used for the correct selection and sizing of the other components of the converter. Concerning the identification of the DC-link capacitors of both bridges, by allowing a $10V$ voltage ripple with the maximum current value flowing in the switches ($50A$), the resulting computed capacitance value is $12.5uF$. Values in the range of tens of uF allow the employment of film capacitors, which have higher voltage rating and less parasitics than electrolytic technology. DC-link capacitor RMS

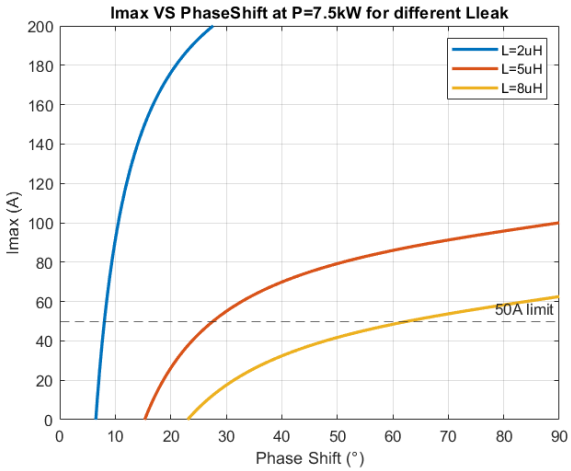
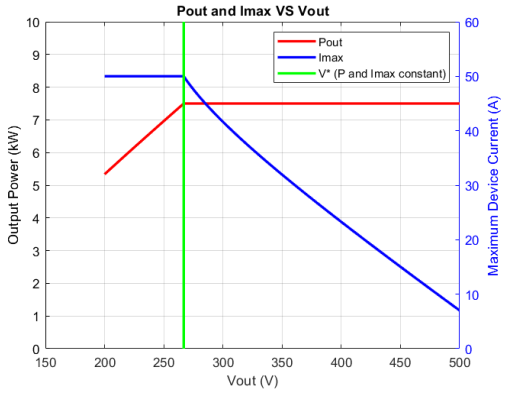
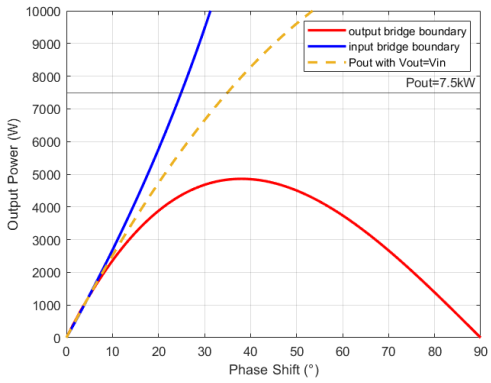


Figure 2.24: I_{max} VS Phase-shift at maximum power for different leakage inductance



(a) $P_{out,max}$ and device peak current vs V_{out}



(b) ZVS limits

Figure 2.25: Design characteristics

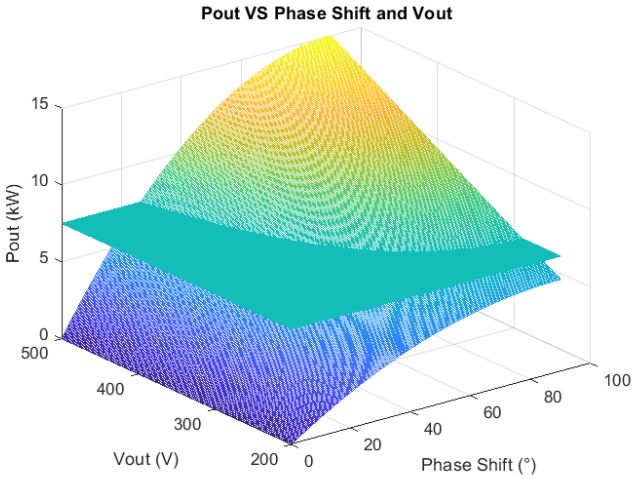


Figure 2.26: Output Power vs output voltage and phase-shift

current, ESR and ESL must be carefully assessed in DAB converter design because of high values of circulating currents in SPS modulation, along with unfiltered RMS currents in both input and output ports. The most stressful operating point is when both the current and power are at their maximum values, and this happens for $V_{out} = 267V$, where constant current and constant power regions collide. In this condition, the time-domain PSIM simulations show how the RMS currents on output and input capacitor are $19.8A_{RMS}$ and $28.2A_{RMS}$, respectively. These values set a condition for the maximum ESR of capacitors. As far as regarding the ESL, this also must be minimized to avoid high voltage spikes due to the very fast commutations of the GS66516B switch, with corresponding di/dt as high as $1.3A/ns$. These considerations lead to use multiple film capacitor in parallel in order to share the RMS current and obtain a lower equivalent ESL. Three TDK B32776P6226K000 polypropylene film capacitors are used: their main characteristics are $C = 22uF, V_{max} = 630V, I_{RMS} = 17.5A_{RMS}, ESL = 13.2nH$. Even with a wise selection of capacitors, the voltage spikes and ringing on the output voltages are not compatible with the direct connection to a battery in a battery charging operation. Thus, an additional light LC filter was inserted at the output to remove the voltage spike and ringing and facilitate an output current control strategy.
A high frequency (i.e. $200kHz$) transformer in planar technology was custom made by Himag Planar with 1:1 turn ratio. In contrast to wounded transformer, the planar architecture provides an easier thermal management, the low profile perfectly suites the typical charger form-factors and its realization increase reliability and a precise control and repeatability of parasitics as the leakage inductance.

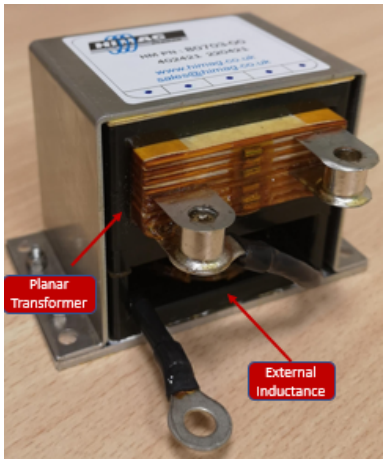


Figure 2.27: Planar Transformer with the external power inductor

Table 2.7: Planar transformer specification

Pout	Freq	Magn. Ind.	Total input Ind.	Turn ratio	In/Out current	In/Out voltage	Dimensions
$7.5kW$	$200kHz$	$1.17mH$	$8.5uH$	8 : 8	$36A_{RMS}$	$200V - 500V$	94x53x65mm

The total selected input series inductance $L = 8.35uH$ was obtained as the sum of the transformer leakage inductance and external power inductor in series to the

primary. The realized component is depicted in Figure 2.27: the external inductor is realized in the same enclosure of the transformer, practically doubling the transformer volume. The transformer characteristics are shown in Table 2.7. The specified RMS current comes form the simulations. A realization of the transformer with a leakage inductance equal to the target value of $L = 8.35uH$ would have minimized dimensions and maximized efficiency (the estimated inductor power loss are $34W$ against the $27.6W$ of the transformer for full power operations), but was not possible, since to obtain such leakage inductance the deterioration of the magnetizing inductance would have been too large. Nonetheless, the transformer + inductor component is still very compact (94mm x 53mm x 65 mm) and its predicted efficiency at full power very high (99.2%).

2.2.2.2 Simulations of relevant working points and efficiency evaluation

In Figure 2.28, the computed relationship between output voltage and output current of the converter is shown. Different relevant operating points are highlighted and selected for simulations. As discussed before, point A, B and C are at maximum output power, whereas in D the output power is limited by maximum peak current on the switches ($50A$). In Figure 2.29, the primary current and the voltages across the primary and secondary windings are obtained through PSIM simulations for each operating points. The different shape of the current allows to distinguish buck-mode (Point B, C), boost-mode (Point A) and nominal (i.e. $V_{prim} = V_{sec}$, Point B) conditions. The main results are summarized in Table 2.8: as expected, the RMS and the peak device current values are the highest in the C case. Clearly, point B is the most convenient point in terms of RMS currents, controllability and efficiency; on the other hand, point C is the most stressful operating condition for the converter, due to high circulating currents.

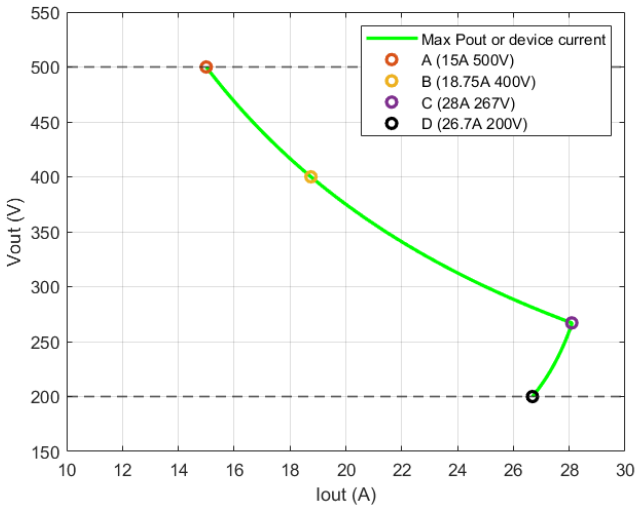


Figure 2.28: DAB converter Vout VS Iout chart

The thermal/efficiency assessment of the converter in steady-state condition is also computed in PSIM simulations by the means of Thermal Modules.

In Table 2.9 the computed power dissipation values of all the 8 GaN devices (4 in the primary side bridge , 4 in the secondary side bridge) and their maximum junction temperatures are listed with the losses of the main passive components

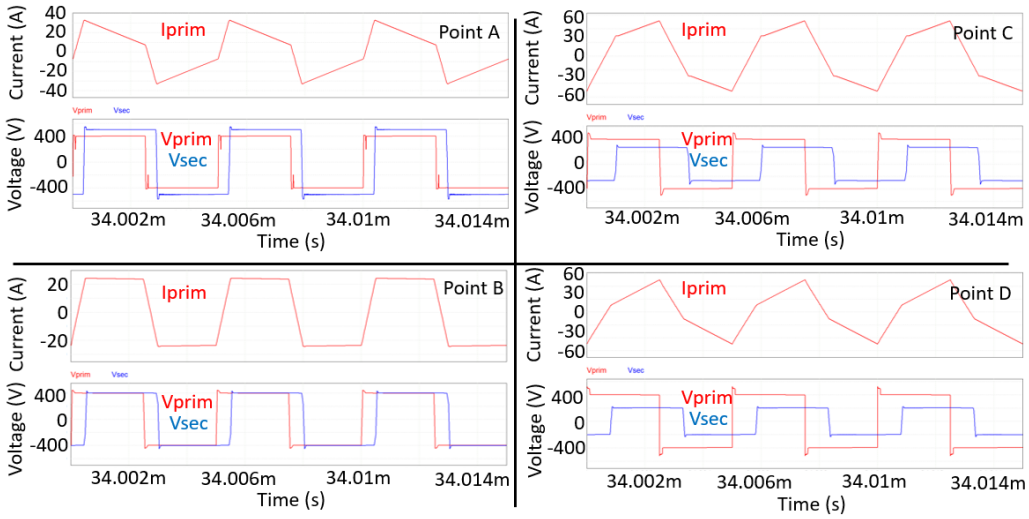


Figure 2.29: Primary current and primary/secondary voltages for the four operating points specified in Figure 2.28

Table 2.8: Main simulation results for the operating points specified in Figure 2.28. The power dissipations in the first two columns are comprehensive of all the four switches of the input and output full bridge (FB), respectively.

Point	**Phaseshift**	**Vout**	**Iout**	**Pout**	$I_{L,max}$	I_{RMS}
A	24.6°	$500V$	$15A$	$7.5kW$	$33A$	$20.9A$
B	35°	$400V$	$18.75A$	$7.5kW$	$24A$	$21.9A$
C	67°	$267V$	$28A$	$7.5kW$	$50A$	$34.4A$
D	60°	$200V$	$26.7A$	$5.33kW$	$50A$	$30.4A$

within the power stage (capacitors, inductance and transformer, considering all their known parasitics). The ambient temperature used in the simulations is $40°C$.

Table 2.9: Main results of thermal simulations for the operating points specified in Figure 2.28. The power dissipations in the first two columns are comprehensive of all the four switches of the input and output full bridge (FB), respectively.

Point	$P_{diss,cond}$ / $P_{diss,sw}$ **input FB**	$P_{diss,cond}$ / $P_{diss,sw}$ **output FB**	T_j **device prim/sec**	P_{loss} **Transformer**	P_{loss} **Inductor**	P_{loss} **Capacitor**	**Efficiency**
A	31.12/ 30.4W	46.4/ 38W	64/73$°C$	12.04W	28.74kW	0.44W	98.1%
B	39.6/ 22.4W	42/ 21.6W	64/65$°C$	12.52W	29.53W	0.4W	98.2%
C	139.6/ 56.4W	124.8/ 17.32W	116/95$°C$	20.24W	42.17W	1.9W	95%
D	101.2/ 53.6W	102.8/ 7.20W	100/74$°C$	17.5W	37.69W	1.47W	94.7%

The efficiencies reported in Table 2.9 are in line with the state of the art for DAB converters in GaN technology for charging applications reported in [40], [41] and [42]. The main difference is that the proposed converter delivers twice of the power with respect to the one describe in [40], [41] and [42]. The converter efficiency is very high in the conditions close to the nominal one. Indeed, as expected, Point B is the most efficient condition for the DAB converter due to the unit voltage gain, where the RMS current are minimized under same power condition. The maximum junction temperature reached in the worst condition (Point C) is $116°C$, which guarantees a large safety margin from the maximum rating of $150°C$. The converter is designed to operate at full power at up to $65°C$ of ambient temperature. Particularly interesting is the Point D, where the switching losses in the secondary side bridge are notably low. As described in Figure 2.30, this is due to an almost ZCS behavior, since the drain current of switches Q5/Q8 is near to zero at ON and OFF transition, whereas Q1/Q4 manages higher current level at commutations. Finally, Figure 2.31 shows how the losses are distributed on the overall system for Point B. For these computations also the losses of device drivers and low voltage controlling and sensing circuitry that is described in the next section have been budgetary considered. It is evident that transistors losses account for more than 70% of total losses, where 2/3 of it is due to conduction losses, while the leakage inductor overcomes the transformer losses. If the inductance value could be embedded directly into the planar transformer, the efficiency gain would be significant. This graph also points out that the selection of $200kHz$ switching frequency is a good compromise between compactness and performance for this voltage and current levels: at lower current/voltage levels this GaN technology can switch up to $500kHz$, but for the I/V levels of this circuit the switching losses at such high frequency would significantly decrease the efficiency. Moreover also the core losses in the transformer would increase significantly at higher frequencies.

From the losses breakdown shown in Figure 2.31 it is evident that the ZVS condition is very important for the converter efficiency maximization. Indeed, the

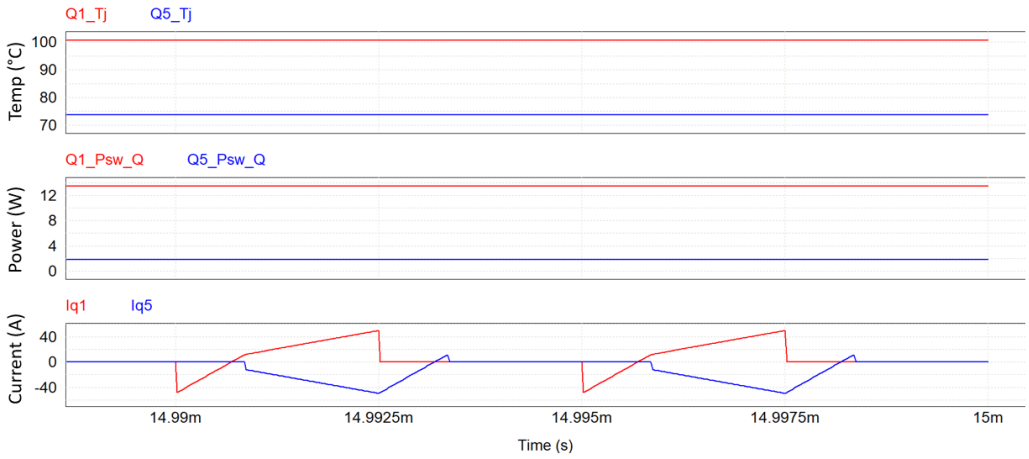


Figure 2.30: Junction temperatures, switching power losses and drain current of Q1 and Q5, with 40°C ambient temperature at Point D, Pout = 5.33kW.

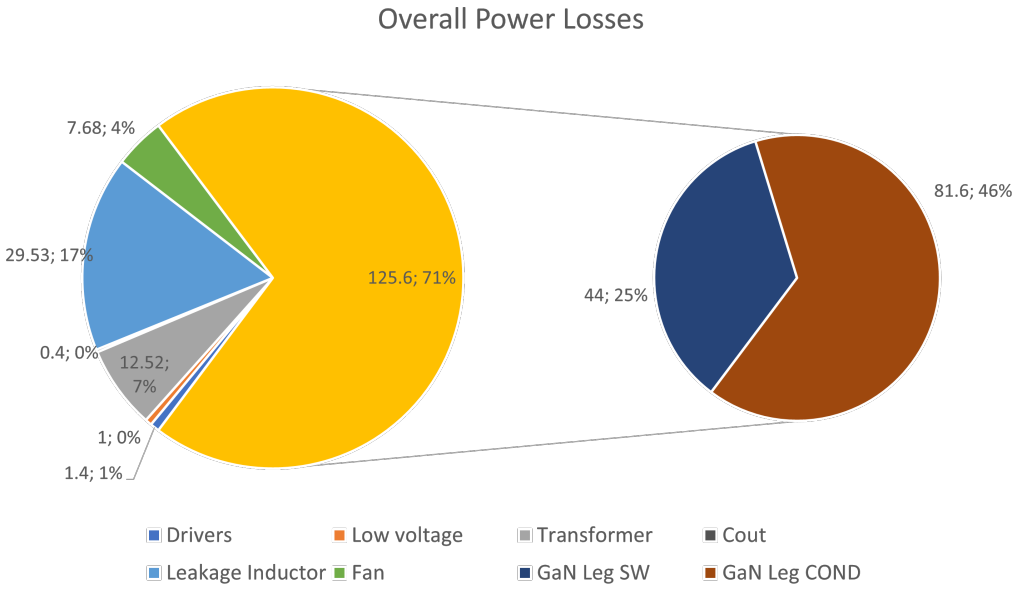


Figure 2.31: Distribution of power losses in the overall system at Pout = 7.5 kW, Point B.

elimination of turn ON switching losses assured by ZVS, makes the switching losses contribution about 1/2 of the conduction losses' ones, even though the switching frequency is high. It has to be mentioned the considerable losses of the magnetics, with particular attention on the leakage inductor contribution. Higher switching frequency would been feasible by the GaN devices, but at the price of additional increment of magnetics inefficiency. For an accurate evaluation of the actual ZVS commutations implemented by the component selection, SPICE model of GaN transistor and behavioral model of drivers are employed to perform accurate time-domain non-linear dynamic simulations in the Advanced Design System (ADS) simulation environment, a circuital simulation tool by Keysight Technologies. Figure 2.32 shows the voltage and the channel Drain-Source current of the the switches (lower charts) and gate signals (upper charts) of each device in the DAB converter, during the turn-ON commutations for operative point C. It can be noted how, for every switch of the DAB, at the switching-off of the complementary transistor (i.e. during the dead-time (100ns)) the V_{DS} drop to zero, allowing a lossless switch-ON commutation of the transistor: V_{DS} and I_{DS} (channel conductive current) and the transistors do not overlap in the lower charts.

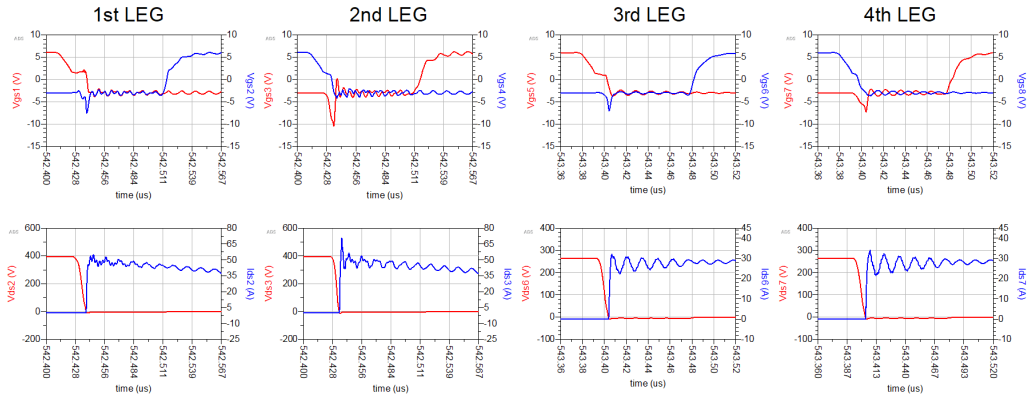


Figure 2.32: ZVS tunr-ON condition is met for every transistor in worst-case scenario of Point C

2.2.2.3 Architecture of the prototype converter

The converter architecture follows the same modular approach of the AC/DC converter described in Section 2.1.2.2 where the three modules constituting the system are the Mother Board, the Control Board and GaN Daughter Module. The schematic of the entire converter is shown in Figure 2.33. To shape the input and output full-bridges, 4 half-bridge GaN modules are used, while the control board is opportunely modified to account the different conditioning of sensed signals and provide 8 PWM signals. In particular, the UCD3138 feature to generate 4 PWM signal couples at high time resolution (250ps) interlocked by an embedded phase-shift mechanism turns out to be very useful. The Mother Board is a 265x223mm FR4 PCB with 2mm thickness with 4 layers of 2oz of copper to withstand high current levels of the power section. In addition, wide copper exposed area, either on top and bottom layers connected by thermal vias, is arranged for a better thermal conductivity of the transformer. The low voltage section is populated by sensors and conditioning circuits of analogue signals and by PWM signal traces too. Power and low-voltage sections reference grounds are kept separated by the commercial

isolated DC/DC AE40-EW-S12 by CUI that acts as auxiliary supply providing $12V$ and $3.3A$ maximum. This auxiliary supply is largely over-sized for this application and was mainly selected for its availability: the dimensions of this functional block can be widely reduced with a custom design. In the layout design $1.6mm$ and $4.5mm$ of clearance and creepage distance are applied in conformity with the IEC 61010-1 and IEC 60335-2-29 standards. Concerning the sensing section, the controller acquires 10 analog signals: 4 currents, 2 voltages and 4 temperatures, plus a flag signal for over current protection.
Concerning the first characteristics, the primary current (I_{prim}), the input current (I_{in}) and two output currents (I_{filter}, I_{out}) are sensed. As described in Figure 2.33, the difference between I_{out1} and I_{out2} is the position of the sensor respect to the capacitance of the output filter; in particular. For the current flowing through the primary and the leakage inductor, the ACS732KLATR-75AB-T [43] Hall sensor by Allegro is employed. This sensor is able to sense a $75A$ bidirectional current with a $1MHz$ bandwidth. Its output is opportunely scaled by an Op-Amp in differential configuration. The sensor provides a fast flag signal that is set to trigger when the peak current goes beyond 65A. For I_{in} and I_{out}, the MLX91221KDC [44] Hall sensor by Melexis is used. Here, just the DC component is relevant, so high bandwidths is not required. The maximum current sustained is 38A with is sufficient to acquire the $28A$ of I_{out} in the worst case ($P_{out} = 7.5kW$, $V_{out} = 267V$). Regarding I_{filter}, the ACS724KMA Hall sensor by Allegro is used allowing $65A$ bidirectional current sensing. Since the current before C_{out} has a strong harmonic content the employment of a sensor with wider input range is required. One signal between I_{filter} and I_{out} sensing is provided to the uC by the position of a jumper. The choice can be made depending on a much fast should be the current feedback loop since I_{out} gives a slower response than I_{filter}.
All the low voltage output signals are conditioned by an Op-Amp in differential configuration. Voltages at the input and output ports are sensed by two resistive divider. Since electrical isolation must be kept between high and low voltage section, the output of divider is provided to the ACPL-C87A [45] Broadcom isolated OPAMP with dual power supply. The V_{out} signal is used to close the voltage loop, while V_{in} is used for OVP and also for feed-forward operation.
The temperature signals provide information about GaN transistors case temperature.

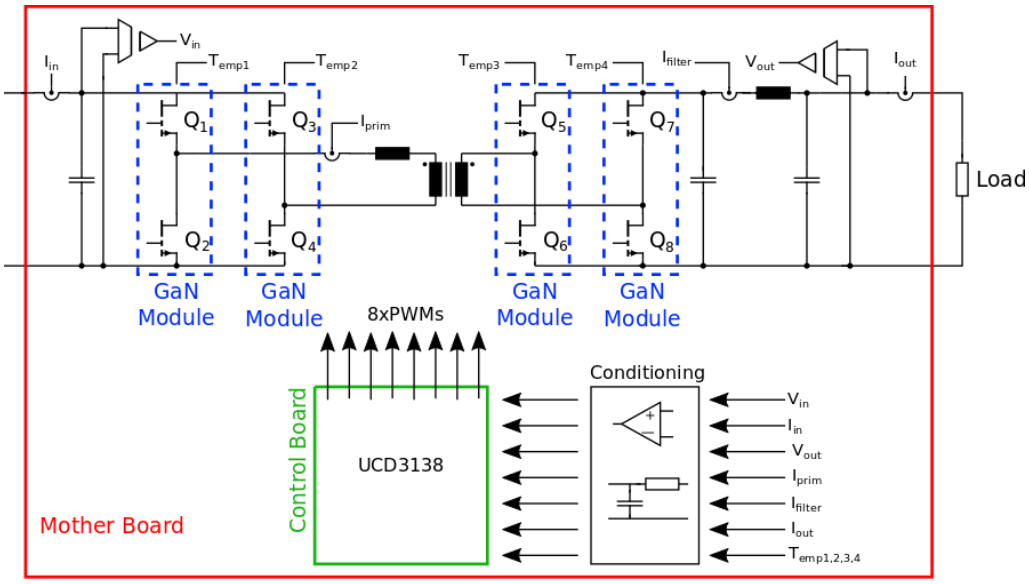


Figure 2.33: Simplified schematic of the entire converter

2.2.3 Converter implementation and experimental Results

In Figure 2.34 the converter prototype (230x348x107 mm^3) is displayed highlighting the main hardware sections. As discussed before, the prototype design was not optimized for space saving, but for ease of testing and tweaking. In the picture, a large part of the space is occupied by the bulky auxiliary power supply (largely over-sized), the fans (largely over-sized) and the heat sink of the GaN IMS board. All these components may have much smaller dimensions in a final implementation of the converter for on-board battery charging application: it his case the cooling could be probably liquid and a more optimized 3D layout can be produced. The compactness of the key components that are the GaN Daughter boards, the magnetics and the DC-link capacitors is the important data in this regards. The functionality of the prototype is tested through the setup schematized in Figure 2.35a and implemented as in Figure 2.35b. This set up is power-limited, so unfortunately the converter cannot be tested at full power. Further testing will be done in a successive phase. The input voltage is provided by two DC-supplies in series connection: the $840W$ AIM-TTI CPX400D and the $1.54kW$ Delta Elektronika SM 70-22. The maximum input power available is $1.33kW$ due to the limitation of the input current ($7A$) of CPX400D. The scope is a MSO-56 Tektronix, the load consists of power resistors in series-parallel connection, while the master controller is a laptop directly connected to the Control Board via a PMBus interface forcing a fixed phase-shift value to perform tests in open-loop conditions. Regarding the acquisition of primary current, primary voltage and secondary voltage, two differential active voltage probes (Aaronia DP1 - DC to $40MHz$, DP25 CHAUVIN ARNOUX - DC to $25MHz$) and a wide-band DC/AC current probe (Keysight N2783A, $30A_{RMS}$, DC to $100MHz$) are used.

Table 2.10 illustrates the measured prototype performances in three different conditions in terms of input/output voltages and load resistance. Also in these operating conditions that are largely different from the nominal ones, the measured converter efficiency is remarkably high (even though, obviously, some

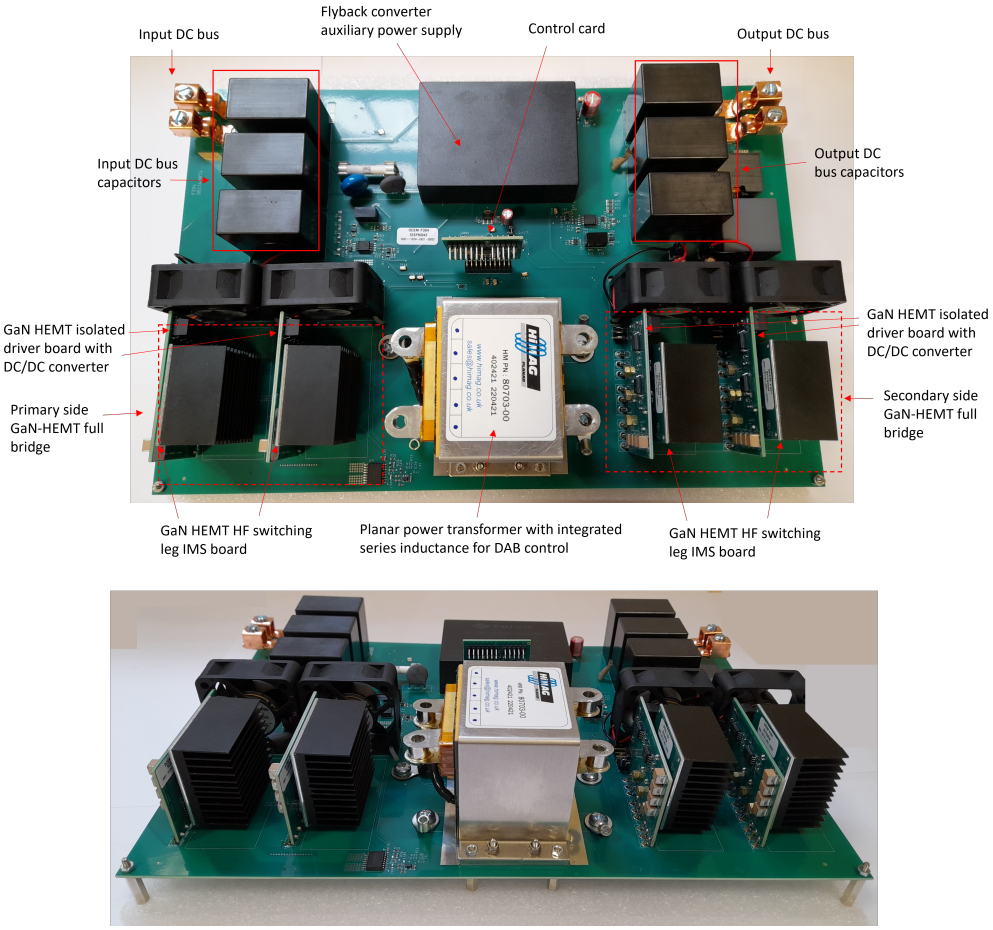
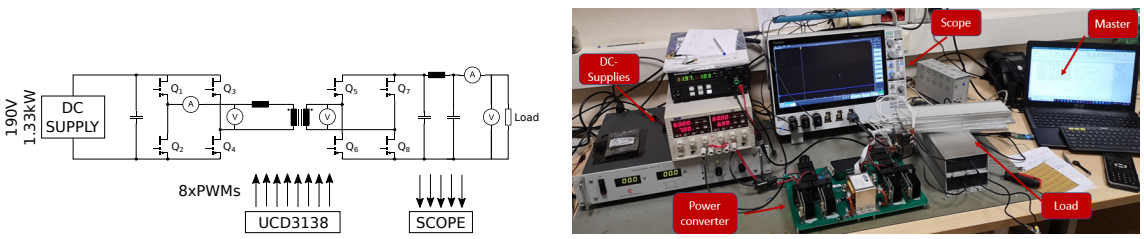


Figure 2.34: Dual Active Bridge prototype



(a) Schematic (b) Implemented

Figure 2.35: Measurement setup for prototype functionality test at reduced power

percentage point less than what expected in nominal conditions). Considering the last operating point of Table 2.10, it is interesting to notice how in Figure 2.36 the measured primary/secondary voltages and primary current are in very good accordance with PSIM simulations. This indication of the accuracy of the simulation predictions gives a good confidence that the simulated performance of Table 2.8 and Table 2.9 at full power may be actually delivered by the prototype. In the waveforms of Figure 2.36, it is noteworthy how the measured secondary voltage displays larger spikes during the transitions than the primary voltage. This is basically due to the effect of intra-windings capacitance of the transformer at the secondary stage, while the effect of the same capacitance at primary is filtered by the external series inductance. Nevertheless, the effect of such parasitic capacitance doesn't represent a concern for the DAB operation, since the spike amplitude is limited and no time-extended oscillations are present in the high-frequency voltage and current waveforms.

Table 2.10: Measurement results for three different input voltages

V_{in}	Phaseshift	I_{in}	P_{in}	R_{out}	V_{out}	I_{out}	P_{out}	eff
$100V$	30°	$3.84A$	$384W$	22Ω	$90.2V$	$4.1A$	$369.8W$	96.3%
$150V$	40°	$5.03A$	$754.5W$	11Ω	$88.4V$	$7.96A$	$703.6W$	93.2%
$190V$	25°	$6.43A$	$1222W$	24.6Ω	$176.2V$	$6.7A$	$1176.6W$	96.3%

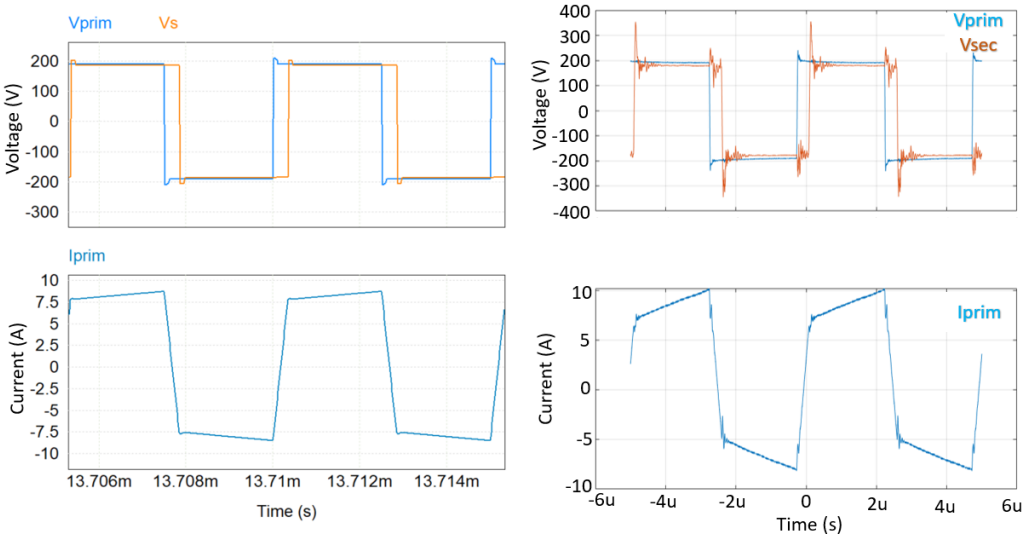
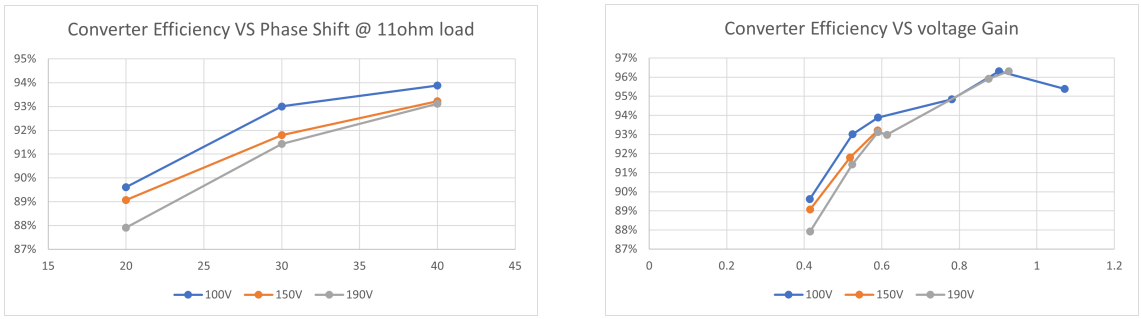


Figure 2.36: Comparison between simulation (left) and measured (right) value of Primaray/secondary voltages and primary current in the $V_{in} = 190V$, $R_{out} = 24.6\Omega$ condition

Additional interesting measured data are shown in in Figure 2.37, where the trend of converter efficiency is assessed varying the phase-shift control. Performance improvements seem be linked to higher phase-shift values in Figure 2.37a: however this is true just because in the tested conditions higher phase-shift coincides to a voltage gain (V_{out}/V_{in}) closer to unity: as described in Figure 2.25b, unity voltage gain is the best working condition for the DAB.

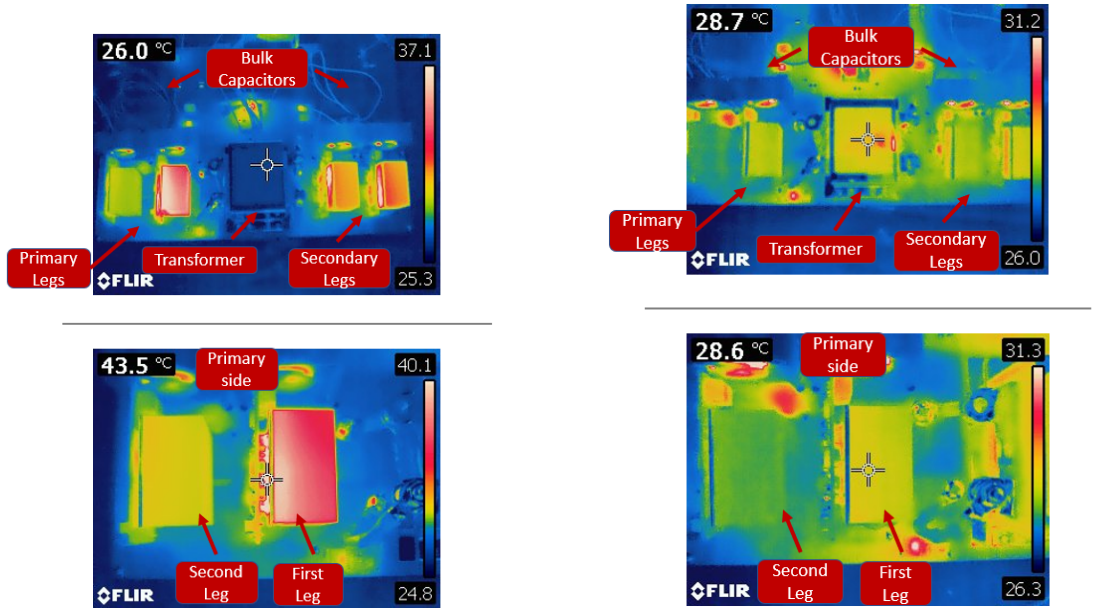
Finally it is also interesting to show some pictures provided by the infrared thermal camera that were used during the prototype first assembly and characterization to identify eventual hot spots that may indicate assembly issues or

design shortcomings. Figure 2.38 correspondent to the converter operating in the $V_{in} = 100V, Rout = 22\Omega$ condition, provides an insight of the temperature rises of different parts of the circuit for two different phase-shift control values. The transformer (comprehensive of external inductance) and bulk capacitors remain at ambient temperature while the GaN modules (mainly their heat sink are visible) show a modest temperature variation. Looking at the magnification of the primary side FB in the lower part of the figure, it is possible to appreciate some additional thermal stress of the first leg compared to the second one: from this slight asymmetry in the temperature, it was possible to identify an issue in the layout of the ground loop of this leg in the mother board, that induced an higher stray inductance: this will be fixed in the successive realization of the board to further increase the efficiency performance.



(a) Efficiency vs Phase-shift for fixed 11Ω load (b) Efficiency vs Voltage Gain

Figure 2.37: Efficiency results for $V_{in} = 100V, 150V, 190V$



(a) Phaseshift=35°C (b) Phaseshift=30°

Figure 2.38: Thermal images of the prototype during $V_{in} = 100V$, $R_{out} = 22\Omega$ working operation

2.3 Conclusions

The design of a bidirectional and high efficiency 7.5kW single-phase AC/DC converter exploiting 650V GaN technology for charger application has been presented in terms of chosen topology, dimensioning, proposed control algorithm and performances. The employment of GaN devices has unlocked the possibility to perform CCM in the Tote-Pole topology enabling a simpler control management leading to better input current THD and PF. The PSIM simulations integrated with thermal modules and the described control loops depicts an efficiency at full load of 98% with a 50$^{\circ}C$ margin on devices junction temperature. This confirms the feasibility of the project which can be assessed in future steps directly on the realized converter. The lack of measurement results is due to the development of control scheme into the UCD3138 controller that has required a considerable extra scheduled time in order to properly set the internal hardware state-machine.

Then, a 7.5kW DC-DC DAB converter has been designed and implemented exploiting 650V GaN technology and planar transformer technology at 200kHz switching frequency. The converter operates in full power mode from a nominal input voltage of 400V to a variable output voltage in the range $267V - 500V$. For the $400V - 500V$ output voltage range the efficiency is larger than 98%. The proposed prototype converter is air cooled and its overall layout has not been optimized for space, but the dimensions of the power bridge modules, of the magnetics and of the DC capacitors show the potentiality of the selected technologies for a very high volumetric power density. This makes this technological solution very attractive for automotive battery charging applications

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Chapter 3

Design of a 350kW DC/DC converter for battery emulation testing

The fast growing of the market of hybrid and electric vehicles requires the exploitation of advanced electronic test benches for both the development and product testing of automotive components. The battery emulator is a key instrumentation for the characterization and development of automotive batteries, electronic chargers, traction inverters, DC-DC converters, E-motors and E-axles. Wide voltage and current ranges, high power, fast dynamics and high accuracy are the characteristics that guarantee the flexibility required to cover a wide range of application scenarios. In addition, high power density and overall compactness are also extremely valuable. In this chapter, the design and implementation of a battery emulator with state-of-the art performance is described. Cutting edge performance, flexibility and compactness are obtained by exploiting 1200-V SiC modules, high switching frequency, planar transformer technology, suitable topology solutions and fast digital control strategies. The implemented battery emulator is a liquid-cooled, bidirectional converter with galvanic isolation capable of 350 kW continuous output power, output voltage range 48-1000 V, continuous output current up to 800 A (1600 A peak), voltage/current rump-up time below 10/2 ms and current/voltage accuracy. The entire instrument is implemented in a standard full-height 19-inches rack cabinet.

3.1 Introduction

Nowadays, the strong drive towards electrification in the automotive sector made electronic power converters and traction batteries key components of the energetic transition, gaining investments from industrial organizations and attentions from the scientific community. In particular, the development of new generations of power converters with enhanced characteristics in terms of power density, efficiency and dynamic response is fundamental to extend the performance of hybrid (HEV) and electric vehicles (EV). High power bidirectional DC-DC converters are used in several parts of the vehicle: as regulators between the high voltage and low voltage DC buses, as voltage booster between the battery pack and the high voltage bus, in on-board and off-board battery chargers and also for lower power applications to drive different points of load in the vehicle. Switching-mode inverters are used for traction and energy recovery in both EV and HEV. Also the

battery centrality is evident considering that it can represent up to the 50% of an Electric Vehicle (EV) value [1]. Several technologies are available in the market, as Lead-Acid, Nichel, and Lithium-ion [2] (even though the last is the most used in the automotive field [3]), with different nominal voltages and characteristics. The performance of automotive electronic power converters connected to traction batteries as power source or load depend on the battery characteristic and state. Since the battery behavior is strongly affected by numerous factors, State of Charge (SOC), State of Depletion (SOD), temperature, humidity, age, etc..., performing tests in different conditions becomes strategic for the development and verification of power electronic components. However, the battery procurement and the pre-conditioning procedure are highly costing and time-consuming. Moreover, in this way the measurement are not fully repeatable since the battery changes its status in every test cycle. To overcome this issues a Battery Emulator (BE) system can be employed. The BE is a programmable power electronic system capable to provide a voltage/current profile to a load or to a source, behaving as a real battery. To this aim, it must be capable of source and sink DC supply behavior (bidirectional current flow). The emulation capabilities are strictly dependent on the BE electrical performance in terms of power rating, accuracy and dynamic behavior and on the battery model used by the control as a reference. Several modeling methods have been reported in literature, as the Thevenin-based approach in combination with Shepard equation [4], [5], [6], however this is beyond the scope of the chapter that focuses on the BE hardware design and control fulfillment. Desirable characteristics of the battery emulator are the capability of large voltage/current swings, high accuracy and fast dynamic response: maximizing all these requirements in a compact, easily deployable solution is an important goal for the implementation of a highly flexible instrument that can be exploited in a large set of applications. In particular, the aim of the BE prototype here described is to provide a testing system employable in the development and test of automotive power converters and batteries with state of the art performance, when compared to existing commercial products [7], [8], [9]. For this reason, in this design non-conventional solutions are exploited in terms of circuit topology, power electronic devices and magnetic components. Simulations of the power converters are carried out in PSIM environment [10], whereas the control strategy is implemented in Simulink. For dynamic assessment, co-simulations between Simulink and PSIM are performed.
The chapter is organized as follows. In Section 3.2, the technological choices and the design and simulations of the power system are described; in the Section 3.3 the control strategy and its implementation are detailed along with some additional simulations on dynamic performance of the converter; finally, in Section 3.4 the system implementation is shown in combination with a preliminary functional test at de-rated power regimens.

3.2 Power System

The battery-emulator (BE) system envisages the design of a bidirectional (2-quadrant) and isolated DC/DC power converter, comprehensive of digital control board and a sensor network , according to the electrical specifications in Table 3.1.

The converter architecture, topology and technologies were selected to meet

Table 3.1: BE specifications.

Vin	**Vout**	**Iout**	**Pmax**
$750V$	$48 - 1000V$	$\pm 800A$	$350kW$
Current, Voltage ramp-up time	**Current, Voltage reproducibility**	**Current, Voltage ripple**	
$< 1ms, < 10ms$	$< 0.1\%I_{out}$, $< 0.1\%V_{out}$	$< 0.5\%I_{out}$, $< 0.5\%V_{out}$	

these demanding requirements, while minimizing complexity. The solution of a single stage DC/DC converter was discarded due to the wide output voltage range and the necessity for a high equivalent switching frequency to fulfill demanding dynamic specifications. Thus, the selected converter architecture is based on a two-stage approach, as summarized in Figure 3.1. In the operative installation of the converter, the Vin = $750V$ input voltage is provided by the commercial $500kW$ AFE200-72000 Active Front End (AFE) by Gefrem [11]. As will be described in the following, the two-stage approach enables the possibility to operate the two cascaded converters in their optimal operating conditions, while delivering high frequency galvanic isolation and precise current/voltage output values required by the application.

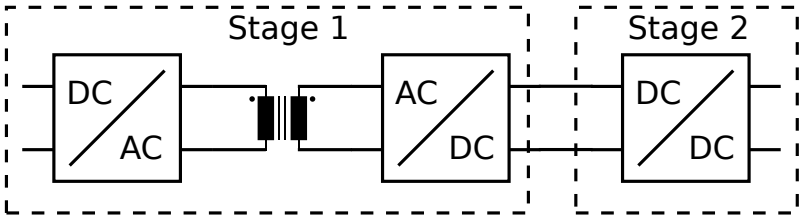


Figure 3.1: Two-stage topology

For the first stage, a Dual Active Bridge (DAB) isolated converter is chosen: this topology, as described in Section 2.2, assures bidirectionality, fairly wide output voltages range and ZVS region, along with simplicity in the control [12], [13]. The second stage is realized by means of a multi-way synchronous Buck converter with interleaved control, that allows improved control bandwidth and a fine regulation of the output characteristics, due to higher equivalent switching frequency of the interleaved regime. Beside boosting the control bandwidth, the interleaved-induced equivalent-frequency step-up enables magnetic and capacitors form-factors reduction in the filter, without increasing semiconductor switching losses, thus permitting higher volumetric power density of the system. Multiple double-stage topologies are possible: the final selection depends on several considerations involving various aspects as transistor maximum blocking voltage (V_{BR}), transformer manufacturing, current management, control strategies and others. One important driving factor for the topology/technology selection in this application is the requirement of a maximum output voltage of $1000V$: that specification has implications in the selection of the technology ($650V$, $900V$, $1200V$, $1700V$ technologies are the possible candidates) and impose to consider topologies characterized by device stacking to sustain the voltage. Moreover, the $800A$ current requirement practically rules out the use of discrete switches and

is a clear indication of the necessity to exploit power modules. In Figure 3.2 four possible solutions that have been considered in the preliminary design phase are depicted.

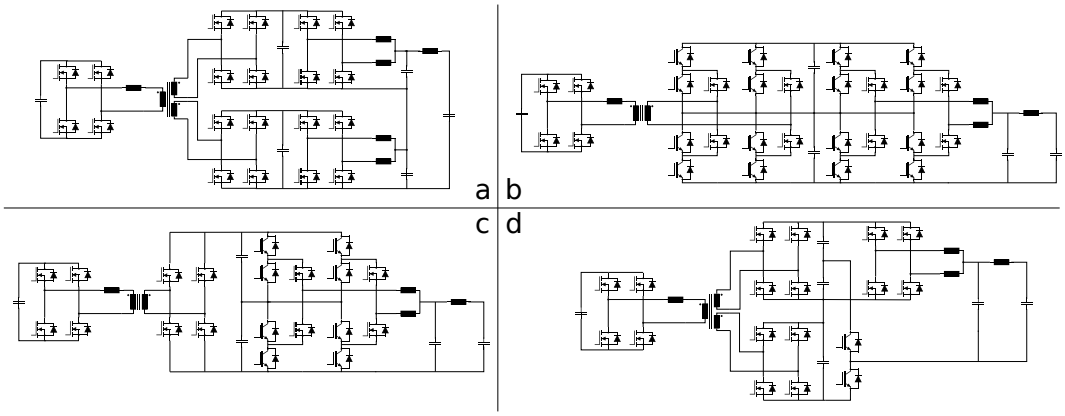


Figure 3.2: Four possible topologies for the implementation of the battery emulator power converter

In sub-figure a) the first stage is implemented by a DAB converter with double secondary, whilst the second stage is made of two synchronous Buck interleaved converters series-connected with an additional output filter. In this way each transistor in the system share the same V_{BR}. In sub-figure b) the DAB secondary is realized through a multilevel approach, which is also exploited in the cascaded Buck converter. In this solution, a double-secondary transformer is avoided. The multilevel structure allows to exploit lower voltage technology in all the secondary side of the converter. In sub-figure c) the DAB secondary is simplified compared to b) thanks to the exploitation of devices capable of withstanding higher V_{BR}, while sub-figure d) the series connection is directly at the end of DAB converter since the Buck converter is a 3-level interleaved single stage. Summarizing, all the illustrated alternatives, except for the first, make use of multilevel solutions, however their additional complexity in terms of controls, the limited availability of suitable multilevel modules and the relatively few advantages assured by them, suggested the use of a simpler two-level approach. Moreover, the need for an high switching frequency to minimized dimensions and optimize the instrument dynamic response, practically ruled out the possibility to select a $1700V$ technology. For this reasons, the topology a) was adopted. With this topology (which is shown with more details in Figure 3.3) the isolation of the two secondaries of the transformer enables the series connection of the secondary-side converters. In this way, the overall $1000V$ maximum output voltage is equally divided between the series connected legs of the secondary-side converters, halving the voltage stress on the power switches and enabling to exploit $1200V$ technologies.

In order to get a cost-effective system with an attractive market value in the automotive testing industry, it is important to take in consideration the overall system efficiency and volume. Typically, the bulkiest components in a power converter are the magnetics and the DC-link capacitors; in addition, large magnetic components typically degrade the power dissipation budget. Increasing the switching frequency, the overall power density of the converter rises up, the dimensions of magnetics and capacitors are reduced and the control algorithm is able to meet higher dynamic requirements. Frequency up-scaling is possible by

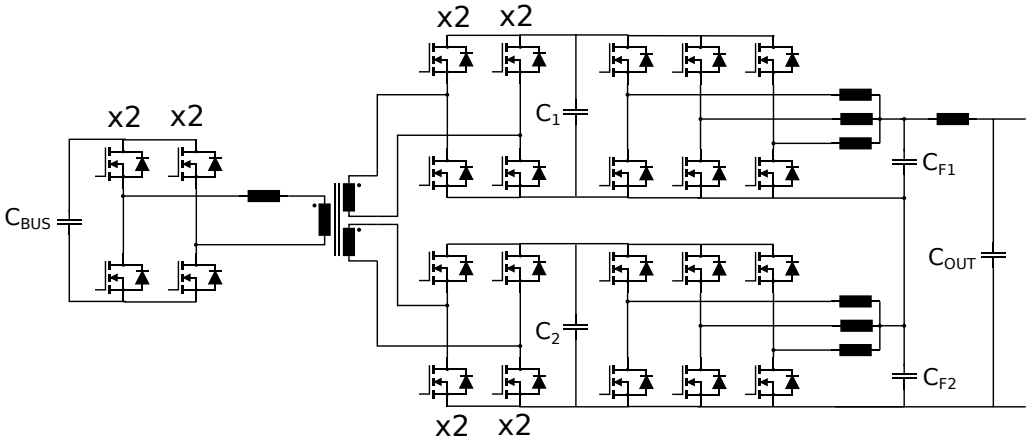


Figure 3.3: Selected topology for the implementation of the BE power converter

replacing traditional IGBT power devices with Wide-Bandgap (WBG) transistors as Silicon Carbide (SiC) or Gallium Nitride (GaN) switches. Their lower gate charge and reduced parasitic capacitances enable faster commutations allowing to switch at tens of kHz instead of few kHz units [14] for the power ratings needed for this application. This is achieved without penalties in terms of conduction losses, since also $R_{DS,ON}/mm$ is lower than for Si devices [14]. Thus, coming back to the selected topology a), considering the very high power rating required, $1200V$ power modules rather than discrete transistor must be addressed. Since there are not commercially available GaN modules at $1200V$, the choice went for $1200V$ SiC modules, which is a product that already gained a good heritage in the market and can assure the required characteristics of availability and reliability needed for the development of a commercial product. The selected power module is Wolfspeed CAB425M12XM3 [15]: it is a $1200V$, $2.6m\Omega$ half-bridge module capable to deliver $450A$ of continuous drain current at $25°C$ backside temperature. Since the module is also rated to operate with more that $400A_{RMS}$ current switching at $50kHz$, due to its very limited E_{ON}/E_{OFF} losses [15], this frequency has been preliminary selected for the design and then confirmed with the simulations computing the associated switches losses, as described in the following. Referring to Figure 3.3 in first stage, the DAB converter ([16], [17], [18]) regulates the power exchange of the system and sets the input voltage of the second-stage synchronous interleaved Buck converter. In the DAB converter topology, the H bridges at the primary and secondary sides of the transformer operates at 50% fixed duty cycle and at the same fixed frequency. The power flow is bidirectional and is controlled with the phase shift between the primary and the secondary square voltage wave-forms. The Single Phase Shift (SPS) control law is used among the possible controlling strategies of the DAB converter [16]. SPS law is described in Equation 2.11 in Section 2.2 where n, V_1, V_2, f_s, L, ϕ are respectively the transformer primary to secondary turn ratio, the input voltage, the DAB output voltage, the switching frequency, the transformer leakage inductance and the phase-shift between gate signals of primary and secondary bridges. More complex controlling strategies for the DAB had been considered and discarded to avoid further complexity in addition to the double-secondary configuration, that already imposes an extra task to the control algorithm to maintain the voltage balancing of the secondaries. Nonetheless, precise control of power regulation is provided by the high resolution control of the phase shift enabled by the micro-controller.

Equation 2.11 is referred to the primary side, therefore V_2 is the sum of the output voltages of the two secondaries. The turn ratio n is selected such as the voltage transfer ratio $d = (n \cdot V_2)/V_1$ is unity with nominal input voltage $V_1 = 750V$ and nominal maximum output voltage $V_2 = 1000V$. This indeed guarantees that, for the proper selection of the leakage inductance, both primary and secondary H bridges experience soft switching (ZVS) commutation for a broad range of output power [17]. Therefore $n = 6/8$ in Equation 2.11, where physically the two secondaries will have half of the secondary turn due to the output series connection. Choosing $\phi = 45°$ for nominal conditions of maximum output power, i.e. $P_{out} = 350kW$, $V_1 = nV_2$, and $f_s = 50kHz$, L is approximately $3uH$, providing a good setup to obtain wide output voltage range as described in Figure 3.4, where Equation 2.11 is graphically analyzed for a series of noticeable operating regimes. The y-axis Figure 3.4 represents the sum of secondary voltages (V_2), while the x-axis is the "equivalent" input mean current at the primary side of the DAB (i.e. output power divided by input voltage, neglecting efficiency). The area limited by the green power-constant curve at $350kW$ and the V_{min}, V_{max} lines represents the V_2 range for which every $P_{out} \leq P_{out,max}$, while the converter operative region extends also below V_{min} accounting for a power derating. V_{min} is selected to limit the device peak and RMS currents for $P_{out} = 350kW$ at a level compatible with the module maximum ratings, whereas V_{max} is selected to be $1150V$ to guarantee a large soft switching region (the higher is V2 the smaller the soft-switching region for fixed power). On the other hand, $V_2 = 1150V = V_{out,max}/0.87$ enables to limit the duty cycle of the buck converter at 87% when delivering $V_{out} = V_{out,max} = 1000V$. Four example points are highlighted (A to D) in Figure 3.4. A to C are $350kW$ full-power operating points with different combinations of voltage and current, whereas at D the DAB converter delivers roughly one half of the full power ($180kW$ at $200V$). Point B represents the maximum stress in terms of RMS currents for the switches and for the DAB transformer. The vertical lines represent different current levels set for for different phase-shift values. The dead-time limit curve represents the minimum phase shift between the bridges below which the dead-time effects, as phase shift drifting and voltage polarity reversal phenomenon, become significant [19], making Equation 2.11 not strictly valid anymore. In this design, the selected dead time is $300ns$, corresponding to a minimum phase shift of 5.4° for the dead-time limit. The $54.3kW$ curve in Figure 3.4 represents the edge between the normal working mode in SPS and the area where the converter characteristics is affected by the dead-time. Finally, the $38.4kW$ constant power curve is covered when at the $48V$ and $800A$ are required at the output of the BE. For the selection of the switches (i.e. power module number) and the design of the transformer and magnetics it is necessary to determine the maximum peaks of the currents their RMS values. It is well known that in the DAB converter the RMS and peak current stress of the devices are quite high and are affected by the choice of the leakage inductance in series with the transformer. With SPS, the current flowing at the primary through the leakage inductance has a trapezoidal shape where the corner values at the end

of phase-shift time and at half of the period can be calculated as follow [20]:

$$i_L(\pi) = \frac{V_1\pi + nV_2(2\phi - \pi)}{4\pi f_s L} \tag{3.1}$$

$$i_L(\phi) = \frac{nV_2\pi + V_1(2\phi - \pi)}{4\pi f_s L}, \tag{3.2}$$

where the difference with Equations 2.8, 2.8 lies just in the accounting of the turn ratio coefficient n. Specifically, when the DAB converter works in Buck-mode ($V_1 > nV_2$), Equation 3.1 represents the current peak, while in Boost-mode ($V_1 < nV_2$) Equation 3.2 becomes the new current peak. Considering the case B of Figure 3.4, the primary current peak value calculated is $861A$. In addition, the signs of Equation 3.1 and Equation 3.2 are useful to evaluate the soft-switching region as declare in Section2.2.2 and in [18]. This indicates that the converter tends to exit the soft switching region as the phase shift decreases, then for lower output power. From Equations 3.1 and 3.2 it is possible to plot the soft switching region of the actual converter in Figure 3.5. The ZVS region is limited by the two boundaries curves: the input bridge operates in ZVS for all the points below the "input bridge boundary curve" (blue curve), whereas the output bridges operate in ZVS for all the point above the "output bridge boundary curve" (red curve). Thus, the shaded region in the plot represents working conditions where both input and output bridges operate in ZVS. It is important to notice that the nominal condition $V_{in} = nV_{out}$ is entirely included (except for a negligible section under $P_{out} = 500W$ due to the C_{oss} contribution), indicating that not only the converter operates in ZVS at full power, but also that a control strategy that aims at forcing this nominal voltage ratio is capable to extend the ZVS region down to very low output power levels. Since the input H bridge boundary is directly linked to boost-mode operations and the PS value of the intersection with $P_{out} = 350kW$ line is lower than the value needed for maximum power at $V_2 = 1150V$, also the point C of Figure 3.4is in ZVS region.

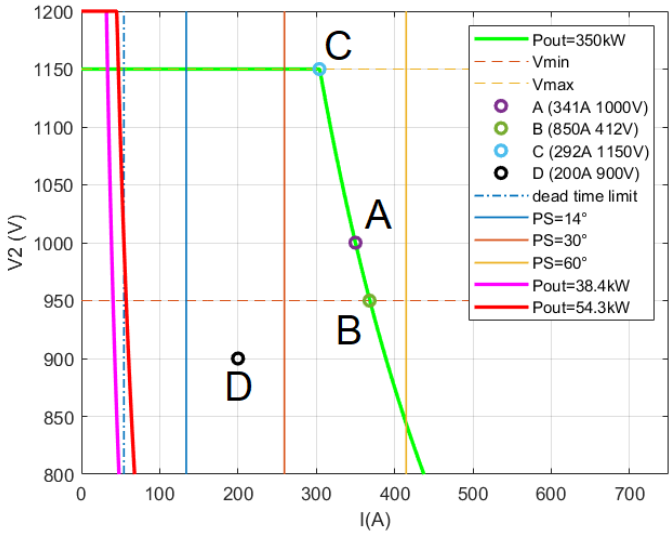


Figure 3.4: DAB relevant operating points

The maximum RMS current values have been preliminary evaluated by means of simulations of the converter working in the critical point B of Figure 3.4. For

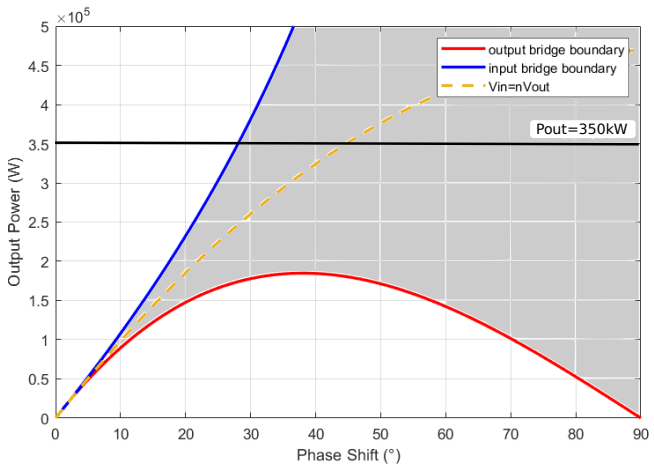


Figure 3.5: DAB ZVS region

this preliminary simulations that had the goal to identify the target current ratings, almost ideal device models where adopted in PSIM simulation environment [10]. More detailed simulation for an accurate assessment of the converter performance are describe in the following. The simulated primary current are shown in Figure 3.6 along with the primary and secondary voltages. The peak value of the current is in accordance with Equation 3.1, whereas the RMS value is $I_{prim,RMS} = 625A_{RMS}$.

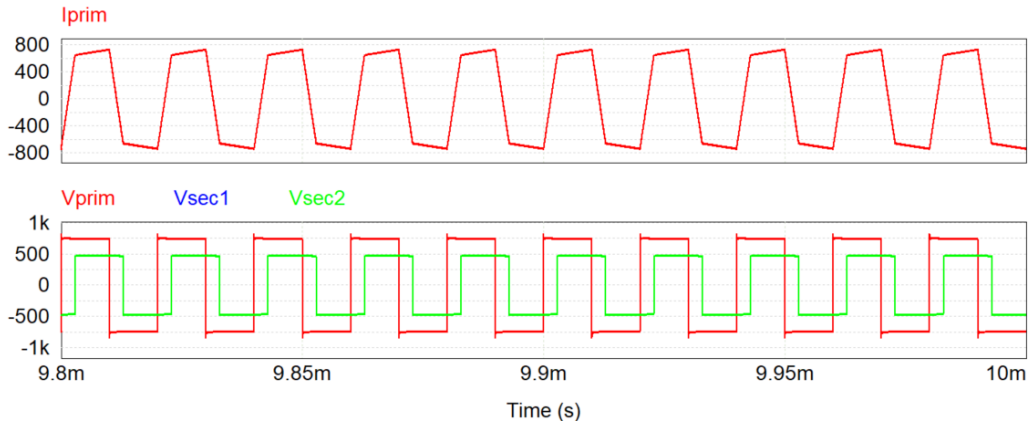


Figure 3.6: Primary current and primary and secondaries' voltages for working point B

Since at $25°C$ backside temperature the maximum rating of pulsed current of the CAB425M12XM3 module is $900A$ and the maximum RMS current abut $450A_{RMS}$, each leg of every H bridge of the DAB converter is made of two power modules in parallel connection, allowing also the a good margin in terms of reliability and safety margin for uneven current distribution between parallel modules. The modules are mounted on cold plates that are designed to maintain the module base at $25°C$. Due to the transformer turn ratio n=6:8 (6:4:4), the current at the secondary side is 3/4 of the primary current, thus the described sizing of two modules in parallel is even more conservative for the secondary-side H bridges.

For the Buck section, considering a maximum output current of $800A$, the mean current flowing into each leg is $267A$ (neglecting the ripple) thanks to the three interleaved phases. Since the maximum DC drain current of CAB425M12XM3 is

$450A$ (at $T_C = 25°C$), a single module for each leg of the Buck converter is adequate with good margin (also considering a typical $10 - 15\%$ additional current ripple), since the module backside is effectively cooled at $25°C$ by cold-plates, as in the case of the modules in the DAB converter. It is also fair to notice, that during very fast load transient (i.e. from $0W$ to $350kW$ in $1ms$) the dynamic current requirement for the Buck converter to obtain a fast change in the output voltage can be much higher. With the designed set-up, the Buck converter allows to deliver $2400A$ of output current for $1ms$, due to the the $900A$ maximum pulsed current rating of each module combined with the transient thermal impedance characteristic of the module. The switching frequency of the Buck interleaved is set to $60kHz$ in order to avoid synchronous switching sequence with the DAB converter, and consequent additional noise in sensing circuitry. Due to the 3-phase interleaved operation, the equivalent output switching frequency is $180kHz$, that enables large controlling bandwidth and eases the output filtering. This is possible also in terms of switching losses, since the maximum RMS current levels managed by the modules of the Buck converter are lower with respect to the ones in the DAB. For the accurate assessment of component selection, thermal management and of the converter performance, a detailed simulation setup was implemented in PSIM. The high operating frequency and the large values of currents and voltages and their derivatives di/dt and dv/dt require a detailed modeling of each component for an accurate simulation of the converter. The SiC modules are modeled exploiting PSIM Thermal Module [10] modeling tool.
As discussed before, the operating point B of Figure 3.4 was tested, since it is the worst case scenario (maximum input current, maximum output power). The sum of the secondary voltages of the DAB is $850V$, while V_{out} and I_{out} at the BE output are $500V$ and $700A$. The simulation results are presented in Table 3.2.

Table 3.2: System assessed in working point B using thermal modules of CAB425M12XM3 in PSIM.

I_{RMS} *prim*	I_{peak} *prim*	T_j *prim*	T_j *sec*	P_{diss} *prim*	P_{diss} *sec*
$624A_{RMS}$	$710A$	$121°C$	$99°C$	$3.91kW$	$3.01kW$
I_{RMS} *sec*	I_{peak} *sec*	P_{diss} *buck*	T_j *buck*	**efficiency**[1]	
$470A_{RMS}$	$574A$	$1.45kW$	$88°C$	96.5%	

[1] Magnetics and capacitor losses not considered

I_{RMS} *prim*, I_{peak} *prim*, T_j *prim*, P_{diss} *prim*, P_{diss} *sec* are respectively the *RMS* and peak values of current at the transformer primary, the junction temperature of the devices in the primary full-bridge and the total power dissipation (conduction and switching) of the primary and one secondary H-bridge, while P_{diss} *buck*, T_j *buck* and efficiency are the dissipated power of the Buck interleaved, the junction temperature of a single device in the Buck and the total system efficiency. The values of the RMS and peak current at the primary and secondary are in accordance with the initial predictions and confirm the correct sizing of the H bridges. They are also used as specification for the transformer. The junction temperature of the switches in the worst case condition is largely within the $175°C$ limit. The relative high switching frequency (i.e. high for this voltage/current levels) enabled by the SiC technology, allows for the design of a compact planar transformer. The

transformer was designed under the specification provided in Table 3.3 . Moreover the transformer is designed to sustain RMS currents as high as 1300 Arms for 1 ms to allow fast dynamic control of sudden changes in the load. Planar transformers [21] provide very good thermal characteristics and high power density thanks to their lower profile and more extended flat surface of the core than conventional wire-wounded ones. This allows a better thermal management and assembly. In addition, the process of PCB winding realization can be easily automated obtaining strong repeatability, accuracy and characterization of parasitics. Also in terms of efficiency, the planar configuration is attractive for the simpleness of interleaving the PCB windings to reduce eddy currents and proximity effect. Due to the very large power rating, the transformer was realized by $2x175kW$ transformers with connected primaries. The predicted efficiency at full power (i.e. $350kW$) is about 99.5%. The $1.5kW$ of dissipated power is managed by a cold plate at 25°C coolant temperature. The transformer is very compact ($373x375x75mm$) and weights $35kg$. The measured leakage inductance at primary side is $0.8uH$, hence an additional external power inductor was designed to obtained the target $3uH$ series inductance for the proper operation of the DAB converter. The power inductor has an inductance of $2.2uH$, dimension of $105x146x198mm$ and weights $12kg$. The estimated losses of $240W$ can be practically neglected in nominal full power conditions. Litz wire windings and ferrite core were used for the high operation frequency. To obtain a stable inductance value for a wide range of current values, the implemented air-gap extends the saturation current to $1600A$, assuring a stable inductance in a wide range of current values. In Figure 3.7 the picture of the transformer and of the series inductor are shown.

Table 3.3: Planar transformer specifications

Pout	**Freq**	**Magn. Ind.**	**Turn ratio**	**In/Out current (RMS)**	**In/Out voltage**	**dimensions**
$2x175kW$	$50kHz$	$410uH$	$6:4:4$	$630-560A$	$800V-200/1400V$	373x375x75mm

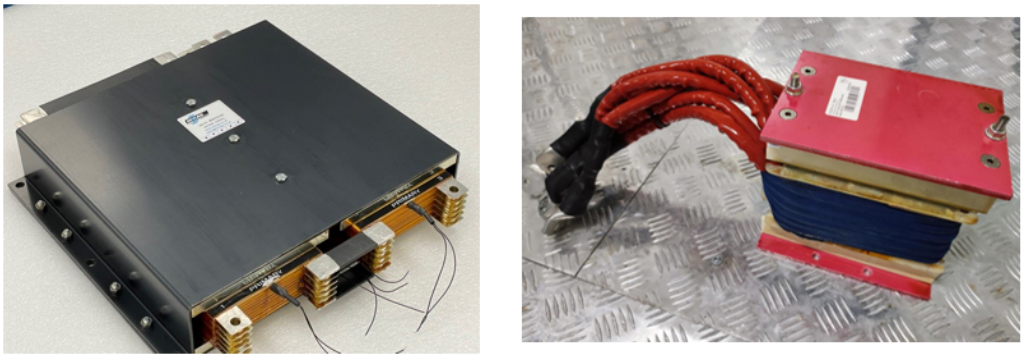


Figure 3.7: Picture of the planar transformer (left) and of the ferrite series inductor (right)

As described in Figure 3.3, additional inductors are used in the two-stage low pass filter at the converter output. The inductors are designed (along with capacitors) for the output current ripple and dynamic control requirements of Table 3.1. Requirements for L_1 and L_2 are summed up in Table 3.4, with particular

attention to the inductance in overload conditions during fast steps of the load. L_1 is implemented with a nanocrystralline core for lower power dissipation, while L_2 has a grain-oriented core due to the low AC residual ripple (second stage of the LC filter) of the current.

Table 3.4: L_1 and L_2 specifications

Inductor	**Nom. inductance**	**Nom. curr.**	**ripple p-p**	f_{sw}	**Overload curr.**	**residual ind.**
L_1	$50uH$	$267A$	$50A$	$60kHz$	$800A$	$25uH$
L_2	$15uH$	$800A$	*negligible*	$180kHz$	$2400A$	$7.5uH$

A picture of these inductors is provided in Figure 3.8

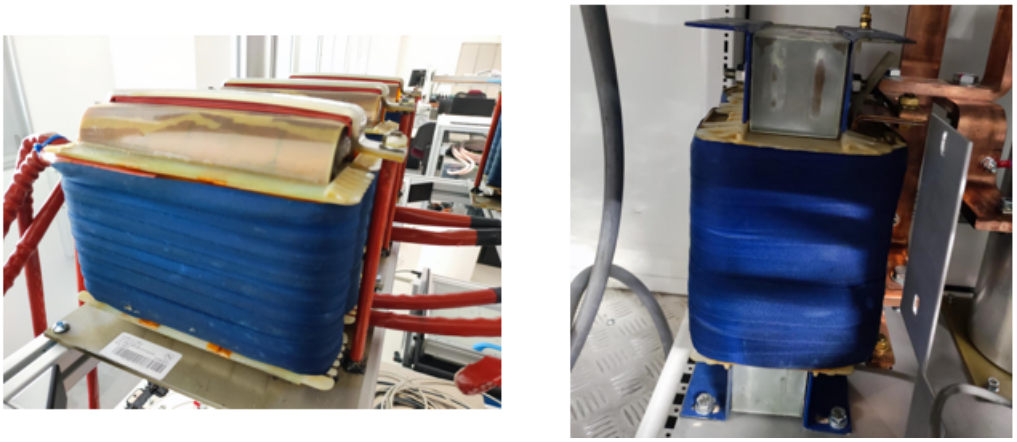


Figure 3.8: Buck filter inductor (left) and output filter inductor (right)

The selection and sizing of the capacitors depend on their function in the converter. Referring to Figure 3.3, C_{BUS} and $C_{1,2}$ are DC-link capacitors, whereas $C_{F1,F2}$ and C_{OUT} are LC-filter capacitors. DC-link capacitors need to meet simultaneously several requirements: transient energy-related, PWM-ripple-related and di/dt-related requirements. As far as regarding energy-related requirements, C_{BUS} must maintain a DC voltage close to $750V$ in case of overload, while delivering the high required RMS currents without overheating. The PWM ripple generated by the DAB converter is at $100kHz$ (2xf_s), whereas the low-frequency ripple from the AFE is at $300Hz$. Transient simulations performed with Simulink with a control bandwidth of $30kHz$ (see next section on the control) where used to identify $C_{BUS} = 15mF$ as the minimum value necessary to maintain a DC link voltage over $680V$ during the maximum power step of $1ms$. In this condition the RMS current to be delivered by C_{BUS} is about $520A_{RMS}$ with a peak value of $1330A$. With this value of capacitance the ripple requirements are automatically satisfied provided that low ESR/ESL capacitors are used. Considering the capacitor ESL, the most stringent requirements come from the very high di/dt required from the DC-link capacitors during SiC modules commutation. Since the estimated di/dt is $di/dt = 9A/ns$, the maximum allowed parasitic inductance should be $L_{TOT} = 11nH$ to limit the maximum overshoot to $100V$. The contributions to L_{TOT} are the power module inductance ($3.5nH$ for two modules in parallel), the ESL of the capacitors and the parasitic inductance of the bus bars connecting

the SiC modules to the capacitors. Custom laminated DC bus-bars that allow magnetic field cancellation for inductance minimization have been adopted for the connection of the SiC modules to the DC-link capacitors: with this solution the parasitic inductance of this connection is less than $2nH$. This leaves about $5.5nH$ for the maximum value for the equivalent ESL of the C_{BUS}. Considering all these constrains (along with the space requirement constrain), the adopted solution was to implement the $15mF$ C_{BUS} with a combination of electrolytic and polypropylene film technologies: $12.6mF$ of $550V$ electrolytic capacitors (series connection) are used as the main energy bulk, whereas $2.4mF$ of $1100V$ film capacitors provide the required very low ESL and very high peak current[22]. For the identification of $C_{1,2}$, the considerations are similar, but in this case the requirement in terms of energy bulk for dynamic response is more relaxed due to the fast response of the DAB converter that feeds this DC link. Thus the identified value for this component is $C_{1,2} = 1.2mF$ and it is entirely implemented in polypropylene film technology. For the capacitors $C_{F1,F2}$ and C_{OUT} in the two-stages output filter, there is not di/dt stress due to the presence of the inductors. Moreover, in steady-state the RMS currents through the capacitors are quite small. However, in dynamic conditions large variations of output power and voltage levels produce high dynamic currents, so ESR must be very small, high peak current capability is required and capacitance value is selected to maintain a stable voltage during transient (PWM ripple requirement are less stringent). Therefore, polypropylene film capacitors are chosen also in this section. The selected value are: $C_{F1,F2} = 1.2mF$ ($900V$ film capacitors providing $450A$ peak); $C_{OUT} = 2.4mF$ ($1400V$ film capacitors providing $2000A$ peak).

3.3 Control System

In this section the overall control system is described along with some details on the PCB boards developed to its implementation. The sensing and command set-up that interfaces the power and control systems is shown in Figure 3.9. As described in the figure, the system counts 15 analog sensors (current and voltage sensors), 18 CAB425M12XM3 modules with relative CGD12HBXMP driver boards by Wolfspeed and 24 PWM signals to control the power flow.

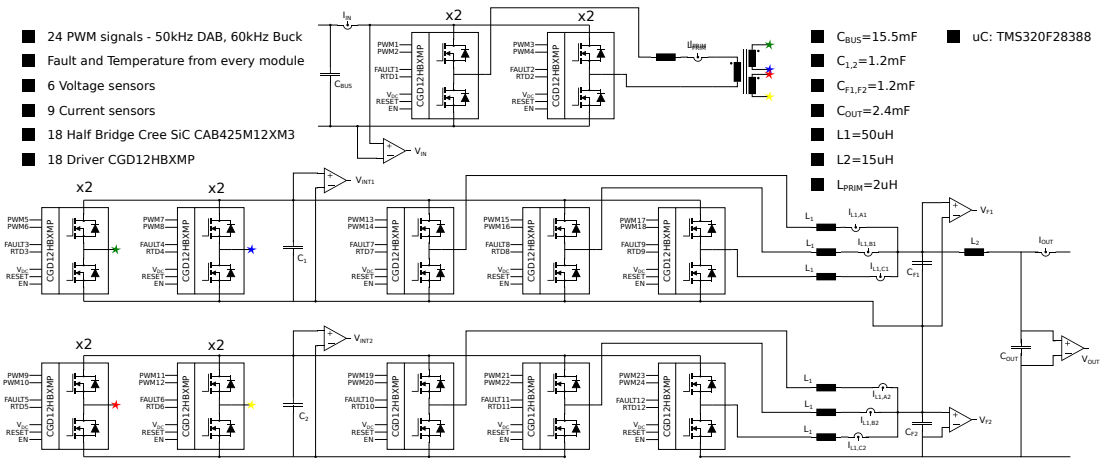


Figure 3.9: Sensing and commands structure

In the implementation of the system prototype, several sensing points are used, some of them can be avoided in the final set-up. In addition to the BE output current and voltage I_{out} and V_{out}, voltages at output ports of AFE, DAB and Buck ($V_{in,DC}$, $V_{int1,DC}$, $V_{int2,DC}$, $V_{out1,DC}$, $V_{out2,DC}$) and currents at input port, transformer primary winding and each Buck interleaved phase ($I_{in,DC}$, I_{prim}, $I_{L1,a1}$, $I_{L1,b1}$, $I_{L1,c1}$, $I_{L1,a2}$, $I_{L1,b2}$, $I_{L1,c2}$) are sampled. At the output stage, the demanding specifications in terms of dynamic and accuracy require the adoption of the top-of-the-line sensors. For the current, the ITN 900-S ULTRASTAB by LEM provides capability to sense $\pm 900A$ with a $300kHz$ bandwidth and 0.0011% accuracy, whereas the CV-3 2000 voltage sensor by LEM senses the output voltage up to $1400V$ with a $300kHz$ bandwidth and 0.2% accuracy. I_{prim} and $I_{in,DC}$ are used for protection purposes, so the LF 1005-S by LEM ($\pm 1500A$, $1000A_{RMS}$, $150kHz$ bandwidth, 0.4% accuracy) is chosen, while for the current balancing among Buck interleaved phases the LF 510-S by LEM ($\pm 800A$, $\pm 500A_{RMS}$, $200kHz$ bandwidth, 0.5% accuracy) has been selected. All the previous transducers have closed loop compensation for performance enhancement. The remaining voltage measurements are carried out by inexpensive resistive dividers.
A dedicated CGD12HBXMP driver board has been chosen to drive each power module since it provides full compatibility to XM3 Wolfspeed Half Bridge Power Modules in terms of optimal assembly, high-frequency operations and fault protection. High-side and low-side gate signals are supplied to the board in differential mode for noise immunity and are transformed into single-ended signals before reaching the two single-channel ADuM4135 (Analog Devices) isolated gate driver used inside the driver board. The ADuM4135 is able to furnish $\pm 10A$ peak gate current for fast commutations and embeds de-saturation circuitry which, in combination with external over-voltage and shoot-though prevention circuits, generates the main output fault signal of the driver board. Moreover, the driver board acquires the temperature of the power module from die-level NTC sensor and outputs it applying a frequency modulation.

3.3.1 Control Strategy

The control strategy aims to regulate the DAB and the Buck interleaved converters shown in Figure 3.4 with a single voltage closed loop and a double voltage-current closed loop respectively.

3.3.1.1 Buck Control

Two feedback loops are implemented for the Buck control: the external and slower one regulates the output voltage, while the internal and faster one the current of each interleaved phase, providing also current balancing.
The inputs of voltage regulator are V_{out} (potential of C_{out}), the voltage set-point V^*_{out}, the output current I_{out} requested from the load for the feed-forward contribution and the output voltages V_{F1}, V_{F2} of the two Buck interleaved for balancing purposes. The output of the controller is the reference I^*_1 for the internal loop that represents the current sum of each interleaved phase contribution. For clarity sake, the control loop is schematized in Figure 3.10 where the main characteristics are reported (for the complete acquired characteristics refer to Figure 3.9).

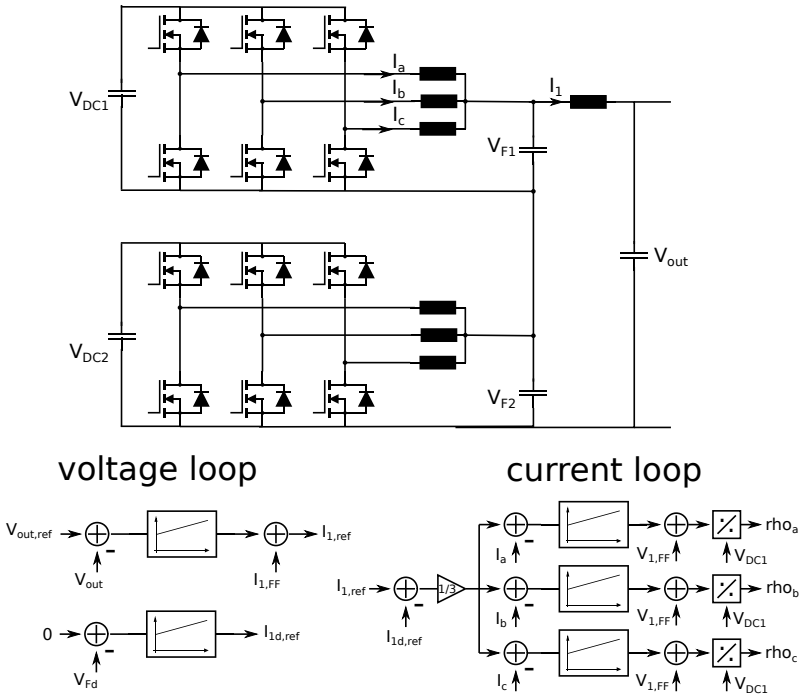


Figure 3.10: Control diagram of the output section. Only the current loop for the upper Buck interleaved converter is shown.

The plant consists basically in the cascade of the Buck filter and the output LC-filter ($C_{F1,2}$, L_1 and C_{out}, L_2 respectively) resulting in a system described by the following state equations:

$$\begin{aligned} C_{out}\frac{dv_{out}}{dt} &= i_2 - i_{out} - \frac{v_{out}}{R_{dout}} \\ L_2\frac{di_2}{dt} &= (v_{F1} + v_{F2}) - v_{out} - R_{L2}i_2 \\ C_{F1}\frac{v_{F1}}{dt} &= i_{1up} - i_2 - \frac{v_{F1}}{R_{df1}} \\ C_{F2}\frac{v_{F2}}{dt} &= i_{1dw} - i_2 - \frac{v_{F2}}{R_{df2}} \end{aligned} \tag{3.3}$$

where i_2 is the current in L_2, R_{dout} is the external discharge resistance in parallel to C_{out}, R_{L2} is the ESR of L_2, i_{1up} and i_{1dw} are the current sum of the two Buck interleaved, R_{df1} and R_{df2} are discharge resistances of C_{F1}, C_{F2}. Considering

$$C_{F1} = C_{F2}; \quad v_{Fs} = v_{F1} + v_{F2}; \quad v_{Fd} = v_{F1} - v_{F2} \quad i_1 = \frac{i_{1up} + i_{1dw}}{2}$$

the following equations can be obtained

$$\begin{aligned} C_{out}\frac{dv_{out}}{dt} &= i_2 - i_{out} - \frac{v_{out}}{R_{dout}} \\ L_2\frac{di_2}{dt} &= v_{Fs} - v_{out} - R_{L2}i_2 \\ \frac{C_{F1}}{2}\frac{v_{F1}}{dt} &= i_{11} - i_2 - \frac{v_{F1}}{2R_{df1}} \\ C_{F1}\frac{v_{Fd}}{dt} &= i_{1d} - i_2 - \frac{v_{Fd}}{R_{df2}} \end{aligned} \tag{3.4}$$

From the first three equations of Equation 3.4 the transfer function (t.f.) $G_{v1} = \frac{i_{out}}{v_{out}}$ and $G_{v2} = \frac{i_1}{v_{out}}$ are computed and shown in Figure 3.11, where G_{v2} is the one used for the control. The control bandwidth must be above $1krad/s$ to have a time constant less than $1ms$ and distant from the resonance peak at $19krad/s$ ($3kHz$). Anyway, the feed-forward terms and additional resistive losses help against the resonant peak. The feed-forward term i_{1ff} can be calculated as

$$\begin{aligned} i_{2ff} &= i_{out} + \frac{v_{out}}{R_{dout}} + C_{out}\frac{dv^*_{out}}{dt} \\ v_{Fsff} &= v^*_{out} + L_2\frac{di_{2ff}}{dt} + R_{L2}i_{2ff} \\ i_{1ff} &= i_{2ff} + \frac{C_{F1}}{2}\frac{v_{Fsff}}{dt} + \frac{v_{fs}}{2R_{df1}} \approx i_{out} + (C_{out} + \frac{C_{F1}}{2})\frac{v^*_{out}}{dt}. \end{aligned} \tag{3.5}$$

Hence the current reference i^*_1 for the current loop can be computed

$$i^*_1 = i_{1ff} + PI(v^*_{out} - v_{out}) \tag{3.6}$$

where the Proportional-Integral (PI) regulator bandwidth is sufficiently slow to exclude the resonant peak.
Considering the last equation of Equation 3.4, the current balancing among the two Buck interleaved is implemented by

$$i^*_{1d} = PI(0 - v_{Fd}) \tag{3.7}$$

and using it for the reference values of current loop

$$\begin{aligned} i^*_{1up} &= i^*_1 + \frac{i^*_{1d}}{2} \\ i^*_{1dw} &= i^*_1 - \frac{i^*_{1d}}{2} \end{aligned} \tag{3.8}$$

For the current internal loop only the upper Buck interleaved is treated since it is identical to the other. The plant is described as follows:

$$\begin{aligned} L1\frac{di_{1up,a}}{dt} &= v_{up,a} - v_{F1} - R_{L1}i_{up,a} \\ L1\frac{di_{1up,b}}{dt} &= v_{up,b} - v_{F1} - R_{L1}i_{up,b} \\ L1\frac{di_{1up,c}}{dt} &= v_{up,c} - v_{F1} - R_{L1}i_{up,c} \end{aligned} \tag{3.9}$$

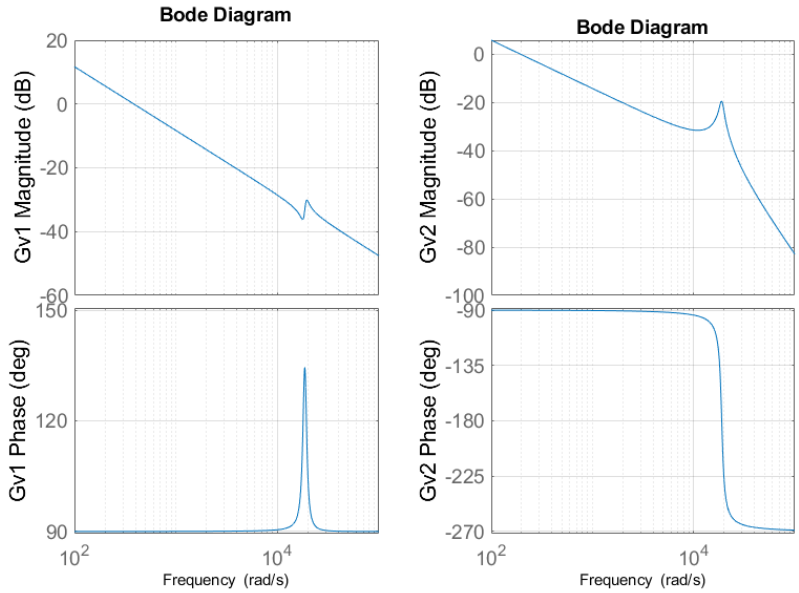


Figure 3.11: Bode plots of G_{v1} (left) and G_{v2} (right)

where the a, b, c letters indicate the three interleaved phases. Each phase current is sensed and employed for the error calculation in combination with $i^*_{1up}/3$ set-point and provided to a PI regulator to obtain the voltage reference for duty calculation. Also in this case a feed-forward term is used

$$v_{up,a,b,c} = v_{up1ff,a,b,c} + PI\left(\frac{i^*_{1up}}{3} - i_{1up,a,b,c}\right) \quad v_{up1ff,a,b,c} = v_{F1} + L_1\frac{di^*_{1up}}{dt} \tag{3.10}$$

The bandwidth of the PI current regulator is set to be ten times the one of the PI voltage regulator to be able to have noise rejection with a PWM frequency of $60kHz$ and a control frequency of $30kHz$. Nevertheless, it is important to have synchronous current sampling with PWM signal to regulate the mean value of the phase current and acquire at the middle of ON time for low switching noise. Once $v_{up,a,b,c}$ are calculated, the modulation indices are retrieved

$$\rho_{a,b,c} = V_{DC1}/v_{up,a,b,c}$$

3.3.1.2 DAB control

The role of the DAB converter is to maintain a stable voltage at the input of the Buck converter providing also a fast dynamic variation of power transfer according to the load requests. For this purpose the V_{C1} and V_{C2} voltages of the C_1, C_2 capacitor between the DAB and the Buck converter are sensed and the correspondent phase-shift to be applied to the gate signals is obtained. Since the power transfer is determined by the voltage across the series inductor at the transformer input (i.e. leakage inductance + additional series inductance), it is important that the square voltages of the two transformer secondaries must be as equal as possible in terms of amplitude and delay. Therefore two separate phase-shift terms ϕ_{up} and ϕ_{dw} are used. In Figure 3.12 the control diagram is depicted along with the scheme indicating where V_{C1} and V_{C2} are located.

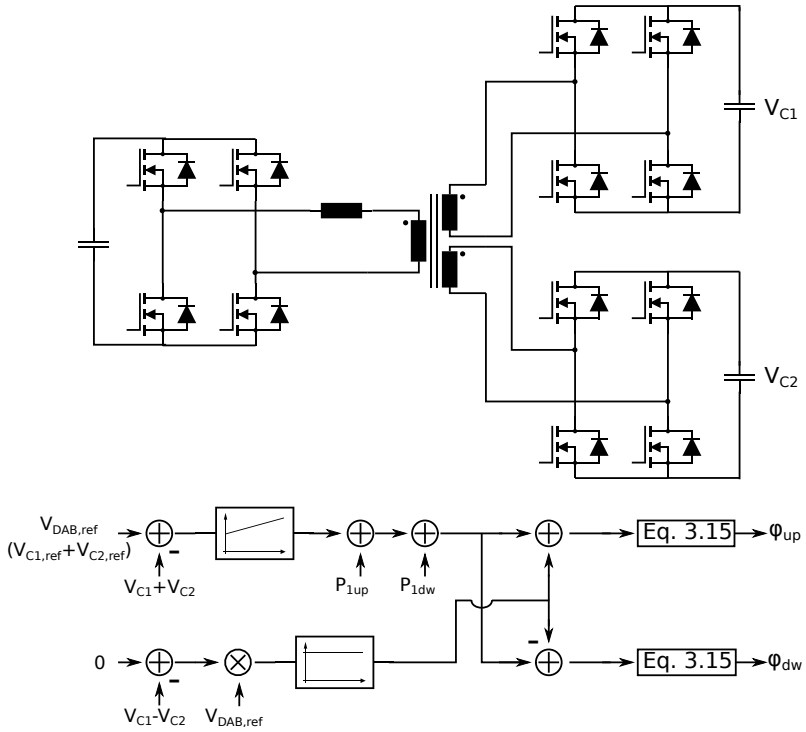


Figure 3.12: Control diagram of the DAB converter

Considering the V_{C1}^* and V_{C2}^* reference nominal values for v_{C1} and v_{C2}, we can write:

$$\begin{aligned} C_1 \frac{dv_{C1}}{dt} &\approx \frac{p_{outDAB,up} - p_{1up}}{V_{C1}^*} - \frac{v_{C1}}{R_{dC1}} \\ C_2 \frac{dv_{C2}}{dt} &\approx \frac{p_{outDAB,dw} - p_{1dw}}{V_{C2}^*} - \frac{v_{C2}}{R_{dC2}} \end{aligned} \tag{3.11}$$

where p_{1up}, p_{1dw} are the power levels requested by the load from the upper and lower branches, while $R_{dC1,2}$ represent the discharge resistances of C_1 and C_2. Imposing the following constraints:

$$v_{C1} + v_{C2} = v_{outDAB}; \quad v_{C1} - v_{C2} = v_{dDAB}; \quad C_2 = C_1; \quad R_{dC2} = R_{dC1};$$

$V_{C2}^* = V_{C1}^*$; $\quad p_{DAB} = p_{outDAB,up} + p_{outDAB,dw}$; $\quad p_{dDAB} = p_{outDAB,up} - p_{outDAB,dw}$

the following equations can be obtained:

$$C_1 \frac{dv_{outDAB}}{dt} = \frac{p_{DAB} - (p_{1up} + p_{1dw})}{V_{C1}^*} - \frac{v_{outDAB}}{R_{dC1}} \tag{3.12}$$

$$C_1 \frac{dv_{outDAB}}{dt} = \frac{p_{DAB} - (p_{1up} - p_{1dw})}{V_{C1}^*} - \frac{v_{dDAB}}{R_{dC1}} \tag{3.13}$$

From Equation 3.12 the control for the power flow demanded from the DAB converter is computed by a PI regulator on voltage error and feed-forward contributions

$$p_{DAB} = p_{1up} + p_{1dw} + PI(2V_{C1}^* - v_{outDAB}) \tag{3.14}$$

Once the power is computed, the phase-shift is calculated (from Equation 2.11) as

$$\phi = \pm\frac{\pi}{2}\left(1 - \sqrt{1 - \frac{8 f_s L}{V_1 n (v_{C1} + v_{C2})}|p_{DAB}|}\right) \tag{3.15}$$

To keep v_{C1} and v_{C2} balanced it is sufficient a proportional control on the voltage difference

$$\phi_{up} = \phi + k_{vdiff} v_{dDAB} \quad \phi_{dw} = \phi - k_{vdiff} v_{dDAB}$$

In addition, a further control is implemented to avoid transformer saturation according to the technique described in [23].

In the implemented control strategy, the reference voltages V_{C1}^* and V_{C2}^* are kept at nominal values ($\frac{1}{2}\frac{V_1}{n} = 500V$) in order to let the DAB working in the optimal condition (ZVS, low current stress), as long as the output requires less than $1000V$ or the Buck converter reaches the minimum possible duty cycle value ρ_{min}. In the first case, the DAB output voltages are increased to $600V$, while in the second the DAB output is decreases until the BE output set point is reached with the Buck duty cycle at $\rho = \rho_{min}$. Finally a soft start procedure is implemented for converter turn-on: the gate signals of secondary side bridges are kept OFF, while the phase-shift between the two diagonals of the full-bridge at primary side is ramp-up from 0 to π, i.e. the point where the H-bridge diagonals work alternatively. In this way, C_1 and C_2 are slowly charged through the body diodes of the devices of secondary side bridges until the nominal voltage is reached. Once the target voltage is sensed, the control turn ON all the gate signals of DAB and Buck interleaved converters.

3.3.2 Simulations of the Battery Emulator

The described simulation strategy has been implemented in Simulink and the PSIM - Simulink co-simulation feature (i.e. PSIM SimCoupler) was exploited for a detailed simulation of the entire system including the control dynamics. Figure 3.13 shows some details of the PSIM and Simulink schematics.

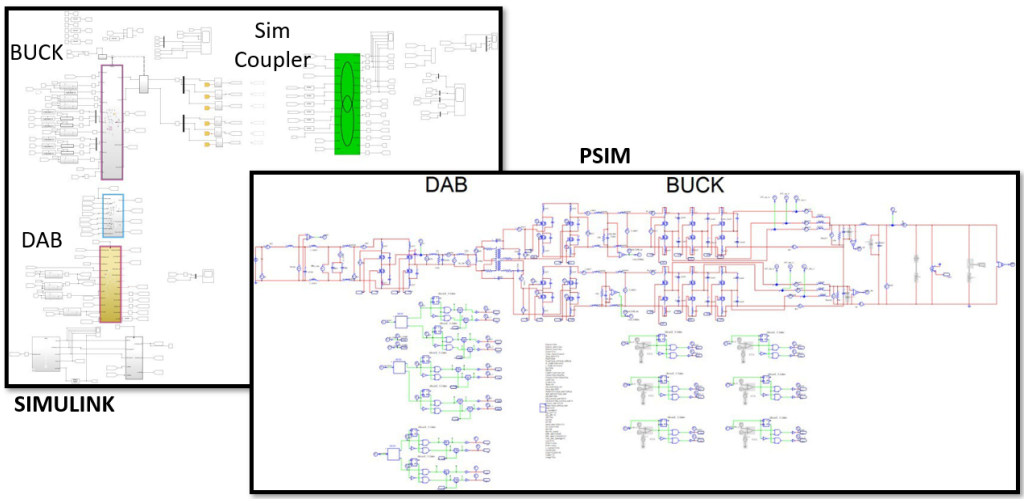


Figure 3.13: PSIM and Simulink schematics for the system co-simulation

The Simulink engine takes as input the sensed characteristics from the PSIM schematic providing back the gate signals accordingly to the described control strategy; the power systems simulation in PSIM is controlled by these signals generated in Simulink. The PSIM simulation takes into account all the main parasitics introduced by passive components, as ESR, ESL, bus-bar stray inductance and conduction/commutation losses of the switches.Thus this simulation set-up is capable of an accurate evaluation of the converter performance, both in terms of steady state regime and transient response to load or command changes.

The results of the simulation of three relevant steady-state working point of the entire battery emulator exploiting the co-simulation feature are shown in Table 3.5. As described in the caption of the table, Case A is a full-power working point at the maximum output current, Case B is a full-power point at the maximum output voltage and Case C is a low-power working point corresponding to the combination of minimum voltage and maximum current.

Table 3.5: System performances in steady-state conditions. Case A: $V_{out} = 437.5V$, $I_{out} = 800A$, $P_{out} = 350kW$. Case B: $V_{out} = 1000V$, $I_{out} = 350A$, $P_{out} = 350kW$. Case C: $V_{out} = 48V$, $I_{out} = 800A$, $P_{out} = 38.4kW$.

Case	I_{RMS} $p.$	I_{peak} $p.$	T_j $p.$	T_j $s.$	T_j $b.$
A	$590A$	$709A$	$122°C$	$99°C$	$83°C$
B	$536A$	$798A$	$81°C$	$110°C$	$104°C$
C	$298A$	$622A$	$85°C$	$33°C$	$70°C$
P_{diss} $p.$	P_{diss} $s.$	P_{diss} $b.$	P_{in}	P_{out}	eff.
$4.28kW$	$2.51kW$	$1.78kW$	$361kW$	$348kW$	96%
$2.39kW$	$2.5kW$	$0.76kW$	$354kW$	$348kW$	98%
$2.47kW$	$0.28kW$	$1.17kW$	$46kW$	$38kW$	83%

The data listed in Table 3.5 are the primary current RMS and peak value, the total power dissipation for the primary full-bridge (P_{diss} $p.$), one secondary full-bridge (P_{diss} $s.$) and a Buck interleaved converter, hottest device junction temperature, the overall input and output power and the efficiency. Simulations highlight a large safety margin for the junction temperatures and elevated efficiency at full power. The efficiency decrement in Case C is due to the low reference voltage adopted for the DAB converter: indeed, to produce $48V$ at the emulator output, the Buck converter input voltage must be low (e.g. $200 - 300V$), since it is not possible to operate it at very low duty cycle because of the required 800 A output current. Consequently, the DAB converter works far from the nominal condition (i.e. $V_{out,DAB} = 240V$) . The consequence is a high peak primary current and higher power dissipation compared to the secondary side. For the evaluation of the dynamic response of the converter, three different cases are described as relevant examples. Figure 3.14 describes the converter response to a $0 - 800A$, $10ms$ load step in the worst case, i.e. when the out voltage is at its minimum $V_{out} = 48V$ and DAB and Buck converters are working far from nominal condition. The response of the system is fast, with a maximum undershoot of V_{out} of $6.5V$ and a almost total recovery of the nominal value after less than $2ms$. In Figure 3.15 the converter response to a load current steps $0 - 800A$ is described in term of output voltage variation from the nominal point $V_{out} = 437.5V$ at no load condition. The

low frequency ripple is due to the null output power condition when $I_{out} = 0A$. It can be appreciated that the maximum variation of the output voltage in about 2%.

Finally, Figure3.16 shows how V_{out} follows the a $1000V - 48V$ reference step within $10ms$ as specified with a null current required by the load.

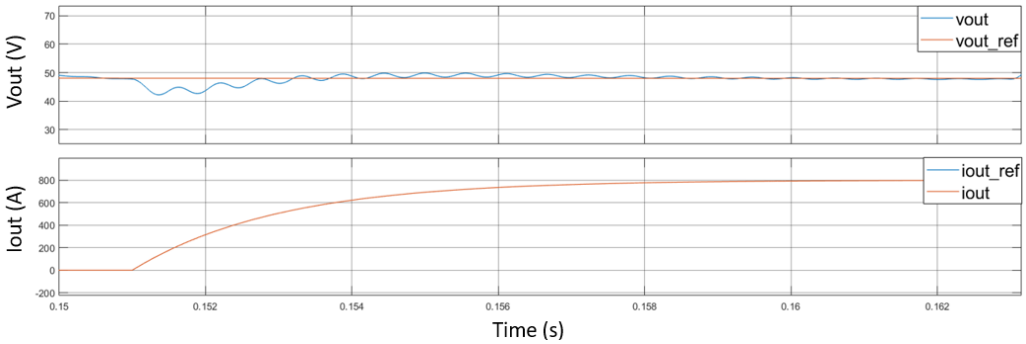


Figure 3.14: System response to a $0 - 800A$ current load request with fixed $V_{out} = 48V$

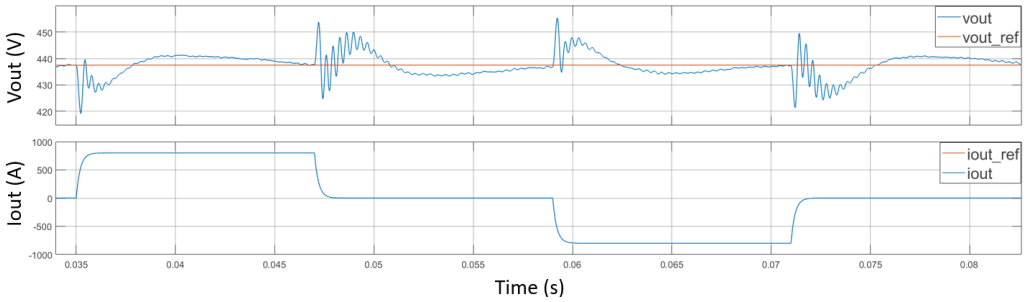


Figure 3.15: System response to a $0 - 800A$ current load request with fixed $V_{out} = 437.5V$

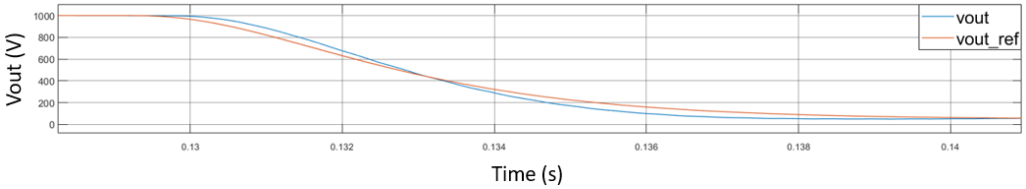


Figure 3.16: System response to a $1000V - 48V$ output voltage step

3.3.3 Hardware for the control system

As described in Figure 3.9, due to the complexity of the converter, the control system must provide 24 high frequency ($50 - 60kHz$) PWM signals, read several sensors and provide many dedicated power supplies to drivers, sensors and signal conditioning chains. The hardware dedicated to control purposes has been split in two separated PCBs, an Auxiliary Supply Board and a Control Board. In this way, the power generation for analog circuits (including sensors) and digital circuits is confined in the Auxiliary Supply Board avoiding additional switching noise into the Control board, where the micro-controller, the communication peripherals and signal conditioning are placed. In addition, the single-board solution would have a very large dimension with less immunity to electromagnetic interference and more complex housing into the rack.

3.3.3.1 Auxiliary Supply Board

From the external AFE, the Supply Board receives an already filtered $230V_{AC}$ mono-phase voltage and a $150W$ $12V$ DC isolated voltage. The latest is used for the supply of CGD12HBXMP drivers and digital circuits ($12V$, $5V$, referred to GND), while the second is used by sensors and analog circuits ($\pm 18VA$, $+5VA$, referred to GNDA, where the suffix A stands for Analog). The scheme is presented in Figure 3.17. The $12V$ is directly passed as output and also used to obtain $5V$ through a $20W$ buck converter realized with the TPS5450DDARG4 Texas Instrument IC considering a $500kHz$ switching frequency and $100mV_{pp}$ output voltage ripple.

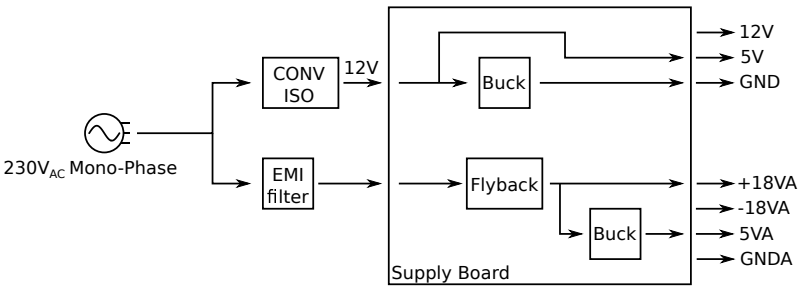


Figure 3.17: Supply Board scheme

Concerning the analog section, the converter is designed considering a maximum power request of $40W$, where large part of it are ascribed to LEM sensors ($36W$). Since the LEM sensors need a stable $\pm 15V$, the Supply Board generates a switching $\pm 18VA$ voltage, which is scaled down by linear converters in the Control Board. The converter topology is a Flyback with bipolar output as shown in Figure 3.18, where at the input, the alternate voltage is rectified by a diode bridge and filtered. The control and the main switch are integrated in the same TOP257YN IC [24] by Power Integration that regulates at $132kHz$ switching frequency an overall $36V$ ($18V + 18V$) output voltage by an opto-isolator. The transformer is a custom design. The converter is designed to provide $80W$ not only for safety margin but also because, in the unlikely event in which each current sensed by LEM has same polarity and is at the maximum peak allowable, the current drawn from the Flyback is concentrated in just one branch of the bipolar output. The last voltage, $5VA$ is generated by the TPS5450DDARG4 integrated buck converter by Texas Instruments, like for the $5V$, starting from the $+18VA$ with a $15W$ maximum output power.

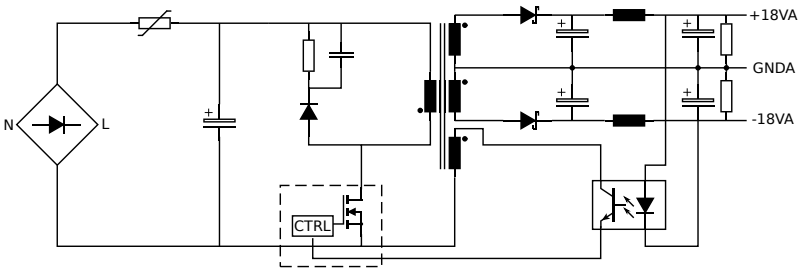


Figure 3.18: Bipolar Flyback scheme

3.3.3.2 Control Board

The Control Board is the hardware platform in which the control algorithm is executed taking advantages of sensors measurements and producing PWM signals, with the features of diagnostic and external communication. Its basic scheme is shown in Figure 3.19.

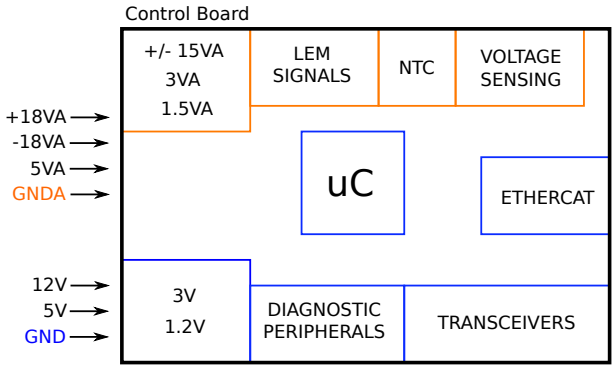


Figure 3.19: Control Board conceptual scheme

The microcontroller adopted is the TMS320F28388D [25] of the C2000 family by Texas Instruments. To the best of our knowledge it was the top-notch real-time microcontroller available on the market for industrial application at the time of design. The elevated number of frequency-independent PWMs (32) and the $200MHz$ system clock perfectly fit the requirements of complex power converter topologies that exploits WBG devices as SiC technology. The dual-core architecture in combination with CLA furnishes the necessary computational resources for executing complex control algorithm fastly, while high resolution sampling is guaranteed by 24 ADC inputs settable in 12-bit or 16-bit mode. Moreover, the TMS320F28388D embeds EtherCAT Slave Controller reducing the bill-of-material of the PCB. Such protocol is used for master communication so that the user can set output conditions and check the system status.The KSZ8081MLXIA is chosen as physical layer transceiver among the options suggested by Beckhoff [26] and set to $100Mbit$ speed. Due to high-speed communication, the RX and TX lines traces are matched in terms of impedance and shielded RJ45 connectors with embedded transformers are used. Other two peripherals, RS485 and CAN, are present into the board for diagnostic purposes during test operations.
For the supply of the board, the input voltages are provided by the Auxiliary Supply Board and opportunely scaled. For the digital circuits, the $5V$ is used to generate $3.3V$ and $1.2V$ (used by uC cores) through LDO regulators.The $\pm 15V$, $3VA$ and $1.5VA$ voltages are obtained by LDO regulators as well. Since the $\pm 15V$ voltages are dedicated to the LEM sensors, the most power-consuming elements in the control system, and linear regulators show typically poor efficiency, three couple of $15V$, $-15V$ LDO are deployed. In particular, for balanced power-sharing the first and second couples supply three LF510-S and LF1005-S (Buck-interleaved, input and primary currents), while the last deals with the more powerful ITN900-S ULTRASTAB and CV3-2000 current and voltage transducers. For a correct working operation, the uC checks also the status of $12V$ and $\pm 18VA$ voltages through two voltage dividers that generate power-good signals.
Concerning the acquisition network of current signals, the LEM sensors produce a current-mode output which has to be transformed in voltage, conditioned by an

opamp and then supplied to the ADC. The current-mode signal is more immune to interference and can easily travel unchanged through the cabinet and the board up to the burden resistor. The burden resistor is placed as close as possible to the opamp in the control board to minimize voltage noise. Then the signal must scaled and positively biased to take into account bidirectional current. For this purpose, an opamp in differential configuration with level-shifter is used.
Regarding the voltage sensing, as said previously V_{out} is acquired by the CV3-2000 LEM sensor, while voltage dividers are exploited for the others. The voltage dividers are directly placed on the Control Board, meaning that very high voltage must be accounted in the PCB. This choice consents a better measurement resolution because high voltage is less sensible to switching noise when terminated to high impedance as in this case, however a $6mm$ creepage distance is kept among potentials referred to different grounds. Of course isolation is needed [27], so the ACPL-C87AT-500E isolated differential amplifier by Broadcom is used for the acuisition of these signals. Its isolated voltage supply is generated by a very low-power push-pull converter. Since the voltages are referred two three bus-bars, three push-pull converters are adopted and power-good signals are provided to uC for measurement consistency through opto-couplers. For V_{out}, the LEM sensor outputs directly a voltage that can be conditioned. Since this signal can be affected by noise, a back-up voltage divider is deployed in case of issues on CV3-2000 output. From safety and normative point of view, the most critical section is the sensing of V_{in}. This voltage comes from the AFE without galvanic isolation. Hence, the Annex K of IEC 61010-1 [27] normative must be followed. In particular, the voltage category II is considered where the creepage distance is $3mm$. However, to implement double-isolation, a creepage of $6mm$ is kept. For the other voltages the situation is less critical thanks to the high-frequency transformer, but same distance is kept anyway.
The Control Board interacts with power modules by means of 18 CGD12HBXMP driver boards. The signals between the control board and the drivers are: PWM gate control, fault, temperature, enable and reset signals. Except for the last two, the other signals are differential, so TX and RX line driver transceivers are used. In particular, transceivers with four differential inputs for TX ones in the same chip and 4 differential outputs for RX ones in the same chip have been chosen. This allows to manage a couple of power modules with a couple of TX/RX transceiver simplifying the routing and minimizing the skew delay on PWM signals. The minimization of the skew is very important because of the high commutation frequency, the fast commutation of SiC devices and the short dead time adopted for efficiency maximization. The source of skew in the PWM signal has been accurately investigated and its minimization is obtained by accurate component selections. The main components contribution to this misalignment of time delays of different gating signals are shown in Figure 3.20: the TX transceiver in the Control Board, the RX transceiver, shoot-through protection circuit and isolated drivers in the driver board.

Summing up all the contributions, considering opposite delay terms for the signals in every chip, a maximum skew of $43ns$ could be estimated. However this is an unrealistic computation, therefore a more realistic value of $25 - 30ns$ can be considered. This skew can be considered acceptable given an estimation of the SiC module minimum commutation time around $50ns$ and the selected dead

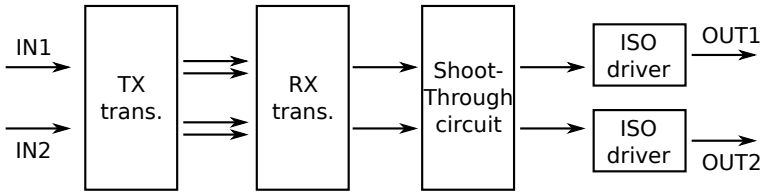


Figure 3.20: PWM signal path

time of $300ns$. Regarding the frequency-modulated signals for monitoring the temperature of the SiC modules, given the slow dynamic of this characteristic, they are multiplexed and acquired one by one through the eCAP embedded peripheral by the CPU, while the fault inputs are in OR-ing configuration to obtain a main fault signal for the DAB converter and another for the Buck interleaved stage.
For temperature measurement purposes, in particular for magnetic components, ten NTC inputs are handled by typical voltage divider configuration and opamp for signal buffering. Then a multiplexer controlled by uC acquires each temperature signal for a fixed period still faster than temperature time-constants.

3.4 System implementation and preliminary functional tests

3.4.1 Hardware System

The compactness of the design enabled by the described choices on technologies and operating frequency enabled to place the entire DC-DC converter in a single standard 19' rack cabinet (2200x800x800mm). The layout of the entire system was accurately developed in a 3-D CAD: the accuracy of the 3-D design of the system is very important for an accurate placement of all the components: this is fundamental to minimize parasitic effects, avoid strong interference and spurious signal couplings and to optimize the cooling system effectiveness. Figure 3.21 gives a frontal view of the system highlighting three main sections. Section A is made of the primary bus-bar, capacitors forming C_{bus}, the primary-side full-bridge of DAB and the planar transformer. In section B there are the two secondary-side bus-bars that connect the secondary-side full-bridges of the DAB and Buck-interleaved converters, including the first filtering stage (L_1, $C_{F1,2}$). Lastly, section C is basically the output filter of the system consisting in L_2 and C_{out}. In the picture of Figure 3.22, a secondary side bus bar connecting the SiC modules of the secondary-side bridge of the DAB to the SiC modules of the Buck converter is provided. It is interesting to notice that the connections among sections have different requirements. In the DAB stage, the AC current flowing between power modules and transformer has a $50kHz$ fundamental and a non-negligible 3^{rd} harmonic. Considering also the skin effect, Litz cable have been chosen. The currents flowing into Buck filters have a reduced AC component at $50kHz$ ($20A_{RMS}$) thanks to L_1 inductors, however same previous Litz cable are used for maximum performance. Instead, simple connection bars are used in section C given the negligible PWM content of output current.
The developed Control Board and the Auxiliary Supply Board are shown in Fig-

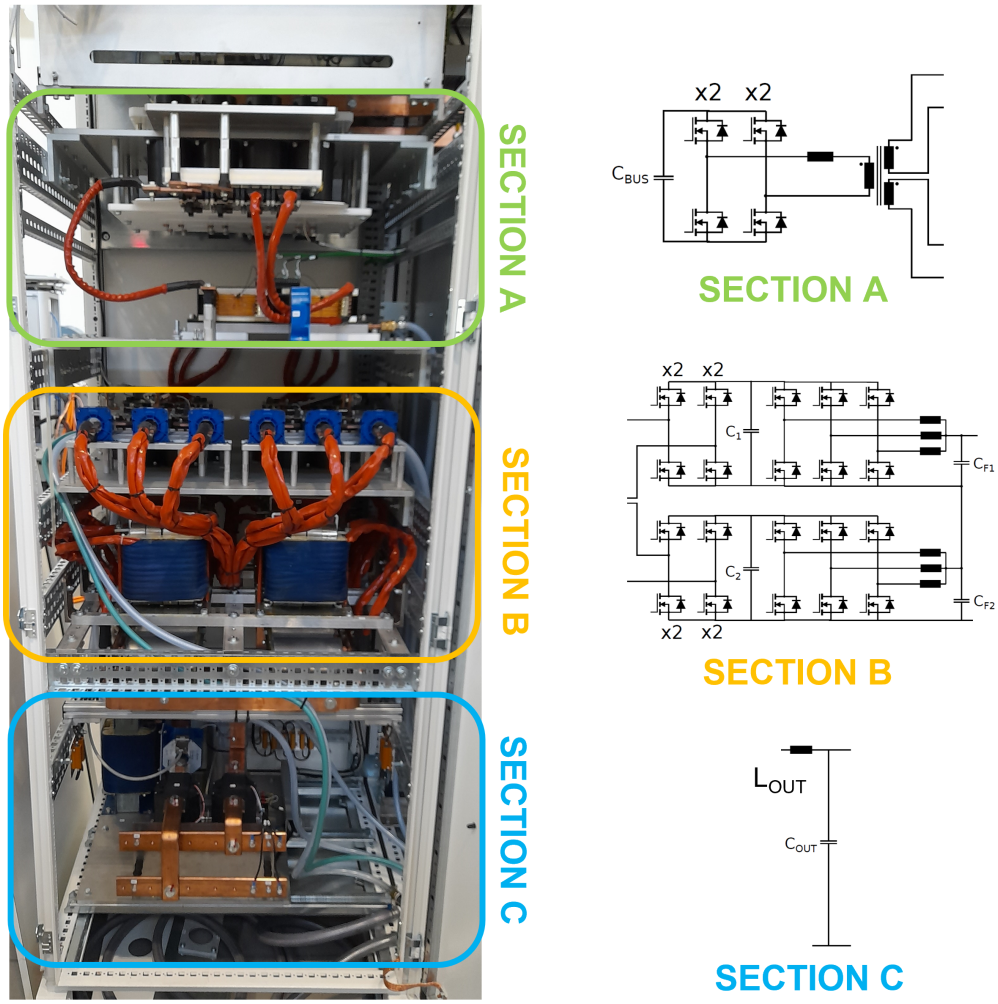


Figure 3.21: Power system picture and associated block diagrams

ure 3.23.They have been implemented in 4-layers FR4 PCBs. The dimensions of the Control Board are $215x301mm$. This board can be divided in five macro sections, highlighted by rectangles in the picture. The central rectangle (white) includes the CPU and the communication peripherals, the bottom rectangle (yellow) the driver connectors and transceivers, the right one (red) the supply signals for the digital and analog components, the upper left (orange) the voltage sensing and the last one (blue) the current sensing. The Auxiliary Supply Board has dimensions $150x160mm$. The Flyback circuit is within the yellow rectangle, while the Buck for the digital $5V$ is in the blue one.

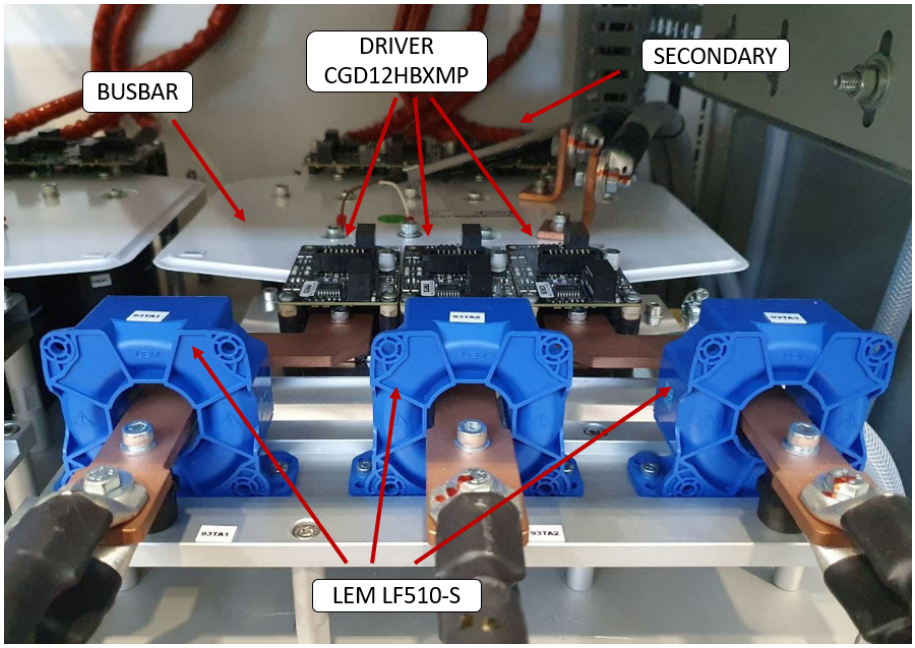
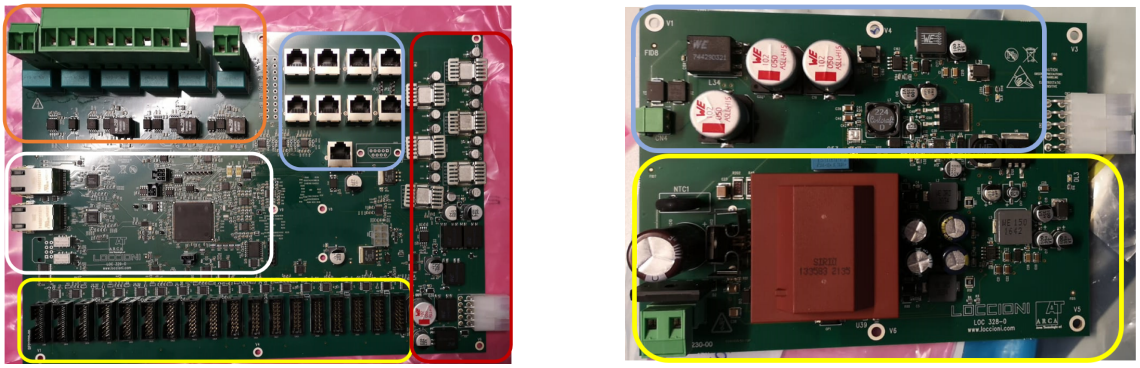


Figure 3.22: Secondary side Bus-bar and SiC power modules with drivers



(a) Control Board (b) Supply Board

Figure 3.23: PCBs for the control algorithm managing

3.4.2 Experimental results

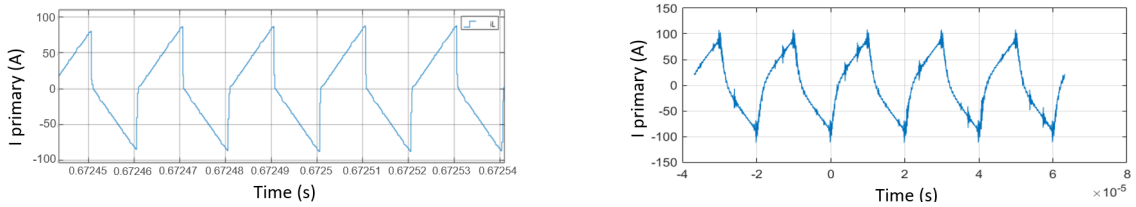
Some preliminary functional tests have been carried out on a part of the prototype converter. The testing setup is made of the DAB converter kept in open-loop (fixed ϕ) with one secondary left in open circuit, while the other is connected to the Buck interleaved converter in closed-loop control. The input voltage is

provided by the ITECH IT6018C-1500-40 power supply while the load is made of four parallel power resistors of 10Ω, 6kW each. The characteristics of the power supply limit the test to 18kW of input power. A 16kW output power test was carried out to preliminary test the functionality of the system. A PSIM-Simulink co-simulation was carried out with the same conditions. The expected voltages for the different sections of the converter in this test are listed in Table 3.6

Table 3.6: 16kW test

V_{in}	V_{DAB}	V_{out}	P_{out}
420V	280V	200V	16kW

It can be noticed that the voltage produced by the DAB converter V_{DAB} is just V_{in} multiplied by the transformer winding factor. Indeed for this low power target, the phase-shift value is absorbed by the dead-time without regulating V_{DAB}. The measured value of the voltages and of the the primary current of the transformer are shown in Figure 3.25 and are in fairly good accordance with simulations. Figure 3.24. This test is a preliminary indication of the effectiveness of the design of the power converter, and controlling boards and of the usefulness of the developed simulation set up that is capable to reproduce the actual converter operation even in a regime very far from nominal operation.



(a) Simulation (b) Scope acquisition

Figure 3.24: Primary current of the transformer in the 16kW functional test

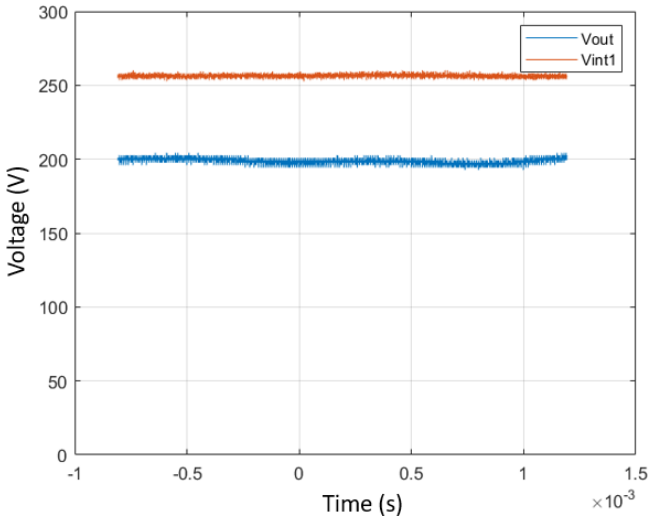


Figure 3.25: V_{DAB} and V_{out} scope acquisitions for the 16kW test

After these preliminary functional test, the same configuration of the set up (i.e. with on a single branch of the secondary side of the DAB connected to an

interleaved Buck converter) has been connected to a $100kW$ power supply and a $80kW$ electronic load to test the system in an higher power regime. In this high-power test bench the converter was tested in 3 different steady state conditions, with the DAB converter working in Boost Mode, Buck mode and Nominal mode (i.e. $Vin = nVout$ in the DAB waveforms). The measured waveforms of the primary side current and primary/secondary side voltages of the DAB converter for this characterizations are shown in Figure 3.24: the waveforms are very clean and the shape of the primary side current (i.e. the slope of the current) is clearly representative of Boost Mode, Buck mode and Nominal mode operating regimes. In Table 3.7 the corresponding measured performance of the converter for these three tests are listed. It can be noted that the overall efficiency is very high even for these operating points at about 1/3 of full power (considering that only 1 half of the converter is operating) and the results are in very good accordance with what expected with the simulations. The complete system is undergoing a complete set of functional and performance e test at the Loccioni Laboratories before final industrialization and commercialization.

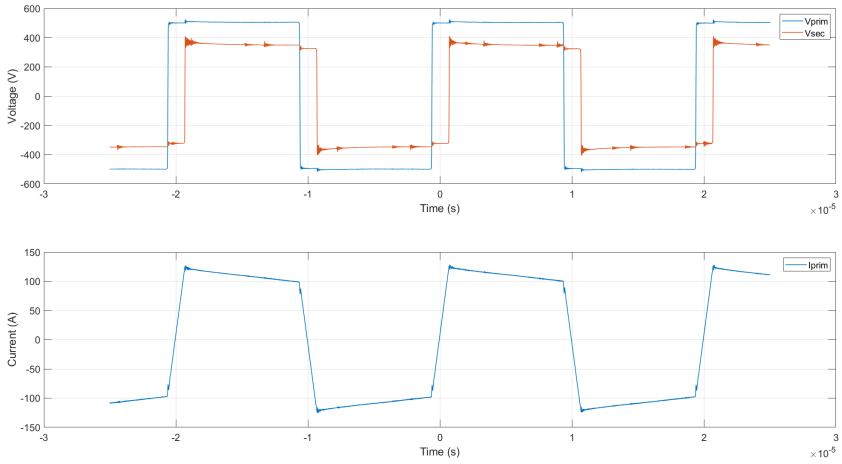


Figure 3.26: Measured primary and secondary voltage waveforms and input current of the DAB operating in Boost mode with the system delivering $Pout = 49.6kW$

Table 3.7: Main results for the test in steady-state condition for the single-branch working configuration (with parallelized power modules on DAB primary side)

Case	ϕ	V_{in}	I_{in}	P_{in}
Boost Mode	23.7°	$510V$	$101.18A$	$51.6kW$
Buck Mode	24.9°	$510V$	$101.18A$	$51.6kW$
Nominal Mode	40.2°	$510V$	$143A$	$72.9kW$
$V_{out,DAB}$	V_{out}	I_{out}	P_{out}	efficiency
$350V$	$200V$	$248A$	$49.6kW$	96.1%
$330V$	$200V$	$248A$	$49.6kW$	96.1%
$340V$	$200V$	$350A$	$70kW$	96%

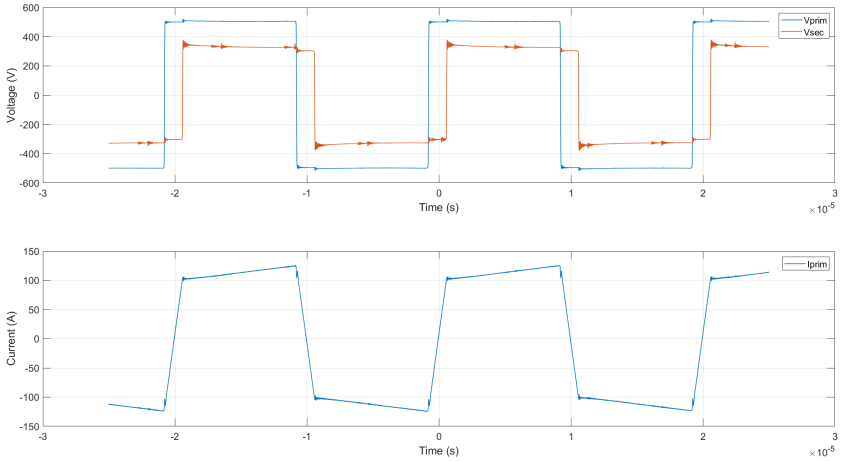


Figure 3.27: Measured primary and secondary voltage waveforms and input current of the DAB operating in Buck mode with the system delivering $Pout = 49.6kW$

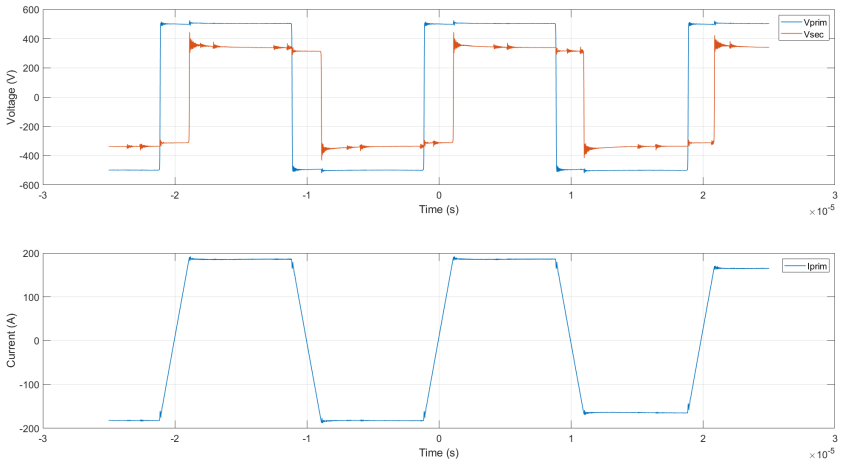


Figure 3.28: Measured primary and secondary voltage waveforms and input current of the DAB operating in nominal mode (i.e. unit voltage gain) with the system delivering $Pout = 70kW$

3.5 Conclusions

The design of a 350kW DC-DC power converter to be used as a battery emulator for automotive component testing has been described. The design choices in terms of components, technologies, circuit topologies and control architecture enable to meet state of the art performance in a compact and easily deployable instrument solution. The instrument has been fully implemented and tests up to more than 1/3 of full power have shown results that match the design goal and simulations. The system is undergoing final tests before industrialization and commercialization.

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Chapter 4

Measurement setups for GaN HEMT transistor ON-Resistance characterization

High voltage (i.e. $> 600V$) GaN power switches are today the major enabler towards the development of a new generation of switching-mode power converters with upgraded performances in terms of power density, efficiency and simplified thermal management. The superiority of this Wide Band Gap (WBG) technology can be mainly summarized as reduced conduction and switching losses with respect to silicon technologies. Compared to SiC WBG technology, for nominal breakdown voltages up to $650V$, GaN has also demonstrated the capability to further increase the application frequency, allowing for an additional enhancement of volumetric power density, due to reduced dimensions of magnetics and capacitors [1], [2]. Higher frequency regimes with associated high efficiency have also beneficial impact in the choice converter topologies [3],[4] and on the power converter control bandwidth. High-voltage GaN switches for power conversion applications are typically AlGaN/GaN-on-Si high electron-mobility transistors (HEMTs) ([5]). This type of devices (mainly with SiC substrates) have a 20-year heritage in the field of RF and microwave applications, where they are nowadays adopted for the implementation of analog amplifiers delivering up to tens of watts up to $40 - 50GHz$. The adaptation of these technologies to power converter applications required technological solutions to obtain higher breakdown voltages [6] (from tens of volts to several hundreds of volts) and the exploitation of p-doped GaN gate to get normally-OFF devices [7] (RF/microwave GaN HEMTs are normally-ON devices). At present, these developments have led to availability of GaN power switches with typical breakdown voltages up to 600-$650V$ and optimal driving voltage V_{GS} of about $5V$ [8], [9], [10]. Other switches with $50V$, $100V$, $200V$ breakdown voltage with very high current capability can also be found in the market [11], [12], whereas only very few experimental devices of $900V$ technologies have recently been proposed [13]. While there is a tremendous interest on this high-voltage GaN technology especially in the automotive market [14], these products have a limited heritage and several providers are still optimizing their processes internally or in contract research foundries. One peculiar characteristic of GaN technologies is the presence of charge trapping effects. As documented in the literature, GaN transistors are always affected by trapping states that modulate

the number of carriers available for conduction into the channel [15], [16]. The high electric field induced by the high voltage applied to the device during the blocking state of switching-mode operation triggers charge capture. The charge trapping is a very fast process that is typically almost entirely activated even for very short duration of the blocking voltage (ns). Conversely, when the device is driven into conduction with $V_{DS} \simeq 0V$, the inverse phenomenon takes place, namely charge release, which is typically much slower. For this reason, operatively, when the blocking voltage is removed, and the device is switched ON for the conduction part of the period, several charges are not available for the conduction and the observed R_{ON} in dynamic condition is larger than its static value. The slower is the charge release mechanism the higher is the degradation of dynamic R_{ON} [17], [18]. The charge release time constants are accelerated by higher temperature. Thus, R_{ON} degradation is a function of the switching frequency (i.e. amount of time for charge release during the device ON-time) and temperature. Moreover, it is also a function of the application voltage, since the amount of charge trapping increases with the electric field, that is a function of the blocking voltage. The dynamic modulation of R_{ON} is a very important topic, since it directly affects the converter efficiency and can lead to reliability concerns due to the higher dissipated power than expected from nominal static characteristics of the device. While a complete elimination of this effect is impossible for GaN devices, its minimization is possible by means of technological choices and optimizations [18], [19]. In this context, it is extremely useful for foundries and research centers to perform a reliable characterization of R_{ON}, not only by traditional static or small signal measurements, but also in large-signal and dynamic regime, in which the dependence of this phenomenon to voltage, frequency and temperature should be identified. For this purpose two measurement setups have been implemented to evaluate the R_{ON} degradation of an experimental $600V$ GaN switch as a function of the V_{DS} blocking voltage, the V_{GS} driving voltage, and at different temperatures. The first performs the characterization of the ON-resistance directly at on-wafer level (Section 4.1), the second proposes a technique for the characterization under real operating conditions by means of the design of a half bridge switching leg in which the DUT is operated under conditions that resemble its operation in a power converter (Section 4.2).

4.1 On-Wafer measurement setup

This section describes a measurement set-up for a precise characterization of the dynamic R_{ON} of high-voltage on-wafer devices with the possibility to modify the V_{DS} blocking voltage, the V_{GS} gate driving voltage, the commutation period and the temperature to assess the impact of each contribution. This type of set up can be valuable for foundries to test different solutions of experimental devices during the optimization of a new process and for the quality verification of production wafers. Indeed, since it is associated to trapping phenomena, the wafer to wafer dispersion of the dynamic R_{ON} can be also considered an indication of possible reliability concerns. The proposed measurement methodology is described in Section 4.1.1; Section 4.1.2 describes the implemented set up, while the experimental measurements are provided in Section 4.1.3.

4.1.1 Dynamic measurement methodology

The proposed time-domain technique for the evaluation of the power switch DUT $R_{DS,ON}$ is described in this section. The DUT is measured under a periodic isothermal regime described in the waveforms of Figure 4.1. The diagram of Figure 4.2 summarizes the measurement procedure settings and steps. During the period, the DUT is switched between a bias state $(V_{GS,ON}, V_{DS,ON})$ and a blocking state $(V_{GS,OFF}, V_{DS,Block})$. As described in the waveforms of Figure 4.1, a short safety margin T_D ($500ns$, as will be described in the next section) between V_{GS} and V_{DS} transitions is used to avoid over-currents at the application/release of the blocking voltage $V_{DS,Block}$. The blocking state duration is negligible with respect to the period, thus the DUT is biased in the selected bias state for more than 99% of the period (i.e. V_{GS} waveform duty cycle is more than 99%). The bias state $(V_{GS,ON}, V_{DS,ON})$ is selected so that the corresponding $I_{DS,ON}$ meets the following requirements: 1) it must be large enough to enable an high-accuracy current sensing; 2) it must be small enough to induce a negligible power dissipation $(P_{DISS} = R_{DS,ON} \cdot I^2_{DS,ON})$, so that the DUT can be considered isothermal with the thermal chuck of the probe station over which is placed during the entire duration of the measurement.

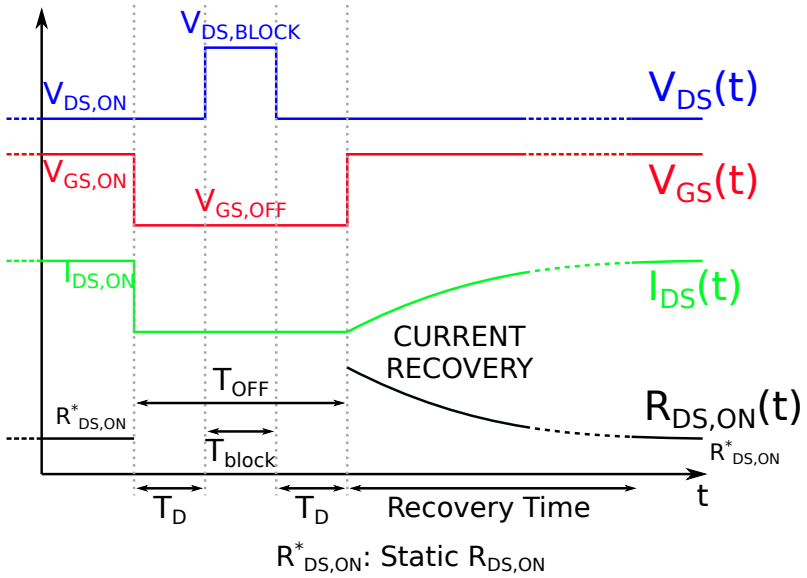


Figure 4.1: Typical waveforms of V_{GS}, V_{DS} and I_{DS} during the dynamic characterization

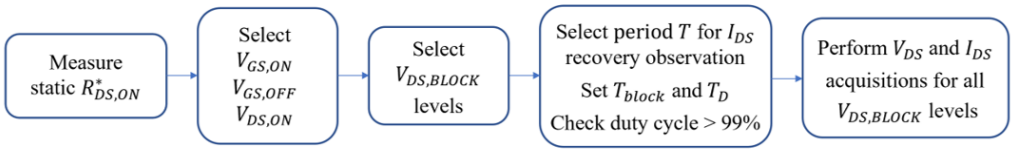


Figure 4.2: Setting and steps of the proposed measurement procedure under periodic regime.

In this way, thermal effects are not involved in the observed dynamics of the drain current, and they can be exclusively ascribed to trapping/de-trapping mechanisms. During the application of the blocking voltage in T_{Block}, the combination $(V_{GS,OFF}, V_{DS,Block})$ applies high electric fields to the DUT channel that trigger

charge trapping phenomena, as in switching-mode power converter operation. By reapplying the same bias state $(V_{GS,ON}, V_{DS,ON})$ after the blocking event, the slow recovery of the drain current towards the $I_{DS,ON}$ can be observed. If the period duration is selected large enough to complete the entire de-trapping mechanism, $I_{DS,ON}$ at the end of the period can be considered the static value of the current, and the corresponding value of the ratio $R_{DS,ON}(T_P) = R^*_{DS,ON} = V_{DS}(T_P)/I_{DS}(T_P)$ at the end of the period T_P the static $R^*_{DS,ON}$. The result of this characterization is the dynamic variation of $R_{DS,ON}$ over time after the blocking voltage event that triggers the trap capture, which is the lower plot of Figure 4.1. This gives an immediate indication of the time constants related to the de-trapping mechanisms, which is a useful input for process evaluation and for the physical modeling. On the other hand, also a direct indication related to the application can be obtained considering the inverse of the recovery time $f_s = 1/T_{recovery}$ as the corresponding switching frequency of the application: in this way, $R_{DS,ON}$ degradation for the actual switching frequency of the application can be evaluated. By varying the values of $V_{DS,Block}$ and $V_{GS,OFF}$, the dependence of $R_{DS,ON}$ degradation from applied voltages is assessed. Finally, by varying the thermal chuck temperature (and thus the DUT temperature since it is practically iso-thermal) the effect of temperature can also be evaluated: indeed trap energy states are temperature dependent. The proposed set up can implement this characterization with the flexibility to vary all the described parameters. The main challenges of this implementation are the capability to apply precise dynamic high voltage excitations to the DUT and to realize a precise and noiseless dynamic sensing of current/voltages for the computation of the dynamic $R_{DS,ON}$.

4.1.2 Setup description

A functional simplified description of the setup is illustrated in Figure 4.3. The DUT is placed in a probe station where gate, source and drain pads are directly contacted with low-parasitics on-wafer probes, while a thermal controlled chuck (Temptronic TP03215A) sets the working temperature beneath the wafer or the metal carrier used for soldering bare die device samples.

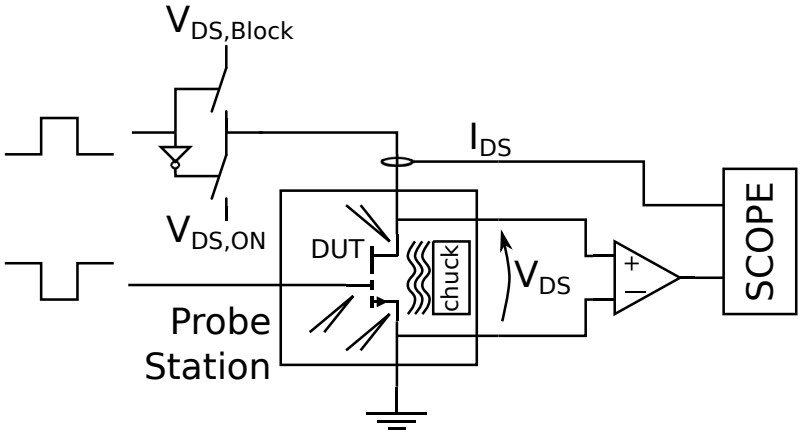


Figure 4.3: Functional simplified description of the setup

The V_{DS} excitation switching between $(V_{DS,ON}, V_{DS,Block})$ values needs to be provided by an isolated and fast switching-leg that alternatively connects the DUT drain pad between two isolated voltage sources at $V_{DS,ON}$ and $V_{DS,Block}$ values

provided by dedicated power supplies. The DUT $I_{DS,ON}$ and $V_{DS,ON}$ are sensed by current/voltage probes and acquired by a digital oscilloscope. A more detailed description of the implemented set-up is provided in Figure 4.4.

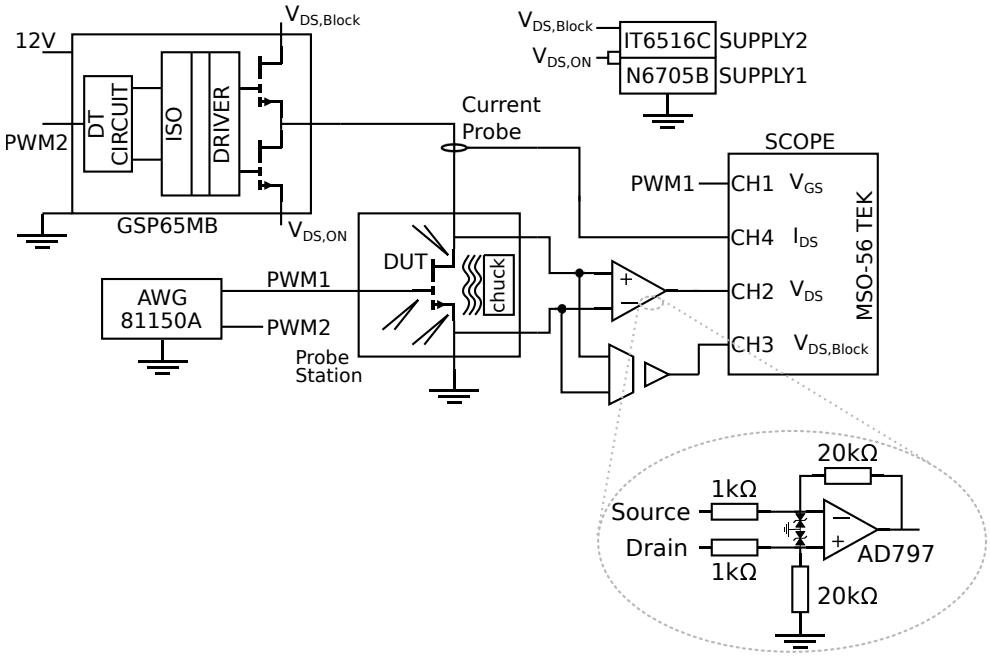


Figure 4.4: Schematic of the reconfigurable setup for dynamic R_{ON} measurement

The Probe station is a Cascade Microtech Summit 9000 equipped with a Temptronic ThermoChuck system. In order to reproduce excitations similar to operative regimes, the switching-leg needs to have dynamic characteristics similar to the DUT. Thus, it is realized exploiting the GSP65MB Evaluation Board of GaN System [20]: this is basically an half bridge exploiting commercial $25m\Omega$, $650V$ GaN HEMT devices (which represent the state of the art high-voltgae GaN switches), Silicon Labs Si4121 isolated gate drivers, dead-time logic circuitry for selectable dead-time control and local low-inductance DC-link capacitors to sustain fast commutations without voltage drops. The DC supplies for the bias $V_{DS,ON}$ and blocking voltage $V_{DS,Block}$ generation are Agilent N6705B and ITECH IT6516C, respectively. The Agilent 81150A arbitrary waveform generator is used to control the switching-leg (PWM2 in the figure) and to directly control the DUT gate (PWM1 in the figure), assuring the required synchronization to the two excitations (V_{GS}, V_{DS}). Wide-band current sensing is provided with Keysight $100MHz$ N2783A current probe with 1% accuracy. The sensing of the device V_{DS} is quite complex, because of the required dynamic range: the characterization procedure needs to measure high $V_{DS,Blocking}$ during the device switch-OFF to verify the blocking voltage and its synchronization with the DUT V_{GS}, and very low $V_{DS,ON}$ during device conduction for an accurate evaluation of $R_{DS,ON}$. In particular for $600V$ GaN switch technology, the maximum $V_{DS,Block}$ is in the order of $400V$ and $V_{DS,ON}$ in the order mV. For this reason a single acquisition channel for V_{DS} is not a viable solution, but two different methods are used simultaneously, as described in Figure 4.4. A first acquisition channel uses the isolated active differential probe with $40MHz$ bandwidth Aaronia ADP1 to acquire the entire evolution of V_{DS} in the period and scale it 100:1 to fit the oscilloscope voltage range: this is useful to monitor $V_{DS,Block}$ and the synchronization with V_{GS}, but this acquisition does not

have enough sensitivity for a precise and useful acquisition of $V_{DS,ON}$. For this acquisition, a high sensitivity and wide-band acquisition channel is implemented in a dedicated PCB exploiting the low-offset and low-noise Analog Devices AD797 operational amplifier, in the x20 voltage gain configuration described in the inset of Figure 4.4. This acquisition channel enables the accurate characterization of V_{DS} waveform below $1mV$. As described in [21], with this configuration, the Op-Amp input is protected by means of two TVS diodes in antiparallel configuration from high-voltage $V_{DS,Block}$. This solution avoids the saturation of the oscilloscope acquisition channel and largely limits the saturation of the Op-Amp. As a consequence, few us after the blocking event, the Op-Amp exits saturation and is capable to correctly measure $V_{DS,ON}$ and then $R_{DS,ON}$ can be computed. Finally, a simple passive probe is used to sense the driving voltage V_{GS} applied to the DUT. The digital oscilloscope used in the setup is Tektronix MSO-56 scope. A picture of the entire set up is provided in Figure 4.5.

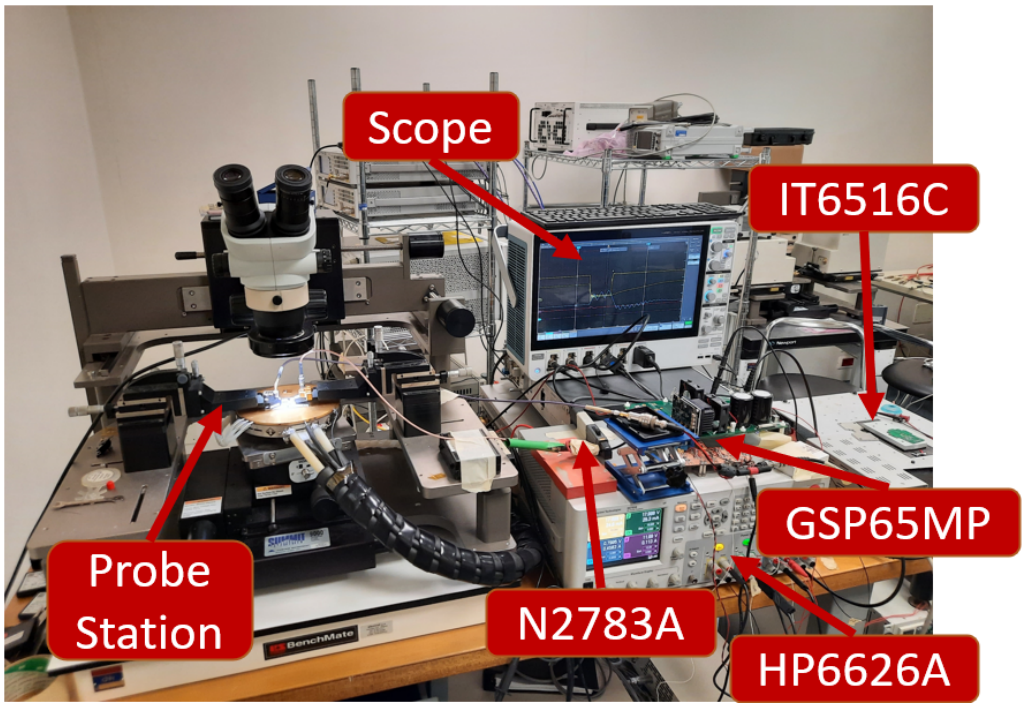


Figure 4.5: Picture of the reconfigurable setup for dynamic R_{ON} measurement in the laboratory

4.1.3 Experimental characterization of 600 V GaN switches

The described measurement setup is used to characterize the dynamic ON-resistance of $600V$ GaN transistors. The transistors are p-GaN e-mode HEMTs on Silicon substrate coming from an experimental wafer of a process under development phase in a research foundry. The preliminary electrical specifications of the switches are shown in Table 4.1. The very low values of parasitics are indicative of the capability of this technology for high-switching frequency.

The transistors dies have been soldered to a metal carrier and contacted with on-wafer micro-probes.

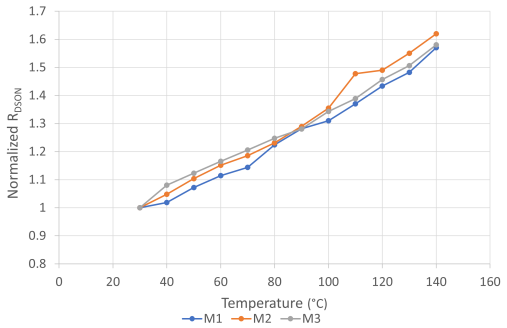
Table 4.1: DUT preliminary electrical specifications.

V_{BD}	V_{gs}	V_{th}	R_{DS}	C_{ISS}[1]	C_{OSS}[1]	C_{RSS}[1]
$600V$	$5-6V$	$2-2.5V$	0.5Ω	$43pF$	$18pF$	$1pF$

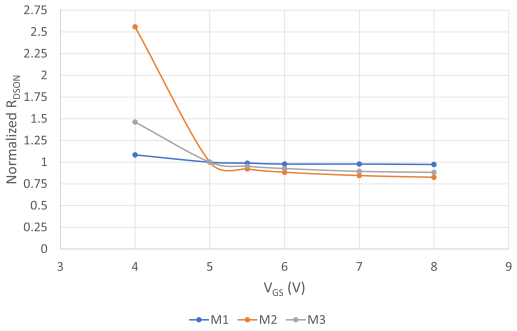
[1] $V_{DS} = 200V$

4.1.3.1 Static Measurements

For the evaluation of the dynamic ON-resistance degradation the static $R_{DS,ON}$ must be identified. A de-embedding procedure based on the measurement of the parasitic resistance of the setup when the DUT is replaced by a short circuit was performed. As discussed before, to guarantee iso-thermal conditions in temperature-dependent measurements of the sole trapping phenomena, the DUT must be properly biased to show a negligible self-heating compared to the temperature controlled by the chuck. Thus a "measuring" bias current of $500mA$ was selected as a good compromise between current measurement accuracy and device self heating. Indeed, since the estimated thermal resistance of the DUT is $2.2°C/W$ and the static $R_{DS,ON}$ around 0.5Ω, the dissipated power is about $125mW$ with a resulting negligible temperature increase $\Delta T = 0.275°C$. This bias current was used for both static and dynamic measurements, that can consequently considered isothermal. The static $R_{DS,ON}$ of three samples M1, M2, M3 was measured at increasing temperature up to up to $140°C$ (maximum rating of the probes): the results are shown in Figure 4.6a, where the $R_{DS,ON}$ is normalized to the reference value at 30°C. Additional static measurements were carried out at different V_{GS} to evaluate the gate driving voltage requirements. The results are shown in Figure 4.6b, where the static R_{DS} is plotted versus the gate driving voltage and normalized to the value at $V_{GS} = 5V$. Above $V_{GS} = 5V$ all the samples are fully ON since the channel resistance reveals a negligible improvement for higher voltages, whilst for $V_{GS} = 4V$ the devices show different behaviors probably due to a shift of threshold voltage which is expected for a young technological process [22]. Hence, $V_{GS,ON} = 5V$ is chosen for dynamic measurements.



(a) Normalized $R_{DS,ON}$ VS Temperature at $V_{GS} = 5V$



(b) Normalized $R_{DS,ON}$ VS V_{GS} for ON state

Figure 4.6: Static measurements for M1, M2, M3 samples

4.1.3.2 Dynamic Measurements

The dynamic measurements were carried out following the procedure described before in Figure 4.1. The measurement period is fixed to $1ms$: indeed, this corresponds to an equivalent application-related switching frequency regime of $1kHz$ and any additional recovery from traps related to higher time constants has surely no interests for any practical application. According to the notation of Figure 4.1, the selected $T_{Block} = 500ns$, whereas the entire $T_{OFF} = 1.5us$ to include two additional $500ns$ dead bands to avoid over-current events. The first test was the sensitivity of $R_{DS,ON}$ to the gate switch-OFF voltage $V_{GS,OFF}$. Normally-ON GaN devices are typically switched off with null or negative V_{GS}. While $V_{GS,OFF} = 0V$ is suitable for a complete device turn off, negative value are often used to shorten the commutation time and increase the margin against undesired turn-ON due to G-D Miller capacitance effect. Nonetheless, negative $V_{GS,OFF}$ values increase the electric fields in the channel during turn off and can potentially increase trapping with a consequent higher degradation of the dynamic $R_{DS,ON}$ effects. The investigation on the sensitivity towards the sole $V_{GS,OFF}$ was performed by setting the blocking voltage $V_{DS,Block} = 0V$ at $25°C$. The time domain waveforms of this test are shown in Figure 4.7.

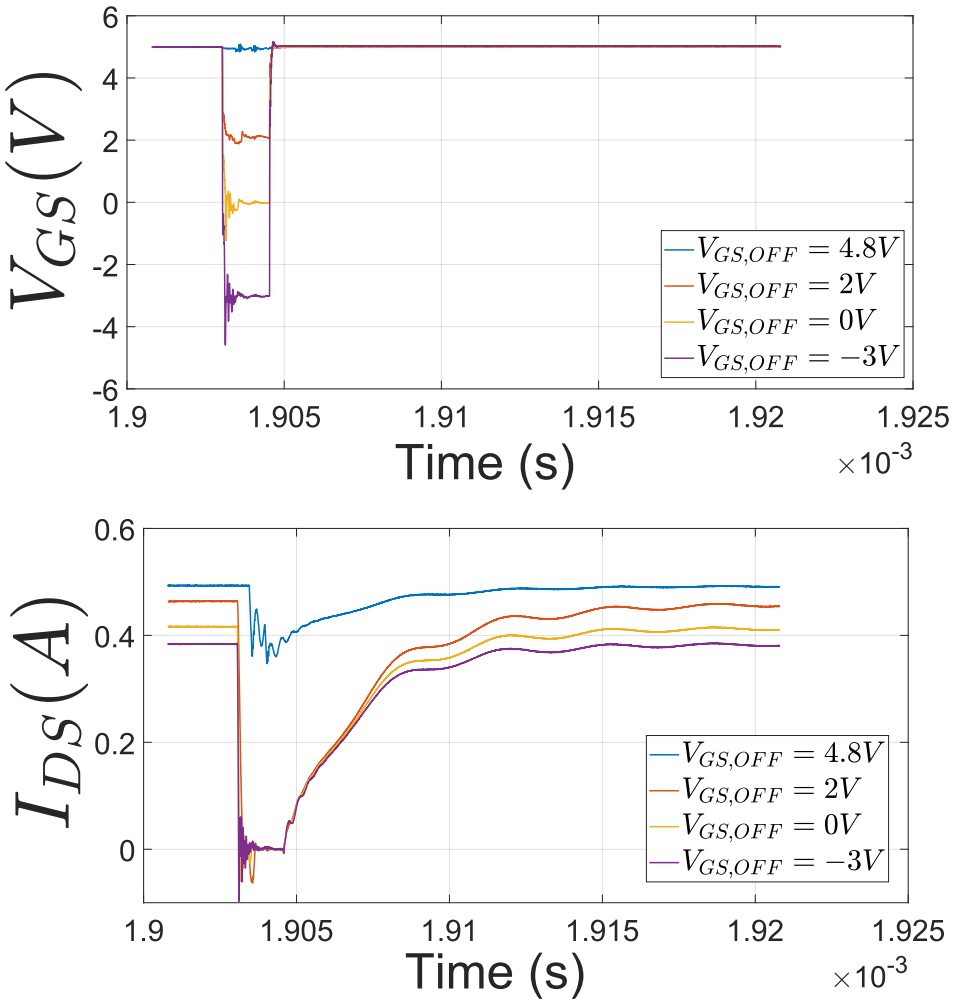


Figure 4.7: V_{GS} (up) and I_{DS} (down) waveforms in case of null blocking voltage at $25°C$. The displayed time interval starts $5us$ before the trigger event and ends $20us$ after the trigger event.

It is evident that $V_{GS,OFF} = 2V$ is sufficient to completely switch off the device: the simple event of device switch-off triggers trap capturing mechanisms that causes a decrease of the drain current, that do not recover completely even after the entire period of $1ms$. Indeed, the asymptotic current value (i.e. $I_{DS,ON}$ of Figure 4.1) for all the conditions where the device has effectively switched off (i.e. $V_{GS,OFF} = 2V, 0V, -3V$) is lower than the reference value with $V_{GS,OFF} = 4.8V$. The lower $V_{GS,OFF}$, the higher the current $I_{DS,ON}$ reduction for fixed $V_{GS,ON}, V_{DS,ON}$. From the figure it can also be observed that the current recovery is divided in two parts: an initial fast recovery where in $15 - 20us$ the current reaches about 90% of its asymptotic value and a second slow recovery that lasts for the rest of the $1ms$ period. This is an indication of different time constants associated to the de-trapping mechanisms as observed in other studies [23]. As a summary, in Figure 4.8 the measured degradation of $R_{DS,ON}$ (evaluated at $1ms$) for the three samples and normalized to the nominal case is shown. For this particular technology, still in the early development phase, if the device is switched-off with negative $V_{GS,OFF}$ for better driving performance (increased noise immunity and fast commutation) the conduction performance get worse, due to increased trapping effects. $V_{GS,OFF} = 0V$ is chosen to perform dynamic measurements at variable blocking voltage provided in the following.

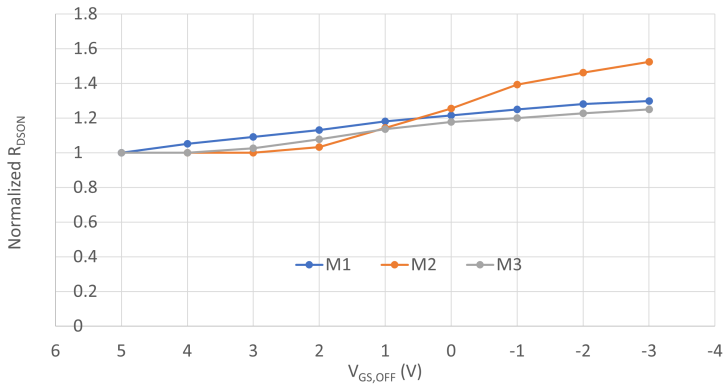


Figure 4.8: Normalized $R_{DS,ON}$ VS $V_{gs,OFF}$ for M1, M2, M3 samples

The effect of increasing blocking voltages $V_{DS,Block}$ on $R_{DS,ON} = 0V$ has been investigated varying $V_{DS,Block}$ up to 400 V, which is typically the maximum DC link voltage for a $600V$ technology. In Figure 4.9 the four main characteristics measured by the setup are displayed.

The two different acquisition channels of V_{DS} show significant information during different parts of the period. The increasing blocking voltages during T_{Block} can be evaluated from the acquisition of the isolated voltage probe, whereas the small value of V_{DS} during the rest of the period is acquired by the high accuracy Op-Amp channel and used for the computation of $R_{DS,ON}$.

It is interesting to observe that the V_{DS} waveform from this latest channel shows the saturation interval of the Op-Amp that lasts only about $2us$ after T_{Block}. Once the Op-Amp exits saturation additional $15 - 18us$ are necessary for a complete extinction of a residual oscillation. Thus the computation of $R_{DS,ON}$ can be considered completely reliable about $20us$ after the blocking voltage event. Additional minimization of parasitics in the construction of the bench could be implemented to shorted this acquisition delay. From the data of Figure 4.9, $R_{DS,ON}$

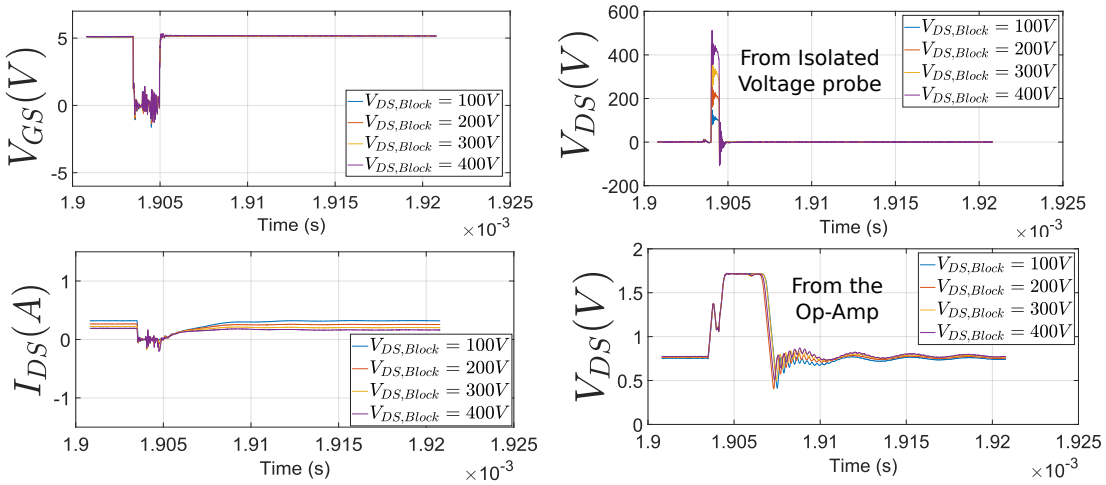


Figure 4.9: V_{GS}, I_{DS}, V_{DS} (from isolated voltage probe and Op-Amp) acquired waveforms for $R_{DS,ON}$ calculation at increasing blocking voltage. The displayed time interval starts 5us before the trigger event and ends 20us after the trigger event.

is computed for the entire period and is shown in Figure 4.10, normalized to the $V_{DS,Block} = 0V$ case.

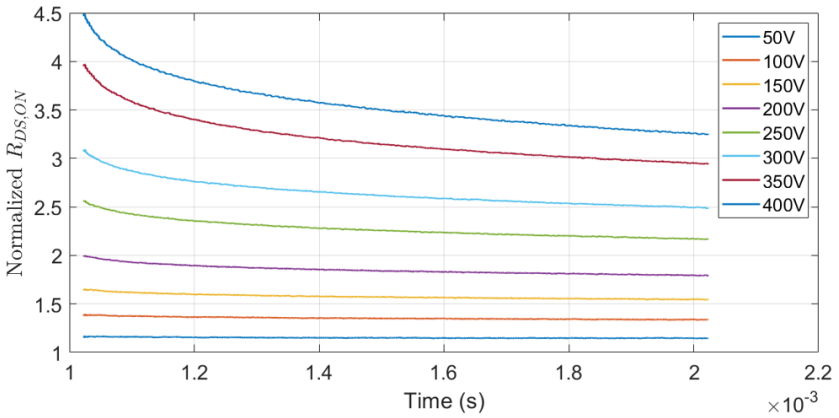


Figure 4.10: Normalized $R_{DS,ON}$ of a single sample measured over the entire ON-time

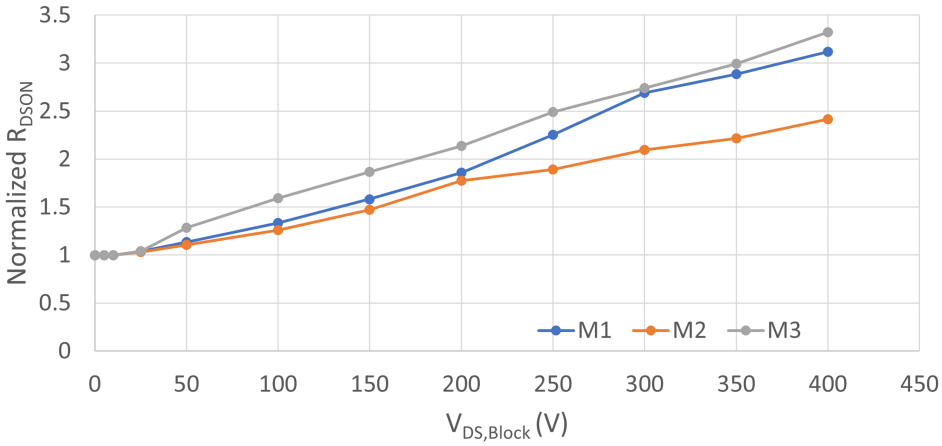


Figure 4.11: Normalized $R_{DS,ON}$ evaluated at the end of ON-time for M1, M2, M3 samples

The waveforms point out that the trap-activated degradation of the dynamic $R_{DS,ON}$ for this technology under development is very relevant. This effect is already detectable at $V_{DS,Block} = 50V$ and gets worse at increasing voltages with $R_{DS,ON}$ reaching up to x4.5 degradation just after the blocking voltage pulse for the higher $V_{DS,Block} = 400V$. In Figure 4.11, the measured $R_{DS,ON}$ at the end of the ON-state is shown for the three samples as a function of blocking voltage. These data confirm the high degradation levels and the dependence with the applied voltage. Nonetheless non negligible differences between samples suggest significant parameter dispersion among devices, another sign of the low level of maturity of the process. The effect of temperature was estimated measuring the DUT $R_{DS,ON}$ for different chuck temperatures. The $R_{DS,ON}$ measured at the end of the $1ms$ period for sample M2 at different chuck temperatures is shown in Figure 4.12. $R_{DS,ON}$ is normalized to its static value at the corresponding temperature. The plots show that the trap-related degradation effect on $R_{DS,ON}$ decreases for higher temperatures. As observed in [24], this is probably due to the fact that higher temperatures accelerate trap release transients and increase the number of compensating trap release events during T_{Block}. The flexibility of the set up enables to set the different parameters according to different requirements. For instance, for trap physical modeling purposes, it could be interesting to evaluate the trap release mechanisms for a longer time frame. The dynamic test at different blocking voltages have been repeated with a much wider period of $40ms$. Figure 4.13 shows $R_{DS,ON}$ evolution from $5ms$ to $40ms$ after T_{Block}: it can be observed that even in a such large time frame the static value of $R_{DS,ON}$ is not reached, indicating that the time constants associated to traps are extremely long.

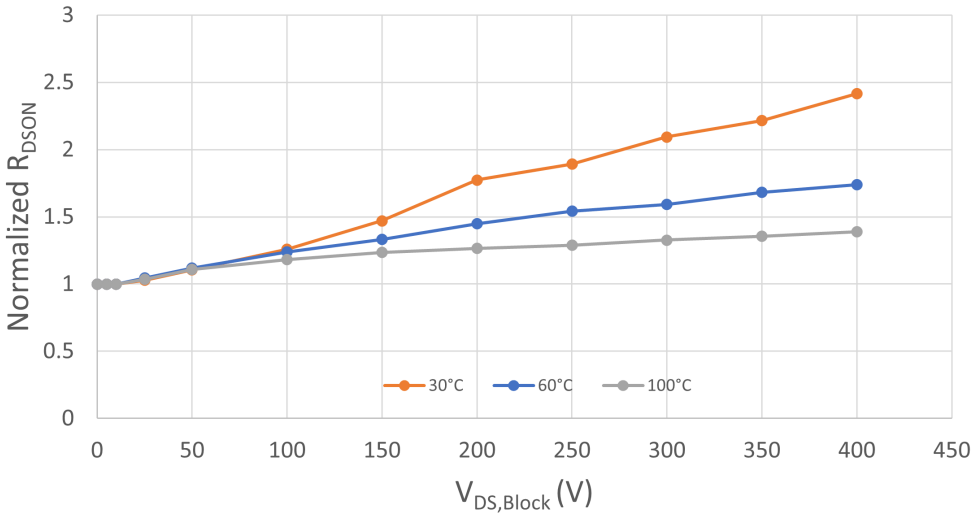


Figure 4.12: Normalized $R_{DS,ON}$ VS V_{block} of sample M2 for three temperature: $30°C$, $60°C$ and $100°C$

Another parameter that can be varied is the duration of the blocking voltage application T_{Block}. This parameter is often described in the literature as the duration of the trap filling pulse. The dependence of the trap induced degradation to the duration of the trap filling pulse has been investigated in the literature, sometimes

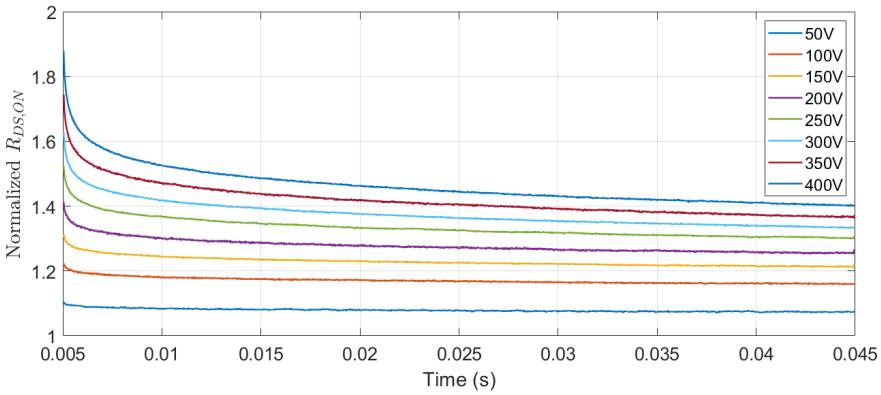


Figure 4.13: Normalized $R_{DS,ON}$ VS $V_{DS,Block}$ with an extended $40ms$ period to evaluate traps' long time constants.

with observed opposite behaviors depending on the duration scale of T_{Block} [17], [25], [26], [27]. For switching mode power converter applications, a dependency of $R_{DS,ON}$ toward T_{Block} implies additional dependency of the device performance versus the variation of the duty cycle. Since the target application frequency of this technology is tens to hundred of KHz, measurements with T_{Block} ranging from $500ns$ to $50us$, while maintaining the same duty cycle, were carried out. These measurements showed practically no dependence of $R_{DS,ON}$ degradation to T_{Block} (in this pulse width variation range).

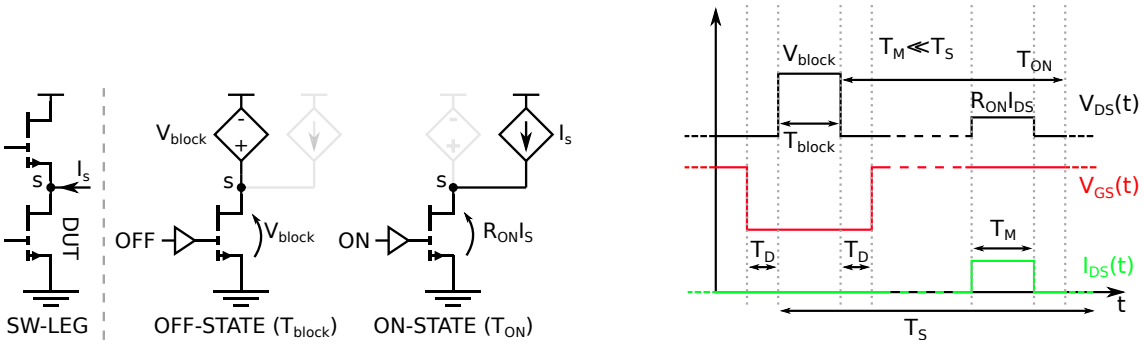
4.2 In-Situ Measurement setup

In this section we propose a set-up and a measuring technique that accurately mimics the operating conditions of the real application. A custom switching module is designed in order to embed the DUT in a half-bridge switching-stage and a measurement procedure is implemented to characterize its dynamic R_{ON} when operating as in a real power converter. The setup is designed to test $600 - 650V$ switches in different voltage, frequency and temperature switching conditions. In Section 4.2.1 the measured procedure is described. The design and implementation of switching module and of the measurement set up are described in Section 4.2.2 and Section 4.2.3, respectively. Finally the results of the experimental characterization of $600V$ GaN switches are provided in Section 4.2.4.

4.2.1 Measurement procedure

The measurement procedure is similar to the one proposed in [21] for low voltage devices. The circuit described in this section implements an half bridge commutation leg with two identical device samples. The low-side switch is the DUT, whereas the high-side device is used to complete the switching leg that is necessary to operate the DUT in the same condition of the real application. The working principle of the measurement technique is outlined in Figure 4.14a and Figure 4.14b.

When the switching leg is commutating, the period can be divided in two parts: during T_{block} the DUT is OFF and the high side device connects the DUT drain to the blocking voltage V_{block} (triggering charge trapping); during T_{ON}, the DUT



(a) Switching leg states during the dynamic periodic measurement procedure

(b) Waveforms of the proposed measurement technique

Figure 4.14: Measurement technique working principle

is in conduction and a precise current source connected to the switching node S is used to inject a measuring current I_{DS} into the DUT. The measuring window within T_{ON} is called T_M. During the measuring window, both the DUT current I_{DS} and the DUT voltage V_{DS} are sensed with accuracy, so that the ON resistance is given by the ratio $R_{ON} = V_{DS}/I_{DS}$. According to Figure 4.14b a safety dead time is introduced between V_{DS} and V_{GS} transitions to avoid shoot through as in a real application. There are two ways to characterize the DUT dynamic R_{ON} as a function of the switching frequency, that are illustrated in Figure 4.15.

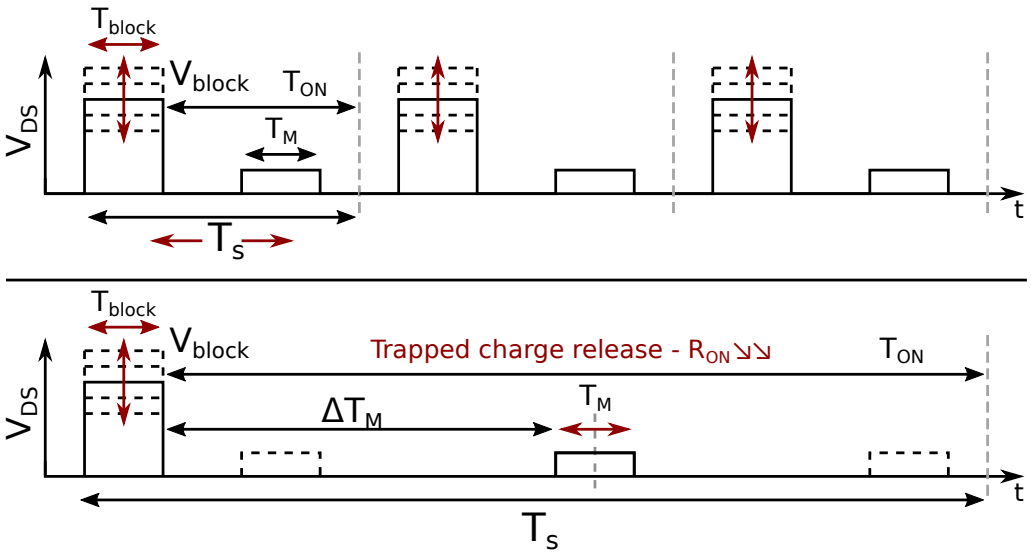


Figure 4.15: Two different measurement regimes. Upper: direct characterization of $R_{ON}(f_S)$ varying the period $T_S = 1/f_S$. Lower: indirect characterization of $R_{ON}(f_S)$ at fixed period T_S and varying ΔT_M

The more direct method is to vary the period T_S within the values of interests for practical applications and measure R_{ON} for every different switching frequency $f_S = 1/T_S$ regime. The waveforms corresponding to this method are shown in the upper part of Figure 4.15: the drawback of this method is that the switching losses also vary with T_S and so the different characterizations are not isothermal. This inhibits the possibility to separate trapping and thermal effects. As described in the lower trace of Figure 4.15, the alternative solution that is proposed is to maintain a fixed, very long period T_S with 99.9% V_{DS} duty cycle (i.e. $T_{block} << T_S$ and $T_{ON} \simeq T_S$) and characterize the R_{ON} variation over time by moving the measurement

window T_M along the very long T_{ON} of the DUT. Indeed, during T_{ON}, the trapped charge release mechanism takes place decreasing the R_{ON} over time. This is an indirect, still equivalent, way to characterize the dependence of the dynamic R_{ON} vs frequency, since we can consider R_{ON} measured in ΔT_M equal to $R_{ON}(f_S)$ with $f_S = 1/(\Delta T_M)$. As can be observed in Figure 4.15, ΔT_M is the distance between the beginning of T_{ON}, and of the associated trapped charge release mechanism, and the measuring instant. This consideration strictly holds if the duration of T_{block} is not important for the observed device performance, that is an alternatively way to state that the charge trapping event can be considered almost instantaneous, with respect to the application time scale. This has been verified and will be documented in the measurement section and it was also observed in other studies [21]. With the proposed procedure the characterization of the dynamic R_{ON} over time, and then, equivalently, over switching frequency, is isothermal, allowing to separate thermal and trapping effects. Moreover, the DUT temperature can be known with fairly good precision by controlling the temperature of the testing module: indeed, by selecting values of the measuring current I_{DS} and measuring window T_M small enough to have negligible self heating effect on the DUT, the DUT channel can be considered at the same temperature of the module carrier. Finally the dependence of the dynamic R_{ON} on the application voltage can be assessed by varying the value V_{block} applied to the DUT.

4.2.2 Design and implementation of the switching module

As discussed in the introduction, the DUT is embedded in a switching module that accurately matches the actual operation of the DUT in a real application. Thus, the designed module is practically the active section of an half bridge power converter. GaN technology characteristics set the specification for the module design. Here the DUT is the same experimental $600V$ p-GaN e-mode HEMT power device on silicon substrate specified in Section 4.1.3 which characteristics are reported in Table 4.1 and with bare-die form with the gate, drain and source pads on the top of the die (Figure 4.16). The extremely low values of parasitic capacitances highlight the potentiality of this technology for very fast commutations. The expected commutation time is around $1ns$, which imposes to accurately design the power converter layout to minimize parasitic inductances and to select a proper driver and by-pass capacitors.

Therefore, all the connections to the rest of the module need to be provided with wire bonding, whose length must be kept as short as possible to minimize parasitics and have a minimal impact on commutation waveforms. Moreover, the die thickness of $1.05mm$ further complicates the design of the switching module assembly (the die is not lapped to the typical $100um$ thickness, since it comes from experimental wafers: this is very typical during process development) . Thus, as illustrated in the sectional view of Figure 4.17, a double-board approach is followed.

A 2-layer 1mm-thick FR4 board is dedicated to the placement of all the SMD components of the module, whereas the switches are placed at the same plane of the top of the FR4 board, exploiting two apertures implemented for their placement (see Figure 4.18). On the other hand, an IMS board is employed as carrier of the GaN switches and stacked beneath the FR4 board. In this way, as

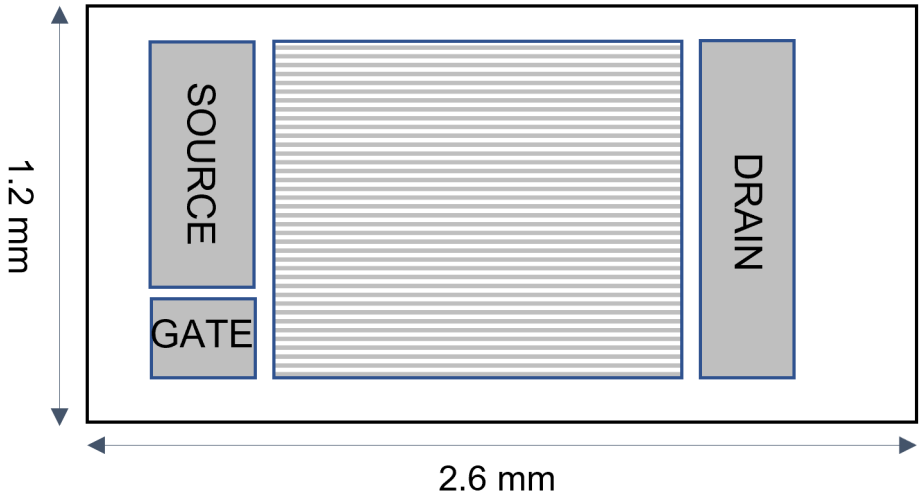


Figure 4.16: Schematic of the bare-die GaN power switch dimensions along with gate, source and drain pads

can be appreciated in the photograph of Figure 4.18, the access points for gate, source and drain pads are on the same level of the FR4 board and the bonding wires' length from the board to the die are minimized. The switches' dies are attached to the IMS board by means of a high-thermal and high-conductive paste: the backside of the switches is the substrate potential, that must be connected to the source of each switch available in the upper side of the FR4 board, thanks to wire bonding connections. Thus, as described in Figure 4.17, filled VIAs in the FR4 board are used to connect the substrate potentials in the IMS board to the device sources on the top layer of the FR4 board.

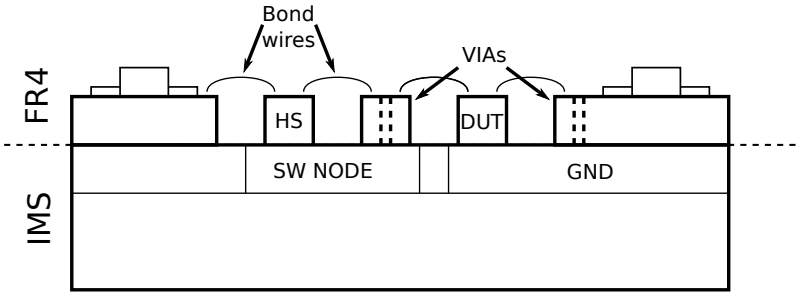


Figure 4.17: Lateral section of half-bridge module

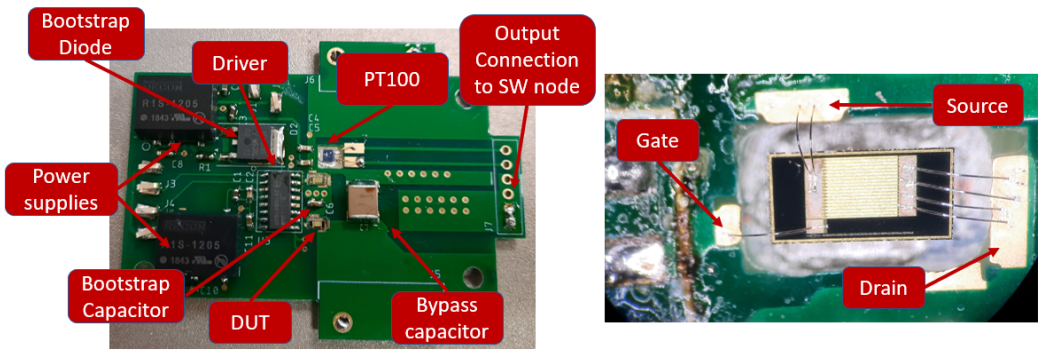
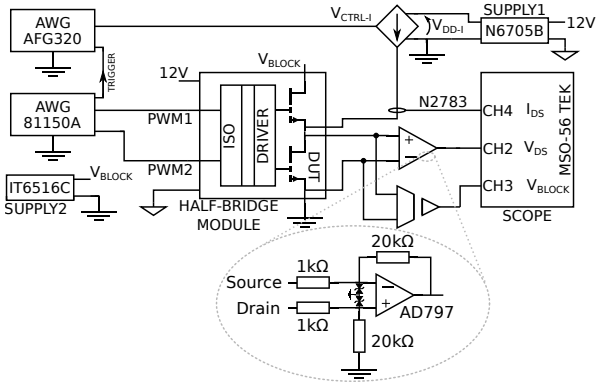


Figure 4.18: Photograph of the implemented half-bridge module with magnification of the die connections to FR4 board with wire bonding

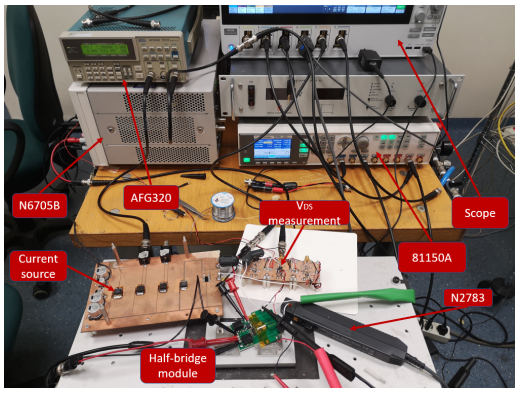
The FR4 board is populated with the SMD components, which are detailed in Figure 4.18. An high-side/low-side Si8273 isolated gate driver by Skyworks Solutions[28] is used to drive the GaN switches with $V_{GS,OFF}/V_{GS,ON} = 0V/+5V$. The component guarantees $2.5kV_{RMS}$ isolation, a $+1.8/-4A$ forward/sink peak currents and very fast rise/fall times, which are ideal characteristics for GaN applications. The high-side driver configuration implements a diode-capacitor bootstrap circuit. The diode is a Schottky rectifier to reduce recovery time and withstand high blocking voltages [29], while $1uF$ is chosen as bootstrap capacitance. It's noteworthy how the capacitance value could be selected ten times smaller for a typical design, given the very low gate charge of this devices [30], [31]; however, a bigger value was selected to sustain the high-side gate driving during the extended commutation periods used in the proposed characterization procedure described above. Two $1W$, 12V-5V low-ripple isolated DC/DC switching converters R1S-1205 by RECOM [32] are used to supply the first and second stage of the isolated gate driver. A $1uF$ ceramic DC-link by-pass capacitor is placed close to the switching leg in parallel to the input voltage (V_{block}) to minimize the power loop stray inductance. The last component of the system is a PT100 thermistor directly placed on the IMS thanks a third opening in the FR4 board. Even though the sensor is not very close to the switches, it provides a good temperature estimation thanks to the wide aluminum substrate of IMS with high thermal conductivity.

4.2.3 Measurement set-up

As described in the Section 4.2.1, the measurement of the dynamic R_{ON} implies the accurate sensing of the drain-source voltage V_{DS} and of the drain current I_{DS} during T_{ON}. As can be appreciated in Figure 4.18, the switching node of the half-bridge is easily accessible: at this node the measuring current I_{DS} is injected and V_{DS} is sensed, as described in the schematic of the set up in Figure 4.19a.



(a) Characterization set-up schematic



(b) Photograph of the characterization set-up (IT6516C and isolated probe are not visible)

Figure 4.19: Characterization set-up description

The measuring current I_{DS} is provided with a current source circuit already described in [21], made by two power Si P-MOS devices in cascode mode to maximize the generator output impedance. As described in [21], the current source is controlled with a ON/OFF command V_{CTRL-I}, while the current value I_{DS} is regulated by the value of the supply voltage V_{DD-I}. As observed before, it is

important to regulate amplitude and duration of the measuring current pulse in order to have a well-detectable V_{DS}, without inducing non-negligible self-heating to maintain isothermal conditions. The current value is measured by the Keysight high-bandwidth ($100MHz$) Hall-effect probe N2783A with 1% accuracy. As described in Figure 4.19a, there are two different paths for the sensing of V_{DS}. One path with high dynamic range acquires the entire V_{DS} waveform along the period: in this path, an isolated active differential probe with $40MHz$ bandwidth (Aaronia ADP1) is used to scale the V_{DS} waveform 100:1 to fit the oscilloscope voltage range. This channel is useful to monitor V_{block} during T_{block} and the synchronization with the measuring current, according to the measurement procedure described in Figure 4.14b and Figure 4.15, but this acquisition does not have enough sensitivity for a precise evaluation of V_{DS} during T_{ON} for the computation of R_{ON}. Thus, a second high-sensitivity and wide-band acquisition channel is implemented in a PCB visible in Figure 4.19b. In this channel, a low-offset and low-noise Analog Devices AD797 operational amplifier is used, in the x20 voltage gain configuration described in the inset of Figure 4.19a. This acquisition channel enables the accurate characterization of V_{DS} waveforms during T_{ON} that are used for the computation of R_{ON}. Similarly to what described in [21], with this configuration, the Op-Amp input is protected by means of two TVS diodes in anti-parallel configuration from high-voltage V_{block} during T_{block}. The presence of these didoes avoids the saturation of the oscilloscope acquisition channel and largely limits the saturation of the Op-Amp, so that few μs after the blocking event, the Op-Amp exits saturation and is capable to correctly measure V_{DS}. The high-resolution Tektronix MSO-56 scope is used for the time-domain acquisition of waveforms. The control of the power module and of the current generator according to the measurement procedure is provided by two synchronized arbitrary waveform generators (AWG): Agilent 81150A and Tektronix AFG320. The first AWG generates the PWM signals for the half-bridge switching module, while the second controls the current source.

4.2.4 Measurements

The measurement procedure described in Section 4.2.1 was adopted with the described setup. The duration T_{block} of the blocking voltage V_{block} was initially set to $1us$. The dead time T_D to $500ns$. The value of the blocking voltage V_{block} is varied between $10V$ to $400V$. The duration of the measuring window T_M is set to $40\mu s$. The amplitude of the current injected by the controlled current source is set to $0.45A$, guaranteeing isothermal tests, since the induced temperature increment due to self heating is estimated in $\Delta T = 0.22°C$. This is also confirmed by the flat I_{DS} shape during the entire measuring window T_M that can be appreciated in the acquired waveforms (Figure 4.20, Figure 4.21). The distance ΔT_M is varied from $20\mu s$ to $400\mu s$ that, according to the consideration in Section 4.2.1, corresponds to an equivalent switching frequency $f_S = 1/\Delta T_M$ ranging from $50kHz$ to $2.5kHz$. The acquired waveforms of the DUT V_{DS}, and I_{DS} for different blocking voltages are shown in Figure 4.20 for the acquisition at ΔT_M=$20\mu s$ and in Figure 4.21 for the acquisitions with ΔT_M=$400\mu s$, respectively.

It can be observed that T_{block} saturates the Op-Amp of the accurate acquisition channel of V_{DS}, but after less than $10\mu s$ the Op-Amp exits saturation and the measurement is available. The saturation of the Op-Amp and the presence of some

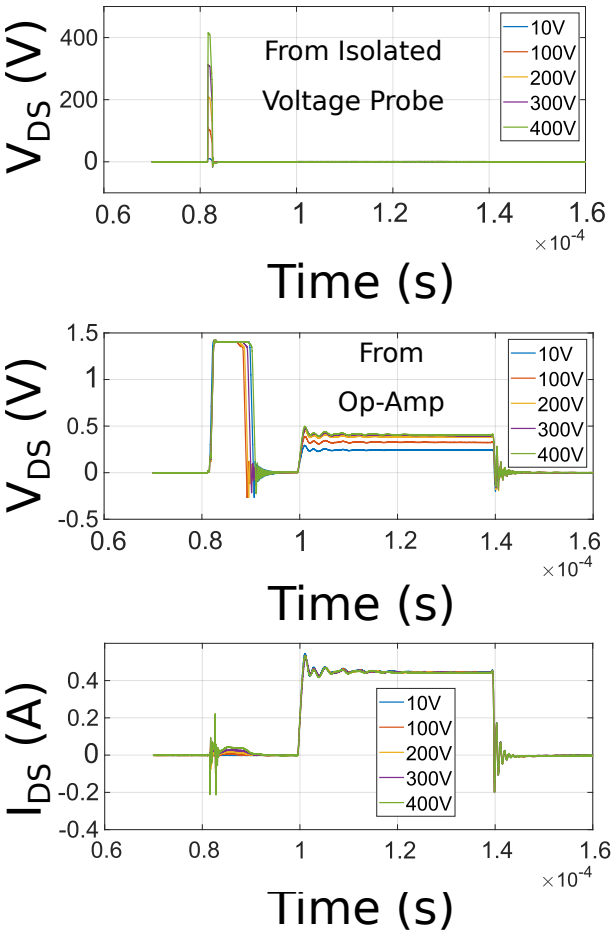


Figure 4.20: V_{DS} and I_{DS} DUT waveforms acquired by the scope for ΔT_M=20μs

residual ringing prevent to decrease ΔT_M to lower values and thus directly observe R_{ON} for higher equivalent switching frequency. To this aim, the minimum ΔT_M can be reduced by a different selection of the Op-Amp. Nonetheless, observing the flat shapes of V_{DS} and I_{DS} pulses during T_M, suggests that negligible recovery is observed up to $60\mu s$ (i.e. ΔT_M + T_M) from the V_{block} event. Therefore it is safely possible to conclude that trap recovery is very slow and R_{ON} degradation is the same for application frequencies from $50kHz$ upwards. This is an indirect, still reliable, indication that for this technology the observed R_{ON} at $50kHz$ is representative also for higher application frequencies.

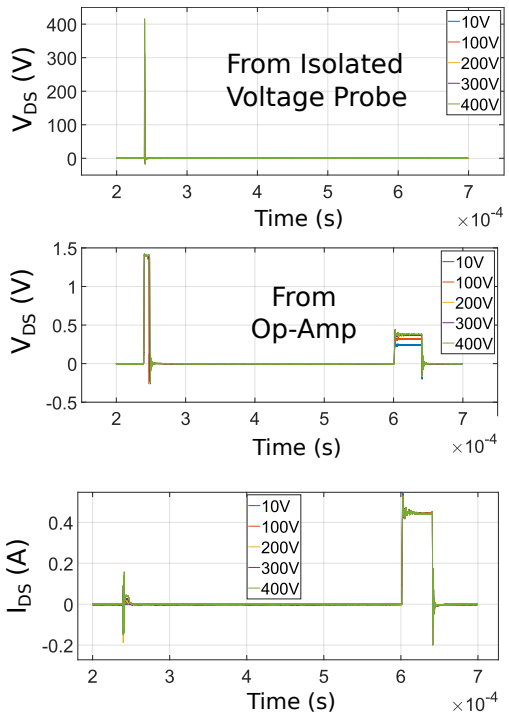


Figure 4.21: V_{DS} and I_{DS} DUT waveforms acquired by the scope for ΔT_M=400μs

From waveforms as the ones described in Figure 4.20 and Figure 4.21, R_{ON}=V_{DS}/I_{DS} is computed for different ΔT_M. The trends of the R_{ON} as a function of the blocking voltage evaluated at ΔT_M=20μs, ΔT_M=100μs and ΔT_M=400μs are plotted in Figure 4.22, where the normalization factor is the value at $V_{block} = 0V$ for all cases. The observed degradation of the dynamic R_{ON} is relevant.

It is useful to recall, (as suggested in Figure 4.22), that the corresponding application frequencies $f_S = 1/(\Delta T_M)$ are $50kHz$, $10kHz$ and $2.5kHz$. Thus, since the target switching frequencies for high voltage GaN technology are typically in the range $50kHz - 500kHz$, the trap recovery does not give any beneficial effect to dynamic R_{ON} in real application scenario. Therefore, the significant curve in Figure 4.22 is the one associated to ΔT_M=20$\mu s/f_S = 50kHz$ (green curve), and for the consideration made before about the practical absence of recovery in the window ΔT_M=$20 - 60\mu s$, this curve is the right reference also for higher switching frequencies. For this particular DUT, we can observe that the degradation of R_{ON} versus V_{block} appear to saturate after $300V$. The explanation of this behavior is not immediate and should be investigated with a physic-level insight that is outside the scope of this chapter.

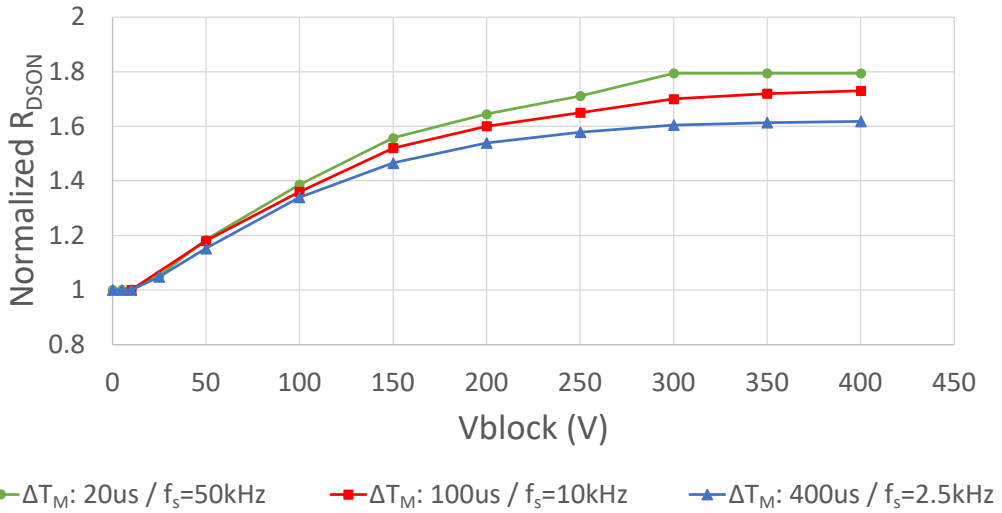
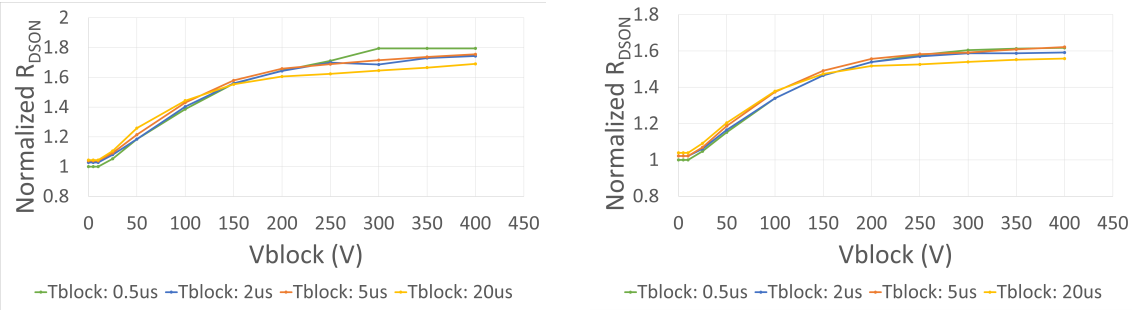


Figure 4.22: Normalized dynamic R_{ON} VS V_{block} evaluated at ΔT_M=20μs, ΔT_M=100μs and ΔT_M=400μs, with a T_{block}=500ns blocking voltage impulse

The observed R_{ON} degradation is significant, with a maximum increase up to 80% with respect to the static value. This is quite typical for new GaN technologies under development, as the one evaluated in this work, whereas more limited dynamic R_{ON} degradation can be observed for more mature commercial processes [33], [34], [35]. In this sense, the proposed technique an be a useful asset, not only for the assessment of the performance of GaN transistor under operating regime, but also for the evaluation of the technological advances of a process under development.

Finally, Figure 4.23 describes the sensitivity of the dynamic R_{ON} to the duration T_{block} of the blocking voltage V_{block}. As expected, the effect is very limited, and probably within the accuracy of the measurements. This corroborates the observation that the majority of charge capture mechanisms are very fast.



(a) R_{ON} at ΔT_M=20μs for different T_{block} (b) R_{ON} at ΔT_M=400μs for different T_{block}

Figure 4.23: Normalized R_{ON} VS V_{block} evaluated in two distinct time instants ΔT_M

All the measurements have been performed at 30°C DUT temperature (it is the temperature of the IMS, that corresponds to the DUT temperature since the measurement is isothermal with practically zero ΔT temperature increase). By varying the IMS temperature the same characterization can be made to determine the variation of the degradation of dynamic R_{ON} vs temperature. Unfortunately these data are not available due to the lack of a proper thermal controlled carrier capable to house the power module. When performing the same measurements

at increasing IMS/DUT temperature, we expect a slight improvement of RON performance, as observed in [21] for lower voltage technologies. Finally, it is interesting to note, that the proposed set up is also suitable to work in different regimes with respect to the one exploited for this characterization. Thus, other tests on the DUT dynamic R_{ON} can also be performed forcing other conditions as hard/soft-switching, inductive load, double pulse, high-impedance, resonant-mode.

4.3 Conclusions

A flexible set up for the characterization of the dynamic $R_{DS,ON}$ of on-wafer high-voltage power transistor has been implemented and used for the characterization of $600V$ GaN on Si power switches. The set up enables to characterize the degradation of $R_{DS,ON}$ varying driving voltage, blocking voltage, temperature and the duration/timing of the applied waveforms, enabling to explore the degradation of the device performance at different application regimes and also to acquire important information for the process' physical modeling and optimization. Due to the very limited power dissipation involved in the measurement, the proposed technique can accurately control the DUT temperature without the need of advanced thermal modeling and allows to apply high voltage excitations compatible with real application scenario directly on wafer. The capability to characterize the dynamic $R_{DS,ON}$ of GaN devices directly on wafer before the dicing and packaging of power transistor is very valuable and time saving. Therefore, the proposed set up and measurement technique can be valuable for foundries during the evolution of a new technology or for quality tests of production wafers.

To further investigate the dynamic R_{ON} of high-voltage GaN transistors during an operating regime of the DUT that resembles a real application scenario, a measurement technique and a dedicated switching power module have been developed and exploited for the characterization of bare-die $600V$ GaN switches of a process under development. As for the on wafer case, the acquisition method allows to neglect the self-heating phenomenon loosing consistency on the results. The measurements show a relevant degradation of R_{ON} that increases with the applied blocking voltage. This degradation fully applies to the entire range of switching frequencies of interests for this technology (i.e. $>50kHz$). Indeed, due to the observed long time constants associated to trap recovery mechanisms, a partial improvement of the dynamic R_{ON} is observed only for switching frequencies below $10 - 20kHz$, that are of very limited interest for this technology.

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Chapter 5

Conclusions

In the presented work, the design procedures and implementations of three different prototypes for automotive applications has been carried out exploiting WGB devices instead of Silicon technology, while two setups for the ON-resistance characterization of high-voltage experimental GaN HEMT transistors from early stage development have been proposed.

- In Chapter 2 two bidirectional $7.5kW$ AC/DC and DC/DC converters have been designed for charger applications, where the main requirement was the maximization of the overall efficiency. For this purpose the identification of the proper topology and technology become the decisive factor. Concerning the AD/DC converter, a PFC Bridgeless Totem-Pole topology was employed for the elimination of the inefficient diode rectification bridge and the combined possibility to work in CCM thanks to the reduced switching losses introduced by GaN power transistors with in the high-frequency leg. The simulations that take into account plant parasitics, control strategy and E_{ON}, E_{OFF} devices contributions have pointed out an overall efficiency of 98% with good input performances ($THD < 8\%$, $PF > 98\%$) and safe operating junction temperatures. On the other hand, for the DC/DC stage, the DAB topology has been chosen for its possibility to work in ZVS mode for a wide range of load conditions, the symmetric structure and the simpler control compared to resonant alternatives. With the exploitation of the same GaN transistor of BTTP high-frequency leg, the switching frequency is pushed to $200kHz$ with significant impact on magnetics manufacturing. The efficiency in the simulated nominal case goes above the 98% and the preliminary tests at reduced voltages provided efficiencies beyond 96%, in accordance with the predictions. All in all, the base cell made of these two converters should be able to supply $7.5kW$ to the load with an efficiency peak around 96%. This result can be considered quite promising if it is taken into account the fact that the prototypes are not optimized in terms of volume occupied favoring the testability process. Therefore, with a second revision of the system, a significant number of parasitics can be reduced, with a consequent gain of performances, possibly in combination with an additional step in the switching frequencies. In this way, an assessment on how the magnetics losses at faster periodic regimes limit the potentialities of GaN devices.

- In Chapter 3 the design and realization of a 350kW DC/DC converter for battery emulation tests has been described. The design procedure is the result of several contributions which encompass power electronics, control and software aspects in order to deal with the system complexity. Indeed, the system is made of the series of two stages, 1) a dual-secondary DAB converter for high-frequency galvanic isolation and power management, 2) a double Buck 3-way interleaved for output regulation. The converter includes 24 power modules and more the 60 digital/analog signals to handle. Given the strict requirements, the hardware section is simulated integrating the control algorithm by means of detailed co-simulation between PSIM and Simulink, providing crucial insights on the system behavior. Here the employment of SiC power modules has guaranteed fast commutation periods for the reduction of the isolation transformer sizes and significant losses decrement compared to IGBT traditional implementation. In this way it has been possible to save 1/3 of the space usually required for such test equipment using Silicon technology. The prototype has performed preliminary tests up to 80kW with results totally comparable with the simulations and efficiencies in the order of 96%. This has demonstrated the validity of the design procedure and bodes good results also for the subsequent full power tests.

- In Chapter 4 the critical issue of trapping charge in GaN HEMT transistors is introduced and pointed out as one of the most challenging defect to be mitigated in technological processes. On the system level, the degradation of the channel resistance during ON state caused by this mechanism can heavily affect the operative conditions of GaN devices and drastically reduce the reliability of the converter. Therefore it is important to characterize the R_{ON} during the development of the manufacturing process not only by typical static and small-signal tests but also in dynamic and large-signals conditions. Therefore two setups with two different measurement methodologies have been implemented. The first allows to vary the triggers conditions of trapping phenomenon as blocking voltage, gate voltage temperature and duration of applied signals in a on-wafer devices. In particular, the DUT is kept OFF for 1% of the period in which the trapped charge level is modulated by almost instantaneous high-voltage impulse, while for the remaining time the DUT is kept ON measuring V_{DS} and I_{DS} for the resistance calculus. The method application on the 600V experimental DUT has shown a strong deterioration of R_{ON} in function of blocking voltage, reaching up to 3.5x increment compared to normalized value, with a considerable deviation on measurement results of devices belonging to the same batch and long release time constants (calculate in seconds) indicating a still non-optimized process. The second method consists on testing the DUT in a real application scenario by means of a half-bridge module tailored on the DUT. Even in this case it is possible to set different values of blocking voltages, temperatures and switching frequency, nevertheless the method is slightly different from the on-wafer version. Here the period is kept fixed to a large value, while a narrow measurement window is moved back and forth the trigger event in order to vary the switching frequency. If the incremental factor of the R_{ON}

versus blocking voltage is below 2, so quite lower than on-wafer case, the presence of very long charge release process doesn't allow to employ the DUT on a real power electronic application. Both setups has provided the same results but highlighting different aspects of the DUT behavior. This feature gives important hints to the foundries in order to tune the process and increment the reliability of their products.

In conclusion, can be seen from the described activities how WBG materials have become pervasive in the power electronics applied to the automotive sector. The necessary reduction of converters form-factors without sacrificing, or even increasing, the delivering power forces to substitutes Silicon power mosfet and IGBT with SiC or GaN devices. SiC still represents the best choice for higher power levels for its longer heritage and higher thermal conductivity compared to GaN. However the latter has theoretically wider margins in terms of blocking voltage and electron mobility, which makes the optimization of the process more fruitful. Considering the development of new techniques of characterization in combination with a more similar process to Silicon than SiC, GaN technology is expected to steal market shares not only to silicon but also to silicon carbide for applications in the medium power range.