Alma Mater Studiorum - Università di Bologna

DOTTORATO DI RICERCA IN

INGEGNERIA ELETTRONICA, TELECOMUNICAZIONI E TECNOLOGIE DELL'INFORMAZIONE

Ciclo 35

Settore Concorsuale: 09/E3 - ELETTRONICA

Settore Scientifico Disciplinare: ING-INF/01 - ELETTRONICA

DESIGN AND CHARACTERIZATION OF WIDEBAND HALL CURRENT SENSORS IN BCD TECHNOLOGY FOR SMART POWER AND METERING APPLICATIONS

Presentata da: Sana Fatima Syeda

Coordinatore Dottorato
Prof. Aldo Romani

Supervisore
Prof. Marco Crescentini

Co-Supervisore
Prof. Aldo Romani

Esame finale anno 2023

"The most beautiful experience we can have is the mysterious. It is the fundamental emotion that stands at the cradle of true art and true science"
— Albert Einstein

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Acknowledgments

First and foremost, I owe my sincere and humble gratitude to my outstanding mentors and supervisors Prof. Marco Crescentini and Prof. Aldo Romani for their invaluable guidance and expertise throughout the program. Their adept knowledge, insightful remarks and constructive criticism enabled me to optimize solutions from diverse perspectives to obtain results. I also owe a heartfelt thanks to Prof. Marco Tartagni, for always instigating our weekly group meetings with much zeal, inviting fruitful discussions of curiosities, problems and solutions on a broader research horizon.

I would like to acknowledge STMicroelectronics for providing us the platform and access for the advanced silicon process technologies to carry out our research activities and design of the silicon chips. A special thanks to Giulio Ricotti for being a great inspiration on design discussion, Marco Marchesi for his extensive support for Hall device physics modelling and our Unibo - STMicroelectronics coordinator, Roberto Canegallo for his invaluable support during the fabrication and development phases of the silicon chips.

My gracious thanks to members of the sensor group for their valuable contributions, and all my dearest colleagues and friends for their unending support and encouragement during the research activity.

I would also like to acknowledge the joint support by the European Union's Horizon 2020 research and innovation program, under the Electronic Components and Systems for European Leadership (ECSEL) Joint Undertaking, and from Germany, Slovakia, Netherlands, Spain, and Italy under grant agreement No. 876868 (PROGRESSUS).

My reflection is incomplete without the indebted gratitude to my beloved family, from whom I receive unconditional love and support.

Abstract

Power electronic circuits are moving towards higher switching frequencies, exploiting the capabilities of novel devices, so as to shrink the dimension of the passive components. This trend demands sensors capable enough to operate at such high frequencies. This thesis aims to demonstrate through experimental characterization, the broadband capability of a fully integrated CMOS X-Hall current sensor in current mode, chip CH09, realized in CMOS technology for power electronics applications such as power converters. Current-mode operation alleviates the impact of stray capacitive loading at the probe-readout interface and enables the usage of a transimpedance amplifier (TIA) as readout circuit, offering better bandwidth, noise and power performance than conventional instrumentation amplifiers. The system exploits a common-mode control system to operate the sub-modules at dual supply voltages, respectively 5-V for the X-Hall probe to achieve high sensitivity, and 1.2-V for the readout to exploit the high transition frequency of transistors with reduced oxide thickness. A chip-on-board mounting limits the parasitic inductive effects on the host PCB. The developed prototype achieves a maximum acquisition bandwidth of 12 MHz. With a power consumption of 11.46 mW and a resolution of 39 mA_{rms}, it presents a sensitivity of 8 %T^{-1} and achieves a FoM of 569-MHz/A^2mW, which is significantly higher than current state-of-the-art hybrid Hall/coil solutions.

Further, enhancements were proposed to CH09 as a new chip CH100, aiming for accuracy levels that are a prerequisite for a real-time power electronic application. The internal analog read-out circuits were optimized for a wider bandwidth of 26.7 MHz with nearly 30% reduction of the integrated input referred noise of 26.69 nA_{rms} at the probe-Analog Front End (AFE)

interface in the frequency band of DC-30 MHz, and a 10% improvement in the dynamic range. Preliminary results show an upper bandwidth limit of the system as 26.87 MHz. The input range of the expected prototype is 5-A as it will be realized using a stud-bump instead of the chip on board. The chip incorporates a dual sensing chain for differential sensing as an option to overcome common mode interferences. A novel offset cancellation technique is proposed that would require switching of polarity of bias currents using a switched Hall bias circuitry. In contrast to the spun Hall sensors, it does not involve switching between the Hall probe contacts, hence the methodological limit is not imposed due to the switch parasitics, rather, the realized bandwidth would be a function of the frequency of switching the bias currents. Thermal gain drift was improved by a factor of 8 and will be calibrated digitally off the chip utilizing a new built-in temperature sensor module that can provide a post-calibration measurement accuracy greater than 1%. The estimated power consumption of the entire differential sensing system is 55.6 mW. Both prototypes have been implemented through a 90-nm microelectronic process from STMicroelectronics and occupy a silicon area of 2.4 mm^2.

Keywords: Current sensing, Magnetic sensors, Hall sensors, broadband sensing, X-Hall, current mode, residual-offset cancellation, Integrated sensors, Microelectronic circuits, BCD technology, Precise current sensors, Power electronic applications

Chapter 1

Introduction

1.1 Motivation and objectives

Power electronics is a challenging and exciting interdisciplinary domain that applies the knowledge of analog/digital electronics, control systems, electromagnetism, sensors, signal processing, etc, and deals with solid-state devices designed for various applications, for the control and conversion of electrical power. In other words, power electronic circuits form a power converter that can transduce energy from a supply to a load or an energy storage device in any of the combinations: AC-AC, AC-DC, DC-AC and DC-DC, with a possibility of systems combining the converters. Control electronics would be the heart of such an interconnected system and their algorithms could involve the sensing and measurement of voltages and currents that could act as input to trigger a specific control cycle to attain a stable operation, depending on the application. Moreover, they are usually based on high-frequency switching semiconductors that enable high-speed signal processing [1, 2]. When we focus on power electronics and their applications, and aim to address their requirements, we must understand that power electronic systems are usually modeled in two classes based on the objective of study: (i) evaluation of responses to the harmonics introduced by a power electronics sub-system, (ii) evaluation of a complex range of practical issues that arise due to the interdependence of two connected systems or subsystems. The latter is a crucial evaluation as it involves control loops and

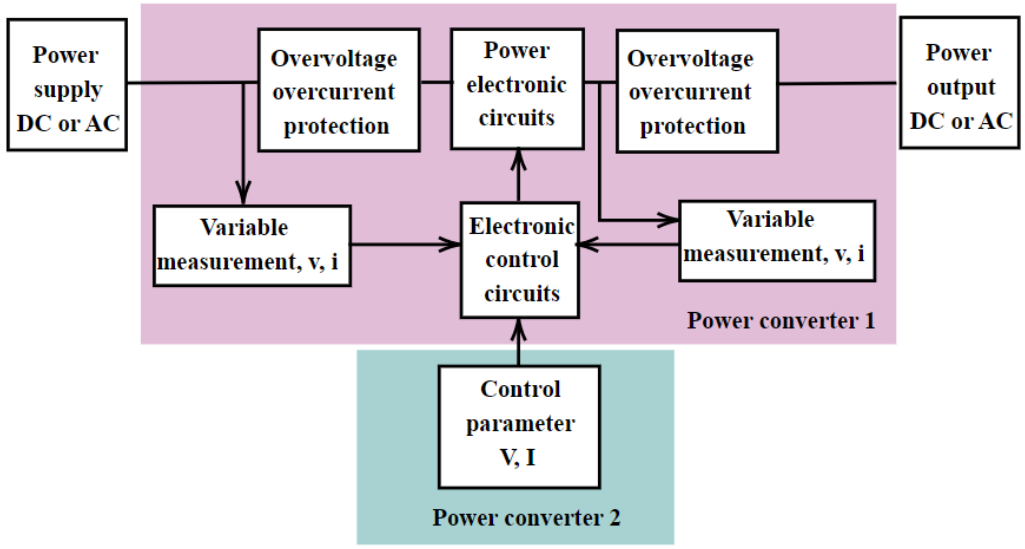


Figure 1.1: Block diagram of a power converter in an autonomous power electronic application

their accurate monitoring of dynamic variation of parameters such as voltage or current which can directly or indirectly affect the performance of the entire system [3]. A typical block scheme of an autonomous power converter is as shown in Fig.1.1. Detection of sharp transients or fluctuations of voltage/current or magnetic perturbations beyond the accepted threshold, due to the high-speed switch semiconductors can prevent damage to the converters and protect the power switches. This is where high-performance broadband current sensors come into play and their requirement is highlighted with utmost importance by a broad range of power electronic applications, from small scale systems used in electrical appliances to macro systems of energy supply and distribution. Some examples of such applications [4], include electric vehicles, DC-DC converters, photovoltaics, magnetometers, motor drives, and smart grids.

Fig.1.2 illustrates a wireless architecture for a smart grid lab [5] which is connects to various energy sources through Intelligent Power Switches (IPS) that can route power from one point to another. The power meter is an important device that is used to measure the current in the test line using a current sensor and in this case for experimental purpose, a Hall sensor by Al-

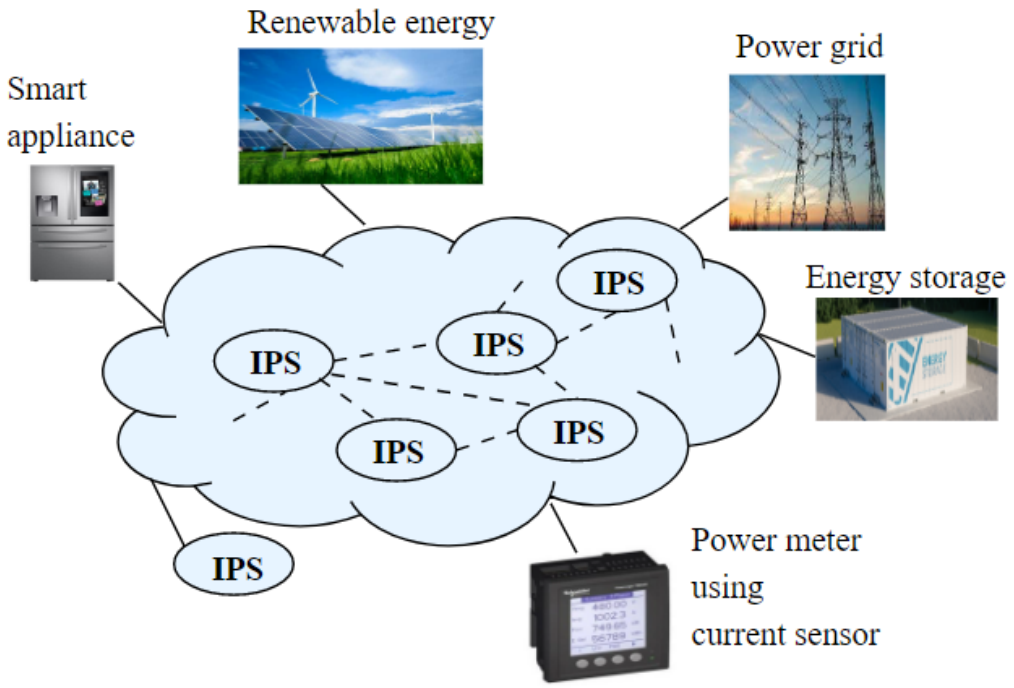


Figure 1.2: Architecture of a general wireless power network in a smart grid illustrating the use of current sensor for the computation of power

legro Microsystems, ACS714 was used. Modern hybrid/ electric vehicles use several integrated power electronic modules for compactness, reduced costs and reduced interconnects but this also causes the accessibility to internal information signals to become more difficult. To measure the current circulated between the motor and the motor-drive subsections, on-site current measurements within the power modules using highly sensitive Giant Magnetoresistance (GMR) current sensors were demonstrated in [6] while Fig.1.3 illustrates a general block diagram of an Electric Vehicle [7]. The sensors were also used for temperature sensing and thus, proved to be highly useful in protecting the functionalities of the semiconductor electronics within the power modules. A current sensor was also used for fault diagnosis algorithm proposed by [8]for brushless dc motors that find use in highly reliable electromobility systems. DC-DC converters especially high voltage converters, have an incessant need for load or inductor current monitoring in order to

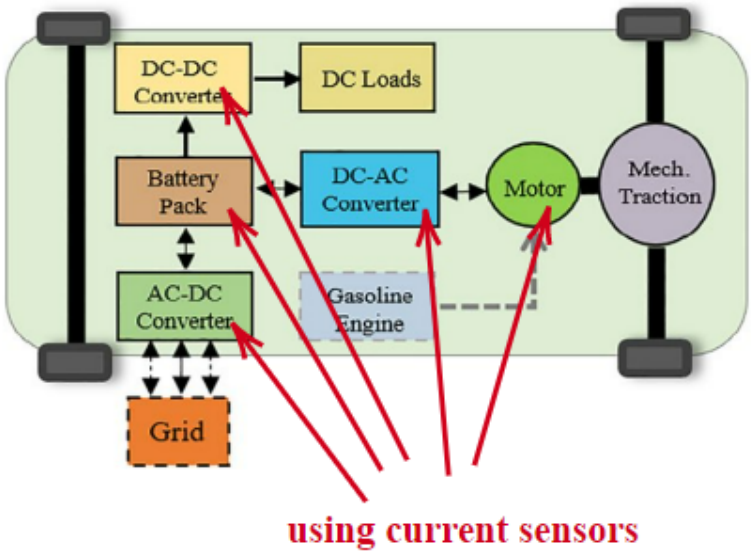


Figure 1.3: Block diagram of a generic Electric Vehicle

implement the in-built control loop compensation. Current sensing becomes a challenge due to the wide input common mode voltage range of the converter and stringent time specifications. There is a gaining interest to exploit fully integrated and low cost broadband sensing to achieve good regulation losses. High power shunts using sense resistors with low tolerance for current sensing are hard to integrate due to their size and additional components, and so a compact and economical sense-FET with a high immunity to board level parasitics that could degrade the system efficiency was implemented for a 40-V buck converter [9]. It achieved a gain bandwidth, GBW of 20.3 MHz but could only sense the current for a half cycle while the other half could only be partially sensed.

As the applications of power electronics call for an increased necessity of critical and accurate monitoring and control of their modules and interdependent submodules, there has been progress in research towards high-frequency and efficient contactless current sensing techniques to compensate the efficiency degradation and improve the switching frequency of converters [11]. Current being an indispensable parameter for their real-time control, traditional current sensing techniques can no longer serve the requirements of

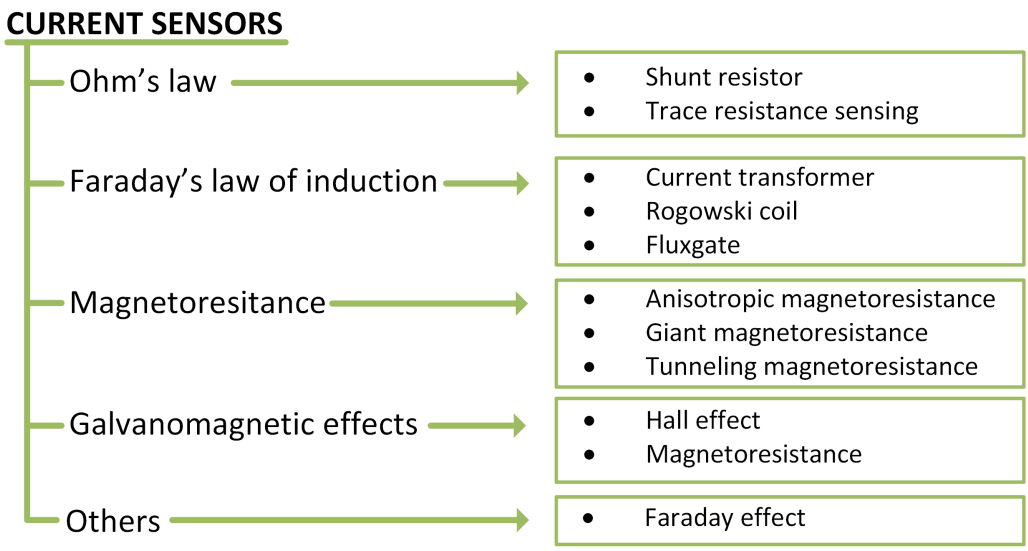


Figure 1.4: Figure from source [10]. Overview of current sensing techniques ordered by their operating principle.

modern power converters. Smart and unattended current and energy metering are basic to such applications as they enable the detection of failures, analysis of power consumption and reduction of energy losses. Broadband current acquisition is also integral to non-invasive load monitoring applications in which the appliances are recognized based on the actual consumed current waveform. Miniature and low-power sensors highly affect the development of smart grids in this aspect and must be characterized in themselves to perform power management and sustainable operation [12]. There are several applied techniques for current sensing, but to respond to the demand for fast switching power electronics, the challenge lies in seeking innovative current-sensing solutions that facilitate high signal bandwidths. So, an ideal approach would be the deployment of a non-invasive current sensor, compact in size, fully integrable, which fulfills the criteria of the broadband operation of power electronics, supports AC and DC sensing with perfect galvanic isolation, and low power consumption. Fig.1.4 illustrates one of the possible classifications for the various sensing techniques found in literature, based on the sensing principle [13].

In contrast to other sensing techniques, sensors based on Ohm's law are

usually invasive. They lack galvanic isolation but can accurately measure both AC and DC currents with limitations for the input range at the expense of the power dissipation. They are conventionally bulky and adding galvanic isolation using additional expensive electrical isolation amplifier limits its broadband capability [14,15]. Recent advances in research achieve a galvanic isolation by implementing a fully integrated semiconductor shunt sensor with an input range of ±1.25 A and 12.5 MHz bandwidth [16]. Zhong Tang et al., [17] demonstrated a shunt resistor implemented both as a PCB trace and a metal alloy with a microelectronic readout circuitry for battery management applications, but with a bandwidth limited to a few kHz. Galvanic isolation was achieved by bonding the die to the shunt trace with an insulative glue.

The Rogowski coil (RC) [18] and the Current Transformers (CT) [14, 19] are competent in terms of realizable bandwidth (up to GHz) [20], galvanic isolation, but the resulting sensor is bulky due to the coil wounded core, difficult to integrate, and loses the DC signal component. RCs can be realized using Printed circuit board (PCB) technology [21] with a precise geometry and improved thermal drift and although difficult, was fully integrated into a chip [22]. Fluxgate sensors exploit the magnetic hysteresis of ferromagnetic materials in order to sense very small magnetic fields. They can be used to realize highly accurate current sensors, yet they have limited Dynamic Range (DR) and bandwidth.

Magnetoresistive (MR) sensors or XMRs are based on the variation of resistivity due to the presence of an external magnetic field. They can be grouped by the underlying magnetoresistance effect: anistropic magnetoresitance (AMR), giant magnetoresistance (GMR), and tunneling magnetoresistance (TMR) [23]. AMR sensors exploit the magnetic anisotropic scattering of conduction electrons in ferromagnetic materials [24], while GMR and TMR are based on physical effects arising in multilayer devices with magnetic materials [13, 25]. MR sensors are very good candidates for modern power applications in the aspect of size, reliability and low power but they all require specific back-end processes in the semiconductor technology, leading to relatively high costs. some commercial sensors such as the TLE5501 and the TMR2301 could reach a few hundreds of kHz [26] [27] and the literature

state-of-the art demonstrates a bandwidth of 5 MHz [28].

Galvanomagnetic sensors rely on the Lorentz force acting on moving electrons to sense the magnetic field [29]. They can be grouped depending on the dominant galvanomagnetic effect: the geometrical magnetoresistive effect causes a change in the resistivity of the material along the main path of moving electrons, whereas the Hall effect generates a voltage drop orthogonal to the path of moving electrons. Compared to most sensors, Hall - Effect Current Sensors (HECS)s, which are the argument of this thesis, are highly compatible with standard silicon technology and can be either integrated with CMOS circuits or might leverage on alternative compounds to achieve better performance hence, allowing for a very compact solution for any application. Their conventional usage is found in a wide range of contactless industrial applications for proximity, magnetic field, speed and current sensing in the fields of automotives, electric motors, photovoltaics, smart grids, etc. To get an idea, angular position of a magnetic target can be determined using Hall-effect sensor to sense the magnetic field if it is placed at the centre of rotation of a magnetic field generated by a magnetic target. As the target rotates, it will be exposed to the field from different directions and responds monotonically to the components in a single axis over a range of $\pm 90^{\circ}$ of rotation. For full range measurement of 360°, two Hall probes are placed at 90° orientation with respect to each other as illustrated in Fig.1.5, for example, one for the x-axis and one for the y-axis followed by mathematical operation to determine the output. Exclusive mechanical systems risk wear and tear that limit their speed and performance and in some applications, it would be tedious to install ferrous targets or gears [30] to sense their speed or position, however the requirement is still called for, in numerous industries. Extraction of an electrical signal from the passing features of the gear teeth is a sought after challenge. A Hall-effect sensor can be utilized to detect the variation of magnetic flux between the airgap of a permanent magnet and the ferrous gearteeth and yield a usable electric signal. The magnet is used to magnetize the gearteeth, so as the teeth move across the surface of the magnet, the flux changes. MLX90217 geartooth sensor from Melexis [31] realized digitized output with a reset which is activated when the signal changes po-

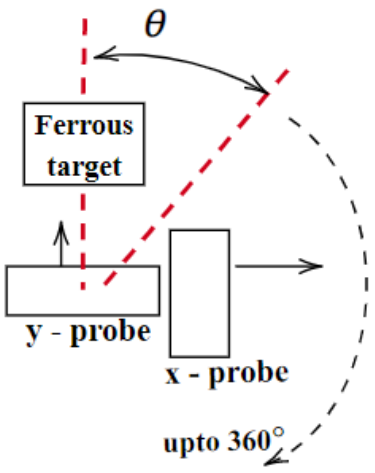


Figure 1.5: Angular sensing for full range of 360° using two Hall-effect probes positioned at 90° with respect to each other.

larity and changes the output level based on signal threshold, thus creating a zero speed peak detection speed sensor. The sensor bandwidth is 15 kHz and challenging time requirements such as for crank position sensing suffer accuracy issues at high speeds. The constraint for high-speed operation is even higher for Power electronic applications that require current sensing in a minimal time frame for peak and over-current detection of fast switching currents. Let us now overview the state of the art for Hall sensors and the challenges to overcome.

State of the art for Hall sensors

The HECS finds much of its appeal in the applications and market owing to its low cost, low heat dissipation, galvanic isolation, large DR, good linearity, and the ability to measure DC currents, make HECS well suited for modern power applications [15,32]. Practically, the device also comes with its own set of imperfections in terms of device geometry, doping concentration, and other fabrication issues, resulting in an undesirably high intrinsic offset of tens of mV that completely dominates the detected signal, which usually is in the order of a few μV. Additionally, low sensitivity, limited bandwidth which barely reaches the MHz range [33–35], sensitivity to external electric

fields, and temperature dispersion of the parameters also limit its performance. Nevertheless, all these limitations can be mitigated by exploiting exotic materials for devices, additional back-end processes, and smart circuit configurations and design [36–38]. To overcome these limitations, state-of-the-art broadband current sensing techniques have adopted hybrid solutions by combining RC or CT with compact Hall-effect current sensors [39, 40] for high speed switching and fully galvanically isolated current sensing. The input measurand current range is also wide without risking the coil saturation. This approach is however challenged by non-linearity issues mainly arising from the matching of different frequency responses. When following a hybrid approach, reduction of the non-linear deviation is of primary concern [41], while the bandwidth requirements are usually assured by the CT or RC. Multiple solutions were proposed to overcome the limitation of the offset which highly affects the accuracy of the sensor [10, 42]. The most used offset-reduction method is the Spinning Current Technique, (SCT) [43], which uses a single Hall plate but spins the bias current around it using all the contact pairs sequentially while sensing the Hall voltage at contacts perpendicular to the respective bias direction. The measurement is made at every $T_{spin} = 1/f_{spin}$ implying a rotation time of n-T_{spin} for an n-phase SCT. Summing all the measurements over a complete rotation leads to a reduction of the offset by almost a factor of 100 [10, 44]. A detailed discussion can be found in section 2.6.2 and the illustration in Fig.2.12(c). The downside of this, is that at higher spin frequencies, there is also a degradation of the offset. Besides this, the practical implementation of this technique increases the capacitive load seen by the Hall plate, which sets a significant limit to the bandwidth. This methodological bandwidth limit was overcome by the design of the X-Hall probe [45] by providing intrinsic static offset cancellation, hence eliminating the need for the SCT and speculating an improved practical limit of 200 MHz bandwidth achievable by the X-Hall probe itself, subject to the AFE's design. This would place the X-Hall sensor ahead of the state-of-the-art hybrid solutions. Practically, the X-Hall sensing system operated in voltage mode [46] achieved a 4-MHz bandwidth when implemented in 0.16 μm technology with a Differential-Difference Current Feedback Am-

plifier (DDCFA) as AFE. The limitations in bandwidth were mainly due to the amplifier itself and the parasitic inductive effects at package level. From a technological perspective, purely silicon-based HECSs also have lower sensitivity with respect to GMR and TMR sensors, with resolutions that are usually limited to a few hundreds μT [47, 48] in standard implementations, or a few μT when using magnetic concentrators [49, 50]. Based on a fresh study of 2022 by Allegro Microsystems, most industrial and automotive application requirements overlap and comparing the Hall sensors with the XMRs, the Hall sensors will continue to be the best solution for such applications unless the XMRs would find a balance between performance and costs [51]. A further improvement in sensitivity , offset (down to a few hundred nT) and a resolution of about 30 nT in the sub-Hz range in heterostructure-based Hall plates can be obtained by exploiting the 2D electron gas (2DEG) layer of quantum-well Hall sensors (QWHS) [52] that exhibit a high electron mobility and a very stable density. Higher bandgap GaN-based Hall-effect devices have also caught up on the trend in research due to their high resilience in extreme environments of upto 600 $^{\circ}C$ with a guaranteed sensitivity recovery, unlike silicon-based devices [38, 53, 54].

Well, moving apart from the hybrid solutions and other technological alternatives for Hall devices and focusing on just the purely semiconductor based Hall-effect sensor, it was mainly considered for low frequency applications, however, it has immense potential to become a valuable solution in broadband applications, by boosting its bandwidth limit in the MHz range [10, 55] and beyond [56]. Table 1.1 summarizes the features of the different state of the art current sensors and highlights the problem area and direction for necessary research in the field of Hall sensors. My PhD activity was primarily focussed on overcoming the challenges of the bandwidth limitation of the HECS and to push the performance metrics such as the noise, resolution and further working on the limitations of accuracy that relate to the offset and drift with respect to time and temperature beyond the state of the art, with the ultimate future goal of integrating the sensor with a real power electronic application such as the DC-DC converter to monitor LDMOS degradation [57]. A HECS can be generally treated as a three-stage

Sensor type	Bandwidth	Accuracy	DC measure	CMOS integration	Galvanic isolation	Heat dissipation	Compact	Cost
Shunt	High	Yes	Yes	Possible	Difficult	Yes	No	Low
CT	Very high	Yes	No	Difficult	Yes	No	No	low
Coil	Very high	Yes	No	Difficult	Yes	No	No	High
Fluxgate	Limited	Yes	Yes	Easy	Yes	No	No	High
XMR	Limited	Yes	Yes	Easy	Yes	No	Yes	High
Hall	limited	moderate	Yes	Easy	Yes	no	yes	Low

Table 1.1: Overview of features of State-of-the-art current sensors

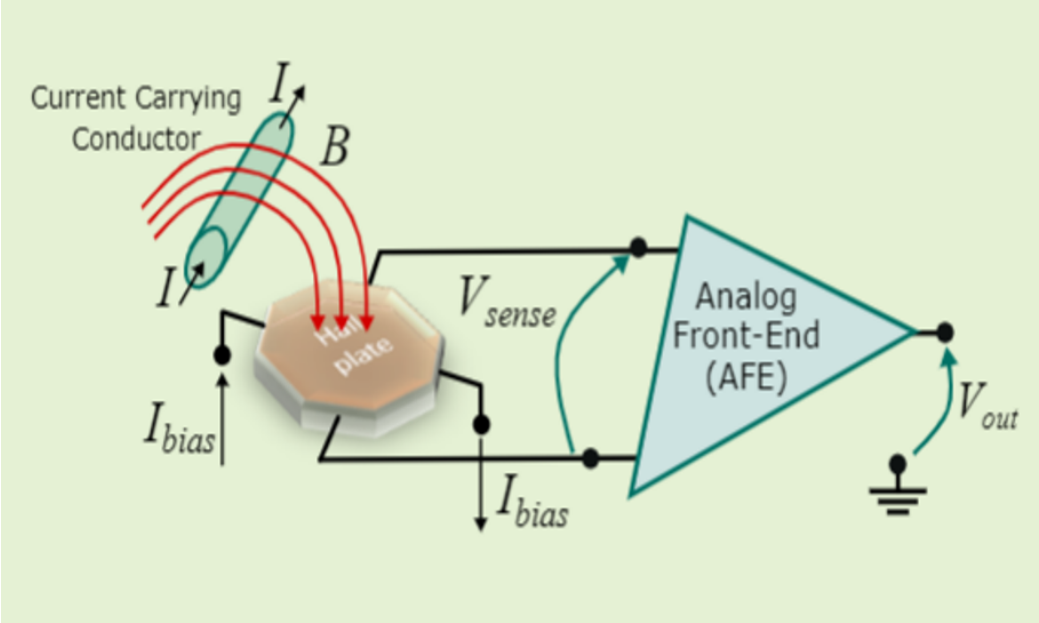


Figure 1.6: Hall - Effect Current Sensor system with (i Current to magnetic field transducer, (ii) Hall plate, and (iii) the Analog Front End

sensing chain as illustrated in Fig.1.1 consisting of: *i)* a current-to-magnetic field transducer; *ii)* the Hall probe itself (i.e., the magnetic sensitive device), and *iii)* the analog front-end (AFE). The analysis of each of these stages is critical for a proper design of the current sensor [1]. The design considerations

[1]Note: The reader must not confuse with 'sensor' as just the Hall plate. Throughout the thesis, when referring to a 'sensor', a 'Hall-sensor' or 'HECS' or 'sensor system' it is inclusive of the entire sensing chain, while when referring to a Hall element, the terms

took into account were minimum power consumption, system acquisition bandwidth, BW to be achieved beyond the state of the art as greater than 10 MHz. In an on-chip power system, the measurand current is usually in the mA to A range, so a soft input current limit for the Minimum Detectable Signal, (MDS) of 5 mA and a maximum of 5 A was aimed for. The sensor should also be insensitive to the magnetic field generated by other sections of the application circuit. This aspect however, is for future investigation.

Sensor Metrics

Before proceeding further, we must understand that when analyzing any sensor, it is important to define the main Figure of Merits, (FoM)s to be considered for performance evaluation [23, 30], the knowledge of which is essential to characterize and compare it with the other sensors in the state of the art. From a functional perspective, current sensors can be generally described by expressing the output voltage V_{out} as a function of the measurand current I [58] and the relation is formulated as:

$$V_{out} = SI + V_{os} + f_{nl}(I) + v_n; \tag{1.1}$$

where the following definitions are introduced:

- *Sensitivity*, indicated by S, is defined as the ratio between the increment in the output voltage over the increment in the measurand current. Sensitivity is a fundamental performance metric that expresses the ability of the device in sensing small variations of the measurand current and translate them into a large and robust voltage signal at the output. So, from a designer's perspective, high sensitivity is a bonus point as it would reduces the complexity and cost of electronics required to process the large output signal. In conjunction, the thermal drift of sensitivity, or let us say, the stability of sensitivity in extreme conditions is also a parameter that adds merit to the characterization of the sensor. It is much desirable for a sensor to have as low temperature

'Hall plate' or 'Hall probe' are used.

coefficient (TC) as possible.

- *Additive DC Offset*, indicated by V_{os}, is defined as the non-zero output voltage value at DC in the presence of a null measurand current. This quantity is intended as the result of different effects, including the electrical offset introduced by the electronic front-end, as well as the effect of the earth magnetic field. Similar to the case of sensitivity, the stability of the offset with thermal variations is important with a low TC. It is necessary to validate that the offset returns to the same value at nominal temperature after being subjected to extreme hot and cold temperatures. This allows one point compensation of the offset.

- *Non-Linearity*, indicated by $f_{nl}(I)$, is defined as the deviation from linearity for the relationship between the output voltage and the measurand current.

- *Noise*, indicated by v_n, is the output-referred noise density integrated over the acquisition bandwidth (in V). Alternatively, it can be expressed as an input-referred noise (in A) by v_n/S. The noise property is a random variation of the sensor output when the measurand quantity is zero. It is characterized by its Power Spectrum Density at a given frequency, PSD(f), and by integrating over a frequency range f_l, f_h, noise is expressed as a root mean square (rms) value. In this case, the frequency band for which it holds true must be specified.

- *Bandwidth*, defined as the frequency interval from DC to the 3-dB attenuation point of the transfer function of the sensor. Usually, increasing the bandwidth also means increased noise levels within the frequency range of interest.

- *Dynamic range*, defined as the ratio between the maximum measurable current and the minimum detectable signal (MDS). The MDS of course is determined by the output referred noise of the sensor itself.

1.2 Thesis structure

The thesis is organized as follows:

Chapter 2 aims to provide an exhaustive review on the necessary background on the Hall-effect sensors, study on the associated physical effects, their realization, functioning modes and the technicalities for integrating a Hall probe into a system. Further, a discussion is made on its evolution to the present state of the art, the limitations it has to overcome and a mention of modern day applications.

Chapter 3 initiates with the discussion of the base of the research target and the benchmark for the project, semiconductor chip KF94, with its achievements and limitations.

Chapter 4 proposes the current mode solution, chip CH09 for bandwidth enhancement, with a section explaining and validating the theory, a description of its architecture. This is followed by a discussion on the preliminary simulated results and the experimental characterization results carried out for the chip CH09 in our lab.

Chapter 5 proposes a new chip CH100 with its architecture and preliminary results with fine refinements and improvements for chip CH09 to cope with thermal gain drift. It further proposes a novel off-chip offset cancellation technique.

Chapter 6 covers general conclusions for this thesis and state of the art comparison.

Chapter 2

Background on Hall Sensors

2.1 Galvanomagnetic effects

The physics is always amazing and to brace ourself with the fundamental knowledge and understanding of the various effects that take place at the sub-atomic level, makes their exploitation to meet our purpose even more interesting. This section aims to summarize and provide the necessary analytical background of physical effects in a Hall-effect device. The galvanomagnetic effects refer to the charge mobilization that manifests in condensed matter carrying electrical current in the presence of magnetic field and is an integration of three different effects: the Hall-effect, magnetoresistance effect and the galvanothermomagnetic effects . The first two effects are characterized under isothermal conditions while the latter is a non-isothermal galvanomagnetic effect. Although, the Hall-effect device could be composed of any conductive material such as metal or semiconductor, for the sake of staying inclined to the scope of this project which is based on semiconductor based microelectronic technology, we would always consider a semiconductive material. The forthcoming analysis, will consider practical and ideal geometry of the semiconductor material, thereafter referred to as the Hall plate. The plate dimensions could either be long, with the plate length greater than the width, or on the contrary, it could be short. Such an analysis will give us clarity on the variation of the physical effects in the device.

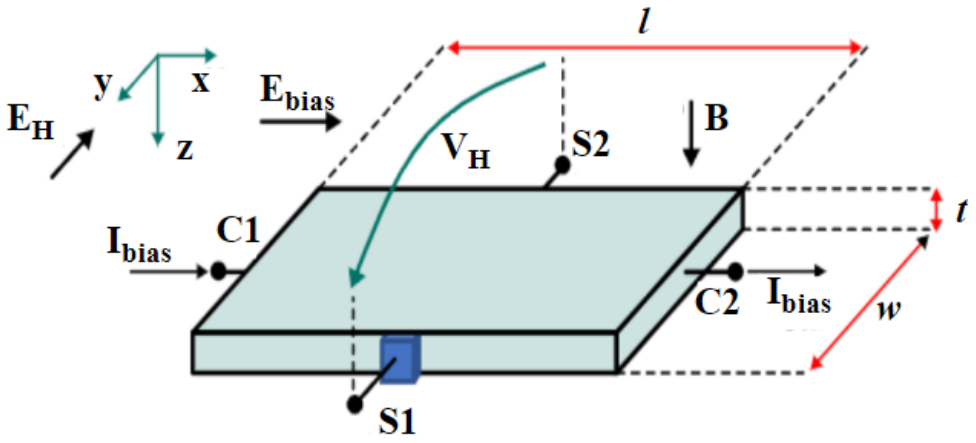


Figure 2.1: Rectangular semiconductor plate highlighting the generation of a transverse electric field when an out-of-plane magnetic field is applied.

Let us consider a strong extrinsic n-type rectangular semiconductor (refer Fig.2.1) with electron concentration n, thickness t, width w, and length l, in which a current I_{bias} is forced to flow through the contacts C1 and C2 due to an external electric field $\mathbf{E_{bias}}$. When an orthogonal magnetic field $\mathbf{B}$ is applied to the device, the Lorentz force acting on electrons is composed of the electrostatic and the magnetic components [10, 59, 60] respectively and can be described as:

$$\mathbf{F} = \mathbf{F_{bias}} + \mathbf{F_{mag}} \tag{2.1}$$

$$\mathbf{F} = -q\mathbf{E_{bias}} - q(\mathbf{v} \times \mathbf{B}); \tag{2.2}$$

Let us begin our analysis with a short device. From Fig.2.1, we get an idea that the device is compressed laterally between two bias current contacts.

Case I: Short Hall device (l $\ll$ w) and an initial condition $\mathbf{B} \approx 0$, hence $\mathbf{F_{bias}} \gg \mathbf{F_{mag}}$

To obtain the equivalent current densities in a short device ($l \ll w$), the total equivalent Lorentz electrical force in eq.(2.2) is given by $-q\mathbf{E}$ with $\mathbf{E}$ being the total equivalent electric field component and so eq.(2.2) can be re-written as:

$$-q\mathbf{E} = -q\mathbf{E_{bias}} - q(\mathbf{v} \times \mathbf{B}); \tag{2.3}$$

where $q = 1.6 \times 10^{-19}$ C is the electron charge and $\mathbf{v}$ the local velocity of the carriers due to the thermal agitation which is influenced by the drift velocity, $\mathbf{v_{dn}} = \mu_n.\mathbf{E_{bias}}$, μ_n being the drift mobility of the electrons. Since we follow the condition, $\mathbf{F_{bias}} \gg \mathbf{F_{mag}}$, most of the electric field is contributed to $\mathbf{E_{bias}}$. Multiplying the eq.(2.3) with $-\mu_\mathbf{n}\mathbf{n}$ we can arrive to the corresponding current density equation as a function of applied magnetic field:

$$-\mu_n nq\mathbf{E} = -\mu_n nq\mathbf{E_{bias}} - \mu_n^2 nq(\mathbf{E_{bias}} \times \mathbf{B}) \tag{2.4}$$

From equation 2.4, we arrive at the definition of the corresponding total equivalent current density:

$$\mathbf{J_n}(\mathbf{B}) = \mu_n nq\mathbf{E}, \tag{2.5}$$

where the current density in the absence of magnetic field

$$\mathbf{J_n}(\mathbf{0}) = \mu_n nq\mathbf{E_{bias}} \tag{2.6}$$

and the contribution to overall current density due to the magnetic field is perpendicular to the current density component at $\mathbf{B} = 0$

$$\mathbf{J_{mag}} = \mu_n(\mathbf{J_n}(\mathbf{0}) \times \mathbf{B}) \tag{2.7}$$

Hence, the equivalent current density in the device from Eq.2.4,

$$\mathbf{J_n}(\mathbf{B}) = \mathbf{J_n}(\mathbf{0}) - \mu_n(\mathbf{J_n}(\mathbf{0}) \times \mathbf{B}) \tag{2.8}$$

Case II: Short Hall device (l $\ll$ w) and $\mathbf{B} \not\approx 0$, hence $\mathbf{F_{mag}} \gg \mathbf{F_{bias}}$

In this case, most of the bias electric field is masked by the magnetic field and so Eq2.4 is transformed accordingly as:

$$-\mu_n nq\mathbf{E} = -\mu_n nq\mathbf{E_{bias}} - \mu_n\mu_n nq(\mathbf{E} \times \mathbf{B}); \tag{2.9}$$

This implies an equivalent current density

$$\mathbf{J_n}(\mathbf{B}) = \mathbf{J_n}(\mathbf{0}) - \mu_n(\mathbf{J_n}(\mathbf{B}) \times \mathbf{B}) \tag{2.10}$$

The current density when applied magnetic field, $\mathbf{B} = \mathbf{0}$ is aligned to $\mathbf{E_{bias}}$ but the equivalent current density, $\mathbf{J_n}(\mathbf{B})$ is not collinear with $\mathbf{E_{bias}}$ and deflects at an angle, also referred to as the Hall angle, θ_H [59] as can be observed in Fig.2.2(a). This is true for equations 2.8 and 2.10

$$\tan\theta_H = \mu_n \mathbf{B_z}. \tag{2.11}$$

This results in a transversal current in the device with the magnetic electromotive force being shorted, thus nulling the Hall voltage. This is also known as the current deflection effect.

Case III: Long Hall device ($l \gg w$) such that $t \sim 0$ and $\mathbf{B} \not\approx 0$

Then most of the electric field in Eq. 2.3 along the longitudinal axis of the device is primarily due to the external bias $\mathbf{E_{bias}}$. So, the associated current density

$$\mathbf{J_n} = q.\mu_n \mathbf{E_{bias}} \tag{2.12}$$

Writing the magnetic part of the Lorentz force without considering the thermal agitation, from eq(2.3) we obtain:

$$\mathbf{F_{mag}} = -q.\mu_n[\mathbf{E_{bias}} \times \mathbf{B}] \tag{2.13}$$

This magnetic part pushes the electrons toward one edge of the device along the y-direction, creating a space charge density gap across the edges in the device which creates an electric field $\mathbf{E_H}$ along y as shown in Fig.2.1. This electric field acts on the charges with a force

$$\mathbf{F_H} = -q.\mathbf{E_H} \tag{2.14}$$

that, at a steady state, counterbalances the magnetic action of the Lorentz

force. Hence, equating the equations 2.13 and 2.14, $\mathbf{E_H}$ can be expressed as

$$\mathbf{E_H} \approx \mu_n(\mathbf{E_{bias}} \times \mathbf{B}) \tag{2.15}$$

This generation of a transverse electric field under the influence of Lorentz force across a current carrying conductor due to an applied magnetic field normal to the conductor's surface is called the Hall-electric field. The total electric field in the device is given by

$$\mathbf{E_{tot}} = \mathbf{E_{bias}} + \mathbf{E_H} \tag{2.16}$$

which is not aligned with the applied $\mathbf{E_{bias}}$ and therefore is not aligned to the current density along the device from equation2.12 and this results in a deflection between $\mathbf{E_{tot}}$ and $\mathbf{J_n}$ as illustrated in Fig.2.2(b) referred to as the Hall angle,

$$\tan\theta_H = \frac{|\mathbf{E_H}|}{|\mathbf{E_{bias}}|} = \mu_n \mathbf{B_z} \tag{2.17}$$

The Hall angle is a fundamental metric for the Hall effect devices, as it clearly expresses the perceptibility of the Hall effect with respect to the electrostatic bias. It is also identical for long and short Hall devices as derived from Eq.(2.11) and (2.17). It also clarifies that the mobility of the charge carriers,μ_n is a key parameter in the selection of a Hall device as it takes into care thermal agitation, scattering effects due to thermal agitation, and velocity distribution as will also be explained shortly. Now, if we include the contribution of the effect of thermal agitation of the carriers,

$$\mathbf{E_H} \approx \mu_{H_n}(\mathbf{E_{bias}} \times \mathbf{B}) \tag{2.18}$$

In this equation, μ_{H_n} represents the Hall mobility of the carriers, which is a product of the drift mobility and the Hall scattering factor, r_H that differs by less than 20% from unity and considers the influence of the thermal motion

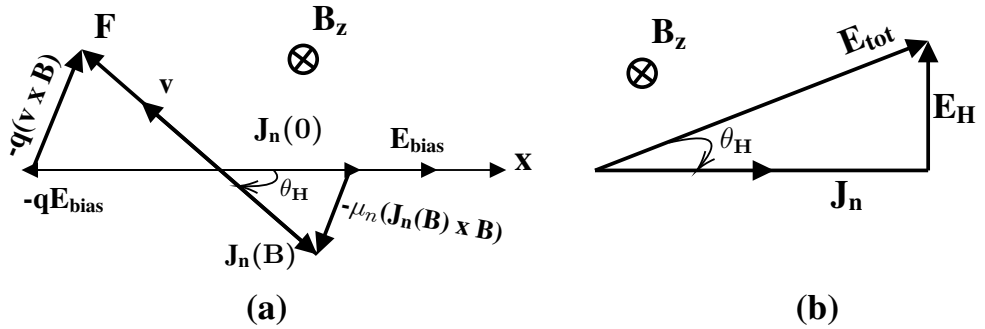


Figure 2.2: Vector diagram illustrating the Hall angle, θ_H for an n-type semiconductor device (a) a short device: The Hall effect shows up through the tilting of the current density $\mathbf{J_n(B)}$ with respect to $\mathbf{E_{bias}}$, (b) long device: the Hall effect develops through the tilting of the total electric field, $\mathbf{E_{tot}}$ relative to $\mathbf{E_{bias}}$ and the current density, $\mathbf{J_n}$, which in this case, are collinear in the sample.

of carriers and their scattering on the Hall-effect,

$$\mu_H = \mu_n . r_H \tag{2.19}$$

Thus, from equations 2.15 and 2.18, the Hall electric field is proportional to the external electric and magnetic fields with a proportionality constant of carrier mobility. So, in order to have a high mobility characteristic for a Hall device, we would usually prefer n-type semiconductor than a p-type.

Further, by accounting for (2.15), the Hall effect in a device ultimately results in a transverse Hall voltage between contacts S1 and S2:

$$V_H = \int_{S_1}^{S_2} \mathbf{E_H}\, dy = \frac{\mu_n}{\sigma t} I_{bias} B_z = \frac{1}{nqt} I_{bias} B_z. \tag{2.20}$$

with $\sigma = nq\mu_n$ being the electrical conductivity which also contains information on the geometrical magnetoresistance effect, as will be discussed shortly. From equation 2.20, we can clearly understand that V_H is directly proportional to the vertical magnetic field and the applied bias, and inversely proportional to the geometrical/physical parameters of the device. So, in order to increase the output Hall voltage, the device must feature low carrier concentration and be as thin as possible. This is the reason, Hall-effect devices are usually referred to as Hall plates. Including the thermal agitation of the

carriers and include Hall mobility as in equation 2.19 in Equation 2.20, we obtain another expression for V_H introducing the Hall coefficient, $R_H = r_H/nq$ as:

$$V_H = \frac{r_H}{nqt} I_{bias} B_z = R_H \frac{I_{bias}}{t} B_z, \tag{2.21}$$

With the definition of the transversal Hall voltage, we conclude with the primary contributor of the galvanomagnetic effects.

Let us now forego our earlier assumptions of orientations of an applied orthogonal magnetic field, **B** and the external field, $\mathbf{E_{bais}}$ and try to interpret the current density components. If we observe in Fig.2.2(a), for short Hall plates, the current deflection due to the magnetic field, causes an attenuation of the current density such that $J_n(0) > J_n(B)$. Similarly, for a long device, the current deflection effect creates a longer path for the current density lines and adds a greater effective longitudinal resistance and therefore attenuates them in the presence of magnetic field. This is known as the magnetoresistance effect. It can be shown that, $J_n(B)$ is a function of the effective conductivity of the semiconductor, σ_B and to determine the factor by it is attenuated, we solve the eq.2.10 with respect to $J_n(B)$:

$$J_n(B) = \frac{J_n(0) - [J_n(0) \times B] - B[J_n(0) \cdot B]}{1 + (\mu_n B)^2} \tag{2.22}$$

For a perpendicular magnetic field, $[J_n(0).B] = 0$, hence

$$J_n(B) = \frac{J_n(0) - [J_n(0) \times B]}{1 + (\mu_n B)^2} \tag{2.23}$$

$$J_n(B) = \frac{n\mu_n q E_{bias} - n\mu_n^2 q[E_{bias} \times B]}{1 + (\mu_n B)^2} \tag{2.24}$$

The conductivity of the n-type semiconductor is given by

$$\sigma = n\mu_n q \tag{2.25}$$

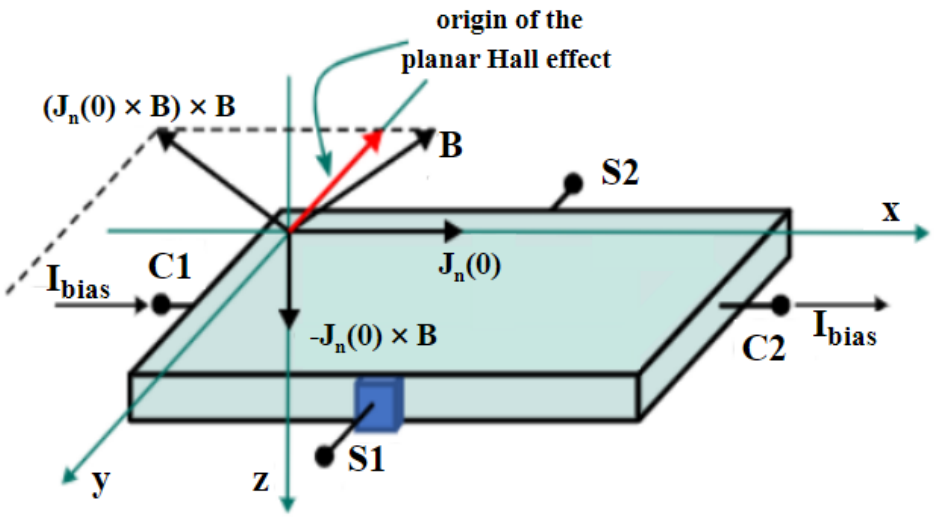


Figure 2.3: Graphical representation of the planar Hall effect

and effective conductivity, σ_B

$$\sigma_B = \frac{\sigma}{1 + (\mu_n B)^2} \tag{2.26}$$

Hence, eq2.24 can be expressed to define the magnetoresistance effect:

$$J_n(B) = \sigma_B E_{bias} - \sigma_B \mu_n [E_{bias} \times B] \tag{2.27}$$

Another effect characteristic of Hall devices is that they are sensitive to not only the magnetic field incident perpendicular to their surface, but also to a field aligned to the plane of the Hall plate. This is referred to as the Planar effect [61] and corresponds to a deflection of current (and related generation of induced electric field) collinear with the magnetic field **B**. This effect can be easily observed in Fig. 2.3 by assuming that the magnetic field is in-plane with the bias current (i.e., on the x-y plane). In this case, due to the Lorentz force, the bias current generates a component of $\mathbf{J_n}$ in the z-direction that, in turn, causes the generation of another deflection current by magnetic action in the x-y plane, decomposed into J_x and J_y. This last term will produce a Hall voltage that is transverse to the bias current, but

in-plane with the magnetic field contributing an error in the sensed voltage. If we invalidate the hypothesis of negligible device thickness, all the three-dimensional components of the magnetic field **B** should be taken into account in the solution of Eq.(2.4). In this case, it can be demonstrated that the current density in the device can be written as [59]:

$$\mathbf{J_n}(\mathbf{B}) = \sigma_B \mathbf{E_{bias}} - \mu_H \sigma_B (\mathbf{E_{bias}} \times \mathbf{B}) + Q_H (\mathbf{E} \cdot \mathbf{B})\mathbf{B} \tag{2.28}$$

where the third term is referred to as the planar Hall effect, and Q_H is the planar Hall-current coefficient.

This effect is usually negligible in Hall plates, which are the devices exploiting the Hall effect to realize a magnetic sensor and it has been shown that specific crystal orientations and the geometry of vertical Hall devices would counteract to an extent of an order of magnitude, the influence of such planar Hall voltage compared to the plate-shaped devices.

Finally, galvanothermomagnetic effects are characterized non-isothermally and include the Ettingshausen effect, which is the appearance of a transverse temperature gradient in a sample as a consequence of a Hall effect taking place in the sample; the Nernst effect, which is the generation of a voltage in a Hall device with the heat flow replacing the current; and the Righi–Leduc effect, which is a thermal analogue of the Hall effect. An in-depth analysis of these effects is not within the scope of this thesis, nevertheless, a rigorous and detailed description can be found in [59]. Now that we have an understanding of the physical effects that take place within the device, let us enquire into the composition of the device, the possible materials for construction and their role in device performance. The following sections will furnish the reader with information regarding the conventional technologies used to realize Hall devices with considerations to their possible geometries.

2.2 Materials

The choice of device material plays a significant role in originating the Hall effect [10, 59, 60, 62, 63]. As also pointed out earlier, the equation (2.20)

Table 2.1: Characteristics (at 300 K) of semiconductors used for Hall-effect sensors.

Material	μ ($\mathrm{cm^{-2}V^{-1}s^{-1}}$)	n ($\mathrm{cm^{-3}}$)	R_H ($\mathrm{cm^{-3}C^{-1}}$)
doped Si	1500	2.5×10^{15}	2.5×10^{3}
InSb	80000	9×10^{16}	70
InAs	33000	5×10^{16}	125
GaAs	8500	1.45×10^{15}	2.1×10^{3}

clearly shows that the Hall voltage is directly proportional to the carrier mobility, and that it is inversely proportional to conductivity and carrier concentration.

Metals are characterized by carrier concentrations (e.g., $n = 8.4{\times}10^{22}\mathrm{cm^{-3}}$ for copper), which are orders of magnitude higher than those present in intrinsic semiconductor materials (e.g., $n \approx 1 \times 10^{10}\mathrm{cm^{-3}}$ for intrinsic silicon), thus resulting in a very low Hall voltage.

Suitable candidates for HECS devices are, instead, semiconductor materials like silicon (preferebly the n-type) and III-V compounds (e.g., InSb, GaAs, InAs) with high mobility and relatively low conductivity. Apart from having a choice of the dominant charge carriers, using doped semiconductor materials is beneficial primarily because in pure semiconductors, the carrier concentration is highly influenced by temperature, while doping changes this property and instead makes it a function of dopant concentration which is fixed and usually constant over temperature. Table 2.1 reports the mobility, the average carrier concentration, and the Hall coefficient of semiconductors typically used for HECS devices. Nevertheless, it should be noted that low energy bandgap materials usually show high mobility but also high carrier concentration, leading to a trade-off. Moreover, when choosing the device material, the designer must consider compatibility with the available semiconductor technologies in terms of integrability, economic feasibility, and reliability.

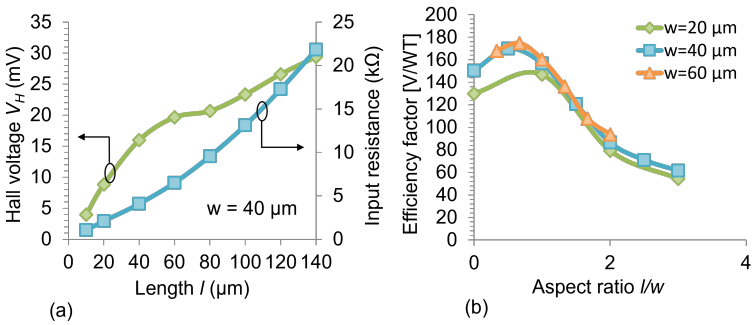


Figure 2.4: (a) Variation of Hall voltage and input resistance with device length for a 40 μm wide Hall plate biased at 500 μA under 50 mT of out-of-plane field (b) Device efficiency as a function of its aspect ratio.

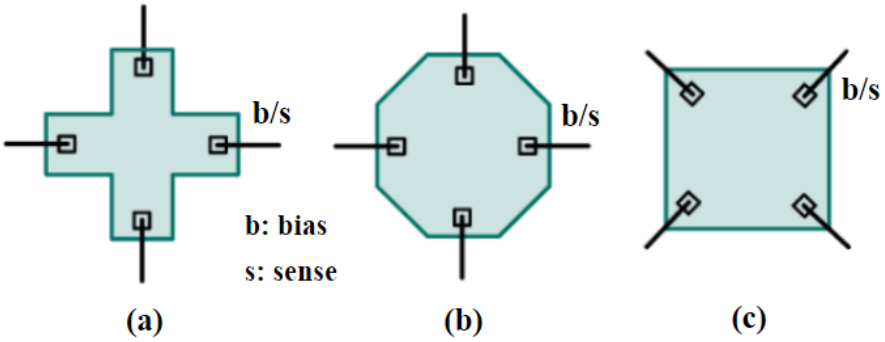


Figure 2.5: Different geometries of the active area (i.e., n-type well) for Hall plates: a) cross b) octagonal c) square with contacts on the angles

2.3 Hall plate technology

The Hall probe is a four-terminal solid-state device that relies on the Hall effect discussed in Sec. 2.1. Equation (2.21) was obtained for an ideal device characterized by $l \gg w$, negligible contacts, and unconstrained by any specific technology process. However, the technological aspects are important when dealing with the implementation of the sensing device [64]. In this Section, the analysis will focus on CMOS technology, but similar considerations can be applied to other semiconductors.

A real Hall-effect device cannot be assumed infinitely long, and at least four contacts are needed to realize a Hall plate. Two contacts are necessary for the flow of electrical energy, also called bias contacts, and two sense

contacts positioned orthogonally and at equipotential points at the plate boundary. Their sizing is crucial for the Hall plate and affects the basic plate structure, for if they are too large, the sense contacts may create local short circuits with the bias current, thus reducing the Hall voltage, and on the contrary if they are too small, then the material resistance surrounding the contact contributes a high resistance relative to the device as a whole [23]. Their doping concentrations also play a role, as highly doped sense contacts create space charge regions that lower the measurable Hall voltage [65]. The effects of the implemented shape are taken into account by defining the Hall geometrical factor [59],

$$G_H = \frac{V_H}{V_H^{\infty}} \tag{2.29}$$

as the ratio between the actual Hall voltage (V_H) and that generated by an infinitely long Hall device (V_H^{∞}). Therefore, the Hall voltage of a generic Hall plate can be expressed as

$$V_H = \frac{G_H R_H}{t} I_{bias} B_z. \tag{2.30}$$

The exact value of G_H depends on the shape of the device, on the sizing and position of the contacts, and also on the Hall angle, θ_H as also discussed in [59]. The G_H factor of a specific device shape can be analyzed by using different techniques, e.g., conformal mapping [59], boundary element methods, or finite element methods (FEMs) [64,66]. Some general design rules are summarized in [64]. Following the definition of G_H, the longer the device, the higher the Hall voltage, up to the theoretical limit (see Fig. 2.4a). However, increasing the length of the device also increases the input resistance (also observed in Fig. 2.4a). In this case, a higher bias voltage is required to force the same I_{bias}, causing an overall raise in power consumption. This trade-off is well represented by the efficiency factor η (also known as power-related sensitivity):

$$\eta = \frac{V_H}{V_{bias} I_{bias} B}, \tag{2.31}$$

which shows a local maximum for an aspect ratio $l/w \simeq 1$ (see Fig. 2.4b). Therefore, highly symmetrical shapes are preferred from an energy perspective. Moreover, symmetric devices are easier to fabricate, and symmetry can be also exploited to improve the final performance of the sensor.

In this context, FEM analyses revealed that, for a generic square shape, the G_H factor can be maximized by using large bias contacts (as large as half the width of the device) and small sense contacts placed at half the length of the device [58]. However, this compromises the perfect symmetry of the plate, and small sense contacts are more susceptible to misalignment errors, giving rise to an additive offset voltage. Figure 2.5 reports on the Hall plate geometrical aspects and their optimization, while an in-depth analysis can be found in [67–72]. The cross shape was demonstrated to achieve high values of G_H even employing large sense contacts, while the square shape displayed higher sensitivity values.

Regardless of the chosen shape, the Hall plate is meant to be a bidimensional device with negligible thickness. In standard CMOS implementations, the Hall probe is usually realized by a low-doped n-type well because of the higher mobility with respect to p-type wells. The thickness is defined by the diffusion depth set by the CMOS process, and cannot be changed by the designer [37]. The n-type active well is encapsulated in a p-type layer, which could be the epitaxial substrate or an isolation layer. In any case, the encapsulation in the p-type well originates a pn junction with its corresponding depletion layer, which lowers the effective thickness of the Hall probe and makes it non-constant along the Hall plate [58, 72, 73]. Moreover, it causes spurious dependencies on the bias and the magnetic field by means of the magnetoresistive effect and the junction field effect, leading to nonlinearity [74, 75]. The p-type layer can be reverse-biased to enlarge the depletion layer, reduce the effective thickness, and increase the sensitivity. However, the achievable improvement is negligible with respect to the increased complexity of the electronics. Alternatively, the effective thickness can be reduced by placing a shallow trench isolation on top of the active layer, or can be modulated by covering the n-well with a thin p-type implantation layer (which creates another depletion region) or a poly gate inducing

a field effect [72, 73]. In all the cases, an equivalent capacitance can be associated to the depletion region, setting a fundamental bandwidth limit for the HECS [36, 76, 77]. Taking our attention to interfacing a Hall device, the bias contacts must be connected to a current source with high output impedance and the sense contacts connected to a high input impedance AFE for sensing the Hall voltage without sinking current, although alternative configurations can be developed [78–80]. This constraint is applicable when the Hall plate is configured in voltage mode, however, when its dual is implemented as current mode, the criteria of the impedance of the AFE changes to low impedance as will be discussed in the next sections and also is the subject of this project.

2.4 Operating modes

The output signal of a Hall-effect device can be generated in one of the two complementary configurations: The voltage mode or the current mode. The earlier discussions related to the general concepts of the Hall effect where in the output signal was a Hall voltage is the most conventional configuration of the Hall sensor. When the output signal is its dual, i.e, a Hall current obtained by shorting of the sense contacts such that the Hall voltage is forced to be zero, the Hall sensor is said to be configured in the current mode. The two configurations are illustrated for a square shaped Hall plate biased with a current, I_{bias} in the presence of a magnetic field, B_z in Fig.2.6. Their respective output signals are a sum of the Hall signal: Hall voltage, V_H or a Hall current, I_H and the plate offset, $V_{OS,plate}$ and are given as follows [1]:

$$V_{probe} = V_H + V_{os,plate} \tag{2.32}$$

$$I_{probe} = I_H + I_{os,plate} \tag{2.33}$$

It is to be noted that the current related sensitivities of the two configurations are different and incomparable. The sensitivity of a sensor biased with voltage in voltage mode and a sensor biased with current in current mode

[1] **Note:** V_{probe} and I_{probe} are interchangeably used with V_{sense} and I_{sense} respectively

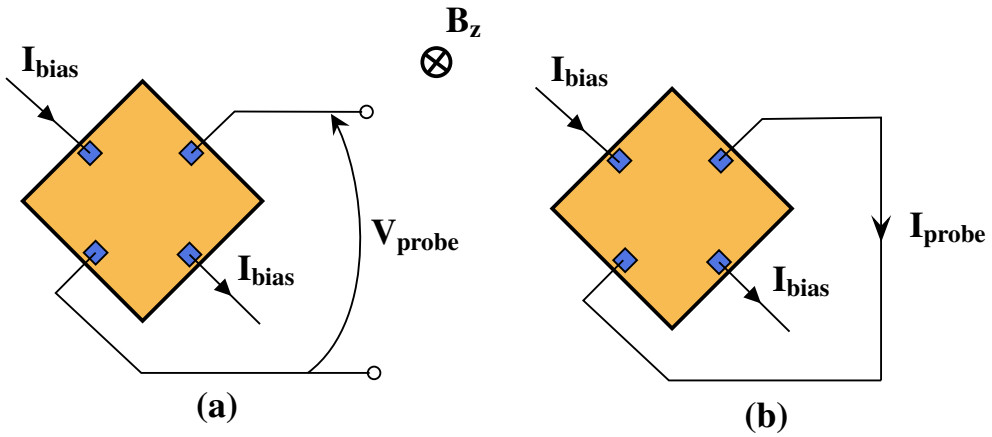


Figure 2.6: Square shaped Hall-effect device configured in (a) Voltage mode, (b) Current mode

has been compared as it has been found in literature based on equating the units of the derived results [81], but this is not a fair comparison because the biasing conditions affects the temperature-magnetic cross sensitivity and linearity of the device. Usually, high-mobility, thin-film semiconductor materials with a small band-gap are intrinsic at room temperature and usually biased by a voltage source that results in a low temperature-magnetic cross-sensitivity. But their device current has a very high temperature coefficient, and therefore is susceptible to thermal breakdown. Other semiconductor materials such as silicon and GaAs, on the contrary, are strongly extrinsic at nominal temperature and the temperature-magnetic cross-sensitivity of a current biased Hall device is much smaller than that of a voltage-biased device [59]. This is also a primary reason for our choice of current biasing in this project as will be discussed in the next chapters.

The following mathematical formulations hold true for the sensitivity of the Hall device:

Voltage-related sensitivity, when biased by voltage , V_{bias} in voltage mode

$$S_V^V = |\frac{V_{probe}}{V_{bias} \times B_z}| \quad [V/VT] = [T^{-1}] \tag{2.34}$$

Voltage-related sensitivity, when biased by voltage in current mode

$$S_V^I = |\frac{I_{probe}}{V_{bias} \times B_z}| \quad [A/VT] \tag{2.35}$$

Current-related sensitivity, when biased by I_{bias} in voltage mode

$$S_I^V = |\frac{V_{probe}}{I_{bias} \times B_z}| \quad [V/AT] \tag{2.36}$$

Current-related sensitivity, in current mode

$$S_I^I = |\frac{I_{probe}}{I_{bias} \times B_z}| \quad [A/AT] = [T^{-1}] \tag{2.37}$$

More elaborate discussion on the operating modes can be referred in sections 3.3 and 4.

2.5 Horizontal versus Vertical Hall sensors

In contrast to the conventional structuring and usage where the magnetic field to be measured is perpendicular to the plate surface, specific applications would require measuring the magnetic field which could be parallel to the plate surface or is non-homogenous over the volume of Hall device. In other words, a multi-axis sensor on a single semiconductor wafer may be required. Non-plate-like or vertical or in other terms 3-D Hall devices fulfill this sensing requirement by adapting to conform to the shape of the magnetic field. Fig. 2.7 illustrates a vertical Hall device with five contacts. In the presence of magnetic induction, now planar to the device surface, and normal to the applied bias current, which arches across the device and sinks into the ground through contacts 1 and 5 resulting in the Hall signal between the sense contacts 3 and 4. To create a three axis sensitivity, a pair of these devices aligned to each other by 90° can be used with the horizontal Hall-effect device [30]. However, it is worth highlighting that the vertical Hall devices lack the general four-way symmetry that is present in the horizontal devices and the sensitivity when configured in voltage mode is usually lower

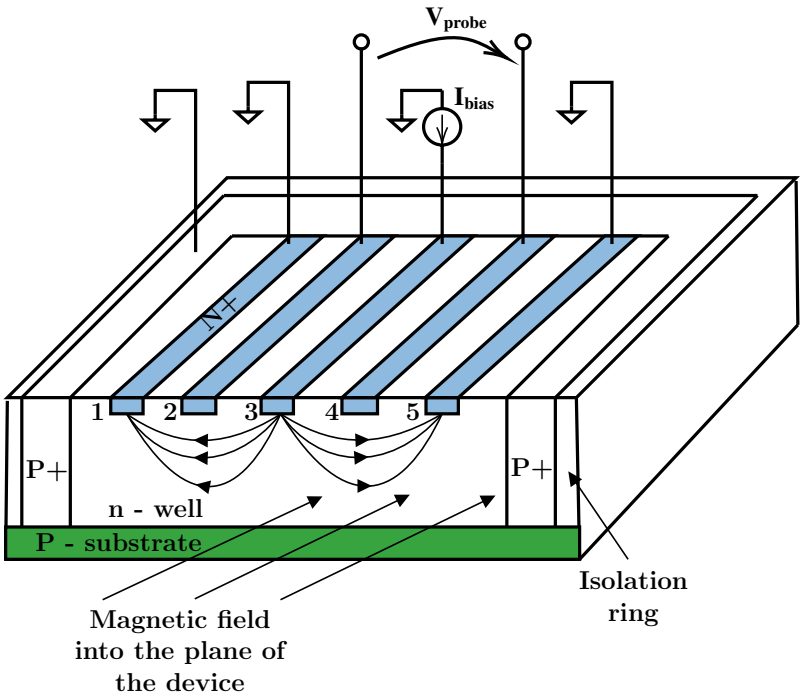


Figure 2.7: Vertical Hall-effect transducer with five contacts

in contrast to the configuration in current mode [81].

2.6 Hall - Effect Current Sensor

Having gained an understanding of the composition of a Hall device, the various factors that contribute to the sensed Hall voltage and the possible technologies for realizing it and the various modes it can be configured with their corresponding sensitivities, we must also realize that the Hall plate cannot be used for current or magnetic field sensing as a standalone for a practical application. This is because the sensed signal is a small quantity that must be amplified with an appropriate microelectronic readout circuitry for usability. Moreover, the sensed voltage or current is a sum of the actual Hall electric output with an offset (refer Eq.2.32 and 2.33), which is usually orders of magnitude higher than the usable Hall signal itself. With these technicalities, one must not be disinclined, because unlike most sensing techniques the realization of the Hall sensor is quite easy to implement and integrate

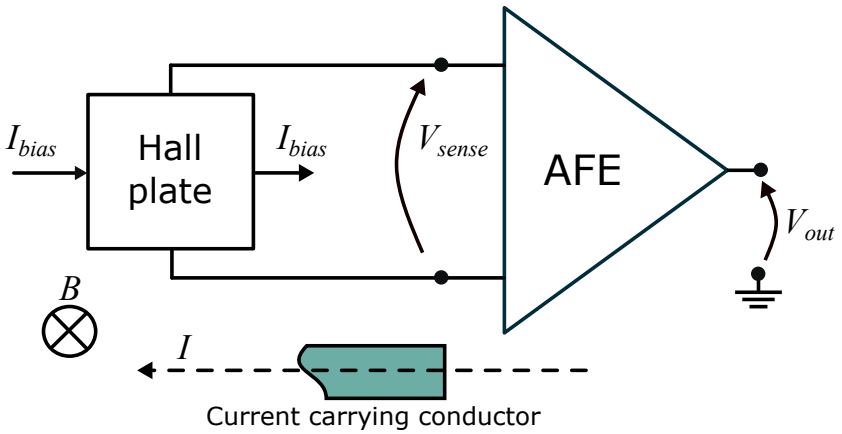


Figure 2.8: Typical sensing chain of the HECS, consisting of the current-to-magnetic field transduction, the Hall plate, and the AFE.

with standard CMOS or BCD processes which gives a strong motivation for the design of the supporting circuits for amplification and trimming of the offset. Before gaining an insight into the realization of the HECS, Fig.2.8 recalls the overall HECS system block diagram. For an overview, the chain includes the magnetic field induction on the Hall plate for the generation of the Hall electric output. The offset within the output must be trimmed and the useful signal read and amplified. A detailed description follows:

2.6.1 Current-to-Magnetic Field Transduction

The transduction from current to magnetic field is based on the Ampere's circuital law. In the magnetostatic case, and considering the simple example of a conductor of infinite length and negligible cross area traversed by a constant current I, the Ampere's law can be simplified by using the Biot-Savart formula:

$$|\mathbf{B}(r)| = \frac{\mu_0 \mu_r I}{2\pi r}; \tag{2.38}$$

where μ_0 is the magnetic permeability of the vacuum, μ_r is the relative permeability of the media surrounding the current conductor, and r is the distance between the conductor and the point in space at which the magnetic

field is sensed/evaluated. The Ampere's law and its derivations state that it is always possible to indirectly estimate a current by sensing the associated magnetic field at a known distance r. However, magnetic interferences may corrupt (2.38) with an additive term, affecting the selectivity of the HECS.

The current-to-magnetic field transduction factor, G_{ib} is of paramount importance in HECSs, as it can affect many sensor metrics, e.g., sensitivity, input full-scale range, and MDS. For the example above, it can be defined from (2.38) as

$$G_{ib} = \frac{|\Delta \mathbf{B}(r)|}{\Delta I} = \frac{\mu_0 \mu_r}{2\pi r}, \tag{2.39}$$

highlighting a direct dependence of G_{ib} to the exact distance of the sensor from the conductor by means of the parameter r. This dependence may cause many issues like increased sensitivity to mechanical noise and nonlinear effects. While (2.39) reports the transduction factor for a simple academic case, an accurate analysis of the magnetic circuit and geometries are required for getting the exact formulation of G_{ib} in practical cases. Usually, the G_{ib} factor should be maximized to improve the MDS and sensitivity, and should be made insensitive to thermo-mechanical effects.

Moreover, the magnetic environment should be designed to reduce the sensitivity to external EMI. In general, the use of a core allows to shunt stray magnetic fields around the sensor. Conversely, coreless architectures are susceptible to stray fields from high-current carrying traces, which may be captured by the Hall plate and eventually cause inaccurate current measurements. In this case, a differential Hall plate configuration can be employed, although any mismatch between the Hall plates, or any field disuniformity, will result in a deviation in the output signal. In the following, the most used and important arrangements employed in HECSs are briefly summarized.

Yoke-Hall

An arrangement combining a Hall plate with a gapped magnetic yoke is shown in Fig. 2.9a [29, 82–84]. Specifically, the magnetic core is clamped around the current-carrying conductor (i.e., a wire or a busbar), and all the

magnetic flux generated by the current I is concentrated on the core itself and focused on the Hall plate, which is placed in the air gap of the magnetic core. This arrangement is named open-loop configuration and changes the equation of the magnetic field on the Hall plate as follows:

$$|\mathbf{B}| = \frac{\mu_0 \mu_r I}{2\pi(r-d) + d\mu_r}, \tag{2.40}$$

where d is the thickness of the air gap, while the distance r can be usually approximated with the yoke diameter. A good design satisfies the inequality $d\mu_r \gg 2\pi r$, allowing to simplify (2.40) in

$$|\mathbf{B}(r)| = \frac{\mu_0 I}{d}, \tag{2.41}$$

which is independent of the relative position of the wire. By comparing (2.41) and (2.38) in free space, it is possible to notice that G_{ib} in the yoke-Hall open-loop configuration has been increased by a factor $2\pi r/d$, and that it can be increased even further by wounding the wire around the yoke. This arrangement offers G_{ib} factor as high as 1 mT/A and it is robust against EMI, but the bandwidth, weight, and space are affected by the presence of the yoke, which also suffers from magnetization in case of large over-current events.

The closed-loop configuration, also known as zero-flux sensor, copes with this last issue [13, 29, 82–84]. In this case, the output of the Hall probe drives a secondary coil wound around the magnetic core, in order to null the magnetic flux density inside the core (Fig. 2.9b). This arrangement still exploits the advantages given by the core to improve the sensitivity and to reduce the dependency on the geometry, as well as the sensitivity to EMI. It should be noted that the Hall plate is placed in the feedback loop, so that the output of the HECS is the voltage potential on the output resistor. Moreover, this arrangement resembles a CT at high frequencies [84, 85], improving the bandwidth. Nevertheless, its usage is not straightforward in modern applications given the weight and space occupation.

Yoke-less open-loop sensor

A more compact arrangement can be obtained by realizing a yoke-less open-loop configuration at PCB level, as shown in Fig. 2.9c. [29, 48, 86–91]. In this case, the current-carrying conductor is realized as a trace on the top conductive layer of the PCB (or on a separated bus bar) and the Hall probe is implemented as an integrated circuit (IC) placed vertically on top of the trace in order to maximize the G_{ib} factor. Thus, the G_{ib} factor for this configuration can be approximated as [87]:

$$G_{ib} = \frac{\mu_0}{2(W + 2H)}; \tag{2.42}$$

where W is the trace width and H is the trace-to-sensor distance. Yet, package-to-PCB clearance as well as package and die thicknesses usually imply $H > 0.3$ mm [91]. Typical values of G_{ib} factor are in the order of 100 μT/A. However, multi-layer/multi-turn techniques, as well as ferromagnetic shields [87] can be used to further increase the G_{ib} factor by concentrating the magnetic field on the Hall probe.

An important implication of the PCB approach is that the magnetic field lines on the Hall probe lie on the x-y plane, while the Hall plate is sensitive to the out-of-plane field. Thus, it is required to either rotate the Hall IC or bend the field lines. The usage of a through-hole package for the sensor allows to rotate the Hall IC and place it vertically with respect to the board

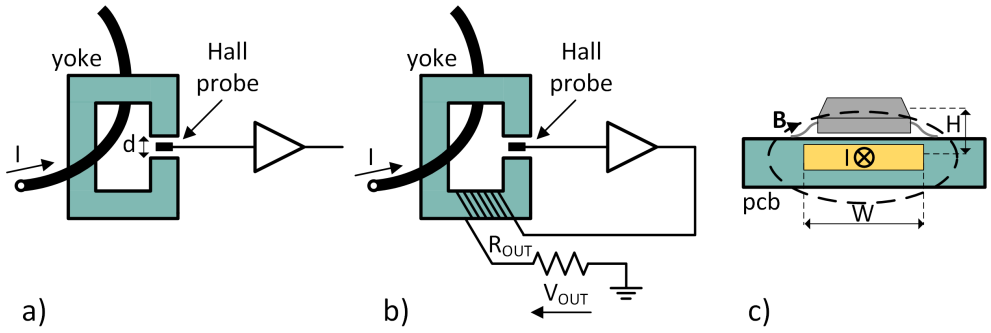


Figure 2.9: a) Open-loop HECS with magnetic yoke. b) Closed-loop HECS with magnetic yoke. c) Open-loop yoke-less HECS with current-carrying trace realized at PCB level.

plane. However, this technique increases the trace-to-probe distance above 1 mm.

Alternatively, it is possible to integrate magnetic flux concentrators (IMCs) in the same IC used for the Hall probe [49, 50, 92–94]. IMCs are thin layers (10 – 100 μm) of high-permeability ferromagnetic material spattered over the silicon die. The magnetic field lines converge on one edge of the magnetic material and diverge on the opposite one. Hence, the field lines bend in the proximity of the flux concentrator edge, creating a convenient positioning for the Hall plate (Fig. 2.10). Moreover, the concentration of the field lines lead to an amplification of the magnitude of the magnetic field, with an amplification factor depending on the shape and thickness of the concentrator, on the relative position of the Hall device, and on other geometical factors. Magnetic gain values from 5 to 10 are reported in the literature [49, 92]. It should be noted that IMC can suffer from the saturation of the ferromagnetic material, making the G_{ib} factor nonlinear at high-field, hence limiting the full-scale range.

Open-loop sensor with on-chip trace

To reduce the trace-to-probe distance down to a few μm, it is possible to integrate the current-carrying trace and the Hall probe within the same IC [32, 77, 95, 96] by exploiting thick copper layers [97], redistribution layers

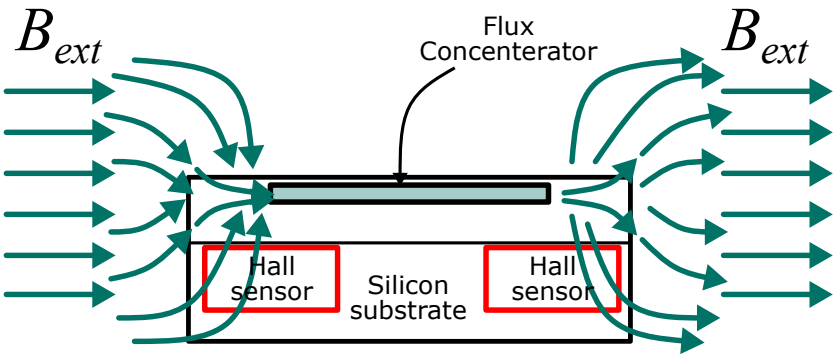


Figure 2.10: 2D representation of the magnetic effects of IMCs. The flux lines due to the external magnetic field are bended and concentrated into the IMC, where the flux density is higher.

in wafer-level packaging, or copper frames. However, when placing the Hall plate at the minimum allowed distance, i.e., vertically beneath the trace, the out-of-plane field acting on the probe is zero. As IMCs and other magnetic techniques cannot be exploited at such a small scale, the only possible solution is moving the probe laterally away. This will increase the trace-to-probe distance and lower the magnitude of $\mathbf{B}$, but the component of the field on the z-axis will increase, leading to a design trade-off.

Figure 2.11 reports the z-component of the field at the silicon-oxide interface beneath the trace, showing that the optimum position for the Hall probe is exactly below the edge of the current-carrying trace. This geometrical arrangement also implies that the magnetic field on the Hall probe is not confined to the z-direction, and a non-negligible in-plane field will arise. This could trigger spurious behaviour at the probe level, like planar Hall effects (see Sec. 2.1).

The integration of the trace and probe on the same IC provides a good rejection of mechanical noise, allowing to assume a noiseless $I - B$ transduction, given the precise and stable definition of the relative distance. On the other hand, the lack of magnetic circuits makes the HECS sensitive to exter-

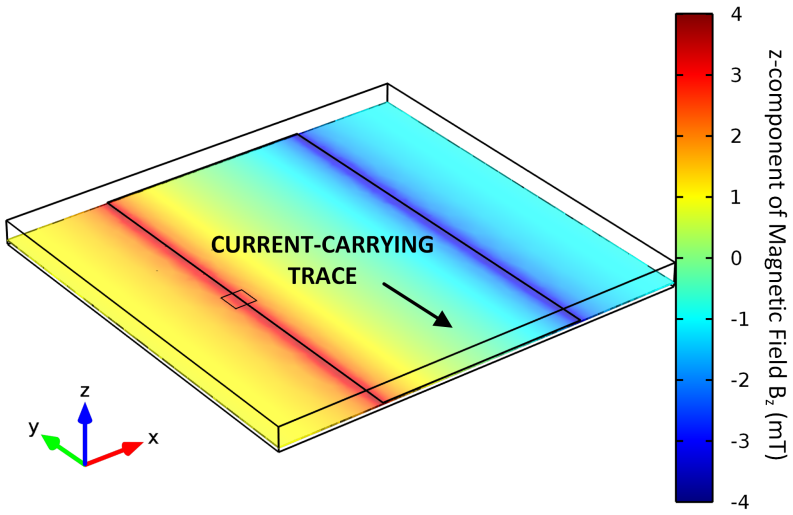


Figure 2.11: Bidimensional map of the B_z field computed at the silicon-oxyde interface 10 μm beneath the copper current-carrying trace. The map shows a maximum of the B_z field at the vertical projections of the edge of the trace.

Table 2.2: Full-scale ranges for open-loop current sensors.

Technical Solution	Typical Input Full-scale Range
Open-loop HECS with yoke	up to 700 A
Bus bar with magnetic shield	From 50 A to 700 A
On-board PCB trace	From 10 A to 50 A
On-board PCB trace with multi-turn	From 2 A to 10 A
open-loop sensor with trace on WLCSP	< 20 A

nal magnetic fields. This issue can be mitigated by placing two Hall plates below the opposite edges of the trace and combining their output voltages to eliminate any common-mode magnetic field interference, e.g., the earth magnetic field, or the one induced by noisy power circuits [98]. With this arrangement, G_{ib} factors in the order of a few mT/A can be achieved [77]. The thick copper layer presents low sheet resistance values, yet it poses a limitation on the maximum allowed current due to electromigration and heat dissipation. Although large integrated copper traces could present a resistance lower than 10 mΩ [48], a 10-A current would already imply a few W of heat power to be dissipated and this may result in an orthogonal temperature gradient when a magnetic field also referred to as the Righi–Leduc effect or the thermo-Hall effect. Dedicated package solutions with low thermal resistance are thus mandatory in this case. Moreover, specific lead and bonding techniques with low resistivity values must be implemented. At the same time, the package, leads, and bonding wires can critically reduce the operating bandwidth, as they create spurious parasitic elements, which couple the magnetic field generated by the sensed current into sensitive signal nodes [36]. Different packaging solutions are available on the market, which differ with respect to the maximum allowed current on the integrated trace. The Wafer-level chip-scale package (WLCSP), with the measurand flowing on redistribution layer (RDL) copper traces [77], or a flip-chip mounted Hall plates on U-shaped copper frames, can handle up to a few tens of A [48]. Table 2.2 reports the standard full-scale ranges for different types of open-loop current sensors based on the Hall effect.

2.6.2 Offset cancellation

The offset voltage is one of the main constraints in Hall plates, as it can be up to a few mV, leading to an input-referred magnetic field offset from a few mT to tens of mT [99, 100]. The intrinsic offset voltage of the Hall plate ($V_{OS,plate}$) can be caused by both systematic and random sources, e.g., resistivity gradients, crystal defects, and mechanical stress [23, 100, 101].

The output voltage V_{probe} of the Hall probe is the differential voltage measured between the sense contacts, that can be written as

$$V_{probe} = \int_{S1}^{S2} \mathbf{E}\, dl \tag{2.43}$$

where $\mathbf{E}$ is the global electric field resulting from both electrostatic and magnetic actions. The expression of $\mathbf{E}$ can be generally split into the sum of the two orthogonal components $\mathbf{E_H}$ and $\mathbf{E_{bias}}$

$$\begin{aligned} V_{probe} &= \int_{S1}^{S2} \mathbf{E_H} + \mathbf{E_{bias}}\, dl \\ &= \int_{S1}^{S2} \mathbf{E_H}\, dl + \int_{S1}^{S2} \frac{\mathbf{J_{bias}}}{\sigma_B}\, dl = V_H + V_{os,plate}. \end{aligned} \tag{2.44}$$

The first term in (2.44) is the Hall voltage, while the second term is an additive perturbation, i.e., the offset voltage $V_{OS,plate}$, which is originated by the non-ideal implementation of the Hall plate. Looking at Eq.(2.44), one can see that the offset voltage is zero only if the current density lines due to the biasing electric field are perfectly orthogonal with respect to the straight line from S1 to S2. However, the misalignment of the sense contacts and the finite geometrical realization of the Hall plate do not allow for perfect orthogonality. The other important sources of offset are related to imperfections in the device fabrication, non-uniformity of the semiconductor properties, and mechanical stresses due to the piezo-resistance effect. Some of these effects (like doping gradients) are isotropic, so their effects can be cancelled by Spinning Current Technique, SCT. Nevertheless, mask misalignment and mechanical

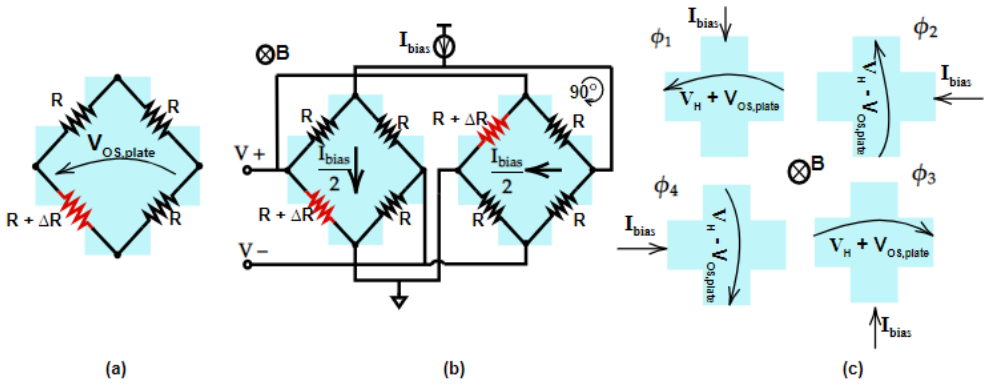


Figure 2.12: (a) Wheatstone bridge model of the intrinsic offset in CMOS Hall sensors. (b) Connection of two Hall plates in the pairing technique with modelling of systematic offset, only. (c)Graphical representation of 4-phase spinning-current technique for cancellation of the intrinsic offset.

stresses could still lead to residual offset, ΔV_{OS}.[2]

Given its importance, many works in the literature [102–106] have dealt with its modelling and compensation. The basic model for $V_{OS,plate}$ is the unbalanced resistive Wheatstone bridge (Fig. 2.12a), where the differential voltage between the two branches results in

$$V_{os,plate} = \frac{\Delta R}{4R} V_{bias}. \tag{2.45}$$

While there exist more complicated equivalent circuit models, they all derive from the basic Wheatstone bridge.

In theory, the easiest way to lower the offset is pairing two Hall plates and connect them in parallel, while rotating one of the two plates by 90 degrees (Fig. 2.12b). Nevertheless, this technique also doubles the area and power consumption [100, 107–109]. If the Hall plate is symmetric and reciprocal (i.e., the bias and sense contacts can be interchanged without any effect on the Hall voltage), it is acceptable to concentrate the unbalance of the Wheatstone bridge into a single element, as in Fig. 2.12. In fact, it can be easily found that the offset is theoretically nulled by applying the pairing technique [107]. Unfortunately, the offset of the two probes is not

[2]**Note:** V_{OS} represents the residual offset seen at the output of the Hall plate after the intrinsic offset, $V_{OS,plate}$ is cancelled.

the same due to the statistical nature of some of the offset sources, leading to a residual value. In addition, the offset is time- and temperature-dependent, thus requiring periodic calibration.

The main advantage of Hall plates realized on silicon is the straightforward integration with standard CMOS technology, allowing to implement a series of dedicated circuits and systems addressing the non-idealities of the Hall probe [110, 111]. Also, complex digital circuits can be integrated for the realization of smart sensors [95, 112]. A noteworthy circuit dealing with the offset voltage problem in symmetric Hall plates is the spinning-current (SC) technique [113]. It involves biasing the same Hall plate in four orthogonal directions, dynamically swapping contacts between biasing and sensing every $T_{spin} = \frac{1}{f_{spin}}$, so that a full rotation takes a total time of $4T_{spin}$ (Fig. 2.12 (c)). Due to the symmetries of the Hall probe, a 90-degree spatial rotation of the bias current causes a change in the sign of $V_{OS,plate}$, while its magnitude remains approximately the same [74, 113]. As a result, the offset voltage is modulated at frequency $\frac{f_{spin}}{2}$ and can be attenuated by a low-pass filter. Moreover, a proper choice of the SC phase sequence allows to suppress interferences, low-frequency noise, and pick-up noise [52].

Nevertheless, a residual ripple will typically remain, and its removal has been the subject of research in the last years [91, 111, 114]. In addition, due to the anisotropy of the Hall plate (caused by, e.g., junction-field effect and piezoresistivity) [74, 99, 103] the value of $V_{OS,plate}$ changes with the bias direction, causing a residual DC offset, yet $\times 100$ lower than the intrinsic one.

A complex switching network, used to route the contacts of the Hall plate either to the generator of the bias current or to the readout circuit, is required to implement the SC technique. This network can be smartly designed to work as SC for the Hall plate, and as chopper for the AFE, reducing the area required by the electronic interface. Regarding the AFE, the CCIA presents the lowest input-referred offset thanks to the chopper architecture. However, the implementation of the switches adds non-ideal effects, like charge injection and clock feedthrough. To cope with these effects, the switches are usually large, increasing the capacitive load seen by the Hall plate and limiting the achievable bandwidth.

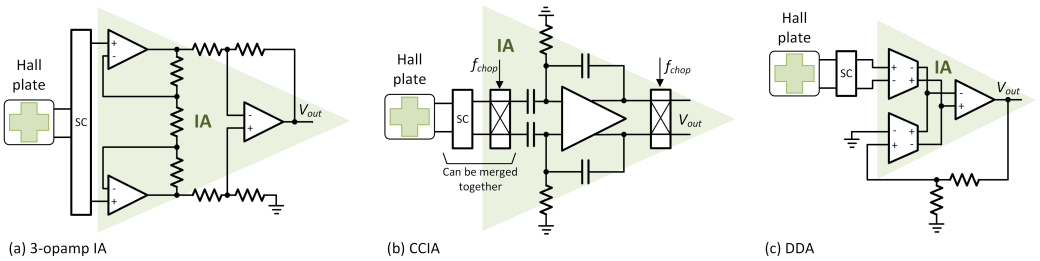


Figure 2.13: Examples of instrumentation amplifiers (IAs) used as analog front-end (AFE) for Hall plates. (a) Three operational amplifiers (three-opamp) IA; (b) capacitively-coupled instrumentation amplifier (CCIA) with choppers; (c) differential-difference amplifier (DDA). All the AFEs are connected to the Hall plate by a circuit implementing the SC technique.

2.6.3 Analog Front-End

The AFE has a crucial role since it directly affects the sensor performance, and it must be adapted to the characteristics of the Hall plate. In general, the AFE includes the circuits required for both biasing the Hall plate and for sensing the Hall electric signal which could be a voltage or current. The choice of biasing the Hall device is dependent on the semiconductor technology of the Hall probe and can affect the resultant performance of the sensor as a whole (refer section 2.4). Biasing the Hall probe with a current source suits our requirement as it would result in a lower temperature coefficient of the resultant signal. It could be implemented using a simple standard current mirror, an operational amplifier or an outboard opamp. Some possible biasing configurations are shown in Fig.2.14. The configurations in Fig.2.14(a) and (c) have the Hall-effect transducer terminal grounded and the current drive and stability of the bias current with respect to rail voltages and temperature can be set by design choices. For the Howland source, the resistors R_A must be well matched and much higher than R_S, so the output bias current is given by V_{REF}/R_S. The configuration in Fig.2.14(b) uses feedback to regulate current through R_S given by V_{REF}/R and so, it is usually thermally constant, however the transducer is floating at an indeterminate point between supply rail and ground.

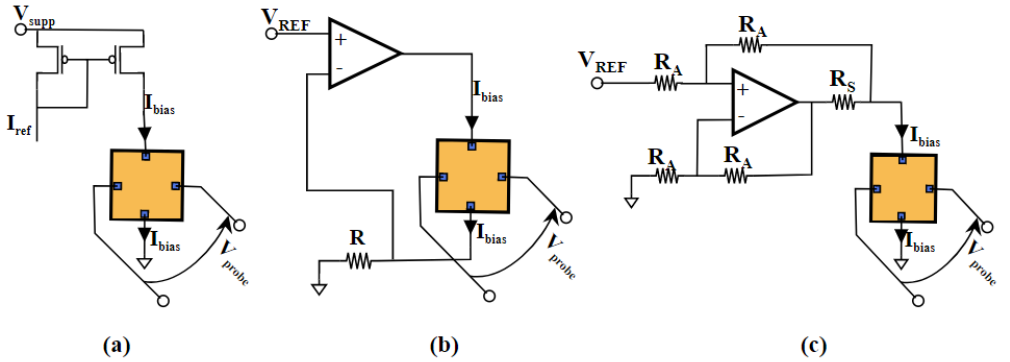


Figure 2.14: Hall probe biasing techniques using (a)standard current mirror, (b) opamp, (c) Howland current source

Voltage mode

The AFE for a Hall transducer configured in voltage mode must fulfill many requirements, among which [112]:

- high differential gain, usually greater than $\times 100$, depending on the application and technology;
- high input impedance, to avoid drawing current from the sense contacts;
- negligible offset with respect to the inherent one displayed by the Hall plate.

The first two requirements imply the adoption of an instrumentation amplifier (IA). The IA can be implemented by using different circuital architectures, like the three operational amplifiers (thee-opamp) topology [107] (Fig. 2.13a), the capacitively-coupled instrumentation amplifier (CCIA) [96, 114] (Fig. 2.13b), or the differential-difference amplifier (DDA) [32, 77] (Fig. 2.13c).

The three-opamp is the standard IA architecture, but the usage of three amplifiers increases the noise level, together with a considerable power consumption. In addition, while the usage of off-chip resistors leads to high accuracy, it also increases the cost and area. The CCIA is a non-inverting

fully-differential operational amplifier using capacitors instead of resistors in the feedback loops. In this way, the circuit does not draw any DC current from the sensor, but its DC operating point must be carefully set using high-value resistors or pseudo-resistors [115, 116]. It offers very good performance in terms of noise and power consumption, since it is based on a single gain stage [116]. However, it requires an input upconversion stage to allow for DC signal sensing, which would otherwise be filtered out by the input capacitance [116]. This modulation stage can be implemented by a chopper circuit, which grants very low input-referred offset, but it also limits the input impedance $Z_{in,AFE}$, which is inversely proportional to the chopping frequency and input capacitance [117]:

$$Z_{in,AFE} = \frac{1}{2\pi f_{chop} C_{in}}. \tag{2.46}$$

The main disadvantage of the CCIA is a limited acquisition bandwidth due to the frequency-dependent input impedance given by (2.46) and the high capacitive input load given by the switches used in the chopper. The DDA, formally described by [118], is an extension of the operational amplifier featuring two differential inputs, suitable for the processing of floating voltages. It can be used by means of a standard resistive feedback without sinking DC current from the input. It offers a good trade-off among noise, power consumption, and input impedance, while being intrinsically more noisy than the CCIA due to the presence of more gain stages and resistors. However, the Hall plate can be DC-coupled to a differential input pair, sinking negligible current from the sense contacts. This architecture allows to minimize the capacitive input load and enlarge the bandwidth by minimizing the size of the input transistors [77], or adding capacitive cancellation systems based on positive feedback [119].

Current mode

The current mode, in which the Hall voltage is nulled and the output of the Hall plate is a differential current, is indeed possible as discussed earlier. In this case, the AFE is realized by a transimpedance amplifier (TIA) [120].

In contrast to the requirements for a voltage mode X-Hall probe interface, the TIA must ensure

- A very low input impedance so that the majority of the output current I_{probe} sinks into the TIA
- A high transimpedance gain so the input input impedance is negligible and for a high signal to noise ratio, SNR.
- high acquisition bandwidth (in MHz) and low power consumption.

Apart from the AFE choices based on the mode of operation of the device, other interface issues relate to the linearization of the sensor, the connected load, calibration of sensitivity, trimming of the offset and analog to digital conversion of the output signal which is optional and implemented if required.

2.7 Non-idealities

Non-idealities of the Hall plate set the main performance limitations of the current sensor. Therefore, it is important to analyze the specific performance criteria of the Hall plate.

Sensitivity

Recalling the definition of sensitivity in Sec. 1.1 and 2.4 for a Hall plate, the sensitivity of the HECS can be expressed as:

$$S = G_{ib} S_A G_{AFE}, \tag{2.47}$$

where G_{ib} is the current-to-magnetic field transduction, G_{AFE} is the electronic gain of the AFE, and S_A is the absolute sensitivity of the Hall plate, which can be expressed as:

$$S_A = \frac{V_{probe}}{B_z} = \frac{G_H R_H}{t} I_{bias}. \tag{2.48}$$

Table 2.3: Current-related sensitivity for different Hall probes.

Reference	Semiconductor technology	S_I (V/AT)
[36]	Silicon BCD	200
[121]	GaN	130
[122]	Graphene	1000
[37]	Silicon BCD	800
[123]	Silicon CMOS	250

According to (2.47), all the three stages of the sensing chain have the same importance in determining the sensor sensitivity. The absolute sensitivity S_A cannot be used as a FoM for the Hall plate, since it depends on the applied polarization. Therefore, two other sensitivities are defined for Hall plates: the current-related sensitivity S_I=S_A/I_{bias} and the voltage-related sensitivity S_V=S_A/V_{bias}, which are selected according to the applied bias (either current or voltage, respectively). These are related to each other by the input resistance of the Hall plate

$$R_{in,plate} = \frac{V_{bias}}{I_{bias}}. \tag{2.49}$$

The current-related sensitivity, which is the most used one, it is expressed in V/AT units. State-of-the-art values are reported in Tab. 2.3 for different Hall probes and materials. It is important to note that the S_I is a function of temperature due to the thermal dispersion of the Hall coefficient R_H and the concentration of free carriers n in the active region [74].

Offset

The generation of an intrinsic offset voltage and its modelling has been discussed in 2.6.2. Apart from that, the additive DC offset in (1.1) also takes into consideration the offset of the AFE, as well as other magnetic interferences. The earth magnetic field is a typical example of this kind, but also other spurious magnetic fields generated by nearby currents should be considered.

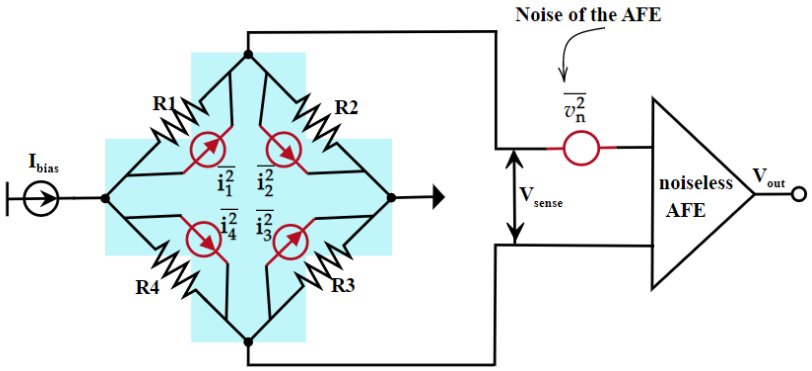


Figure 2.15: Wheatstone's bridge model of a Hall sensor with noise contributers

Noise

Concerning the Hall plate, random fluctuations of the free carriers in the semiconductor active region set the ultimate limit for the HECS resolution. As seen earlier, the Hall probe can be modelled as a Wheatstone's bridge, whose resistances R_1, R_2, R_3, R_4, in fact contribute to the thermal noise, $\overline{i_n^2}$ modelled by the current sources as illustrated in Fig.2.15

$$\overline{i_n^2} = \frac{4KT\beta}{R_n} \tag{2.50}$$

where K = 1.38 $\times 10^{-23}$J/K is the Boltzmann's constant, T = 300 K is the absolute temperature and β is the bandwidth. The additional input referred noise voltage from the AFE can be expressed as

$$\overline{v_n^2} = 4KT\beta R_n \tag{2.51}$$

This also implies that the Hall probe itself acts as a limiter to achieving a broadband performance by impacting the resolution at higher frequencies. The other limits to bandwidth would be discussed later in sec.3

The noise in a Hall plate is mainly due to thermal and flicker noise. The latter can be reduced by using the buried Hall plate, so that the silicon-oxide interface is moved away from the active region by a superficial p-type layer. Being low-pass, flicker noise is also attenuated by SC. On the other hand, the

thermal noise, which is related to the resistivity of the silicon well used to realize the Hall plate, cannot be removed. The most used metric to quantify noise generated by the Hall plates, which adds to the output voltage measured between the sense contacts, is the noise equivalent magnetic field (NEMF), that is the equivalent magnetic field that would have been generated by the same output:

$$\text{NEMF} = \frac{v_n}{S_A}; \tag{2.52}$$

where v_n is the r.m.s. noise integrated over the acquisition bandwidth.

As far as the entire HECS is concerned, also the noise from the AFE has an important role and can be added (in the power domain) to the plate noise, given that they are uncorrelated. CCIA offers the lowest possible noise because it does not rely on resistors, minimizes the number of active elements, and employs the chopping technique to reduce the flicker noise. On the contrary, the current-to-magnetic field transduction can be treated as noiseless.

Bandwidth

To suit the modern application requirements of power electronics, it is important that the Hall sensor achieves a high frequency of operation. Historically, the sensor has faced numerous limitations and so was used for low-frequency applications. If the sensor is to be designed for accuracy, its bandwidth must be times greater than the signal bandwidth itself [30]. Compared to other types of sensors, the magnetic sensitivity of Hall devices is lower which implies an AFE with a high electronic gain which will degrade the bandwidth for a constant gain bandwidth product. Integrated use of magnetic concentrators is proven to improve the magnetic sensitivity and hence the bandwidth [59]. Recent broadband current sensors combine low-frequency Hall-plates with high-frequency coils or current transformers into the same silicon chip, but they are more complex and suffer from the sub-optimal match of the frequency responses [91]. A discussion on the various bandwidth limits is made in the following chapter.

Chapter 3

Bandwidth enhancement in Hall sensors

3.1 Bandwidth limits

This section aims to highlight the main limitations to the bandwidth of Hall sensors in general and the following sections and the proposed solutions that form the argument of this thesis, will demonstrate how this work overcomes certain limits. Crescentini et al. recognized four limits to bandwidth [45] for purely semiconductor based Hall sensors.

1. The ultimate **physical limit** which is in the range of GHz - THz range depends on the quantum phenomena related to the relaxation time of the charge carriers and so this limit is rendered practically unachievable,

2. The **fundamental limit** that ranging from MHz - GHz range is dependent on the technology and practical implementation and is set by the product of the transversal resistance, R of the probe and the intrinsic capacitance, C due to the depletion region over the n-well (as shown in 3.1(a)), the $\tau = RC$ time constant and the related frequency pole,

3. The electronic/ readout circuits connected to the probe add a capacitive load to it, which usually is minimal in case of an ideal front-end. But

practically, the AFE adds a significant capacitive load thus setting the **practical limit**.

4. The **methodological bandwidth limit** is set by the readout techniques, eg., by the widely adopted Spinning Current Technique, SCT for offset reduction in standard spun Hall sensors and limits the bandwidth to less than $\frac{1}{4T_{spin}}$. The switch parasitics of the (SCT) and its dynamic performance play a significant role in setting this limit which may not be exceeded in a given particular sensor design. The DDA architecture can be exploited to partially remove the issue by moving the switches required by SCT after the AFE [77], thus minimizing the size of the input transistors of the DDA. Broader bandwidth can be achieved by replacing SC with passive offset compensation techniques and improving the DDA with current-feedback solutions [36, 112].

3.2 The X-Hall probe

3.2.1 Device model

The sensors in voltage mode can be biased either with voltage V_{bias} or current I_{bias}. The output differential voltage can be formulated as, $V_{probe} = V_H + V_{OS,plate}$, where the Hall voltage, V_H is usually altered by a large offset voltage, $V_{OS,plate}$ requiring additional techniques for its reduction leading to system complexity, higher cost, area and limited bandwidth. The X-Hall probe was introduced for the very first time in 2018 at the IMEKO XXII World Congress by Crescentini et.al. [124], in pursuit to push the Hall sensor bandwidth limit to its technological limit while also providing a significant reduction in the offset voltage. The structural framework of the probe was designed on a purely DC bias approach without the need for additional switch/timing circuitry that would otherwise be conventionally required in spinning current approaches for offset reduction. The probe was designed as an octagon, bearing a horizontal axis of symmetry and is based on the theory of containing and merging two identical probes, probe A and Probe

B, that work as a current splitting Hall-effect sensor along the horizontal axis of symmetry in the same lightly doped n-well as shown in Fig.3.1(a) which serves as the magneto-sensitive active region. It is surrounded by a p-well which is connected to ground to warrant electrical isolation from the substrate. The choice of the lightly doped active region as n-well is preferred over the p-well as it offers higher current related sensitivity, S_I. This encapsulation however, generates a non-uniform depletion region around the n-well and that creates : (i) parasitic capacitance effect, (ii) assymetries in the sensor because the thickness of the depletion region is proportional to the local bias potentials. Eight highly doped contacts: 4 large bias contacts (T, B, L, R) orthogonally oriented to the edges of the probe, and 4 small sense contacts (1, 2, 3, 4) are used to access the active region. The contacts L and R are shared by the two Hall-effect probes and are grounded as in Fig. 3.1(b). The enlarged bias contacts minimize the access resistance to the Hall probe, while the sense contacts are optimally shrunk to minimize the associated parasitic capacitance and enhance sensitivity also taking into care that excessive reduction in size could make the probe susceptible to lithographic errors during fabrication and can increase the probe offset.

To reach a clear understanding of the concept of the X-Hall probe, let us consider that the device is biased with nominally equal currents I_A and I_B, the magnetic field in the z -direction is zero and the sense contacts are floating. We consider 2 identical probes, A and B along the horizontal axis of symmetry. If the probes A and B are fully symmetric and homogeneous, then the currents, I_A and I_B that flow are equally distributed along the y-axis and the associated current density is uniform throughout the device thus rendering,

$$\begin{aligned} V_A &= 0, \\ V_B &= 0 \end{aligned} \tag{3.1}$$

Then consider a magnetic field, B_z is applied along the z-axis. The current density over the entire device now will no more be uniform and will concentrate on one side. This can be represented by the corresponding unbalance

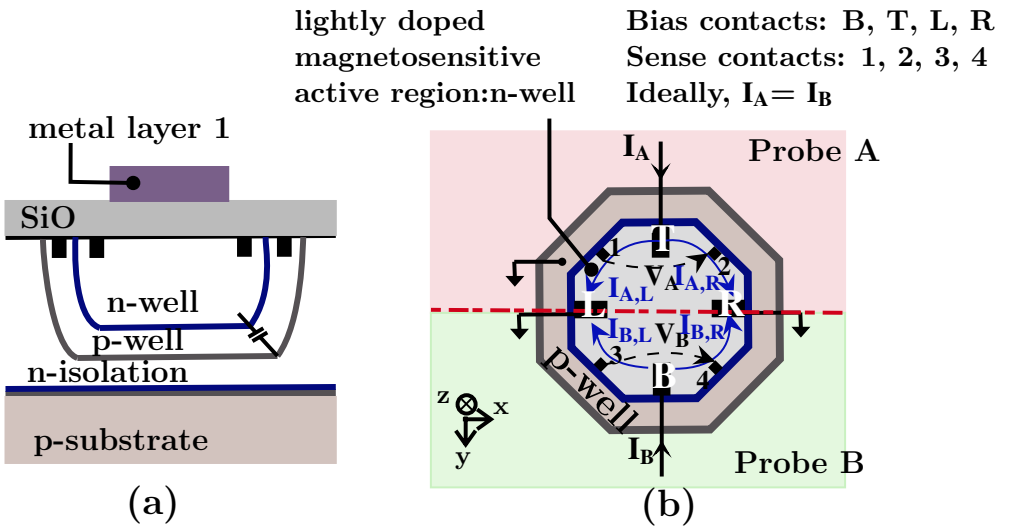


Figure 3.1: Concept of X-Hall effect device: (a) Vertical cross section of the X-Hall probe illustrating the encapsulation of the active magneto-sensitive region by a p-well and parasitic capacitive effects due to reverse biased junction, (b) Schematic of the octagon shaped Hall effect probe without magnetic field applied.

of bias currents on the right or left sides, $I_{A,R}$ and $I_{A,L}$ in the top half of the probe, in response to the tilting of the equipotential lines. Considering that the structure can be viewed as a composition of two Hall probes, there is a similar unbalance between $I_{B,R}$ and $I_{B,L}$,

$$\begin{aligned} I_A &= I_{A,L} + I_{A,R}, \\ I_B &= I_{B,L} + I_{B,R} \end{aligned} \tag{3.2}$$

Hence, the differential Hall voltage potentials V_A and V_B void of any offset respectively appear across the sense contacts (1, 2) and (3, 4). The bias currents, I_A and I_B are applied equally but act in opposition to each other, causing an equal and opposite sign for the Hall voltage, V_H for probes A and B and a Hall voltage, as shown in Fig 3.2(a):

$$\begin{aligned} V_A &= V_2 - V_1 = V_H, \\ V_B &= V_4 - V_3 = -V_H, \end{aligned} \tag{3.3}$$

Further, if we consider the inhomogeneities of the Hall plate such as the

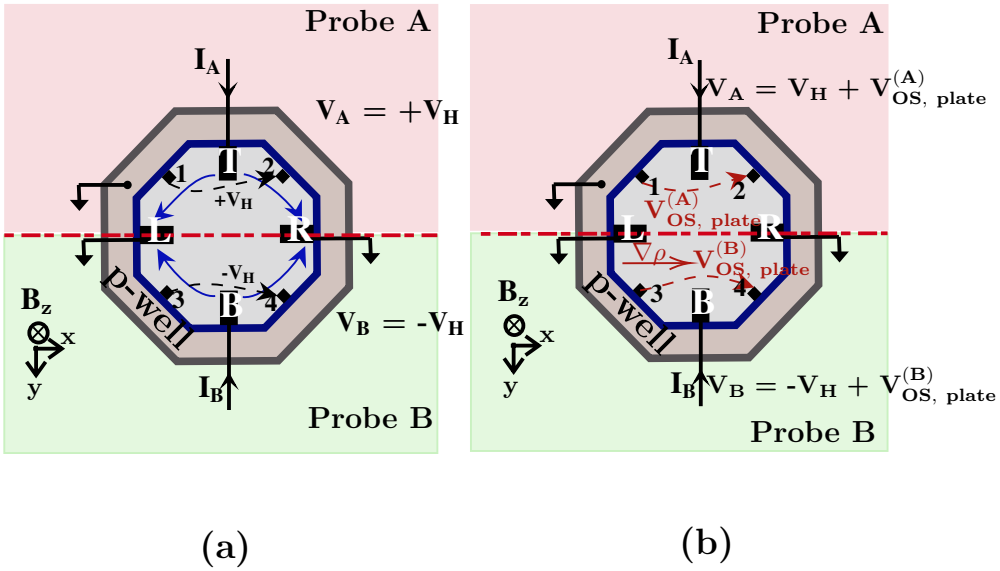


Figure 3.2: (a) Occurance of the differential Hall voltages V_A and V_B void of any offset due to an imbalance of bias currents in the presence of magnetic field, (b) generation of the global offset due to the resistivity gradient adding up to the Hall voltage

resistivity gradient of silicon, $\nabla\rho$, as in Fig.3.2(b), then an offset voltage is generated independent of the magnetic field in each probe and adds to their respective Hall voltages. The magnitude and sign of the offset voltages would be the same if, $\nabla\rho$ is uniform throughout the plate

$$V_A = V_H + V_{OS,plate}^{(A)}, \tag{3.4}$$

$$V_B = -V_H + V_{OS,plate}^{(B)}, \tag{3.5}$$

The two floating output voltages can be processed using two differential amplifiers and a subtractor circuit, cancelling the offset voltages of the plate. However, some imbalances in the offset could occur from various local sources such as an imbalance in the bias currents or any defects at the semiconductor level hence contributing to a residual offset voltage, ΔV_{OS} ,

$$V_A - V_B = 2V_H + \Delta V_{OS}, \tag{3.6}$$

This method however intuitive it may be, makes the implementation of the

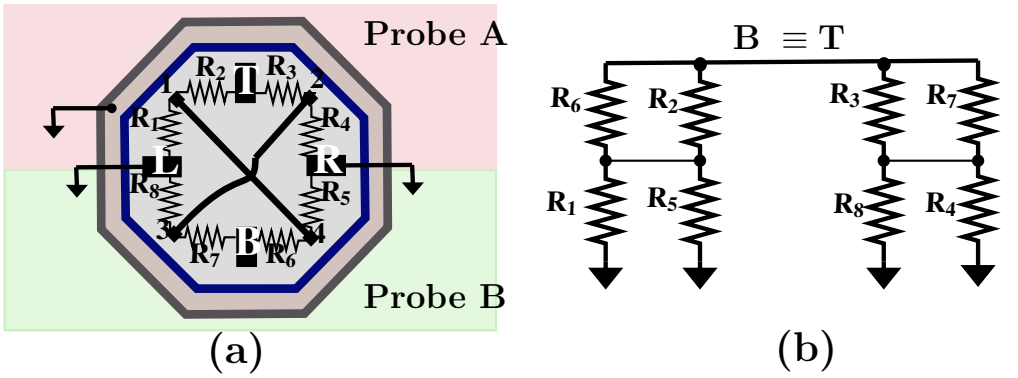


Figure 3.3: (a) Resistive bridge model of the X-Hall probe to illustrate the effects of diagonally short circuiting the sense contacts (b) common centroid connection derived from the resistive bridge model

readout circuitry very complex with a high input capacitance that severely degrades the electronic bandwidth limit. Instead of processing the two floating voltages as discussed in equation 3.6, diagonal shorting of the sense contacts was proposed and this (i) imposes a boundary condition for the net charge distribution within the probe reducing the overall offset contributions to V_A and V_B, (ii) simplifies the electronic readout design, (iii) forces an electrical equality such that the Hall probe output voltage,

$$V_{probe} = V_A = -V_B \tag{3.7}$$

This is better illustrated by the resistive bridge model of the X-Hall probe as shown in Fig.3.3(a). If the applied bias currents are identical, then the potential at the bias terminal B and T are equal and that implies that each resistance modelling a branch of probe A is parallel to the resistance in the opposite branch of probe B in a common centroid architecture as shown in Fig3.3(b). The global offsets are superimposed and perfectly cancelled, however a small non-zero residual offset due to the local defects and non-idealities in bias currents, ΔV_{OS} would add up to the output voltage as,

$$V_{probe} = V_H + \Delta V_{OS} \tag{3.8}$$

The incident magnetic field B_z, which is generated by the current to

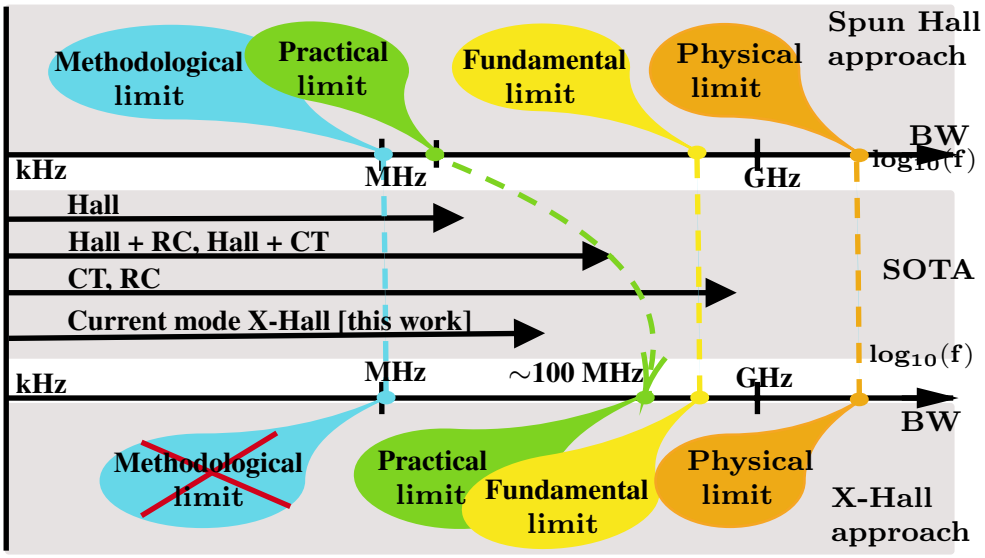


Figure 3.4: Bandwidth limit enhancement provided by the X-Hall architecture compared with spun Hall sensors

be sensed, causes a potential difference V_H that develops across the sense terminals to follow the static formulation:

$$V_H = S_I \cdot I_{bias} \cdot B_z, \tag{3.9}$$

where I_{bias} is the applied bias current and S_I is the current-related sensitivity [10].

Thus, the X-Hall probe architecture as shown in Fig. 3.5 provides a just reduction of the intrinsic offset at the probe level rather than at the sensor level [125] without any additional offset cancellation techniques such as the SCT [126] that would otherwise require switching of bias currents between bias contacts. It replaces the dynamic SCT cancellation with a static offset cancellation apart from significantly simplifying the overall readout architecture in the sensing chain. Eliminating the switches associated to the SCT significantly lowers the total capacitive load seen by the probe and pushes the bandwidth limit at higher frequencies, thus overcoming the methodological limit. Fig.3.4, illustrates the limits for both standard spun Hall sensors and the X-Hall based approach along with the present State of the Art bandwidth for spun Hall, hybrid Hall and the X-Hall based sensors. In conclusion,

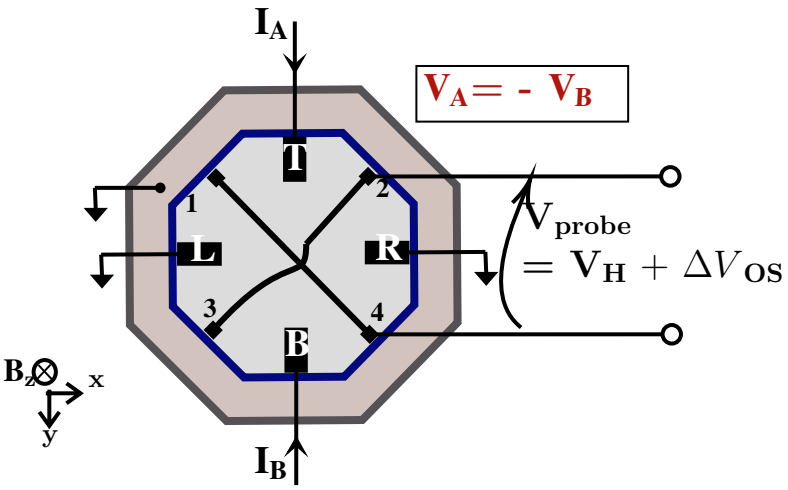


Figure 3.5: Scheme of the X-Hall probe with readout connections

the sensor bandwidth based on the X-Hall architecture would technically be limited to the design of the AFE and potentially could be well competent to achieve bandwidth as high as the hundreds of MHz comparable to the hybrid Hall-coil approaches and the probe can now utilize the maximum achievable bandwidth of the electronic readout circuitry with the input capacitance of the electronic readout circuit being its limit.

3.3 KF94: X-Hall implementation in voltage mode

The first samples of this novel X-Hall probe were implemented in voltage mode using a smart power application compliant Bipolar CMOS DMOS (BCD), 160nm technology from STMicroelectronics as illustrated in Fig.3.6. The device essentially is sensitive to the magnetic field component, B_z and the silicon chip occupied an area of 4 mm^2. The size of the Hall probe is less than 1 mm^2. Static characterization of the probe were performed by using a bias generator to bias the probe at T and B terminals respectively with I_A=I_B=I_{bias} = 500 μA with an output voltage measurement uncertainty of 20 μV. The probe showed a linear response and an estimated current related sensitivity, S_I^V of 165 [V/AT] which stood comparable to the sensitivities of

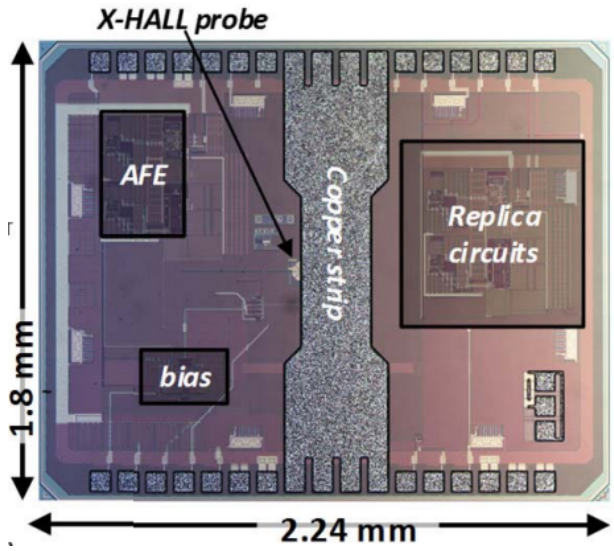


Figure 3.6: Microphotograph of KF94: the X-Hall sensor implemented in voltage mode.

standard Hall effect probes realized with CMOS technology. TCAD simulations of the X-Hall probe reported the resistance between each contact, R = 3.6 kΩ with total probe intrinsic capacitance acting on the sense contacts of a few hundred femtofarads. Further, based on the analysis of prospective technology to realize the sensor (BCD technology) and typical design of readout circuits for probe configurations in voltage mode, lead to an estimated range of input capacitance of the readout circuitry as 600 fF to 800 fF and an acquisition bandwidth greater than 40 MHz. Further discussion related to the characterization of acquisition bandwidth can be found in Section 4.1. The mean residual offset, $\overline{V_{OS}}$ over 20 samples was found to be -0.27 mV and by overcoming the methodological limit, the acquisition bandwidth is just limited by the bandwidth of the Analog Front End (AFE). However, it is more than tens of μV higher than the spun Hall sensors at low frequencies, f_{spin} [124] and as already earlier, the spun Hall sensors suffer degradation in offset reduction at higher frequencies reducing the efficiency of the scheme. Thus, the acquisition bandwidth in the X-Hall can be extended to the electronic limit without offset degradation. The residual offset drift was at a rate of $1\mu V/°C$ over 40 °C range. The HECS configured in voltage mode and powered at 5 V was developed by incorporating the following (refer Fig.

3.8):

(i) A copper strip on the top most metal layer of the chip for current to magnetic field transduction. The strip due to its low resistivity would support a high-value current that could generate the magnetic field to be measured. The trace width and the probe area were chosen to maximize the SNR and input current range of upto 20 A. COMSOL Finite Element Method (FEM) simulations on an emulated model of the strip with a Hall probe placed beneath, estimated a current to magnetic field transduction factor, G_{ib} of 2 mT/A.

(ii) A DDCFA-based readout circuitry that could drive capacitive loads of upto 1 pF and support input capacitance of few hundred femtofarads.

The readout circuitry was designed with the following constraints in perspective, to make the most benefit from the practical bandwidth limit for the X-Hall sensor:

- a high input impedance, Z_{in} such that, ideally a zero current flows into the AFE from the sense terminals of the probe
- a diminished input capacitive load and high GBW
- low residual offset voltage, V_{OS} ideally less than a few microvolts
- high closed loop voltage gain to support a Hall voltage which usually is of the order of a few tens to hundreds of microvolts.

The application targets higher frequencies and demands higher closed loop voltage gain, so a Current Feedback (CFA) architecture was preferred (refer Fig.3.7) for a general architectural perspective) over the Voltage Feedback Architecture (VFA) since they are current operated devices and hence, are not susceptible to the Miller effect caused due to the stray capacitances, which otherwise would cause an abrupt reduction in the open loop gain, A_{OL} at high frequencies. For a non-inverting configuration, the loop gain, $A\beta$ for any VFA inversely incorporates its closed loop gain, A_{CL} as in Eq.3.10 while

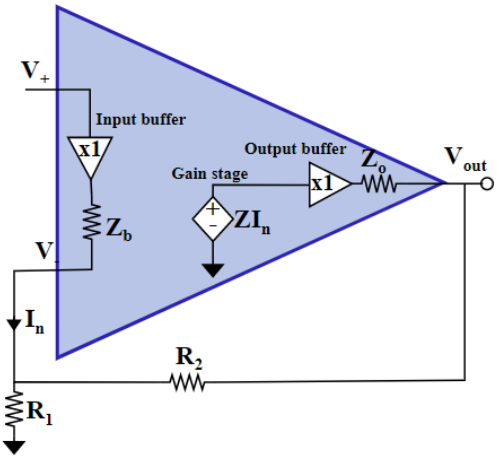


Figure 3.7: Scheme of a Current Feedback Amplifier architecture

it remains independent for a CFA scheme based on the Eq.3.11.

$$A_{CL} = \frac{A_{OL}}{1 + A\beta} \tag{3.10}$$

$$A_{OL}\beta = \frac{Z}{R_2[1 + \frac{R_B}{R_2||R_1}]} \tag{3.11}$$

where A_{OL} is the opamp open loop gain and Z is the transimpedance gain derived from the gain stage of the CFA.

Due to this, the VFAs are often limited to precision and general purpose applications while the CFAs are much useful for high frequency applications above 100 MHz. On the downside, the CFA suffers with high offset and assymetric inputs in terms of impedance. This is because the non-inverting input being the input of a buffer is a high impedance node, while the inverting input is a low impedance node from the output of the buffer and so there is no work around this mismatch. Symmetric design of the two buffers however, can aid in alleviating the problem of offset. The transistor level schematic of the implemented DDCFA is as shown in Fig.3.9. The differential coupled pairs were implemented using 5-V graded MOSFETS with thick gate oxide, while the current mirrors were implemented using 1.8-V graded MOSFETS to enhance the dynamic performance of the amplifier at

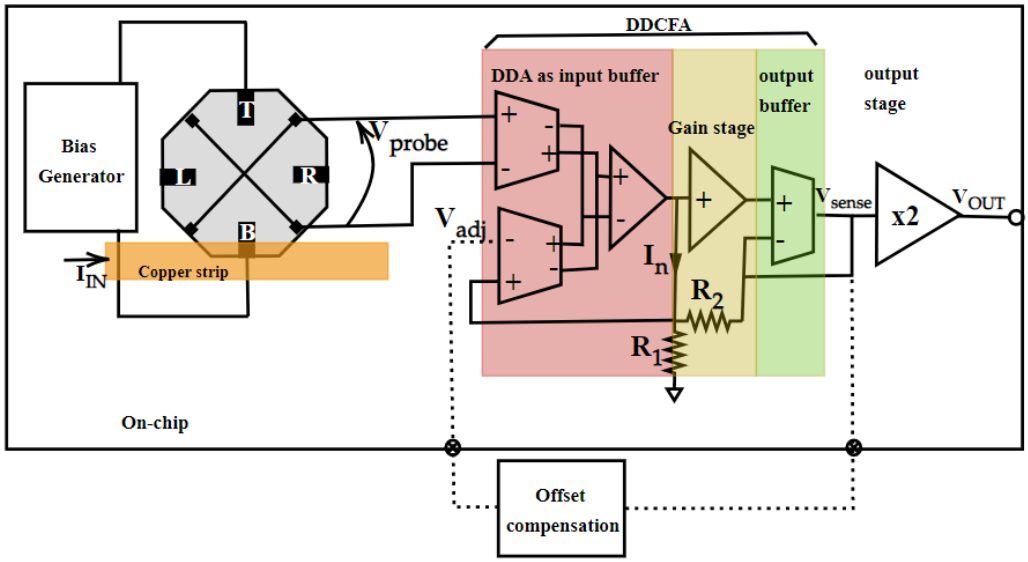


Figure 3.8: X-Hall current sensing system implemented in voltage mode with a DDCFA based Analog Front End depicting an external off-chip offset compensation loop

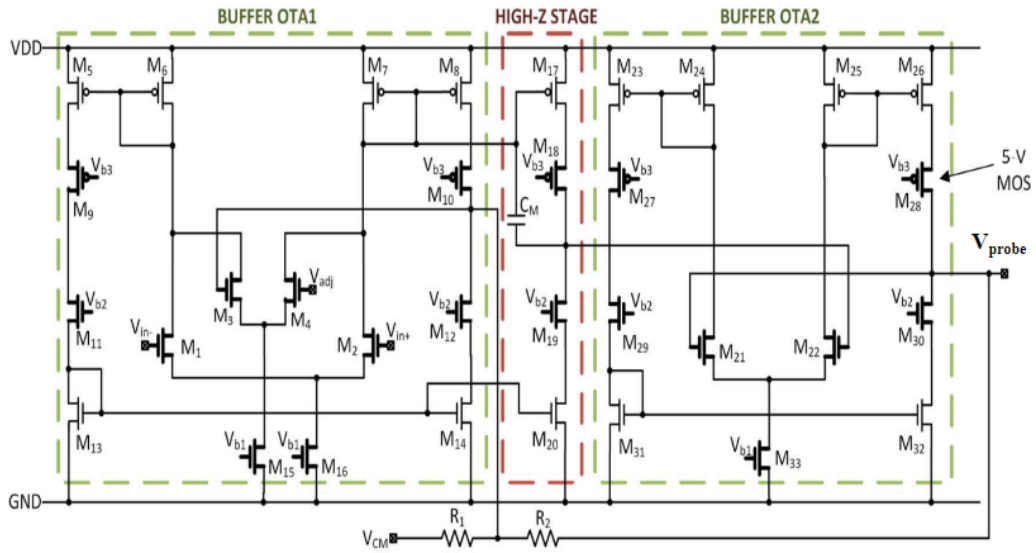


Figure 3.9: Schematic of the DDCFA implemented for the X-Hall current system in voltage mode, [112].

high frequencies. The architecture is designed as single stage, cascode output Operational Transconductance Amplifiers (OTA) in unity gain feedback for a set bandwidth of 65 MHz with a closed loop gain of 35 dB and a minimized

	GAIN				OFFSET				BANDWIDTH		
Input range FS	Current-to-field G_{IB}	AFE G_{ELE}	Hall probe G_H 0.5 mA bias	Nonlin. error	Mean value	Time dispersion over 100 hours	Temp. dispersion [-15°,85°] C	Relative temp. coeff.	AFE sim.	X-Hall Probe sim.	X-Hall sensor meas.
10 A	2 mT/A	100	115 mV/T	<2% FS	0.56 mT 280 mA	0.2 mT 100 mA	11 µT/°C 5.5 mA/°C	0.7 %/°C	65 MHz	200 MHz	4 MHz

Table 3.1: Performance summary of X-Hall sensor configured in voltage mode

total integrated input referred noise power. The cascode architecture allows protection of the lower voltage transistors as the 5 V transistors can pull through high source-drain voltage drops. The output differential voltage of the probe, V_{probe} is amplified through the input buffer OTA1. An additional external input that can be controlled by the user, V_{adj} is applied to OTA1 to compensate the offset of the CFA and the residual offset of the Hall probe. The output buffer stage OTA2 is identical to OTA1 except that it is void of a differential-difference input. Miller capacitance is used for pole-zero cancellation. The transimpedance gain stage of the CFA is designed by mirroring the output current of the OTA1 to a high-impedance node. Another output stage with gain set to 2 is placed after the DDCFA to drive external loads of upto 1 pF.

3.3.1 KF94 prototype issues

The chip was encapsulated in a power small outline (PWSSO) package with a thermal pad exposed for appropriate thermal dissipation and easy testing. A summary of the performance of the X-Hall probe configured in voltage mode is as given in table 3.1. The experimentally estimated transfer function plot of the KF94 prototype is as shown in Fig. 3.10(a)for different values of I_{bias}. It can be observed that the low frequency increases with I_{bias} but at higher frequencies the gain converges and rises by 20 dB/dec due to the parasitic inductive coupling between I_{IN} and power nodes. Packaged RFICs operating beyond hundreds of MHz are usually susceptible to inductive coupling and are defined by high dI/dt values. Although the band of operation for the X-Hall sensor is quite in the sub-range of the RFIC's, the scope of application of the Hall sensors are power circuits that support high ampli-

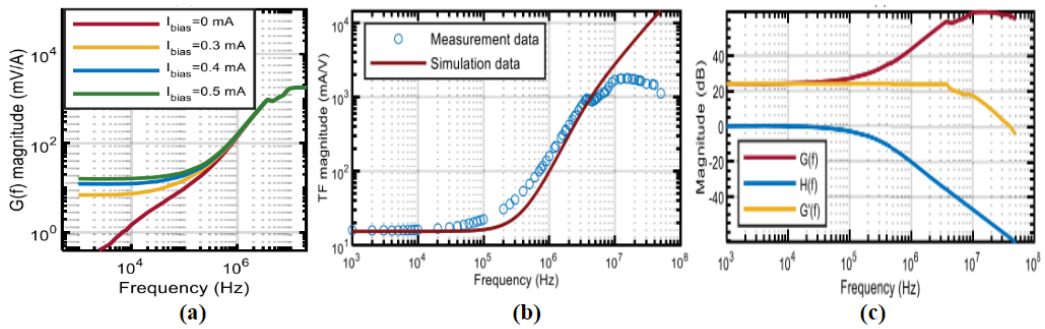


Figure 3.10: (a)Transfer function of the KF94 Hall sensor prototype in voltage mode, (b) Comparison of experimental results with post layout simulation considering the effect of dynamic parasitics of the bondwires using RLC + L models, (c) Transfer function, G'(f) with an acquisition bandwidth of 4 MHz after compensating the dynamic perturbations present in actual transfer function, G(f) using a high pass deemphasis filter with transfer function, H(f), [46]

tudes of I_{IN} and so, usually would be characterized by high dI/dt values, thence making the problem of inductive coupling at package level critical. This reasoning was also verified through comparison of experimental data as shown in Fig.3.10(b), with a post-layout simulation taking into account the self-inductance of package bondwires as 3-nH and mutual inductance of 1.5 nH between adjacent wires. The total estimated stray capacitance adding to the bandwidth limit is approximately between 1 to 3 pF. Hence, the output of the realized prototype assuming the sensor output as purely algebraic in the 20 MHz band can be modelled as :

$$V_{out}(f) = G(f)I_{IN}(f) \tag{3.12}$$

Further, to get a realistic model, the additive dynamic perturbation, $\Delta V(f)$ due to the parasitic effects is included

$$V_{out}(f) = G_0 I_{IN}(f) + \Delta V(f) \tag{3.13}$$

Where, $\Delta V(f) = G\tilde{(f)}I_{IN}(f)$, assuming linearity with respect to I_{IN} was compensated online using a post-deemphasis filter as a low-pass filter with a transfer function, $H(f) = G_0/(G_0 + G\tilde{(f)})$. This allowed real-time com-

pensated acquisition of the X-Hall sensor response, $G'(f) = G(f)H(f) \approx G_0$ in the 20 MHz band. It can be observed post compensation, the sensor can be characterized by an acquisition bandwidth of 4 MHz. Although not quite close to the practical bandwidth limit of the AFE of 65 MHz, it was a breakthrough for a purely semiconductor-based Hall sensor [46, 127].

Having had an insight regarding the potential of the X-Hall probe and a thorough study of the causes of its limitations (inductive coupling and package parasitics) that prevent the bandwidth from reaching the practical limit, it was necessary to vision possible solutions to reach the AFE practical bandwidth limit. The following chapter introduces and proposes a new configuration of the X-Hall sensor in current mode and discusses the validation of the theory and simulations through experimental characterization of the realized prototype.

Chapter 4

CH09: Proposed X-Hall sensor in current mode

Although most conventional applications have usually employed the Hall sensors in voltage mode, what differentiates them from the current mode is the output of the Hall probe to be either a differential voltage or a current. It is also essential that the sensitivity of the sensor and signal-to-noise Ratio (SNR) be high while the offset is minimized with respect to the desired Hall voltage. In contrast to the voltage mode, the current mode of operation provides more favorable conditions in this regard [128] as demonstrated by the state of art [129] [130]. However, an explicit effect on the overall bandwidth of the sensor has not been reported, as their implementation used spinning techniques. An added advantage is that the current-mode operation requires the readout circuits to be based on transimpedance amplifiers (TIA), for example a shunt-feedback TIA is interfaced with the Hall plate as shown in Fig.4.1, which could be faster than conventional readouts based on instrumentation amplifiers, differential-difference amplifiers, etc., thus providing a wider scope of bandwidth improvement. The independent sense contacts 2 and 4 are virtually shorted through the input impedance of the TIA, which should be as low as possible, to allow sinking a large part of the current from the probe and force the potential difference between the contacts to be zero; hence behaving as a dual of the voltage mode. This short circuit avoids the accumulation of charges on the edges of the probe and the creation of the

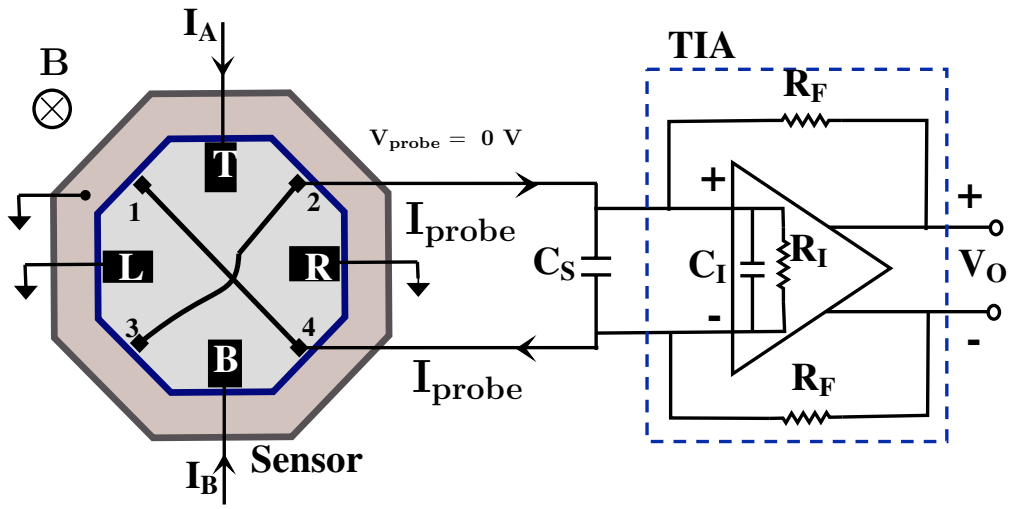


Figure 4.1: X-Hall probe configured in current mode. The Hall voltage is nulled and the current out from the probe is measured using a transimpedance amplifier (TIA).C_S is the output capacitance of the Hall plate, C_I is the intrinsic capacitance of the shunt feedback TIA with feedback resistors, R_F

Hall voltage by constantly sinking/sourcing current at the sense nodes. The imbalance of the current densities in the presence of magnetic field results in a current through the sense terminals,

$$I_{probe} = I_H + \Delta I_{OS} \tag{4.1}$$

where I_H is the Hall current and ΔI_{OS} is the residual current offset. This modality allows to overcome the bandwidth limit set by the capacitive load of the AFE by lowering the impedance value associated to the node and the relative time constant. The inherent output capacitance of the plate C_S sums up with the input capacitance of the TIA, C_I and the stray capacitances of the interconnects, which makes up the total capacitance at the input node, C_T that could be several pF. The equivalent resistance at that node is mainly defined by the low input resistance, R_I of the TIA, which is given by

$$R_I = \frac{2R_F}{A_{OL}}, \tag{4.2}$$

where R_F is the feedback resistance of the TIA and A_{OL} is the open-loop gain of the operational amplifier. The following section works out to theoretically

assess the feasibility of realizing the X-Hall sensor in current mode through a balanced comparison of the KF94 performance metrics.

4.1 Theoretical validation

Prior to proceeding with the comparison between the voltage and the current modes mode of operation, it is important to highlight that the current-related sensitivity of the Hall sensor operated in current mode is different from that of the one operated in the voltage mode and they are not comparable. The two sensitivities can be respectively expressed as [131]:

$$S_I^I = \frac{I_{probe}}{I_{bias} B_z} \qquad [T^{-1}], \tag{4.3}$$

$$S_I^V = \frac{V_{probe}}{I_{bias} B_z} \qquad [V/AT] \tag{4.4}$$

Table 4.1 compares the performance of the the X-Hall probe in voltage mode and in current mode at different biasing current values of 500 μA and 1 mA . The performance values reported for the voltage mode have already been measured from a previous study [46] and the performance of the X-Hall probe in the proposed current mode is first speculated theoretically by following an assumption strategy for its unknown sensitivity to be 1% $[T^{-1}]$, 2% $[T^{-1}]$ or higher and later estimated and verified with a TCAD simulation. The sensitivity of the probe in voltage mode is 250 V/AT. The calculations considered constant parameters: the Boltzmann's constant $K = 1.38 \times 10^{-23} J/K$, absolute temperature, T = 300 K, X-Hall resistance referring to the Wheatstone's bridge model = 3 kΩ [46]. A practical bandwidth limit of 10 MHz, which is higher than that achieved by the KF94 chip was targetted for the electronic front end is also taken into consideration. This not only would align the sensor for power applications but a higher bandwidth also implies a reduced integrated input referred noise in the concerned frequency band at the probe

Parameters	Notation	Voltage mode		Current mode							
Current related Sensitivity	S_I^V (V/AT) or S_I^I (T^{-1})	250		1%		2%		4%		6%	
Bias current	I_{bias} (mA)	0.5	1	0.5	1	0.5	1	0.5	1	0.5	1
rms noise referred to magnetic input of Hall probe	B_{in} (mT_{rms})	0.18	0.09	0.74	0.37	0.37	0.19	0.19	0.09	0.12	0.06
Total noise referred to the input current	i_{in_tot} (mA_{rms})	31.78	15.89	108.96	54.48	54.48	27.24	27.24	13.62	18.16	9.08
Maximum measurable magnetic field	$B_{\_max}$ (mT)	96	48	600	300	300	150	150	75	100	50
Maximum measurable current that generates the input magnetic field	$I_{\_max}$ (A)	12	6	75	37.5	37.5	18.75	18.75	9.38	12.5	6.25
Max SNR	DR (dB)	51.54		56.76							

Table 4.1: Performance: Voltage mode versus current mode

- AFE interface following the relation:

$$I_{n_{min}} = \sqrt{\frac{4KT}{G_{ELE}BW}} \tag{4.5}$$

A higher current to magnetic field transduction factor was also aimed at, since it greatly impacts the sensitivity of the system as well as is inversely proportional to the total integrated noise referred to the main current input of the sensor in the selected bandwidth range. Further, to choose the best shape for the current-carrying strip, FEM simulation was done using COMSOL, emulating with accuracy, the geometry of the probe and with the input current-carrying strip curved and shaped to resemble a coil to improve the transduction as shown in Fig.4.2 in contrast to that of the KF94 chip. The simulation resulted in a current to magnetic transduction factor, G_{IB} of 7.5 mT/A. With all these set parameters, it can be observed from the table that if the current-related sensitivity is at 4% T^{-1} or higher, the current mode shows a substantial improvement in performance over the voltage mode in terms of the total noise, i_{in_tot} referred to the input current on the strip that generates the magnetic field. A 56% raise in the maximum measurable magnetic field, $B_{\_max}$ for the current mode is also evident. A remarkable improvement can be noted for the maximum measurable magnetic field, $B_{\_max}$

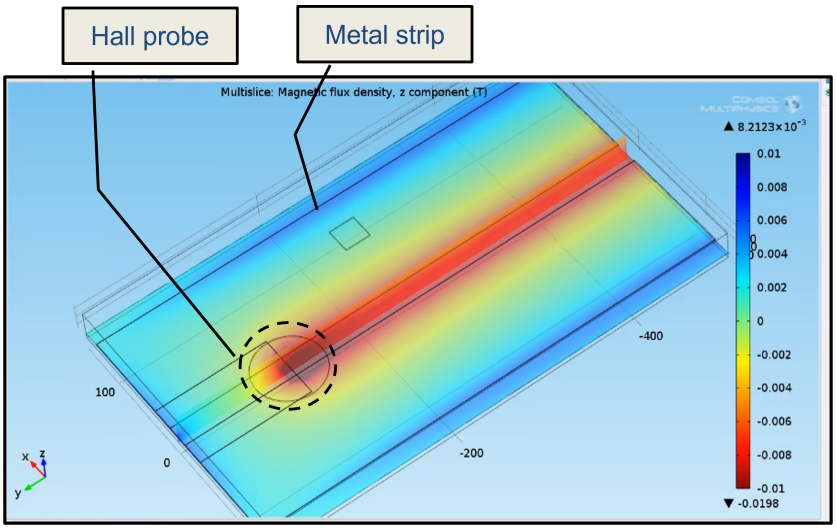


Figure 4.2: FEM simulation: The distance between the strip and the probe is 2.771 μm and the trace width = 100 μm.

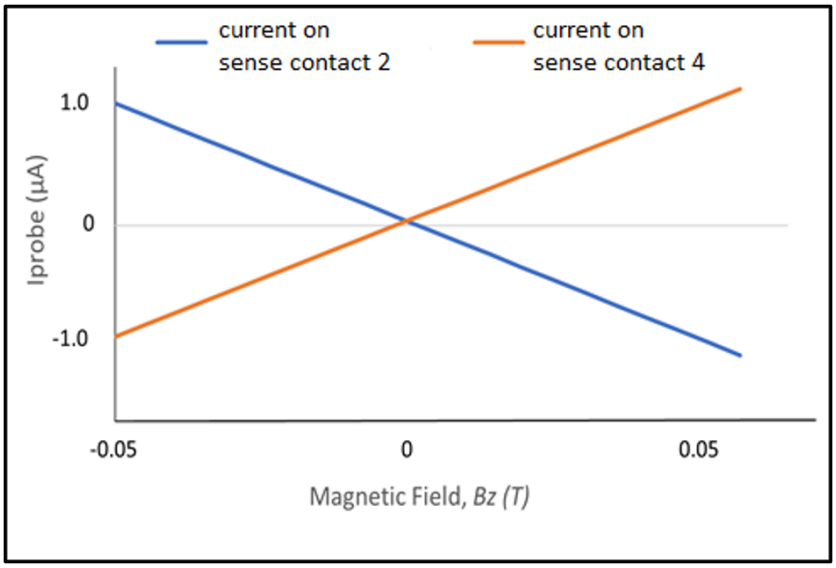


Figure 4.3: TCAD simulation plot for current mode configuration: magnetic induction versus I_{probe}

that evaluates to 150 mT and 75 mT for I_{bias}, 0.5 mA and 1 mA respectively, while it is only 96 mT and 48 mT in the voltage mode for the same values of biasing current. However, a slight improvement in the dynamic range (DR) of current mode can be expected over the voltage mode.

A TCAD simulation was carried out for the X-Hall probe configured in

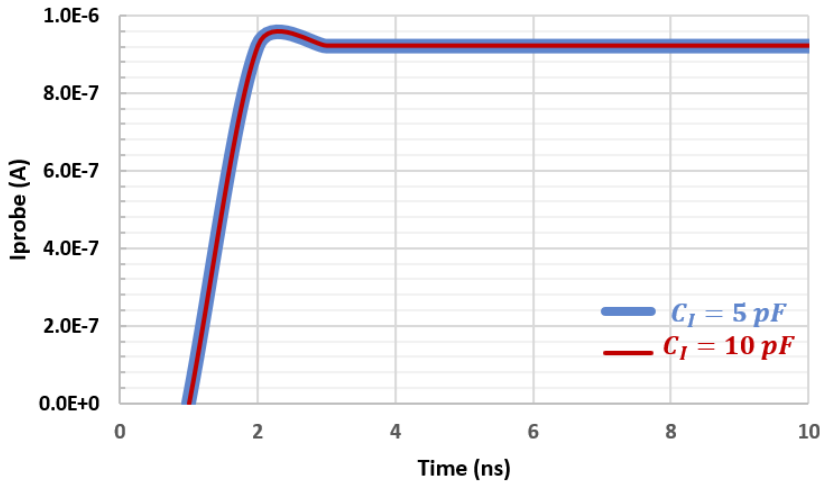


Figure 4.4: Time response of X-Hall probe in current mode to a magnetic field step stimulus of 50 mT at t = 0 s and biased at 500μA.)

current mode to estimate its sensitivity and relate to our theoretical analysis. A bias current of 500 μA and magnetic induction of 50 mT was applied to obtain a maximum output differential current, I_{probe} of 1 μA as in Fig.4.3. The slope of the graph is calculated to be 20 $\mu A/T$ and using these results in Eq.4.3, a relative sensitivity of 4% T^{-1} is obtained. Similarly, a bias current of 1-mA, resulted in a maximum differential current I_{probe} of 3 μA and a relative sensitivity of 6% T^{-1}. This result proves the suitability of the X-Hall probe to be implemented in current mode. We consider that this modality of operating the sensor in current mode, allows to overcome the bandwidth limit set by the capacitive load of the AFE by lowering the impedance value associated to the node and the relative time constant. To verify this, another TCAD simulation of the probe, considering equivalent resistance of the probe R =3 $k\Omega$ and C_S=0.7 pF [56], working in the current mode interfaced with an ideal TIA model with input capacitance of 5 pF and 10 pF, demonstrates the possibility to achieve a bandwidth greater than 200 MHz (Fig. 4.4). This gives a time constant of about $\tau = 2$ ns in both cases, highlighting the negligible impact of the self-loading capacitance of the probe in the current-mode.

4.2 CH09: Proposed architecture

This work proposes to implement a dual-supply prototype of the sensing system in 90-nm BCD technology by interfacing a 5-V powered X-Hall sensor operated in current mode with a dedicated readout circuitry based on a self-biased transimpedance amplifier (TIA) powered at 1.2 V. To the best of the author's knowledge, this would be the first implementation of an integrated Hall sensor in current mode without any spinning technique, while being compliant with the bandwidth criteria in the MHz range. With the goal of using the current sensor for power electronic applications such as DC-DC converters, tables 4.2 and 4.3 summarize the specifications targeted for its microelectronic design. The usage of low-voltage sub-micron technology grants high transition frequency and hence wide operating bandwidth. The common-mode voltage control at the probe - AFE interface controls the voltage at the output terminals of the Hall probe such that it is never more than 1.2 V, hence it is compatible with the AFE without any voltage shifting circuitry. An on-chip copper track is used to generate the magnetic field incident on the X-Hall probe. The probe, operated in current mode, generates a Hall current, I_{probe} instead of the Hall voltage, which is applied to a tunable-gain TIA to generate a wideband differential voltage at the output. Self-biasing operational amplifier (op-amp) architecture offers many advantages in terms of stability against Process Temperature Variations (PVT), lower area, and power consumption [132]. The choice of the resistive TIA architecture combined with the self-biasing scheme offers the AFE a high acquisition bandwidth, low current consumption, and minimal area as no additional biasing circuitry is required.

The architecture of the complete broadband current sensor is illustrated in Fig. 4.5. A detailed description of the main subsystems will follow. The dc sensitivity of the system, G_0 is based on the model,

$$G_0 = G_{ib} G_H G_{ELE} \tag{4.6}$$

where the multiplication terms are the current-magnetic field transduction factor, the gain of the probe, and the gain of the electronic front end,

Table 4.2: Current sensor specifications

Parameter	Specification
Power supply	±2.5 V, ±0.6 V
Minimum Detectable signal, MDS	5 mA
Input current, I_{IN}	5 A
Bandwidth, BW	10 MHz
Total current consumption	$<$ 10 mA
Signal to Noise ratio, SNR	$\approx$ 60 dB
Insensitivity to external magnetic interferences	maximum possible

Table 4.3: TIA specifications

Parameter	Specification
Power supply	±0.6 V
Input impedance, Z_{in}	$<$ 300 Ω
Open loop gain, A_{OL}	$>$ 50 dB
Minimum transimpedance, R_T	$>$ 80 kΩ
Power consumption	$<$ 2.5 mW
Bandwidth, BW	50 MHz (for C_L = 100 fF)
Output voltage swing	$>$ ± 300 mV
Variation of gain, BW and noise (Temperature range: -20 degC to 100 degC	± 1 %
Integrated input referred noise at probe-AFE interface (DC-10 MHz), I_{nmin}	$<$ 2 nA_{rms}

respectively.

4.2.1 I-B Transducer

The transduction of the current into a magnetic field incident on the Hall probe is realized by the flow of the input current I_{IN} through an on-chip 174-μm-wide metal path shaped as an 'S' and realized on the top copper layer. The copper track can conduct a DC or rms power current up to 3 A according to the electromigration prevention rules. The shape was chosen so that the copper track focuses the transduced magnetic field on the Hall probes, thus supporting a higher transduction factor G_{ib}. Finite-element method (FEM) simulations of a simplified model of the copper layer reported an estimated G_{ib} of 7.5 mT/A. This is an improvement over the previous design of the KF94 chip bearing a straight metal strip, which had G_{ib} = 2 mT/A. Two

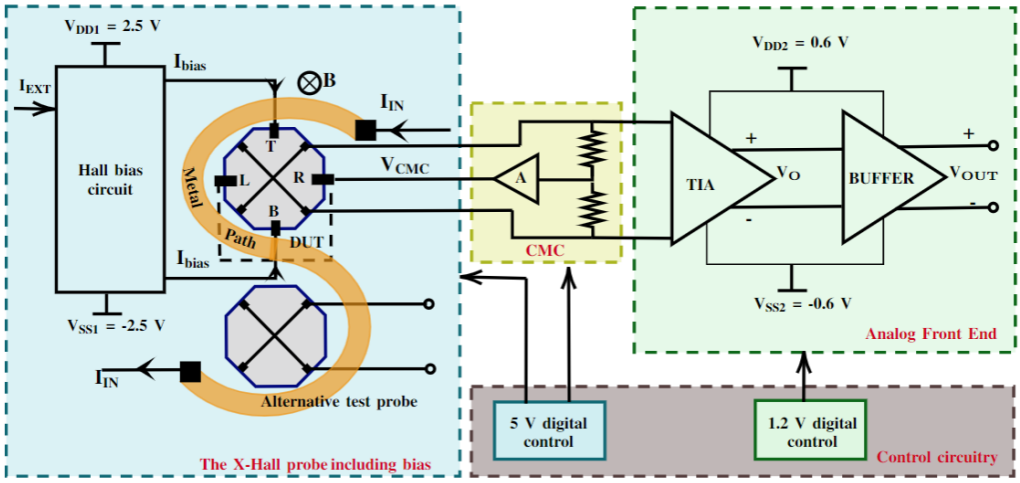


Figure 4.5: Block scheme of the proposed X-Hall sensing system in current mode)

X-Hall probes are placed in between the curvatures of the metal trace. One probe is connected to the TIA while the second one is used for testing

4.2.2 X-Hall probe

The probe is realized in BCD technology as an octagon shape. The active layer is made by using a low-doped n-well typically used for high-voltage devices. Sensing contacts are smaller than bias contacts to minimize parasitic capacitances and increase sensitivity. The physical area occupied by each Hall probe is 7.8 μm^2. When biased, the probe is contemporarily excited in four orthogonal directions, keeping a uniform current density distribution within the active region. The sensor is biased by two 1-mA currents applied at two opposite bias contacts (Fig. 4.5).

4.2.3 Common mode control

Regardless of the operation of the X-Hall in either voltage or current mode, the transduction gain of the Hall plate is proportional to I_{bias}, as shown in equation 3.9 following the static formulation of the development of the Hall voltage. Then, higher bias currents and voltages are beneficial to improve the sensitivity of the sensor, implying the connection of the Hall

plate to a rather high voltage supply (e.g, 5-V supply). On the contrary, the TIA would benefit from the exploitation of low-threshold transistors at low voltage supply (e.g, 1.2-V supply) to achieve wider bandwidth, leveraging the higher transition frequency. This creates an interfacing problem at the AFE input side since it should work with input common-mode (CM) voltage levels higher than its supply voltage. Moreover, the X-Hall probe is DC biased by two currents that may be different from the nominal value or can drift apart in response to temperature variations, altering the output CM voltage of the probe during operation.

To cope with these problems, the sensor system has two different dual supplies with a common ground and a CM feedback is implemented to force the CM output voltage of the Hall plate to ground. The principle of the feedback system is reported in Fig.4.6. The error between the X-Hall CM output voltage and ground is nulled by the feedback amplifier, which drives the two opposite bias contacts that should be connected to a low impedance node. In this way, the voltage bias across the Hall plate, with equivalent resistance R, is adjusted so that the CM output voltage is ideally nulled for an amplifier with infinite open loop gain A, following the equation:

$$V_{CM} = \frac{RI_{bias}}{1 + A}. \tag{4.7}$$

The Common Mode voltage Control (CMC) block in CH09, computes the CM voltage by using a resistive divider network placed at the interface of the X-Hall probe with the AFE. The computed CM voltage is then negatively fed back to the L and R bias terminals of the X-Hall probe by using an operational amplifier. This feedback forces the output of the X-Hall probe to always work around the common ground, satisfying the CM input voltage range criteria of the TIA. The CMC circuit also improves the stability performance since the X-Hall is forced to work with a mid-voltage fixed to ground. The feedback amplifier operates at an open-loop gain of 37 dB and with bandwidth limited to a few kHz.

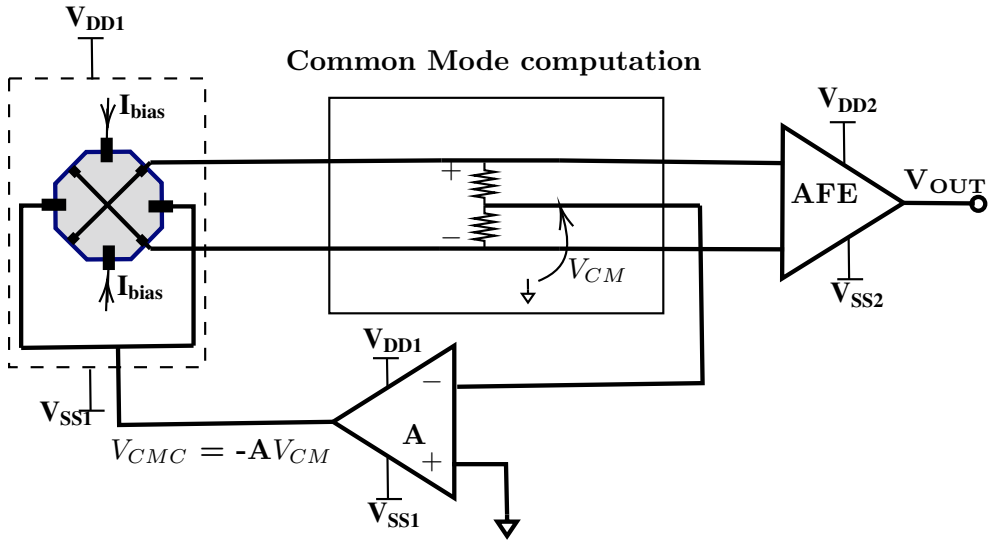


Figure 4.6: Scheme of the common mode voltage control loop

4.2.4 Analog Front End

The X-Hall probe operating in current mode must be interfaced with a fully differential transimpedance amplifier for high performance. In contrast to the DDCFA requirements for a voltage mode X-Hall probe interface, the TIA must ensure i) a very low input impedance compared to that of the Hall probe, so that the majority of the the output current I_{probe} sinks into the TIA, which in turn translates into a high open-loop voltage gain of at least 50 dB; ii) transimpedance gain of around 100 kΩ to obtain optimal SNR and a minimum detectable signal of at least 5 mA; iii) high acquisition bandwidth (in MHz) for capacitive loads up to 5 pF. Low power consumption along with a wide output swing and stability with respect to temperature and process variations are some of the other desirable features that would boost the performance of the integrated Hall sensing system.

To cope with the above challenges, we have designed a self-biased two-stage, fully-complementary push-pull inverter-based transimpedance amplifier (Fig. 4.7), using 1.2-V, 90-nm microelectronic process from STMicroelectronics. What is appealing of this architecture is that it consumes minimal power of only 0.4 mW and area of less than 0.4 mm^2, whilst coping with the target specifications and achieving a very high gain bandwidth product

(GBW) of 30 GHz. The two stages are identical and so the differential gain is doubled at the output of the second stage. It follows a self-biasing scheme for a fully differential amplifier [132–134] and so does not require any additional biasing circuitry, hence minimizing the utilization area. It is also purely symmetrical in terms of architecture. In order for the circuit to be biased in a stable fashion, the currents through devices PTx and NTx, must be identical. Any difference in currents through these two devices would result in extreme shifts in amplifier bias voltages. Tying the gate voltages of the bias transistors to an internal node voltages, V_{bias1} and V_{bias2} creates a self bias and a negative feedback loop, thus stabilizing the bias voltages within the dashed region of Fig. 4.7. The stabilized node voltages V_{bias1} and V_{bias2} are responsible to control the bias and attenuate any variations. The TIA employs a resistive feedback architecture and so the transimpedance gain [135] of the amplifier is set by the feedback resistance, R_F used as per the formulation:

$$R_T = \frac{A_{OL}}{A_{OL}+1}(R_F) \tag{4.8}$$

The open loop gain, A_{OL} does not significantly affect the transimpedance gain, but on the contrary, a high value would lower the input resistance of the TIA based on the relation,

$$R_T = \frac{2R_F}{A_{OL}} \tag{4.9}$$

which is quite a necessary requirement in the present application, to sink majority of the current from the X-Hall probe. The two-stage open loop gain achieved is 70 dB and the transimpedance gain can be set to 106 dBΩ and 99.2 dBΩ by switching the values of the feedback resistors to 90 kΩ and 200 kΩ respectively. The overall transimpedance limit is 27.6 MΩ. The transimpedance limit [135] refers to the maximum DC transimpedance the TIA can reach for a given bandwidth and is expressed as:

$$R_T \leq \frac{GBW}{2\pi C_T (BW)^2} \tag{4.10}$$

where C_T is the total input capacitance at the input of the amplifier. It

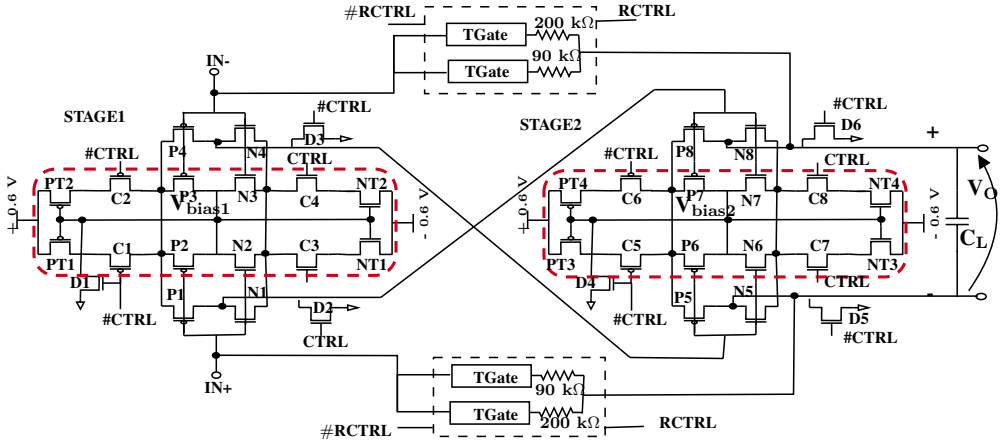


Figure 4.7: Schematic diagram of a two-stage self biased TIA

can be observed that the limit is controlled by the parameter, GBW/C_T and the transimpedance also degrades with the square of the bandwidth, BW [3] Due to a high open-loop gain, the input impedance is as low as 65 Ohms and nearly 50 times lower than the Hall probe resistance of 3 kΩ thus allowing maximum sinking of the current from the Hall plate into the AFE and reducing the effect of the parasitic capacitances. The transistors are sized quite small and are designed to achieve a maximum and minimum acquisition bandwidth conditional to the feedback resistor used (90 kΩ or 200 kΩ) in the TIA for a load capacitance C_L of 100 fF as 45 MHz and 28.3 MHz respectively. A rail-to-rail output swing is achieved with a current consumption of only 120 μA which is due to the fact that the biasing tail transistors: PTx and NTx of the two stages operate in the linear region. The transistors Cx act as switches and are driven by control signals that enable the amplifier to turn on or off. When the CTRL signals are low, the switches are open and the TIA is no longer functional. Any residual currents within the circuit are then sunk to ground through transistors Dx. The architecture also does not need additional compensation for stability and has a phase margin of 51 degrees for a transimpedance gain of 106 dBΩ and close to 45 degrees for a transimpedance gain of 99.2 dBΩ. The main drawback of this architecture is its reduced input common-mode range, however this issue is solved by the CMC block that set the input CM voltage of the TIA to ground

Table 4.4: Transistor sizing of the TIA

Transistor	Feature size, W/L (μ)
PT1, PT2,PT3, PT4	20/1
C1, C2, C5, C6	46.66/0.5
P1 - P8	12/1
N1 - N8	7/1
C3, C4, C7, C8	50/1
NT1, NT2, NT3, NT4	5/1
D1 - D6	10/0.5

Noise contributor at the probe – AFE interface	Integrated input referred noise at probe-AFE interface (DC – 10 MHz)	Contributing factors
TIA	20.7 nA_{rms}	*Probe – TIA interface transistors: drain-source thermal noise = 36.4%* *Flicker noise = 16.4 %* *R_F thermal noise = 0.18%*
Hall probe + current to magnetic field transducer	10.5 nA_{rms}	Thermal noise = 46.4%
Output buffer	0.85 nA_{rms}	Resistor thermal noise = 0.12%
Common mode control (CMC)	0.52 fA_{rms}	*≈0.5%*
Hall bias circuitry	0.52 fA_{rms}	
5-V current reference generator for Hall bias circuitry and CMC	0.52 fA_{rms}	
Full system	23.28 nA_{rms}	*100%*

Table 4.5: CH09 sub-module noise contributions at the X-Hall probe - AFE interface

and limits its variations. The TIA is followed by another self-biased single-stage buffer in order to support the system in handling a load up to 5 pF. However, this last stage limits the overall bandwidth of the AFE to about 12 MHz, depending on the highest capacitive load connected to the output.

4.3 Preliminary results

Preliminary tests through simulations show that the sensitivity of the X-Hall probe configured in current mode is 6% $[T^{-1}]$ for a bias current of 1-mA. The TIA architecture is application specific and not suitable for generalized use as it has a narrow input common mode range (-40, +40 mV) as shown in

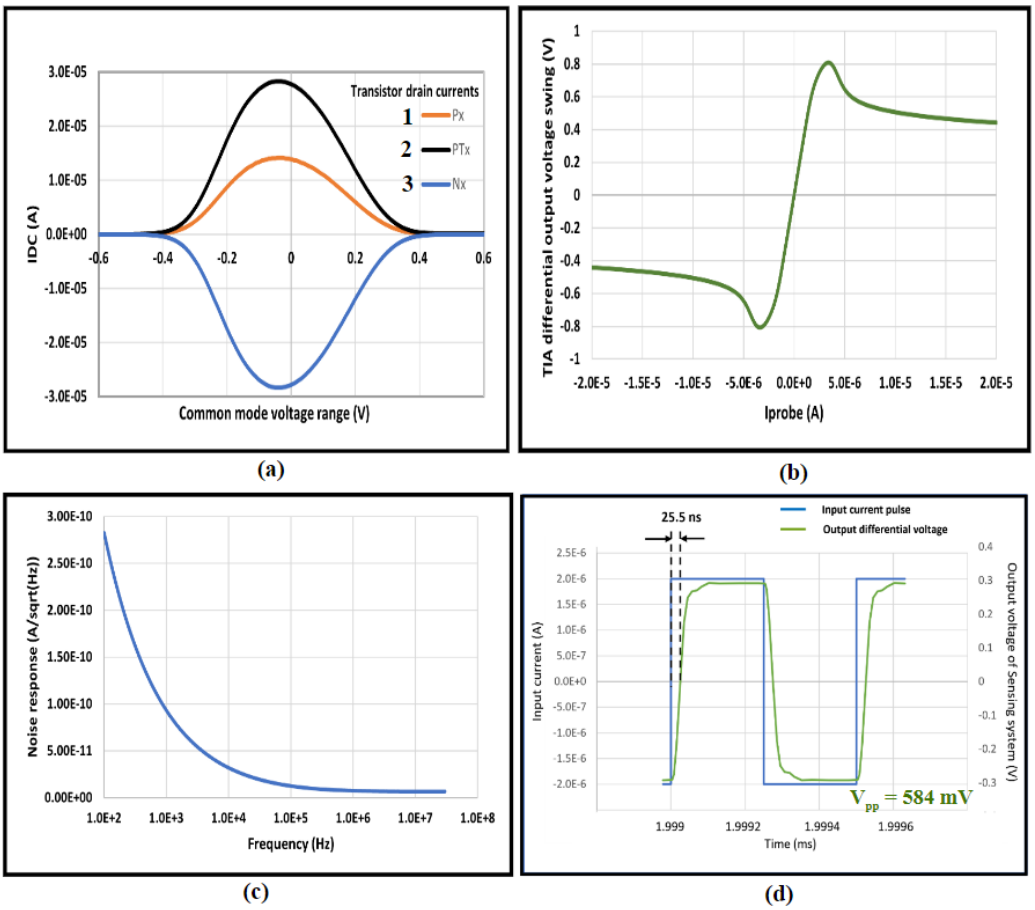


Figure 4.8: Simulation results of the X-Hall sensor prototype operating in current mode (a) Input common mode voltage range of the AFE; (b) Differential output voltage swing of the TIA; (c) Equivalent input referred noise - referred to the probe at a bandwidth limit of 10 MHz; (d) Transient response of the system

Fig. 4.8(a) where curves: 1 and 3 are the dc bias currents through the bias transistors, PTx and NTx swept across an input common mode voltage range, while curve 2 illustrates the splitting of the tail biasing currents through the branches of TIA flowing as drain currents of Px and Nx. It can be seen that the tail biasing currents remain constant at very narrow range of input common mode voltage. However, we have coped with this issue by controlling and setting the common mode at the interface of the X-Hall probe and the TIA as shown in Fig.4.5. A rail-to-rail output swing is achieved by the implemented TIA as shown in Fig. 4.8(b). A plot of equivalent input referred

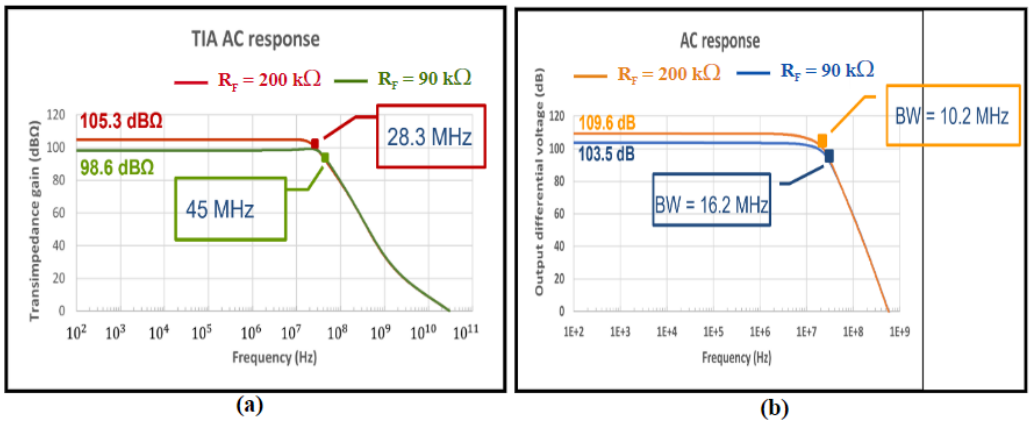


Figure 4.9: Simulated AC response of the (a) TIA (b) X-Hall sensor operating in current mode

noise at the probe being 6.59 pA/$\sqrt{Hz}$ at 10 MHz is shown in Fig.4.8(c). The total input referred noise in a bandwidth of 10 MHz is 23.34 nA_{rms}, considering all the sources of noise of the sensing system, from the Hall probe to the AFE. The individual sub-module noise contributions in their decreasing order are listed in the table 4.5. [1] From the perspective of a stand-alone AFE, the input-referred noise in 10 MHz bandwidth is 13.07 nA_{rms}. We can also calculate the rms integrated noise contributed by the TIA alone in this frequency band from the difference between the noise powers of the total system and that of the TIA as $\sqrt{(23 \times 10^{-9})^2 - (20 \times 10^{-9})^2}$ to obtain 11 nA_{rms} which is also coherent with our simulated result for a standalone TIA. Fig.4.8(d) illustrates the transient response of the sensing system to a sharp current pulse edge of 250 ns with a response time of 25.5 ns, while for a standalone TIA the delay in the response is 10 ns. Fig. 4.9(a) highlights the simulated acquisition bandwidth of the TIA of 28.3 MHz and 45 MHz for the two values of feedback resistances, R_F of 200 kΩ and 90 kΩ for $C_L = 100$ fF while the complete system AC response respectively is 10.2 MHz and 16.2 MHz to a capacitive load of 5 pF. The gain bandwidth is 746 MHz and the system is stable without compensation with a phase margin of 51 degrees. It

[1] **Note:** The noise model of the Hall probe in the simulation is not accurate as it is modelled as a pure resistor and therefore presents only the thermal noise, while the flicker noise is not considered. The latter however will be present during experimental testing.

Table 4.6: Performance summary of the transimpedance amplifier at R_F = 200 kΩ

Parameter	Value
Voltage supply	1.2 V
Current consumption	110.2 μA
Open loop gain	69.7 dB
Transimpedance limit	27.669 MΩ
Transimpedance gain	105.34 dBΩ
-3 dB bandwidth	28.3 MHz
GBW	30 GHz
Phase margin	51.71°
Common mode input range	-150 mV to 50 mV
Output swing	-600 mV to +600 mV
R_I	65.46 Ω
Input referred integrated noise (100 Hz - 10 MHz)	11 nA_{rms}

is also possible to achieve higher bandwidth by lowering the transimpedance gain of the TIA to not less than 100 kΩ. Although this is not so desirable, the performance can be enhanced by trading off with power consumption satisfactorily by increasing the size of the transistors in the TIA. By doing so, the power consumption would still be times lower than the state of art. Table 4.6 summarizes the performance of the TIA.

4.4 Experimental characterization

The X-Hall current sensing system in current mode was implemented using a 90-nm BCD technology provided by STMicroelectronics on a total chip area of 2.39 mm^2 with the active area occupied by the submodules being only 0.578 mm^2 (Fig. 4.10(a)). The measured power consumption of the X-Hall probe is 10.98 mW and that of the AFE is only 0.4 mW. The bare die is bonded on the PCB with staggered leads and using a conductive glue to provide a better ground connection of the back contact to the substrate (Fig. 4.10(b)). A special consideration was taken to minimize the length of the bond wires used to convey the input current and, at the same time, maximize the distance from all the other bond wires. This was done in an effort to minimize the parasitic inductance between the wires that limits the dynamic performance of the sensors [46]. However, due to issues during the assembly

process related to the properties of bonding wires, the prototype is limited to a maximum current of 800 mA, although the metal path inside the chip can handle up to 3 A. This limitation can be easily handled in the future by using thicker bond wires or moving to other packaging techniques like solder bumps.

4.4.1 Static characterization

The characterization of the static response was carried out with the setup indicated in Fig.4.11. A Keysight E3633A DC power supply connected through a 5-Ω, 35-W power resistor was used to generate the input current through the metal path inside the chip. The applied input current is accurately measured using a Tektronix TCPA300 current probe together with a Rohde & Schwartz RTM3004 scope. The sensor output voltage is measured using a Keysight CX1105A differential probe and a CX3324A waveform analyzer. The prototype does not incorporate a temperature compensation mechanism, which is quite standard [34], thus the input current was applied in bursts of 7 s while simultaneously monitoring the temperature over the

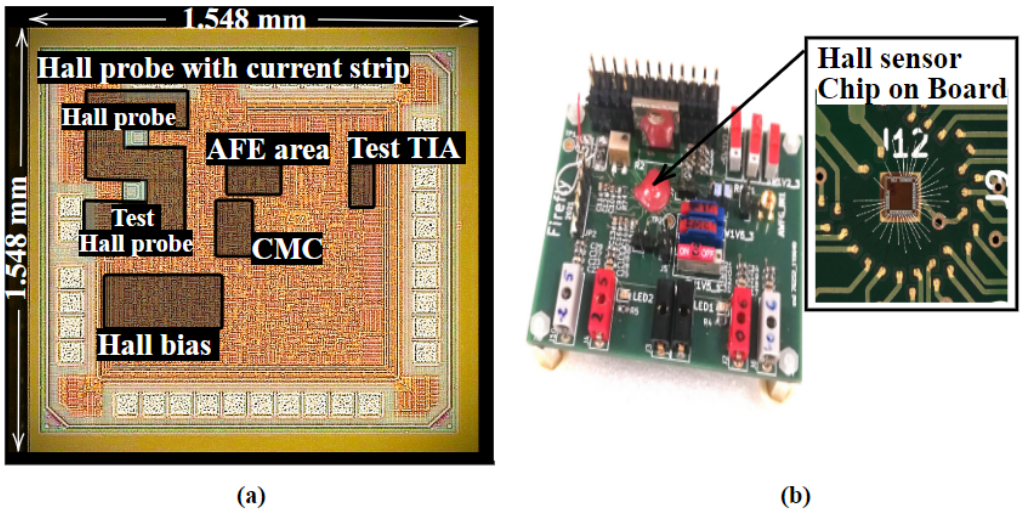


Figure 4.10: (a)Chip microphotograph of the X-Hall sensor IC, (b)Picture of the test board developed for characterizing the X-Hall sensor IC with a magnification of the chip-on-board bonding solution.

chip surface to avoid overheating of the sensor with sufficient cool-down time between each measurement. The output voltage was acquired at 16-bit resolution and low sampling rate, and the DC value was estimated by averaging all the samples over a single 7-s-long acquisition. The results of the static characterization are reported in Fig. 4.12 for the X-Hall probe internally biased at I_{bias} = 1.05 mA and R_F values of 90 kΩ and 200 kΩ, yielding a DC sensitivity of the entire system G_0 = 62.7 mV/A and 120.1 mV/A, respectively. The non-linearity error (NLE) is computed for a full-scale range of ±3 A and is about 2.6%FS and 2.2%FS for the R_F of 90 kΩ and 200 kΩ, respectively over the measured range (Fig. 4.12). The NLE is almost close to the real-time application requirement of 1%FS and is an optimistic underestimate of the real value as the sensor could not be excited to its full scale.

Furthermore, if we assume that G_{ib} is aligned to the simulation value of 7.5 mT/A, the practical values achieved of G_0 correspond to a mean current-related sensitivity, S_{I_I} of 8.6% T^{-1} with the variability accounting to an exact value of R_F of 90 kΩ or 200 kΩ. The achieved S_{I_I} is greater than the stated sensitivity of 6.86 % T^{-1} for a cross shaped Hall sensing system in current mode [136]. Finally, the gain spread of the system across the temperature range was experimentally evaluated as in Fig. 4.13 and it is found to be around ±4 dB over the entire temperature range. Note that a temperature compensation circuit is usually implemented in state-of-the-art Hall sensors and since, the main focus of this prototype was to demonstrate bandwidth enhancement, it overlooked this aspect and therefore, has no analog temperature compensation.

4.4.2 Offset

The nominal input referred offset of the tested prototype is 224 mA at 25 $^{\circ}C$, as shown in Fig.4.12, and it is found to be long-term stable, facilitating one-point compensation. To evaluate the stability of the offset under temperature and time variations, the setup indicated in Fig.4.11(b) was used. The prototype, with R_F set to 200 kΩ, was placed inside a ACS DY110(T)

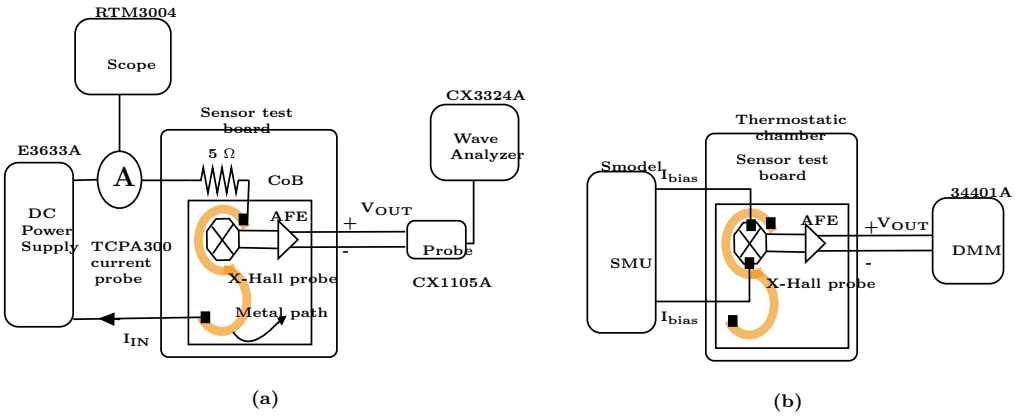


Figure 4.11: Measurement setups: (a) Static characterization; (b) Offset drift

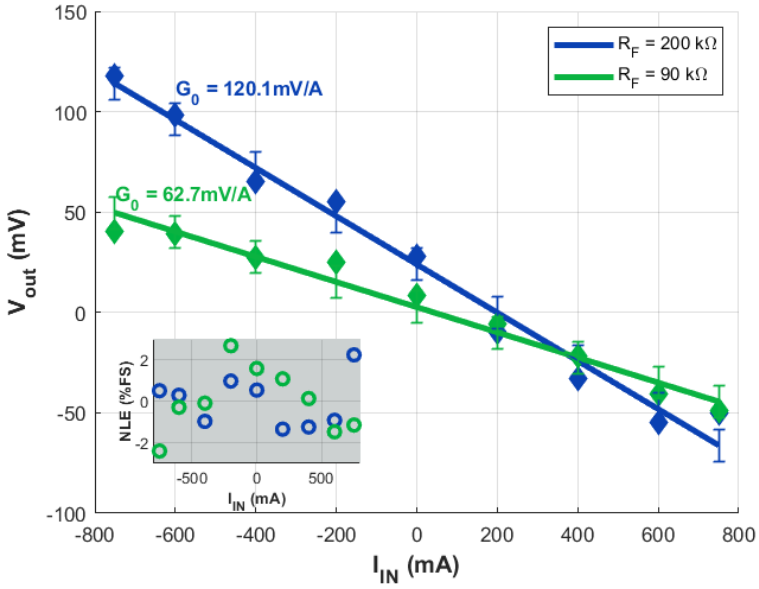


Figure 4.12: Static characteristics: output voltage versus input current. The measured non-linearity error (NLE) as a percentage of Full Scale of 3 A corresponding to the data points of the main plot are also reported in the inset.)

climatic chamber with controlled temperature.

The variability of the offset with respect to time was evaluated at zero input over 100 hours with an Agilent 34401A digital multimeter (DMM) recording the offset voltage at an interval of 10 minutes and the internal temperature of the thermostatic chamber set to $27 \pm 0.5°C$. The Hall probe was

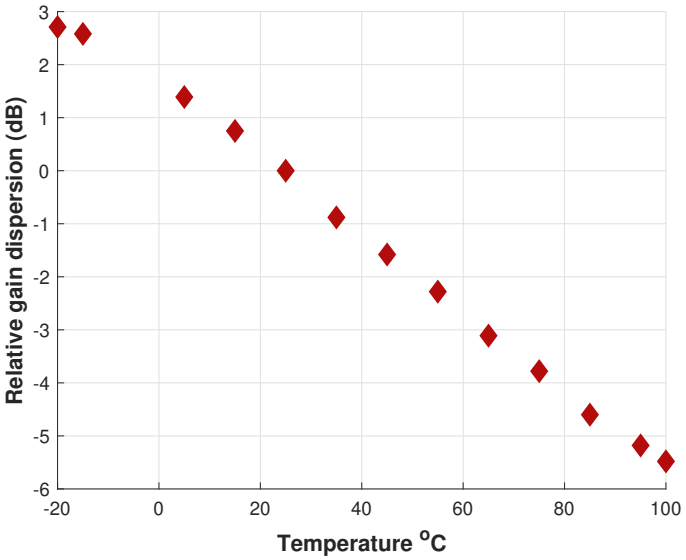


Figure 4.13: Transduction gain dispersion with respect to temperature. The frequency of I_{IN} is at 500 kHz and the $R_F = 200k\Omega$

externally biased using the Keithley 2450 Source Meter Unit. The result of this experiment, shown in Fig.4.14, reports a dispersion of the input-referred offset at a stable temperature of ±26 mA with a drift of 0.33 mA/hour, which correspond to a dispersion of ±197 μT and a drift of 2.5 μT/hour.

Fig.4.15 reports the dispersion of the input referred offset current of the prototype in the ambient temperature range of $-20\ ^\circ C$ to $+100\ ^\circ C$. The temperature was swept in both directions of heating and cooling using the climatic chamber to check for possible hysteretic behavior. The mean of 20 sample values of the output offset voltage V_{OS} was recorded by the DMM at each temperature point and then referred to the input of the system mathematically to obtain the input referred offset, $I_{OS} = V_{OS}/G_0(T)$, where $G_0(T)$ is the gain of the system expressed as a function of temperature T. Least squares linear interpolation of the measured data separately in the cold region ($-20°C$ to $+30°C$) and the hot region ($+31°C$ to $+100°C$) resulted in two different temperature coefficients of -8.4 mA/$°C$ and -4.1 mA/$°C$ respectively. Considering the sensor would most likely operate in the warmer region in practical application, then the proposed sensor is more stable than

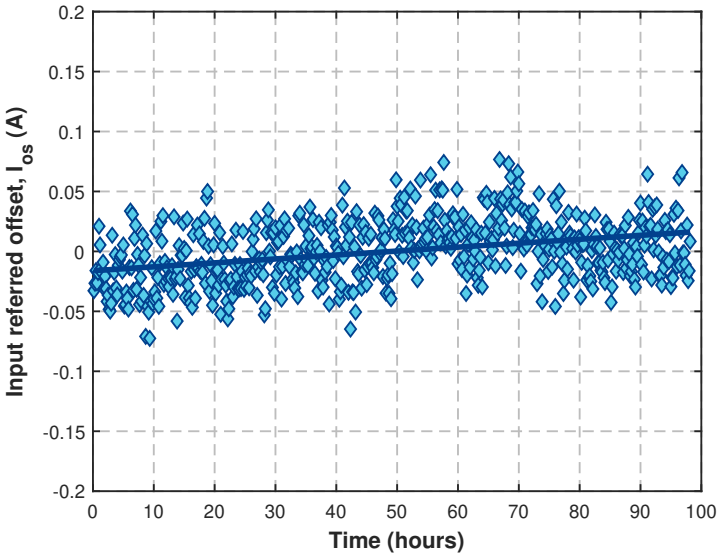


Figure 4.14: Time drift of the input-referred offset normalized to the mean of the measurement points. The measurement was carried out at a stable temperature of $27 \pm 0.5°C$ for 98 hours. The measurement reports a mean standard deviation of the offset as ±26 mA and a total offset drift of 0.33 mA/hour

the voltage-mode X-Hall sensor described in [46], which reported TC = 5.5 $mA/°C$, and slightly higher to TC = 2.4 $mA/°C$ of standard spun Hall sensors [137]. Additionally, the variation of the voltage V_{CMC} generated by the CMC block is simultaneously measured. The resistance of the Hall probe changes with temperature, and with a constant I_{bias} would alter the output CM voltage of the probe, risking the exposure of AFE to higher voltage. The V_{CMC} counteracts this variation due to temperature, always attempting to force the output CM voltage to ground, hence demonstrating the functionality of the CMC block.

4.4.3 Dynamic characterization

The transfer function of the prototype is estimated by applying a sinusoidal input current of 37 mA_{rms} using the RTM3004. The input current flows through the 5-Ω power resistor soldered on the test board before flowing through the metal trace within the chip. The input current is measured and controlled by using the Tektronix TCPA300 current probe. The differen-

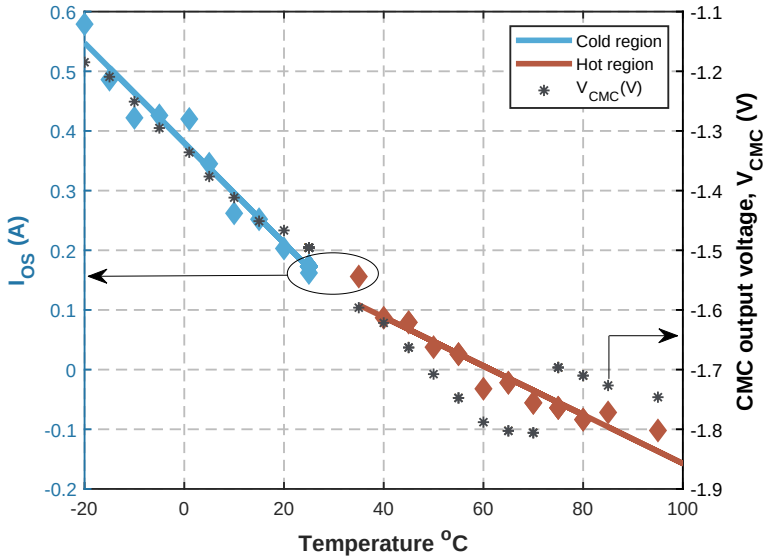


Figure 4.15: Input referred offset drift with respect to temperature, TC(cold region) = -8.4mA/degC, TC(Hot region) = -4.1mA/degC

tial voltage at the output of the sensing system is acquired using the 45-MHz differential probe CX1105A and observed on the CX3324A scope. The amplitude of the applied current is limited by the available instrumentation and it is below the minimum detectable signal (MDS) of the sensor, therefore the scope is used in averaging mode over an adequate number of waveform captures to enhance the experimental resolution on the output voltage. Acquiring both the stimulus current and the output voltage on the CX3324A scope allows accurate synchronization and minimum time skew. Ten frequency points per decade were acquired in the 100 Hz to 20 MHz frequency range. The plot of the transfer function obtained with the Hall sensing system internally biased at 1.05 mA and its corresponding phase response are shown in Fig.4.16 and 4.17. Fig.4.16 clearly demonstrates achieved bandwidths of 10 MHz and 12 MHz for the case of $R_F = 200$ kΩ and $R_F = 90$ kΩ, respectively. Above these frequency values, perturbative inductive effects due to the bondwires come into play, as also observed and discussed in [46]. The shaded region corresponds to the standard uncertainty of measurement and is in the order of tens of $\mu V/A$. To the best of our knowledge, this pro-

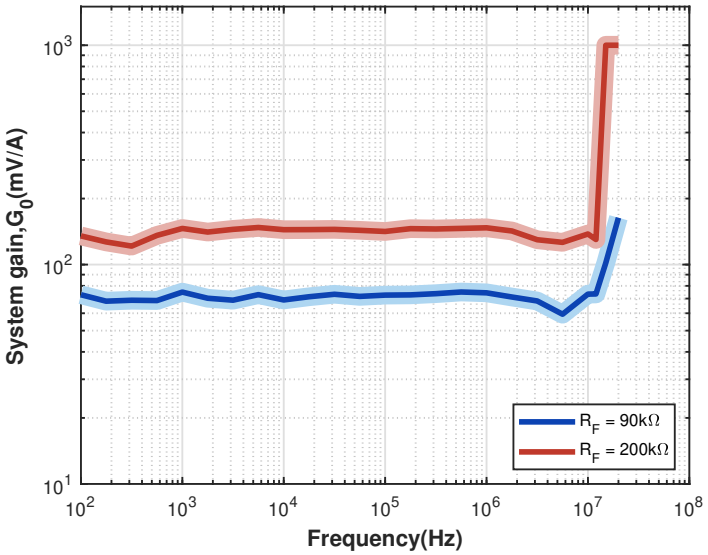


Figure 4.16: Transduction gain as a function of frequency

totype implemented using using standard CMOS process, demonstrates the highest acquisition bandwidth compared to state-of-the-art purely Hall-effect sensors.

The input-referred noise power spectrum density of the sensor is shown in Fig. 4.18. The total in-band noise (DC - 20 MHz) referred to the output of the system is 4.7 mV_{rms}. Referring the rms noise to the main input of the current sensor leads to a resolution $i_{in_{tot}}$ of 39 mA_{rms}. Further, calculating the input referred integrated noise in the same frequency band with R_F set to 200 kΩ, 4.7mV_{rms}/200 kΩ results in 23.5 39 nA_{rms} which is completely in accordance with our simulated result discussed in section 4.3.

4.4.4 Validation

The capability of the proposed system to sense very fast current events is validated in the acquisition of a pulsed current stimulus of 100 mA_{pk-pk} with a frequency of 100 kHz, 30 % duty cycle and trail edges of 50 ns, as shown in Fig.4.19. The figure compares the applied current, acquired using the commercial TCPA300 current probe, with the output of the system. The 100 mA_{pk-pk} pulse is transduced into a 12 mV_{pk-pk} pulse at the output with

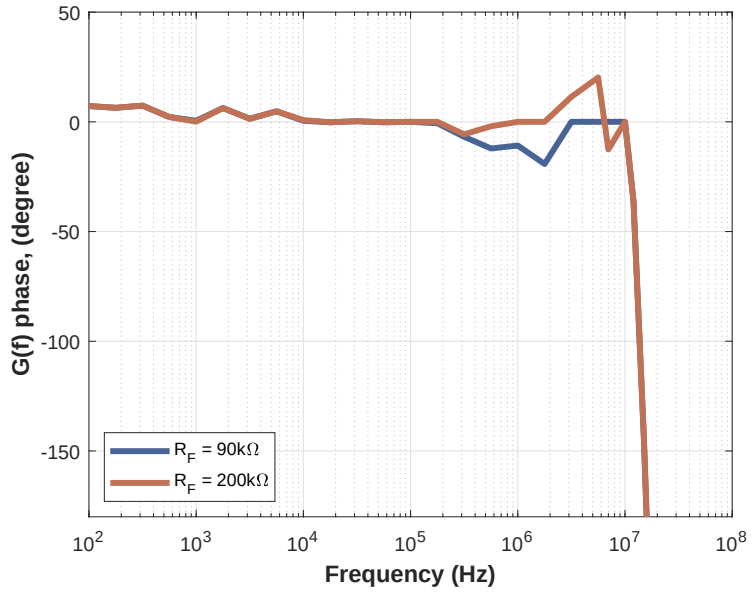


Figure 4.17: Phase response as a function of frequency)

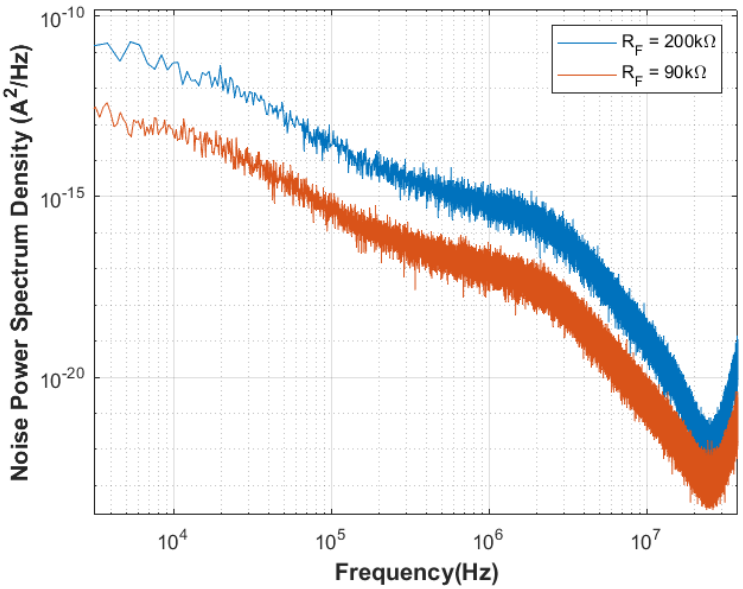


Figure 4.18: Noise Power Spectral Density)

peaks added on the trailing edges due to second order effects and the high-frequency inductive parasitic element. Despite this stray effect, the prototype

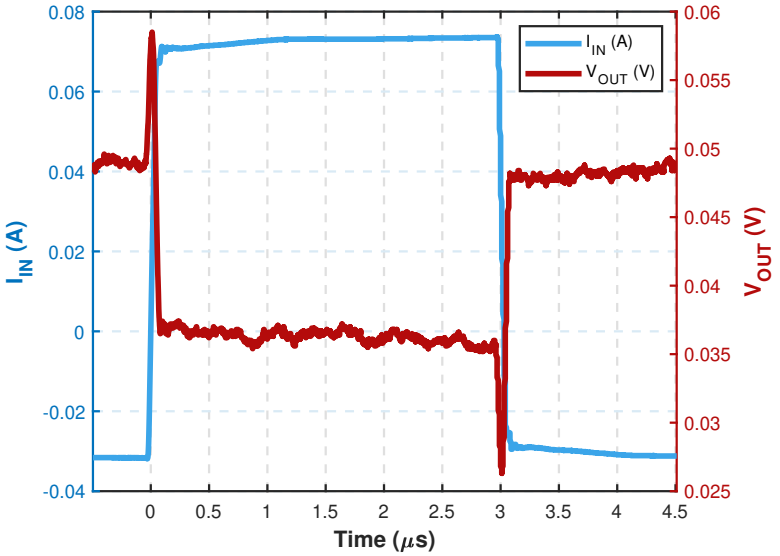


Figure 4.19: Transient response of the system to a 100 kHz pulsed input current of 50 mA_{rms}. The observed delay in response is 25 ns

demonstrates a delay in the response as short as 25 ns.

4.4.5 Magnetic sensitivity

In all of the above measurements, we have assumed the value of Gib is aligned to the simulation value of 7.5 mT/A. To substantiate this assumption, a magnetic sensitivity test using the 3B1000906 Helmholtz coils was performed using the setup as shown in Fig.4.20. It is important to highlight here that, the sample that had been used to obtain the previous characterizations had been unfortunately damaged and so, two different samples are used for magnetic testing. The applied magnetic field is limited to ±0.7 mT given by the formulation [138],

$$Bcoil = 7.433.(10^{-4}).Icoil \tag{4.11}$$

where Icoil is generated and limited to 1-A by Keithly 2450 Source meter unit which supplies the current to the Helmholtz coils. The magnetic field due to the superimposition of the two coils is quite uniform within the mean

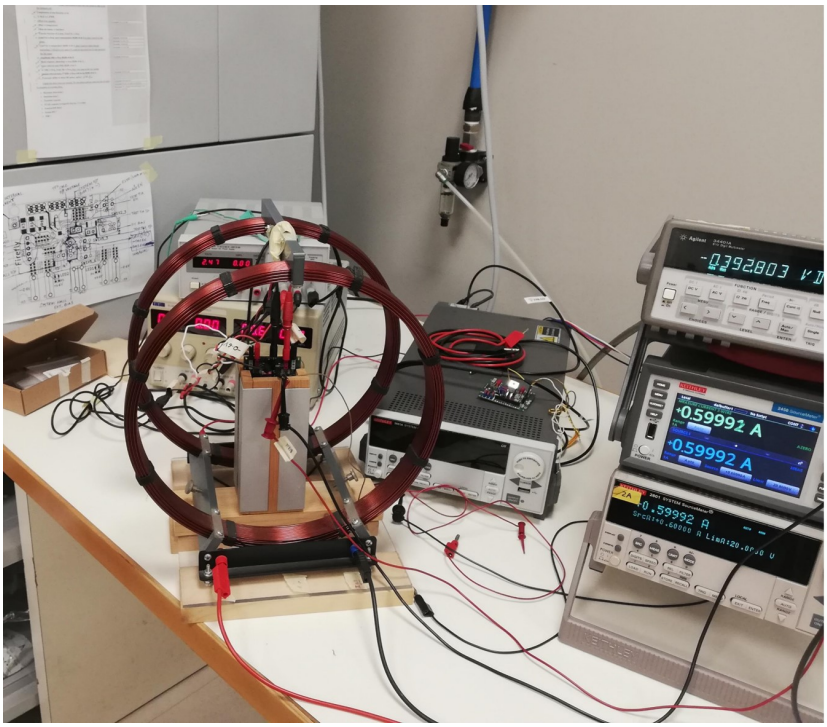


Figure 4.20: Helmholtz coil setup to test the magnetic sensitivity of CH09

radius of the coils and the sensor positioning within this radius does not affect much the measurement. However, for best accuracy, the sensor was positioned at the center of the Helmholtz coils. the sensor output voltage is measured using the Agilent 34401A DMM with a reading measurement accuracy of ±0.006% in the 100 mV range. The results of this magnetic characterization for two samples are reported in Fig.4.21 with the X-Hall probe being internally biased at 1.05 mA. Sample 1 with R_F set at 90 kΩ and 200 kΩ yields a DC sensitivity due to the magnetic input, G'_0 of -10.529 V/T and -21.3 V/T respectively, while sample 2 whose R_F is set at 200 kΩ yields a G'_0 of -16.658 V/T. The current to magnetic field transduction factor, G_{ib} is estimated from the ratio of the DC sensitivity to current input as in equation 4.6 and the DC sensitivity to magnetic input which is defined by the equation:

$$G'_0 = G_H.G_{ELE} \tag{4.12}$$

The values of G_0 used for computation correspond to those in Fig.4.12.

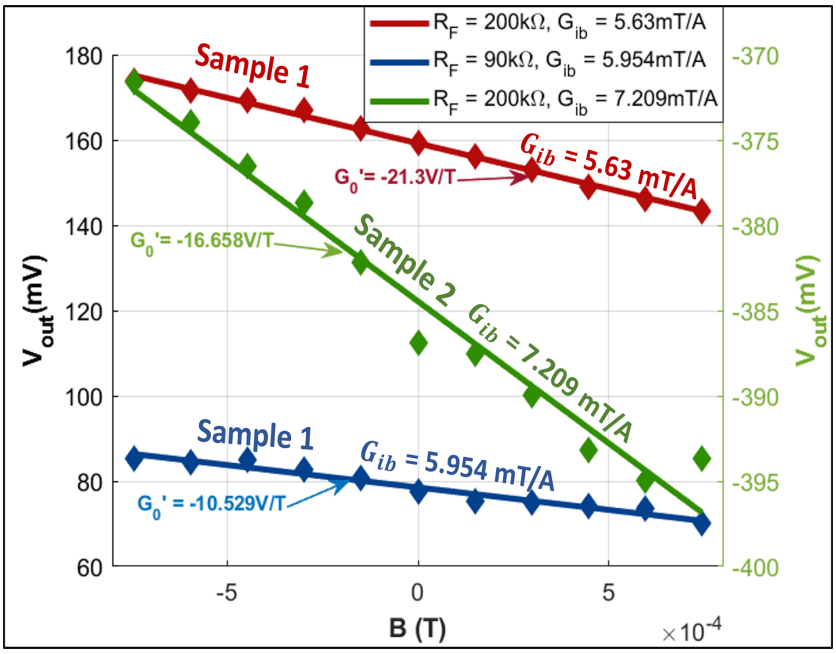


Figure 4.21: Estimation of *Gib* from the magnetic response of the X-Hall sensor for two different samples

We can reasonably expect a variation of 20% in the experimental values of G_0' for samples 1 and 2 compared to those obtained from Fig. 4.12 with the possibility of the main source of variation being the feedback resistors of the TIA. The estimated G_{ib} for sample 2 is quite in accordance with our simulated value while it differs by almost 20% for sample 1. The mean G_{ib} over the two samples is 6.26 mT/A.

Chapter 5

CH100: Enhancements to CH09

This chapter focuses on overcoming the limitations for the CH09 prototype and discusses the proposition of its enhanced version, the CH100. The main limitations to CH09 are:

1. Thermal gain drift of ±4 dB in the temperature range of -20°C to 100°C.

2. Limited input current range of ±800-mA due to the type of prototype realization.

3. Thermal offset drift in the temperature range of -20°C to 100°C.

The functionality and ideas are demonstrated theoretically and through preliminary results, as the prototype for characterization would be available no earlier than Jun 2023. The main goal of designing and implementing a broadband-integrated Hall sensor is to make it suitable for real-time power applications such as power converters, smart grids, etc. So, the sensor design must fulfill multiple stringent requirements such as operation accuracy in extreme temperature conditions and deliver high-speed responses to the measurand signal. These features deliver accurate and timely information about the state of key parameters of the concerned application, hence preventing loss of productivity [139]. Low cost and easy installation and replaceability

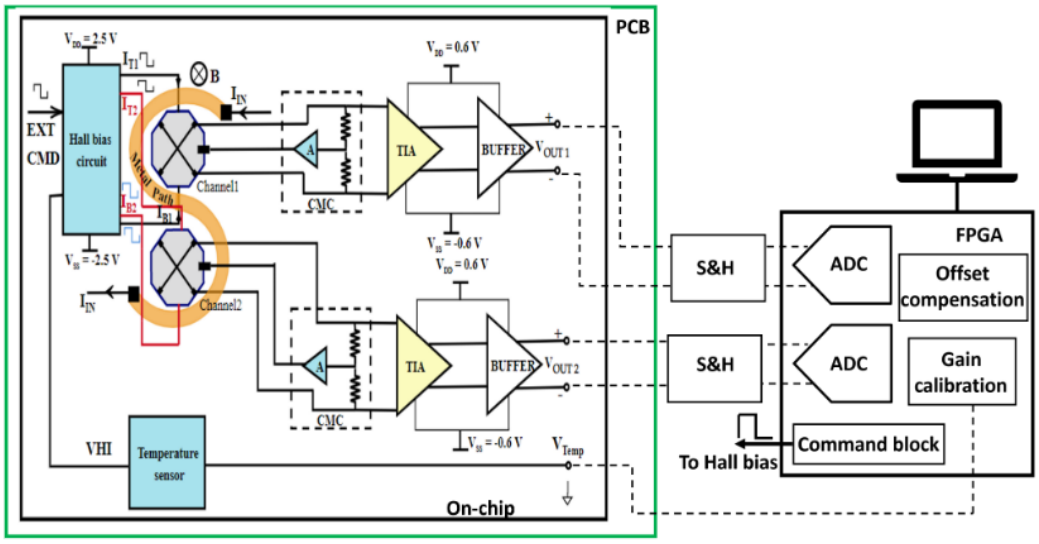


Figure 5.1: Proposed block diagram

would be other helpful characteristics. There are numerous efforts to cope with non-idealities, but we must bear in our knowledge that, as we near our performance goals, we also come closer to the challenges posed by the intrinsic properties of the device itself. When a Hall device is used as a magnetic sensor, the reproducibility of the sensor output is a critical aspect of concern. This is because, the sensitivity is proportional to the Hall coefficient (refer Eq. 2.21 and 2.48), which is dependent on the charge density of carriers, nt on the surface which could alter due to any physical effects, e.g., Magnetoresistance effect under stress conditions. These are also referred to as surface effects. We will now directly proceed to the proposition of a new architecture for the CH100 prototype, followed by the main issues of CH09 with their solutions.

5.1 Proposed architecture

The new architecture for the CH100 prototype as illustrated in the block diagram in Fig. 5.1 proposes a differential sensing scheme for the cancellation of common mode interferences, thus featuring, dual sensing chains utilizing two X-Hall probes. It is up to the user to use a single/double channel for

sensing and their respective differential signals are available on the chip for post-processing. This step would be necessary to digitally compensate the offset and calibrate the gain of the sensors and it comprises a programmable FPGA with preferably high-resolution and high sampling rate differential Analog-to-Digital Converters (ADCs). The new sub-modules within the chip are shaded in blue, while the yellow-shaded ones indicate an optimization. An built-in temperature sensor, that utilizes the linear temperature variant signal, VHI from the Hall bias circuit is also designed, to accurately calibrate the system gain digitally, thus coping with the thermal gain drift problem. For a detailed discussion, refer to section 5.2. The design features a new internal switched biasing scheme for the X-Hall probe, for the purpose of residual offset cancellation. The Hall bias can be activated by the user through suitable digital command signals. The details of which can be referred in section5.4.2.

5.2 Gain drift

We have seen from Fig.4.13 that the overall relative transduction gain dispersion in the temperature sweep from -20°C to +100°C is approximately ± 4dB. This is also in close accordance with the simulated gain dispersion. In practice, a digital or analog gain compensation is usually implemented as seen in [40] while there is no compensation applied to the sensor in CH09. Exploring the origin and possible causes, that could cause this drift, we straight away refer to the system model related to the sensitivity as given in Eq.4.6, from which we can gather that the three parameters, G_H, G_{ib} and G_{ELE} could be affected due to temperature and hence cause a manifestation of the dispersion of the transduction gain. The former two are set by the technology and design and cannot be altered much for the improvement of dispersion, while the AFE design choices could in particular contribute to improvement. It was found through simulations that the transimpedance amplifier as a standalone module, contributes to 3 dB of variation. Since its architecture uses resistive feedback, it is doubtless that the semiconductor resistance changes with temperature or has a high-temperature coefficient

contributing to the thermal drift. The possible workaround for this was either to modify the architecture such that the gain thermal drift is reduced, or to explore the TC of the used R_F and compare the TCs of the resistors provided by technology. We initiated with the latter and found that the used R_F which was a high-value Nplus Poly resistor on substrate, had a high TC of the order of k$\Omega/°C$. This was replaced in the TIA by an unsilicided P+ resistor on substrate with nearly a 94% reduced temperature coefficient which resulted in the thermal drift of the TIA alone, being approximately 0.3 dB in the above-mentioned temperature range. Further, to check and bring our simulations close to the emulation of the practical prototype scenario, the temperature coefficient of the resistivity of the active region of the X-Hall probe interfaced with an ideal AFE model (Fig. 5.2) was estimated through device simulations in TCAD over a temperature range of $-20°C$ to $+100°C$ (refer Fig.5.3(a)) along with the variation of the output probe current, I_{probe} (refer Fig.5.3(b)). The plots reveal a TC of $8.814 \times 10^{-3}/°C$ and $-1.76 \times 10^{-3}/°C$ respectively for a bias current, $I_A = I_B = I_{bias}$ = 1-mA. The plot for I_{bias} =500 μA is not shown, however, the resistivity of the n-well would be unaffected by I_{bias}. The corresponding sensitivity drift of the X-Hall probe in the above-mentioned temperature range at I_{bias} 500 μA and 1-mA was estimated using the standard formulation in Eq.4.3 as shown in

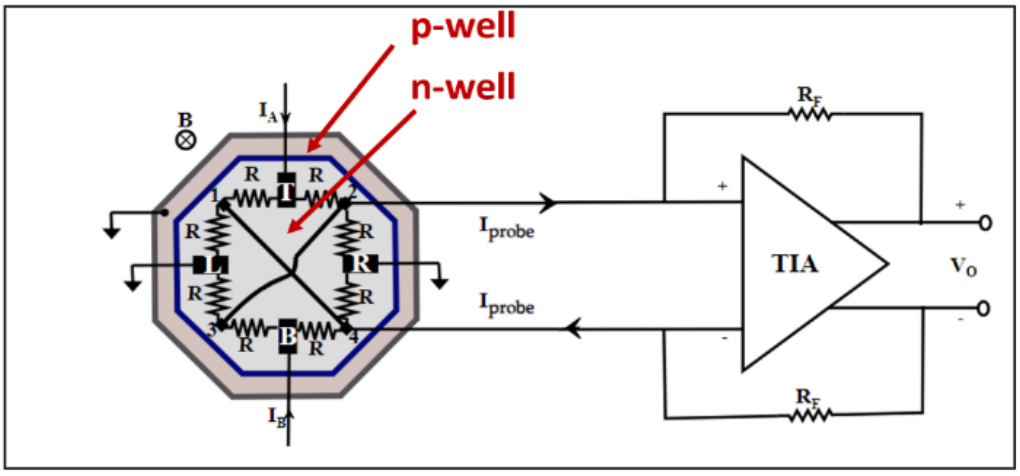


Figure 5.2: Illustration of the simulation model of the X-Hall sensor in current mode

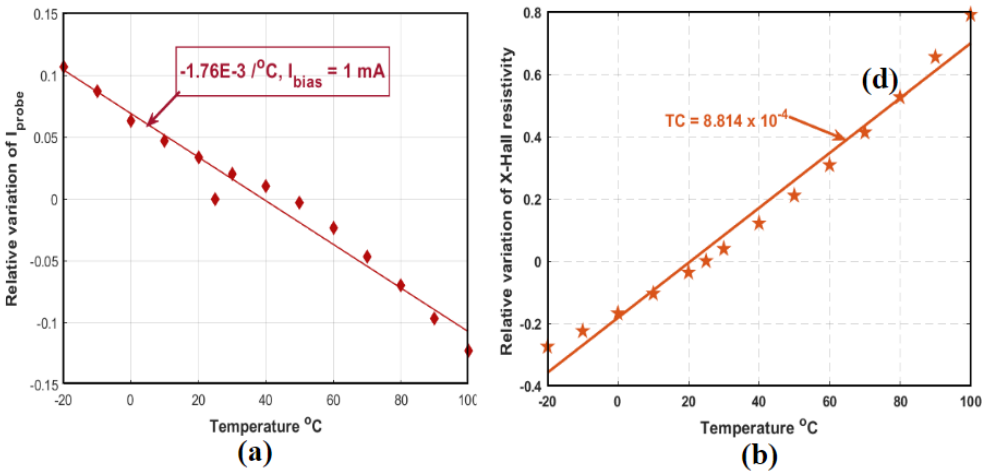


Figure 5.3: TCAD simulation plots for the temperature range of -20°C to +100 °C at an applied magnetic field of 50-mT: (b) relative variation of the resistivity of the n-well of the X-Hall probe, the temperature coefficient is $8.814 \times 10^{-3}/°C$, for a bias current of 1-mA

Fig. 5.4 and it can be observed that the sensitivity of the Hall probe increases with I_{bias} with a reduced TC of $-1.07 \times 10^{-4}/°C$. The TC of the n-well and I_{probe} are then introduced as simulation parameters to realistically analyze the gain and offset thermal drift(as will be discussed in the next section). The thermal drift for the entire system was then simulated and it showed a relative gain variation of less than 0.7 dB which is an improvement by a factor of 8 compared to the experimental result of CH09 and can be viewed as a preliminary result in Fig.5.5.

5.2.1 Temperature sensor

To digitally calibrate the thermal gain variation, we opted to use the sensor itself for temperature sensing. An internal signal, VHI which forms the gate node voltages of the high-compliance current mirror connected to a resistive V-I converter in the Hall bias circuit (refer Fig.5.1 and 5.14 for a schematic view) was selected such that its variation is almost proportional to the temperature with a non-linearity error of ±0.01%. Fig.5.6(a) illustrates the schematic of the readout circuitry for the designed temperature sensor

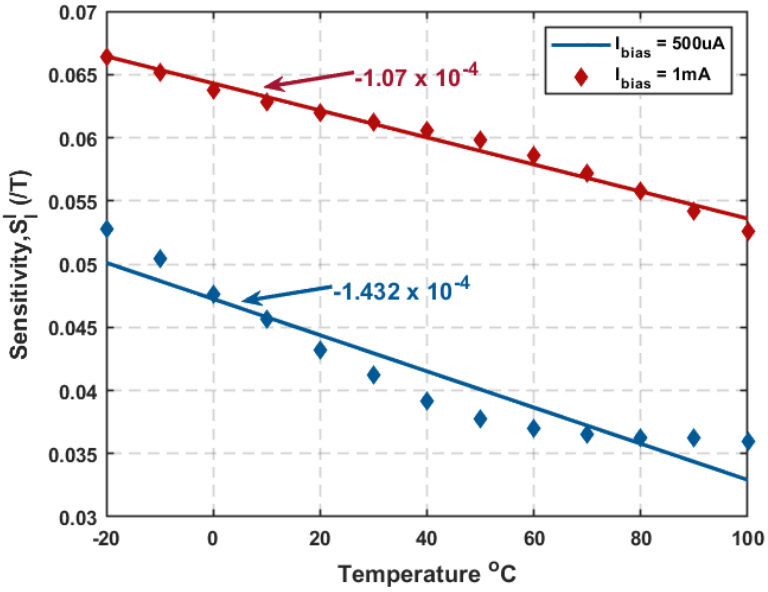


Figure 5.4: illustration of the current related sensitivity drift with respect to temperature derived from the plots in Fig.5.3(a) and (b)

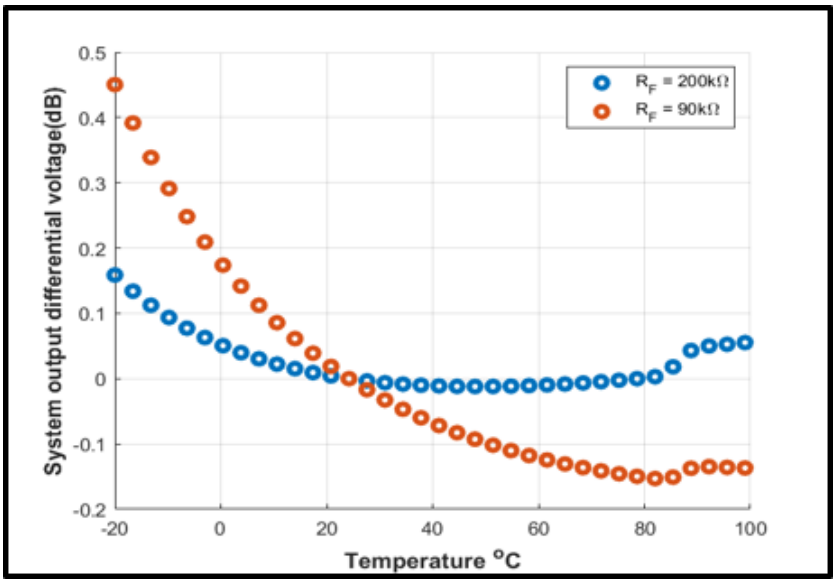


Figure 5.5: Improved gain drift with less than 0.7 dB variation in the temperature sweep from -20 $^{\circ}C$ to +100 $^{\circ}C$.

which is based on a series-shunt feedback amplifier. The internal scheme of the amplifier can be seen in Fig.5.6(b). The closed loop gain, A_{CL} of the

operational amplifier with open loop gain, A is given by

$$A_{CL} = \frac{V_{Temp}}{VHI} = \frac{A}{1 + A\beta} \tag{5.1}$$

with loop gain $A\beta$ formulated as

$$A\beta = \frac{AR_i}{R_i + R_f} \tag{5.2}$$

and β is the feedback factor given by the standard equation:

$$\beta = \frac{R_i}{R_i + R_f} \tag{5.3}$$

The gain of the operational amplifier was roughly estimated theoretically based on the range of VHI over the temperature range from -20 $°C$ to +100 $°C$ as can be observed in the plot in Fig.5.7(a). In Fig.5.7(b), we see the voltage range of VHI and also graphically present the extreme expected voltage range post-amplification. The gain of the operational amplifier is estimated through V_{Temp}/VHI which results in a gain of 13. Since we chose an extreme output voltage range, the gain of the readout circuitry could be lower. A high valued $R_f = 250\ k\Omega$ to prevent excess current withdrawal and a lower $R_i = 35.7\ k\Omega$ were selected to finally achieve a closed loop gain of around 8 (18 dB). It can be seen in Fig.5.7 that the amplified signal of the temperature sensor, V_{Temp} is similar to VHI and almost proportional to the temperature. Since the temperature is not a rapidly varying quantity, the bandwidth of the sensor is not crucial. The sensor however has a bandwidth of 3.8 MHz, a gain bandwidth of 19 MHz as shown in Fig.5.8 which could be lowered in order to reduce the estimated power consumption of 0.3 mW of the sensor. The temperature sensor readout acts as a capacitive load to VHI, hence the system noise performance is unaffected by it.

Now, if we want to calibrate the gain of the system with respect to temperature, $G_0(T)$, what would be the required accuracy of the temperature sensor if we target a gain post calibration accuracy of 1%? The gain of the

system at a temperature, T can be modeled using a linear function:

$$G_0(T) = G_0(T_0)(1 + TC_{G_0}\Delta T) \tag{5.4}$$

where the TC of the system gain, $TC_{G_0} = \Delta G_0/[G_0(T_0)\Delta T]$ from simulation of the present design is approximately $0.06\%/^\circ C$.

$$TC_{G_0} = \frac{\Delta G_0}{G_0(T_0)\Delta T} \tag{5.5}$$

The law of propagation of uncertainty states that " uncertainties propagate along the sensor chain by means of the square of the sensitivities computed around the bias point or the estimated point". Thus, if we target a post-calibration accuracy of the temperature sensitivity to be 1%, the associated uncertainty of temperature measurement can be estimated as follows [140]:

$$u^2(G_0(T)) = [\frac{dG_0(T)}{d\Delta T}]^2.u^2(\Delta(T)) \leq 1\%/^\circ C \tag{5.6}$$

Inserting Eq5.4 to solve the above derivative,

$$\frac{u^2(G_0(T))}{G_0^2(T_0)} = TC_{G_0}^2.u^2\Delta(T) \leq 1\%/^\circ C \tag{5.7}$$

This implies

$$u^2\Delta(T) \leq \frac{1}{TC_{G_0}^2} \tag{5.8}$$

$$u\Delta(T) \leq \frac{1}{TC_{G_0}} \tag{5.9}$$

$$u\Delta(T) = \frac{1}{0.06\%/^\circ C} = 16.6^\circ C \tag{5.10}$$

This uncertainty of temperature measurement must be greater than the square root of the sum of squares of the rms noise of the temperature being sensed(in $^\circ C$), σ_n and the associated non-linearity error.

$$u\Delta(T) \geq \sqrt{\sigma_n^2 + NLE^2} \tag{5.11}$$

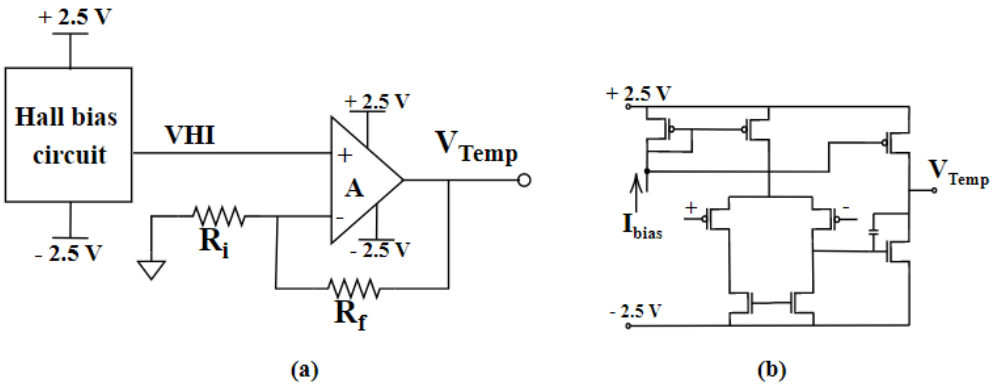


Figure 5.6: (a) Block diagram of the series-shunt feedback amplifier readout for temperature sensing acquiring the temperature variant signal VHI from the Hall bias circuitry, (b) schematic of the amplifier used

Considering temperature, T as input to the sensor and output voltage as a function of temperature, $V_{Temp}(T) = KT$, the output rms noise, σ_n in the frequency band of 100 to 10 MHz was found through simulation to be 560 μV_{rms} and $V_{Temp}(T)$ varies at a rate of $-14.5mV/°C$. So the noise voltage when referred to the temperature input of the sensor results in σ_n of 40 $m°C_{rms}$. The % NLE as already mentioned above is 0.01% and it corresponds to 0.1 V or $0.1/-14.5mV/°C = -7°C$. From this, we understand that, the NLE is the dominant factor in the uncertainty of temperature measurement. Thus, inserting the obtained values in Eq.5.11, we obtain $u\Delta(T) \geq 7°C$ which is much lower than what corresponds to the targeted 1% accuracy. In other words, the post-calibration measurement accuracy of the designed temperature sensor can be better than 1%.

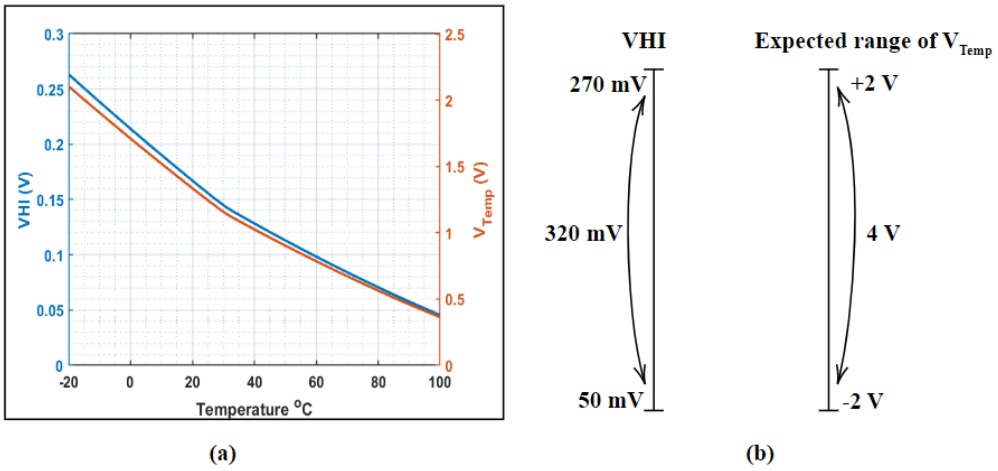


Figure 5.7: (a)Thermal drift of VHI and the amplified temperature sensor output, V_{Temp}, (b) graphical representation of the input-output voltage ranges of the temperature sensor for estimating the gain

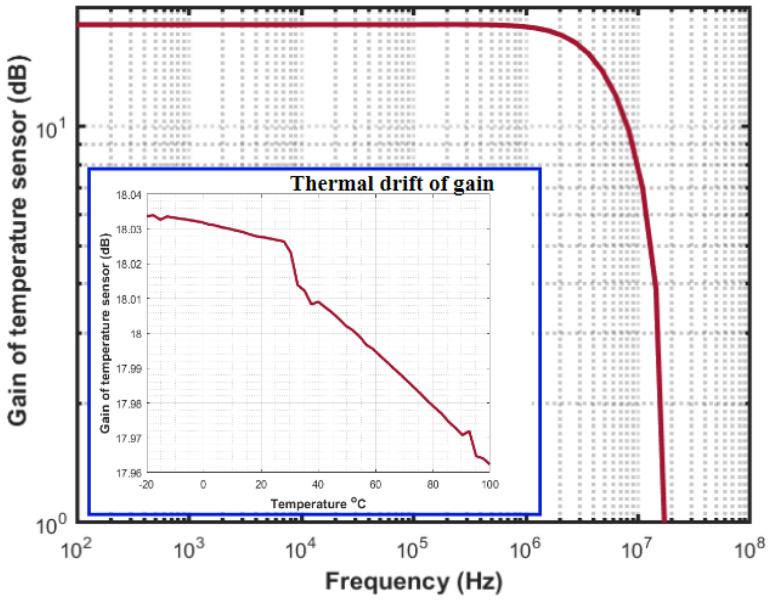


Figure 5.8: Gain response of the designed temperature sensor as a function of frequency. Inset shows an almost 0.4% thermal variation of the gain

5.3 Dynamic range

Another limitation of the CH09 prototype was the limited range of up to ± 800 mA for the input current. Despite the metal trace within the chip capable of handling up to 3A of current, higher currents could not be applied for testing due to erroneous implementation of the bondwires in terms of thickness and material or the chip-on-board implementation of the prototype. They should have been copper wires with a diameter of 1 mils or more instead of gold with 1.5 mils, preventing the practical usability of the sensor. For the proposed prototype, we opted for the stud-bump realization instead, which gets rid of the delicate leads thereby, lowering the inductive coupling between them as well, and so we target ± 5-A of input current range. Apart from this, the TIA was optimized for much higher bandwidth and lower AFE-probe input referred noise by enlarging the widths of the transistors by a factor of 3.5, trading off to a current consumption by the same factor to 412 μA. The resultant acquisition bandwidth of the system is now 26.87 MHz and 17.7 MHz when loaded with a capacitance of 5 pF. The integrated input referred noise of a standalone TIA reduced from 12.8 nA_{rms} to 9.33 nA_{rms} in the DC -10 MHz range. Simulations by integrating the optimized TIA with the system show a nearly 30% reduction of the integrated input referred noise at the probe - AFE interface with the value being 16.83 nA_{rms} in the band mentioned above, while in the frequency band of DC-30 MHz, it is only 26.69 nA_{rms} compared to CH09's 23.5 nA_{rms} in the DC-10 MHz range. The total in-band noise (DC-30 MHz) referred at the output of the system is 4.18 mV_{rms}, resulting in the resolution $i_{in_{tot}}$ of 39 mA_{rms}. Hence, the estimated dynamic range is 42 dB and shows a 10% improvement from CH09 prototype for a full-scale input current range of 5-A.

5.4 Offset reduction

From the characterization results of CH09, thanks to a high G_{ib}, we observed that the input offset referred to the current input is the lowest (224 mA) compared to the state-of-the-art (refer table 6.1), with a higher TC in

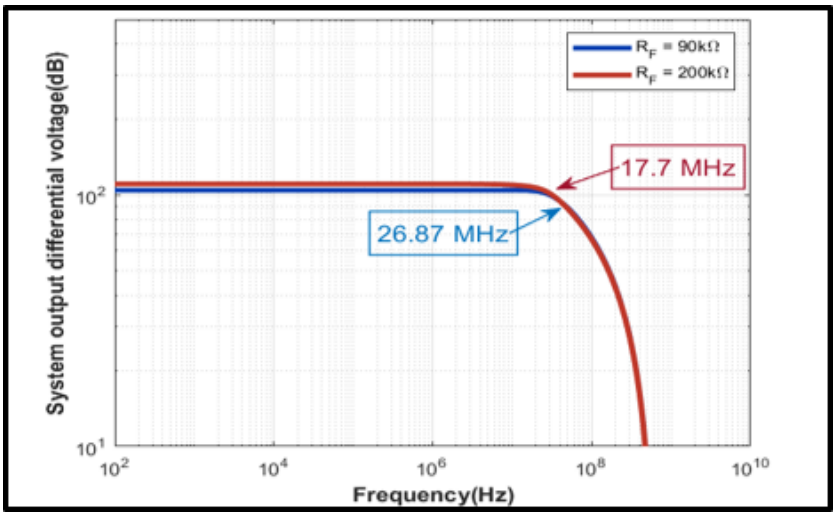
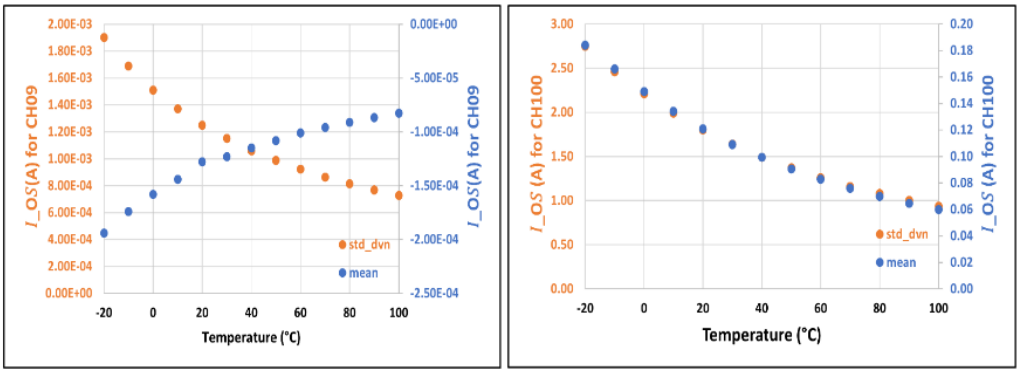


Figure 5.9: The gain of the integrated system as a function of frequency after optimizing the TIA, depicting the improvement in system acquisition bandwidth.

the cold region and lower TC in the hot region when compared to that of the voltage mode as in Fig.4.15. It however, has a non-adequate magnetic offset of 1.68 mT which must be minimized if the sensor must measure high current ranges, for which the current carrying trace cannot be integrated on chip.

A relative analysis through Monte-Carlo simulations was done to analyze and understand the impact of the unsilicided P+ resistor on the system offset thermal drift. Plots of the mean and standard deviation of the system input current referred offset for the two different technology type resistors are shown in Fig.5.10(a) and (b). The input referred offset was computed using the experimental value of $G_0 = 120.1$ mV/A. The results of extracting the temperature coefficients in the cold and hot regions can be observed in Table.5.1. Although the numerical values are not exactly equal to the experimental values but are quite relatable and sufficient for a relative analysis. It is clear that the system model using the unsilicided P+ resistor as R_F for the TIA has a remarkable reduction in thermal offset drift apart from the thermal drift of the gain and therefore, we expect this behaviour to reflect in the real prototype scenario in future during testing unlike in CH09, which demonstrated a high temperature coefficients in the hot and cold regions for



(a) (b)

Figure 5.10: Montecarlo simulation results for the thermal drift of input current referred offset with mean and standard deviation, σ for (a)the prototype CH09 with its TIA implementing a high value N + poly feedback resistor on substrate, (b)the prototype CH100 with its TIA implementing unsilicided P+ feedback resistor on substrate

Table 5.1: Monte Carlo simulations for offset

Temperature coefficient	Experimental I_{os}	R_F=N+ poly	R_F=unsilicided P+
TC(cold)(mA/° C)	-8.4 ($-63\mu T/°C$)	-1.5 ($-11.2\mu T/°C$)	0.00145($10.8nT/°C$)
Standard deviation, σ		-22 ($-166.5\mu T/°C$)	-0.0149($(-0.11\mu T/°C$)
TC(hot)(mA/° C)	-4.1 ($-30.7\mu T/°C$)	-9.21 ($-690\mu T/°C$)	0.00053($4nT/°C$)
Standard deviation, σ		-9.21 ($-69\mu T/°C$)	-5.51($(-41nT/°C$)

the offset.

5.4.1 Novel offset cancellation

In CH09, the current offset at a stable room temperature was observed to be almost time stable with a drift of 0.33 mA/hour or 2.5 μ T/hour which can facilitate one-point compensation. However, it is not as stable as commercial solutions. To push more for a lower offset and cancel it, here, we propose novel techniques for residual offset cancellation which are theoretically and experimentally validated using the test X-Hall probe in the CH09 prototype assuming the configuration in voltage mode. These, however, are also applicable if the probe is to be configured in the current mode.

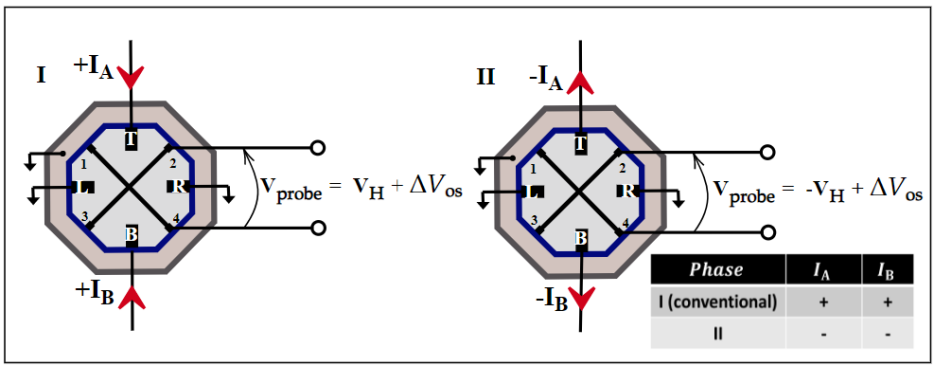


Figure 5.11: Technique to cancel offset (I) conventional biasing with nominally equal bias currents I_A and I_B being sourced into the probe, (IV) I_A and I_B sunk out of the probe resulting in a negative V_H.

We have two possible ways to bias the X-Hall probe and obtain the output voltage of the probe,V_{probe} as illustrated by the figure 5.11 and its inset, with '+' and '-' implying the current being sourced into the probe and sunk out from the probe respectively. The objective is to subject the probe through the two bias phases instead of a constant dc bias. Phase I is the conventional bias method that yields a Hall voltage summed with the residual offset (also refer Eq.3.8), while phase II biasing is in complete opposition of phase I and hence, results in a similar Hall voltage but with a sign reversal. We can now mathematically manipulate these possible results in order to achieve our goal of cancelling the residual offset using a Chop-like technique with math operation: Phase(I-II)/2.

The Hall bias currents are continually switched between phases I and II applied at a frequency, f. At the end of each phase II, the mathematical operation, (I-II)/2 can be performed to obtain the residual offset which dynamically can be separated from the Hall voltage, V_H.

With a clarity of the theory and idea for the cancellation of offset, we now proceed to validate the theory through experimental data. The setup for the static experiment is shown in Fig.5.12. The probe is dc biased as required using two Keithly 2450 SMUs and the probe output voltage, V_{probe} is measured using the Agilent 34401A DMM. An input current of 200 mA is applied to the metal trace within the chip through a 5 Ω power resistor

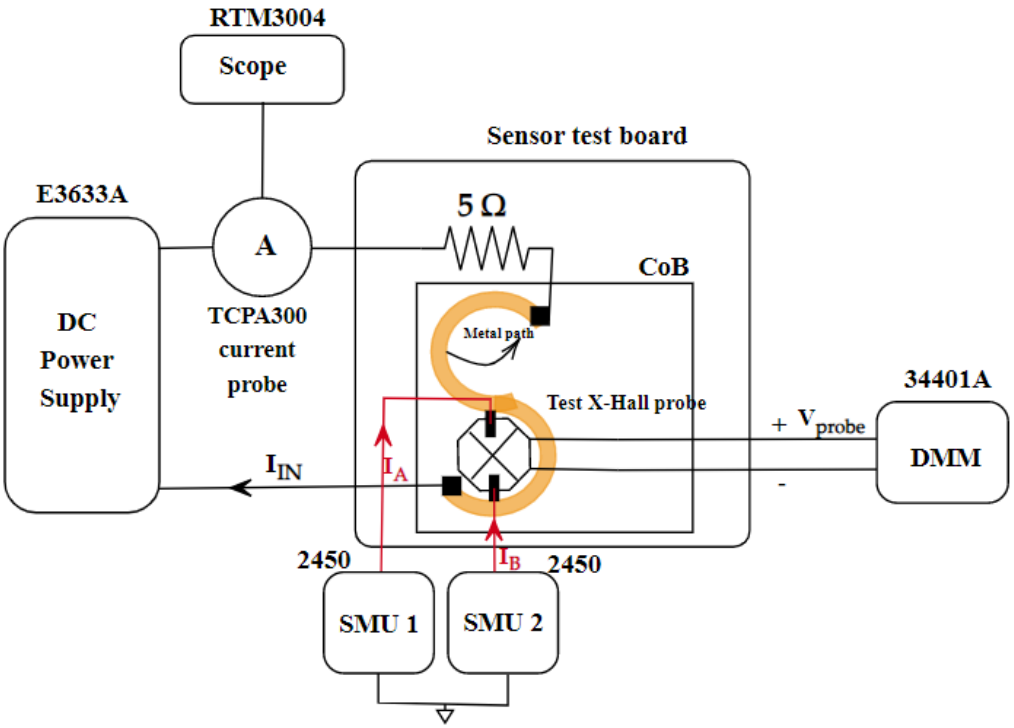


Figure 5.12: Experimental setup used to demonstrate offset cancellation using static switch X-Hall probe bias technique

and is measured with ±1% reading accuracy using the Tektronix TCPA300 current probe. Table 5.2 projects the static experimental results along with possible data elaboration techniques to cancel the offset, the experiment was also done with AC switching of the bias and the results are almost coherent to those projected.

The grey region in the table5.2 projects the V_{probe} measurement results for the four phases at applied probe bias current $I_{bias} = \pm 500\mu A$ or ± 1-mA. The voltage values for $I_{IN} = 0$, of course, indicate the residual offset of the probe as no magnetic field is incident on it, while the V_{probe} values when I_{IN} is applied contain the Hall voltage element depending on the phase applied. One can also observe that the variation of the obtained V_H is proportional to the variation of the applied bias current and that we would require just 2 switch phases of bias current and no intermediate stage to compute the offset.

	$I_{bias} = 500\ \mu A$			$I_{bias} = 1\ mA$		
	V_{probe} (mV)			V_{probe} (mV)		
Phase	I_IN = 0 A	I_IN = 0.2 A	V_H (V)	I_IN = 0 A	I_IN = 0.2 A	V_H (V)
I ($V_H + \Delta V_{OS}$)	0.05	0.147		0.123	0.284	
II ($-V_H + \Delta V_{OS}$)	-0.015	-0.094		0.025	-0.12	
(I-II) / 2	0.0325	0.1205	0.088	0.049	0.202	0.153

Table 5.2: OFFSET CANCELLATION TECHNIQUE

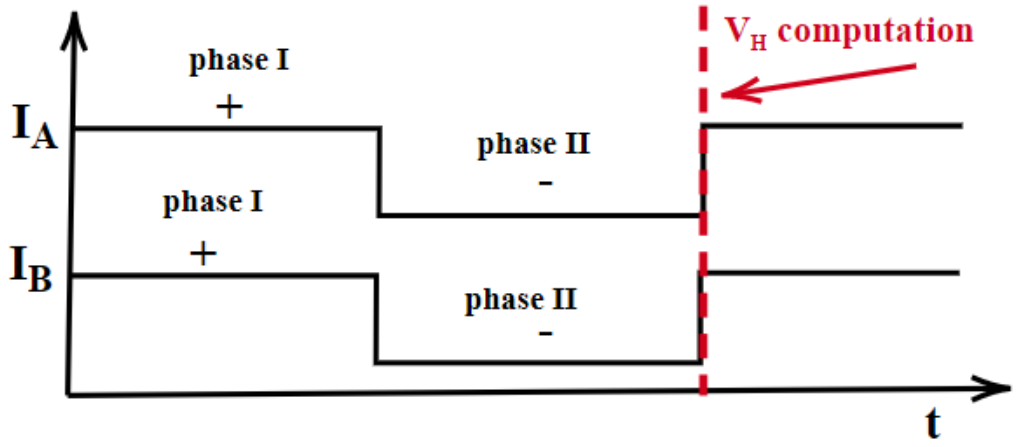


Figure 5.13: Illustration of the switched bias currents applied at a frequency, f in a sequence of phase I and IV and the computation of V_H using technique 1

This technique is very different compared to the conventional current spinning technique since we do not switch the bias contacts and swap with the sense contacts which electronically would require switching circuitry and add further the parasitic elements which impose a methodological limit on the bandwidth of the sensor. Instead, implementing this technique, the bias and sense contacts remain fixed and the bandwidth of the sensor would be limited only by the applied bias switch frequency For example, ideally considering the sensor's upper limit of the bandwidth to be 20 MHz, and we apply switch bias current at a high frequency of 20 MHz and use the chop like technique to extract V_H as illustrated in Fig.5.13, the bandwidth of the sensor would be halved to 10 MHz. The offset cancellation process is a necessary evil for the

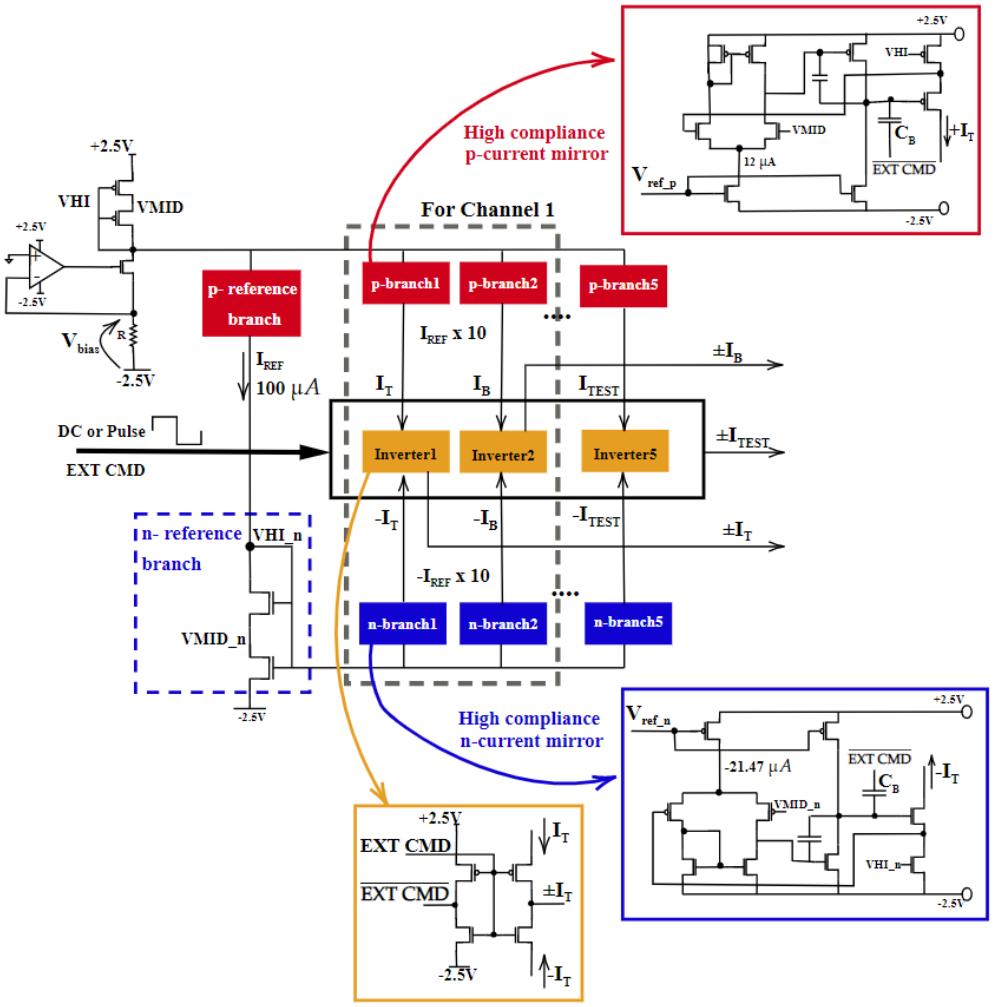


Figure 5.14: Schematic of the Hall bias circuitry that supports pulsed/ switched internal biasing for the X-Hall probe by responding to an external command provided by the user.

Hall sensor and with this technique, we trade-off the bandwidth yet again, but the limit is dependent on the frequency of switching the bias current and smart AFE designing instead of the switch parasitics as seen in spun Hall sensors.

5.4.2 Switched Hall bias circuit

The Hall bias scheme used in CH09 was redesigned for CH100 to facilitate pulsed or switched bias currents instead of constant dc bias to the two

terminals (T and B) of the X-Hall probe. A self-biased reference generator with startup creates the bias currents required by all the 5-V modules except for the bias currents used to polarize the X-Hall probe. Fig. 5.14 gives an abstract view of the designed Hall bias scheme for a single channel sensing chain. A resistive V to I converter connects to 5-branched high-compliance p and n current mirrors. The p and n reference branches generate a reference current of $100\mu A$ which is then multiplied by a factor of 10 by their respective branchx (x = 1 to 5), each interfaced to a corresponding CMOS inverter to generate the bias currents of $\pm I_T, \pm I_B$ and $\pm I_{Test}$. The first two, bias the T and B terminals of the X-Hall probe respectively, while $\pm I_{Test}$ is meant only for functionality testing and user monitoring of the bias currents to the probe. Each p(n) branch comprises of a single-ended n-mos(p-mos) differential pair, biased with a current of around 12(-21.4) μA which is a result of the multiplication of the reference bias current from the startup circuitry. From a layout point of view, the branches have been placed very close to each other to obtain optimal matching. An external command, EXT CMD, either pulse voltage at a set frequency or a constant dc voltage must be provided by the user to activate the biasing, and that dictates the polarity of the currents to the probe terminals, to be either positive or negative. During switching between EXT CMD pulses, the opamp in the inactive branch enters saturation and therefore requires a certain recovery time to reach its operating point when it is commanded to an active state. This is hastened by a 5-V p-well bootstrap capacitor which is connected from the output of the opamp driving the current mirror load and inverter circuit, to provide the necessary charge to force the opamp out of saturation.

Fig.5.15 shows the transient response of the new optimized system to a high-frequency emulated input current pulse with a time period of 1 μs when the Hall probe is biased in a conventional way with no current switching. The delay in the response time is 19.5 ns and the V_{pk-pk} of the output differential signal is 691 mV. Fig.5.16 shows the transient response of the system when switched biasing is applied. In this case, the EXT CMD triggered the Hall bias circuitry in such a way that there was no delay in terminal currents, I_T and I_B and both were of the same frequency. It can be observed that

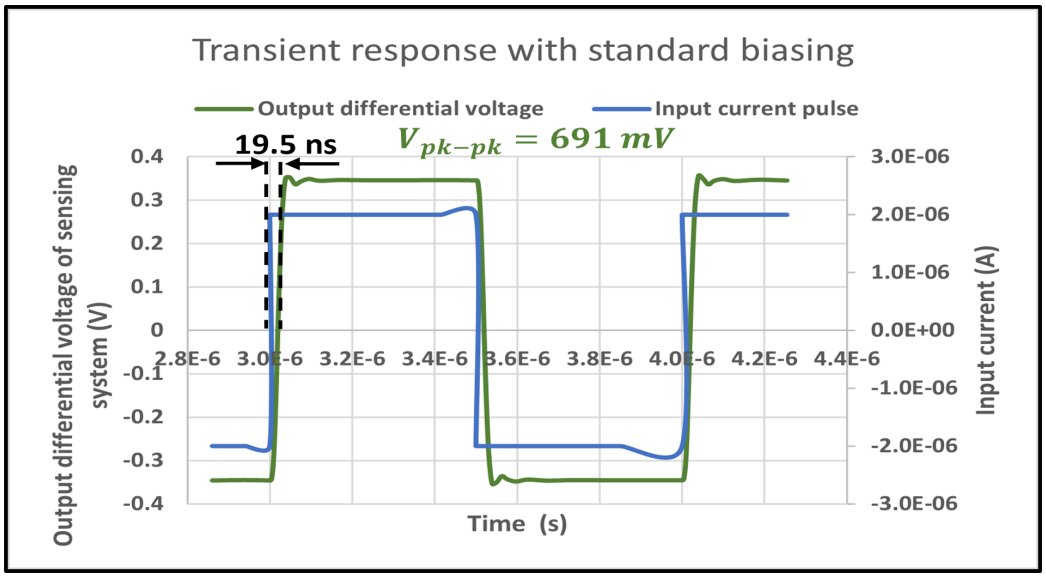


Figure 5.15: Transient response of a single channel sensing chain when the X-Hall probe is biased in a standard way with positive dc currents of 1-mA at the B and T terminals. The delay in the response is 19.5 ns

the positive and negative Hall bias currents take at least 500 ns and 700 ns to reach their steady state after which the sensor responds. This imposes a limit on the frequency of switching the bias currents and hence also on the bandwidth of the sensor when offset compensation techniques as discussed earlier are applied. This is mainly as discussed, due to the saturation of the gain boost operational amplifier used with the bias mirror in the p and n-branches and therefore, will be unable to respond to the high-frequency switch command signals rapidly and so must be designed with higher bandwidth.

5.5 Common mode control amplifier

Finally, the common mode voltage control amplifier in CH100 was replaced by a high gain, wide voltage swing folded cascode architecture as shown in Fig.5.17 (from STMicroelectronics, due to time constraints) to com-

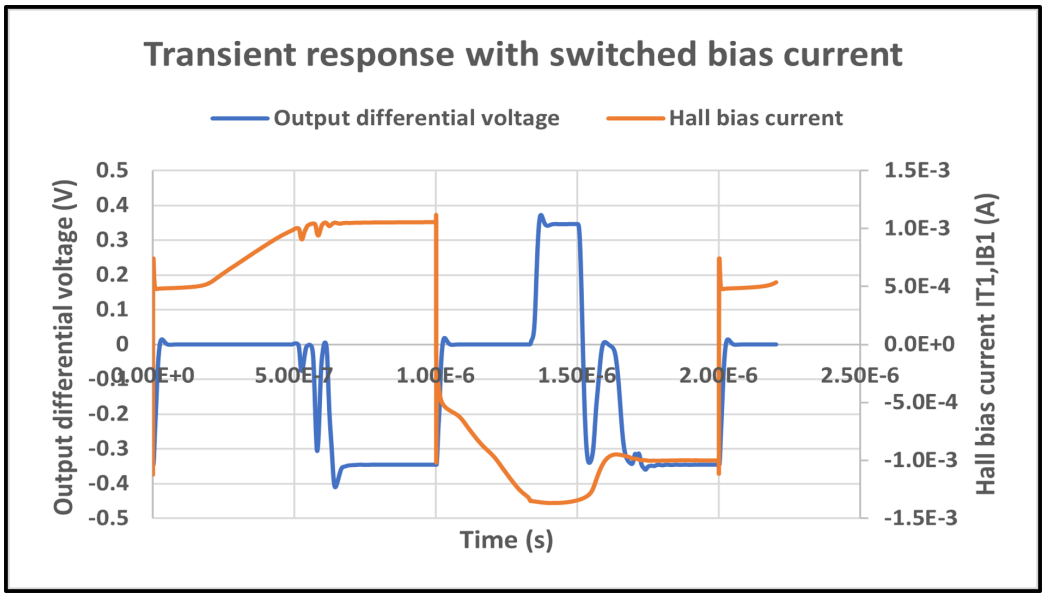


Figure 5.16: Transient response of a single channel sensing chain when the X-Hall probe is subjected to switched bias current pulse of T = 2μs. The sensor response to an emulated input current pulse of T= 1us is also shown

ply with the switching of Hall bias and fulfill its purpose of forcing the common mode voltage of the Hall probe to ground as discussed in section4.2.3. When the bias currents are sourced into the terminals of the X-Hall probe, the voltage variations at the common mode amplifier output tend towards the negative side of the rail voltage and vice versa when the bias terminals source the current out of the probe. This means the amplifier must have a high output voltage swing requirement on either side of the supply and in our case approximately is, -1.4 V/+1.4 V. The opamp used meets the output voltage swing requirement with -1.3 V/+2.49 V and a DC gain of about 122 dB. It was designed for a bias current of 450 μA which is too high for our application and so we reduced it to 1 μA and do not use the amplifier to its full capacity. The bandwidth is not a constraint and is a few hundred kHz.

5.6 Implementation

The proposed architecture was implemented using the 90-nm technology provided by ST microelectronics. The total chip area is the same as that

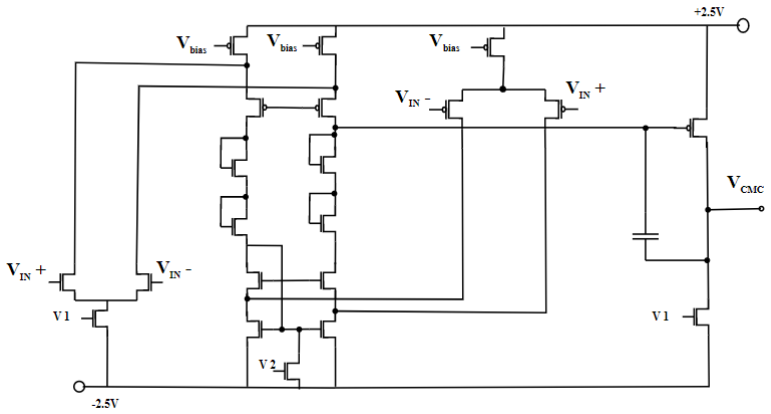


Figure 5.17: Source: STMicroelectronics. Double input folded cascode amplifier for Common Mode Control

of CH09 of 2.4 mm^2, however the estimated power consumption is 55 mW for the entire differential current sensing system. The layout of the designed chip can be seen in Fig.5.18.

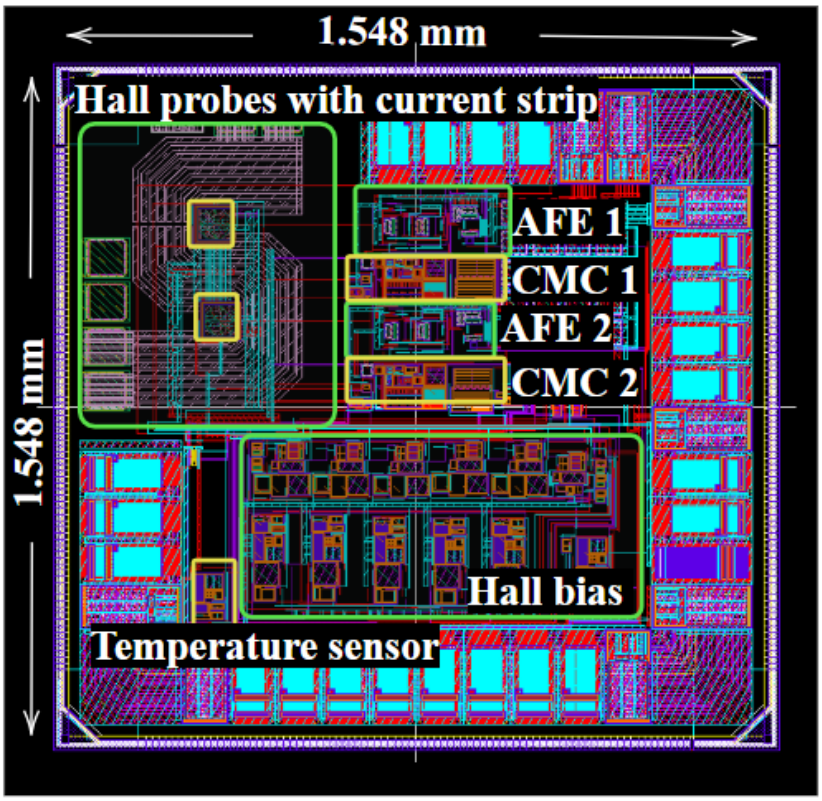


Figure 5.18: Layout of the chip CH100

Chapter 6

Conclusions

The objective of this thesis was to demonstrate the ideas and possibility of designing and implementing broadband Hall sensors for high frequency integrated power electronic applications. The thesis discusses in detail the background of HECS and the state of the art and the challenges to achieving high acquisition bandwidth. The research outcomes and microelectronically designed chips: CH09 with experimental characterization, and CH100, an enhanced version of CH09 with preliminary results are further discussed. The results excel the state of the art, are very encouraging and promising a bright scope for Hall sensors in power electronic applications.

Personal contributions: The entire project was carried out in collaboration with STMicroelectronics utilizing its resources within the joint research laboratory of the University of Bologna, and under the guidance of my supervisors. I contributed to the theoretical validation through simulations, the design of the electronic front ends, the design and layout of the PCB prototype with experimental characterizations. The layout of the chips is a combined work of me and my supervisor Prof. Marco Crescentini.

6.1 CH09: X-Hall sensor in current mode

In this work, we demonstrated a broadband dual-supply integrated current sensor for measuring currents in the Ampere range. The broadband

capability of the sensor is granted by the X-Hall architecture operated in current mode, which removes the methodological bandwidth limit of the SCT and reduces the effects of parasitic capacitances at the probe-AFE interface. The analog front-end is realized by a resistive feedback TIA supplied at the lower power domain of 1.2 V to exploit the fastest transistors. A common-mode control circuit is used to align the CM voltage of the X-Hall probe and the TIA, which are connected to different power domains. The sensor features a remarkable performance with a maximum acquisition bandwidth of 12 MHz, a resolution of 39.16 mA_{rms}, and a power consumption of 11.46 mW, leading to a Figure of Merit 25 times better than the state of the art. The input DC sensitivity of the prototype is 120.1 mV/A and 62.7 mV/A based on the selected transimpedance gain. The probe sensitivity is calculated as about 8% T^{-1}, assuming the current to magnetic transduction G_{ib} follows the simulated value of 7.5 mT/A. The prototype also shows good input-referred offset, which is granted by the high value of G_{ib} provided by the S-shaped copper trace realized on the top metal layer. To compare with the state-of-the-art Hall sensors, we use the conventional Figure of Merit also used in [40] which is the ratio of the bandwidth of the system and the product of the square of the resolution of the sensor referred to its main input and the total system power consumption and is expressed as:

$$FoM = \frac{BW(MHz)}{Resolution(A_{rms})^2 \cdot Power(mW)} \tag{6.1}$$

Table 6.1 summarizes at a glance, the performance of the state-of-the-art Hall sensor designs. The purely Hall based sensor proposed in this work achieves the highest bandwidth with a low power consumption and the highest FoM without using SCT. It can also be observed that, as a necessary trade-off, the performance in terms of magnetic offset is not the best reported and would need to be improved if the application targets a high Ampere measurement range in which case, the current strip cannot be integrated into the silicon chip affecting the G_{ib}. Due to the limitations in the wire-bonding procedure of the prototype, the measured current range for now was restricted to 800 mA and this will be addressed in future designs

Table 6.1: STATE OF THE ART COMPARISON

Parameter	this work	[46]	[136]	[40]	[137]	[39]	[22]	[141]	[142]
Supply voltage (V)	5/1.2	5	3.3	1.8/3.3	3.3	1.8	1.8	1.8	3.3
Sensor type	X-Hall	X-Hall	Hall	Hall +coil	Hall	Hall +coil	Hall +coil	Hall	Hall
Spin/chop	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Mode	Current	Voltage	Current	Voltage	Voltage	Voltage	Voltage	Current	Voltage
Tech node (μm)	0.09	0.16	0.18	0.18	0.35	0.18	0.18	0.18	N.A
Area (mm^2)	2.4	4	1.54	4.6	N.A	2.74	3.17	1.16	N.A
Sensor BW(MHz)	12/10	4	0.03	1.8	1.7	15.3	75	0.01	1
Power (mW)	11.46	27.5	15.4	19.5	13.2	63.5	33.7	0.12	N.A
Resolution (mA_{rms})	39.16 (293 μT)	75	(52 μT)	64	480	710	150	N.A	100
I_{OS} (mA)	224* (1.68 mT)	280	(100 μT)	268.5	279*	N.A	N.A	(50 μT)	N.A
FoM (MHz/A^2_{rms}mW)	569**	25.8	N.A	22.5	1.02	0.48	99	N.A	N.A

* The I_{OS} is indicated for one tested chip sample, while the values indicated in SOTA are computed for a mean over samples.
**The lower limit of BW is used for computation of FOM

by opting for a stud-bump mount. Moreover, as previously discussed, the architecture would benefit from a temperature compensation scheme to cope with the temperature drift of the Hall sensitivity and offset. The widening of the bandwidth allows the detection of fast transients, and moves a further step towards the development of integrated power systems operating at high switching frequencies, and to new applications in smart metering like non-intrusive load monitoring. However, it is still limited by the inductive parasitic effect, which has been minimized but unsolved. Despite the presence of the parasitic effect, the sensor has been validated in the acquisition of fast current pulses, reporting a delay of the sensor response of only 25 ns, comparable to the trail edge of the current pulse. Lead-free packages with flip-chip assembly (stud-bump method) which will be used for the enhanced version (chip CH100) should completely resolve the problem of the parasitics and the input current range that for now limit the practical usability of the sensor. This will be investigated in the future.

6.2 CH100: X-Hall sensor for accuracy

This chip proposes to overcome the limitations of CH09 in terms of accuracy and also proposes a novel residual offset cancellation scheme. Preliminary results show an improvement in the thermal drift of the gain by a factor of 8 with a relative gain variation of less than 0.7 dB in the temperature range of -20 to 100, which was facilitated by using an unsilicided P+ resistor on substrate for feedback in the TIA. The same also applies to an improvement in the thermal drift of offset in a relative analysis. The scheme also proposes gain calibration using an inbuilt temperature sensor within the chip with the estimated post-calibration accuracy to be better than 1%. An improved input current range of 5-A was targetted by aiming for lead-free implemention using stud-bump mount for the chip. The TIA was optimized to obtain nearly 30% reduction of the integrated input referred noise of 26.69 nA_{rms} at the probe-AFE interface and an estimated resolution of 39 mA_{rms} in the frequency band of DC - 30 MHz band, as well as an enhancement in the upper bandwidth limit of the system to be 26.87 MHz for $R_F = 90\ k\Omega$ trading off with current consumption. A novel residual offset cancellation technique was proposed which requires switching the polarities of the X-Hall bias currents without switching between bias and sense contacts and so the Hall bias was redesigned to generate pulsed currents. This preserves the possible practical bandwidth limit to the design of the AFE and the frequency of applied bias currents instead of the parasitics induced by switching circuitries as in SCT. Under a standard biasing scheme, the transient delay in the response is 19.5 ns. A high output voltage swing CMC amplifier unit from STMicroelectronics was used for common mode voltage control complying with the switched bias scheme. The chip incorporates a differential sensing scheme with dual sensing chains as an option to cancel common mode interferences. The overall chip area is 2.4 mm^2 and total power consumption of 55.6 mW. This will not be a problem for now as the primary goal of the chip is to demonstrate in future the accuracy and offset cancellation ideas.

The power consumption can be improved with optimized design of the Hall bias and the Common mode control amplifier.

List of Tables

List of Figures

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