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MODELS AND SIMULATIONS OF DIAMOND-LIKE CARBON FOR LARGE-AREA HIGH-VOLTAGE POWER DIODES

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Abstract

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Doctor of Philosophy

Models and Simulations of Diamond-like Carbon for large-area high-voltage Power Diodes

by Luigi BALESTRA

Silicon-based discrete high-power devices need to be designed with optimal performance up to several thousand volts and amperes to reach power ratings ranging from few kWs to beyond the 1 GW mark. To this purpose, a key element is the improvement of the junction termination (JT) since it allows to drastically reduce surface electric field peaks which may lead to an earlier device failure. This thesis will be mostly focused on the negative bevel termination which from several years constitutes a standard processing step in bipolar production lines. A simple methodology to realize its counterpart, a planar JT with variation of the lateral doping concentration (VLD) will be also described. On the JT a thin layer of a semi insulating material is usually deposited, which acts as passivation layer reducing the interface defects and contributing to increase the device reliability. A thorough understanding of how the passivation layer properties affect the breakdown voltage and the leakage current of a fast-recovery diode is fundamental to preserve the ideal termination effect and provide a stable blocking capability. More recently, amorphous carbon, also called diamond-like carbon (DLC), has been used as a robust surface passivation material. By using a commercial TCAD tool,

a detailed physical explanation of DLC electrostatic and transport properties has been provided. The proposed approach is able to predict the breakdown voltage and the leakage current of a negative beveled power diode passivated with DLC as confirmed by the successfully validation against the available experiments. In addition, the VLD JT proposed to overcome the limitation of the negative bevel architecture has been simulated showing a breakdown voltage very close to the ideal one with a much smaller area consumption. Finally, the effect of a low junction depth on the formation of current filaments has been analyzed by performing reverse-recovery simulations.

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Chapter 1

Preliminaries

A semi-classical description of the charge transport in power semiconductor devices can be addressed by using the drift-diffusion model. It can be derived starting from the Maxwell equations and assuming that the current density can be written as the sum of a drift and a diffusion term. The first one simply accounts for the Ohmic conduction and is thus proportional to the electric field. The second one models the movement of charges from the region with higher carrier concentration to the region with lower concentration. The main generation-recombination process are also discussed with a special focus on the impact-ionization generation which is responsible for the strong increase of the leakage current in power diode subjected to high reverse bias. The one-dimensional pn junction is then briefly described and the different conduction regions are illustrated.

1.1 Drift-Diffusion Model

The drift-diffusion model can be derived from the Maxwell's equations [1]:

$$\nabla \cdot \boldsymbol{D} = \rho, \qquad \nabla \times \boldsymbol{H} = \frac{\partial \boldsymbol{D}}{\partial t} + \boldsymbol{J} \tag{1.1}$$

$$\nabla \cdot \boldsymbol{B} = 0, \qquad \nabla \times \boldsymbol{E} = -\frac{\partial \boldsymbol{B}}{\partial t} \tag{1.2}$$

and the constitutive relations:

$$\boldsymbol{B} = \mu \boldsymbol{H}, \qquad \boldsymbol{D} = \varepsilon_S \boldsymbol{E} \tag{1.3}$$

where ρ is the charge density, $\boldsymbol{J}$ is the current density while μ and ε_S represent the magnetic permeability and the dielectric permittivity, respectively. Taking the divergence of the second equation in (1.1) and remembering that $\boldsymbol{\nabla} \cdot \boldsymbol{\nabla} \times \boldsymbol{H} = 0$, the result is:

$$\frac{\partial \rho}{\partial t} + \boldsymbol{\nabla} \cdot \boldsymbol{J} = 0 \tag{1.4}$$

which is called continuity equation of the carrier density.
Eq.1.4 can be rewritten as two different continuity equations, one for each type of charge carriers [2] [3]:

$$\frac{\partial n}{\partial t} - \frac{1}{q} \boldsymbol{\nabla} \cdot \boldsymbol{J}_n = W_n \tag{1.5a}$$

$$\frac{\partial p}{\partial t} + \frac{1}{q} \boldsymbol{\nabla} \cdot \boldsymbol{J}_p = W_p \tag{1.5b}$$

Where n (p) is the electron (hole) concentrations and $\boldsymbol{J}_n$ ($\boldsymbol{J}_p$) is the electron (hole) current density. W_n is the difference between the number of electrons entering and leaving the conduction band. It can be expressed ad the difference between the generation and recombination rates of electrons $W_n = G_n - U_n$. Similar consideration can be applied to $W_p = G_p - U_p$. Assuming that the different generation recombination processes are uncorrelated and taking the steady state approximation for the trap populations, one finds:

$$U_n - G_n = U_p - G_p = U_{SRH} + U^{AI} + U^D \tag{1.6}$$

Where U_{SRH}, U^{AI} and U^D represent the net recombination rates associated to the thermal recombination, the Auger recombination together with the

impact-ionization generation, and photon- and phonon-induced direct transitions, respectively. Further details about U_{SRH} and U^{AI} are provided in the next Sections. U^D will be neglected since optical generation is not relevant for the purpose of this work. In addition, it has been assumed that direct phonon-induced transitions are negligible when compared to the trap-assisted counterpart (SRH). The electron and the hole current densities are expressed as:

$$\boldsymbol{J}_n = q\mu_n n\boldsymbol{E} + qD_n\boldsymbol{\nabla} n \tag{1.7a}$$

$$\boldsymbol{J}_p = q\mu_p p\boldsymbol{E} - qD_p\boldsymbol{\nabla} p \tag{1.7b}$$

Both mobility ($\mu_{n,p}$) and diffusion coefficient ($D_{n,p}$) depend on the electric field. However, under non-degenerate conditions (the Boltzmann statistics can be used as an approximation of the Fermi-Dirac distribution), the Einstein relationship relate the two quantities [4]:

$$D_{n,p} = \mu_{n,p}\frac{k_B T}{q} \tag{1.8}$$

where k_B is the Boltzmann constant and T the absolute temperature. The free carrier densities, using the Boltzmann approximation, can be expressed as:

$$n = N_C \exp\left(-\frac{E_C - E_{Fi}}{k_B T}\right)\exp\left(\frac{E_F - E_{Fi}}{k_B T}\right) = n_i \exp\left(\frac{E_F - E_{Fi}}{k_B T}\right) \tag{1.9}$$

$$p = N_V \exp\left(-\frac{E_{Fi} - E_V}{k_B T}\right)\exp\left(\frac{E_{Fi} - E_F}{k_B T}\right) = p_i \exp\left(\frac{E_{Fi} - E_F}{k_B T}\right) \tag{1.10}$$

where N_c and E_c are the effective density of states and the lower edge of the conduction band, respectively. Similarly, N_v and E_v are the effective density of states and the upper edge of the valence band, respectively. E_F is the Fermi level of the semiconductor. The electron concentration and the Fermi level indicated with n_i and E_{Fi} refer to a semiconductor free from impurities (intrinsic). It is worth nothing that $np = n_i^2$ independently from the position of

the Fermi level. Under non-equilibrium conditions, it is necessary to define two quasi Fermi potentials $E_{F,n}$ and $E_{F,p}$ for electrons and holes, respectively. The previous equations then become:

$$n = n_i \exp\left(\frac{E_{F,n} - E_{Fi}}{k_B T}\right), \tag{1.11a}$$

$$p = p_i \exp\left(\frac{E_{Fi} - E_{F,p}}{k_B T}\right), \tag{1.11b}$$

$$np = n_i^2 \exp\left(\frac{E_{F,n} - E_{F,p}}{k_B T}\right). \tag{1.11c}$$

Using the Einstein relations, the current density equations can be rewritten in a form more suitable for the numerical simulations of semiconductor devices:

$$\boldsymbol{J}_n = -\mu_n n \boldsymbol{\nabla} E_{F,n}, \tag{1.12a}$$

$$\boldsymbol{J}_p = -\mu_p p \boldsymbol{\nabla} E_{F,p}. \tag{1.12b}$$

The charge density of the Poisson equation can be expressed in terms of free carriers (electrons and holes) and ionized atoms coming from the addition of dopants inside the semiconductor:

$$\boldsymbol{\nabla} \cdot (\varepsilon_S \boldsymbol{E}) = \rho = q(p - n + N_D - N_A) \tag{1.13}$$

where N_D and N_A are the concentrations of ionized donor and acceptor, respectively. Equations (1.5), (1.12) and (1.13) constitute the drift-diffusion model.

1.2 Generation-recombination processes

Inter-band generation-recombination processes allow the transition of electrons from the valence to the conduction band and vice-versa. We can distinguish between direct and trap-assisted processes. In the former case, the transition occurs directly between the two bands (Auger recombination, impact ionization generation), while in the latter it is assisted by the presence of trap levels into the band gap which originate from defects in the lattice crystal of the semiconductor (Schockley-Read-Hall theory).

1.2.1 Schockley-Read-Hall recombination

It describes the trap-assisted thermal recombination assuming the presence of a single trap level with energy E_t and steady state condition. If more than one level is present, the contributions of the individual levels should be summed at the end of the calculation (tunnelling between different trap levels is also neglected). However, it can be shown that the most efficient value of E_t is located approximately at the mid-gap. The other trap levels can then be neglected. It is usually expressed as:

$$U_{SRH} = \frac{np - n^{eq}p^{eq}}{\tau_{p0}(n + n_B) + \tau_{n0}(p + p_B)} \tag{1.14}$$

Where n^{eq} (p^{eq}) and τ_{n0} (τ_{p0}) are the electron (hole), equilibrium concentration and lifetimes respectively while:

$$n_B = \frac{n^{eq}}{d_t} \exp\left(\frac{E_t - E_F}{k_B T}\right), \qquad p_B = d_t p^{eq} \exp\left(\frac{E_F - E_t}{k_B T}\right). \tag{1.15}$$

d_t is the degeneracy coefficient of the trap. An excess of np with respect to equilibrium indicates that recombinations prevails over generation, and vice-versa.

1.2.2 Auger recombination and impact ionization

Two electrons into the conduction band may collide and exchange energy. If at the end of the collision one of the electrons exhibit a loss of energy equal or greater than the energy gap and it can experiences a transition into an empty state of the valence band. The other electron acquires the same amount of energy and gains a higher-state of the conduction band. This process is usually called Auger recombination initiated by electrons. Analogue considerations can be made for a collision between two holes into the valence band.
Impact-ionization transitions occur when an electron whose initial state is into the conduction band at high energy, collides with another electron whose initial state is in the valence band. After the collision, the first electron is still in the conduction band but with a lower energy, while the second one acquires enough energy to a transit into the conduction band. This process is called impact-ionization initiated by electrons. The net recombination rates due to Auger recombination and impact-ionization generation can be expressed as:

$$U_n^{AI} = c_n n^2 p - I_n n, \qquad U_p^{AI} = c_p p^2 n - I_p p \tag{1.16}$$

Where U_n^{AI} and U_p^{AI} refer to electron and hole-initiated transition, respectively. c_n and I_n are called Auger recombination and impact-ionization generation coefficients for electrons. Analogue considerations can be made regarding c_p and I_p for holes. At the equilibrium, we must have $U_n^{AI} = U_p^{AI} = 0$ which implies $I_n = c_n n^{eq} p^{eq}$, $I_p = c_p n^{eq} p^{eq}$. Not too far from the equilibrium the Eqs. 1.16 can be rewritten as.

$$U_n^{AI} = c_n n(np - n^{eq} p^{eq}), \qquad U_p^{AI} = c_p p(np - n^{eq} p^{eq}) \tag{1.17}$$

The probability that two electrons in the conduction band or equivalently two holes in the valence band can collide is usually low at room temperature since the probability of a collision of a charge carrier with phonons is much higher. The Auger recombination become relevant only when the carrier concentration is very high. On the contrary, the carrier generation due to impact-ionization occurs only when an electron or a hole acquires an energy larger than the energy gap. This can happens only in presence of a strong electric field which provides a sufficient amount of energy to the charge carrier over a distance much shorter than the average collision-less path. To summarize, Auger recombination is dominant in heavily doped regions with a high charge density, and as a consequence, low electric field, while Impact-ionization is dominant in regions with a low doping concentration and a high electric field [2].

Impact Ionization Coefficients Far from equilibrium, when impact ionization dominates over the other generation recombination process $U_n - G_n = U_p - G_p \approx U^{AI} \approx -I_n n - I_p p$. Under static conditions the continuity equations becomes

$$\boldsymbol{\nabla} \cdot \boldsymbol{J}_n = -qnI_n - qI_p p, \qquad \boldsymbol{\nabla} \cdot \boldsymbol{J}_p = qnI_n + qI_p p, \tag{1.18}$$

Assuming that the Ohmic term is dominant due to the high electric field yield to $\boldsymbol{J}_n \approx q\mu_n n\boldsymbol{E}$ and $\boldsymbol{J}_p \approx q\mu_p p\boldsymbol{E}$. Rewriting the current densities as $\boldsymbol{J}_n = J_n\boldsymbol{e}$ and $\boldsymbol{J}_p = J_p\boldsymbol{e}$ where $\boldsymbol{e} = \boldsymbol{E}/|\boldsymbol{E}|$, Eqs. 1.18 become:

$$-\boldsymbol{\nabla} \cdot \boldsymbol{J}_n = k_n J_n + k_p J_p, \qquad \boldsymbol{\nabla} \cdot \boldsymbol{J}_p = k_n J_n + k_p J_p, \tag{1.19}$$

where

$$k_n = \frac{I_n}{\mu_n |\boldsymbol{E}|}, \qquad k_p = \frac{I_p}{\mu_p |\boldsymbol{E}|}, \tag{1.20}$$

are called impact ionization coefficients.

Van Overstraeten model for the avalanche generation The impact ionization coefficients, k_n and k_p, can be modelled as exponential functions of the electric field as predicted by van Overstraeten-de Man model [5] which is based on the Chynoweth law [6]. It reads:

$$k_{n,p} = \gamma a_{n,p} \exp\left(-\frac{\gamma b_{n,p}}{E}\right) \tag{1.21}$$

with:

$$\gamma = \frac{\tanh\left(\frac{\hbar\omega}{2k_B T_0}\right)}{\tanh\left(\frac{\hbar\omega}{2k_B T}\right)} \tag{1.22}$$

where $\hbar$ is the reduced Plank constant. The factor γ expresses through the phonon energy $\hbar\omega$ the temperature dependence of k_n and k_p. The coefficients $a_{n,p}, b_{n,p}$ and ω have been measured for both electrons and holes by van Overstraeten and de Man using diffused silicon pn junctions [5].

1.3 The power p-i-n diode

Power diodes are needed in power electronics to control the direction of current flow in circuits. They are widely used for power conversion purpose such as rectifiers (AC-DC), or together with other components to create inverters (DC-AC) and choppers (DC-DC). The structure of the device is schematically represented in Fig.1.1a. Differently from low-power diode, a wide lightly doped region, called intrinsic or drift- region, is placed between the p and n regions in order to withstand high reverse voltage as shown in Fig. 1.1b where the vertical doping profile is reported.

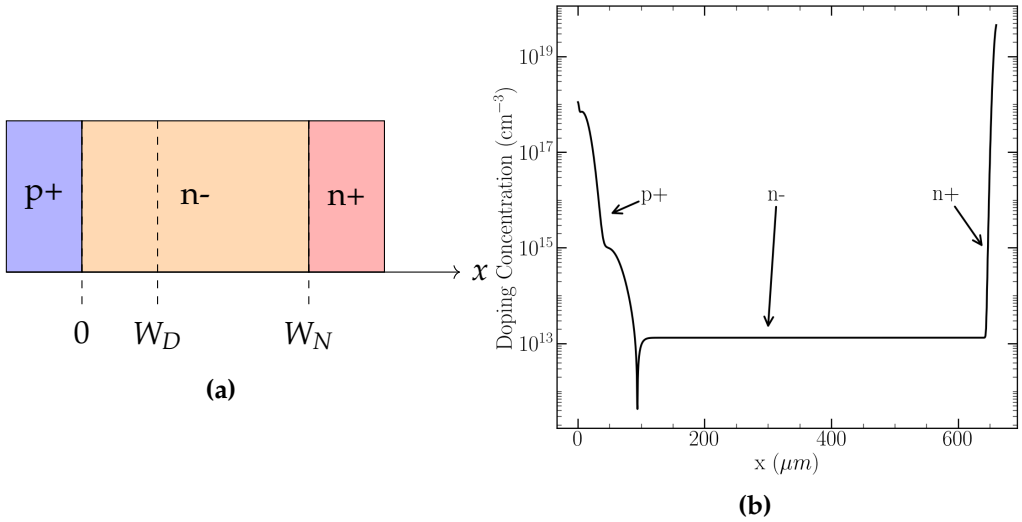


Figure 1.1: (a) Schematic representation and (b) vertical doping profile of a power diode

1.3.1 Forward Bias

The power-diode is forward biased when a positive voltage is applied to the anode and a negative one to the cathode. Following [7], the on-state current flow is dominated by three transport mechanisms:

- Recombination current: at very low current the transport is dominated by carrier recombination within the space-charge region of the p-n junction. In the depletion region, under the assumption that the electron and hole concentrations are equal [7]:

$$n = p = n_i e^{\frac{qV_a}{2k_B T}} \tag{1.23}$$

  Where V_a is the applied voltage and n_i the intrinsic carrier concentration. In addition, since the recombination centre is located at the mid-gap $p_B = n_B = n_i$. Substituting these relations in to Eq. 1.14 the SRH recombination rate can be rewritten as [7]:

$$U^{SRH} = \frac{n_i}{\tau_{n0} + \tau_{p0}} e^{\frac{qV_a}{2k_B T}}. \tag{1.24}$$

As a consequence, the current density is [7]:

$$J_{rec} = qU^{SRH}W_D = \frac{qn_iW_D}{\tau_{SC}} e^{\frac{qV_a}{2k_BT}}, \tag{1.25}$$

Where $\tau_{SC} = \tau_{n0} + \tau_{p0}$ and W_D is the depletion region width.

- Diffusion current: at low current density the transport is dominated by the diffusion of minority carriers injected into the drift region. Here, differently from low-voltage devices, the relation $N_A >> N_D$ holds due to the presence of the lightly doped drift region. For this reason, the minority carrier concentration on the p-side $n_{0P} = n_i^2/N_A$ is much smaller when compared with the n-side $p_{0N} = n_i^2/N_D$ and the diffusion current due to injection into the P-side can be considered negligible. The current density due to injection into the N-drift region is:

$$J_{TN} = \frac{qD_p p_{0N}}{L_p \tanh\left(W_N/L_p\right)} \left(e^{\frac{qV_a}{k_B}} - 1 \right) \tag{1.26}$$

In the above equation L_p is the hole diffusion length and W_N the width of the drift region.

- High-level injection current: the hole and the electron concentrations into the drift region are much higher than the background doping concentrations. This phenomenon is called *conductivity modulation* of the drift-region and it is fundamental to obtain a low on-state voltage drop in the power P-i-N rectifier. The current density is proportional to:

$$J \sim e^{\frac{qV_a}{2k_BT}}. \tag{1.27}$$

1.3.2 Reverse Bias and Breakdown Voltage

When the diode is reverse biased the space charge region expands according with the applied voltage. The leakage current can be calculated starting from the SRH recombination rate under depletion condition:

$$U^{SRH} = -\frac{n_i}{\tau_{SC}} \tag{1.28}$$

By integrating the continuity equation one gets:

$$J_{SC} = \frac{qW_D n_i}{\tau_{SC}} \tag{1.29}$$

Another contribution to the leakage current comes from the minority carrier accumulated in proximity of the junction. The total leakage current can then be expressed as:

$$J_{Leakage} = \frac{qD_p p_i^2}{L_p N_{DN+}} + \frac{qD_n n_i^2}{L_n N_{AP+}} + \frac{qW_D n_i}{\tau_{SC}} \tag{1.30}$$

The electric field and the depletion region width can be calculated by solving the Poisson equation in one dimension:

$$\frac{d^2\Phi}{dx^2} = -\frac{dE}{dx} = -\frac{Q(x)}{\varepsilon_S} = -\frac{qN_D}{\varepsilon_S} \tag{1.31}$$

Integrating this equation with the boundary condition that at the edge of the depletion region, i.e., $E(x = W_D) = 0$, reads:

$$E(x) = -\frac{qN_D}{\varepsilon_S}(W_D - x) \tag{1.32}$$

Integrating the previous equation with the boundary condition in the p+ region,i.e., equal to zero and using the condition $V(W_D) = V_a$, the thickness of

the depletion region width as function of the applied voltage can be calculated:

$$W_D = \sqrt{\frac{2\varepsilon_S V_a}{qN_D}} \tag{1.33}$$

The maximum value of the electric field at the p-n junction is

$$E_m = \sqrt{\frac{2qN_D V_a}{\varepsilon_S}} \tag{1.34}$$

The onset of the avalanche generation occurs when E_m reaches its critical value for breakdown (E_c). The breakdown voltage (V_{BD}) is then defined from the previous equation as:

$$V_{BD} = \frac{\varepsilon_S}{2qN_D} E_c^2 = \frac{E_C W_D}{2} \tag{1.35}$$

Punch-through diode Due to the conductivity modulation, the ON-resistance of the diode does not depend on the drift region doping concentration. For this reason, it is preferable to use a thinner depletion region with a reduced doping concentration. With this configuration, when the diode is reverse biased, for sufficiently high voltage, the depletion region reach the n+ region giving rise to a trapezoidal electric field distribution as shown in Fig. 1.2 where it is compared with the triangular distribution of a non punch-trough diode. The device failure occurs when the maximum value of the electric field is equal to the critical electric field E_c for the avalanche generation. The breakdown voltage can be written as:

$$V_{BD,Punch-through} = E_c W_D - \frac{qN_D W_D^2}{2\varepsilon_S} \tag{1.36}$$

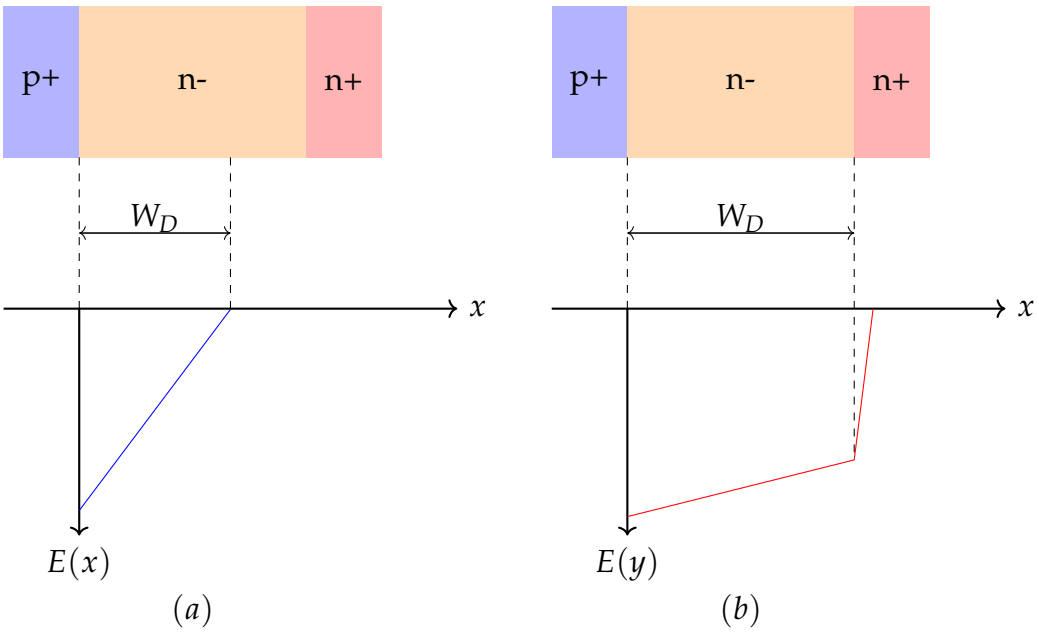


Figure 1.2: Electric field profile for a non punch-through diode (a) and a punch-through diode (b) under reverse bias condition. If $E(x = 0) = E_c$ the device failure occurs due to avalanche generation.

1.4 Junction termination and passivation Layer

In the previous sections, only one dimensional structures have been considered, assuming that all derivatives along the y and z axis vanish. However, all semiconductor devices have finite size since they are produced starting from large wafers which are sawed by using diamond coated blades. The sawing process results in to a significant damage of the crystal. If the sawing is performed across the junction that must support high voltage, crystal damages create high leakage current that degrades the blocking capability of the device. This problem can be solved in two different ways: (i) by using planar junction termination designed in order to move the depletion region far from the saw lines, (ii) by shaping the edge of the device. Historically, different technique have been developed from field plates and field p-rings to the bevel edge terminations. In the following sections the negative bevel termination and the planar termination with variation of the lateral doping will be described.

1.4.1 Negative Bevel Termination

Devices with a blocking capability above 2000V are required in power distribution applications. The current rating is usually very high for the devices due to the high power levels encountered in these applications. Consequently, these types of devices are manufactured with an entire wafer serving as a single device. In addition, in order to improve the breakdown voltage capability, it is advantageous to prepare deep diffusions with low surface concentration because this creates a graded doping profile at the junction which results into higher breakdown voltage when compared with the abrupt junction [3][7]. Due to the low diffusion coefficient of boron in bulk silicon, Aluminium is used to prepare deep junctions with low surface concentrations.
The process of bevelling consists of removal of silicon at the edges of the wafer at a precisely controlled angle. A negative bevel is defined as one in which the active area of the device decreases when proceeding from the lightly doped side to the highly doped side of the P-N junction. A schematic representation of a negative bevelled power diode with angle θ is shown in Fig. 1.3 where the dashed lines represent the edges of the depletion region. Inside the silicon bulk, it has length W_p on the p-side and W_n on the n-side. Along the bevel termination, the space charge region expands toward the anode and contracts on the n-side since, by cutting the wafer, more charge is removed from the p-side of the junction. This is depicted in Fig 1.3 where the red and the blue hatched areas represent the silicon (and then the charge) removed on the p-side and the n-side respectively. The doping concentration at the p-side is usually much higher when compared with the drift region leading to an increase of the surface electric field. The extension of the depletion region along the bevel (W_S) is given by:

$$W_S = \frac{W_P}{\sin(\theta)}. \tag{1.37}$$

However, by using a graded doping profile together with a very small grinding angle, the width of the space charge region can be significantly increased resulting even in a 5 times lower surface electric field when compared with the bulk one (Fig. 1.5). For $\theta = 0$, which means without termination, a strong electric field is present on the lateral edge of the device (Fig. 1.4) leading to surface discharge under reverse bias.

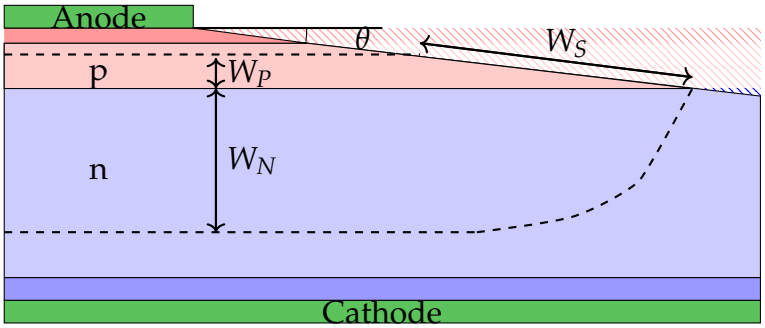


Figure 1.3: Schematic representation of a power diode with a negative bevel termination with a graded doping profile. Red and blue hatched areas represent the silicon (and the corresponding doped volumes) removed on the p-side and the n-side, respectively. As a consequence, the charge of the corresponding depleted region is removed through bevelling.

1.4.2 Juntion Termination Extension (JTE)

The junction extension technique is complementary to the above described bevel termination. While the latter is based on selectively removing charge from both sides of the junction, the former consists in selectively adding charge into the junction termination (Fig. 1.6). The charge implanted within the JT must be controlled in order to obtain a breakdown voltage very close to the optimal one. If the charge is too small, the breakdown occurs close to the edge of the active region of the diode due to the curvature of the cylindrical junction (point A). If it is too high, the JT would not be depleted and the electric field peak is located at the end of the termination doping profile due to the curvature of the aluminium doping profile of the JT (point B). A simple

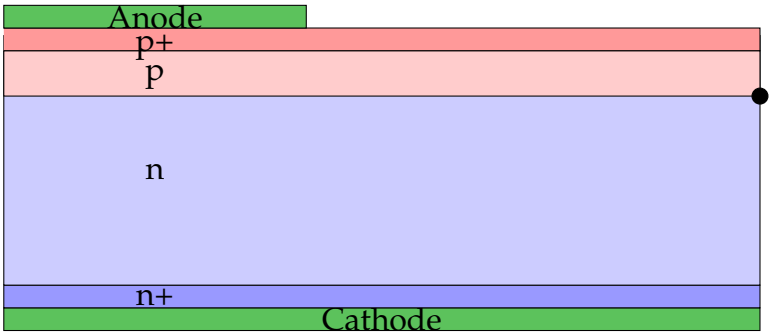


Figure 1.4: Schematic representation of a negative bevel power diode with $\theta = 0$. The black dot shows the location of the electric field peak at the surface.

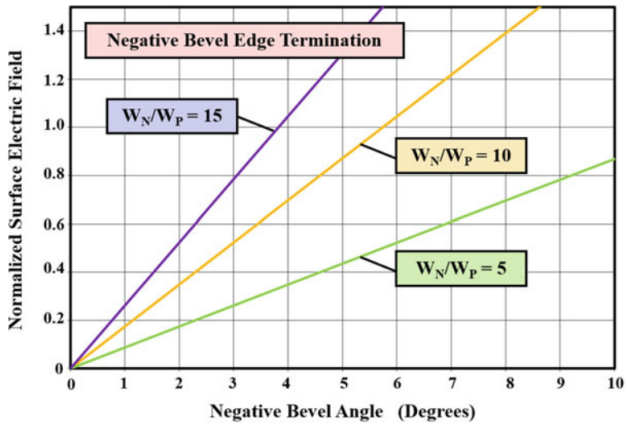


Figure 1.5: Ratio between the maximum electric field along the JT and the maximum electric field in the silicon bulk as function of the bevel angle θ [7]

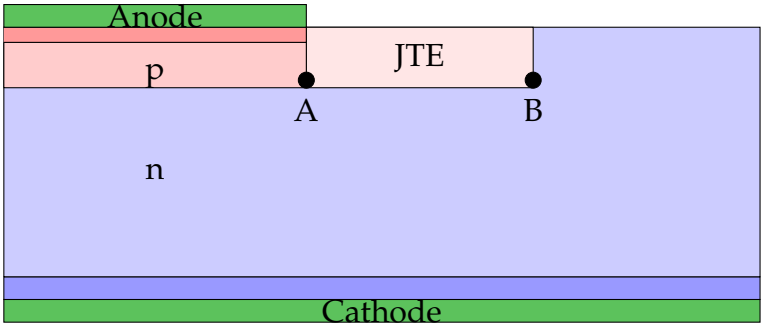


Figure 1.6: Schematic representation of a power diode with a junction termination extension

technique to find the ideal value of the implanted charge will be provided in chapter 3.

1.4.3 Passivation Layer

The surface damage produced by bevelling results in the presence of mobile charge that can lead to alterations of the electric field at the edges of the devices. The damage is firstly removed by chemical etching followed by the deposition of a thin layer of a semi-insulating material which passivates the remaining surface defects and improve the blocking capability stability. The presence of fixed charge inside the passivation layer can modify the width of the depletion region at the Si/Passivation interface affecting the breakdown voltage. In addition, if its conductivity is comparable to that of a depleted silicon, it can provide an additional path for carrier. Recently, diamond-like carbon (DLC) has been proposed as one of the most promising passivation materials due to its unique electrical and mechanical properties. A detailed description of the DLC features is provided in the following chapter.

1.5 Numerical simulations of semiconductor devices

The drift-diffusion model described so far can be solved analytically only in a few simple cases, like the one-dimensional pn-junction shown in the previous sections. On the contrary, when the complexity of the device geometry increases, numerical simulations are fundamental to understand the effects of each physical model on the behaviour of the device. Different software suites are today available to reproduce the different levels of abstraction, they include: process, device and circuit simulations. With process simulations, the ion implantation and the dopant diffusion can be reproduced together with oxidation, etching and lithography steps. The outcome of the simulations contains the device geometry and the doping profile of the device under investigation. However, when the details of the fabrication processes are not relevant to the device analysis, the structure of the device can be recreated in the simulator without process simulations, provided that the

geometry is known and that the doping profiles have been measured. This is usually achieved by using specific tools available into the software suite. The recreated device geometry and doping profiles are then used as input for the device simulations in which the drift-diffusion model is solved numerically. The device is divided into a discretized structure called mesh. Thus each differential equation of the system is solved at each of the mesh vertices. The Poisson equation and the transport equations for electrons and holes are solved iteratively until the convergence is achieved. The current-voltage (I-V) and capacitance-voltage (C-V) characteristics can thus be simulated and compared against measurements performed on real devices. Once all the physical models of the device are well calibrated, the outcome of device simulations serves as input to create a compact model which can be used in circuit simulations. They are usually carried out with a SPICE simulator where a system of non-linear differential algebraic equations is solved. The solution of such simulations provides the branch voltages and the nodal current of the circuit.

In this work, the commercial suite provided by Synopsys Inc. has been used. Process simulations have not been considered since all the information about geometry and the doping profile were already available. Sentaurus Structure Editor has thus been used to define the device and the mesh structure. The electrical characteristics have been simulated through Sentaurus Device which solves numerically the drift-diffusion model. To conclude, there is no need to create a compact model of the device under investigation since the effects of the passivation layer can be accounted for by using the already existing model for power semiconductor diodes.

Chapter 2

Diamond-Like Carbon

Diamond-Like Carbon (DLC) is a metastable form of amorphous carbon containing a significant fraction of sp^3 bonding. It has outstanding electrical, mechanical and thermal properties. It has a wide range of applications such as biomedical coating and micro-electromechanical devices (MEMs) [8].

2.1 Physical and chemical properties

Carbon is located in the fourth group of the periodical table and as such it has four electrons in the valence band that can form bonds with other atoms. According to the Valence Shell Electron Pair Repulsion theory (VSEPR) carbon atoms can organize themselves in three different hybridizations:

- sp^3: as in diamond, each valence electron makes a bond with a different adjacent atom giving rise to four strong σ bonds.
- sp^2: as in graphite, three of the four valence electrons makes σ bonds located on the same plane. The fourth electron makes a π bond which lies in a plane normal to the σ ones.
- sp^1: 2 electrons form σ bonds along the $\pm$ x-axis while the other two electrons make π bonds in the y and z directions.

All C-C and C-H σ bonds give rise to occupied states in the valence band and empty σ^* in the conduction band separated by a wide energy gap as

in diamond. On the contrary all sp^2 and sp^1 sites form filled π bonds and empty π^* bonds separated by a narrower gap. Based on the assumption that

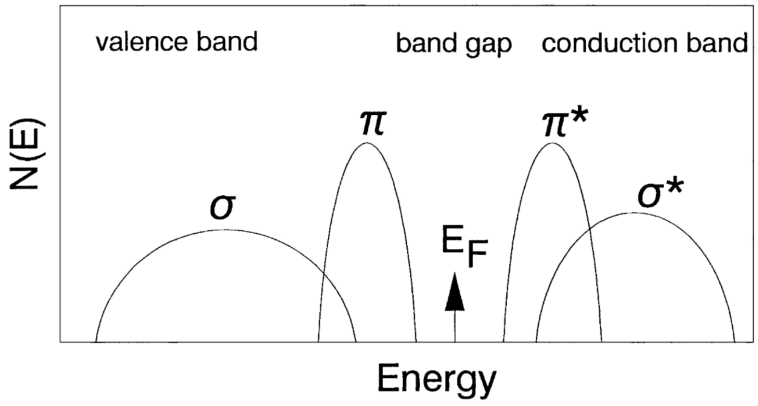


Figure 2.1: Schematic DOS of a carbon showing σ and π states [8].

the interaction between σ and π bonds is small since they lie on orthogonal plane and involves very different energy ranges, it is possible to describe the DLC structure with the so called cluster model. Within this model, DLC can be approximately described as a lattice of sp^3 hybridized carbon atoms with some clusters of sp^2 carbon atoms. Clustering of sp^2 sites results in an energy gain when compared with randomly distributed sp^3 and sp^2 sites. A schematic of sp^2 clusters is shown in Fig. 2.2 The cluster formation occurs

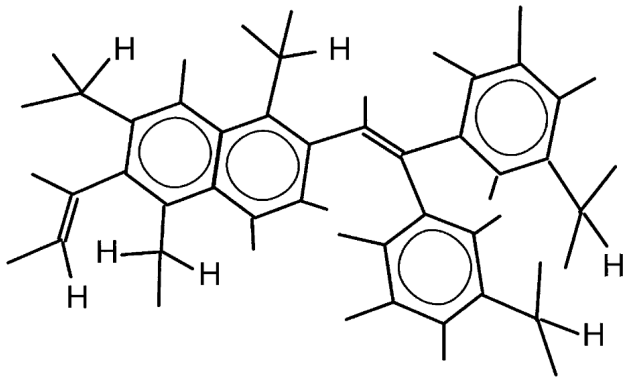


Figure 2.2: Schematic of sp^2 clusters in a-C:H [8].

according to the following rules:

- Each cluster has an even number of π orbitals

- A pair of sp^2 sites tend to align their π states to maximize the interaction, as in ethylene
- more than two sp^2 sites tend to form planar clusters
- three pairs of C=C bonds organize themselves into a six-fold ring, as in benzene
- Six-fold benzene-like rings tend to form graphitic sheets

The energy band gap depends on the sp^2 states and varies inversely with the cluster diameter d_C.

$$E_g \propto \frac{1}{d_C} \tag{2.1}$$

However, the cluster size calculated from energy gap measurements is largely overestimated for as-deposited DLC. It has been found that the sp^2 are arranged also in olefinic clusters in addition to graphitic ones. According to [9], the cluster model is valid for the case of low disorder limit which is typical of annealed DLC.

Doping of DLC layers Differently from silicon. DLC is intrinsically a p-type semiconductor since its Fermi level lies just below the midgap. However, during the deposition, impurities can be added with the aim to control the conductivity and the polarization of the material. As in a traditional semiconductor, both n-type and p-type doping can be realized by using nitrogen or boron, respectively. nitrogen doping promotes the formation of sp^2 cluster and an increase of the existing cluster size. Electrical characterizations have shown different behaviours depending on the deposition processes: (i) a monotonic increase of the DLC conductivity due to a reduction of the band gap instead of a Fermi level shift, (ii) the conductivity as a function of the doping concentration shows a minimum which corresponds to a shift of the Fermi level toward the conduction band. The minimum occurs when the

Fermi level crosses the mid-gap. In addition, not all nitrogen atoms occupy a substitutional position as it has been confirmed by the presence of rings with a lone pair of electrons such as pyridine and pyrrole which are not doping configurations but are characterized by an electric dipole different from zero. The band structure of DLC is profoundly modified by the presence of nitrogen giving rise to a very high concentration of states close to the Fermi level [10]. The current density measured as function of the applied voltage usually shows an exponentially increasing conductivity with a dependence from the electric field nicely described through the Poole-Frenkel (PF) model [11]. A detailed explanation of the PF mechanism is given in Chapter 3.
Boron doped DLC has been much less studied. However, most of features are similar to those previously described for nitrogen such as the increase of defects and the Poole-Frenkel hopping conduction. The role of different doping type for the present case will be described in the following sections.

2.2 Diamond-Like Carbon Characterization

In order to understand the basic properties of a DLC layer, Metal-Insulator-Metal (MIM) and Metal-Insulator-Semiconductor (MIS) structures have been realized and characterized by ABB Switzerland Ltd Semiconductors. Metal-DLC-Silicon devices were prepared as follows. Phosphorus was diffused from backside to create good ohmic contact, followed by Al or Pt evaporation and sintering (Fig.2.3, bottom-left). Boron was diffused from backside (B-spray) to create good ohmic contact, followed by Al evaporation and sintering (Fig. 2.3, bottom-right). DLC was deposited by placing the wafers in the center of a PECVD machine. After the DLC deposition, top electrical contacts (Al or Pt) were evaporated through a shadow mask to create dots of different diameters. MIM devices have been prepared as follows: silicon discs of n- or p-type were evaporated by Al on the front side and DLC was

deposited by placing the wafers in a PECVD machine. After the deposition, the electrical contacts were evaporated on top as mentioned above (Fig. 2.3, top).

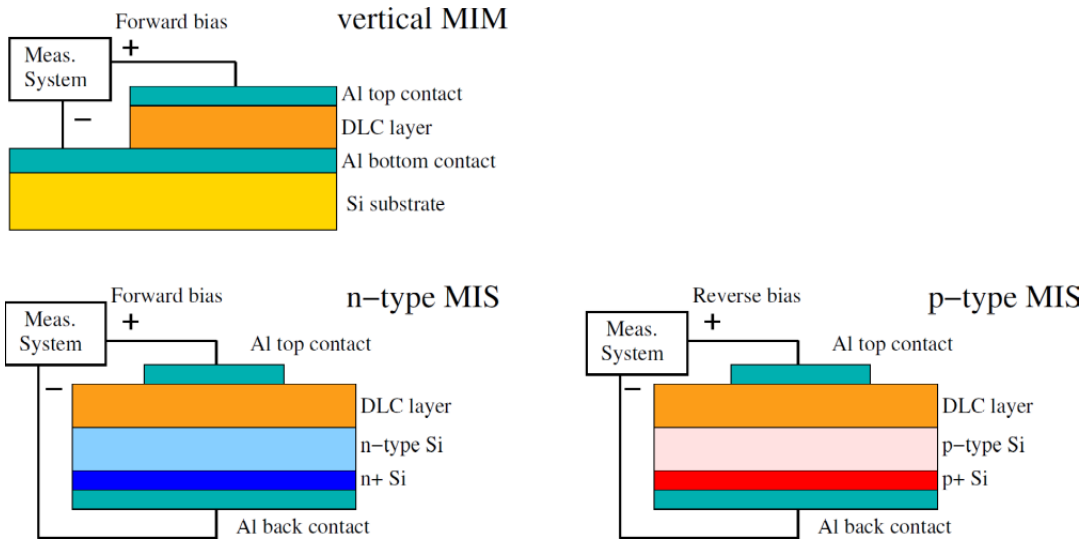


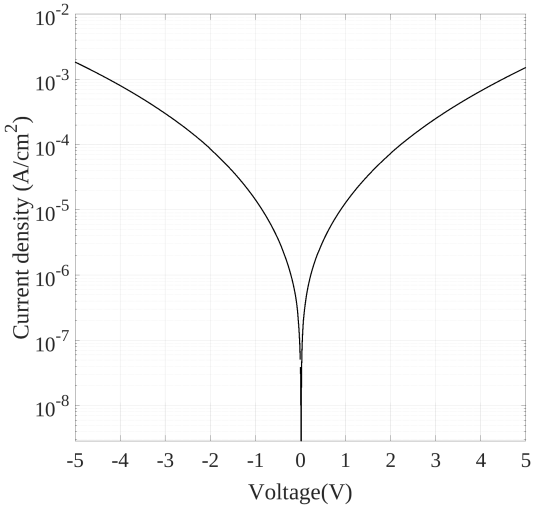
Figure 2.3: Schematic views and measurement configuration of the MIM, the n-type MIS and p-type MIS devices (structures are not in scale).

2.2.1 Metal-Insulator-Metal

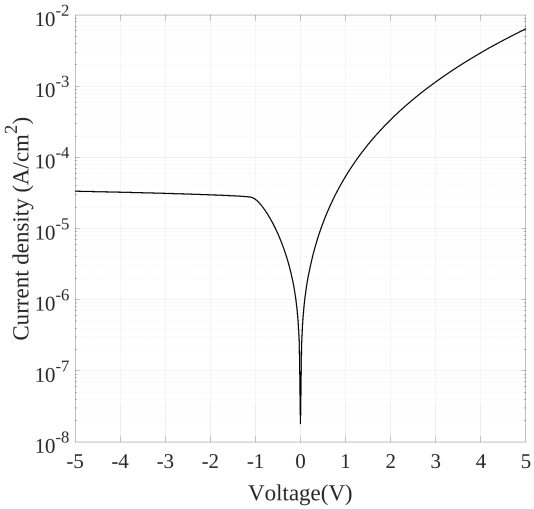
The MIM structure exhibits a specular behaviour with respect of the sign of the applied voltage (Fig. 2.4a). The JV curves represented on a log-log plot show the following features:

- an ohmic region at low applied voltages, with a slope of 1 ($J \sim V$);
- a space charge limited (SCL) region, governed by the Mott-Gurney equation, with a slope of 2 ($J \sim V^2$);
- a space charge limited region enhanced by Poole-Frenkel field emission, with a slope greater than 2 ($J \sim V^n$, with n>2);

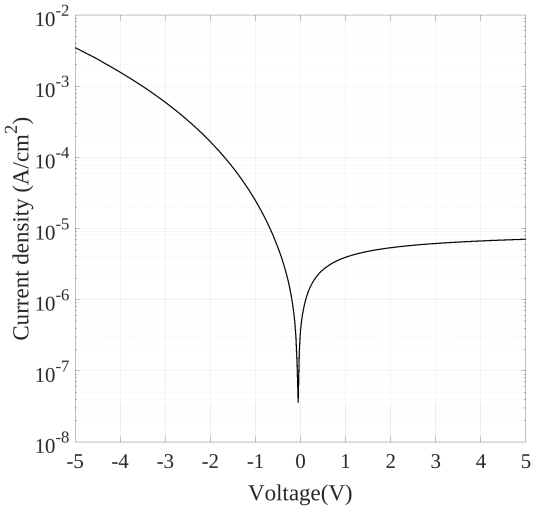
In Fig. 2.5 the forward bias JV curves corresponding to Fig. 2.4b is reported in a log-log plot together with lines corresponding to different transport regimes.



(a) Measured JV curves of a MIM structure with undoped DLC at T = 300K.



(b) Measured JV curves of a MIS structure with undoped DLC and n-type Si substrate at T = 300K.



(c) Measured JV curves of a MIS structure with undoped DLC and p-type Si substrate at T = 300K.

Figure 2.4

Ohmic Region The DLC conductivity σ could be calculated from the JV curve in the ohmic region, where $\boldsymbol{J} = \sigma \boldsymbol{E}$ holds. Since $\boldsymbol{J}$ and $\boldsymbol{E}$ are orthogonal to the MIS electrodes, their absolute value J and E can be considered without loss of generality. Under such conditions, $E = V/t$, where t is the DLC thickness. From a linear fitting of the low-bias region of the JV curve and assuming $J = \frac{\sigma}{t} V$ the conductivity can then be calculated. Analysing several samples with different deposition conditions, the conductivity roughly ranges from 10^{-11} to $10^{-7} S/cm^2$.

Space Charge Limited Current Region The SCL conduction mechanism is very common in poor conductive materials and wide-band semiconductors, where the concentration of thermally generated carriers is small and most carriers come from external sources, i.e., they are injected from ohmic contacts [12]. The onset of the SCL conduction takes place when the injected charge density in the DLC layer is larger than the thermal charge density [13]. From a theoretical point of view, the applied voltage at which this occurs, namely the cross-over or transition voltage, V_{SCL}, has a direct proportionality with the squared thickness of the sample and the thermal-equilibrium charge density and a reverse proportionality with the dielectric permittivity and the free-to-total carrier density ratio. Moreover, V_{SCL} could be numerically extrapolated by a piece-wise linear fit of the JV curve in a log-log plot. More specifically, it represents the abscissa of the interception point between the fitted lines in the ohmic and SCL regions as shown in Fig. 2.5. Analysing several samples with different deposition biases V_{SCL} ranges from 0.1V to about 0.7V.

High injection regime When the applied voltage is approximately higher than 1-1.5V, the current density curves of Metal-DLC-Metal devices show a more than quadratic dependence over potential. This can be ascribed to Poole-Frenkel emission, which is very common for many organic materials [14]. Considering an electron in a trap center, the Coulomb potential energy of the electron is reduced by the applied electric field across the DLC layer. The potential-energy reduction increases the probability of an electron being thermally excited out of the trap into the conduction band and leads to higher current densities.

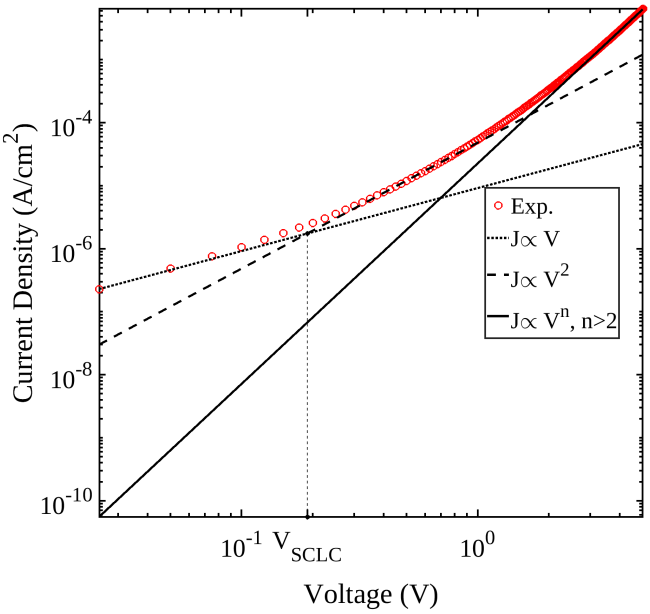


Figure 2.5: Forward bias JV curves of a MIS structure with doped DLC and n-type Si substrate at T = 300K (Fig. 2.4b) in a log-log plot together with curves corresponding to different transport regimes in the DLC. In this case $n = 3.5$ and $V_{SCLC} = 0.19V$

Capacitance Measurements The capacitance per unit area of Metal-Insulator-Metal devices has been measured at different frequencies by sweeping the voltage and also at fixed bias by sweeping the frequency. The capacitance of the DLC layer has been extracted assuming a parallel RC model. Experiments show that the DLC capacitance is constant with respect to the applied voltage, but exhibits a significant frequency dependence (Fig. 2.6).

Interface Layer Al-DLC-Al structures with the DLC film deposited on a glass substrate (Fig. 2.7) have been characterized in order to measure the lateral conductivity of the DLC. I-V curves show a linear Ohmic behaviour independently on the applied voltage with a conductivity two order of magnitude larger when compared with vertical MIM structures. This has been ascribed to the presence of a blocking interface layer as confirmed by TEM images of MIM and MIS structures. The difference between the vertical and the lateral conductivity will be a key element in the TCAD modelling of the

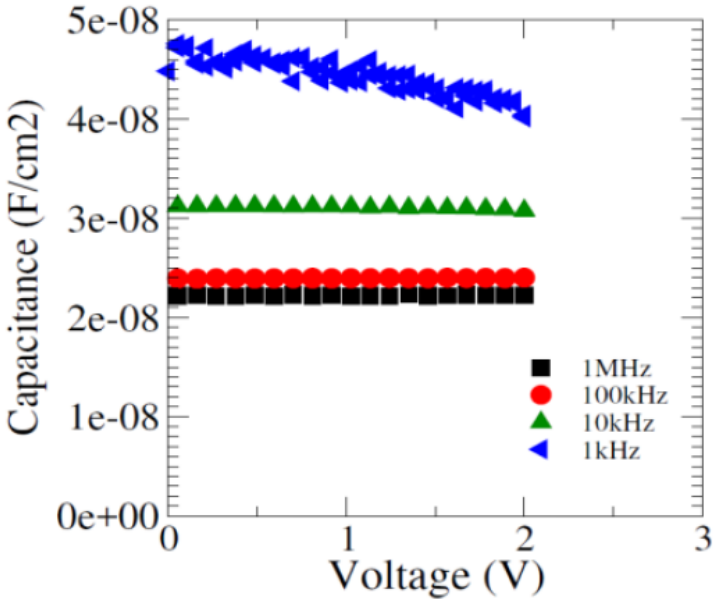


Figure 2.6: Measured CV curves of a MIM structure for different frequencies as function of the applied voltage

diode breakdown voltage as explained in the following chapters.

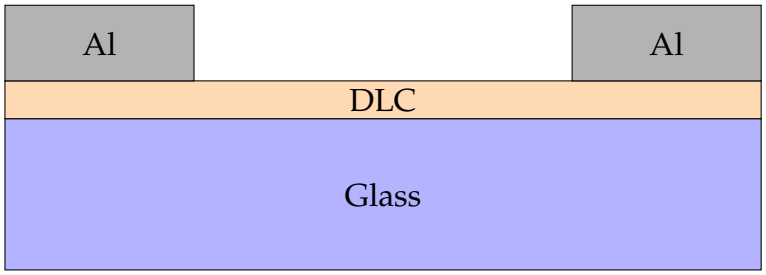


Figure 2.7: Schematic representation of an Al-DLC-AL structure with the DLC layer deposited on a glass substrate

2.2.2 Metal-Insulator-Semiconductor

DLC-Silicon hetero-junction devices, irrespective of the DLC recipe, exhibit a moderate rectifying behaviour. Such devices have two distinct modes of operation, the forward bias and the reverse bias ones. The voltage polarity associated with these modes depends on the silicon substrate doping: for the n-type case (Fig. 2.4b), the forward mode takes place when the positive voltage is applied to the electrode contacting the DLC layer and the reverse mode is when the opposite is the case; for the p-type case (Fig. 2.4c), a positive

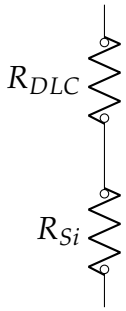


Figure 2.8: Macroscopic model of a MIS structure

voltage applied to the top electrode is related to the reverse mode. Under forward bias conditions, Metal-DLC-Silicon structures show similar trends to the Metal-DLC-Metal devices. This happens because the Silicon substrate and the DLC can be approximately modelled as two resistors in series as shown in Fig. 2.8 The silicon conductivity, according to the drift-diffusion model, depends on mobility and carrier concentration as follows:

$$\sigma = e(\mu_n n + \mu_p p) \tag{2.2}$$

In the n-type silicon $\sigma \approx e\mu_n n$ while in the p-type one $\sigma \approx e\mu_p p$.The doping concentration can be extracted from conductivity measurements as:

$$N_D \approx n \approx \frac{\sigma}{e\mu_n}, N_A \approx p \approx \frac{\sigma}{e\mu_p} \tag{2.3}$$

The manufactured MIS structures have $\sigma = 0.023 S/cm^2$ and $\sigma = 0.060 S/cm^2$ for the n-type and p-type silicon respectively which result in a doping concentration of the silicon substrate of $N_D \approx 10^{14} cm^{-3}$ and $N_A \approx 8 \cdot 10^{14} cm^{-3}$. For this reason, the forward bias J-V curves of MIS structure are almost entirely dominated by the DLC layer conductivity. On the contrary, they show a current saturation in reverse bias mode. This is not due to the metal/DLC energy barrier, as demonstrated by the symmetrical Metal-DLC-Metal experiments with no saturation regime, but it is related to the presence of the Silicon substrate. In reverse-bias regime, a depletion region is formed in the

silicon substrate, which widens with the increase of the reverse bias: its resistivity becomes higher than the DLC layer, so that the whole potential drops across the substrate and the resulting current is quite constant. The applied voltage at which the saturation occurs is related to the flat-band voltage, as it represents the threshold bias between electron-injection regime and depletion regime (i.e., the threshold voltage for band-bending with different sign).

Capacitance Measurements In the metal-insulator-semiconductor structures the DLC layer acts as a frequency dispersive insulator. The capacitance of this structure is the series result of the capacitance of DLC film and that of the space-charge region in Si substrate. As mentioned before for the MIM structures, it has been extracted performing CV measurements at different frequencies and assuming a parallel RC model. Under forward bias, i.e. in accumulation mode, the overall capacitance is expected to be dominated by the DLC contribution and then, it should be constant over the applied voltage. This is partially true for some samples, especially at high frequencies. In some other cases, the CV curves exhibit a roll-off, due to high leakage current (in ideal MOS structures no current flows in the oxide layer). Under reverse bias, i.e. in depletion mode, the silicon starts to be depleted and its contribution can no longer be neglected. As the reverse bias increases, the depletion width in the silicon widens and the overall capacitance decreases. Deep depletion in the silicon is observed but no inversion occurs. The measured CV curves of a Metal-Insulator-Semiconductor structure with n-doped silicon substrate are shown in Fig. 2.9.

Role of the Metal Workfunction MIS structures with the top electrode made of aluminum or platinum have been compared. Despite these two metals have very different work functions (4.28 eV for Al and 5.12-5.93 eV for Pt), the Al-DLC-Si and Pt-DLC-Si hetero-junctions do not exhibit relevant changes of

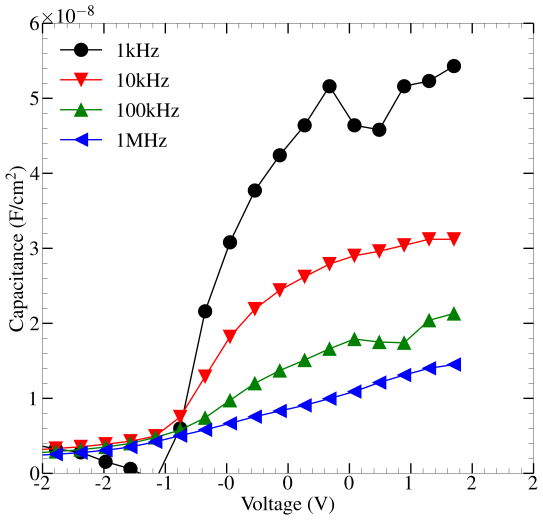


Figure 2.9: Measured CV curves of a MIS structure for different frequencies as function of the applied voltage

the measured current-voltage curves. This can be ascribed to the large number of available conductive states inside the DLC energy gap close to the mid-gap as shown in [10] and [15], inducing a strong pinning of the Fermi-level at the mid-gap and a very small Schottky barrier effect.

Doped DLC

With the aim of understanding the effect of nitrogen or boron incorporation inside the DLC layer, MIS structures with different DLC doping types and concentrations have been realized. Doped DLC samples exhibit higher conductivities and polarization due to the increasing disorder inside the material as confirmed by Raman spectroscopy. This leads to a larger number of hopping sites and to an increase of the available states in both the conduction and the valence band. From measurements, a very small decrease of the optical band gap has been observed (Fig. 2.10) thus confirming a shift of the Fermi level from the mid-gap. Figs. 2.11a and 2.11b show the experimental J-V curves of the MIS structures with different substrate doping for both boron- and nitrogen-doped DLCs (the cases with maximum doping level are used

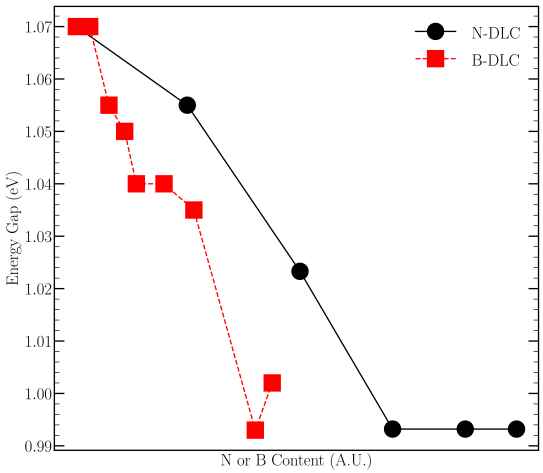


Figure 2.10: Measured optical DLC energy gap as function of the doping concentration for both N-DLC and B-DLC

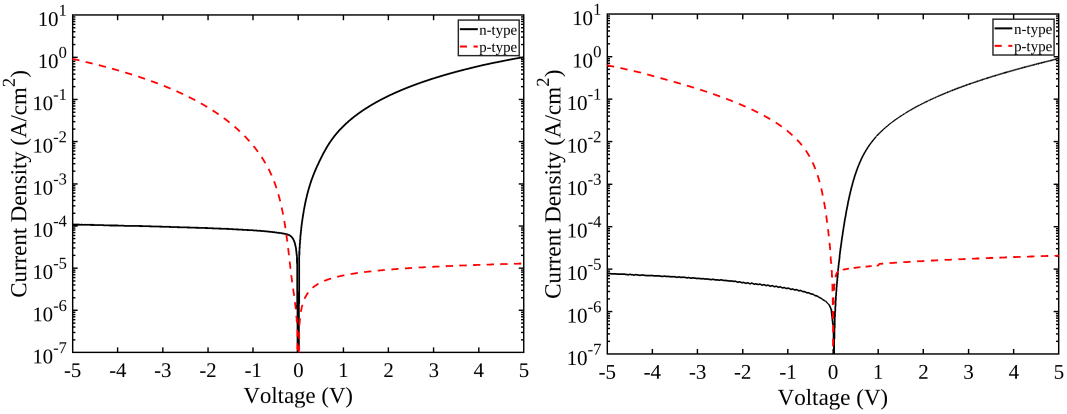
here as reference). The doped DLC provides a strong increase of the current under forward bias compared to the undoped case [16]. Moreover, here we compare the forward-bias current curves of MIS structures with different doping types of the substrate (p-Si and n-Si). Surprisingly, no significant threshold voltage is observed in the two different substrate doping configurations and symmetric forward-bias curves have been found in any DLC doping configuration. However, at very low bias, the current density depends on the DLC doping type:

- NDLC: $J_{n-Si} > J_{p-Si}$
- BDLC: $J_{n-Si} < J_{p-Si}$

Where J_{n-Si} (J_{p-Si}) is the current density of the MIS structure with a n-type (p-type) silicon substrate. This can be ascribed to the presence of fixed charge inside the DLC bulk. The current levels in forward mode at high bias are very similar, while in reverse mode they still depend on the doping type:

- NDLC: $J_{n-Si} > J_{p-Si}$
- BDLC: $J_{n-Si} < J_{p-Si}$

The capacitance curves, differently from the undoped DLC, show a very pronounced peak at the threshold voltage followed by a quick decrease of the



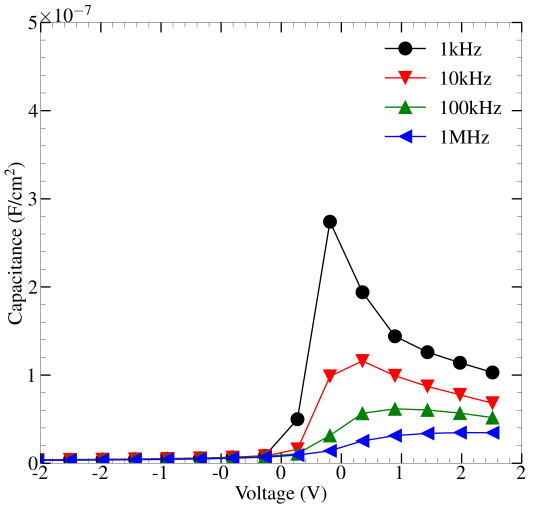
(a) Measured JV curves of a MIS structure with N-DLC and different doping type of the silicon substrate at T = 300K.

(b) Measured JV curves of a MIS structure with B-DLC and different doping type of the silicon substrate at T = 300K.

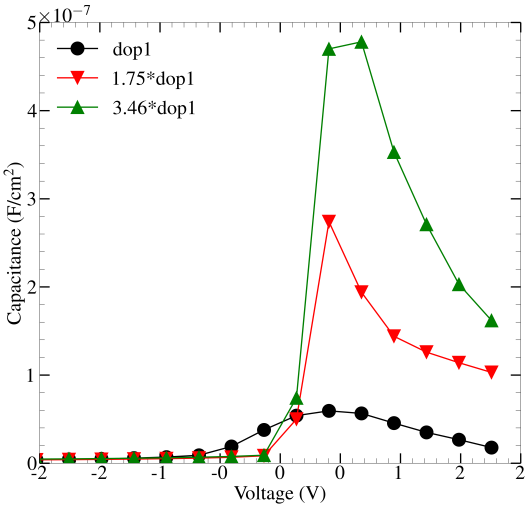
Figure 2.11

capacitance due to the high conductivity of the DLC layer as can be observed in Fig. 2.12a where the capacitance measurements for a MIS structure with boron doped DLC and n-type silicon substrate are reported for different frequencies. In Fig. 2.12b, the CV curves are reported at $f = 1kHz$ for different boron concentrations. As expected, a higher amount of B results in a large capacitance peak at the threshold voltage due to the increase of disorder followed by a faster roll-off at higher bias as a consequence of the increased conductivity.

Temperature Dependence To further distinguish the above different transport regimes, the J-V characteristics were measured at 300, 325, 350 and 375 K. Some examples are shown in Fig. 2.13. The strong increase of the current density under forward bias conditions can be ascribed to the Poole-Frenkel conductivity model. The predicted Arrhenius-like temperature dependence has been confirmed by fitting the current density extracted at $\pm$1V assuming $J \sim \exp(-E_a/k_BT)$. The activation energies E_a for different DLC recipes are shown in Figs. 2.14a and 2.14b.

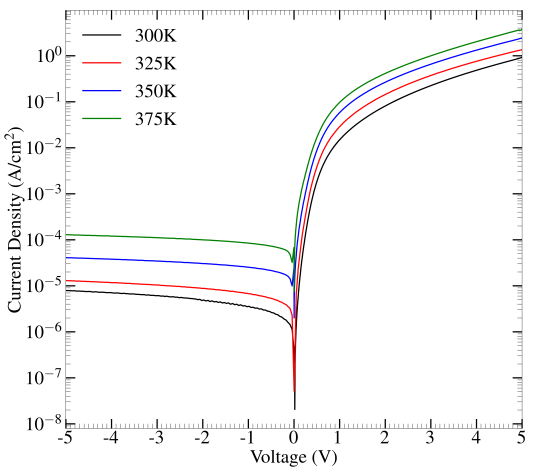


(a) Measured CV curves of a MIS structure with B-DLC for different frequencies of the applied signal. The sample with doping concentration = "1.75dop1" has been used.

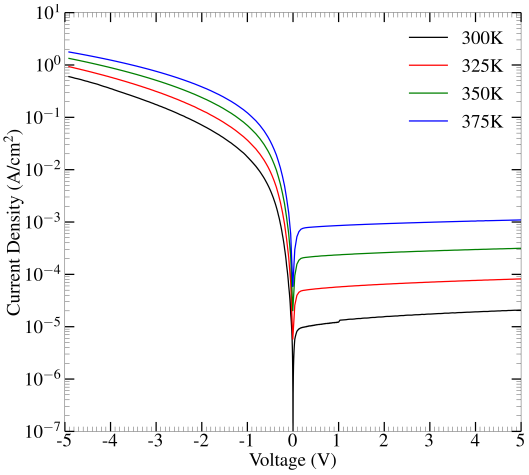


(b) Measured CV curves of a MIS structure with B-DLC for different DLC doping concentration.

Figure 2.12



(a) Measured JV curves of a MIS structure with B-DLC and n-type Si substrate for different temperatures



(b) Measured JV curves of a MIS structure with B-DLC and p-type Si substrate for different temperatures

Figure 2.13

2.2.3 P-i-N Diode Passivated with DLC

Discrete fast recovery diodes with a nominal breakdown voltage of 4.5kV and a diameter of approximately 90mm have been manufactured by ABB Switzerland Ltd Semiconductors in order to understand the effects of a DLC layer on a negative bevel junction termination. A schematic representation of the JT with the DLC on top is shown in Fig. 2.15. By using the technique

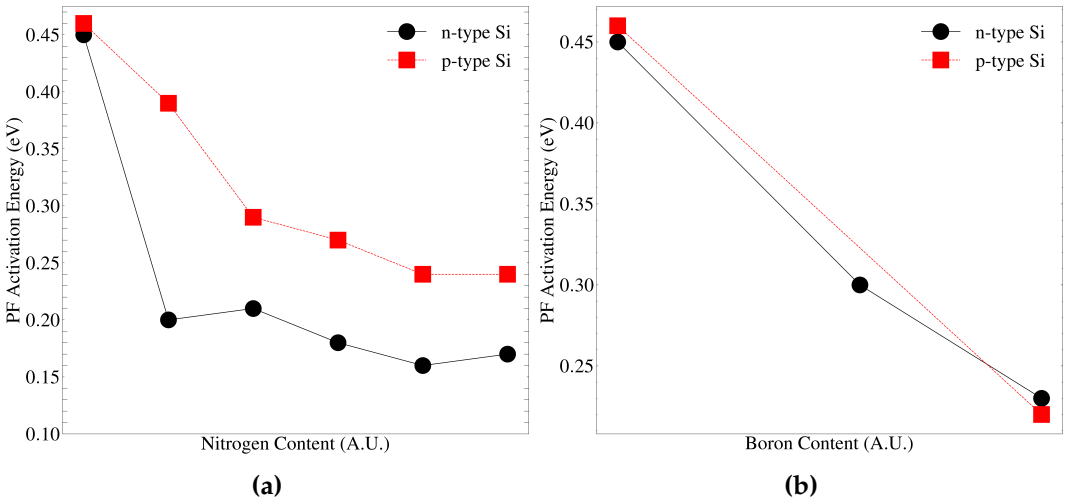


Figure 2.14: Activation energy of the forward-bias JV curves extracted from Arrhenius fitting for (a) NDLC and (b) BDLC for different doping type of the Silicon substrate

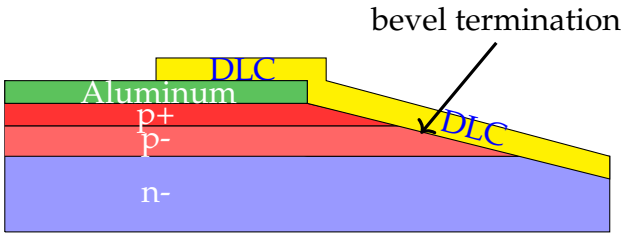


Figure 2.15: Schematic representation of a negative bevel termination passivated with DLC (yellow area). Structure not in scale

previously adopted for the realization of test structures (MIM and MIS) different DLC recipes have been tested. In addition, the role of the passivation layer thickness has been analysed acting on the deposition time. Fig. 2.16 shows the BV and the leakage current of the diode under investigation for different doping concentration and different DLC thicknesses.

Leakage Current The presence of a semi-insulating layer as passivation, provides an additional path for charge carrier along the bevel when its conductivity is comparable to that of a depleted silicon. An increased amount of impurities (N or B) results in a large number of available states inside the energy gap together with an enhanced mobility as observed from the MIS

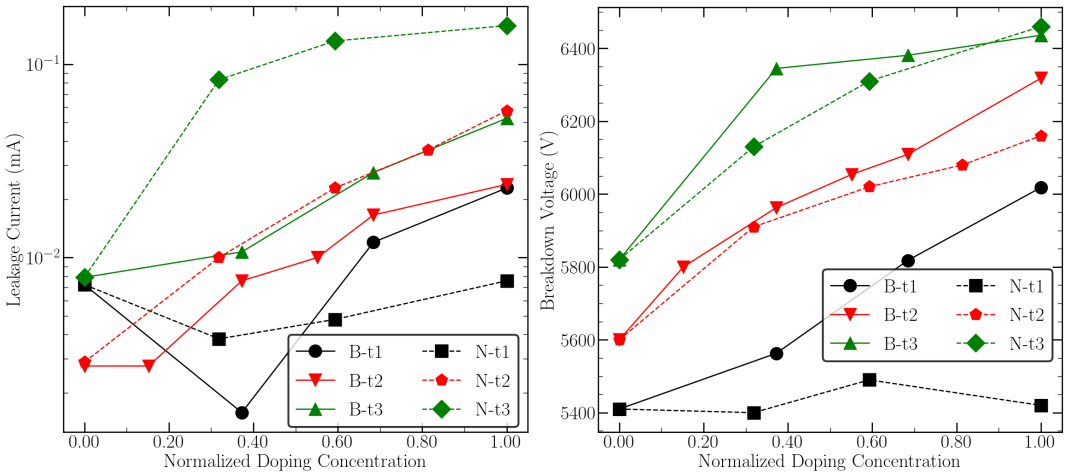
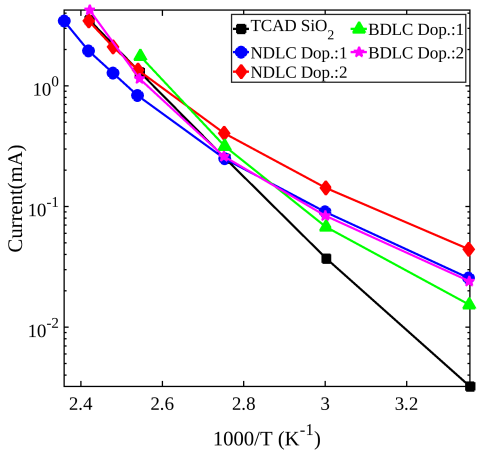


Figure 2.16: Leakage current (left) and breakdown voltage (right) of negative bevelled power diodes passivated with diamond-like carbon for different DLC thickness as function of the doping concentration. N and B represent the nitrogen and boron Doped DLC. t1, t2, t3 correspond to different thicknesses of the DLC layer: $t2 \approx 2t1$ and $t3 \approx 3t1$

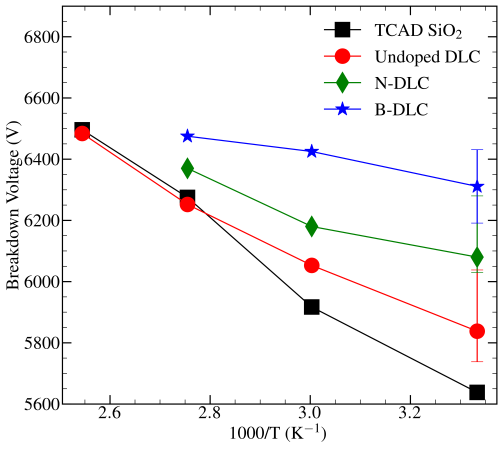
characterization. Moreover, a thicker passivation layer has a larger cross-sectional area and then a lower resistance. These assumptions explain the increase of the leakage current with the doping concentration and the DLC deposition times (Fig. 2.16a).

Breakdown Voltage As observed by comparing MIS structures with differently doped DLC layers and different substrate doping type, doped DLC contains a certain amount of fixed charges due to the substitutional N or B atoms. Such dopants can modify the width of the depletion region along the bevel termination affecting the breakdown voltage. A higher doping concentration lead to a higher fixed charge. The same is true for a larger passivation thickness (Fig. 2.16b).

Temperature effects Measurements of the breakdown voltage and the leakage current have been performed up to the maximal allowed junction temperature T = 413K. Following Eq. (1.30) the leakage current of a pn junction depends on the intrinsic carrier concentration which exponentially increases with temperature. However, an unusual deviation from the expected Arrehnius-law has been observed at higher temperatures in the DLC-coated power diode. The presence of a DLC layer affects the leakage current only at low temperature while it reduces to that of a simulated diode passivated with an ideal SiO_2 (Figs. 2.17a) at $\approx$ 400K. Similar considerations can be made on the breakdown voltage. The impact-ionization coefficients exponentially decrease by increasing the temperature and then a strong increase of the blocking capability is expected. On the contrary, experiments show a very week temperature dependence of the breakdown voltage when compared with a simulated ideal SiO_2 coated power diodes.



(a) Measured temperature dependence of the Leakage current for different DLC recipes compared with a simulated diode with an ideal SiO_2 passivation layer



(b) Measured temperature dependence of the Breakdown Voltage for different DLC recipes compared with a simulated diode with an ideal SiO_2 passivation layer

Figure 2.17

Chapter 3

TCAD Modelling of DLC layers for high voltage applications

From a theoretical point of view, amorphous organic materials such as DLC can not be modelled as crystalline semiconductors since the absence of a periodic lattice makes the Bloch's theorem no longer valid. In addition, the charge transport into DLC layers is dominated by hopping between localized states. Different models, based on the DLC electrical characterization shown in the previous chapter, have been proposed in the recent years. All of them are based on the solution of the drift-diffusion model with a Poole-Frenkel mobility to account for the field dependence of the conductivity. Moreover, the high polarization observed in the capacitance measurements has been modelled by solving the first-order Debye equation together with the ferroelectric model. However, they rely all on the definition of a valence band and a conduction band as for a crystal, while completely different band structures are expected for the amorphous DLC when compared with classical semiconductors. Standard parabolic bands with trap levels in the energy gap have been proposed in order to reproduce the MIM and MIS JV curves with undoped DLC on top [16]. Nitrogen doped DLC has been firstly modelled by assuming the presence of active doping and donor traps [17]. Finally, simulations with no ionized atoms but asymmetric Gaussian DOS have been proposed for boron-Doped DLC [18] [19]. However, these models are not

able to reproduce all the DLC charge transport features since the symmetries observed in the MIS JV curves are not captured. As a consequence, the impact of a DLC passivation on the diode performance can not be fully predicted. For this reason, a new model has been finally developed and validated against the experiments [20] [21]. The first section of this chapter describes the TCAD setup used to simulate the reference device: a discrete negative bevelled power diode with an active area of approximately 60cm^2 and a nominal breakdown voltage of 4.5kV. The Poole-Frenkel mobility equation and the ferroelectric model, which are common to all the approaches proposed to describe the DLC features are discussed in the second section. In the third section all the proposed DLC models are discussed providing advantages and limits. Finally, the complete DLC model which is able to reproduce the behaviour of MIS structures and predicts the breakdown voltage and the leakage current of a negative bevelled power diode is described with details in the fourth section.

3.1 TCAD setup for power diodes

The device under test, a circular discrete diode, is schematically represented in Fig. 3.1. The DLC is used as passivation layer directly in contact with the silicon bevel edge. The same device geometry was used with different DLC depositions for the investigation of the DLC features. The 2D radial description has been used in the framework of the TCAD tool by assuming cylindrical coordinates. Since the diodes ruggedness under dynamical turn-off conditions is not affected by the material used as passivation layer, the fabricated devices do not experience the usual shaping of the carrier lifetime through irradiation. For this reason, electrothermal simulations are not necessary to calibrate the deep energetic levels in the bandgap introduced by this

process [22]. Thus, the drift-diffusion isothermal simulations have been carried out to investigate the OFF-state regime up to the avalanche breakdown. The doping profiles have been extracted from the spreading resistance profiling. As far as the Silicon material is concerned, the Shockley-Read- Hall model for the thermal generation-recombination has been used with carrier lifetime fitted against the reverse leakage current curves at different temperatures when an undoped DLC was used as the passivation layer. The predicted I_{OFF} values correspond to the simulated curves for an ideal SiO_2 passivation which are very close to the experimental results with undoped DLC. The Van Overstraeten model for the impact ionization generation has been used for Silicon with default parameters. No impact-ionization is expected in the DLC. The leakage current and the breakdown voltage can be extracted from quasi-stationary voltage ramps under reverse bias condition. However, they require a long computational time due to the poor convergence close to the breakdown voltage condition. For this reason, transient simulations with a very small dV/dt has been used to emulate quasi-stationary conditions and at the same time avoid numerical convergence problems.
It is worth nothing that the geometry of the device and the silicon parameters do not depend on the passivation layer used on the bevel termination. For this reason, the setup described so far can be used regardless the transport model adopted to describe the DLC properties.

3.2 Poole-Frenkel effect & Ferroelectric model

In this section the Poole-Frenkel effect and the Ferroelectric model available into the TCAD tool [23] will be illustrated. In addition, simple rules will be provided to fit their parameters according with the available experiments. The approaches shown here are valid for all the models described in the following sections.

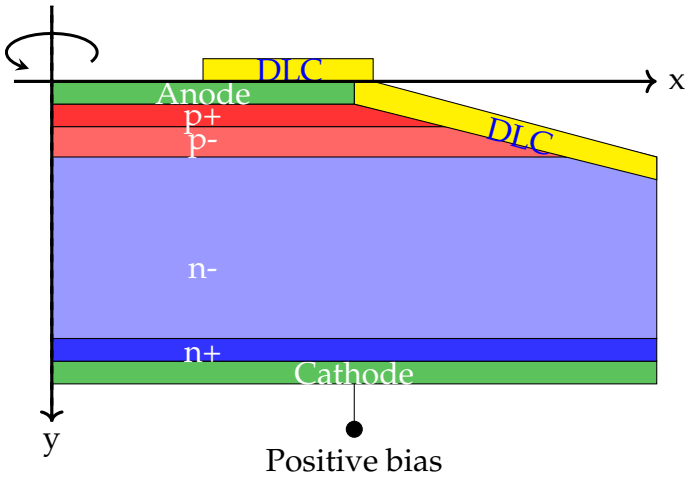


Figure 3.1: Schematic representation of a power diode with negative bevel termination and DLC as passivation layer. Structure not in scale

3.2.1 Poole-Frenkel effect

Consider a trap level at energy E_t which is neutral when filled and positive when empty. A captured electron has a probability to escape into the conduction band that is proportional to $\exp(-e\Phi_{tn}/k_BT)$ where $q\Phi_{tn} = E_c - E_t$ is the energy barrier k_B the Boltzmann constant and T the absolute temperature. In presence of strong electric field the effective barrier is reduced. Assuming a Coulomb interaction between the emitting carrier and the remaining charged trap the Poole-Frenkel effect (PF) can be written as [11]:

$$\Phi_{eff} = \Phi_{tn} - \sqrt{\frac{e^3 E}{\pi \varepsilon_r \varepsilon_0}} \tag{3.1}$$

The reduced barrier increases the emission probability of the traps increasing the corresponding density of free carrier in the conduction band n_{PF}. Thus, the Poole-Frenkel conductivity reads:

$$\sigma_{PF} = e\mu_n n_{PF} = e\mu_n n_0 \exp\left(\frac{e}{k_BT}\left(\sqrt{\frac{e}{\pi \varepsilon_r \varepsilon_0}}\right)\sqrt{E}\right) \tag{3.2}$$

where μ_n and n_0 are, the field independent mobility and the electron density in the conduction band, respectively. Eq. 3.2 is the so-called Pool-Frenkel model for electrons. Similar considerations can be made for holes.

Poole-Frenkel mobility model implemented in the TCAD setup Unfortunately, in the drift-diffusion model, the electron and hole concentrations are calculated assuming transport of free carriers in the conduction or valence bands. They can be expressed as:

$$n = \int_{-\infty}^{+\infty} g_e(E) f(E) dE, \qquad p = \int_{-\infty}^{+\infty} g_h(E)(1 - f(E)) dE \tag{3.3}$$

Where $g_e(E)$ and $g_h(E)$ are the electron and hole density of states (DOS), respectively and $f(E)$ is the Fermi-Dirac distribution:

$$f(E) = \frac{1}{e^{(E-E_F)/k_B T} + 1}, \qquad 1 - f(E) = \frac{1}{e^{(E_F-E)/k_B T} + 1} \tag{3.4}$$

Far from the equilibrium condition, the Fermi potential E_F is replaced by the two quasi-Fermi potential $E_{F,n}$ and $E_{F,p}$ as described in Chapter 1. It is worth noting that Eqs. (3.3) can be applied for the description of the DLC charge transport independently from the DOS shape. In order to account for the conductivity field dependence predicted by the Poole-Frenkel effect, the following model is available:

$$\mu = \mu_0 \exp\left(-\frac{E_a}{k_B T}\right) \exp\left(\sqrt{E}\left(\frac{\beta}{T} - \gamma\right)\right) \tag{3.5}$$

where μ_0 is the low-field mobility, E_a is the effective activation energy which corresponds to $q\Phi_{tn}$ of Eq. (3.2), $\beta = \frac{1}{k_B}\sqrt{\frac{e^3 E}{\pi \varepsilon_r \varepsilon_0}}$ represents the barrier lowering due to the high electric field and γ is a fitting parameter. In the following simulations, the latter parameter was fixed to 0, thus adopting the theoretical Poole-Frenkel model. The conductivity of the DLC is then calculated as

follows:

$$\sigma = e(\mu_n n + \mu_p p) \tag{3.6}$$

Where μ_n and μ_p are the field dependent electron and hole mobility calculated according to Eq. (3.5). However, the parameter E_a of Eq. (3.5) merely defines the temperature dependence of the mobility and does not imply the presence of any trap level coupled with the conduction or the valence band. For this reason, the concentration n and p are not affected by the presence of the Poole-Frenkel mobility model. Even though these assumptions are not rigorous from a physical point of view, they allow to simplify the description of the DLC charge transport and to significantly reduce the computational time.

The PF mobility model parameters can be fitted against the J-V curves of MIM structures or forward bias MIS structure where the DLC conductivity is much lower when compared to silicon as discussed in the previous chapter. The low-field mobility μ_0 has been fitted against J-V curves at low-bias, where the ohmic regime is dominating while β has been calibrated against the J-V curves in the high-bias regime, where $J \propto V^n$ with n > 2. The activation energy E_a has been chosen by comparing the J-V curves at different temperatures.

3.2.2 Polarization Model

As observed in the previous chapter, CV curves of MIM and MIS structures show a strong capacitance peak together with a significant frequency dependence of the associated polarization. The presence of polarization can be macroscopically described defining the vector $\boldsymbol{P}$ as the dipole moment per unit of volume. The constitutive relation for the electric displacement can then be written as [1]:

$$\boldsymbol{D} = \varepsilon_0 \boldsymbol{E} + \boldsymbol{P} \tag{3.7}$$

If the material is isotropic and uniform the induced polarization $\boldsymbol{P}$ is parallel to $\boldsymbol{E}$:

$$\boldsymbol{P} = \varepsilon_0 \chi_e \boldsymbol{E} \tag{3.8}$$

where χ_e is is the electric susceptibility of the medium. Different microscopic phenomena can contribute to polarization [24]:

- Electronic polarization ($\boldsymbol{P}_e$): when an electric field is applied to a dielectric the electronic clouds are shifted from their equilibrium position resulting in a weak electric dipole
- Ionic or atomic polarization ($\boldsymbol{P}_a$): positive and negative ions tend to move toward each other resulting in a larger polarization when compared with the electronic one.
- Orientational or molecular polarization ($\boldsymbol{P}_o$): the asymmetrical bonding structure of some molecules produce a permanent polarization (an electric dipole is present even if the applied field is zero). When $\boldsymbol{E} \neq 0$ the molecules carrying a permanent dipole will orient the dipole along the direction of $\boldsymbol{E}$. This kind of polarization is usually dominant into disordered materials such as DLC.
- Interfacial polarization ($\boldsymbol{P}_i$): due to the accumulation of charges at the interfaces at the metal/insulator interface. It can neglected since it was not observed in the DLC.

The total polarization can then be written as:

$$\boldsymbol{P} = \boldsymbol{P_e} + \boldsymbol{P}_a + \boldsymbol{P}_o \tag{3.9}$$

When the dielectric is subjected to a dynamical electric field the different polarization mechanisms behave differently depending on the frequency f of the applied signal. We can distinguish two limiting cases:

- $f \to \infty$: $\boldsymbol{P} = \boldsymbol{P}_\infty = \boldsymbol{P}_e + \boldsymbol{P}_a = \varepsilon_\infty \varepsilon_0 \boldsymbol{E}$
- $f = 0$: $\boldsymbol{P} = \boldsymbol{P}_s = \boldsymbol{P}_\infty + \boldsymbol{P}_{so} = \varepsilon_s \varepsilon_0 \boldsymbol{E}$. With $\boldsymbol{P}_{so} = \boldsymbol{P}_o(f = 0) = \varepsilon_0(\varepsilon_s - \varepsilon_\infty)\boldsymbol{E}$

This means that $\boldsymbol{P}_e$ and $\boldsymbol{P}_a$ are relevant up to very high f and can be considered constant in the whole frequency range. However, since molecules need time to respond to the applied excitation, $\boldsymbol{P}_o$ has a more complicated frequency dependence. From a theoretical point of view, different molecules can have different relaxation times. However, only a single-time constant response described by the Debye equation is available into the TCAD simulator. It reads:

$$\frac{d\boldsymbol{P}}{dt} = \frac{\boldsymbol{P}_s - \boldsymbol{P}}{\tau} \tag{3.10}$$

Where P is the polarization vector and τ is the relaxation time. $\boldsymbol{P}_{so}$ is the polarization vector induced by the applied electric field. Under static condition $\boldsymbol{P} = P_{so}$. Assuming a sinusoidal electric field, the dielectric constant can be rewritten as:

$$\varepsilon = \varepsilon_\infty + \frac{\varepsilon_s - \varepsilon_\infty}{1 + i\omega\tau} \tag{3.11}$$

with $\omega = 2\pi f$. With the ferroelectric model available into the TCAD simulator, it is possible to describe the polarization vector $\boldsymbol{P}_{so}$ by using three scalar equations, one for each component [23]. Each equation relates the polarization with the electric field by using an hysteresis cycle described by the following equation:

$$P_{so} = cP_s \tanh(w * (E \pm F_c)) + P_{off}, \qquad w = \frac{1}{2F_c} \ln\left(\frac{P_s + P_r}{P_s - P_r}\right) \tag{3.12}$$

Where P_s, and P_r are the saturation and the residual polarization respectively while F_c is the coercive field. P_{off} and c result from the polarization history of the material. An example of hysteresis is given in Fig. 3.2. Since measurements do not show the presence of saturation, a very high value of P_s

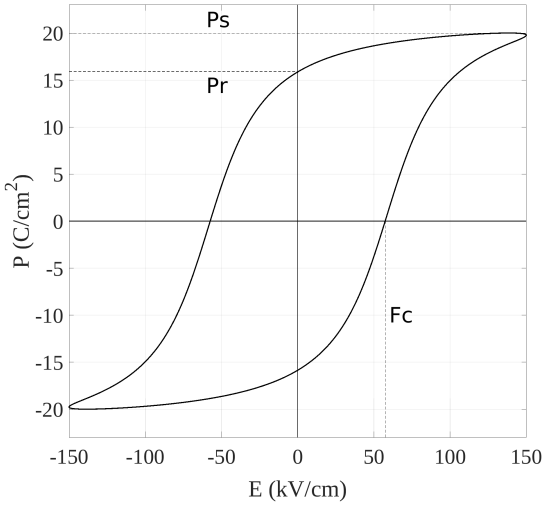


Figure 3.2: Example of hysteresis cycle

has been chosen together with a small value of F_c. In this way, the hysteresis cycle is reduced to a simple linear relation between $\boldsymbol{P_0}$ and $\boldsymbol{E}$. In this way, a frequency dependent $\varepsilon(\omega)$ can be modelled without hysteresis or saturation. The parameters of the polarization model have then be fitted against the forward bias CV curves using the following rules:

- $F_c = 10^4 V/cm$ and $P_s = 1.5 \cdot 10^{-6} C/cm^2$ for all simulations
- Dielectric constant $\varepsilon = \varepsilon_\infty$ against the CV curves measured at the highest frequency (usually 1MHz)
- P_r and τ by looking at the capacitance peak and to its frequency dependence in the range $1kHz \leq f \leq 100kHz$

3.3 Different approaches to the DLC modelling

The DLC modelling can be performed by using very different approaches. Here some preliminary models are described together with their limitations.

3.3.1 Undoped DLC

A simple model for undoped DLC applicable *only* to MIM and n-type MIS structures has been proposed in [16]. A schematic representation of the 2D structures used into the simulator is reported in Fig. 3.3. In order to normalize the simulation results to the current density in A/cm^2, the area of the electrodes is multiplied by an Area Factor in order to obtain an equivalent top-electrode surface of 1cm^2. Parabolic bands have been used to emulate

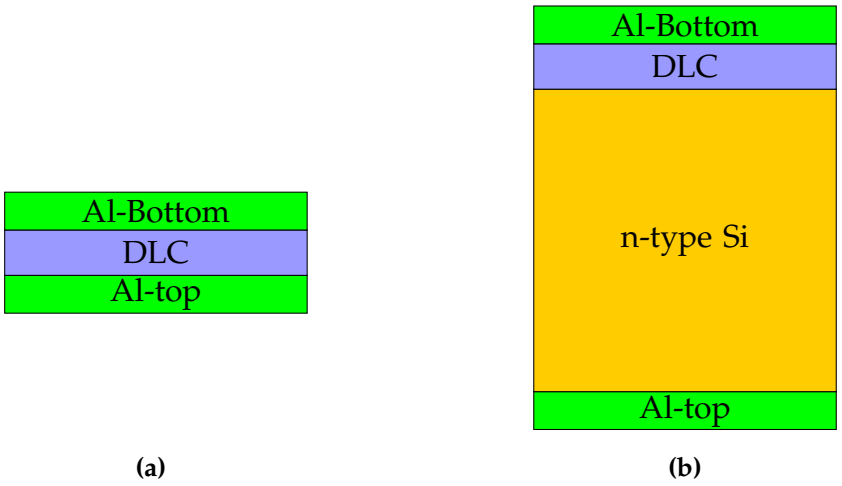


Figure 3.3: Schematic representation of (a) MIM structure and (b) MIS structure implemented into the TCAD simulator (structure not in scale)

the presence of sp^3 sites with σ bonds. The number of states in the conduction and the valence band, Nc and N_v respectively, has been fitted against DFT calculations. The localized sp^2 sites with π bonds are accounted for by using acceptor trap levels as shown in Fig. 3.4. As far as the boundary conditions are concerned, the metal Schottky barrier and the DLC affinity have been fixed so to reproduce the J-V experimental data of both MIM and MIS devices with the correct activation energies. Starting from the MIM curves, a relatively low Schottky barrier, i.e. 25mV, has been selected as no saturation is observed in the J-V curves. Added to the pinning effect of the trap level in the gap and to the activation energy of the PF mobility, it gives the exact temperature dependence of the experimental J-V curves. By using the

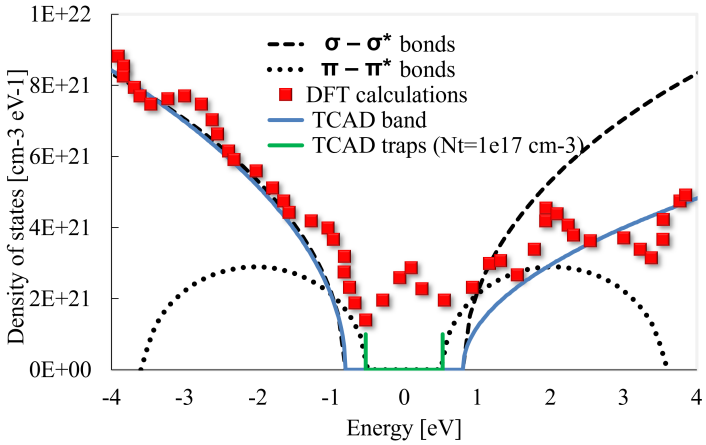


Figure 3.4: DLC band structure implemented into the TCAD simulator compared with the optical model ($\sigma - \sigma^*$ and $\pi - \pi^*$ bonds) extracted from [25] and DFT calculations [26].

same Schottky barrier for the MIS diode, the DLC affinity has been fixed at $\chi_{DLC} = 3.9eV$ according to the temperature dependence of the forward bias JV curves at very low bias. TCAD simulations and experiments are compared in Figs. 3.5 and 3.6. This model, is strongly physically based since it correctly

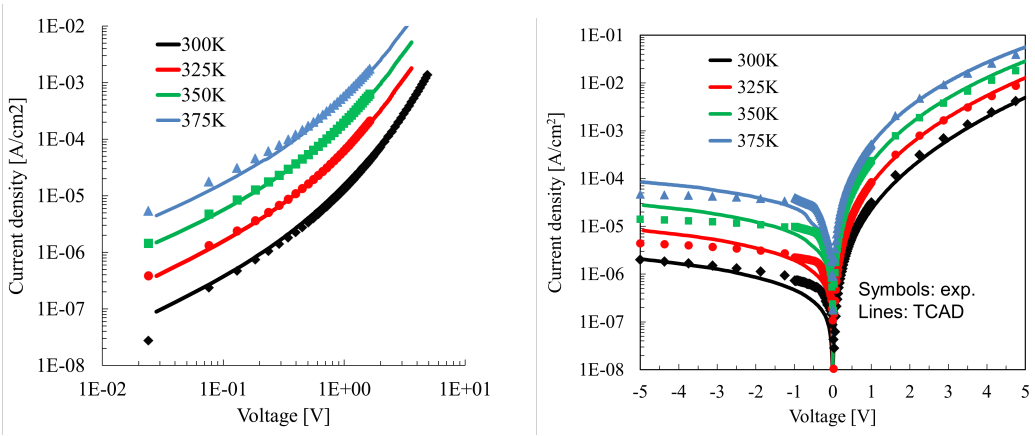


Figure 3.5: Simulated JV curves of MIM and MIS structures for different value of the ambient temperature compared with experiments.

accounts for the presence of both σ and π bonds. However, it provides completely wrong results when applied to MIS structures with a p-type silicon substrate. In addition, the presence of the interface layer observed from TEM

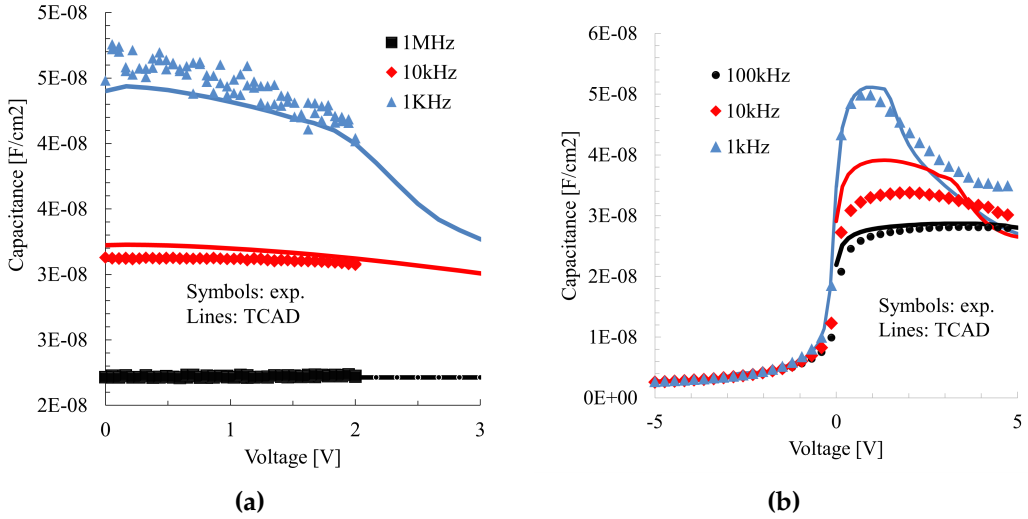


Figure 3.6: Simulated CV curves of MIM and MIS structures for different value of the ambient temperature compared with experiments.

images (Sect. 2.2.1) is not taken into account. Consequently, the difference between the vertical and the lateral conductivity of the DLC is not reproduced. Simulations on the negative bevelled power diode show that the role of the DLC passivation is not captured at all.

3.3.2 Nitrogen-doped DLC

Here, differently from the previous section, parabolic bands are used to emulate the presence of sp^2 sites [17]. N_c and N_v are fitted, as before, against DFT calculations[26]. Since the energy gap between σ and σ^* bonds is very large when compared with $\pi - \pi^*$ bonds, the contribution of sp^3 sites to the carrier density contribution has been completely neglected. Gaussian traps distribution together with active nitrogen doping are used to take into account the nitrogen incorporation into the DLC layer as shown in Fig. 3.7. The difference between the vertical and the lateral conductivity is now accounted for by splitting the DLC layer in two parts (Fig. 3.8): DLC1 placed at the Si/DLC interface playing the role of the blocking layer observed from TEM images and DLC2 on top of DLC1 which represent the bulk material. No interface

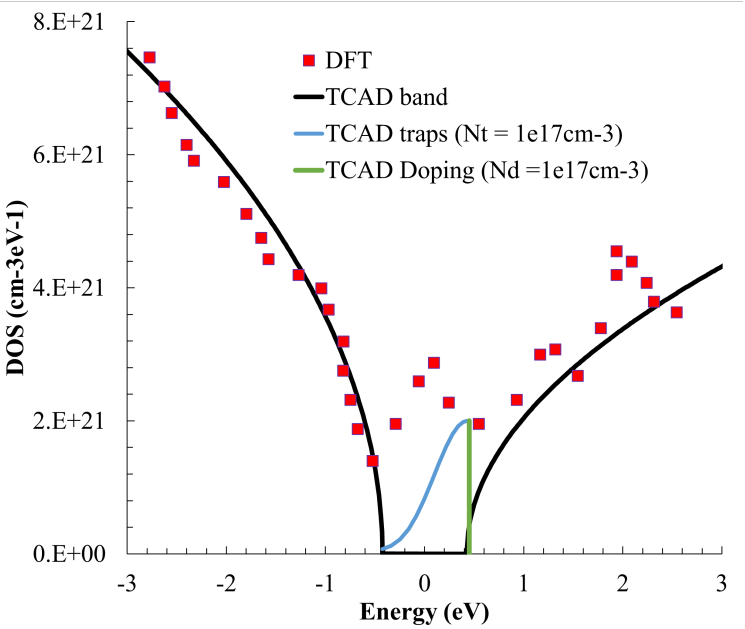


Figure 3.7: DLC band structure implemented into the TCAD simulator compared with the optical model and DFT calculations [26]

layer has been experimentally observed at the metal/DLC interface. In the TCAD simulations of all MIS structures we assume that:

$$\mu_{DLC2} = 100\mu_{DLC1} \tag{3.13}$$

in accordance with the experimental outcomes shown in Sect. 2.2.1. Thus, low-field mobility is the only parameter which differs for DLC1 and DLC2. This means that, in both forward and reverse bias condition, the DLC1 parameters set is anyway dominant on the whole device characteristics, because the DLC1 resistance is the highest one. Thus, it can be fitted against MIS experiments. This model is based only on MIS structures with undoped or, for the first time, nitrogen doped DLC (N-DLC) on top and n-type silicon substrate. Unfortunately, MIM structures with doped DLC are not available. The increase of the current density under forward-bias condition has been reproduced by increasing the low field mobility when compared with the

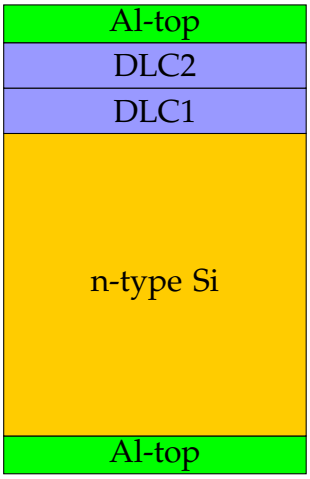


Figure 3.8: Schematic representation of a MIS structure with the DLC layer splitted in two parts.

undoped case. The stronger capacitance peaks are reflected into higher dielectric constant and polarization vector. Both the JV and CV curves are well reproduced as shown in Fig. 3.9.

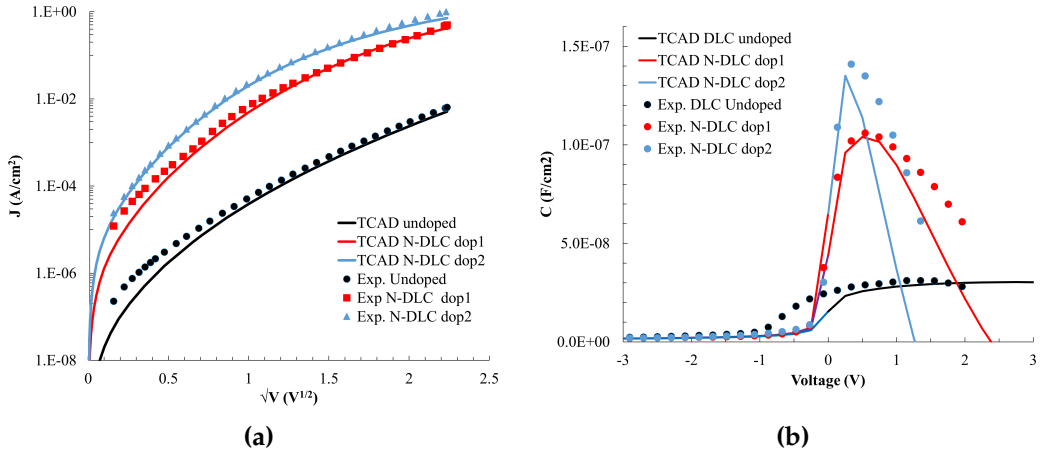


Figure 3.9: Simulated JV and CV curves of MIS structures with undoped DLC and N-DLC compared with experiments.

Application of the DLC model to the simulations of the reference power diode

The breakdown voltage is well captured for different doping concentration and different passivation layer thicknesses due to the presence of positive fixed charge which increase the width of the depletion region along the bevel

(Fig. 3.10a). The role of polarization on the blocking capability has also been investigated. In Fig. 3.10b, the electric field profile along the bevel is reported at a fixed bias of 5400 V, showing the role of the DLC transport properties on the critical surface electric field. The effect of the polarization is quite relevant, as it positively changes the electrostatics within the bevel region, significantly reducing the peak electric field.

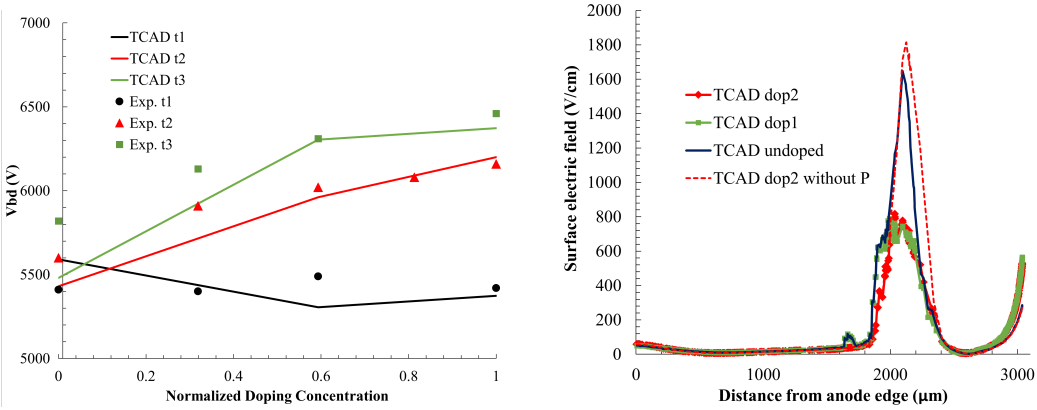


Figure 3.10: (a) The simulated breakdown voltage V_{BD} of the negative bevelled diodes is compared with experiments for different doping concentration and different thicknesses of the DLC layer. (b) Electric field along the bevel vs. distance from anode edge. Solid lines: TCAD results with different nitrogen doping concentrations. Dashed line: TCAD result with maximum doping without the polarization model described in Sect. 3.2.2.

This model has the following drawbacks: it is calibrated only for T = 300K and is not able to reproduce the JV curves of MIS structures with p-type substrate. As shown in Fig. 3.11 , it strongly underestimate the current density under reverse bias condition and shows a significant threshold voltage in the forward regime which is not observed in the experiments. It nicely predicts the breakdown voltage at room temperature. However the leakage current of the power diode can still not be reproduced.

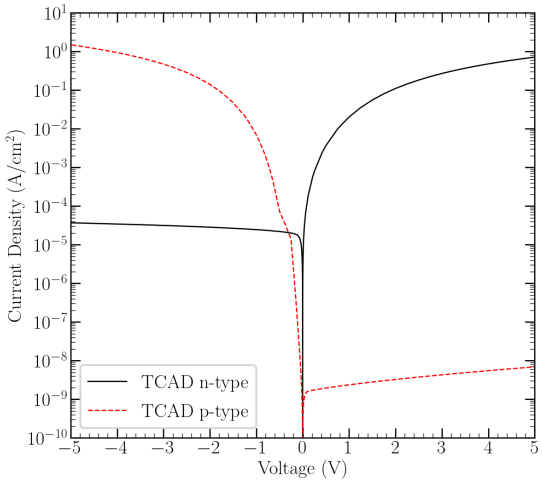


Figure 3.11: Simulated JV curves of MIS structure with N-DLC on top and different doping type of the silicon substrate.

3.3.3 Boron-Doped DLC

The model for boron-doped DLC (B-DLC) is applicable on MIS structures with B-DLC on top and n-type Silicon substrate. Diodes coated with B-DLC have been considered as well. The presence of an interface layer is taken into account as before. Since MIS structures with B-doped DLC and n-type silicon substrate do no exhibit significant threshold voltage no bulk fixed charge is expected to be present in the DLC layer. This means that neither boron ionized atoms for active doping nor acceptor traps can be used. For this reason, two Gaussian density of states, one for each carrier type, have been accounted for as shown in Fig. 3.12. They can be written as:

$$\Gamma(E) = \frac{N_t}{\sqrt{2\pi}\sigma} \exp\left(-\frac{(E-E_0)^2}{2\sigma^2}\right) \tag{3.14}$$

Where N_t is the total number of hopping states σ is the standard deviation and E_0 is the energetic centre of the Gaussian DOS. The number of charge carriers available for the conduction can be calculated using the Fermi-Dirac distribution:

$$n = \frac{N_{t,n}}{\sqrt{2\pi}\sigma_n} \int_{-\infty}^{\infty} \exp\left(-\frac{(E-E_{0,n})^2}{2\sigma_n^2}\right) \frac{1}{1+e^{(E-E_{F,n})/k_BT}} dE \tag{3.15}$$

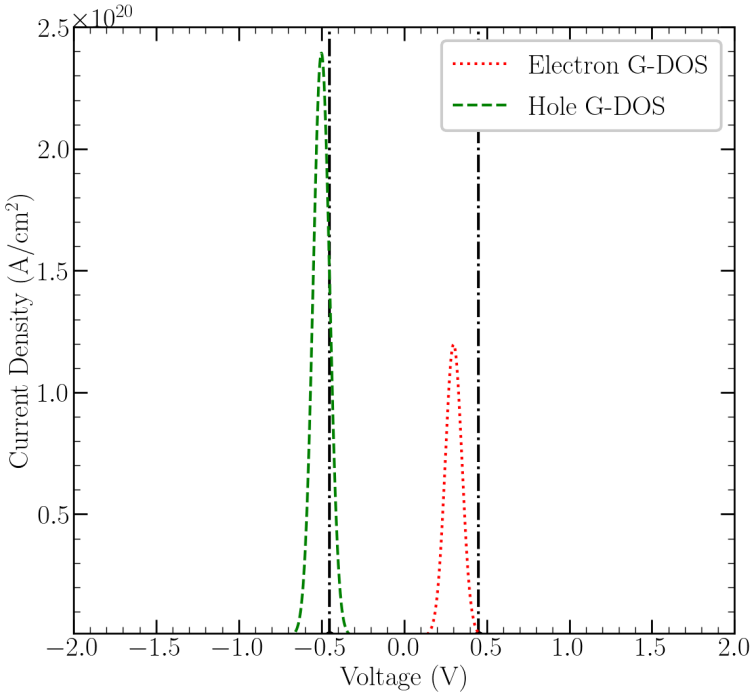


Figure 3.12: Example of Gaussian Density of states into the DLC. The dot-dashed black lines represent energetic reference for the calculation of the energy barrier at the metal/DLC and Si/DLC interface.

$$p = \frac{N_{t,p}}{\sqrt{2\pi}\sigma_p} \int_{-\infty}^{\infty} \exp\left(-\frac{(E - E_{0,p})^2}{2\sigma_p^2}\right) \frac{1}{1 + e^{(E_{F,p} - E)/k_B T}} dE \tag{3.16}$$

The integrals shown above are solved by the simulator using an analytic approximation. [23] [27].The DOS peaks have been calibrated by fitting the J–V curve reported in Fig. 3.13. The high increase of current in forward regime is ascribed to the Poole–Frenkel-like hopping model which has been tuned as discussed before. The standard deviation of the G-DOS has been kept at the default value of the TCAD simulator ($\sigma = 0.05eV$) since the reference experiments at room temperature do not provide any additional information to fix this parameter. In Fig. 3.14a the simulated CV curves are compared with experiments as a function of the applied voltage for different frequencies, while in Fig. 3.14b the capacitance peaks extracted from simulations are compared with experiments as function of the frequency.

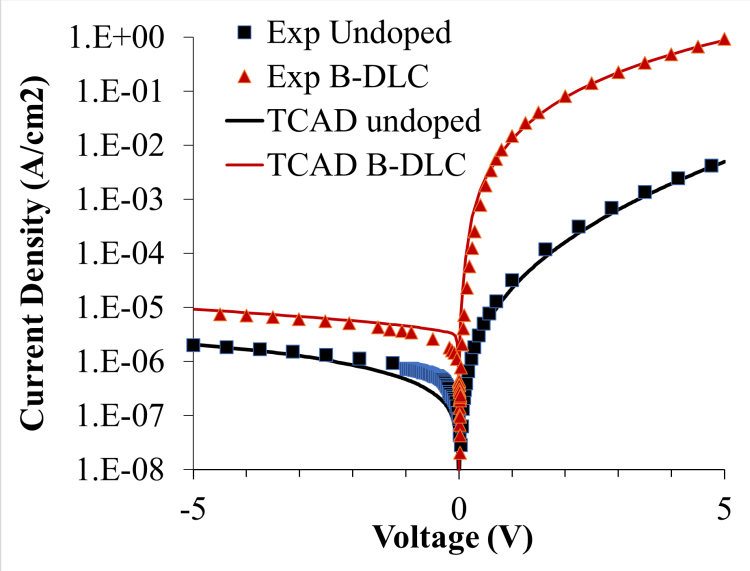


Figure 3.13: Simulated JV curves of MIS structures with undoped and doped DLC compared with experiments.

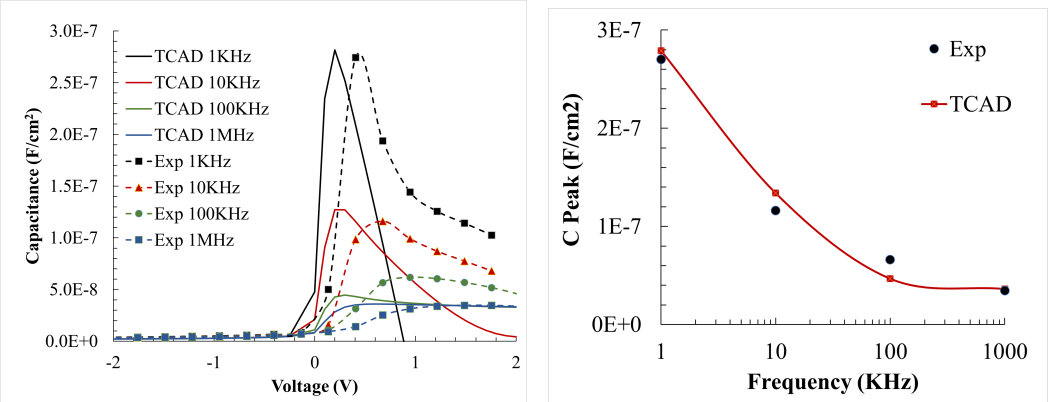
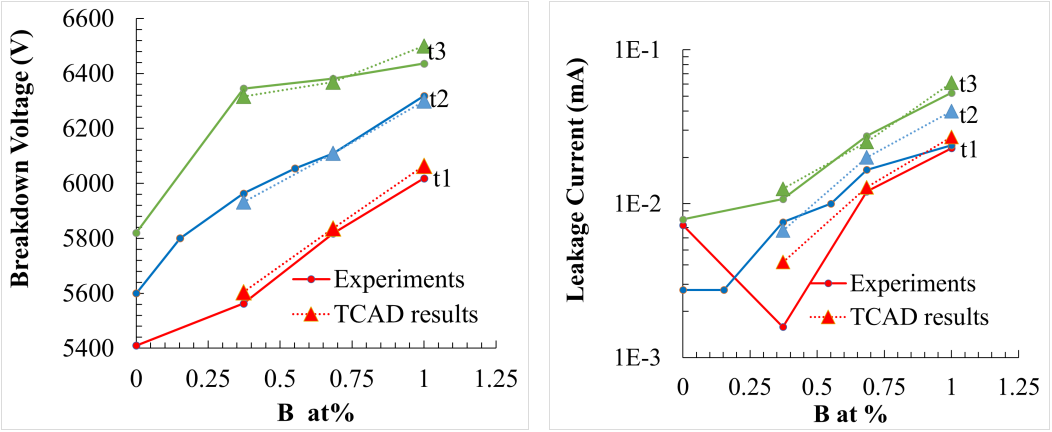


Figure 3.14: (a) Simulated C-V curves of the n-type MIS device with boron-doped DLC on top compared with experiments at different frequencies. TCAD nicely reproduces experiments except for a small shift of threshold voltage. (b) Simulated capacitance peak value extracted from the C-V curves of a n-type MIS device with boron-doped DLC on top compared with experiments. The polarization model nicely reproduces the frequency dependence. Solid line: TCAD results. Symbols: experiments.

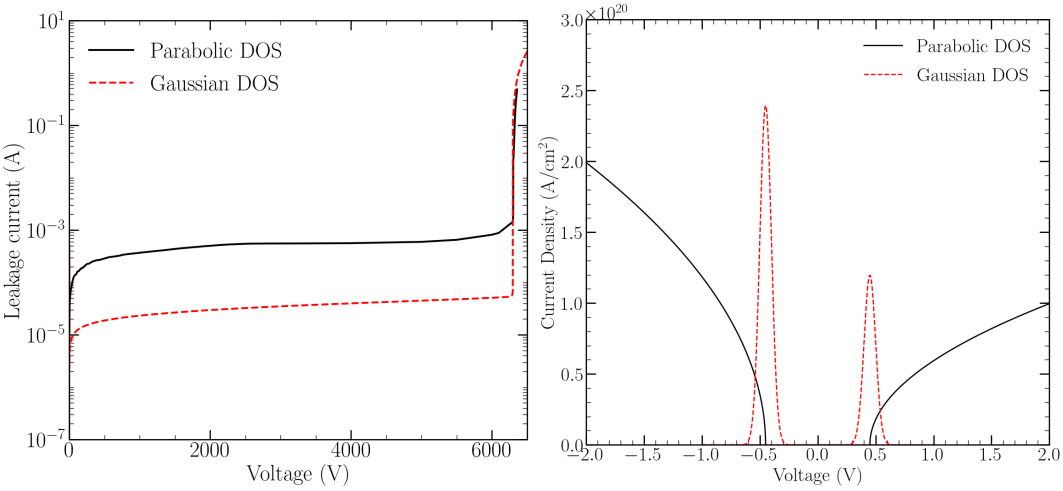
Application of the DLC model to the simulations of the reference power diode The asymmetry between the two G-DOS provides the desired spreading of the depletion region width along the bevel resulting into a higher breakdown voltage. Both the blocking capability and, for the first time, the leakage current are nicely reproduced at room temperature for different boron

concentrations and DLC layer thicknesses. The same results, in terms of



(a) **(b)**

Figure 3.15: Simulated breakdown voltage (a) and leakage current (b) of negative bevelled power diodes passivated with B-DLC compared with experiments for different B concentration and different thickness of the passivation layer



(a) **(b)**

Figure 3.16: (a) Simulated I-V curves of power diodes with different DLC band structure (b) schematic representation of the band structure corresponding to simulations shown in (a)

blocking capability, could have been obtained by using parabolic density of states. In Fig 3.16a, the I-V curves of two simulated diodes under reverse bias condition are shown. In these simulations, the same parameters set have been used in the passivation layer except for the DOSs shape as shown in Fig 3.16b. In both cases, the conduction and the valence band are separated by

the same energy gap (0.9eV) and provide the same intrinsic carrier concentration at the equilibrium ($3.1 \cdot 10^{12} \mathrm{cm}^{-3}$). Similar breakdown voltage can be observed. However, parabolic DOSs result in a much higher leakage current since they have, differently from G-DOS, an infinite number of states available for the conduction. To obtain lower leakage current with parabolic DOSs, N_c and N_v can be tuned as shown in the following section. However, this produces a strong underestimation of the saturation current of MIS structures.

3.4 Improved TCAD model for DLC layers

When compared to the previous sections, a different point of view has been adopted in developing the improved DLC model. Firstly, simulations of the power diode with different coatings have been carried out to understand which parameters of the passivation layer are dominant on the blocking capability and the off-state losses. In addition, both n-type and p-type MIS structures have been considered at the same time. By doing so, it is evident that parabolic DOS or sharp G-DOS cannot provide the desired low Schottky barrier effect and negligible threshold voltage for both electrons and holes as observed in the experiments. In the following sections, a detailed discussion of the TCAD model is provided. More specifically, simulations of the power diode with an ideal SiO_2 or a simple semiconductor as passivation layer are reported in the first-subsection. Then, in the second section, the new TCAD setup for DLC layers is carefully described. Finally, in the third section the application of the new DLC model to the simulations of the reference negative bevelled power diode is shown

3.4.1 Preliminary simulations of a Power Diode

In this section, the simulations with an ideal insulator performed to analyse the electrostatic effect of the passivation layer are discussed in detail. In particular, the presence of an additional path for carriers generated by impact-ionization in the depletion region has been investigated by using a simple semiconductor, with the same band structure of Silicon, on top of the bevel termination.

Electrostatic effect of the passivation layer on the diode performance

As shown in Chapter 1, when a negative bevelled power diode is subjected to a reverse bias, the depletion region along the junction termination W_S has a different width when compared with the bulk silicon W_D. For the device under investigation, if an ideal insulator is assumed as passivation layer, it is $W_S > W_D$ since a very low value of the bevel angle, $\theta \approx 2^\circ$ has been adopted together with a graded doping profile. Fig. 3.17a shows the electric field distribution to along the vertical direction for two different x positions (Fig. 3.17b): (i) at a location where the electric field has its maximum value at the junction termination ($x = 44.26mm$) (ii) far from the junction termination where the electric field distribution is equivalent to that of a one-dimensional simulation ($x = 24mm$). It can be observed that, along the bevel, the surface electric field is lower than in the bulk as expected from a properly designed termination. The maximum electric field is, however, slightly higher when compared with the maximum electric field at a location far from the junction termination. For this reason, the negative bevelled power diode exhibits a reduced breakdown voltage ($BV \approx 5500V$) with respect ot to one-dimensional simulations of the ideal p-n junction is ($BV \approx 6800V$).In the next paragraphs, the presence of bulk fixed charge or electric dipoles in the passivation layer

will be accounted for in order to understand their impact on the diode breakdown voltage.

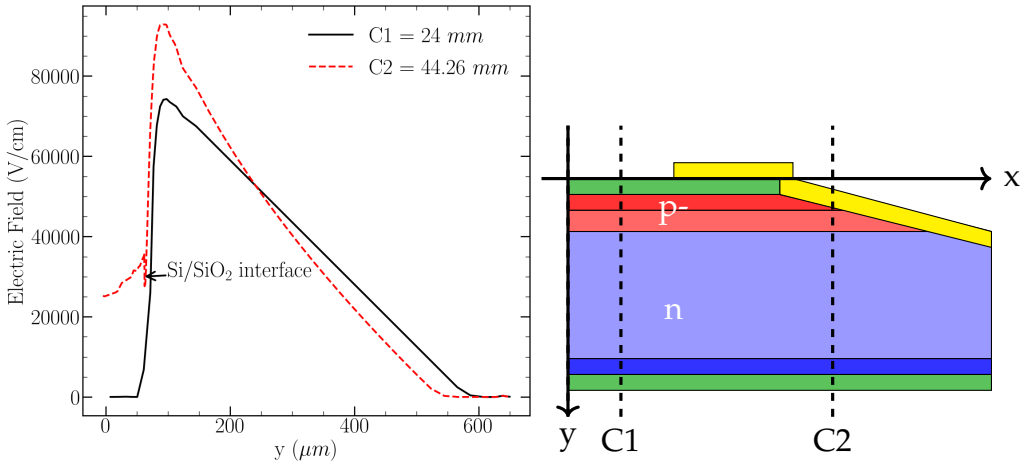


Figure 3.17: (a) Electric field distribution (y-component) along the vertical direction for different x positions in the negative bevelled power diode. (b) Schematic representation of the power diode with negative bevel termination and SiO_2 as passivation layer (yellow area). Black dashed lines (C1 and C2) show the position of the cutlines used to extract the electric field profiles shown in (a). Structure not in scale

Fixed charge The simplest case is represented by a perfectly insulating passivation layer with positive or negative bulk fixed charge. In the following simulations SiO_2 has been used as passivation material. From simulations it can be deduced that the the leakage current is not affected by the presence of fixed charge: an ideal SiO_2 gives no contribution to the charge transport and for this reason there is not an additional path for carrier generated in the space charge region. On the contrary, the breakdown voltage increases with negative fixed charge and decreases with positive fixed charge when compared with a structure without fixed charge. The different electric field distribution shown in (Fig. 3.18) and then the different breakdown voltage reported in table 3.1 can be explained with the analysis of the influence of the fixed charge on the charge distribution in Silicon.

Table 3.1: Breakdown voltage

Charge type	Quantity	Breakdown Voltage
+	5e16 (cm^{-3})	5302
-	5e16 (cm^{-3})	6086
/	0	5540

- Positive charge: it pushes away holes from the interface → Si is more depleted in p- region → the electric field is shifted toward the p+ region but the width of the depletion region decreases → the electric field is higher → lower breakdown voltage.
- Negative charge: it attracts holes at the interface → Si is depleted in n- region → the width of the depletion region increases → lower electric field → higher breakdown voltage.

In Fig. 3.19 the 2D contour plot of the electrostatic potential into the junction termination region is reported for the different cases shown in Fig. 3.18.

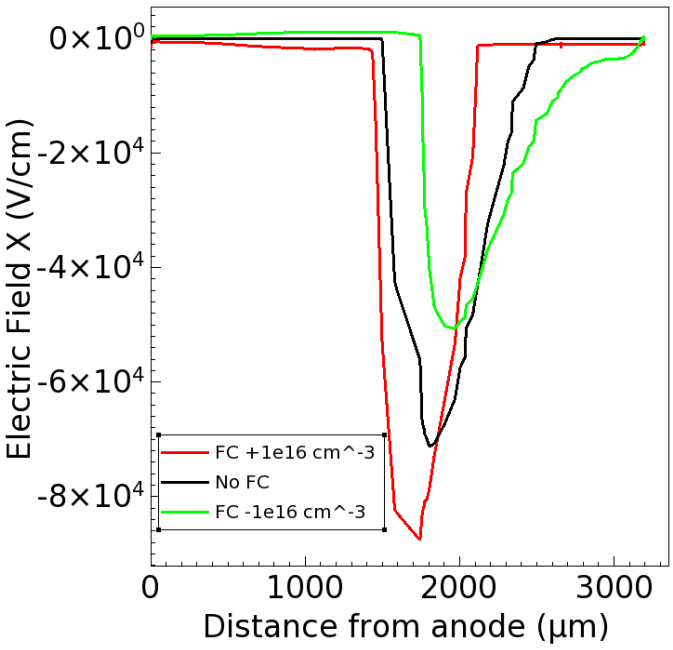


Figure 3.18: X-component of the electric field along the bevel for different amount of fixed charge inside the passivation layer extracted at 4000V under reverse bias condition.

From the significant reduction of the blocking capability with positive fixed

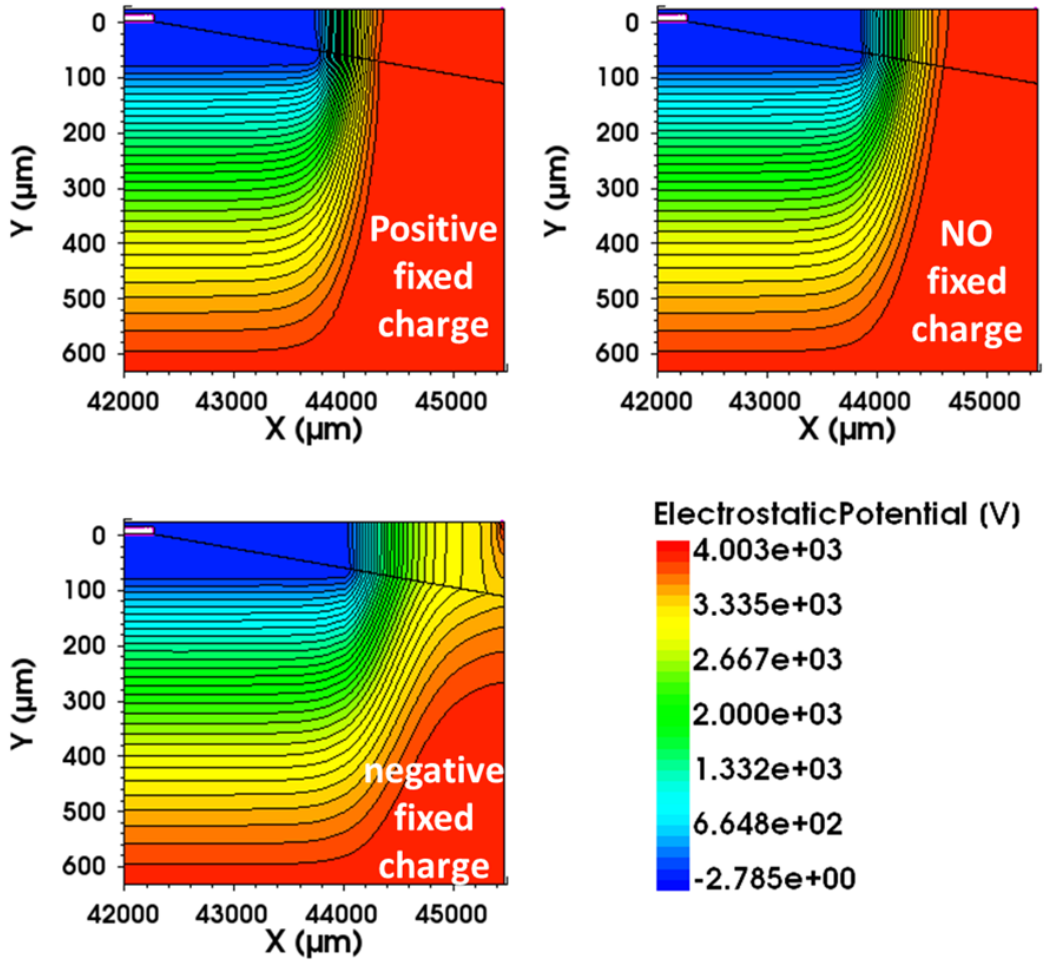


Figure 3.19: Electrostatic potential distribution in the diodes for different types of fixed charge inside the passivation layer

charge, it can be deduced that negative bevel junction termination can not be passivated with ideal SiO_2. Indeed, the large number of defects coming from the wafer sawing can results in a significant and unpredictable amount of fixed charge at the Si/SiO_2 interface. It can negatively affects the reproducibility of the breakdown voltage and the long-term reliability of the device

Polarization By performing simulations with SiO_2 as passivation layer switching on the ferroelectric model, it is possible to observe the effects of polarization on the breakdown voltage. Simulations show that polarization has a

small influence on the performance of the device. Usually a higher polarization vector ***P*** provides a increase of the breakdown voltage as shown in Fig. 3.20

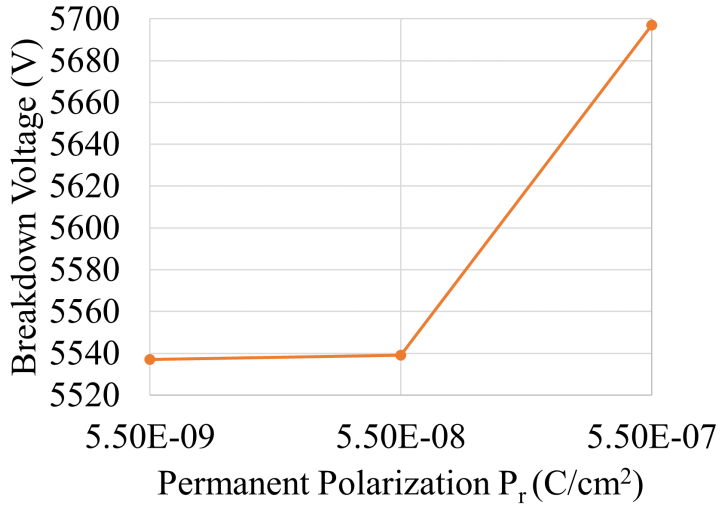


Figure 3.20: Breakdown voltage as function of the Residual polarization inside the SiO_2 layer.

Charge transport effect of the passivation layer on the diode performance

When the passivation layer is able to transport charge it can provide an additional path for carriers generated in the space charge region. In order to simplify the treatment, a simple semiconductor with the following characteristics has been used:

- Electron affinity and band gap of silicon $\rightarrow$ no barrier between the passivation layer and the silicon substrate.
- Simple parabolic band structure
- Constant mobility
- SRH Generation-recombination processes are not allowed

Without the presence of fixed charge inside the DLC bulk or at DLC interface, it is not possible to modify the breakdown voltage. However, the

leakage current is strongly influenced by the intrinsic carrier density thought the number of states available for the conduction. In Fig. 3.21, the breakdown voltage and the leakage current of a semiconductor with the features reported above are reported. It possible to observe a negligible decrease of the breakdown voltage by increasing the intrinsic carrier density and a very high increase of the leakage current. Considering a doped semiconductor

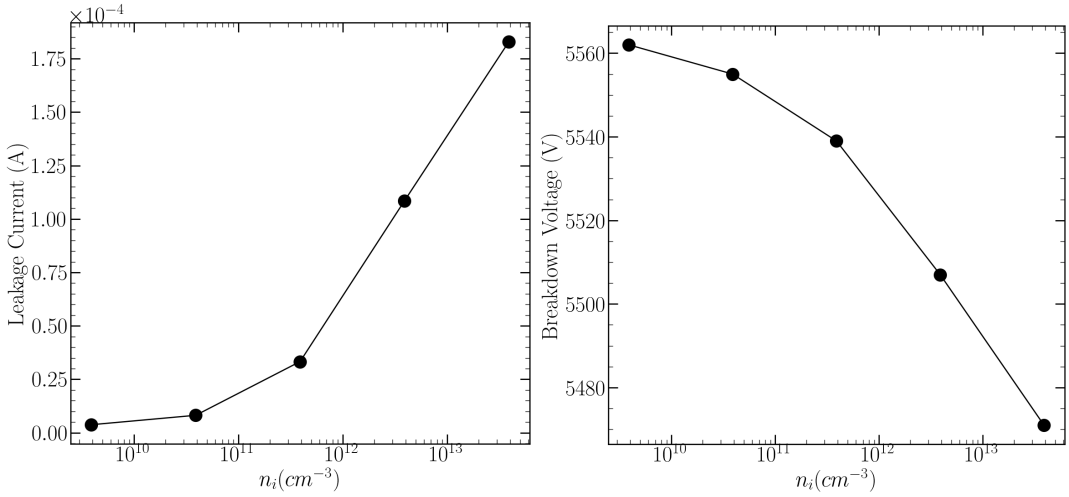


Figure 3.21: Simulated leakage current (I_{IOFF}) (a) and breakdown voltage (b) at room temperature as function of the intrinsic carrier density of the passivation layer.

applied to the bevel termination, a significant variation of the breakdown voltage can be obtained.

- n-type semiconductor: when active nitrogen doping is added in the semiconductor, differently from the previously described ideal insulator, the electric field peak is not only shifted toward the p+ region but its magnitude is reduced due to a spreading of the depletion region. It is then observed an increase of both leakage current and breakdown voltage. In Figure 3.22, the TCAD results performed with $n_i = 3.94 \cdot 10^{12} cm^{-3}$, doping concentration $5 \cdot 10^{16} cm^{-3}$ and different mobilities are reported. If the blocking interlayer is taken into account (red lines), the best performance is obtained. In these examples $\mu_{DLC1} =$

$10^{-6} cm^2/Vs$, $\mu_{DLC2} = 10^{-4} cm^2/Vs$ and an interlayer thickness of $t_{DLC1} = 70nm$.

- p-type semiconductor: negative fixed charge has been added by using boron active doping with concentration $N_A = 5 \cdot 10^{16} cm^{-3}$. It provides a spreading of the depletion region towards the n- region as shown for the SiO_2 case. Both leakage current and breakdown voltage increase with thickness if the mobility is sufficiently high (Fig. 3.23).

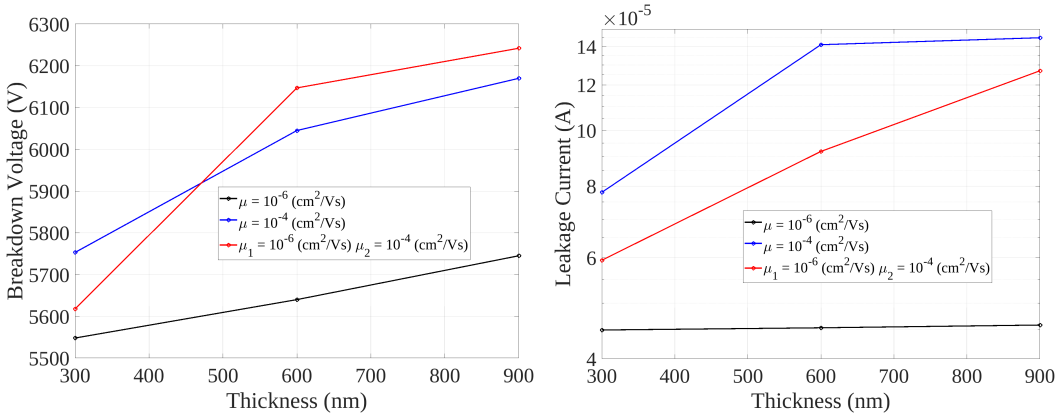


Figure 3.22: Breakdown voltage (a) and leakage current (b) as function of the total DLC thickness for different value of the passivation layer mobility assuming the presence of positive fixed charge.

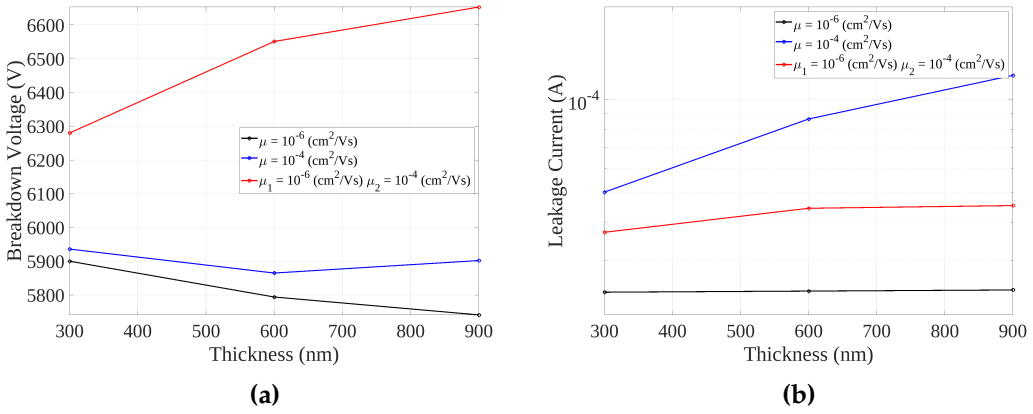


Figure 3.23: Breakdown voltage (a) and leakage current (b) as function of the total DLC thickness for different value of the passivation layer mobility assuming the presence of negative fixed charge.

The SRH model has been finally switched on assuming the presence of a trap level in the mid-gap with very small carrier lifetimes ($\tau_e = \tau_h = 5 \cdot 10^{-10} s$) to emulate the presence of a high number of defect states. Simulations were carried out using $\mu_1 = 10^{-6} \frac{cm^2}{Vs}, \mu_2 = 10^{-4} \frac{cm^2}{Vs}$ and nitrogen active concentration $N_D = 5 \cdot 10^{16} cm^{-3}$ because it is the setup that provided the best fitting in the previous analysis. It comes out that the SRH recombination plays a very small role since it provides negligible variations of the breakdown voltage (Fig. 3.24a) and a small increase of the leakage current (Fig. 3.24b).

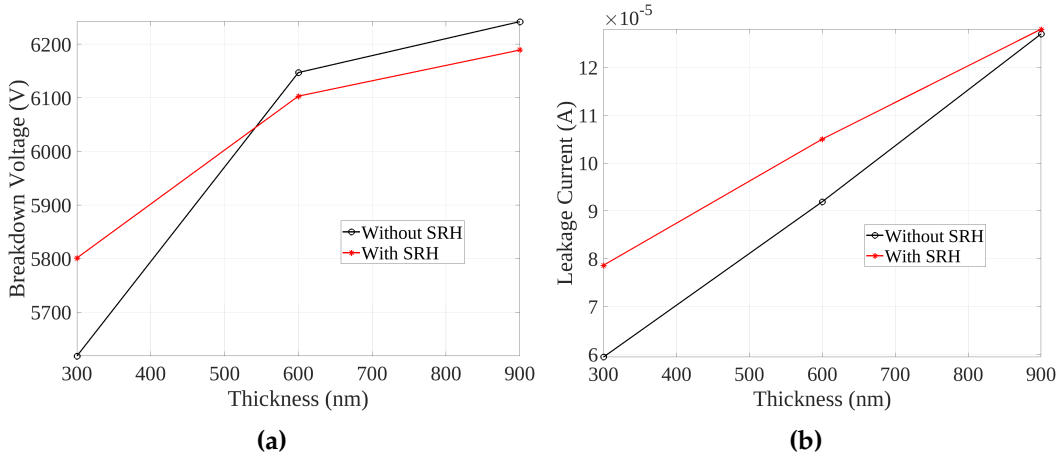
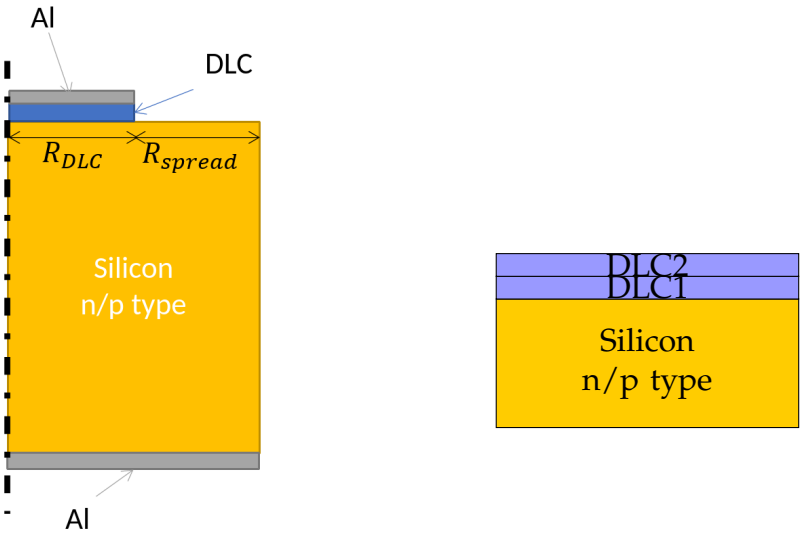


Figure 3.24: Breakdown voltage (a) and leakage current (b) of the simulated power diode as function of the passivation layer thickness assuming the presence of positive fixed charge. The SRH recombination model is activated with lifetimes $\tau_e = \tau_h = 5 \cdot 10^{-10} s$.

3.4.2 TCAD setup for MIS structure

MIS simulations were performed on a 2D structure with cylindrical symmetry in order to account for the effect of the current spreading within the substrate in the samples (Fig. 3.25a). R_{DLC} and R_{spread} have been fixed to a reference radius value and lateral extension, respectively. As done in the previous models, an area factor has been used to normalize the simulations results. R_{spread} was chosen large enough to guarantee that the influence of the Silicon substrate resistance due to the current vertical spreading is completely



(a) Schematic representation of the simulated MIS structures **(b)** Detail of the interlayer at Si/DLC interface in the TCAD domain

Figure 3.25

accounted for. A few checks have been carried out to verify that the chosen geometry can be correctly used to simulate the different structures. Quite no significant effect of the spreading resistance is visible when $\sigma_{DLC} << \sigma_{Si}$, as all the experimental data carried out on MIS devices with different top-electrode areas can be normalized and nicely compared. Vice versa, in the MIS devices experiencing large DLC doping and large temperature, the contribution of the Silicon resistance becomes relevant, and the lateral spreading needs to be accounted for. The DLC layer has been divided in two parts as in the previous model (Fig. 3.25b). In addition, since JV curves of MIS structure with the same DLC on top but different substrate doping type are almost symmetrical, *the same parameter set has been used for electrons and holes in DLC*.

Band structure

The band structure properties of the new DLC model are described in this section. In the first paragraph, a new setup for the Gaussian density of states is proposed. Differently from the previous model on B-DLC, completely symmetric bands with large standard deviation are now implemented. The

effects of this approach on the metal/DLC Schottky barrier are described in the second paragraph.

Gaussian density of states Gaussian density of states (G-DOS), one for each charge carrier have been accounted for as shown in Fig. 3.12. The gap between the two bands is equal to 1eV according to optical measurements performed by ABB Switzerland Ltd Semiconductors. Since symmet-

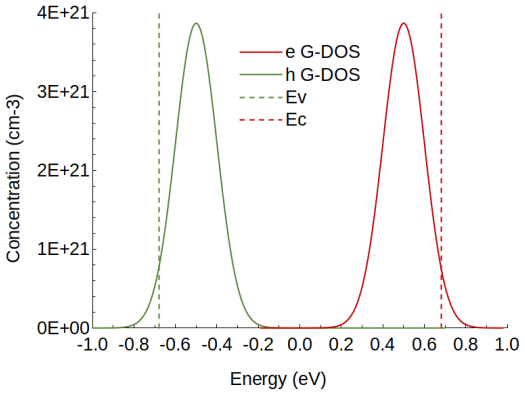


Figure 3.26: Example of Gaussian Density of states into the DLC. E_c and E_v represent the energetic reference value for the conduction and the valence band respectively

rical bands are required to reproduce the JV curves of MIS structures with different substrate doping type it has been assumed that $N_{t,n} = N_{t,p}$, $\sigma_n = \sigma_p$ and $E_{0,n} = -E_{0,p}$. This means that the width of the depletion region along the bevel termination can not be increased by exploiting the asymmetry of the G-DOS as done in the previous section (see Fig. 3.12) for the B-DLC [19]. This can be addressed by using active doping which provides the required amount of bulk fixed charge as suggest by the preliminary simulations performed on the diode. In addition, it gives the slightly asymmetry in the reverse bias current density observed in the experiments.

Effect of the GDOS bands on the metal/DLC Schottky barrier The impact of the value of the metal work-function on the MIS J-V curves is reported in Fig. 3.27 for two different G-DOS standard deviations. By using a broad

G-DOS for both electrons and holes ($\sigma \approx 0.1eV$), the J-V curves show a very limited dependence on the metal work-function due to partial E_F pinning given by the band tails. However, to obtain symmetrical J-V curves, it is still necessary to fix the metal work-function of the top electrode at

$$\Phi_M = \chi_{DLC} + \frac{E_{g,DLC}}{2}, \tag{3.17}$$

where χ_{DLC} is the electron affinity of the DLC and $E_{g,DLC}$ is the DLC energy gap, thus assuming a strong E_F pinning at the mid-gap. In this way, electrons and holes experience the same energy barrier at the metal-DLC interface and consequently give the same contribution to current both in positive and negative bias regimes. In Fig. 3.28 the simulated J-V curves are reported for dif-

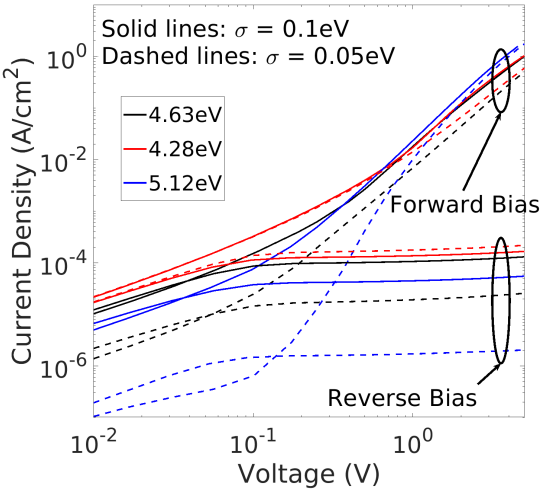


Figure 3.27: Simulated J-V curves curves of a MIS structure with nitrogen doped DLC and n- type Silicon substrate for different values of the metal workfunction and two different values of the standard deviation of the G-DOS

ferent N_t in the G- DOS. The figure clearly shows a significant dependence of the saturation current levels on N_t and an undesired threshold voltage in the forward curve of the p-type MIS for the lowest magnitudes of N_t. A schematic representation of the band diagram is reported in Fig. 3.29. The standard deviation has been thus fixed to $\sigma = 0.1eV$ since this value provides the desired independence of the JV curves from the metal work-function and

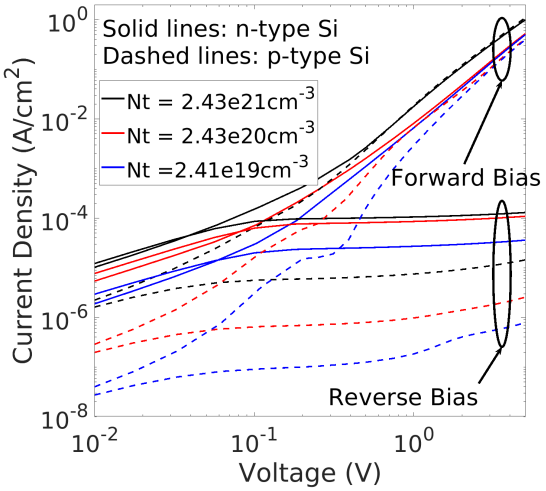


Figure 3.28: Simulated forward and reverse bias JV curves of a MIS structure with NDLC and different doping substrate

it is in nice agreement with the Gaussian disorder model described in [28] and [29]. In addition, symmetrical energetic barriers at Si/DLC are assumed, that is $\Delta E_c = \Delta E_v$ defined as $\Delta E_c = \chi_{Si} - \chi_{DLC}$. Their exact value is relevant to reproduce the temperature dependence of the reverse bias JV curves as described in the following sections.

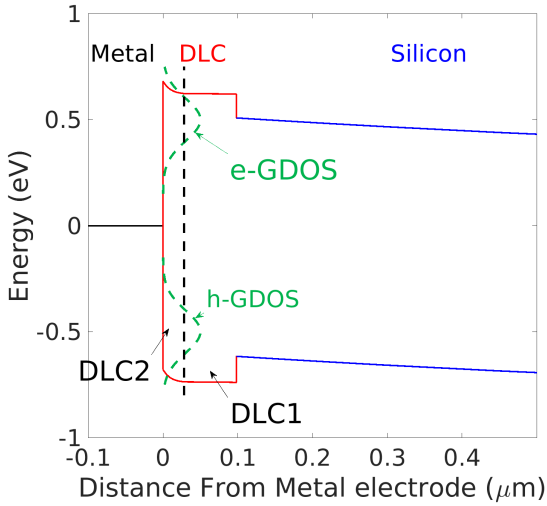


Figure 3.29: Energy band diagram of a MIS structure with nitrogen doped DLC and n-type Silicon substrate

SRH recombination

The SRH recombination has been accounted for assuming, as shown in the preliminary simulations on the power diode, that the trap level is placed at the mid-gap with $\tau = \tau_e = \tau_h = 5 * 10^{-10}$ s. However, the specific value of the carrier lifetime is not relevant at all. It can be changed by several order of magnitude without affecting significantly the MIS behaviour as shown in Fig. 3.30 where the JV curves with different values of τ are compared.

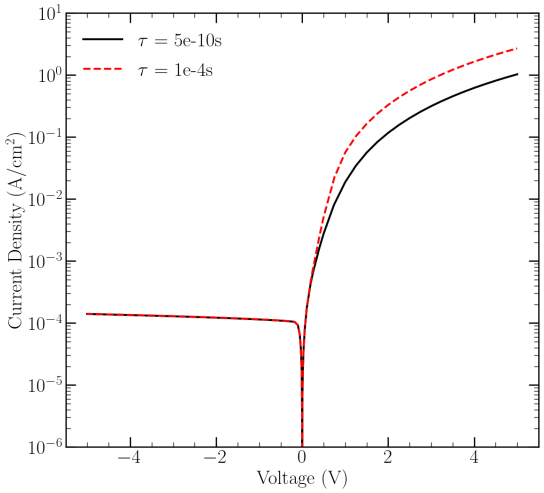


Figure 3.30: Simulated JV curves of MIS structures with different values of the SRH lifetimes.

The role of active doping on the asymmetry of the J-V curves

The model described so fare makes no distinction between electron and holes since the same parameter set has been used for both charge carriers. Differently from the models described in the previous section (e.g. Fig. 3.11), this leads to perfectly symmetric JV curves of MIS structures with different doping type of the silicon substrate. The experimentally observed asymmetry in the saturation current can be explained assuming the presence of bulk fixed charge into the DLC layer which has been modelled using active doping. Fig. 3.31 shows the extracted value of the simulated saturation current at $\pm$5 V for MIS structures with different doping type of the DLC layer and different substrate as function of the DLC doping content. The small difference

observed in the undoped case are ascribed to the different doping concentration of the silicon substrate: $N_D \approx 10^{14}$ cm^{-3} for n-type Si while for p-type Si $N_A \approx 8.1 \cdot 10^{14}$ cm^{-3}.

Thanks to the additional active doping, the DLC bands of the N-DLC device are shifted towards lower energy reducing the difference between the conduction band and the Fermi level (not shown). If the silicon substrate is n-doped (Fig. 3.32a) this results into a slightly higher electron concentration close to the Si/DLC interface what reduces the resistivity of the MIS structure. On the contrary, for a p-doped silicon the energy difference between the valence band and the Fermi level is increased with a consequent reduction of the hole concentration. Close to the Si/DLC interface, the silicon resistivity is then increased with the consequence of a lower reverse current density (Fig. 3.32b). Symmetric considerations can be made for the B-DLC.

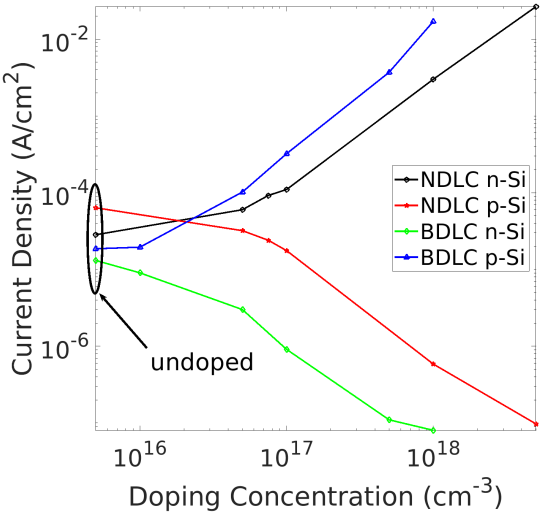
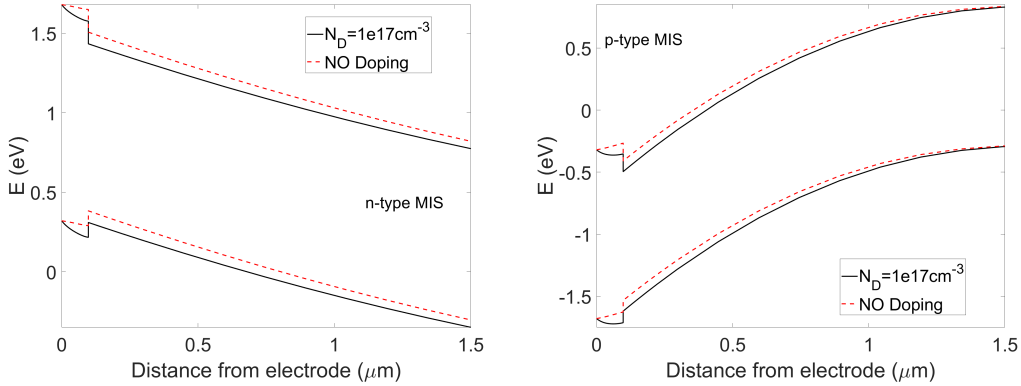


Figure 3.31: Saturation current of MIS structure under reverse bias condition extracted at $\pm 5V$ with different doping type and concentration

Temperature dependence

In order to extend the validity of the propose approach to different temperatures it is necessary to analyse how the different models described in the previous sections contribute to the temperature dependence of the JV curves.



(a) **(b)**

Figure 3.32: Band diagrams of MIS structure with or without doping. (a): n-type MIS, (b): p-type MIS

The temperature dependence of the forward bias JV curves is affected only by the activation energy of the PF mobility as shown in Fig.3.33a. When $E_a = 0$, which means that the mobility is temperature independent, the current density extracted in the SCLC region becomes constant in the whole temperature range. On the contrary, under reverse bias conditions different phenomena contribute to the temperature dependence of the saturation current since the current density still increases with temperature even if $E_a = 0$ (Fig. 3.33b). Moreover, the DLC intrinsic carrier concentration plays a limited role since the temperature dependence of the broad G-DOS is very weak [27]. A significant contribution is instead given by the barrier height at the Si/DLC interface ΔE_C. For example, by changing ΔE_C from 0.12 to 0.3 eV, the depletion region on the silicon side close to the interface is differently modulated (Fig. 3.34a), giving rise to a correlated temperature dependence as shown in Fig. 3.34b. With the setup described above it is then possible to reproduce the JV curves of MIS structures with the same DLC on top but different doping type of the silicon substrate with the same parameter set in the whole temperature range (Fig. 3.35 - 3.38). The room temperature (300K) experimental J-V curves of the MIS structures with different substrate doping for both boron- and nitrogen doped DLCs (the cases with maximum doping

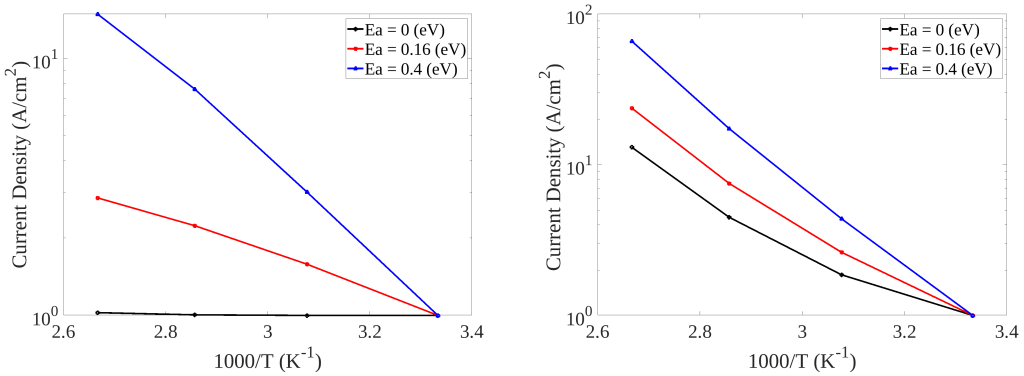


Figure 3.33: Forward bias (a) and reverse bias (b) current densities extracted at $\pm 2V$ as function of the inverse temperature for different value of the Poole-Frenkel activation energy.

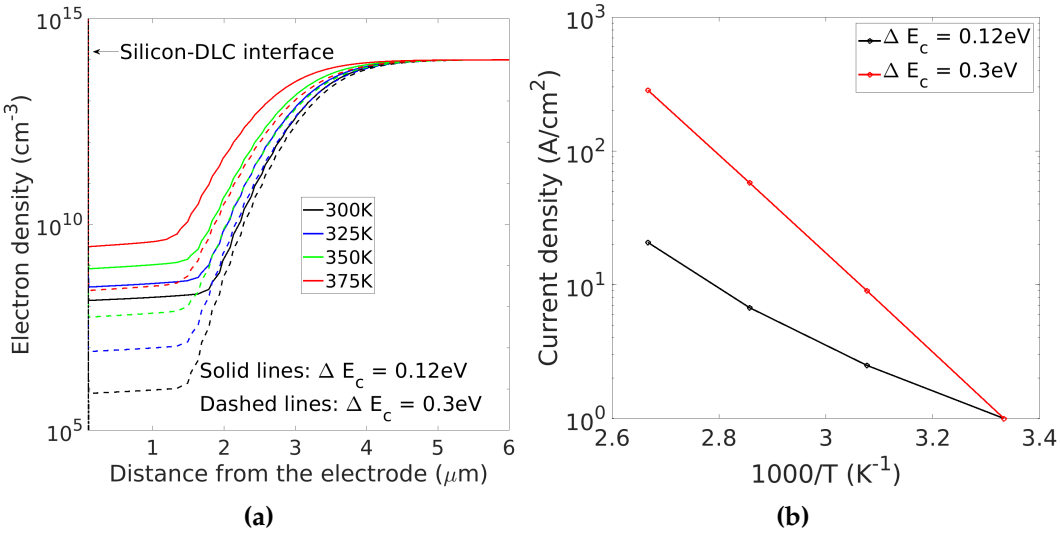


Figure 3.34: (a) Simulated electron density at the DLC/Si interface for different temperatures and different values of ΔE_c for a MIS structure with NDLC and n-type Silicon (b) Simulated current densities normalized with respect to the current density at room temperature, under reverse bias condition at -5V for different temperatures and two different values of ΔE_c for a MIS structure with NDLC and n-type Silicon.

level are used here as reference) are compared with the TCAD simulations in Fig. 3.35. A nice agreement between TCAD simulations and experiments has been found. Also the temperature effects are well captured as shown in Figs. 3.36 and 3.37. Fig. 3.38 shows a comparison between the simulated CV curves and the experiments. It can be observed that even with a

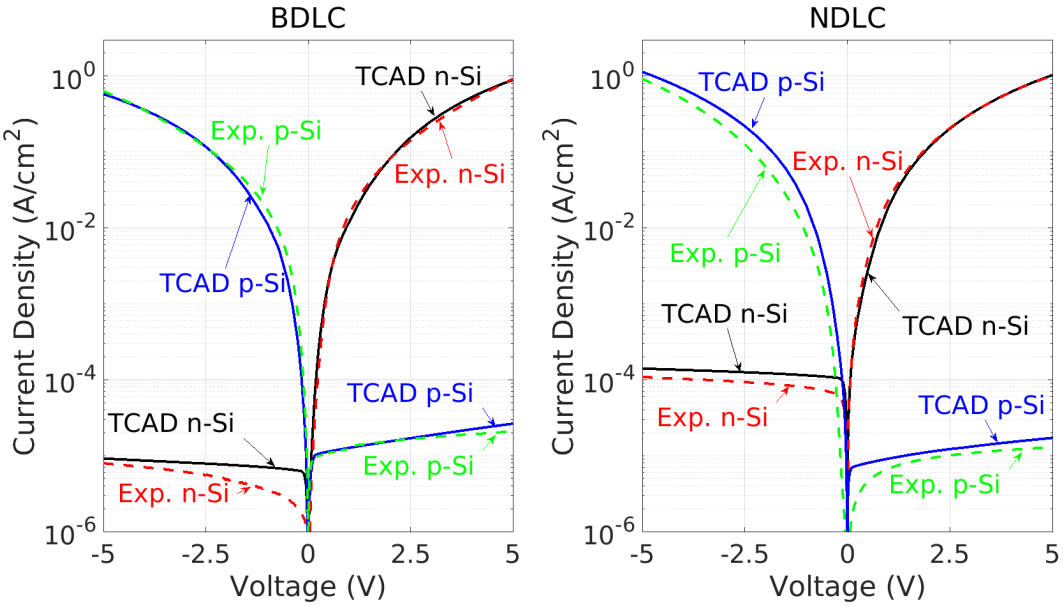


Figure 3.35: J-V curves of MIS structures at room temperature for different silicon substrates. Experiments (dashed lines) are compared with TCAD predictions (solid lines). (left): boron-doped DLC. (right): nitrogen-Doped DLC.

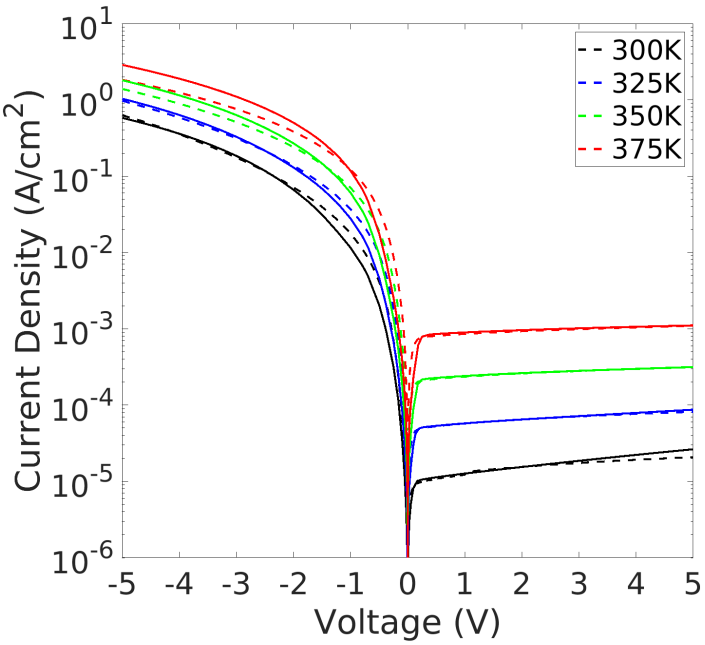


Figure 3.36: J-V curves of MIS structures with p-type silicon substrate and BDLC at different temperatures. Experiments (dashed lines) are compared with TCAD predictions (solid lines).

single time-constant equation it is possible to qualitatively reproduce the frequency dependence of the capacitance. The parameter set for both NDLC and BDLC with the highest doping concentration are summarized in Table

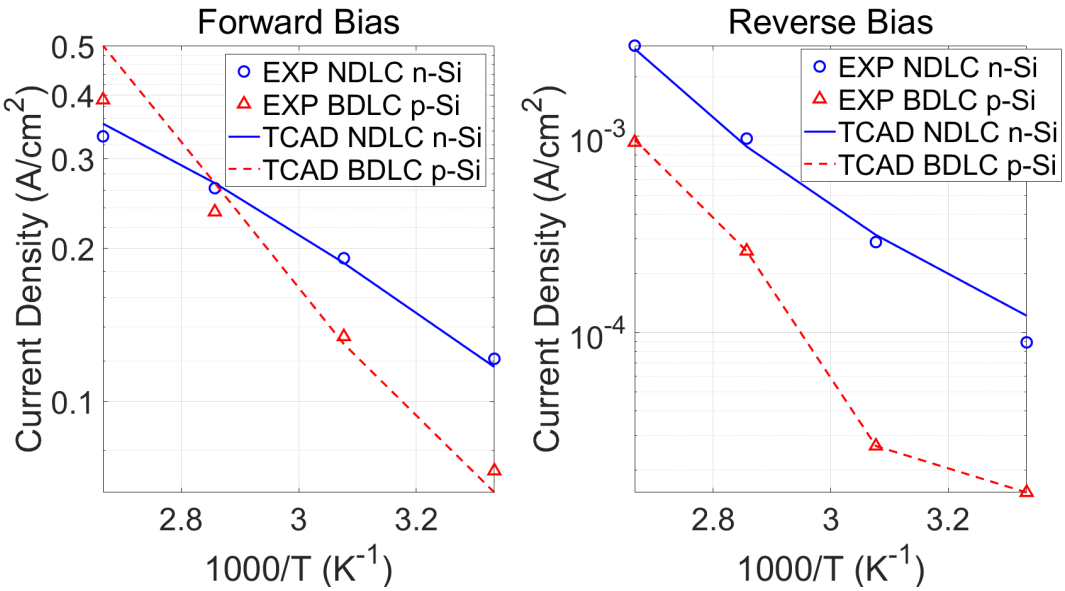


Figure 3.37: Current density extracted at Vbias = ± 2V as function of temperature. Experiments (symbols) are compared with TCAD predictions (lines).

3.2. As described before, the gap between the two G-DOS is fixed by optical measurements. The values used for σ and N_t provide a low Schottky barriers for both carriers and avoid the undesired threshold voltage in the forward bias JV curves. In addition, similar values have been found in literature for amorphous materials[28] [29]. No correlation has been observed between the relative dielectric constant and the parameter β of the PF mobility model which should be given by $\beta = \frac{1}{k_B}\sqrt{\frac{e^3}{\pi\varepsilon_r\varepsilon_0}}$. The value of the PF activation energy used in the TCAD simulations is very close to those extracted from the Arrhenius fitting shown in Fig. 2.14. The relative dielectric constant ε_r fitted against the CV curves measured at 1MHz is consistent with literature [30].

3.4.3 Simulations of power diodes with DLC passivation

It has been shown that the breakdown voltage of the power diode can be affected only by the presence of fixed charge inside the passivation. In addition, the presence of a low mobility interlayer close to the Si/DLC interface

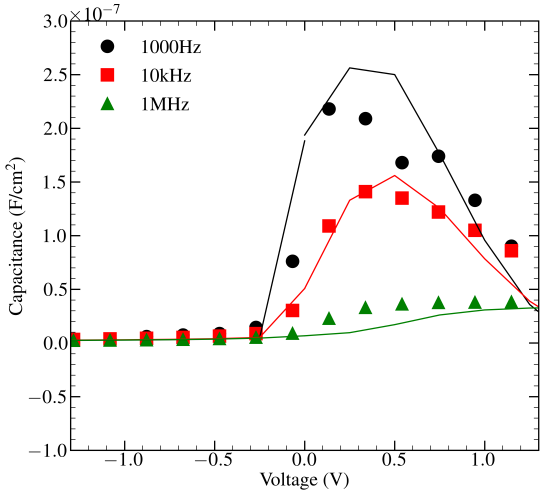


Figure 3.38: Measured CV curves of a MIS structure with N-DLC and n-type silicon substrate as function of the applied voltage for different frequencies compared with TCAD simulations

Table 3.2: TCAD parameters set

Symbol	Quantity	NDLC	BDLC
t_{DLC}	Measured total DLC thickness (nm)	98	140
t_{DLC1}	DLC1 thickness (nm)	70	70
t_{DLC2}	DLC2 thickness (nm)	28	70
E_g	Energy gap (eV)	1.36	1.36
χ	Electron Affinity (eV)	3.95	3.95
Φ_M	Metal Work function (eV)	4.63	4.63
N_t	Number of hopping states (cm^{-3})	$2.43{\cdot}10^{21}$	$2{\cdot}10^{20}$
$E_{0,e}$	Electron G-DOS energy position (eV)	0.18	0.18
σ	Standard deviation (eV)	0.1	0.1
N_D	Doping concentration (cm^{-3})	10^{17}	10^{16}
$\mu_{0,DLC1}$	DLC1 Low-field mobility (cm^2/Vs)	$3.07{\cdot}10^{-4}$	0.01
$\mu_{0,DLC2}$	DLC2 Low-field mobility (cm^2/Vs)	$3.07{\cdot}10^{-2}$	1
E_a	Poole-Frenkel activation energy (eV)	0.16	0.23
β	Fitting parameter ($Kcm^{0.5}/V^{0.5}$)	1.2	1.7
ϵ_r	Relative dielectric constant	4	5.4
P_s	Saturation Polarization (C/cm^2)	$1.5{\cdot}10^{-6}$	$1.5{\cdot}10^{-6}$
P_r	Permanent Polarization (C/cm^2)	$3{\cdot}10^{-8}$	$6{\cdot}10^{-8}$
F_c	Coercive Field (kV/cm)	10^4	10^4
τ	Relaxation time (s)	$1.7{\cdot}10^{-5}$	$3.1{\cdot}10^{-5}$

further increases the blocking capability for higher thicknesses of the semi-insulating layer. Moreover, the leakage current is mainly affected by the intrinsic carrier density of the passivation. A significant contribution comes

from its mobility and thickness. These results, especially those concerning the leakage current, need to be extended and validated against experiments. In order to do so, the band diagrams of the Si-DLC vertical structure along the bevel and the corresponding MIS devices are reported in Fig. 3.39 . In the p- region (Fig. 3.39 (a)), silicon is fully depleted at the surface and the equivalent MIS structure is reverse-biased 3.39 (c)): holes are injected from DLC into silicon, the leakage current is limited by the reverse-biased regime. In the n-doped region 3.39 (b)), silicon is fully depleted at the surface and the equivalent MIS structure is reverse-biased 3.39 (d)): electrons are injected from DLC into silicon, but the leakage current is limited by the reverse-biased regime. When moving to the quasi-neutral regions at the p+ or at the bevel edge, silicon is no more depleted at the surface, but the equivalent MIS structure is still slightly reverse-biased (at the anode side or switched off. Thus, I_{OFF} depends mainly on the intrinsic carrier density and the doping concentration of the DLC as in the reverse biased MIS devices. At room temperature, the I_{OFF} can be then tuned by acting on the G-DOS without significant changes in the breakdown voltage as previously shown in Fig. 3.21. The DLC model has been finally validated comparing TCAD predictions with measurements on the reverse-biased diode at room temperature for the four differently doped passivations and different DLC thicknesses (Figs. 3.40 and 3.41). A nice agreement has been found up to the onset of avalanche regime as can be observed from the IV curves shown in Fig. 3.42. The 2D contour plots of the electrostatic potential at the junction termination of the 4.5kV diode are shown in Fig. 3.43. As expected, the depletion region width at the Si/DLC interface is strongly influenced by the doping type inside the DLC. When the NDLC is used, silicon at the interface is more depleted in the p-region since positive ions in the DLC improve the p-doped silicon depletion underneath. Symmetric considerations can be made for electrons in the silicon n-region when the passivation layer is realized with a B-DLC.

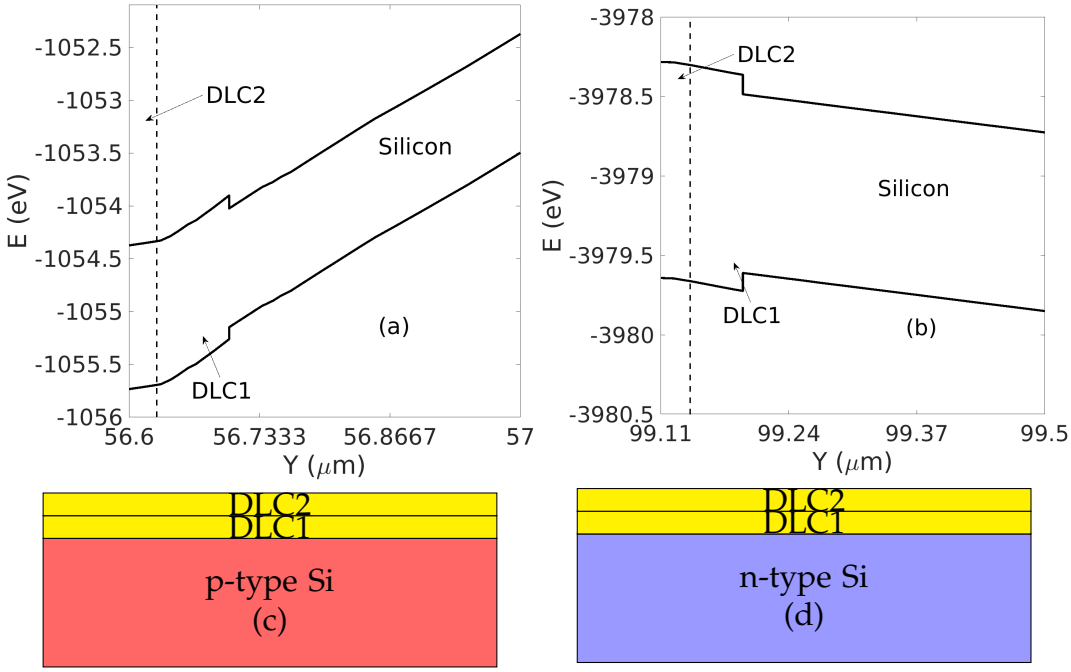


Figure 3.39: Band plot of the Si-DLC vertical structure along the bevel of the power diode at different x-positions. (a) p-/DLC interface in the space charge region (b) n-/DLC interface into the space charge region. (c) and (d): MIS structures corresponding to the band diagrams in the p- and n- region respectively. Data extracted at V = 4000V and T = 300K. A nitrogen doped DLC has been used.

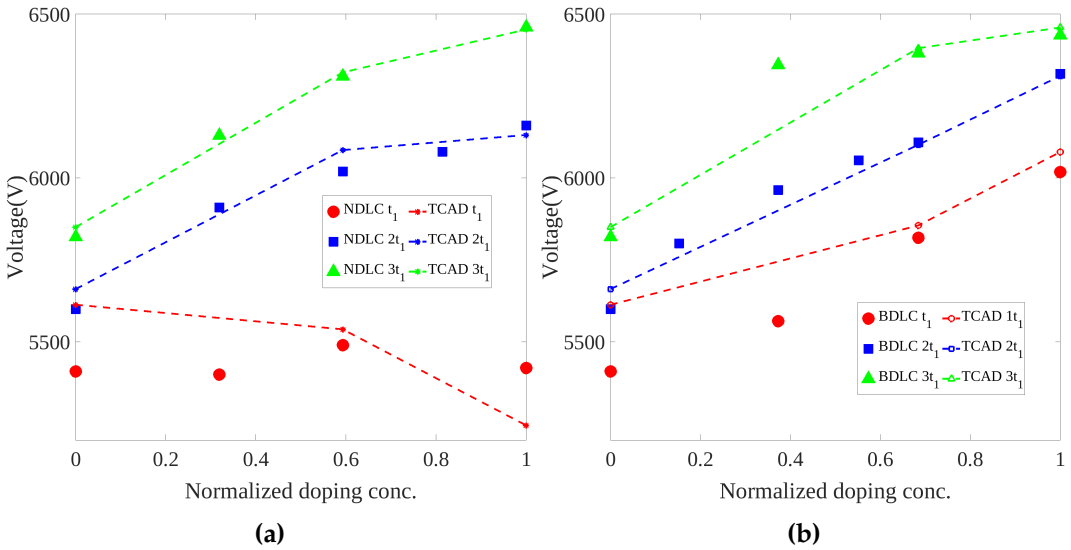


Figure 3.40: Simulated breakdown voltage versus nitrogen/boron atomic concentration for three different thicknesses of the DLC passivation layer compared with experiments. (a): NDLC, (b): BDLC (T = 300K).

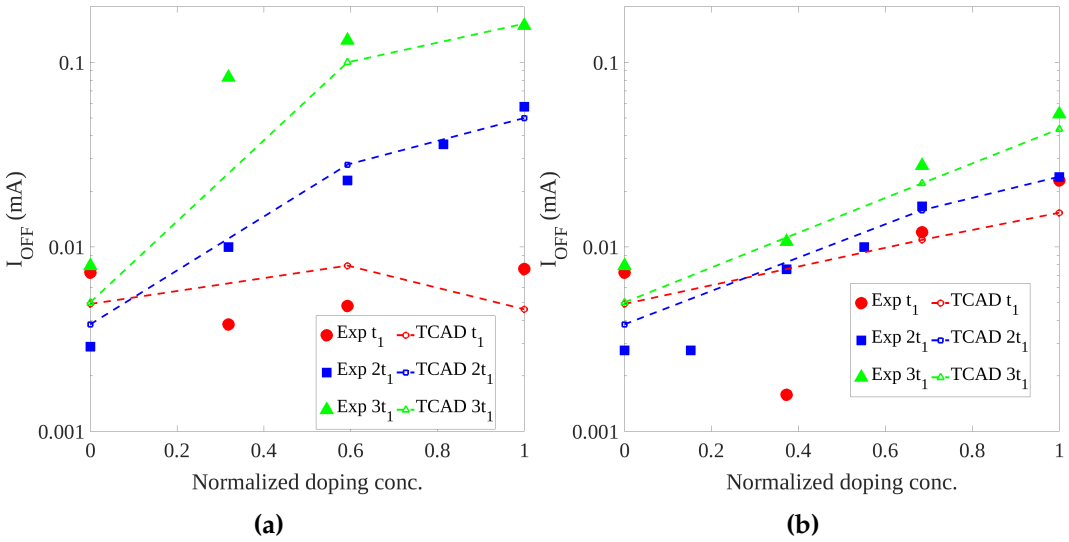


Figure 3.41: Simulated breakdown voltage versus nitrogen/boron atomic concentration for three different thicknesses of the DLC passivation layer compared with experiments. (a): NDLC, (b): BDLC (T = 300K).

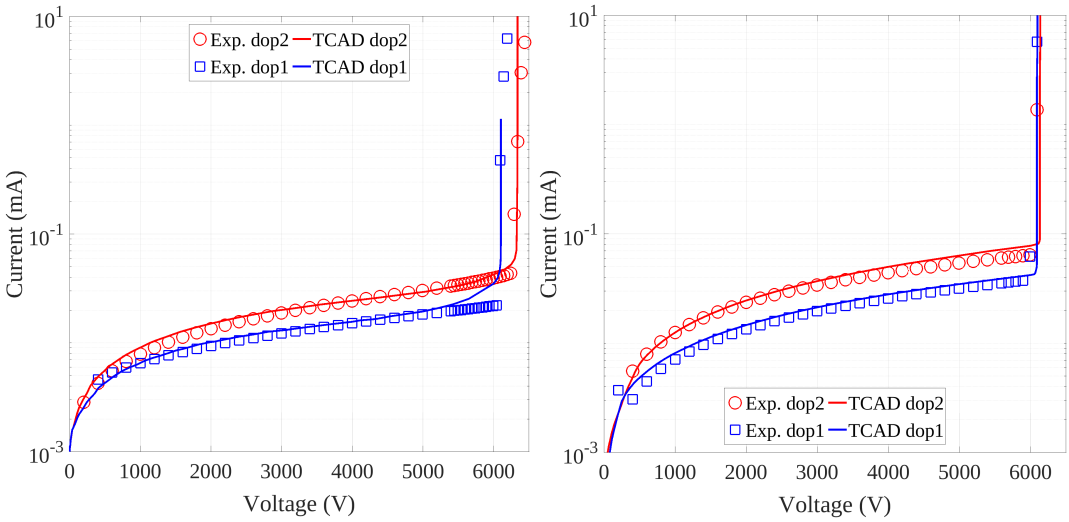


Figure 3.42: I-V curves of the power diode under reverse bias condition for different DLC passivation layer (T = 300K). (a) NDLC. (b) BDLC. DLC thickness = $2t_1$

Temperature effects on the leakage current Under reverse bias condition current density of an ideal pn junction is dominated by the recombination of charge carriers into the depletion region according with Eq. (1.30). Since

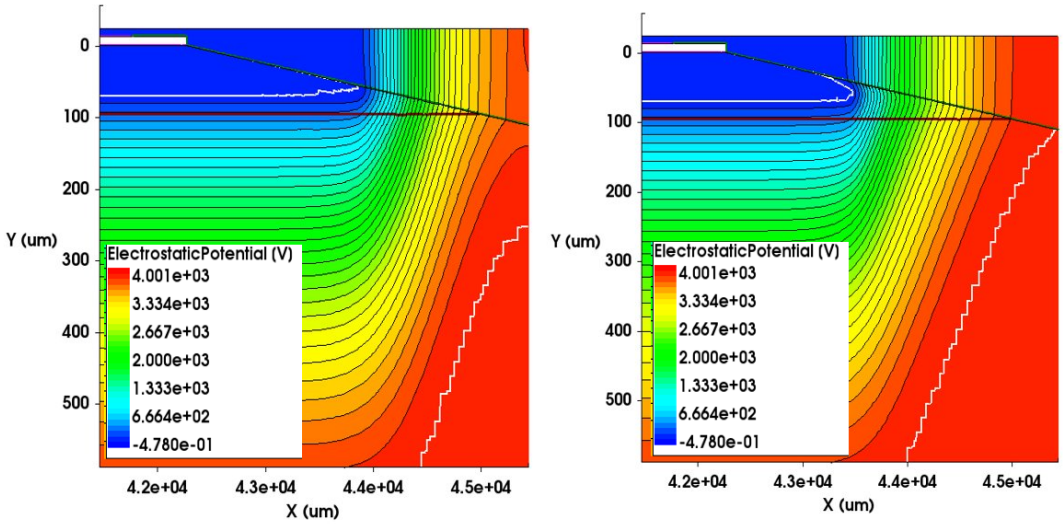


Figure 3.43: 2D potential contour plots of the diode JT extracted at V = 4000V under reverse bias condition. (left) BDLC, (right) NDLC. T = 300K

$n_i \propto \exp\left(-E_g/2k_BT\right)$ an Arrhenius-like temperature dependence of the intrinsic carrier density is expected. However, it is necessary to take into account also the additional contribution coming form the semi-insulating passivation layer on the junction termination. It has been demonstrated that for negative bevelled power diode the key element is the DLC intrinsic carrier density ($n_{i,DLC}(T)$). For this reason, it is necessary to analyse the behaviour of the Gauss-Fermi integrals at different temperatures. The normalized carrier concentration as function of temperature is reported in Fig. 3.44 for different value of the standard deviation. By using $\sigma = 0.1eV$ the temperature dependence of the carrier concentration is very weak giving the desired behaviour of the leakage current (Fig. 3.45).

Temperature effects on the breakdown Voltage Silicon power diodes usually show a strong increase of the breakdown voltage with temperature, which follows from the reduction of the impact ionization generation due to the decrease of the impact ionization coefficients [31] [32]. However, when DLC is

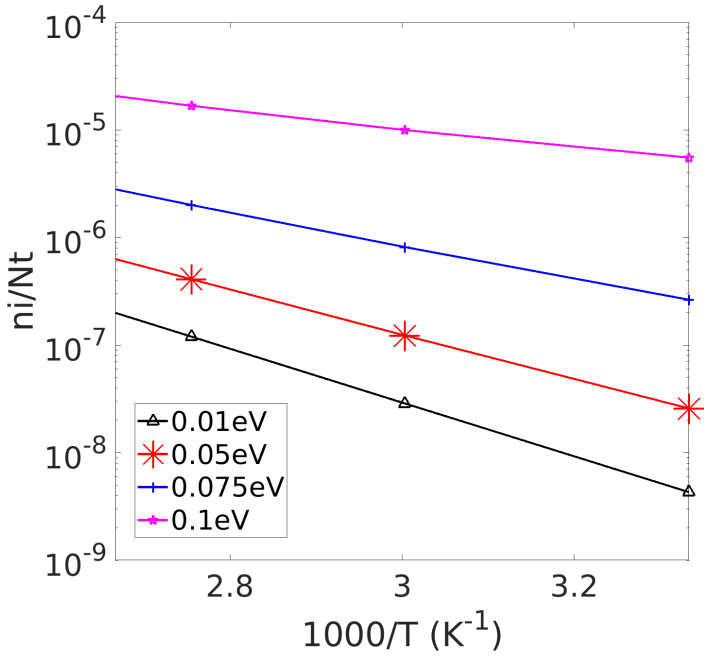


Figure 3.44: Carrier density as function of the ambient temperature for different value of the standard deviation σ

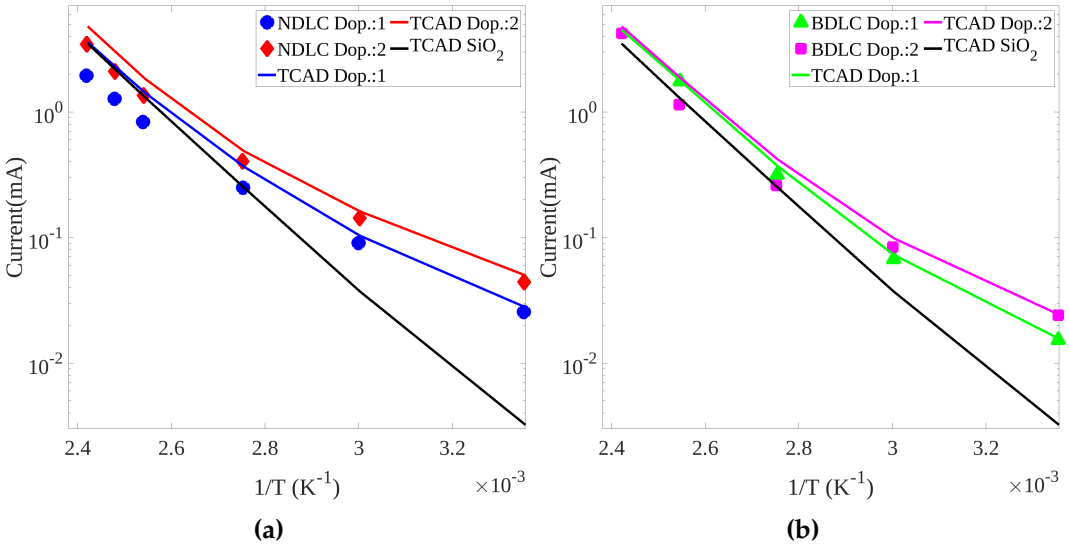


Figure 3.45: Leakage current extracted at 4000V as function of temperature for different DLC oping concentration. (a) NDLC. (b) BDLC. DLC thickness = $2t_1$

used as semi-insulating passivation material the BV exhibits a weaker temperature dependence when compared to the silicon bulk material. Two different approach have been proposed to explain the experimental data: (i)

accounting for the charge de-trapping at high temperatures by using a temperature dependent doping concentration (ii) assume that different Poole-Frenkel activation energies must be used into the DLC layer depending on the distance from the Si/DLC interface.

The former is based on the assumption that the charge transport is dominated by the Poole-Frenkel hopping between traps. As observed in many different materials, as reported in [33][34], at higher temperatures trapped charges acquire enough energy to overcome the barrier between the trap level and the conduction or valence band: as a consequence, the amount of fixed charge available to modify the depletion region width along the bevel is drastically reduced. This can lead to a limited increase of the BV with temperature. In Fig. 3.46 the measured BV as function of the ambient temperature is compared with TCAD simulations. The undoped DLC behaves as a lightly doped p-type semiconductor [35] [8] and provides a small amount of negative trapped charge which results in a slight increase of the BV at low temperatures when compared with simulations with ideal SiO_2. At higher temperatures, for doped DLCs, the predictions of the improved TCAD model show an overestimation of BV. The low BV temperature dependence observed in the experiments can be explained assuming that above 300K traps tend to empty [36]. In order to reproduce this feature through TCAD simulations, it has been assumed that the doping concentration is a decreasing function of temperature following an exponential curve as shown in Fig. 3.47. In Fig. 3.48, the electrostatic potential distribution close to the junction termination is compared for passivation layer with constant and variable doping concentration. The width of the depletion region along the bevel is lowered due to the reduced doping concentration.

The latter can be also obtained by removing the constraint that the top layer (DLC2) has a 100 times larger carrier mobility when compared with the DLC layer close to Silicon (DLC1). Assuming different activation energies for

DLC1 and DLC2 the temperature dependence of the BV voltage can be modified as shown in Fig. 3.49. This can be ascribed to the different current density distribution inside the DLC along the bevel. When the ratio between the two mobilities is high the charge carriers mainly flow in the top region of the DLC leaving the underlying layer largely depleted. The excess of positive/negative space charge close to the Si/DLC interface acts on the width of the space charge region along the bevel as discussed before. However, when the mobility of the DLC1 approaches that of the DLC2, the current density is uniformly distributed giving rise to a lower amount of space charge which result in a lower breakdown voltage of the power diode.

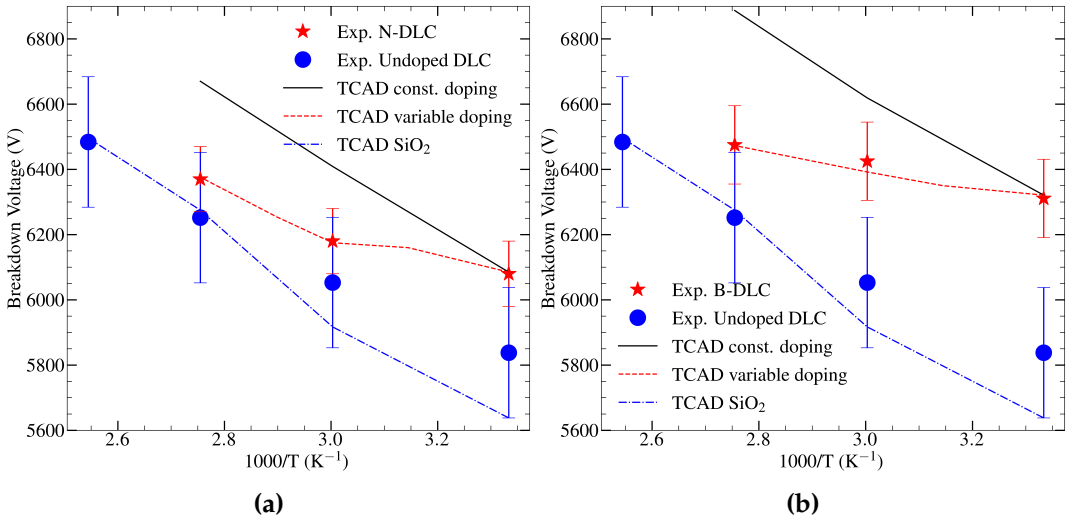


Figure 3.46: Breakdown voltage of negative bevelled power diode with NDLC (a) and BDLC (b) as passivation. Error bars refer to room temperature measurements. Symbols: experiments. Lines: TCAD simulations.

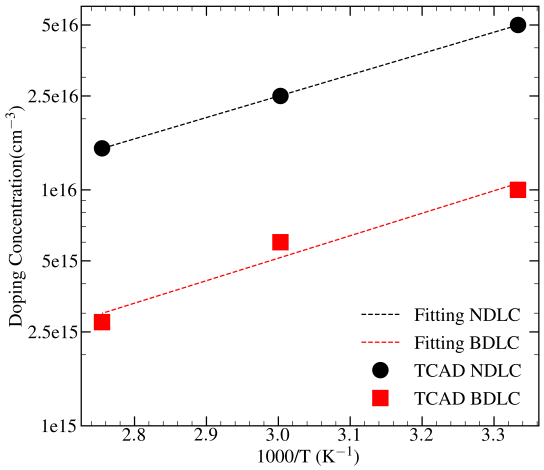
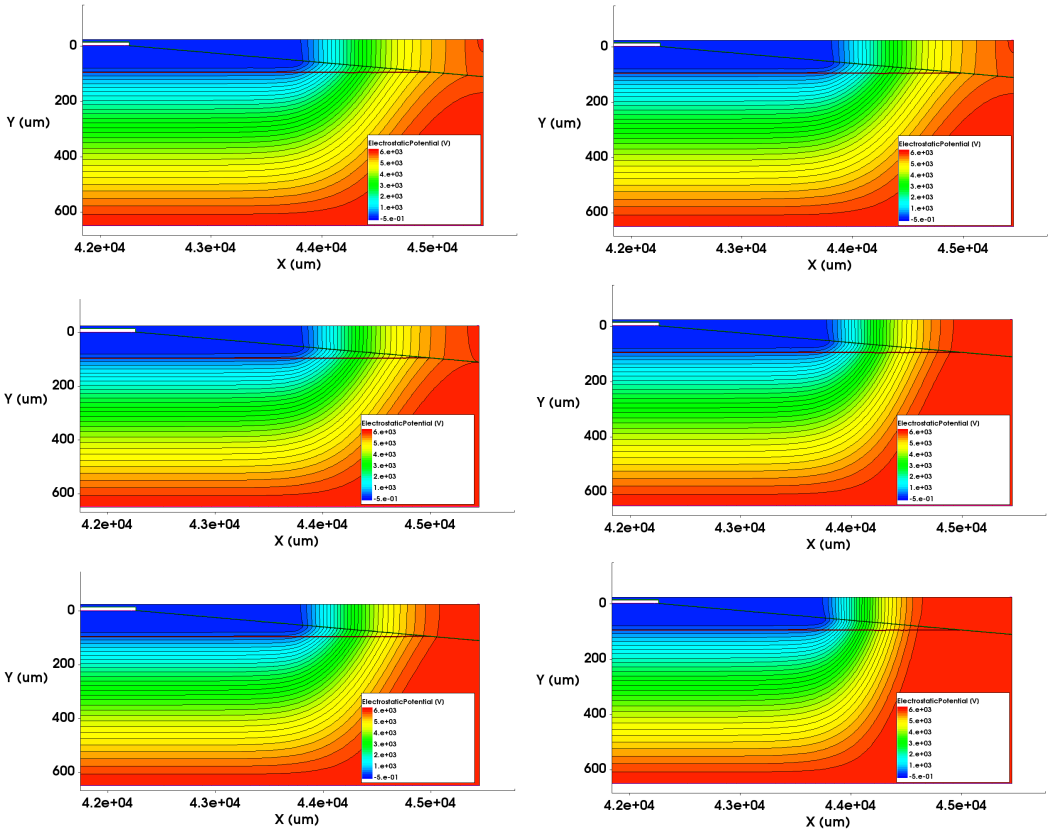


Figure 3.47: Effective DLC Doping concentration as function of temperature. Symbols: values of the doping concentration that provide the desired breakdown voltage. Dashed lines: fitting with an exponential function.



(a) **(b)**

Figure 3.48: 2D Contour plot of the electrostatic potential of the diode with BDLC for three different temperatures using a constant (a) of variable (b) doping concentration. Top: 300K, Middle: 333K, Bottom: 363K

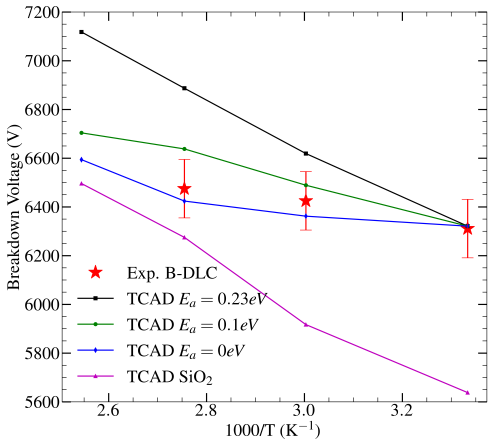


Figure 3.49: Breakdown voltage of negative bevelled power diode with BDLC as passivation. TCAD simulations refer to different value of the barrier height E_a in the DLC2 layer. The DLC1 has $E_a = 0.23eV$ in all simulations. Error bars refer to room temperature measurements. Symbols: experiments. Lines: TCAD simulations

Summary

The modelling of thin DLC layers has been carefully addressed in this chapter. The microscopic description of the charge transport by means of spatial and energetic trap to trap hopping, although possible, is not suitable for simulations of large-area negative bevelled power diode due to the high computational cost. For this reason, it has been assumed that charge transport in the DLC occurs only in the conduction and in the valence band which can be modelled with either parabolic or Gaussian density of states. In addition, simulations performed with a simple semiconductor as passivation layers, have shown that the effects of a DLC coating on the blocking capability of the power diode can be qualitatively described by assuming the presence of active doping and a resistive layer close to the Si/DLC interface. The leakage current and its temperature dependence are instead dominated by the intrinsic carrier density of the passivation layer. However, to obtain a more accurate description of the DLC properties it is necessary to account for all the phenomena observed in the experimental characterization of MIM and MIS structures. The forward bias JV curves show a field-dependent conductivity

which has been modelled by using the Poole-Frenkel mobility. The low-field mobility μ_0 and the fitting parameter β, have been fitted against the forward bias characteristics in the Ohmic and high-injection regimes, respectively. In addition, it has been shown that the PF activation energy E_a is fundamental to reproduce the experimental temperature dependence of the MIS structure current density under forward bias. The CV curves are characterized by a strong peak of the capacitance which has been reproduced through the ferroelectric model and assuming a single time-constant equation to describe the frequency dependence of the polarization vector. The dielectric constant of the material ε_r has been fitted against the high-frequency CV curves while the time-constant τ and the residual polarization P_r has been tuned to give the correct capacitance peak in the whole frequency range. The saturation polarization P_s and the coercive field F_c have been chosen in order avoid saturation and hysteresis. However, metal/DLC interfaces exhibit a very low Schottky barrier for both electrons and holes independently from the metal workfunction. Moreover, the absence of a significant threshold voltage in MIS structures made by DLC layer and Silicon substrate with opposite doping type has been found. All these features, can not be explained by using parabolic density of states or asymmetric sharp G-DOS. Indeed, symmetric Gaussian density of states with a large standard deviation ($\sigma \approx 0.1$) are needed. With their tail, they emulate the presence of an high number of defects close to the mid-gap which pin the Fermi level. By doing so, also the desired low temperature dependence of the intrinsic carrier density is obtained resulting in a nice prediction of the diode off-state losses up to 413K. The energy gap between the two Gaussian functions has been fixed according to experiments while the number of hopping states N_t has been chosen to give the desired current density of the MIS structure under reverse-bias condition. The SRH generation has been accounted for with $\tau_e = \tau_h = 10^{-10}s$. However, the specific value of the carriers lifetime is not relevant as shown

in Fig. 3.30. A doping concentration into the DLC has been added to reproduce the asymmetry in the reverse-bias JV curves observed comparing MIS structures with different doping types in the silicon substrate but with the same DLC on top. The fixed charge provided by the addition of dopants leads to a larger width of the depletion region along the bevel termination of the power diode thus increasing the breakdown voltage when compared to TCAD simulations with ideal SiO_2 as passivation. The difference between the vertical and the lateral conductivity is accounted for by splitting the DLC layer in two parts: DLC1 placed at the Si/DLC interface playing the role of the blocking layer observed from TEM images and DLC2 on top of DLC1 which represent the bulk material. This has been proved to be fundamental to reproduce the increase of the BV in the negative bevel power diode with the DLC thickness. Finally, two qualitative interpretations of the low temperature dependence of the breakdown voltage have been provided: (i) a charge de-trapping at high temperature, (ii) DLC1 and DLC2 have different temperature dependence of the conductivity. The former has been emulated assuming a temperature-dependent doping concentration of the DLC. The latter has been implemented by using different activation energy E_a in the PF mobility model for DLC1 and DLC2.

It has thus been demonstrated that the proposed model can predict the performance of negative bevelled power diode comparing TCAD simulations against the experiments.

Chapter 4

Diode featuring planar termination with variation of the lateral doping (VLD)

The negative bevel termination is actually widely used in discrete power devices such as diodes and thyristors since it is able to reduce the electric field at the edges of the device with high reproducibility and limited costs. However, it requires long drive-in to obtain a large junction-depth and a significant area consumption. In addition, experiments and simulations, show a reduced breakdown voltage due to the lowering of the depletion region width along the bevel. Even if an optimized DLC passivation is adopted, it is not possible to achieve the same blocking capability of the one-dimensional pn junction. For this reason, a planar junction termination (JT) with laterally variable doping concentration (VLD) is proposed in this chapter. This concept is not new and it has been discussed in different papers [37][38]. However, TCAD simulations accounting for the passivation layer and its charge transport properties have never been addressed since it is usually modelled as an ideal insulator with fixed charge. In this chapter, a very simple design approach is proposed in order to replace the bevel termination with the VLD while retaining limited additional costs. The DLC model developed

in Chapt. 3 is applied to the new JT and a comparison with the previously simulated bevelled diode is carried out.

4.0.1 Junction termination design rules

The bevel termination is replaced by a planar JT doping profile following the VLD technique [38] as depicted in Fig. 4.1. More specifically, a Gaussian function along the y-axis is defined with a peak concentration linearly decreasing along the termination region. From an analytical point of view, it reads [39]:

$$N(x,y) = g(y)h(x)\,, \tag{4.1a}$$

$$g(y) = N_{\text{peak}} e^{-\frac{(y-y_0)^2}{2\sigma^2}}\,, \tag{4.1b}$$

$$h(x) = \left(\frac{N_{\text{drift}}}{N_{\text{peak}}} - b\right)\frac{x}{L_{\text{VLD}}} + b\,, \tag{4.1c}$$

with N_{peak}, σ and y_0 the peak concentration, standard deviation and peak position of the Gaussian function, N_{drift} the doping concentration in the drift region (labelled as n^- in Fig. 4.1), L_{VLD} the total length of the VLD profile and b a fitting coefficient of the linear variation along the x-axis. As a specific case study, $y_0 = 0$ and $b = 1$ have been fixed without loosing any relevant dependence in the following analysis. The dose Q corresponding to the vertical profile is determined by

$$Q = \int_0^\infty g(y)dy\,. \tag{4.2}$$

Different lateral function $h(x)$ can be tested. However, this will lead to more complex mask design without significant improvement of the of the blocking capability.

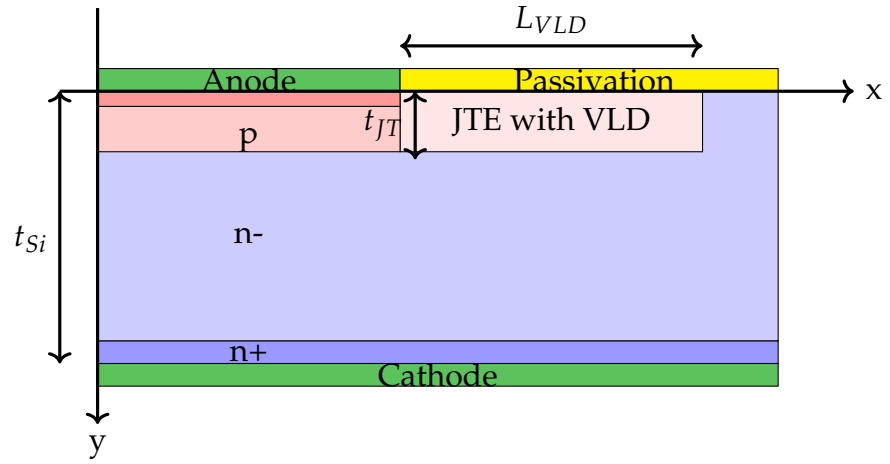


Figure 4.1: Schematic representation of a power diode with a VLD junction termination.

4.0.2 TCAD Simulations

In order to optimize the VLD profile for the diode under study, an ideal SiO_2 has been used as passivation layer on top of a planar termination with total length L_T equal to the bevelled diode investigated before. The maximum dose of the Gaussian profile providing the best performance in terms of V_{BD} has been obtained by changing N_{peak} and σ so to keep the depth of the pn junction unchanged. In Fig. 4.2, V_{BD} is reported as a function of Q showing an optimal value for $Q = 3.2175 \times 10^{12}$ cm^{-2}. As expected, V_{BD} is equal to 99% of the ideal one-dimensional simulation, outperforming the bevelled-diode case reaching only 80%.

The passivation material has been then replaced by boron- and nitrogen-doped DLC in order to check the role of doping, transport and polarization of the passivation layer on the device performance. Differently from the bevel termination, V_{BD} and I_{OFF} are almost independent of the doping type in the DLC layer as shown in Fig. 4.3. In addition, since the depletion width in silicon is mostly controlled by the VLD-JT profile, the effect of additional charge on the top layer is very limited as confirmed by the I_{OFF} levels compared with the bevelled diode cases reported in Fig. 4.3a. A small degradation of the diode performance in terms of V_{BD} is observed for L_{VLD} reduced to half

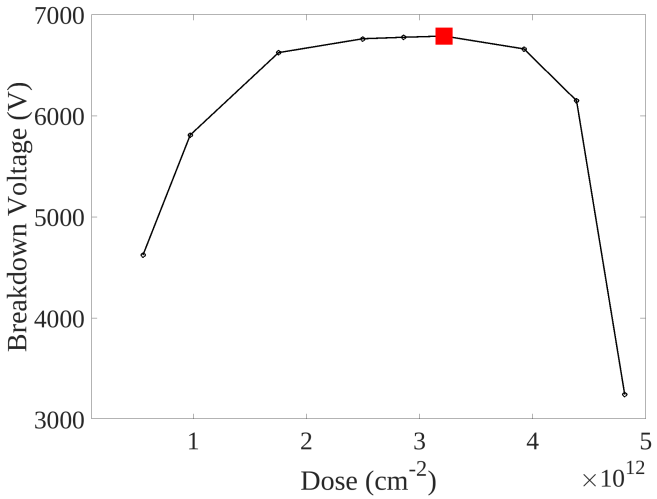


Figure 4.2: Breakdown voltage of the power diode with VLD-JT as function of the JT dose. The red square represents the optimal value for the dose Q. Passivation material: SiO_2.

of the original L_T (Fig. 4.3b). The largest degradation effect is observed for the nitrogen-doped DLC and can be ascribed mostly to the highest dielectric polarization: the presence of electric dipoles at the Si/DLC interface affects the electric field distribution not only along the interface but also in the bulk silicon. Simulations clearly show that if a nitrogen-doped DLC is used, the polarization vector at the Si/DLC interface is large and positive near the cathode and changes to negative values by moving towards the edge of the termination (Fig. 4.4), leading to additional positive charge near the cathode and to a consequent reduction of the interface electric field. However, it should be noted that in an optimized VLD-JT, the onset of avalanche is not correlated to the Si/DLC interface but to the electric field peak located deeper into the bulk region where, vice-versa, the electric field is increased by the additional positive charge on top. In other words, polarization in a nitrogen-doped passivation layer provides a significant reduction of the leakage current and breakdown voltage as shown in Fig. 4.5. Similar considerations can be applied to the boron-doped DLC passivation, but the polarization vector in this case causes a negligible variation to the vertical electric field, which is very close to the ideal condition, and no V_{BD} degradation is observed (Fig.

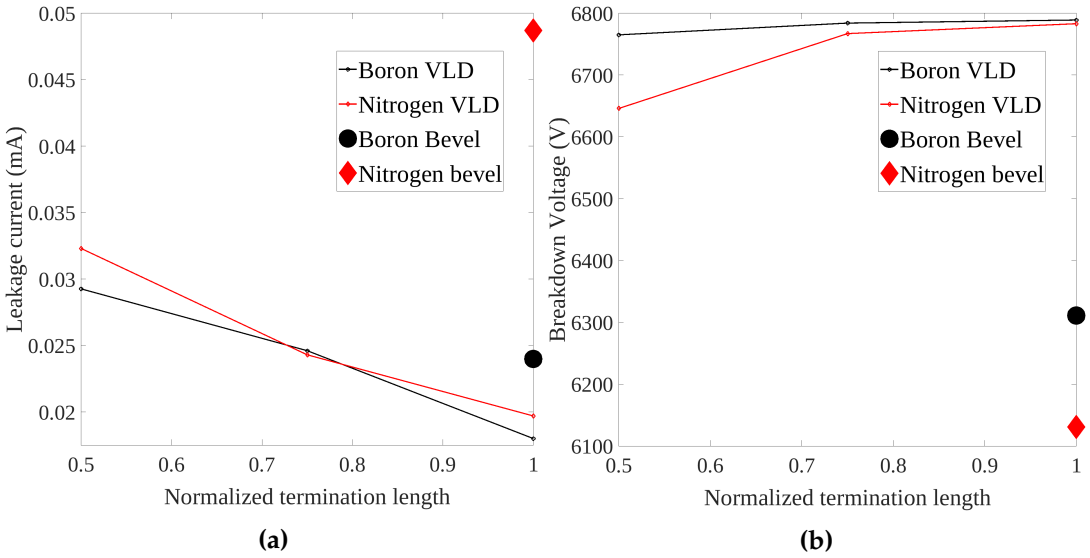


Figure 4.3: (a) Leakage current and (b) breakdown voltage of the power diode with VLD-JT as a function of the normalized length L_{VLD}/L_T compared with the results previously obtained with a bevelled termination of length L_T. Two differently doped passivation layers are considered.

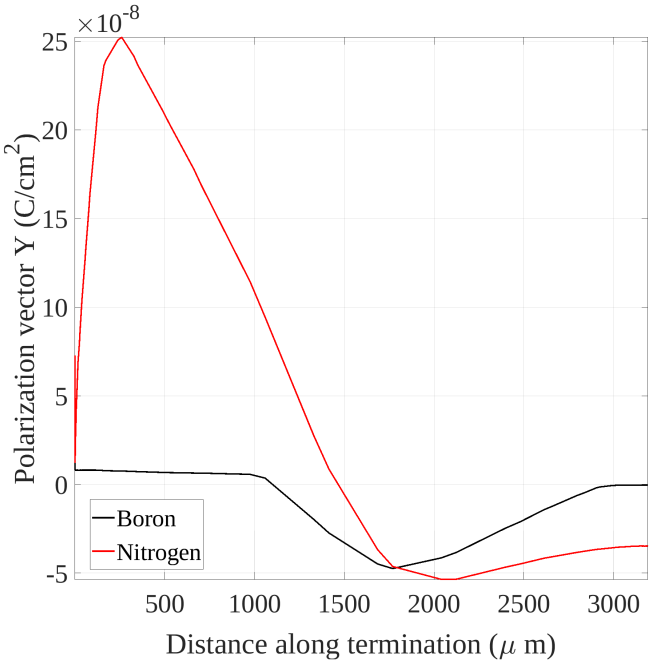


Figure 4.4: Normal (y-axis) component of the polarization vector along the VL-JT.

4.5b). On the other hand, the effects of the DLC polarization on I_{OFF} are quite independent of the DLC doping type (Fig. 4.5a) because in both cases the polarization at the Si/DLC interface provide an increase of the depletion region width. This means that carriers flow through a longer resistive path reducing

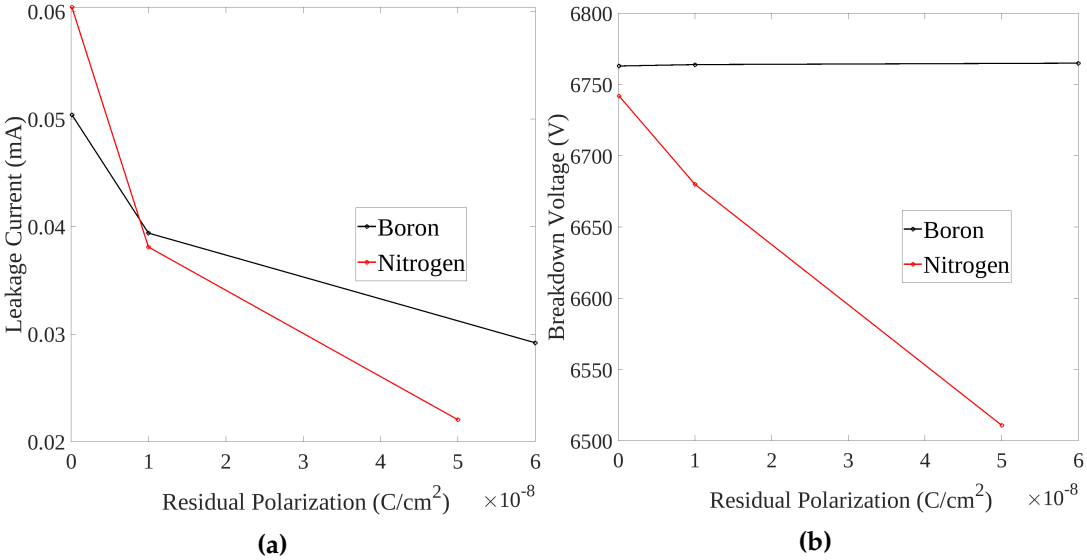


Figure 4.5: (a) Leakage current and (b) breakdown voltage as a function of the residual polarization.

I_{OFF}. The latter results clearly show that the VLD-JT can drastically reduce L_{VLD}, increasing the ON-state performance per area.

Reduction of the junction depth

The use of a negative bevel requires to place the pn-junction deeper in silicon. This implies that an overall thicker structure is required for the discrete power devices with a practical trade-off as explained in [40]. The VLD-JT comes out to be an interesting approach to decouple the vertical thickness from the termination structure, giving the possibility to design a thinner pn-junction under the termination and consequently the total thickness of the structure, namely, t_{JT} and t_{Si} as defined in Fig. 4.1. Since V_{BD} is affected mainly by Q and L_{VLD}, optimized as illustrated above, it is possible to reduce t_{JT} to its minimum value by keeping them unchanged without compromising the blocking capability. This is confirmed by the V_{BD} analysis reported in Fig. 4.6, showing the limited variation with a significant reduction of t_{JT} for different t_{Si}. As expected, no significant dependence of V_{BD} on t_{JT} is found because V_{BD} is dominated entirely by the active region of the device, while

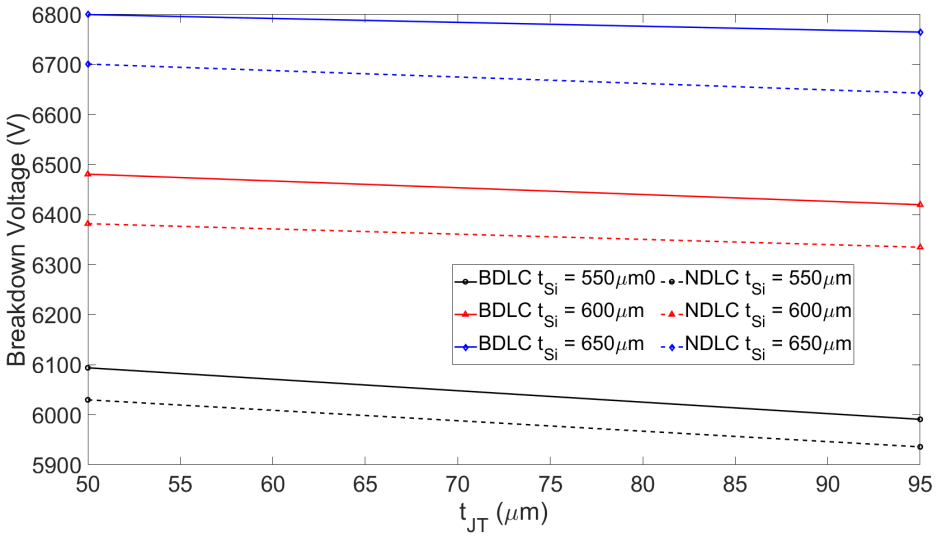


Figure 4.6: Breakdown voltage as function of the junction depth (t_{JT}) for different values of t_{Si}.

it decreases at lower t_{Si} as the full volume of the device is affected by this variation. When the nitrogen-doped DLC is used, a slight reduction of the BV is observed, which can be ascribed to the positive fixed charge effect on the termination junction.

A good final compromise between the on-state losses and dimensions is obtained by reducing the silicon thickness and the termination length by 7.7% and 50% with respect to the reference bevelled structure as shown in Fig. 4.7. A small reduction of the V_{BD} is experienced, but a value still larger than the reference case is found, while a very similar I_{OFF} is obtained. In addition, the smaller wafer thickness results in a lower resistance of the drift region with a consequent reduction of the on-state voltage drop.

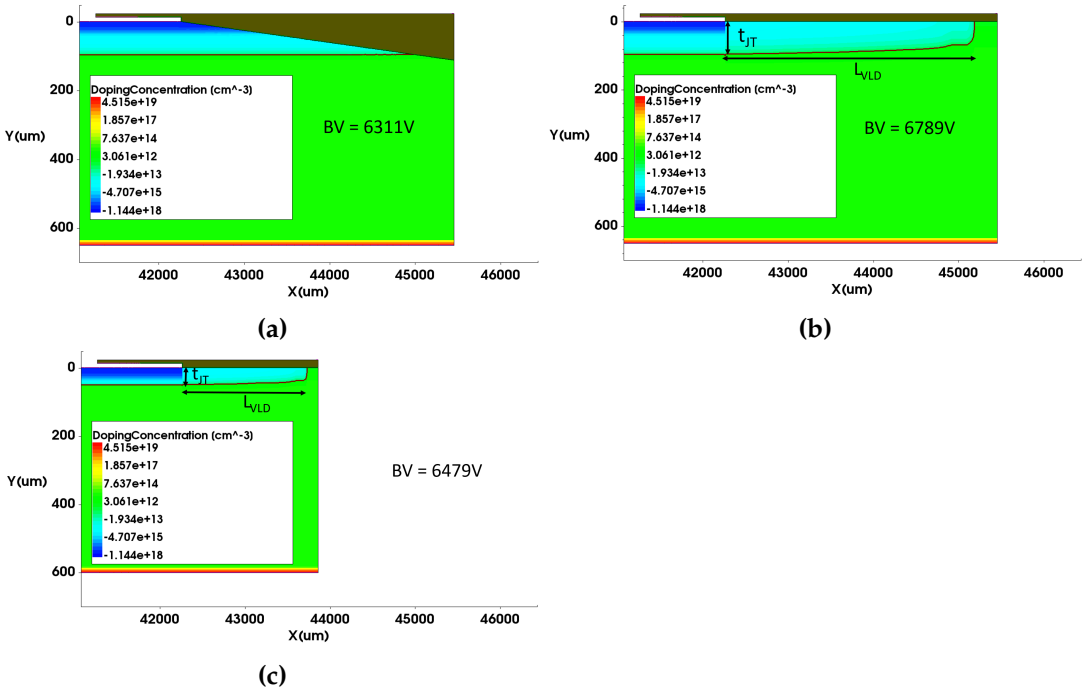


Figure 4.7: Doping profile and structure of the diode terminations under study. (a) reference bevelled geometry; (b) VLD-JT realized with the same area and t_{JT} as the reference diode; (c) VLD-JT with optimized vertical and lateral thicknesses. Structures are not in scale. The additional encapsulation material is drawn in dark colour on top.

Chapter 5

Current filamentation in silicon power diodes

It has been shown that by using a VLD termination, diodes with shallow p-n junction can be realized preserving, at the same time, the blocking capability. However, a low junction depth can reduce the device stability during the reverse recovery process i.e. the switching from the on-state to the blocking state. Under such conditions, the so-called dynamic avalanche condition occurs: the charge carriers extracted from the plasma cross the space charge region of a blocking junction and increase the effective positive/negative charge hereby enhancing the electric field peaks [41]. For this reason, the effective breakdown voltage (BV) during the reverse recovery transient can be significantly lower than the static BV, leading to current instabilities [42] [43] [44]. During the reverse recovery, diodes can exhibit a negative differential resistance which is correlated with the inhomogeneous current density distribution along the device [45] [46]. The consequent current filamentation may lead to the destruction of the device[47][48][49]. In the first section, the reverse recovery process and the concept of dynamical avalanche will be briefly summarized. In the second section, by performing reverse-recovery TCAD simulations the formation of current filaments will be illustrated. A method to suppress the numerical error and to clearly distinguish fluctuations due to the discretization of transport equation from those coming from

a non-homogeneity in the device is provided. Finally, the study of different phenomena that can lead to the production of current filaments is addressed and discussed.

5.1 Theoretical Background

In this section, the reverse recovery process is described following [7] and the concept of dynamical avalanche is introduced as key element for the formation of current filaments.

5.1.1 Reverse-Recovery

The switching process of a P-i-N diode from the on-state to the blocking state is defined as reverse recovery. Usually, power diodes are used into rectifiers connected to an inductive load. A simple example is shown in Fig. 5.1. Due to the presence of the inductor, the current flowing to the device then reduces at a constant ramp rate $\frac{di}{dt} = -a$ (Fig. 5.2). The reverse recovery process can

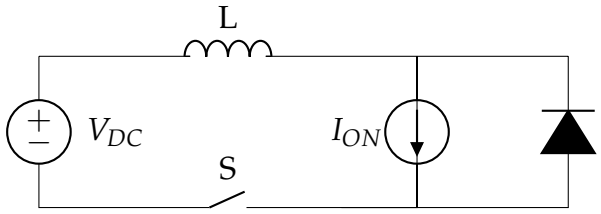


Figure 5.1: Example of reverse recovery circuit.

be divided into the following phases:

- For $t < 0$ the switch is open and the current I_{ON} flow through the diode with a voltage drop V_F across the device. When the high injection regime holds the minority carriers concentration exceeds the background doping concentration (N_D) into the drift region. The charge neutrality requires that:

$$n \approx p \tag{5.1}$$

The average electron density in the drift region is:

$$n_a = \frac{J_T \tau_{HL}}{qW_N} \tag{5.2}$$

Where J_T is the current density flowing into the diode under steady-state condition, τ_{HL} is the high-level lifetime and W_N the width of the drift region [7].

- At $t = 0$ the switch is closed and the dc voltage source is connected to the anode through an R-L load. Assuming $V_{DC} >> V_F$, the current starts to decrease linearly with a slope $a \approx V_{dc}/L$.
- At $t = t_0$ the current changes sign but the diode is still forward-biased since a large excess of current is present in the drift region.
- At $t = t_1$ the voltage drop across the diode suddenly decrease and the diode switch into its reverse-bias mode. A space-charge region appears at the $p^+ - n$ junction.
- At $t = t_2$, the voltage on the diode is $V = V_{dc}$ and the current reach its maximum value J_{PR}. However, a certain amount of charge Q is still stored in the drift region. It is removed between t_2 and t_3 with a rate: $I_{PR}^2/2Q$.
- At $t = t_3$, the excess of carriers from the n-region has been completely removed and the current flowing trough the diode is equal to the static leakage current.

5.1.2 Dynamical Avalanche

For $t > t_1$ the current density into the space charge region is mainly due to the holes extracted from the plasma layer toward the anode contact. If the concentration of holes becomes comparable or even higher than the ionized

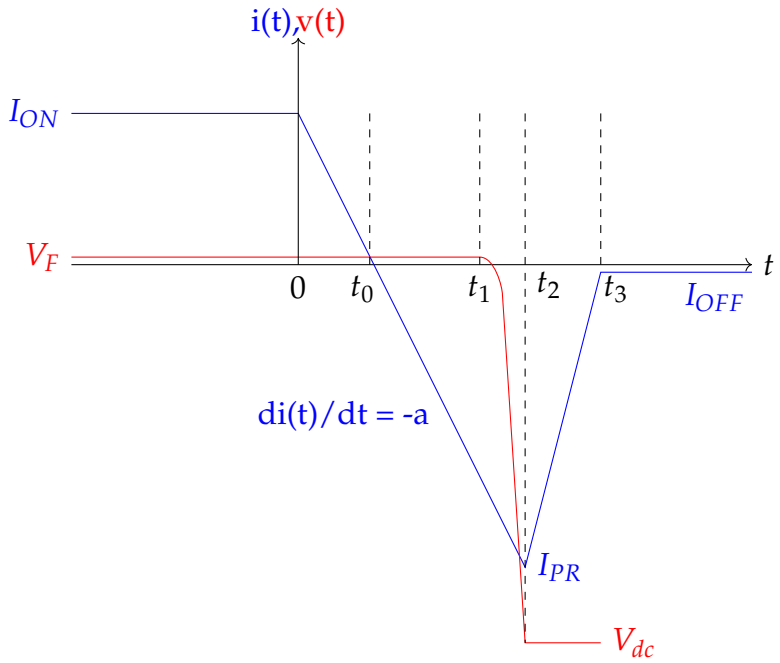


Figure 5.2: Anode current and voltage for a P-i-N diode during the reverse recovery process

donor concentration N_D the effective total space charge affects the electric field distribution into the depletion region. The one dimensional Poisson's equation 1.31 becomes:

$$\varepsilon_0 \varepsilon_S \frac{dE}{dx} = q(N_D + p - n) \approx q(N_D + \frac{J_P}{q v_{P,sat}}) \tag{5.3}$$

Where it is assumed that the diffusion term in the hole current density is negligible and the electric field is sufficiently high, so that holes move with their saturation velocity $v_{P,sat}$. The increase of positive space charge results in an enhanced electric field gradient and therefore in an increase of the electric field peak. For this reason, electron-hole pairs are generated by impact-ionization at reverse bias much below the static breakdown voltage investigated in the previous chapters. When the impact ionization rate is very high, also the electron concentration (n) becomes larger than N_D resulting in an electric field configuration which may significantly deviates from the usual triangular shape. This can lead to negative differential resistance and, as a

consequence, to current filamentation.

5.2 Current Filament

5.2.1 TCAD setup

In order to illustrate the formation of current filament TCAD simulations have been performed on a Fast Recovery Diode (FRD) with a wafer thickness of 660 μm. The effective device area is in the order of 10^8 μm2 regardless of the lateral width L_x of the structure. Device simulations have been performed by the drift-diffusion transport equations in two dimensional (2D) structure under transient condition. The SRH recombination has been accounted for with lifetimes equal to $\tau_e = \tau_h = 1$ms. Avalanche generation (UniBo impact ionization model), Auger recombination, mobility doping dependence and carrier-carrier scattering have been accounted for with default parameters. Default values of the surface recombination velocities have been used at the aluminum/silicon interfaces. Iso-thermal conditions have been assumed with a fixed ambient temperature of T = 413K. A schematic view of the device is shown in Fig. 5.3a. The circuit used to simulate the reverse recovery transient is reported in Fig. 5.3b along with the corresponding component values taken from a real power converter.

5.2.2 Quasi-1D Simulations

In Fig. 5.4, the voltage and current waveforms for a diode with a lateral dimension $L_x = 5\mu m$ are reported. In Fig. 5.5a electron and hole densities are compared with the background net doping concentration. Two space charge regions appear: one at the anode side and one at the cathode side. Close to the p-n junction, the electric field is dominated by the excess of positive

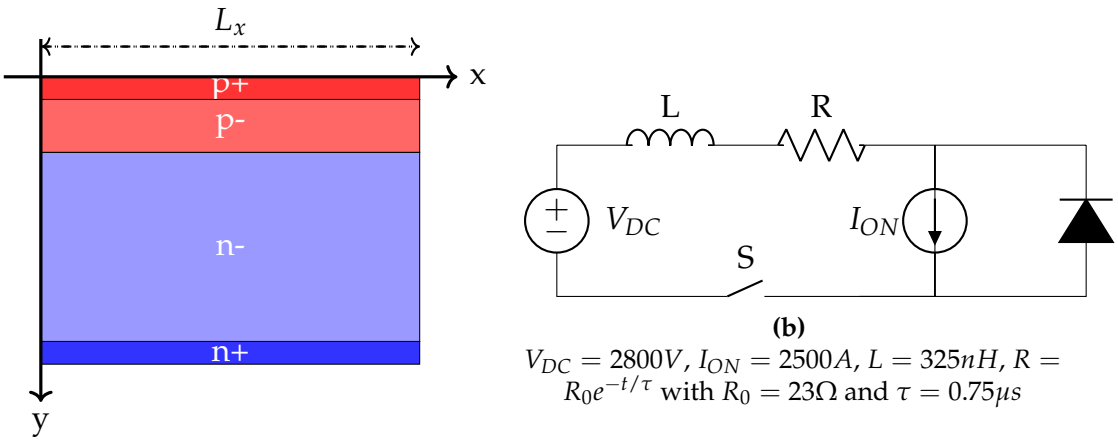


Figure 5.3: (a) Schematic representation of the power diode. (b) Reverse recovery circuit used for mixed-mode simulations

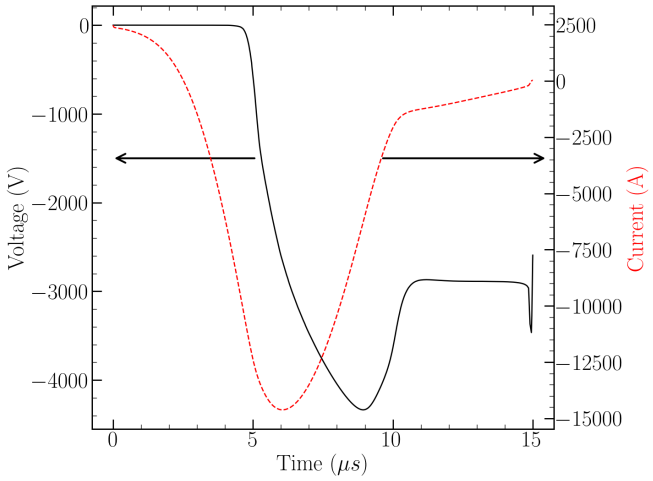
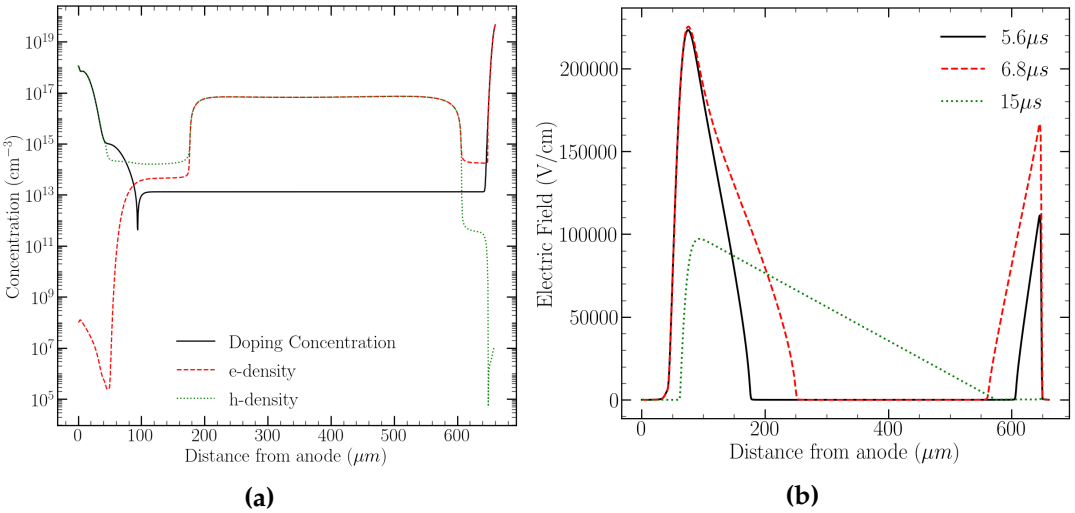


Figure 5.4: Current and voltage waveform of the power diode under reverse recovery condition

charge as previously described in Eq. (5.3). On the contrary, the n-/n+ junction electric field peak is dominated by the high electron density. In Fig. 5.5b the electric field distribution inside the device is reported for two different instant of times. For t = 5.6μs, it has the usual triangular shape. However, at t = 6.8μs the electric field distribution at the anode side is altered by electrons generated via impact ionization close to the pn junction. This deformation, leads to teh negative differential resistance. However, due to the limited lateral dimension of the device current fluctuations are negligible and filaments do not appear.



(a) **(b)**

Figure 5.5: (a) electrons and holes densities compared with the background doping concentration extracted at $t = 5.6\mu s$ (b) Electric field distribution inside the device for three different instant of time.

5.2.3 2D Simulations

The diode shown before has been simulated by setting $L_x = 1000\mu m$. The waveforms reported in Fig. 5.6a show significant voltage drops which can be ascribed to the formation of current filaments. At $t = 6.6\mu s$, the current density distribution along the lateral dimension (x) is still uniform (Fig. 5.7) and the simulation provides the same outcome of the quasi 1D structure shown before. However, a voltage drop is present at $t = 6.9\mu s$ and the current density along the device is no more uniform (Fig. 5.7). This is correlated with the formation of a current filament both at the anode and at the cathode sides of the diode as shown in Fig. 5.8a where the 2D contour plot of the current density is reported at $t = 7.0\mu s$. A qualitative illustration of the development of an anode-side filament is given in Fig. 5.9: (a) the dynamic avalanche is negligible and the current density distribution, dominated by holes, is uniform. In Fig. 5.9 (b), the dynamic avalanche occurs and electron-hole pairs are generated close to the p-n junction where the electric field is higher. A small local increase of the electric field due to some inhomogeneities results in a local increase of the dynamic avalanche (Fig. 5.9 (c)). Electrons move toward

the plasma region and locally reduce the space charge in the depletion region attracting more holes from the plasma. The inhomogeneity develops until a current filament appears (Fig. 5.9(d)). Similar considerations can be applied to cathode side filaments at the $n^- - n^+$ junction. However, the anode-side filament does not stay in its original position. Indeed, the filament moves towards the left side of the diode and reaches the edge of the device at $t = 7.0\mu s$ (Figs. 5.7 and 5.8b). At $t \approx 7.5\mu s$ another small voltage drop occurs (Fig. 5.6b) which corresponds to the formation of a new anode-side filament at the right edge of the structure (Figs. 5.7 and 5.8c). The filament starts to move toward the left border of the diode (Figs. 5.7 and 5.8d). On the contrary, the position of the cathode-side filament is almost constant in time. In addition, the latter filament has a much smaller width when compared with the anode counterpart, which results into a higher current density. For these reasons, in real devices, anode filaments produce a limited local heating and do not lead to the device failure. On the other hand, cathode filaments produce a strong local heating and can have disruptive consequences for the diode.

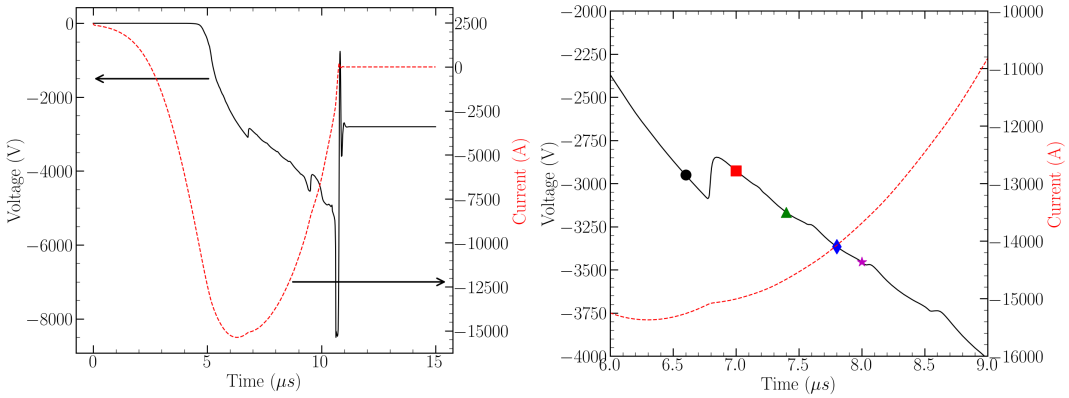


Figure 5.6: (a) Current and voltage waveform of the power diode under reverse recovery condition (b) detailed view of the current and voltage waveform between $6\mu s$ and $9\mu s$. Markers correspond to $t = 6.6\mu s$, $t = 7.0\mu s$, $t = 7.4\mu s$, $t = 7.8\mu s$ and $t = 8\mu s$

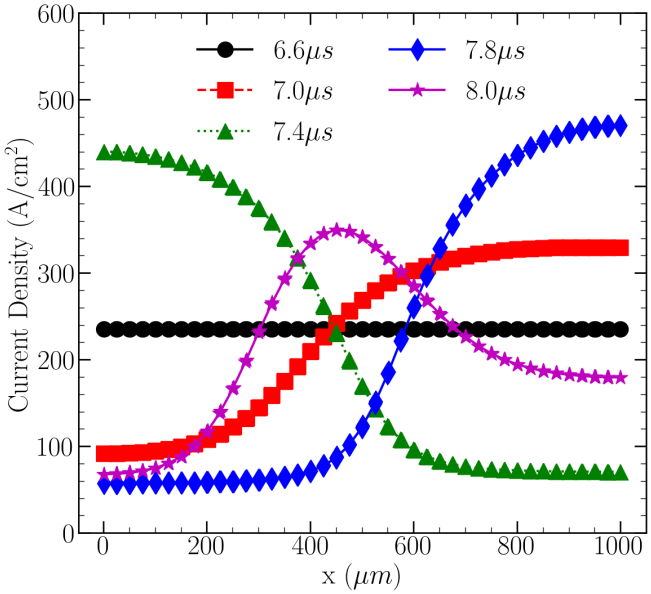


Figure 5.7: Current density distribution along the x-direction extracted at the pn junction $y = 95\mu m$ for different instant of time.

5.3 Reduction of the Numerical Error

It has been shown that current filaments can be generated in perfectly uniform structures. From a theoretical point of view, quasi-1D and 2D simulations should give exactly the same results since $\partial/\partial y = 0$ for each physical quantity. However, due to the discretization of the drift-diffusion equations, the lateral component of the electric field and consequently of the current density can be significantly different from zero. In this section, a meshing criterium which is able to minimize the numerical error is provided which can be used as indicator and the device stability. [51].

5.3.1 Mesh-Strategy

First of all, uniform rectangular grid geometry was chosen because, differently from the triangular mesh used above, it reproduces the homogeneity of the current distribution as shown in [52]. The grid used to simulate the diode was defined as follows. A uniform spacing along the x-axis (dx) is fixed with $dx = 25\mu m$. Differently, in the vertical direction, the p-n junction needs to be

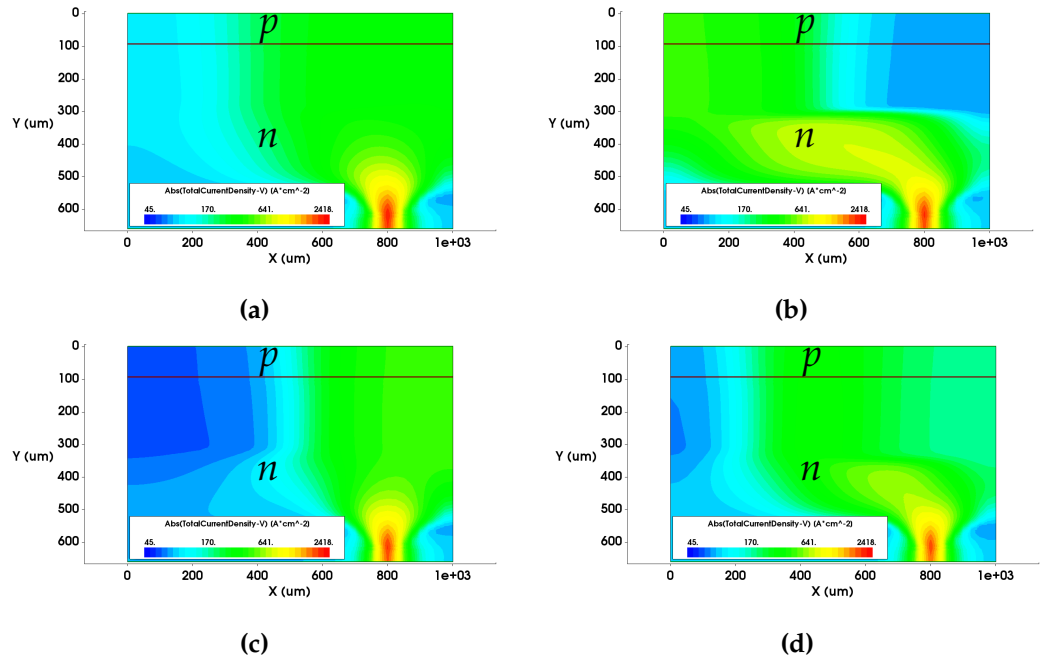


Figure 5.8: 2D contour plot of the current density extracted at (a) $t = 7.0\mu s$, (b) $t = 7.4\mu s$, (c) $t = 7.8\mu s$ and (d) $t = 8\mu s$. The anode (top side) is negatively biased with respect to the cathode and a reverse current is flowing. The horizontal black lines indicate the location of the pn junction.

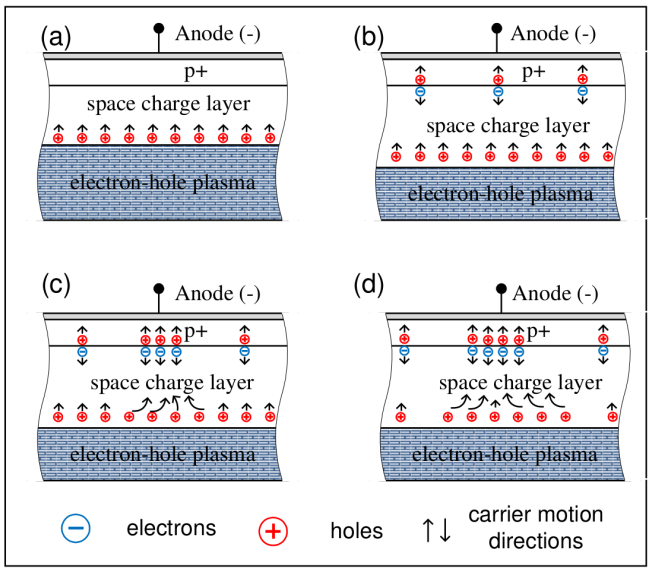


Figure 5.9: Schematic diagram showing the development of a filament. The figures show a portion of a large area diode during reverse recovery phase for different instant of time. The anode (top side) is negatively biased with respect to the cathode (not shown) and a reverse current is flowing. Space charge layer has been developed. [50]

correctly defined by adapting a fine grid spacing close to the p-n junction and near the electrodes. To this purpose the spacing along the y-axis (dy) is fixed to 1 μm in the latter regions for all simulations. Different dy have been tested in the drift region. In Fig. 5.10, the simulated voltage and current curves for the FRD in reverse recovery conditions are reported for different vertical grid space. The V(t) curves of structures with larger dy ($10\mu m$ and $25\mu m$) show significant voltage overshoots, which correspond to the presence a of moving anode filaments and a static cathode-side filament in the middle of the device as shown in Fig. 5.11. In the case of shorter dy, smooth and regular curves were observed for both $dy = 5\mu m$ and $dy = 2.5\mu m$. However, by monitoring the maximum current contribution to current density in the x-direction during reverse recovery, which should be ideally zero due to the uniformity of the p-n junction, a significantly higher contribution was found for $dy > 2.5\mu m$ as shown in Fig. 5.12(a). This led to the choice of the dy in the drift region, as the one which gives a numerical error on the current fluctuations comparable to the case of a uniform grid as shown in Fig. 5.12(b). In conclusion, the most suitable setup for the reverse recovery simulations of power diodes consists of a uniform rectangular grid with spacing along the y-axis small enough to suppress as much as possible the x-component of the current density.

5.4 Factors enhancing the probability of producing current filaments

With the setup described above, different factors that can cause a pattern formation on filaments can be investigated. Firstly, the consequences of a shallower pn junction, typical of VLD terminations, have been studied. In addition, very large lateral widths have been considered, as it is very useful to

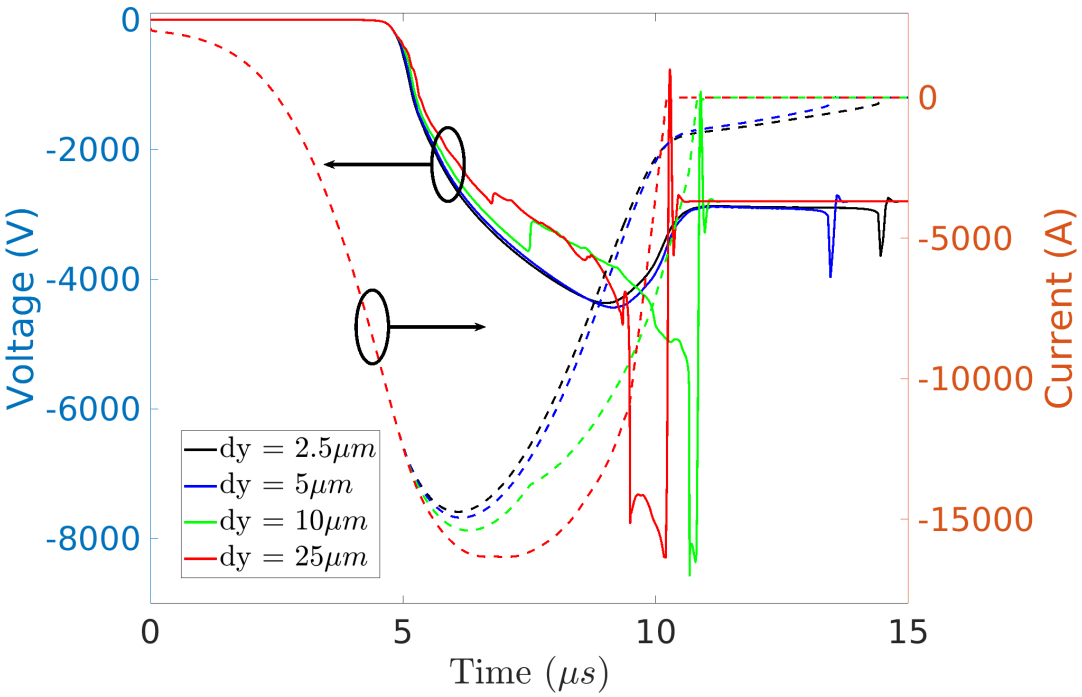


Figure 5.10: V(t), I(t) for the same device but with different mesh spacing in the drift region

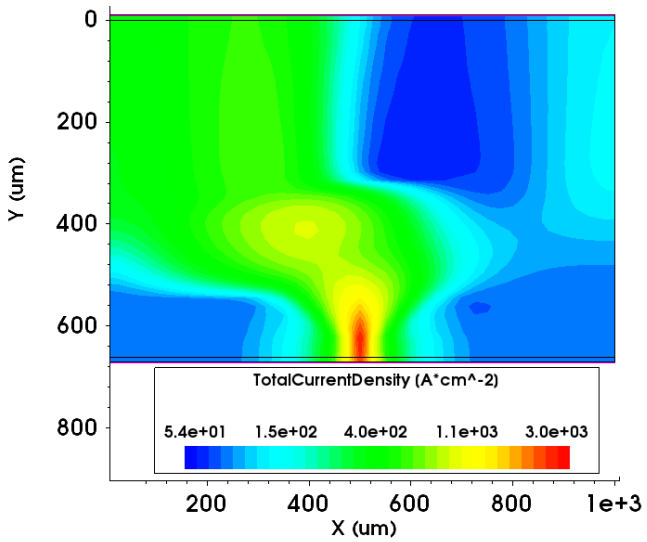


Figure 5.11: 2D contour plot of the simulations with mesh-spacing dy = 25μm at t = 7.41μs showing the presence of cathode-side current filaments.

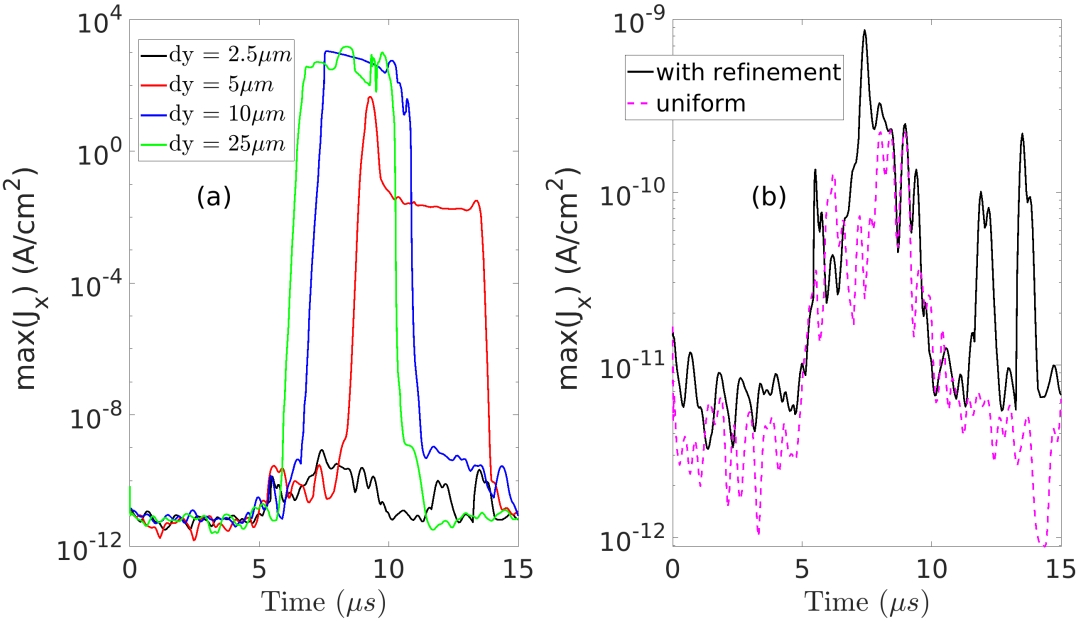


Figure 5.12: Maximum value of the current density x-component as function of time. (a) $\max(J_x)$ corresponding to simulations of Fig. 5.10. (b) both simulations have $dy = 2.5\mu m$ in the drift region. Black solid line: with refinement ($dy = 1\mu m$) at the p-n junction and at the contact. Magenta dashed line: with $dy = 2.5\mu m$ everywhere.

predict how much discrete power diodes with large active area are sensitive to current filamentation, Finally, the presence of small doping fluctuations is analysed.

5.4.1 Anode doping profile

Simulations of the FRD with different anode doping profiles have been carried out as shown in Fig. 5.13 (a). The depth of the p-n junction, y_J, has been chosen so as to have the same static breakdown conditions due to the punch through and, simultaneously, to strongly affect the electric field peak at the p-n junction for $t > t_0$ of Fig. 5.2 leading to a large dynamic avalanche condition. This is clearly shown in Fig. 5.13 (b) where the J_x fluctuations are compared for the different y_J. No significant fluctuations are observed for $y_j \geq 95\mu m$. On the contrary, there is no way to suppress current fluctuations for lower y_j, even if the device is ideally uniform. This gives rise to

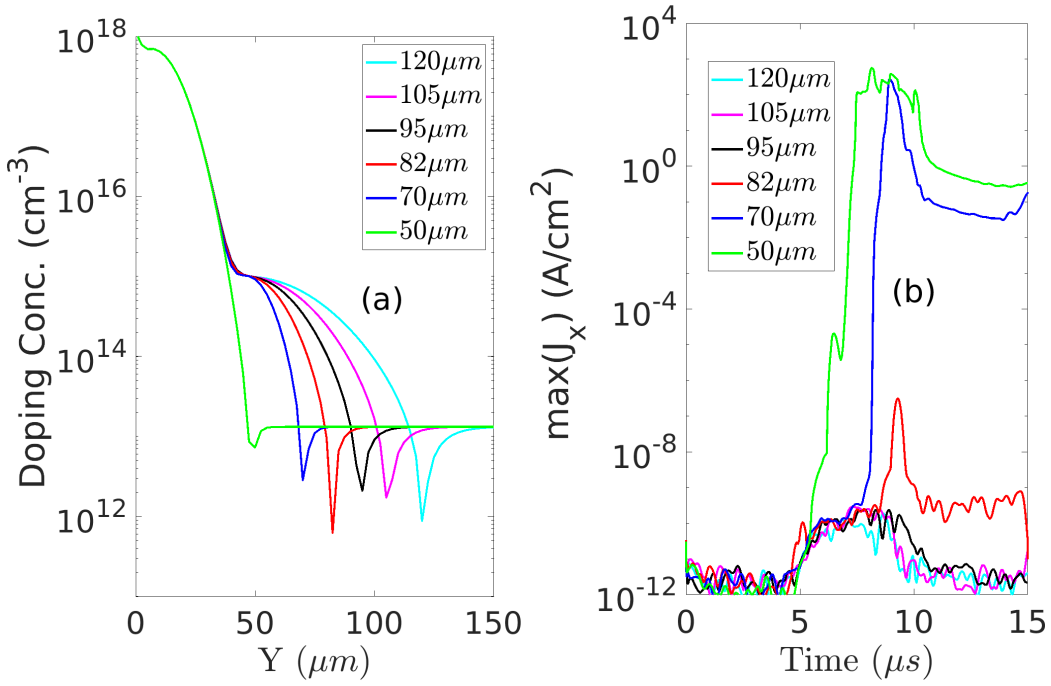


Figure 5.13: (a) Anode doping profile with different junction depth (y_J). (b) Maximum value of J_x as function of time.

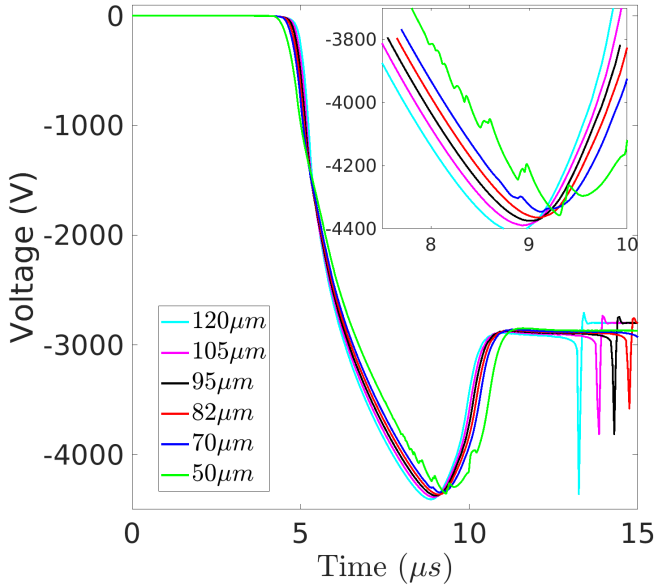


Figure 5.14: V(t) reverse recovery curves of diode with the doping profile shown in Fig. 5.13(a).Inset: zoomed curves in the time range from 7.5 to 10us.

current filaments occurring in the time range from 7.5 and 10 μs, as shown in Figs. 5.14 and 5.15. By using this kind of simulations, the smallest value of y_j providing high ruggedness to dynamic turn-off can be extracted.

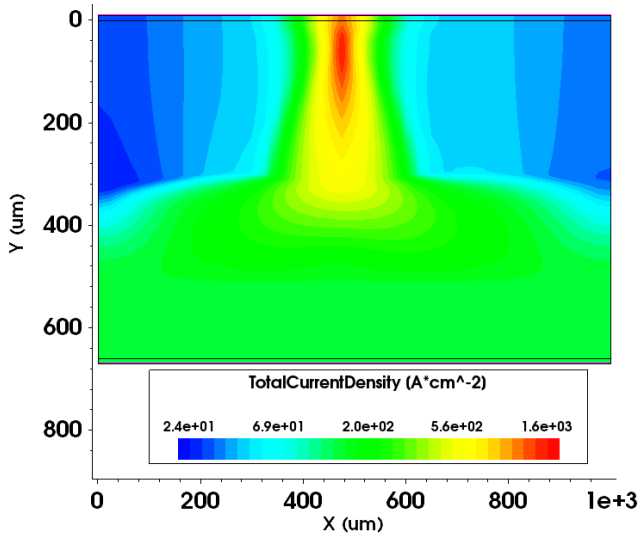


Figure 5.15: 2D contour plot of the diode with the $50\mu m$ deep p-base from Fig. 5.13(a) at t = $8.65\mu s$ showing the presence of anode-side current filaments.

5.4.2 Lateral width of the simulated device

It is known form literature [53] that instabilities can easily develop into current filaments if the device has large lateral dimension L_x. This can be shown by performing simulations of the same diode but with different L_x. In Fig. 5.16, simulations of three diodes with $y_J = 50\mu m$ and lateral lengths L_x = 1000, 5000 and $10000\mu m$ are compared. The shortest one corresponds to the reference diode used in the analysis of the anode doping profile which gives rise to the anode current filament shown in Fig. 5.15. The comparison of the V(t) curves shows, that the significant voltage peaks in the V(t) of the diodes with larger Lx (Fig. 5.16(a)) correspond to the sudden increases of Jx (Fig. 5.16(b)) manifested by the formation of a cathode-side filament in addition to the anode-side one (not shown). This result is in good agreement with expected theoretical results showing an increased instability for large area structures [53]and experimental evidence on small (chip) diodes which can sustain high di/dt even with very narrow anode doping profiles [54].

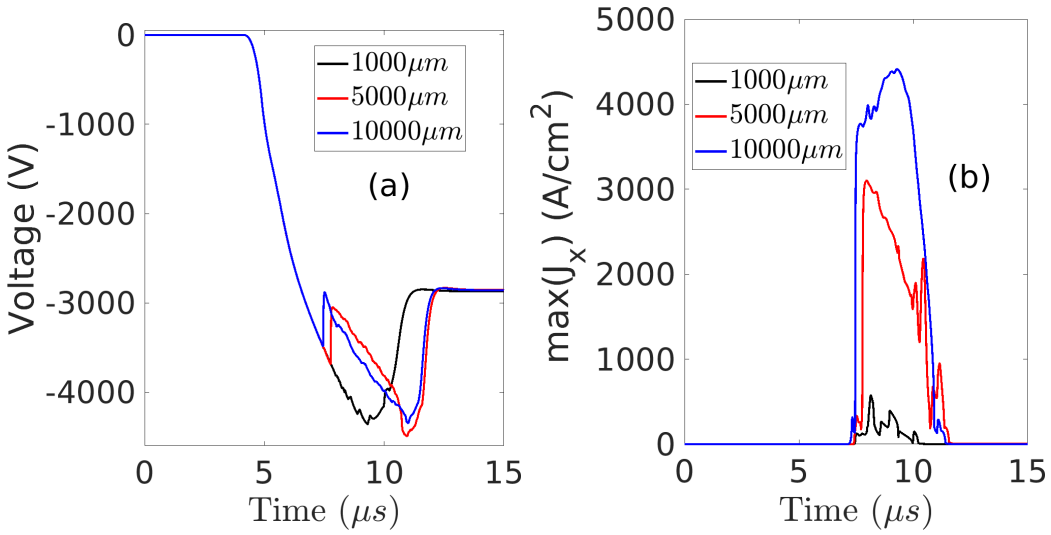


Figure 5.16: (a) V(t) curves of the diode with $50\mu m$ deep anode doping profile and different lateral width L_x (b) Maximum value of J_x corresponding to simulations shown in (a).

5.4.3 Doping Fluctuations

Small doping inhomogeneities in the anode profile, which are common in all power diodes [55], are suspected to play a role in the onset of current instabilities. In order to investigate the effect of such non-uniformities on the generation of current filaments, a single doping inhomogeneity has been added in the middle of the diode structure with $y_J = 95\mu m$ and $L_x = 1000\mu m$, which is one of the stable structures in Fig. 5.13. The lateral extension of the inhomogeneity was fixed to $100\mu m$, while different possible profile shapes of a potential non-uniformity have been tested as shown in Fig. 5.17 (a). The corresponding magnitudes of the maximum J_x reported in Fig. 5.17 (b) clearly show that the worst case is given by the doping profiles with locally lowered concentration (B1 and B2) contrary to the increased one (A1 and A2). Even if no filaments were generated by such fluctuations, a larger instability with respect to the homogeneous reference case is found, which might be the cause of the onset of the current filamentation if other factors promoting instabilities, like those discussed above, take place.

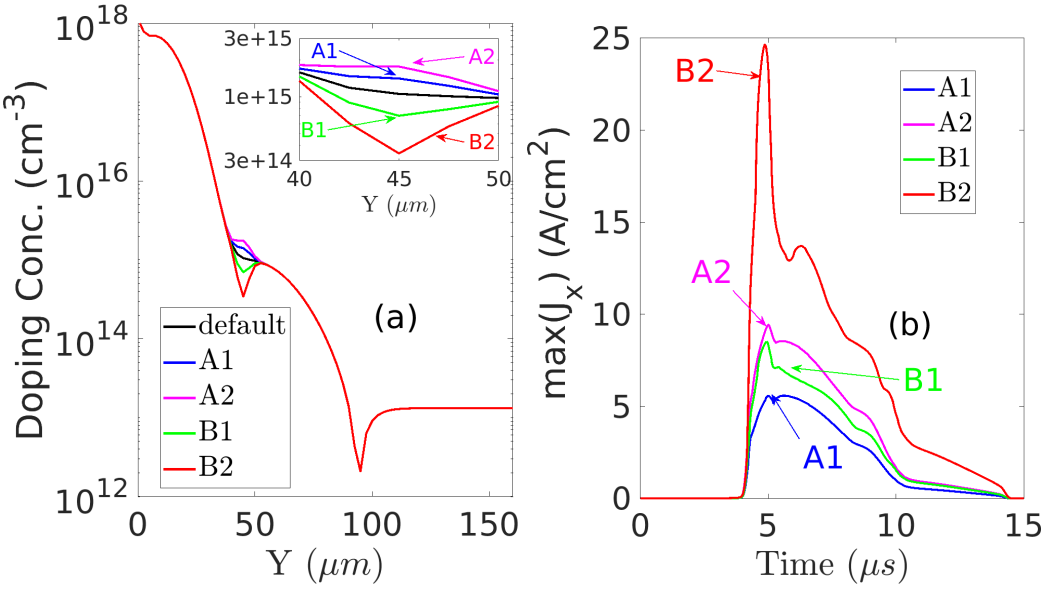


Figure 5.17: (a) Vertical doping profile with small inhomogeneities (A1, A2, B1, B2) magnified in the inset (b). Maximum value of J_x corresponding to the simulations shown in (a).

Chapter 6

Conclusions

Negative bevelled power diodes with Diamond-like Carbon coating, exhibit very high performance in terms of reliability. Indeed, a significant increase of the breakdown voltage can be obtained with limited variations of the leakage current with respect to the non passivated device. However, the benefits coming from the DLC passivation disappear at higher temperatures where the properties of the silicon bulk are dominant. An accurate TCAD model of the DLC transport mechanisms is thus necessary to give a physical interpretation to the observed phenomena. In this thesis, based on the characterization of MIM and MIS structures, a TCAD model for thin DLC layers has been developed. It has been shown, that DLC exhibits some peculiarities, such as the absence of significant threshold voltage in the JV curves of MIS structures and the low Schottky barrier for both carriers. For these reasons, a modelling approach which differs from those typically used for disordered materials is needed. In particular, the presence of broad Gaussian density of states has been assumed together with a Poole-Frenkel mobility model for the charge transport and a Ferroelectric model for the polarization phenomena. The effects of nitrogen or boron incorporation has been accounted for assuming an increase of disorder. This has been modelled by assuming: (i) a higher carrier mobility, (ii) a large number of available states for the conduction, (iii) larger polarization vector, (iv) the presence of active doping. The proposed model is thus able to predict the breakdown voltage and the leakage current of a

negative-bevelled power diode over a wide range of temperatures. In addition, it can be applied to different devices and different junction terminations as shown in Chapt. 4 where the effects of a DLC passivation on a VLD planar termination have been investigated. Finally the formation of current filaments in silicon power diode during the reverse recovery has been studied and an accurate TCAD approach has been proposed to reduce the numerical error coming from the discretization of the transport equations. It can be considered as a solid starting point for a rigorous analysis of the impact of different inhomogeneities, which may appear in large-area high-voltage fast recovery diodes, hereby providing a useful tool for a further enhancement of their ruggedness and reliability.

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