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MODULAR MULTILEVEL CONVERTERS WITH INTERLEAVED HALF-BRIDGE SUBMODULES

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Preface

Power electronics have gone through several stages of development during last few decades, especially in the fields of high-power, high- and medium-voltage applications, giving rise to a new generation of power conversion equipment in either ac or dc form. Currently, the modular approach in the power converter design dominates the market. There are several modular converter topologies that are commonly employed in various high-power applications, namely cascaded H-bridge, H-bridge neutral-point clamped, and modular multilevel converter (MMC). Among them, MMC-based structures have received wide acceptance from both industry and academia thanks to their high degree of modularity, built-in redundancy, high efficiency, and low harmonic content. Modular multilevel converters are made up of a series connected strings of submodules (SM), whose classical arrangement is either half- or full-bridge. These configurations can easily match the constraints for high-power, high/medium-voltage applications; but they do not efficiently meet the requirements for high-power, low/medium-voltage application niche, e.g., ultra-fast electric vehicle (EV) charging infrastructures, electric traction system, etc. The current project was aimed to fill the gap in modular and efficient converter design for such applications. Hence, the main development of this thesis is based on high-power, low/medium-voltage converter arrangement with reference to high-power EV chargers. Nevertheless, the proposed converter is not limited to the aforementioned applications and can be equally employed in all-voltage levels, high-current converter designs, owing to its highly modular structure.

The analyzed converter topology was initially proposed by Prof. Gabriele Grandi (University of Bologna) and his research team (including the author himself) in September 2020, while the key project developments were accomplished in cooperation with Prof. Remus Teodorescu (Aalborg University) and his research group, over author's research period abroad (November 2020 - July 2021).

In summary, this thesis is a unique and comprehensive work dealing with the modeling, control, modulation and technical challenges of the novel, advanced modular multilevel converter based on interleaved half-bridge submodules. The thesis is separated into four distinct parts, the first part offers an overview of state-of-the-art in MMC and interleaved converter technologies. It also explores some trending high-power applications, where the new converter topology can benefit the most. The second part covers theoretical aspects of operating principle, control methods, modulation and converter efficiency analysis. The third and forth parts are dedicated to solutions of the technical challenges associated with new converter structure. Each section, apart from the first, includes extensive either hardware-in-the-loop or experimental results to support the explained concept.

The thesis is written in a simple language to make it accessible to a wide audience. The necessary analysis and further developments are provided for each concept. The author hopes the reader will find the thesis useful and stimulating for further research of the proposed converter structure.

Bologna, Italy Aleksandr Viatkin
January 26, 2022

Acknowledgements

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In our group I was very lucky to count with the help of my colleagues and dearest friends Riccardo Mandrioli, Francesco Lo Franco, Marija Vujacic, Milan Srndovic, Manel Hammami and Rudolf Francesco Palumbo Paternost. They always provide me with the right answers to all my questions and doubts, while wearing a cheery smile on their faces. Many thanks to you all.

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always feel blessed to have such people around me in good and bad times. Nothing would have ever been the same without them and their endless support.

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Abstract

Recent trends in industry and transport sectors decarbonization revealed an immense power demand. This new paradigm is changing the way the electrical grid is conceived. New and emerging concepts in generation, transmission, distribution, storage, and consumption of electrical power transform casual power networks into power electronic-based power systems. In this scenario, a new generation of high-performance, high-power conversion systems is needed at all stages of power delivery. These converters have a major influence on the efficiency, reliability, cost, and dynamic behaviour of the power system. Thus, all these aspects must be addressed in the new power converter design.

Modular converter structures have been receiving increasing attention in recent years mainly due to their redundancy capabilities, superior dynamic performance, and greater reliability in comparison with conventional converters. Among them, modular multilevel converter (MMC) has a prominent potential thanks to its exceptional characteristics, including modularity, flexibility to adapt to any voltage level, significant reduction in average switching frequency without compromising remarkable harmonic performance and many other. However, due to structural constraints of the existing submodule arrangements in classical MMCs the power scalability at submodule levels is limited.

To address this issue, this PhD thesis reports a novel Modular Multilevel Converter with Interleaved half-bridge Sub-Modules (ISM-MMC). The ISM-MMC exhibits a higher modularity and scalability in terms of current ratings with respect to conventional MMCs, while preserves the typical voltage level adaptiveness. The ISM-MMC brings the known advantages of classical MMC to low/medium-voltage, high-current applications, where classical MMCs are rarely used. While ISM-MMC opens a new market niche for MMC-based converters, it is not limited to only that and can be equally employed in standard MMC applications, e.g. high-voltage, direct current (HVDC) electric power transmission systems, flexible alternating current transmission systems (FACTSs), motor drives, power electronic transformers, smart grid, etc.

A detailed description of operating principle along with the converter's average model, outer and internal control methods, a hybrid modulation scheme that helps to exploit advantages of the interleaving scheme and converter efficiency analysis are given in this thesis. It has been verified that the typical MMC control methods are still applicable for ISM-MMC. A comprehensive comparison between several design examples of ISM-MMC and classical MMC in terms of output characteristics and efficiency is also provided. Furthermore, it has been demonstrated that the number of ac voltage levels is synthetically multiplied by the number of interleaved half-bridge legs in each submodule.

The thesis also concerns a current balancing problem that is typical in interleaved converters, while it is very new issue in MMC-based structures. The problem has been rigorously studied and two control strategies have been proposed in this work to cope with the aforementioned matter. The first method is based on individual current sensing in each interleaved half-bridge leg, while the second relies on interleaved currents estimation. The developed observer allows estimating the currents through interleaved half-bridge legs in each submodule of ISM-MMC basing only on arm current and submodule's capacitor voltage measurements. This technique minimizes the number of required current sensors in ISM-MMC, thereby reducing the converter's cost, weight, and volume. Capabilities of the proposed interleaved currents sensor-based and sensorless balancing methods have been tested against standard parameter tolerances of the composing passive elements.

To make operation of such current regulators possible, a new capacitor voltage balancing strategy suitable for both ISM-MMCs and conventional MMCs is developed. The novel algorithm contains main advantages of the classical capacitor voltage balancing methods while provides an opportunity to decouple two internal tasks of ISM-MMC, namely capacitor voltage and interleaved legs current balancing. The proposed control methods feature good dynamic performance and are compliant with a digital processor's operational constraints. Extensive numerical simulations, hardware-in-the-loop, and experimental tests on a scaled-down, single-phase ISM-MMC laboratory prototype are carried out to demonstrate the feasibility of the proposed topology, implemented modulation and control schemes.

Index Terms – modular multilevel converters (MMCs), interleaved converters, interleaved half-bridge submodule, current balancing, current sharing, sensorless current balancing, high power conversion efficiency, energy balance method, capacitor voltage balancing, sorting algorithms, hybrid pulse width modulation, charging stations, electric vehicles.

Sommario

I recenti sforzi per la decarbonizzazione dell'industria e dei trasporti hanno rivelato un'immensa domanda di energia. Questo nuovo paradigma sta cambiando il modo in cui viene concepita la rete elettrica. Nuovi ed emergenti concetti riguardanti generazione, trasmissione, distribuzione, stoccaggio e consumo di energia elettrica stanno trasformando le reti elettriche tradizionali in sistemi di alimentazione basati sulla conversione elettronica di potenza. In questo scenario, è necessaria una nuova generazione di sistemi di conversione ad alte prestazioni e ad alta potenza che si estenda su tutti gli stadi di trasmissione dell'energia. Questi convertitori influiscono in maniera rilevante sull'efficienza, affidabilità, costi e comportamento dinamico del sistema di alimentazione. Pertanto, tutti questi aspetti devono essere affrontati e tenuti in considerazione durante la progettazione di nuovi convertitori elettronici di potenza.

I convertitori a struttura modulare hanno ricevuto crescente attenzione negli ultimi anni principalmente a causa delle loro capacità di ridondanza, prestazioni dinamiche superiori e maggiore affidabilità rispetto ai convertitori convenzionali. Tra questi, il "modular multilevel converter" (MMC) ha un potenziale prominente grazie alle sue eccezionali caratteristiche, tra cui fra le altre, modularità, flessibilità nei confronti di qualsiasi livello di tensione e significativa riduzione della frequenza media di commutazione senza compromissione delle notevoli prestazioni armoniche. Tuttavia, a causa dei vincoli strutturali legati alla topologia dei sottomoduli MMC classici, la scalabilità di potenza a livello del singolo sottomodulo è limitata.

Per affrontare questo problema, questa tesi di dottorato riporta un nuovo "Modular Multilevel Converter" avente i SottoModuli realizzati utilizzando la configurazione "Interleaved half-bridge" (ISM-MMC). L'ISM-MMC presenta una maggiore modularità e scalabilità in termini di valori nominali di corrente rispetto agli MMC convenzionali, pur preservando la tipica adattabilità del livello di tensione. L'ISM-MMC introduce i noti vantaggi del MMC classico anche nelle applicazioni a bassa/media tensione e alta corrente, dove l'MMC classico viene raramente utilizzato. Nonostante ISM-MMC apra una nuova nicchia di mercato per i convertitori del tipo MMC, non si limita solo a questo e può essere ugualmente impiegato in applicazioni MMC convenzionali, ad esempio, sistemi di trasmissione dell'energia del tipo "high-voltage direct current" (HVDC), "flexible alternating current transmission systems" (FACTSs), azionamenti elettrici, "power electronic transformers", "smart grid", ecc.

In questa tesi, vengono descritti in maniera dettagliata il convertitore, il suo principio di funzionamento, il modello medio, i metodi di controllo esterno e interno, uno schema di modulazione ibrido che aiuta a sfruttare i vantaggi dello schema "interleaving" e l'analisi dell'efficienza. È stato verificato che i tipici metodi di controllo per MMC sono ancora applicabili anche per ISM-MMC. Viene inoltre fornito un confronto completo tra diversi esempi di progettazione di

ISM-MMC e MMC classici in termini di caratteristiche di uscita ed efficienza. Inoltre, è stato dimostrato che il numero di livelli di tensione risulta moltiplicato direttamente per il numero di "half-bridge" collegati in modalità "interleaved" in ogni sottomodulo.

La tesi tratta anche il problema del bilanciamento delle correnti, tipico dei convertitori "interleaved", ma del tutto inedito nelle strutture basate su MMC. Il problema è stato rigorosamente studiato e in questo lavoro sono state proposte due strategie di controllo per far fronte a quest'ultimo. Il primo metodo si basa sul rilevamento della corrente effettuato individualmente su ogni "half-bridge", mentre il secondo si basa sulla stima delle correnti "interleaved" attraverso l'utilizzo di un osservatore. L'osservatore sviluppato consente di stimare le correnti incidenti ogni half-bridge all'interno dei sottomoduli basandosi solamente sulla corrente di "arm" e sulle misure di tensione dei condensatori in ogni sottomodulo. Questa tecnica riduce al minimo il numero di sensori di corrente richiesti per l'ISM-MMC, riducendo così il costo, il peso e il volume del convertitore. Le prestazioni della modalità basata sull'utilizzo di sensori e della modalità con osservatore "sensorless", sono state testate tenendo in considerazione la presenza di parametri soggetti alle tipiche tolleranze degli elementi passivi.

Per rendere possibile il funzionamento di tali regolatori di corrente, viene sviluppata una nuova strategia di bilanciamento della tensione dei condensatori sia negli ISM-MMC che negli MMC convenzionali. Il nuovo algoritmo contiene i principali vantaggi dei classici metodi, seppur disaccoppiando i due compiti interni agli ISM-MMC, vale a dire il bilanciamento della tensione del condensatore e il bilanciamento delle correnti "interleaved". I metodi di controllo proposti presentano buone prestazioni dinamiche e sono conformi ai vincoli operativi di un processore digitale. Molteplici simulazioni numeriche, "hardware-in-the-loop" e prove sperimentali su un prototipo in scala ridotta di ISM-MMC monofase sono state eseguite per dimostrare la fattibilità della topologia proposta e dei relativi schemi di modulazione e controllo implementati.

Contents

Chapter 1

Introduction

This chapter introduces the global context, from which the motivation of current thesis is originated. The chapter deals with state-of-the-art and recent advancements in high-power converter topologies. In general, all high-power converter topologies can be classified into two main groups, namely power converters that use an intermediate dc-link or those which do not. The latter approach is the direct power conversion from ac to ac, where the vivid members of this group are cycloconverters [1] and matrix converters [2, 3]. Power converters from the first group, based on the type of dc-link, can be further categorized into voltage source converters (VSCs) [4–7], current source converters (CSCs) [1, 2, 4, 8] and their derivatives – hybrid topologies [4]. Among all mentioned technologies, VSCs have the highest market share and are widely used in industries. Therefore, this overview mainly focuses on the VSC group.

With power being the product of voltage and current, it seems logical that converter's unlimited power ratings can be achieved by increasing either the rated voltage or current. Alternatively, both of them can be leveled up. In that respect, the well-known two-level converter, which belongs to the VSC family, is commonly limited to a relatively low-power conversion level, mainly due to semiconductor rating constrains. The commercially available semiconductor devices and their voltage and current ratings are shown in Table 1.1. From this perspective, selection of a particular semiconductor technology leads to a certain boundaries in the converter's functioning. For high-power applications, two-level converters require either semiconductors in series to arrive at medium- or high-voltage operation with comparatively low currents or the devices in parallel to carry high-current at low-voltage operation. The hybrid schemes are also possible. However, such series or/and parallel connections of semiconductor devices do not introduce any enhancements in output waveforms harmonic performance and dv/dt reduction. Imperfect dead-times synchronization, negative temperature coefficient (for some semiconductor technologies), uneven power losses and voltage blocking are just a few issues that must be handled in such high-power converter arrangements. Hence, conventional two-level converters have very limited usage in high-power applications.

To overcome the limitations of semiconductor device ratings, a modular, scalable converter design approach has been introduced. Based on this method, identical submodules are cascaded to reach the higher operating voltage. Likewise, some submodule configuration can be placed in parallel to increase operating current. In such manner, the scaling of voltage and/or current ratings in power converters can be easily adjusted to the needs of a specific application. Furthermore, maintenance of such power converters can be reduced, and their availability can be significantly improved due to the fact that in case of submodules failure, this converter can still

operated with reduced performance. In this context, modular power converters have become attractive solution for many high-voltage, high-current applications.

Table 1.1 – Market overview of power semiconductors

Semiconductor device/Parameter	Blocking voltage	Current
power diode	8.5 kV @ 4.45 kA	13.5 kA @ 0.4 kV
thyristor	10 kV @ 1.7 kA	6.1 kA @ 1.8 kV
GTO	9 kV @ 2.5 kA	6 kA @ 6 kV
IGCT	9 kV @ 1.7 kA	6.5 kA @ 4.5 kV
IGBT	6.5 kV @ 1 kA	3.6 kA @ 1.7 kV
MOSFET	3.3 kV @ 0.75 kA	1.1 kA @ 0.75 kV

Several modular converter topologies have been introduced in literature, however just few of them were adopted in industry. Among them, the cascaded H-bridge (CHB) [9–11] and cascaded neutral-point clamped (CNPC) [11, 12] converters, which generally designed for medium- or high-voltage, high-power conversion, gained decent popularity. Reduced component's voltage stress, good output power quality, easy scalability are just few intrinsic advantages that they can offer over the traditional non-modular converters. On the other hand, these topologies feature high number of switch counts. Several works were dedicated to reduce switch count, preserving high power quality [13, 14]. Another major issue associated with these converters is the need of separate dc sources for each submodule, which increases the overall footprint and cost of the conversion system. On the contrary, another advanced, scalable topology, namely modular multilevel converter (MMC) preserves the features of cascaded converters while can be supplied by a single power source [15, 16]. Moreover, given an excellent performance in quality of input/output waveforms and adjustable to any voltage level structure, MMC can be connected to medium- or high-voltage power source without an intermediate transformer. Hence, the MMC technology is selected for further analysis in the current thesis.

Unlike high-voltage converter designs, the VSC family can offer just few converter configurations that are specifically designed for high-current operation [17–19]. Instead, most of the research is devoted to a parallel operation of monolithic converters (e.g., the two-level, neutral point clamped (NPC), flying capacitor (FC) converters, etc.) [7, 20, 21] or some structural parts (semiconductor device, submodule, branch, phase leg, etc.) of the modular converters (e.g. cascaded H-bridge, modular multilevel converters, etc.) [22–25]. In this context, the family of multi-unit interleaved converters demonstrate superior performance characteristics, which are, for example, high current-carrying capabilities, having parallel power stages, and reducing input/output waveforms ripple without increasing the switching frequency [18, 26]. Thus, further interleaved converters are taken as a benchmark in high-current converter design.

In the following sections, the basic concepts and terms that are employed throughout this dissertation are presented. A review is carried out by demonstrating the most noteworthy research contributions in modular multilevel and interleaved converters. Later, an overview of some emerging high-power applications is introduced. The thesis motivation, employed methodology and outline complete this introductory chapter.

1.1 Modular Multilevel Converters

The modular multilevel converter (MMC) is currently one of the growing power converter technology, which has attracted particular attention among researchers and industry worldwide. The MMC belongs to the multicell converter family, and it was first introduced in [27] for high-voltage applications. Over the past years, this topology has been further extended to other applications in the medium-voltage level. It features, high quality of output waveforms (voltages and currents), great modularity and it is easy scalable to any voltage ratings, as a result of using identical submodules SMs. On top of this, having inherent redundancy it is capable to provide high availability of the whole power conversion system. However, MMC unique characteristics such as the large number of SMs, a need of dedicated internal control for floating capacitor voltages balancing and circulating currents, make this converter topology a particularly complex structure. In this section, a general overview of the MMC basics along with its typical applications are discussed. Finally, the state-of-the-art MMC modulation and control methods are presented.

1.1.1 Topologies and Applications

The most employed three-phase MMC configuration is the one shown in Figure 1.1, which commonly referred as a double-star topology. Many other converter architectures have been presented in the literature. Each configuration aims to improve certain features or address some specific needs of the applications where converter is used. Several of these configuration and related applications are discussed here.

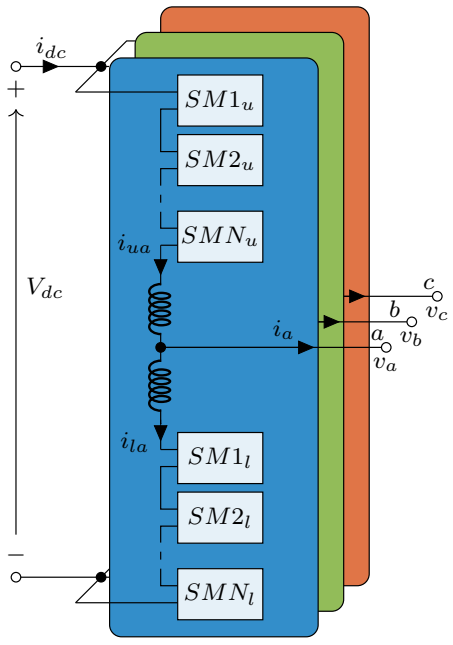

Figure 1.1 – Dc to ac three-phase MMC topology

Among other conventional MMC circuit configurations [28] that commonly appear in literature are single-star topology with full-bridge cells (also referred as "cascaded multilevel converter with star connection") [29], single-delta configuration with full-bridge cells (also known as "cascaded multilevel converter with delta connection") [29, 30], modular multilevel matrix converter [31] and hexagonal converter [32]. Nevertheless, recently several advanced and hybrid

MMC topologies [15, 33] have been presented to address the operational and technical issues associated with the conventional MMCs. For example, alternate arm MMC [34], in which each arm is formed by a string of full-bridge SM, a director switch, and an arm inductor is capable significantly reduce switching losses in comparison with the conventional half-bridge MMC [35]. Another MMC configuration with a middle SM, in which the upper and lower arms are connected to load/grid through a middle SM synthesizes the phase voltage waveform with a identical number of voltage levels as the conventional MMC, while requires less number of SMs [36]. The next hybrid MMC configuration is a derivative of MMC with a middle SM, in which two submodules of each phase leg are connected to the positive and negative bars of the upper and lower arms, respectively. Such arrangement inherently reduces SM capacitor voltage ripple, which positively affects on size and cost of the converter [37]. The following interesting configuration referred as a flying capacitor MMC. In this converter architecture, the midpoints of the upper and lower arms are connected through a floating capacitor. This capacitor is employed to balance energy between the corresponding arms, which eventually minimizes the SM capacitor voltage ripple [38]. Other two configuration, which allow to achieve smaller the SM capacitor voltage ripple, are star- and delta-channel MMCs [39, 40]. The standard double-star MMC topology can be used as a interleaved dc/dc converter where each phase leg is connected to a common point through inductors [41]. The list of possible MMC configurations is constantly increasing and many other advanced MMC structure come in the future.

Although the most commonly used SM circuit structures are the half- and full-bridge topologies, depicted in Figures 1.2a and 1.2b, respectively, many other alternative SM topologies have been introduced in the literature [6, 15, 16, 33, 42, 43] to cope with different MMC-related issues such as blocking capabilities of dc-side fault current, reduced capacitor voltage ripple and circulating currents, and high converter efficiency. The most popular and recently proposed advanced SM configurations in MMC are demonstrated in Figure 1.2. The above introduced half-bridge SM has a simple architecture, control and design, while it does not support bipolar operation and dc fault blocking [6]. In this context, full-bridge SM supports both aforementioned features, while requires double the number of semiconductors in each SM. Moreover, this SM structure allows to reduce capacitor voltage ripple in comparison with half-bridge SM-based MMC.

Advanced, multilevel SM configurations allow improve performance and efficiency of the converter. These SM structures (cf. Figures 1.2c – 1.2j) are cascaded half-bridge [44], active neutral-point clamped [45], neutral-point piloted (also known as "T-connected neutral-point clamped") [46], flying capacitor [47], clamp-double [48, 49], cross-connected [50], single-clamped [51, 52] and IGCT-based SM [53]. Among the above mentioned multilevel SM configurations only clamp-double and cross-connected SMs generate positive/negative voltage levels at the output, hence support dc-side fault blocking capabilities. The single-clamped SM originates a family of submodules with bypass clamping diodes and it supports fault-clearing in the MMC. IGCT-based SM improves converter's efficiency, facilitates higher voltage ratings and reliability.

All discussed above SM have one common characteristic, which in high-power applications can be seen as a drawback, namely lack of scalability in current capacity. In other words, current passing through the elements of these submodules is limited by current ratings of the "weakest" element in the chain. Therefore, MMC converters based on these SMs cannot be simply boosted in terms of current ratings and other forms of parallel connectivity are required [22, 24].

MMCs in the form of standard and customized products have become the most attractive multilevel converter topology for medium/high-power applications. Currently, it is widely used in several industrial applications such as power high-voltage dc transmission systems [54, 55], medium-voltage autonomous dc grids, e.g., in shipboards [56, 57], industrial motor drives

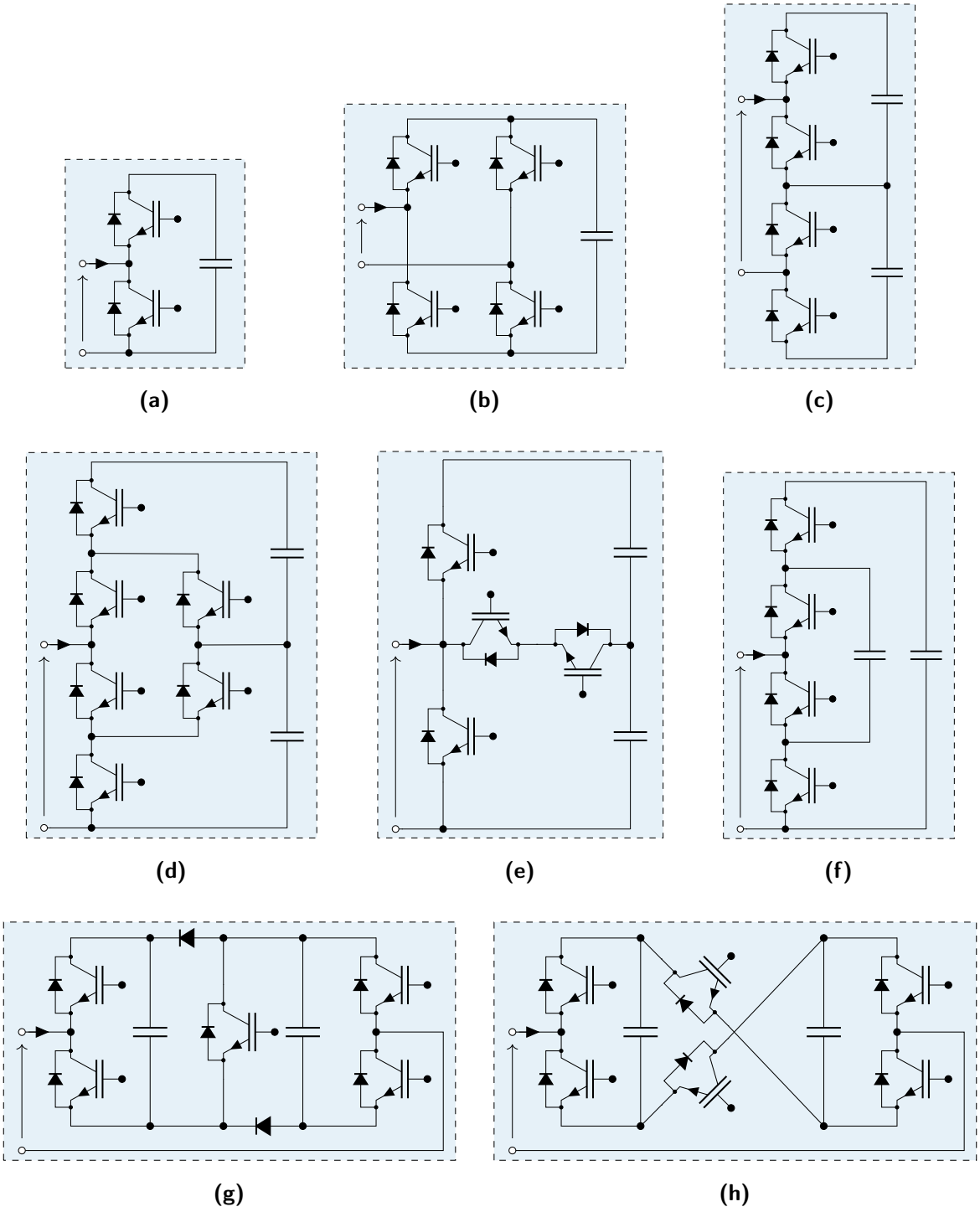

Figure 1.2 – Circuit configuration of MMC submodules: (a) half-bridge SM, (b) full-bridge SM, (c) cascaded half-bridge SM, (d) active neutral-point clamped SM, (e) neutral-point piloted SM, (f) flying capacitor SM, (g) clamp-double SM, (h) cross-connected SM

[58–60], high-power dc/dc conversion, grid power quality improvement, e.g. STATCOM [61, 62], distributed energy storage systems [63–65], solid-state transformers [66–68], high-voltage pulse generators [69, 70], etc.

Addressing existing challenges of classical MMC structures will from one side improve the availability of the MMC-based power system, enhance converter's performance, minimize its

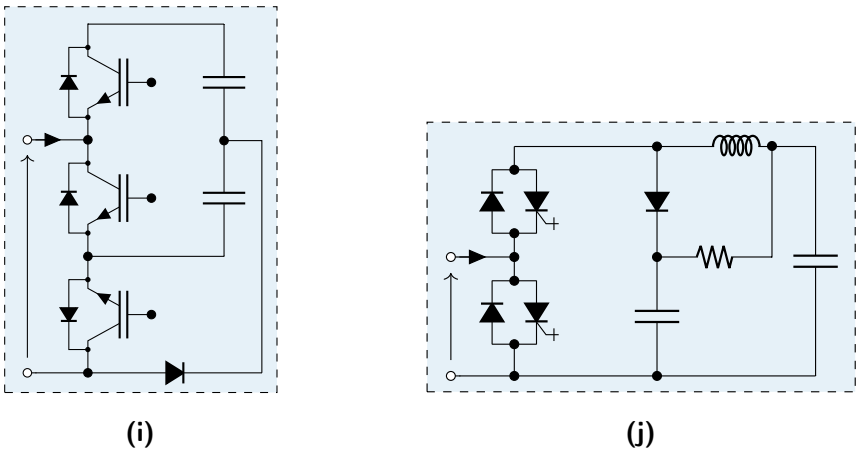

Figure 1.2 – Circuit configuration of MMC submodules (cont.): (i) single-clamped SM, (j) IGCT-based SM

footprint, reduce its capital and maintenance cost, while from another it will promote usage of MMCs in non-conventional applications.

1.1.2 Control and Modulation

To guarantee safe, stable, and efficient operation of the MMC converter, while providing high power quality, an appropriate modulation and control methods must be employed. The control of MMC is quite challenging task, and it involves multiple control objectives. The MMC control layout irrespectively of application is usually build out of several stages: an outer control stage (voltage, speed, etc.), an output current control stage, a circulating current control, an internal capacitor voltage balancing, and an arm energy (voltage) control stage [71–74]. Detailed description of the classical MMC control method can be found in Section 2.4, while here a very brief introduction of other trending control methods is given.

Each application uses a different control technique to regulate output characteristics. Most of the control strategies introduced in the literature perform quite well in the applications with a fixed ac frequency, e.g., grid-connected applications, dc/dc conversion, etc. For such application the classical MMC control or MPC-based [75–77] methods are widely used. On the other hand, in variable ac frequency applications, e.g., motor drives, special types of control methods are presented. For instance, sliding mode control has been proposed in [78]. Several alternatives to the classical MPC approach have been proposed as well, e.g., modulated MPC [79–81]. Another recently introduced control method that can be found in literature is a virtual synchronous machine control technique for MMCs with inertia response [82]. In grid-forming applications, a droop control for MMC manages parallel operation with other voltage sources and provides active power support [83, 84]. Continuous research is ongoing in the field of new control methods for classical and innovative MMC-based structures, while other concern the tailoring of several well-established control strategies, taking into account the application specifics [15, 33, 42, 85].

Modular, scalable structure of MMC permits to employ a great variety of modulation techniques, including those which are not generally suitable for other types of power converters (e.g., stair-case modulation). Review on most frequently used modulation strategies in MMCs, with relation to the current project is given in Section 2.5. Here instead, the ongoing research works in the field of advanced and hybrid modulation strategies is highlighted. In this context, most

of the research attention is given to an optimized operation of the existing solutions or their combinations. For example, authors in [86] propose a hybrid modulation method combining nearest level control (NLC) and phase-shifted pulse width modulation (PS-PWM) that allows to simplify SM's capacitor voltage balancing and significantly reduce output current distortion. Similar approach was implemented in [87] with fundamental switching frequency modulation and PS-PWM. Other researchers contribute into optimization of PWM-based techniques, e.g., single-carrier PWM method in [88], variable switching frequency PWM in [89], the voltage drop in the power devices and parasitic resistances for PWM methods is accounted in [90].

1.2 Interleaved Converters

Parallel power conversion systems have been drawing more attention in recent years due to increased range of high-current applications. As it was mentioned in beginning of this chapter, a general approach to boost current-handling capabilities of the conversion system is parallel connectivity at inner or outer converters levels (e.g., parallel units in multicell converters, parallel connections of the monolithic converters, etc.) [22, 24, 85, 91]. The main focus of this work is dedicated to the parallel connectivity at conversion unit level, promoting modular, scalable structures. The key features of the converters constructed from multiple identical units include: simple thermal design since each unit handles only a part of the total power; enhanced system reliability due to parallel redundancy and reduced thermal stress on the power components; effortless expansion of the system's power capabilities [91]. The same converter with parallel-connected units can be operated in multiple ways. The simplest way is identical switching pattern among all parallel units, in this case the whole hardware behaves as a single converter. In this context, interleaving concept adds additional advantages to the parallel-connected structures, namely it helps to avoid the parallel connection of semiconductor devices and associated with that issues (e.g., switching instants equalization, mitigation inter-unit circulating currents, etc.), ripple minimization at converter's input and output, higher efficiency [92–94]. Even though interleaved concept can be equally applied in ac/dc (e.g., interleaved power factor correction (PFC) converters) or dc/dc (e.g., interleaved buck, boost converters) conversion systems, however they share common operational principle therefore analysis of one of them would be enough to highlight the key operating features. In this regard, this section focuses more on well-established research in the field of interleaved ac/dc converters.

Figure 1.3 provides an example of interleaved dc/ac converter by depicting a generic multi-unit (K) structure of interleaved converter. Each unit is composed by a half-bridge leg and an inductor. Other multilevel units are possible, e.g., based on active neutral-point clamped leg [95] or even MMC-leg-based [96, 97]. It should be mentioned though that interleaving in MMC structures up to now was considered only at converter, leg or arm levels. This discussion continues in Chapter 2.

Commonly interleaved converters are employed in uninterruptible power supplies [98, 99], variable speed motor drives [100], and traction power supplies [101, 102], wind-power applications [103, 104], ultra-fast electric vehicles charging [18, 26, 93] and many other, where reliability and high-current ratings of the conversion equipment are required.

Assuming ideal operating conditions of the interleaved converter, the current among parallel units should be equally shared to avoid excessive thermal stress on the components and an increase of power losses, however this objective cannot be easily satisfied unless actively controlled. The typical reasons of this current imbalance and detailed description on the basic

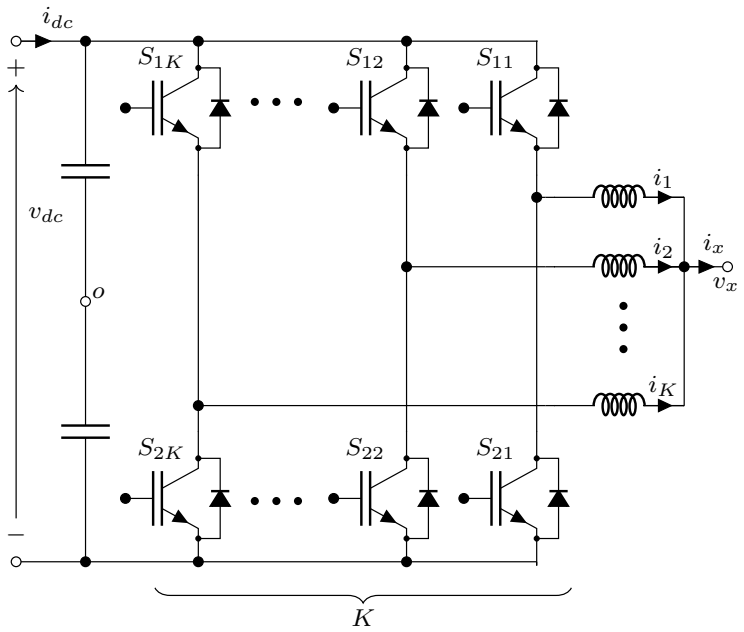

Figure 1.3 – Circuit scheme of a single-phase, multi-unit interleaved converter

existing solutions is discussed in Chapter 3 of this thesis. A great variety of other control methods have been proposed in literature to advance operation of the interleaved converters, among them distributed droop control [105], supervisory control [106], modular current sharing control [107], average control, and a circular chain control [108]. Another very promising approach to achieve current balancing among interleaved legs based on a sorting algorithm, similar to voltage capacitor balancing in MMCs, is introduced in [92].

Most of the commercial interleaved converters handle interleaving with a help of the phase-shifted pulse width modulation [103, 104, 109, 110] or space-vector modulation [111–113]. Usage of selective harmonic elimination PWM technique for interleaved converters was suggested in [114]. Some works propose to enable level-shifted PWMs in interleaved converters [92, 115].

1.3 High-Power Applications

This section provides an overview of present-day high-power application that have particular requirements on supply ratings, its availability, power modularity and expansibility, dynamic performance, possibility to provide power conditioning services and efficiency. Each subsequent subsection is dedicated to a specific application and related to it technical characteristics. The given list of such applications is not exhaustive, hence other emerging high-power application can be considered as well as a reference.

1.3.1 Ultra-Fast Charging of Electrical Vehicles

In recent years, the automotive industry has been undergoing a radical transformation driven by environmental awareness with most car manufacturers shifting their production towards more plug-in hybrid electric vehicles and zero emission battery electric vehicles (EV). Meanwhile, governments around the world are developing a variety of strategies aimed at more favorable

market conditions for electrical vehicles expansion and widespread adoption of charging infrastructure. However, the main impediment that does not allow you to quickly switch to EVs is still considered to be customer concern about the limited driving range. To face customers "range anxiety", automakers try to maximize the battery autonomy, however the concern about long charging times is still present. Typically all modern passenger EVs are equipped with an integrated on-board charger [116–118], fed by the domestic or public low-power grids. This commonly results in significant charging times ($>$ 6 hours) [119]. To cope with this problem other charging power levels have been introduced, commonly referred as fast ($<$ 3 hours, $<$ 50 kW) and ultra-fast ($<$ 1 hour, $>$ 50 kW) [120–122]. Such high charging power levels require the charger to be installed off-board. Nowadays, the most powerful commercially available all-in-one ultra-fast dc charger is "Terra 360" (ABB Ltd.) with charging power in the range 90-360 kW and dc charging voltage 150-920 V [123] that permits to recharge a car within 15 min. However, most commercialized standalone ultra-fast dc chargers for passenger cars are in the power range of 50-180 kW (e.g., “Terra 184”, ABB Ltd. [124]; "Exceed DC Dc180P", Noodoe Inc.; "DS 180", Phihong Technology Co. Ltd.). Typically these chargers include both rectification and dc/dc stages and are supplied by the low-voltage mains (400 or 480 V), thus input ac current can range up to 310 A. Authors in [125, 126] propose a statistical-based method for predicting daily power consumption in the joint parking/charging stations. This method estimates the charging time of each vehicle, which is extrapolated from the real collected data of the arrival and departure times in parking lots. EV characteristics, charging ratings, and driver behavior are taken into account in this technique. Based on this method Figure 1.4 depicts two possible charging scenarios. The first includes charging only with fast ac-based chargers (22 kW), while the other considers charging with ultra-fast fast dc-based chargers (180 kW).

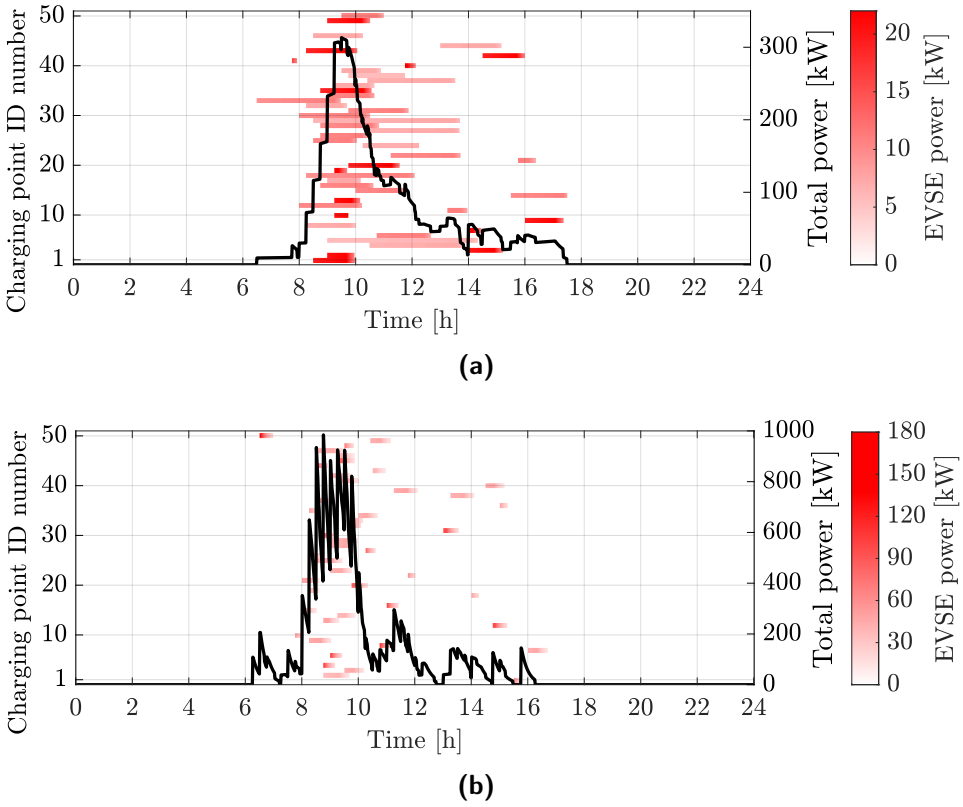

Figure 1.4 – Power supplied by individual standalone chargers at a parking/charging station with 50 parking spots equipped with: (a) 22 kW chargers, (b) 180 kW chargers

In the first scenario the charging process is more spread in time due to the low charging power, so the peak cumulative supply power does not exceed 350 kW at any given instant. On the other hand, charging with 180 kW chargers is very time dense and at the rush hours aggregate supply power can reach 1 MW. In both these cases, switch from distributed standalone low-voltage chargers to a centralized medium-voltage system with remote dispensers would be beneficial from the system point of view.

The above discussion in most cases is related to charging infrastructure for light and passenger EVs. However, when it comes to battery-electric commercial transport (bus, truck, heavy equipment, etc.) other charging power levels are required [127]. The available on the market solutions are presented by 350 kW - 1.5 MW range (e.g., “NBSK1000”, Power Electronics Corp. [128]; “1.5MW Charger”, Proterra Corp. [129]). These charging systems are usually built as a centralized conversion system with remote dispensers. The supply can be either low- or medium-voltage with input ac currents up to 2200 A (at low-voltage supply).

1.3.2 Electric Traction Systems

Electric traction systems is another very promising application for high-power converters. With private passenger transport switching to EVs, electric traction systems (e.g., locomotive, tram, metro, etc.) have gained additional attention from both academia and industry. Equipment for electric traction systems can be commonly categorized as on- and off-board. This subsection will be mostly dedicated to off-board infrastructure, while on-board equipment will be covered in subsequent Subsecton 1.3.4.

There are two types of traction power supply system, namely dc-based with typical voltage levels 600-750 V, 1500 V, 3000 V [130] and and single-phase ac-based with terminal voltage 15 kV at 16.7 Hz [131]. The transformer-rectifier substations for dc traction systems include usually uncontrolled diode (e.g., "Enviline TDR", ABB Ltd.) or controller thyrisistor-based (e.g., "Enviline TCR", ABB Ltd.) rectifiers and multi-winding traction transformer. In addition to that an energy recuperation system can be added. The common rectification schemes are 6-, 12- and 24-pulse. The common power ratings of dc traction power supplies are 5-8 MW. Despite the availability of high-power IGBT-based semiconductors, they have significantly higher losses and cost in comparison with diode-based systems [132]. Nevertheless, the need of advanced rectification systems, which support bidirectional power flow and able to provide conditioning services, have been proven in [133]. Single-phase 16.7 Hz railway networks usually are interconnected with the 50 Hz grid through the use of step-down three-phase transformer and power converters. Significant power usually must be drawn from the industrial three-phase grid and converted to supply single-phase railway networks. Therefore, the conversion system must be able to handle high-currents at medium-voltage level.

1.3.3 Hydrogen Electrolyzers

Hydrogen electrolysis is the cost-effective and eco-friendly process to produce hydrogen in industrial quantities. The production can be even more efficient and flexible if it is integrated with renewable energy generation that further supports the decarbonization of heavy industry processes. It has another beneficial aspect that could help balance peak demands, which electrical grid is experienced in rush hours, by creating hydrogen energy storage [134]. The very basic idea of the electrolysis is that a steady dc current passing through water. Therefore, this process requires a very specific electrical power supply, which must be reliable, modular, dynamically

scalable in power to support partial load operation, and fully grid-compliant. Typical units of the supply run with power in the range of 1-30 MW at dc voltage up to 1500 V, while in some cases it can be scaled up to 100 MW (e.g., "DCS880", ABB Ltd.; "Hydrogen DC Power Supply", Neeltran Inc.). Clearly in such operational constrains a power converter needs to deal with high/medium input voltage and tremendous currents at the output. Typically, thyristor-based rectifiers are used with a similar supplying scheme as for off-board dc traction supply systems. However, such configuration requires bulky multi-winding transformers.

1.3.4 Solid-State Transformers

The concept of a solid-state transformer (SST) or often called as a power electronic transformer (PET) was created to replace a conventional power transformer in its entire range of applications. The common applications of SST that are widely discussed in literature refer to on-board traction supply systems [23, 135] or shipboard supply systems [57], where volume, weight reduction and efficiency enhancement can be attained, in smart grids because of their controllability and ability to provide ancillary services [136, 137], in electrical vehicles charging systems or similar applications where the galvanic isolation is essential due to safety reasons [138]. In smart grids SSTs are especially attractive since they can be sort of a bridge between two or more voltage levels, networks with different fundamental frequencies, ac–dc networks connectivity, etc., while realizing multi-port structure. In addition to that modular structures, which are commonly adopted in SSTs, allow to reach high efficiency, reliability and maintainability of the transformer [136]. Furthermore, the SST gives possibility to act as an active filter at all connected sides of the transformer, providing e.g., harmonic compensation, reactive power compensation, grid currents balancing, voltage support, etc. Some internal features that help to optimize operation of SSTs can be also achieved, e.g. power routing in multi-cell structures [139]. There are great variety of SST topologies has been introduced recently in literature [140–142], trying to meet specific requirements of particular applications. In this context, voltage and current ratings vary significantly. So the new converter topologies to be applied in SSTs must meet all aforementioned requirements.

1.4 Thesis Motivation and Objectives

The previous sections have shown that currently the industry is in great need of a cost-effective, flexible and fully controllable, high-power conversion system, while this demand in the future will only grow [7, 60, 119]. Significant research has been carried out in this field to find a unique solution, which can meet if not all but most requirements demanded either from application side or supply/grid side. In this context, modular converter structures have gained remarkable attention, being commercially realized in many different forms [15, 16, 85, 94, 135]. MMC-based converters constantly take over the high-power converter market, where power can be boosted via an increase of the operating voltage (e.g., high- or medium-voltage). However, it is almost absent in the market of high-current, low/medium-voltage conversion systems. Another engineering question arises in the design of MMC converter for relatively high-current, high/medium-voltage applications, whether it is better to build a high-current switching unit by paralleling discrete semiconductor devices or by a single high-current rated switch. It has been demonstrated on a practical example in [94] that paralleling of power switches can be a competitive solution, having significantly lower losses at full power or almost the same losses at low operating power. In this regard, the paralleling adds an additional advantage being capable

to further reduce the losses working at low power by deactivating some parallel devices from the circuit path to realize almost nominal power operation. Moreover, high-power switches typically require a very scrupulous design, hence a new release on the market of monolithic high-power devices is very rare, while the devices are particularly expensive. Thus, many manufactures prefer achieve high-power ratings in complete converter design by paralleling low-power, inexpensive hardware.

It is clear from above discussion that paralleling of power units enhances efficiency and operational capabilities when a high/medium-current converter design is required. However, a simple parallel connection of power switches has several challenges since it is particularly difficult to guarantee equal instantaneous output voltages across semiconductor/power unit terminals [108]. Furthermore, as it was previously pointed out in Section 1.2, in such arrangement all parallel units act as a single unit, simply sharing the total current among parallel branches. To achieve better performance interleaved concept has been introduced. Among many advantages that this technique offers, a multi-level voltage waveform [92] and current ripple cancellation [18, 122] can be attained at the output terminals of an interleaved converter.

Summarizing the discussion above the primary objective of this work is to merge benefits of both converter technologies (i.e., MMC and interleaved converter) to realize a highly modular structure in both voltage and current ratings. Even though interleaving effect (also parallel connectivity) can be realized at different structural stages of MMC (e.g., phase legs interleaving of the same MMC, arms interleaving, etc.) this thesis focuses on interleaving/paralleling at the submodule level, based on basic half-bridge units. This choice is motivated by the fact that the selected unit is mass-produced, simple and requires low component count per unit. Another notable reason that supports parallel connectivity at SM level is the fact that such converter structure will bring well-known modularity of classical MMCs at another level by adding extra degree of freedom. Widely recognized redundancy and reliability of MMC will also benefit from such converter arrangement since failure of one parallel unit in a single SM does not mean failure of the whole SM, hence bypass of the SM is not always necessary. Nevertheless, one should bear in mind that the right choice whether to bypass solely the failed parallel unit or the whole submodule must be made including the studies on minimal power reduction caused by the bypass action. In such manner, a new highly-scalable and reliable converter structure will be developed.

It has been demonstrated that the classical MMC is by default a complex converter topology requiring several different control layers. Adding an extra degree of modularity to the new MMC-based converter will further increase the control complexity. In this regard, the second objective of this thesis is to analyse controllability of the new converter and suggest a robust control method. An additional aim of this work is to examine and compare efficiency of the new converter solution with its close competitors. On top of this, the proposed converter concept, its control and converter's behavioural characteristics must be verified via experimental tests. Thus, a scaled-down, laboratory prototype should be build and tested.

1.5 Methodology

To achieve the above mentioned research objectives, the following methodology is employed:

Problem statement. The first step is to identify the problem and search for the existing solutions. For doing so, an extensive literature research on high-power converters and their traditional as well as emerging applications has been done. Currently, scientists and industry representatives

are well emphasizing the lack of flexible, scalable high-power conversion systems, especially in low/medium-voltage, high-current applications. Among the great variety of already introduced high-power converter structures, the MMC-based and interleaved converters were short-listed as the most trending and promising technologies. The selection was made based on the numerous advantages that these conversion systems can offer, e.g., high degree of modularity, reliability, excellent input/output harmonic performance and many other, which are well reported in literature. Bringing together advantages of the aforementioned converters, a new highly-scalable in both voltage and current ratings, high-power power electronic topology was developed. Exhaustive search for the close analogs among the existing solutions has not revealed similarities.

Detailed modeling and analysis. The next stage is to derive mathematical model of the new converter structure and verify its operational capabilities. In addition, the mathematical modeling servers for the subsequent control design phase. In this manner the average model of the novel converter was developed, pointing out its working capabilities. Then, basing on the average model the control strategy was suggested.

Time-domain simulations. Having already implemented mathematical modeling and control design, the following phase is to verify the converter concept via numerical simulations, primarily in open-loop operation and then with the suggested control method. Based on the obtained results it is already possible with certain degree of confidence to declare feasibility of the proposed converter structure.

Hardware-in-the-loop tests. Nowadays, the hardware-in-the-loop (HIL) test has become an essential stage of the embedded software verification and concept validation process. There are several reasons why HIL tests are highly recommended before actual deployment of new control algorithms on a controller linked with its plant. First, software can be tested even before the actual hardware is built or available. Second, the risk of damaging the hardware due to control errors is eliminated. Third, real operating and abnormal conditions can be easily created to test the control actions and system behaviour. Eventually, modern HIL platforms allow to run very complex systems at full scale, which is not always possible to realize, especially in laboratory environment [143].

Prototype assembling and experimental verifications. Hardware-in-the-loop tests are only intermediate step to identify hardware implementation challenges. Therefore, the next stage is to built a laboratory, down-scaled prototype. At this point the robustness of the control can be extensively verified since it must account uncertainties and non-linearities that come along with the converter operation, e.g., measurement uncertainties, internal element uncertainties, inductor saturation, etc. Basing on the performed experimental test, a preliminary conclusion about the converter's dynamic and steady-state behavior can be drawn.

1.6 Thesis Outline

In the following chapters, the details about the design of the high-power modular multilevel converter with interleaved half-bridge submodules will be presented. This thesis focuses on the general design principles to justify the feasibility of the introduced power converter. The organization of this thesis is as follows.

Chapter 1 presents the necessary review on the three principal areas that are dealt with in this thesis report. First of all, the most significant publications of the modular multilevel converters domain are summarized, providing necessary MMC-related terminology and description of

typical MMC structures and applications, modulation and control schemes as well as operating issues. Similar overview has been prepared for the field of interleaved converters. Finally, some emerging technologies, where the proposed converter structure can benefit the most, are discussed as well, highlighting the key application-related requirements. The rest of the chapter is dedicated to main objectives of the thesis and followed methodology.

Chapter 2 introduces a detailed explanation of the modeling principles for the new converter and derives equations that form the basis for the subsequent control system design. To drive the converter an advanced modulation scheme is adopted. The chapter is structured in the manner to point out the principle similarities/differences between classical MMCs with half-bridge submodules and the novel MMC based on interleaved half-bridge submodules. In this context, their control design, structural and performance characteristics, including efficiency analysis are confronted basing on either general converter design or comparable, application-specific converter configurations. In either way, each concept is supported by an analytical example and/or simulation results. The overall control system is deduced and verified by means of time-domain simulations and hardware-in-the-loop tests, performed by using the same per-phase converter arrangement and initial parameters.

Chapter 3 is dedicated to examination and resolution of the converter-specific problem, namely currents balancing within the new submodule structure. The solution is obtained by means of a devoted control loop that is designed and integrated into converter's overall control layout. To do so a new capacitor voltage balancing strategy is implemented. Its main features and performance characteristics are pointed out. The chapter is finalized by the presentation of numerical simulations and experimental results from a down-scaled laboratory setup.

Chapter 4 presents an advanced, current sensorless version of the current balancing method discussed in Chapter 3. The upgraded method relies on the currents estimation rather than their direct measurements. Advantages and limitations of the new method are discussed in great detail, verifying its workability in the frame of converter's overall control organization. These concepts are also validated though extensive numerical simulations and experimentally in a down-scaled laboratory prototype.

Finally, **Chapter 5** summarizes the major contributions of the dissertation as well as discusses on directions for future work. Last but not the least, **Appendix A** contains comprehensive description of efficiency computation procedure that is common for all MMC-based converter architectures. **Appendix B** provides the full description of the down-scaled laboratory setup that has been built in the frame of this thesis work.

Chapter 2

Modular Multilevel Converters with Interleaved Half-Bridge Submodules

2.1 Introduction

In this chapter, fundamental aspects of modular multilevel converter with interleaved half-bridge submodules are considered. The ISM-MMC has more complex internal dynamics with respect to classical MMC structures. Therefore, this chapter starts with a detailed description of the proposed converter topology for the following dynamics analysis. Further, operating principle and the average model of the converter are presented in Section 2.3. Converter's control system design with regard to its operation in the rectification mode is considered in Section 2.4. A novel, topology-specific modulation scheme is given in Section 2.5. It follows by modified submodule energy balancing methods, which are summarized in Section 2.6. Average modeling, in Section 2.3, is structured on a per-phase basis. Nevertheless, generally speaking, the presented theory is applicable to any single- or multi-phase ISM-MMCs. Since the converter dynamics can be reasonably modeled on a per-phase basis, the explicit phase notation in most of the expressions has been generally omitted for short notation unless otherwise is stated. It should be mentioned though that typically the vast majority of high-power applications, where initially ISM-MMC is meant to be, are three-phase based. For this reason, a comparative analysis of several three-phase designs of classical MMC and newly proposed ISM-MMC is prepared in Section 2.7. This analysis is supported by numerical simulations introduced in the same section. In addition to that efficiency related studies with respect to compared structures are summarized in Section 2.8. Verification of ISM-MMC concept and its control method is supported by hardware-in-the-loop (HIL) simulations in Sections 2.9. The chapter is finished by an overview of main ISM-MMCs' features in Section 2.10.

2.2 Fundamentals

A structural representation of an M phase (typically 3 phase) MMC using a half-bridge (HB) submodule configuration is shown in Figure 2.1a. The depicted MMC employs two arm arrangement in each phase leg, commonly labeled as the upper (u) and lower (l) arms. Each MMC arm consists of N series connected power submodules and an arm inductor. Every SM is made

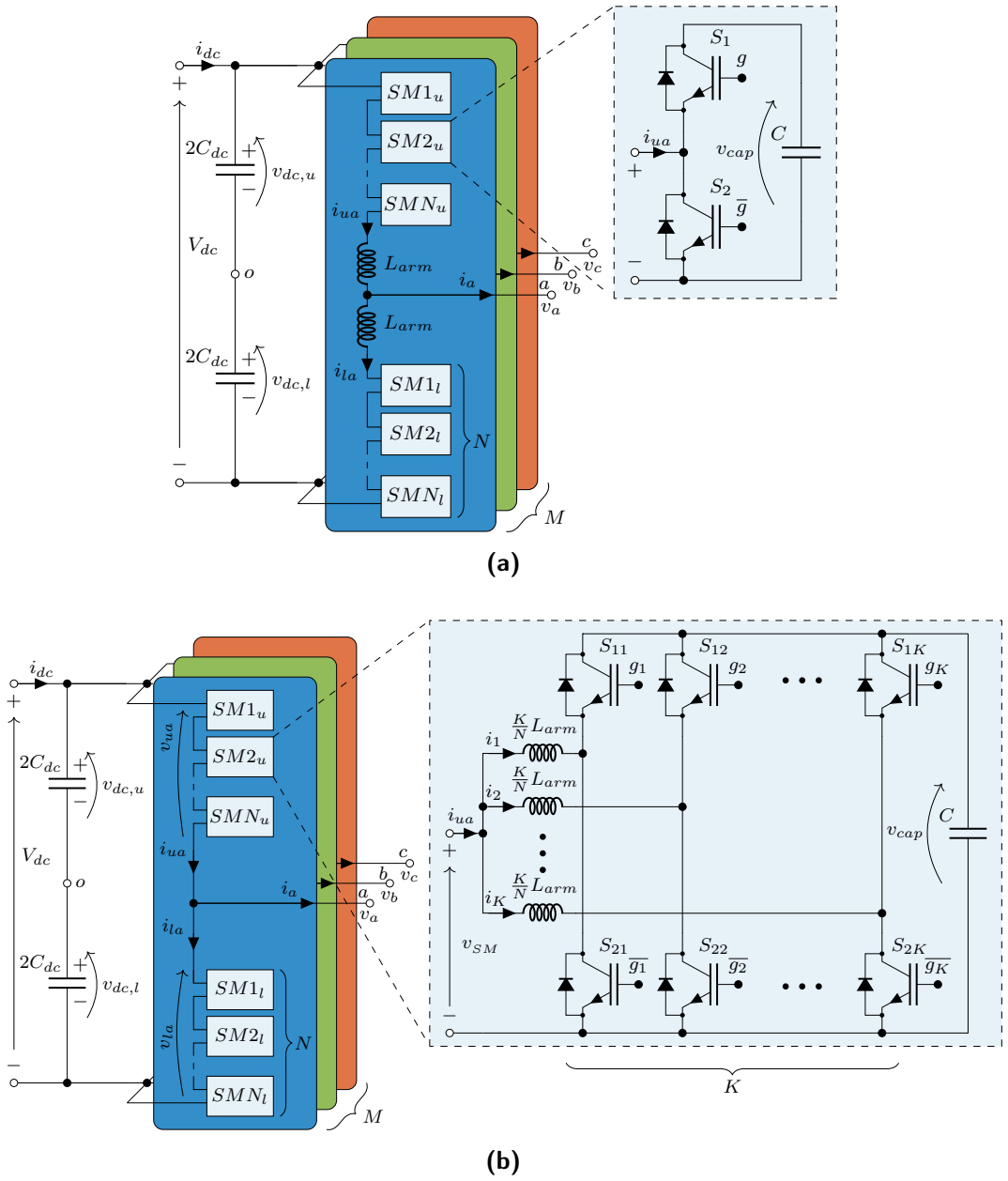

Figure 2.1 – General circuit scheme of (a) the standard MMC converter with half-bridge submodule and (b) the proposed ISM-MMC converter with interleaved half-bridge submodule [144]. © 2022 IEEE

up by a single half-bridge leg joined in parallel with a capacitor. The output terminals of the submodule are the midpoint of the half-bridge leg and one of the sides of the capacitor (here low side is taken by default). The arm inductor has a purpose to limit the current spikes caused by the insertion or bypass of the SM's capacitor [145]. The voltage level and power capacity of this type of MMC can be generally increased by the series connection of power submodules in each arm. In relation to the given MMC design, as it was explained in [146] the arm inductor can be evenly distributed among the arm composing submodules without affecting the equivalent circuit of the whole converter. Having an inductor in each SM, it can be further split into K equally sized parallel inductors. Then, by connecting each one of these inductors to the midpoint of a dedicated half-bridge leg and linking their outputs, a new configuration of a submodule with K parallel-connected legs can be derived. It should be highlighted that the K parallel-connected "inductor – HB-leg" assemblies can commutate simultaneously (this

idea was partially supported by [22]) or in interleaved mode with a proper modulation [146]. The proposed MMC with interleaved half-bridge submodules [146] is labeled as ISM-MMC and illustrated in Figure 2.1b. It should be noted that the interleaved half-bridge legs on the dc side share a common floating capacitor. This fact does not introduce extra complexity for the capacitor voltage balancing algorithms that are well established for classical MMCs. This aspect is rigorously discussed in Section 2.6.

Similarly to HB-based submodules in a classical MMC [71], the interleaved submodules can be switched in three different ways (cf. Figure 2.1b):

- **Inserted:** Any combination of the switches S_{11},...S_{1K} (either one, some or all of them) is turned on and the corresponding switches S_{21},...S_{2K} are off. This action inserts the submodule capacitor into the arm circuit. Depending on the direction of the arm current the capacitor charges or discharges.
- **Bypassed:** All switches S_{11},...S_{1K} are turned off and the switches S_{21},...S_{2K} are on. In this operating mode the submodule capacitor is bypassed. Disregarding the capacitor self-discharge, its voltage remains constant.
- **Blocked:** All switches S_{11},...S_{1K} and S_{21},...S_{2K} are turned off. This mode is typically used (with reference to classical MMCs) for energizing the converter, due to the fact that the submodule capacitor may charge through the anti-parallel diodes of switches S_{11},...S_{1K}.

The current rating of 'inductor – HB-leg' units in the proposed submodule can be K times lower in comparison with switches and arm inductor in a classical MMC (cf. Figure 2.1a). Alternatively, the total rated current of the new SM can be K times higher than the classical HB-based SM, preserving properties of individual HB-legs. Therefore, ISM-MMC introduces an additional way for increasing power capacity of the standard MMC structures by stepping up both voltage and current levels. In this context, the proposed ISM-MMC is well suited for all voltage levels, high-current applications. The concepts of power scalability and/or power partitioning, discussed in [22], [23], with ISM-MMC gain an extra degree of freedom in comparison with classical MMCs, namely power expansion on the submodule level. Since the degree of modularity in each of MMC levels: number of phases, number of series connected cells (SMs) and number of parallel (interleaved) HB legs in SMs are independent from each other, these three axes can be considered as orthogonal to one another, enabling a representation as shown in Figure 2.2. Here, each cube represents a specific design with a certain degree of modularity in each of the axes.

For instance, an element close to origin would represent a design with low-level of modularity in all axes, i.e., a single-phase, single-cell MMC. On the other hand, an element distant from the origin would represent a highly expansive structure, i.e., a multi-phase, multi-cell ISM-MMC.

Number of components in power electronic converters and in particular switching devices is very important aspect of the converter design. It is commonly accepted that the fewer components it is better. However, it is not always true, especially in high-power converter designs, where converter's availability and resiliency play even bigger role. For example, when it comes to HVDC applications or medium-voltage drives, modular multilevel converter structures are highly appreciated. In those converter designs to have extra redundant submodules is a common practice. It is also known that in order to achieve better quality of ac waveforms and eventually optimize power losses, the choice of switches with the highest blocking voltage in the market is usually avoided due to higher losses and thermal stress [147, 148]. Hence, even though it is possible to build an MMC with fewer components, nevertheless most of the commercially available MMCs follow the optimum design procedure, resulting in greater number of semiconductors.

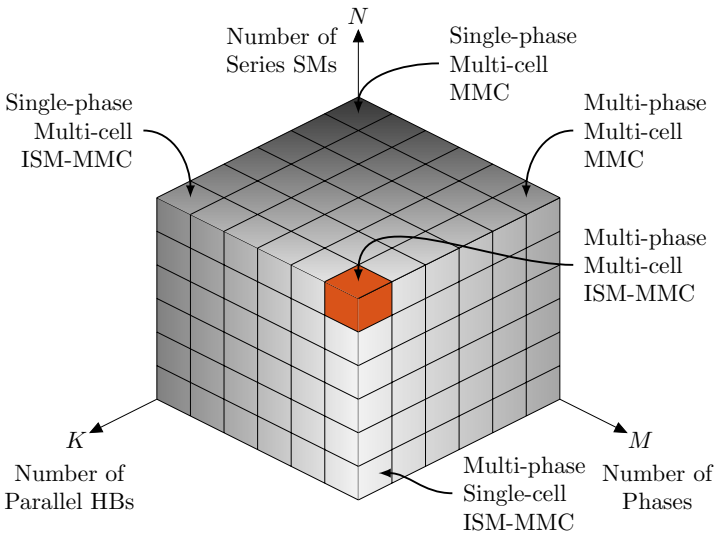

Figure 2.2 – Graphical representation of the three main degrees of modularity of ISM-MMC topologies [144]. © 2022 IEEE

Similar discussion can be applied to an ISM-MMC, while in this case the optimization can be achieved with an extra degree of freedom.Nevertheless, this converter's optimal design falls out of scope of the current work.

Another optimization in ISM-MMC can be associated with interleaved inductors. An interleaved inductor design is very attractive method to downsize magnetic components and improve power conversion efficiency in ISM-MMC. Several design techniques of magnetic components for interleaved converters have been proposed in literature. Among these methods, winding connection and magnetic integration techniques have gained the most attention. For example, authors in [149] proposed a three-phase interleaved isolated LLC converter with Y-connected windings on the primary or secondary side to balance the power transfer in each phase. Similarly, integrated magnetic components, consisted of multiple windings installed on a single magnetic core, are known as effective method to minimize interleaved inductors [150]. Nevertheless, this dissertation work is focused on the proof of ISM-MMC concept rather than on its optimization. Therefore, subjects concerning optimum design of the converter and its main components have been leaved out of scope of the current work.

The proposed ISM-MMC has an additional feature that has not been discussed so far, namely the possibility not only sharing high-current among the parallel HB legs in each SM but also to further enhance the quality of ac voltage waveforms by applying the interleaving concept. This ISM-MMC property leads to a very modest filtering requirements on the grid side. This aspect is covered in great detail in following section.

2.3 Operating Principle and Average Model

Assuming a balanced and constant dc-link bus voltage equal to V_{dc} (cf. Figure 2.1b), then the per phase relation among each x^{th} phase (for three-phase system $x = a,b,c$) voltage, corresponding arm voltages and dc-link voltage in ISM-MMC can be expressed as:

$$\frac{V_{dc}}{2} - v_u = v, \quad -\frac{V_{dc}}{2} + v_l = v \tag{2.1}$$

being v_u upper and v_l lower arm voltages, v ac phase voltage. Here and throughout the whole paper, for simplicity, the phase label (x) is generally omitted unless it is strictly necessary to indicate relation to a particular phase. The presented equations are derived per phase. The phase voltage then is defined as a voltage between ac terminal x and midpoint of dc-link o.

The arm voltages v_u and v_l, which are measured between the midpoint of the converter's arm and the corresponding dc rails, can be represented as a sum of composing submodule voltages:

$$v_{u,l} = \sum_{n=1}^{N} v_{SMn|u,l} \tag{2.2}$$

where $v_{SMn|u,l}$ is the n^{th} submodule's voltage of the upper or lower arm. It can be derived as:

$$v_{SMn} = \frac{1}{K}\left[L\sum_{k=1}^{K}\frac{di_{n,k}}{dt} + R\sum_{k=1}^{K} i_{n,k} + v_{cap,n}\sum_{k=1}^{K} g_{n,k}\right] \tag{2.3}$$

where K is the number of legs inside the submodule (with $K = 1$ the classical MMC (Figure 2.1a) can be obtained, while $K > 1$ presents the case of the interleaved configuration, Figure 2.1b) and n represents an ordinal number of the corresponding n^{th} SM of the upper or lower arm. Parameters L and R respectively are the equivalent inductance and resistance of a HB-leg path, which normally account series/parallel (e.g., on-state resistance of a power switch) and parasitic values within the HB-leg. However, for now, unless otherwise is specified, all these additives are not considered and R, L values are entirely composed by internal resistance and inductance of a leg inductor inside of each SM, respectively. Here for simplicity, the main components' parameters (R, L and C) are assumed to be equal among similar ones, unless otherwise is stated. The term $i_{n,k}$ is the current of the k^{th} leg inside the n^{th} SM. It is worth to note that $i_{n,k}$ is equal to $i_{u,l}$ in case of classical MMC being the SM composed of only one HB-leg. Finally, v_{cap} and sum of firing signals $g_{n,k}$ ($g_{n,k}$ can have value either 0 or 1) represent capacitor voltage and the corresponding number of HB legs in the n^{th} SM, where the top switch is "on". An interesting observation can be made here, namely, unlike in the classical MMC with HB submodules, the submodule voltage $v_{SMn|u,l}$, as well as the arm voltages v_u and v_l in ISM-MMC comprise voltage drops on interleaved inductors. Therefore, strictly speaking, the corresponding voltages from these both topologies cannot be directly compared, unless they properly matched.

As it can be noted from Equation (2.3), the aforementioned enhancement effect of converter's ac voltage is achieved due to the fact that the voltage across ac terminals of each submodule is actually multilevel itself. In fact, in total, there are $K+1$ open-circuit voltage levels ranging between "0" and "v_{cap}". In fact, this comes directly from Equation (2.3) by setting the sum of all interleaved currents (i.e., arm current) to zero ($\sum_{k=1}^{K} i_{n,k} = 0$), which corresponds to open-circuit operation of the converter. Similarly, the concept "$K+1$ voltage levels" can be explained by Millman's theorem. Having identical inductor values, the open-circuit voltage across ac terminals is simply the average of composing pole voltages of the parallel branches. Depending on state of the HB-legs' switches, the corresponding pole voltage can be either "0" or "v_{cap}". By applying the interleaving concept, the averaging of pole voltages will result in multilevel voltage structure with the following states: 0, v_{cap}/K, $2v_{cap}/K$, ..., $(K-1)v_{cap}/K$, v_{cap}. For instance, in interleaved SM with three HB-legs ($K = 3$) the following combinations of gate signals for upper switches (S_{11},..., S_{1K}) are possible: [000], [001], [010], [011], [100], [101], [110], and [111] (cf. submodule structure in Figure 2.1b). Therefore, in open-circuit operation with zero arm current one can count four possible levels: 0, $v_{cap}/3$, $2v_{cap}/3$, v_{cap}. Depending on the direction of the arm current, the capacitor voltage either increases or decreases. When all top switches are "off",

the ac output submodule voltage is equal to "0". In this mode, the capacitor voltage remains constant, irrespective of the current direction.

The phase (i) and converter's leg-common mode (i_{cir}) currents in the ISM-MMC are alike in classical MMCs and they can be defined as:

$$i = i_u - i_l, \quad i_{cir} = \frac{i_u + i_l}{2} \tag{2.4}$$

where i_u and i_l are the upper and lower arm currents, respectively. Combining relations from Equation (2.4) allows to express arm currents in the following form:

$$i_u = \frac{i}{2} + i_{cir}, \quad i_l = -\frac{i}{2} + i_{cir} \tag{2.5}$$

Therefore, according to Figure 2.1b, sum of the mean values of currents flowing through M upper/lower arms with constant dc-link voltage equals to mean dc current.

$$I_{dc} = \sum_{m=1}^{M} \bar{i}_{m|u,l} \tag{2.6}$$

This implies that under balanced ac-side conditions the average values of arm currents are given by

$$\bar{i}_u = \bar{i}_l = \bar{i}_{cir} = \frac{I_{dc}}{M} \tag{2.7}$$

According to Equation (2.7), in order to keep rms value of converter's leg-common mode current and corresponding to that losses at their minimum, it is necessary to maintain this current with only dc component present.

Another useful relation comes from circuit of interleaved SM and Kirchhoff's current law, namely the sum of the individual leg currents in is equal to the arm current $i_{u,l}$:

$$i_{u,l} = \sum_{k=1}^{K} i_{n,k|u,l} \tag{2.8}$$

By combining Equations (2.1)-(2.4) and (2.8) the two equations that govern phase and converter's leg-common mode currents are:

$$\begin{aligned} \frac{NL}{2K}\frac{di}{dt} &= \frac{1}{2K}\sum_{n=1}^{N}\left[v_{cap,n|l}\sum_{k=1}^{K} g_{n,k|l} - v_{cap,n|u}\sum_{k=1}^{K} g_{n,k|u}\right] - \frac{NR}{2K}i - v \\ \frac{NL}{K}\frac{di_{cir}}{dt} &= \frac{V_{dc}}{2} - \frac{1}{2K}\sum_{n=1}^{N}\left[v_{cap,n|l}\sum_{k=1}^{K} g_{n,k|l} + v_{cap,n|u}\sum_{k=1}^{K} g_{n,k|u}\right] - \frac{NR}{K}i_{cir} \end{aligned} \tag{2.9}$$

Let us define sum capacitor voltage per arm as $v^{\Sigma}_{cap|u,l}$, so the following equation holds:

$$v^{\Sigma}_{cap|u,l} = \sum_{n=1}^{N} v_{cap,n|u,l} \tag{2.10}$$

To guarantee stable and efficient operation of the MMC-like converters in most of industrial applications, all capacitor voltages must be kept around the same mean value, unless their imbalance is required by the design. The active submodule balancing usually allows to mitigate the individual differences between the capacitor voltages, so they can be neglected in the

dynamic model of the converter. Therefore, the individual SM capacitor voltages in Equation (2.9) can be approximated, with decent accuracy, by the averaged value of sum capacitor voltage per arm $v^{\Sigma}_{cap|u,l}/N$.

Normalized sum of SM's firing signals in Equation (2.9) represent the so-called "submodule insertion index".

$$u_{n|u,l} = \frac{1}{K}\sum_{k=1}^{K} g_{n,k|u,l} \tag{2.11}$$

In classical MMC structures with HB submodules it can take values either 0 or 1, whereas in ISM-MMC it can attain $K+1$ states within [0,1] range (i.e., 0, $1/K$,...,$(K-1)/K$, 1). Value $u_{n|u,l} = 0$ indicates that top switches in all HB-legs inside the interleaved SM are turned "off", so the SM capacitor is bypassed, and $u_{n|u,l} = 1$ shows that the top switches are turned "on", so the submodule voltage equal to the capacitor voltage with small voltage drop on the equivalent SM's inductor. Having number of interleaved half-bridges inside the SM (K) large enough, it allows approximating the submodule insertion index as continuous on [0,1].

Normalized sum of submodule insertion indices within an arm denotes as "per-arm insertion indices".

$$u_{u,l} = \frac{1}{N}\sum_{n=1}^{N} u_{n|u,l} = \frac{1}{NK}\sum_{n=1}^{N}\sum_{k=1}^{K} g_{n,k|u,l} \tag{2.12}$$

In classical MMC built by HB submodules it can attain any value from [0,1] range with $1/N$ discrete steps (in total $N+1$ state). Likewise, in ISM-MMC the range is the same [0,1], however the total number of discrete states is $NK+1$: 0, $1/(NK)$,...,$(NK-1)/(NK)$, 1. Again, if the joint number of submodules and interleaved HB-legs, NK, is large enough the insertion indices can be considered continuous on [0,1] range.

Inductances L and internal resistances R of the individual inductors in SMs can be easly matched to K/N times of the arm inductance L_{arm}, as depicted in Figure 2.1b:

$$L = \frac{K}{N}L_{arm}, \quad R = \frac{K}{N}R_{arm} \tag{2.13}$$

Assumptions and simplification introduced by Equations (2.10)-(2.13) allow Equation (2.9) to attain more elegant form as:

$$\begin{aligned}
\underbrace{\frac{NL}{2K}}_{L_{arm}/2}\frac{di}{dt} &= \underbrace{\frac{1}{2K}\sum_{n=1}^{N}\left[v_{cap,n|l}\sum_{k=1}^{K} g_{n,k|l} - v_{cap,n|u}\sum_{k=1}^{K} g_{n,k|u}\right]}_{(u_l v^{\Sigma}_{cap|l} - u_u v^{\Sigma}_{cap|u})/2 = v_s} - \underbrace{\frac{NR}{2K}}_{R_{arm}/2} i - v \\
\underbrace{\frac{NL}{K}}_{L_{arm}}\frac{di_{cir}}{dt} &= \frac{V_{dc}}{2} - \underbrace{\frac{1}{2K}\sum_{n=1}^{N}\left[v_{cap,n|l}\sum_{k=1}^{K} g_{n,k|l} + v_{cap,n|u}\sum_{k=1}^{K} g_{n,k|u}\right]}_{(u_l v^{\Sigma}_{cap|l} + u_u v^{\Sigma}_{cap|u})/2 = v_{cir}} - \underbrace{\frac{NR}{K}}_{R_{arm}} i_{cir}
\end{aligned} \tag{2.14}$$

The phase and converter's leg-common mode currents are two state variables in the ISM-MMC per-phase dynamic model. In addition, each capacitor voltage as a state variable is governed by:

$$C\frac{dv_{cap,n}}{dt} = \sum_{k=1}^{K}(i_{n,k}g_{n,k}) \tag{2.15}$$

Being fundamental components of individual interleaved currents equal among themselves (this is naturally true if the interleaved currents within a submodule are balanced) and taking into account Equations (2.11), Equation (2.15) can be simplified to:

$$C\frac{dv_{cap,n|u,l}}{dt} \approx \underbrace{i_{u,l}\frac{1}{K}}_{i_{n,k|u,l}} \sum_{k=1}^{K} g_{n,k|u,l} = i_{u,l}u_{n|u,l} \tag{2.16}$$

Summation over all N capacitors in the arm and bearing in mind that the arm current is the same for all the submodules yields

$$\underbrace{C\sum_{n=1}^{N}\frac{dv_{cap,n|u,l}}{dt}}_{dv^{\Sigma}_{cap|u,l}/dt} = i_{u,l}\underbrace{\sum_{n=1}^{N}u_{n|u,l}}_{Nu_{u,l}} \tag{2.17}$$

Combining Equations (2.17) and (2.5), the following relations can be obtained

$$\frac{C}{N}\frac{dv^{\Sigma}_{cap|u}}{dt} = u_u\left[\frac{i}{2}+i_{cir}\right], \quad \frac{C}{N}\frac{dv^{\Sigma}_{cap|l}}{dt} = u_l\left[-\frac{i}{2}+i_{cir}\right] \tag{2.18}$$

Equations (2.14) and (2.18) comprise the averaged dynamic model of the ISM-MMC being identical to the averaged model of a classical MMC [71]. In fact, as it will be shown later, only few modifications are required to be introduced into submodule energy balancing scheme of ISM-MMC in comparison with standard MMC control method. This characteristic makes ISM-MMC solution very attractive for retrofitting already built MMCs when higher power capacity of the new converter is required. In addition to that by taking advantage of a proper modulation for driving interleaved HB-legs of each SM, the output characteristics of the converter can be significantly improved.

2.4 Control Methods

One may notice from derived average models of ISM-MMC that it is equivalent to the one of classical MMC with HB submodules. Therefore, strictly speaking, arm voltage references as control variables can be regulated in a similar manner as it is made for classical MMCs. Literature discusses the functionality of classical control methods for the standard MMC topology in great detail. For example, [71], [72] describe the operating and control principle very clearly. Nevertheless, this section refreshes some control methods in relation with the ISM-MMC structure working in the rectification mode (ac/dc). It should be pointed out though that ISM-MMC naturally supports bidirectional power flow. Therefore, inversion mode (dc/ac) is also possible, although it is not covered in this work. Control methods in the section are discussed in relation to a three-phase ISM-MMC, since most of the high-power applications are three-phase based. Thus, Subsections 2.4.2 and 2.4.3 refer to control design in three-phase form with necessary variable transformations. The other subsections are presented in per-phase structure.

Figure 2.3 depicts a block diagram with the high-level control method of ISM-MMC, framed by red dashed line. The latter one resembles the classical MMC control scheme. It includes the phase-locked loop (PLL), which is used for grid synchronization, dc-bus voltage control, circulating current control and arm-energy control. Each one of these blocks is explained in the

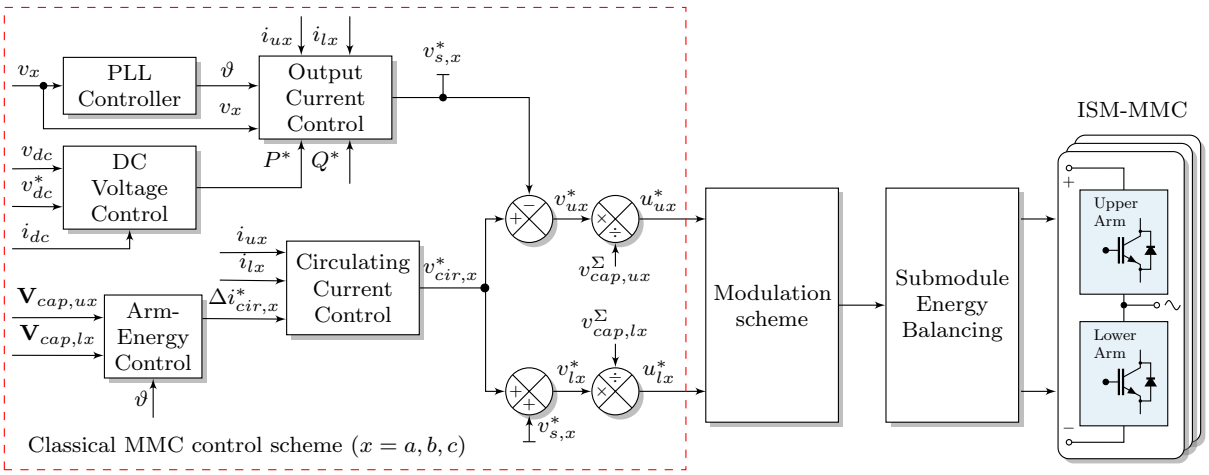

Figure 2.3 – Block diagram of the implemented high-level control method for ISM-MMC [144]. © 2022 IEEE

following subsections. Independent sections of the chapter are dedicated to the modulation strategy and submodule energy balancing method. Therefore, they are not covered in the current section.

The proposed ISM-MMC has primary and secondary control objectives, in the same manner as the classical MMC. The submodule energy balancing, and output current control are the primary objectives that directly relate to the operation of ISM-MMC. At the same time, the circulating current control is a secondary objective and associated with size, reliability, and efficiency of a converter. Unlike standard MMC, the ISM-MMC has an additional secondary control objective that deals with equal current sharing among interleaved HB-legs in each SM. This problem becomes quite challenging with an increase of both series connected submodules and interleaved HB-legs. In addition to that, current balancing within a SM in MMC structures is a new control task that has not been addressed yet. Therefore, this subject is discussed separately and scrupulously in Chapter 3. In fact, the current balancing of the interleaved legs is a decoupled control task that is associated with performance of a single submodule and with acceptable level of currents imbalance it does not affect the operational behavior of the whole converter (the output characteristics remain unchanged). This argument is supported by the results of performed HIL simulations in Section 2.9. However, it should be noted that the obvious drawback of such unsupervised SM currents operation is a need in oversizing SMs' components. All these aspects are addressed in Chapter 3.

2.4.1 Dc Voltage Control

Constant dc voltage, which is the objective of dc voltage regulator, means that the mean values of arm currents form dc current in steady state. In other words, oscillations and transients in the dc-link voltage can be provoked by residual ac components and transients between dc current and sum of arm currents. The effective dc-bus dynamics including submodule capacitors has been already derived in [71, 151]. Therefore, since the average models of classical MMC with

HB submodules and ISM-MMC are identical, the derivation process of dc-bus dynamics here is omitted. Instead, it is given in the final form:

$$\underbrace{\left(C_{dc}+\frac{2MC}{N}\right)}_{C'_{dc}}\frac{dv_{dc}}{dt}=i_{dc}-\frac{P}{v_{dc}} \tag{2.19}$$

being C and C_{dc} total capacitance of submodule's and converter's dc-link, respectively. Term C'_{dc} denotes effective dc-link capacitance. It is larger than C_{dc}, due to contribution from the submodule capacitors. Parameters M and N represent, correspondingly, number of converter's phases and number of submodules in each arm of the converter. Variables v_{dc} and i_{dc} are instantaneous values of dc-bus voltage and current, respectively. Finally, variable P is the mean active ac-side power of the converter.

Multiplying both sides of Equation (2.19) by v_{dc} and recalling rules for obtaining derivatives of powers leads to

$$\underbrace{\frac{C'_{dc}}{2}\frac{dv_{dc}^2}{dt}}_{dW_{dc}/dt}=\underbrace{v_{dc}i_{dc}}_{P_{dc}}-P \tag{2.20}$$

where W_{dc} is the effective stored dc-bus energy and P_{dc} is the active dc-side power. Traditionally, simple PI controllers are used for dc voltage reference tracking. Output of a PI controller with reference to effective dc-bus energy error can be expressed as

$$P^*_{fb}=\alpha_{p,dc}\left(1+\frac{\alpha_{i,dc}}{s}\right)(W_{dc}-W^*_{dc}) \tag{2.21}$$

By combining Equations (2.20) and (2.21) with the assumption $P=P^*_{fb}$, the following closed-loop system can be obtained:

$$W_{dc}=\frac{\alpha_{p,dc}(s+\alpha_{i,dc})}{s^2+\alpha_{p,dc}s+\alpha_{p,dc}\alpha_{i,dc}}W^*_{dc}+\frac{s}{s^2+\alpha_{p,dc}s+\alpha_{p,dc}\alpha_{i,dc}}P_{dc} \tag{2.22}$$

With $\alpha_{i,dc}>0$, the transfer function from P_{dc} to W_{dc} has zero static gain, thus, the energy difference $W_{dc}-W^*_{dc}$ will be eliminated regardless of P_{dc}. According to [71] the controller bandwidth can be selected as follows

$$\alpha_{i,dc}<\frac{\alpha_{p,dc}}{2},\quad \alpha_{p,dc}<\omega \tag{2.23}$$

being ω the fundamental angular frequency.

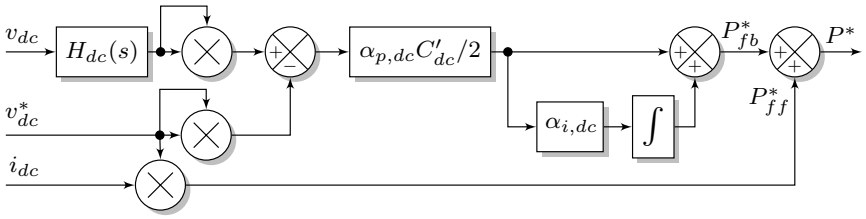

Figure 2.4 – Block diagram of the dc-link voltage controller [71]

A block diagram of the implemented dc-bus voltage controller is depicted in Figure 2.4. In addition to what already has been described, there are two aspects that must be commented. The first one relates to a $H_{dc}(s)$ filter that has been added to the path of measured dc voltage (v_{dc}).

Its purpose to suppress high-frequency ripple and other disturbances. Its bandwidth must not be selected below $\alpha_{p,dc}$, since this would worsen the performance of closed-loop dc-bus voltage dynamics. An appropriate choice would be a second-order Butterworth low-pass or simple moving-average filter. The second aspect concerns the feedforward path (P^*_{ff}) that has been implemented to speed up the convergence of v_{dc} to a steady state value. It requires measurement of the dc-bus current.

2.4.2 Phase-Locked Loop

Many grid synchronization techniques have been developed and proposed in the literature for single-phase [152–155] and three-phase systems [156–159]. Phase-locked loops (PLLs) [153, 157] and frequency-locked loops (FLLs) [154, 158] are two main categories of closed-loop synchronization techniques that are used in power applications. In this work a popular strategy based on a phase-locked loop has been used. In the following discussions when the grid synchronization is mentioned the PLL-based method is considered by default. The PLL is a closed-loop control system that locks its output to the system input with a constant phase error (ideally zero). The PLL provides continuous information about the phase angle and magnitude of the variable of interest (typically, fundamental grid voltage), which are used in many parts of the control scheme. All PLLs, regardless of their differences, consist of three parts, namely phase detector (PD), loop filter (LF) and voltage-controlled oscillator (VCO):

- The **phase detector** generates a phase error signal, in other words, a signal that contains the error between real and estimated phases. Depending on the type of PD that has been used, ac high-frequency components appear along with the dc phase-angle error signal.
- The **loop filter** is a low-pass filter, which is mainly responsible for suppressing ac high-frequency disturbances from the PD output. The dynamic response, tracking characteristics, and stability properties of the PLL are mainly dictated by the LF [153]. Typically, this block is formed by a first-order low-pass filter or a PI controller.
- The **voltage-controlled oscillator** is responsible for generating the synchronized signal with the PLL input.

Several methods can be used to implement each of the aforementioned blocks forming a PLL. A detailed examination of these blocks falls out the scope of this work, instead this subsection provides a necessary description of the PLL method that has been used for ISM-MMC – grid synchronization. Commonly, in literature, this method is labeled as dual second order generalized integrator PLL (DSOGI-PLL). The structure of implemented DSOGI-PLL is presented in Figure 2.5.

The PD of the PLL module (cf. Figure 2.5) is based on a set of two quadrature signal generators (QSGs) for the α and β components of the input vector. An adaptive filter based on second order generalized integrator (SOGI) is applied to the input of phase detector. Joined QSG block with the SOGI-based adaptive filtering is named as second-order generalized integrator QSG (SOGI-QSG). The filtering characteristic of SOGI-QSG attenuates effect of distorting high-order harmonics from the input to output. According to [156] the gain of SOGI-QSG can be set to $k_{pll} = \sqrt{2}$. The output direct v'_α, v'_β and in-quadrature signals qv'_α, qv'_β are inputs of a positive-/negative-sequence calculation unit (PNSC), which computes the sequence components on the $\alpha\beta$ reference frame. Matices $T_{\alpha\beta}$ and T_{dq} are the operators of Clarke's and Park's transformations, respectively. The PLL block is built in synchronous reference frame (SRF) by using positive sequence signals ($\mathbf{V}'^{+}_{dq}$) and labeled in Figure 2.5 as SRF-PLL. The loop filter is formed by a

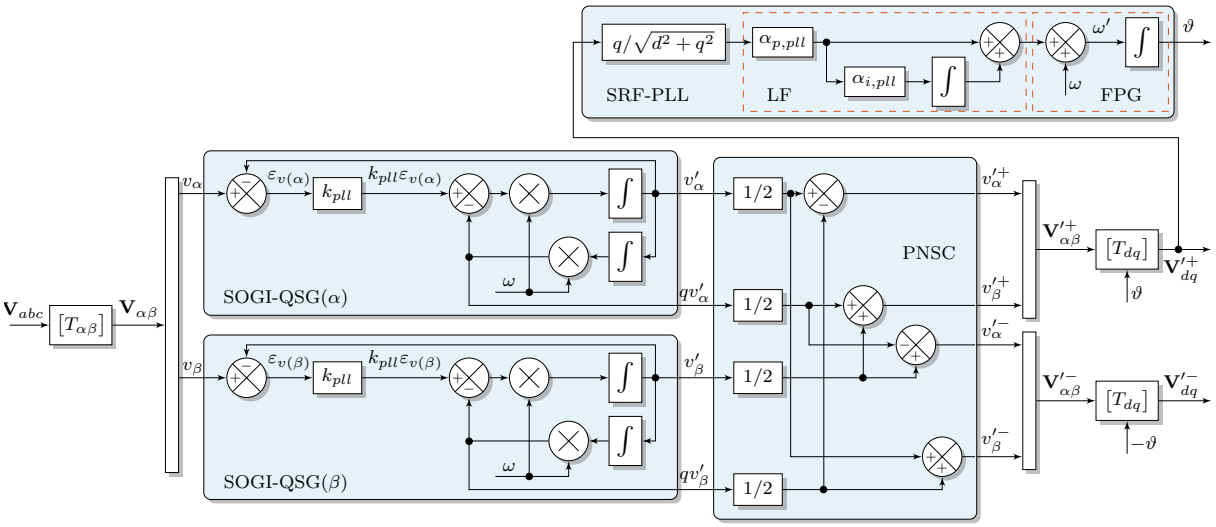

Figure 2.5 – Block diagram of the DSOGI-PLL [156]

PI controller with proportional control-loop bandwidth $\alpha_{p,pll}$ and integrator bandwidth $\alpha_{i,pll}$. Reference [152] provides a detailed description on the PI controller parameters tuning. Therefore, in the following sections these parameters will be given for the specific design examples with reference to [152]. The VCO in SRF-PLL block has been removed and a new sub-block called the frequency/phase-angle generator (FPG) has been added to provide the phase-angle for the sinusoidal functions of the Park transformation. All in all, the implemented DSOGI-PLL generates accurate grid voltage phase ϑ along with positive ($\mathbf{V}'^{+}_{dq}$) and negative ($\mathbf{V}'^{-}_{dq}$) sequence components of the grid voltage in synchronous reference frame. The voltage components are useful for current reference generation (cf. Section 2.4.3) under grid voltage unbalanced conditions. Study of ISM-MMC's operation behaviour under grid unbalanced conditions is outside the work's scope. Operation with balanced grid (balanced phase voltages and currents) is considered only.

2.4.3 Output Current Control

As it was mentioned in Chapter 1, the proposed modular multilevel converter can be used in wide range of high-power applications including traditional MMC applications such as, high-voltage direct current (HVDC) transmissions, static synchronous compensators (STATCOMs), medium-voltage (MV) motor drives [15, 16, 33, 85] and those which have not been considered before suitable for MMCs such as, low-voltage, ultra-fast electrical vehicles (EV) battery charging, dc traction power supplies, large scale hydrogen electrolyzers (HE) [146]. Each application requires different output current control techniques. For instance, voltage-oriented control (VOC) is typically used in EV battery charging applications, dc traction power supplies or HVDC, whereas field-oriented control (FOC) or direct torque control (DTC) is usually designed for MV motor drives. The aforementioned control methods can be realized in stationary abc, $\alpha\beta$ or synchronous dq reference frames. This section provides fundamental details of the VOC-based output current control loop implemented in stationary $\alpha\beta$ reference frame.

Figure 2.6 illustrates the structure of implemented output current control loop. It consists of two main blocks, namely current reference generator and output-current control loop. The aim of the first block can be understood from its name, which is to generate current reference for the subsequent feedback control actions, given power references (both active and reactive).

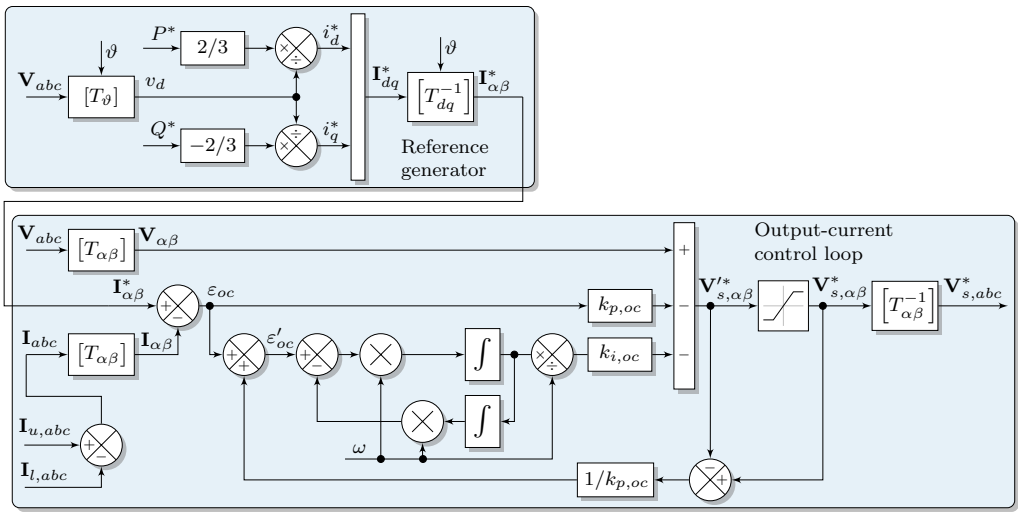

Figure 2.6 – Block diagram of the output current control

Active power reference can be obtained as the output of dc-link voltage control loop, depicted in Figure 2.4. Reactive power reference can be attained based on the desirable power factor (typically in the grid-connected applications a unity power factor is required, $Q^* = 0$). Having ideal grid conditions (i.e., the grid voltage is not affected by either harmonic distortion or unbalances), the input three-phase voltage vector ($\mathbf{V}_{abc}$) from stationary *abc* reference frame can be translated to the *dq* rotating reference frame by using Park's transformation $[T_\vartheta]$.

$$[T_\vartheta] = [T_{dq}][T_{\alpha\beta}] = \frac{2}{3}\begin{bmatrix} cos\vartheta & cos(\vartheta - \frac{2\pi}{3}) & cos(\vartheta + \frac{2\pi}{3}) \\ -sin\vartheta & -sin(\vartheta - \frac{2\pi}{3}) & -sin(\vartheta + \frac{2\pi}{3}) \end{bmatrix} \tag{2.24}$$

$$[T_{dq}] = \begin{bmatrix} cos\vartheta & sin\vartheta \\ -sin\vartheta & cos\vartheta \end{bmatrix}, \quad [T_{\alpha\beta}] = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \tag{2.25}$$

From (2.24), the $[T_\vartheta]$ transformation has been rescaled by using a $2/3$ factor in order to detect the amplitude of the sinusoidal input signal. Therefore, in the steady state, the *d* component (v_d) resembles the amplitude of the sinusoidal positive-sequence input voltage ($v_d'^+$) that can be obtained by DSOGI-PLL block (cf. Figure 2.5).

The active and reactive power produced/consumed by the grid converter can be calculated by

$$P = \frac{3}{2}(v_d i_d + v_q i_q), \quad Q = \frac{3}{2}(v_q i_d - v_d i_q) \tag{2.26}$$

Assuming that the *d* axis is perfectly aligned with the grid voltage (i.e., $v_q = 0$), the active power ($P^* = P$) and the reactive power ($Q^* = Q$) references will therefore be proportional to reference currents i_d^* and i_q^* respectively:

$$i_d^* = \frac{2P^*}{3v_d}, \quad i_q^* = -\frac{2Q^*}{3v_d} \tag{2.27}$$

Multiplying the *dq* reference current vector ($\mathbf{I}_{dq}^*$) by reverse matrix operator $[T_{dq}^{-1}]$, the $\alpha\beta$ reference current vector ($\mathbf{I}_{\alpha\beta}^*$) can be obtained. Here the job of the reference generator block is done. The next step is to apply this current reference in the feedback path of the output-current control loop (cf. Figure 2.6).

In [71] several sections are dedicated to output-current controller design. This method is applied in the current work. Therefore, here only necessary comments will be made, while the detailed description of the derived control concept can be found in [71]. The control loop is based on the first expression in the set of Equations (2.14):

$$\frac{L_{arm}}{2}\frac{di}{dt} = v_s - v - \frac{R_{arm}}{2}i \implies i = \frac{2}{sL_{arm} + R_{arm}}(v_s - v) \tag{2.28}$$

and includes proportional-resonant (PR) feedback controller and feedforward path. The entire control block is built in stationary $\alpha\beta$ reference frame, therefore, the input measured quantities, such as grid phase voltages ($\mathbf{V}_{abc}$) and currents ($\mathbf{I}_{abc}$, computed with help of Equation (2.4), given vectors $\mathbf{I}_{u,abc}$ and $\mathbf{I}_{l,abc}$) must be translated into $\alpha\beta$ reference frame ($\mathbf{V}_{\alpha\beta}$ and $\mathbf{I}_{\alpha\beta}$, respectively). This operation is done by the transform matrix $[T_{\alpha\beta}]$. The control law, thus, can be formulated as follows

$$\mathbf{V}'^{*}_{s,\alpha\beta} = \mathbf{V}_{\alpha\beta} - k_{p,oc}\varepsilon_{oc} - \frac{k_{i,oc}s}{s^2 + \omega^2}\varepsilon_{oc}, \quad \varepsilon_{oc} = \mathbf{I}^{*}_{\alpha\beta} - \mathbf{I}_{\alpha\beta} \tag{2.29}$$

where $k_{p,oc}$ and $k_{i,oc}$ are proportional and resonant gains of the PR controller. Term ε_{oc} represents current error. The minus sings in (2.29) indicate that the converter works in rectification mode. The PR controller gains can be selected as suggested in [71]:

$$k_{p,oc} = \frac{\alpha_{c,oc}L}{2}, \quad k_{i,oc} = 2\alpha_{r,oc}k_{p,oc} = \alpha_{r,oc}\alpha_{c,oc}L, \quad \alpha_{r,oc} \ll \alpha_{c,oc} \tag{2.30}$$

where $\alpha_{c,oc}$ and $\alpha_{r,oc}$ are the desired closed-loop and resonant bandwidth that associate with output current controller, respectively.

The voltage reference ($\mathbf{V}'^{*}_{s,\alpha\beta}$) computed by Equation (2.29) is an ideal value that needs to be bounded by the range $[-V_{dc}/2, V_{dc}/2]$. Therefore, a saturation block is introduced into the path. A windup effect may occur in resonant path due to the saturation block. It introduces a non-linearity in the control loop that makes the control error larger than in the unsaturated situation. There are several possible ways to prevent windup. In this work, method, known as *back calculation* has been applied. The *back calculation* results in a modified control error (ε'_{oc}), which can be computed by:

$$\varepsilon'_{oc} = \varepsilon_{oc} + \frac{1}{k_{p,oc}}(\mathbf{V}^{*}_{s,\alpha\beta} - \mathbf{V}'^{*}_{s,\alpha\beta}) \tag{2.31}$$

The modified control error (ε'_{oc}) is used as the input signal to the resonant part (cf. Figure 2.6), effectively preventing the windup effect. The last operation in the control loop is the back transform of voltage reference $\mathbf{V}^{*}_{s,\alpha\beta}$ into stationary *abc* reference frame ($\mathbf{V}^{*}_{s,abc}$) by reverse matrix operator $[T^{-1}_{\alpha\beta}]$.

2.4.4 Circulating Current Control

Circulating current is a major issue in classical MMCs related to the performance and stability of the converters. Converter's leg-common mode current can be decomposed into two main components, namely purely dc ($\bar{i}_{cir}$, cf. Equation (2.7)) and ac (Δi_{cir}) parts, typically referred as circulating current. The circulating current originates from the voltage difference between the upper and lower arms of the converter leg or/and between the phase converters' legs. It consists of low- and high-frequency (switching harmonics) parts with the dominant element as negative sequence component at twice the fundamental frequency. Circulating currents from converters' phase legs do not enter the dc link (they sum up to zero), nor are they visible from the

ac terminals, it can be said that they circulate inside of the converter. Nevertheless, circulating currents cause an increase of the peak/rms value of the arm currents (cf. Equation (2.5)). As a result, the current ratings of the converter components must be extended. Furthermore, power losses, and ripple in submodule capacitor voltages increase as well [15, 42]. According to Equation (2.7), to keep the converter losses and the rms arm currents at a minimum, it is desirable that the converter's leg-common mode current i_{cir} should be pure dc. Several active methods have been proposed in literature to reduce the circulating current. For instance, authors in [151] use an active resistance (proportional controller) to control circulating current, which includes an estimate of the arm resistance. Implementing the double fundamental frequency $abc - dq$ transformation, reference [160] proposes to eliminate the circulating currents by controlling their dq components with a pair of PI controllers. Alternatively, resonant regulators are employed to control the circulating currents in the stationary abc frame. References [161–163] target the elimination of the ac components of the leg-common mode currents through a PR controller. In this approach, the PR regulators are designed to eliminate the specific harmonic frequency components such as second- and fourth-order harmonics from the circulating current. Another paper [164] proposes a control method based on weighted model predictive control (MPC) with a normalized cost function to select the converter switching patterns, which control the load current, while minimizing voltage fluctuation and circulating current. Although the main control strategy regarding circulating currents is to suppress them completely, it has been recently proven that the injection of a specific circulating current can be used to reduce losses [165] and also capacitor voltage ripples [166].

Section 2.3 provides fundamental aspects of the newly introduced ISM-MMC topology, clearly demonstrating that the average models of ISM-MMC and classical MMC with HB submodules are matching. Thus, circulating current issue in ISM-MMCs can be addressed in a similar way as for the MMC. This work does not aim to develop a new strategy for suppressing circulating currents in ISM-MMCs, therefore a commonly applied method in classical MMC structures based on PR regulator is taken as a design reference. This circulating current control loop is adapted to suit the voltage control scheme presented in Figure 2.3 and it is implemented in the stationary abc frame. The circulating-current dynamics can be explained based on the second expression of Equation (2.14):

$$L_{arm}\frac{di_{cir}}{dt} = \frac{v_{dc}}{2} - v_{cir} - R_{arm}i_{cir} \implies i_{cir} = \frac{1}{sL_{arm} + R_{arm}}\left[\frac{v_{dc}}{2} - v_{cir}\right] \tag{2.32}$$

Internal voltage v_{cir} can be represented as its time delayed reference v^*_{cir} and an additive parasitic component Δv_{cir}. The latter comprises switching harmonics and negative sequence component at twice the fundamental frequency. To suppress the double fundamental frequency harmonic a resonant term is incorporated into the circulating current regulator. On top of it, a feedforward term $V_{dc}/2 - R_{arm}i^*_{cir}$ can be included into the control law to compensate for the resistive voltage drop and term $V_{dc}/2$ in Equation (2.32). As a result, the following control law is obtained

$$v^*_{cir} = \frac{V_{dc}}{2} - R_{arm}i^*_{cir} - R_{cir}\left[1 + \frac{k_{i,cir}s}{s^2 + (2\omega)^2}\right](i^*_{cir} - i_{cir}) \tag{2.33}$$

where R_{cir} represents a proportional gain and it commonly referred in literature as an "active resistance" or "virtual resistance" [71, 151]. The reference i^*_{cir} can be derived as sum of desired dc value (cf. Equation (2.7)) and an additive component Δi^*_{cir}.

$$i^*_{cir} = \underbrace{\frac{I_{dc}}{M}}_{\bar{i}_{cir}} + \Delta i^*_{cir} \tag{2.34}$$

The current reference increment (Δi^*_{cir}) arises from action of arm-energy control and it is discussed in Subsection 2.4.5. The desired value of converter's leg-common mode current $\bar{i}_{cir}$ can be extracted from indirectly measured value of i_{cir} (cf. Equation (2.4)) by applying a Butterworth second-order low-pass filter (LPF). Figure 2.7 depicts a block diagram of entire circulating current control loop.

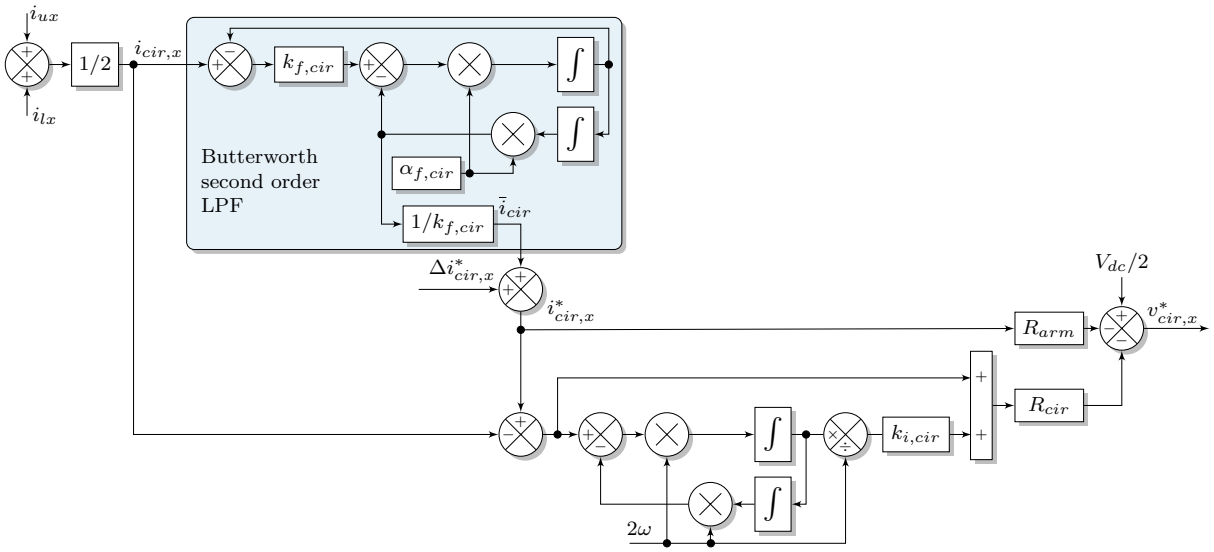

Figure 2.7 – Block diagram of the circulating current control

The circulating current regulator must be tuned in a way to provide decent rejection of the parasitic component Δv_{cir} and for reducing the time constant of arm RL circuit (from L_{arm}/R_{arm} to $L_{arm}/(R_{arm}+R_{cir})$], however it should not be faster than the output current controller.

$$R_{arm} \ll R_{cir} \leq k_{p,oc} \tag{2.35}$$

where $k_{p,oc}$ is the proportional gain of the output current controller. The resonant gain $k_{i,cir}$ can be selected based on the bandwidth of resonant path:

$$k_{i,cir} = 2\alpha_{2,cir}, \quad \alpha_{2,cir} < \omega \tag{2.36}$$

2.4.5 Arm-Energy Control

The employment of distributed floating capacitors in the MMC structures results in high complexity of internal dynamics (dynamics between SMs of the same arm, upper and lower arms of the same converter's leg, and different phase legs). Such a converter is particularly hard to stabilize over the wide range of operating modes. The topic of active arm/leg capacitor voltage control, and arm/leg energy control, considering both normal and abnormal cases has been

broadly investigated in literature [71, 151, 167–172]. Early investigations of MMC structures identified the importance of controlling the converter's internally stored capacitive energy for stable operation [151, 169, 172]. The total energy stored inside the MMC can be controlled from either dc or ac side, depending on the operating mode (inverter/rectifier). Nevertheless, for ensuring equal average energy distribution among all arms, the MMC control method should guarantee the energy equalization between the phase legs, referred as horizontal balancing, and the balancing of the energy between the upper and lower arms in each phase, referred as vertical balancing. Apart from securing equal energy distribution among the converters' arms, the control algorithm must ensure equal distribution of energy among the SMs within the same arm [167, 171]. Dedicated control methods are designed to deal with this problem and they commonly referred in literature as submodule energy control. This subject is discussed in a separate Section 2.6, hence is not covered in the current subsection. Henceforward, the term arm-energy balancing denotes the arm/leg energy transfers, while assuming uniform energy distribution among the SMs of one arm. References [71, 151, 167, 169] provide comprehensive analysis of the internal energy dynamics of the classical MMC with HB submodules and suggest effective control strategies. The structural changes performed on the standard MMC to derive ISM-MMC architecture do not affect the internal energy distribution, due to the fact that interleaved submodules employ a unique, shared floating capacitor in the similar manner as it is implemented in the typical HB-based SM. Therefore, control methods designed for the classical MMC can be equally employed for ISM-MMC. Current work does not aim to go in depth of the existing arm-energy control methods nor introduce a new one, hence, a typical closed-loop energy balancing scheme [71] is used to regulate energy transfer inside of the proposed ISM-MMC. It is achieved through the so-called arm-differential (Δ) and arm-sum (Σ) energy control mechanisms. Considerations of arm-energy balancing given unbalanced or abnormal ISM-MMC operations fall out of the work's scope.

Given the ac phase ($v^*_{s,x}$) and internal ($v^*_{cir,x}$) voltage references and in the accordance with the underbraced expressions in Equation (2.14), the reference modulating signals (insertion indexes per arm) can be formulated as:

$$u^*_{ux} = \frac{v^*_{cir,x} - v^*_{s,x}}{v^{\Sigma}_{cap|ux}}, \quad u^*_{lx} = \frac{v^*_{cir,x} + v^*_{s,x}}{v^{\Sigma}_{cap|lx}} \tag{2.37}$$

By substituting Equation (2.37) into Equation (2.18) and dropping the phase label x, the steady-state sum-capacitor-voltage ripples per phase can be calculated by:

$$\frac{C}{N}\frac{dv^{\Sigma}_{cap|u}}{dt} = \frac{v^*_{cir} - v^*_s}{v^{\Sigma}_{cap|u}}\left[\frac{i}{2} + i_{cir}\right], \quad \frac{C}{N}\frac{dv^{\Sigma}_{cap|l}}{dt} = \frac{v^*_{cir} + v^*_s}{v^{\Sigma}_{cap|l}}\left[-\frac{i}{2} + i_{cir}\right] \tag{2.38}$$

By multiply both sides of these two relations respectively by $v^{\Sigma}_{cap|u}$ and $v^{\Sigma}_{cap|l}$, while bearing in mind the derivative rule for a power function, Equation (2.38) can be transformed into:

$$\underbrace{\frac{C}{2N}\frac{d(v^{\Sigma}_{cap|u})^2}{dt}}_{dW_u/dt} = (v^*_{cir} - v^*_s)\left[\frac{i}{2} + i_{cir}\right], \quad \underbrace{\frac{C}{2N}\frac{d(v^{\Sigma}_{cap|l})^2}{dt}}_{dW_l/dt} = (v^*_{cir} + v^*_s)\left[-\frac{i}{2} + i_{cir}\right] \tag{2.39}$$

The left-hand side of expressions in Equation (2.39) represent time derivative of total stored upper (W_u) and lower (W_l) arm energy. Having the total per phase energy (W_Σ) and imbalance energy (W_Δ) defined as:

$$W_\Sigma = W_u + W_l, \quad W_\Delta = W_u - W_l \tag{2.40}$$

Equation (2.39) can be further simplified, leading to the following form:

$$\frac{dW_\Sigma}{dt} = 2v^*_{cir}i_{cir} - v^*_s i, \quad \frac{dW_\Delta}{dt} = v^*_{cir}i - 2v^*_s i_{cir} \tag{2.41}$$

Some assumptions can be made at this stage, namely $v^*_{cir} = V_{dc}/2$ (fairly enough since $v_{cir} \approx V_{dc}/2$) and the leg's common-mode current i_{cir} are assumed to be pure dc ($i_{cir} = I_{dc}/M = P_{dc}/(MV_{dc})$), while phase voltage reference v^*_s and phase current i can be treated as pure sinusoids, given by

$$v^*_s = \sqrt{2}V_s cos\vartheta, \quad i = \sqrt{2}Icos(\vartheta - \varphi) \tag{2.42}$$

where V_s and I are rms values of converter's phase voltage and current. Angles ϑ and φ represent respectively fundamental grid voltage angle and current phase angle (lagging) relative to the voltage. Given the assumptions and in accordance with Equation (2.41), the dc component of the leg's common-mode current affects the total energy (Σ) stored within a leg. Hence, it deals energy balancing in horizontal direction. Instead, the ac component of the leg's common-mode current affects the energy difference (Δ) between two arms of the same leg. Thus, it is responsible for the vertical balancing. Introducing aforementioned assumptions into Equation (2.41) and integrating it over fundamental period, yields

$$\begin{aligned} W_\Sigma &= W^*_\Sigma - \underbrace{\frac{V_s I}{2\omega} sin(2\vartheta - \varphi)}_{\Delta W_\Sigma} \\ W_\Delta &= W^*_\Delta - \underbrace{\left[\frac{2\sqrt{2}V_s P_{dc}}{MV_{dc}\omega} sin\vartheta - \frac{\sqrt{2}V_{dc}I}{2\omega} sin(\vartheta - \varphi)\right]}_{\Delta W_\Delta} \end{aligned} \tag{2.43}$$

where W^*_Σ and W^*_Δ are the integration constants, which are represented by

$$W^*_\Sigma = \frac{CV^2_{dc}}{N}, \quad W^*_\Delta = 0 \tag{2.44}$$

By regulating the average values of W_Σ and W_Δ to W^*_Σ and W^*_Δ, respectively, brings the mean values of $v^\Sigma_{cap|u}$ and $v^\Sigma_{cap|l}$ to the desired voltage V_{dc}. To achieve that an increment of reference circulating current ($\Delta i^*_{cir,x}$) needs to be generated and added to the circulating current controller scheme (cf. Figure 2.7).

$$\Delta i^*_{cir,x} = k_\Sigma(W^*_\Sigma - \underbrace{\frac{(2\omega)^2}{s^2 + \alpha_{f2,W}s + (2\omega)^2}}_{H_{2,W}(s)} \Delta W_\Sigma) + k_\Delta(W^*_\Delta - \underbrace{\frac{\omega^2}{s^2 + \alpha_{f1,W}s + \omega^2}}_{H_{1,W}(s)} \Delta W_\Delta)cos\vartheta_x \tag{2.45}$$

where low-pass filters $H_{1,W}(s)$ and $H_{2,W}(s)$ are required to suppress the arm-energy ripples and should have bandwidths $\alpha_{f1,W} < \omega$ and $\alpha_{f2,W} < 2\omega$, respectively [71]. The $cos\vartheta_x$ term induces a fundamental frequency oscillation, generating an ac pulse in i_{cir} for a nonzero W_Δ. Control gains for the total energy path k_Σ and for the difference energy path k_Δ can be calculated by:

$$k_\Sigma = \frac{\alpha_W}{V_{dc}}, \quad k_\Delta = \frac{\alpha_W}{\sqrt{2}V}, \quad \alpha_W < \omega \tag{2.46}$$

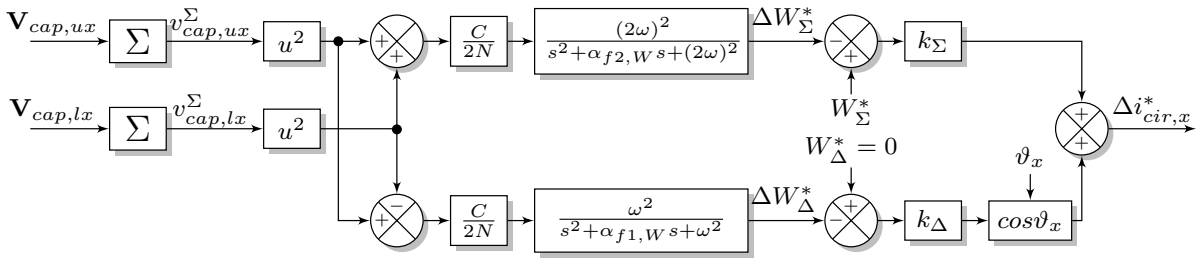

Figure 2.8 – Block diagram of the arm-energy control

Figure 2.8 depicts entire arm-energy control scheme. It should be mentioned though, that in single-phase ISM-MMC implementations of current work the direct control scheme has been employed [71]. This type of control assumes that arm sum-capacitor voltages $v^{\Sigma}_{cap|u}$ and $v^{\Sigma}_{cap|l}$ equal to mean dc voltage V_{dc} and an increment of reference circulating current given by arm-energy balancing equal to zero, hence substituting the corresponding terms in the ISM-MMC control scheme (cf. Figure 2.3). This is motivated by the fact that the total energy (Σ) control path in the arm-energy control (cf. Figure 2.8), working with energy regulation in horizontal direction cannot be implemented, while actions of the difference energy (Δ) regulator can be sufficiently substituted by operation of the circulating current control (cf. Subsection 2.4.4). These facts significantly reduce control complexity of the single-phase ISM-MMC.

2.5 Modulation Scheme

There are generally two fundamental issues to be dealt with while selecting an appropriate modulation strategy for the standard MMC converter. Namely, the modulation of output voltages and balancing of the submodule capacitor energies within each converter arms [173]. Many modulation schemes have been adopted to MMC based topologies. Among them the most widely employed modulation techniques can be categorized as multilevel carrier-based PWM techniques with either level-shifted (LS-PWM) or phase-shifted (PS-PWM) carriers [174, 175], staircase waveform modulations [176, 177], and space vector modulation (SVM) [178–180].

Staircase modulation methods feature fundamental switching frequency, reduced switching losses and simple realization, however it comes with the price of increased harmonic distortion of the output voltage and current waveforms. The quality of output waveforms can be improved by increasing the number of submodules, which is the case for an MMC-based high voltage applications. These staircase methods mainly include selective harmonic elimination (SHE) scheme and nearest level modulation (NLC). The NLC approach is computationally less complex, however its performance is significantly affected by the sorting algorithm and sampling frequency, especially when the number of submodules is low [177]. The SHE scheme requires off-line computation of a large number of switching angles, which increase the computational complexity with the growth of the number of voltage levels.

The SVM directly controls the line-to-line voltages of a modular multilevel converter and allows generating the phase voltages implicitly. In this way SVM eliminates the influence of common-mode voltages and provides more flexibility (i.e., redundant switching sequences) to optimize switching pattern [179]. Nevertheless, the SVM method is difficult to implement for a converter from the MMC family with many voltage levels due to high computational burden.

On the other hand, carrier-based modulation schemes are widely applied to control multilevel power converters due to their simple implementation and ease of extension to higher number of voltage levels. In PS-PWM, the triangular carriers with an identical magnitude are horizontally biased, while in LS-PWM they are disposed vertically. The LS-PWM can be further classified based on the phase relationship between the adjacent carriers into phase disposition (PD), phase opposition disposition (POD), alternate phase opposition disposition (APOD) and other hybrid schemes. The carrier-based modulations usually fall into the high switching frequency category, therefore, have higher switching losses in comparison with staircase modulation schemes. Moreover, an accurate synchronization between the carriers is essential to generate high-quality voltage and current waveforms [175]. To circumvent the aforementioned synchronization problem in controlling the MMC having a large number of SMs, a simple pulse width modulator using a single triangular carrier is proposed in [88].

Similarly, the interleaving modulation methods have been well-reported in literature as well. Most of the attention in this regard has been drawn to a phase-shift in the operation of the parallel branches, generally achieved through PS-PWM [109] or SVM [111]. Another trending modulation strategy to handle interleaving in VSCs is the LS-PWM [92, 115].

To drive the proposed ISM-MMC, a hybrid modulation scheme is implemented in [144, 146]. This modulation method has been already applied in modular multi-cell structures, e.g. in [181]. It is composed of LS-PWM for synthesizing voltage levels given by series connected SMs (N carrier levels per arm) whether PS-PWM scheme handles interleaving of parallel HB-legs within each SM (K evenly phase-shifted carriers at each level-shifted level). Therefore, in total, this method employs NK carriers per arm. Technically, different sets of NK carriers can be applied to the converters' arms to realize distinct modulations, as for example, anti-phase displacement between upper and lower arm carrier sets [182]. However, this topic falls out the scope of the current work. Hence, in further discussions a unique set of carriers is applied to the converters' arms. Figure 2.9 depicts an example of the PD-based (carriers) hybrid modulation scheme for the case of $N = 2$ and $K = 3$.

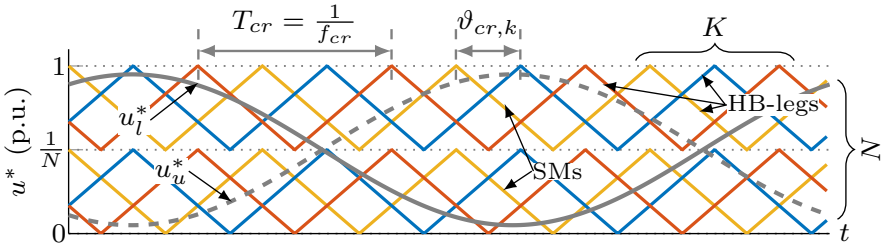

Figure 2.9 – Example of the PD-based hybrid modulation scheme for the case of $N = 2$ and $K = 3$ [146]. © 2021 IEEE

Some fundamental definitions can be derived from this figure. The first is the carrier period (T_{cr}), which is inversely proportional to the carrier frequency f_{cr}. The carrier phase shifts of the different carriers within a carrier level can thus be formulated as

$$\vartheta_{cr,k} = 2\pi\frac{k-1}{K} + \Delta\vartheta_{cr}, \quad k = 1, ..., K. \tag{2.47}$$

where $\Delta\vartheta_{cr}$ is a phase displacement of the carriers. Setting appropriate phase displacements between carriers at adjacent levels distinct level-shifted PWM strategies can be derived (e.g. $\Delta\vartheta_{cr} = 0$ for PD LS-PWM, or $\Delta\vartheta_{cr} = \pi$ for APOD LS-PWM). Similarly, phase displacement

between carrier sets of upper and lower arms of the converter can be handled. The amplitude A_{cr} and level displacement d_{cr} of the carriers in p.u. are given by

$$A_{cr} = \frac{1}{N}, \quad d_{cr} = \frac{n-1}{N}, \quad n = 1, ..., N. \tag{2.48}$$

Another key concept is the modulation index, which relates the magnitude of the desired fundamental voltage component at the converter output phase x to half of the pole-to-pole dc voltage:

$$m_x = \frac{\sqrt{2}V_x}{V_{dc}/2} = \frac{2\sqrt{2}V_x}{V_{dc}} \tag{2.49}$$

where V_x, V_{dc} are the rms value of a phase voltage and mean value of dc pole-to-pole voltage, respectively. For the sake of simplicity, this work considers only sinusoidal modulation (sinusoidal references), while other modulating strategies with common-mode injections, typical for classical MMCs, are possible as well.

Figure 2.10 illustrates a block diagram of the implemented hybrid modulation scheme for ISM-MMC and its position in the control structure of an the converter.

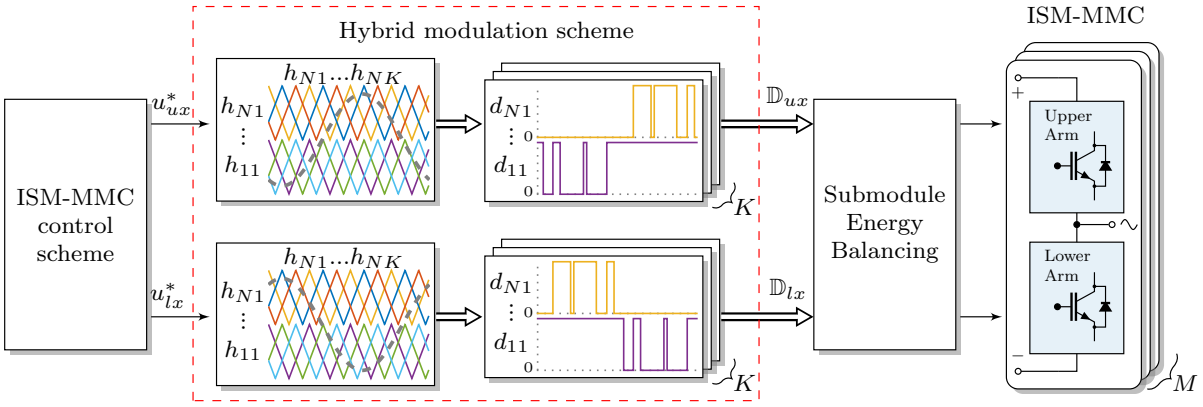

Figure 2.10 – Block diagram of the hybrid modulation scheme for ISM-MMC [144]. © 2022 IEEE

The arm modulation signals, generated by the high-level control scheme described in Section 2.4, are compared with corresponding arm carrier signals. For instance, the upper arm ISM-MMC modulation signal is compared with the upper arm carrier signals (h_{11},..., h_{nk},..., h_{NK}). In this notation the ordinal numbers n and k correspond to the carrier position in the modulation structure. The output of the comparator block is a set $\mathbb{D}_{ux}$ of logical PWM signals (d_{11},..., d_{nk},..., d_{NK}). Similarly, the lower arm PWM set $\mathbb{D}_{lx}$ is generated. Later, these two sets are applied to the voltage balancing strategy as discussed in Section 2.6.

The choice of the phase disposition scheme in level-shifted modulation method affects performance of the standard MMC converter [173]. Similar situation appears in relation to ISM-MMC. To introduce these differences for the ISM-MMC configuration, this section demonstrates modified APOD and PD methods depicted in Figures 2.11a and 2.11b, respectively, for the ISM-MMC structure with $N = 2$ and $K = 3$. Similar line style has been used to highlight the correspondence between adjacent level-shifted carriers (cf. solid yellow, dashed blue, and dash-dotted red lines in the plots). Again, it can be noted that identical set of carriers has been used for upper u^*_u and lower u^*_l arm references. Plots are drawn for a general case in the normalized form.

A classical MMC with N SMs per arm (cf. Figure 2.1a) can provide either $N + 1$ or $2N + 1$ levels in the output voltage, depending on whether adjacent level-shifted carriers are synchronized

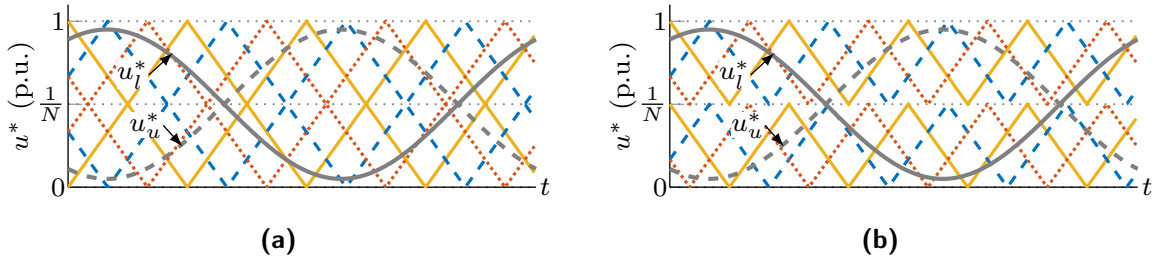

Figure 2.11 – Hybrid modulation using level-shifted carriers with different carrier phase displacement schemes: (a) APOD and (b) PD, for the ISM-MMC structure with $N = 2$ and $K = 3$

or they are in anti-phase. In relation to LS-PWM $N + 1$ levels correspond to APOD scheme, while $2N + 1$ levels can be generated with PD approach. Furthermore, as it was pointed out in Section 2.3, each interleaved submodule can produce additional $K + 1$ voltage levels. Therefore, in total, the implemented hybrid modulation scheme (cf. Figure 2.10) can synthesize $2KN + 1$ levels in case of PD LS-PWM or $KN + 1$ levels in case of APOD LS-PWM [146].

Another characteristic that should be discussed for the implemented hybrid modulation scheme is the equivalent switching frequency of ISM-MMC. It is well-known that depending on whether phase displacement between adjacent level-shifted carriers is applied or not the switching frequency of classical MMC can be defined either $Nf_{sw|SM}$ or $2Nf_{sw|SM}$, respectively. The term $f_{sw|SM}$ represents the switching frequency of a submodule. For PS-PWM it is equal to the carrier frequency ($f_{sw|SM} = f_{cr}$), while for LS-PWM it can be calculated as f_{cr}/N. At the same time, the submodule interleaving action given by PS-PWM increases equivalent switching frequency by a factor K. In this context, the hybrid modulation scheme APOD LS-PWM + PS-PWM will result in the converter's switching frequency Kf_{cr}, while PD LS-PWM + PS-PWM gives $2Kf_{cr}$.

To point out the aforementioned differences in relation to the converter's ac phase voltage, Figure 2.12 shows the simulation results of a single-phase converter, either a classical MMC or ISM-MMC, working in intvertion mode (from dc to ac) with open-circuit ac side (no load current). The structure of the simulated single-phase MMC can be derived from Figure 2.1a, bearing in mind only two submodules per arm ($N = 2$). Similarly, the shape of the ISM-MMC can be seen from Figure 2.1b with two submodules per arm and three interleaved HB-legs per SM ($N = 2$, $K = 3$). The pole-to-pole dc bus voltage (V_{dc}) is set to 1000 V and carrier frequency (f_{cr}) is 1 kHz. Ideal voltage sources are placed instead of SM capacitors to remove the effect of capacitor voltage imbalance. Voltage drops on the circuital elements are neglected. The simulating system has been run in open-loop regulation mode by manually setting required modulation index. In this case to demonstrate the full range of voltage levels in phase voltage, modulation index was set to 1 (cf. Equation (2.49)). Thus, being dc bus voltage 1000 V, the phase voltage ranges in [-500, 500] V. The very first concept that could be easily observed is the number of voltage levels in relation to the implemented modulation strategy. The simulated MMC structure, as it is well known, can feature maximum either 3 $(2 + 1)$ or 5 $(2 \times 2 + 1)$ phase voltage levels by utilizing APOD or PD, respectively. At the same moment, ISM-MMC can synthesize 7 $(2 \times 3 + 1)$ or 13 $(2 \times 2 \times 3 + 1)$ voltage levels, accordingly. Furthermore, the equivalent switching frequency of the converter increases passing from APOD to PD and from MMC to ISM-MMC. As a consequence of these notable differences, the magnitude of switching harmonics is considerably lower in case of PD LS-PWM with respect to APOD method, as well as the dominant harmonic components appear at higher frequencies. For example, in case of ISM-MMC with voltage characteristics plotted in Figures 2.12g and 2.12h the first PWM cluster

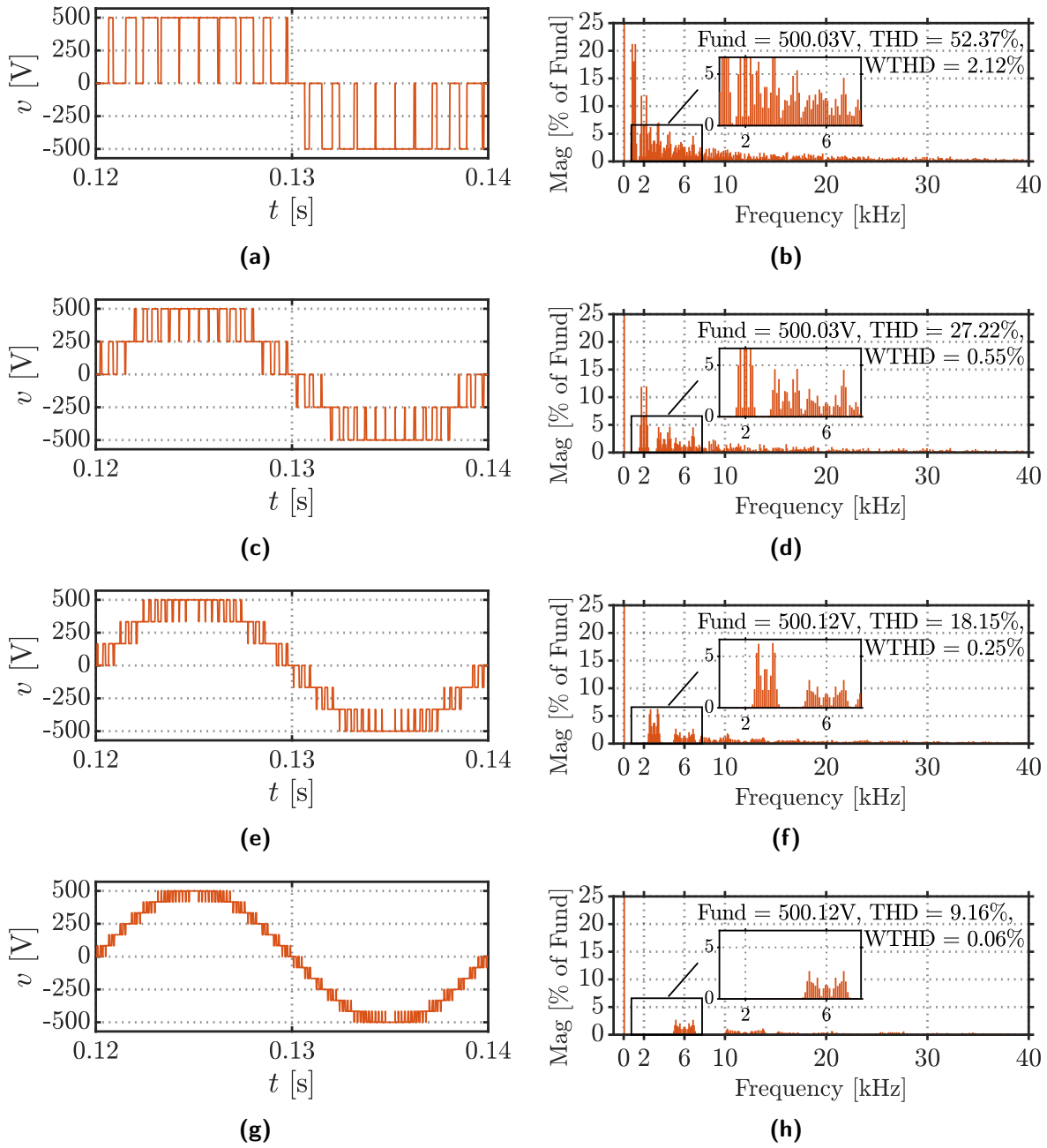

Figure 2.12 – No load phase voltage and its corresponding harmonic content in case of classical MMC with $N = 2$, $K = 1$ (a-d) and ISM-MMC with $N = 2$, $K = 3$ (e-h) for the following phase displacement schemes in LS-PWM: (a,b) MMC, APOD; (c,d) MMC, PD; (e,f) ISM-MMC, APOD; (g,h) ISM-MMC, PD

is located at about 6 kHz ($2 \times 3 \times 1$ kHz). All these aspects result in lower harmonic pollution of the corresponding phase voltage.

Unlike phase voltages in Figure 2.12, the submodule and arm voltages cannot be compared directly among the standard MMC and ISM-MMC topologies. Typically, definition of those voltages in standard MMC structures exclude arm inductance. Instead, in ISM-MMCs the "interleaved" inductors are part of a SM, hence, according to the definition of the SM voltage (cf., Equation (2.3)), currents passing through the inductors will change the shape of the voltage. For the sake of fair comparison, the arm inductor shall be distributed among the HB submodules

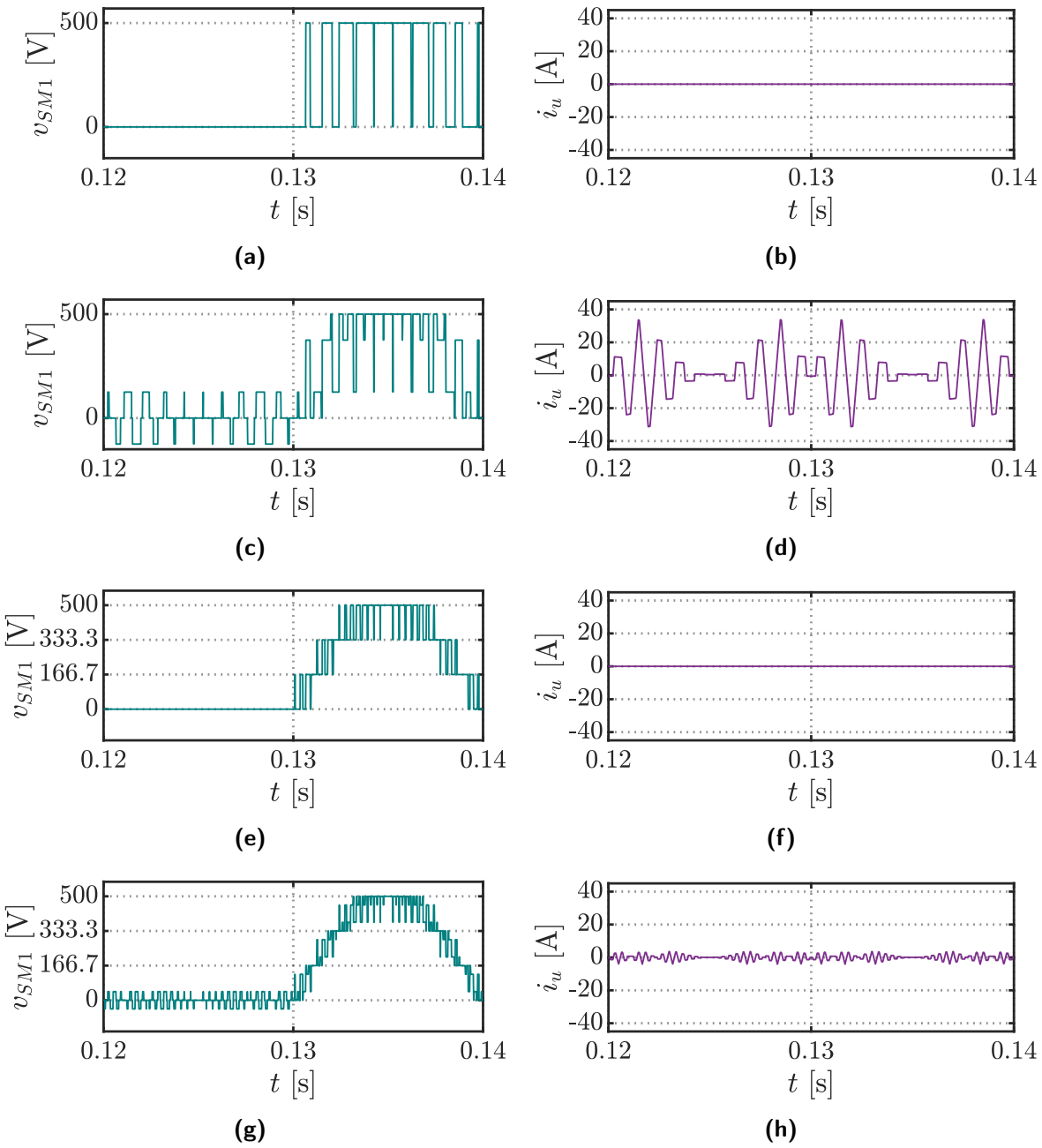

Figure 2.13 – No load submodule voltage (SM1) and corresponding arm current in case of classical MMC with $N = 2$, $K = 1$ and distributed arm inductor (a-d) and ISM-MMC with $N = 2$, $K = 3$ (e-h) for the following phase displacement schemes in LS-PWM: (a,b) MMC, APOD; (c,d) MMC, PD; (e,f) ISM-MMC, APOD; (g,h) ISM-MMC, PD

composing classical double-star MMC, while not changing the equivalent circuit values. Having introduced this MMC rearrangement, the SM voltages are compared in Figure 2.13. As it was specified above, the classical MMC with two SM per arm can synthesize only two level SM voltage. In the classical MMC configuration with distributed arm inductance this holds in case of APOD (cf. Figure 2.13a), while the waveform of the SM voltage in case of PD has extra sublevels. This happens due to the fact that the phase displacement between adjacent levels in PD create voltage difference between SMs. The higher the excursion between the standard voltage levels (e.g., "0" and "500 V" in Figures 2.13a and 2.13c) the higher the corresponding arm current. This current passing through the inductor inside a SM induces voltage over the inductor that is

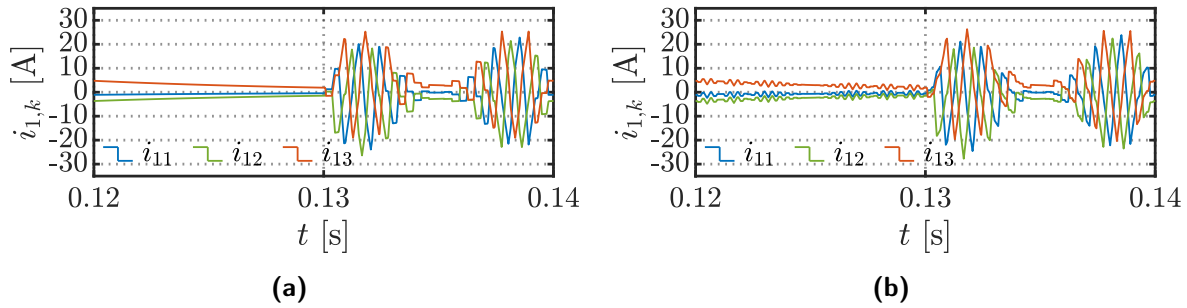

Figure 2.14 – No load current through HB-units of SM1 in case of ISM-MMC with $N = 2$, $K = 3$ for the following phase displacement schemes in LS-PWM: (a) APOD; (b) PD

added or subtracted from the "two level" SM voltage depending on the sign of the arm current. Similar situation can be observed in ISM-MMC (cf. Figures 2.13g and 2.13h). It should be noted though, that in case of multi-level SM voltage, the voltage differences between adjacent SMs are smaller, resulting in lower arm current. On the other hand, in ISM-MMC working with APOD modulation, the SM voltage level can be clearly distinguished (four equally distributed voltage levels: "0", "166.7 V", "333.3 V" and "500 V", cf. Figure 2.13e).

Another interesting observation can be made in case of no load operation of ISM-MMC. Even though there are no ac phase and arm currents (cf. Figure 2.13f), the currents inside SMs are not zero. Figure 2.14 demonstrates this effect for the APOD and PD schemes of LS-PWM.

In the following sections of this work sinusoidal PD LS-PWM (without common-mode injections) has been selected as a default submodulation method (part of hybrid modulation scheme) to maximize the number of output levels. Other level-shifted phase dispositions are outside the scope of this work and can be analyzed/compared in the future works.

2.6 Submodule Energy Balancing

Depending on the selected modulation strategy, the task of reference voltage modulation and submodule selection can be decoupled. In such schemes there is a need for methods to low down the voltage differences among the submodule capacitors within an arm [168, 173]. Two main approaches exist to fulfil this task, namely controlling each SM capacitor by an individual feedback regulator [73, 183, 184] or by means of an algorithm that handles all SM capacitors of each converter's arm. The reference voltage for each cell needs to be modified in the first approach in order to ensure almost constant stored energy in each cell capacitor over time by voltage reference increments. These voltage adjustments must be small to avoid modulation disruption. Hence, this fact makes the individual capacitor voltage feedback loops the slowest of all nested loops in the MMC control system [173]. In the second approach, there is no need in individual capacitor voltage control loop. This method is based on a sorted list of the SM capacitor voltages and special algorithm insert or bypass the SM depending on the direction of the arm current [27]. The family of methods using this capacitor voltage balancing strategy commonly referred in literature as "sorting algorithms". These post-modulation methods, which operate on the generated firing pulses, are decoupled from other control loops and do not require tuning control parameters. Typically, they are much faster in comparison with the individual control loop approach [185]. Many sorting-based schemes for submodule energy balancing in conjunction with different modulation techniques have been proposed recently. Among them

the conventional sorting algorithm based on NLC [27], predictive sorting [186, 187], tolerance band methods [188, 189], FPGA-based sorting networks [190], capacitor voltage mapping [191], capacitor voltage balancing utilizing extracted disturbance [192] and many other.

Technically all aforementioned submodule energy balancing methods in conjunction with appropriate modulation strategy can be equally applied for the newly proposed ISM-MMC topology. In the current work a classical MMC sorting algorithm in relation with LS-PWM (part of the hybrid modulation scheme, cf. Section 2.5) is used. Figure 2.15 illustrates a block diagram of the capacitor voltage balancing scheme based on the sorting algorithm in the frame of the entire ISM-MMC control method.

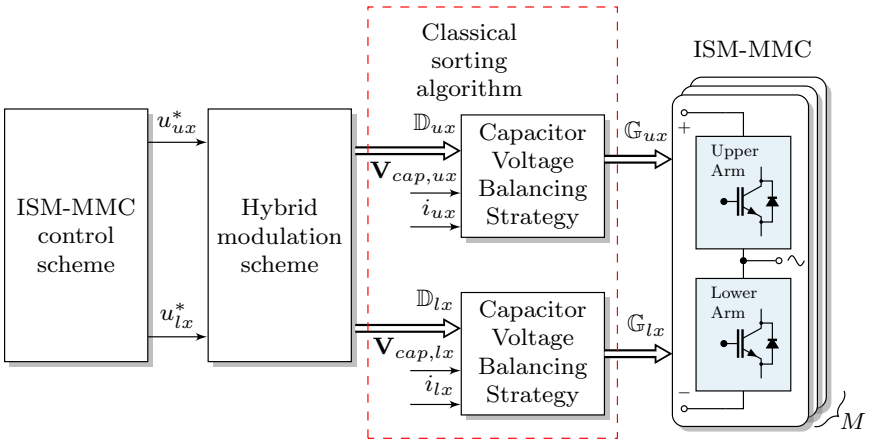

Figure 2.15 – Block diagram of the submodule energy balancing scheme for ISM-MMC [144]. © 2022 IEEE

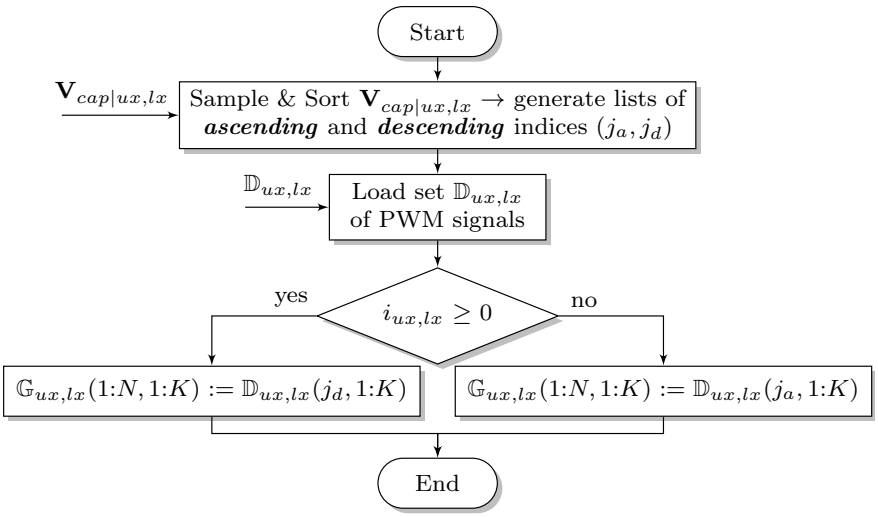

Figure 2.16 – Flowchart of the classical sorting algorithm, using hybrid modulation scheme for the waveform synthesis part

In the classical balancing method, associated with level-shifted PWM, the capacitor voltages (vectors $\mathbf{V}_{cap,ux}$, $\mathbf{V}_{cap,lx}$) within an arm are sorted either in ascending or descending order in accordance with the direction of the arm current. Then, the input firing signals of the SMs within an arm are rearranged in agreement with the sorted capacitor voltages and the direction of the arm current. This algorithm operates directly on the generated PWM signals, which are result of comparison between modulating signals and carriers. In the standard MMC structures based on HB submodules (cf. Figure 2.1a) each submodule is supplied by one firing signal (let's assume for the high switch of the HB-leg), while the remaining switch is working in the

complementary manner with a preset dead-time. Therefore, strictly speaking the classical sorting algorithm in classical MMCs rearranges these firing signals between the active submodules within an arm. In relation to the ISM-MMC structure, there are K number of firing signals for each submodule. Hence, input sets of the capacitor voltage balancing block are 2D arrays $\mathbb{D}_{ux}$, $\mathbb{D}_{lx}$ (each with dimensions $N \times K$) of PWM signals and they are formed by hybrid modulation scheme (cf. Section 2.5). The output of this block is a set of logical gate signals (2D arrays $\mathbb{G}_{ux}$, $\mathbb{G}_{lx}$ with the same dimensions $N \times K$) that drive the corresponding switches. The algorithm itself does not require a modification to meet the balancing requirements for an ISM-MMC since interleaving of HB-legs inside a submodule does not change its equivalent circuit. Furthermore, the interleaving concept is working entirely within a submodule, therefore, depending on the sorting algorithm action (bypass or insert the submodule), the group of gate signals (rows of 2D arrays $\mathbb{G}_{ux}$, $\mathbb{G}_{lx}$) can be swapped with similar group from another submodule that should be either inserted or bypassed. In this way the voltage balancing algorithm is irrespective of the number of interleaved HB-legs inside the submodule. Figure 2.16 depicts the complete flowchart of the implemented LS-PWM-based classical sorting algorithm in relation with the new topology.

2.7 Numerical Simulations and Comparison

In this section, numerical simulation results are presented to demonstrate main features of the proposed ISM-MMC in comparison to the conventional MMC structures. The comparison of working characteristics are done basing on the converter structures given in Figure 2.1. A three-phase ISM-MMC with two SMs per arm ($N = 2$) and three interleaved HB-legs in each SM ($K = 3$) was selected as a base architecture. Depending on which carrier frequency was applied either 1 or 0.333 kHz, the converter is labeled as "**N2K3f1k**" or "**N2K3f333**", respectively. A classical MMC, having two HB-based SMs per arm ($N = 2$) with three parallel switches, which commutate simultaneously at $f_{cr} = 1$ kHz, is labeled as "**N2Kp3f1k**". Another MMC configuration with six HB-based SMs per arm ($N = 6$) and $f_{cr} = 1$ kHz is labeled as "**N6K1f1k**". These labels are used throughout the whole chapter for short notation of the compared configurations. The configurations have been chosen to demonstrate key differences between the classical MMC and new ISM-MMC having similar design features (i.e., individual SM capacitance, total number of switches, etc.) and total power ratings. On the other hand, as it will be shown shortly the main output characteristics (i.e., number of ac phase voltage levels, etc.), switching frequencies, and related with that qualitative properties may vary drastically. To make unbiased comparison, the system example was selected in relation to a real design (technical specification) of the front-end converter in ultra-fast electric vehicle (EV) chargers (e.g., "Terra 184" ABB Ltd. [124]). The main system parameters of compared configurations are listed in Table 2.1. It should be noted that ISM-MMC is easily scalable to any voltage and current levels, therefore, other EV charger designs with few MW power and more can be easily implemented (e.g., "NBSK1000" Power Electronics Corp. [128], "1.5MW Charger" Proterra Corp. [129]). Obviously, the potential applications for ISM-MMC are not limited to only automotive industry and there are many other high-power demands that can benefit from ISM-MMC. Some of the trending industries suitable for ISM-MMC are listed in Section 1.3. Proper selection of ISM-MMC design parameters (e.g., number of series connected SMs, number of interleaved HB-legs in each SM, etc.) is an optimization problem that includes many variables, for example, cost, power ratings of the components, power quality requirements, etc. This topic is beyond the scope of this work and should be investigated in detail in future works.

Table 2.1 – Main system parameters for compared configurations [144]. © 2022 IEEE

Description	Symbol	N2K3f1k	N2K3f333	N2Kp3f1k	N6K1f1k
System parameters					
number of SM in each arm	N	2	2	2	6
number of HB-legs in each SM	K	3	3	1 (3 paral. sw.)	1
rated dc output power and dc-link voltage	P_{dc}, V_{dc}	180 kW, 1000 V			
rated ac input power, phase current (rms)	S_{ac}, I_x	214 kVA, 310 A			
ac line-to-line voltage (rms) and fundamental frequency	V_{xy}, f	400 V, 50 Hz			
carrier frequency	f_{cr}	1 kHz	333 Hz	1 kHz	
equivalent arm inductor / individual interleaved inductor (if applicable)	R_{arm}, L_{arm} / R, L	4 mΩ, 1.7 mH / 6 mΩ, 2.5 mH (@ 103.3 A rms)		4 mΩ, 1.7 mH (@ 310 A rms) / –	
equivalent arm capacitance / individual SM capacitance	C_{arm} / C, R_{ESR}	3.2 mF / 6.4 mF, 0.2 mΩ			3.2 mF / 19.2 mF, 0.2 mΩ
IGBT module (Infineon Technologies AG)	–	FF150R12RT4 [193]			FF450R07ME4 [194]
Control settings					
circulating current control	R_{cir} ∣ $\alpha_{2,cir}$	1.7 Ω ∣ 250 rad/s			
LPF of circulating current control	$k_{f,cir}$ ∣ $\alpha_{f,cir}$	$\sqrt{2}$ ∣ 100 rad/s			
arm-energy control	α_W	40 rad/s			
LPF of arm-energy control	$\alpha_{f1,W}$ ∣ $\alpha_{f2,W}$	100 rad/s ∣ 200 rad/s			
sorting frequency	f_{sort}	333 Hz			

Performance of the compared configurations was firstly verified under open-loop control operation mainly to demonstrate differences of ac voltage characteristics (cf. Figure 2.17) and to introduce behavioral relation between sorting frequency, which is used in the capacitor voltage balancing algorithm (cf. Section 2.6), and proper current sharing among interleaved HB-legs in each SM (cf. Figure 2.18). The latter matter is in a thoroughly manner discussed in Chapter 3. It must be noted that although the given simulation results refers to "open-loop control" operation, nevertheless, the internal control methods (cf. Figure 2.3), such as arm-energy control, circulating current control and capacitor voltage sorting algorithm, are enabled. The dynamic response of the converter working under classical MMC control strategies (cf. Section 2.4) is verified directly through hardware-in-the-loop simulations presented in Section 2.9.

For this test, the compared topologies operate in invertion mode delivering power from dc to ac side. The reference output power was selected similar to the system design example (cf. Table 2.1), namely 180 kW. To depict the maximum of available ac phase voltage levels, the highest modulation index from linear modulation range of the sinusoidal PWM (without overmodulation) was selected. Differently from simulation results presented in Section 2.5, these test account power delivery (currents are present). To speed up convergence of output characteristics to steady state values after the start-up, higher internal resistance of interleaved inductors was set (R_{arm} = 156.4 mΩ / R = 234.7 mΩ where it is applicable). Considering internal resistances of the other components (i.e., IGBT modules, capacitors, etc.) they remain unchanged. The increase results in a higher equivalent arm resistance and consequently larger voltage drop. This effect is well noticeable in Figure 2.17. However, it does not introduce tremendous effect on the performed comparative analysis. As expected, configurations "**N2K3f1k**", "**N2K3f333**" and "**N6K1f1k**" can generate 13 voltage levels operating under PD LS-PWM scheme (cf. Section 2.5).

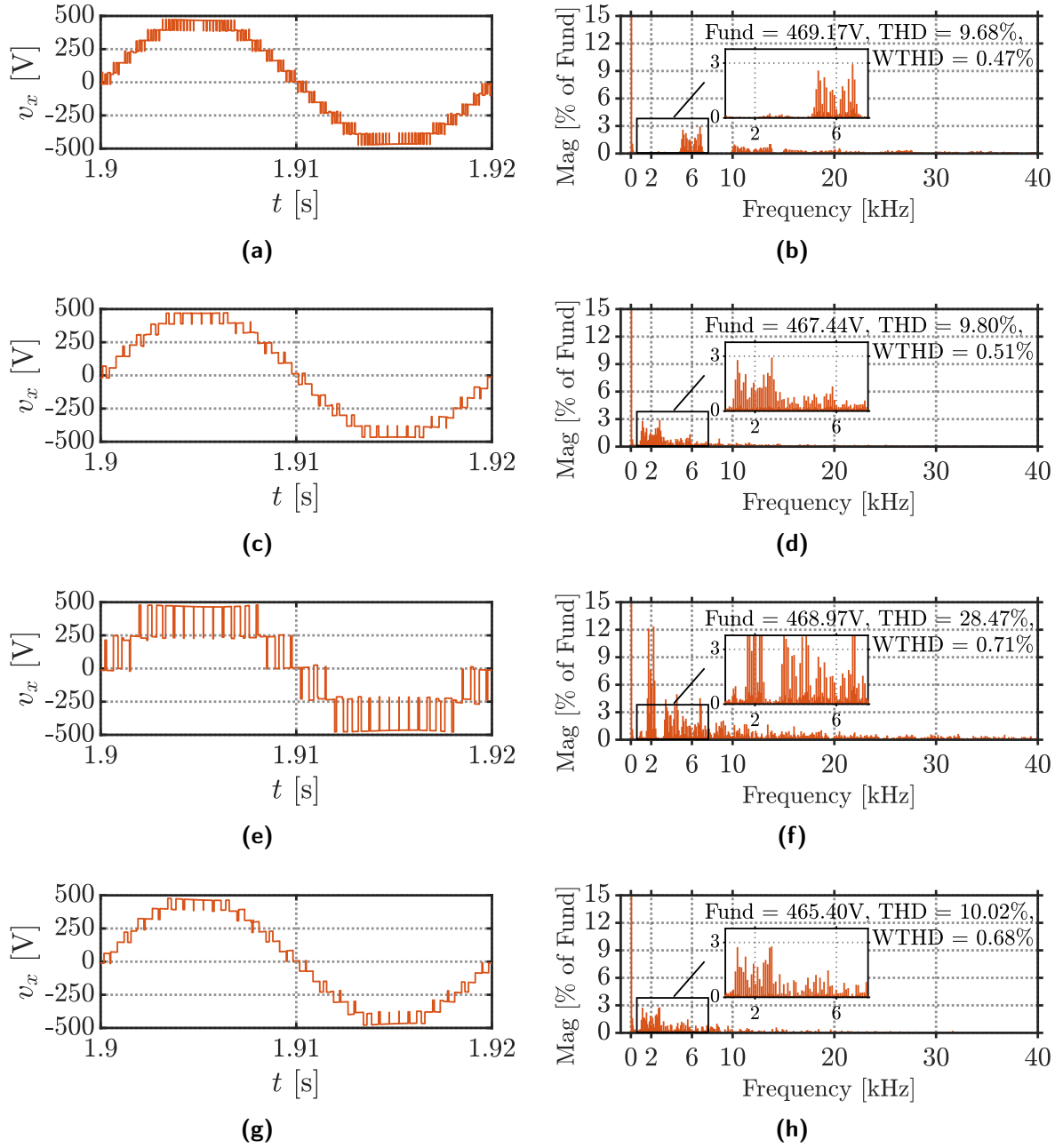

Figure 2.17 – Phase voltage and its corresponding harmonic content in ISM-MMC (a-d) and classical MMC (e-h) for the following subcases: (a,b) **N2K3f1k**; (c,d) **N2K3f333**; (e,f) **N2Kp3f1k**; (g,h) **N6K1f1k** [144]. © 2022 IEEE

It is interesting to notice here that "**N2K3f333**" and "**N6K1f1k**" have quite similar harmonic spectrum with dominant switching harmonic components appearing as a first sideband at 2 kHz. This effect is well explained in Section 2.5. On the other hand, "**N2K3f1k**" with similar THD exhibits superior performance since the first sideband harmonics are located around 6 kHz, consequently reducing requirements for the ac interface filter. In this context, weighted THD (WTHD) [195] can quantitatively justify greater performance of "**N2K3f1k**" in comparison with other converter arrangements. At the same time "**N2Kp3f1k**" having the same number of SMs (capacitors) and power switches that work without interleaving scheme can synthesize only 5 voltage levels with remarkably high harmonic pollution (cf. Figures 2.17e and 2.17f).

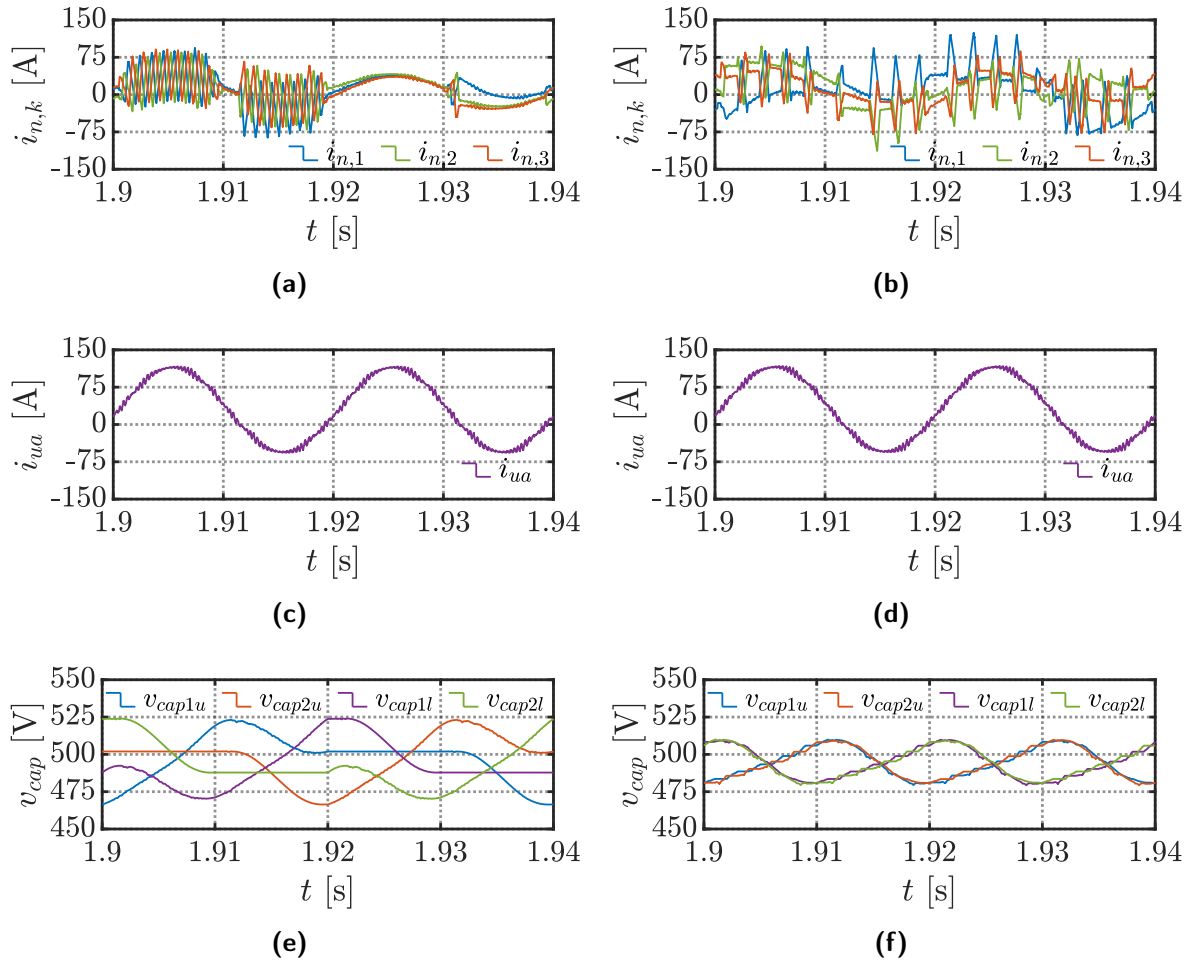

Figure 2.18 – Interleaved leg currents in one submodule of ISM-MMC (a,b), the corresponding arm current (c,d) and capacitor voltages in phase 'a' of ISM-MMC (e,f) at sorting frequency 50 Hz (a,c,e) and at 1 kHz (b,d,f) [144]. © 2022 IEEE

Another noteworthy characteristic of ISM-MMC is the relation between sorting frequency of capacitor voltage balancing algorithm, and equal current sharing among interleaved HB-legs in each SM. It is well visible from Figure 2.18 that operating with low sorting frequency of voltage balancing method, better current distribution among interleaved legs can be achieved. Conversely, higher sorting frequency results in higher imbalance of the currents in interleaved legs. This fact can be explained by significant time constants caused by relatively high inductance and small equivalent resistance of each HB-leg, large number of commutations within one fundamental period provoked by capacitor voltage balancing algorithm. This aspect must be taken into account while selecting sorting frequency. It is also evident that the output SM's current (i.e., the arm current) is not affected by the high magnitude current ripple that present in the interleaved currents. It is canceled out by summing up the interleaved currents. Similarly, it does not appear in the output phase current, as well as the leg's common-mode current that is part of the arm current (cf. dc offset in Figures 2.18c and 2.18d).

This section gives a comparative analysis of major features of the converter configurations listed in Table 2.1. The first aspect to be compared is the number of main components (i.e., IGBT modules, inductors, capacitors, etc.) and their characteristics (current and voltage ratings, etc.). All configurations have the same number of power switches, while arrangement and operation modes are different. The two chosen reference IGBT modules are from the same generation,

device family and manufactured by the same company. The "FF150R12RT4" module is designed with the following maximum rated values: collector-emitter voltage 1200 V and continuous dc current 150 A. Similarly, the "FF450R07ME4" has the following maximum ratings: 650 V and 450 A, respectively. Configurations "**N2K3f1k**" and "**N2K3f333**" feature distributed inductor arrangement, having six inductors in total per arm. In contrast, "**N2Kp3f1k**" and "**N6K1f1k**" have only one inductor per arm. Although structural characteristics of these inductors are different (internal resistance and inductances), one should note that distributed (interleaved) inductors carry only a portion of arm current, thus, can be designed with a significantly smaller cross-section of composed wires. This fact directly reflects on cost, weight and volume of the converter. To form either ISM-MMC ("**N2K3f1k**" and "**N2K3f333**") or classical MMC ("**N2Kp3f1k**") configurations with two SMs per arm only two capacitors per arm are needed. In fact, for high current applications those SM capacitors are composed of a set of parallel connected capacitors. However, for simplicity it will be assumed that the SM capacitors are single components. For the "**N6K1f1k**" configuration six capacitors per arm are required. Yet, to keep voltage ripple across the capacitors within $\pm 10\%$ tolerance band of its average value, the size of capacitors must be increased drastically. As a matter of fact, the classical MMC configuration is not well suitable for low-voltage, high-power applications, since an increase of ac voltage levels results in a corresponding increment of series connected SMs in each arm, while low dc-link voltage significantly reduces allowed fluctuating voltage range of SM capacitors, therefore, a bigger capacitance is required in each SM. Nevertheless, it must be mentioned that the total stored energy in a converter's arm of all the compared configurations is always constant. Therefore, the overall active part of capacitors will be as well the same in each case, resulting in similar overall dimensions/weight of all capacitors.

2.8 Efficiency analysis

Efficiency is a critical criterion for high-power converter design. The efficiency of each component and implemented control/modulation solutions relates to system power loss and the thermal performance. Passive elements of a converter (inductors, capacitors, etc.) contribute to the power dissipation through the parasitic internal resistances. Semiconductor devices add their contribution up to system losses during the switching events and also conduction time. The conduction loss can be characterised by the on-state voltage drop of the device. Its value typically depends on the device voltage and current ratings. Switching losses originate from the charging and discharging of semiconductor junctions at each switching event. This type of losses is influenced by manufacturing technology and dynamic performance of the semiconductor device. Switching losses are proportional to the switching frequency, so a modulation method with low switching frequency is highly preferable [196]. The aforementioned sources of power losses contribute the major part in the total converter's losses. However, an additional fraction can be added on top, namely losses in gate-drive circuit. Analytical developments for the MMC efficiency estimation have been discussed in literature in great detail (e.g., [197–200]). Therefore, for sake of conciseness, derivation of the efficiency expressions is omitted in the current work. Instead, the necessary formulations along with adopted simplifications and assumptions are given in Appendix A. The focus of this section has been aimed to the efficiency comparison between configurations studied in Section 2.7.

Figure 2.19 depicts efficiencies for the compared converter configurations. Firstly, "**N2K3f1k**" and "**N2Kp3f1k**" have almost identical efficiency curves since they have similar circuital structure and operating switching frequencies, leading to indistinguishable conduction and switching

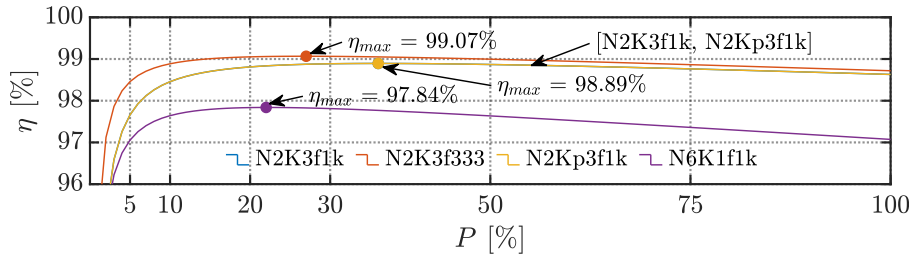

Figure 2.19 – Converter efficiency for compared cases [144]. © 2022 IEEE

losses. The main difference among them is the interleaving effect, which almost does not affect the efficiency (in this analysis current ripple is neglected). Instead, "**N2K3f333**" operates with switching frequency, reducing by 66% switching and losses in comparison to "**N2K3f1k**" or "**N2Kp3f1k**". A significantly lower efficiency can be observed in the "**N6K1f1k**" case due to higher conduction losses provoked by the large number of series submodules. Capacitor- and inductor-related losses do not play relevant role here. Losses in gate-drive circuit do not create much difference among the compared configurations since the number of switches is the same for all the cases and switching frequencies of semiconductors are similar as well (apart the "**N2K3f333**" case). Overall, it is evident from the analysis that the ISM-MMC can offer higher or equal efficiency in comparison with classical MMC, while having the same or enhanced output characteristics of the converter, depending on operating switching frequency. Table 2.2 provides a summary of the performed comparison including some structural and performance features. To demonstrate unique performance characteristic of the conversion system, weighted efficiencies with labels "eu" and "cal" are included in Table 2.2. They represent equivalent conversion efficiencies and determined similarly to the so called "European" ("eu") and "Californian" ("cal") efficiencies in [201] for the grid-connected photovoltaic systems. Unfortunately, there is no unique standard on quantitative performance characterization of the efficiency curves with dissimilar shapes (maximum efficiencies at different operating powers). In fact, it also hard to predict the power operating ranges of the general design converter since the operating modes entirely depends on the application. Therefore, weighted efficiencies that are common for the grid-connected photovoltaic systems were calculated in this work to create an evident example, while in other industries the presented efficiency performance can vary drastically.

Table 2.2 – Summary of the comparison (three-phase system) [144]. © 2022 IEEE

Characteristic	N2K3f1k	N2K3f333	N2Kp3f1k	N6K1f1k
number of active switches (rated blocking voltage, rated rms current)	72 (1200 V, 150 A)	72 (1200 V, 150 A)	72 (1200 V, 150 A)	72 (650 V, 450 A)
number of SM capacitors (capacitance, rated voltage)	12 (6.4 mF, 1200 V)	12 (6.4 mF, 1200 V)	12 (6.4 mF, 1200 V)	36 (19.2 mF, 400 V)
number of arm/interleaved inductors (inductance, rated rms current)	- / 36 (2.5 mH, 103.3 A)	- / 36 (2.5 mH, 103.3 A)	6 / - (1.7 mH, 310 A)	6 / - (1.7 mH, 310 A)
maximum number of phase voltage level @ PD LS-PWM	13	13	5	13
equivalent switching frequency @ PD LS-PWM (carrier frequency)	6 kHz (1 kHz)	2 kHz (333 Hz)	2 kHz (1 kHz)	2 kHz (1 kHz)
weighted efficiency "eu"/"cal"	98.68% / 98.81%	98.95% / 99.01%	98.68% / 98.81%	97.66% / 97.72%

2.9 Hardware-in-the-Loop Simulations

Figure 2.20 depicts a view of the HIL setup and circuital scheme of the single-phase ISM-MMC converter. The single-phase structure of ISM-MMC was used for HIL implementations due to high requirements of three-phase model (analog input/output channels, intense computational burden, etc.). This section contains necessary description of the model, main parameters that have been used for performed tests and summary of the obtained results. The HIL tests are designed to demonstrate dynamic behavior of the new ISM-MMC topology and verify applicability of the classical MMC control techniques.

Recently, HIL simulators have been widely adopted for commissioning and testing of multilevel converters [202]. In current work, HIL tests have been performed using RT Box 2 [203] (Plexim GmbH) in the Plecs environment with sampling period 12.5 μs.

At the heart of the RT Box 2 employs the latest generation Xilinx Zynq Ultrascale+ (ZU9EG) multiprocessor system-on-chip that consists of an FPGA and four CPU cores (ARM Cortex-A53, 1.5 GHz). Three out of four cores can be used for real-time simulations, while the remaining core runs an embedded Linux OS for internal processes and communication. The FPGA inside the system-on-chip is employed to control the digital I/Os and analog data conversion. The ADCs and DACs in the RT Box 2 both feature 16 bit resolution with simultaneous sample and update (maximum sample/update rate is 5 Msps). RT Box 2 contains 16 analog inputs, 16 analog outputs, 32 digital inputs and 32 digital outputs. The voltage ranges in inputs and outputs can be adjusted. All I/Os are isolated. The communication with a PC is made through gigabit Ethernet ports. The 480 GB of internal memory can be used for continuous data points storage. RT Box 2 supports multi-tasking mode, where the designed model can be split into separate physical sub-systems and run in parallel on different CPUs [203].

The HIL simulation results are presented for "**N2K3f1k**" case only. To reduce the computation burden of the HIL setup, for these tests a single-phase ISM-MMC with two SMs per arm ($N = 2$) and tree interleaved legs in each SM ($K = 3$) was used (cf. Figure 2.20b). The entire model (power and control stages) were deployed in a single RT Box 2. To make it possible analog and digital inputs/outputs of the RT Box 2 were interconnected, correspondingly (cf. Figure 2.20a). The real-time simulation was performed in a multi-tasking mode, distributing tasks between available CPUs, such that power circuit was emulated on both CPU1 and CPU2, while the entire control has been deployed on CPU3. The target machine (RT Box 2) was controlled via external PC, while monitoring electrical signals on its screen. The measured signals sampled with the same sampling period (cf. Table 2.3) and stored on the internal memory of RT Box 2 for the subsequent post-processing (figures plotting) in Matlab (MathWorks Inc.).

Table 2.3 summarizes the main parameters of the designed HIL model. The single-phase, grid-connected (230 V rms) ISM-MMC supplies a dc load (60 kW) with unity power factor via the dc-link. To provide a reference neutral wire connection, a split dc-link capacitor (C_{dc} = 15 mF) has been used. The dc load was realized as a controlled current source (i_{dc}) with known demand profile. The profile includes a step-like change of dc current by 50% from half to full demand and back. The second dc current step is applied when the system has already experienced a step-like drop of dc-link voltage by 10%. The internal resistance of interleaved inductors was set to a higher value in comparison with Table 2.1 (R_{arm} = 30.3 mΩ / R = 45.5 mΩ) to smooth divergence of interleaved currents from one another since the interleaved currents are not actively controlled (the control is discussed in Chapter 3). On the other hand, the resistance values were selected smaller in comparison to those in Section 2.5 to have a well noticeable current imbalance within SMs and consequently demonstrate that this imbalance does not affect

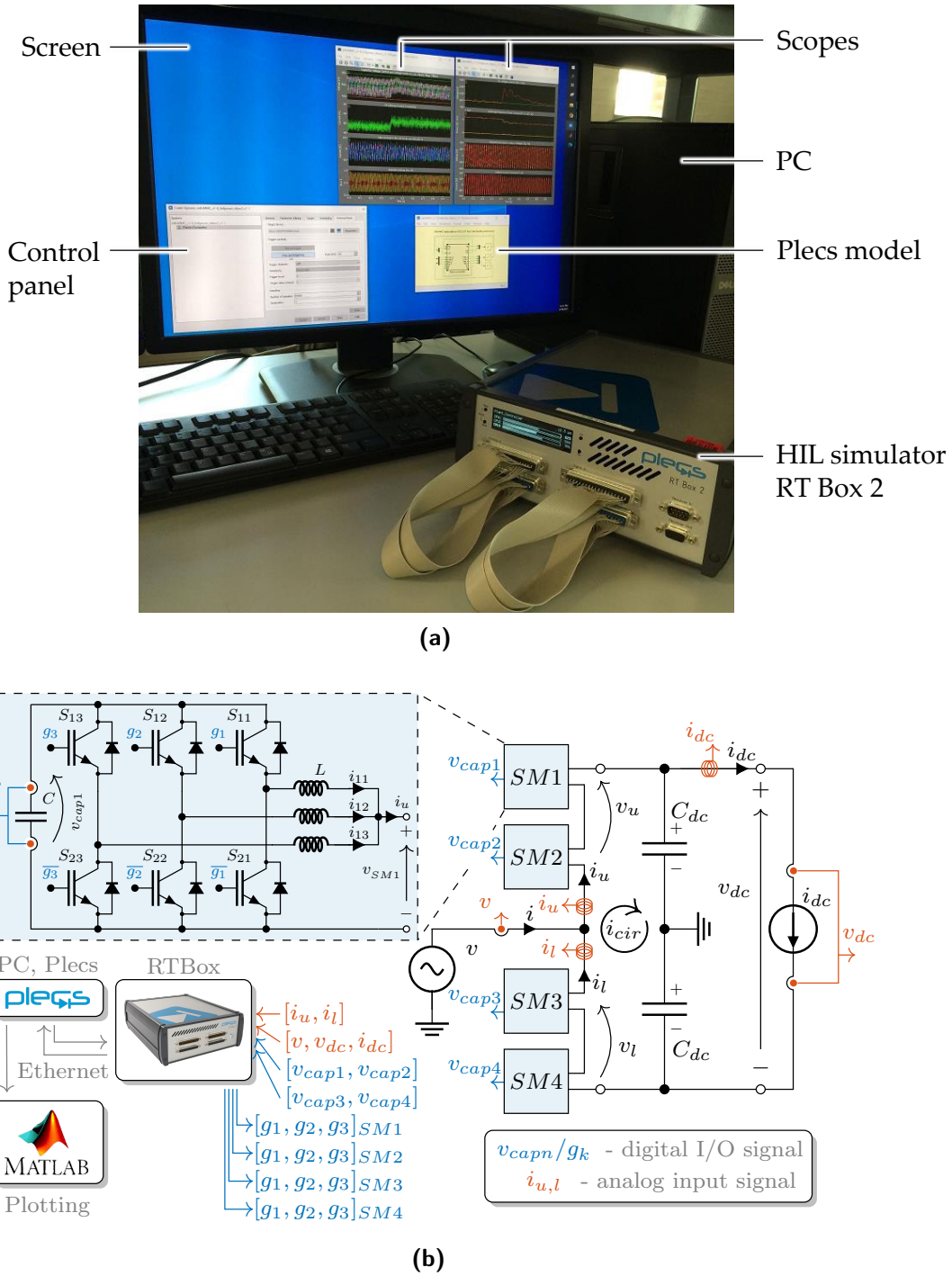

Figure 2.20 – View of the HIL simulator (a) and circuital scheme of the test single-phase ISM-MMC (b) [144]. © 2022 IEEE

the input/output converter's characteristics. These equivalent resistances include also on-state resistance of an IGBT.

The rest parameters of passive components (L, C) were assigned with reference to real commercial components having standard tolerances. For R, L the tolerance is 15%, while for C it is 10%. Accounting of these tolerances in simulations was made by generating random values following a Gaussian distribution and having a confidence interval of $\pm 4\sigma$.

Table 2.3 – Main parameters of the HIL model [144]. © 2022 IEEE

Description	Symbol	Parameters
System parameters		
converter configuration (single-phase version)	–	**N2K3f1k**
number of SMs per arm	N	2
number of HB-legs in each SM	K	3
rated dc output power and dc-link voltage	P_{dc}, V_{dc}	60 kW, 1000 V
rated ac input power, phase current (rms)	S_{ac}, I	71.6 kVA, 310 A
ac phase voltage (rms) and fundamental frequency	V, f	230 V, 50 Hz
carrier frequency	f_{cr}	1 kHz
dc-link split capacitance (2×)	C_{dc}, $R_{ESR,dc}$	15 mF, 3.4 mΩ
individual interleaved leg inductor parameters	R, L	45.5 mΩ, 2.5 mH
individual SM capacitance	C, R_{ESR}	6.4 mF, 0.2 mΩ
IGBT module (Infineon Technologies AG)	–	FF150R12RT4 [193]
Control settings		
dc voltage control bandwidth	$\alpha_{p,dc}$ | $\alpha_{i,dc}$	15 rad/s | 5 rad/s
averaging time of the dc moving-average filter (H_{dc})	–	10 ms
loop-filter bandwidth (PLL)	$\alpha_{p,pll}$ | $\alpha_{i,pll}$	50 rad/s | 10 rad/s
output current control bandwidth	$\alpha_{c,oc}$ | $\alpha_{r,oc}$	2000 rad/s | 50 rad/s
circulating current control	R_{cir} | $\alpha_{2,cir}$	1.7 Ω | 250 rad/s
LPF circulating current control	$k_{f,cir}$ | $\alpha_{f,cir}$	$\sqrt{2}$ | 100 rad/s
sorting frequency	f_{sort}	333 Hz
discretization step size	–	12.5 μs

Figure 2.21 depicts measured ac power (active and reactive) supplied by the grid, the corresponding ac phase current, and dc-link voltage along with its reference. Figure 2.21a confirms that the HIL simulated ISM-MMC operates with unity power factor (supplied reactive power is zero).

Figure 2.22a presents measured capacitor voltages from each submodule of the single-phase ISM-MMC. The dashed lines in this plot represent ±10% voltage ripple tolerance band and mean value of capacitor voltage. Dynamic behavior of leg's common-mode current in response of the imposed system changes can be seen from Figure 2.22b . This current after some transients reaches steady state values depending on the operating point. The leg's common-mode current is composed of dc current and high frequency ripple component. Overall, the system behavior under classical MMC close-loop control demonstrates expected, stable performance in all tested operational modes having unequal parameters of passive components.

Figure 2.23 confirms the fact that the balancing of interleaved currents is a decoupled control task and should be implemented individually in each SM. Balancing of interleaved currents as it was mentioned previously is thoroughly discussed in Chapter 3 and therefore, not presented here. Nevertheless, it worth to notice that even though the currents inside of a SM are unbalanced (cf. fundamental components of the currents) and feature high-magnitude ripple, the sum of them (arm current) remains balanced and sinusoidal-like. Similarly, ac phase current has a balanced shape.

Careful inspection of test scenarios provided above reveals that the presented waveforms correspond to their expected shapes, leading to the conclusion that the classical MMC control can seamlessly implemented for the proposed ISM-MMC, having stable system response.

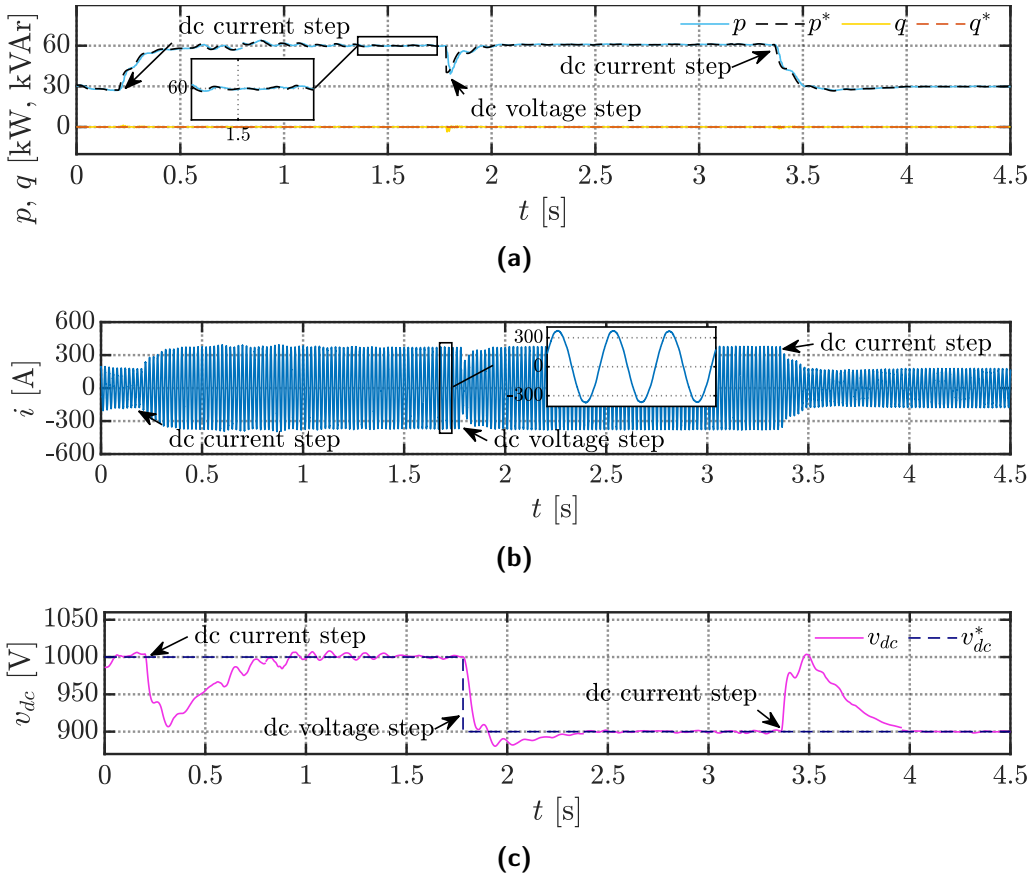

Figure 2.21 – Active and reactive power (a) supplied by the grid (solid traces) along with their reference values (dashed lines), ac phase current (b) and dc-link voltage (c) – measured value (solid trace) and its reference (dashed trace) [144]. © 2022 IEEE

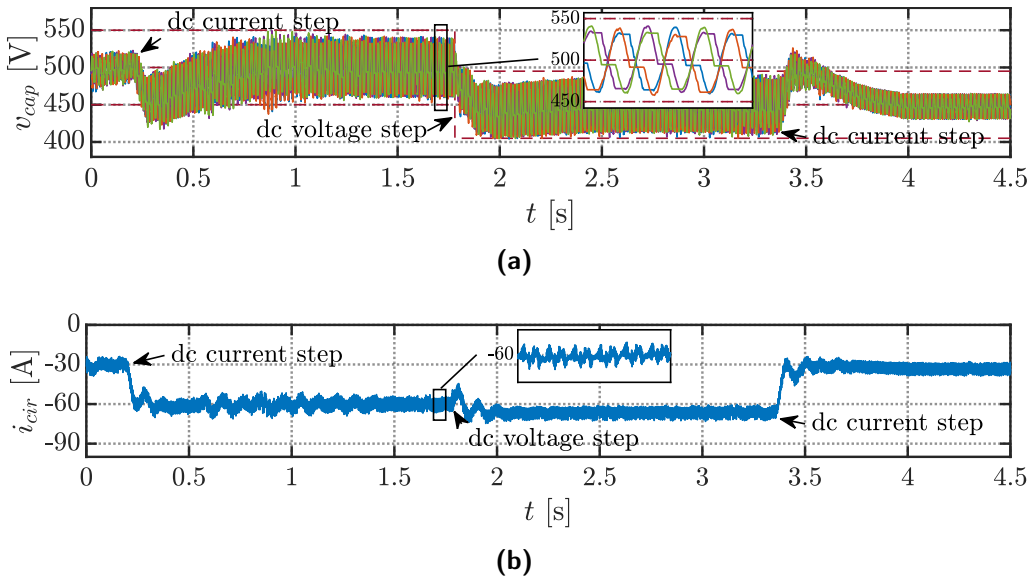

Figure 2.22 – Capacitor voltages (a) from each submodule of the ISM-MMC (solid traces) along with its ±10% tolerance band and mean value (dashed lines) and corresponding leg's common-mode current (b) in phase leg of ISM-MMC [144]. © 2022 IEEE

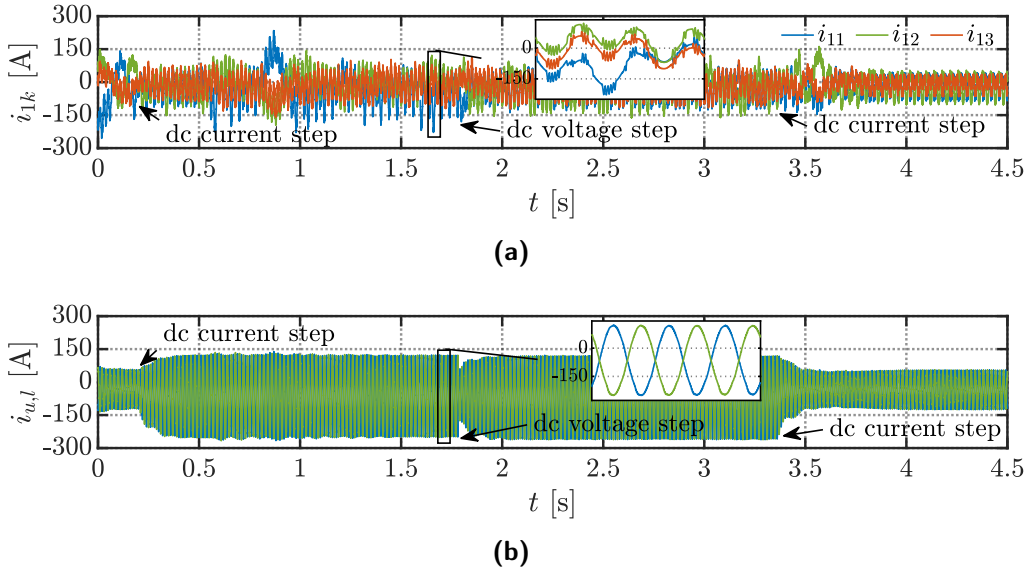

Figure 2.23 – Currents in interleaved legs of the submodule SM1 (a) and arm currents of ISM-MMC (b) [144]. © 2022 IEEE

2.10 Summary

This chapter considers fundamentals of the proposed MMC structure based on interleaved half-bridge submodules and its modeling using averaging principle. It has been shown that the average model of ISM-MMC resembles the average model of the classical double-star MMC with HB submodules. The obtained converter model serves to design a control method for the new topology. Classical MMC control techniques can be used for the ISM-MMC since the average models are matching. The presented control strategies for ISM-MMC, which works in rectification mode, include dc-bus voltage control, grid synchronization method, output current control and two internal controls, namely circulating current control and arm-energy control. Necessary description for each block along with bandwidth and control gains calculation has been provided. The topology-specific, hybrid modulation scheme has been presented in this chapter. It is composed by well-known carrier based techniques, namely level- and phase-shifted PWMs. Later, summary of submodule energy balancing techniques based on typical MMC sorting algorithms is presented. It has been demonstrated that neither the implemented hybrid modulation scheme and nor ISM-MMC structure do not change the principle of submodule energy balancing. Another section is dedicated to numerical simulations and comparative analysis of the few related configurations of the new ISM-MMC and classical MMC. Efficiency study is also presented for these converter configurations to point out potential performance of the proposed ISM-MMC. Finally, hardware-in-the-loop tests were conducted for one of the ISM-MMC to demonstrate its dynamic behaviour and fitting of classical MMC control methods for the new structure. The HIL tests results verify stable operation of the new multilevel converter design with implemented control method.

Chapter 3

Interleaved Currents Balancing Control

3.1 Introduction

The problem of equal current sharing in MMC structures at submodule level is quite new topic and has not been elaborated in depth so far apart from [204]. The existing methods to cope with this problem in other power converter configurations (e.g. two-level interleaved PFC configurations) cannot be simply introduced into classical MMC control method due to specifics of its operation, therefore some modifications are required. The main contribution of this chapter is an implementation of the current balancing control loop for ISM-MMC structure in the frame of classical MMC control law presented in Chapter 2, as well as an analysis of its dynamic behavior under various system perturbations. In addition to that, a new capacitor voltage balancing strategy is introduced to make possible the operation of the interleaved currents balancing technique.

The chapter is structured as follows. Section 3.2 introduces the current equalization problem in ISM-MMCs, providing essential control diagrams. In the following Section 3.3 the modified capacitor voltage balancing strategy along with converter's modulation are discussed. Design of interleaved legs current balancing control is introduced in Section 3.4. Simulation results in Section 3.5 prove the stable functioning of the introduced methods in a three-phase ISM-MMC with component parameters that individually experience a step change at the given instant. Verification of the proposed balancing concepts is supported by experimental results presented in Section 3.6. Finally, the summary of the current chapter is drawn in Section 3.7.

3.2 Problem statement

To start, this section refreshes some structural fundamentals of ISM-MMC. The single-phase structure of ISM-MMC is depicted in Figure 3.1. The ISM-MMC resembles double-star MMC topology without standalone arm inductors. In this case, the arm inductors are distributed among the converter submodules. The submodule itself consists of K parallel half-bridge legs connected to a capacitor on the dc side. The midpoint of each leg is linked with an inductor (L). The other side of the inductors is joined together, creating a positive terminal of the SM.

Under ideal conditions, the total arm current is equally shared among the parallel half-bridges in each SM. However, the interleaving modulation scheme applied to the SM implies that the

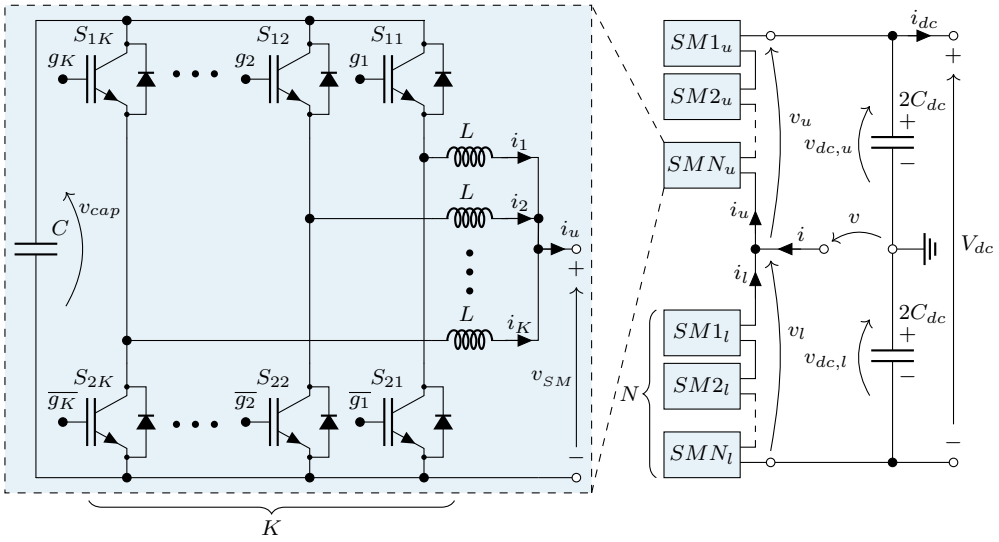

Figure 3.1 – Structure of a single-phase ISM-MMC [204]. © 2022 IEEE

commutation between parallel legs happens in a non-simultaneous manner. In addition to that, circuit nonlinearities (differences among equivalent branch resistances), unequal dead-times, control actions and many other factors may lead to the instantaneous current imbalance (fundamental components) between the interleaved legs. A uniform distribution of the total arms current among the parallel legs has to be ensured to avoid excessive converter losses and saturation of the inductors, while guaranteeing optimal capacity utilization of the SM half-bridges. This problem is well-known for interleaved-based converters and has been widely reported in the literature. For instance, authors in [205, 206] proposed to mitigate current imbalances between parallel legs in an interleaved buck converter by a feedback control scheme. A similar concept has been applied to an interleaved ac-dc converter in [207]. In MMC structures, this problem is quite new since scalability in the direction of high currents is a recent trend for this type of converter [22], especially at the submodule level.

It is worth to notice in Figure 3.1 that the average ISM-MMC model does not change with respect to a classical MMC structure based on a half-bridge submodule (cf. Section 2.3). Therefore, strictly speaking, the typical outer and inner control loops of the classical MMC are also applicable for the ISM-MMC. Section 2.4 gives a comprehensive description of the ISM-MMC control structure that is further discussed in the current chapter. Therefore, here the necessary overview, which helps to highlight the proposed concepts, is given only.

A block diagram of the implemented control-modulation loops, which have been previously examined in Sections 2.4-2.6, with reference to the single-phase ISM-MMC (cf. Figure 3.1) and its operation in rectification mode, is illustrated in Figure 3.2. Here for simplicity high-level control scheme (cf. Figure 2.3) is depicted as a single block since it falls out of interest point of current chapter. Instead, the main focus is drawn to remaining blocks, namely the capacitor voltage balancing method (cf. Section 2.6) and modulation technique (cf. Section 2.5), designed specifically for ISM-MMCs [146].

Having as an input of the modulation block the normalized upper arm voltage reference (u_u^*), it produces a 2D set ($\mathbb{D}_u$) of logical PWM signals (d_{11},..., d_{NK}). Similarly, the lower arm PWM set $\mathbb{D}_l$ is generated. Later, these two sets are applied to the classical capacitor voltage balancing strategy. In the classical balancing method, associated with carrier-based PWM, the capacitor voltages (vectors $\mathbf{V}_{cap,u}$, $\mathbf{V}_{cap,l}$) within one arm are sorted either in ascending or descending order in

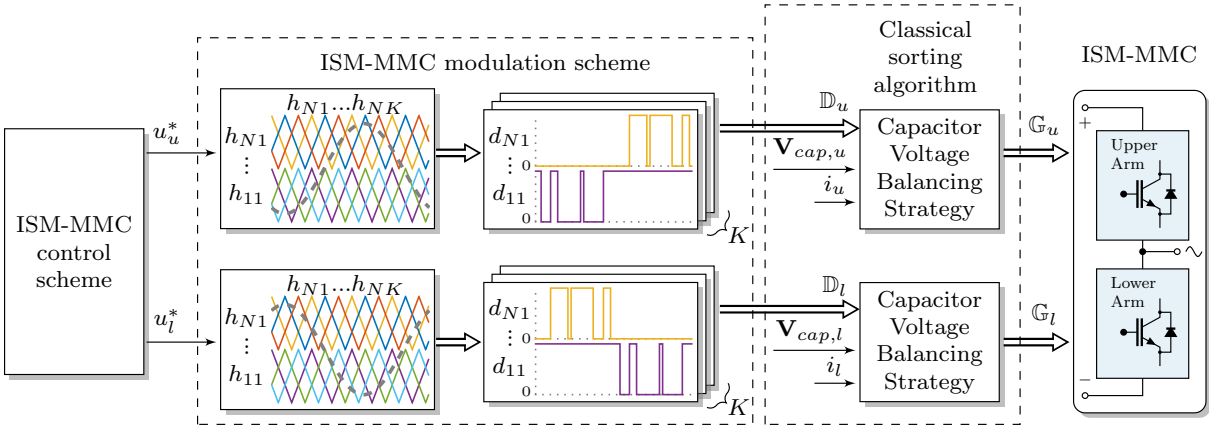

Figure 3.2 – Block diagram of the ISM-MMC control employing classical capacitor voltage balancing technique [144, 204]. © 2022 IEEE

accordance with the direction of the corresponding arm current. Then, the input gate signals are rearranged based on the sorting lists. It is important to notice that this algorithm operates directly on the generated set of PWM signals (2D arrays $\mathbb{D}_u$, $\mathbb{D}_l$). The output of this block is a set of logical firing signals (2D arrays $\mathbb{G}_u$, $\mathbb{G}_l$) that drive power switches. Since regulation of capacitor voltages in this control arrangement is the independent and ultimate step of the ISM-MMC control, it is not hard to show that this regulator will try to balance capacitor voltages disregarding the proper share of the interleaved currents within each submodule. Therefore, any control method designed to balance the interleaved currents and applied upstream of the capacitor voltages balancing block (e.g., acting on arm voltage references) will fail. In addition, the small internal resistance of the individual interleaved inductors, having standard tolerances, may result in huge current imbalances among the interleaved legs (cf. Figure 2.23a). This fact becomes even more evident when the values of those internal resistances are comparable with, for instance, the equivalent on-state resistance of the power switches. Thus, a control strategy that balances interleaved currents is essential for ISM-MMC.

It is worth noticing that the regulation of interleaved currents features faster dynamics with respect to capacitor voltage balancing. So, the interleaved currents control must be the ultimate step of the ISM-MMC control. Moreover, as it is explained in the following sections, this work presents an interleaved legs current balancing regulator that acts individually on modulating voltage references of each SM [204]. Therefore, a new capacitor voltage balancing function that operates directly on reference signals is introduced here as well.

3.3 Modified Submodule Sorting Algorithm

This section explains a few modifications of the conventional MMC closed-loop method that must be implemented to successfully balance both capacitor voltages in series connected SMs and interleaved currents in each SM. Various adjustments into the modulation have been proposed in literature to either improve converter's operational performance and reduce complexity of the control/modulation [88] or propose a new capacitor voltage balancing technique for MMC structures [208]. Unlike the reference [208], where the new capacitor voltage balancing method is based on carrier rotation technique, the reference [204] proposes to split arm reference voltages into individual SM voltage references taking into account the level of each capacitor voltage. The sorting principle is developed in a similar manner to the classical sorting algorithm discussed in

Section 2.6. This section describes the proposed balancing strategy from [204] and it is elaborated in per-phase structure with reference to Figure 3.1. The principal block scheme of the modified control part is illustrated in Figure 3.3. It consists of the classical MMC control part that generates normalized voltage references for upper (u_u^*) and lower (u_l^*) converters' arms; a novel capacitor voltage balancing strategy, which directly operates with the modulating signals, producing K copies of the normalized individual SM voltage references (e.g., u_{u11}^*..., u_{uN1}^*); an original interleaved legs current balancing method that eventually followed by the hybrid ISM-MMC modulation scheme (cf. Section 2.5). The current section is dedicated to the proposed sorting algorithm (framed by red dashed box in Figure 3.3).

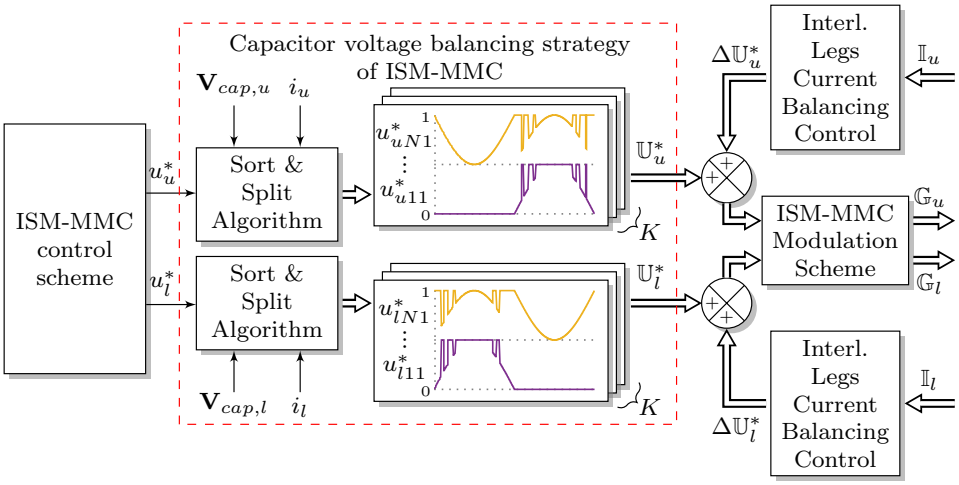

Figure 3.3 – Block diagram of the modified ISM-MMC control method [204]. © 2022 IEEE

As suggested in [196] with reference to a classical MMC, arm voltage synthesis can be decoupled from the selection of which SM must commutate at each instant. Based on this idea, several "sorting & select" algorithms have been proposed in the literature (more details on classical MMC sorting algorithms can be found in Section 2.6) to maintain capacitor voltage ripple within a specific limit. As pointed out in Section 2.3, the average model of ISM-MMC is identical to the one of classical MMC with half-bridge SMs. Therefore, strictly speaking, all invented sorting functions for the classical MMC are equally applicable in the case of ISM-MMC. The new "Sort & Split" algorithm permits to employ the paradigm of the well-established sorting functions while operating with reference voltages rather than with firing pulses. The flowchart depicted in Figure 3.4 explains the logic behind the new algorithm.

It starts by sampling and sorting capacitor voltages with a constant updating frequency (f_{sort}), eventually generating lists of indices (j_a, j_d) with sampled capacitor voltages in ascending and descending order. By considering the sign of the corresponding arm current that demonstrates whether the capacitor is charging or discharging, the reference voltage of each SM is synthesized. The rule to form SM reference voltage is the same for both paths, and it is based on the general idea of adding/removing extra levels following the reference arm voltage. The difference is in selecting a SM that must be inserted or bypassed (where n is the ordinal number of a SM and N is the total number of SM per arm). This selection is based on the previously generated lists of indices. During a sorting period, SM reference voltages are organized in descending order if arm current is positive; otherwise, in ascending order. At this stage, vectors of normalized SM reference voltages ($\mathbf{U}_{u,l}^*$) for the upper and lower arms are formed. A saturation block is required to split arm voltage reference between the SMs properly. The possible shape of the generated SM voltage references can be seen in Figure 3.3. It is clear that the waveform of reference SM voltages is highly dependent on updating frequency f_{sort}. The next block creates K copies of

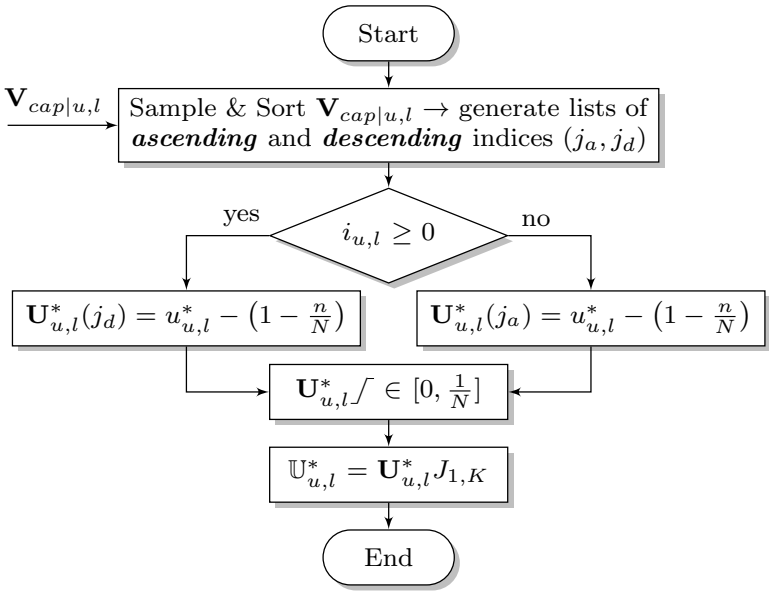

Figure 3.4 – Flowchart of the proposed Sort & Split algorithm [204]. © 2022 IEEE

the reference vectors by multiplying the initial reference vector with an array of ones ($J_{1,K}$), composing 2D sets ($\mathbb{U}^*_{u,l}$) of SM reference voltages for the upper and lower arms, respectively. This mathematical operation is required for subsequent adjustments of the reference voltages individually for each interleaved leg within a SM.

It can be easily demonstrated that the new sorting function produces an identical switching pattern in comparison with the analogous sorting algorithm for the classical MMC control (cf. Figure 2.16). In fact, the proposed technique can be used for the classical MMC as well by setting K equal to 1. The output of the proposed capacitor voltage balancing block has been numerically simulated and the results are presented in Section 3.5.

3.4 Controller Structure

Having individual voltage references for each HB-leg inside a SM it is possible to modulate them independently. This fact opens a possibility for individual adjustments of the voltage references to moderate the current, which flows through the corresponding HB-leg. Individual closed-loop controllers are proposed in [204]. This section describes the introduced method.

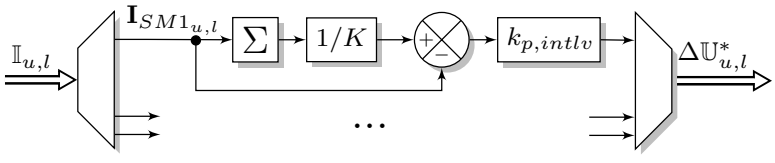

Figure 3.5 – Block diagram of the interleaved legs current balancing control [204]. © 2022 IEEE

Figure 3.5 illustrates a block diagram of the proposed interleaved legs current balancing technique. It is based on an individual current feedback loop for each interleaved leg. Every control loop includes a reference input signal as the average leg's current (it can be calculated once as an arm current divided by the number of commutating, interleaved legs in a SM) and individually acquired currents throughout each interleaved leg. Therefore, in total, the proposed

approach requires knowledge of $N(K-1)+1$ instantaneous interleaved legs' currents in each ISM-MMC arm. The rest of the currents can be obtained based on the Kirchhoff's current law. The individual HB-leg currents can be either measured or estimated. Estimation of the instantaneous interleaved legs' currents is out of the scope of the current section and it is thoroughly elaborated in Chapter 4; therefore, for now it is assumed that all currents are measured. Then, individually computed current errors are followed by a proportional controller ($k_{p,intlv}$) that generates normalized portions of reference voltages. These normalized voltage fractions are eventually added to the individual, normalized SM voltage references that have been formed by the introduced "Sort & Split" algorithm (cf. Figure 3.3). All in all, each interleaved leg is independently controlled, providing a high dynamic response to any rapid disturbance in the controlled system. It is evident that the sum of current errors (difference between real interleaved current and its balanced average value) within a SM is equal to zero. Thus, the sum of additive normalized voltage portions ($\Delta\mathbb{U}^*_{u,l}$) generated by the control loop in Figure 3.5 within one SM is also zero. As a result, the average value of SM voltage remains unchanged due to the operation of the proposed control. However, subtraction or adding large voltage portions from/to the SM reference voltage will force switches in each interleaved leg to remain in an on/off state for a longer time (the interleaved control loop is the ultimate control method before the modulation block, cf. Figure 3.3), therefore introducing high disturbance to the capacitor voltage balancing algorithm.

3.5 Numerical Simulations

Even though up to now the proposed balanced methods were discussed in the context of a single-phase ISM-MMC, it can be easily demonstrated that all introduced initiatives are equally valid for multi-phase systems, e.g., a three-phase structure. A three-phase ISM-MMC that works in the rectification mode (with reference to ultra-fast electrical vehicle chargers) is depicted in Figure 3.6. Each converter phase consists of four interleaved submodules (two submodules per arm, $N=2$), while each submodule has three interleaved half-bridge legs ($K=3$). A fully controllable current source represents the dc load.

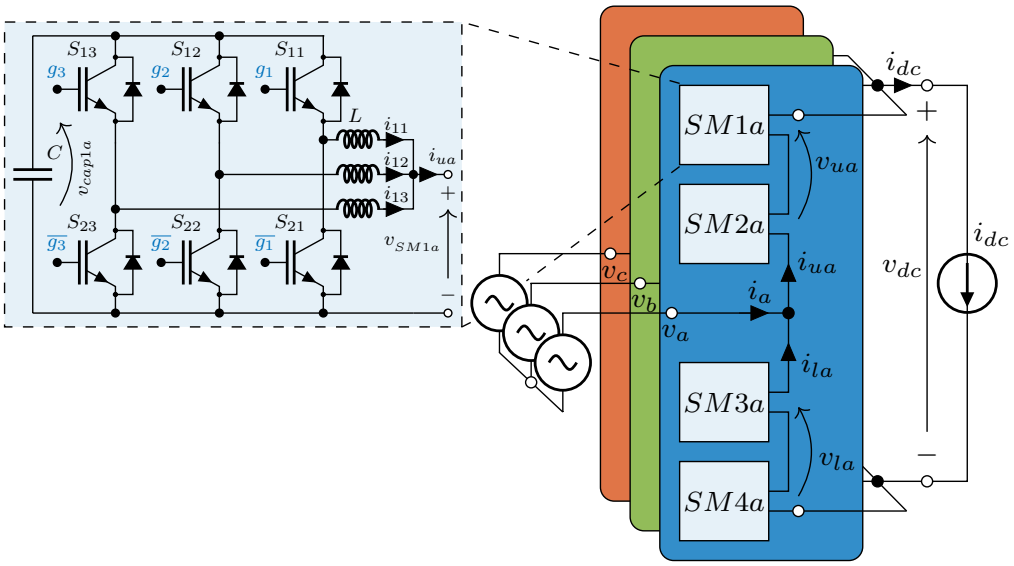

Figure 3.6 – Three-phase ISM-MMC working in the rectification mode [204]. © 2022 IEEE

The application and main system parameters are identical to those listed in Table 2.1 and have been chosen with reference to the design example "**N2K3f1k**" given in Section 2.7. Here they are summarized along with control gains in Table 3.1 for the reader's convenience.

Table 3.1 – Main system parameters of the three-phase ISM-MMC [144, 204]. © 2022 IEEE

Description	Symbol	Parameters
System parameters		
converter configuration (three-phase version)	–	**N2K3f1k**
number of SMs per arm	N	2
number of HB-legs in each SM	K	3
rated dc output power and dc-link voltage	P_{dc}, V_{dc}	180 kW, 1000 V
rated ac input power, phase current (rms)	S_{ac}, I_x	214 kVA, 310 A
ac line-to-line voltage (rms) and fundamental frequency	V_{xy}, f	400 V, 50 Hz
carrier frequency	f_{cr}	1 kHz
individual interleaved leg inductor parameters	R, L	6 mΩ, 2.5 mH
individual SM capacitance	C, R_{ESR}	6.4 mF, 0.2 mΩ
IGBT module (Infineon Technologies AG)	–	FF150R12RT4 [193]
Control settings		
dc voltage control bandwidth	$\alpha_{p,dc}$ | $\alpha_{i,dc}$	15 rad/s | 5 rad/s
averaging time of the dc moving-average filter (H_{dc})	–	10 ms
loop-filter bandwidth (PLL)	$\alpha_{p,pll}$ | $\alpha_{i,pll}$	50 rad/s | 10 rad/s
output current control bandwidth	$\alpha_{c,oc}$ | $\alpha_{r,oc}$	2000 rad/s | 50 rad/s
circulating current control	R_{cir} | $\alpha_{2,cir}$	1.7 Ω | 250 rad/s
LPF circulating current control	$k_{f,cir}$ | $\alpha_{f,cir}$	$\sqrt{2}$ | 100 rad/s
arm-energy control	α_W	40 rad/s
LPF of arm-energy control	$\alpha_{f1,W}$ | $\alpha_{f2,W}$	100 rad/s | 200 rad/s
sorting frequency	f_{sort}	333 Hz
interleaved current balancing	$k_{p,intlv}$	0.006 A^{-1}

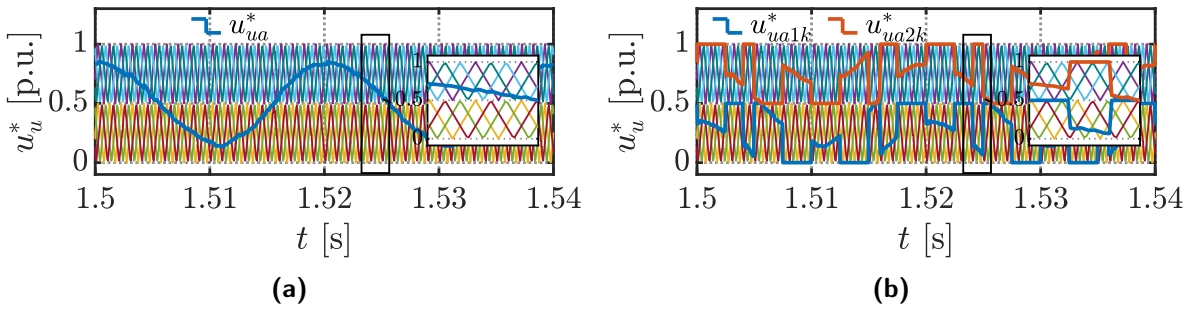

Figure 3.7 – Normalized reference voltage of the upper arm of ISM-MMC (ph. a) along with hybrid modulation carriers (a) before and (b) after Sort & Split algorithm [204]. © 2022 IEEE

Figure 3.7 illustrates the functioning of the introduced above "Sort & Split" capacitor voltage balancing strategy. Without the new balancing algorithm, the arm reference voltage entering the modulation block is directly compared with hybrid modulation (LS-PWM and PS-PWM) carriers, producing firing signals. It is clear that when normalized reference arm voltage (u^*_{ua}) remains in the upper sector ($0.5 - 1$ p.u., Figure 3.7a), for example, only one SM is commutating introducing unbalance among capacitor voltages in the arm. Therefore, additional actions to balance capacitor voltages are required, right after the modulation block. Typically, these sort of actions are done

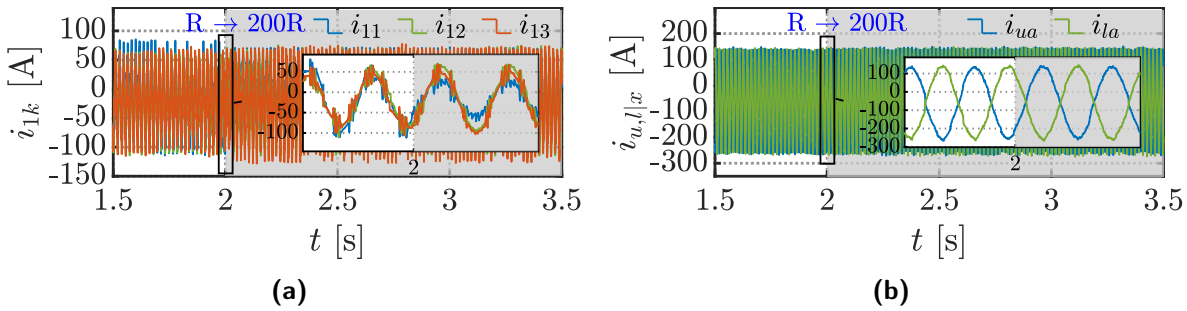

Figure 3.8 – Step change of the internal resistance of an interleaved inductor in phase a. Currents through interleaved legs of the submodule SM1a (a) and arm currents in phase a of ISM-MMC (b) [204]. © 2022 IEEE

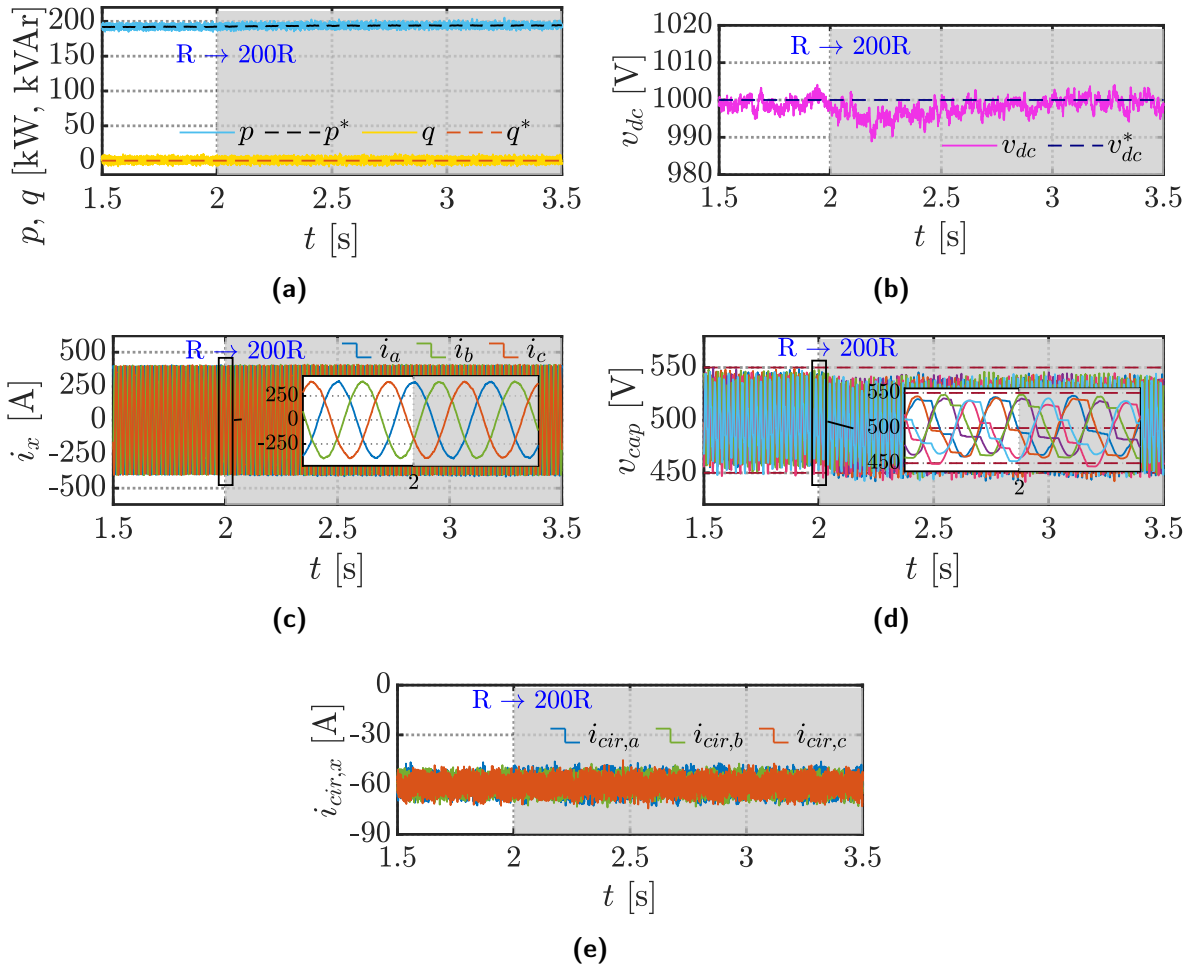

Figure 3.9 – Step change of the internal resistance of an interleaved inductor in phase a. Active and reactive powers (a) supplied by the grid (solid traces) along with their reference values (dashed lines); dc-link voltage (b) – measured value (solid trace) and its reference (dashed trace); ac phase currents (c); capacitor voltages (d) from each submodule of the upper arm of ISM-MMC (solid traces) along with their ±10% tolerance band and mean value (dashed lines); (e) phase leg common-mode currents [204]. © 2022 IEEE

by classical capacitor voltage balancing sorting algorithms that operate with firing signals. On the other hand, the proposed "Sort & Split" technique allows splitting a reference arm voltage into submodule normalized reference voltages (e.g., u^*_{ua1k} and u^*_{ua2k}) before the modulation

block. These SM reference voltages maintain volt-second balance within a fundamental period. In Figure 3.7 one may notice that when one of the submodule is commutating the other one is clamped either to zero or to the level maximum. It should be mentioned that the waveform of SM reference voltages strongly depends on sorting frequency (f_{sort}).

To demonstrate how the system behaves with different interleaved inductor parameters, two simulation tests were performed. In the first one, the system experiences a step-like 200-times increase in the internal resistance of a single interleaved inductor in phase a (cf. Figure 3.8 and Figure 3.9). Such significant resistance step is required to create a noticeable change in interleaved current amplitude (blue trace in Figure 3.8). Due to active-duty cycle adjustment the effect of smaller changes will be invisible. It also must be noted that selected nominal resistance of interleaved inductors has the same order of magnitude with typical value of equivalent on-state resistance of the active switches. For this reason, smaller resistance steps have minor effect in equivalent resistance of the circuit. From Figure 3.8a one may notice a reduction of the interleaved current amplitude (i_{11}) at the change point of 2 s, while the other two (i_{12}, i_{13}) slightly increase, remaining symmetrical around the present dc component. Obviously, to draw an interleaved current in high-impedance path is not a trivial task for the proportional controller, however, it keeps the fundamental components of all interleaved currents of that submodule sinusoidal-like and around their average dc component, compensating for all current imbalances that originate from upstream control actions (compare with Figure 2.23a). From this point of view it fulfils its main task. On the other hand, Figure 3.8b proves that unequal distribution of interleaved currents in one submodule does not affect the corresponding arm current. Furthermore, profiles of input ac power and three-phase currents (cf. Figures 3.9a and 3.9c) have no visible effect of the introduced resistance increase. Instead, capacitor voltages experience a small drop of their average value due to increased equivalent resistance of the circuit (cf. Figure 3.9d). Also, a tiny drop of dc-link voltage (v_{dc}), visible in Figure 3.9b, is cleared after 1 s. A slight increase of ripple amplitude is noticeable in Figure 3.9e. All in all, the system operation is stable, despite the performed change.

The second test is related to a similar step change, but this time it is a 10-times drop of inductance in one interleaved inductor of phase a (cf. Figures 3.10 and 3.11). For the sake of clarity, component's parameters have been set disregarding their standard manufacturing tolerances. The shaded area in the plots of this section indicates the time duration of the performed step change.

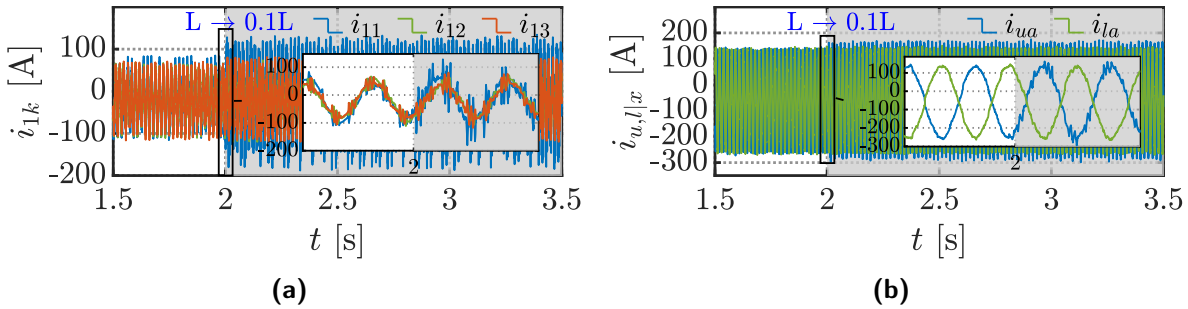

Figure 3.10 – Step change of the inductance of an interleaved inductor in phase a. Currents through interleaved legs of the submodule SM1a (a) and arm currents in phase a of ISM-MMC (b) [204]. © 2022 IEEE

Unlike the internal resistance growth (cf. Figures 3.8 and 3.9), the inductance reduction of an interleaved inductor does not change the fundamental component's amplitude. Therefore, there are no related problems with interleaved current imbalances within a SM. Instead, a

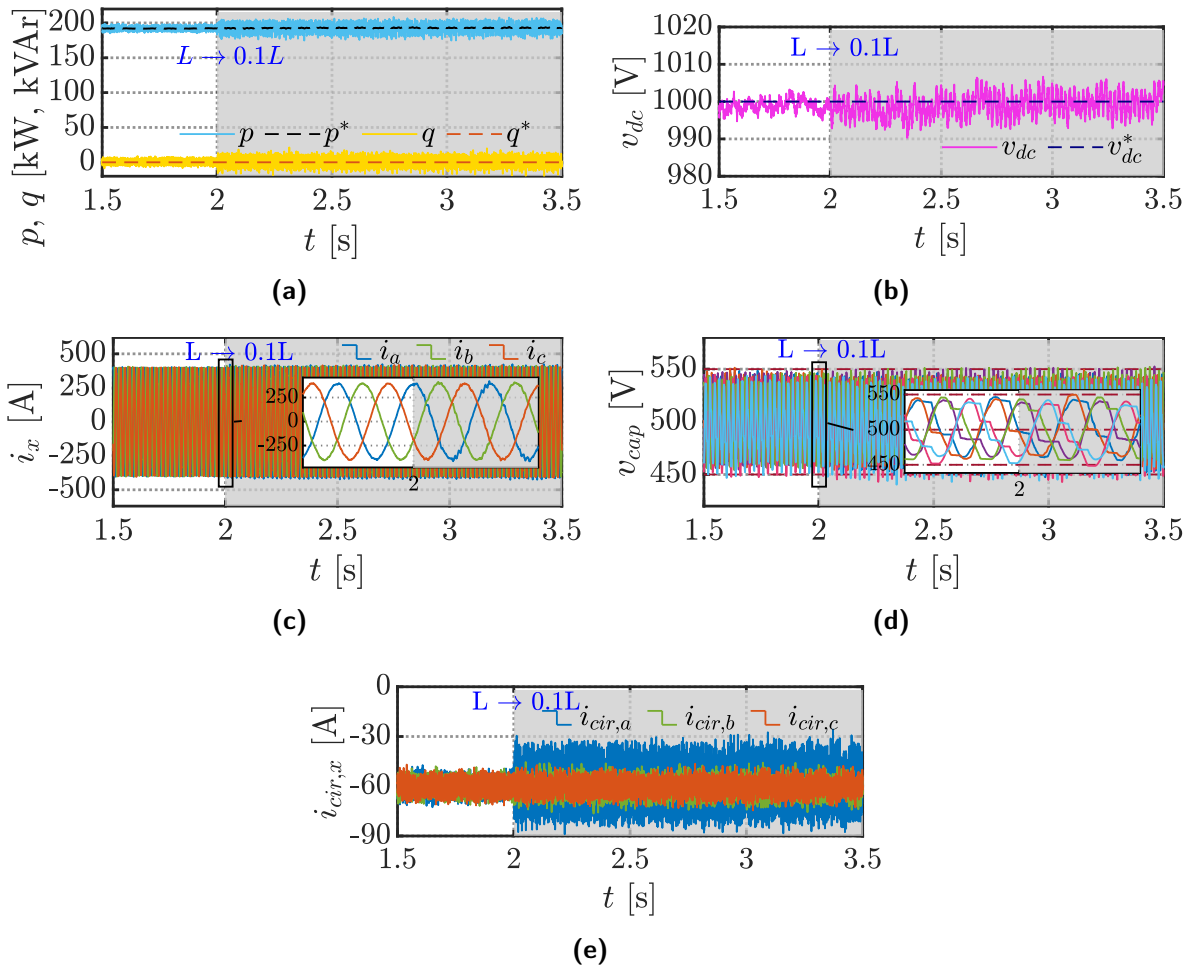

Figure 3.11 – Step change of the inductance of an interleaved inductor in phase a. Active and reactive powers (a) supplied by the grid (solid traces) along with their reference values (dashed lines); dc-link voltage (b) – measured value (solid trace) and its reference (dashed trace); ac phase currents (c); capacitor voltages (d) from each submodule of the upper arm of ISM-MMC (solid traces) along with their ±10% tolerance band and mean value (dashed lines); (e) phase leg common-mode currents [204]. © 2022 IEEE

smaller inductance value of the interleaved inductor produces a higher magnitude switching ripple. Having that ripple not canceled out within a SM (cf. Figure 3.10a), it propagates on the corresponding arm current (cf. Figure 3.10b) and further. While ac currents (cf. Figure 3.11c), input power (cf. Figure 3.11a) and dc-link voltage (cf. Figure 3.11b) get slightly disturbed, the leg's common-mode current is greatly affected due to the higher presence of switching ripple. However, similar to the previous test, such parameter inequality does not introduce instability problems into the conversion system. Eventually, it can be concluded that standard manufacturing tolerances of the interleaved inductors will not affect the stable operation of the ISM-MMC.

3.6 Experimental Tests

The experimental tests were carried out to verify the dynamic and steady-state behavior of ISM-MMC, operating with newly proposed control methods. Figure 3.12 depicts circuit dia-

gram of the laboratory setup arrangement, assembled specifically for the current experiment. Detailed description of the test bench along with summary of main parameters can be found in Appendix B. Here necessary comments to the setup configuration in relation to the conducted experiment is given only.

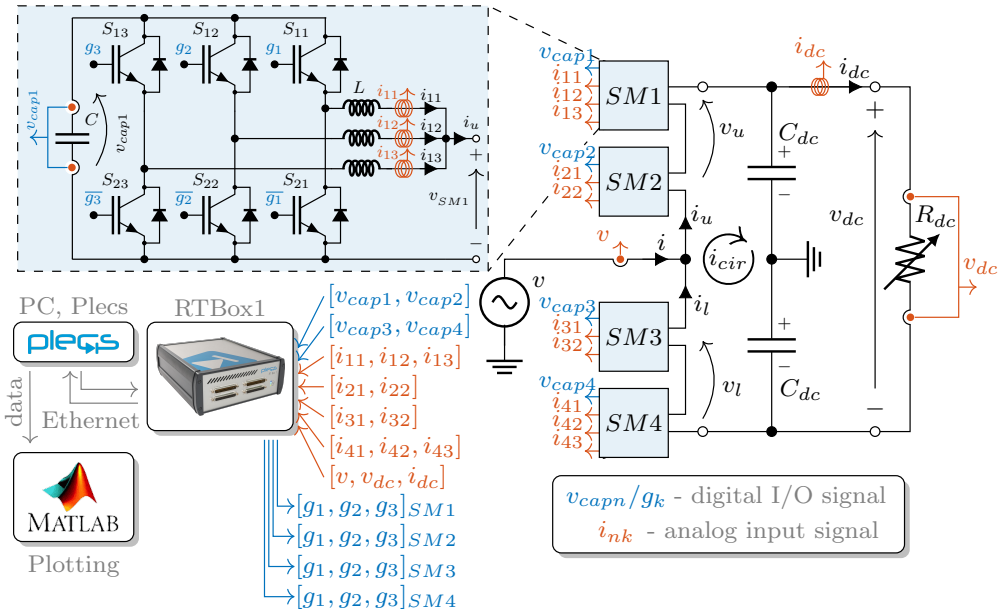

Figure 3.12 – Circuit diagram of the laboratory test ISM-MMC setup [204]. © 2022 IEEE

The laboratory ISM-MMC has a single-phase structure with two SMs per arm. Each submodule consists of a three-leg converter connected to a capacitor (C) at its dc side, while ac terminals are linked with uncoupled iron-core inductors (L). The second terminal of the inductors is joined together, forming a positive port of the SM. The negative port of the SM is directly connected with the negative dc rail of the three-leg converter. This setup arrangement was assembled in a such way that currents in each HB-leg of a SM were sensed individually. Measured voltages and currents enter controller (RT Box 1) either as analog (marked in red, Figure 3.12) or digital (marked in blue, Figure 3.12) signals. The rest quantities of interest (e.g., arm currents, leg's common-mode current, etc.) are computed via common circuit laws. The digital outputs of RT Box 1 are used to generate firing PWM signals (g_k) for the power switches. The controller operates with a maximum sampling period of 20 μs. The acquired signals were sampled with the same sampling time and transmitted to the PC for following post-processing (figures plotting) in Matlab environment (MathWorks Inc.).

Several experiments were performed to confirm the stable operation of ISM-MMC under input/output characteristics variation and the interleaved current control perturbation. The first test demonstrates the system response after a dc current step from 0 to 3 A. In this experiment, the implemented interleaved currents balancing control was constantly active.

Figure 3.13 illustrates the main input/output and internal characteristics of the ISM-MMC, namely instantaneous active and reactive powers supplied by the grid emulator along with their references, ac phase current, dc-link voltage, and its reference capacitor voltage of the composing SMs. The transient of dc-link voltage caused by the dc current step is cleared around 3 s, while steady-state values exhibit a clean and well-balanced response.

The interleaved legs currents of the submodule SM2 and arm current of the converter are depicted in Figure 3.14. It is visible from Figure 3.14a that fundamental components of the

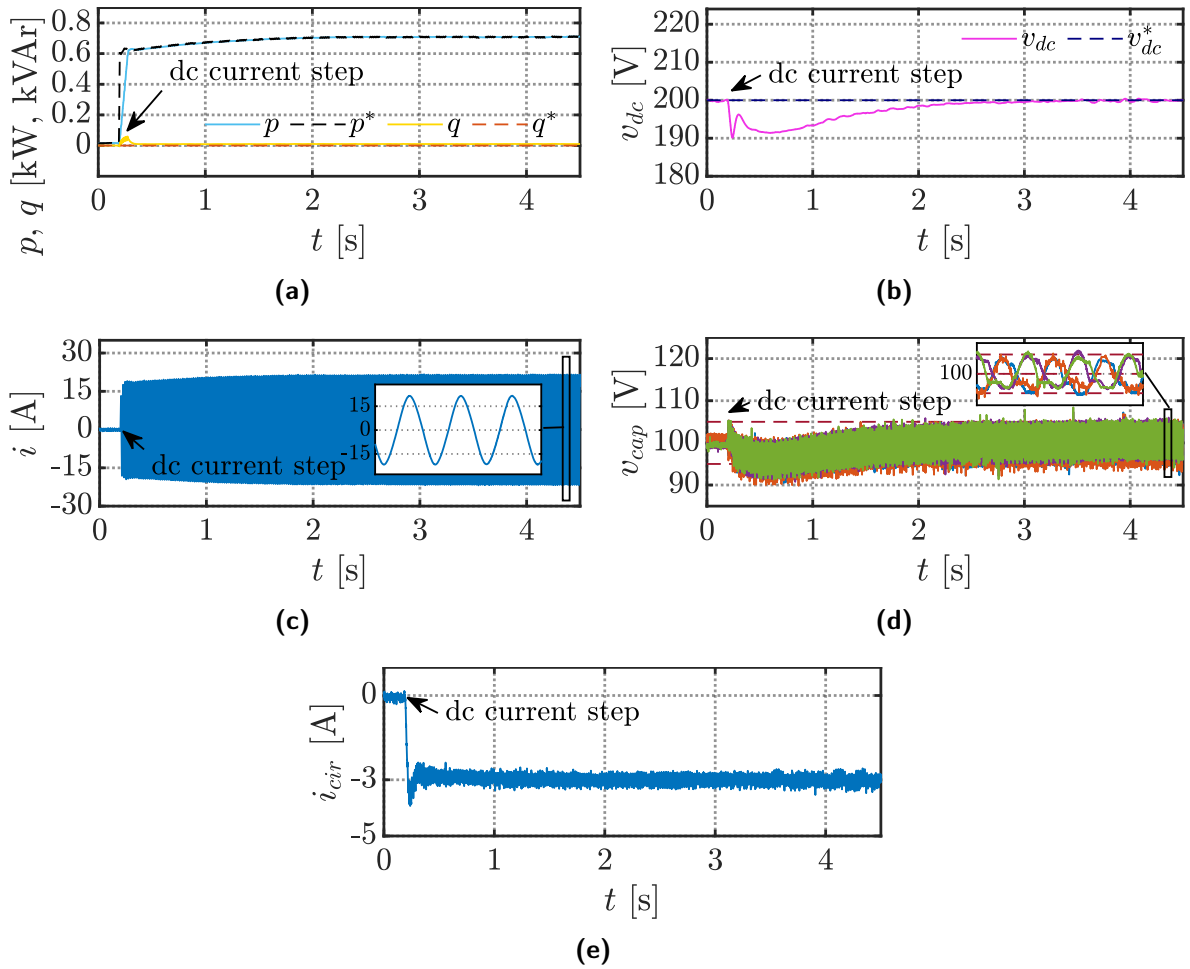

Figure 3.13 – Dc current step. Active and reactive powers (a) supplied by the grid (solid traces) along with their reference values (dashed lines); dc-link voltage (b) – measured value (solid trace) and its reference (dashed trace); ac phase current (c); capacitor voltages (d) from each submodule of ISM-MMC (solid traces) along with its ±5% tolerance band and mean value (dashed lines); (e) phase leg common-mode current [204]. © 2022 IEEE

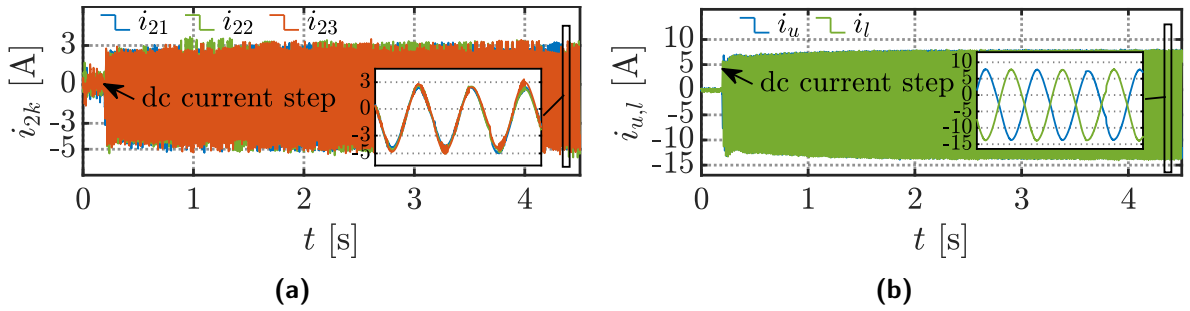

Figure 3.14 – Dc current step. Currents through interleaved legs of the submodule SM2 (a) and arm currents of ISM-MMC (b) [204]. © 2022 IEEE

currents through interleaved legs are well balanced at all times during the transient and steady-state operation. Similarly, the arm currents in Figure 3.14b are level-headed.

Similarly, Figure 3.15 and Figure 3.16 illustrate the system response after a dc voltage step from 200 to 170 V. Again, all measures show clean and well-balanced feedback.

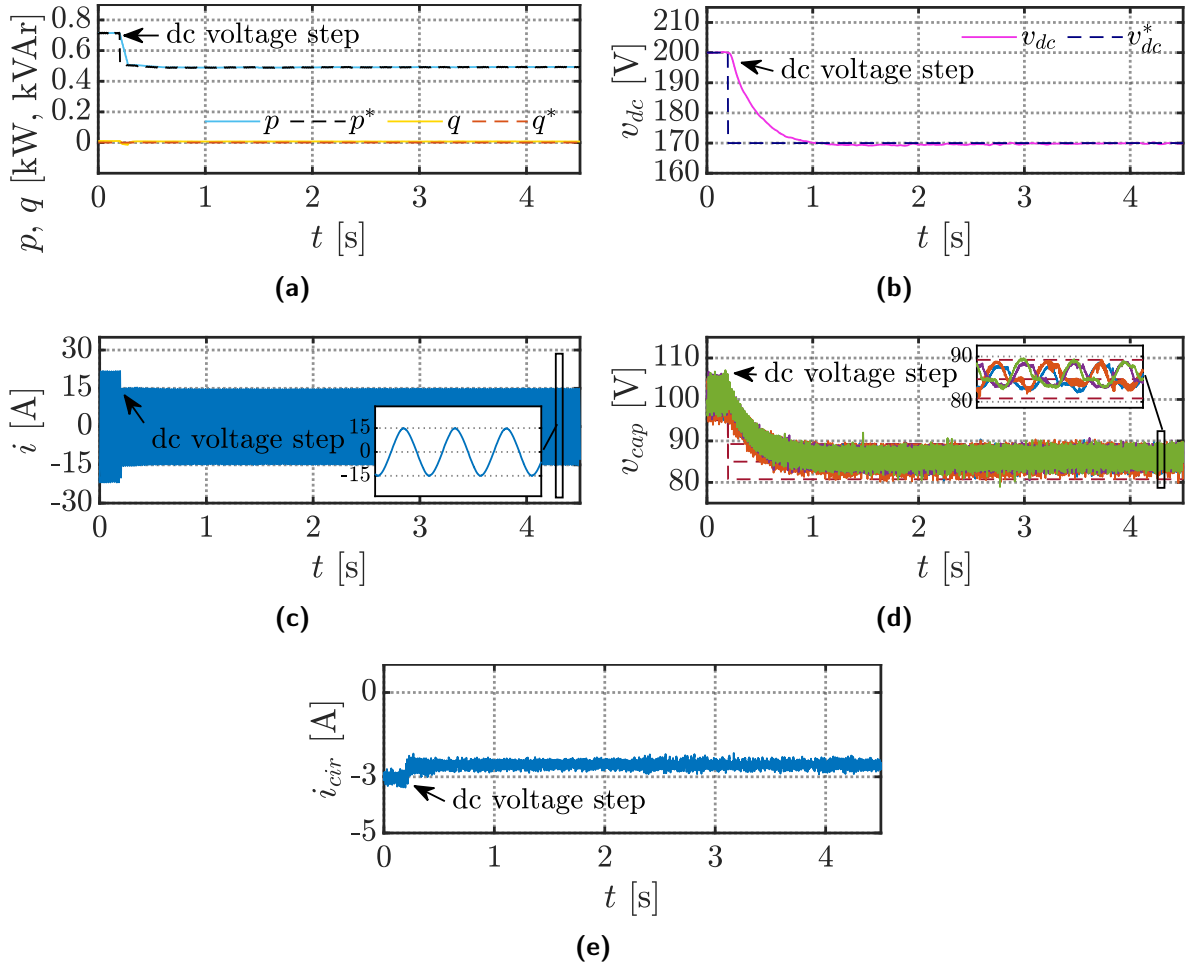

Figure 3.15 – Dc voltage step. Active and reactive powers (a) supplied by the grid (solid traces) along with their reference values (dashed lines); dc-link voltage (b) – measured value (solid trace) and its reference (dashed trace); ac phase current (c); capacitor voltages (d) from each submodule of ISM-MMC (solid traces) along with its ±5% tolerance band and mean value (dashed lines); (e) phase leg common-mode current [204]. © 2022 IEEE

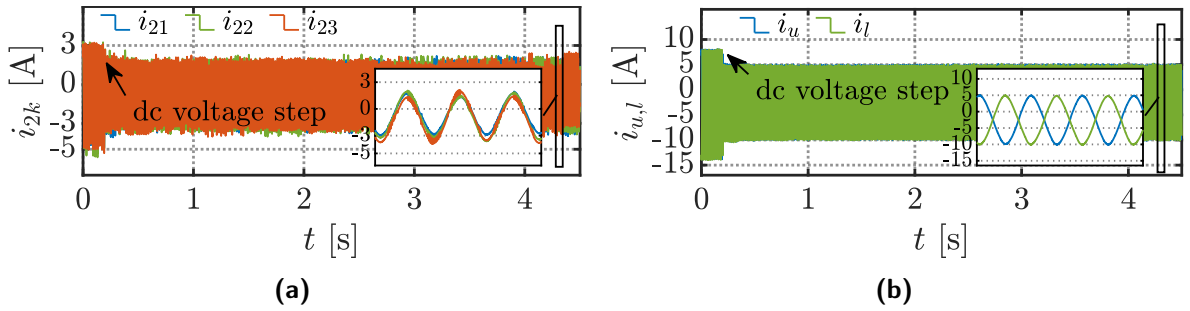

Figure 3.16 – Dc voltage step. Currents through interleaved legs of the submodule SM2 (a) and arm currents of ISM-MMC (b) [204]. © 2022 IEEE

The following experiment, results of which are depicted in Figures 3.17 and 3.18, was conducted to prove the stable converter operation under grid voltage perturbations, namely a phase voltage dip by 10% of the nominal value. In fact, a sudden reduction of supply voltage from 50 to 45 V has been accompanied by a proportional increase of ac current (cf. Figure 3.17c), which eventually produced a current rise in the converter arms (cf. Figure 3.18b) and interleaved legs

of each SM (cf. Figure 3.18a). As it can be noted the transient has been cleared shortly after the step and all characteristics are well balanced in steady-state condition.

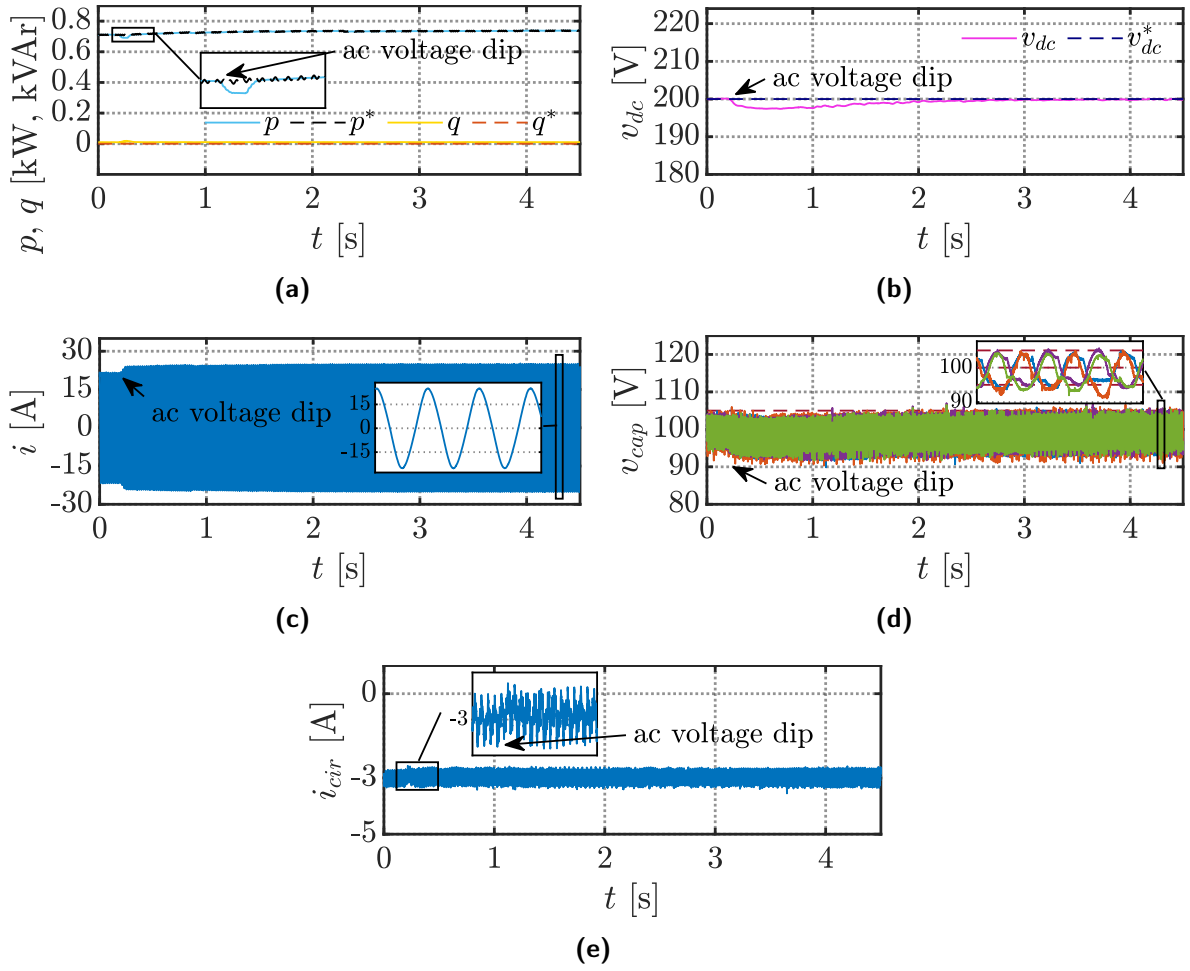

Figure 3.17 – Ac voltage dip. Active and reactive powers (a) supplied by the grid (solid traces) along with their reference values (dashed lines); dc-link voltage (b) – measured value (solid trace) and its reference (dashed trace); ac phase current (c); capacitor voltages (d) from each submodule of ISM-MMC (solid traces) along with its ±5% tolerance band and mean value (dashed lines); (e) phase leg common-mode current [204]. © 2022 IEEE

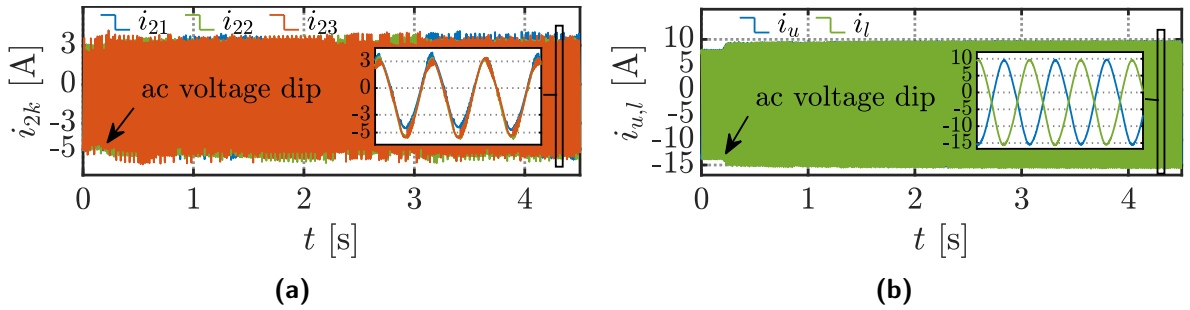

Figure 3.18 – Ac voltage dip. Currents through interleaved legs of the submodule SM2 (a) and arm currents of ISM-MMC (b) [204]. © 2022 IEEE

Another test was performed to demonstrate what happens if the interleaved current balancing control is disabled in one SM. The shaded (grey) area in Figures 3.19 and 3.20 highlights the time period when the interleaved current balancing control is off. As one may note, the input/output

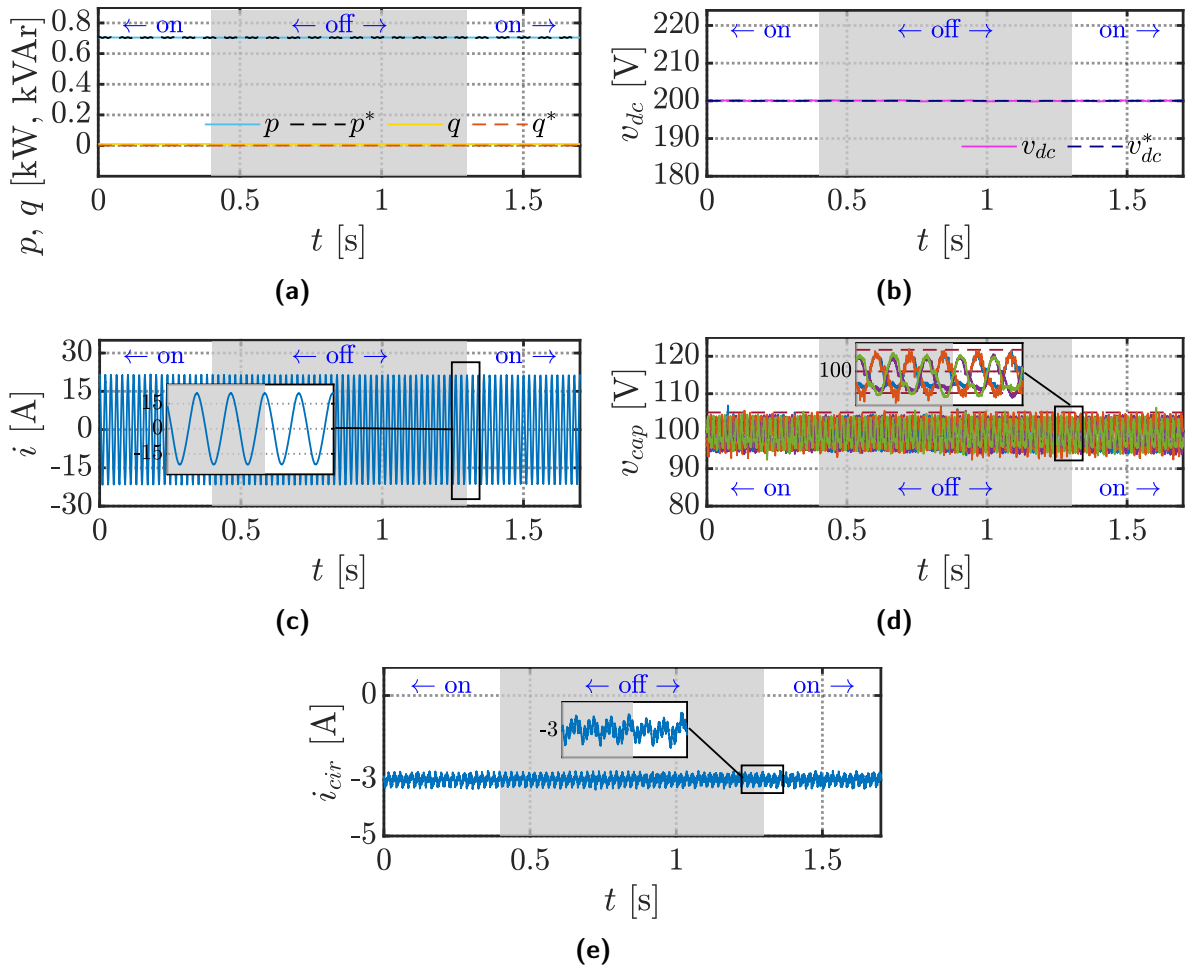

Figure 3.19 – Interleaved currents balancing enable/disable. Active and reactive powers (a) supplied by the grid (solid traces) along with their reference values (dashed lines); dc-link voltage (b) – measured value (solid trace) and its reference (dashed trace); ac phase current (c); capacitor voltages (d) from each submodule of ISM-MMC (solid traces) along with its ±5% tolerance band and mean value (dashed lines); (e) phase leg common-mode current [204]. © 2022 IEEE

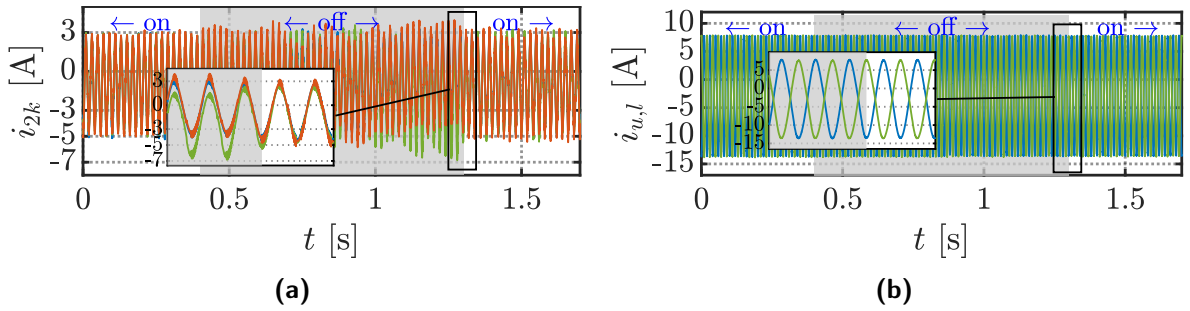

Figure 3.20 – Interleaved currents balancing enable/disable. Currents through interleaved legs of the submodule SM2 (a) and arm currents of ISM-MMC (b) [204]. © 2022 IEEE

characteristics of the converter are not affected, supplied ac power, ac phase current, and dc-link voltage have no visible effect between "on" and "off" stages of the interleaved control. Similarly, capacitor voltage in SMs does not notice the control perturbation. On the contrary, as soon as the interleaved control in one SM is off, the currents within this SM get unbalanced. This effect is well visible in Figure 3.20a the current perturbations are well damped by relatively

high equivalent resistances of HB-assemblies inside the SM. There are several reasons for the currents to get imbalanced. The obvious one is non-equalities among aforementioned equivalent resistances of a single leg circuit (internal resistances of the interleaved inductors, on-state resistances of the switches, etc.). Another reason has been described in Section 3.2, and it relates to the operation of the upstream capacitor voltage balancing algorithm. Nevertheless, as soon as the operation of the interleaved current control is resumed, the currents within the SM get balanced again. Interestingly, the arm current is invariant to the control perturbation since the sum of the unbalanced currents within the SM results in a balanced arm current anyway.

All in all, performed tests demonstrate the expected behavior of the converter under various system perturbations.

3.7 Summary

This chapter is dedicated to a newly proposed interleaved currents balancing strategy in ISM-MMC structures. It has been shown that the interleaved current imbalance can originate not only from hardware-related causes, such as circuital parameters variance, unequal dead-times, etc., but also from the actions of the capacitor voltage balancing loop that is typically present in all MMC-based architectures. Therefore, a method that guarantees proper currents sharing among interleaved HB-legs within a SM is essential in ISM-MMCs. To ensure the precise current balancing, the new control loop must be placed as a ultimate control task in the whole control frame. Following this idea, a new capacitor balancing algorithm was introduced in this chapter. The proposed capacitor balancing method from one side resembles the classical capacitor voltage balancing function, typically implemented in standard MMCs in conjunction with LS-PWM, while operates with voltage references rather then with firing signals. In this way, subsequent control tasks, which relay on voltage reference adjustments, can be implemented downstream. The proposed interleaved current balancing control has distributed structure and implemented individually for each SM in ISM-MMC. It is formed by a simple feedback loop where knowledge about each interleaved current is required. The effectiveness of the proposed control strategy was extensively verified by a numerous of numerical simulations and experimental test, which are performed on the laboratory prototype. Some of them are presented in this chapter. The dynamic behaviour of the introduced control loop as well as performance of the whole system was investigated by imposing step-like perturbation in the input/output quantities of the converter. In addition to that functioning of the converter was investigated with enabled and disabled interleaved current balancing loops. The presented results demonstrate importance of the new regulator in the frame of classical MMC control applied for ISM-MMC and validate its stable, robust operation.

Chapter 4

Sensorless Interleaved Currents Balancing Control

4.1 Introduction

Most of the conventional ways to solve unequal current sharing among parallel units in power converters are based on sensing each unit current to provide the information for the dedicated active control loop. This approach is well established for dc/dc [205, 209] and some ac/dc converters [207]. A similar method was proposed in [204] for an ISM-MMC and has been scrupulously explained in Chapter 3. An obvious drawback of these current balancing methods is the large number of current sensors that is almost proportional to the number of parallel/interleaved units. To compact the converter and reduce its cost and complexity, several current estimation techniques have been developed for interleaved dc/dc converters, based on parasitic resistance estimation [210], small-signal duty cycle perturbation [211], self-tuning digital filter [212], temperature equalization [213] and many other. Similarly, several works have been dedicated to estimation algorithms to deal with another common balancing problem for MMC structures, namely capacitor voltage balancing. For instance, authors in [214] proposed a current sensorless capacitor voltage balancing method based on a state observer. The observer provides estimates of arm currents that are typically used in most capacitor voltage balancing algorithms.

Since ISM-MMC has been just recently introduced, very few works are dedicated to this topology. Thus, to the best of the author's knowledge, no publications apart from [215] have been focused on estimating the interleaved currents in ISM-MMCs. This chapter is devoted to the aforementioned technique, that upgrades the interleaved current balancing control presented in Chapter 3. Therefore, the main contribution of the current chapter is the implementation of a sensorless current balancing method for ISM-MMC that is capable to evenly allocate interleaved HB-leg currents, while purely relaying on their estimation. In this context, the word "sensorless" means that there are no interleaved currents measurements needed. The sensorless solution, in general, requires a computation-intensive estimation algorithm that can be sensitive to parameter variation. Moreover, the estimation method must run in real-time in order to get the estimated values at the proper instant. In this chapter, it is also demonstrated that even though the circuital parameter variation affects performance of the implemented observer, the current balancing method can still compensate for the current imbalance, which mainly originates

from the actions of the upstream capacitor voltage balancing strategy. Capabilities of the newly introduced observer and the implemented interleaved current control loop has been thoroughly investigated via numerous numerical simulations and experimental tests.

The required mathematical background of the proposed state observer is explained in Section 4.2. In this section, observability and stability of the implemented state estimator is discussed in great detail. The modified current balancing technique is discussed in Section 4.3. Sections 4.4 and 4.5 verify the usefulness of the proposed current sharing technique by presenting simulation and experimental results, respectively. In addition to that, some considerations about the observer's sensitivity concerning parameter variation, are highlighted there as well. Section 4.6 summarizes and concludes the chapter.

4.2 State Observer Design

To derive mathematical formulation of the proposed state estimator, some structural fundamentals of ISM-MMC must be refreshed. As depicted in Figure 4.1, a single-phase ISM-MMC consists of two arms; each one of them comprises a series connection of switching cells, referred to as submodules. The submodules are formed using multiple half-bridge converters (units) connected in parallel to a common dc capacitor (C). Inductors (L) are used to connect each half-bridge converter to a common point, which forms a positive terminal of the submodule. The second terminal of the submodule constitutes the negative dc rail. Resistances (R) placed in series with inductors represent equivalent series resistances of each branch. For the following analysis, parameters (R, L, C) in all N submodules and in all K units are assumed to be identical among themselves, unless otherwise stated.

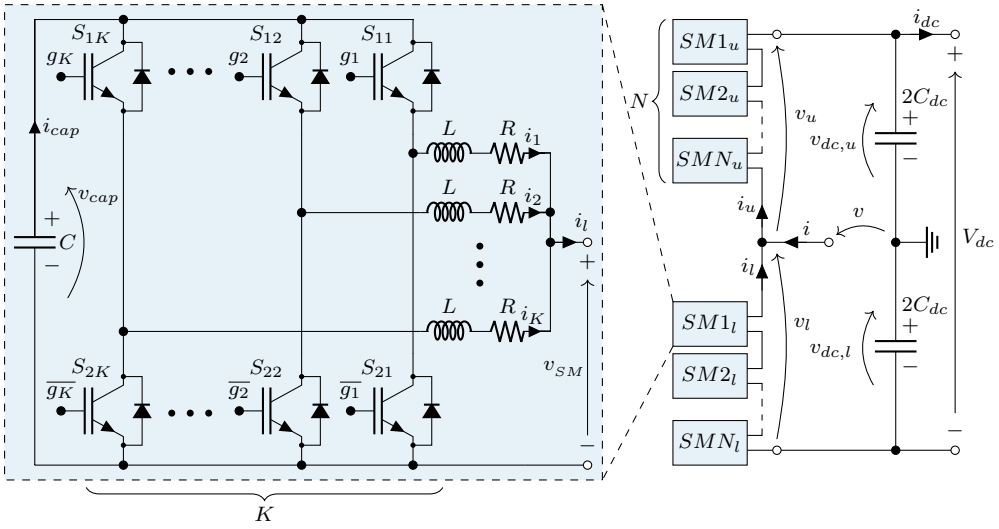

Figure 4.1 – Circuit diagram of a single-phase ISM-MMC [215]. © 2022 IEEE

The whole derivation process makes reference to Figure 4.1 with predefined path of current flow. However, it should be noted that observer design is identical regardless the direction of current flow. In this regard, the derivation is made for a specific case for clarity only. With respect to Figure 4.1, the voltage of a generic n-th submodule can be written as

$$v_{SMn} = \frac{1}{K}\left[v_{cap,n} \underbrace{\sum_{k=1}^{K} g_{n,k}}_{\zeta_n} - L \sum_{k=1}^{K} \frac{di_{n,k}}{dt} - R \sum_{k=1}^{K} i_{n,k} \right] \tag{4.1}$$

where $i_{n,k}$, $g_{n,k}$, $v_{cap,n}$, v_{SMn} and ζ_n are the current flowing in the k-th interleaved unit, switching functions (binary values), submodule's capacitor voltage, submodule's terminal voltage and number of active half-bridge legs in n-th submodule, respectively. By applying the second Kirchhoff's law for a generic half-bridge unit within the SM, derivative of the current, flowing through the branch, can be found by

$$\frac{di_{n,k}}{dt} = \frac{1}{L}\left[v_{cap,n} g_{n,k} - R i_{n,k} - v_{SMn} \right] \tag{4.2}$$

Current passing through the n-th SM's capacitor ($i_{cap,n}$) at any instant can be determined either from the capacitor equation or as an active legs' current summation:

$$i_{cap,n} = -C\frac{dv_{cap,n}}{dt} = \sum_{k=1}^{K} (i_{n,k} g_{n,k}) \tag{4.3}$$

Therefore, from Equation (4.3) one can obtain the time derivative of the capacitor voltage as

$$\frac{dv_{cap,n}}{dt} = -\frac{i_{cap,n}}{C} = -\frac{1}{C}\sum_{k=1}^{K} (i_{n,k} g_{n,k}) \tag{4.4}$$

Summing up each single current derivative in Equation (4.2) evaluated for all active HB-legs (i.e., firing signals of upper switch in those legs $g_{n,k} = 1$) capacitor current time derivative in accordance with Equation (4.3) can be written as:

$$\frac{di_{cap,n}}{dt} = \underbrace{\frac{\zeta_n}{L}}_{1/L'} \left[v_{cap,n} - \underbrace{\frac{R}{\zeta_n}}_{R'} i_{cap,n} - v_{SMn} \right] \tag{4.5}$$

where R' and L' accordingly represent SM's equivalent resistance and inductance with respect to a number of active HB-legs. In other words, capacitor current can be referred to an equivalent branch current that accounts for all interleaved currents in ζ_n active HB-legs. Equations (4.4) and (4.5) form the basic set of equations that describe state variables ($v_{cap,n}$ and $i_{cap,n}$) of an equivalent n-th SM.

Observability

A system is said to be observable if the entire system's behavior can be estimated from the system's outputs, which are generally sensed. It can be noted from Equation (4.4) that the capacitor voltage, by means of the capacitor current, contains information about all interleaved currents that flow within the submodule. Therefore, by selecting capacitor voltage as an output of the system, the observability of the newly proposed state estimator can be verified based on any arbitrarily selected number of half-bridge units. Since in Equations (4.4) and (4.5) there

is no more dependency on the firing signals $g_{n,k}$, they can be transformed into the state-space representation for linear time-invariant (LTI) systems:

$$\begin{cases} \dot{\mathbf{x}} = \mathbb{A}\mathbf{x} + \mathbb{B}\mathbf{u} \\ \mathbf{y} = \mathbb{C}\mathbf{x} \end{cases} \tag{4.6}$$

where state, input and output vectors can be defined as $\mathbf{x} = [v_{cap,n}, i_{cap,n}]^T$, $\mathbf{u} = v_{SMn}$ and $\mathbf{y} = v_{cap,n}$, respectively. Matrices $\mathbb{A}$, $\mathbb{B}$ and $\mathbb{C}$ denote state, input, and output matrices, respectively. Replacing Equations (4.4) and (4.5) inside Equation (4.6), the state-space form can be rewritten as

$$\begin{cases} \dfrac{d}{dt}\begin{bmatrix} v_{cap,n} \\ i_{cap,n} \end{bmatrix} = \begin{bmatrix} 0 & -\dfrac{1}{C} \\ \dfrac{\zeta_n}{L} & -\dfrac{R}{L} \end{bmatrix}\begin{bmatrix} v_{cap,n} \\ i_{cap,n} \end{bmatrix} - \dfrac{\zeta_n}{L}\begin{bmatrix} 0 \\ 1 \end{bmatrix} v_{SMn} \\ v_{cap,n} = \begin{bmatrix} 1 & 0 \end{bmatrix}\begin{bmatrix} v_{cap,n} \\ i_{cap,n} \end{bmatrix} \end{cases} \tag{4.7}$$

The Kalman observability matrix $\mathbb{O}$, in the form

$$\begin{cases} \mathbb{O} = \begin{bmatrix} \mathbb{C} \\ \mathbb{C}\mathbb{A} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & -\dfrac{1}{C} \end{bmatrix} \end{cases} \tag{4.8}$$

has always full rank regardless the time varying nature of ζ_n. Therefore, as foreseeable, it is always possible observe states $v_{cap,n}$ and $i_{cap,n}$, having sensed the capacitor voltage only.

Carriers phase shift, associated with interleaved modulation scheme (cf. Section 2.5), has a crucial role in interleaved currents estimation since it opens a possibility, within each carrier period T_{cr}, to formulate multiple values of capacitor current (vector $\mathbf{I}_{cap,n|k}$) derived from corresponding vectors of HB-leg currents $\mathbf{I}_{n,k}$ bearing in mind HB-leg's active states (i.e., $g_{n,k} = 1$). If K capacitor currents related to a set of independent K-tuple gate signals $g_{n,k}$ can be identified, the vector of K HB-leg currents $\mathbf{I}_{n,k}$ can be reconstructed every switching period from the sole knowledge of the capacitor voltage $v_{cap,n}$. The latter statement can be formalized by stacking K times Equation (4.3) in the form

$$\underbrace{\begin{bmatrix} i_{cap,n|1} \\ i_{cap,n|2} \\ \vdots \\ i_{cap,n|K} \end{bmatrix}}_{\mathbf{I}_{cap,n|k}} = \underbrace{\begin{bmatrix} g_{n,1|1} & g_{n,2|1} & \cdots & g_{n,K|1} \\ g_{n,1|2} & g_{n,2|2} & \cdots & g_{n,K|2} \\ \vdots & \vdots & \ddots & \vdots \\ g_{n,1|K} & g_{n,2|K} & \cdots & g_{n,K|K} \end{bmatrix}}_{\mathbb{G}_k} \underbrace{\begin{bmatrix} i_{n,1} \\ i_{n,2} \\ \vdots \\ i_{n,K} \end{bmatrix}}_{\mathbf{I}_{n,k}} \tag{4.9}$$

where each row represents a different capacitor current composition, depending on the binary states of high switch in each HB-leg. The latter term composes matrix $\mathbb{G}_k$.

If the duty cycle δ given by the modulating signal stays below $1/K$ level, it is always possible to rewrite matrix $\mathbb{G}_k$ as the identity matrix. On the other hand, if the duty cycle δ attain values above $(K-1)/K$ level, the matrix $\mathbb{G}_k$ converts into a matrix of ones with the main diagonal made of zeros. For all the remaining values of duty cycle δ, the Hamming space of gate signals K-tuple is characterized by non-repetitive configurations, which sequentially permutate with unity Hamming distance. Therefore, it is always possible to find K set of independent K-tuple gate signals $g_{n,k}$. In other words, regardless of the number of interleaved half-bridges, at least

one invertible matrix $\mathbb{G}_k$ can be identified every switching period. Hence, being Equation (4.9) solvable at any time instant, the observability of each interleaved current with aforementioned state variables can always be guaranteed.

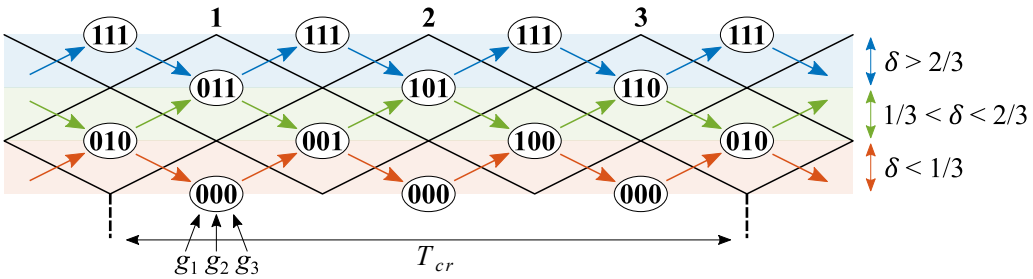

Figure 4.2 – SM's interleaved carriers and their Hamming space in case of $K = 3$ [215]. © 2022 IEEE

These considerations are intuitively depicted in Figure 4.2 for a submodule having three half-bridges ($K = 3$). It clearly stands out that a SM is observable only in the occurrence of switching actions. Interleaved currents in bypassed or fully inserted submodules with all the gate signals of upper switches in HB-legs either equal to 0 or 1 are not observable with above mentioned state variables (at least within a generic switching period).

Observer

The state observer model of a physical LTI system can be represented by

$$\begin{cases} \dot{\hat{\mathbf{x}}} = \mathbb{A}\hat{\mathbf{x}} + \mathbb{B}\mathbf{u} + \mathbb{L}(\mathbf{y} - \hat{\mathbf{y}}) \\ \hat{\mathbf{y}} = \mathbb{C}\hat{\mathbf{x}} \end{cases} \tag{4.10}$$

where $\hat{\mathbf{x}}$ and $\hat{\mathbf{y}}$ are estimates of the corresponding plant's state and output. Matrix $\mathbb{L}$ comprises observer gains.

By substituting Equations (4.4) and (4.5) into Equation (4.10) and denoting variables of matrix $\mathbb{L} = [l_v, l_i]$, the following equations can be derived

$$\frac{d\hat{v}_{cap,n}}{dt} = -\frac{\hat{i}_{cap,n}}{C} + l_v(v_{cap,n} - \hat{v}_{cap,n}) \tag{4.11}$$

$$\frac{d\hat{i}_{cap,n}}{dt} = \frac{\zeta_n}{L}\left[v_{cap,n} - \frac{R}{\zeta_n}\hat{i}_{cap,n} - v_{SMn}\right] + l_i(v_{cap,n} - \hat{v}_{cap,n}) \tag{4.12}$$

being $\hat{v}_{cap,n}$ and $\hat{i}_{cap,n}$ estimates of capacitor voltage and current, respectively. By analyzing Equation (4.12), one may notice that the knowledge of submodule voltage is required to derive the state of the capacitor current. Although this voltage can be measured directly, such an approach requires to double number of voltage sensors in ISM-MMC in comparison with classical MMCs, which is not an optimal solution from many perspectives (cost, volume, etc.), including a concern about sufficient bandwidth of the voltage sensors. Thus, the voltage can be derived indirectly from Equation (4.1), bearing in mind that the sum of interleaved currents inside an SM is actually the arm current (cf. Equation 2.8), resulting in the following expression of SM voltage

$$\hat{v}_{SMn|u,l} = \frac{1}{K}\left[v_{cap,n|u,l} \cdot \zeta_{n|u,l} - L\frac{di_{u,l}}{dt} - Ri_{u,l}\right] \tag{4.13}$$

Estimate sign ("hat") is added to submodule voltage in Equation (4.13) to point out that it is indirectly obtained based on sensed capacitor voltage and arm current. It should be noted that the arm current sensors are required in addition to typical capacitor voltage measurements. Nevertheless, the arm currents are commonly measured in MMC structures (depending on the control design). It also must be highlighted that the considered in Equation (4.13) equivalent circuit parameters (R/K, L/K) are rated values and likely to be different in a real system. However, the voltage drops accounted by the parameters in Equation (4.13) have significantly lower magnitude with respect to the capacitor voltage ($v_{cap,n}$). In addition, variation of real circuitry parameters is generally limited by manufacturing tolerances, which are in the range of few tens of percent. Therefore, the reconstructed SM voltage has quite a good accuracy with respect to the actual value, and it can be treated as an independent variable in Equation (4.12).

Having the estimates of capacitor current in each SM's switching configuration, the HB-leg currents with reference to Equation (4.9) can be derived by

$$\mathbf{I}_{n,k} = \mathbb{G}_k^{-1}\mathbf{I}_{cap,n|k} \tag{4.14}$$

Stability of the Observer

Considering definition of the estimated model (capacitor voltage and current) given by Equations (4.11), (4.12) and subtracting it from the plant's model formulated by Equations (4.4) and (4.5), the observation error dynamics has the following form:

$$\frac{d\tilde{v}_{cap,n}}{dt} = -\frac{\tilde{i}_{cap,n}}{C} - l_v\tilde{v}_{cap,n} \tag{4.15}$$

$$\frac{d\tilde{i}_{cap,n}}{dt} = -\frac{R}{L}\tilde{i}_{cap,n} - l_i\tilde{v}_{cap,n} \tag{4.16}$$

where $\tilde{v}_{cap,n} = v_{cap,n} - \hat{v}_{cap,n}$ and $\tilde{i}_{cap,n} = i_{cap,n} - \hat{i}_{cap,n}$ are observation errors of capacitor voltage and current, respectively.

The stability of the designed observer (i.e., the trajectories of estimates do not diverge from their corresponding real values) can be formulated by exhibiting a Lyapunov function that corresponds to the energy in the increment with respect to an arbitrary, nominal state trajectory. For the observer, the energy in the increment takes the form [216]:

$$W_\varepsilon = \frac{1}{2}C\tilde{v}_{cap,n}^2 + \frac{L}{2\zeta_n}\tilde{i}_{cap,n}^2 \tag{4.17}$$

which is clearly positive definite function. Its derivative is

$$\dot{W}_\varepsilon = C\tilde{v}_{cap,n}\dot{\tilde{v}}_{cap,n} + \frac{L}{\zeta_n}\tilde{i}_{cap,n}\dot{\tilde{i}}_{cap,n} \tag{4.18}$$

By substituting Equations (4.15) and (4.16) into Equation (4.18) yields

$$\dot{W}_\varepsilon = -l_vC\tilde{v}_{cap,n}^2 - \frac{R}{\zeta_n}\tilde{i}_{cap,n}^2 - (1 + l_i\frac{L}{\zeta_n})\tilde{v}_{cap,n}\tilde{i}_{cap,n} \tag{4.19}$$

where circuital parameters (R, L, C), number of active half-bridge legs ζ_n and observer gains (l_v, l_i) are strictly positive real numbers. In Equation (4.19), the first two terms are negative definite, while the last term bounded and can be either positive or negative. Therefore, selecting relatively

large l_v and reasonable l_i can ensure $\dot{W}_\varepsilon < 0$, which will force the observation error converge to zero.

4.3 Modified Interleaved Currents Balancing Control

This section explains a few modifications, which are introduced into the interleaved current balancing method for ISM-MMC (cf. Chapter 3). Figure 4.3 depicts a block diagram of the proposed current balancing scheme. There are few steps to obtain estimated values of interleaved currents that are typically used in the feedback loop of the proportional controller. The very first step is to compute submodule voltage (cf. Equation (4.13)) based on measured values of arm current, capacitor voltages and known set of firing signals. At the same time, an estimate of each capacitor voltage must be obtained based on Equations (4.9) and (4.11). Eventually, both those quantities enter the interleaved current prediction block formed by Equations (4.9), (4.12) and (4.14). Later all individual current derivatives are integrated to obtain estimated interleaved currents for each SM. A proportional controller with gain $k_{p,intlv}$ computes voltage reference increments that must be added to the set of identical SM voltage references created to modulate each HB-leg separately (cf. Chapter 3).

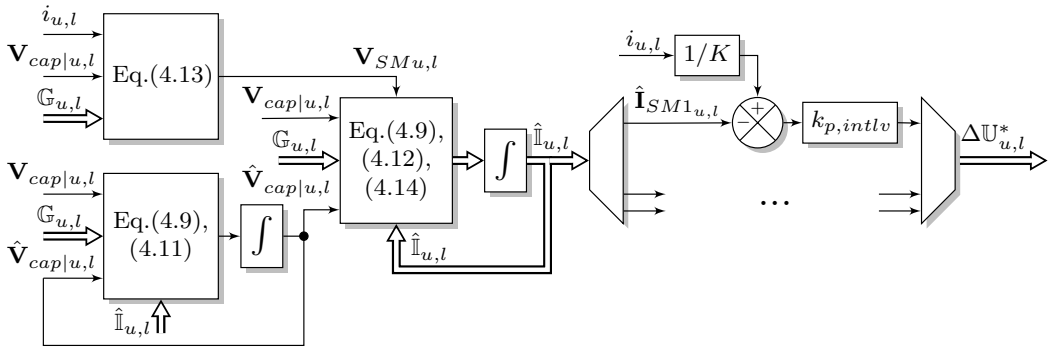

Figure 4.3 – Block diagram of the proposed state observer-based interleaved legs current balancing control [215]. © 2022 IEEE

The implemented sensorless interleaved legs current balancing control has the objective to balance fundamental components of the interleaved currents within a single SM, naturally unbalanced due to upstream control actions. Hence, it is an individual, SM-level control method. With the rise of the number of SM, the computation burden on a controller will increase proportionally. Therefore, an efficient hardware realization of the control constitutes an optimization problem. This discussion falls outside the scope of this thesis. Given that the observer part (cf. Equations (4.11), (4.12) and (4.13)) has only a few derivatives and integrals to compute, as well as the switching frequency of individual semiconductors in ISM-MMCs usually tend to be up to a few kHz; hence the controller has sufficient time to compute and update the estimates in one PWM cycle. In this context, most of the entry-level microcontrollers will satisfy the computation requirement of the presented current balancing method.

4.4 Numerical Simulations

This section presents some simulation results that aim to validate the performance of the implemented state observer and the interleaved legs current sensorless balancing method.

It must be stressed once again here, that this control loop's primary objective is to balance individual interleaved currents in each HB-leg around their average value given the current imbalance because of capacitor voltage balancing. So, the main focus here is whether the built interleaved current regulator can balance the currents or not. To validate this matter, the simulation model involves a simple single-phase ISM-MMC structure with two SMs per arm ($N = 2$) and three interleaved HB-legs within each SM ($K = 3$) (cf. Figure 4.1). The converter works as an inverter supplying power from dc to ac side connected to a constant, passive load. The converter is regulated with output current open-loop control by setting desired reference phase voltage manually with limit of 353.6 V (rms) in linear modulation range. The internal control loops, namely circulating current control and capacitor voltage balancing, are always activated to keep the operation of ISM-MMC stable and balanced (cf. Section 2.7). Two ideal voltage sources are placed instead of dc-link split capacitors ($2C_{dc}$, cf. Figure 4.1) to eliminate related dc voltage imbalances in single-phase structure. The key parameters of the implemented simulation model are given in Table 4.1, and they correspond to the design example introduced in Section 2.7 (a single-phase only).

Table 4.1 – Main parameters of the simulation model for single-phase ISM-MMC [215]. © 2022 IEEE

Description	Symbol	Parameters
System parameters		
converter configuration (single-phase version)	–	**N2K3f1k**
number of SMs per arm	N	2
number of HB-legs in each SM	K	3
rated ac power and line-to-neutral voltage (rms)	P_{ac}, V	60 kW, 353.6 V
power factor	–	0.985
fundamental frequency	f	50 Hz
rated dc-link voltage	V_{dc}	1000 V
carrier frequency	f_{cr}	1 kHz
individual interleaved leg equivalent parameters	R, L	234.7 mΩ, 2.5 mH
individual SM capacitance	C, R_{ESR}	6.4 mF, 0.2 mΩ
IGBT module (Infineon Technologies AG)	–	FF150R12RT4 [193]
Control settings		
dc voltage control bandwidth	$\alpha_{p,dc}$ | $\alpha_{i,dc}$	15 rad/s | 5 rad/s
averaging time of the dc moving-average filter (H_{dc})	–	10 ms
loop-filter bandwidth (PLL)	$\alpha_{p,pll}$ | $\alpha_{i,pll}$	50 rad/s | 10 rad/s
output current control bandwidth	$\alpha_{c,oc}$ | $\alpha_{r,oc}$	2000 rad/s | 50 rad/s
circulating current control	R_{cir} | $\alpha_{2,cir}$	1.7 Ω | 250 rad/s
LPF circulating current control	$k_{f,cir}$ | $\alpha_{f,cir}$	$\sqrt{2}$ | 100 rad/s
sorting frequency	f_{sort}	333 Hz
interleaved current balancing	$k_{p,intlv}$	0.006 A^{-1}
observer current and voltage gains	l_i, l_v	10 H^{-1}, 20000 s^{-1}

The first simulation test was designed to demonstrate the performance of the proposed state observer-based interleaved legs current balancing control under ideal working conditions, namely when the system R, L, C parameters are well known and equal among themselves. Figure 4.4 depicts simulated interleaved currents, their comparison against the corresponding estimated values and distribution of observation errors when interleaved current control in the entire ISM-MMC is enabled (zones with white background) or disabled (gray zone). It is interesting to note that when the implemented state observer-based interleaved current

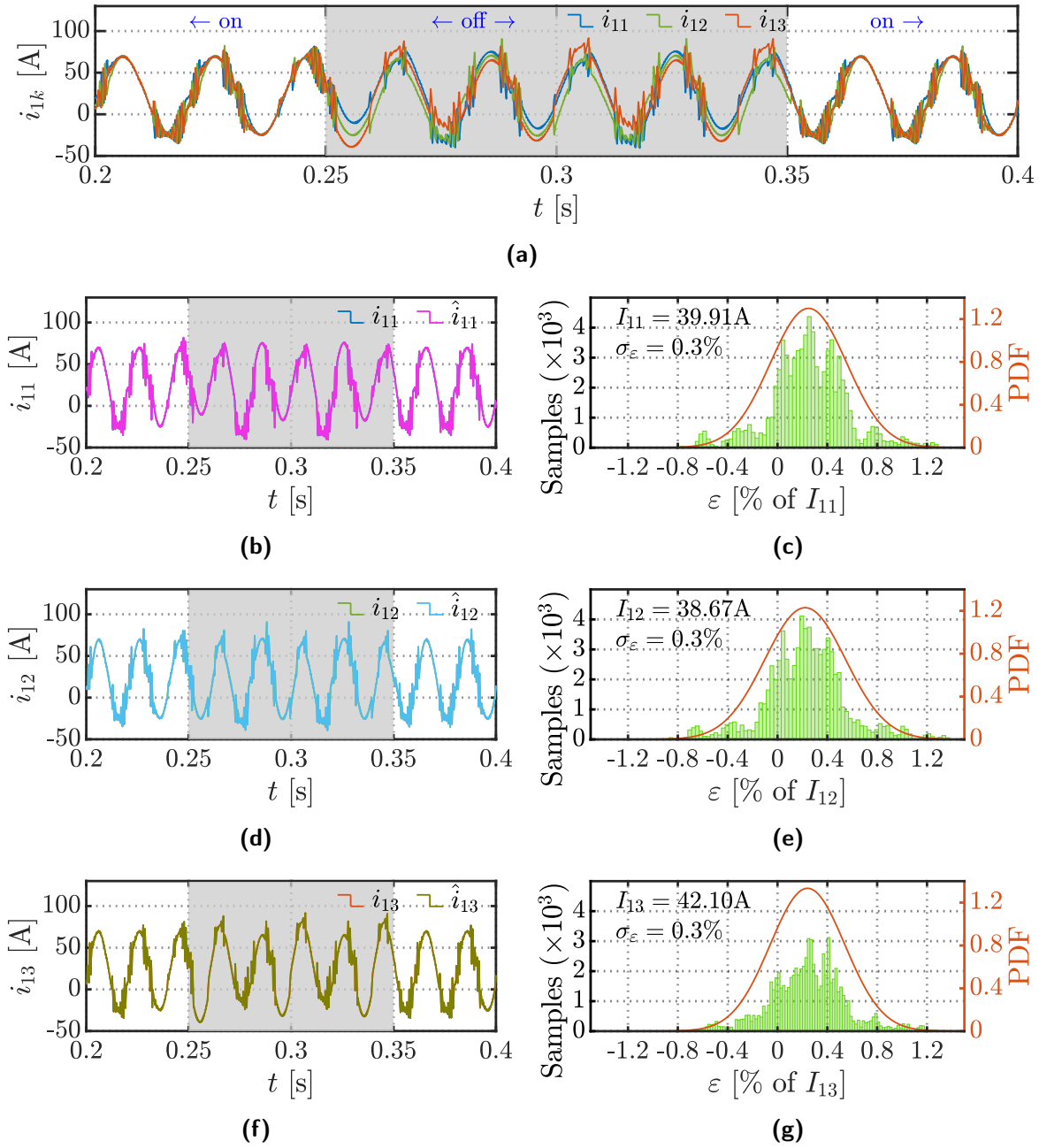

Figure 4.4 – Simulated interleaved currents in SM1 (a), timeseries of simulated and observed interleaved currents (b,d,f) with corresponding distribution of observation error (c,e,g) under **equal** R, L, C parameters and timeslots of enabled/disabled interleaved current balancing control [215]. © 2022 IEEE

balancing method is active, the fundamental components of currents within a SM are perfectly balanced. Once it is deactivated, these currents start getting instantly imbalanced. The reason is that the capacitor voltage balancing control forces switches commutate in a specific manner to satisfy its objective, balance capacitor voltages around their mean (cf. Section 3.2). The equivalent resistance of individual HB-legs acts as a damping factor limiting this unbalance. The lower the value of the equivalent resistance, the greater the current imbalance. Nevertheless, as it is visible from Figures 4.4b-4.4g, the estimated interleaved currents nicely repeat the simulated counterparts with minimal observation error staying within $\pm 1.2\%$ of each individual current rms value. The absolute error value is calculated at each sample within a given time range,

subtracting simulated from estimated values. The error normalization is done with individual current rms since these currents are composed of dc, fundamental and high (switching) frequency components. Probability density functions (PDF) are calculated by using either "normal" or "kernel" distributions.

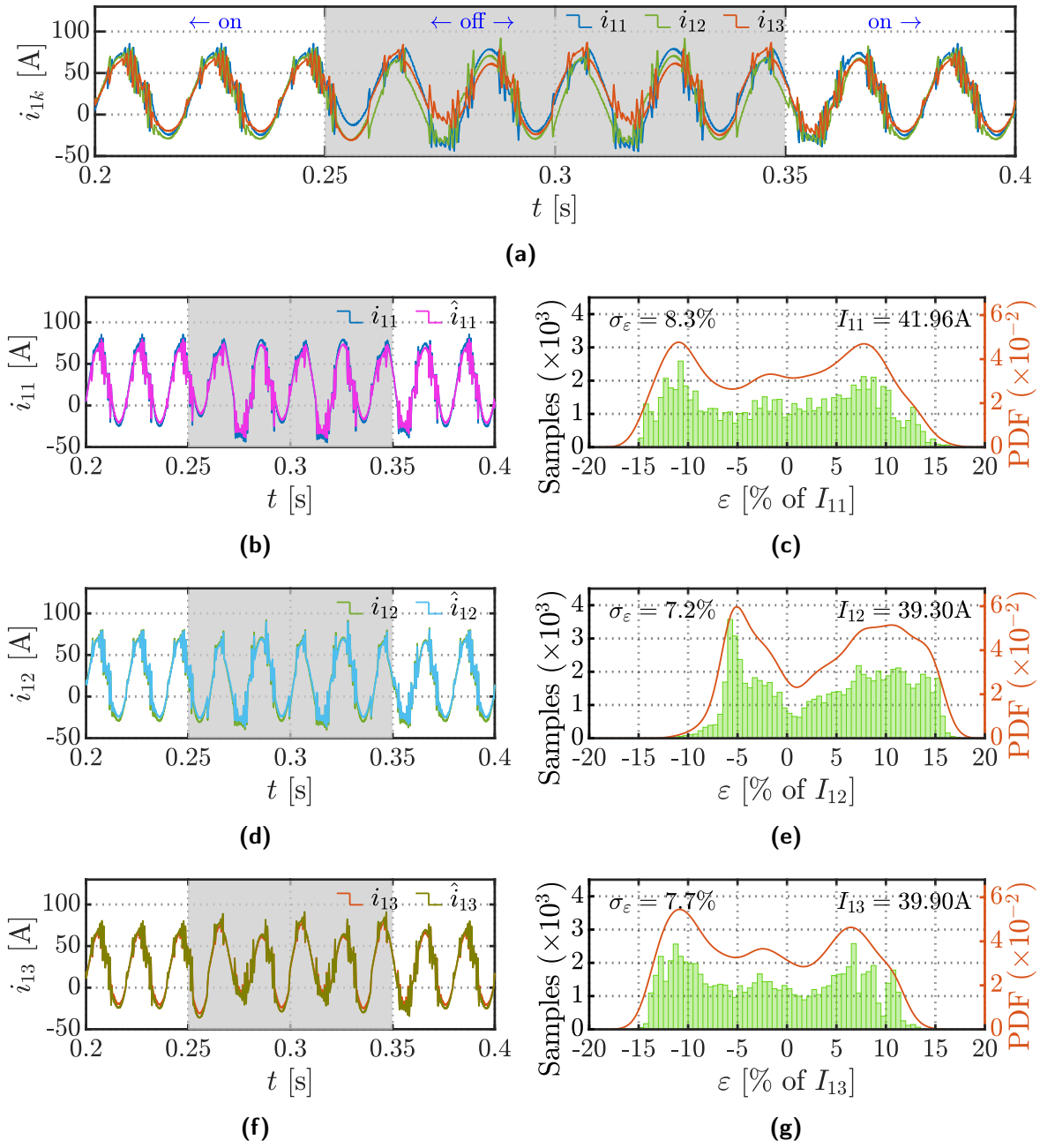

Figure 4.5 – Simulated interleaved currents in SM1 (a), timeseries of simulated and observed interleaved currents (b,d,f) with corresponding distribution of observation error (c,e,g) under **random** R, L, C parameters and timeslots of enabled/disabled interleaved current balancing control [215].

To verify that the current balancing can be implemented in a real system, where all internal components are subjected to manufacturing tolerances, the next numerical test is done with unequal circuitry parameters within each SM. The following simulation test shows similar zones (cf. Figure 4.4) with active and inactive interleaved currents balancing loops. However, this time the R, L, C parameters of each SM in ISM-MMC have randomly distributed values. The

parameter tolerances are limited by 30% of their nominal values (cf. Table 4.1). Accounting for these tolerances in the simulation is made by generating random numbers with a Gaussian distribution and confidence interval of $\pm 4\sigma$. For example, equivalent resistances per HB-leg of SM1 (upper arm) are [229.3, 252.7, 228.5] mΩ, inductances [2.3, 2.4, 2.8] mH and capacitance of the SM's capacitor is 6 mF (cf. Table 4.1). These parameters are different for each SM of the ISM-MMC. It can be noted from Figure 4.5a that due to these unequal parameters within a SM, the interleaved currents cannot be perfectly aligned as it was in the case of Figure 4.4a, even with activated interleaved current control. However, those currents are stabilized around their average value, demonstrating balanced, sinusoid-like waveforms. Again, once the control is disabled, the currents got imbalanced, however, with a larger magnitude due to the parameter's inequality. This time the estimation error is almost uniformly distributed in ±15% of each individual current rms. Nevertheless, state observer performs quite well, following the real, simulated currents in interleaved legs.

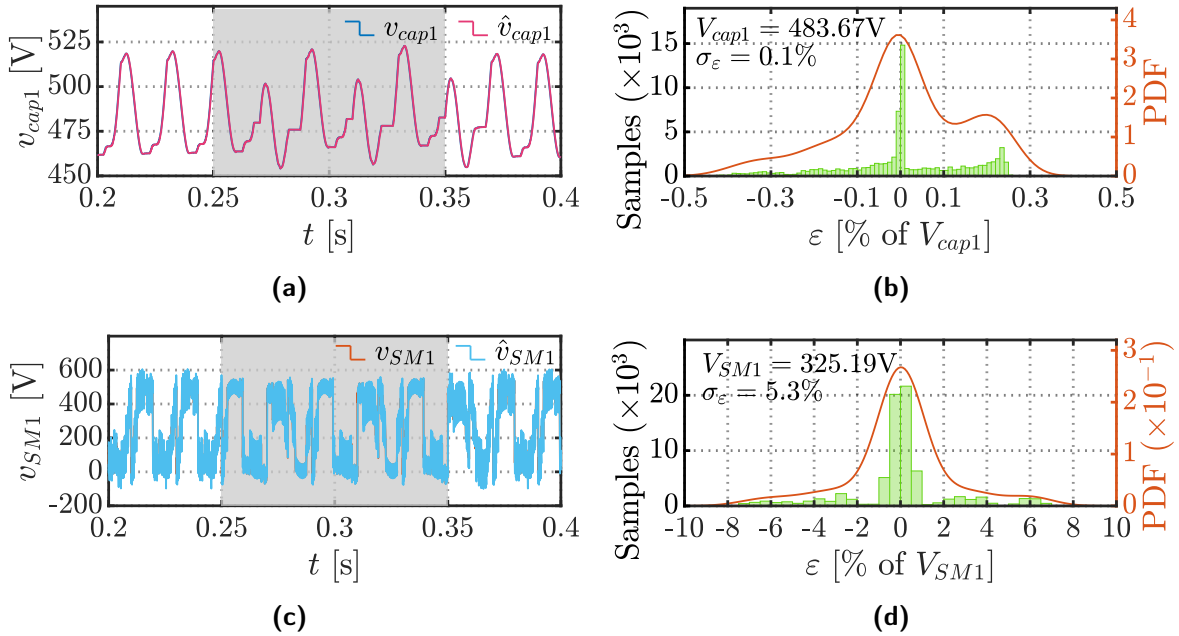

Figure 4.6 – Timeseries of simulated and observed capacitor voltage (a) and submodule voltage (c) of SM1 with corresponding distribution of observation error (b) and (d) under **random** R, L, C parameters and timeslots of enabled/disabled interleaved current balancing control [215].

To demonstrate estimation performance in terms of capacitor and submodule voltage, which are variables of the observer law, Figure 4.6 depicts time-series with simulated and observed capacitor and submodule voltage of SM1 with corresponding observation errors. The absolute values of these errors were normalized with the corresponding rms value of the voltage, similar to interleaved currents. The observation error for capacitor voltages is close to 0, showing that inequality of the parameters does not play a relevant role here. In the case of capacitor voltage estimation, this happens mainly because capacitor voltage is an output of the observer and it is a simulated value; hence, the observer can track this voltage precisely. Unlike the capacitor voltage, the submodule voltage is estimated based on arm current and simulated capacitor voltage, and it depends on the equivalent circuit of an SM (cf. Equation (4.13)). Despite that, as explained in Section 4.2, the voltage drops on the R, L elements of the circuit are small compared to SM capacitor voltage. Hence relatively small mismatch in the parameters does not produce a vast estimation error.

Overall, the implemented state observer-based interleaved legs current balancing control is able quite well to reach its objective, namely balancing the individual interleaved currents around their average even in the case with unequal circuit parameters. In this context, the current regulator compensates the current imbalance due to upstream control (the main contribution comes from the capacitor voltage balancing algorithm). Hence, there is always a current error present between individual interleaved leg current and the legs common average value even in the case with equal circuitry parameters. This error provokes the controller to generate a proportional voltage increment that adds to the HB-leg's average voltage. This action repeats until the estimated current does not reach the target. The current imbalance given by characteristic inequality of the composing elements (typically small due to the proper design of the converter) cannot be eliminated since the designed observer operates with rated values rather than real system parameters. An additional estimation loop can be implemented to assess the actual parameters of the SM circuit. However, this subject falls out of the scope of this thesis.

4.5 Experimental Tests

The experimental tests were performed to demonstrate dynamic and steady-state behavior of ISM-MMC, operating with the proposed state observer-based interleaved legs current balancing control. The tests were executed on a laboratory prototype, the circuital diagram of which can be found in Figure 4.7. Detailed description of the test bench along with view and summary of main parameters can be found in Appendix B. Here necessary comments to the setup configuration in relation to the conducted experiment is given only.

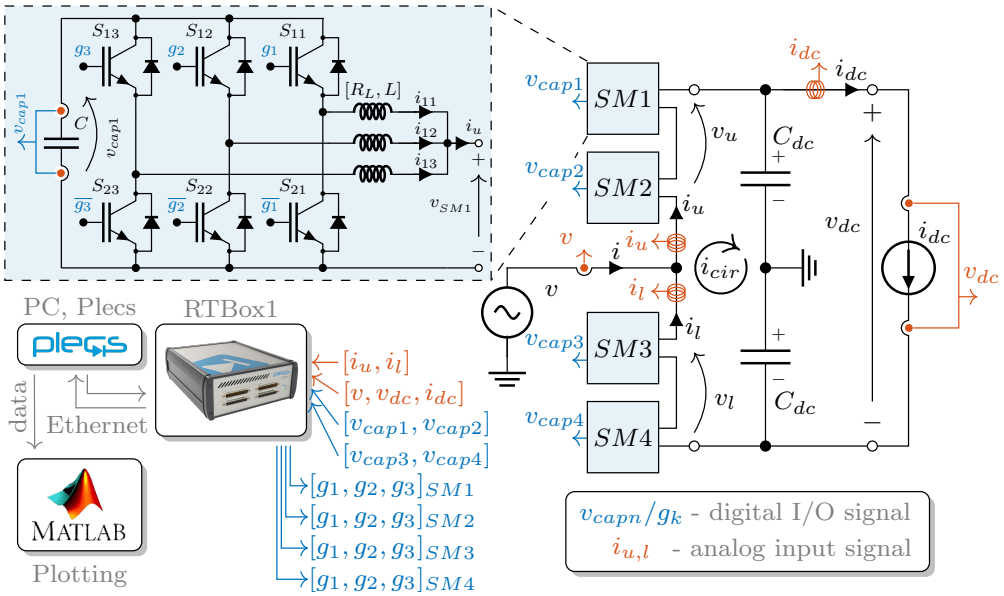

Figure 4.7 – Circuit diagram of the laboratory test ISM-MMC setup in relation to the implemented interleaved currents sensorless control [215]. © 2022 IEEE

The laboratory ISM-MMC has a single-phase structure with two SMs per arm ($N = 2$) and three HB-legs per SM ($K = 3$). A controller for rapid prototyping RT Box 1 (Plexim GmbH) governs the power stage of the laboratory prototype. Measured currents and voltages enter the controller either as analog (marked in red, Figure 4.7) or as digital (marked in blue, Figure 4.7) input signals. In addition to the depicted in Figure 4.7 analog measurements, the interleaved

currents from SM2 (i_{21}, i_{22}, i_{23}) and SM3 (i_{31}, i_{32}, i_{33}) were sampled via RT Box 1 (are not depicted in Figure 4.7) for comparison with estimated values that are used in the new control strategy. Table B.1 provides a summary of the main parameters of the laboratory setup.

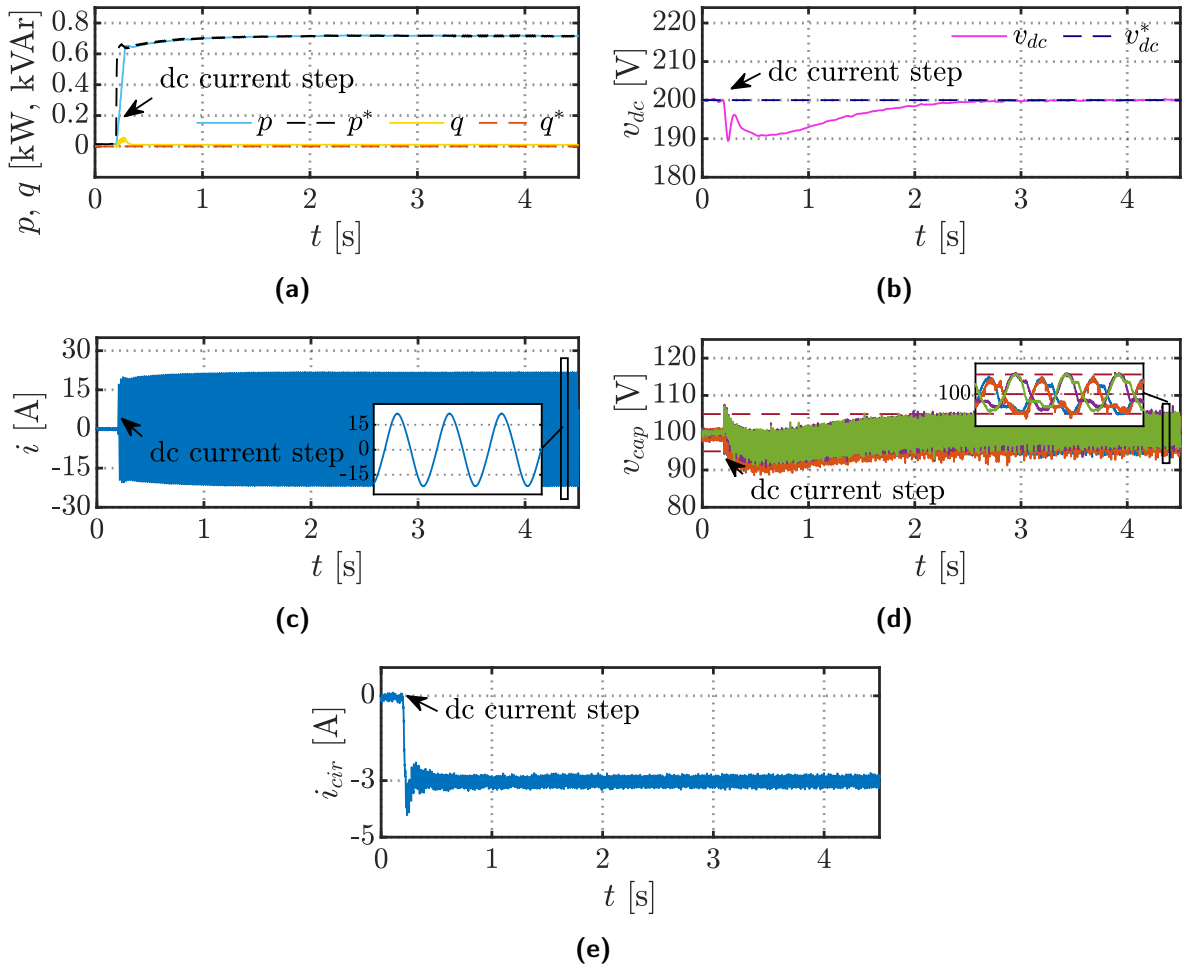

Figure 4.8 – Dc current step. Active and reactive powers (a) supplied by the grid (solid traces) along with their reference values (dashed lines); dc-link voltage (b) – measured value (solid trace) and its reference (dashed trace); ac phase current (c); measured capacitor voltages (d) from each submodule of ISM-MMC (solid traces) along with its ±5% tolerance band and mean value (dashed lines); (e) phase leg common-mode current [215]. © 2022 IEEE

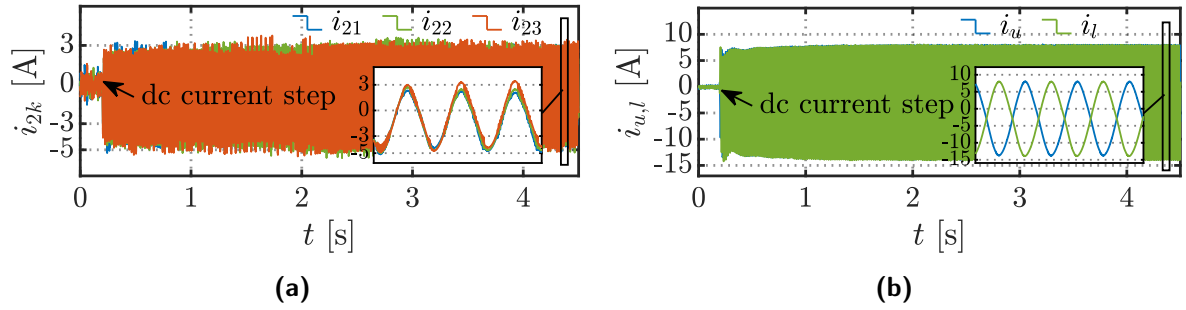

Figure 4.9 – Dc current step. Measured currents through interleaved legs of the submodule SM2 (a) and arm currents of ISM-MMC (b) [215]. © 2022 IEEE

The dc current step from 0 to 3 A has been introduced to the test ISM-MMC to demonstrate the dynamic performance of the implemented observer and associated with that interleaved

current regulator. Based on the state observer, the discussed interleaved current balancing loops were always active during the conducted experiment. Figures 4.8 and 4.9 depict the main input, output and internal characteristics of ISM-MMC, namely supplied ac power (active and reactive), ac phase current, dc-bus voltage, capacitor voltages, phase leg common-mode current, arm currents and individual currents of SM2 (cf. Figure 4.7). It should be stressed here that the quantities presented by Figures 4.8 and 4.9 are directly measured or derived by employing common calculus rules (Kirchhoff's current law, power calculation, etc.) from the measured quantities. It is well visible from these pictures that all waveforms are well balanced and reach their steady-state value after some transient time that finishes around 2.5 s of the plot scale. The key point here to be checked is the distribution of interleaved currents within the SM (cf. Figure 4.9a). In fact, they are nicely balanced, having a minor mismatch at the peaks of sinusoids, provoked by circuital parameter inequality. However, as will be demonstrated shortly, the rms values of these currents are pretty close.

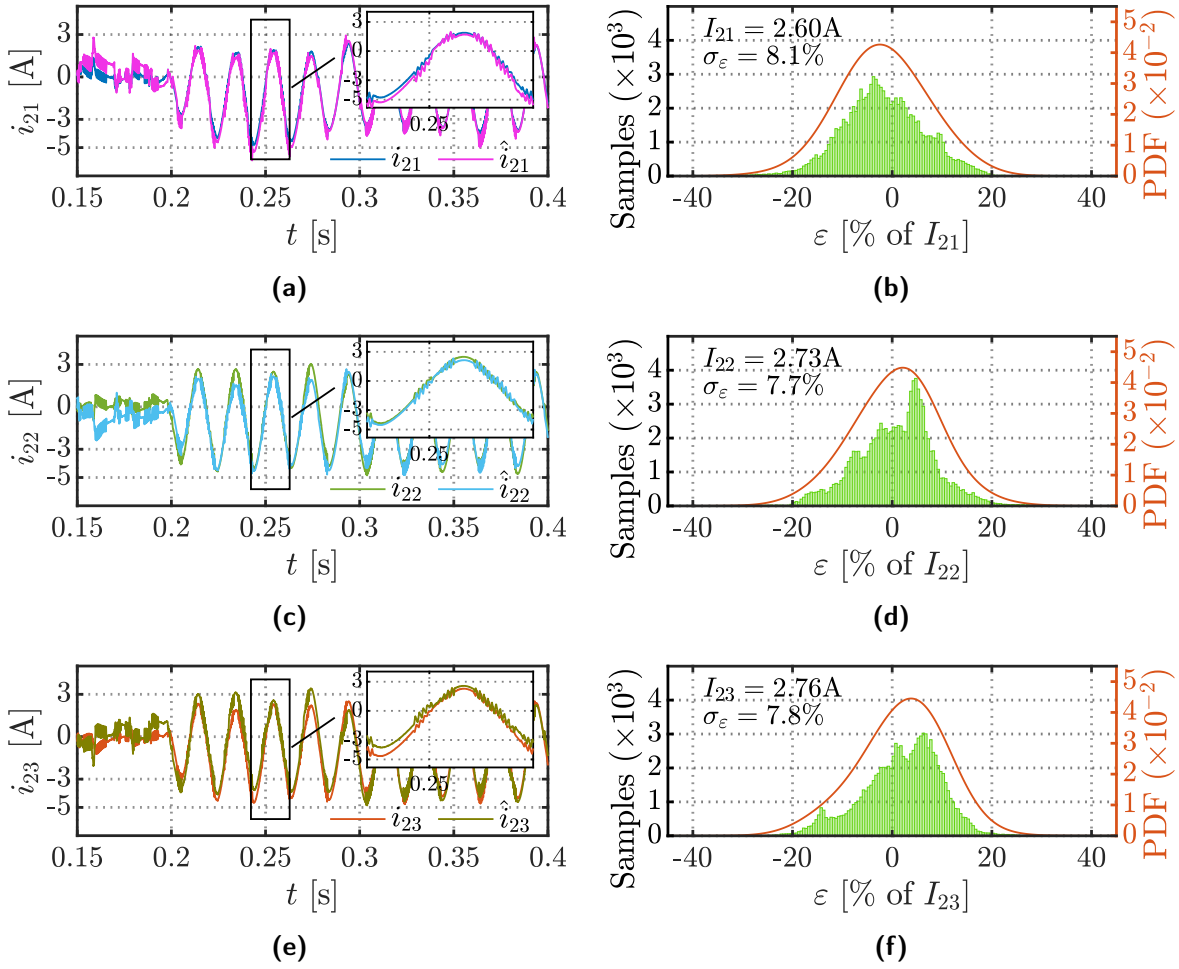

Figure 4.10 – Dc current step. Measured and estimated currents through interleaved legs of the submodule SM2 (a,c,e) with corresponding distribution of observation error (b,d,f) [215]. © 2022 IEEE

To visualize the dynamic behavior of the implemented state observer, measured interleaved currents from Figure 4.9a are plotted versus their estimates (cf. Figures 4.10a, 4.10c and 4.10e). The corresponding error distributions over the steady-state range (from 2.5 s to 4.5 s of the plot scale in Figure 4.9a) are depicted in Figures 4.10b, 4.10d and 4.10f. The normalization of the errors is done based on measured rms values of the corresponding interleaved currents (left-upper corner of the plots). It is noticeable from both time-series and error distribution plots that the

estimates of all three interleaved currents fit quite well to the real waveforms with absolute error bounded in the range ±20% of the measured currents rms, which is very close to the error range from performed simulations with random circuital parameters (cf. Figures 4.5c, 4.5e and 4.5g). In fact it can be noticed, that since the circuital parameter variance is constrained by manufacturing tolerances, so the error is also bounded at some range. In addition, it is also visible that the errors fit quite well to Gaussian distribution. Nevertheless, even though the estimated currents cannot repeat their measured counterpart, the fact that the interleaved currents are decently balanced in Figure 4.9a proves the feasibility of the proposed state observer-based interleaved current regulator.

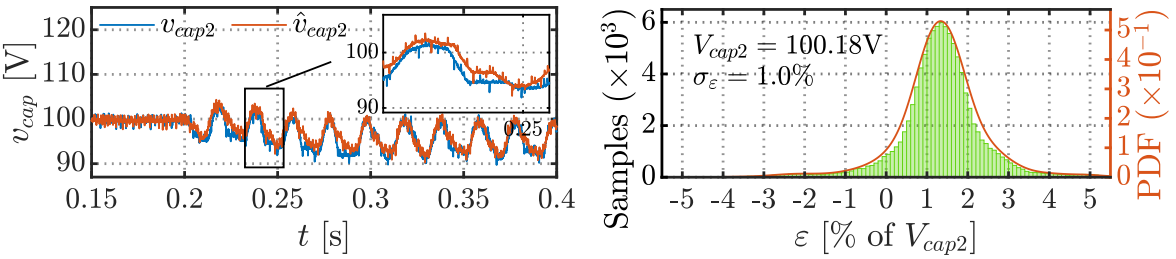

Figure 4.11 – Dc current step. Measured and estimated capacitor voltage of submodule SM2 (a) with corresponding distribution of observation error (b) [215]. © 2022 IEEE

Likewise, to the current estimate, it is also essential to depict a similar comparison in the case of capacitor voltages (cf. Figure 4.11) since the observer is built based on capacitor voltage error. This fact is particularly evident when the ac phase current is zero (open-circuit case). At this operating point, the variation of capacitor voltage is minimal and interleaved currents almost purely consist of high (switching) frequency components. In such conditions, precisely estimating interleaved currents is very difficult.

Overall, the dynamic and steady-state behavior of the newly proposed sensorless interleaved currents balancing strategy is stable and predictable.

4.6 Summary

A current sharing problem in interleaved SMs of ISM-MMC that mostly arises from the upstream control actions is solved in this chapter with help of a new interleaved currents sensorless method. A new state observer-based feedback control that operates individually with each SM has been introduced into classical ISM-MMC control layout. The implementation is discussed in great detail in this chapter, providing necessary mathematical background. Observability and stability of the observer has been verified here as well. The implemented state observer employs only a few mathematical operations, hence it does not require high computation power. Instead, the new interleaved currents balancing method requires only a few measurements from the sensors, which are already employed in other control actions. This fact reflects positively on the cost, volume and complexity of the ISM-MMC converter. In addition to that it preserves effortless scalability philosophy in design of ISM-MMC since it does not require to place or remove sensors while number of HB-legs in a SM varies. One particular drawback that associates with this balancing method was highlighted in this chapter, namely it has been demonstrated that the observer, having no precise information about circuital parameters in a SM, provides

non-accurate current estimations. However, as it was verified by numerical simulations and experimental results, this estimator-related drawback does not vastly degrade performance of the based on it interleaved current balancing loop. Instead, the control is able adequately response on the internal and external step-like system perturbations.

Chapter 5

Conclusions and Future Research

5.1 Summary and Contributions

The modular multilevel converter (MMC) has come a long way since its introduction almost two decade ago. Ongoing improvements and advances in MMC technology have extended the range of medium and high-voltage applications where the MMC de-facto has become a standard. It features competitive advantages in comparison with conventional or other multilevel counterparts, such as quality of output characteristics (voltage, current), high modularity and simple voltage-level scalability by stacking the so-called submodules in a series. On the other hand, the existing submodule structures do not permit flexible current-level scalability. To tackle this problem a new interleaved submodule structure has been proposed for modular multilevel converters, forming a novel topology named Modular Multilevel Converter with Interleaved half-bridge Sub-Modules (ISM-MMC). Among strong points of the new converter structure are easily scalable voltage and current ratings, suitable for all voltage levels high power applications, enhanced output waveforms, improved efficiency and fault tolerance capability in comparison with classical MMC architectures. The latter concept can be justified by highly modular SM's structure in ISM-MMC exploiting benefits of parallel systems (term in readability studies), where failure of a single component (HB-leg) does not mean failure of whole system (SM). In addition to that superb scalability in both voltage and current levels promotes the usage of low-voltage, low-current power modules. In such scenario, other semiconductor technologies can be exploit (e.g., MOSFET). Looking from another angle, extra degree of freedom in power partitioning brings possibilities to independently design each converter stage, enabling the synthesis of highly optimized components, bring down converter losses and optimize design of the cooling system, making it more distributed and efficient. Moreover, fault blocking capabilities of ISM-MMC can be substantially increased since each interleaved unit handles only a portion of the fault current.

Another feature that originates from interleaving concept is the further quality enhancement of ac voltage waveforms, which diminish filtering requirements on the grid side. This cumulative effect emerges from two properties that interleaving submodule produces in ISM-MMC. The first property is the number of synthesized phase voltage levels, which in case of ISM-MMC is not only proportional to a number of series connected submodules within an arm but also to a number of parallel connected HB-units in a SM. The second feature is the equivalent converter

switching frequency that in case of the proposed hybrid carrier-based modulation scheme is a multiple of the carrier frequency and number of interleaved HB-units in a SM.

On the contrary ISM-MMC has some obvious structural drawbacks, such as increased complexity of the converter architecture with many commutating devices to be controlled and larger number of required inductors. Nevertheless, it should be pointed out that a distributed arrangement of these inductors is not necessarily a weak point since the current ratings of the inductors is proportionally less than a classical arm inductor. Therefore, with an optimal design equal or superior qualitive characteristics (cost, weight, volume, etc.) can be reached.

All aforementioned ISM-MMC characteristics along with derived average converter model, control and modulation schemes are exhaustively discussed in Chapter 2 of this thesis. Here, the applicability of classical MMC control techniques for ISM-MMC has been proven. Furthermore, this part of the thesis is devoted to performance and efficiency comparison between several ISM-MMC and standard MMC configuration, with the fixed number of semiconductors and power ratings. It has been demonstrated that in most of the examined characteristics, ISM-MMC can offer superior or equal performance in comparison with classical MMCs. A relative efficiency gain up to 1.56% (with total power losses reduction up to 53.24%) depending on the compared configurations and operating power level can be achieved. This chapter also presents numerical simulations and hardware-in-the-loop tests that were carried out to validate key features of ISM-MMC and the implemented control/modulation techniques, eventually proving feasibility of the proposed MMC-based structure with reference to a low-voltage, ultra-fast EV charging infrastructure.

Another important contribution of this thesis regards the development of a control strategy that resolves the hidden within a SM interleaved currents balancing problem. This problem is quite common in interleaved converters, while it is new in MMC structures and has not been deeply elaborated in literature. It has been proven that a reasonable level of interleaved currents imbalance does not cause instability problems in ISM-MMC. Moreover, this effect is practically invisible from outside of a SM. However, high magnitude imbalanced currents cause excessive converter losses, saturation of the inductors and thermal stress on the SM components, which eventually may lead to their failure. Therefore, a uniform distribution of the total arms current among the interleaved HB-legs has to be ensured. Comprehensive analysis of this problem shows that substantial part of the currents imbalance is provoked by the capacitor voltage balancing algorithm, which is frequently implemented with sorting functions. To compensate its actions the new interleaved current balancing method should be the ultimate task in the ISM-MMC control arrangement. However, implementation of such control layout with common MMC sorting algorithms for capacitor voltage balancing is troublesome since their operation is based on reassignment of firing signals. To manage this issue a new capacitor voltage balancing algorithm is presented in this thesis. It operates with voltage references rather than with firing signals, hence the outputs of this capacitor voltage balancing block are still voltage references, providing greater flexibility in terms of control tasks arrangement. After that the new current balancing method, which is based on simple feedback loop, can be introduced. The reference voltage adjustment for each interleaved HB-leg takes place individually, ensuring high dynamic response and control flexibility. Chapter 3 deals with all above mentioned aspects. Furthermore, it has been shown that standard manufacturing tolerances of the interleaved inductors do not cause instability problems in ISM-MMC. At the same time, the proposed balancing method can successfully cope with such non-idealities. The proposed control loops are compatible with digital processors and show decent performance with a relatively large sampling period. This aspect has been fully verified during extensive experimental tests on a laboratory prototype. The

dynamic and steady-state behavior demonstrate expected performance under several system and control perturbations.

The initially proposed interleaved current balancing control relies on individual interleaved currents sensing. This approach has an evident disadvantage, namely a very large number of required current sensors, which is almost proportional to the number of interleaved legs in the whole converter. To cope with this challenge a new state observer is proposed. Observers typically add complexity to the control system and demand high computational resources, especially in the highly modular structures as ISM-MMC. However, the implemented state observer employs only a few mathematical operations and can fit in an entry-level controller. In addition to that, it requires only a few measured quantities, namely capacitor voltages and arm currents that are typically sensed in classical MMCs for operation of internal control loops. Therefore, the proposed interleaved current balancing method does not need excessive interleaved currents measurements that directly reflects on the cost and complexity of the ISM-MMC converters. It can adequately share the arm current among interleaved legs of a SM, compensating the primary cause of the high current imbalance, namely actions of capacitor voltage balancing technique. Both numerical simulations and experimental tests verified the steady-state and dynamic performance of the introduced current balancing method. It has been shown thought that the implemented observer provides current estimations with lower accuracy when the circuit parameters vary from their observer preset values. This accuracy is bounded by the variance of real parameters from the preset ones in the estimator. However, in a good converter design, this variance is limited; hence the observer-related estimation error is also limited. In this case, the potential current imbalance due to parameter variance can be effectively bounded. All these matters are covered in Chapter 4.

5.2 Proposal for Future Research

Even though this thesis tries to cover the key aspects of the new converter design, there are several challenges, questions and new stimulating ideas arise. Indeed, based on the concepts developed in this work, a few future research guidelines can be proposed. The experimental validation, performed in the frame of this thesis to prove feasibility of proposed topology, control and modulation methods, is based on a reduced scale laboratory prototype (a single-phase converter). Therefore, the real-scale, application-specific implementation issues cannot be fully investigated. In this regard some auxiliary systems of the new modular high-power converter can be optimized, e.g. cooling, communication, etc.

Another attractive research topic for the future converter development refers to an optimal design of ISM-MMC, considering cost and characteristics of the composing components (i.e., less SMs/interleaved HB-legs with higher ratings or more SMs/interleaved HB-legs with reduced ratings). Proper selection of these design parameters is a multi-variable optimization problem that must consider, for instance, cost, power ratings of the components, power quality requirements, etc. In addition, a proper design of interleaved inductors must be studied, considering maximum allowed peak-to-peak current ripple in interleaved assemblies and output characteristics of the converter. Similar task can be addressed to a SM capacitor voltage ripple study.

The implemented ISM-MMC control structure, which is presented in current thesis, is based on a classical MMC control approach. Hence, other modern, application-related control methods (e.g., predictive, repetitive, artificial intelligence based control, etc.) can be applied, providing

a comparative analysis of the converter dynamic and steady-state behaviour. Control task distribution in hardware implementation can be optimized, detaching several control rings (e.g., converter level, arm level and submodule level). The proposed observer-based interleaved current control can be upgraded with a help of advanced observers that allows to take into account variance of the real circuital parameters from their nominal value. Similarly to the control, other frequently used and advanced modulation schemes can be analyzed and compared. In this context, different common-mode injections for carrier-based modulations may be topic of interest for future developments.

The new conversion system has been tested under balanced power supply conditions (balanced voltages and currents) and regular operation of the converter. From this prospective, stable and robust functioning of ISM-MMC must be investigated, for example, during a system fault, active/reactive power oscillations, abnormal ISM-MMC operations, etc. The latter subject is especially interesting since it is directly linked with system survival and optimized functioning. As an example, operation with disconnected on purpose or due to a fault, single or multiple HB-units within a SM could be examined.

From an application point of view different ISM-MMC arrangements can be analyzed as well, for example, similar to standard MMC realizations, namely single-star, single-delta, double-star, etc. Likewise, full-bridge interleaved submodule arrangements can be tested, dividing interleaved HB-units into the groups.

In this work a simple HB-unit has been considered in the interleaved structure of a SM, while other basic units commonly manufactured can be considered, e.g., multilevel legs (NPC, FC, etc.).

Another interesting research path would be to compare structural and performance differences between ISM-MMC and other non MMC-based high-power converters (e.g., active-neutral-point-clamped converter). However, to make this comparison fair one should bear in mind that the key characteristics of the compared converters (e.g., power and voltage ratings, number of semiconductors, application type, etc.) must be preserved the same.

Finally and given the large number of hardware elements, studies on the failure rates and reliability of such complex power conversion system as a ISM-MMC, in association with fault management techniques and implementations of redundancy schemes shall be reported.

Appendix A

Efficiency calculations

A power converter's efficiency can be determined by relation of the output power (in rectification mode, $P_{out} = P_{dc}$) to its input power, where the last part can be represented by sum of output power and total losses ($P_{in} = P_{dc} + P_{loss}$). The latter term consists of several sources of power losses and strongly depends on the converter structure. In most of MMC-based structures (including the proposed ISM-MMC), the total power losses sum up from power dissipation in inductors (P_{ind}), losses in floating SM capacitors (P_{cap}) and losses in switching devices. The last mentioned loss portion has a major impact on the total converter efficiency and it can be represented by conduction losses (P_{con}), switching losses (P_{sw}), constant power dissipation in IGBT drive circuit (P_{driv}) and switching frequency-dependent gate-drive losses (P_{gate}).

$$\eta = \frac{P_{dc}}{P_{dc} + P_{loss}} = \frac{P_{dc}}{P_{dc} + P_{ind} + P_{cap} + P_{con} + P_{sw} + P_{driv} + P_{gate}} \tag{A.1}$$

The following subsections provide necessary formulations for each source of power losses. The following assumptions have been considered:

- constant SM capacitor voltage;
- leg's common-mode current is purely composed by a dc component, which can be computed as the dc current equally shared among converters' phases;
- converter operates with unity power factor;
- current ripple associated with switching process is neglected;
- currents inside each submodule are balanced and equally distributed among the HB-legs;
- losses in the connecting wires are neglected;
- two submodule configurations ($N = 2$) are taken as a reference (e.g., "**N2K3f1k**", "**N2K3f333**", "**N2Kp3f1k**)", while the calculus can be extended to any arbitrary number of SMs.

Inductor losses

Power dissipation in inductors can be determined by the following formula:

$$P_{ind} = 2MI_{u,l}^2 R_{arm} \tag{A.2}$$

where expression "2M" represents total arm number in M-phase converter, $I_{u,l}$ is rms value of the corresponding arm current. Term R_{arm} stands for the equivalent internal resistance of an arm inductor. In ISM-MMC topology it can be derived by equivalent transformations of the converter circuit. Assuming that the total power losses are in the range of few percent of the output power, per-phase rms value of arm current can be defined by

$$I_{u,l|x} = \frac{I_{dc}}{M}\sqrt{1+\frac{2}{m_x^2}} = \frac{P_{dc}}{MV_{dc}}\sqrt{1+\frac{2}{m_x^2}} \tag{A.3}$$

where V_{dc} is the rated dc-bus voltage and per-phase modulating index m_x is defined by Equation (2.49). Finally, by substituting Equation (A.3) into Equation (A.2), losses associated with inductors in MMC or ISM-MMC circuit are expressed as

$$P_{ind} = \frac{2P_{dc}^2}{MV_{dc}^2}\left[1+\frac{2}{m_x^2}\right]R_{arm} \tag{A.4}$$

It should be noted that Equation (A.4) accounts copper losses only. The inductor core losses due to eddy currents and hysteresis effect are not considered here.

Capacitor losses

Power losses due to equivalent series resistance (ESR) of the SM floating capacitors can be calculated taking into account the time periods when the capacitor is inserted or bypassed. Neglecting the effect of capacitor voltage balancing (constant SM capacitor voltage), the time periods when each capacitor in the arm string is inserted can be evenly distributed among all of them. In this example only two SMs are considered, however it can be easily extended to any arbitrary number of SMs.

$$P_{cap} = \frac{4M}{T}R_{ESR}\left[\int_0^{T/4} i_{u,l}^2 d_{on}\,dt + \int_{T/4}^{T/2} i_{u,l}^2(1-d_{on})\,dt\right] \tag{A.5}$$

where expression "4M" accounts number of arms (two arms) in each M-phases of the converter and half-wave symmetry of the instantaneous upper or lower arm current $i_{u,l}$ (integrals are calculated only over a half-period). Term d_{on} represents the on-state duty cycle of the high switch(es) in each SM and T is the fundamental time period. It must be noted though that interleaving effect in average does not change the amount of current passing through the capacitor, hence the computation can be based on the total arm current, which has the following form:

$$i_{ux} = \frac{I_{dc}}{M}\left[1+\frac{2cos\omega t}{m_x}\right], \quad i_{lx} = \frac{I_{dc}}{M}\left[1-\frac{2cos\omega t}{m_x}\right] \tag{A.6}$$

where I_{dc} is the rated dc-bus current (proportional to the converter's output power) and ω is the fundamental angular frequency. The on-state duty cycle is determined by

$$d_{on} = 1 - m_x cos\omega t \tag{A.7}$$

By combining Equations (A.5)-(A.7) and taking into consideration upper arm current, the power dissipated in the SM floating capacitors is

$$P_{cap} = \frac{4P_{dc}^2}{MTV_{dc}^2} R_{ESR} \left[\int_0^{T/4} \left(1 + \frac{2cos\omega t}{m_x}\right)^2 (1 - m_x cos\omega t)\, dt + \right. \\ \left. + \int_{T/4}^{T/2} \left(1 + \frac{2cos\omega t}{m_x}\right)^2 m_x cos\omega t\, dt \right] \tag{A.8}$$

Semiconductor conduction losses

The conduction loss in semiconductors (e.g., IGBT with anti-parallel diode) is calculated using the semiconductor V-I on-state characteristic and the instantaneous current flowing through the each part of the semiconductor. Since the on-state characteristic of IGBTs and diodes are usually non-linear functions of the device current, piece-wise linear approximation is used to simplify the conduction loss calculation. Conduction losses are calculated within one fundamental frequency period T using the portions of arm currents that pass through either the IGBT or diode in particular time slot of the fundamental period and the piece-wise linear characteristic curves from datasheet of the device.

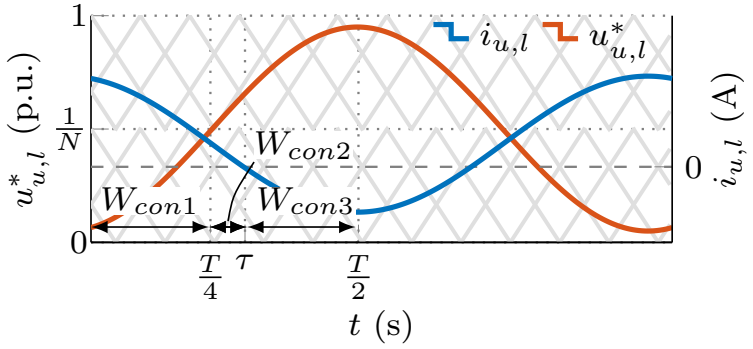

Figure A.1 – Normalized arm voltage reference and corresponding arm current

Figure A.1 depicts a general case of normalized arm voltage reference ($u^*_{u,l}$) versus the corresponding arm current ($i_{u,l}$). Thanks to the arm voltages and currents half-wave symmetry, computation of the conduction losses P_{con} can be restricted to one-half of the fundamental period ($T/2$). In that case three time slots must be considered. The first one is [0,$T/4$] that corresponds to energy loss W_{con1} and the time frame when only one SM is inserted (cf. $u^*_{u,l}$ is within [0, $1/N$] level) while the other is bypassed (neglecting the capacitor voltage balancing). The second time diapason (with energy loss W_{con2}) is when two SMs are inserted (cf. $u^*_{u,l}$ is within [$1/N$, 1] level), while the arm current is still positive. The last time frame (with energy loss W_{con3}) is similar to

the previous case with negative arm current. Based on this discussion, the conduction losses P_{con} can be expressed as:

$$P_{con} = \frac{2}{T}\Bigg[\underbrace{2MK\int_{0}^{T/4}|\bar{i}_{k|u,l}|\left[\left(V_{ce}(|\bar{i}_{k|u,l}|)(1+d_{off1})+V_f(|\bar{i}_{k|u,l}|)d_{on1}\right)\right]dt}_{W_{con1}}+ \\ \underbrace{+2MK\int_{T/4}^{\tau}|\bar{i}_{k|u,l}|\left[\left(V_f(|\bar{i}_{k|u,l}|)(1+d_{on2})+V_{ce}(|\bar{i}_{k|u,l}|)d_{off2}\right)\right]dt}_{W_{con2}}+ \\ \underbrace{+2MK\int_{\tau}^{T/2}|\bar{i}_{k|u,l}|\left[\left(V_{ce}(|\bar{i}_{k|u,l}|)(1+d_{off3})+V_f(|\bar{i}_{k|u,l}|)d_{on3}\right)\right]dt}_{W_{con3}}\Bigg] \tag{A.9}$$

where expression "$2MK$" accounts number of HB-legs (K) inside a SM, number of arms (two arms) in each M-phases of the converter. Terms V_{ce} and V_f are the conduction voltage functions of positive average current that passes through a SM's HB-leg in upper or lower arm ($|\bar{i}_{k|u,l}|$) and it is evaluated at a junction temperature of 125°C for IGBT and diode, respectively. Figure A.2 depicts V-I output characteristic of the IGBT and anti-parallel diode that are embedded in IGBT modules that are used for reference design configurations (cf. Table 2.1).

The duty cycles are formulated as follows

$$\begin{aligned} &d_{on1} = 1 - m_x cos\omega t, \quad d_{off1} = 1 - d_{on1} = m_x cos\omega t \\ &d_{on2} = -m_x cos\omega t, \quad d_{off2} = 1 - d_{on2} = 1 + m_x cos\omega t \\ &d_{on3} = d_{off2}, \quad d_{off3} = d_{on2} \end{aligned} \tag{A.10}$$

where d_{on} represent amount of time when the diode is conducting (numerical part of the subscript (1, 2 and 3) denotes the time interval according to Figure A.1), while d_{off} is the amount of time when the IGBT is conducting. Time instant τ can be determined by

$$\tau = \frac{1}{\omega} arccos\left(-\frac{m_x}{2}\right) \tag{A.11}$$

Semiconductor switching losses

Calculation of switching losses requires the counts of the switching transitions and the values of switching energy loss per switching event. It can be done numerically with help of simulation software or can be calculated analytically with decent accuracy. This work employs the analytical method. The IGBT's turn-on, turn-off loss energies (W_{on}, W_{off}), and the diode reverse recovery energy (W_{rec}) can be found in the corresponding semiconductor datasheet of the IGBT modules "FF150R12RT4" [193] and "FF450R07ME4" [194]. The non-linear, current dependent

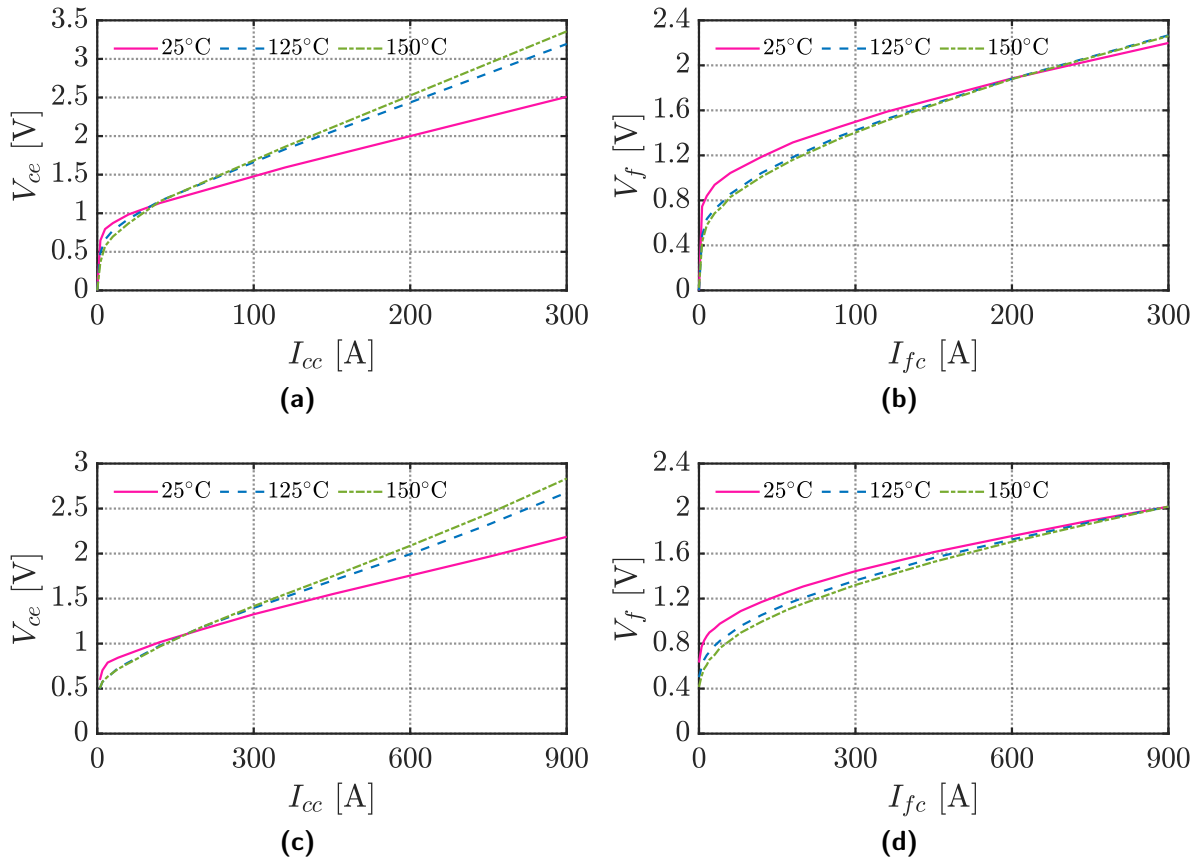

Figure A.2 – V-I output characteristic of IGBT (a,c) and anti-parallel diode (b,d) for the IGBT modules: (a,b) FF150R12RT4 [193] and (c,d) FF450R07ME4 [194]

characteristics of the energies are approximated using piece-wise linear functions. The switching losses are computed within one fundamental period by

$$P_{sw} = \frac{MKV_{dc}f_{cr}}{NTV_{ce}} \int_0^T [W_{on}(|\bar{i}_{k,u}|) + W_{on}(|\bar{i}_{k,l}|) + W_{off}(|\bar{i}_{k,u}|) + W_{off}(|\bar{i}_{k,l}|) + W_{rec}(|\bar{i}_{k,u}|) + W_{rec}(|\bar{i}_{k,l}|)]\, dt \tag{A.12}$$

where V_{dc} is the rated dc-bus voltage, N is the number of SM within one arm string, f_{cr} is the carrier frequency and V_{ce} is the collector-emitter blocking voltage of an IGBT. Terms W_{on}, W_{off}, and W_{rec} represent IGBT's turn-on, turn-off energy losses, and the diode reverse recovery energy losses computed as functions of average current through one HB-leg of a SM. The switching energies are scaled by the ratio of the mean capacitor voltage to the reference blocking voltage from datasheet. The employed switching energy characteristics for the corresponding IGBT modules can be found in Figures A.3 and A.4. It must be noted though that the diode turn-on losses are neglected.

Driving circuit losses

Operation of a converter results in some unavoidable losses associated with driving circuit, which can be divided into two categories. The first part P_{driv} is self power consumption of the driving and control circuits, which can be assumed constant. In current work, for the comparative

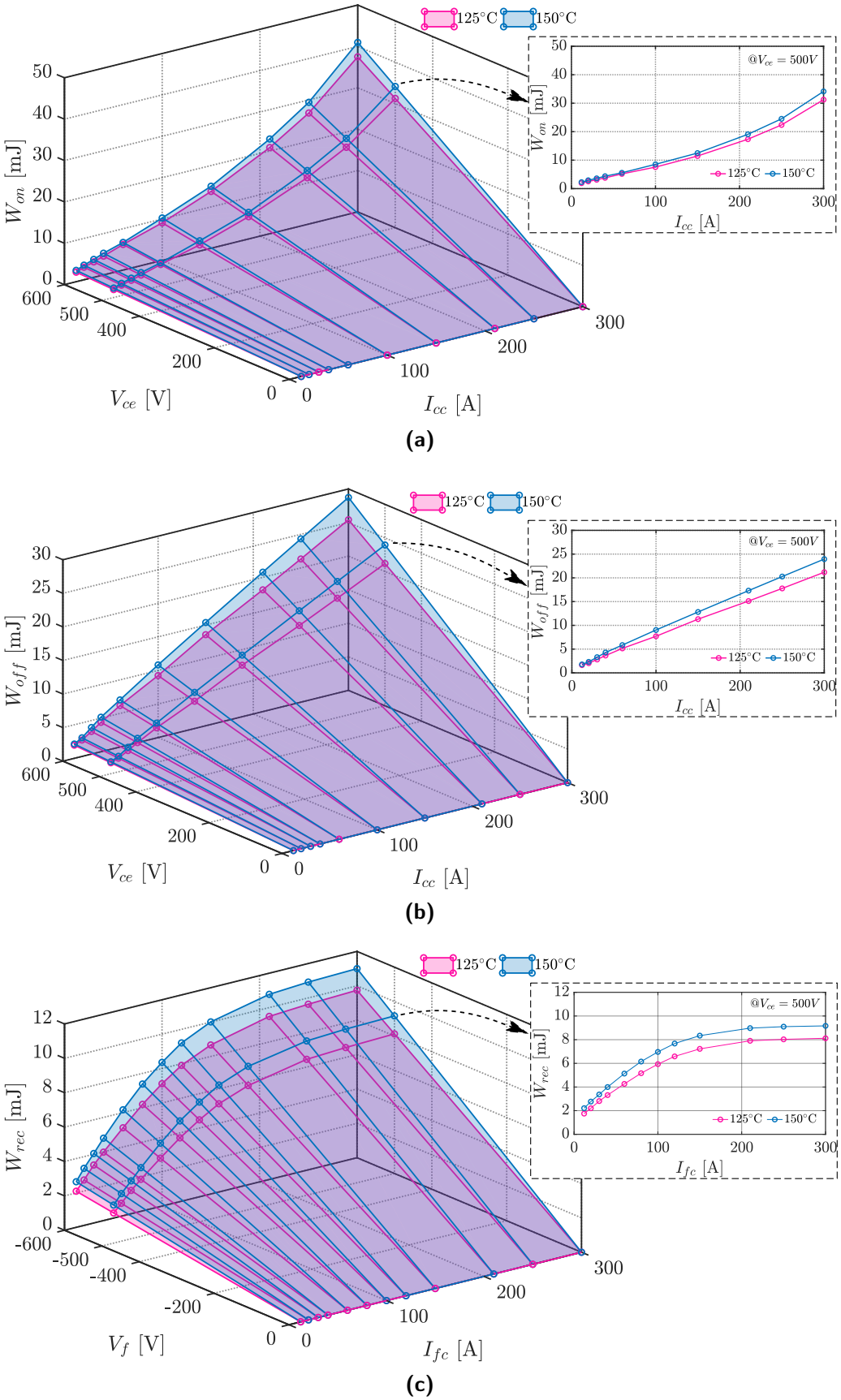

Figure A.3 – Switching losses characteristics of the FF150R12RT4 [193] IGBT module: (a) turn-on (b) turn-off (c) recovery

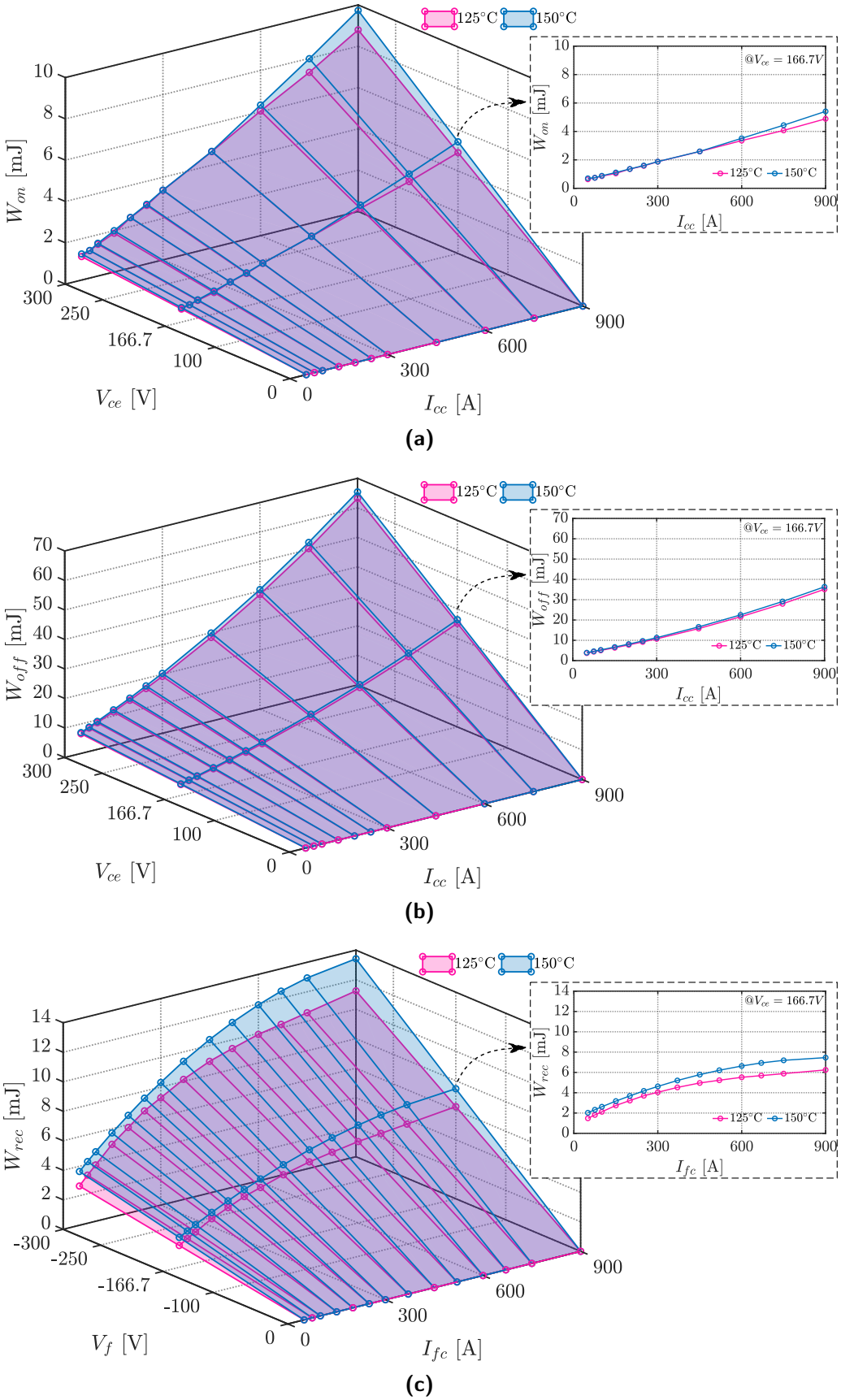

Figure A.4 – Switching losses characteristics of the FF450R07ME4 [194] IGBT module: (a) turn-on (b) turn-off (c) recovery

analysis held in Section 2.8, P_{driv} is arbitrarily set to 50 W for each converter configuration. The second category is the losses in gate-driving circuit that is caused by switching actions in the semiconductor. Turning on or off the IGBT involves charging or discharging the equivalent capacitor in gate circuitry. When the voltage across a capacitor is changing, a certain amount of charge has to be transferred. It can be characterized by the typical gate charge vs. gate-to-source voltage curves available in most semiconductor datasheets [217]. Once the total gate charge is obtained, the gate charge losses (P_{gate}) of an entire converter can be calculated by

$$P_{gate} = 4MNK \cdot V_{ge} Q_g f_{cr} \tag{A.13}$$

where expression "$4MNK$" represent the total number of switching devices in an M-phase, double star ISM-MMC with N submodules per arm and $2K$ switches per SM. Term V_{ge} is the amplitude of the gate-emitter voltage, Q_g gate charge, and f_{cr} is the carrier frequency.

Appendix **B**

Laboratory Prototype

This section briefly describes the main elements of the downscaled laboratory ISM-MMC prototype built and used for the experimental validation of several concepts presented in this thesis. The prototype design has been focused on the versatility of the implementation, having adjustable structure to satisfy the needs of specific experiment. In addition, to that this prototype has been constructed primarily to justify the concept of ISM-MMC and its control principles, while optimization of the converter structure is beyond of the scope of current work. This section also describes the key techniques that have been used in the conducted experiments and reveals basic characteristics of the employed instruments.

Figure B.1 – View of the laboratory test setup [204]. © 2022 IEEE

Figure B.1 shows an overview of the single-phase converter rig and auxiliary equipment. Depending on the specifics of performed experiments, the support tools vary (e.g. type of dc load), therefore, this picture presents one specific case only. In general, the experimental setup consists of a metal rack, comprising all necessary elements of the ISM-MMC, programmable ac source (grid emulator), and dc load (either variable resistor or electronic dc load). The system has

been naturally designed for the operation in rectification mode, however, ISM-MMC supports bidirectional power flow, hence inverter mode is also applicable. The digital oscilloscope present in the figure has an aim to display/verify certain quantities, while measurements and data acquisition, as it will be explained further, are made by employing standalone sensors and capabilities of the system controller. Circuital schematics and their description are given along with presented experimental results in the corresponding chapters of this thesis, while here they are omitted to avoid repetition. Therefore, it is assumed that the reader has familiarized him/herself with the structure of laboratory prototype and experimental setup before referring to this section. Table B.1 summarizes all necessary parameters and settings that has been used in all conducted experimental tests.

Table B.1 – Main parameters of the ISM-MMC laboratory prototype [144, 204]. © 2022 IEEE

Description	Symbol	Parameters
Power part parameters		
number of SMs per arm	N	2
number of HB-legs in each SM	K	3
rated dc output power and dc-link voltage	P_{dc}, V_{dc}	600 W, 200 V
rated ac input power, phase current (rms)	S_{ac}, I	750 VA, 15 A
ac phase voltage (rms) and fundamental frequency	V, f	50 V, 50 Hz
carrier frequency	f_{cr}	2 kHz
dc-link split capacitance (2×)	C_{dc}, $R_{ESR,dc}$	5.2 mF, 7.6 mΩ
individual interleaved leg inductor parameters	R_L, L	244.2 mΩ, 12.6 mH
individual SM capacitance	C, R_{ESR}	3.54 mF, 3.5 mΩ
Control settings		
dc voltage control bandwidth	$\alpha_{p,dc}$ | $\alpha_{i,dc}$	15 rad/s | 5 rad/s
averaging time of the dc moving-average filter (H_{dc})	–	10 ms
loop-filter bandwidth (PLL)	$\alpha_{p,pll}$ | $\alpha_{i,pll}$	50 rad/s | 10 rad/s
output current control bandwidth	$\alpha_{c,oc}$ | $\alpha_{r,oc}$	2000 rad/s | 50 rad/s
circulating current control	R_{cir} | $\alpha_{2,cir}$	1.7 Ω | 250 rad/s
LPF circulating current control	$k_{f,cir}$ | $\alpha_{f,cir}$	$\sqrt{2}$ | 100 rad/s
sorting frequency	f_{sort}	400 Hz
interleaved current balancing	$k_{p,intlv}$	0.006 A^{-1}
observer current and voltage gains	l_i, l_v	10 H^{-1}, 20000 s^{-1}
discretization step size	–	20 μs

B.1 Power Part

The metal rack, presented in Figure B.1 contains a single-phase ISM-MMC, a controller, measurement boxes and all necessary auxiliary power supplies mounted on the back-planes of the rack. This section is dedicated to the power stage of the laboratory ISM-MMC, while control and measurement subsystems are discussed in the following sections.

The laboratory ISM-MMC is formed by two interleaved submodules per arm (branch). A custom-made, two-level, three-leg converter that shapes the submodule is depicted in Figure B.2. The SM capacitor is mounted on printed circuit board (PCB) as well and attached to the dc rails of the SM converter. The converter's PCB design is based on integrated IGBT modules and it is made by Aalborg University, primary for other projects. The converter has been adopted for the

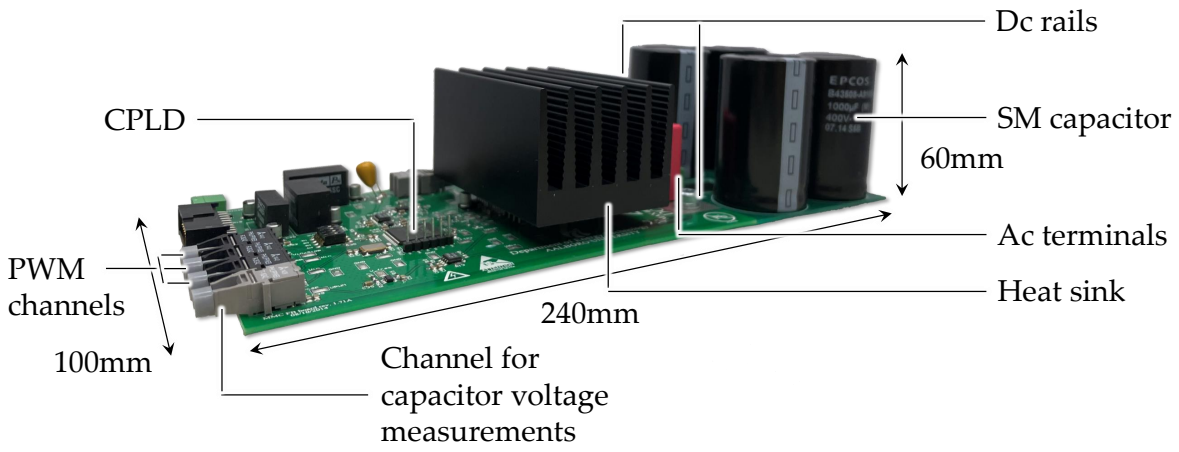

Figure B.2 – View of a custom-made three-leg converter that forms a SM of the laboratory ISM-MMC

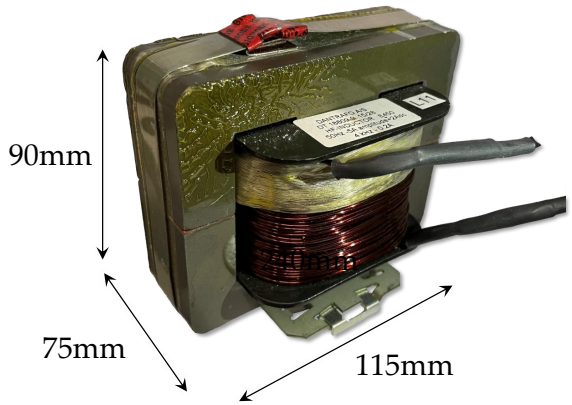

Figure B.3 – View of an individual interleaved HB-leg inductor that forms a SM of the laboratory ISM-MMC

Table B.2 – Technical characteristics of the laboratory ISM-MMC elements

Component	Type Name	Characteristics
ISM-MMC elements		
interleaved SM	–	up to 100 V, 4 A (rms)
dc-bus electrolytic capacitor	PEH200XO4220MU2 (Kemet Corp.)	385 V, 2.2 mF ±20%
	PEH169VV433GQ (Kemet Corp.)	400 V, 3.3 mF -10% +30%
SM converter-related components		
IGBT module [218]	DIPIPM PS219B4-AS (Mitsubishi Electric Corp.)	600 V, 15 A (@25°C), $f_{PWM} \leq 20$ kHz
CPLD chip	XC95144XL (Xilinx Inc.)	100-pin TQFP, system freq. $\leq$ 178 MHz
voltage controlled oscillator	LTC6990 (Analog Devices Inc.)	$f_{out} = 0.488...2000$ kHz, BW = $0.4 f_{out}$
Other SM components		
SM capacitor (×4)	B43508-A9108-M (Epcos AG)	400 V, 1000 μF ±20%
individual, custom-made interleaved inductor (×3)	DT 18809-9 15/28 (Dantrafo A/S)	±5 A amplitude + 2 A dc offset, 12.6 mH (@50 Hz)

current prototype realization. Therefore, the choice of current and voltage ratings of a single SM were dictated by the corresponding ratings of the converter components and individual interleaved inductors (cf. Figure B.3). Similarly, the initial choice of the inductors was dictated by reasonable switching current ripple within a SM at the given maximum amplitude of the fundamental current component and selected switching frequency. Table B.2 provides the basic characteristics of the ISM-MMC elements, with specific focus on the components of a single SM. This table introduce the rated values, guaranteed by manufacturer, while Table B.1 provides the real measured values of the component parameters (e.g., resistance, inductance, capacitance) with the help of precision LRC meter (4284A, Keysight Technologies Inc.).

Some additional details must be highlighted about the SM converter illustrated in Figure B.2. First of all, the mounted on top of the board CPLD (XC95144XL, Table B.2) has an aim to provide start-up PWM synchronization and internal protection services (e.g. over-voltage, excessive thermal stress) of the converter. If a fault happens, the internal logic of the CPLD will open all converter's switches to protect the board from damage. Secondly, the board features an integrated dc-link voltage transducer built based on voltage controlled oscillator (LTC6990, Table B.2). The output of the oscillator is a frequency modulated signal that is transmitted via optical transmitter (gray front port, Figure B.2). Ports of PWM channels are also made by optic receivers. In such arrangement the I/O of the board are galvanically isolated from the ISM-MMC controller.

The laboratory ISM-MMC has the double-star arrangement, where the composing arms from on one side are connected to the corresponding dc-bus terminals (positive or negative), while on the other side are joined together and linked with an ac supply. The midpoint of dc-bus split-capacitors (cf. Table B.2) provides a connection point for the neutral wire of the ac supply. To achieve the sufficient value of dc-bus split-capacitors (C_{dc}, cf. circuital diagram of the laboratory setup), each one of them is formed by parallel connection of two electrolytic capacitor types listed in Table B.2.

To supply the low voltage electronics, an auxiliary power supply units are included in the equipment enclosed in the rack. For short-circuit and over-current protection, miniature current breakers are introduced in both main (ac and dc) and auxiliary power circuits with corresponding characteristic trip curves. The metal cases of the equipment, including ISM-MMC rack are grounded to ensure safety from earth fault currents. A power contactor is included in the main ac power circuit to create a possibility for manual disconnection of the converter from the power supply. The remote button to operate the contactor along with a light indicator is placed on the front door of the converter's rack.

Table B.3 – Technical characteristics of the auxiliary instruments employed in the laboratory setup

Component	Type Name	Characteristics
programmable ac power source (grid emulator)	MX 30 (Ametek Inc.)	30 kVA, output voltage range 0...300 V
programmable dc electronic load	EA-EL 9400-50 (Elektro-Automatik GMBH)	2400 W, 0...400 V / 0...50 A
variable resistive load	ZRF (Danotherm Electric A/S)	2500 W, 600 V, 3Y: 57R5, 115R, 230R, 460R
digital oscilloscope	DL9040 (Yokogawa Electric Corp.)	5 GS/s, 500 MHz

To isolate the laboratory ISM-MMC from grid mains and adjust the required level of ac voltage, a programmable ac power source (grid emulator) has been used. The grid emulator has internal

over-current protections that limit the currents, providing additional safety loop to the circuit. At the dc terminals, the converter is connected to either a variable resistor (R_{dc}) or a programmable dc electronic load. The electronic load is also featured by over-current protection.

MMC-based converters, having relatively high capacitive energy storage, are well-known for large inrush currents at start-up. To prevent potential damage of the equipment, the ac supplied has been programmed to increase its output voltage starting from 10 V to the nominal value with a ramp. Once the converter capacitors are precharged, the converter's controller is activated and experiment may start. Table B.3 provides a basic information for the instruments that have been employed.

B.2 Control Part

The entire control scheme and ADC/DAC conversion are implemented inside the controller for rapid prototyping RT Box 1 [203]. The RT Box 1 is formed by a Xilinx Zynq Z-7030 system-on-chip that embeds two CPU cores (ARM Cortex-A9, 1 GHz) on an FPGA. One of this cores is used to run an embedded Linux OS for communication and ancillary services, while the remaining core performs the controller computations. The FPGA is employed to control the digital I/Os and analog data conversion. The ADC/DAC converters in the RT Box 1 both feature 16 bit resolution with simultaneous sample and update (maximum sample/update rate is 5 Msps). RT Box 1 contains 16 analog inputs, 16 analog outputs, 32 digital inputs and 32 digital outputs. The voltage ranges in inputs and outputs can be adjusted to the standard industrial values. All I/Os are isolated. The communication with a PC is made through gigabit Ethernet ports. RT Box 1 supports multi-tasking mode, where the designed model can be split into separate physical sub-systems and run in parallel on the same CPU with different sampling periods. The full RT Box 1 specification is available in [203].

The RT Box 1 operates as a target machine governed by a host computer with running Plecs Standalone and Plecs Coder (Plexim GmbH). The Plecs Coder compiles a pre-designed for an experiment Plecs model and uploads it into the RT Box 1. The original Plecs model on the host computer can be interconnected with the RT Box 1 using an External Mode. This allows from one side to tune parameters of the controller in real-time, including control enabling/disabling sequences and from the other side to visualize from Plecs Scope the quantities processed by RT Box 1.

A Plecs model with the control schemes suggested in this thesis was built. The model is structured in a versatile manner, so different control regimes (e.g. dc current and voltage steps, interleaved current control loop enabling/disabling, etc.) can be implemented on fly. In addition to that a Python script was prepared to control RT Box 1 for automated test environment (both control requests and data capture) using an XML-RPC interface. XML-RPC is a protocol for executing functions on a remote machine. In this manner, the RT Box 1 acts as an XML-RPC server, which processes requests sent from scripts running on the host computer.

B.3 Measurements and Signal Acquisition

Several measurement boxes are mounted on the front-top and back-planes of the rack to provide sensed analog signals to the controller. As it pointed out in Section B.2, analogue-to-digital

conversion is handled by RT Box 1, while practically all the required signals (cf. experiment-related circuital diagram of the laboratory setup) apart of SM capacitor voltage measurements enter RT Box 1 as analog inputs. In Section B.1 it is explained that the SM capacitor voltage measurements are processed on the SM converter board with digital output. Therefore, these signals are transmitted to the controller via its digital inputs. Later they are demodulated and used for control monitoring purposes.

Table B.4 – Technical characteristics of the sensors employed in the laboratory setup

Component	Type Name	Characteristics
voltage transducer	LV 25-P (LEM Europe GmbH)	$I_{PN} = 10$ mA, $V_{PN} = 10...500$ V, total err. $\pm 0.9\%$
current transducer	LA 55-P (LEM Europe GmbH)	$I_{PN} = 50$ A, total err. $\pm 0.65\%$, BW = DC...200 kHz

Two types of galvanically isolated voltage and current transducers were employed in the laboratory setup. Their characteristics are depicted in Table B.4. The sensing ranges has been adjusted accordingly to the maximum permitted quantities at the measuring points to insure high sensing resolution.

All measured quantities of interest are sampled and/or processed by the controller along with some internal controller-related quantities are transmitted to a host computer and stored on its internal memory by using a high speed Ethernet interface. Later these data points are elaborated by Matlab (MathWork Inc.) for analysis and data visualisation. High sampling frequency and relatively low switching frequencies of the converter guarantee accurate reconstruction of real analog quantities.

List of Abbreviations

N2K3f1k	ISM-MMC configuration with two SMs per arm ($N = 2$) and three interleaved HB-legs in each SM ($K = 3$) that operates with carrier frequency 1 kHz ($f_{cr} = 1$kHz)
N2K3f333	ISM-MMC configuration with two SMs per arm ($N = 2$) and three interleaved HB-legs in each SM ($K = 3$) that operates with carrier frequency 333 Hz ($f_{cr} = 333$Hz)
N2Kp3f1k	MMC configuration with two HB-based SMs per arm ($N = 2$), where HB-leg composed by two sets (upper and lower) of three parallel switches ($Kp = 3$) that commutate simultaneously with carrier frequency 1 kHz ($f_{cr} = 1$kHz)
N6K1f1k	MMC configuration with six HB-based SMs per arm ($N = 6$) that operates with carrier frequency 1 kHz ($f_{cr} = 1$kHz)
2D	Two dimensional
ac	Alternating current
ADC	Analog-to-digital converter
APOD	Alternative phase opposition disposition (level-shifted pulse-width modulation)
BESS	Battery energy storage system
CHB	Cascaded H-bridge (converter)
CNPC	Cascaded neutral-point clamped (converter)
CPLD	Complex programmable logic device
CPU	Central processing unit
CSC	Current source converter
DAC	Digital-to-analog converter
dc	Direct current
DSOGI-PLL	Dual second order generalized integrator PLL
DTC	Direct torque control

ESR	Equivalent series resistance
EV	Electrical vehicle
FACTS	Flexible alternating current transmission system
FC	Flying capacitor (converter)
FLL	Frequency-locked loop
FOC	Field-oriented control
FPG	Frequency/phase-angle generator
FPGA	Field-programmable gate array
GTO	Gate turn-off thyristors
HB	Half-bridge
HE	Hydrogen electrolyzer
HIL	Hardware-in-the-loop (simulation)
HVDC	High-voltage direct current (transmission)
I/O	Input/output
IEEE	Institute of electrical and electronics engineers
IGBT	Insulated-gate bipolar transistor
IGCT	Integrated gate-commutated thyristors
ISM-MMC	Modular multilevel converter with interleaved half-bridge submodules
LF	Loop filter
LLC	Abbreviation for an arrangement that consist of inductance (L) and capacitance (C)
LPF	Low-pass filter
LRC	Abbreviation for an arrangement that consist of inductance (L), resistance (R) and capacitance (C)
LS-PWM	Level shifted pulse-width modulation
LTI	Linear time-invariant (system)
MMC	Modular multilevel converter
MOSFET	Metal-oxide-semiconductor field-effect transistor
MPC	Model predictive control
MV	Medium-voltage
NLC	Nearest level control (modulation)
NPC	Neutral-point clamped (converter)

OS	Operational system
PC	Personal computer
PCB	Printed circuit board
PD	Phase disposition (level-shifted pulse-width modulation)
PD	Phase detector
PDF	Probability density functions
PET	Power electronic transformer
PFC	Power factor correction (converter)
PI	Proportional–integral (controller)
PLL	Phase-locked loop
PNSC	Positive-/negative-sequence calculation (block)
POD	Phase opposition disposition (level-shifted pulse-width modulation)
PR	Proportional–resonant (controller)
PS-PWM	Phase shifted pulse-width modulation
PWM	Pulse-width modulation
QSG	Quadrature signal generator
rms	Root-mean-square
SHE	Selective harmonic elimination
SM	Submodule
SOGI	Second-order generalized integrator
SOGI-QSG	Second-order generalized integrator QSG
SRF	Synchronous reference frame
SRF-PLL	Synchronous reference frame PLL
SST	Solid-state transformers
STATCOM	Static synchronous compensator
SVM	Space vector modulation
THD	Total harmonic distortion
VCO	Voltage-controlled oscillator
VOC	Voltage-oriented control
VSC	Voltage source converter
WTHD	Weighted total harmonic distortion

List of Symbols

Variables, parameters, and functions

$\alpha_{2,cir}$	Desired resonant bandwidth of circulating current regulator
$\alpha_{c,oc}$	Desired closed-loop bandwidth of output current controller
$\alpha_{f1,W}, \alpha_{f2,W}$	Desired bandwidth of low pass filters in arm-energy control
$\alpha_{i,dc}$	Dc-bus voltage integrator bandwidth
$\alpha_{i,pll}$	PLL integrator bandwidth
$\alpha_{p,dc}$	Dc-bus voltage control-loop bandwidth
$\alpha_{p,pll}$	PLL proportional control-loop bandwidth
$\alpha_{r,oc}$	Desired resonant bandwidth of output current controller
α_W	Desired bandwidth of arm-energy control
$\Delta i_{cir,x}$	Increment of phase leg-common mode current (for three-phase system $x = a,b,c$, otherwise phase label is omitted)
δ	Duty cycle
$\Delta\vartheta_{cr}$	Phase displacement between carriers (LS-PWM)
η	Converter efficiency
η_{max}	Peak (maximum) converter efficiency
$\mathbb{A}, \mathbb{B}, \mathbb{C}$	State, input and output matrices in LTI state-space representation
$\mathbb{G}_k$	Set of firing signals for a SM, where each row represent different combination of upper switch states (dimensions $K \times K$)
$\mathbb{L}$	Matrix with observer gains $\mathbb{L} = [l_v, l_i]$
$\mathbb{O}$	Kalman observability matrix

ω	Fundamental angular frequency
$\overline{g}_{n,k}$	Bottom switch firing signal in the k-th HB-leg of the n-th submodule
σ	Standard deviation
$\mathbf{x}, \mathbf{u}, \mathbf{y}$	State, input and output vectors in LTI state-space representation
ε'_{oc}	Modified current error of output current controller, associated with antiwindup controller function
ε_{oc}	Current error of output current controller
$\vartheta_{cr,k}$	Carrier phase shift (PS-PWM) for k-th HB-leg
ϑ_x	Grid voltage phase angle (for three-phase system $x = a,b,c$, otherwise phase label is omitted)
ζ_n	Number of active HB-legs in the n-th submodule
A_{cr}	Carrier amplitude (LS-PWM) in p.u.
C'_{dc}	Effective converter's dc-link capacitance
C, R_{ESR}	Capacitance of the submodule's dc-link capacitor and its equivalent series resistance
C_{arm}	Equivalent arm capacitance
$C_{dc}, R_{ESR,dc}$	Capacitance of the converter's dc-link capacitor and its equivalent series resistance
d_{cr}	Level carrier displacement (LS-PWM) in p.u.
d_{nk}	Logical PWM signal for the k-th HB-leg of the n-th submodule (output of the carriers and modulation signal comparator block)
d_{on}, d_{off}	On-state and off-state duty cycle
f	Fundamental frequency
f_{cr}	Carrier frequency (PWM modulation)
f_{sort}	Sorting frequency
$g_{n,k}$	Top switch firing signal in the k-th HB-leg of the n-th submodule
$H_{1,W}, H_{2,W}$	Low pass filters in arm-energy control
H_{dc}	Low pass filter in dc-bus voltage control-loop
h_{nk}	Carrier signal for the k-th HB-leg of the n-th submodule
$i_{cap,n}$	Capacitor current in the n-th submodule

$i_{cir,x}$	Converter's phase leg-common mode current (for three-phase system $x = a,b,c$, otherwise phase label is omitted)
i_{dc}	Dc-bus current
$i_{n,k}$	Interleaved current in the k-th HB-leg of the n-th submodule
i_{ux}, i_{lx}	Upper and lower arm currents within a phase leg (for three-phase system $x = a,b,c$, otherwise phase label is omitted)
i_x	Phase current (for three-phase system $x = a,b,c$, otherwise phase label is omitted)
$J_{1,K}$	Vector of ones with dimensions $1 \times K$
j_a, j_d	Lists of indices in ascending and descending order (capacitor voltage balancing algorithm)
K	Number of parallel/interleaved half-bridges inside each submodule
k_Σ, k_Δ	Control gains of arm-energy control for total and difference energy path
$k_{f,cir}, \alpha_{f,cir}$	Gain and desired bandwidth of LPF in circulating current control
$k_{i,cir}$	Resonant gain of circulating current regulator
$k_{p,intlv}$	Proportional gain of interleaved current balancing controller
$k_{p,oc}, k_{i,oc}$	Proportional and resonant gains of a PR controller
k_{pll}	Gain of SOGI-QSG block
M	Number of converter phases
m_x	Phase leg modulation index (for three-phase system $x = a,b,c$)
N	Number of submodules in each arm
P	Mean ac-side active power
P^*_{fb}	Reference active power given by feedback control loop
P^*_{ff}	Reference active power given by feedforward control loop
P_{cap}	Converter's power losses in SM capacitors
P_{con}, P_{sw}	Converter's conduction and switching power losses
P_{dc}	Dc-side power
P_{driv}	Constant power dissipation in semiconductor drive circuit
P_{gate}	Switching frequency-dependent gate-drive losses

P_{ind}	Converter's power losses in inductors
P_{in}, P_{out}	Converter's input and output power
P_{loss}	Total converter's power losses
Q_g	Gate charge in a semiconductor
R', L'	SM's equivalent resistance and inductance with respect to a number of active HB-legs
R, L	Equivalent resistance and inductance of the HB-leg path in a SM
R_{arm}, L_{arm}	Resistance and inductance of an arm inductor
R_{cir}	Proportional gain of circulating current regulator ("active resistance")
s	Complex number frequency parameter (Laplace transform)
S_{1k}, S_{2k}	Top and bottom switches in the k-th HB-leg of a SM
S_{ac}	Apparent ac-side power
$T_{\alpha\beta}, T_{dq}$	Operators of Clarke's and Park's transformations, respectively
T_{cr}	Carrier period (PWM modulation)
u_n	Normalized submodule insertion index (modulating signal)
$u_{u,l}$	Normalized per-arm insertion index (modulating signal)
$v_{cap,n}$	Capacitor voltage in the n-th submodule
$v_{cir,x}$	Converter's phase internal voltage (for three-phase system $x = a,b,c$, otherwise phase label is omitted)
$v_{dc,u}, v_{dc,l}$	Pole-to-ground dc-bus voltages
v_{dc}	Pole-to-pole dc-bus voltage
$v_{s,x}$	Converter's phase output voltage (for three-phase system $x = a,b,c$, otherwise phase label is omitted)
v_{SMn}	SM's voltage of the n-th submodule
v_{ux}, v_{lx}	Upper and lower arm voltages within a phase leg (for three-phase system $x = a,b,c$, otherwise phase label is omitted)
v_{xy}	Line-to-line voltage (for three-phase system $x = a,b,c$, $y = b,c,a$)
v_x	Phase voltage (for three-phase system $x = a,b,c$, otherwise phase label is omitted)
$W^*_{\Sigma}, W^*_{\Delta}$	Integration gains of total per-phase and imbalance energy

W_Σ, W_Δ	Total per-phase and imbalance energy
W_ε	Energy in the increment (Lyapunov function)
W_{dc}	Effective dc-bus energy
W_{on}, W_{off}, W_{rec}	Turn-on, turn-off loss and diode reverse recovery energies in a semiconductor
W_u, W_l	Total stored upper and lower arm energy

Principle Notation

Δz	Increment of z values
$\hat{z}$	Estimated value of z
$\mathbb{Z}$	2D array (matrix) of variables z
$\overline{z}$	Mean value of z
$\mathbf{Z}$	Vector of variables z
$\tilde{z}$	Error value between real z and its estimate $\hat{z}$
Z	rms value of z (for dc - mean value)
z	Instantaneous value of z
z^*	Reference value of z
z^+	Positive sequence component of z
z^-	Negative sequence component of z
z^Σ	Sum of related to z values

Superscripts, subscripts, circumflexes, and prefixes

α, β	Component indicators of the stationary $\alpha\beta$ reference frame
d, q	Component indicators of the synchronous dq reference frame
m	Ordinal number of a converter's phase leg
n, k	Ordinal number of a submodule (SM) and an interleaved half-bridge inside the SM
u, l	Upper and lower arm indicators
x	Phase label (for three-phase system $x = a,b,c$)

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Aleksandr Viatkin

Curriculum Vitae

Education

Oct. 2021 | **Ph.D. Electrical Engineering, UNIVERSITY OF BOLOGNA, Italy**

Nov. 2018 | **Period abroad:** *Guest PhD student, **Aalborg University, Aalborg, Denmark (Nov. 2020 - Jul. 2021)***

Project: *Modular Multilevel Converters with Interleaved Half-Bridge Submodules*

- Developed a new MMC-based topology specifically suitable for high-current, low-voltage applications
- Designed the converter's closed-loop control algorithm for operation in grid-connected applications
- Created analytical formulation and numerical simulation models (Simulink, Plecs). Tested the designed system in hardware-in-the-loop simulator (RTBox, Plexim). Built a laboratory prototype

Project: *Smart EV charging technology*

- Designed a front-end side of an on-board EV charger that is capable to work in both G2V an V2G modes, constantly providing power conditioning serviced to the power grid
- Composed converter's closed-loop control algorithm
- Created numerical simulation models (Simulink). Built a laboratory prototype

Power electronics | MMC | Closed-loop control | Hardware-in-the-loop | On- and off-board EV chargers | V2G

Dec. 2017 | **M.Sc. Electrical Energy Engineering, UNIVERSITY OF BOLOGNA, Italy**

Oct. 2015 | **Period abroad:** *ERASMUS program, **Technical University of Munich, Munich, Germany (Sep. 2016 – Oct. 2017)***

Thesis: *Development of a Test Bench for Multilevel Cascaded H-Bridge Converter with Self-Balancing Level Doubling Network*

Power electronics | Multilevel converter | CHB | LDN | Closed-loop control | Power quality | Battery Energy Storage

Jun. 2010 | **Electrical Engineering degree (5 years), URAL FEDERAL UNIVERSITY, Russia**

Sept. 2005 | **Thesis:** *Development of technical solutions for reducing energy losses in the heating producing company of Chelyabinsk*

Power quality | Reactive power compensation | Static compensator

Professional Experience

Nov. 2021 – present

R&D Scientist - Power Electronics, HITACHI ENERGY, Sweden

- Develop and provide solutions for technical challenges in R&D projects
- Conduct laboratory tests, analyze data, and improve/optimize the solutions
- Lead R&D projects or work-packages with a structured working style, target-oriented strategy and effective leadership

HVDC | FACTS | E-STATCOM | BESS

Oct. 2018 – Feb. 2018

Research assistant (power electronics), UNIVERSITY OF BOLOGNA, Italy

Project: Superconducting Energy Storage for Smart Electrical Grid DRYSMES4GRID

- Developed an entire control method for a grid supporting system based on a hybrid battery and superconducting magnetic energy storage

Grid-forming & grid-following converter control | Active power filter | SMES

Aug. 2015 – Oct. 2014

Electrical Project Engineer (construction site), INTERNATIONAL PAPER, Svetogorsk, Russia

Project: Reconstruction of the main step-down substation 110/10 kV PGV-1 with replacement of cable lines 10 kV from the factory power plants PP-3 and PP-4

- Prepared detailed project schedule, monitored procurement and logistic of equipment and materials
- Examined and approved electrical design drawings for the construction
- Inspected contractors working on site (50 workers), ensuring agreement with safety code
- Supervised electrical equipment installation, commissioning and acceptance of the finished work

SF6 switchgear | IEC61850 protection & control | Project management

Dec. 2013 – Jul. 2011

Electrical Design Engineer (relay protection & automation), ENERGOPROJECT LTD., Ekaterinburg, Russia

Projects for the Federal Grid Company of Russia:

- System integrity protection for the overhead power line 500 kV "Krasnoarmeyskaya – Gazovaya"
- Reconstruction of the substation 500 kV "Yuzhnay", Ekaterinburg
- Construction of the substation 220 kV "Nadezhda", Ekaterinburg

- Developed a concept of protection & control, measurement and monitoring systems
- Prepared electrical schematics, control layouts, specifications and wiring diagrams for manufacturing and installation of electrical equipment on site

Vacuum & SF6 switchgears | IEC61850 protection & control | IEEE C37.118.2 synchronized phasor measurements

Jun. 2011 – Aug. 2009 | **Electrical Design Engineer (relay protection), URAL DESIGN INSTITUTE TELPRO LTD., Ekaterinburg, Russia**

Projects: Construction of the substations 110 kV "Palniki" (Perm region), 110 kV "Tobol" (Kurgan) and several projects in chemical, gas & oil industries (Perm and Sverdlovsk regions)

- Prepared electrical schematics, control layouts, specifications and wiring diagrams for manufacturing and installation of medium voltage switchgears

Vacuum switchgear

Competencies

Microcontrollers, SOCs & Target Machines	TMS320F2837xD (TI), STM32F4x (STMicroelectronics), Arduino Due A000062, Zedboard Zynq-7000 (Xilinx), Performance RTTM 109200 (Speedgoat), dSpace DS1006, RT-Box (Plexim)
Programming languages	C, C++, Python, Matlab, SystemVerilog, VHDL
Development platforms	MATLAB/Simulink, Plecs, LTSpice, LabView, ANSYS Electronics, CCS, ModelSim, Vivado Design Suite, ATPDraw, SKM, EMTP
Design tools	Autodesk AutoCAD (2D, 3D, Electrical), Autodesk Eagle, Altium Designer
Languages	**Russian** (Native speaker) **English** (C2, Fluent) **Italian** (B1, Intermediate)

Grants and Awards

2020/21 Marco Polo Scholarship, University of Bologna, Bologna, Italy

2016/17 University Excellence in Studying Award, University of Bologna, Bologna, Italy

2016/17 ER.GO Study Grand, ER.GO, Bologna, Italy

Scientific Record

THE FULL LIST OF PUBLICATIONS IS ACCESSIBLE VIA ORCID OR GOOGLE SCHOLAR

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Bibliometric indicators (updated on January 26, 2022):

- scientific publications: 20
- total citations: 103
- h-index: 6
- i10-index: 2