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Dc-link current and voltage ripple analysis in single-phase and multiphase voltage source inverters

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Abstract

Dc-link switching and low-frequency current and voltage ripple components in two-level single-phase and multiphase voltage source inverters have been analyzed in this thesis. Analysis of dc-link inverter variables is important for estimating dc voltage ripple profiles that affect all the dc-link components. These ripple profiles can be used to size the dc-link capacitor properly and to assess the life-span or degradation of components such as battery packs and the dc-link capacitor itself. Hence, simple and effective methods for designing the dc-link capacitor are proposed in this thesis, relating the value of capacitance to the maximum required peak-to-peak value of the dc voltage ripple.

Voltage ripple components are calculated based on the corresponding dc-link current components and by considering a non-ideal dc voltage source, representing an input filter (such as a dc reactor) or a resistive dc supply (such as a PV system). However, switching ripple analyses are also valid in most of the dc power supplies since the dc source impedance usually becomes much higher than the dc-link capacitor reactance at the inverter switching frequency. The peak-to-peak voltage switching ripple amplitude is derived over a fundamental period as a function of operational conditions: modulation index, the amplitude of phase current and power phase angle. For all presented multiphase topologies reference is made to the two most commonly applied modulation techniques, sinusoidal PWM and space vector modulation.

The initial investigation of the dc-link variables has been focused on single-phase H-bridge inverter, considering both, switching and low-frequency dc ripple components. The analysis has been further extended to the case of two-level multiphase inverters with balanced load. Some general steps in the analysis of the dc-link current and voltage switching ripple in multiphase inverters have been presented considering an odd number of phases. The approach has been specifically developed for three-, five- and seven-phase inverters. To present the behavior of the peak-to-peak dc voltage ripple amplitude, different diagrams are shown covering full range of modulation index and power phase angle. Maximum of the peak-to-peak voltage ripple amplitude is determined as a function of modulation index. The cases with different phase numbers are compared and the effect of increasing the number of phases on the dc-link capacitor sizing has been discussed.

The final analysis has also included the impact of a slight load unbalance on the dc-link variables in multiphase inverters. Considered unbalance is present in practice in every multiphase ac motor, it is in order of a few percent, and introduces a low frequency instantaneous power oscillation. This reflects in low frequency (i.e. double-fundamental) current and voltage ripple on the dc-link inverter side. Therefore, the amplitudes of both ripple components are calculated and the importance of taking them into consideration for the dc-link capacitor design has been discussed.

All analytical developments are validated with detailed simulations and experimental results.

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Chapter 1

Introduction

1.1 Motivation for Research

Move to a more energy efficient and sustainable society is an objective shared by many countries worldwide. One of the key technologies in that transition is power electronics which enable conversion of electrical energy from one stage to another. Due to the continuous improvements and new developments in power electronics components, the range of their applications has greatly expended over the last years, such as in electrical power generation, transmission, distribution and end-user electricity consumption.

In recent years, the major requirements that have been set by industrial and energy sector are high reliability and efficiency of power electronics systems, as well as low operational and maintenance cost. To achieve the desired electrical performance of the system, within acceptable price, it is necessary to properly size and design power electronics components. Besides active semiconductor power devices, capacitors are another type of components that fail more frequently than other parts in power electronics systems.

Dc-link capacitors in voltage source inverters (VSIs) have multiple and critical role in the system. They serve to balance the instantaneous power difference between the input source and output load, as well as to reduce the emission of electromagnetic interference (EMI) and to limit voltage/current ripple both for steady-state and transient. As a consequence of the high-frequency PWM switching in an inverter, high frequency current ripple component is injected to the dc-link. On the other side, depending on the source and inverter topology, low frequency ripple component can be injected from the source side. The presence of high ripple currents on the dc-link side causes the increase of capacitor's core temperature, and thus accelerates the degradation of the capacitor itself. The dc-link voltage ripple results in undesirable impact on the reliability of the dc-link capacitors. Therefore, current and voltage dc-link ripple components are considered as crucial factors for the dc-link capacitor design and its lifetime prediction analyses.

The research effort related to the selection on the dc-link capacitor type in voltage source inverters has been mainly focused on the investigation of the current ripple spectrum. By calculating the current ripple stress and depending on the required capacitance, a preliminary capacitor design can be determined. There are, however, different perspectives

on the challenges in the design and selection of dc-link capacitors. Some of them are the reduction of weight and volume, the ensurement of high reliability for exposure to harsh environments (in emerging applications, high ambient temperature, excessive humidity, etc.), the prevention of overheating, the extension of life time and cost reduction. For instance, in real-world applications, such as the applications of renewable energy, the ambient temperature profile and the degradation of the power electronic components, such as the dc-link capacitor itself and the switching devices, could affect the dc-link current ripple components and should be also taken into account. Hence, considering various factors such as the ambient temperature, energy dump handling capability, capacitor parasitics, the maximum tolerable dc-link voltage, overall system stability when multiple power converters and sources/loads are connected to a common dc-link capacitor, the sizing of this capacitor turns to be complex task.

Usually, in order to simplify the theoretical analysis, the power converters are assumed to be lossless and parasitic elements of the dc-link capacitors - an equivalent series resistor (*ESR*) and the equivalent series inductor (*ESL* or L_s) - are neglected. The equivalent series resistance represents the conducting and dielectric losses of the capacitor while the inductance is introduced by the leads or terminals of the capacitor as well as the inner construction of the capacitor itself. However, depending on a given application and the type of the capacitor, the parasitic elements can significantly affect capacitor's performance for high frequencies. To understand if said parameters have the effect on the dc-link current and voltage ripple, a capacitor is most commonly modelled as a series connection of an ideal capacitor (C) and its parasitic elements. By comparing the inverter's switching frequency with the self-resonance frequency of the dc-link capacitor, the effect of L_s can be established. Similarly, to establish the effect of *ESR*, a comparison between the *ESR* and the value of sqrt(L_s/C) should be also made. For the switching frequencies well below the self-resonant frequency of the dc-link capacitor, its inductive reactance is negligible comparing to the capacitive reactance, and the same applies to *ESR* if it has similar or lower value compared to sqrt(L_s/C). Usually, in application such as inverter-fed drives an adopted dc-link capacitor is in the order of few hundred or thousand μF, and the resulting self-resonant frequency is always higher comparing to the switching frequency. This means that, for said application, the effects of capacitor's parasitic elements on the dc-link voltage ripple are negligible at the switching frequency.

Depending on the wide range of power electronics applications different inverter topologies are utilized and consequently various types of capacitors are adopted. Single-phase voltage source inverters cover mostly the low-power range applications. With simple structure they are widely used in industry applications such as uninterruptible power supply (UPS), power supplies and renewable energy conversion system. In medium- and high-power applications, such as three-phase variable speed drives, flexible ac transmission systems (FACTs), stand-alone and grid-connected power generation systems, the most fre-

quently utilized power inverters by far are the three-phase two-level ones. This is mainly due to the wide off-the-shelf availability of both three-phase machines and converters. However, for some specialized applications, such as the high-power industrial applications, electric and hybrid electric vehicles (EVs), railway traction, ship propulsion, "more-electric" aircraft, etc., three-phase drives usually do not satisfy certain specifications and the multiphase inverter-fed variable-speed drives appear as a preferable solution. Multiphase power inverters can be built with an arbitrary number of phases and from the hardware point of view the only necessity is to have equal number of inverter legs and phases. Among many beneficial features of multiphase inverter-fed drives which make them highly desirable solutions for aforementioned high-power applications, particularly important ones are reduced current (power) rating of the semiconductor switches and excellent fault-tolerant operation features.

The type selection and design of the capacitor in the dc-link of inverters is dictated by the application requirements and circuit parameters. Generally, fundamental and widely used capacitors are: aluminum electrolytic and film capacitors. They are used in both low and high-power applications covering the wide range of size, voltage and capacitance variations. Conventional capacitor design strategies have been using the set of aluminum electrolytic capacitors due to their high capacitance per unit volume and good price over performance ratio. This type of capacitor is particularly suitable in the applications such as the diode/thyristor rectifier front-end where the low-frequency current ripple is imposed at the input (dc-link) side, consequently introducing the large dc-link voltage ripple. However, in case of high frequency ripple current, a single low-inductance high-current film capacitor could be a good alternative option reducing its size, improving reliability and significantly reducing voltage spikes. Moreover, a use of film capacitor allows the life expectancy to be extended and lower value of capacitance is needed in comparison with an electrolytic counterpart. The reason is that a film capacitor is limited by the maximum dc-link voltage ripple rather than by the ripple current rating.

Most of the analysis related to the dc-link current and voltage ripple of the inverters are based on RMS calculations. However, there is a lack of analysis related to the peak-to-peak voltage ripple behavior particularly for two-level multiphase inverters. This thesis is devoted towards the analysis of the dc-link current and voltage ripple components in two-level single-phase and multiphase voltage source inverters aiming to provide simple guidelines for designing the dc-link capacitor based on developed strategy.

1.2 Research objectives and main contributions

The principal objective of this research has been the development of a novel methodology to mathematically model and analyse the dc-link peak-to-peak voltage switching and low-frequency ripple components that could be used for the dc-link capacitor design. It has been focused on two-level single-phase and multiphase inverters with an odd number

of phases. Initially, only balanced loads have been considered such as multiphase ac motors. Postliminary, a small degree of unbalance, always present in real-world applications, has been also examined. Theoretical approach has been verified by numerical simulations and comprehensive experimental tests for all considered inverter topologies.

The main objectives of this research can be summarized as follows:

1. To calculate the dc-link current ripple components in single-phase and multiphase inverters with the dc-source impedance, considering balanced and (slightly) unbalanced load conditions.

2. To perform theoretical investigation of the dc-link voltage switching and low-frequency ripple components in single-phase H-bridge inverter, and to calculate the peak-to-peak dc-link voltage ripple envelopes. To prove theoretical analysis by means of numerical simulations and experimental tests.

3. To extend the analysis of the dc-link peak-to-peak voltage switching ripple component to multiphase inverters with an odd number of phases, with special emphasize on three-, five- and seven-phase inverters. To apply two most popular modulation techniques to all examined inverter configurations and to make a comparison within different cases. To verify the analytical approach by numerical simulations and experimental tests.

4. To investigate the impact of slightly unbalanced load on the dc-link variables in three-phase inverters. To calculate the current sequence components and to estimate the current unbalance level. To determine the amplitudes of the dc-link low-frequency current and voltage ripple components. To verify the analytical developments by numerical simulations and experimental tests.

5. To extend the analysis of low-frequency current and voltage ripple components to the general *n*-phase case. To calculate the current sequence components and the amplitude of the low-frequency voltage ripple. To provide numerical and experimental tests for five- and seven-phase inverters and to make comparison within considered cases.

5. To propose the dc-link capacitor design based on the dc-link switching and low-frequency voltage ripple requirements for all mentioned inverter topologies. To investigate the impact of increasing the number of phases on the dc-link capacitor sizing.

Significant new knowledge and original contribution have been produced by achieving the objectives listed above. A particular contribution has been achieved by the development of the dc-link variables for the two-level seven-phase inverters. Also, important is the comparison of the maximum peak-to-peak value of the dc-link voltage switching ripple amplitude within different inverter topologies and its effect on the dc-link capacitor design. The effect of slightly unbalanced load to the dc-link variables in multiphase inverters has

been also investigated for the first time in this thesis. The original contribution is partially evidenced by the already published journal and conference papers that are given in the following sub-section 1.4.

1.3 Thesis outline

The thesis is structurally divided into six chapters and original contribution is provided by Chapters 2-5.

Chapter 1 presents the main concepts of the thesis together with the motivations supporting the study performed, research objectives and original contributions which have been produced by achieving them.

Chapter 2 introduces the dc-link current and voltage ripple analysis for the most fundamental configuration used for dc/ac power conversion – single-phase H-bridge inverter with dc source impedance. Both low-frequency and switching frequency dc-link voltage ripple components are analyzed. Based on the dc-link voltage ripple requirements, the design of the dc-link capacitor is proposed. The theoretical analysis is accompanied with the numerical simulations and experimental results.

Chapter 3 extends the analysis of the dc-link current and voltage ripple to two-level three-phase inverters with balanced load. A brief overview of two most commonly applied modulation techniques is provided. Dc-link voltage switching ripple envelope is derived and its maximum peak-to-peak value is calculated. The dc-link capacitor design is proposed relating the value of capacitance to the maximum value of the voltage switching ripple amplitude. Numerical simulations and experimental results are included to support the theoretical developments.

Chapter 4 deals with the analysis of the dc-link variables in two-level multiphase inverters with an odd number of phases, considering balanced load. A short review of two most popular PWM techniques for multiphase inverters, sinusoidal and space vector, is given. The dc-link voltage switching ripple envelope is calculated focusing on five- and seven-phase inverters. The comparison in terms of the peak-to-peak voltage switching ripple amplitude is made considering different number of phases, two modulation techniques and different operational conditions. The impact of the dc-link capacitor's parasitic elements on the dc-link voltage ripple has been also examined. Simple guidelines for designing the dc-link capacitor are proposed. Obtained theoretical results are verified by numerical and experimental tests.

Chapter 5 examines the impact of slightly unbalanced load on the dc-link current and voltage ripple in three-phase and multiphase inverters. An overview of the most popular transformations applied for the analysis of three-phase and multiphase systems is provided. Different methods for calculating the current sequence components, as well as for estimating the current unbalance level are presented. Furthermore, the methods are adopt-

ed, and the amplitude of low-frequency voltage ripple component is calculated on the basis of the corresponding dc-link current component. Although theoretical findings are general, the focus is set on three-, five- and seven-phase inverter configurations. A dc-link capacitor design methodology is proposed based on the low-frequency voltage ripple requirements. The numerical simulations and experimental results are included.

Chapter 6 gives the main conclusions of the thesis and discuss future perspectives.

1.4 Authored papers

- Journal Publications

  - **M. Vujacic**, M. Hammami, M. Srndovic and G. Grandi, "Analysis of dc-link voltage switching ripple in three-phase PWM inverters," *Energies*, vol. 11, Feb. 2018.
  - **M. Vujacic**, M. Hammami, M. Srndovic and G. Grandi, "Theoretical and experimental investigation of switching ripple in the dc-link voltage of single-phase H-bridge PWM inverters," *Energies*, vol.10, Aug. 2017.

- International Conference Proceedings

  - D. X. Llano, **M. Vujacic**, R. A. McMahon, "Dc voltage ripple estimation in high performance electric power-trains," *in Proc. IEEE ICIT*, Melbourne, Australia, Feb 2019.
  - **M. Vujacic**, O. Dordevic and G. Grandi, "Evaluation of dc-link voltage ripple in seven-phase PWM voltage source inverters," *in Proc. IEEE INTELEC*, Torino, Italy, Oct. 2018.
  - **M. Vujacic**, M. Hammami, O. Dordevic and G. Grandi, "Evaluation of dc-link voltage ripple in five-phase PWM voltage source inverters," *in Proc. IET PEMD*, Liverpool, U.K., Apr. 2018.
  - M. Hammami, **M. Vujacic** and G. Grandi, "Dc-link current and voltage ripple harmonics in three-phase three-level flying capacitor inverter with sinusoidal carrier-based PWM," *in Proc. IEEE ICIT*, Lyon, France, Feb. 2018.
  - **M. Vujacic**, M. Hammami, M. Srndovic and G. Grandi, "Evaluation of dc voltage ripple in three-phase PWM voltage source inverters," *in Proc. IEEE ISIE*, Edinburgh, U.K., June 2017.
  - **M. Vujacic**, M. Srndovic, M. Hammami and G. Grandi, "Evaluation of dc voltage ripple in single-phase H-bridge PWM inverters," *in Proc. IEEE IECON*, Florence, Italy, Oct. 2016.

Chapter 2

Dc-link analysis in single-phase H-bridge inverters

2.1 Introduction

Single-phase full-bridge (H-bridge) inverter is the most fundamental configuration used for DC/AC power conversion. It presents the basis for other various power topologies such as three-phase and multiphase inverters with different output voltage levels. Essentially, it is made up of two single-phase legs connected to the common dc bus. Each leg consists of two series connected switches, which are formed by the parallel combination of an insulated gate bipolar transistor (IGBT) type controlled switch and inverse conducting diode. Such a switch combination permits bidirectional current flow but requires only one polarity of voltage blocking activity. The general structure of a single-phase full-bridge (H-bridge) inverter is shown in Fig. 2.1.

The single-phase configuration is used in many low-power applications, either grid connected or stand-alone, with special emphasis on the interface of renewable energy sources in distributed generation systems, such as photovoltaic (PV) power plants. A comprehensive survey of different inverter topologies for connecting PV modules to a single-phase grid has been given by [2.1]. Different standards that inverters for PV and grid applications must fulfill have been covered too, focusing on power quality, the maximum allowable amount of injected dc current into the grid, detection of islanding operation, and system grounding. One interesting thing that has been pointed out is that the voltage ripple amplitude should not be above 8.5% of the maximum power point (MPP) in order to reach a utilization ratio of 98%.

The efficiency and power quality of the inverter operation is directly related to its modulation. For the single-phase H-bridge inverters the simplest and the most widely used control method is the high frequency sinusoidal pulse width modulation (SPWM). The two switches in each phase leg are modulated in a complementary pattern by a simple comparison between a high-frequency triangular carrier waveform and a low-frequency sinusoidal reference waveform. When the reference waveform is greater than the carrier, the phase leg should be switched to the upper (positive) side of the dc-link. In contrary, if the carrier waveform is greater than the reference waveform the phase leg should be switched to the lower (negative) side of the dc-link. The resultant phase leg output should have the reference waveform as a fundamental component. Detailed analysis of carrier-based PWM

techniques for two level and multilevel, single-phase and three-phase VSIs is given in [2.2] where the techniques are compared analytically using two-dimensional Fourier approach for signal spectrum calculation.

When SPWM is applied to single-phase inverters, employed switching frequency is usually much higher than fundamental frequency. As a result, the low order harmonics are very small and the total harmonic distortion (THD) in the line current is a function of switching frequency, with higher frequency resulting in lower THD and smaller filter requirements. On the other side, the switching losses in the inverter increase proportionally to the switching frequency. In order to achieve good compromise between the switching losses and the ripple requirements, optimal variable switching frequency scheme is proposed on the basis of the peak-to-peak and RMS values of current ripple [2.3]. The current quality of PWM based inverter is evaluated in [2.4] for a single-phase inverter with an arbitrary number of voltage levels. The analysis is carried out in time domain using current ripple normalized mean squared (NMS) criterion.

Referring to the input side of single-phase inverters, a critical characteristic seems to be the double-fundamental frequency harmonic on the dc-link. The conventional way to deal with the input current ripple, and in general to maintain the dc-link stability in single-phase inverters, is to connect a considerably large capacitor (usually aluminum electrolytic) to the dc-link. Consequently, it leads to a massive converter volume and low power density. In order to avoid the use of a large capacitor, the minimum energy and capacitance requirements for the dc-link capacitor are discussed in [2.5]. A comprehensive dc-link voltage control strategy for minimizing the dc-link capacitance in single-phase grid-connected photovoltaic inverters has been proposed in [2.6]. The development is based on the analysis of a double fundamental frequency voltage ripple across the dc-link. Another control technique aiming to reduce the power oscillation and, consequently, the dc-link capacitor size in a single-phase full-bridge converter has been proposed in [2.7]. However, the technique is suitable for applications with the same input and output converter frequency. Analysis of the dc-link capacitor current harmonics in single-phase H-bridge inverters is given in [2.8], where the individual harmonics of the dc-link current with sinusoidal and overlaid harmonic output currents are calculated based on the double Fourier analysis. Investigations of voltage and current ripples in the dc supply voltage of PV arrays, considering only double-fundamental frequency, are presented in [2.9]. The dc-link switching harmonic current RMS equations have been derived in [2.10] under arbitrary low-order harmonics in the AC current.

In this chapter, the dc-link voltage ripple is analyzed in terms of the peak-to-peak value. Namely, the peak-to-peak voltage ripple envelope has been calculated considering both voltage ripple components: low (double-fundamental) frequency and high (switching) frequency. The voltage ripple components are analytically calculated based on the corresponding dc-link current components and by considering the total dc-link impedance.

Peak-to-peak value is defined as the difference between the maximum and the minimum value of the voltage ripple within the considered period. Based on voltage ripple requirements simple guidelines when designing the dc-link capacitor have been presented. Numerical simulations and experimental results are included to verify the analytical analysis. Finally, the results are briefly discussed in the last section of the chapter.

Original contribution of this chapter has been presented, and the content of the following sections has been used, in one conference [2.11] and one journal paper [2.12].

2.2 Dc-link current analysis

2.2.1 General assumptions

The general configuration of a single-phase full-bridge (H-bridge) inverter is shown in Fig. 2.1. The inverter is connected to a constant dc voltage supply (V_{dc}). The equivalent series dc source impedance is modelled by Z_{dc}, representing an input filter (such as a dc reactor) or a resistive dc supply (such as a PV system). The dc-link capacitor C is required to maintain the dc-link voltage and to handle current and voltage ripple. The power semiconductor switches are assumed to be ideal in order to simplify theoretical analysis. The load is represented by a passive R_L-L_L load or, if the inverter is connected to the electrical grid, by a sinusoidal grid voltage v_g. In case of the grid connection R_L and L_L would present a liking inductance with its inner resistance.

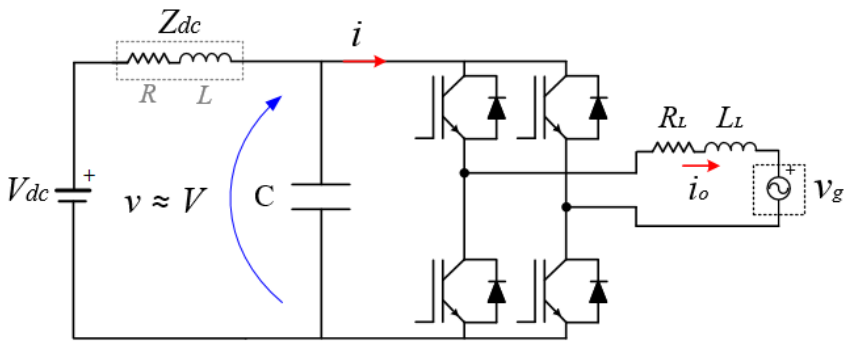


Fig. 2.1: A single-phase full-bridge (H-bridge) inverter.

Considering the linear region of modulation and neglecting the dc-link voltage oscillations compared to its average value ($v \approx V$), the desired inverter output voltage, averaged over the switching period T_{sw}, is sinusoidal and defined as:

$$v_0^* = m V \sin(\vartheta), \tag{2.1}$$

where $\vartheta = \omega t$, $\omega = 2\pi/T$ is the fundamental angular frequency and T is the fundamental period. Modulation index m is defined as the ratio of the fundamental output phase voltage magnitude and the dc supply voltage. When the switching frequency is much higher than the fundamental frequency, the reference signal is considered constant over one switching period. The output voltage and its fundamental component (averaged value) are shown in Fig. 2.2.

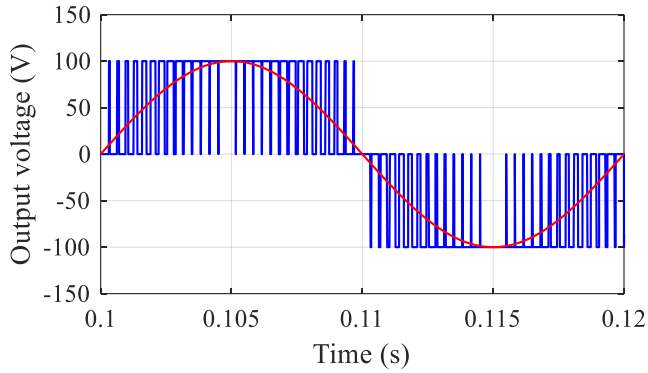


Fig. 2.2: Ideal PWM inverter output voltage (instantaneous component, blue trace) and its averaged counterpart (fundamental component, red trace) in case of V_{dc} = 100 V and m = 1.

Considering sinusoidal output voltage (2.1) and neglecting the switching ripple, the inverter output current is expressed as a sinusoid as well:

$$i_0 = I_0 \sin(\vartheta - \varphi), \tag{2.2}$$

where I_0 is the output current amplitude, and φ is the power phase angle.

2.2.2 Dc-link current components

The instantaneous dc-link current $i(t)$, shown in Fig. 2.3, is composed of three components: dc (average) component $I = I_{dc}$, low-frequency (double-fundamental frequency, i.e. 100Hz) component $\tilde{i}(t)$ and switching frequency component $\Delta i(t)$. Therefore, the dc-link current is expressed as:

$$i(t) = I_{dc} + \tilde{i}(t) + \Delta i(t). \tag{2.3}$$

The dc-link current averaged over the switching period T_{sw} represents the low-frequency input current harmonics and can be expressed as:

$$\bar{i} = I_{dc} + \tilde{i}. \tag{2.4}$$

Under the assumption of ideal circuit conditions such as constant dc-link voltage equal to *V*, and lossless switches, the input/output power balance can be written as:

$$V\,\bar{i} = v_0\,i_0\,. \tag{2.5}$$

Introducing (2.1) and (2.2) in (2.5), the averaged dc-link current is calculated as:

$$\bar{i} = m\,I_0 \sin\vartheta \sin(\vartheta-\varphi) = \frac{m\,I_0}{2}\left[\cos\varphi - \cos\left(2\vartheta-\varphi\right)\right]. \tag{2.6}$$

The average and the low-frequency (double-fundamental frequency) dc-link current components, can be simply expressed and readily obtained by (2.4) and (2.6) as:

$$I_{dc} = \frac{m\,I_0}{2}\cos\varphi\,, \tag{2.7}$$

$$\tilde{i} = -\frac{1}{2}m\,I_0\cos(2\vartheta-\varphi)\,. \tag{2.8}$$

Further, the amplitude of the low-frequency dc-link current component can be expressed as:

$$\tilde{I}_{pk} = \frac{1}{2}m\,I_0\ . \tag{2.9}$$

According to the expressions for the dc-link current and its components given by (2.3), (2.4) and (2.6), the switching frequency current component can be calculated as:

$$\Delta i = i - \bar{i} = I_0\sin(\vartheta-\varphi)\,(1-m\sin\vartheta)\,. \tag{2.10}$$

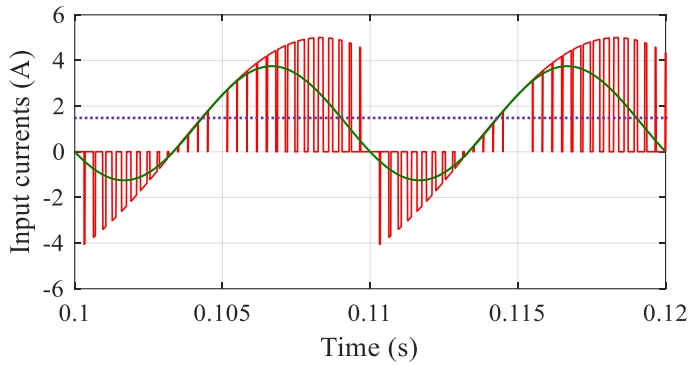


Fig. 2.3: Dc-link inverter current (red trace), its averaged counterpart (green trace), and average component (dashed line) in case of m = 1, I_0 = 5 A and φ = 60°.

2.3. Dc-link voltage ripple analysis

Similarly to the inverter dc-link current, the instantaneous dc-link voltage can be expressed by three relevant components: dc (average) component *V*, low-frequency (double-fundamental) component $\tilde{v}$ and switching frequency component Δv:

$$v(t) = V + \tilde{v}(t) + \Delta v(t) \,. \tag{2.11}$$

Each voltage component can be calculated on the basis of the corresponding current component and by considering the dc-link equivalent impedance calculated at the relevant frequency component, as it will be shown in the following.

2.3.1 Low-frequency voltage component

The average component *V* is calculated by subtracting the voltage drop on the series dc source resistance *R* from the dc supply voltage V_{dc} as:

$$V = V_{dc} - R\, I_{dc} \,. \tag{2.12}$$

The low-frequency dc-link voltage component $\tilde{v}$ can be calculated on the basis of the corresponding input current component, given by (2.8), and the dc-link equivalent impedance Z_{2f}, as follows:

$$\tilde{v} = Z_{2f}\, \frac{m\, I_0}{2}\, \cos\left(2\vartheta - \varphi + \varphi_z\right). \tag{2.13}$$

Subscript 2*f* stands to highlight that the frequency at which the impedance is calculated is double-fundamental (i.e. 100 Hz). Being Z_{2f} the parallel between the dc source impedance Z_{dc} and the reactance of the dc-link capacitor, following equations are obtained for the magnitude and the phase angle of the dc-link equivalent impedance:

$$\mathrm{Z}_{2f} = \frac{1}{2\omega C} \sqrt{\frac{R^2 + (2\omega L)^2}{R^2 + \left(2\omega L - \dfrac{1}{2\omega C}\right)^2}}\,, \tag{2.14}$$

$$\varphi_z = \mathrm{arctg}\left[\frac{2\omega L}{R}\left(1 - 4\omega^2 L\, C - \frac{R^2 C}{L}\right)\right]. \tag{2.15}$$

Finally, the amplitude or the peak value of the low-frequency voltage ripple component is given by:

$$\tilde{V}_{pk} = Z_{2f}\, \tilde{I}_{pk} \quad . \tag{2.16}$$

2.3.2 Switching frequency voltage component

Instantaneous dc-link current (red trace) and voltage ripple (blue trace) are depicted in Fig. 2.4 over the switching period T_{sw}. Considering sinusoidal PWM, the "on-time" interval t_{on} can be calculated as:

$$t_{on} = m \sin \vartheta \, T_{sw} \,. \tag{2.17}$$

Being the switching frequency much higher than the double-fundamental frequency, the variation of the low-frequency dc-link voltage component within the switching period T_{sw} can be neglected. The peak-to-peak amplitude of the switching frequency dc-link voltage component Δv_{pp} can be defined as the difference between its maximum and minimum value within the switching period:

$$\Delta v_{pp} = \max\left\{\Delta v(t)\right\}_{T_{sw}} - \min\left\{\Delta v(t)\right\}_{T_{sw}} \,. \tag{2.18}$$

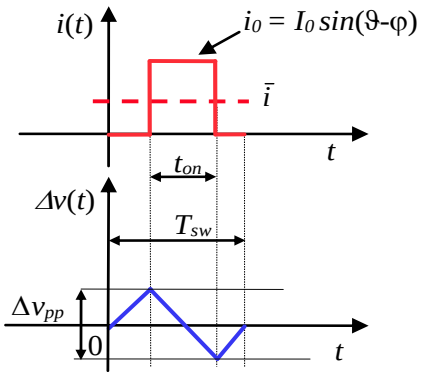


Fig. 2.4: Dc-link current and voltage ripple in one switching period T_{sw}.

In order to obtain the peak-to-peak voltage switching ripple Δv_{pp}, the dc-link switching frequency current component Δi has to be determined first. For determining the switching ripple components, an equivalent circuit of the dc-link inverter side is introduced in Fig. 2.5, with the reactances referred to the switching frequency ($\omega_{sw} = 2\pi f_{sw}$).

One can see that the equivalent dc source impedance, $Z_{dc}(\omega_{sw})$, and the reactance of the dc-link capacitor C, $1/(\omega_{sw}C)$, are connected in parallel. Assuming that the capacitor reactance is much smaller than the equivalent dc source impedance (calculated at the switching frequency), the whole switching frequency current ripple component (Δi) circulates only through the dc-link capacitor. In this case, only the capacitance value is determining the amplitude of the voltage switching ripple. Note that this assumption is generally considered for the analysis of the dc voltage switching ripple component in this thesis. As a consequence, the dc-link equivalent impedance becomes:

$$Z_{\omega_{sw}} = \frac{1}{\omega_{sw} C} \sqrt{\frac{R^2 + (\omega_{sw} L)^2}{R^2 + \left(\omega_{sw} L - \frac{1}{\omega_{sw} C} \right)^2}} \cong \frac{1}{\omega_{sw} C} \ . \tag{2.19}$$

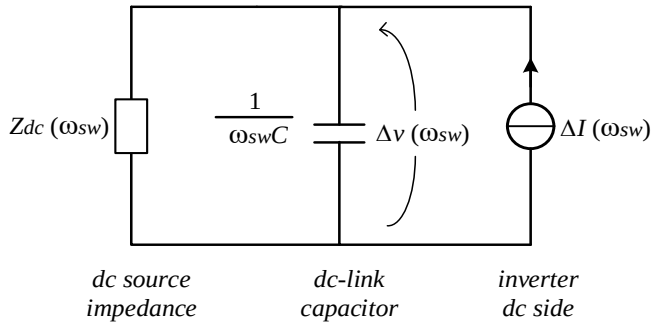


Fig. 2.5: Equivalent circuit of the inverter dc-bus for switching frequency components.

Introducing the "on-time" interval t_{on} calculated in (2.17), the corresponding peak-to-peak switching voltage ripple over the interval (0–t_{on}) is given by:

$$\Delta v_{pp} = \frac{1}{C} \int_0^{t_{on}} \Delta i \, dt \ . \tag{2.20}$$

The peak-to-peak dc-link voltage switching ripple amplitude can be calculated utilizing the switching frequency current component (2.10), the "on-time" interval t_{on} (2.17), and (2.20). Finally, it is expressed as:

$$\Delta v_{pp} = \frac{I_0 T_{sw}}{C} \, m \left| \sin \vartheta \sin(\vartheta - \varphi)(1 - m \sin \vartheta) \right| . \tag{2.21}$$

The normalization of Δv_{pp} can be introduced as follows:

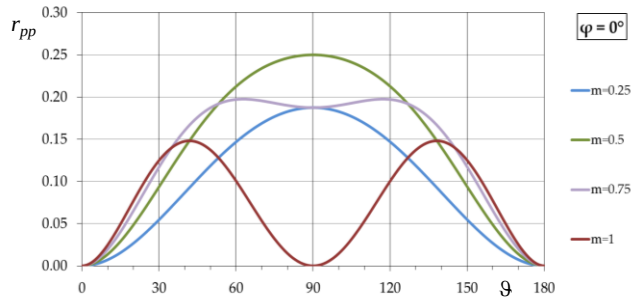
$$\Delta v_{pp} = \frac{I_0 T_{sw}}{C} \, r_{pp}(m, \vartheta, \varphi) , \tag{2.22}$$

leading to the simplified expression of the normalized peak-to-peak voltage switching ripple amplitude $r_{pp}(m,\vartheta,\varphi)$:

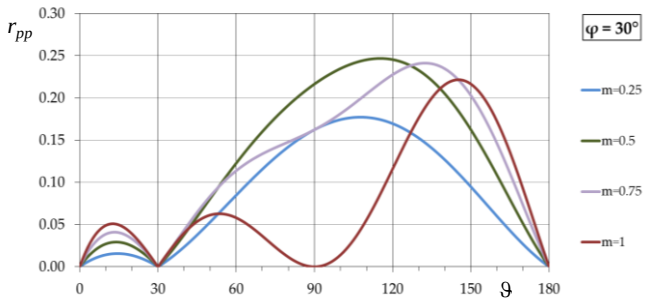
$$r_{pp}(m, \vartheta, \varphi) = \left| m \sin \vartheta \sin(\vartheta - \varphi)(1 - m \sin \vartheta) \right| . \tag{2.23}$$

In order to predict the behavior of the dc voltage switching ripple, the distribution of the normalized peak-to-peak voltage switching ripple amplitude r_{pp} is shown in Fig. 2.6.

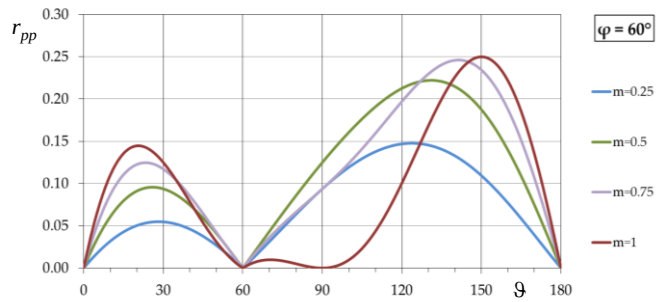
(**a**)



(**b**)



(**c**)



(**d**)

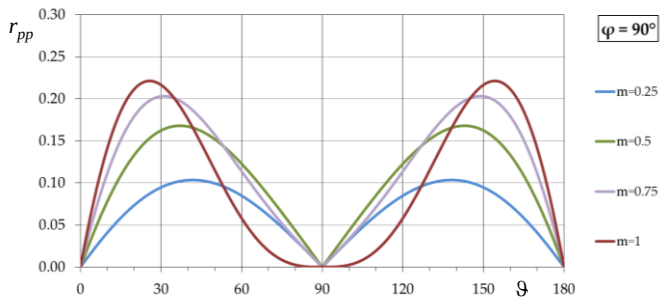


Fig. 2.6: Normalized peak-to-peak dc-link voltage ripple amplitude $r_{pp}(\vartheta)$ over the half-fundamental period [0, 180°] for different modulation indices, m = 0.25, 0.5, 0.75 and 1, and power phase angle φ = 0° (**a**), 30° (**b**), 60° (**c**) and 90° (**d**).

Dc voltage switching ripple component is calculated by (2.23) and shown over the half-fundamental period i.e., ϑ = [0, 180°]. In order to cover full range of operational con-

ditions, four values of modulation index have been selected m = 0.25, 0.5, 0.75 and 1, and four power phase angles have been considered, φ = 0, 30°, 60°, and 90°.

It can be seen in Fig. 2.6 that the amplitude of the normalized peak-to-peak voltage switching ripple $r_{pp}(\vartheta)$ ranges between 0 (minimum) and 0.25 (maximum). In each of four considered cases of power phase angle, the $r_{pp}(\vartheta)$ minimum and $r_{pp}(\vartheta)$ maximum appear at different angles ϑ for different values of modulation index m over the half-fundamental period. For two phase angles φ = 0° and φ = 90°, voltage ripple distributions are symmetrical with regard to the middle of the considered half-fundamental period. For other values of phase angle, no symmetry in the voltage ripple distributions is noticed. The maximum of the peak-to-peak voltage switching ripple amplitude changes with different operational conditions what will be examined in the following analysis.

In the case of a unity output power factor (φ = 0°), which corresponds to most of the grid-connected applications, the maximum of the normalized peak-to-peak voltage switching ripple amplitude is obtained from (2.23) as:

$$r_{pp}^{\max}(m,\varphi=0°)=\begin{cases} m\,(1-m) & \text{for } 0\le m\le\dfrac{2}{3} \\ \dfrac{4}{27}\dfrac{1}{m} & \text{for } \dfrac{2}{3}\le m\le 1 \end{cases}. \tag{2.24}$$

Fig. 2.7 shows the maximum of the normalized peak-to-peak voltage ripple amplitude $r_{pp}^{\max}$ over the whole modulation index range, for φ = 0°, 30°, 60°, and 90°. In the case of φ = 0°, $r_{pp}^{\max}$ is analytically determined by (2.24) (blue trace), while for the other three cases it is obtained numerically.

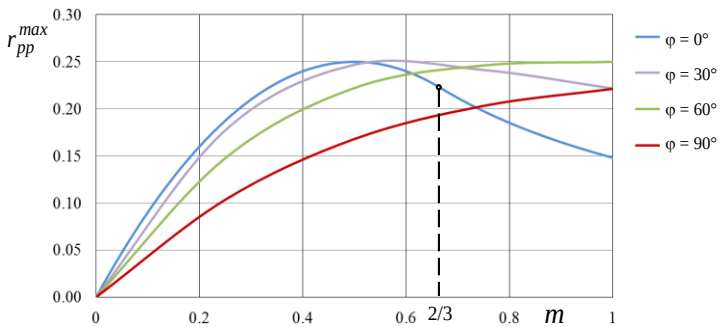


Fig. 2.7: Maximum of normalized peak-to-peak voltage switching ripple amplitude for different power phase angles φ = 0°, 30°, 60° and 90°.

It can be noticed that for the modulation index range (0÷0.5) the maximum of voltage switching ripple amplitude increases with increasing modulation index. The behavior is the same for all considered power phase angles. However, for the higher values of

modulation index, the maximum changes variously for different phase angles. Namely, in case of lower phase angles the maximum decreases with increasing the modulation index value and increases for the higher values of phase angle. However, the global maximum is always in 0.25 except for φ = 90° when it is in 0.22.

Since the instantaneous dc-link voltage switching ripple $\Delta v(t)$ is a symmetric triangular waveform with the amplitude corresponding to the half of the peak-to-peak ripple envelope ($\Delta v_{pp}/2$), the root mean square (RMS) value of the triangular signal ΔV_{rms} can be easily determined by dividing its peak value by √3. In the case of variable amplitude, the RMS over a (half) fundamental period can be calculated as:

$$\Delta V_{rms} = \sqrt{\frac{1}{\pi}\int_0^{\pi} \Delta v^2 \, d\vartheta} = \frac{1}{\sqrt{3}} \sqrt{\frac{1}{\pi}\int_0^{\pi} \left(\frac{1}{2}\Delta v_{pp}\right)^2 d\vartheta} \,. \tag{2.25}$$

Introducing (2.21) into (2.25), yields:

$$\Delta V_{rms} = \frac{I_0 T_{sw}}{C} \frac{m}{4\sqrt{3}} \sqrt{\left(\frac{m^2}{2} - \frac{16}{5\pi} m + \frac{1}{2}\right)\cos(2\varphi) + \left(\frac{3}{4} m^2 - \frac{16}{3\pi} m + 1\right)} \,. \tag{2.26}$$

After normalization of (2.26) as in (2.22), one has for the normalized dc-link voltage switching ripple RMS:

$$r_{rms}(m,\varphi) = \frac{m}{4\sqrt{3}} \sqrt{\left(\frac{m^2}{2} - \frac{16}{5\pi} m + \frac{1}{2}\right)\cos(2\varphi) + \left(\frac{3}{4} m^2 - \frac{16}{3\pi} m + 1\right)} \,. \tag{2.27}$$

Fig. 2.8 shows the normalized dc-link voltage switching ripple RMS given by (2.27) as a function of the modulation index *m* for different power phase angles φ. It can be noted that there is one value of the modulation index when r_{rms} becomes completely independent on the power phase angle φ, and it depends only on *m*. By exploiting (2.27), this specific value of *m* corresponds to the following condition:

$$\frac{m^2}{2} - \frac{16}{5\pi} m + \frac{1}{2} = 0 \,. \tag{2.28}$$

Solving (2.28) results to:

$$m = \frac{16 - \sqrt{256 - 25\pi^2}}{5\pi} = 0.825 \,. \tag{2.29}$$

Introducing (2.29) into (2.27), the corresponding normalized dc-link voltage switching ripple RMS is: r_{rms} (m = 0.825) ≅ 0.04, according to the diagram in Fig. 2.8.

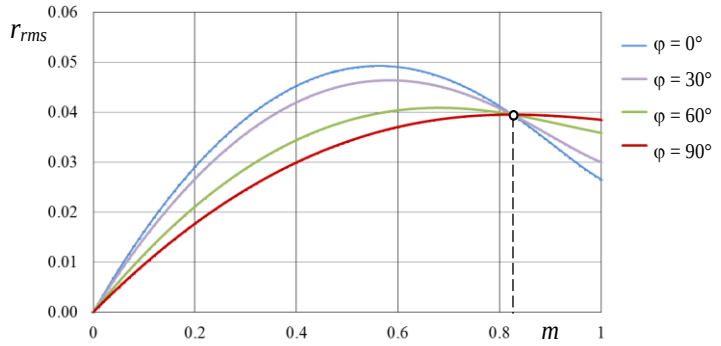


Fig. 2.8: RMS of normalized voltage switching ripple as a function of modulation index for φ = 0°, 30°, 60° and 90°.

2.4 Dc-link capacitor design

In this section, simple and effective guidelines when selecting the dc-link capacitor in single-phase H-bridge inverters are proposed. The capacitance can be calculated taking into account requirements or restrictions on the switching frequency or the double- fundamental frequency voltage ripple component. A brief discussion on the results and some practical considerations of presented calculations follow the analysis.

As discussed earlier, concerning the dc-link voltage ripple at the switching frequency in the order of kHz, the capacitive reactance ($1/\omega_{sw}C$) is certainly much lower than the dc source impedance Z_{fsw} (calculated at the switching frequency). Hence, the amplitude of the voltage switching ripple is determined only by the size of the dc-link capacitor.

Following the analytical developments presented in the previous sections, the selection of the dc-link capacitor can be performed on the basis of one of the following constraints: based on the maximum amplitude of the peak-to-peak voltage switching ripple; or based on the RMS of the voltage switching ripple ΔV_{rms}. Of course, in both cases the worst scenario should be considered for final choice of the capacitor. As the worst scenario, the global maximum in the Figs. 2.7 and 2.8 is logically taken.

According to Fig. 2.7, the maximum amplitude of the normalized peak-to-peak ripple is 0.25 and therefore the global maximum peak-to-peak voltage switching ripple can be expressed as:

$$r_{pp}^{\max} \approx \frac{1}{4} \quad \rightarrow \quad \Delta v_{pp}^{\max} \cong \frac{1}{4}\frac{I_0}{f_{sw}C} \ . \tag{2.30}$$

On the basis of (2.30) and by considering the maximum output current I_0, the dc-link capacitance can be readily calculated as a function of the required peak-to-peak voltage switching ripple amplitude Δv_{pp}^{*}:

$$C \geq \frac{1}{4}\frac{I_0}{f_{sw}\Delta v^*_{pp}} \ . \tag{2.31}$$

If, however, the focus is on the voltage switching ripple RMS rather than on the peak-to-peak voltage switching ripple amplitude, a reasonable approximation of ΔV_{rms} for the whole range of the modulation index and power phase angle corresponds to the condition given by (2.29), i.e. the operating point emphasized in Fig. 2.8. Hence, the dc-link voltage switching ripple RMS can be simplified as:

$$r_{rms} \approx 0.04 = \frac{1}{25} \quad \rightarrow \quad \Delta V_{rms} \cong \frac{1}{25}\frac{I_0}{f_{sw}C} \ . \tag{2.32}$$

Therefore, given as conditions the RMS of the switching ripple and the maximum output current I_0 (2.32), the dc-link capacitor can be sized basing on:

$$C \geq \frac{1}{25}\frac{I_0}{f_{sw}\Delta v_{rms}} \ . \tag{2.33}$$

Unlike the switching ripple voltage component, if the low-frequency dc-link voltage ripple is concerned, i.e., the double fundamental frequency, its amplitude generally depends not only on the capacitance C, but also on the parameters of the dc source impedance Z_{dc}. According to (2.9), (2.14) and (2.16), the dc-link low-frequency voltage ripple amplitude is calculated as:

$$\tilde{V}_{pk} = \frac{m\, I_0}{2}\frac{1}{2\omega C}\sqrt{\frac{R^2 + (2\omega\, L)^2}{R^2 + \left(2\omega L - \frac{1}{2\omega C}\right)^2}} \ . \tag{2.34}$$

The expression given by (2.34) could be adopted to design the dc-link capacitance. However, it is a rather cumbersome calculation. A reasonable simplification can be introduced if one of the following assumptions for inductively or resistively dc source can be made:

$$\begin{cases} 2\omega L >> \dfrac{1}{2\omega C} & \textit{inductively dominant dc–link} \ ; \\ R >> \dfrac{1}{2\omega C},\ 2\omega L & \textit{resistively dominant dc–link} \ . \end{cases} \tag{2.35}$$

Assuming that one of two conditions in (2.35) is satisfied, i.e., a photovoltaic dc supply having a high equivalent series resistance R (around the MPP is $R_{PV} = V_{mpp}/I_{mpp}$), or

a dc-link inductive filter having a high series reactance $2\omega L$, the double-fundamental frequency dc-link voltage ripple can be calculated by simplifying (2.34) as:

$$\tilde{V}_{pk} \cong \frac{m\, I_0}{2} \frac{1}{2\omega C} \ . \tag{2.36}$$

Finally, given the amplitude of the double-fundamental dc voltage ripple component $\widetilde{V}$ and the maximum output current I_0 as the conditions, the dc-link capacitor can be sized by reversing (2.36):

$$C \geq \frac{m\, I_0}{2} \frac{1}{2\omega \tilde{V}_{pk}} . \tag{2.37}$$

In order to illustrate the proposed dc-link capacitor design/selection process, a simple flowchart is introduced in Fig. 2.9.

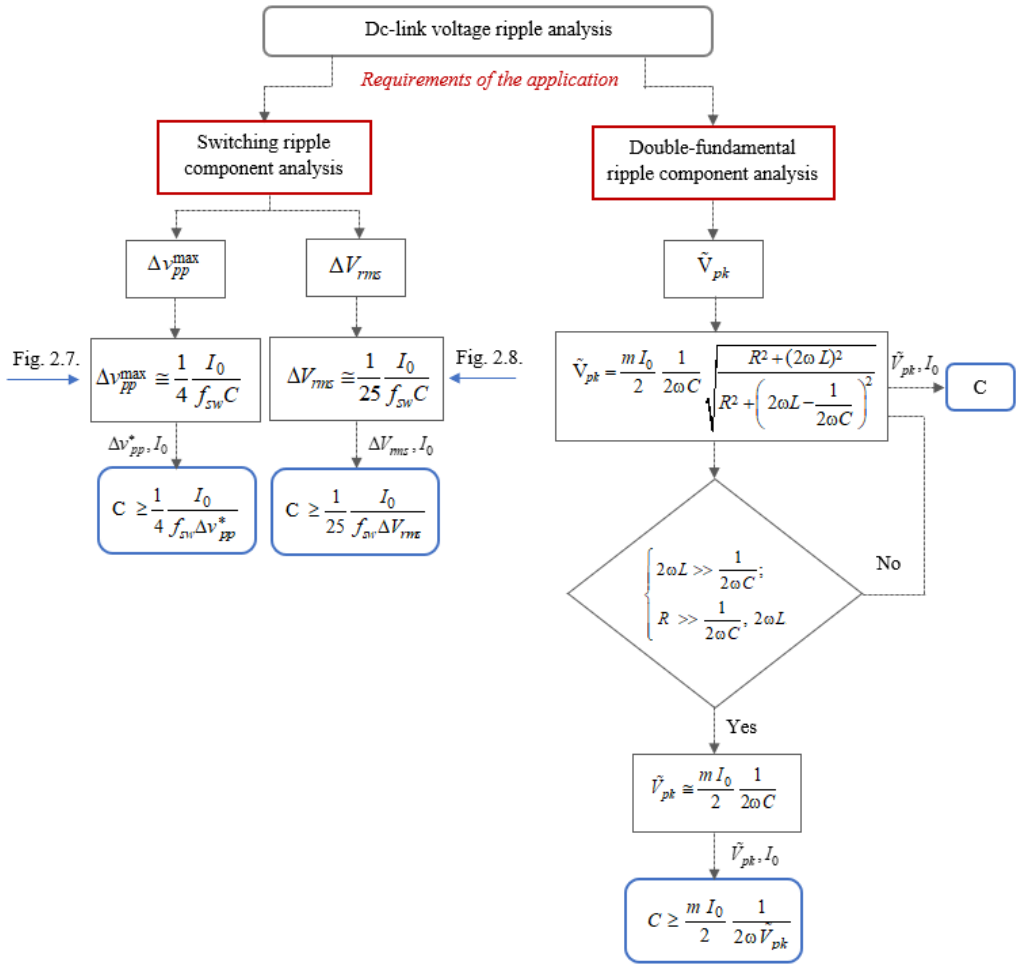


Fig. 2.9: A flow-chart of the proposed capacitor design/selection process.

The previous analysis shows that the dc-link capacitor sizing based on switching or low-frequency voltage ripple component results in different values of capacitance. Therefore, a brief discussion on the reasons for taking into account restrictions referred to one or the other voltage ripple component follows.

Namely, if comparable voltage ripple amplitude restrictions are set, the design of the dc-link capacitor C based on the double-fundamental frequency voltage ripple component (2.37) results in higher value comparing to the value obtained by considering only the switching frequency voltage ripple component ((2.31) or (2.33)). On the other hand, considering the same dc-link capacitor as in the real circuit, the ratio between the two ripple amplitudes is practically given by the inverse ratio between the corresponding frequencies, which could be in the range 20–200, making the voltage switching ripple obviously much smaller than the voltage double-fundamental ripple.

However, the voltage switching ripple amplitude could have additional specific restrictions to limit switching noise, electromagnetic interferences and voltage stress on the dc bus components. In this case, the capacitor could be oversized considering (2.31) or (2.33) instead of (2.37). Moreover, there are specific cases in which the voltage switching ripple amplitude exceeds the double-fundamental ripple amplitude. In particular, this situation could occur in the case of small dc source impedance at the double-fundamental frequency, when condition (2.35) would not be satisfied. This is the case of an almost ideal dc source when the double-fundamental frequency ripple practically disappears, and the voltage switching ripple can be evaluated by (2.31) or (2.33).

Finally, if the amplitudes of the two voltage ripple components are comparable and the restriction is set on the maximum amplitude of the total dc-link voltage ripple, both ripple components should be taken into consideration for the final dc-link capacitor sizing. In this case, sum of the maximum of the two voltage ripple amplitudes could be taken into account as the worst case scenario.

2.5 Simulation and experimental results

In this section, selected simulation and experimental results for the single-phase H-bridge inverter are given. The confirmation of the analytical developments, as well as the comparison of simulations and experiments have been shown and commented.

The circuit simulations have been carried out by MATLAB/Simulink. The inverter was controlled by the sinusoidal PWM with the switching frequency f_{sw} set to 2.5 kHz. Only linear PWM region is analyzed and the maximum modulation index is 1. The parameters in simulations are set in the mind to match the corresponding values used in experiments.

The input terminals of inverter are connected to external dc source and dc supply voltage is set to V_{dc} =96V. The dc source impedance is modelled using the following parameters: dc source resistance R=5.5Ω and dc source inductance L=19mH. The dc-link ca-

pacitor is connected in parallel to the dc source having a capacitance C =1.1mF. Two different kinds of load are considered in order to obtain two different power phase angles φ = 0° and φ = 60°. In Fig. 2.10 the electrical circuit scheme of the load is presented. The corresponding load parameters are determined by the LCR meter Agilent 4263B. In case of power phase angle φ = 60°, passive *R-L* load is used having the following parameters: R_L=13.9Ω and L_L=76.5mH. In order to simulate grid-connected application and obtain the power phase angle φ = 0°, in series to *R-L* load with the following parameters R_L=4.7 Ω and L_L=43.3 mH, resistor R_0=29.7 Ω and a parallel capacitor C_0=43.3 μF are added. Using these parameters, the output current ripple is small and can be neglected, and the analysis presented in previous sections can be applied.

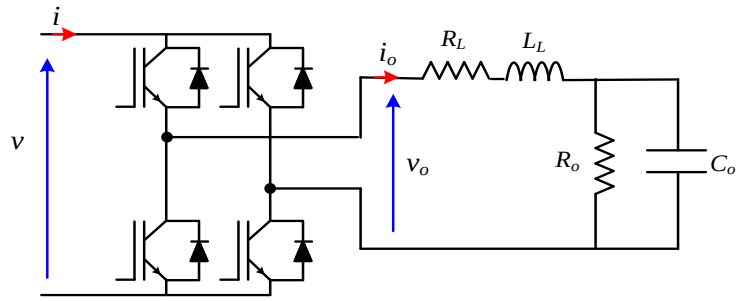


Fig. 2.10: Load configuration for the experimental setup

In Figs. 2.11 and 2.12, the instantaneous dc-link voltage switching ripple $\Delta v(t)$ (blue trace) is compared with the half peak-to-peak voltage switching ripple envelope $\pm\Delta v_{pp}/2$ calculated by (2.21) (red traces), over one fundamental period (T = 20ms). Two different power phase angles φ = 0° (Fig. 2.11) and φ = 60° (Fig. 2.12) are considered, and the four sub-cases (a)-(d) correspond to different modulation indexes m: 0.25, 0.5, 0.75, and 1. The switching ripple $\Delta v(t)$ have been numerically obtained by properly high-pass filtering the instantaneous dc-link voltage, according to (2.11).

It is possible to observe a good agreement between the analytically calculated dc-link voltage switching ripple envelopes and the simulated dc voltage ripple shown in Figs. 2.11 and 2.12, in terms of the absolute amplitude as well as the dc-link voltage ripple profile. Moreover, behavior of the maximum peak-to-peak voltage switching ripple amplitude shown in Fig. 2.7 has been confirmed for two power phase angles φ = 0° and φ = 60° by the results given in Figs. 2.11 and 2.12, respectively. It can be noted that in case of φ = 60° increasing the modulation index also the maximum of the switching ripple amplitude increases, more noticeable for lower values of modulation index and less noticeable for the higher modulation index values. On contrary, in case of φ = 0° the global maximum of the voltage switching ripple amplitude is achieved around m = 0.5 and it decreases when modulation index further increases.

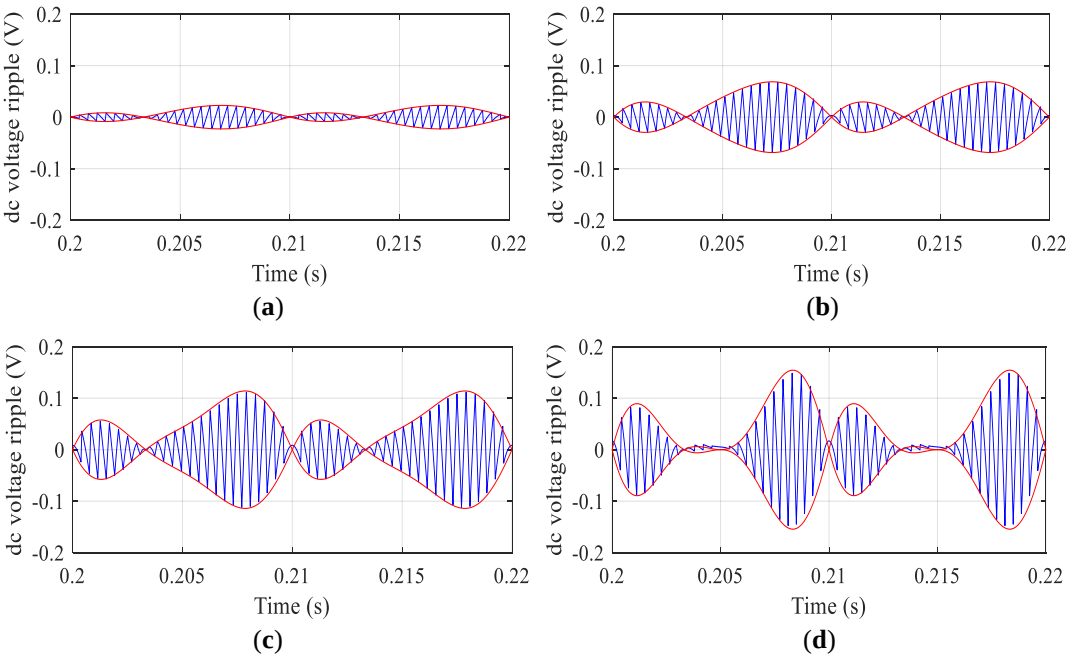


Fig. 2.11: Dc-link voltage switching ripple: simulation results (blue trace) and calculated peak-to-peak envelope (red trace) over a fundamental period for φ = 60°,
(**a**) *m* = 0.25, (**b**) *m* = 0.5, (**c**) *m* = 0.75, and (**d**) *m* = 1.

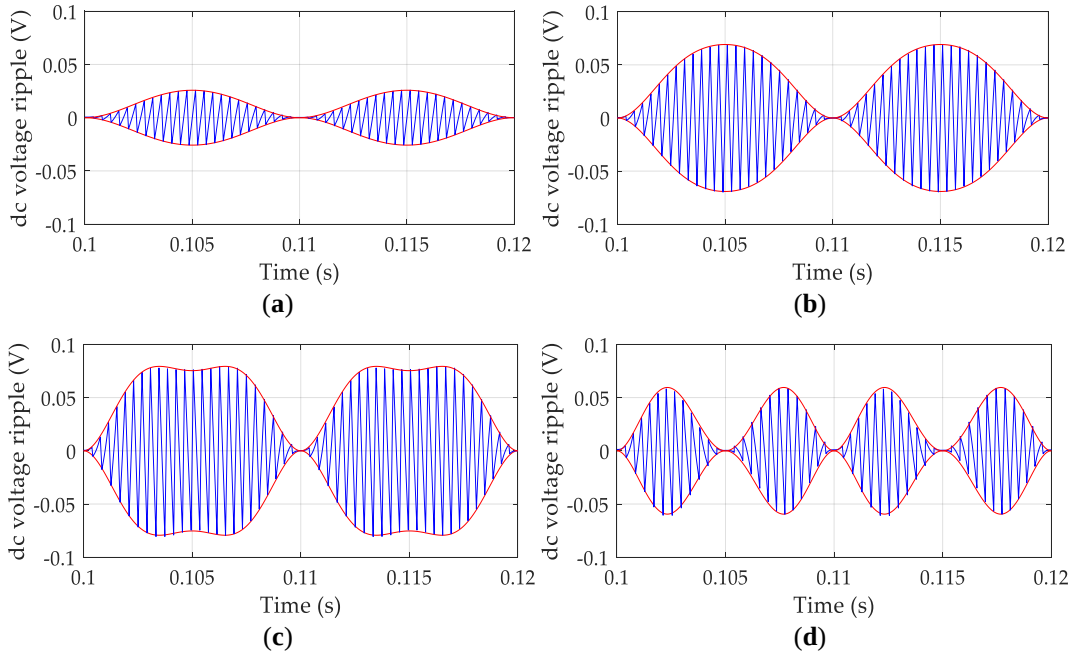


Fig. 2.12: Dc-link voltage switching ripple: simulation results (blue trace) and calculated peak-to-peak envelope (red trace) over a fundamental period for φ = 0°,
(**a**) *m* = 0.25, (**b**) *m* = 0.5, (**c**) *m* = 0.75, and (**d**) *m* = 1.

Fig. 2.13 shows the total instantaneous dc-link voltage ripple $\tilde{v}(t)+\Delta v(t)$ (double-fundamental and switching frequency ripple, blue trace) and its envelopes (red traces), calculated on the basis of (2.13) and (2.21) as

$$\tilde{v} \pm \frac{1}{2}\Delta v_{pp} = \frac{mI_0}{2}\left[Z_{2f} \cos\left(2\vartheta - \varphi + \varphi_z\right) \pm 2\pi X_{f_{sw}} \sin\vartheta \sin(\vartheta-\varphi)(1-m\sin\vartheta) \right], \qquad (2.38)$$

where Z_{2f} is the parallel between the equivalent dc source impedance (Z_{dc}) and the reactance of the dc-link capacitor calculated at double-fundamental frequency (i.e. 100Hz) and X_{fsw} is the dc-link capacitive reactance calculated at the switching frequency.

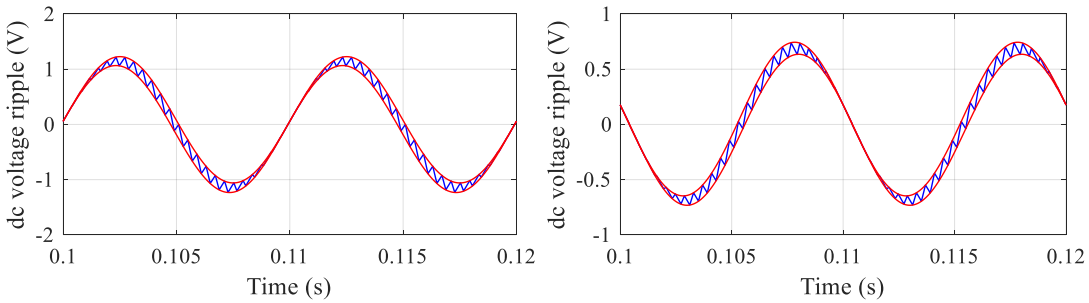


Fig. 2.13: Total dc voltage ripple: simulation results (blue trace) and calculated peak-to-peak envelopes (red traces) over a fundamental period for m = 0.5, (**a**) φ = 0°, (**b**) φ = 60°.

Fig. 2.13 confirms the good agreement between the theoretical dc-link voltage ripple developments and numerically simulated total dc-link voltage ripple. It can be concluded that the effectiveness of the proposed analytical developments is proved by means of simulation results shown in Figs. 2.11-2.13.

In order to prove both, theoretical developments and numerical results, experimental verifications have been carried out. Experimental setup is illustrated in Fig. 2.14. It consists of a custom-made three-phase inverter with Mitsubishi power IGBT module IPM PS22A76 (1200 V, 25 A), where only two legs are connected on the PCB board and the third one is properly grounded. The inverter was controlled by an "Arduino DUE" microcontroller board (84 MHz Atmel, SAM3X83 Cortex-M3 CPU). Communication between microcontroller board and inverter is established through an optical interface board. Experimental results are shown by Yokogawa DLM 2024 oscilloscope. For the voltage and current measurements, the PICO TA057 differential voltage probe (25 MHz, ±1400 V, ±2%) and LEM PR30 current probe (DC to 20 kHz, ±20 A, ±1%) were used. Additionally, an air-core inductor (*R-L*) is adopted representing a dc source impedance connected in series with the external TDK-Lambda Genesys™ 2U 3.3kW DC source.

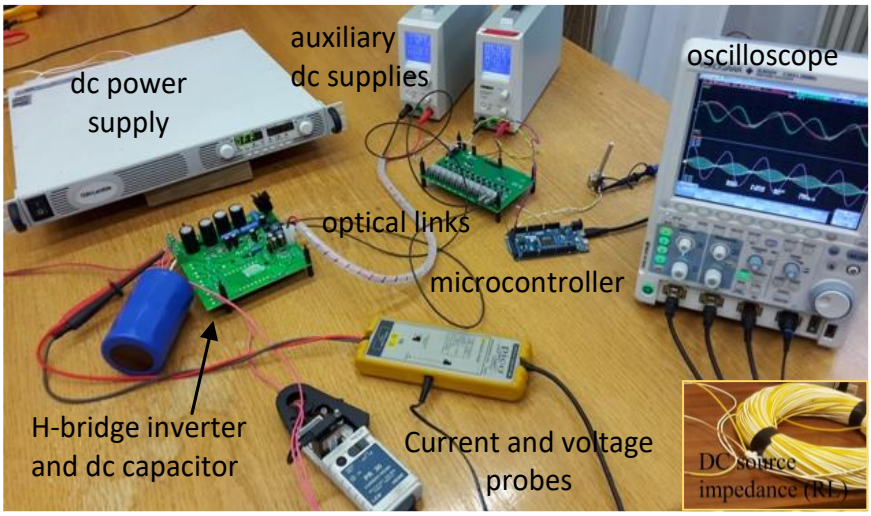


Fig. 2.14: Experimental setup

The first set of measured variables is shown in Fig. 2.15. The load voltage and current and the total dc-link voltage ripple are presented for the case $m = 0.75$ and $\varphi = 0°$, over five fundamental periods ($5T$ = 100 ms). The load voltage and current are presented in the top part of the oscilloscope screenshot, the dc-link voltage is shown in the middle part and one zoomed part of the dc-link voltage emphasizing the presence of 100 Hz and switching ripple components is presented in the bottom part. The zoomed part of the dc bus voltage is marked with the rectangle in the middle part of the screenshot, showing five periods of the 100 Hz components.

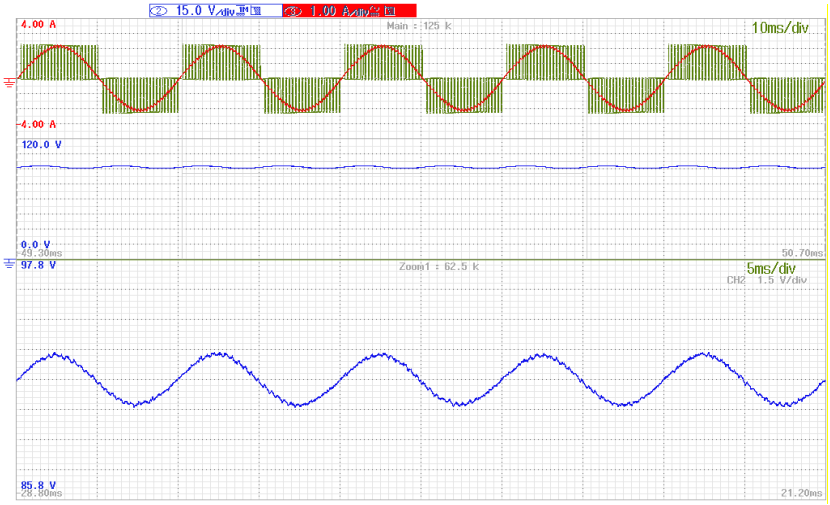
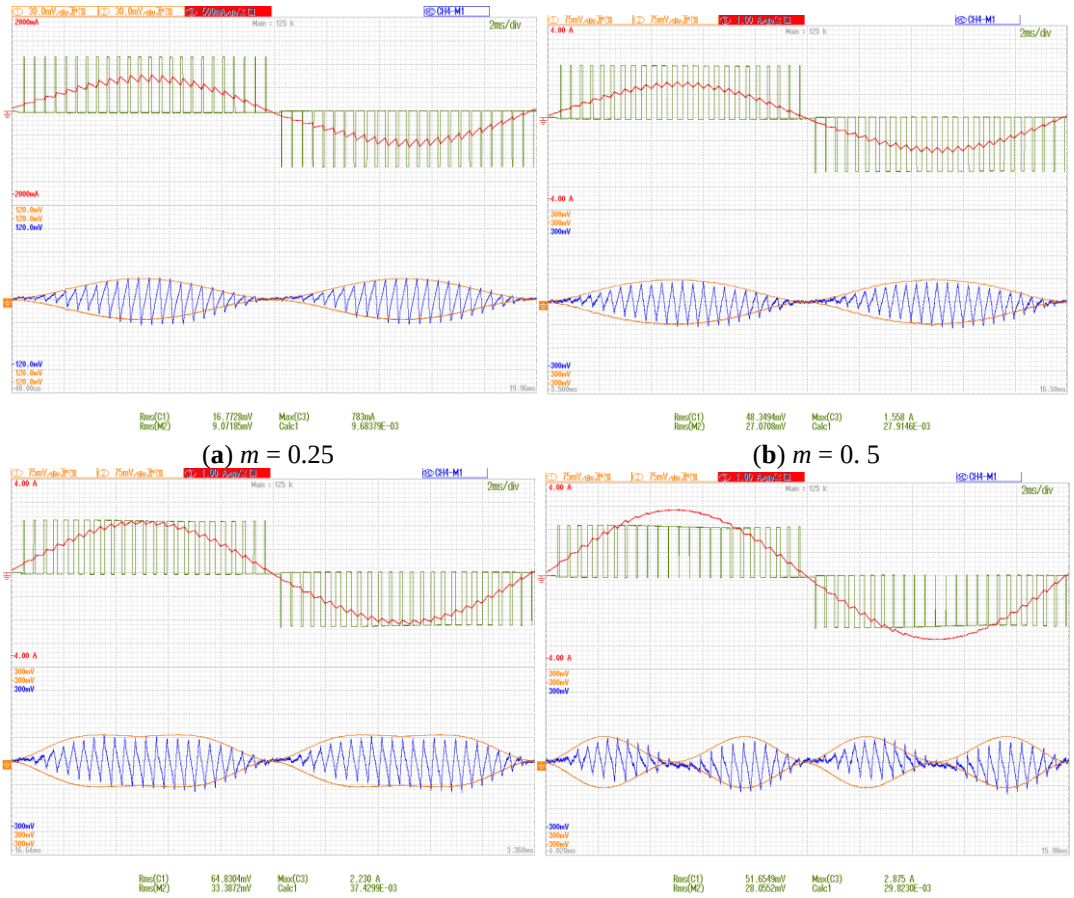


Fig. 2.15: Output load voltage and current (upper part), dc-link voltage (middle part), and zoomed dc-link ripple components (lower part), for m=0.75 and φ=0°.

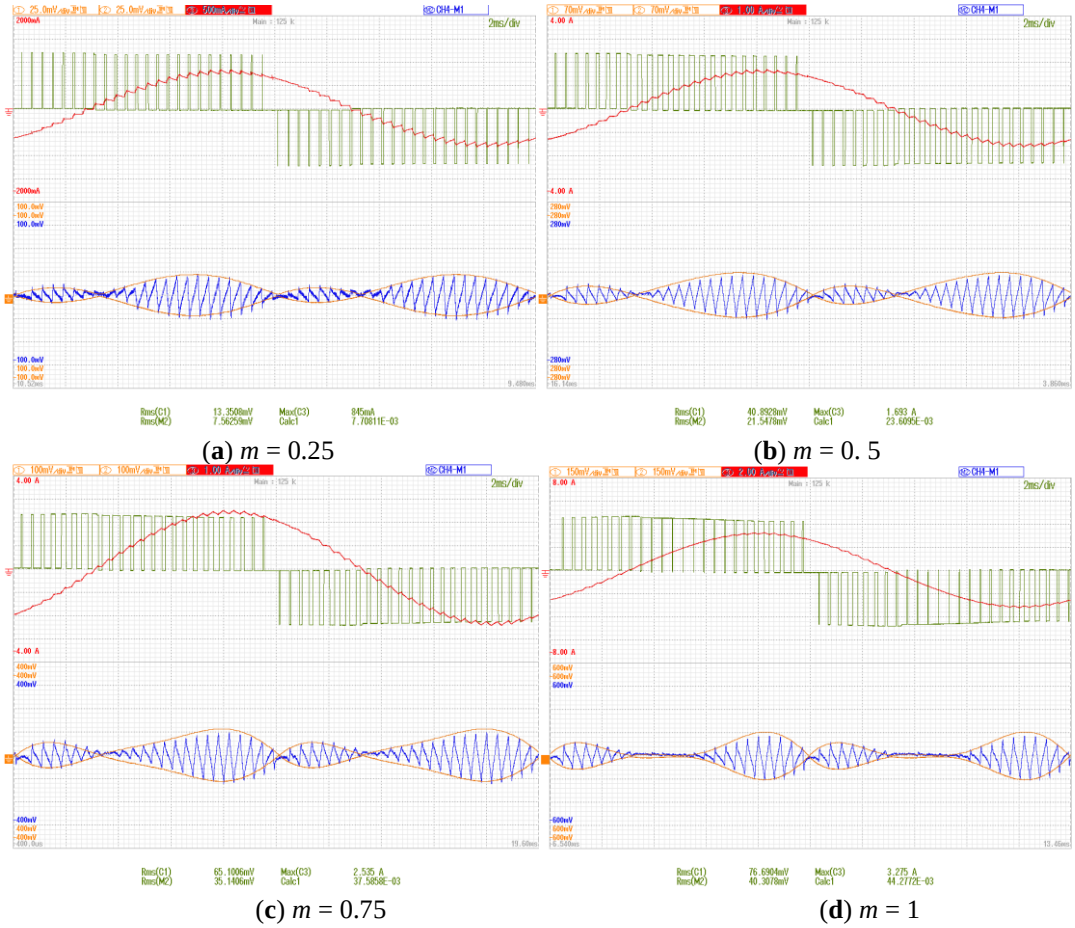
In Figs. 2.16 and 2.17, experimental verifications were carried out considering four different values of the modulation index m = 0.25, 0.5, 0.75, and 1, for two power phase angles φ = 0° and φ = 60°, respectively. In both figures, there are five traces displayed over one fundamental period: top traces present load voltage (green trace) and corresponding load current (red trace), lower blue trace presents the dc-link voltage switching ripple. The two orange traces present the peak-to-peak dc voltage switching ripple envelopes of said ripple ($\pm\Delta v_{pp}/2$), obtained by implementing (2.21) in the microcontroller board and sending to an output DAC channel, with a proper scale factor. Similarly to simulations, the switching ripple component of the dc-link voltage has been obtained by filtering the instantaneous dc-voltage using the "ac coupling" built-in function of the oscilloscope together with the built-in low-pass filter. In that way, electromagnetic noise in the signals was attenuated without affecting any relevant frequency component.



(**a**) m = 0.25 (**b**) m = 0. 5

(**c**) m = 0.75 (**d**) m = 1

Fig. 2.16: Experimental results for φ = 0°: upper half - output voltage and current, lower half – analytically calculated envelope and measured dc voltage switching ripple for (**a**) m = 0.25, (**b**) m = 0.5, (**c**) m = 0.75, and (**d**) m = 1.



(**a**) m = 0.25 (**b**) m = 0. 5

(**c**) m = 0.75 (**d**) m = 1

Fig. 2.17: Experimental results for φ = 60°: upper half - output voltage and current, lower half – analytically calculated envelope and measured dc voltage switching ripple for (**a**) m = 0.25, (**b**) m = 0.5, (**c**) m = 0.75, and (**d**) m = 1.

It can be noticed from Figs. 2.16 and 2.17 that the experimental voltage ripple matches the theoretical envelopes in a very satisfactory way for all the considered cases, both in the absolute amplitude and the dc-link voltage ripple profile, confirming the effectiveness of the proposed analytical developments given by (2.21). Small difference between the measured ripple and the simulated and calculated envelopes is due to the parasitic resistance of electrolytic dc-link capacitor.

Table 2.1 summarizes the calculated, simulated and experimental results for RMS values of dc-link voltage switching ripple (ΔV_{rms}). All considered cases of modulation index and the power phase angles are shown. As it can be seen, the agreement is generally satisfying within the expected resolution and considering the non-idealities of the experimental implementation.

Table 2.1. Comparison of obtained dc-link voltage switching ripple RMS

m	Load angle φ = 0°			Load angle φ = 60°		
	Calc.	*Sim.*	*Exp.*	*Calc.*	*Sim.*	*Exp.*
0.25	9.7	9.6	9.1	7.8	7.8	7.7
0.50	27.5	26.8	27.1	23.6	23.6	21.6
0.75	37.4	35.6	33.4	37.5	37.5	35.1
1.00	29.9	28.7	28.1	44.23	44.3	40.3

2.6 Discussion

In this chapter, dc-link current and voltage ripple analysis of single-phase H-bridge inverter with dc source impedance is presented. The inverter dc-link current, as well as the dc-link voltage, consists of three relevant components and therefore, all of them have been investigated. First, the low-frequency (double-fundamental) current and voltage ripple components are derived. The next, peak-to-peak dc voltage switching ripple amplitude is obtained as a function of operational conditions (modulation index, the amplitude of the output current and power phase angle). Further, the maximum and the RMS of the dc-link voltage switching ripple are determined. In order to show the behavior of the dc voltage ripple components different diagrams are introduced. A simple and effective methodology for designing the dc-link capacitor has been proposed on the basis of the dc-link voltage ripple requirements.

Simulation and experimental results are given considering different values of modulation index and power phase angle. Given results are aimed to show the correctness of analytical calculations comparing the amplitude and the profile of the dc-voltage ripple components with calculated dc-link voltage envelopes.

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Chapter 3

Dc-link current and voltage switching ripple analysis in three-phase inverters

3.1 Introduction

Three-phase two-level voltage source inverters are the most frequently utilized power electronic converters. They are widely used in medium- and high-power applications, such as variable speed drives, uninterruptable power supplies (UPS), flexible AC transmission systems (FACTs), stand-alone and grid-connected power generation systems, etc. The standard three-phase inverter consists of six power switches the switching of which depends on the modulation technique.

In the last decade, various modulation techniques have been proposed in order to improve inverter's performances. Primarily target is the reduction of total harmonic distortion (THD) of output currents, but also the dc bus utilization, electromagnetic interference (EMI), switching losses reduction etc. In essence there are two main approaches to VSI PWM control – carrier-based (CB PWM) and space vector PWM (SVM) [3.1]. CB PWM is more popular for implementation due to its simplicity. It has well-defined harmonic spectrum, fixed switching frequency and less computational time. On the other side, SVM is nowadays more popular for investigation and offers a maximum transfer ratio with lower THD. It is proven that CB PWM can work identically as SVM if a proper zero-sequence signal is injected. Regarding this, both techniques may lead to the same results [3.2].

Recently, output characteristics (voltage and current) of three-phase inverters have been extensively studied. Current ripple is studied in terms of RMS minimization as well as its maximum (peak-to-peak) value. The current ripple analysis in SVM-controlled induction motor drive has been presented in [3.3]. The optimal SVM technique is proposed, characterized by the minimum RMS value of the current ripple over the fundament period. The current ripple RMS has been studied over a subcycle in [3.4] and three hybrid PWM techniques are proposed. The current ripple reduction is achieved by involving multiple switching sequences. The current ripple peak and RMS values are calculated and compared for SVM and discontinues PWM (DPWM) in [3.5]. It has been shown that the current ripple could be predicted in the controller before pulses are generated and so, the switching period could be adaptive to certain ripple requirements. In order to achieve better efficien-

cy and reduce electromagnetic interference (EMI) of three-phase converters while satisfying the ripple current requirements, variable switching control method is proposed in [3.6]. The complete analysis of the peak-to-peak current ripple amplitude distribution over a fundamental period for three-phase VSIs has been given in [3.7]. The peak-to-peak current ripple amplitude is calculated as a function of modulation index, emphasizing its maximum and minimum values.

For three-phase VSIs, input current and voltage characteristics are usually estimated by Fourier series analysis or by root-mean-square (RMS) calculations. The RMS values of the input current and voltage ripple have been calculated in [3.8]. It has been shown no dependency of the inverter input current ripple on the selected PWM scheme, however the optimum reference signal in respect to the inverter input voltage ripple varies with the load power factor angle. In [3.9], the effect of space vector modulation (SVM) and discontinues PWM techniques (DPWM) on the RMS value of the dc-link capacitor current is studied. It is shown that the use of the SVM results in lower dc-link current stress. A simple analytical expression for the current stress on the dc-link capacitor and the experimental verification have been presented in [3.10]. The aim was to reduce the effort for designing the capacitor meeting at the same time the sufficient accuracy for practical inverter system.

Applying a double Fourier series, the dc-link current harmonics are calculated in [3.11], for any kind of conventional modulation strategy with a fixed pulsed frequency. Based on the Fourier analysis, the impact of the harmonic ripple current of the filter circuit on the dc-link capacitor has been investigated in [3.12]. It has been shown that the impact is considerable only in case of small output currents. However, in case of larger loads, it is enough to consider sinusoidal output currents for the dc-link capacitor dimensioning. A general method to calculate dc-link current taking into account ac current ripple has been proposed in [3.13]. This method requires access to various control variables (i_{dq} currents and duty cycles) in real time (sampling time) and this makes it not feasible for some applications, such as in automotive drives.

In order to avoid complex double Fourier integral approach, an approximation for spectral components is provided in [3.14]. The carrier and sideband dc capacitor current harmonics are modeled with an equivalent harmonic at the center, so the dominant harmonics and their effects are better understood. A generalized approach for determining the harmonic spectrum of the dc-link capacitor currents in different two- and three-level VSI topologies has been developed in [3.15]. In [3.16] and [3.17] different modulation methods aiming at reduction of the input current harmonics flowing through the dc-link capacitor have been proposed. The analysis and calculation of the dc-link current and voltage ripple for three-phase inverter under unbalanced load conditions has been presented in [3.18]. The dc-link average and harmonic RMS currents are calculated, and the dc voltage ripple is compared between the balanced and the unbalanced loads.

As it has been shown, the input current and voltage ripple are studied mostly in terms of the RMS minimization, rather than the peak-to-peak value. Two conference papers [3.19] and [3.20] and one journal paper [3.21] that show peak-to-peak dc-link voltage switching ripple distribution over a fundamental period are results of this thesis. The evaluation of the dc-link voltage switching ripple has been done in case of sinusoidal PWM and space vector modulation, being the two most-commonly applied inverter control techniques. Hence, a short review of both modulations is given in section 3.2. The detailed analytical analysis of the inverter's dc-link current and voltage ripple is shown in the next sections 3.3 and 3.4, respectively. The maximum peak-to-peak value of voltage switching ripple amplitude is shown as a function of modulation index for different power phase angles. The dc-link voltage switching ripple requirements are used for the dc-link capacitor design in section 3.5. Simulations and experimental results are further included in section 3.6. Finally, a brief discussion of obtained results is given in section 3.7.

3.2 Modulation techniques

The most widely utilized modulation strategy for *n*-phase voltage source inverters is carrier-based PWM, where the reference waveform of each leg v_n^* is compared with a high-frequency triangular carrier waveform and, as a result, switching signals are generated per each inverter leg. Fig. 3.1 shows generalized concept of the carrier-based modulation including the zero-sequence signal injection.

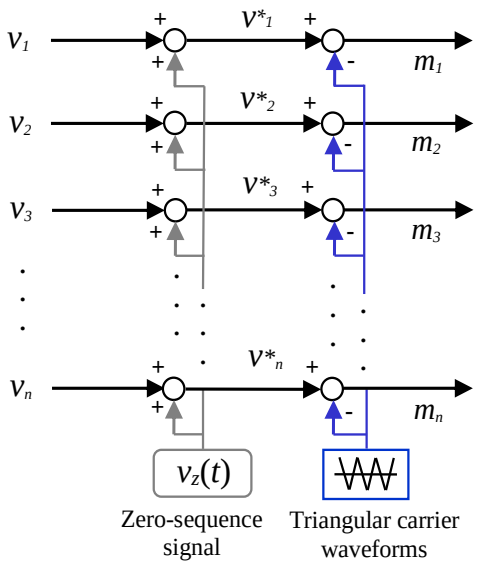


Fig. 3.1: Principle of carrier-based PWM.

Based on Fig. 3.1, three reference signals $v_n^*(t)$ (n = 3) can be expressed as:

$$\begin{cases} v_1^*(t) = mV\cos(\vartheta) + v_z(t) \\ v_2^*(t) = mV\cos(\vartheta - \frac{2\pi}{3}) + v_z(t) \\ v_3^*(t) = mV\cos(\vartheta - \frac{4\pi}{3}) + v_z(t) \end{cases} \tag{3.1}$$

where $v_z(t)$ is the zero-sequence signal summed with the three sinusoidal fundamental signals displaced in time by $2\pi/3$ degrees. $\vartheta=\omega t$, $\omega=2\pi f$ is the fundamental angular frequency, and m is the inverter modulation index defined as the ratio of the fundamental output phase voltage magnitude and the dc supply voltage. Hence, fundamental signals are in the range (-0.5 ÷ 0.5) and for the sake of comparison, the same range is assumed for triangular carrier waveforms. In general, zero-sequence signal can be considered as a degree of freedom and can be used to improve the output current ripple and to increase the dc-bus utilization. Various modulation techniques have been proposed in last years, considering different selections of the zero-sequence. In this thesis, sinusoidal PWM (SPWM) and so called centered PWM (CPWM), obtained by centering the reference voltages with "min-max" injection, equivalent to space vector modulation (SVM), have been used. Therefore, a short review of two modulation strategies will be given in what follows.

Carrier-based PWM

According to Fig. 3.1 and in order to obtain SPWM, the zero-sequence signal is set to:

$$v_z(t) = 0\,.$$

Three reference signals become equal to the sinusoidal fundamental signals, displaced in time by $2\pi/3$ degrees as

$$\begin{cases} v_1^*(t) = mV\cos(\vartheta) \\ v_2^*(t) = mV\cos\left(\vartheta - \frac{2\pi}{3}\right). \\ v_3^*(t) = mV\cos\left(\vartheta - \frac{4\pi}{3}\right) \end{cases} \tag{3.2}$$

Fig. 3.2 shows reference signals of (3.2), compared with the triangle carrier waveforms, for one fundamental period and for modulation index set as m=0.5. It is noticeable that fundamental period can be divided into six sectors, each spanning $\pi/3$ degrees.

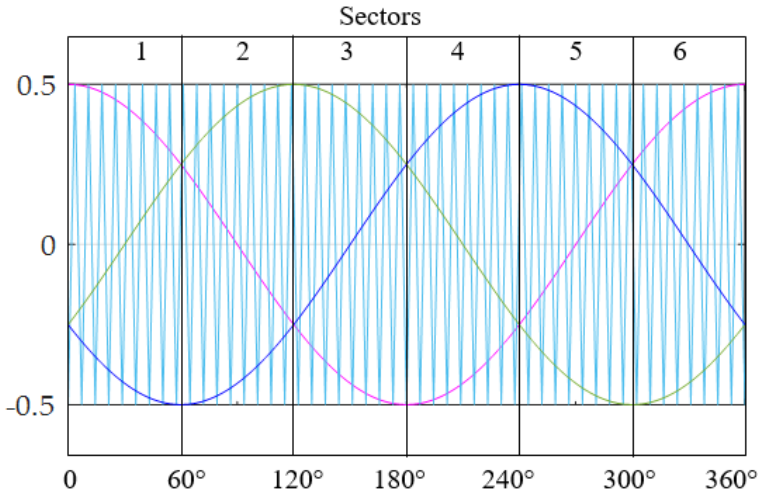


Fig. 3.2: Reference signals for three-phase VSIs over one fundamental period (SPWM).

When the frequency of the carrier (switching frequency) is much higher than the frequency of reference signals, the reference signals can be assumed constant during one carrier period (regular sampled PWM). Considering the first sector, as an example, Fig. 3.3 shows three reference signals over one switching period (T_{sw}) together with a carrier signal, and generated PWM switching patterns (switching functions).

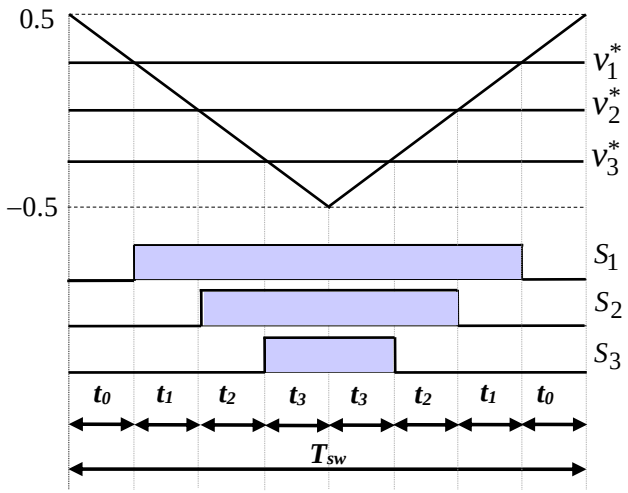


Fig. 3.3: Principle of generation of switching pattern for three-phase VSIs.

The application times t_k, k=0,1,..3 can be calculated based on Fig. 3.3 and by means of simple trigonometry. It is expressed as:

$$t_0 = \frac{T_{sw}}{2}\left(\frac{1}{2} - m\cos(\vartheta)\right), \tag{3.3}$$

$$t_1 = mT_{sw}\frac{\sqrt{3}}{2}\left(\sqrt{3}\cos(\vartheta) - \sin(\vartheta)\right), \tag{3.4}$$

$$t_2 = mT_{sw}\sqrt{3}\sin(\vartheta), \tag{3.5}$$

$$t_3 = \frac{T_{sw}}{2}\left(\frac{1}{2} + m\cos\left(\vartheta - \frac{4\pi}{3}\right)\right). \tag{3.6}$$

According to Fig. 3.1, centered PWM (CPWM) can be achieved by adding to the three sinusoidal reference signals the zero-sequence signal expressed as:

$$v_z(t) = -0.5\left(v^*_{\max} + v^*_{\min}\right). \tag{3.7}$$

Signals inside the brackets are determined based on the maximum and minimum values of the input set of fundamental signals. Such a zero-sequence signal is known as "min-max" injection. Comparing to the SPWM, an increase of around 15.47% in the dc bus utilization, in the linear modulation region, is achieved if CPWM is applied to three-phase system. Thus, in case of three-phase inverters, the modulation limit becomes m_{max}=0.577.

The effect of a "min-max" injection is shown in Fig. 3.4 where three reference signals are shown over one fundamental period.

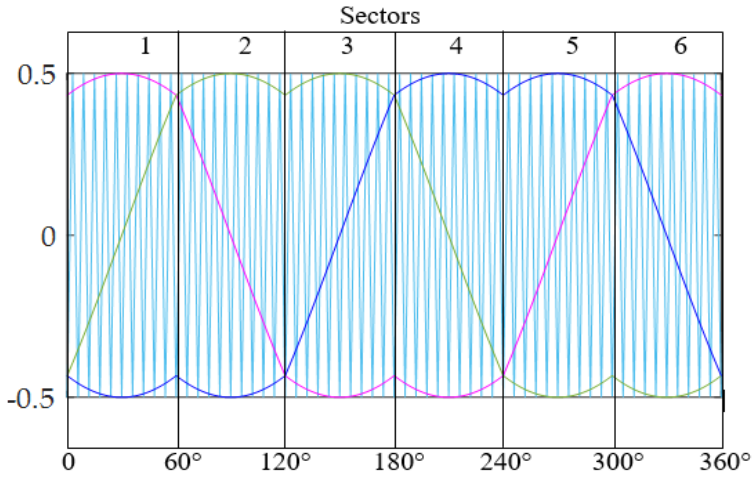


Fig. 3.4: Reference signals for three-phase VSIs over one fundamental period (CPWM).

It can be noted that after the injection (Fig. 3.4) the ordering of the reference signals remains the same as before injection (Fig. 3.2). Thus, it can be concluded that the switching sequences (and so, the application times) of the active space vectors will be the same as in case of SPWM. The difference is in the application times of two zero space vectors. Based on (3.2), (3.7) and Sector 1 (Fig. 3.4), the application times of two zero space vectors are calculated as:

$$t_0 = \frac{T_{sw}}{2}\left[\frac{1}{2} - m\cos(\vartheta) + \frac{1}{2}\left(m\cos(\vartheta) + m\cos\left(\vartheta - \frac{4\pi}{3}\right)\right)\right], \tag{3.8}$$

$$t_3 = \frac{T_{sw}}{2}\left[\frac{1}{2} + m\cos\left(\vartheta - \frac{4\pi}{3}\right) - \frac{1}{2}\left(m\cos(\vartheta) + m\cos\left(\vartheta - \frac{4\pi}{3}\right)\right)\right]. \tag{3.9}$$

Applying basic trigonometric equations, the following simplification is obtained:

$$t_0 = t_3 = \frac{T_{sw}}{2}\left[1 - \sqrt{3}\,m\sin\left(\frac{\pi}{3} + \vartheta\right)\right]. \tag{3.10}$$

Space vector modulation

Although the CBPWM is significantly simpler for implementation, space vector modulation (SVM) offers better performances and is nowadays more popular for investigation. The SVM for three-phase inverters is based on the fact that there are 2^3=8 possible switching configurations (or "switching states"). Fig. 3.5 represents the eight output voltage space vectors corresponding to the switching configurations. Vectors $\vec{V}_1$ to $\vec{V}_6$ are called active vectors, and $\vec{V}_o$, $\vec{V}_7$ are called zero vectors. In one switching period, the reference space vector $\vec{v}^*$ can be given by [3.2]

$$\vec{v}^*(t) = \frac{t_o}{T_{sw}}\vec{V}_o + \frac{t_1}{T_{sw}}\vec{V}_1 + \ldots + \frac{t_7}{T_{sw}}\vec{V}_7, \tag{3.11}$$

where t_o, t_1, …, t_7 are the application times of the vectors $\vec{V}_0$, $\vec{V}_1$,... $\vec{V}_7$ and $\sum_{i=0}^{7} t_i = T_{sw}$.

In general, the decomposition of the reference output voltage space vector $\vec{v}^*$ into the output voltage space vectors has infinite ways. However, the most commonly, two nearest adjacent active vectors and two zero vectors ($\vec{V}_o, \vec{V}_7$) are used in each switching period to synthetize the reference space vector $\vec{v}^*$. The switching sequence begins and ends with the zero-space vector (so called "null switching state"). The center switching pattern is realized when the total application time of the zero vector is equally shared between two

zero space vectors ($\vec{V}_o, \vec{V}_7$). It has been proven in [3.2] that the center switching pattern is equivalent to zero-sequence signal injection defined by (3.7) in carrier based PWM.

In case of symmetrical SVM, the sequence can be determined in $T_{sw}/2$ and symmetrically repeated in the next half of the switching period. The application times of the active and zero space vectors in the first sector (colored triangle in Fig. 3.5), are identical to those of (3.4), (3.5) and (3.10) obtained for CPWM.

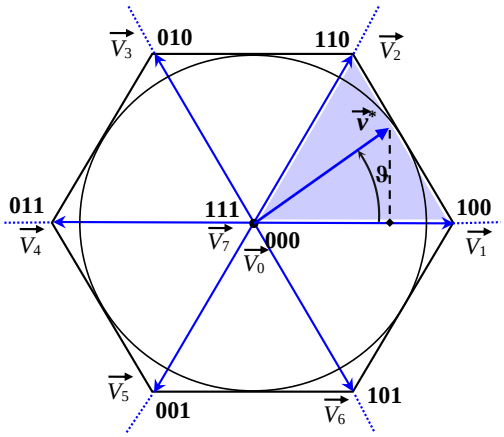


Fig. 3.5: Space vector diagram of inverter output voltage.

3.3 Dc-link current analysis

Configuration of the analyzed topology, the two-level three-phase VSI with balanced passive- or motor-load, is shown in Fig. 3.6. The inverter is supplied by a dc voltage source (V_{dc}) through an equivalent series dc source impedance Z_{dc}. The parallel capacitor C is connected to the dc bus to smooth the voltage ripple.

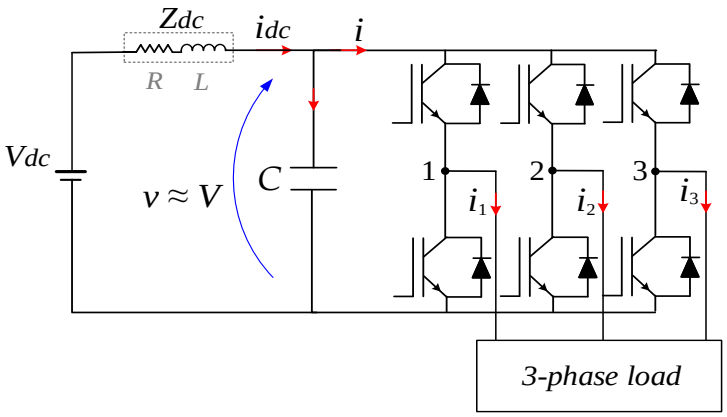


Fig. 3.6: Analyzed topology of a two-level three-phase VSI.

Neglecting the dc-link voltage oscillations ($v \approx V$) and considering the operations in the linear modulation region, the inverter output phase voltages averaged over the switching period correspond to the reference phase voltages given by (3.2).

Considering (3.2), in case of balanced load and neglecting the output current ripple, the corresponding three-phase sinusoidal output currents can be written as:

$$\begin{cases} i_1 = I_0 \cos(\vartheta - \varphi), \\ i_2 = I_0 \cos\left(\vartheta - \frac{2\pi}{3} - \varphi\right), \\ i_3 = I_0 \cos\left(\vartheta - \frac{4\pi}{3} - \varphi\right), \end{cases} \tag{3.12}$$

where I_0 is the output current amplitude and φ is the phase angle between the phase voltage and current, respectively.

As introduced in the section 2.3, the dc-link current $i(t)$ can be expressed by three key components, the dc (average) component, the low-frequency, and the high-frequency (switching frequency) component. When the load is balanced, low-frequency component is zero. Consequently, the inverter input current only contains the dc (average) component $I = I_{dc}$, which comes from the dc supply, and the high-frequency component $\Delta i(t)$ which is bypassed through the dc-link capacitor. Thus, the instantaneous dc-link current of three-phase inverter supplying balanced load can be expressed as:

$$i(t) = I_{dc} + \Delta i(t). \tag{3.13}$$

Under the assumption that inverter power switches are ideal and by considering the input/output power balance as:

$$VI_{dc} = 3\frac{mV}{\sqrt{2}}\frac{I_0}{\sqrt{2}}\cos\varphi, \tag{3.14}$$

the dc-link current averaged over the switching period T_{sw} can be obtained on the basis of (3.14) and it is finally given by:

$$I_{dc} = \frac{3}{2} m I_0 \cos\varphi. \tag{3.15}$$

An instantaneous value of the inverter input current i can be calculated as the sum of three inverter leg currents which are dependent on the inverter switching state. Considering the switching states of each leg through the binary switching function S_k:

$$S_k = \begin{cases} 1 \rightarrow \textit{upper switch ON, lower switch OFF} \\ 0 \rightarrow \textit{upper switch OFF, lower switch ON} \end{cases}, \quad k = 1, 2, 3, \tag{3.16}$$

the input current of each inverter leg can be calculated from switching function and corresponding output current. Consequently, the total inverter input current can be expressed by summing the individual leg currents as:

$$i = \sum_{k=1}^{3} S_k i_k \, . \tag{3.17}$$

The switching frequency dc-link current component can be easily calculated utilizing equations (3.13) - (3.16) as:

$$\Delta i(t) = i - I_{dc} = \sum_{k=1}^{3} S_k i_k - \frac{3}{2} m I_0 \cos\varphi \, . \tag{3.18}$$

Due to the symmetry of the inverter input current, the following analysis can be limited to one sixth of the fundament period ($T/6$ or $\pi/3$ rad).

3.4 Dc-link voltage ripple analysis

3.4.1 Voltage switching ripple evaluation

Similar to the dc-link current, the instantaneous dc-link voltage can be expressed by three following components: the dc (average) component V, the low-frequency component, and the high-frequency component Δv. The low-frequency component is zero since it is determined on the basis of the corresponding current component that is zero when the load is balanced. Correspondingly, the instantaneous dc-link voltage is expressed as:

$$v(t) = V + \Delta v(t). \tag{3.19}$$

The average voltage component V is simply determined by the supply voltage V_{dc} and the voltage drop on the dc source resistance R as:

$$V = V_{dc} - R\, I_{dc} \, . \tag{3.20}$$

The peak-to-peak amplitude Δv_{pp} of the dc-link voltage switching ripple component can be calculated as the difference between its maximum and minimum value within the switching period, as it was shown in the sub-section 2.3.2 and given by (2.18). The same assumption for the dc-link equivalent impedance calculated at the switching frequency,

and therefore for the dc-link current switching frequency component that circulates through the dc-link capacitor, applies to the three-phase case as well.

However, in the three-phase case, the corresponding dc voltage excursion is determined by integrating Δi over the specific application time interval t_k. The application times are calculated in section 3.2 for used modulation strategies and will be correspondingly applied in the following. An effective simplification is obtained by considering Δi constant (ΔI) within the considered application time interval, leading to:

$$\Delta v_{pp}^{k} = \left| \frac{1}{C} \int_{0}^{t_k} \Delta i(t)\, dt \right| \cong \frac{1}{C} \Delta I\, t_k \,. \tag{3.21}$$

Due to the inverter input current $i(t)$ periodicity, the evaluation of the voltage ripple can be reduced to the phase angle range $0 \le \vartheta \le 60°$, i.e. the first $\pi/3$ rad.

Within the first sector, depending on the value of I_{dc}, two different cases can be distinguished according to Fig. 3.7. The global peak-to-peak dc-link voltage ripple amplitude Δv_{pp} is obtained by combining different Δv_{pp}^{k} and finding the maximum within the switching period, as it will be shown in following.

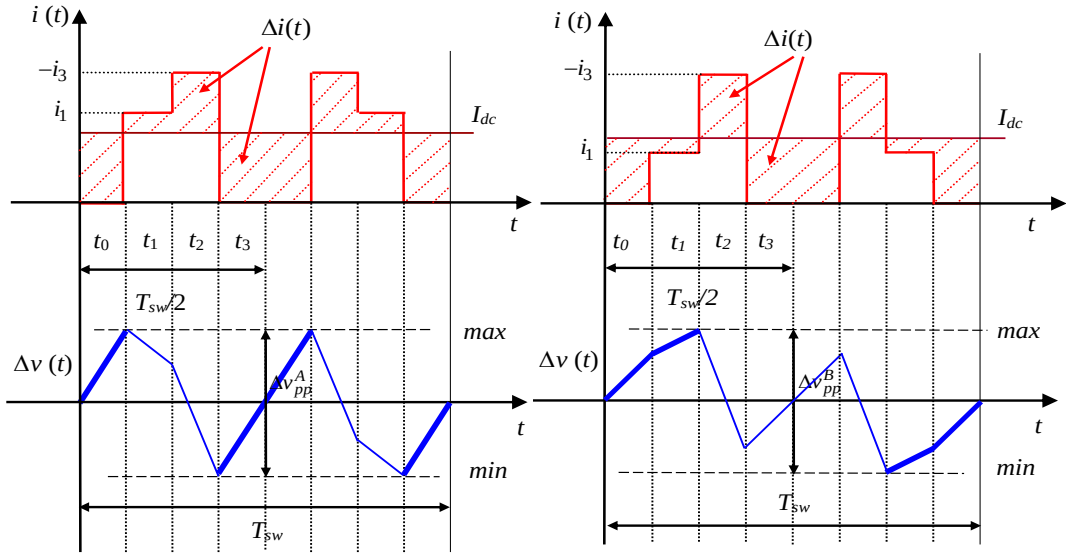


Fig. 3.7: Dc-link current and voltage ripple in one switching period:
(**a**) Case A ($0 \le \vartheta \le \pi/3$, $i_1 \ge I_{dc}$), (**b**) Case B ($0 \le \vartheta \le \pi/3$, $i_1 < I_{dc}$).

The dc-link voltage switching ripple for three-phase VSI is investigated under the sinusoidal PWM and space vector modulation (equivalent to CPWM) as shown in following two sub-sections.

3.4.1.1 Peak-to-peak voltage switching ripple with sinusoidal PWM

Case A.1 – Evaluation in the range: $i_1 \geq I_{dc}$

The dc-link voltage ripple Δv and its peak-to-peak value Δv_{pp} are depicted in Fig. 3.7 (blue line), together with the instantaneous input current $i(t)$ (red staircase line). According to Fig. 3.7(a) two subcases can be distinguish regarding the application time intervals $t_{pp} = t_0$ and $t_{pp} = t_3$ (bold blue trace).

In the first subcase, when $t_{pp} = t_0$, the peak-to-peak voltage ripple can be written on the basis of (3.21) as

$$\Delta v_{pp}^{A1} = \frac{2}{C} I_{dc} t_0 \ . \tag{3.22}$$

Introducing (3.3) and (3.15) into (3.22) leads to

$$\Delta v_{pp}^{A1} = \frac{3}{2} \frac{I_0 T_{sw}}{C} m \cos\varphi \left(\frac{1}{2} - m \cos\left(\vartheta\right) \right). \tag{3.23}$$

In the same way, but considering $t_{pp} = t_3$ time interval, the peak-to-peak voltage ripple is calculated as

$$\Delta v_{pp}^{A2} = \frac{2}{C} I_{dc} t_3 \ . \tag{3.24}$$

Introducing (3.4) and (3.15) into (3.24) leads to

$$\Delta v_{pp}^{A2} = \frac{3}{2} \frac{I_0 T_{sw}}{C} m \cos\varphi \left(\frac{1}{2} + m \cos\left(\vartheta - \frac{4\pi}{3} \right) \right). \tag{3.25}$$

Case B.1 – Evaluation in the range: $i_1 < I_{dc}$

According to Fig. 3.7(b) and considering application interval $t_{pp} = t_0+t_1$ (bold blue trace), peak-to-peak voltage ripple can be written on the basis of (3.21) as:

$$\Delta v_{pp}^{B} = \frac{2}{C} \left(I_{dc} t_0 + (I_{dc} - i_1)\, t_1 \right). \tag{3.26}$$

Introducing (3.3), (3.4), and (3.15) in (3.26) leads to

$$\Delta v_{pp}^{B} = \frac{3}{2}\frac{I_0 T_{sw}}{C} m\left[\cos\varphi\left(\frac{1}{2} - m\cos(\vartheta)\right) + \frac{1}{\sqrt{3}}\left(\sqrt{3}\cos(\vartheta) - \sin(\vartheta)\right)\left(\frac{3}{2}m\cos\varphi - \cos(\vartheta - \varphi)\right)\right]. \quad (3.27)$$

The global peak-to-peak dc-link voltage ripple amplitude Δv_{pp} is obtained by merging the results corresponding to the cases A.1 and B.1:

$$\Delta v_{pp}^{SPWM} = \max\left\{\Delta v_{pp}^{A1}, \Delta v_{pp}^{A2}, \Delta v_{pp}^{B}\right\}. \quad (3.28)$$

Finally, from Equation (3.28), one can see that the magnitude of the dc-link voltage ripple is always determined by the maximum value of those three.

Dc-link peak-to-peak voltage ripple amplitude can be normalized according to:

$$\Delta v_{pp}^{SPWM} = \frac{I_0 T_{sw}}{C} r_{pp}(m, \vartheta, \varphi). \quad (3.29)$$

Applying (3.29) to the case A and the case B, the normalized peak-to-peak voltage ripple amplitude is given by:

$$r_{pp}^{SPWM} = \max\left\{r_{pp}^{A1}, r_{pp}^{A2}, r_{pp}^{B}\right\}, \quad (3.30)$$

being

$$r_{pp}^{A1}(m, \vartheta, \varphi) = \frac{3}{2}m\cos\varphi\left(\frac{1}{2} - m\cos(\vartheta)\right), \quad (3.31)$$

$$r_{pp}^{A2}(m, \vartheta, \varphi) = \frac{3}{2}m\cos\varphi\left(\frac{1}{2} + m\cos\left(\vartheta - \frac{4\pi}{3}\right)\right), \quad (3.32)$$

$$r_{pp}^{B}(m, \vartheta, \varphi) = \frac{3}{2}m\left|\cos\varphi\left(\frac{1}{2} - m\cos(\vartheta)\right) + \frac{1}{\sqrt{3}}\left(\sqrt{3}\cos(\vartheta) - \sin(\vartheta)\right)\left(\frac{3}{2}m\cos\varphi - \cos(\vartheta - \varphi)\right)\right|. \quad (3.33)$$

3.4.1.2 Peak-to-peak voltage switching ripple with SVM

As it was discussed in section 3.2, when space vector modulation is applied the total application time of the zero space vector is equally shared between two zero space vector. It means that the application times t_0 and t_3 (Fig. 3.7) are equal and given by (3.10). Therefore, as in sub-section 3.4.1.1, evaluation of dc voltage switching ripple is further presented for two different ranges according to the average current I_{dc} value and Fig. 3.7.

Case A.2 – Evaluation in the range: $i_1 \geq I_{dc}$

According to Fig. 3.7(a) and considering application interval $t_{pp} = t_0$ (bold blue trace), peak-to-peak voltage ripple can be written on the basis of (3.21) as

$$\Delta v_{pp}^{A} = \frac{2}{C}\left(I_{dc}\frac{t_0}{2}\right) = \frac{1}{C} I_{dc} t_0 . \tag{3.34}$$

Introducing (3.4) and (3.15) into (3.34) leads to

$$\Delta v_{pp}^{A} = \frac{3}{4}\frac{I_{dc} T_{sw}}{C} m \cos\varphi \left(1 - \sqrt{3} m \sin\left(\frac{\pi}{3} + \vartheta \right) \right). \tag{3.35}$$

Case B.2 – Evaluation in the range: $i_1 < I_{dc}$

According to Fig. 3.7(b) and considering application interval $t_{pp} = t_0/2 + t_1$ (bold blue trace), peak-to-peak voltage ripple can be written on the basis of (3.21) as:

$$\Delta v_{pp}^{B} = \frac{2}{C}\left(I_{dc}\frac{t_0}{2} + (I_{dc} - i_1) t_1 \right). \tag{3.36}$$

$$\Delta v_{pp}^{B} = \frac{3}{4}\frac{I_0 T_{sw}}{C} m \cdot \left| \cos\varphi \left(1 - \sqrt{3} m \sin\left(\frac{\pi}{3} + \vartheta \right) \right) + \frac{4}{\sqrt{3}} \sin\left(\frac{\pi}{3} - \vartheta \right) \left(\frac{3}{2} m \cos\varphi - \cos(\vartheta - \varphi) \right) \right| . \tag{3.37}$$

The global peak-to-peak dc-link voltage ripple amplitude Δv_{pp} is obtained by merging the results corresponding to the cases A.2 and B.2:

$$\Delta v_{pp}^{SVM} = \max\left\{ \Delta v_{pp}^{A}, \Delta v_{pp}^{B} \right\}. \tag{3.38}$$

Applying the same normalization as in (3.29), the normalized peak-to-peak voltage ripple amplitude is given by

$$r_{pp}^{SVM} = \max\left\{ r_{pp}^{A}, r_{pp}^{B} \right\}, \tag{3.39}$$

where

$$r_{pp}^{A}(m, \vartheta, \varphi) = \frac{3}{4} m \cos\varphi \left(1 - \sqrt{3} m \sin\left(\frac{\pi}{3} + \vartheta \right) \right), \tag{3.40}$$

$$r_{pp}^{B}(m, \vartheta, \varphi) = \frac{3}{4} m \cdot \left| \cos\varphi \left(1 - \sqrt{3} m \sin\left(\frac{\pi}{3} + \vartheta \right) \right) + \frac{4}{\sqrt{3}} \sin\left(\frac{\pi}{3} - \vartheta \right) \left(\frac{3}{2} m \cos\varphi - \cos(\vartheta - \varphi) \right) \right| . \tag{3.41}$$

In order to show the behavior and make a comparison of the peak-to-peak voltage switching ripple amplitudes over the fundamental period, when sinusoidal PWM and space vector modulation (equivalent to "centered" PWM) are applied, Fig. 3.8 depicts the normalized peak-to-peak voltage switching ripple amplitude.

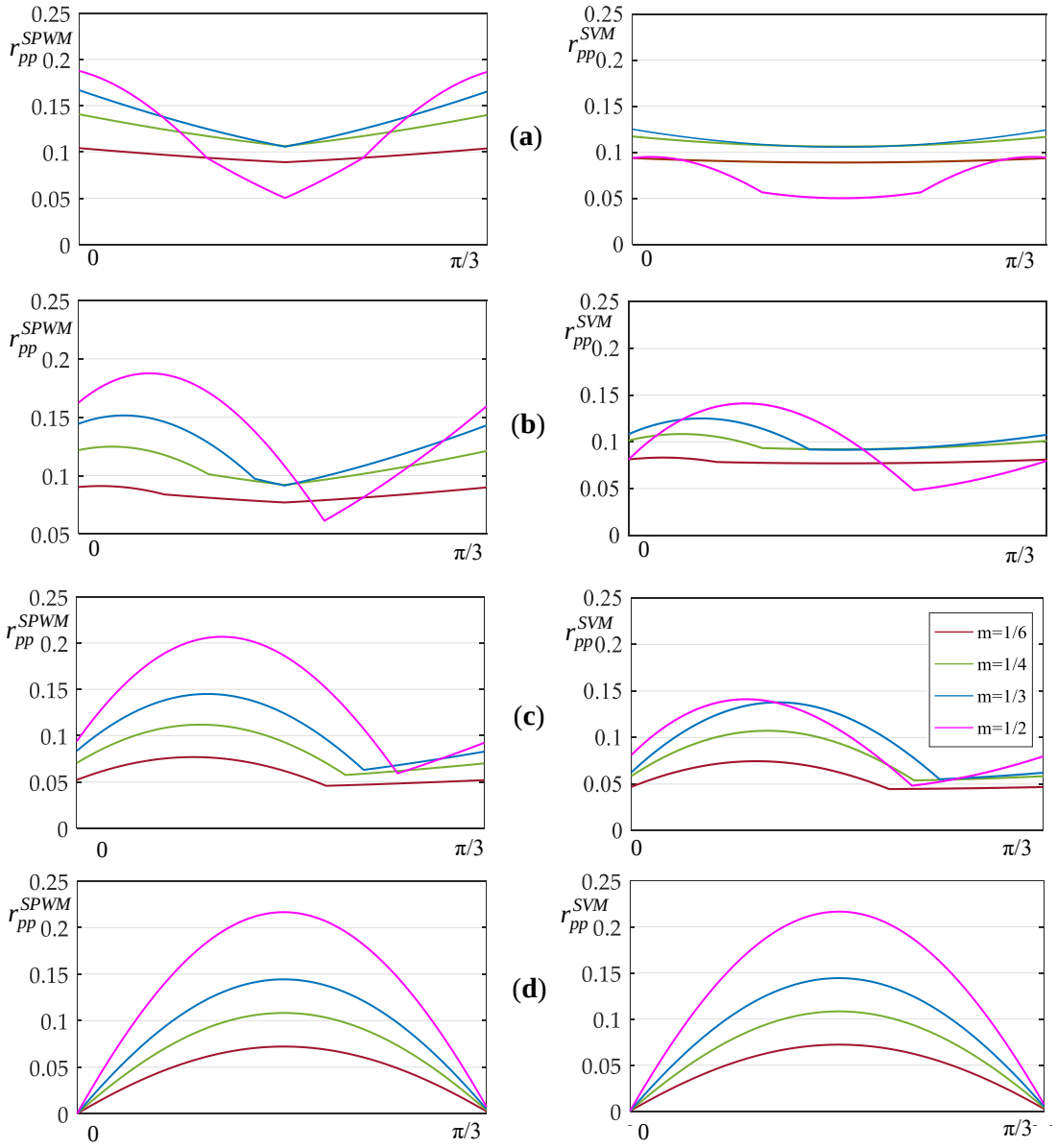


Fig. 3.8: Normalized peak-to-peak dc-link voltage ripple amplitude $r_{pp}(\vartheta)$ over the fundamental period [0, π/3], when SPWM (left) and SVM (right) are applied, for different modulation indices, m = 1/6, 1/4, 1/3 and 1/2, and power phase angles φ = 0° (**a**), 30° (**b**), 60° (**c**) and 90° (**d**).

Four power phase angles ϑ = 0, 30°, 60° and 90° have been considered. Four cases that correspond to the operation with m = 1/6, 1/4, 1/3, and 1/2, respectively, are illustrated for each power phase angle.

It can be seen a wide excursion of the dc voltage ripple amplitude, generally ranging between 0 (minimum) and 0.22 (maximum). An increase in the maximum peaks of the voltage ripple occur with the increase of the modulation index. A slight increase of the peak-to-peak voltage switching ripple amplitude is also noticeable with the increase of the power phase angle in case of both SPWM and SVM. It can be seen that for the same values of power phase angles and modulation index, the peak-to-peak voltage ripple amplitude significantly decreases when SVM is applied instead of SPWM. Only for the power phase angle φ = 90° both techniques are equal.

3.4.2 Maximum of the voltage switching ripple

For the dc-link capacitor design and selection purposes, it is of importance to show the maximum of the normalized peak-to-peak voltage switching ripple amplitude. Fig. 3.9 shows the maximum as a function of modulation index. To provide an illustrative comparison, the maximum voltage ripple amplitude is shown together for SPWM and SVM, considering different power phase angles. Bold traces represent the case when SPWM is applied and dashed traces represent the case when SVM is applied.

For the power phase angle φ = 90° the maximum is analytically determined. It is the same for both modulations, SPWM and SVM, and it is expressed as:

$$r_{pp}^{\max}(m,\varphi=90^\circ)=r_{pp}^{B}\Big|^{\max}=\frac{\sqrt{3}}{4}m\,. \tag{3.42}$$

For the power phase angles φ = 0° the maximum is analytically determined in case of SPWM (3.43) and SVM (3.44) as:

$$r_{pp}^{\max}(m,\varphi=0,SPWM)=r_{pp}^{B}\Big|^{\max}=\frac{3}{4}m-\frac{3}{4}m^2\,, \tag{3.43}$$

$$r_{pp}^{\max}(m,\varphi=0,SVM)=r_{pp}^{B}\Big|^{\max}=\frac{3}{4}m-\frac{9}{8}m^2\,. \tag{3.44}$$

Due to the cumbersome calculations, for other presented values of power phase angles (ϑ = 60° and 30°) the maximum is obtained by properly interpolating data with reasonable degree of approximation. The following equations are obtained:

$$r_{pp}^{\max}(m,\varphi=30^\circ,SPWM)\cong 0.62\,m-0.5\,m^2\,, \tag{3.45}$$

$$r_{pp}^{\max}(m, \varphi = 60^{\circ}, SPWM) \cong 0.375\, m\,, \tag{3.46}$$

$$r_{pp}^{\max}(m, \varphi = 30^{\circ}, SVM) \cong 0.55\, m - 0.54\, m^2\,, \tag{3.47}$$

$$r_{pp}^{\max}(m, \varphi = 60^{\circ}, SVM) \cong 0.45m - 0.13m^2\,. \tag{3.48}$$

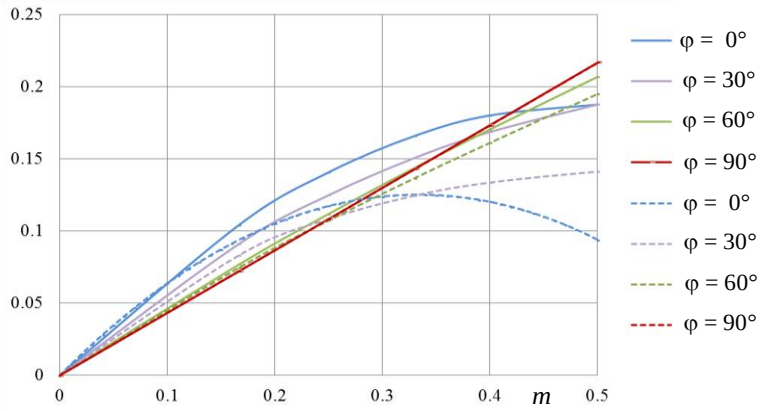


Fig. 3.9: Maximum of normalized peak-to-peak voltage ripple amplitude vs. modulation index for different power phase angles and two modulation techniques (SPWM – bold traces, SVM – dashed traces).

It can be seen from Fig. 3.9 that the maximum voltage ripple amplitude is significantly lower in case of SVM, especially for lower phase angles. Only in case of φ=90° both techniques give the same results. Moreover, in case of SPWM there is no significant difference in terms of global maximum value when different power phase angles are considered. In all considered cases, except the case of φ=0°, the maximum is nearly linear function of the modulation index. When SVM is applied, the maximum of peak-to-peak voltage ripple amplitude is more dependent on the power phase angle and it is double reduced for φ = 0° comparing to φ = 90°. It can be finally concluded that from the point of view of the maximum value of the voltage ripple, SVM is preferable in the considered case of three-phase inverters. Note that for the reason of comparison the maximum modulation index in Fig. 3.9 is 0.5 for both PWM strategies, although in case of SVM m_{max}=0.577.

3.5 Dc-link capacitor design

In this section, the dc-link capacitor design is proposed on the basis of the maximum dc voltage switching ripple shown in Fig. 3.9 for different operational conditions. Two boundary conditions (φ = 0° and φ = 90°) have been chosen for the following analysis. The first case (φ = 0°) corresponds to the most of grid-connected applications. The second case

(φ = 90°) has the highest peak-to-peak voltage ripple value, hence, it requires the biggest dc-link capacitor. The global maximum values of the voltage switching ripple for the corresponding two cases are depicted in Table 3.1, considering both modulation techniques.

Table 3.1: Global maximum of $r_{pp}^{\max}$ as a function of PWM for different power phase angles.

angle	SPWM	SVM
φ = 0°	0.19	0.125
φ = 90°	0.22	

By observing Fig. 3.9, and considering $r_{pp}^{\max}$ given in Table 3.1, a simple expressions for the dc-link capacitor design are obtained on the basis of (3.29) as a function of the required peak-to-peak voltage switching ripple amplitude Δv_{pp}^{*}. For two cases of interest, and considering both modulation techniques, the following formulas are obtained.

For φ = 0º, when SPWM is applied, the capacitance can be calculated as:

$$C \geq 0.19 \frac{I_o}{f_{sw}} \frac{1}{\Delta v_{pp}^{*}}, \tag{3.49}$$

On the other side, when SVM is applied and φ = 0º considered, the capacitance can be calculated as:

$$C \geq 0.125 \frac{I_o}{f_{sw}} \frac{1}{\Delta v_{pp}^{*}}. \tag{3.50}$$

Note that the coefficients in the equations (3.49) and (3.50) clearly suggest the need for higher capacitance value when SPWM is applied instead of SVM, when the same peak-to-peak voltage ripple requirements are set.

For φ = 90º, when either SPWM or SVM is applied, the capacitance is given by:

$$C \geq 0.22 \frac{I_o}{f_{sw}} \frac{1}{\Delta v_{pp}^{*}}. \tag{3.51}$$

It can be noted that the designing procedure is simple and straightforward. Similarly to presented cases, the dc-link capacitor can be designed for any other operational conditions of interest.

3.6 Simulation and experimental results

To validate analytical developments, both simulations and experiments are conducted. The results are presented in Fig. 3.10-3.18, for both PWM techniques, SPWM and SVM (equivalent to CPWM). Numerical simulations have been carried out by Matlab/Simulink. The simulation circuit parameters are set in order to match the corresponding experimental setup parameters and are summarized in Table 3.2. Only linear modulation index is analyzed, and the maximum modulation index is 0.5 and 0.577 for SPWM and SVM, respectively.

Table 3.2: Simulation circuit and experimental setup parameters.

Label	Description	Parameters
V_{dc}	Dc voltage supply	90 V
R	Dc source resistance	5 Ω
L	Dc source inductance	10.15 mH
C	Dc-link capacitance	100 μF
f	Fundamental frequency	50 Hz
f_{sw}	Switching frequency	2.5 kHz

Fig. 3.10 and 3.11 show simulation results in case of SVM and SPWM, respectively. The peak-to-peak envelopes calculated by (3.30) in case of SPWM, and (3.39) in case of SVM, as the half of peak-to-peak dc-link voltage ripple amplitude $\Delta v_{pp}/2(t)$ (red traces) are shown together with the instantaneous dc-link voltage switching ripple $\Delta v(t)$ (blue trace) over a fundamental period (T = 20 ms). Two values of the power phase angles $\varphi = 0°$ (left column in the Figs. 3.10 and 3.11) and $\varphi = 50°$ (right column in the Figs. 3.10 and 3.11) are considered and four sub-cases (a) - (d) correspond to different values of modulation index m: 0.25, 0.33, 0.5, and 0.577 (from top to bottom) when CPWM is applied, and m: 0.25, 0.33, 0.4, and 0.5 (from top to bottom) when SPWM is applied.

A good agreement between the analytically calculated dc-link voltage switching ripple envelopes and the simulated dc voltage ripple is shown for all considered cases, proving the effectiveness of the proposed analytical developments. Also, the behavior of the maximum peak-to-peak voltage switching ripple amplitude shown in Fig. 3.9 has been confirmed. It can be observed that, when the lower value of the modulation index (i.e. $m <$ 0.4) is considered, the global maximum decreases when the power phase angle increases. On contrary, if the maximum modulation index is considered, the voltage switching ripple reaches the maximum at the highest considered power phase angle.

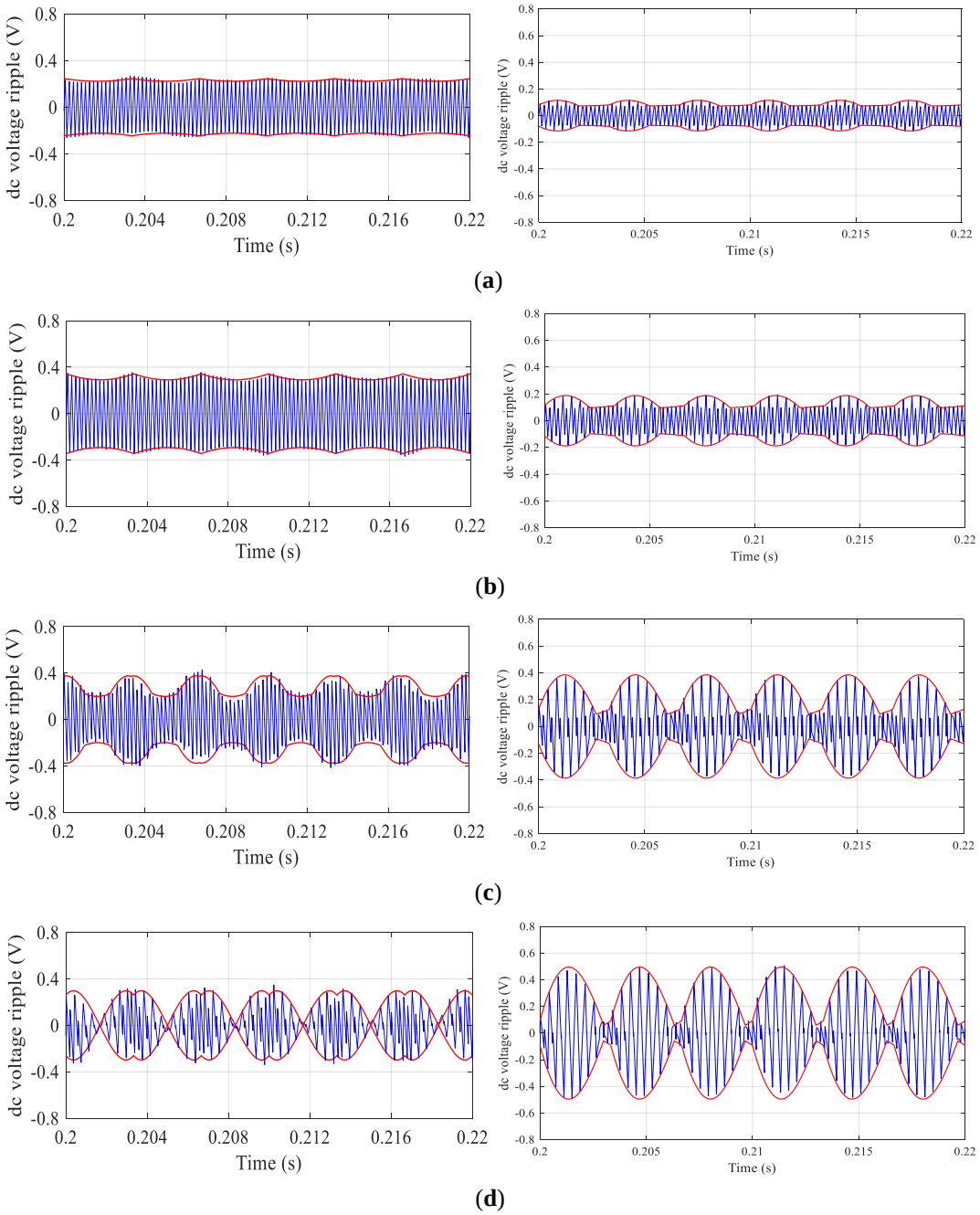


Fig. 3.10: Dc-link voltage switching ripple (SVM): simulation results (blue trace) and calculated peak-to-peak envelope (red trace) over a fundamental period for φ = 0° (left column) and φ = 50° (right column), (**a**) *m* = 0.25, (**b**) *m* = 0.33, (**c**) *m* = 0.5, and (**d**) *m* = 0.577.

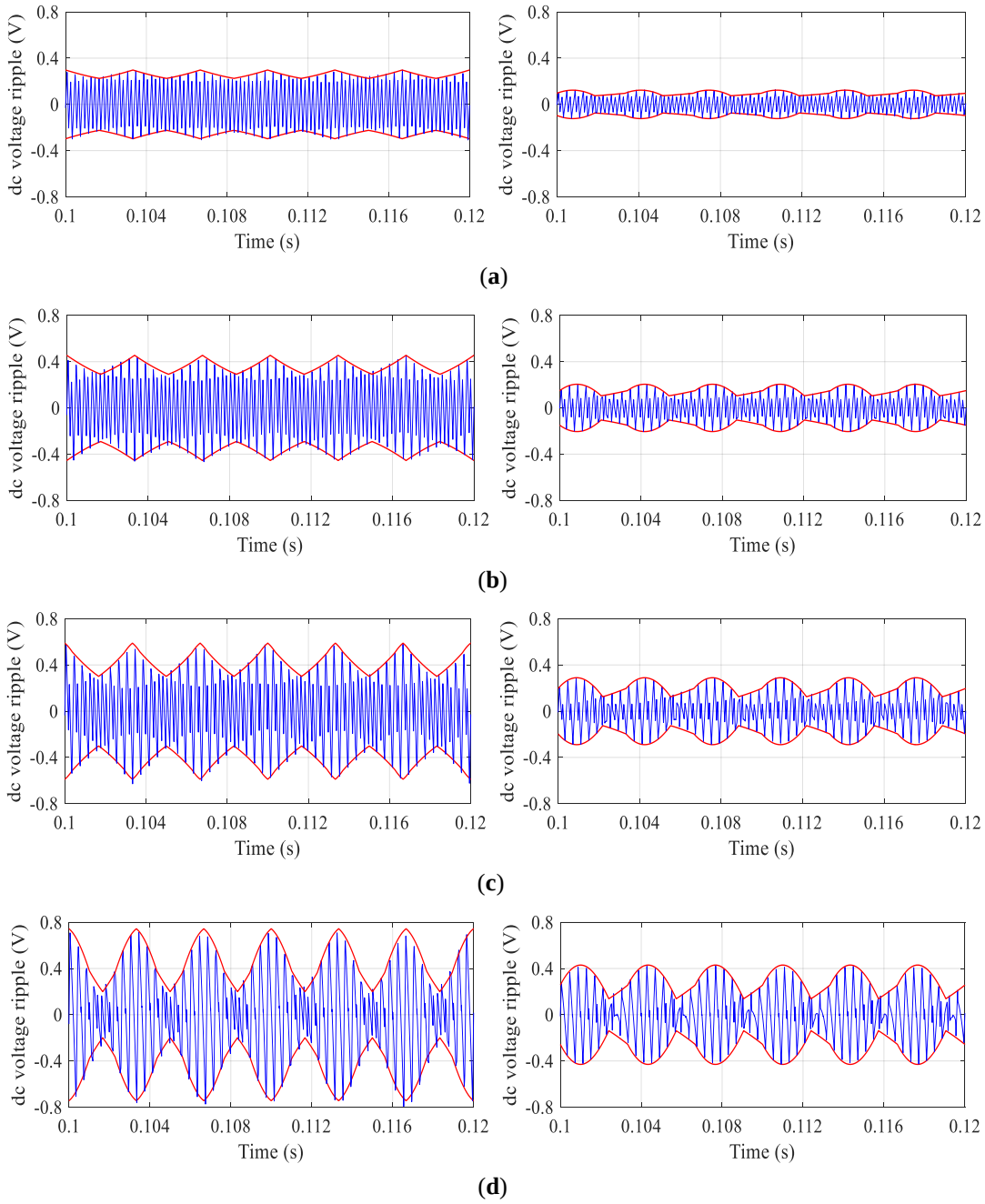


Fig. 3.11: Dc-link voltage switching ripple (SPWM): simulation results (blue trace) and calculated peak-to-peak envelope (red trace) over a fundamental period for φ = 0° (left column) and φ = 50° (right column), (**a**) m = 0.25, (**b**) m = 0.33, (**c**) m = 0.4, and (**d**) m = 0.5.

In order to prove both, theoretical developments and numerical results, experimental tests have been carried out. The whole experimental setup is shown in Fig. 3.12. The main hardware unit is the three-phase custom-made inverter with the Mitsubishi PS22A76 intelligent power IGBT module (1200V, 25A) which is controlled by the DSP microcontroller board. Control signals are transferred to the inverter through an optical interface board. DSP board TMS320F28379D is programmed by Code Composer Studio (CCS), with the possibility of real-time adjustment of modulation parameters by computer interface. For the voltage measurements a PICO TA057 differential probe (25MHz, ±1400V, ±2%) was used. For the current measurements a LEM PR30 current probe (DC to 20kHz, ±20A, ±1%) was used.

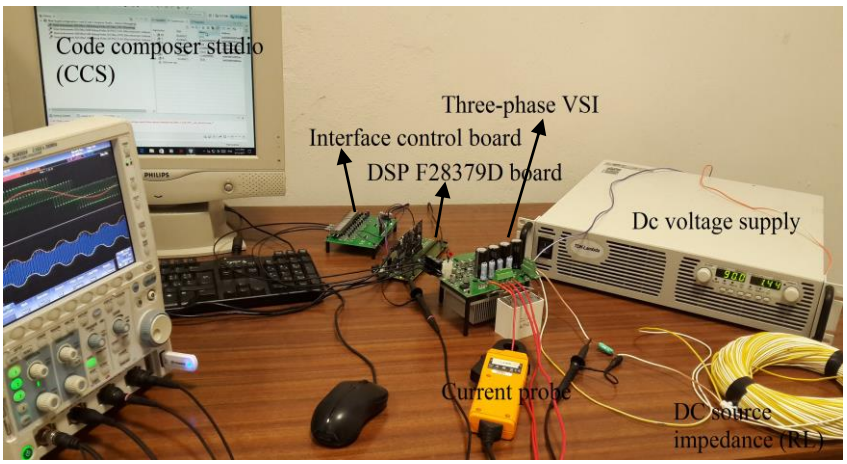


Fig. 3.12: Experimental setup.

For the experimental verification, two different power phase angles (φ = 0° and φ = 50°) are obtained using two different loads. Fig. 3.13 shows the electrical circuit scheme of the experimental load.

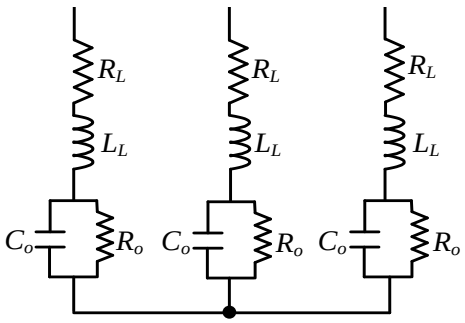


Fig. 3.13: Three-phase load circuit.

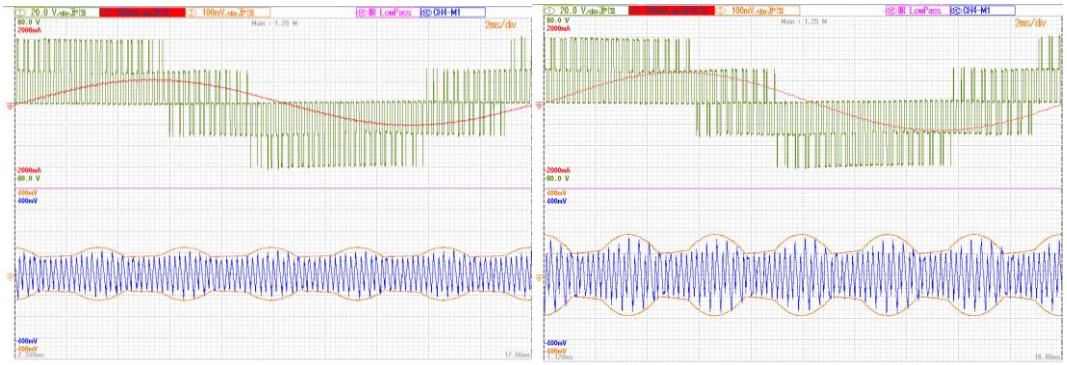
In the case of the power phase angle φ = 50°, 0.5 kW star-connected three-phase induction motor (at stand-still) is used having the following parameters: R_L=26.8 Ω and L_L=103 mH. In the case of the power phase angle φ = 0°, another 2.2 kW star-connected three-phase induction motor is used having R_L=3.16 Ω and L_L=20 mH per phase and adding in series to each phase a resistor R_0=20 Ω and a parallel capacitor C_0=58 μF in order to obtained the desired angle (φ = 0°) (at stand-still) which represents the grid-connected application. All load parameters are estimated using an AC power source/analyzer and direct measurements supplying the load by a 50 Hz three-phase balanced voltage source. Two three-phase motors can be seen in Fig. 3.14.

2.2 kW three-phase IM 0.5 kW three-phase IM

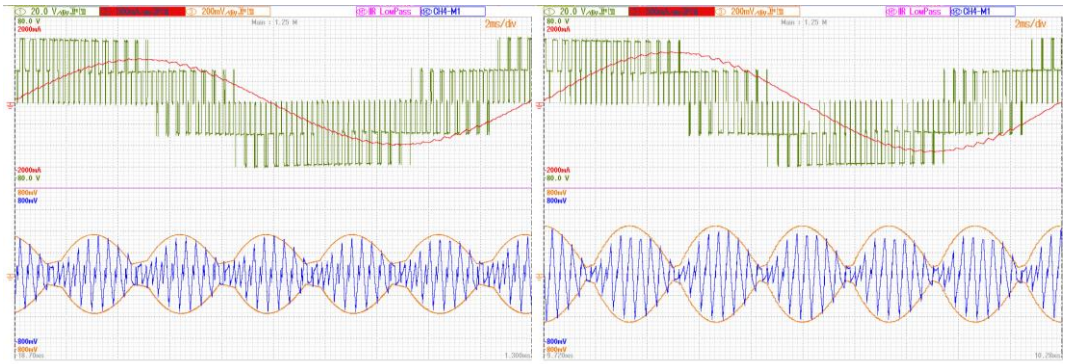
Fig. 3.14: Two three-phase IM

Experimental results are shown by Yokogawa DLM 2024 oscilloscope screenshots and collected in Fig. 3.15 and 3.16 in the case of SVM, and in Fig. 3.17 and 3.18 in the case of SPWM. Two values of the power phase angles φ = 50° (Fig. 3.15 and Fig. 3.17) and φ =0° (Fig. 3.16 and Fig. 3.18) and four values of modulation index are considered. In all screenshots, two upper traces present the load voltage and current (green and red traces, respectively) and the bottom (blue) trace presents the measured dc-link voltage switching ripple $\Delta v(t)$. The additional two orange traces present the calculated envelopes of the voltage ripple ($\Delta v_{pp}/2(t)$) provided by the DSP board and displayed using DAC block with a proper voltage scaling.

The switching ripple $\Delta v(t)$ has been obtained both numerically and experimentally by properly filtering the instantaneous dc-link voltage, according to (3.19). In case of experimental results the “ac coupling” function of the oscilloscope has been used together with a built-in second-order low-pass filter.

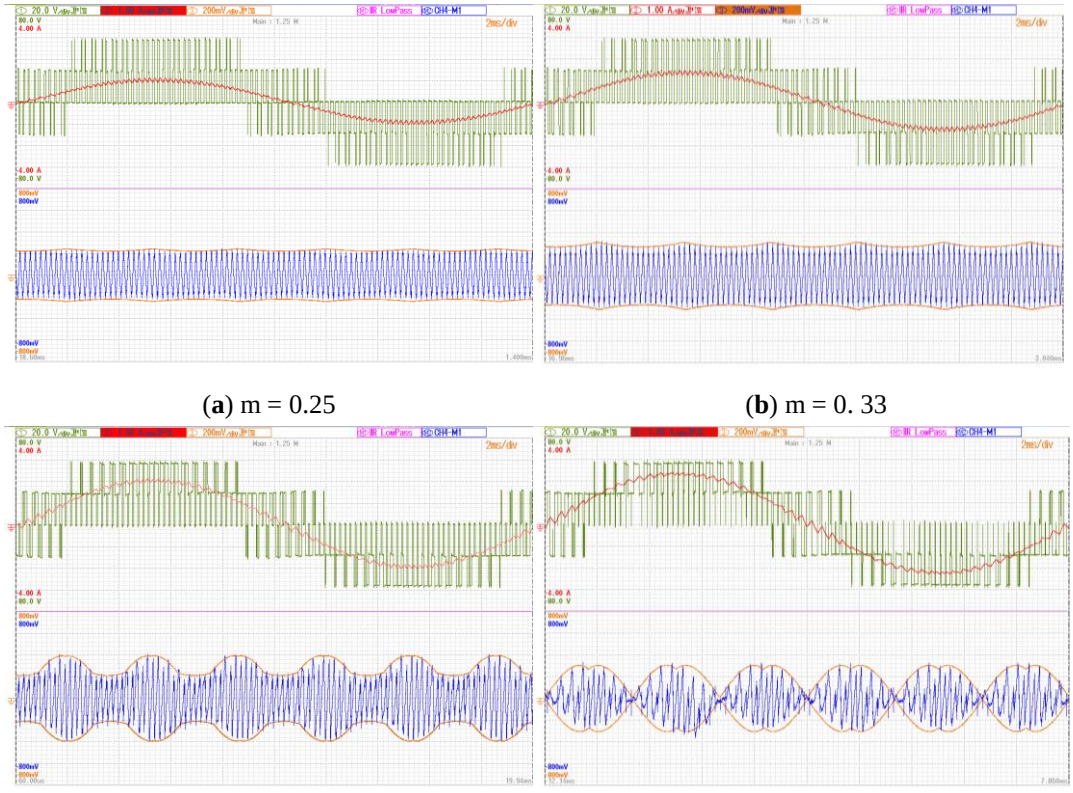


(**a**) m = 0.25 (**b**) m = 0. 33



(**c**) m = 0.5 (**d**) m = 0.577

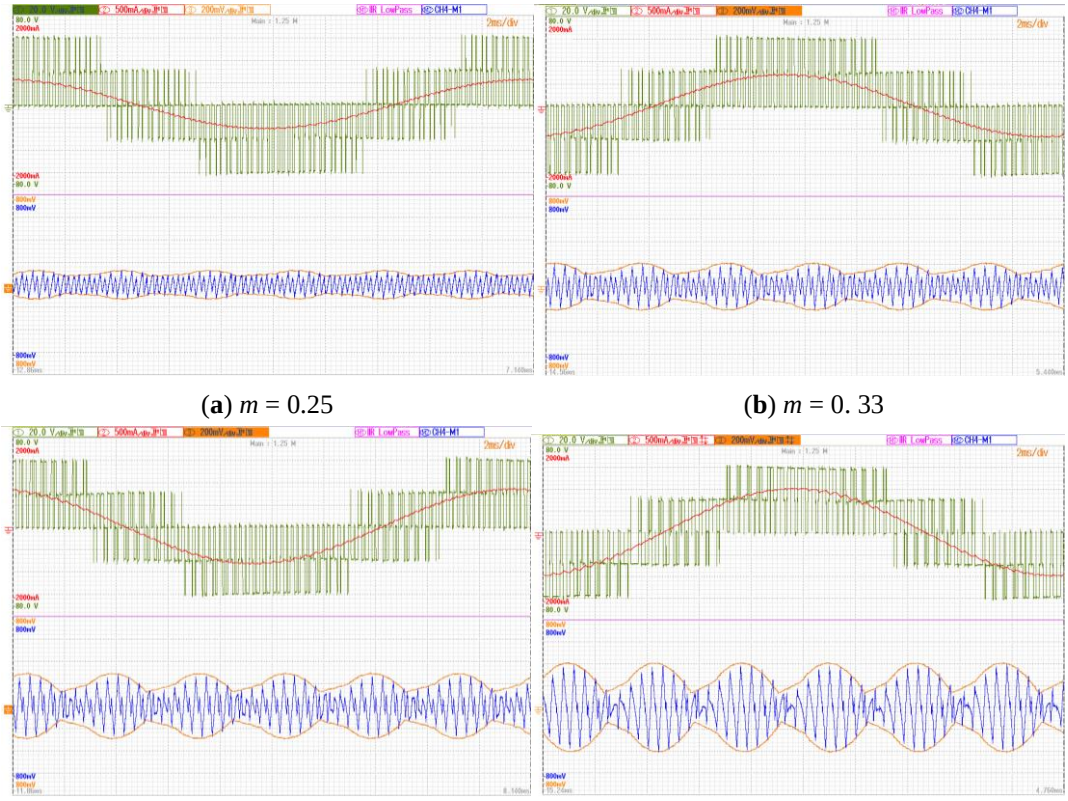
Fig. 3.15: Experimental results for φ = 50° (CPWM): upper half - output voltage and current, lower half – analytically calculated envelope and measured dc voltage switching ripple for (**a**) m = 0.25, (**b**) m = 0.33, (**c**) m = 0. 5, and (**d**) m = 0.577.



(**a**) m = 0.25 (**b**) m = 0. 33

(**c**) m = 0.5 (**d**) m = 0.577

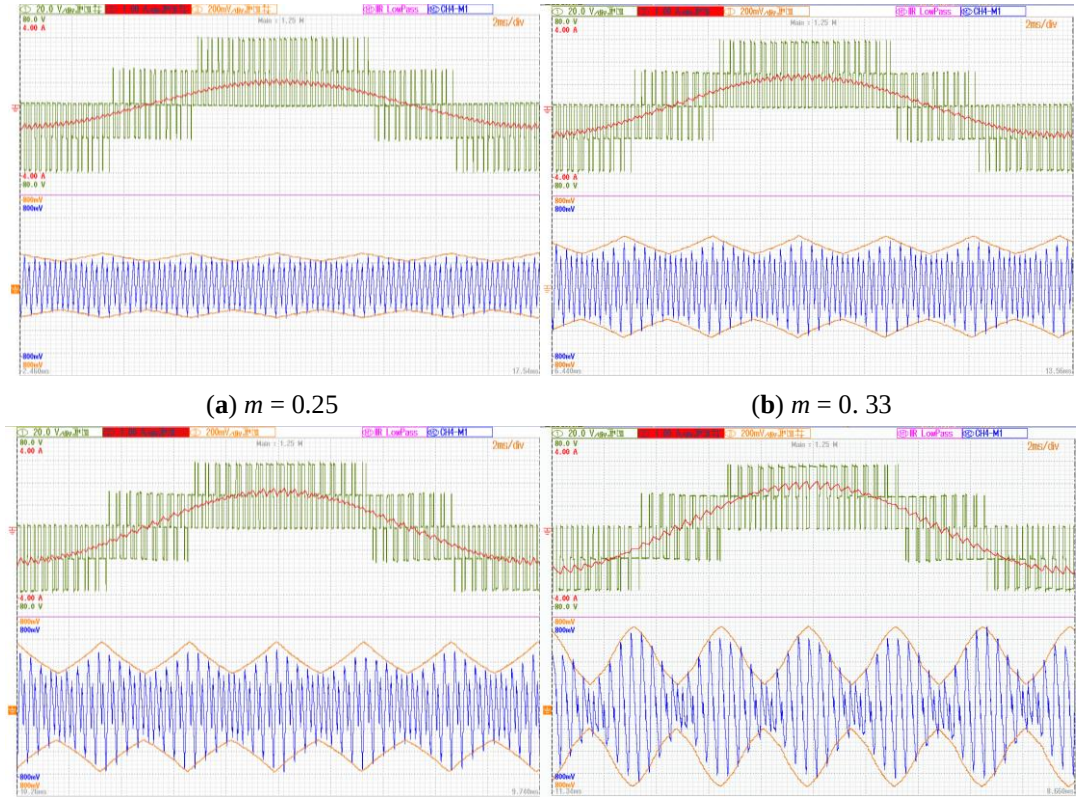
Fig. 3.16: Experimental results for φ = 0° (CPWM): upper half - output voltage and current, lower half – analytically calculated envelope and measured dc voltage switching ripple for (**a**) *m* = 0.25, (**b**) *m* = 0.33, (**c**) *m* = 0. 5, and (**d**) *m* = 0.577.



(**a**) m = 0.25 (**b**) m = 0. 33

(**c**) m = 0.4 (**d**) m = 0.5

Fig. 3.17: Experimental results for φ = 50° (SPWM): upper half - output voltage and current, lower half – analytically calculated envelope and measured dc voltage switching ripple for (**a**) m = 0.25, (**b**) m = 0.33, (**c**) m = 0. 4, and (**d**) m = 0.5.



(**a**) m = 0.25 (**b**) m = 0. 33

(**c**) m = 0.4 (**d**) m = 0.5

Fig. 3.18: Experimental results for φ = 0° (SPWM): upper half - output voltage and current, lower half – analytically calculated envelope and measured dc voltage switching ripple for (**a**) m = 0.25, (**b**) m = 0.33, (**c**) m = 0. 4, and (**d**) m = 0.5.

Experimentally obtained results show good matching between theoretically calculated envelopes and peak-to peak dc-link voltage ripple for all considered cases of modulation indices and power phase angles, proving the effectiveness of the proposed approach.

3.7 Discussion

In this chapter, dc-link current and voltage ripple analysis is presented for two-level three-phase voltage source inverters with balanced load. A short review of carrier-based and space vector PWM for three-phase inverters is provided. The dc-link voltage ripple components are calculated on the basis of the corresponding dc-link current components. The voltage switching ripple amplitude has been derived for two modulation techniques – sinusoidal and centered ("min-max" injection, equivalent to SVM) PWM as a function of operational conditions: modulation index, phase current and power phase angle. The maximum (peak-to-peak) value of voltage ripple amplitude has been evaluated as a function of modulation index for different power phase angles. The comparison between different cases has been made in terms of different operational conditions and applied modulation techniques. Simple and effective expressions for the dc-link capacitor design are proposed based on the maximum dc-link voltage switching ripple amplitude.

Simulations and experimental results for both SPWM and CPWM, considering two power phase angles and different values of modulation index, are given. Given results are aimed to show the matching between analytically calculated dc-link voltage ripple envelope and measured instantaneous dc-link voltage switching ripple. The comparison of dc-link voltage switching ripple between different phase numbers will be given in Chapter 4.

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Chapter 4

Dc-link current and voltage switching ripple analysis in multiphase inverters

4.1 Introduction

The area of multiphase machines (machines with the number of phases greater than three) has gained widespread attention in the last decade. The interest in multiphase machines is rising due to some very specific applications, such as electric and hybrid electric vehicles (EVs), railway traction, ship propulsion, "more-electric" aircraft, remote offshore wind farms for electric energy generation, and the high-power industrial applications (rolling mills, compressors etc). The main reason for utilization of multiphase machines in these applications is the existence of additional degrees of freedom when compared to their three-phase counterparts. The "classical" use of additional degrees of freedom are torque enhancement using low-order stator current harmonic injection and fault-tolerant operation. In addition, the possibility of splitting the motor power across a higher number of phases enables a reduction in the voltage/current rating of power semiconductors of the converters which are used to drive multiphase machines. A comprehensive survey of multiphase machines, covering their basic characteristics, types and variety, advantages over their three-phase counterparts, modelling, vector control, direct torque control, PWM control of multiphase inverters, postfault operating strategies, multiphase multi-motor drive systems, etc. are available in [4.1] and [4.2]. The latest contributions and significant new research results in the multiphase machines' field is available in [4.3], [4.4] and [4.5]. The focus is on innovative uses of the additional degrees of freedom of multiphase drives.

Multiphase machines are predominantly based on utilization of two-level multiphase voltage source inverters with equal number of phases. In order to fully exploit the potential of inverter-fed multiphase machines, a suitable modulation strategy has to be applied. As for the three-phase case, two most common modulation techniques for multiphase inverters are carrier-based PWM (CBPWM) and space vector PWM (SVPWM). The extension from three- to multi- phase VSIs is simple and rather straightforward in case of CBPWM techniques. The improvement of the dc-bus utilization can be easily achieved by appropriate zero-sequence injection into leg voltage references. However, as the number of phases in-

creases, the improvement rapidly reduces. Unlike CBPWM, the application of SVPWM becomes more complicated when the number of phases increase. Space vector PWM methods for symmetrical multiphase machines with an odd number of phases have been extensively discussed in the literature. A generic SVPWM algorithm, applicable to two-level multiphase VSIs, where the number of phases is an odd number, has been presented in [4.8]. Feasibility of generalization has been verified for five-, seven- and nine-phase systems. A comprehensive relationship between SVPWM and CBPWM, followed by the practical implementation issues is provided in [4.9].

Recently, the research focus in the area of multiphase inverters has been placed on the output side of inverters. The output current ripple is studied in terms of RMS minimization and its maximum peak-to-peak value. Referring to two-level five-phase VSIs, the analytical study of the output current ripple RMS, based on space vector theory has been presented in [4.10]. Three different modulation techniques, aimed at sinusoidal output generation, are compared and the results show that, in terms of the output current ripple RMS, the best modulation technique is the sinusoidal PWM. The superiority of the sinusoidal PWM in balanced sinusoidal operating conditions has been confirmed for an odd number of phases in [4.11] using so called "polygon approach". In [4.12], the zero-sequence component of the modulating signals is optimized in each switching period leading to the minimization of the output current ripple for any output voltage waveform. Furthermore, the comparison among several continuous and discontinuous modulation techniques, in terms of output current ripple, has been made and SVPWM shows the nearly-optimal behavior in each operating condition. The analysis related to the output current ripple peak-to-peak value in five-phase inverters has been presented in [4.13], where the peak-to-peak current ripple amplitude is analytically determined as a function of the modulation index, and a simplified expression for its maximum value is obtained. An extension of the analysis and an experimental verification is provided in [4.14]. A further extension to the seven-phase case and derivation of the peak-to-peak current ripple amplitude as a function of modulation index is given in [4.15]. A similar idea is presented in [4.16], where the current ripple prediction method for multiphase PWM converters is proposed based on the equivalent single-phase circuit.

Analysis of input current and dc-link voltage, presented so far, mainly refers to two-level three-phase inverters. However, the input (dc-link) side of multiphase inverters has not been investigated widely. With reference to five-phase inverters, RMS calculations of input current and voltage ripple have been reported in [4.17]. Different modulation techniques are considered and no dependency of the RMS value of the inverter input current ripple on the selected PWM scheme has been shown. It has been shown in [4.18] for a square-wave VSI control that the RMS value of the dc-link current can be decreased by increasing the number of phases. Comparison of square-wave and a PWM control through spectral analysis is conducted for a seven-phase drive. The impact of classical PWM mod-

ulation, with and without common mode injection on the RMS value of the dc current has been studied in [4.19] for dual-three phase induction machine. A PWM strategy dedicated to minimization of the RMS of the dc-link current in dual three-phase drive has been compared in [4.20] with more conventional PWM techniques. It has been shown that PWM strategies have different effect on the RMS of the dc current and on the quality of the output current. However, both constraints must be considered for the dc-link capacitor sizing. The RMS calculations of input current ripple in nine-phase PWM inverter are carried out in [4.21]. Referring to a six-phase drive system, the RMS value of the input current ripple is derived in [4.22]. As an alternative solution to six-phase drive system, double winding and dual inverter fed ac drive systems are considered and the input current ripple is compared among several modulations. In [4.23] is shown that the input current ripple can be reduced by increasing the phase number from three to five. However, when the phase number is higher than nine no significant reduction of the input current ripple is achieved.

As it can be noted, the analysis of the dc-link current and voltage ripple in multiphase inverters is mostly based on the RMS calculations. In this chapter, the dc-link voltage switching ripple in two-level multiphase VSIs with balanced load, where the number of phases is an odd number greater than three, is evaluated in terms of the maximum (peak-to-peak) value. Two most popular PWM techniques – sinusoidal and space vector PWM are applied and compared. A short review of both modulations is given in section 4.2. The theoretical analysis of the inverter's dc-link current is presented in section 4.3 for general *n*-phase case. The voltage ripple is evaluated in section 4.4 and the focus is placed on five- and seven- phase two-level VSIs. The comparison of voltage switching ripple for higher number of phases is made in section 4.5 in terms of the voltage ripple envelope and its maximum value. Dc-link voltage switching ripple requirements are further used for the dc-link capacitor design. Simulations and experimental results are included in section 4.6. Finally, a brief discussion of obtained results is given in section 4.7.

The content of this chapter, based on theoretical analysis and experimental results, has been used in [4.28] and [4.29].

4.2 Modulation techniques

For the dc-link voltage ripple evaluation that follows, a brief review of sinusoidal PWM (SPWM) and space vector modulation (SVM) for multiphase VSIs is given. The multiphase (*n*-phase, *n* is considered as an add number) VSI topology supplying a star-connected balanced passive- or motor-load is presented in Fig. 4.1. The inverter is supplied by a dc voltage source (V_{dc}) via an equivalent series dc source impedance Z_{dc}, representing an inductive filter (L) and/or an equivalent series resistance (R).

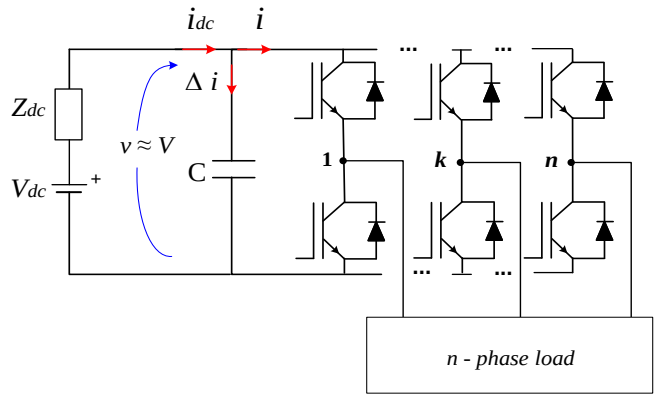

Fig. 4.1: Circuit scheme of *n*-phase voltage source inverter.

Carrier-based PWM

For reason of simplicity, sinusoidal PWM is introduced first. According to Fig. 3.1, the zero-sequence signal is set to zero to obtain SPWM. The *n* reference signals become equal to the sinusoidal fundamental signals, displaced in time by $2\pi/n$ degrees as

$$v_k^*(t) = mV\cos\left(\vartheta - (k-1)\frac{2\pi}{n}\right), k = 1, 2, \ldots n. \tag{4.1}$$

In the following, two multiphase inverter topologies are analyzed, five- and seven-phase two-level inverters. Fig. 4.2 shows reference signals of (4.1) for five-phase case compared with the triangle carrier waveforms, for one fundamental period and for modulation index set as m=0.5.

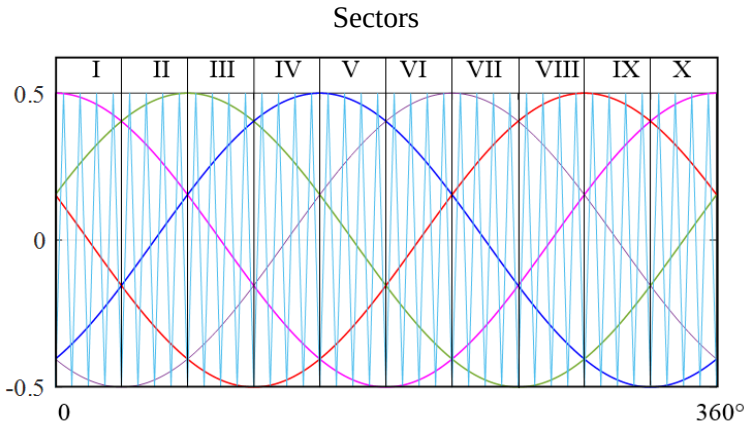

Fig. 4.2: Reference signals for five-phase VSIs over one fundamental period (SPWM).

It is noticeable that fundamental period can be divided into 10 sectors, each spanning $\pi/5$ degrees. Considering the first sector, as an example, Fig. 4.3 shows five reference signals over one switching period (T_{sw}) together with a carrier signal, and generated PWM switching patterns (switching functions).

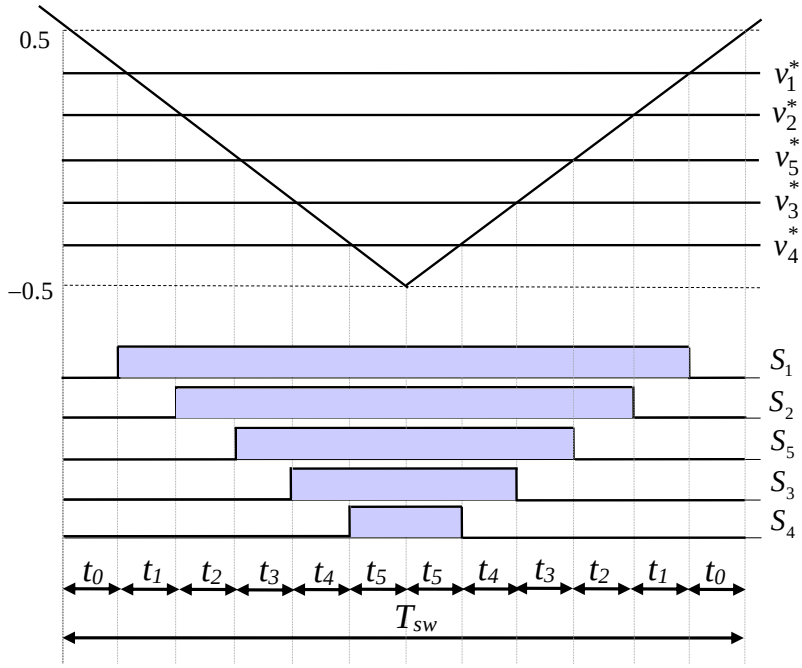

Fig. 4.3: Principle of generation of switching pattern for five-phase VSIs.

The application times t_k, k=0,1,..5 can be calculated based on Fig. 4.3 and by means of simple trigonometry as:

$$t_0 = \frac{T_{sw}}{2}\left(\frac{1}{2} - m\cos(\vartheta)\right), \tag{4.2}$$

$$t_1 = mT_{sw}\sin\left(\frac{\pi}{5}\right)\sin\left(\frac{\pi}{5} - \vartheta\right), \tag{4.3}$$

$$t_2 = mT_{sw}\sin\left(\frac{2\pi}{5}\right)\sin(\vartheta), \tag{4.4}$$

$$t_3 = mT_{sw}\sin\left(\frac{2\pi}{5}\right)\sin\left(\frac{\pi}{5} - \vartheta\right), \tag{4.5}$$

$$t_4 = mT_{sw}\sin\left(\frac{\pi}{5}\right)\sin(\vartheta), \tag{4.6}$$

$$t_5 = \frac{T_{sw}}{2}\left(\frac{1}{2} - m\cos\left(\frac{\pi}{5} - \vartheta\right)\right). \tag{4.7}$$

According to Fig. 3.1, centered PWM (CPWM) can be achieved by adding to the five sinusoidal reference signals the zero-sequence signal expressed as:

$$v_z(t) = -0.5\left(v^*_{\max} + v^*_{\min}\right) \tag{4.8}$$

Comparing to the SPWM, an increase of around 5.15% in the dc bus utilization, in the linear modulation region, is achieved if CPWM is applied to five-phase system. Thus, the modulation limit is m_{max}=0.526. The effect of a "min-max" injection is shown in Fig. 4.4 where five reference signals are shown over one fundamental period.

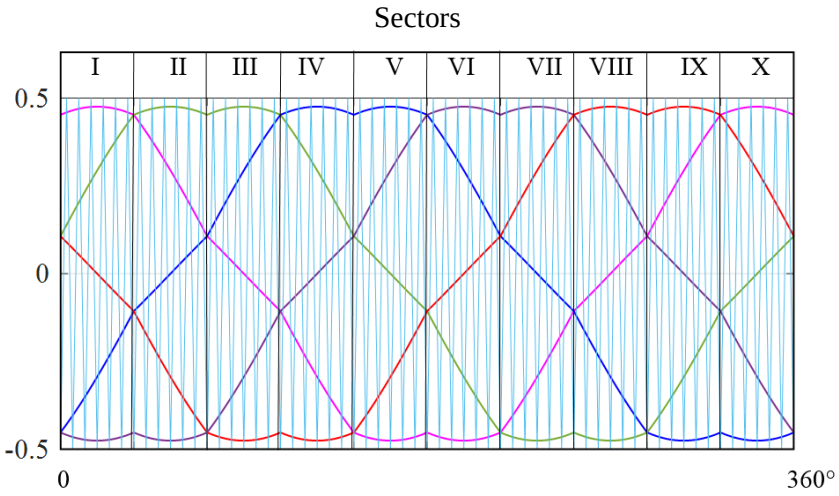

Fig. 4.4: Reference signals for five-phase VSIs over one fundamental period (CPWM).

It can be noted that after the injection (Fig. 4.4) the ordering of the reference signals remains the same as before injection (Fig. 4.2). Thus, keeping in mind that with high enough switching frequency those reference signals are still constant during one carrier period, it can be concluded that the switching sequences (and so, the application times) of the active space vectors will be the same as in case of SPWM. The difference is in the application times of two zero space vectors. Based on (4.1), (4.8) and Sector 1 (Fig. 4.4), the application times of two zero space vectors are calculated as:

$$t_0 = \frac{T_{sw}}{2}\left[\frac{1}{2} - m\cos(\vartheta) + \frac{1}{2}\left(m\cos(\vartheta) + m\cos\left(\vartheta - \frac{8\pi}{5}\right)\right)\right], \tag{4.9}$$

$$t_3 = \frac{T_{sw}}{2}\left[\frac{1}{2} + m\cos\left(\vartheta - \frac{8\pi}{5}\right) - \frac{1}{2}\left(m\cos(\vartheta) + m\cos\left(\vartheta - \frac{8\pi}{5}\right)\right)\right]. \tag{4.10}$$

Applying basic trigonometric equations, the following simplification is obtained:

$$\begin{aligned} t_0 = t_5 &= \frac{T_{sw}}{2} - (t_1 + t_2 + t_3 + t_4) = \\ &= \frac{T_{sw}}{2}\left[1 - m\left(1 + \cos\left(\frac{\pi}{5}\right)\right)\cos\vartheta - m\sin\left(\frac{\pi}{5}\right)\sin\vartheta\right]. \end{aligned} \tag{4.11}$$

Similarly to the five-phase case, Fig. 4.5 shows reference signals of (4.1) for seven-phase case compared with the triangle carrier waveforms, for one fundamental period and for modulation index set as m=0.5. It is noticeable that in this case fundamental period can be divided into 14 sectors, each spanning π/7 degrees.

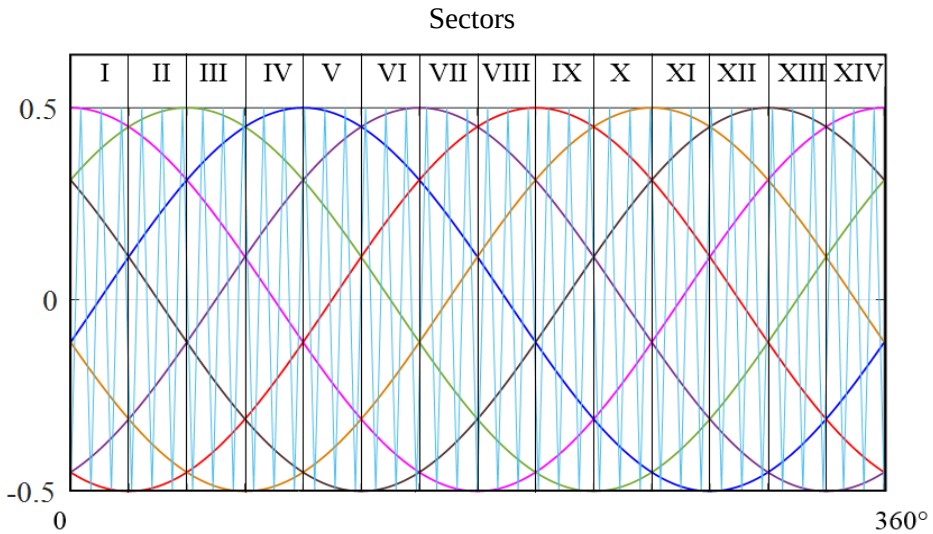

Fig. 4.5: Reference signals for seven-phase VSIs over one fundamental period (SPWM).

Assuming the same (high) ratio of the switching over fundamental frequency as before, and considering the first sector as an example, Fig. 4.6 shows seven reference signals over one switching period (T_{sw}) together with a carrier signal, and generated PWM switching patterns (switching functions).

The application times t_k, k=0,1,..7 can be calculated similarly to the case of five-phase inverters, referring to Fig. 4.6 and by means of simple trigonometry as:

$$t_0 = \frac{T_{sw}}{2}\left(\frac{1}{2} - m\cos(\vartheta)\right), \tag{4.12}$$

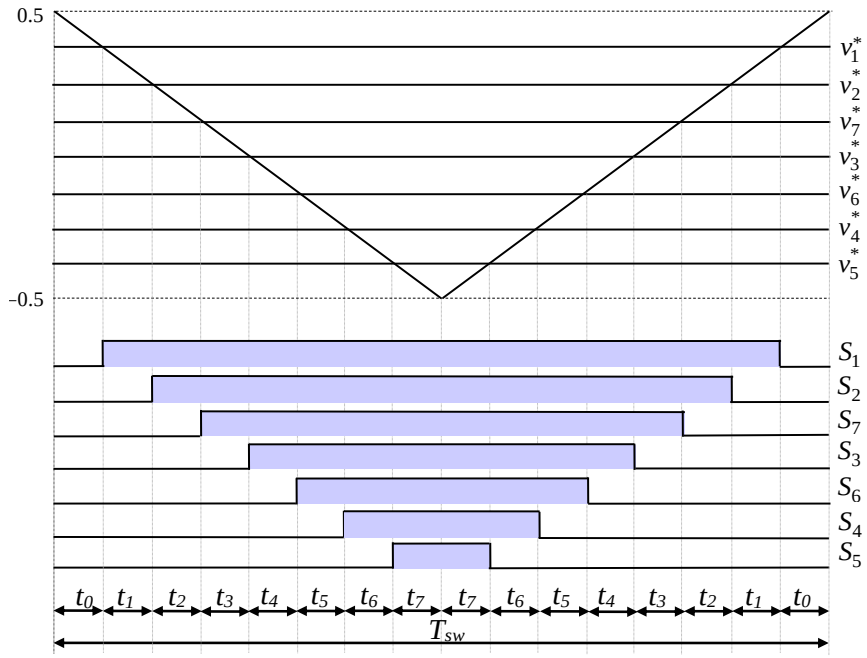

Fig. 4.6: Principle of generation of switching pattern for seven-phase VSIs.

$$t_1 = mT_{sw}\sin\left(\frac{\pi}{7}\right)\sin\left(\frac{\pi}{7}-\vartheta\right), \tag{4.13}$$

$$t_2 = mT_{sw}\sin\left(\frac{5\pi}{7}\right)\sin\left(\vartheta\right), \tag{4.14}$$

$$t_3 = mT_{sw}\sin\left(\frac{3\pi}{7}\right)\sin\left(\frac{\pi}{7}-\vartheta\right), \tag{4.15}$$

$$t_4 = mT_{sw}\sin\left(\frac{3\pi}{7}\right)\sin\left(\vartheta\right), \tag{4.16}$$

$$t_5 = mT_{sw}\sin\left(\frac{5\pi}{7}\right)\sin\left(\frac{\pi}{7}-\vartheta\right), \tag{4.17}$$

$$t_6 = mT_{sw}\sin\left(\frac{5\pi}{7}\right)\sin\left(\frac{\pi}{7}-\vartheta\right), \tag{4.18}$$

$$t_7 = \frac{T_{sw}}{2}\left(\frac{1}{2}-m\cos\left(\frac{\pi}{7}-\vartheta\right)\right). \tag{4.19}$$

Centered PWM (CPWM) can be achieved by adding to the seven sinusoidal reference signals the zero-sequence signal given by (4.8). An increase of around 2.57% in the DC bus utilization, in the linear modulation region, is achieved comparing to the SPWM [4.26]. Thus, in case of seven-phase VSIs, the modulation limit is m_{max}=0.513. The effect of a "min-max" injection is shown in Fig. 4.7 where seven reference signals are shown over one fundamental period.

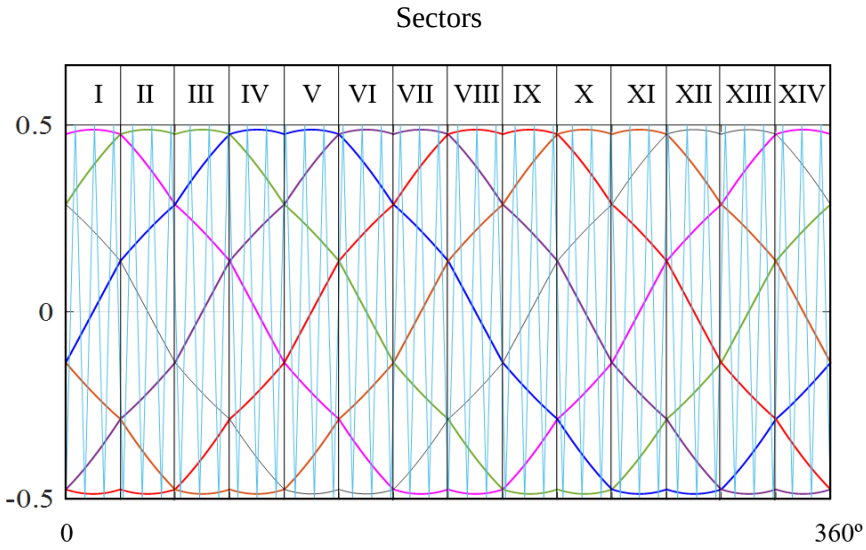

Fig. 4.7: Reference signals for seven-phase VSIs over one fundamental period (CPWM).

As in the five-phase case, the switching sequences (and so, the application times) of the active space vectors, in the first sector, are identical to those given by (4.13) - (4.18) for SPWM. The difference is in the application times of two zero space vectors which are finally calculated as:

$$t_o = t_7 = \frac{T_{sw}}{2} - \left(t_1 + t_2 + t_3 + t_4 + t_5 + t_6\right) = \\ = \frac{T_{sw}}{2}\left[1 - 2m\left(\sin\left(\pi/7\right) + \sin\left(3\pi/7\right) + \sin\left(5\pi/7\right)\right)\left(\sin\left(\pi/7\right)\cos\left(\vartheta\right) + \left(1 - \cos\left(\pi/7\right)\sin\left(\vartheta\right)\right)\right)\right] \quad (4.20)$$

Space vector modulation

Due to the large number of space vectors in multiphase machines there is a lot of flexibility in choosing the proper combination of them. SVPWM method for a symmetrical five-phase machine was first presented in [4.6]. By combining the utilization of two large and two medium length neighbouring space vectors sinusoidal output voltages are obtained without any low-order harmonics. The same dwell times, although calculated in a different way, are obtained in [4.7]. Different schemes based on use of only large active space vec-

tors, two or four per switching period, have been reported as well, but no one of these methods is optimal in the sense of easy implementation and switching losses.

Space vectors in a two-level five-phase VSI can be projected into two two-dimensional sub-spaces or planes. There are 2^5=32 voltage space vectors, comprising of 30 active vectors and 2 zero vectors, and each of them appears in both planes simultaneously. However, in order to generate sinusoidal output voltages, it is enough to apply four active space vectors over a switching period. These are usually two large and two medium neighboring vectors used to reach the reference in the given sector of the first plane. These active space vectors are applied with the times of applications that provide automatically zero average voltage in the second plane. Such times of application of active space vectors can be calculated from the set of fundamental sinusoidal signals and are equal to those given by (4.3) - (4.6). The most commonly adopted - equal distribution of the application times of the zero space vectors is considered leading again to the same expression for zero space vectors time of application as the one given by (4.11). The limit of the linear modulation range is $m \leq m_{\max} \approx 0.526$, where m_{max} is given according to the generalized expression for n phases, (n is odd number) $m_{max} = 1 / [2 \cos(\pi/2n)]$. [4.24]

Fig. 4.8 represents the ten output voltage space vectors in planes α_1-β_1 and α_3-β_3, corresponding to all possible switching configurations.

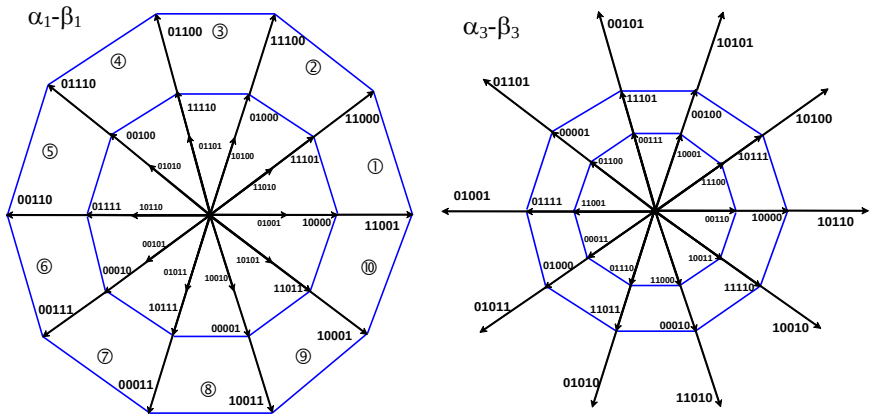

Fig. 4.8: Space vector diagram of five-phase inverter output voltage [4.14]

The SVM for a seven-phase VSIs was first introduced in [4.25]. In [4.26], a set of continuous PWM methods for sinusoidal output voltage generation is presented. The Duty-Cycle Space Vector (DCSV) approach, which combines the multiple space vector representation with traditional carrier-based PWM principle is presented in [4.27].

In seven-phase VSIs there are 2^7=128 voltage space vectors which are obtained in three two-dimensional planes. Each vector has a unique appearance in all three planes except for the zero space vectors which appear originally in all planes. However, to generate

sinusoidal output voltages it is enough to apply six active space vectors over a switching period. The application times of active space vectors are calculated in the way to achieve the cancellation of the 5th and 3rd harmonics, in the 2nd and 3rd plane, respectively. Such times of application of active space vectors are obtained from the set of fundamental sinusoidal signals and are equal to those given by (4.13) - (4.18). The most commonly adopted - equal distribution of the application times of the zero space vectors is considered leading again to the same expression for zero space vectors time of application as the one given by (4.20). Dc bus utilization is increased by 2.57% compared to SPWM and so, the limit of the linear modulation range is $m \leq m_{\max} \approx 0.513$, where m_{max} is given according to the generalized expression for n phases, (n is odd number) $m_{max} = 1 / [2 \cos(\pi/2n)]$. [4.24]

Fig. 4.9 represents the fourteen output voltage space vectors in the planes α_1-β_1, α_3-β_3 and α_5-β_5, corresponding to all possible switching configurations.

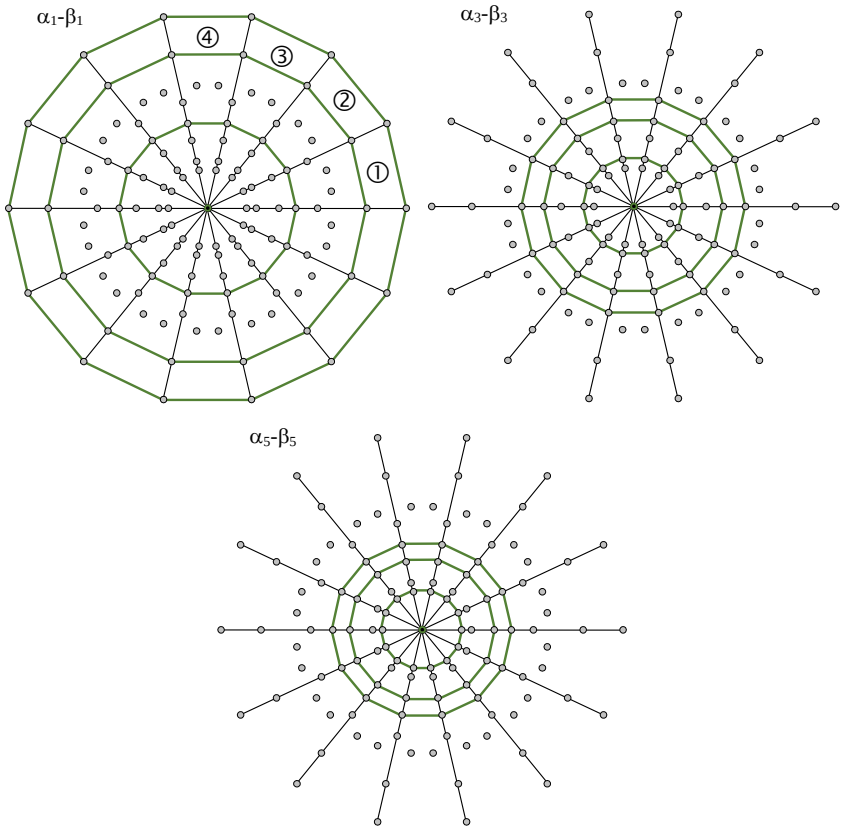

Fig. 4.9: Space vector diagram of seven-phase inverter output voltage. [4.15]

4.3 Dc-link current analysis

Considering that the inverter output phase voltages averaged over the switching period correspond to the reference phase voltages given by (4.1), in case of balanced load and neglecting the output current ripple, the corresponding *n*-phase sinusoidal output currents can be written as:

$$i_k = I_0 \cos\left(\vartheta - (k-1)\frac{2\pi}{n} - \varphi\right),\ k = 1, 2, ...n, \tag{4.21}$$

where I_0 is the output current amplitude and φ is the phase angle between the phase voltage and current.

The instantaneous input current $i(t)$ can be generally expressed by three components: dc (average) component $I = I_{dc}$, low-frequency component and high-frequency (switching frequency) component $\Delta i(t)$. Considering balanced load conditions, the low-frequency component is zero and the inverter input current contains only the dc (average) and the high frequency component, written as:

$$i(t) = I_{dc} + \Delta i(t)\,. \tag{4.22}$$

Under the assumption of the ideal power switches, the input current averaged over the switching period T_{sw} can be obtained based on the input/output power balance. Therefore, the average input current is given by:

$$I_{dc} = \frac{m}{2} n I_0 \cos\varphi\,. \tag{4.23}$$

The input current is the sum of *n* inverter leg currents. Each leg current can be calculated from the binary switching function S_k = [0, 1], k = 1, 2, .., n (where '1'/'0' corresponds to the 'on'/'off' state of the upper switch in particular leg), and corresponding output current. Consequently, the input current can be expressed as:

$$i = \sum_{k=1}^{n} S_k i_k\,. \tag{4.24}$$

The switching frequency input current component can be easily calculated utilizing equations (4.22) – (4.24) as:

$$\Delta i(t) = i(t) - I_{dc} = \sum_{k=1}^{n} S_k i_k - \frac{m}{2} n I_0 \cos\varphi\,. \tag{4.25}$$

Due to the symmetry of the inverter input current waveforms, the analysis can be limited to 1/2n of the fundamental period (T/2n), i.e. first π/n radians.

4.4 Dc-link voltage ripple analysis

As already emphasized in section 3.4, the dc-link voltage can be decomposed in three components. Calculation of the peak-to-peak amplitude of the switching frequency dc-link voltage ripple component Δv_{pp} is of the main interest in this chapter. It can be defined as the difference between the maximum and the minimum value of the voltage ripple within the switching period:

$$\Delta v_{pp} = \max\left\{\Delta v(t)\right\}_{T_{sw}} - \min\left\{\Delta v(t)\right\}_{T_{sw}}. \tag{4.26}$$

Assuming that the reactance $1/(2\pi f_{sw}C)$ of the dc-link capacitor C is much smaller comparing to the equivalent dc source impedance Z_{dc} calculated at the switching frequency (f_{sw}=1/T_{sw}), the whole Δi can be supposed circulating only through the dc-link capacitor. The voltage excursion can be calculated within each application interval t_k (determined in section 4.2 for SPWM and SVM) based on the equation for the voltage drop over capacitor and considering Δi constant within the considered interval:

$$\Delta v_{pp}^{k} = \frac{1}{C}\Delta i\ t_k. \tag{4.27}$$

The global peak-to-peak dc-link voltage ripple amplitude Δv_{pp} is finally obtained by combining different Δv_{pp}^{k} and finding the maximum within the switching period.

Due to the periodicity of the input current $i(t)$ waveform, the evaluation of the voltage ripple can be also reduced to the phase angle range $0 \le \vartheta \le \pi/n$ (corresponding to the first sector in Fig. 4.5). Within the first sector, depending on the value of $I_{dc,}$ n-1 different cases can be distinguished.

In order to analytically determine the dc-link peak-to-peak voltage switching ripple amplitude, two different multiphase schemes are further addressed. In particular, five-phase and seven-phase VSI topologies are analyzed next.

4.4.1 Five-phase inverter

Two different modulation strategies have been applied in the following analysis and the dc-link voltage switching ripple for five-phase inverter is investigated under the two of them. Some remarks on the influence of modulation technique on the voltage switching ripple distribution follow as well.

4.4.1.1 Peak-to-peak voltage switching ripple with sinusoidal PWM

In Fig. 4.10 the peak-to-peak dc-link voltage variations Δv_{pp}^{k} and the instantaneous input current $i(t)$ (red staircase line) are depicted in one switching period. Note that Fig. 4.10 presents just an example of possible current and voltage ripple waveforms. In general, the instantaneous input current $i(t)$ is calculated by (4.22). In order to cover all the possible input current profiles, the *max* function is finally applied to the calculated voltage ripple variations as it will be shown in the following.

Depending on the value of I_{dc}, and if SPWM is applied ($t_0 \neq t_5$), five different cases can be distinguished:

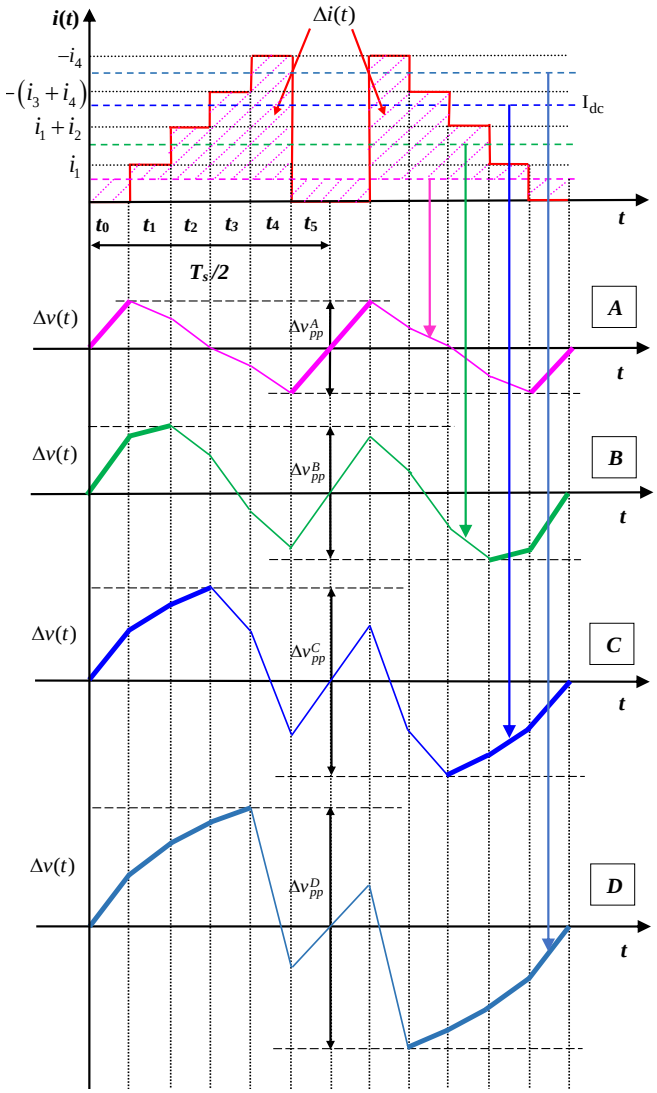

Fig. 4.10: Dc-link current and voltage ripple in one switching period for five-phase VSIs.

- case A: when $i_1 \geq I_{dc}$,
- case B: when $i_1 \leq I_{dc} < i_1+i_2$,
- case C: when $i_1+i_2 \leq I_{dc} < -(i_3+i_4)$,
- case D: when $-(i_3+i_4) \leq I_{dc} < -i_4$,
- case E: when $i_1 \geq I_{dc}$.

According to Fig. 4.10, corresponding peak-to-peak dc-link voltage variations can be expressed as:

$$\Delta v_{pp}^{A} = \frac{1}{C} I_{dc} 2t_0, \tag{4.28}$$

$$\Delta v_{pp}^{B} = \Delta v_{pp}^{A} + \frac{1}{C}(I_{dc} - i_1) 2t_1, \tag{4.29}$$

$$\Delta v_{pp}^{C} = \Delta v_{pp}^{B} + \frac{1}{C}(I_{dc} - i_1 - i_2) 2t_2, \tag{4.30}$$

$$\Delta v_{pp}^{D} = \Delta v_{pp}^{C} + \frac{1}{C}(I_{dc} + i_3 + i_4) 2t_3, \tag{4.31}$$

$$\Delta v_{pp}^{E} = \Delta v_{pp}^{D} + \frac{1}{C} I_{dc} 2t_5. \tag{4.32}$$

Utilizing (4.2) - (4.7), (4.23) and (4.24), the following equations for each sub-sector within the first sector are obtained:

$$\Delta v_{pp}^{A} = \frac{5}{2}\frac{I_o}{f_{sw}C} m\cos\varphi\left(\frac{1}{2} - m\cos(\vartheta)\right), \tag{4.33}$$

$$\Delta v_{pp}^{B} = \Delta v_{pp}^{A} + 2\frac{I_o}{f_{sw}C} m\sin\left(\frac{\pi}{5}\right)\sin\left(\frac{\pi}{5} - \vartheta\right)\left(\frac{5}{2} m\cos\varphi - \cos(\vartheta - \varphi)\right), \tag{4.34}$$

$$\Delta v_{pp}^{C} = \Delta v_{pp}^{B} + 2\frac{I_o}{f_{sw}C} m\sin\left(\frac{3\pi}{5}\right)\sin(\vartheta)\left(\frac{5}{2} m\cos\varphi - \cos(\vartheta - \varphi) - \cos\left(\vartheta - \frac{2\pi}{5} - \varphi\right)\right), \tag{4.35}$$

$$\Delta v_{pp}^{D} = \Delta v_{pp}^{C} + 2\frac{I_o}{f_{sw}C} m\sin\left(\frac{3\pi}{5}\right)\sin\left(\frac{\pi}{5} - \vartheta\right)\left(\frac{5}{2} m\cos\varphi + \cos\left(\vartheta - \frac{4\pi}{5} - \varphi\right) - \cos\left(\vartheta - \frac{6\pi}{5} - \varphi\right)\right), \tag{4.36}$$

$$\Delta v_{pp}^{E} = \frac{5}{2}\frac{I_o}{f_{sw}C} m\cos\varphi\left(\frac{1}{2} - m\cos\left(\frac{\pi}{5} - \vartheta\right)\right). \tag{4.37}$$

The global peak-to-peak dc-link voltage ripple amplitude Δv_{pp} is obtained by merging the results corresponding to these five cases and finding the maximum within the switching period:

$$\Delta v_{pp}^{SPWM} = \max\left\{\Delta v_{pp}^{A}, \Delta v_{pp}^{B}, \Delta v_{pp}^{C}, \Delta v_{pp}^{D}, \Delta v_{pp}^{E}\right\}. \tag{4.38}$$

Also in this case, the normalization of the dc-link peak-to-peak voltage switching ripple amplitude is done according to (3.29). Applying the normalization factor to (4.38), the normalized peak-to-peak voltage ripple amplitude is given by:

$$r_{pp}^{SPWM} = \max\left\{r_{pp}^{A}, r_{pp}^{B}, r_{pp}^{C}, r_{pp}^{D}, r_{pp}^{E}\right\}. \tag{4.39}$$

4.4.1.2 Peak-to-peak voltage switching ripple with SVM

As it was commented in section 4.2, the total application time of the zero space vector is equally shared between two zero space vector when space vector modulation is applied. It means that the application times t_o and t_5 (Fig. 4.10) are equal and given by (4.11). Therefore, the evaluation of dc voltage switching ripple is identical in the following three sub-sectors within the first sector: case B, case C and case D for both modulations, SPWM and SVM. The exception is consideration of the total application time of the zero state ($t_0 + t_5$) leading to only one additional case (instead of two cases when SPWM is applied) in the peak-to-peak voltage switching ripple calculations:

- case A: when $i_1 \geq I_{dc}$,

$$\Delta v_{pp}^{A} = \frac{2}{C} I_{dc} t_0, \tag{4.40}$$

Introducing (4.11) and (4.23) into (4.40) yields to

$$\Delta v_{pp}^{A} = \frac{5}{4}\frac{I_o}{f_{sw}C} m\cos\varphi\left(1 - m\left(1 + \cos\left(\frac{\pi}{5}\right)\cos(\vartheta) - m\sin\left(\frac{\pi}{5}\right)\sin(\vartheta)\right)\right). \tag{4.41}$$

The global peak-to-peak dc-link voltage ripple amplitude Δv_{pp} is obtained by merging the results corresponding to these four cases:

$$\Delta v_{pp}^{SVM} = \max\left\{\Delta v_{pp}^{A}, \Delta v_{pp}^{B}, \Delta v_{pp}^{C}, \Delta v_{pp}^{D}\right\}. \tag{4.42}$$

Normalized peak-to-peak voltage ripple amplitude r_{pp}^{SVM} can be defined by (3.29) with reference to Δv_{pp}^{SVM} as

$$r_{pp}^{SVM} = \max\left\{r_{pp}^{A}, r_{pp}^{B}, r_{pp}^{C}, r_{pp}^{D}\right\}. \tag{4.43}$$

To show the behavior of the peak-to-peak voltage switching ripple amplitude over the fundamental period $\vartheta = [0, \pi/5]$, Fig. 4.11 depicts the normalized peak-to-peak voltage switching ripple amplitude calculated by (4.39) and (4.43), when sinusoidal modulating signal is applied and when the zero-sequence signal is injected, respectively.

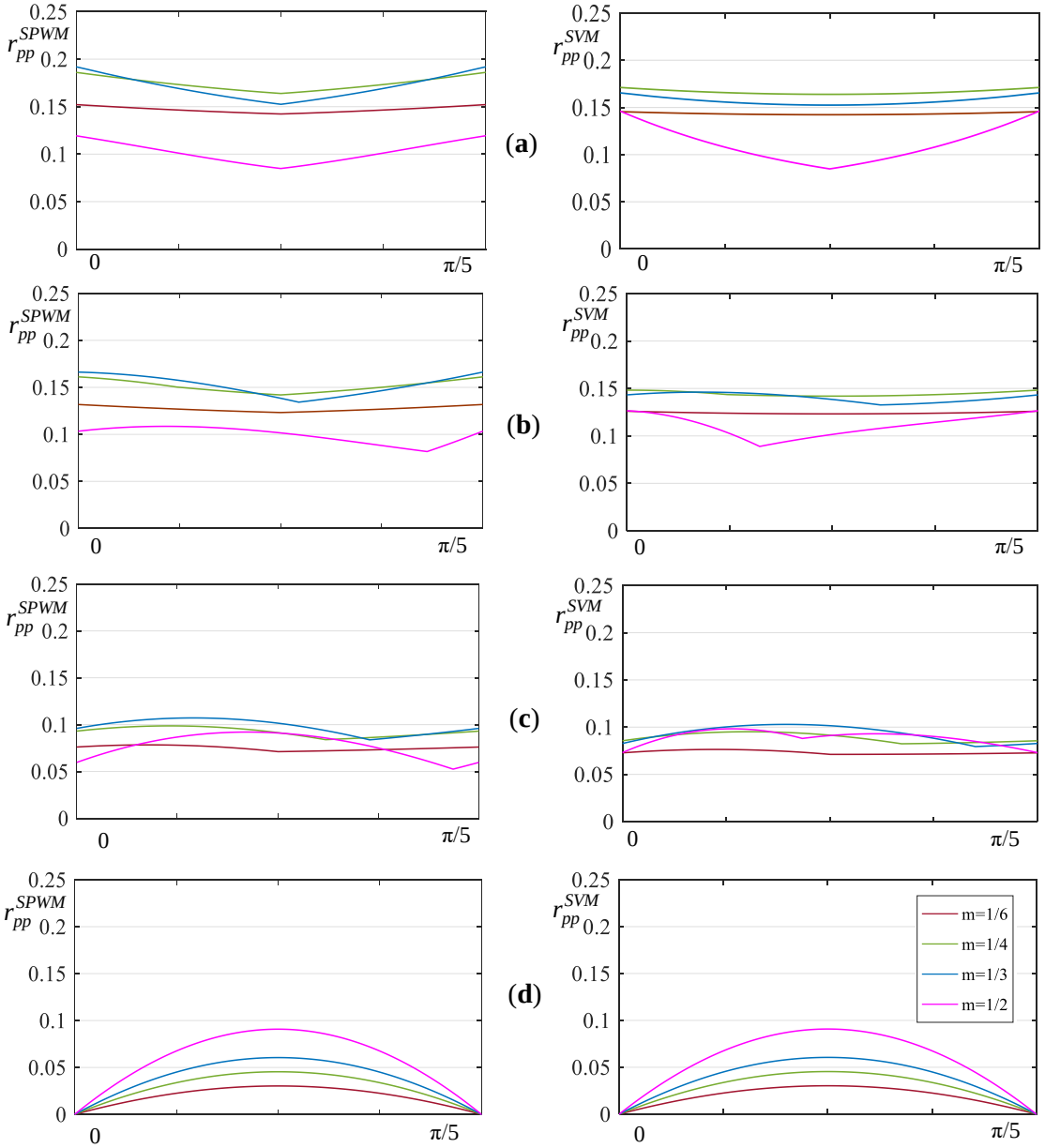

Fig. 4.11: Normalized peak-to-peak dc-link voltage ripple amplitude $r_{pp}(\vartheta)$ over the fundamental period $[0, \pi/5]$, when SPWM (left) and SVM (right) are applied, for different modulation indices, m = 1/6, 1/4, 1/3 and 1/2, and power phase angles φ = 0° (**a**), 30° (**b**), 60° (**c**) and 90° (**d**).

Four power phase angles ϑ = 0, 30°, 60° and 90° have been considered. Four cases that correspond to the operation with m = 1/6, 1/4, 1/3, and 1/2 respectively, are illustrated for each power phase angle. It can be seen from Fig. 4.11 that the dc voltage ripple amplitude generally ranges between 0 (minimum) and 0.2 (maximum). By increasing the power phase angle the peak-to-peak voltage switching ripple amplitude decreases. Also, for all considered values of modulation index the shape of the ripple becomes more flat for higher values of the power phase angles.

4.4.2 Seven-phase inverter

The second multiphase inverter topology which has been analyzed in terms of the dc-link peak-to-peak voltage switching ripple distribution is seven-phase configuration. The investigation of the voltage ripple behavior under the sinusoidal and centered PWM (equivalent to SVM) is shown in the following.

4.4.2.1 Peak-to-peak voltage switching ripple with sinusoidal PWM

In Fig. 4.12 the peak-to-peak dc-link voltage variations Δv_{pp}^{k} and the instantaneous input current $i(t)$ (red staircase line) are depicted in one switching period. As in the five-phase case, just an example of input current waveform is shown aiming to demonstrate the applied approach, but the *max* function, applied finally to the voltage ripple variations, covers all input current profiles.

Depending on the value of I_{dc}, and if SPWM is applied ($t_0 \neq t_7$), seven different cases can be distinguished:

- case A: when $i_1 \geq I_{dc}$,
- case B: when $i_1 \leq I_{dc} < i_1+i_2$,
- case C: when $i_1+i_2 \leq I_{dc} < i_1+i_2+i_7$,
- case D: when $i_1+i_2+i_7 \leq I_{dc} < -(i_4+ i_5+ i_6)$,
- case E: when $-(i_4+ i_5+ i_6) \leq I_{dc} < -(i_4+ i_5)$,
- case F: when $-(i_4+ i_5+ i_6) \leq I_{dc} < -(i_4+ i_5)$,
- case G: when $i_1 \geq I_{dc}$.

According to Fig. 4.12, corresponding peak-to-peak dc-link voltage variations can be expressed as:

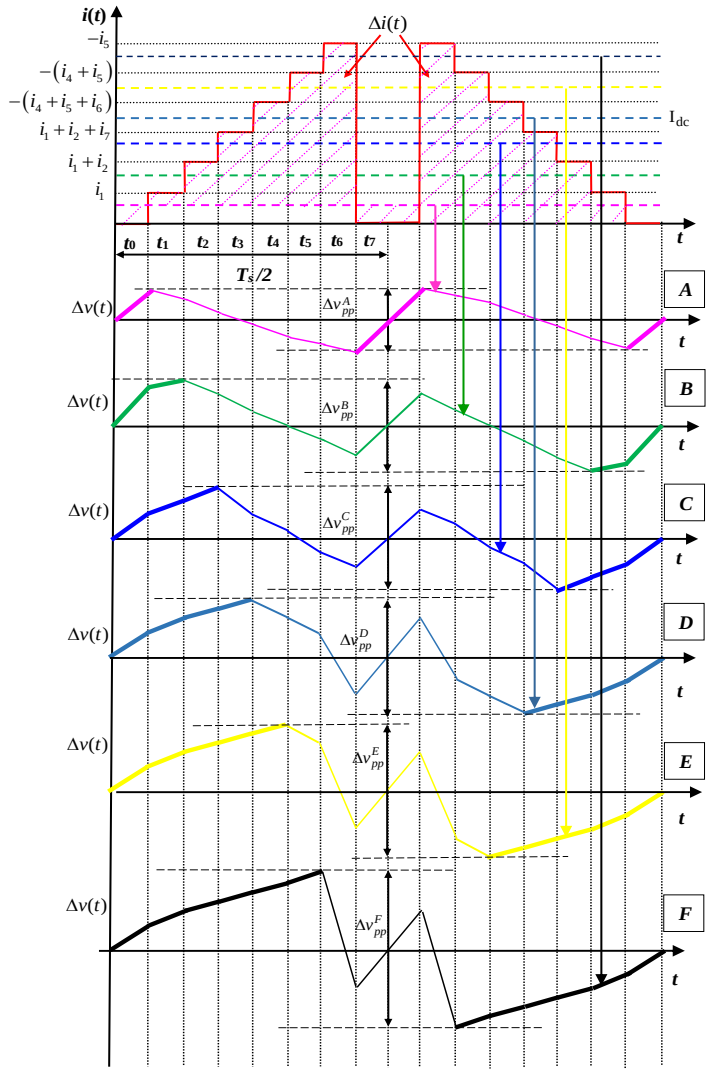

Fig. 4.12: Dc-link current and voltage ripple in one switching period for seven-phase VSIs.

$$\Delta v_{pp}^{A} = \frac{1}{C} I_{dc} 2t_0, \tag{4.44}$$

$$\Delta v_{pp}^{B} = \Delta v_{pp}^{A} + \frac{1}{C}(I_{dc} - i_1) 2t_1, \tag{4.45}$$

$$\Delta v_{pp}^{C} = \Delta v_{pp}^{B} + \frac{1}{C}(I_{dc} - i_1 - i_2) 2t_2, \tag{4.46}$$

$$\Delta v_{pp}^{D} = \Delta v_{pp}^{C} + \frac{1}{C}(I_{dc} - i_1 - i_2 - i_7) 2t_3, \tag{4.47}$$

$$\Delta v_{pp}^{E} = \Delta v_{pp}^{D} + \frac{1}{C}(I_{dc} + i_4 + i_5 + i_6)\,2t_4\,, \tag{4.48}$$

$$\Delta v_{pp}^{F} = \Delta v_{pp}^{E} + \frac{1}{C}(I_{dc} + i_4 + i_5)\,2t_5\,, \tag{4.49}$$

$$\Delta v_{pp}^{G} = \frac{1}{C} I_{dc}\,2t_7. \tag{4.50}$$

Utilizing (4.12) - (4.19), (4.23) and (4.24), the following equations for each sub-sector within the first sector are obtained:

$$\Delta v_{pp}^{A} = \frac{7}{2}\frac{I_o}{f_{sw}C} m\cos\varphi\left(1/2 - m\cos(\vartheta)\right), \tag{4.51}$$

$$\Delta v_{pp}^{B} = \Delta v_{pp}^{A} + 2\frac{I_o}{f_{sw}C} m\sin(\pi/7)\sin(\pi/7 - \vartheta)\left[\frac{7}{2} m\cos\varphi - \cos(\vartheta - \varphi)\right], \tag{4.52}$$

$$\Delta v_{pp}^{C} = \Delta v_{pp}^{B} + 2\frac{I_o}{f_{sw}C} m\sin(5\pi/7)\sin(\vartheta) \left[\frac{7}{2} m\cos\varphi - \cos(\vartheta - \varphi) - \cos(\vartheta - 2\pi/7 - \varphi)\right], \tag{4.53}$$

$$\Delta v_{pp}^{D} = \Delta v_{pp}^{C} + 2\frac{I_o}{f_{sw}C} m\sin(3\pi/7)\sin(\pi/7 - \vartheta) \left[\frac{7}{2} m\cos\varphi - \cos(\vartheta - \varphi) - \cos(\vartheta - 2\pi/7 - \varphi) - \cos(\vartheta - 12\pi/7 - \varphi)\right], \tag{4.54}$$

$$\Delta v_{pp}^{E} = \Delta v_{pp}^{D} + 2\frac{I_o}{f_{sw}C} m\sin(3\pi/7) \left[\frac{7}{2} m\cos\varphi + \cos(\vartheta - 6\pi/7 - \varphi) - \cos(\vartheta - 8\pi/7 - \varphi) + \cos(\vartheta - 10\pi/7 - \varphi)\right], \tag{4.55}$$

$$\Delta v_{pp}^{F} = \Delta v_{pp}^{E} + 2\frac{I_o}{f_{sw}C} m\sin(5\pi/7)\sin(\pi/7 - \vartheta) \left[\frac{7}{2} m\cos\varphi + \cos(\vartheta - 6\pi/7 - \varphi) + \cos(\vartheta - 8\pi/7 - \varphi)\right], \tag{4.56}$$

$$\Delta v_{pp}^{G} = \frac{7}{2}\frac{I_o}{f_{sw}C} m\cos\varphi\left(1/2 + m\cos(\vartheta - 8\pi/7)\right). \tag{4.57}$$

The global peak-to-peak dc-link voltage switching ripple amplitude for SPWM method (Δv_{pp}^{SPWM}) is obtained by finding the maximum value of possible seven cases, as:

$$\Delta v_{pp}^{SPWM} = \max\left\{ \Delta v_{pp}^{A}, \Delta v_{pp}^{B}, \Delta v_{pp}^{C}, \Delta v_{pp}^{D}, \Delta v_{pp}^{E}, \Delta v_{pp}^{F}, \Delta v_{pp}^{G} \right\} . \tag{4.58}$$

By applying (3.9), the normalized peak-to-peak voltage ripple amplitude r_{pp}^{SPWM} is defined as well:

$$r_{pp}^{SPWM} = \max\left\{ \Delta v_{pp}^{A}, \Delta v_{pp}^{B}, \Delta v_{pp}^{C}, \Delta v_{pp}^{D}, \Delta v_{pp}^{E}, \Delta v_{pp}^{F}, \Delta v_{pp}^{G} \right\} . \tag{4.59}$$

4.4.2.2 Peak-to-peak voltage switching ripple with space vector modulation

If SVM modulation is applied to seven-phase inverter, the application times t_o and t_7 (Fig. 4.12) are equal and given by (4.20). Therefore, the evaluation of dc voltage switching ripple is identical in the following five sub-sectors within the first sector: case B, case C, case D, case E and case F for both modulations, SPWM and SVM. The exception is consideration of the total application time of the zero state ($t_0 + t_7$) leading to only one additional case (instead of two cases when SPWM is applied) in the peak-to-peak voltage switching ripple calculations:

- case A: when $i_1 \geq I_{dc}$,

$$\Delta v_{pp}^{A} = \frac{2}{C} I_{dc} t_0, \tag{4.60}$$

Introducing (4.20) and (4.23) into (4.60) yields to

$$\Delta v_{pp}^{A} = \frac{7}{4} \frac{I_o}{f_{sw} C} m \cos\varphi \left[\begin{matrix} 1 - 2m\left(\sin\left(\pi/7\right) + \sin\left(3\pi/7\right) + \sin\left(5\pi/7\right)\right) \\ \left(\sin\left(\pi/7\right)\cos\left(\vartheta\right) + \left(1 - \cos\left(\pi/7\right)\right)\sin\left(\vartheta\right)\right) \end{matrix} \right] . \tag{4.61}$$

The global peak-to-peak dc-link voltage ripple amplitude Δv_{pp} is obtained by merging the results corresponding to these six cases:

$$\Delta v_{pp}^{SVM} = \max\left\{ \Delta v_{pp}^{A}, \Delta v_{pp}^{B}, \Delta v_{pp}^{C}, \Delta v_{pp}^{D}, \Delta v_{pp}^{E}, \Delta v_{pp}^{F} \right\} . \tag{4.62}$$

Normalized peak-to-peak voltage ripple amplitude r_{pp}^{SVM} can be again defined by (3.29) with reference to Δv_{pp}^{SVM} as

$$r_{pp}^{SVM} = \max\left\{ r_{pp}^{A}, r_{pp}^{B}, r_{pp}^{C}, r_{pp}^{D}, r_{pp}^{E}, r_{pp}^{F} \right\}. \tag{4.63}$$

The normalized peak-to-peak voltage switching ripple amplitude calculated by (4.59) and (4.63), when SPWM and SVM are applied, respectively, is shown in Fig. 4.13.

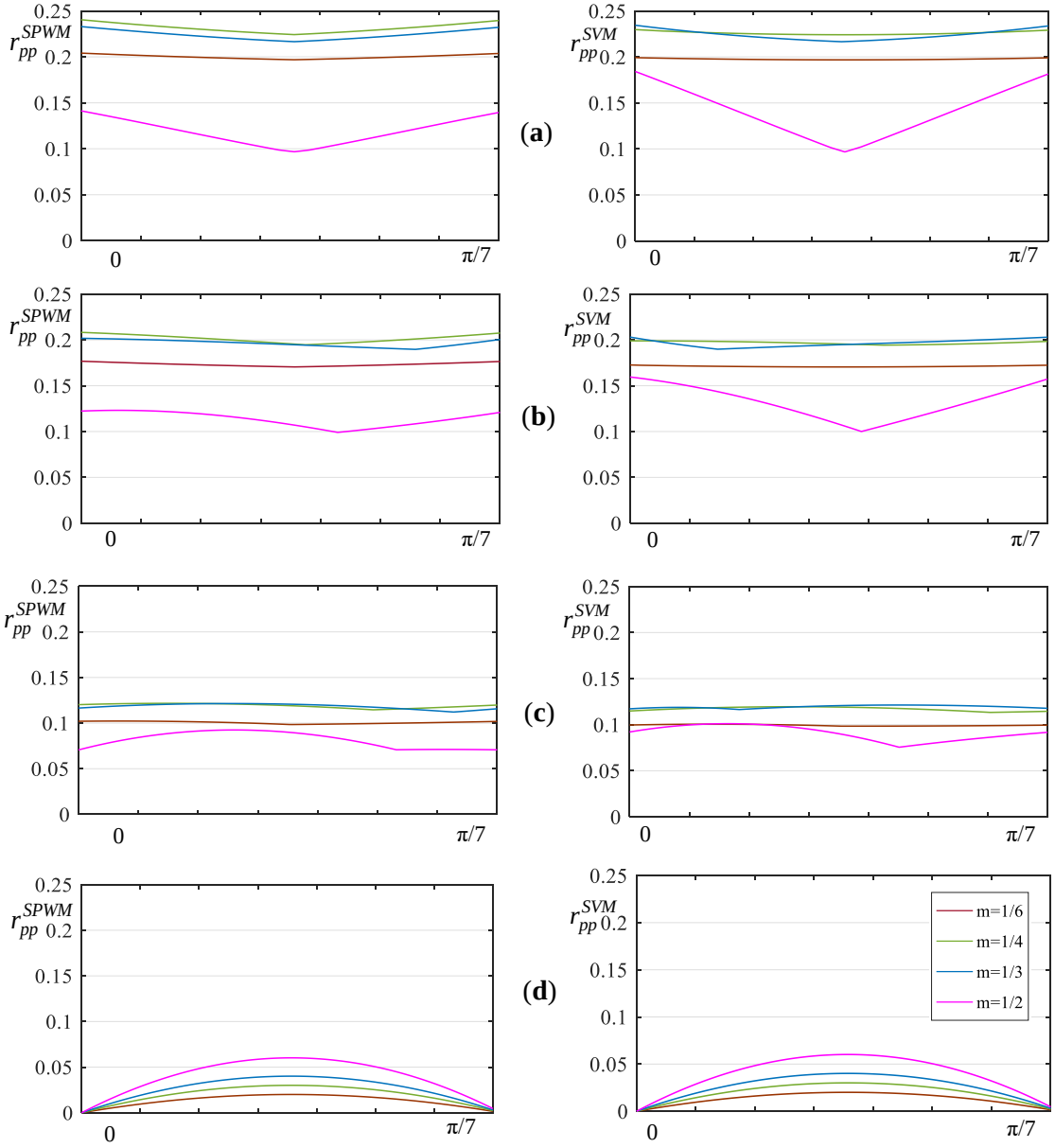

Fig. 4.13: Normalized peak-to-peak dc-link voltage ripple amplitude $r_{pp}(\vartheta)$ over the fundamental period [0, π/7], when SPWM (left) and SVM (right) are applied, for different modulation indices, m = 1/6, 1/4, 1/3 and 1/2, and power phase angles φ = 0° (**a**), 30° (**b**), 60° (**c**) and 90° (**d**).

Four power phase angles ϑ = 0, 30°, 60° and 90° have been considered. Four cases that correspond to the operation with m = 1/6, 1/4, 1/3, and 1/2 are illustrated for each power phase angle. It can be seen from Fig. 4.13 that the dc voltage ripple amplitude generally ranges between 0 (minimum) and 0.25 (maximum). The peak-to-peak voltage switching ripple amplitude decreases when the power phase angle increases. Also, the shape of the ripple becomes more flat for higher values of the power phase angles for all considered values of modulation index. The effect of applied modulation techniques is not significant and no practical deference has been shown neither in the global maximum nor in the voltage ripple profile between sinusoidal PWM and SVM.

4.5 Voltage switching ripple comparison in multiphase inverters

In order to predict the ripple behaviour and make a comparison between analysed cases, Fig. 4.14 shows normalized function of the dc voltage ripple amplitude for three-, five- and seven- phase VSIs. The evaluation is done on the basis of the analyses presented in the previous sub-sections 3.4.1, 4.4.1 and 4.4.2.

For all considered inverter topologies, the ripple normalization is given according to (3.29). As can be noted, the same output current is assumed. This makes a difference compared to the case when the same apparent power is considered. Thus, the new normalization considering the same apparent power instead of the same output current will be introduced in the next sub-section followed by some remarks on maximum peak-to-peak voltage ripple amplitude behaviour.

Three values of modulation index (m = 1/4, 1/3, and 1/2) and two power phase angles are considered in Fig. 4.14. In particular, φ = 20° and φ= 70° have been chosen to approximately represent the usual phase angle range for an induction motor, corresponding to rated and no load conditions, respectively.

The results are shown with reference to both SPWM and SVM (solid and dashed lines, respectively). The global voltage ripple maximum is around 0.2 for all considered cases, and a wide excursion of voltage ripple envelope is noticable. However, it is evident that by increasing the number of phases the profile of the voltage ripple amplitude becomes more flat and uniform. Unlike the three-phase case, in five- and seven- phase case increasing the power phase angle the voltage ripple amplitude is significantly reduced. In presented cases, the amplitude is half reduced and the reduction is better noticable for higher number of phases.

The impact of applied modulation techniques is evident in case of three-phase inverter. Significant reduction in the voltage ripple amplitude can be noted due to the centering performed in the SVM (CPWM), especially for lower power phase angles. It leads to the conclusion that SVM (or CPWM) is preferable modulation for three-phase

inverters from the point of view of the dc-link voltage ripple requirements and the dc-link capacitor sizing.

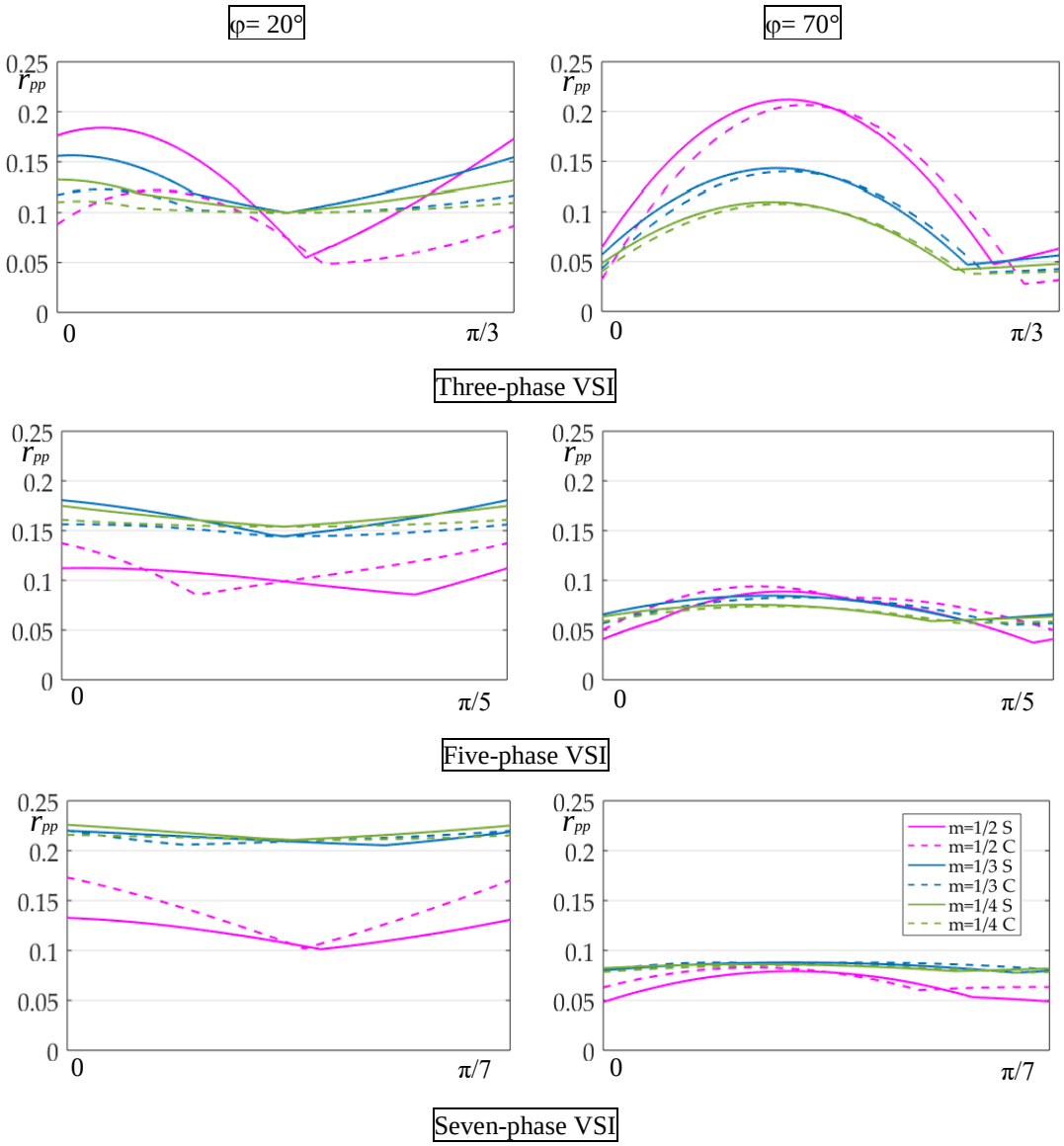

Fig. 4.14: Normalized peak-to-peak dc-link voltage ripple amplitude $r_{pp}(\vartheta)$ over its period for three-, five-, and seven-phase VSIs, considering three modulation indices, m = 1/4, 1/3, and 1/2, two power phase angles φ = 20° (left column) and φ = 70° (right column), with SPWM and SVM (continuous and dashed lines, respectively).

However, no significant influence of SVM (CPWM) on the voltage switching ripple amplitude is shown in case of five- and seven- phase inverters. This is because the

improvement in dc bus utilisation rapidly decreases as the number of phases increases when the centering in the SVM (CPWM) is performed comparing to the pure sinusoidal modulation.

4.5.1 Maximum of the peak-to-peak voltage ripple amplitude

For a fair comparison of inverter topologies with different phase numbers, the same apparent output power should be considered. For this reason, the total output current nI_o is introduced, and a "per-phase" normalization is defined as

$$\Delta v_{pp} = \frac{nI_o}{f_{sw}C} r_{ppn}, \tag{4.64}$$

being $r_{ppn} = \frac{r_{pp}}{n}$ and n - number of phases. Maximum of per-phase normalized peak-to-peak voltage ripple amplitude r_{ppn} is obtained numerically as a function of modulation index and shown in Fig. 4.15. Four power phase angles φ = 0°, 20°, 45° and 70° are considered in order to better cover the considered range. Because the interest in this sub-section is the impact of the number of phases on the dc-link capacitor design rather than of the applied modulation techniques, only SPWM is considered in the following analysis. Moreover, it was shown before that increasing the number of phases there are no significant benefits on the voltage ripple amplitude by applying CPWM.

The following observations are worth noting on the maximum peak-to-peak voltage ripple amplitude (r_{ppn}) displayed in Fig. 4.15. First, the maximum of dc voltage ripple amplitude decreases when the number of phases increases. The reduction is significant when the number of phases increases from three to five, and less significant when it increases to seven. Finally, no practical difference in the maximum voltage ripple is obtained for the number of phases higher than seven.

Referring to the three-phase case, the maximum of the normalized peak-to-peak voltage ripple amplitude is almost linear function of modulation index. It can be noticed in Fig. 4.15 a slight increase of the global maximum value with the decreasing of the power phase angle. However, for five- and seven-phase case the global maximum of the voltage ripple amplitude slightly reduces when the phase angle increases. No further reduction of maximum voltage ripple is observed for higher number of phases ($n > 7$).

These diagrams can be useful for the dc-link capacitor design proposed in the following sub-section.

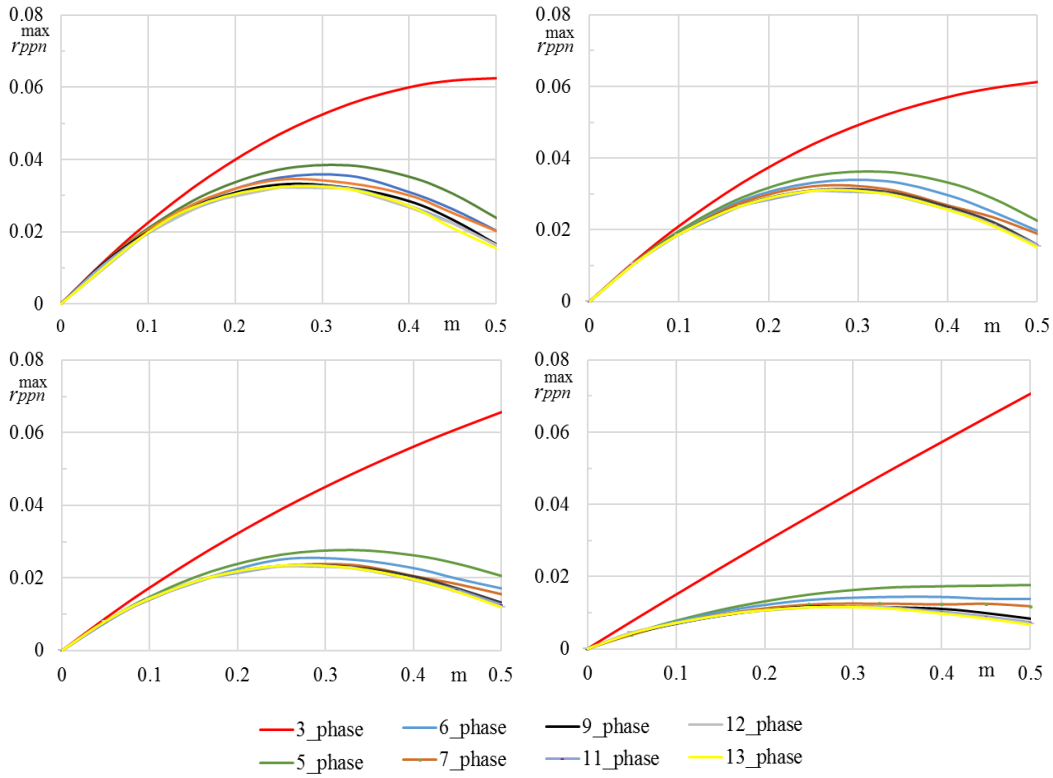

Fig. 4.15: Maximum of peak-to-peak voltage ripple amplitude normalized per total output current r_{ppn}^{max} in multiphase VSIs, as a function of modulation index for power phase angles:

(**a**) φ = 0°, (**b**) φ = 20°, (**c**) φ = 45°, and (**d**) φ = 70°.

According to Fig. 4.15, global maximum r_{ppn}^{max} for different phase numbers and power phase angles is presented in Table 4.1. The values will be used for sizing the dc-link capacitor in the next sub-section.

Table 4.1: Global maximum of r_{ppn}^{max} as a function of number of phases for different phase angles.

angle	Phase number (*n*)							
	3	**5**	**6**	**7**	**9**	**11**	**12**	**13**
φ = 0°	0.0625	0.0384	0.0355	0.0343	0.0323	0.0323	0.0323	0.0323
φ = 20°	0.0614	0.0361	0.0335	0.0323	0.031	0.0309	0.0309	0.0309
φ = 45°	0.0656	0.0276	0.0252	0.0237	0.0234	0.0234	0.0234	0.0234
φ = 70°	0.0706	0.0177	0.0143	0.0126	0.0116	0.0116	0.0116	0.0116

It is evident that by considering the same total output current (apparent power) in different multiphase inverter topologies, the maximum value of dc voltage ripple amplitude reduces with the increase of the phase number up to seven, but not for the higher number of phases.

4.5.2 Dc-link capacitor design

In this sub-section, the capacitor size is designed based on the voltage switching ripple requirements Δv_{pp}^{*} and considering the general assumption applied in this thesis on the dc source impedance (Z_{dc}) and the capacitor reactance ($1/2\pi f_{sw}C$) calculated at the switching frequency (which is at least in order of kHz).

By observing Fig. 4.15, and by considering $r_{ppn}^{\max}$ given in Table 4.1, a simple general formula for the dc-link capacitor design is obtained on the basis of (4.64) and by specifying the desired Δv_{pp}^{*} as:

$$C \geq \frac{nI_o}{f_{sw}} r_{ppn}^{\max}(\varphi) \frac{1}{\Delta v_{pp}^{*}}. \tag{4.65}$$

The worst case scenario should be considered for final design of capacitor. According to Table 4.1, it corresponds to unity power factor ($\varphi \approx 0°$) when $r_{ppn}^{\max}$ is ranging between 0.0625 ÷ 0.0323, depending on the considered inverter topology. However, if the load is an AC motor, two values of phase angle $\varphi = 20°$ and $\varphi = 45°$ are of greater interest. The first one approximately corresponds to motor rated condition and the second one represents the half-loaded motor.

One can notice that the expression (4.65) can be used straightforward in case of any multiphase inverter topology where $n \geq 3$.

As an example, five-phase motor with power phase angle $\varphi = 45°$ is considered as a load. Referring to Table 4.1, the following simplification can be made, and the dc-link capacitance can be calculated as:

$$r_{ppn}^{\max}(\varphi) = 0.0276 \rightarrow C \geq 0.138 \frac{I_o}{f_{sw}\Delta v_{pp}^{*}}. \tag{4.66}$$

Focusing on the particular case and observing the Table 4.1. it can be concluded that, from the point of view of the dc-link capacitor size, there are no benefits increasing the number of phases more than seven for a given load (motor) power, since $r_{ppn}^{\max}$ saturates at 0.0334.

4.6 Simulation and experimental results

In order to validate theoretical developments proposed in previous sections, simulations and corresponding experimental tests have been performed for five- and seven- phase inverters. Reference is made to two most commonly used modulation techniques – sinusoidal PWM and SVM. Numerical simulations have been carried out by Matlab/Simulink. The simulation circuit parameters, summarized in Table 4.2, are set in order to match the corresponding experimental setup parameters. Multiphase passive loads have been preferred to motor load for a better stability of the measured voltage switching ripple profile. Actually, the only requirement to evaluate the dc-link voltage ripple, with the proposed developments, is to have an output current almost sinusoidal and balanced. The two power phase angles of interest are obtained by using two different sets of passive balanced *R-L* load impedances. The parameters of the load are given in Table 4.3.

Table 4.2: The simulation and experimental setup parameters.

Parameter	Symbol	Value
Dc voltage supply	V_{dc}	300 V
Dc source resistance	R_{dc}	5.3 Ω
Dc source inductance	L_{dc}	4.5 mH
Dc-link capacitance (2x film cap.)	C	200 μF
Equivalent series resistance	ESR	10 mΩ
Equivalent series inductance	L_s	25 nH
Fundamental frequency	f	50 Hz
Switching frequency	f_{sw}	2 kHz

Table 4.3: Passive *R-L* load parameters.

5x, 7x	φ = 20°	φ = 70°
R_L (Ω)	24	24
L_L (mH)	25	204

The experimental setup is shown in Fig. 4.16. It consists of the two-level custom-made inverter which has up to eight output legs, and it has been used for the experiments with five- and seven-phase symmetrical *R-L* load. Used IGBT module is FS50R12KE3 (Infineon). Inverter was controlled by dSpace ds1006 real-time system. The software code that is running on ds1006 processor board is automatically generated and loaded from the Matlab/Simulink. The switching frequency was set to 2kHz. For control and visualization of the particular Simulink variables, Control Desk has been used as a user interface. Dc-bus supply voltage is provided from the external dc source Sorensen SGI 600/25. The Z_{dc} impedance is added between the dc source and the dc-link. Equivalent value of two dc-link film capacitors connected in parallel is 200μF. The dead time is configurable in the hardware and set to 6μs. Tektronix oscilloscope MSO2014 with P5205A differential voltage probe was used for measurement.

The dc voltage ripple waveforms were filtered out using a second-order low pass filter to clean the waveforms and attenuate electromagnetic noise in the signals. In addition, FFT was applied in post-processing of the experimental data to remove small low frequency components. Presence of small low frequency components in the dc-link voltage ripple was the consequence of a non-perfectly balanced load. The impact of slightly unbalanced load on the dc-link variables will be discussed in Chapter5.

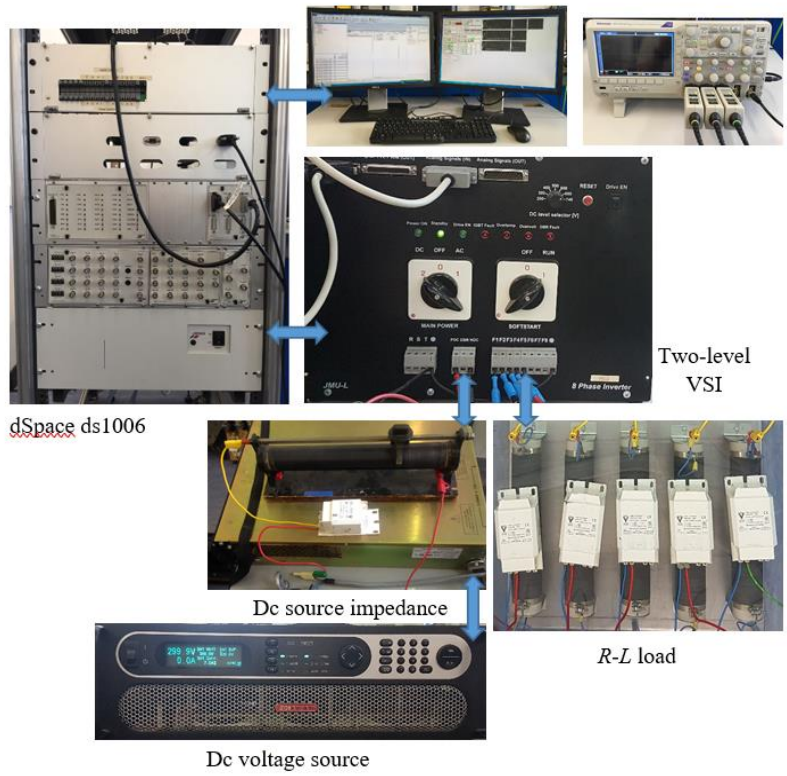

Fig. 4.16: Experimental setup.

4.6.1 Five-phase inverter

Regarding the two-level five-phase inverter supplying the five-phase symmetrical *R-L* load, simulation and experimental results are shown side by side in Fig. 4.17 and Fig. 4.18 when SPWM is applied, and in Fig. 4.19 and Fig. 4.20 when SVM is applied. The peak-to-peak envelopes are calculated by (4.38) and (4.42) as the half of peak-to-peak dc-link voltage ripple amplitude $\Delta v_{pp}/2(t)$ (red traces) for SPWM and SVM, respectively. The envelopes are shown together with the instantaneous dc-link voltage switching ripple $\Delta v(t)$ (blue trace) over a fundamental period (T = 20 ms). Two values of the power phase angles φ= 20° (Figs. 4.17 and 4.19) and φ=70° (Figs. 4.18 and 4.20) are considered. Two subcases (a) and (b) in each figure correspond to two values of modulation index m: 0.25 and 0.5 (top and bottom, respectively).

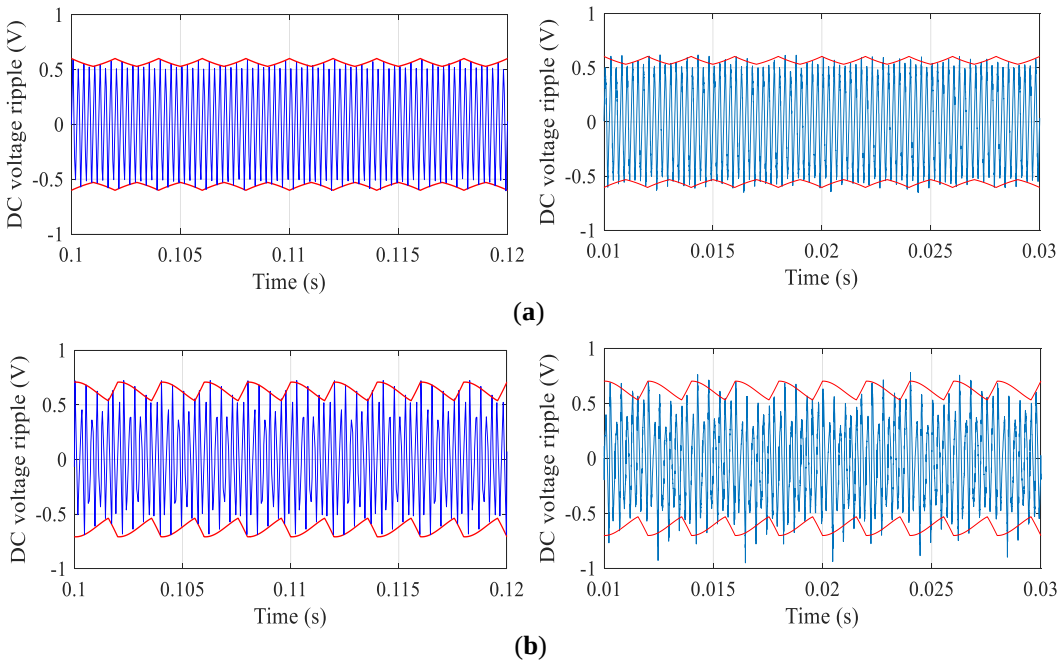

Fig. 4.17: Dc-link voltage switching ripple in five-phase inverter with SPWM: simulations (left column) and experimental results (right column) with calculated peak-to-peak envelope (red trace) over a fundamental period for φ = 20°, (**a**) m = 0.25 and (**b**) m = 0.5.

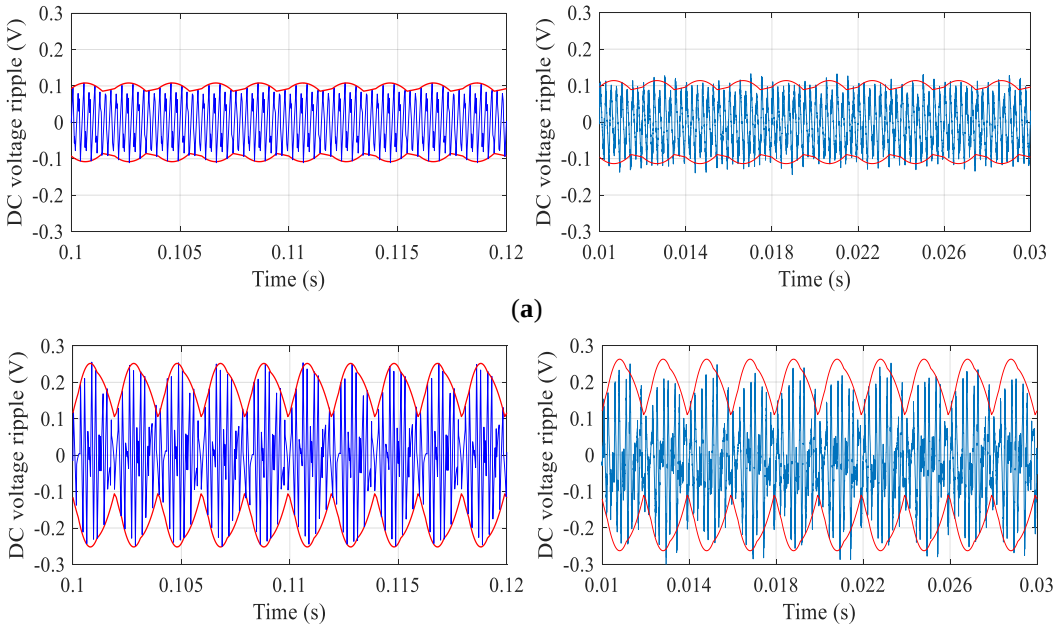

Fig. 4.18: Dc-link voltage switching ripple in five-phase inverter with SPWM: simulations (left column) and experimental results (right column) with calculated peak-to-peak envelope (red trace) over a fundamental period for φ = 70°, (**a**) *m* = 0.25 and (**b**) *m* = 0.5.

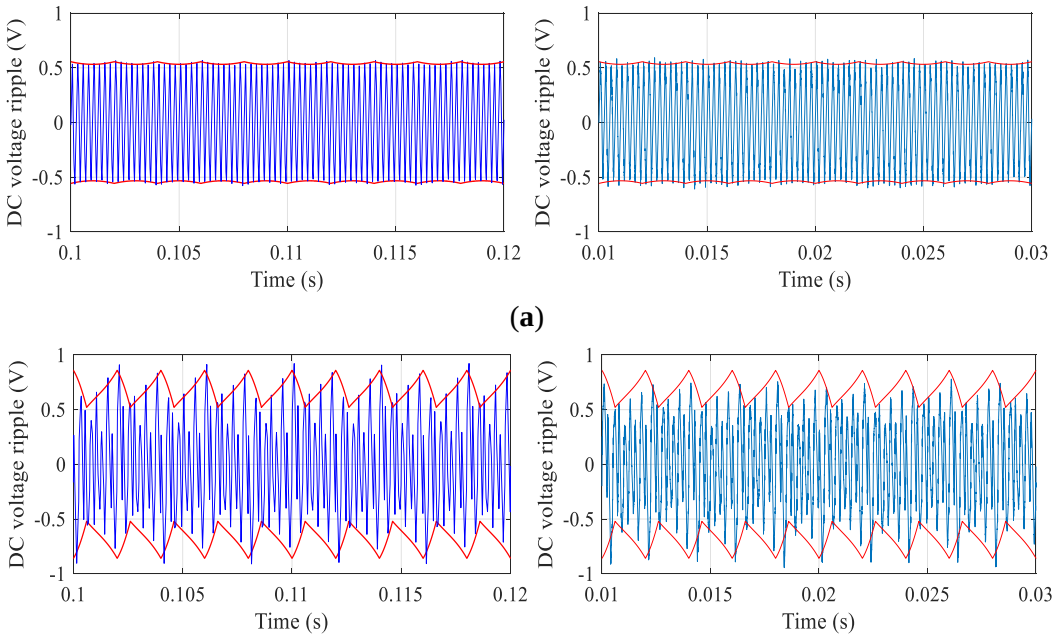

Fig. 4.19: Dc-link voltage switching ripple in five-phase inverter with SVM: simulations (left column) and experimental results (right column) with calculated peak-to-peak envelope (red trace) over a fundamental period for φ = 20°, (**a**) *m* = 0.25 and (**b**) *m* = 0.5.

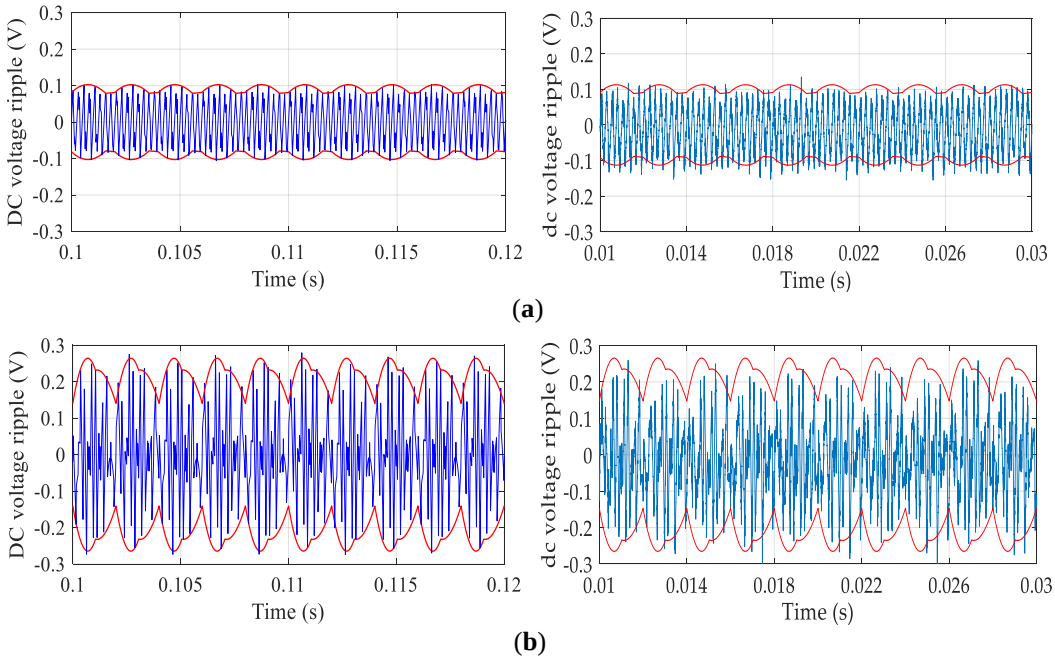

Fig. 4.20: Dc-link voltage switching ripple in five-phase inverter with SVM: simulations (left column) and experimental results (right column) with calculated peak-to-peak envelope (red trace) over a fundamental period for φ = 70°, (**a**) m = 0.25 and (**b**) m = 0.5.

According to the Figs. 4.17-4.20, both, numerical simulations and experimental results are in a good agreement with theoretical developments for all considered cases. A small mismatch in some cases of experimental results, when the dc voltage ripple has a slightly lower absolute amplitude comparing to the calculated envelopes, is due to the filtering performed in post-processing of the experimental data. As an example, Fig. 4.20 sub-case (b) can be taken. In order to justify the slight exceeding of the dc voltage ripple outside of the calculated envelopes, Fig. 4.20 sub-case (a) as an example, further considerations on the dc-link capacitor are introduced.

First, note that an ideal dc-link capacitor has been primarily considered in the simulations. For the additional set of simulations shown below, a real-world capacitor model (a series-connected *RLC* circuit) has been used instead, and the effect of the capacitor's parasitic components on the dc-link voltage ripple is examined. Since the two film capacitors connected in parallel have been used in the experiments, the simulation parameters are set to match the parasitic components given in Table 4.2. In particular, the values of C and *ESR* are measured by *Peak Atlas ESR70* Capacitor *ESR* Meter, and L_s is obtained from the used *KEMET C4AEGBW6100A3NJ* capacitors datasheet. The total impedance of the capacitor (Z_c) is calculated as:

$$Z_c = \sqrt{ESR^2 + \left(2\pi f\, L_s - \frac{1}{2\pi f\, C}\right)^2}\,. \tag{4.67}$$

Fig. 4.21 shows the impedance (Z_c) characteristic of the adopted film capacitor for two values of *ESR*.

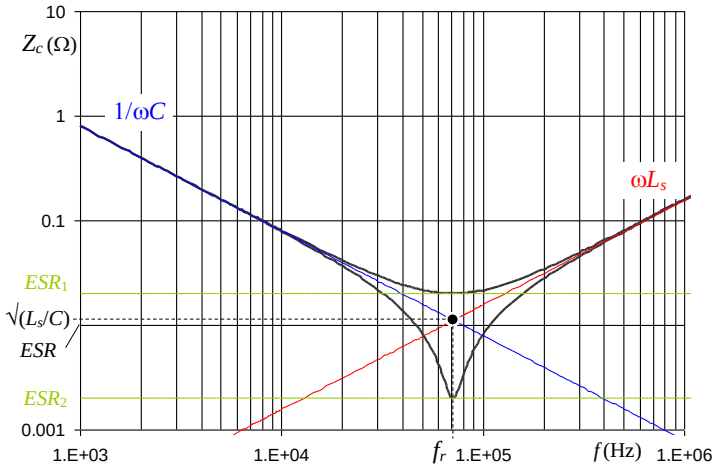

Fig. 4.21: Impedance vs. frequency characteristic of a real capacitor (C = 200 μF, L_s = 25 nH, ESR_1 = 20 mΩ and ESR_2 = 2 mΩ).

It can be noticed in Fig. 4.21 that, in the considered case, the switching frequency is well below the self-resonant frequency of the dc-link capacitor. Hence, its inductive reactance ωL_s is negligible comparing to the capacitive reactance $1/\omega C$. The same applies to *ESR* since it has similar or lower value comparing to sqrt(L_s/C).

This statement is confirmed by numerical simulation results shown in Fig. 4.22 (left) for five-phase case when m = 0.25 and φ = 70°. It corresponds to experimental result shown in Fig. 4.22 (right). Therefore, as commented before for the considered case, the effects of the *ESR* and L_s on the dc-link voltage ripple are negligible. Note that, to attenuate the noise, simulated dc-voltage ripple is filtered in the same way as in the experiments.

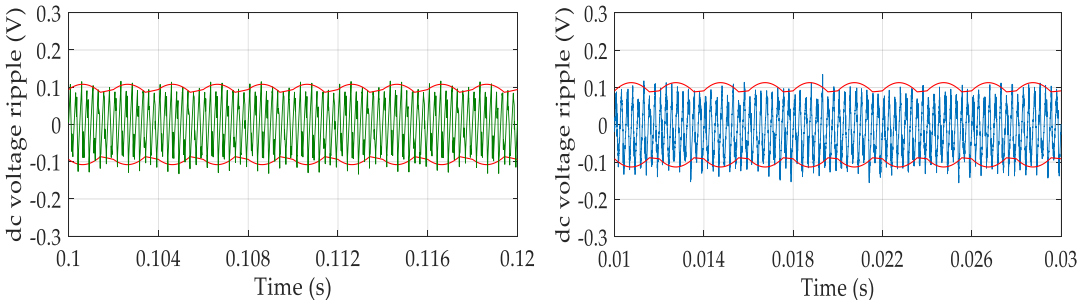

Fig. 4.22: Simulation (left column) and experimental results (right column) for five-phase VSI (m=0.25, φ=70°) considering ESR of the dc-link capacitor.

The effect of the capacitor's parasitic components can be severe in case of the switching frequency close to the self-resonant frequency of the dc-link capacitor, as shown in Fig. 4.21, but the detail analysis of this is beyond the scope of this thesis. Moreover, note that the results prove that when going for higher number of phases, smaller capacitance can be used, which practically means that instead of large electrolytic capacitors, smaller higher quality capacitors (such as film capacitors) with lower *ESR* can be used.

4.6.2 Seven-phase inverter

In case of two-level seven-phase inverter supplying the seven-phase symmetrical *R-L* load, simulations and experimental results were performed and the results are shown in Figs. 4.23-4.26. Figs. 4.23 and 4.24 show simulations (left column) and experimental results (right column) when SPWM is applied, while Figs. 4.25 and 4.26 show simulations (left column) and experimental results (right column) when SVM (equivalent to CPWM) is applied. The peak-to-peak envelopes calculated as the half of peak-to-peak dc-link voltage ripple amplitude $\Delta v_{pp}/2(t)$ (red traces) by (4.58) and (4.62) for SPWM and SVM, respectively, are shown together with the instantaneous dc-link voltage switching ripple $\Delta v(t)$ (blue trace) over a fundamental period (T = 20 ms). Same as before, two values of the power phase angles φ= 20° (Figs. 4.23 and 4.25) and φ=70° (Figs. 4.24 and 4.26) are considered and two sub-cases, (a) and (b), correspond to two values of modulation index m: 0.25 and 0.5, respectively.

There is a good matching between the measured dc voltage switching ripple and calculated envelopes that correspond to positive and negative peak value of the measured variable. These results, similar to those of Figs. 4.17-4.20 for a five-phase case, further confirm validity of theoretical developments presented earlier in this chapter.

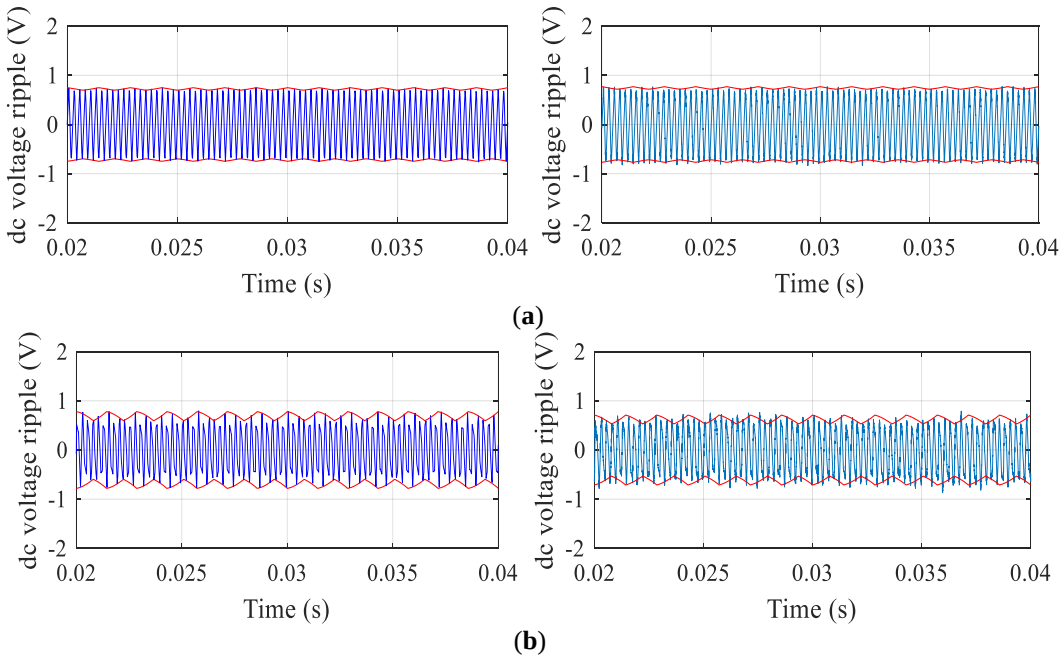

Fig. 4.23: Dc-link voltage switching ripple in seven-phase inverter with SPWM: simulations (left) and experimental (right) results with calculated peak-to-peak envelope (red trace) over a fundamental period for φ = 20°, (**a**) *m* = 0.25 and (**b**) *m* = 0.5.

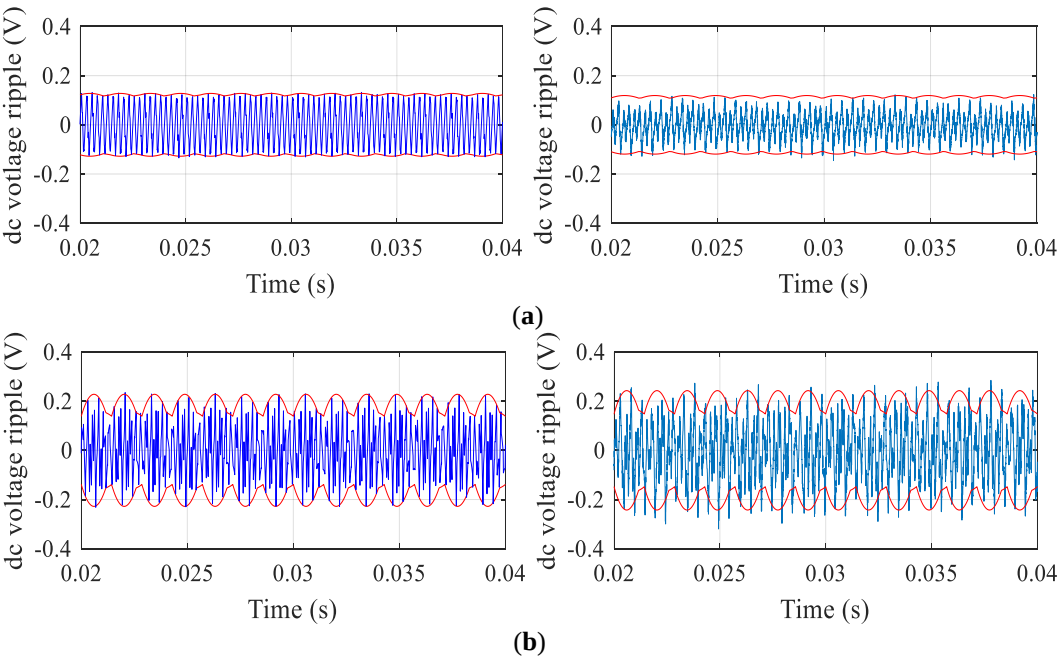

Fig. 4.24: Dc-link voltage switching ripple in seven-phase inverter with SPWM: simulations (left) and experimental (right) results with calculated peak-to-peak envelope (red trace) over a fundamental period for φ = 70°, (**a**) *m* = 0.25 and (**b**) *m* = 0.5.

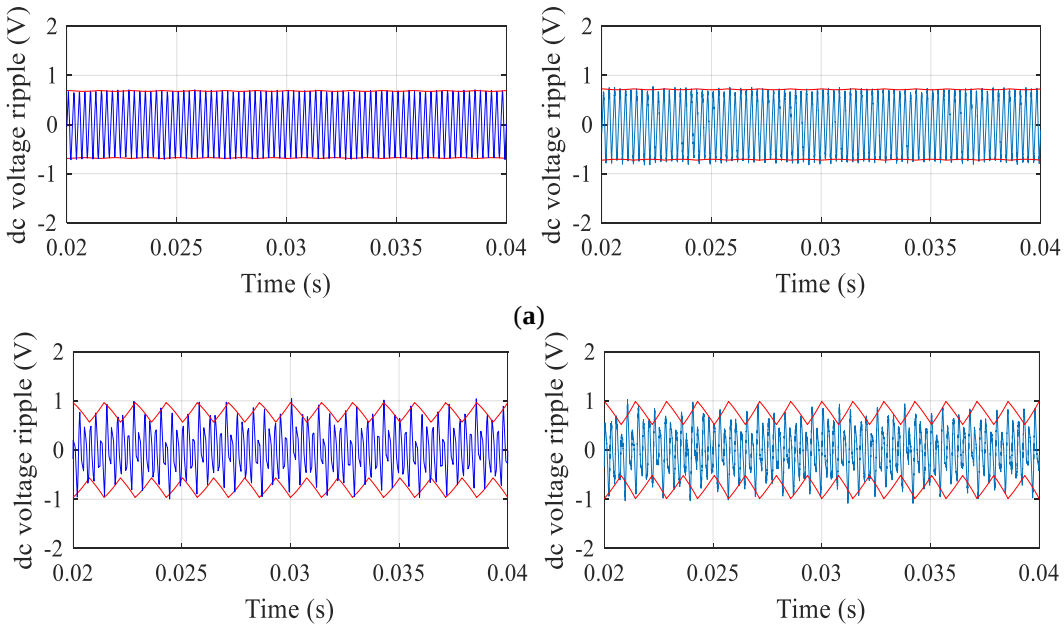

Fig. 4.25: Dc-link voltage switching ripple in seven-phase inverter with SVM: simulations (left) and experimental (right) results with calculated peak-to-peak envelope (red trace) over a fundamental period for φ = 20°, (**a**) *m* = 0.25 and (**b**) *m* = 0.5.

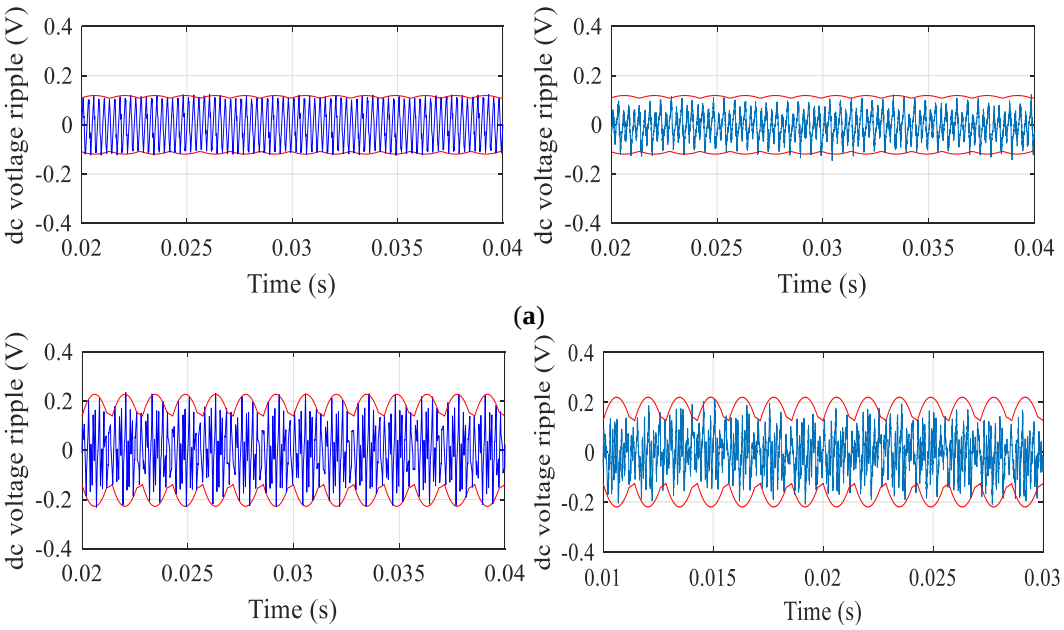

Fig. 4.26: Dc-link voltage switching ripple in seven-phase inverter with SVM: simulations (left) and experimental (right) results with calculated peak-to-peak envelope (red trace) over a fundamental period for φ = 70°, (**a**) *m* = 0.25 and (**b**) *m* = 0.5.

4.7 Discussion

In this chapter, dc-link current and voltage ripple analysis is presented for two-level multiphase voltage source inverters with an odd number of phases greater than three, considering balanced load conditions. Some general steps in the analysis are described but a special focus has been put on five- and seven-phase inverters. A short review of carrier-based PWM and space vector modulation for aforementioned inverter topologies is provided. Furthermore, the dc-link voltage ripple components are calculated on the basis of corresponding dc-link current components. The voltage switching ripple amplitude has been calculated for both applied modulations as a function of operational conditions: modulation index, the amplitude of phase current and power phase angle. The maximum (peak-to-peak) value of voltage ripple amplitude has been evaluated as a function of modulation index for both examined inverter topologies, five- and seven- phase, considering different power phase angles. The comparison of dc-link voltage switching ripple between different phase numbers has been made. Finally, simple and effective guideline for designing the dc-link capacitor based on the maximum required dc-link voltage switching ripple amplitude in multiphase inverters has been proposed. The effect of increasing the number of phases on dc-link capacitor sizing has been discussed as well.

Simulations and experimental results for both SPWM and CPWM, considering two power phase angles and different values of modulation index, are given for two presented inverter topologies. Given results are aimed to show the matching between analytically calculated dc-link voltage ripple envelope and measured instantaneous dc-link voltage switching ripple.

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Chapter 5

Dc-link low-frequency voltage ripple analysis in three-phase and multiphase inverters with unbalanced load

5.1 General considerations of voltage and current unbalance

Any deviation of voltage and current waveforms from symmetric sinusoidal disposition, in terms of magnitude, phase angle, or both, is considered as unbalance. In the literature, the term "asymmetrical" is also used to describe the unbalanced conditions. Depending on the deviation, the unbalance appears as voltage, current or simultaneous voltage and current unbalance. The majority of studies and standards presented in literature discuss voltage unbalance, which appears as a result of unsymmetrical voltage supply among the phases, unsymmetrical line parameters among the phases, or unbalanced loads. A comprehensive survey on the causes of voltage unbalance and the resulting effects on the power system and on equipment, such as induction motors, power converters and drives, is given in [5.1].

The current unbalance and its associated power unbalance appear as a result of unbalanced magnitudes of the phase voltages, angle displacement between the phase voltages or internal impedances of the motor. The impedance unbalance in motor may have been caused by unbalanced heating of the stator [5.2]. Motor unbalance can be also due to a manufacturing problems such as unequal number of turns in the windings, a misaligned rotor or an asymmetric stator. Sometimes, to reduce the time and to lower the costs of the repair process, failed windings are repaired by isolating the failed turn, thus reducing the impedance of the repaired phase. Extreme examples of the current unbalance are faults. Faults usually cause temporary current unbalance. However, if they are not repaired on time, these conditions may cause system instability [5.3].

Most of the power quality standards are related to the supply (grid) voltages and so, they recommend limits for the maximum voltage unbalance. The voltage unbalance is most commonly defined as the ratio of the negative voltage sequence component to the positive voltage sequence component. The American National Standards Institute (ANSI standard C84.1-1995 [5.4]) and European distribution networks (IEC 60038 [5.5]) recommend limits for the maximum voltage unbalance of electrical supply system of 3% and 2%, respectively, when measured at the electric-utility revenue meter under no-load conditions. NE-

MA MG1-1993 “Motors and Generators” standard recommends that for voltage unbalance greater than 1%, AC motors should be derated by the appropriate factor. IEC standards also restrict the allowed voltage unbalance on AC motors up to 1% and require a derating of the machines if unbalance is greater [5.6]. More definitions of voltage/current unbalances will be introduced in the next section.

Although the voltage unbalance has been studied more in the literature, in this thesis current unbalance is of greater interest. Namely, in this chapter, considered configuration is a two-level *n*-phase inverter supplying a star-connected *n*-phase load. Connected load is a standard multiphase ac motor that shows in practice a certain degree of unbalance, in order of a few percent. An example of such a small unbalance in an ac motor is the line-to-line motor resistance which differs up to 2% when compared to the average. As a consequence of the unbalance occurrence, depending on the load power and percentage of the unbalance, the instantaneous power oscillation (at double-fundamental frequency) is introduced and the dc-link capacitor is affected. This reflects in current and voltage low-frequency ripple on the dc-link inverter side. Therefore, not only the switching ripple component but also the double-fundamental one plays a role in sizing the dc-link capacitor properly.

The purpose of this chapter is to study and calculate the amplitude of the low-frequency dc-link current and voltage ripple components in two level multiphase inverters under slightly unbalanced load conditions. For this reason, Fortescue’s and space vector transformations that are commonly used for analyzing multiphase systems have been briefly reviewed. Based on the amplitude of the double-fundamental voltage ripple component simple guideline for designing the dc-link capacitor is proposed. As a simpler but most utilized case, the three-phase inverter is examined first. Furthermore, the extension of the analysis to multiphase inverters is provided as well. Numerical simulations and experimental tests have been carried out for three-, five- and seven- phase inverters. Finally, a brief discussion of presented results is given in the last section.

5.2 Three-phase inverters with unbalanced load

This section presents a background in regard to transformations developed for three-phase systems, particularly focusing on Fortescue’s and space vector transformations. Different methods for calculating the current sequence components, as well as for estimating the current unbalance level are presented. Furthermore, the methods are adopted, and the amplitude of the low-frequency voltage ripple component is calculated on the basis of the corresponding dc-link current component. Finally, the dc-link capacitor design is proposed taking into account restrictions referred to the low-frequency voltage ripple. Numerical simulations have been carried out to validate analytical developments. Finally, both theoretical and numerical results have been confirmed by experimental tests.

5.2.1 Basic definitions and transformations for three-phase systems

The two-level three-phase inverter supplying a star connected passive- and/or motor-load is considered in the following. Configuration of the analyzed topology is shown in Fig. 3.6, Chapter 3. It is assumed that x_k are real quantities, related to the three-phase system (k =1, 2, 3) with sinusoidal waveforms and the same frequency, expressed as:

$$x_k(t) = \sqrt{2} X_k \cos\left(\omega t - (k-1)\frac{2\pi}{3}\right),\ k = 1, 2, 3. \tag{5.1}$$

Then, the three phasors $\bar{X}_k$ can be introduced as

$$\left[\bar{X}\right] = \left(\bar{X}_1, \bar{X}_2, \bar{X}_3\right), \tag{5.2}$$

according to

$$x_k(t) = \mathrm{Re}\left[\sqrt{2}\bar{X}_k e^{j\omega t}\right], \tag{5.3}$$

where X_k is the RMS value of $x_k(t)$, and $\vartheta=\omega t$, being $\omega=2\pi/T$ the fundamental angular frequency and T the fundamental period.

Applying the Fortescue's transformation [5.7] to (5.2) and introducing the concept of positive and negative sequence component, for the three-phase system the three symmetrical sequence components are obtained:

$$\left[\bar{X}_S\right] = \left(\bar{X}_0, \bar{X}_{+1}, \bar{X}_{-1}\right). \tag{5.4}$$

They can be defined as [5.8]:

$$\bar{X}_h = \frac{1}{3}\sum_{k=1}^{3} \bar{X}_k \alpha^{h(k-1)}, h = 0, +1, -1. \tag{5.5}$$

being $\alpha = e^{j\frac{2\pi}{3}}$.

The inverse transformation is given by

$$\bar{X}_k = \sum_{h=-1}^{1} \bar{X}_h \alpha^{-h(k-1)}, k = 1, 2, 3. \tag{5.6}$$

The phasor components can be finally obtained from the previous transformations (5.5) and (5.6), in a matrix form, as follows:

$$\left[\bar{X}_S\right]=\frac{1}{3}\begin{bmatrix}1 & 1 & 1\\ 1 & \alpha & \alpha^{-1}\\ 1 & \alpha^{-1} & \alpha\end{bmatrix}\left[\bar{X}\right], \tag{5.7}$$

$$\left[\bar{X}\right]=\begin{bmatrix}1 & 1 & 1\\ 1 & \alpha^{-1} & \alpha\\ 1 & \alpha & \alpha^{-1}\end{bmatrix}\left[\bar{X}_S\right]. \tag{5.8}$$

It can be noted that the only difference between direct and inverse transformations is in their opposite-sign exponents, and in the scaling coefficient. The product of their normalization factors is required to be 1/3.

Another transformation that can be applied to the real quantities expressed by (5.1) is the space vector transformation. It is formally similar to the Fortescue's symmetrical component transformation, but it is applied to the instantaneous phase quantities instead of phasors, giving the wider generality.

It has been proven that in three-phase system, it is enough to consider only one space vector ($\bar{x}_1$) and unique zero component (x_0). Space vector transformation is usually defined as:

$$x_0=\frac{1}{3}\sum_{k=1}^{3}x_k\ , \tag{5.9}$$

$$\bar{x}_1=\frac{2}{3}\sum_{k=1}^{3}x_k\,\alpha^{k-1}\ . \tag{5.10}$$

If sinusoidal waveforms with the same frequency are considered, as it is the case in (5.1), two previously reviewed transformations – symmetrical sequence and space vector transformation can be related. In order to show the relation between them, the quantities given by (5.1) can be rewritten in the following form [5.8]:

$$x_k=\frac{\sqrt{2}}{2}\left(\bar{X}_k e^{j\omega t}+\bar{X}_k^{*}e^{-j\omega t}\right), k=1,2,3. \tag{5.11}$$

Applying the space vector transformations (5.9) and (5.10) to (5.11), and taking into account the definition of symmetrical sequences given by (5.5), yields:

$$x_0=\mathrm{Re}\left[\sqrt{2}\bar{X}_0 e^{j\omega t}\right], \tag{5.12}$$

$$\bar{x}_1=\sqrt{2}\bar{X}_{+1}e^{j\omega t}+\sqrt{2}\bar{X}_{-1}^{*}e^{-j\omega t}\ . \tag{5.13}$$

Equation (5.13) shows that space vector $\bar{x}_1$ can be decomposed into two counter rotating vectors, a direct and an inverse, with a constant magnitude and opposite angular speed ±ω. The direct or counter clockwise rotating $e^{j\omega t}$ only exist in $\bar{X}_{+1}$, while the inverse or clockwise rotating $e^{-j\omega t}$ exist only in $\bar{X}_{-1}^{*}$. The magnitude of rotating vectors is equal to sqrt(2) of the magnitude of positive and negative symmetrical components of the same sequence.

Note that the previous definitions are general and can be used for any set of physical variables of the three-phase system, i.e. phase voltages, phase currents etc.

5.2.2 Low-frequency current and voltage ripple analysis

Concerning the three-phase inverters and space vector definition given by (5.10), the instantaneous power can be also written in terms of space vector components as

$$p = 3v_0 i_0 + \frac{3}{2}\bar{v}_1 \cdot \bar{i}_1 . \tag{5.14}$$

It can be noted that only voltage and current components of the same sequence interact and take part in the instantaneous power [5.8].

Since the output voltage of the inverter is assumed to be sinusoidal and symmetrical, only the direct rotating component of the voltage space vector is present. Referring to (5.13) it can be expressed as:

$$\bar{v}_1 = \sqrt{2}\bar{V}_{+1}e^{j\omega t} . \tag{5.15}$$

Applying (5.13) to the phase current yields

$$\bar{i}_1 = \sqrt{2}\bar{I}_{+1}e^{j\omega t} + \sqrt{2}\bar{I}_{-1}^{*}e^{-j\omega t} . \tag{5.16}$$

Introducing (5.15) and (5.16) in (5.14), the instantaneous power becomes

$$p = 3\left[V_{+1}I_{+1}\cos\varphi_{+} + V_{+1}I_{-1}\cos\left(2\omega t - \varphi_{-}\right)\right]. \tag{5.17}$$

It can be noted that the active power related to the first positive sequence component represents the average value of the instantaneous power related to the corresponding (first) space vector. Also, it is shown that the first negative current sequence component gives the contribution to the instantaneous power oscillation.

Considering input/output power balance over the switching period T_{sw}, as

$$V_{dc}\bar{i} = p , \tag{5.18}$$

and being

$$V_{+1} = \frac{mV_{dc}}{\sqrt{2}}, \tag{5.19}$$

the averaged input current component can be expressed as

$$\bar{i} = \frac{3}{\sqrt{2}}\left[mI_{+1}\cos\varphi_{+} + mI_{-1}\cos\left(2\omega t - \varphi_{-}\right)\right]. \tag{5.20}$$

The dc and the low-frequency input current components can be readily obtained from (5.20) as:

$$I_{dc} = \frac{3}{\sqrt{2}} mI_{+1}\cos\varphi_{+}, \tag{5.21}$$

$$\tilde{i} = \frac{3}{\sqrt{2}} mI_{-1}\cos\left(2\omega t - \varphi_{-}\right). \tag{5.22}$$

Based on (5.22) the amplitude (or the peak value) of the low-frequency input current component is calculated as:

$$\tilde{I}_{pk} = \frac{3}{\sqrt{2}} mI_{-1}. \tag{5.23}$$

The low-frequency dc-link voltage component $\tilde{v}(t)$ can be determined on the basis of the corresponding current component $\tilde{i}$ (5.22) and by considering the equivalent dc-link impedance Z_{2f}. Subscript $2f$ stands to highlight that the frequency at which the impedance is calculated is double-fundamental (i.e. 100Hz).

The following equation for the low-frequency voltage ripple component is obtained:

$$\tilde{v} = \frac{3}{\sqrt{2}} mI_{1-}Z_{2f}\cos\left(2\omega t - \varphi_{-} + \varphi_{Z}\right). \tag{5.24}$$

Introducing (5.23) in (5.24) the amplitude of $\tilde{v}(t)$ is given by:

$$\tilde{V}_{pk} = \tilde{I}_{pk} Z_{2f}. \tag{5.25}$$

5.2.3 Assessment of current sequence components

In the following, real quantities that are of interest related to the three-phase system are phase currents $i_k(t)$, k =1 to 3. As it was shown before, the current sequence compo-

nents can be calculated by applying the well-known Fortescue's transformation. Therefore, according to (5.7), the positive and negative sequence current components are given by:

$$\bar{I}_{+1} = \frac{1}{3}\left(\bar{I}_1 + \alpha\bar{I}_2 + \alpha^{-1}\bar{I}_3\right), \tag{5.26}$$

$$\bar{I}_{-1} = \frac{1}{3}\left(\bar{I}_1 + \alpha^{-1}\bar{I}_2 + \alpha\bar{I}_3\right), \tag{5.27}$$

where $\alpha = e^{j\frac{2\pi}{3}}$. Considering three-wire three-phase system, in the following analysis the zero-sequence component is equal to zero:

$$\bar{I}_0 = \frac{1}{3}\left(\bar{I}_1 + \bar{I}_2 + \bar{I}_3\right) = 0\,. \tag{5.28}$$

The calculation of the sequence components by (5.26) and (5.27) requires complex mathematical operations and precise instantaneous current measurements, since both - the current phasor's magnitude and angle are involved. That is why many approximated formulas have been proposed in the literature aiming to obtain sequence components from measuring the RMS of the currents and applying only simple mathematics.

The average of three phase RMS currents can be considered as an approximation of the positive current sequence component, as it will be shown in the following, and it is calculated as:

$$I_{+1} \approx I_{avg} = \frac{1}{3}\left(I_1 + I_2 + I_3\right). \tag{5.29}$$

A simple formula giving a good approximation of the negative sequence current component and avoiding the use of complex algebra is proposed in [5.9] and [5.10]. It is expressed as:

$$I_{-1} = \sqrt{\frac{2}{3}\left[\left(I_1 - I_{avg}\right)^2 + \left(I_2 - I_{avg}\right)^2 + \left(I_3 - I_{avg}\right)^2\right]}\,. \tag{5.30}$$

Equations (5.29) and (5.30) can be verified and proved by introducing the small deviations of the current phasors from the symmetric directions. For better understanding of the calculations, Fig. 5.1 shows the (complex) current phasors for a "small" unbalance. The angles β_2 and β_3 represent the deviations of the currents (dashed lines), assuming $\beta_1 = 0$.

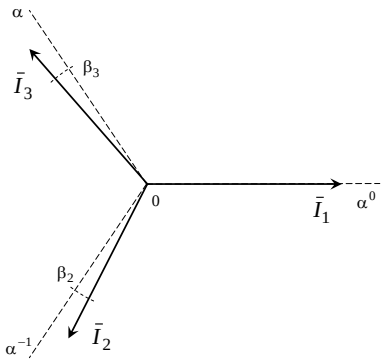


Fig. 5.1: Current phasors for a "small" unbalance.

Considering previous assumptions, the current phasors can be written as:

$$\begin{aligned}\bar{I}_1 &= I_1,\\ \bar{I}_2 &= I_2\alpha^{-1}e^{j\beta_2},\\ \bar{I}_3 &= I_3\alpha e^{j\beta_3}.\end{aligned} \tag{5.31}$$

Introducing (5.31) into (5.26) and (5.27), the positive and the negative sequence current components are rewritten as:

$$\bar{I}_{+1} = \frac{1}{3}\left(I_1 + e^{j\beta_2}I_2 + e^{j\beta_3}I_3\right), \tag{5.32}$$

$$\bar{I}_{-1} = \frac{1}{3}\left(I_1 + \alpha e^{j\beta_2}I_2 + \alpha^{-1}e^{j\beta_3}I_3\right). \tag{5.33}$$

Taking zero sequence component assumption (5.28) into account and considering (5.31), the following equation must be satisfied:

$$I_1 + \alpha^{-1}e^{j\beta_2}I_2 + \alpha e^{j\beta_3}I_3 = 0 \tag{5.34}$$

Introducing the assumption of "small" current unbalance, the exponential functions can be approximated as:

$$\begin{aligned}e^{j\beta_2} &= \left(1 + j\beta_2\right),\\ e^{j\beta_3} &= \left(1 + j\beta_3\right),\end{aligned} \tag{5.35}$$

Replacing (5.35) in (5.34), the angles β_2 and β_3 can be calculated as:

$$\beta_2 = -\frac{I_1 + I_2 - 2I_3}{\sqrt{3}I_2}, \tag{5.36}$$

$$\beta_3 = \frac{I_1 - 2I_2 + I_3}{\sqrt{3}I_3}. \tag{5.37}$$

Introducing (5.36) and (5.37) into (5.32) and (5.33), yields to:

$$\bar{I}_{+1} = \frac{1}{3}\left[I_1 + I_2 + I_3 - j\sqrt{3}\left(I_2 - I_3\right)\right], \tag{5.38}$$

$$\bar{I}_{-1} = \frac{1}{3}\left[2I_1 - I_2 - I_3 + j\sqrt{3}\left(I_2 - I_3\right)\right]. \tag{5.39}$$

The modulus of the two current sequence components (5.38) and (5.39) are:

$$I_{+1} \approx \frac{1}{3}\left(I_1 + I_2 + I_3\right), \tag{5.40}$$

$$I_{-1} = \frac{2}{3}\sqrt{I_1^2 + I_2^2 + I_3^2 - I_1I_2 - I_1I_3 - I_2I_3}. \tag{5.41}$$

It can be noted that equation (5.38) corresponds to (5.30) by considering (5.29).

Finally, an effort has been made in [5.11] to exactly calculate the positive- and negative- sequence components of a three-phase sinusoidal and unbalanced system on the basis of the RMS values of phase voltages. As said before, the expressions are developed for the voltages but since in this thesis the current sequence components are of interest, the equations are applied to the phase currents instead and shown in the following.

Namely, the positive and negative current sequence components are expressed as [5.11]:

$$I_{+1} = \sqrt{\frac{A_m^2 + \frac{4A_s^2}{\sqrt{3}}}{2}}, \tag{5.42}$$

$$I_{-1} = \sqrt{\frac{A_m^2 - \frac{4A_s^2}{\sqrt{3}}}{2}}, \tag{5.43}$$

where

$$A_m^2 = \frac{I_1^2 + I_2^2 + I_3^2}{3}, \tag{5.44}$$

$$A_s^2 = \sqrt{p(p-I_1)(p-I_2)(p-I_3)}, \tag{5.45}$$

$$p = \frac{I_1 + I_2 + I_3}{2}. \tag{5.46}$$

It has been confirmed that the exact and approximation formulas agree very closely for an unbalance up to 5%. By using the approximation formula the complex algebra is totally avoided and thus, it is a preferred way for calculating current sequence components. However, when unbalance increases the approximation formulas deviate from the true values and cannot be used for the precise calculations.

5.2.4 Definitions of the current unbalance level

Calculations of the voltage/current sequence components can be used for defining the unbalance level, known also in the literature as "unbalance factor". In the literature, there are four different methods for estimating the unbalance level. To mention again, the definitions usually refer to the voltage unbalance but the same can be applied to the currents what will be the case in following.

The first method requires measurements of both, current phasor's magnitude and angle and hence, the complex mathematical operations have to be performed. The other three are based on simple measurements of the RMS of phase currents and because of that are generally preferred.

The first method named "Symmetrical components method", defines the "true" unbalance factor (UF) as the ratio of the magnitude of the negative current sequence component to the magnitude of the positive current sequence component [5.12]. The percentage UF factor is expressed as:

$$UF(\%) = \frac{I_{-1}}{I_{+1}} \cdot 100. \tag{5.47}$$

The ANSI/NEMA-MG-14.34 standard defines unbalance as the ratio of the maximum (peak) deviation from the average phase RMS current to the average phase RMS current [5.1]. The unbalance factor is expressed as:

$$UF(\%) = \frac{I_{\max} - I_{avg}}{I_{avg}} \cdot 100 \tag{5.48}$$

where $I_{\max}$ is the current with the maximum deviation from the average current (5.29).

Another accurate procedure to calculate the level of unbalance comes from CIGRE (International Council on Large Electric Systems) where only RMS values of the phase currents are required. The expression is given by [5.13]:

$$UF(\%) = \sqrt{\frac{1-\sqrt{3-6\beta}}{1+\sqrt{3-6\beta}}} \cdot 100\,, \tag{5.49}$$

where

$$\beta = \frac{I_1^4 + I_2^4 + I_3^4}{\left(I_1^2 + I_2^2 + I_3^2\right)^2}\,. \tag{5.50}$$

Equation (5.49) can be used as another approximation of the negative current sequence component as:

$$I_{-1} = \sqrt{\frac{1-\sqrt{3-6\beta}}{1+\sqrt{3-6\beta}}} \cdot I_{+1}\,. \tag{5.51}$$

If the unbalance level is up to *UF*(%) = 5-10%, both expressions (5.41) and (5.51) give the same result for the negative current sequence component.

As the forth method for defining the unbalance level, the following expression is recommended by the IEEE [5.14]:

$$UF(\%) = \frac{I_{\max} - I_{\min}}{I_{avg}} \cdot 100\,, \tag{5.52}$$

being $I_{\max}$ and $I_{\min}$ the maximum and the minimum value among the three-phase currents, respectively.

Unlike the voltage unbalance measurements, where all four definitions give practically the same results, for current unbalanced measurements the choice of definition is more important. It is mostly due to the tendency of the current unbalance to be an order of magnitude larger than voltage unbalance and the tendency of the fundamental current phasors to vary in angle. The final choice of current unbalance definition should be based on the type of the load. ANSI/NEMA definition is preferred in case of electronic loads, however, the symmetrical components definition is preferred in case of inductive or resistive load [5.12].

5.2.5 Simulation and experimental results

To validate the analytical results, numerical simulations and experimental verification have been performed. Reference is made to SPWM with modulation index set to 0.5 and the switching frequency set to 2.5 kHz. Numerical simulations have been carried out by Matlab/Simulink. For experimental tests, the same DSP controlled two-level three-phase inverter shown in Fig. 3.12 (Chapter 3, section 3.6) was used. The dc source impedance was added between the external dc source and the dc-link, and has the following parameters: R_{dc} = 5.5Ω and L_{dc} = 27mH. The dc-link metal film capacitor has the value C_{dc} = 100μF. Measurements have been taken using two star-connected three-phase induction motors. The parameters of the motors are measured by the LCR meter Agilent 4263B and they are shown in Table 5.1.

Table 5.1: Load parameters.

	0.5 kW 3-phase IM	2.2 kW 3-phase IM
R	26.8 Ω	3.16 Ω
L	103 mH	20 mH

The RMS values of the phase currents are measured by digital clamp meter and the measured values are shown in Table 5.2 together with the dc supply voltages. They are used in (5.34) and (5.35) to calculate the angles β_2 and β_3, and in (5.39) to calculate the negative sequence current component. Obtained values, summarized in Table 5.3, are set in the simulations and the comparison between analytical, numerical and experimental results has been made.

Table 5.2: Measured current values and dc supply voltages for the two induction motors.

	0.5 kW 3-phase IM (φ=50°)	2.2 kW 3-phase IM (φ=60°)
V_{dc} (V)	98.8	50.2
I_1 (A)	0.749	2.241
I_2 (A)	0.763	2.256
I_3 (A)	0.768	2.23

Table 5.3: Calculated current sequence components for the two induction motors.

	0.5 kW 3-phase IM (φ=50°)	2.2 kW 3-phase IM (φ=60°)
I_{-1} (A)	0.011372	0.01507
I_{+1} (A)	0.76	2.2423
β_2 (rad)	0.018182	-0.00948
β_3 (rad)	-0.00677	-0.01063

The first set of measurements was done considering 0.5 kW three-phase induction motor (Table 5.1, left column). Simulation and experimental results are shown in Figs. 5.2 and 5.3, respectively. Fig. 5.4 shows the phase currents measured with the three LEM PR30 current probes for the purpose of verifying the RMS values measured with the digital clamp meter. Note that an accurate measurement procedure is essential to avoid any false readings or falsehoods in further analysis. Measured values are compared and the results are shown in Table 5.2.

Fig. 5.2 shows the instantaneous dc-link voltage with subtracted dc component (blue trace) together with its averaged value over the switching period (red trace). The averaged value is obtained applying moving average filter. Considering measured (Table 5.2) and calculated (Table 5.3) parameter values, the amplitude of the alternating dc-link voltage component corresponds to the one calculated by (5.23). In particular, $\tilde{v} = 0.615$V for m=0.5. The unbalance factor (UF), calculated by (5.45) and parameters shown in Table 5.3, is: UF=1.5%.

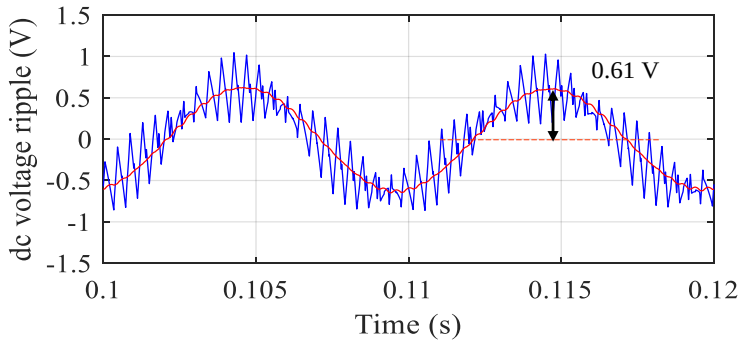


Fig. 5.2: Simulation results: the total instantaneous dc-link voltage ripple with subtracted dc component (blue trace) and its averaged value over T_{sw} (red trace).

Experimental results are shown by Yokogawa DLM 2024 oscilloscope screenshot in Fig. 5.3. The upper (blue) trace presents the total dc-link voltage ripple with subtracted dc

value. It was done by using the "ac coupling" function of the oscilloscope. The bottom (pink) trace presents the low-frequency dc-link voltage ripple component, obtained by filtering the total dc-link voltage ripple with built-in low pass filter of the oscilloscope. The amplitude of the alternating dc-link voltage component is slightly lower comparing to the numerically obtained results. This is due to the small measuring mistake caused by non-ideal measuring equipment.

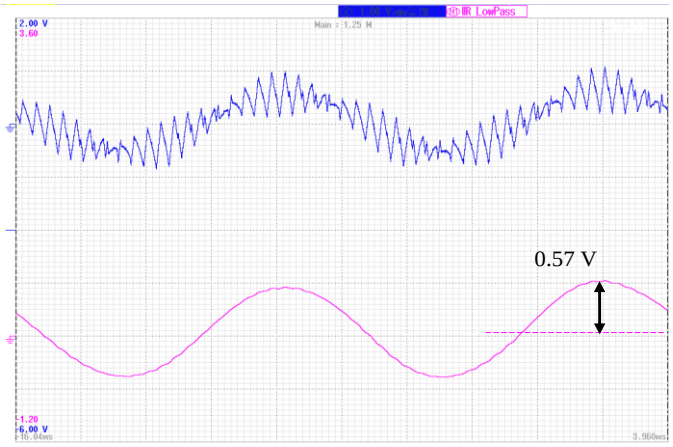


Fig. 5.3: Experimental results: the total dc-link voltage ripple in three-phase inverter (blue trace) and the low-frequency (filtered) voltage ripple component (pink trace).

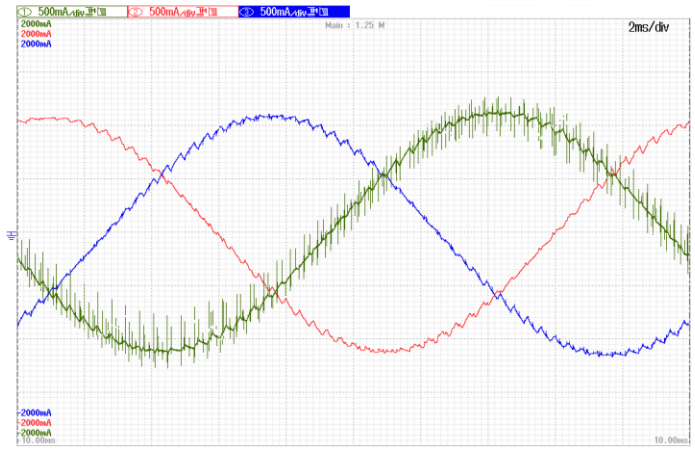


Fig. 5.4: Phase currents when the load is 0.5 kW three-phase induction motor.

The second set of measurements was done considering 2.2 kW three-phase induction motor (Table 5.1, right column). Simulation and experimental results are shown in Figs. 5.5 and 5.6, respectively. The waveforms of the measured output currents are shown in Fig. 5.7. The same measuring equipment was used as for the previous case.

Fig. 5.5 shows the instantaneous dc-link voltage with subtracted dc component (blue trace) together with its averaged value over the switching period (red trace). Considering measured (Table 5.2) and calculated (Table 5.3) parameter values, the amplitude of the alternating dc-link voltage component corresponds to the one calculated by (5.39). In particular, $\tilde{v}$ =0.81 V for m=0.5. The unbalance factor (UF), calculated by (5.45) and parameters shown in Table 5.3, is: UF=0.68%.

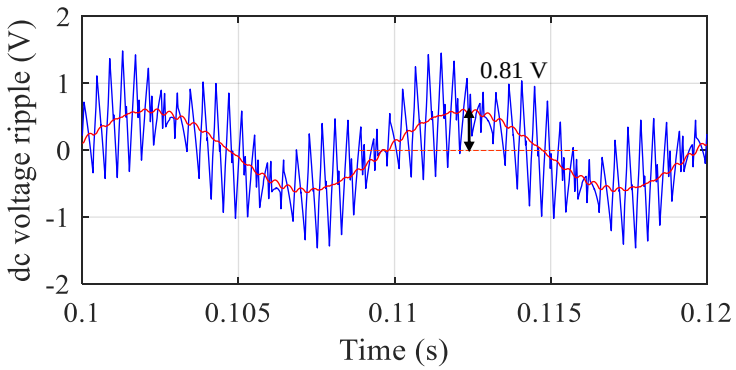


Fig. 5.5: Simulation results: the total instantaneous dc-link voltage ripple with subtracted dc component (blue trace) and its averaged value over T_{sw} (red trace).

Experimental results are obtained in the same way as for the first set of measurements. The results are shown in Fig. 5.6. A good matching between experimental, numerical and analytical results is achieved for all considered cases, confirming validity of the theoretical developments.

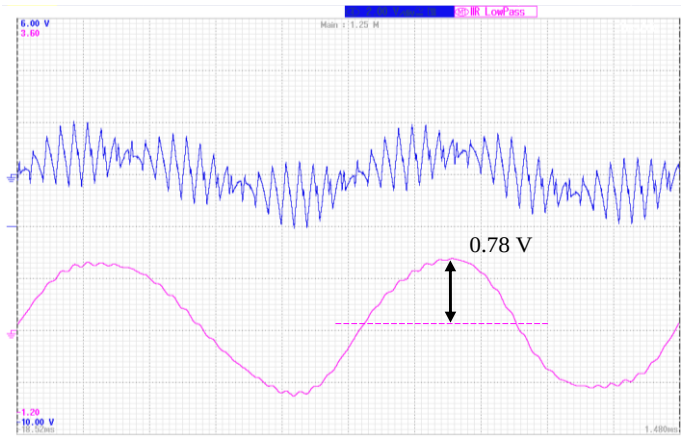


Fig. 5.6: Experimental results: the total dc-link voltage ripple in three-phase inverter (blue trace) and the low-frequency (filtered) voltage ripple component (pink trace).

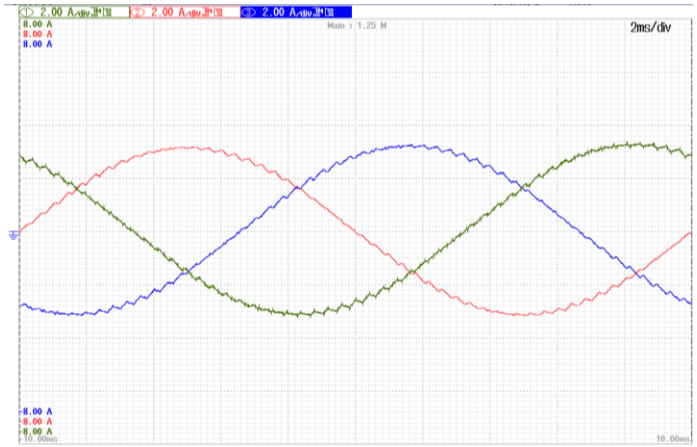


Fig. 5.7: Output currents when the load is 2.2 kW three-phase induction motor.

5.3 Multiphase inverters with unbalanced load

The analysis shown in the previous section for three-phase system has been extended for general *n*-phase system with an odd number of phases. Configuration of the analyzed inverter topology is shown in Fig. 4.1, Chapter 4. Firstly, two transformations for multiphase systems are briefly reviewed, and the amplitudes of the low-frequency current and voltage ripple components are calculated. Simulations and experimental results are provided for five- and seven-phase inverters. The dc-link capacitor design has been proposed on the basis of the requirements referred to the double-fundamental voltage ripple component. General conclusion follows the analysis.

5.3.1 Extended transformations for multiphase systems

Let us assume that x_k are real quantities related to the *n*-phase system (k =1 to n) with sinusoidal waveforms and the same frequency. Then, the *n* phasors $\bar{X}_k$ are introduced as

$$\left[\bar{X}\right] = \left(\bar{X}_1, \bar{X}_2, ..., \bar{X}_n\right), \tag{5.53}$$

according to

$$x_k(t) = \sqrt{2} X_k \cos\left(\omega t - \varphi_k\right) = \mathrm{Re}\left[\sqrt{2}\bar{X}_k e^{j\omega t}\right], \tag{5.54}$$

where X_k is the RMS value of $x_k(t)$ over the fundamental period $T=2\pi f$.

If the direct Fortescue's transformation is applied to (5.53), the *n* symmetrical sequence components are obtained:

$$\left[\bar{X}_S\right]=\left[\bar{X}_0,\bar{X}_{+1},...,\bar{X}_{+r},\bar{X}_{-r},...,\bar{X}_{-1}\right], \tag{5.55}$$

being $r = (n–1)/2$ (for odd n), and the direct transformation defined as [5.8]:

$$\bar{X}_{\pm h}=\frac{1}{n}\sum_{k=1}^{n}\bar{X}_k\alpha^{\pm h(k-1)}\ ,\ h=0,\ 1,\ldots,\ r \tag{5.56}$$

where $\alpha = e^{j\frac{2\pi}{n}}$.

The inverse transformation is given by:

$$\bar{X}_k=\sum_{h=-r}^{r}\bar{X}_h\alpha^{-h(k-1)},k=1,2,...n\ . \tag{5.57}$$

The previous transformations can be rewritten in a compact matrix form as follows

$$\left[\bar{X}_S\right]=\left[\alpha\right]^{-1}\left[\bar{X}\right], \tag{5.58}$$

$$\left[\bar{X}\right]=\left[\alpha\right]\left[\bar{X}_S\right], \tag{5.59}$$

where,

$$\left[\alpha\right]^{-1}=\frac{1}{n}\begin{bmatrix}1 & 1 & 1 & \cdots & 1\\ 1 & \alpha & \alpha^2 & \cdots & \alpha^{n-1}\\ 1 & \alpha^2 & \alpha^4 & \cdots & \alpha^{n-2}\\ \vdots & \vdots & \vdots & \ddots & \vdots\\ 1 & \alpha^{n-1} & \alpha^{n-2} & \cdots & \alpha\end{bmatrix}, \tag{5.60}$$

$$\left[\alpha\right]=\begin{bmatrix}1 & 1 & 1 & \cdots & 1\\ 1 & \alpha^{-1} & \alpha^{-2} & \cdots & \alpha\\ 1 & \alpha^{-2} & \alpha^{-4} & \cdots & \alpha^2\\ \vdots & \vdots & \vdots & \ddots & \vdots\\ 1 & \alpha & \alpha^2 & \cdots & \alpha^{n-1}\end{bmatrix}. \tag{5.61}$$

Another transformation most commonly used for analysing multiphase systems, due to the wider generality when compared to the Fortescue's, is space vector transformation. For *n*-phase system, space vector transformation and inverse transformation can be defined as [5.8]:

$$x_0 = \frac{1}{n}\sum_{k=1}^{n} x_k \,, \tag{5.62}$$

$$\bar{x}_h = \frac{2}{n}\sum_{k=1}^{n} x_k \alpha^{h(k-1)}, h = 1,2,...r \,, \tag{5.63}$$

$$x_k = x_0 + \sum_{h=1}^{r} \bar{x}_h \alpha^{h(k-1)}, k = 1,2,...n \,. \tag{5.64}$$

In order to show the relation between two previously reviewed transformations, symmetrical sequence and space vector transformations, for *n* sinusoidal waveforms with the same frequency, the quantities given by (5.54) are rewritten in the following form [5.8]:

$$x_k = \frac{\sqrt{2}}{2}\left(\bar{X}_k e^{j\omega t} + \bar{X}_k^* e^{-j\omega t}\right), k = 1,2,3,...n. \tag{5.65}$$

Applying (5.62) and (5.63) to (5.65), and taking into account (5.56), yields

$$x_0 = \mathrm{Re}\left[\sqrt{2}\bar{X}_0 e^{j\omega t}\right], \tag{5.66}$$

$$\bar{x}_h = \sqrt{2}\bar{X}_{+h} e^{j\omega t} + \sqrt{2}\bar{X}_{-h}^* e^{-j\omega t}, h = 1,2,...r \,. \tag{5.67}$$

Equation (5.67) is represented in Fig. 5.8. It is shown that each space vector component $\bar{x}_h$ can be decomposed into two counter-rotating vectors, a direct and an inverse, equal in magnitude to √2 of the magnitude of positive and negative symmetrical components of the same sequence, respectively, and with the opposite angular speed ±ω.

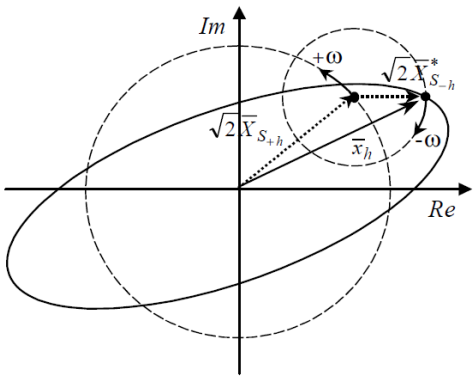


Fig. 5.8: Space vector decomposition in counter rotating components [5.8].

5.3.2 Low-frequency current and voltage ripple analysis

With reference to *n*-phase inverters and space vector definition given by (5.63), the instantaneous power can be expressed in terms of space vector components as [5.8]:

$$p = nv_0 i_0 + \frac{n}{2}\sum_{h=1}^{r} \bar{v}_h \cdot \bar{i}_h^{*}\,,\ h=1,\ 2,\ \ldots r. \tag{5.68}$$

It can be noticed that only the current and voltage components of the same sequence interact. Hence, the instantaneous power can be written as the sum of contributions of each sequence as:

$$p = \sum_{h=0}^{r} p_h\,, \tag{5.69}$$

being

$$p_0 = nv_0 i_0\,, \tag{5.70}$$

$$p_h = \frac{n}{2}\bar{v}_h \cdot \bar{i}_h^{*},\ h=1,\ 2,\ \ldots,\ r. \tag{5.71}$$

In considered case of sinusoidal and symmetrical phase voltages, only the direct rotating component of the voltage space vector is present, which is equal in magnitude to $\sqrt{2}$ of the magnitude of positive symmetrical component of the first sequence. Referring to (5.67) it can be expressed as:

$$\bar{v}_1 = \sqrt{2}\bar{V}_{+1}e^{j\omega t}\,. \tag{5.72}$$

Applying (5.67) to the phase current yields

$$\bar{i}_h = \sqrt{2}\bar{I}_{+h}e^{j\omega t} + \sqrt{2}\bar{I}_{-h}^{*}e^{-j\omega t} \tag{5.73}$$

Because of the interaction between current and voltage components of the same sequence, and due to the existence of only first positive voltage sequence component, the current component which will contribute to the instantaneous power is also the first sequence component. Introducing (5.72) and (5.73) in (5.68), the instantaneous power becomes

$$p = n\left[V_{+1}I_{+1}\cos\varphi_{+1} + V_{+1}I_{-1}\cos\left(2\omega t - \varphi_{-1}\right)\right]. \tag{5.74}$$

Considering the input/output power balance as in (5.18), and taking into account (5.19), the averaged input current component can be expressed as

$$\bar{i} = \frac{n}{\sqrt{2}}\left[mI_{+1}\cos\varphi_{+1} + mI_{-1}\cos\left(2\omega t - \varphi_{-1}\right)\right]. \tag{5.75}$$

The dc and low-frequency current components can be readily obtained from (5.75):

$$I_{dc} = \frac{n}{\sqrt{2}} mI_{+1}\cos\varphi_{+1}, \tag{5.76}$$

$$\tilde{i} = \frac{n}{\sqrt{2}} mI_{-1}\cos\left(2\omega t - \varphi_{-1}\right). \tag{5.77}$$

Based on (5.77) and introducing unbalance factor (UF) defined in (5.47), the amplitude of the low frequency dc-link current component can be expressed as:

$$\tilde{I}_{pk} = n\, I_{+1}\, m\, \frac{UF}{\sqrt{2}}\ . \tag{5.78}$$

It can be noticed in (5.78) that the amplitude is increasing by increasing the number of phases and if the same output current is assumed. However, for a fair comparison of inverter topologies with different phase numbers, the same apparent output power should be considered. Under such consideration, the amplitude of the double-fundamental dc current ripple is affected only by the unbalance factor.

The low-frequency voltage ripple component can be calculated on the basis of (5.77) and by considering the dc-link equivalent impedance Z_{2f} as:

$$\tilde{v} = Z_{2f}\ \frac{n}{\sqrt{2}} mI_{-1}\cos\left(2\omega t - \varphi_{-1} + \varphi_z\right), \tag{5.79}$$

The amplitude or the peak value of $\tilde{v}$ can be finally expressed as a function of unbalance factor as:

$$\tilde{V}_{pk} = n\, I_{+1}\, m\, \frac{UF}{\sqrt{2}} Z_{2f} \tag{5.80}$$

Note that equations (5.75) - (5.80) are practically the same as (5.20) - (5.25) obtained for the three-phase case. The only difference is the coefficient *n* (number of phases). The expression (5.80) is compact, however, comparing to the three-phase case the assessment of current sequence components becomes more complex for multiphase systems. In the following sub-section, some methods for calculating the negative sequence component, which is of interest for final low-frequency voltage ripple calculation, are shown.

5.3.3 Assessment of current sequence components

It has been shown above that the current sequence components can be calculated by applying the well-known Fortescue's transformation using (5.58) and (5.60). The drawbacks of applying such a method are complex mathematical operations and precise instantaneous measurements of current amplitudes and phase angles.

In general, each phase of a multiphase system can exhibit a different impedance on each sequence component of the current. Therefore, knowing the load impedances, the sequence current components $\bar{I}_S$ can be also determined from the voltage sequence components $\bar{V}_S$ and from equivalent impedance of each sequence circuit $\bar{Z}_S$ as:

$$\left[\bar{V}\right]=\left[\bar{Z}\right]\left[\bar{I}\right], \tag{5.81}$$

Applying (5.57) leads to

$$\left[\bar{V}_S\right]=\left[\bar{Z}_S\right]\left[\bar{I}_S\right], \tag{5.82}$$

being $\left[\bar{Z}_S\right]=\left[\alpha^{-1}\right]\left[\bar{Z}\right][\alpha]$.

Current sequence components can be finally calculated as:

$$\left[\bar{I}_S\right]=\left[\bar{Z}_S\right]^{-1}\left[\bar{V}_S\right]. \tag{5.83}$$

However, analytical calculation of a complex matrix $\left[\bar{Z}_S\right]^{-1}$ is cumbersome. More effective way to calculate sequence current components $\bar{I}_S$ knowing the load impedances, and by applying (5.58), is to calculate current phasors by Millman's equation.

If *n*-phase system with a symmetrical star-connected load structure is considered, it can be assumed that load impedances $\bar{Z}_k$ (k=1,2,…n) terminate in a common junction 0, Millman's theorem states that the voltage drop or potential difference between any point in the network (i.e. '0'') and the point 0 is equal to [5.15]:

$$\bar{V}_{0'0}=\frac{\sum_{k=1}^{n}\bar{V}_k\bar{Y}_k}{\sum_{k=1}^{n}\bar{Y}_k}, \tag{5.84}$$

where $\bar{V}_k$ is the voltage drop between the terminal k and the point 0 and $\bar{Y}_k=1/\bar{Z}_k$ is the admittance corresponding to the k-th impedance. As it can be noticed all quantities are

complex numbers. Phasor currents can be further easily calculated from the following equation:

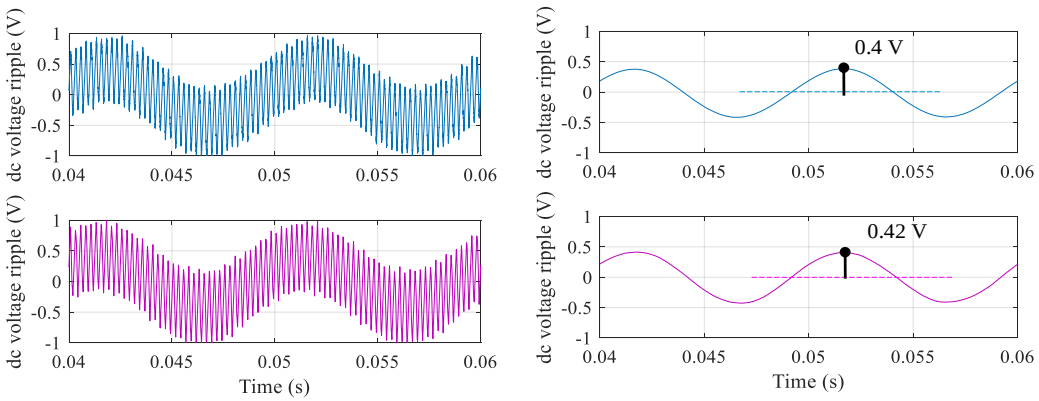
$$\bar{I}_k = \left(\bar{V}_k - \bar{V}_{0'0}\right)\bar{Y}_k . \tag{5.85}$$

5.3.4 Simulation and experimental results

In order to validate analytical developments for multiphase inverters with an odd number of phases supplying a slightly unbalanced load, comprehensive numerical simulations and experimental tests are conducted. Tests were performed for two-level five- and seven-phase inverters. Reference is made to SPWM with modulation index of 0.25 and 0.5. Switching frequency was set to 2 kHz. Simulation results have been obtained using Matlab/Simulink and all parameters were adjusted to corresponding values used in experiments. For experimental tests, the same setup shown in Fig. 4.16 (Chapter 4, section 4.6) was used. The two power phase angles (φ=20° and φ=70°) are arranged using *R-L* passive load. Parameters of the load are summarized in Table 4.3. The unbalance was introduced by adding resistor $R_0 = 4.5\Omega$ in one of the phases. The total dc-link capacitance is 209 μF, 0.03 Ω (ESR).

5.3.4.1 Five-phase

In case of five-phase inverter supplying five-phase *R-L* load, the dc-link voltage ripple across the dc-link capacitor was measured. Tektronix P5205A, 100 MHz, High Voltage differential probe was used. In order to verify the amplitude of the low-frequency voltage ripple component, the total dc-link voltage was filtered by applying a moving average filter in post-processing of the experimental data. Numerical simulations (pink traces) and experimental results (blue traces) are shown in Figs. 5.9-5.12, presenting the total dc-link voltage ripple and its double-fundamental (filtered) component. Two values of modulation index (m=0.25 and m=0.5) and two output phase angles (φ=20° and φ=70°) are considered. The RMS values of the phase currents, and calculated angles $\beta_{k,}$ k=1,2, … n which represent the deviations of the currents from the symmetric directions, are shown in the Tables 5.4-5.7 for corresponding operational conditions. The current sequence components have been calculated by applying Fortescue's transformation. For that purpose, Matlab script has been created. This script produces all current sequence components, their RMS values and angles, and the amplitude of the low-frequency voltage ripple component. Finally, the unbalance factor is calculated. Parameters of interest and analytically calculated amplitudes of the low-frequency voltage ripple component in different operational conditions, are summarized in Table 5.8 together with the corresponding simulations and experimental results. Only the first current sequence components (+ and -) are introduced since they were of interest for the calculations.

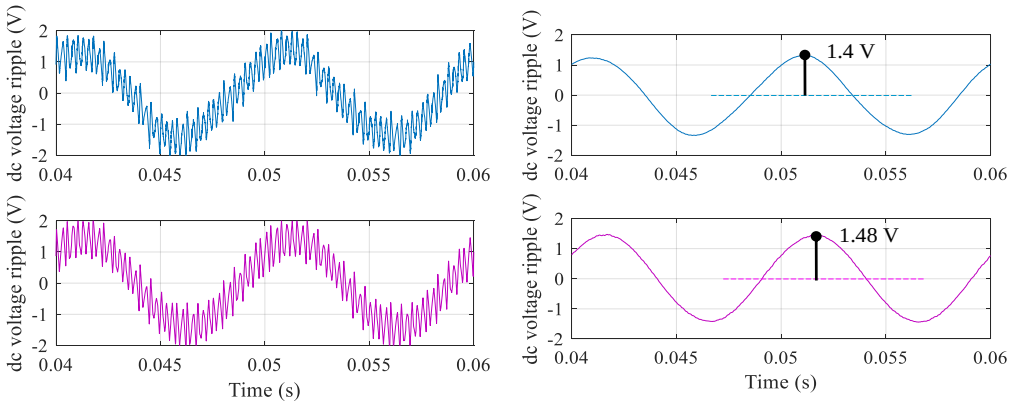


(a) **(b)**

Fig. 5.9: The total dc-link voltage ripple (a) and its low-frequency component (b): simulations (blue traces) and experimental results (pink traces) over a fundamental period for φ= 20°, m = 0.25.

Table 5.4: Measured phase currents RMS and angles' deviations for φ= 20° and m = 0.25.

φ= 20°, m=0.25	**1**	**2**	**3**	**4**	**5**
I (A)	2.158	2.0697	2.0456	2.1171	1.8276
β	0	0.11º	2.45º	3.75º	0.89º

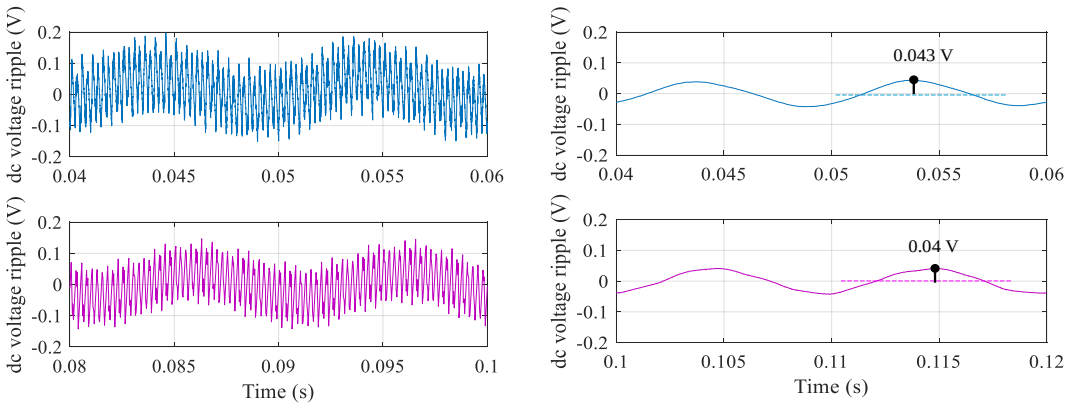


(a) **(b)**

Fig. 5.10: The total dc-link voltage ripple (a) and its low-frequency component (b): simulations (blue traces) and experimental results (pink traces) over a fundamental period for φ= 20°, m = 0.5.

Table 5.5: Measured phase currents RMS and angles' deviations for φ= 20° and m = 0.5.

φ= 20°, m=0.5	**1**	**2**	**3**	**4**	**5**
I (A)	3.995	3.789	3.757	3.873	3.356
β	0	0.28º	2.44º	3.84º	0.92º

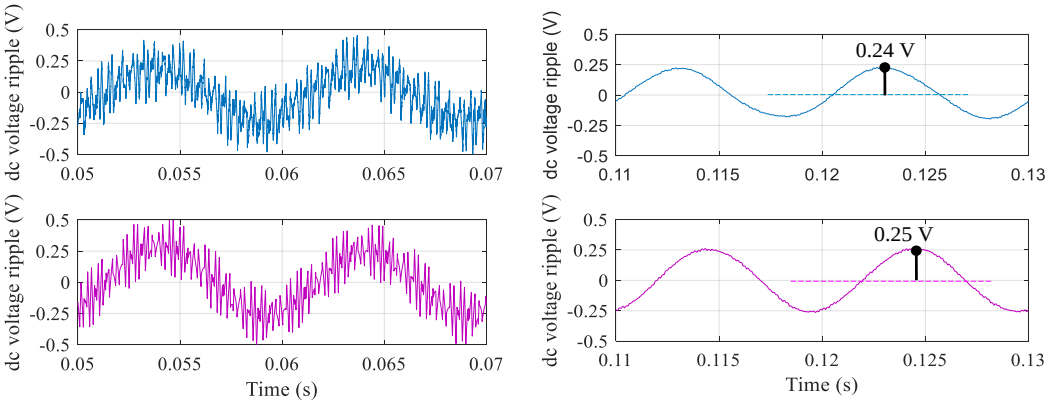


(a) **(b)**

Fig. 5.11: The total dc-link voltage ripple (a) and its low-frequency component (b): simulations (blue traces) and experimental results (pink traces) over a fundamental period for φ= 70°, m = 0.25.

Table 5.6: Measured phase currents RMS and angles' deviations for φ= 70° and m = 0.25.

φ= 70°, m=0.25	**1**	**2**	**3**	**4**	**5**
I (A)	0.779	0.796	0.7912	0.7834	0.7842
β	0	3.07º	0.77º	0.4º	1º



(a) **(b)**

Fig. 5.12: The total dc-link voltage ripple (a) and its low-frequency component (b): simulations (blue traces) and experimental results (pink traces) over a fundamental period for φ= 70°, m = 0.5.

Table 5.7: Measured phase currents RMS and angles' deviations for φ= 70° and m = 0.5.

φ= 70°, m=0.5	**1**	**2**	**3**	**4**	**5**
I (A)	1.1524	1.581	1.562	1.539	1.5405
β	0	3.07º	2.25º	2.75º	3.67º

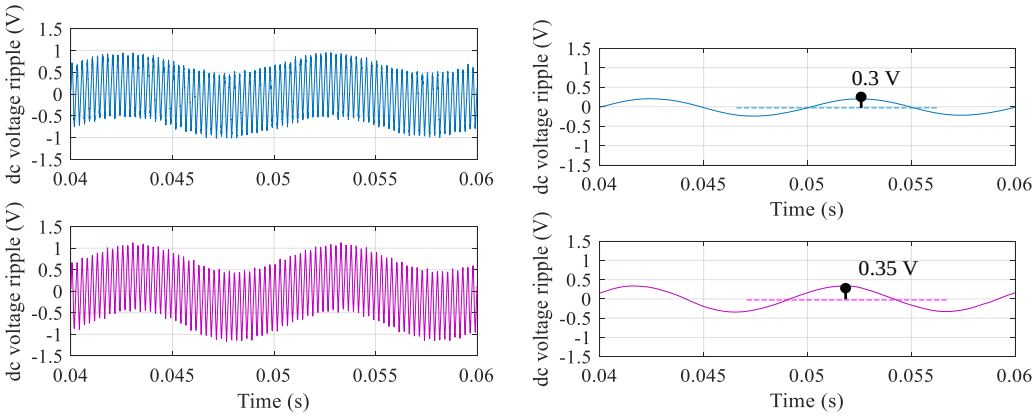
For the reason of comparison, analytical, numerical and experimental results are summarized in Table 5.8. A good matching in the amplitude of the double-fundamental dc-link voltage ripple is achieved, for all considered operational conditions, confirming the proposed analytical developments.

Table 5.8: Current sequence components of interest, unbalance factor and comparison within the dc voltage ripple amplitudes for different operational conditions.

	φ = 20º		φ = 70º	
	m = 0.25	*m* = 0.5	*m* = 0.25	*m* = 0.5
I_{+1} (A)	2.0427	3.7446	0.7866	1.5489
I_{-1} (A)	0.0742	0.1291	0.0071	0.0225
UF (%)	3.6	3.45	0.91	1.45
Calc. $\tilde{I}_{pk}$	0.065	0.228	0.0063	0.04
Calc. $\tilde{V}_{pk}$	0.423	1.479	0.04	0.25
Sim. $\tilde{V}_{pk}$	0.42	1.48	0.04	0.25
Exp. $\tilde{V}_{pk}$	0.4	1.4	0.043	0.24

5.3.4.2 Seven-phase

In case of seven-phase inverter supplying seven-phase *R-L* load, the dc-link voltage ripple across the dc-link capacitor has been measured. Measurements are taken and the experimental data are post-processed in the same way as explained before for five-phase inverter. Numerical simulations (pink traces) and experimental results (blue traces) are shown in Figs. 5.13-5.16, presenting the total dc-link voltage ripple and its filtered double-fundamental component. Four different operational conditions are considered. The RMS values of the phase currents, and calculated angles $\beta_{k,}$ k=1,2, … n, are shown in the Tables 5.9-5.12 for corresponding cases. For a sake of comparison, parameters of interest and the calculated and measured amplitudes of the low-frequency voltage ripple component in different operational conditions are summarized in Table 5.13.

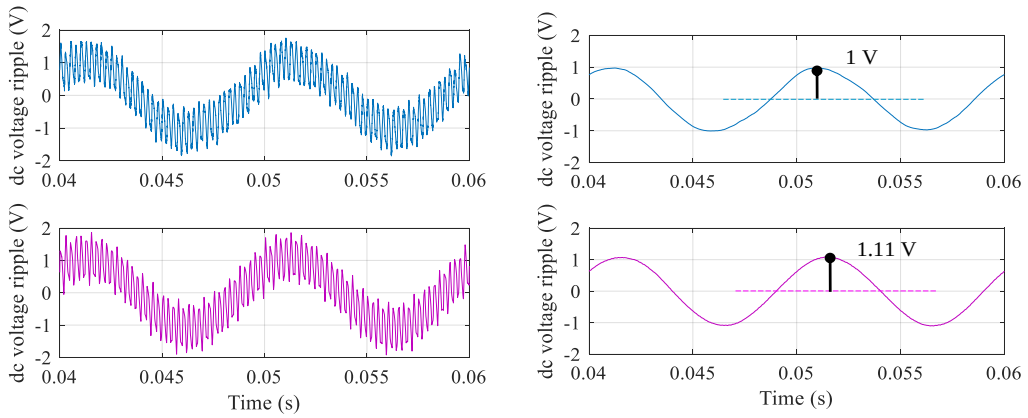


(a) **(b)**

Fig. 5.13: The total dc-link voltage ripple (a) and its low-frequency component (b): simulations (blue traces) and experimental results (pink traces) over a fundamental period for φ= 20°, m = 0.25.

Table 5.9: Measured phase currents RMS and angles' deviations for φ= 20° and m = 0.25.

φ= 20°, m=0.25	**1**	**2**	**3**	**4**	**5**	**6**	**7**
I (A)	2.125	2.091	2.056	2.048	2.067	2.103	1.845
β	0	0.39º	0.127º	0.884º	1.656º	1.927º	1.727º

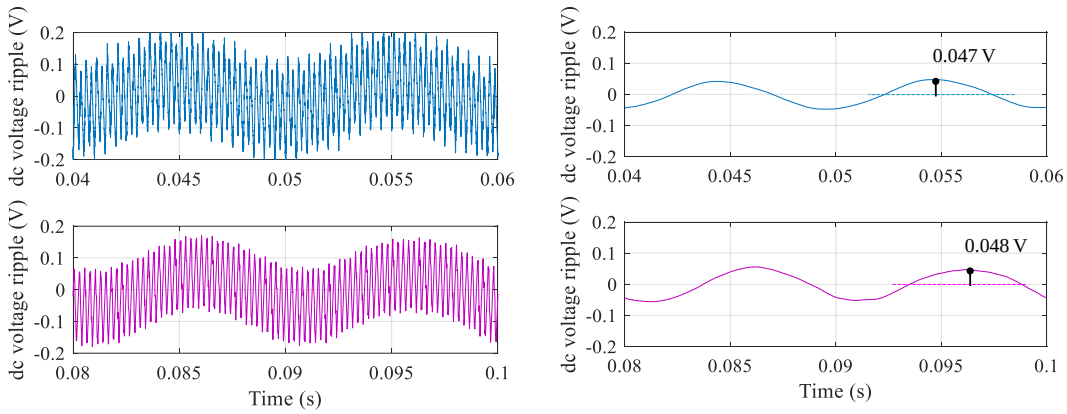


(a) **(b)**

Fig. 5.14: The total dc-link voltage ripple (a) and its low-frequency component (b): simulations (blue traces) and experimental results (pink traces) over a fundamental period for φ= 20°, m = 0.5.

Table 5.10: Measured phase currents RMS and angles' deviations for φ= 20° and m = 0.5.

φ= 20°, m=0.5	**1**	**2**	**3**	**4**	**5**	**6**	**7**
I (A)	3.772	3.702	3.646	3.636	3.663	3.727	3.272
β	0	0.48º	0.073º	0.884º	1.656º	1.927º	1.45º

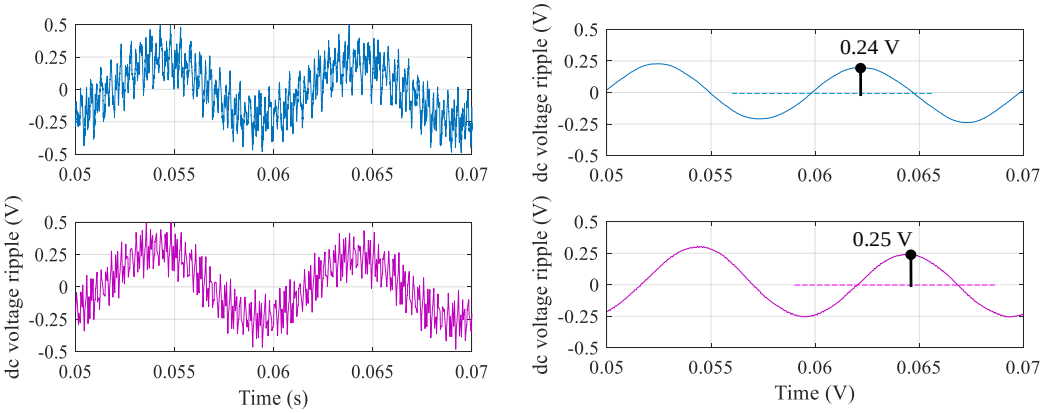


(a) **(b)**

Fig. 5.15: The total dc-link voltage ripple (a) and its low-frequency component (b): simulations (blue traces) and experimental results (pink traces) over a fundamental period for φ= 70°, m = 0.25.

Table 5.11: Measured phase currents RMS and angles' deviations for φ = 70° and m = 0.25.

φ= 70°, m=0.25	**1**	**2**	**3**	**4**	**5**	**6**	**7**
I (A)	0.772	0.794	0.793	0.787	0.783	0.781	0.785
β	0	2.86	2.44º	2.234º	2.41º	2.78º	3.21º



(a) **(b)**

Fig. 5.16: The total dc-link voltage ripple (a) and its low-frequency component (b): simulations (blue traces) and experimental results (pink traces) over a fundamental period for φ= 70°, m = 0.5.

Table 5.12: Measured phase currents RMS and angles' deviations for φ= 70° and m = 0.5.

φ= 70°, m=0.5	**1**	**2**	**3**	**4**	**5**	**6**	**7**
I (A)	1.51	1.563	1.5606	1.5464	1.5344	1.5316	1.5397
β	0	3.49º	2.95º	2.73º	3.006º	3.377º	3.82º

Analytically calculated dc low-frequency voltage ripple amplitudes are shown together with simulations and experimental results in Table 5.13. Also, the first current sequence components and unbalance factor are calculated for all considered operational conditions. A satisfactory matching is achieved between the results confirming the analytical developments.

Table 5.13: Current sequence components of interest, unbalance factor and comparison within the dc voltage ripple amplitudes for different operational conditions.

	φ = 20º		φ = 70º	
	m = 0.25	m = 0.5	m = 0.25	m = 0.5
I_{+1} (A)	2.0474	3.6306	0.7842	1.5405
I_{-1} (A)	0.042	0.0693	0.0083	0.0157
UF (%)	2.05	1.91	1.06	1.02
Calc. $\tilde{I}_{pk}$	0.052	0.1715	0.0103	0.0388
Calc. $\tilde{V}_{pk}$	0.33	1.11	0.05	0.25
Sim. $\tilde{V}_{pk}$	0.35	1.1	0.048	0.25
Exp. $\tilde{V}_{pk}$	0.3	1	0.047	0.024

5.4 Dc-link capacitor design based on low-frequency voltage ripple component

In this section, design of the dc-link capacitor in multiphase inverters is proposed considering requirements referred to the amplitude of the double-fundamental frequency dc voltage ripple component calculated in the previous sections.

According to (5.80), the dc-link low-frequency voltage ripple component depends on the total dc link impedance calculated at the double-fundamental frequency and on the unbalanced factor. The total dc-link impedance is the equivalent of parallel dc source impedance and the reactance of the dc-link capacitor. In this thesis the dc-link equivalent impedance is modelled in the same way for all analyzed voltage source inverter topologies and the expression is given by (2.13) in Chapter 2 (sub-section 2.3.1). Therefore, the amplitude of the corresponding dc-link voltage ripple is expressed as:

$$\tilde{V}_{pk} = \frac{n}{\sqrt{2}} m\, I_{+1} UF \frac{1}{2\omega C} \sqrt{\frac{R^2 + (2\omega L)^2}{R^2 + \left(2\omega L - \frac{1}{2\omega C}\right)^2}}, \tag{5.86}$$

where R and L are the dc source resistance and inductance, respectively, C is the dc-link capacitance, and $\omega=2\pi f$, f is the fundamental frequency.

The expression given by (5.86) can be used for dc-link capacitor sizing. However, it is a rather bulky calculation. As already discussed in Chapter 2, a reasonable simplification can be introduced having a high dc source impedance. In such a case the dc link equivalent impedance can be simplified and expressed as:

$$Z_{2f} \approx \frac{1}{2\omega C} \ . \tag{5.87}$$

Therefore, under the aforementioned assumption for a dc source, the amplitude of the double-fundamental dc voltage ripple (5.86) can be simplified as:

$$\tilde{V}_{pk} = \frac{n}{\sqrt{2}} m\, I_{+1} UF \frac{1}{2\omega C} \ . \tag{5.88}$$

Finally, given $\tilde{V}_{pk}$ and the unbalance factor as a condition, the dc-link capacitor can be designed using the following expression:

$$C \geq \frac{n}{\sqrt{2}} m\, I_{+1} UF \frac{1}{2\omega \tilde{V}_{pk}} \ . \tag{5.89}$$

It can be concluded that from the point of view of the dc-link capacitor sizing, if the same apparent power is considered within compared multiphase inverter topologies, there are no benefits in increasing the number of phases because the amplitude of the low-frequency voltage ripple component depends only on the level of unbalance (UF).

5.5 Discussion

In this chapter, a small degree of unbalance that is present in practice in every standard multiphase ac motor has been discussed and its effect on the dc-link variables has been studied. Namely, the unbalance in the load, although it is in order of a few percent in considered cases, introduces a double-fundamental frequency instantaneous power oscillation. This reflects in current and voltage low-frequency ripple on the dc-link inverter side. Therefore, the amplitudes of the two low-frequency ripple components are calculated. For the reason of analytical developments Fortescue's and space vector transformations are briefly reviewed.

Based on the amplitude of corresponding voltage ripple component simple guideline for designing the dc-link capacitor is proposed. As a simpler but more utilized case, the analysis are firstly carried out for the three-phase inverter. Further on, the extension to multiphase inverters with an odd number of phases is provided as well. The numerical simulations and experimental tests have been performed for five- and seven-phase inverters considering different operational conditions. Correctness of analytical developments and calculations is confirmed for all the cases.

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Chapter 6

Conclusion and Outlook

6.1 Summary and conclusions

This thesis deals with the analysis, development, numerical and experimental verifications of dc-link low–frequency and switching frequency voltage ripple components in two-level single-phase and multiphase voltage source inverters. The analysis is carried out under balanced and slightly unbalanced load conditions. Two most popular PWM techniques, sinusoidal and space vector, are considered for the multiphase inverters with an odd number of phases. Although some general steps in the dc-link current and voltage ripple analysis are described, single-, three-, five- and seven- phase cases are specifically considered for theoretical findings.

Based on the literature survey, the analysis of the dc-link inverter variables in all examined inverter topologies is mostly based on the RMS calculations. However, there was a lack of analysis related to the peak-to-peak dc voltage ripple behavior. In this thesis, the peak-to-peak dc-link voltage ripple envelopes are calculated as a function of operational conditions: modulation index, the amplitude of output current, and power phase angle. The analysis has been based on the corresponding dc current components and by considering a non-ideal dc source. Maximum of the peak-to-peak voltage ripple amplitude is determined as a function of modulation index for different output phase angles and, based on it, the dc-link capacitor design is proposed. Obtained equations for dc-link capacitor sizing are simple and can be readily applied. Furthermore, they allow the more stringent requirements on the dc-link capacitor size reduction to be met.

The comparison between different two-level multiphase inverter topologies in terms of the peak-to-peak voltage switching ripple envelope has been carried out. It has been found that, from the point of view of the dc-link capacitor size and by considering the same apparent power among compared inverters, there are no benefits in increasing the number of phases greater than seven since the maximum peak-to-peak value of the dc voltage switching ripple amplitude saturates for the higher number of phases.

It has been verified that theoretically balanced loads, such as multiphase ac motors, show in practice a certain degree of current unbalance, in order of a few percent, introducing a small instantaneous power oscillation at double-fundamental frequency. This reflects

in current and voltage low-frequency ripple on the dc-link inverter side. For the reason of analyzing this ripple component, the current sequence components are calculated. Based on the negative current sequence component and by considering the equivalent dc-link impedance calculated at the dominant double-fundamental frequency, the amplitude of the corresponding dc-link voltage ripple component is calculated. The investigation is firstly done for three-phase inverters, but the extension to the general *n*-phase inverters is provided as well. Finally, the design of the dc-link capacitor in multiphase inverters is proposed considering requirements referred to dc voltage ripple at double-fundamental frequency.

For all theoretical developments, numerical and experimental verifications are provided, showing always a good matching between measured dc voltage ripple and the estimated amplitude.

6.2 Outlook

As a future research perspective, the complete extension of the dc-link analysis to multilevel inverter topologies can be considered. Some preliminary analysis has been already developed within the working group for neutral point clamped (NPC) and flying capacitors (FC) configurations. The attention has been mostly paid to the low-frequency voltage ripple component. However, it would be of interest to relate the size of the capacitors to the corresponding voltage switching ripple component, for the reasons given in previous chapters, and by following the methodology presented in this thesis.

The analysis related to the dc-link inverter variables can be extended considering also discontinuous and/or asymmetrical modulation techniques, and their possible effect on the maximum peak-to-peak voltage ripple amplitude can be examined.

As another possible future work direction, the extension of the proposed analysis to voltage source inverters which comprise rectifiers or switching dc supplies, could be also considered. In that case, the analysis becomes more complex since the dc-link ripple components introduced by both converters are interfering. Therefore, their mutual contribution should be taken into consideration.

Although the contribution of the dc-link capacitor's parasitic elements was found to be almost negligible for the considered cases in this thesis, in certain applications and types of the capacitor, the effect of above mentioned elements on capacitor's performance can be significant. Therefore, in such applications, the analysis of the dc-link variables should be extended taking into consideration the equivalent series resistance and/or the equivalent series inductance.

Finally, further research should also attempt to simplify the calculation of the current sequence components in multiphase systems. Although the sequence components can be calculated by applying the well-known Fortescue's transformation, the mathematical

operations are complex and precise instantaneous current measurements are required. It would be interesting to find a simpler way for calculating the sequence components, enabling a more effective analysis of multiphase inverters under unbalanced load conditions.