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Robustness and durability aspects in the design of power management circuits for IoT applications

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Esame finale anno 2019

To all my families,
past, present and future

Acknowledgments

Yet another chapter in my life has almost come to an end. During these three years some people has walked out, some other has thankfully appeared, but on the edge of forties, so many times I found myself wondering where I had actually arrived and which was my place. And the weird thing is that now I realize that it would take more than one hundred pages thesis to thanks all who deserve.
Thanks to my parents and my sister, who in a sense brought me where I am, and who I often treat worse than they ever treated me.
Thanks to Roberto, who is much more than a chief for me and taught what sharing means, and thanks to Emanuel, who is that kind of honest friend who everyone should have and who assisted me in the darkest hour.
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Research is a demanding word, and I feel like I'm going to look for till the end, even though I don't know what.

Thank you all
Matteo

Il cammino fatale, incessante, spesso faticoso e febbrile che segue l'umanità per raggiungere la conquista del progresso, è grandioso nel suo risultato, visto nell'insieme, da lontano. Nella luce gloriosa che l'accompagna dileguansi le irrequietudini, le avidità, l'egoismo, tutte le passioni, tutti i vizi che si trasformano in virtù, tutte le debolezze che aiutano l'immane lavoro, tutte le contraddizioni, dal cui attrito sviluppasi la luce della verità. [...] Solo l'osservatore, travolto anch'esso dalla fiumana, guardandosi attorno, ha il diritto di interessarsi ai deboli che restano per via, ai fiacchi che si lasciano sorpassare dall'onda per finire più presto, ai vinti che levano le braccia disperate, e piegano il capo sotto il piede brutale dei sopravvegnenti, i vincitori d'oggi, affrettati anch'essi, avidi anch'essi d'arrivare, e che saranno sorpassati domani

Giovanni Verga
I Malavoglia
Prefazione

Abstract

With the increasing interest in the heterogeneous world of the "Internet of Things" (IoT), new compelling challenges arise in the field of electronic design, especially concerning the development of innovative power management solutions in both integrated and discrete systems. This real technological revolution establishes its foundations in the dissemination and exploitation of distributed IoT smart nodes, with diversified sensing and actuation capabilities. Being this diffusion a consolidated reality nowadays, emerging needs like lifetime, durability and robustness are becoming the new watchwords in the research field relating to such systems. Despite the wide range of different perspective and applications which can be associated in the scope of IoT, power management is a common ground which can dramatically improve service life and confidence in these devices. For instance, the possibility to design nodes which do not need external power supply but operates thanks to energy storages (e.g. batteries), and which therefore can be easily deployed in sparse places, is a crucial point in this scenario. Moreover, the development of autonomous nodes which are substantially maintenance free, and which therefore can be placed in unreachable or harsh environments and have longer operating times is another enabling aspect for the exploitation of this technology. In this respect, the study of energy harvesting techniques is increasingly earning interest again. Ultimately, in order to ensure high performances to IoT devices in terms of lifetime, durability and robustness, innovative power management solutions are required, which are able to efficiently extract and convert power from the available sources, be they harvesting or storage sources, and cleverly distribute the obtained power to the various circuits of the node.

Along with efficiency aspects, degradation aspects are the other main research field with respect to lifetime, durability and robustness of IoT devices, especially related to aging mechanisms which are peculiar in power management and power conversion circuits, like for example battery wear during usage or hot-carrier degradation (HCD) in power MOSFETs. Developing new architectures aiming at limiting the conditions which mainly contribute to degradation is surely an interesting perspective, however new approaches are gaining interest aiming at monitoring the state of health of the involved devices and potentially report to the user the actual degradation level or even the imminent failure of the device itself. As a consequence, the user can intervene in order to prevent the failure or in order to compensate the possible efficiency losses of the system caused by the degradation.

In this thesis different aspects related to lifetime, durability and robustness in the field of power management circuits are studied, leading to interesting contributions.

Innovative designs of DC/DC power converters are studied and developed, especially related to reliability aspects of the use of electrochemical cells as power sources. The proposed solutions limit some recognized stress conditions for

electrochemical cells, which are normally associated to common switching converters, with a resulting increase in battery lifetime.

Moreover, an advanced IoT node is proposed, based on energy harvesting techniques, which features an intelligent dynamically adaptive power management circuit which allows the node to work in a wider range of operating conditions, resulting in longer lifetime and improved robustness, and with the best available data-rate.

As a further contribution, a novel algorithm is proposed, which is able to effectively estimate the efficiency of a DC/DC converter for photovoltaic applications at runtime. In this specific case, the analyzed aspect of the converter is its maximum-power-point-tracking module (MPPT), which is responsible for maintaining the photovoltaic source in its best working point for power extraction. The proposed solution is able to determine if the MPPT module had potentially degraded over time.

Finally, an innovative DC/DC power converter with embedded monitoring of hot-carrier degradation in power MOSFETs is designed. Additional circuits are proposed which are able to estimate, during the normal operation of the converter, the degradation level of the power switches, by means of the variation of their intrinsic on-resistance, and report this information to the user.

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Chapter 1

Introduction

Internet of Things (IoT) is an innovative technology in which a large number of electronic devices are connected together through different communication layers, providing a wide range of heterogeneous information that can be collected and elaborated together in a typical Big Data environment (Fig. 1). This new interrelated architecture represents a promising approach in order to tackle complex management problems where multiple aspects effectively contribute to the identification of the best solution. In a typical IoT application, a mesh of distributed sensor nodes is used to acquire information about environmental conditions (temperature, humidity, pressure etc.), positioning and movement of objects or living things, common habits (spending patterns, preferential behavior, etc.). All these data are then transmitted to an elaboration center through various communication techniques, usually implying the use of wireless transceiver operating with different hardware/software protocols, accordingly to desired distance, data-rate, kind of information, and so on. Inside the elaboration center, this large volume of data, both structured and unstructured, often redundant, constitutes the basis for a Big Data elaboration. Through dedicated mathematical and statistical algorithms, these chaotic pieces of information are collected and combined together in order to obtain new kind of useful data, as for example to forecast particular events or needs, to provide targeted improvement techniques for a specific process, to generate personalized solution and so on.

Fig. 1 Internet of Things (IoT) technology scenario. (Source: https://www.sixcommgroup.it)

In the last few years Internet of Things has become a consolidated reality from an industrial point of view and a very fruitful field of research in academic domain. Nevertheless growing trend is far from slowing down, and recent studies show how expected trend will lead to more than 75 billion installed devices by the end of 2025 (Fig. 2) [1].

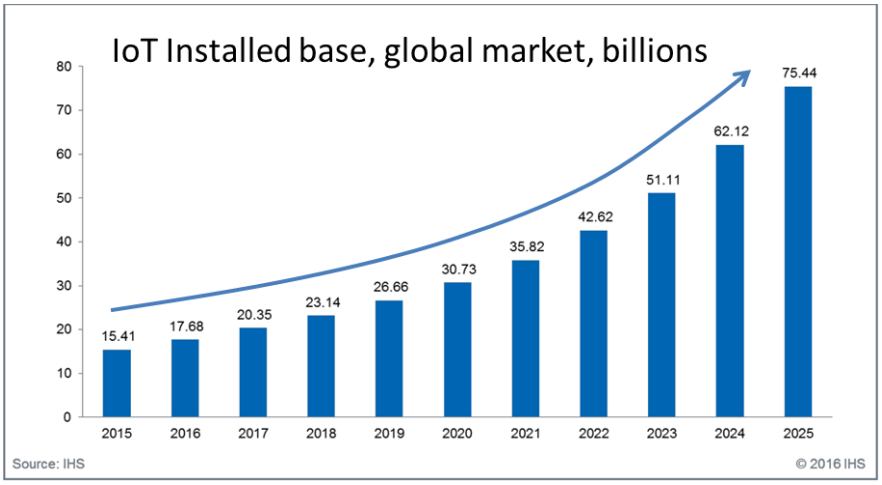

Fig. 2 IoT installed devices growth and forecast (Source: IHS technology - IoT platforms: enabling the Internet of Things – March 2016)

Due to this massive growth new perspectives are gaining more importance especially related to the peculiar application field of such devices. As a matter of fact, IoT nodes are often expected to operate in wireless mode while installed in unreachable and harsh locations, so specific aspects aiming at ensuring stable behavior over time are increasingly discussed. As a consequence, concepts like lifetime, durability, robustness are becoming the new watchwords in the research field related to IoT systems.

1.1 IoT devices and applications: a heterogeneous world

Recent market researches show an interesting picture of the global share of IoT devices and applications (Fig. 3) [2]. There is a huge variety of different sectors which can be potentially affected by this technology, comprising both consumer and enterprise fields such as wearable sensors, smart tags for fitness, work aids, health monitoring, home management and others.

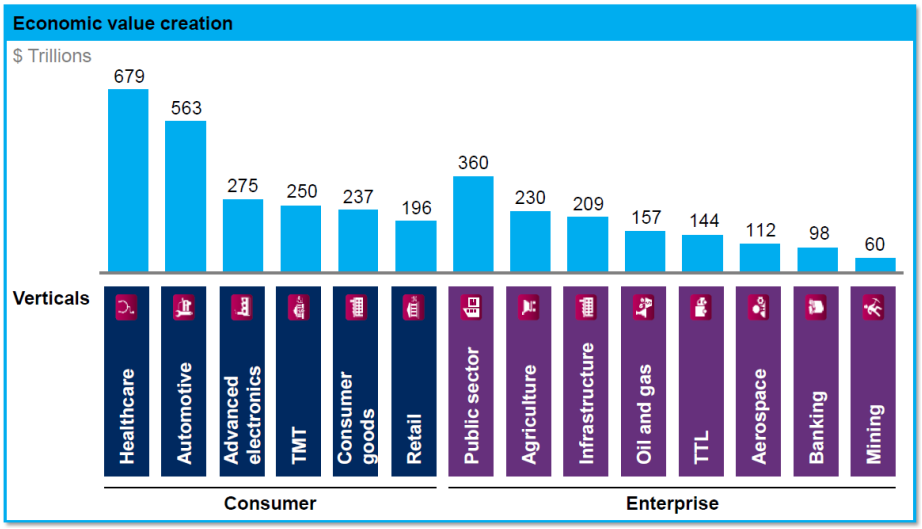

Fig. 3 Heterogeneous distribution of installed applications in IoT market (McKinsey Global Institute analysis - The IoT opportunity – Are you ready to capture a once-in-a lifetime value pool? – June 2016)

The heterogeneity of such devices can be related to a wide range of different aspects, specifically for what concerns:

- The kind of acquired data – environmental / healthcare / localization / statistical / …
- The communication protocol – wireless / wired / Internet compatible / custom protocol / …
- The implementation approach – discrete components / fully integrated / mixed solutions / …
- The power supply – main network / battery / battery-less / autonomous harvesting / …

This diversification introduces new challenges in the design of IoT nodes and especially in the development of the power management modules. Not only power management must face different kinds of power sources but it also have to be specifically designed accordingly to the peculiar power profile of the node.

1.2 The role of dedicated power management

In a typical IoT device the core section is represented by some sensing or monitoring elements which are controlled by a management module – commonly a microcontroller – that also handle the communication interfaces in

order to transmit acquired data to the external world [3]. In order to correctly supply the node an advanced power management section is essential to efficiently extract energy from the different sources and to make it usable by all other modules (Fig. 4) [4, 5].

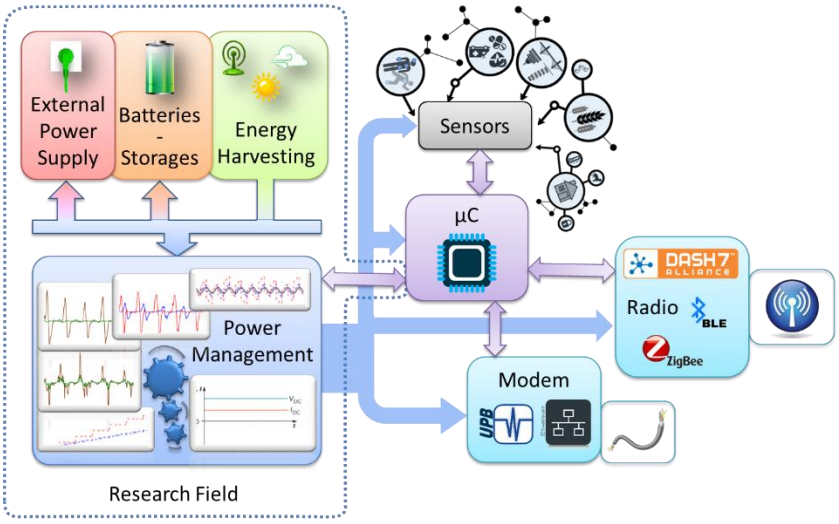

Fig. 4 IoT node typical structure with power management unit architecture highlighted

More precisely, the use of batteries as power supplies forces to carefully consider efficiency aspects related to power conversion and to possibly introduce recharging capability in order to increase battery lifetime [6, 7]. In this direction, the increasing use of harvesting power sources in order to obtain energy autonomous devices introduces new relevant issues:

- Harvesting transducers output voltages can be relatively low with respect to minimum operating voltage of electronic devices, in the order of hundreds of millivolts for radio frequency or indoor photovoltaic harvesting [8, 9].
- Similarly, available power is usually relatively low with respect to power required by the node, so particular focus must be placed on efficiency of power extraction module.
- Renewable sources are by their nature discontinuous, so storage elements must be inserted in order to compensate the possible lack of energy.

Another remarkable aspect related to the use of energy harvesting is the possible development of autonomous battery-less nodes, which is a research field of growing interest [10, 11, 12, 13, 14]. Within this scope new solutions must be provided to face power management issues, especially related to amount of available energy extracted from renewable sources. In fact in typical IoT

applications common renewable energy sources, e.g. radio-frequency or indoor photo-voltaic harvesting, can provide an amount of energy in the order of hundreds of microwatts, far away the value required by the node to correctly operate. This discrepancy leads to the following considerations:

- A storage element must be added, typically a capacitor or super-capacitor, in order to stock the harvested energy for a variable period of time till it is sufficient to switch on the node. As a consequence:
    - The value of storage capacitor must be carefully dimensioned. Higher values allow higher stored energy, which means on one hand higher operative time of the node once switched on, but on the other hand it means higher recharge time at first activation.
    - The voltage provided by the storage element is not ideally regulated, but it typically decrease as the capacitor is discharged during activity periods of the node – and it obviously increase during recharge periods –. Thus a regulation circuit may be necessary to provide controlled voltages to the core circuitry of the node.
- Energy harvested nodes often operates in discontinuous mode, i.e. they combine a recharge phase, in which the node is inactive and the storage element is recharged by mean of the extracted energy from the renewable source, with an active phase in which the node is switched on and performs one or more data acquisition/transmission cycles. As a consequence:
    - Specific circuits must be designed in order to monitor the actual amount of energy available in the storage element to know when it is possible to switch the node to the active phase.
    - Dedicated power off circuits must be added in order to limit the quiescent energy consumption of the node during the recharge phase.

1.3 The importance of durability and robustness aspects in IoT power electronics

IoT architecture is based on the idea of a shared intelligence made of the interaction between extensive and heterogeneous data provided by distributed electronic devices which pervasively cover the monitored space [15]. As a consequence such devices should:

- Be installed in large number to provide sufficient information for elaboration.
- Be placed even in unreachable or harsh locations, e.g. inside walls or bodies.

Due to these characteristics, the challenge we are facing today is to develop such devices in a way that they are substantially maintenance-free as they should be embedded in their environment as much as possible. In this scenario, improving lifetime and decreasing fault rate of the node are key aspects in this direction. These targets must be achieved by considering a wide range of different perspectives:

- The use of batteries as power supplies forces to carefully consider various durability aspects related to the wear of the battery itself due to its particular use and recharge rate [16, 17, 18].
- In order to extend device lifetime battery-less solutions should be investigated by using advanced energy harvesting techniques.
- For IoT nodes based on wireless communication protocols, extending maximum operative range can decrease fault rate.
- Improving power conversion efficiency is a profitable approach for both increasing battery lifetime (for battery-supplied nodes) and operative ranges (for autonomous harvesting nodes), both in terms of maximum distance (for wireless nodes) and minimum necessary amount of environmental energy (for autonomous harvesting nodes).
- Specific degradation effects are observed in power management circuits mainly related to common power conversion techniques, e.g. hot carrier degradation (HCD) in MOS devices of DC/DC switching converters [19], so dedicated solution should be investigated to tackle this issue.

1.4 Dealing with durability and robustness in a differentiate way – A thesis overview

In this thesis the previously mentioned aspects related to durability and robustness requirements for power management in IoT applications have been studied and analyzed, bringing to the development of various solutions following two main parallel paths:

- Hardware solutions
    - Minimize batteries degradation by developing innovative power conversion and management circuits with improved discharge current profiles and enhanced efficiency.
    - Detect and estimate specific *hot carrier degradation* level through on-the-fly measurement techniques applied to advanced power converters with reliability-aware architecture.

- System level solutions
  - Develop autonomous battery-less nodes with enhanced lifetime, with a specific case study related to radio-frequency energy harvesting techniques.
  - Monitor power conversion efficiency in low-power photovoltaic applications by developing noninvasive sensing architectures combined with predictive algorithms.

From a different point of view, issues related to each specific durability and robustness aspects are discussed in this thesis, and both hardware and software solutions are presented according to the following outline:

i. Issues related to the use of batteries as power sources
   - A series of hardware integrated solutions are presented for the design of dedicated DC/DC power converters with specific architectures capable to improve battery lifetime and overall efficiency.

ii. Issues related to the design of autonomous battery-less energy harvesting nodes
   - Different system solution are presented aiming at developing fully autonomous nodes with advanced power management with dynamically adaptive architectures to widen the operating regions of nodes.

iii. Issues related to efficiency degradation of low-power photovoltaic power converters
   - An advanced system solution is presented in order to obtain a runtime estimation of the actual capability of the converter to keep the photovoltaic panel at its best working point for power extraction (i.e. an estimator of the quality of Maximum Power Point Tracking Algorithm).

iv. Issues related to *Hot Carrier Degradation* effects in DC/DC power converters
   - An integrated hardware solution is presented for providing DC/DC converters with the capability of runtime estimation of the actual degradation level of power switches particularly subjected to this kind of degradation.

1.5 Power conversion basis in IoT applications

In this section a review of some general information about power conversion is introduced, which is necessary to understand the concepts presented in this thesis.

In Fig. 5 a typical power management IoT scenario is depicted. On the left arrow lays a large number of typical IoT energy sources with their associated different voltages that must be managed, covering both standard sources like batteries and harvesting sources for autonomous modes like photovoltaic panels, thermo-electrical generators and radio-frequency antennas. It is worth noting that it is a wide range of different input voltages, spanning from hundreds of millivolts up to tens of Volts, while on the other side the electronic core of the IoT device is shown, which accepts just a small range of voltage supplies; consequently, specific circuits must be designed which are able to convert all different source values to the accepted ones.

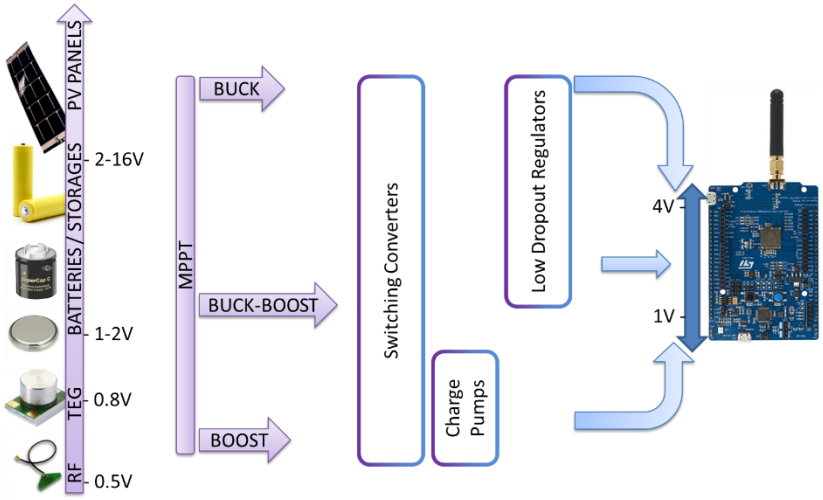

Fig. 5 Typical power management scenario in IoT applications

These circuits are generally referred as DC/DC converters as they transform a direct current input source to another regulated direct current output value. Accordingly to their ability to raise up the input source to higher output voltages or to reduce it to lower values DC/DC converters can be classified as:

- Boost converters: from lower input voltages to regulated output voltage.
- Boost converters: from higher input voltages to regulated output voltage.
- Buck-Boost converters: from any higher or lower input voltages to regulated output voltage.

From an architectural point instead DC/DC converters can be further classified as:

- Switching DC/DC converters: based on the transfer of a controlled amount of energy from source to target on a duty-cycle basis. In each transfer energy is previously stored in an external inductor and then driven to the output load.
  With this architecture both buck and boost converters can be implemented.
- Charge pumps: based on the dynamic connection of a series of pre-charged capacitors. Each capacitor is periodically charged to the input voltage and then connected to others in order to obtain higher voltage values.
  This architecture can be used to implement boost converters.
- Low dropout regulators (LDO): based on a feedback regulation of the output current to obtain a fixed output voltage. A MOS transistor is connected in series between input and output node, and voltage applied on its gate node is modulated in order to dynamically change the associated resistance and therefore control the resulting output voltage.
  LDO can only operate as buck converters.

For the purpose of this thesis only switching DC/DC architecture is considered, as it is the only one allowing the implementation of buck-boost conversion and it is the structure which can theoretically achieve the higher efficiency [20, 21, 22]. In Fig. 6 some typical implementations of switching DC/DC converter are shown, for buck, boost and buck-boost architectures.

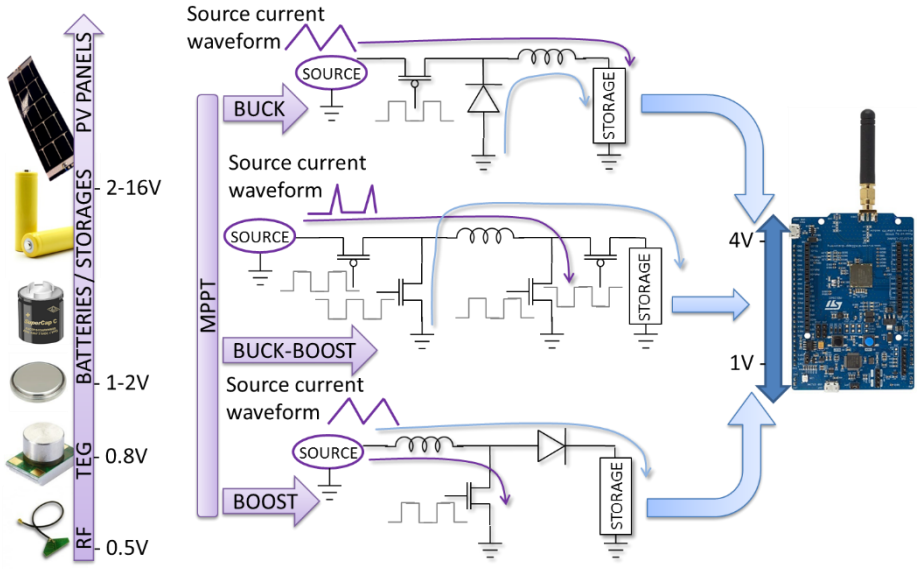

Fig. 6 Common implementation of switching DC/DC architectures

Considering a general purpose case of a buck-boost structure, reported in Fig. 7, its behavior can be described as a continuous sequence of an *ON phase* followed by an *OFF phase*. The two phases are regulated by the alternating activation of MOSs A, D and B, C, which are used as electronic switches.
Although several different architectures of non-inverting buck-boost converters are available in literature, including two-switch topologies [23], single-ended primary-inductor converters [24] and zeta converters [25], the proposed four-switch topology [26] provides the best flexibility in order to study different conversion approaches. As a matter of fact, each switch connected to the inductor provides a bidirectional path to ground or to source-load elements, so that a great variety of control strategies can be implemented by simply modifying the logic which generates the driving signal of the switches. As an example, a buck-boost architecture can be obtained implementing the following timing.

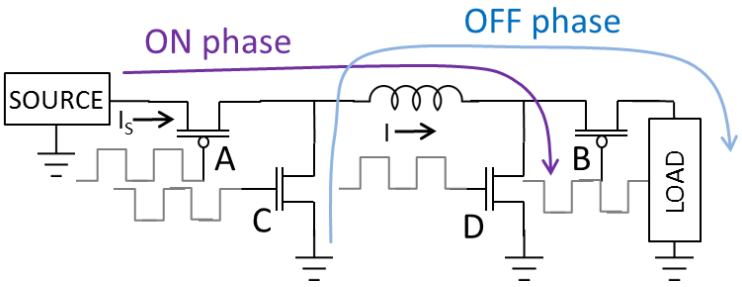

Fig. 7 General purpose implementation of a buck-boost DC/DC converter

During the *ON phase*, *A* and *D* are switched on while *B* and *C* are switched off, so a linearly increasing current flows from source to ground through inductor *L*. In this way an amount of energy equal to

(i)
$$E_L = \frac{1}{2} L (I_{FINAL}^2 - I_{INIT}^2)$$

is stored inside inductor *L*, where I_{INIT} is the current flowing at the beginning of the phase and I_{FINAL} is the peak current obtained at the end of the *ON phase*, after a T_{ON} time:

(ii)
$$T_{ON} = \frac{L(I_{FINAL} - I_{INIT})}{V_{SOURCE}} = \frac{L \cdot \Delta I}{V_{SOURCE}}$$

During the *OFF phase*, *A* and *D* are switched off while *B* and *C* are switched on, so a linearly decreasing current flows from inductor *L* to output load, so that the energy previously stored in the inductor is transferred to the output. If we consider the case in which all stored energy is transferred in each cycle, then

current inside inductor returns to its initial value at the end of the *OFF phase*, after T_{OFF} time:

$$T_{OFF} = \frac{L \cdot \Delta I}{V_{STORAGE}} \qquad (iii)$$

If T is the overall period of operating cycle, then we can also state that

$$T = T_{OFF} + T_{ON} \; ; \; T_{ON} = T \cdot D \; ; \; T_{OFF} = T \cdot (1 - D) \qquad (iv)$$

where D is the duty cycle of the system. Under these assumption the converter works in continuous mode, and the output voltage $V_{STORAGE}$ depends entirely on the value of duty cycle D, according to:

$$\frac{V_{STORAGE}}{V_{SOURCE}} = \frac{D}{1 - D} \qquad (v)$$

On the contrary, if inductor is completely discharged every cycle, and consequently the current is always nullified at the end of the *OFF phase*, then converter works in discontinuous mode. In this case the switching period is defined as

$$T = T_{OFF} + T_{ON} + T_{IDLE} \qquad (vi)$$

where T_{IDLE} is the time between the end of the *OFF phase* and the beginning of the subsequent *ON phase*. Differently from the continuous mode, the output voltage $V_{STORAGE}$ depends on different factors:

$$\frac{V_{STORAGE}}{V_{SOURCE}} = \frac{V_{SOURCE} D^2 T}{2 L I_o} \qquad (vii)$$

where I_O is the output load current.

Finally, it is worth noting that current drawn from the input source has an impulsive waveform which is sketched in Fig. 8.

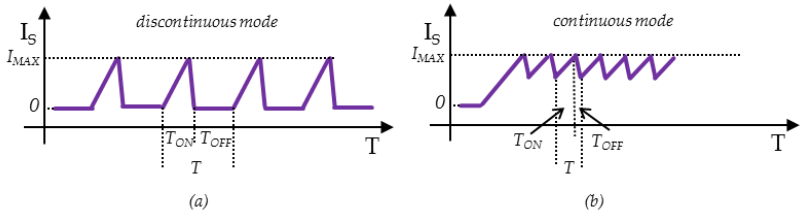

Fig. 8 Typical current profile drawn from supply source by a common DC/DC switching converter, in both discontinuous (a) and continuous (b) mode

Moreover, an important aspect of many energy harvesting transducers is that their characteristic impedance depends on the strength of the considered element (irradiance, RF power, heat, etc.) and, in some cases, like photovoltaic panels, they present a non-linear characteristic in their current / voltage function, i.e. they do not have a pure resistive response. For these reasons, the optimum operating point, in which energy provided to the DC/DC converter is higher than in any other operating point, depends on the kind of transducer and can vary over time [27]. Therefore in many cases switching DC/DC converters have an embedded Maximum Power Point Tracking (MPPT) circuit which is responsible of keeping the input source in the best operating point for power extraction. There are many kinds of MPPT algorithms, basically divided in two categories:

- Dynamic MPPT algorithms: *perturb and observe*, *incremental conductance*, *current sweep*. These algorithms monitor some electrical quantities of the source and try to detect the maximum power point, either inferring the actual I / V characteristic or dynamically move the operating point towards higher values of input energy [28].
- Static MPPT algorithms: *Fractional Open Circuit Voltage*. In this case the maximum point is approximated on the basis of the open circuit voltage of the input source, i.e. the voltage present across the input source with no load connected. As a matter of fact it is proved that in many cases the maximum power point voltage is placed when the load biases the transducer in the proximity of a pre-determined ratio of the open circuit voltage, for example 0.6 - 0.8 for photovoltaic panels and 0.5 for thermos-electrical transducers [29, 30]. From a practical point of view, the converter periodically disconnects the load from the input and it consequently evaluates the open circuit voltage of the source, then setting the operating point to a fixed ratio of that value. This algorithm is less precise than dynamic ones, yet it has a lower power consumption due to its simplicity and therefore it is mainly used in low-power architectures since it implements a usually convenient trade-off.

Chapter 2

Robustness and durability aspects in the use of electrochemical cells

Many studies in the state-of-the-art research tackles the problem of reliability and cycle-time issues in rechargeable batteries due to charge voltage / current profile [17, 6]. In other words, battery degradation is commonly tied to recharge aspects and advanced commercial solutions are nowadays available which perform specific recharge cycles with controlled profiles [31, 32].

Nevertheless, recent studies associate the state of health of the battery also to the peculiar discharge profile it is undergone [33, 34, 35]. For example, in [35] it is established how impulsive discharge current profiles are detrimental to battery lifetime and reliability.

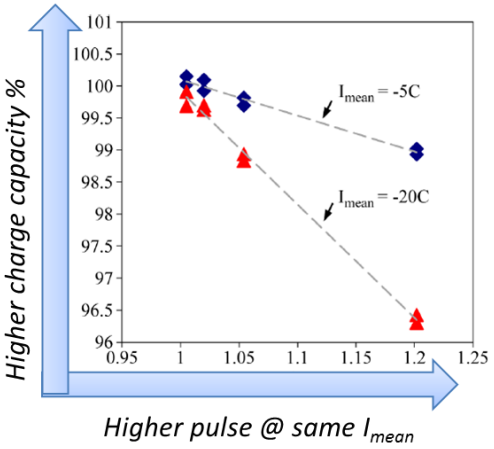

Fig. 9 Dependence of Li-Ion battery End-Of-Life with respect to impulsive discharge current profiles (F. Savoye, P. Venet, M. Millet and J. Groot, "Impact of Periodic Current Pulses on Li-Ion Battery Performance,")

In Fig. 9 experimental results show the effect of periodic pulsed profiles on degradation rates of Li-ion batteries. More precisely, in the graph on the x-axis is reported a form factor index defined as I_{rms}/I_{mean}, which is an indicator of the value of pulses; keeping the average discharge current constant, then the higher are discharge peaks the fastest is the loss of storage capacity of the battery, which is a good estimator of the overall state of health. Moreover, it is clear that this effect is more marked for higher values of the average current (red marks in figure), mainly due to effects related to the Ohm's law. Different studies demonstrates the correlation between high discharge pulsed profiles and Li-Ion batteries lifetime [36, 37], although no clear electromechanical background has

been identified to explain the detrimental effect caused by impulsive discharge. Similarly, in [38, 39] physical and empirical models are presented showing how the cycle life of lithium batteries depends in a complex manner on many factors including discharge profiles along with chemistry and size of the cells, temperature of the tests, the charge algorithm, and the initial and final discharge conditions . From a general point of view, the adoption of load-leveling techniques, such as the introduction of super-capacitors for filtering purposes, is a recognized approach in order to improve battery reliability [36, 37].

The relevant aspect of these studies is that many empirical results demonstrates how impulsive discharge profiles, like the ones shown in Fig. 8 typically associated with DC/DC converter switching activity, have a negative impact on the cycle life of secondary batteries, if compared to constant discharge profile with same average extracted current. As a consequence, alternative ways to reduce or eliminate current peaks drawn from battery sources are currently studied in order to improve lifetime of the supplied system.

2.1 State-of-the-art solutions

From both commercial and academic point of view some attempts have been made in DC/DC converters aiming at limiting maximum current or controlling its average value. In [40] an advanced control on duty cycle is proposed in order to regulate the current shape of the converter, by adding a weighted dependence on the inductor current with respect to a predefined maximum current, in order to prevent the converter from exceeding such value. The objective function of the control algorithm virtually introduces a dynamic resistance in series with the inductor, which is modulated accordingly to the battery current in order to limit its value. Resulting waveforms show that on one hand the average current can be successfully regulated through the modulation of the duty cycle, yet the impulsive nature of the waveform is still present as the regulation only applies to the average value of the current.

Similarly, in [41] a commercial solution is proposed which effectively is able to control the shape of the current profile rather than its mean value. Yet in this case an overshoot regulation is performed, in the sense that current shaping is only accomplished if current drawn from source exceeds a programmable maximum threshold value; if this happens then current demand is limited to the threshold value and a constant flat profile is obtained, thus eliminating harmful peaks. Nevertheless this clamping effect only occurs when power request of output load exceeds input power, while for low current requests peaks are not eliminated. On the other hand, when clamping occurs then desired output voltage cannot be guaranteed anymore.

As a consequence, none of the existing solutions is able to completely regulate the current profile during normal operations of the DC/DC converter.

2.2 Studied solution: a more problem-oriented approach

With the aim of completely control the current profile of the battery discharge a novel architecture is proposed which is able to eliminate all peaks normally associated with common DC/DC converters. This solution represents a fully integrated DC/DC converter which has been proposed and that was subsequently integrated on silicon in collaboration with STMicroelectronics.

The basic idea is that it is physically infeasible to delete the peaks required by the switching DC/DC converter due to its intrinsic architecture, so the proposed solution is to insert an additional stage between the battery source and the active converter in order to decouple them. A schematic of the overall architecture is presented in Fig. 10, where the intermediate decoupling stage and the main DC/DC circuit are pointed out. For this purpose, a known buck-boost architecture has been considered for its generality, although this solution can be applied to any kind of DC/DC converter.

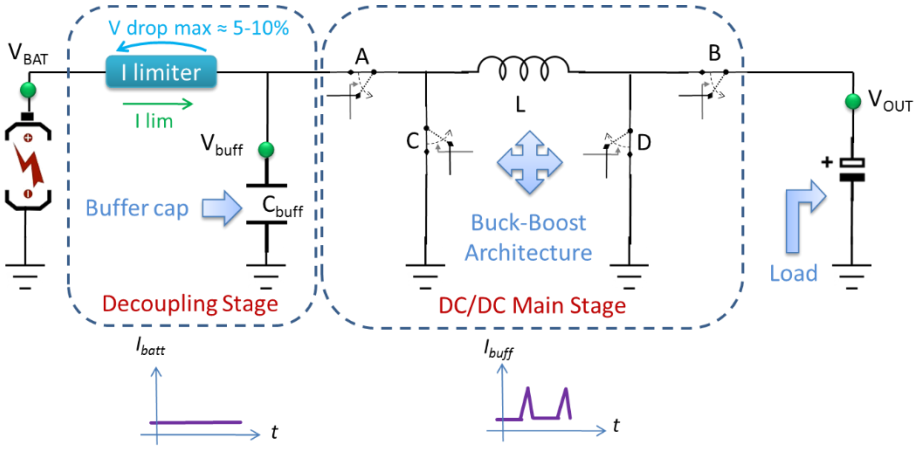

Fig. 10 Block diagram of an innovative DC/DC architecture with complete control of required current profile

The purpose of the decoupling stage is to introduce a current limiter *I limiter* in association with a buffer capacitor C_{buff}. The source, i.e. the battery, simply supplies this intermediate stage with a controlled current and almost constant current, which can be considered safe from the point of view of battery degradation, and linearly charges the buffer capacitor, while the capacitor itself acts as the main energy source for the DC/DC converter and therefore provides the required peaks to the converter. The result is that a constant regulated current is always drawn from the battery, while all the possibly detrimental peaks are sustained by the capacitor, which is actually not affected by this kind of pulsed profile. Of course, the cascading of two blocks poses several constraints related to the overall efficiency, which is the product of the efficiencies of the two blocks.

For this reason, the architecture aims at providing the maximum possible efficiency for every stage.

2.2.1 Battery model

In order to correctly estimate the actual effects of the proposed solution on a real battery, a widely adopted R-C model of a lithium-ion cell was implemented [42, 43], which is shown in Fig. 11.

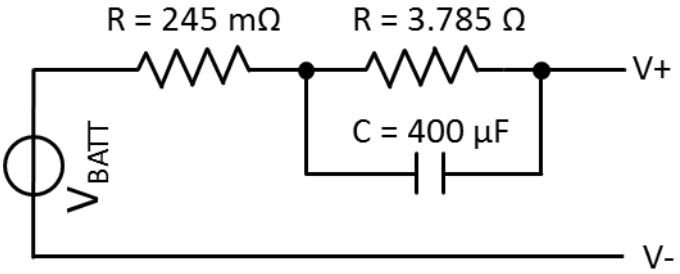

Fig. 11 Adopted battery model to simulate supply source

Values of parasitic elements were derived from the datasheet of a commercial NiMH coin cell with 15 mAh capacity and 1.2 V nominal voltage (Varta® 55602 -101-501). Other models of various complexity are proposed in literature [44], which also include dynamic characteristics related to the aging process of the battery, implemented as both schematic and matlab®/symulink® modules. In future works, the use of this kind of advanced models can also improve the effectiveness of the proposed solution by better analyzing the interaction between the battery and the DC/DC converter in the long term.

Moreover, other categories of batteries show considerably higher values of parasitic series resistance, in the order of few hundreds ohm, like for example in some kinds of thin-film cells [45]. In this case, the parasitic resistance intrinsically limits the maximum flowing current and the maximum peaks, but on the other hand optimal discharge rates, in terms of nominal capacity and end-of-life, are far below maximum values, so that an additional limitation circuit can improve robustness and durability for this categories too.

2.2.2 Functional overview

Basically, the decoupling stage is made of a buffer capacitor which is directly connected to the input source through a current limitation circuit. This forces the battery to recharge the capacitor with the maximum allowed current, whose maximum value is defined by the limiter threshold. A constant current is then drawn by the battery and the maximum allowed power is constantly extracted.

Consequently, the buffer capacitor is linearly charged till a higher value which is controlled through the modulation of the switching activity of the following DC/DC stage. From a functional point of view, DC/DC operations can be divided in different phases:

a) Recharge phase

In this startup phase switches *A*, *B* are OFF, *C*, *D* are ON. No energy is transferred from input source to output load and buffer capacitor is linearly charged from zero to a predefined high level threshold which can be defined as a percentage of battery voltage $\alpha_H \cdot V_{batt}$.

b) ON phase

Once buffer voltage reaches $\alpha_H \cdot V_{batt}$, conversion is activated and switches *A*, *D* are ON while *B*, *C* are OFF. With this configuration inductor L is charged while buffer capacitor is partially discharged, so that its voltage start decreasing. This phase ends when buffer voltage goes below a predefined low level threshold which in turn can be defined as a fraction of battery voltage $\alpha_L \cdot V_{batt}$. Disregarding the loss effects due to parasitic resistances of the circuit and under the assumption of discontinuous current conduction in the inductor, we can state that the energy extracted from the capacitor is totally stored in the inductor, according to the formula:

$$\frac{1}{2}C_{buff}V_{batt}^2(\alpha_H^2 - \alpha_L^2) = \frac{1}{2}LI_{MAX}^2 \xrightarrow{yields} I_{MAX} = \sqrt{\frac{C_{buff}V_{batt}^2(\alpha_H^2 - \alpha_L^2)}{L}} \quad (viii)$$

where I_{MAX} is the peak current inside the inductor at the end of the ON phase. Under the same approximation the duration of the *ON phase* can be estimated according to:

$$V(t) = \alpha_H V_{batt} \sin\left(\frac{1}{\sqrt{LC}}t + \frac{\pi}{2}\right) \xrightarrow{yields} t_{ON} = \sqrt{LC} \cdot \cos^{-1}\left(\frac{\alpha_L}{\alpha_H}\right) \quad (ix)$$

which refers to the common solution of an L-C resonant circuit, formed by inductor *L* and capacitor C_{buff}.

On the other hand, if we consider a real resistive path *R* between the buffer capacitor and the inductor, and introducing following parameters:

$$\begin{cases} \alpha = \dfrac{R}{2L}; & w_0 = \dfrac{1}{\sqrt{LC}}; \quad \zeta = \dfrac{R}{2}\sqrt{\dfrac{C}{L}}; \quad w_d = w_0\sqrt{1-\zeta^2} \end{cases}$$

equations (viii) and (ix) must be updated as follows:

(xi) $$V(t) = \alpha_H V_{batt} e^{-\alpha t}\left[-\frac{\alpha}{w_d}\sin(w_d t) + \cos(w_d t)\right]$$

(x) $$I(t) = \frac{\alpha_H V_{batt}}{L w_d} e^{-\alpha t}[\sin(w_d t)]$$

which cannot be solved analytically for t, so that a definite algebraic form cannot be found for I_{MAX} and T_{ON}. As a consequence, the efficiency of the energy transfer between the buffer capacitor and the inductor depends on the transfer time, with the following expression:

(xii) $$\eta_{CtoL} = \left\{\frac{1}{\sqrt{1-\zeta^2}} e^{-\alpha t}\left[\frac{\sin(w_d t)}{\sin(w_0 t)}\right]\right\}^2$$

c) OFF phase

Once *ON phase* is ended, energy stored inside inductor is transferred to the output load, by configuring switches *A*, *D* OFF and *B*, *C* ON. This phase ends when all energy stored inside inductor is transferred to the output load, i.e. when current inside inductor goes to zero, regardless the voltage value of the buffer capacitor. At the same time, the source battery recharges the buffer capacitor and its voltage value increases again. At the end of the energy transfer operation, when inductor current is zero, if buffer voltage has already reached the higher threshold $\alpha_H \cdot V_{batt}$ then the converter immediately switches to the *ON phase*, otherwise it waits in *Recharge phase* till the higher threshold is reached again. In general, for applicative reasons, the output node is connected to a highly capacitive load, so that its voltage can be considered approximately constant for the time of a single conversion cycle. That being so, during this phase the current inside inductor is linearly decreasing. Then, the duration of the *OFF phase* time can be evaluated with:

(xiii) $$t_{OFF} = \frac{L I_{MAX}}{V_{OUT}}$$

The resulting waveforms are shown in Fig. 12. The red line represents the variation of buffer capacitor voltage over time, while blue lines show the evolution of the current drawn from the battery, the current inside the inductor and the current provided to the output, respectively.

As previously mentioned, the four-switch topology was chosen for its flexibility which allows to implement different types of conversion strategies by simply changing the digital control logic which drives the switches. Similarly, the described behavior and temporization for implementing a buck-boost converter is only one of the possible choices, and it was adopted due to its simplicity, since the main topic of the project is to study the interaction between the current limitation and at the input stage and the actual DC/DC conversion stage, and its potential benefit on the battery source end of life. Nevertheless,

more complex and efficient solutions are proposed in literature for the control logic, for example by introducing additional phases which includes the possibility to temporarily have *A,B* ON and *C,D* OFF, this reducing the root mean square (RMS) value of the current inside the inductor with a benefit for the overall efficiency, at the cost of a more complex digital block [46].

Consequently, after verifying the effectiveness of the studied solution, more advance architectures (like in [46]) are worth to be investigated in order to further improve conversion efficiency.

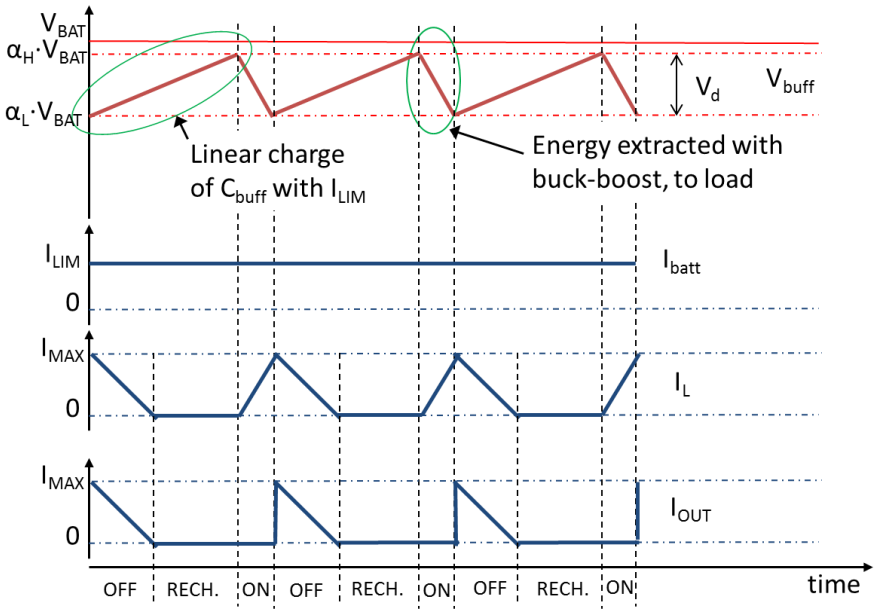

Fig. 12 Waveforms of respectively: Buffer capacitor voltage, Current drawn from battery, Current flowing inside inductor element, current provided to output load, in the proposed DC/DC solution

2.2.3 Control signals

In order to correctly manage the timing of all phases, some comparator circuits have been added for monitoring the voltage of buffer capacitor and the inductor current. A more detailed description of internal architecture with additional comparators is shown in Fig. 13.

- Comparator *TH* is connected to the buffer capacitor and has a hysteretic behavior between $\alpha_H \cdot V_{batt}$ and $\alpha_L \cdot V_{batt}$. It generates a control signal which goes high when buffer voltage exceeds $\alpha_H \cdot V_{batt}$ and returns low when buffer voltage falls behind $\alpha_L \cdot V_{batt}$.
- Comparator *ZCS* monitors the voltage drop across switch *C*. During *OFF phase*, a positive current flows from the source node of the MOS (connected

to ground) to the output load through the inductor. To do so, drain node of MOS *C* (connected to inductor *L*) temporarily drops below zero voltage to allow the current flow in that direction. At the end of *OFF phase* the current is zero, so drain voltage returns positive. *ZCS* comparator senses this zero crossing and generates a trigger signal when current runs out, informing that *OFF phase* must be terminated.

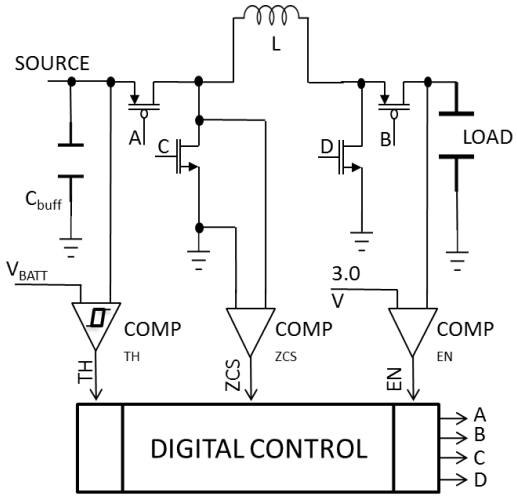

Fig. 13 Block diagram of control signals required to manage DC/DC switching periods in proposed solution

- Comparator *EN* is an additional module which is required to control output voltage. As introduced in section 1.5, in common DC/DC converters the output voltage is often regulated by modulating the duty cycle of the switching activity. Conversely, in this implementation duty cycle is regulated by the specific timings of the *ON*, *OFF* and *Recharge* phases. For this reason, output voltage is here regulated by mean of an *on-off* hysteretic algorithm: if output voltage is below desired value (named *REF V* in picture), then converter is enabled and load is being charged, otherwise system is disabled (*A*, *B* OFF, *C*, *D* ON).

2.2.4 Comparison circuits

An overview of comparison circuits is presented in this section.

$Comp_{TH}$

$Comp_{TH}$ is a typical cross-coupled cross-gate architecture with hysteresis, depicted in Fig. 14. Bias current is 60 nA, with a resulting quiescent current of about 800 nA, while a hysteresis of about 40 mV is obtained through coupled MOS M1-M3 and M2-M4. However, the introduced hysteresis has the only

purpose of increasing the stability of comparator, and it is not used to implement the two thresholds α_H and α_L. On the contrary the two thresholds are set through an external conditioning circuit (typically a resistive divider), which provide both thresholds to the system. Then, the correct threshold to be used (high or low), is selected through a specific multiplexing circuit. The resulting architecture is shown in Fig. 15.

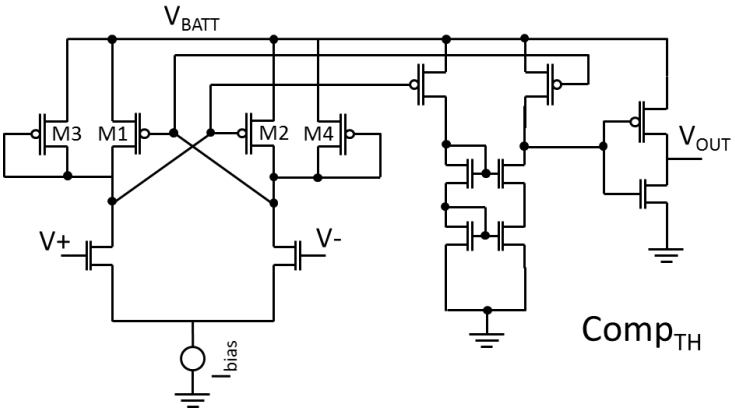

Fig. 14 Schematic of a first comparator architecture for monitoring voltage of buffer capacitor

When threshold signal *TH* is low, $\alpha_H \cdot V_{batt}$ is used as comparison signal for V_{buff}. As soon as V_{buff} exceeds the value of $\alpha_H \cdot V_{batt}$, *TH* goes high and comparison signal is set to $\alpha_L \cdot V_{batt}$ thanks to multiplexer *MUX*. As a consequence, *TH* signal remains high till V_{buff} drops below $\alpha_L \cdot V_{batt}$. Thanks to this architecture, hysteretic behavior is obtained through just one comparator circuit, with a benefit in overall power consumption. Finally, the two thresholds can be set externally, which is fundamental in order fit the behavior of the system to the specific application. In fact, as explained in section 2.2.2, this two thresholds affect switching frequency and average extracted power from source, as well as overall efficiency as explained in detail in section 2.2.6.

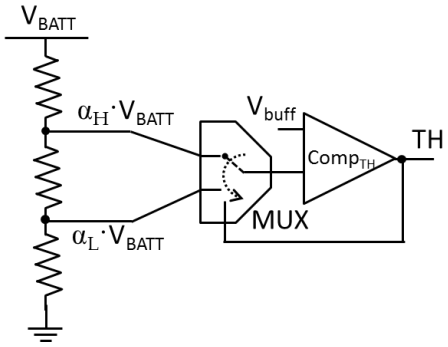

Fig. 15 Schematic of the proposed solution of a full comparator with external programmable hysteresis

Comp$_{ZCS}$

Comparator ZCS has a different role, since it has to detect the amount of current flowing inside the power MOSFET by means of its drain-source voltage, and its architecture is quite different too, as shown in Fig. 16.

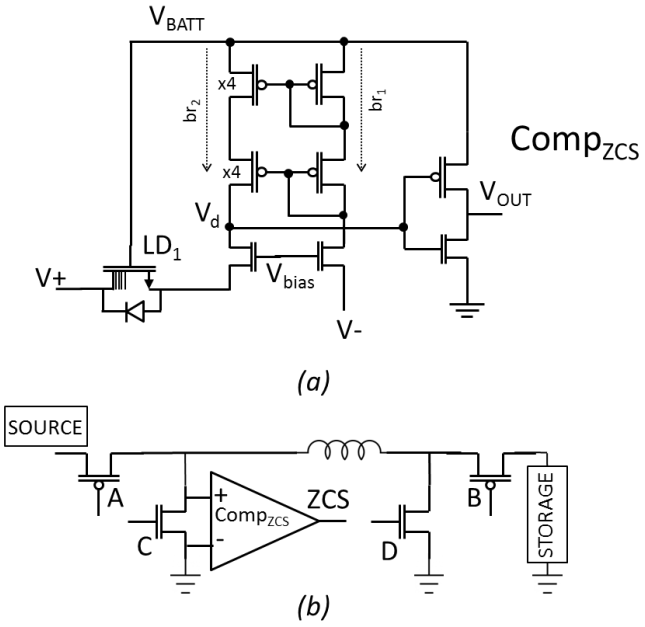

Fig. 16 Schematic of a second comparator architecture for zero-cross detection (a) and specific application for monitoring end of OFF phase in proposed architecture

With reference to Comp$_{ZCS}$, Fig. 16 (a), a proportional current is forced to flow through the two parallel branches br_1 and br_2, which is only possible if V+ is lower than V-. In this situation the current flowing in br_2 forces V_d to a low value, and V_{OUT} is consequently high. On the contrary, if V+ is higher than V-, a lower current is allowed in br_2, and force V_d to rise to a value closer to V_{BATT}. This specific architecture is used to handle input signals which are close to ground or even negative, which would not be possible with an architecture similar to the one presented if Fig. 14. As a matter of fact, comparator *ZCS* is used to monitor the current flowing through one of the power switches connected to ground of the DC/DC converter, as shown in Fig. 16 (b). During the *ON phase*, a positive current flows from source to drain of MOS *C*, and consequently a negative (below ground) potential is forced on the drain node by the inductor current. The role of *ZCS* comparator is to detect when this current goes to zero, this meaning that the drain voltage returns positive. As a consequence, in this application node V- of comparator Comp$_{ZCS}$ is connected to ground, while V+ can be either positive or slightly negative. The proposed architecture is therefore capable to handle this specific range, differently from previous solution. Concerning quiescent current, a simulated value of approximately 600 nA is obtained for this

architecture. The multiplying factor x4 is used in order to speed-up the response time of the comparator, while the introduction of LDMOS LD_1 with cascoded configuration is necessary to protect the rest of the circuit from the possible voltage spikes associated with the inductor behavior during commutations between *ON* and *OFF phases*.

$Comp_{EN}$

For what concerns comparator *EN*, an architecture similar to $Comp_{TH}$ can be used. Nevertheless, in the proposed solution, the control of the output voltage has been left outside the integrated circuit, and the enable signal *EN* must be provided to the circuit though an external pin.

2.2.5 Cross-conduction aspects

The management of signals *A*,*B*,*C*,*D* along with their correct timing, is accomplished through a dedicated digital module which has been implemented with a standard automatic digital flow starting from a Verilog HDL [47] description of the behavior of the block.

If compared to a general purpose DC/DC converter, this architecture works either on the boundary between continuous and discontinuous conduction mode (see section 1.5) or in discontinuous conduction mode, depending on whether the buffer voltage is already above the high threshold at the end of the OFF phase. In any case, energy stored inside inductor in each cycle is always

$$E_L = \frac{1}{2} L I_{MAX}^2 \qquad (xiv)$$

Similarly to common DC/DC architectures, it is necessary to carefully avoid cross-conduction effects during commutations between ON and OFF phases. More precisely, it is necessary to avoid any conductive path between input or output and ground through the switches elements. This can easily happen if

- During the commutation between *OFF* and *ON phase*: switch *D* is closed before *B* is opened or switch *A* is closed before *C* is opened.
- During the commutation between *ON* and *OFF* phase: switch *B* is closed before *D* is opened or switch *C* is closed before *A* is opened.

This means that in the first case the switching on of *D* and *A* should be delayed compared to *B* and *C*, while in the second case their switching off should be anticipated compared to same signals.

In order to understand how to cope with this effect, it is worth noting that although the adopted architecture presents four switches, they can be grouped accordingly to their state during *ON* and *OFF phases*. More precisely, *A* and *D*

are always ON together (during *ON phase*) and always OFF together (during *OFF phase*). Conversely, *B* and *C* are always ON together (during *OFF phase*) and always OFF together (during *ON phase*). For this reason, a single control signal may be generated to drive switches *A*-*D* and another single one may be generated for *B*-*C*.

From an operative point of view, switches *A* and *B* are implemented via a power pMOS, so they are ON if driven by a low signal, while switches *C* and *D* are implemented via a power nMOS, so they are ON if driven by a high signal. Consequently, although from a logical point of view it is reasonable to group switches as *A*-*D* and *B*-*C*, from an electrical point of view it is more convenient to group control signal as *A*-*C* and *B*-*D*. As a matter of fact, if we connect *A*-*C* to the same signal then one and only one of them is ON, which is exactly what we expect; same behavior can be obtained with a unique control signal connected to *B*-*D*. That being so, we can consider separately the two control signal *A*-*C* and *B*-*D* and insert a proper delay in each of them in order to avoid cross-conduction. If we consider signal *A*-*C* (the same approach can be used for *B*-*D*), then it is true that:

- If *A* is low (switched on) converter is in *ON phase* and therefore *C* should be delayed compared to *A*.
- If *A* is high (switched off) converter is in *OFF phase* and therefore *A* should be delayed compared to *C*.

In order to obtain such behavior, a dedicated mixed analog/digital circuit has been introduced, shown in Fig. 17.

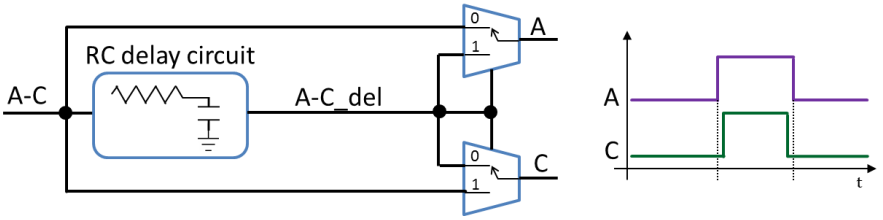

Fig. 17 Proposed circuit to introduce specific delays in control signals of DC/DC converter in order to avoid cross-conduction during commutations

2.2.6 Efficiency aspects

Due to the insertion of the decoupling stage an efficiency reduction must be taken into account, which is directly related to the operative voltage of the buffer capacitor. As a matter of fact, if in first approximation we consider as negligible the current consumption of the limiting circuit, then input and output current of decoupling stage are the same, and therefore efficiency can be exactly defined as

the ratio between output and input voltage. As already introduced in section 2.2.2, the buffer capacitor is continuously switching between two different thresholds $\alpha_H \cdot V_{batt}$ and $\alpha_L \cdot V_{batt}$, as recalled in Fig. 18.

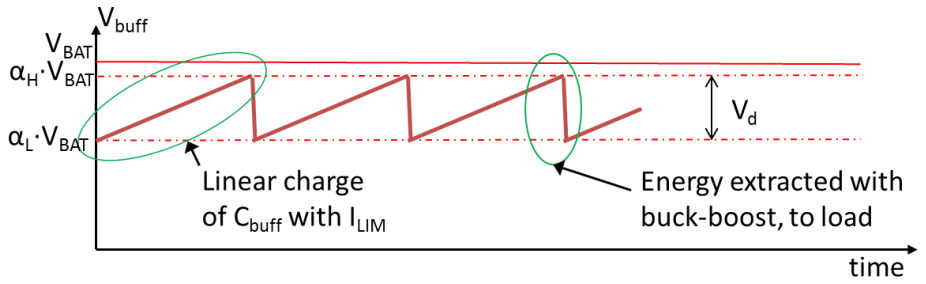

Fig. 18 Waveform of buffer capacitor voltage during normal operation of proposed DC/DC converter

Consequently, the average dropout voltage is

$$V_{drop} = \frac{\alpha_H + \alpha_L}{2} \cdot V_{BAT} \tag{xv}$$

while resulting efficiency can be estimated as:

$$\eta_{LIM} = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT}}{V_{IN}} = \frac{\frac{\alpha_H + \alpha_L}{2} \cdot V_{BAT}}{V_{BAT}} = \frac{\alpha_H + \alpha_L}{2} \tag{xvi}$$

It is clear that the higher these thresholds are, the higher is the resulting efficiency. Nevertheless, it is not suitable to choose the high threshold too close to V_{BATT} since it would imply the development of a comparator with an increased complexity, which would increase power consumption beyond the increase in efficiency, since it should be able to detect a signal which is very close to its supply voltage. Similarly, the low threshold cannot be chosen too close to the high one, otherwise the switching frequency could reach high values and threshold comparators should have therefore very high bandwidth and precision with, once again, increased power consumption that would not justify the increased efficiency. As a consequence, a proper trade-off should be considered to define the thresholds. Reasonable values in the range of 98%-99% for α_H and 90%-95% for α_L are acceptable. For example, with a high threshold of 98% and a low threshold of 92% the obtained efficiency is 95%.

Finally, the efficiency related to decoupling stage must be combined with the efficiency of the cascaded DC/DC stage, according to:

$$\eta_{TOT} = \eta_{DC/DC} \cdot \eta_{LIM} \tag{xvii}$$

so that efficiency of DC/DC stage should be carefully considered in order to overcome the losses introduced by the decoupling stage.

2.2.7 Studied solutions

For what concerns implementation of limiting decoupling stage and digital control, different solutions have been studied aiming at reaching various targets mainly related to the heterogeneity of IoT applications already introduced in section 1.1. More in detail three solutions have been implemented:

- An adaptable limiter architecture: considering the capability of forcing a constant regulated input current flowing from battery to DC/DC, it is interesting to include the capability of dynamically regulate the value of the constant current, in order to fit it to the specific kind of battery or to the average power requirements of the load.
- An ultra-low power architecture: as already mentioned in section 1.4, since in IoT applications it is common to use micro-power energy harvesting sources for increasing the lifetime of the system, then a nano-power architecture can successfully work even in the weakest conditions and then extend the operating time.
- An improved efficiency architecture: in order to partially overcome the efficiency limitations related to the decoupling stage estimated in (xvi), new approaches are investigated in the direction of increasing transfer efficiency between buffer capacitor and output capacitor, by exploiting different techniques like for example adiabatic charging.

Although these different solutions have to be suitable to operate at switching frequencies of DC/DC converter of few hundreds of kilohertzes, this is not the main timing constraint they have to satisfy. As a matter of fact, they are supposed to correctly operate, i.e. to limit the flowing current, even during the fast transitions between on and off stages of the converter, which may occur with slew-rates in the order of 1-2 V/ns, in a bandwidth of hundreds of megahertzes. As a consequence, particular attention has been devoted to the design and dimensioning of these blocks in terms of timing response, as explained in detail in following sub-sections.

2.3 An adaptable limiter architecture

A first solution with a configurable current limitation module is proposed, which is able to efficiently meet the specifications of the source battery and to adapt to the power demand of the load.

The structure of the limiting circuit is shown in Fig. 19, and basically consists of three different current mirrors.

The first one, composed of MOSFETs *M1* and *M2*, is a simple mirror, whose purpose is to replicate a 100 nA reference current inside the integrated circuit with an x4 factor. By doing so, the main current branch is not directly applied to the external generator, whose impedance specification is actually unknown and that could be detrimental to the overall operation. Conversely, critical stages are connected to this first mirror, which can be dimensioned accordingly.

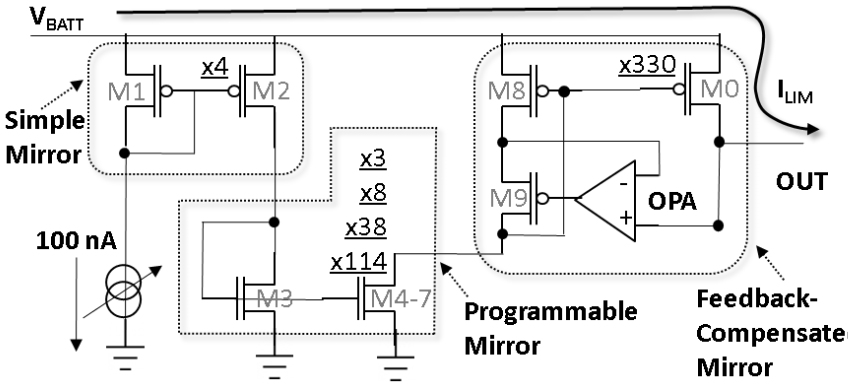

Fig. 19 Block diagram of the proposed structure of the current limiting stage based on a cascade of current mirrors

The second stage is a programmable mirror composed by *M3* and *M4-7*. Four transistors with different sizes *M4-7* are included for implementing four different mirror ratios (x3, x8, x38, and x114). Supplementary transistors are also included in order to select one out of *M4-7* through two dedicated input signals.

Finally, an output stage is designed, implementing a feedback-compensated current mirror with an x330 ratio (*M8*, *M9*, *and M0*). This architecture allows compensating mirror mismatch due to different values of drain voltage between input and output branches [48, 49]. As V_{OUT} is forced by the output capacitance, then we need to add the feedback circuit composed by the OPA and *M9*, which actually modulates the resistance of *M9* in order to minimize the voltage drop between the drain terminals of *M0* and *M9*. The resulting circuit acts like a single current mirror with four programmable output currents of 396 µA, 1.056 mA, 5.016 mA or 15.048 mA. The selection of desired programmable current is performed by mean of two external pins.

For what concerns the specific efficiency of this block, considering the bias current we can infer that, with respect to output current, the current flowing in feedback-compensated mirror is at most equal to:

$$I_{BIAS} = I_{BIAS_{M89}} + I_{BIAS_{M47}} + I_{BIAS_{M3}} =$$
$$= \left(\frac{1}{330} + \frac{1}{330 \cdot 3} + \frac{1}{330 \cdot 3 \cdot 4}\right) \cdot I_{OUT} \cong 0.0043 \cdot I_{OUT} \qquad \textit{(xviii)}$$

which can impact as a 0.5% loss in efficiency as worst case. On the other hand, bias current of op-amp OPA is approximately 1 µA, thus accounting for another 0.4% loss as worst case. Ultimately, an overall 1% loss in efficiency can be considered for all bias currents of this block.

2.3.1 Simulation results

Simulation results of the designed block are shown in Fig. 20.

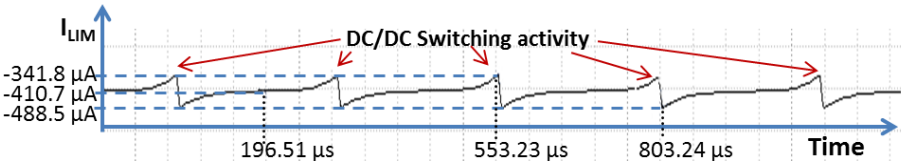

Fig. 20 Simulation results of the proposed structure of the current limiting stage based on a cascade of current mirrors, considering required current peaks by the DC/DC of 85 mA

Presented waveform refers to a programmed limitation of 400 µA with a buffer capacitance of 20 µF and source voltage equal to 3 V, with associated current peaks required by the DC/DC converter of approximately 85 mA. Controlled spikes of about 10%-20% are present in correspondence with DC/DC commutations. However, such fluctuations are negligible with respect to peak currents generated by conventional converters, which are correlated to battery reliability issues. Similar results are obtained for the other programmable limitation values.

In Fig. 21 two waveforms are presented related to current inside inductor (blue) and current provided to output load (red), with a maximum current of about 87 mA. Simulated results have been obtained with following dimensioning:

Table 1 Dimensioning of the test case used to obtain current waveforms of proposed DC/DC converter

Parameter	Value	Unit
V_{BATT}	2.8	V
V_{OUT}	2.45	V
α_H	98	%
α_L	92	%
T_{ON}	3.51	µs
I_{MAX}	87	mA

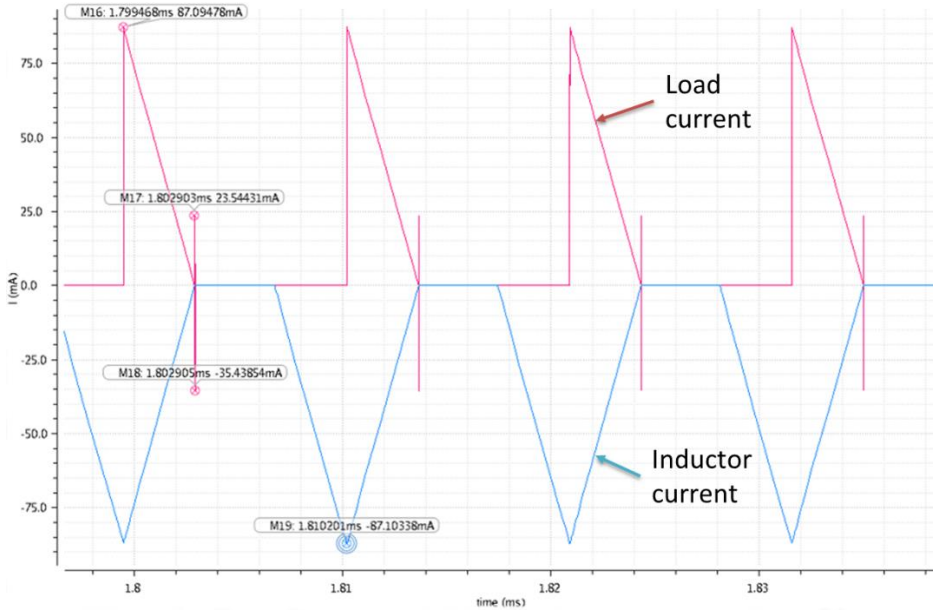

Fig. 21 Simulated waveforms of respectively: current inside the external inductor (blue) and current provided to the output load (red) for the proposed DC/DC converter

Moreover, a parasitic current peak is observed at the end of the OFF phase, mainly due to capacitive coupling between drain node and gate / source nodes of the output switch *B*.

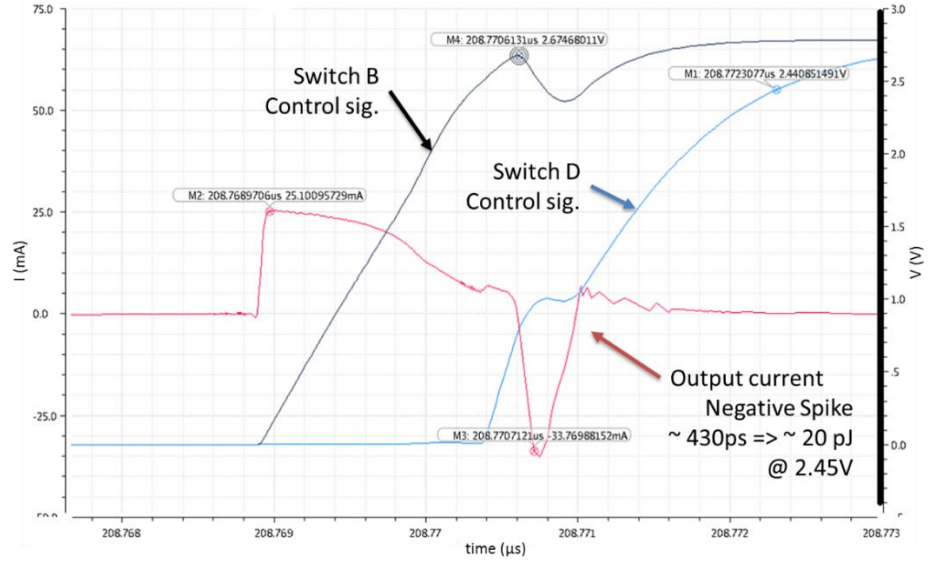

Fig. 22 Analysis of the parasitic current peak that occurs during commutations of proposed DC/DC converter

As a matter of fact, in order to reduce the intrinsic resistance of the switches, which is actually a predominant factor in determining the overall efficiency of this kind of DC/DC converters, width values must be chosen in the order of few tens of millimeters, this leading to significant parasitic capacitances. Nevertheless, the impact of such peaks is substantially insignificant when compared to the amount of energy transferred per cycle, as observed in Fig. 22.

It is also worth noting the time gap between the rising of control signal of switch *B* and control signal of switch *D*, which is regulated by delay structure described in Fig. 17 in order to avoid cross-conduction effects.

2.3.2 Physical implementation

Entire design has been developed in a 180 nm BCD technology, which allows to combine on the same substrate bipolar, CMOS and DMOS devices [50]. Thanks to this feature, digital block has been developed with CMOS standard cells using automatic CAD flows, while in main DC/DC 5V-tolerant MOS devices have been mainly used. For power switches double diffusion DMOS are finally used. Resulting physical layout is presented in Fig. 23 with different sections highlighted. Along with described modules, some complementary circuits are designed for service purposes.

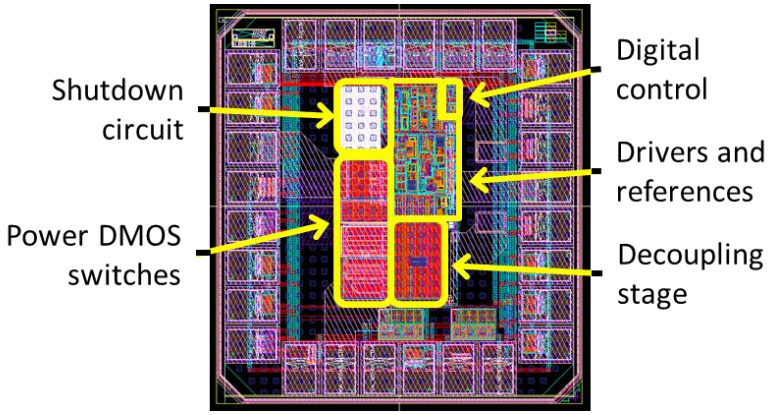

Fig. 23 Layout of proposed DC/DC converter with current limitation based on a cascade of current mirrors

A series of adopted circuits was made available in process libraries, among which:

- Drivers
  - Digital signals are both 1.8 V and 5 V due to compatibility issues with external world, so dedicated level shifters must be included.

- Output switch MOS B is connected to a load which may have a voltage level higher than battery supply, so its control signal on gate terminal should be able to reach the output voltage in order to correctly switch it off, this requiring a specific driving circuit.
- Operative range of proposed design is 2.0 V – 6.2V, in order to match specifics of common commercial batteries. Since operative range of standard CMOS devices in the adopted 180 nm BCD technology is maximum 5 V, then ad-hoc regulators are needed to clamp supply voltage.
- Specific delay RC circuits are designed to regulate timing aspects of particular signals, like for example for control signals of switch drivers to avoid cross-conduction (Fig. 17).

- References
  - Dedicated circuits are included to generate bias currents for analog circuits.
- Shutdown circuits
  - Additional modules are designed in order to completely switch off all the circuits so providing a zero-bias shutdown mode.

In this scenario, the proposed design was included in a more articulated integrated circuit dedicated to power management functions for IoT applications. The overall design is shown in Fig. 24.

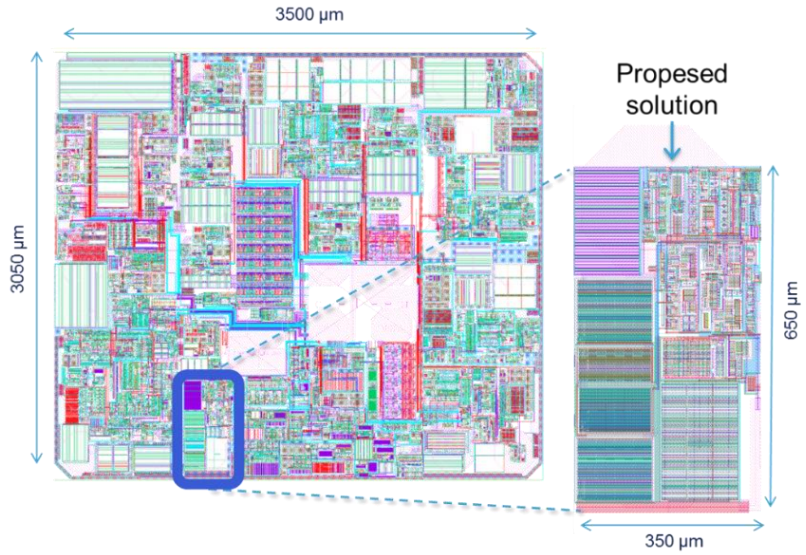

Fig. 24 Prototype of the power management IC including the proposed solution

Finally, in Table 2 a summary of principal features of the implemented design is presented.

Table 2 Electrical characteristics of the proposed DC/DC architecture with current limiter module based on a cascade of current mirrors

Parameter			Value		Unit
Design					
Input Voltage Range			2.0-6.2		V
Output Voltage Range			0-8		V
Quiescent Current			4		µA
Efficiency	Limiter	DC/DC	95	89	%
	Overall		85		
Thresholds (α_H- α_H)			92-98		% of V_{BAT}
Area			0.2275		mm^2
Switch A (W/L)			14/0.6		mm/µm
Switch B (W/L)			14/0.6		mm/µm
Switch C (W/L)			7/0.43		mm/µm
Switch D (W/L)			6/0.6		mm/µm
External components					
C_{BUFF}			1		µF
L			100		µH

2.4 An ultra-low power architecture

A second architecture has been investigated with an ultra-low power current limitation circuit, in order not to drain battery charge over time and to better suit the shortage of energy typically experienced in harvesting applications.

The structure of the limiting circuit is shown in Fig. 19, and basically consists of a feedback architecture with a sense resistor and a control P-MOS driven by an op-amp with a fixed input offset.

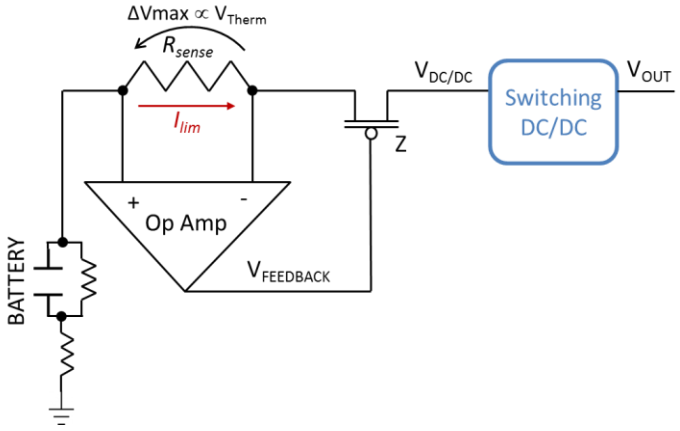

Fig. 25 Block diagram of the proposed structure of the current limiting stage based on feedback architecture with an operational amplifier and a sense resistor

From an operative point of view, the operation amplifier is designed to have a fixed input voltage offset. Resistor R_{SENSE} is dimensioned to have a voltage drop equal to the input offset when the desired current is flowing. Consequently, the operation amplifier tries to maintain the voltage drop constant across the resistance by modulating the impedance of the PMOS *Z* through its gate potential.

This is a simpler solution compared to the one presented in section 2.3, and provides a fixed regulation for the current which is defined by the predefined value of the resistor R_{SENSE}. On the other hand, this architectures guarantees a significantly lower power consumption since bias currents are only related to the implementation of the operational amplifier, while in the previous solution the adoption of the cascade of various mirror stages requires the duplication of a scaled current in each stage. Such lower static currents in the order of few hundreds of nanoamperes produces a negligible effect of the state of charge of the battery over time. The most remarkable aspect related to this solution is the introduction of specific dynamic biasing techniques, which guarantee high slew rates of the output signal yet maintaining low values of quiescent currents. More precisely, target values for the design are less than 1 µA of quiescent current with output responses of 20 mV/µs for output loads of 500 pF.

2.4.1 Feedback regulation with dynamic biasing

From an implementation point of view, the operation amplifier consists of a common structure with an input differential stage and a gain stage, plus biasing circuits.

In order to obtain a stable value for the offset value, a BJT differential stage is proposed in Fig. 26.

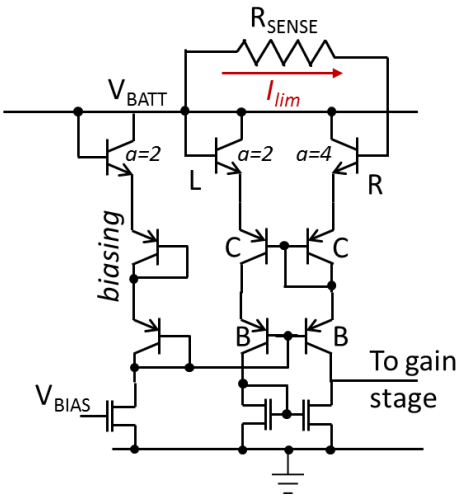

Fig. 26 Differential stage of the proposed operational amplifier

Main differential pair if formed by BJT devices *L* and *R*. Since their area is different, while their collector currents are equal due to the connected nMOS current mirror, then an input offset proportional to the thermal voltage is obtained, accordingly to the formula:

(xix) $$V_{OFFSET} = V_T \cdot \ln\frac{a(R)}{a(L)} = \frac{kT}{q} \cdot \ln 2 = 18\ mV\ (@\ 300\ °K)$$

The offset is then only dependent on thermal voltage, which is mainly uncorrelated to process variation but directly proportional to temperature. On the other hand, R_{SENSE} has a temperature dependence too, according to its *Temperature Coefficient of Resistance (α ppm/°C)*, so that the resulting limited current can be expressed with the following formula:

(xx) $$I_{lim} = \frac{V_{OFFSET}}{R_{SENSE}} = \frac{kT \cdot \ln 2}{q \cdot R_{SENSE\_nom}[T\alpha 10^{-6} + (1 - T_{nom}\alpha 10^{-6})]}$$

being R_{SENSE_nom} the nominal value of R_{sense} at T_{nom} (typically 300 °K). If the *Temperature Coefficient of Resistance* - α- is equal to $T_{nom}^{-1} \cdot 10^{-6}$, then resistor R_{sense} is in first approximation proportional to absolute temperature (PTAT), and as a consequence the limited current I_{lim} is no longer dependent on temperature, as expressed in:

(xxi) $$I_{lim} = \frac{kT \cdot \ln 2}{q \cdot R_{SENSE\_nom}\left[T \cdot T_{nom}{}^{-1}\right]} = \frac{kT_{nom} \cdot \ln 2}{q \cdot R_{SENSE\_nom}}\ (if\ R_{sense}\ PTAT)$$

Common aluminum resistors, which has a temperature coefficient of about 3900 ppm/°C, can be a good choice to approximately match the required 3333 ppm/°C in order to obtain the desired PTAT resistance. Alternatively, other elements can be adopted, like Tantalum or Constantan, which offers a closer value of temperature coefficient, or it is also possible to combine heterogeneous resistors together.

Common base structure *B* is used to set bias current in the differential stage, while cascoded pair *C* is added in order to shrink the dynamic of the output signal so improving the time response of the system.

Considering these dimensioning, in order to obtain a controlled current of about 400 µA, a resistor of about V_{OFFSET}/400 µA = 18 mv/400 µA = 45 Ω is the correct choice.

An additional stage is added in order to increase overall gain and improve response time of operational amplifier. The gain stage is depicted in Fig. 27.

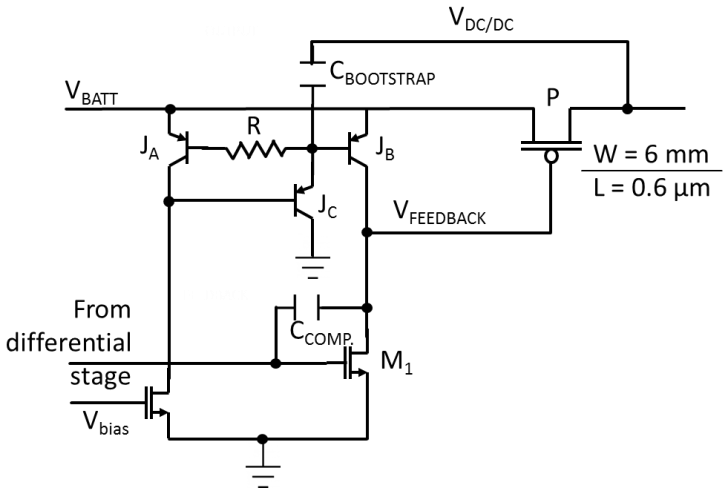

Fig. 27 Gain stage of the proposed operational amplifier

Gain is obtained by mean of the g_m of M_1, while polarization current is provided by J_B. The combination of J_A, J_B and J_C provides a dynamic biasing architecture which is fundamental in order to contain the quiescent current of the circuit while guaranteeing high frequency response.

During normal operation, output node $V_{DC/DC}$ suffers from relatively fast transitions from high to low voltage values due to the switching activity of the subsequent DC/DC converter, and as a consequence the feedback operation amplifier should guarantee very fast transitions, in the order of few microseconds, from low to high voltage values in order to compensate the current flow through the control MOS *P*. On the other hand, the parasitic capacitance associated with MOS *P* is relatively high, in the order of hundreds of picofarads, since its form factor should be large enough to minimize parasitic resistance.

So in order to limit the static power consumption, a dynamic biasing mechanism has been adopted to provide higher bias only during these fast transitions.

The polarization stage is based on a buffered feedback BJT current mirror (J_A, J_B, J_C), which copies the bias current to the common emitter stage, while a bootstrap capacitor $C_{BOOTSTRAP}$ is added which connects the common base node and the fast-moving output node. As output node rapidly goes down, the bootstrap capacitor forces a higher V_{BE} voltage on J_B, thus temporary increasing the available current to charge the feedback node. The additional bias then decays with a time constant given by the bootstrap capacitance and the series resistance *R* towards the BJT base. Thanks to this architecture, starting from a static bias current of solely 800 nA for the whole op-amp, it is possible to obtain

a peak output current of up to 10 µA with a voltage drop of 100 mV on the bootstrap node during commutations.

Finally, a compensation capacitor C_{COMP} is included for stability purposes.

Results and dimensioning of passive elements used for dynamic polarization and compensation are reported in Table 3.

Table 3 Dimensioning of the dynamic biasing architecture for the proposed solution of a current limiter based on operational amplifier feedback and sense resistor

Parameter	Value	Unit
$C_{BOOTSTRAP}$	20	pF
$C_{COMPENSATION}$	150	fF
R	1	MΩ
Time constant of dynamic polarization	20	µs
Bias current	800	nA

Biasing voltages are obtained through a bandgap structure reported in Fig. 28, featuring a common BJT architecture with degeneration resistor *R1* [51]. The insertion of *B1* and *B2* as bootstrap devices is necessary to guarantee the correct switching on of the bandgap after power on.

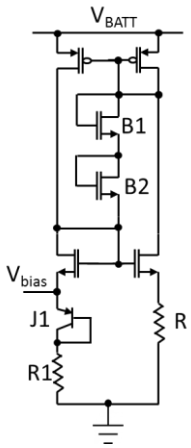

Fig. 28 Bandgap reference voltage circuit of proposed operational amplifier

2.4.2 Simulation results

In Fig. 29 simulated results are shown related to limiter module with a 3 V battery source. It is possible to note the fast transition of the $V_{DC/DC}$ node of about 30 mv/µs and the resulting compensation of the gate voltage of PMOS (in red). The consequent regulation of the battery current in blue shows a stable behavior during the transition with a small variation between 430 µA and 330 µA with a

nominal expected value of 400 µA. Furthermore a short impulse of about 20 mA for 10 ns is observable at the end of transition mainly due to commutation of the digital logic, especially with reference to driving elements of the power MOSFETs. A slow variation of regulated current during commutation is in any case acceptable since it doesn't introduce degradation effects for the battery source, while the final peak is anyhow negligible with respect to the ones required by the DC/DC stage and it can be potentially reduced by using proper filter capacitors. The capacitance associated to the gate of MOS *P* is approximately 500 pF, and thanks to the dynamic biasing providing an extra current of 10 µA the required slew rate of 20 mV/µs is eventually obtained.
The switching stage is the same as in the previous solution and therefore for related waveforms the reader can refer to Fig. 21 and Fig. 22.

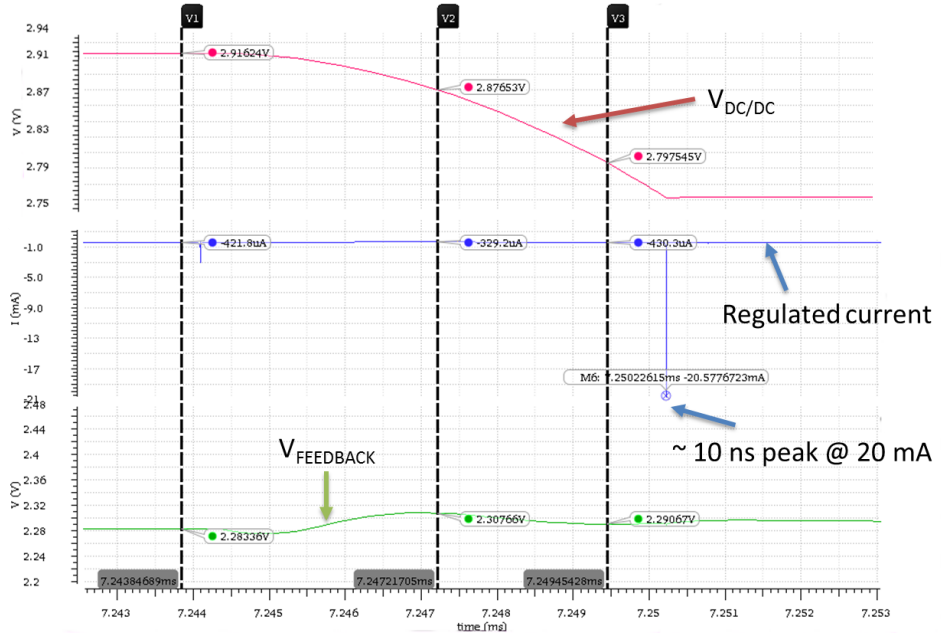

Fig. 29 Simulated waveforms of respectively: output voltage (red), regulated current (blue) and feedback control signal (green) for the proposed solution of a current limiter based on operational amplifier feedback and sense resistor

2.4.3 Physical implementation

From an implementation point of view, in order to minimize power consumption, the operating range of solution has been reduced to up to 5 V, which is sufficient for most rechargeable Li-ion batteries operating at 4.2 V. Then, in this specific version of the circuit, no additional gate driver was necessary. Moreover, switch-off circuits have also been eliminated so that bias current of the entire system can be reduced to that of the current limiter module.

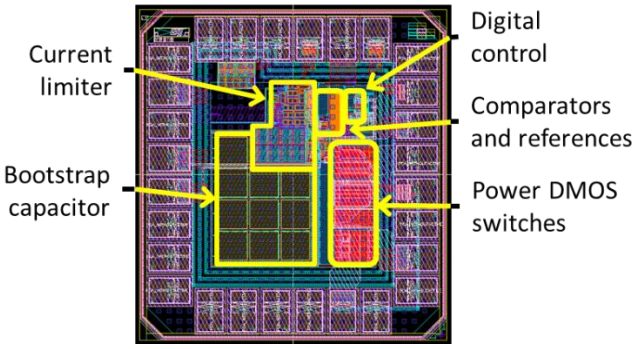

Fig. 30 Layout of the proposed DC/DC converter with current limitation based on a feedback architecture with operational amplifier and an external sense resistor

Layout of designed solution is presented in Fig. 30, where it is clear that a considerable portion of the overall area is used to implement the bootstrap capacitor for dynamic biasing.

Moreover, in this version of the circuit, the delay blocks used to shift edges of control signals of power switches to avoid cross-conduction are implemented through specific digital delay blocks instead of standard RC circuits, in such a way that their insertion has been integrated in the design of the digital block.

Final simulated results and characteristics of the proposed solution are reported in Table 4.

Table 4 Electrical characteristics of the proposed DC/DC architecture with current limiter module based on a feedback architecture with operational amplifier and sense resistor

Parameter			**Value**	**Unit**
Design				
Input Voltage Range			2.0-5.0	V
Output Voltage Range			0-5	V
Quiescent Current			0.8	µA
Efficiency	Limiter	DC/DC	95 | 94	%
	Overall		89	
Thresholds (α_H- α_H)			92-98	% of V_{BAT}
Area			0.3454	mm^2

2.5 An improved efficiency by means of step-wise energy transfer architecture

One of the most relevant limitation about the proposed architecture is the efficiency loss due to the first limitation stage. Aiming at overcoming this limitation an improved solution is proposed to implement a more efficient

energy transfer between the buffer capacitor and the output load, in order to partially compensate the energy losses of the first stage.

The modified approach consists in introducing the concept of quasi-adiabatic capacitive charge [52], in which the overall charge of a capacitor is split into multiple charges at intermediate values of the final voltage. This method is proved to be the best solution for capacitive charge in terms of power dissipation [53]. Using this idea, a stepwise charge of the output is proposed which actually splits the transfer into N consecutive steps of 1/N energy amount, as shown in in Fig. 31.

As a consequence, peak current inside the inductor is limited with respect to the case of a single step, which also reduces losses. As a matter of fact, since the circuit is basically composed of resonant LC elements, the current waveform is a portion of an exponentially damped sinusoid, where the damping factor is related to all parasitic resistances in the current path.

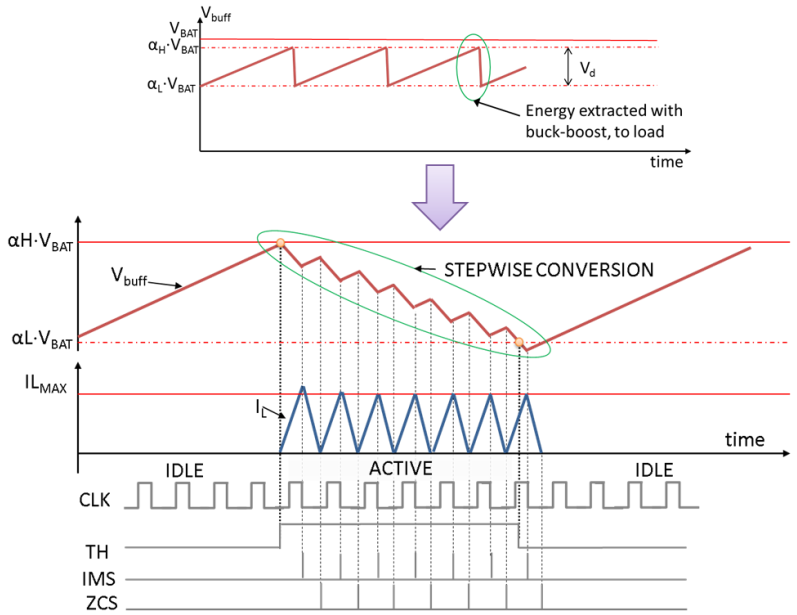

Fig. 31 Waveforms of respectively: buffer capacitor voltage (red), current flowing inside inductor (blue) and control signals (grey) for the proposed solution of a DC/DC converter with stepwise energy transfer

Each stepwise energy transfer has a shorter duration than a one-shot transfer, then the damping effect is limited too [54], which means that the fraction of lost energy is reduced. As in quasi-adiabatic charge, the split is applied to the output voltage, so that the resulting charge is not linear.

From a practical point of view, an additional external clock source is provided to the digital block in order to regulate the timing of each step.

Furthermore, a complete redesign of the digital functionality is necessary in order to handle the new stepwise approach.

In the original solution, the *ON phase* lasts exactly the time needed to discharge the buffer capacitance from $\alpha_H \cdot V_{batt}$ to $\alpha_L \cdot V_{batt}$ (see section 2.2.6), while the *OFF phase* lasts exactly the time needed to nullify the current inside the inductor. Differently, in this case, as soon as the high threshold is overcome, i.e. when the *TH signal* is asserted, the stepwise transfer is started, and a precise sequence of *ON-OFF phases* is performed, each regulated by the frequency of the external clock.

Always referring to Fig. 31, a new signal *IMS* (I max switch) is added, which is necessary to trigger the changeover between an *ON* and *OFF phase*, and which is generated from the clock signal, as explained in section 2.5.1. The *OFF phase* indeed always ends as soon as the current inside the inductor falls to zero, as in previous solution. It is obvious that the clock frequency, by regulating the duration of the *ON phase*, regulates accordingly the maximum current flowing through the inductor.

The use of a generated *IMS* signal instead of the simple clock signal is necessary due to synchronization problems with the control signals that advise the overcoming of the high and low threshold. As a matter of fact a problem may occur if the first *ON phase* is too short, i.e. the first *IMS* edge is too close to the edge of the *TH* signal. In this circumstance the maximum current inside the inductor is therefore limited, yet a minimum value is required by the *ZCS* comparator to properly detect the zero-cross event. In other words, *ZCS* comparator is able to correctly detect the zeroing of the inductor current only if it has reached a minimum value in advance, as shown in graph of Fig. 32.

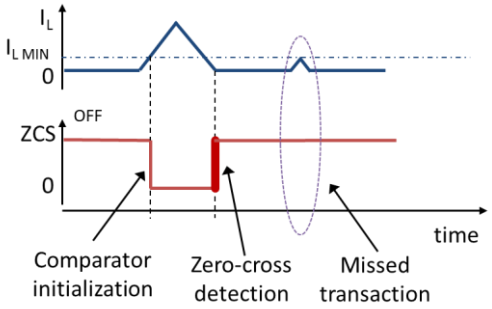

Fig. 32 Timing issue in detecting zero-current condition for proposed DC/DC converter with stepwise energy transfer

2.5.1 Maximum current signal (IMS) generation

For this reason *IMS* signal is introduced, which is generated as following:

- When *TH* goes high, if *CLK* is high then *IMS* is triggered by a positive edge of *CLK*. On the contrary, if *CLK* is low then *IMS* is triggered by a negative edge of *CLK*. In this way the first *ON phase* after DC/DC activation has a length of at least half clock period.

- After *TH* goes down, the current energy transfer is completed, that means that the ON phase is in any case ended by the *IMS* signal, even if *TH* has gone done in the meanwhile. Again, this is necessary to prevent an excessively short first stage and the resulting malfunctions of control comparators. With this behavior, the voltage of buffer capacitor may potentially fall down below the low threshold, this having a negative impact on efficiency. Nevertheless this is a negligible effect compared to the advantages provided by stepwise transfer.

The proposed solution has a positive impact on converter efficiency if compared to a single-step architecture. Under the approximation that each step has a triangular current waveform of length T_{CLK}, energy losses due to resistive paths can be estimated as:

$$E_{LOSS} = \int_0^{T_{CLK}} R \cdot I(t)^2 \cdot dt = \int_0^{T_{CLK}} R \cdot \left\{ \frac{I_{MAX}}{T_{CLK}} \cdot t \right\}^2 \cdot dt = R I_{MAX}^2 \frac{1}{3} T_{CLK} \qquad (xxii)$$

As a consequence, a general equation for comparing single-step versus stepwise transfer is

$$\frac{E_{LOSS(multi)}}{E_{LOSS(single)}} = \frac{R \cdot \frac{1}{3} \left(I_{MAX(multi)} \right)^2 \cdot N_{STEPS} \cdot T_{CLK}}{R \cdot \frac{1}{3} \left(\sqrt{N_{STEPS}} \cdot I_{MAX(multi)} \right)^2 \cdot \sqrt{N_{STEPS}} \cdot T_{CLK}} = \frac{1}{\sqrt{N_{STEPS}}} \qquad (xxiii)$$

The resulting improvement in efficiency is

$$\eta_{multi} = \frac{E_{IN} - E_{LOSS(multi)}}{E_{IN}} = \frac{E_{IN} - \frac{E_{LOSS(single)}}{\sqrt{N_{STEPS}}}}{E_{IN}} = \eta_{single} + \left(1 - \eta_{single}\right) \cdot \left(1 - \frac{1}{\sqrt{N_{STEPS}}}\right) \qquad (xxiv)$$

basically proportional to the inverse of the square root of the number of steps. In Fig. 33 a graph is presented which shows the estimated improvement in transfer efficiency thanks to step-wise transfer with respect to different single-step efficiencies.

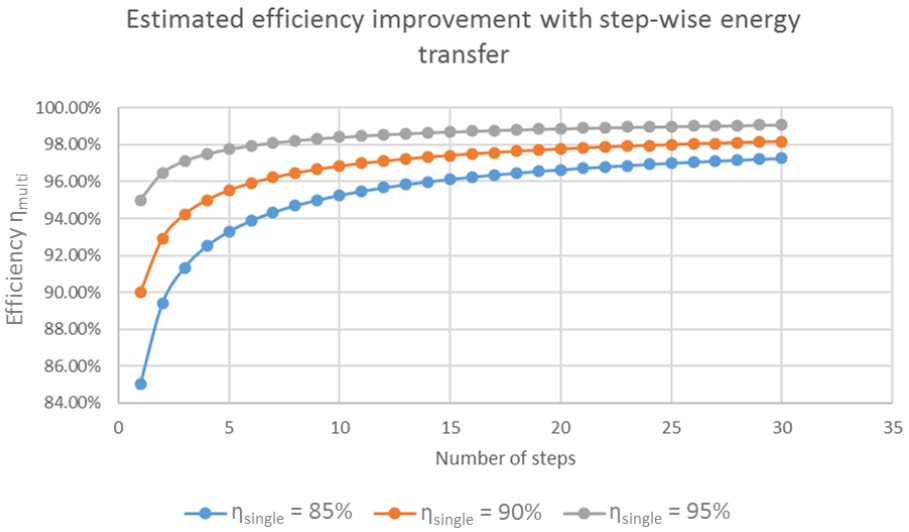

Fig. 33 Analytic graph of the efficiency improvement due to step-wise energy transfer: obtainable efficiency vs number of steps

Considering the impact on efficiency due to the introduction of the clock, which operates at hundreds of kHz in our case, state-of-the art external oscillators operating in this range feature bias currents down to 500 nA [15], while integrated solutions reach down to 24 nA [16]. In worst case of an external oscillator, the overall impact on efficiency due to the additional consumption can be estimated in the order of 0.5(µA)/400(µA) = 0.12%.

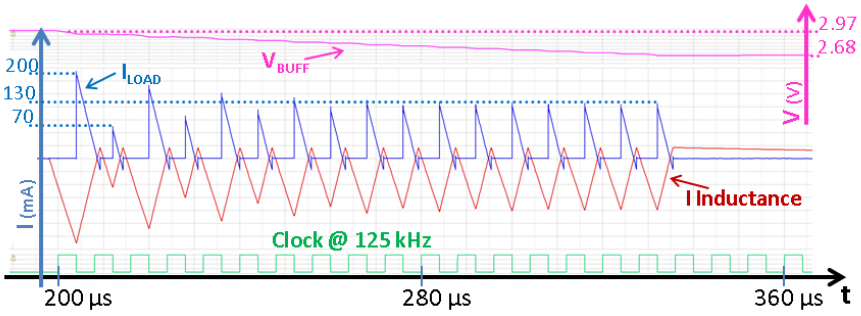

Fig. 34 Simulated waveforms of respectively: buffer capacitor voltage (purple), current flowing inside inductor (red), current provided to the output load (blue) and clock signal (green) for the proposed solution of a DC/DC converter with stepwise energy transfer

Fig. 34 depicts simulated current waveforms for inductor and output capacitance, showing a 17-step transfer with a maximum value I_{MAX} of about 130 mA lasting 17 clock periods (T_{CLK}) at 125 kHz. Simulation results, with C_{buff} = 20 µF, L = 100 µH and f_{CLK} = 125 kHz are shown in Table 5.

Table 5 Electrical characteristics of the proposed DC/DC architecture with stepwise energy transfer

Parameter			Value		Unit
Input Voltage Range			2.0-6.2		V
Quiescent Current			4		µA
Efficiency	Limiter	DC/DC	93	92	%
	Overall		86		
Thresholds (α_H- α_H)			93-97		% of V_{BAT}
Area			0.2335		mm²

For what concerns the implementation of current limiter module, drivers and other components this architecture reuses the solution provided for the adaptable limiter design (see section 2.3).

The two solutions are therefore substantially identical except for the implementation of the stepwise transfer procedure, which actually impact only in the design of the digital block, while all other modules are unchanged.
Layout of this solution is presented in Fig. 35, where it is possible to notice the enlargement of the digital block due to its increased complexity.

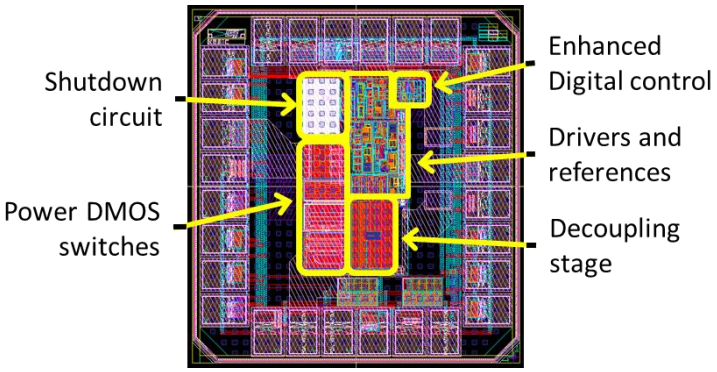

Fig. 35 Layout of proposed DC/DC converter with stepwise energy transfer architecture

2.6 Results and discussion

Preliminary tests have been performed on samples of the three integrated solutions in order to verify general behavior and validate proposed architectures. Aiming at speeding up testing time a common dual-in-line ceramic package (DIP) was used, mounted on a breadboard with external passive elements. On the other hand, high parasitic resistances – in the order of few ohms – and inductances – in the order of few nanohenries – must be taken into account when considering efficiency and resulting waveforms. Further analysis can be performed by using more efficient solutions like a printed circuit board (PCB)

with surface-mount-device (SMD) packages. Particular attention must be also paid in the choice of buffer capacitor and inductor, in order to minimize leakage currents for capacitor and parasitic resistances for both capacitor and inductor. More precisely, the peak currents associated to the switching activity of the DC/DC converter flow from buffer capacitor to inductor and from inductor to external load, thus any resistive element on these two paths has a significant impact on efficiency of overall system, as already mentioned in section 2.5.

2.6.1 Adaptable limiter architecture

First measures relate to the *adaptable limiter architecture* which actually provides the reference design of the three solutions and which can be therefore used as a term of reference for results of other test chips.

In Fig. 36 an overview of the DC/DC conversion operation is depicted.

Referring to Fig. 13, red line represents the voltage on the buffer capacitor C_{buff}. As explained in section 2.2.2 and described in Fig. 12, it has a saw-tooth shape due to the combined effect of the input current limitation (voltage linearly increase during the recharge phase till an high-threshold value) and the consequent extraction of a predefined amount of energy (voltage rapidly decrease down to a low-threshold voltage).

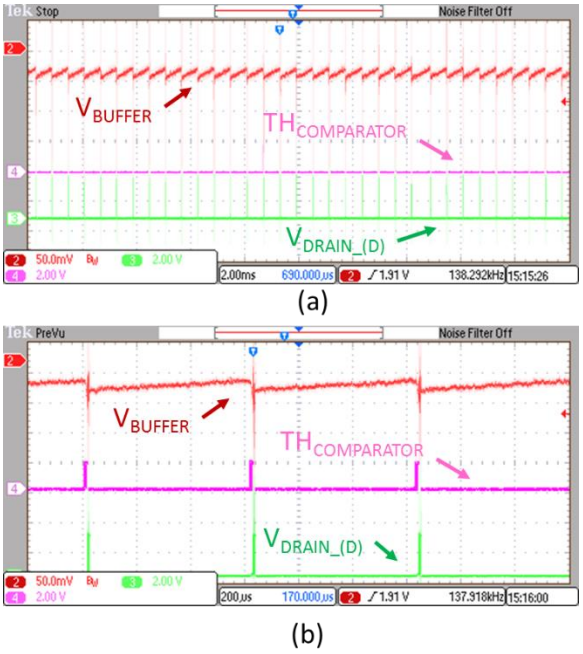

Fig. 36 Waveforms of DC/DC conversion for "adaptable limiter architecture" solution. Referring to block diagram in Fig. 13, respectively: buffer capacitor voltage (red), threshold comparator signal (purple) and drain voltage of MOS D (green). V_{IN} = 2 V; V_{OUT} = 2.77 V; C_{buff} = 53 µF; L = 100 µH; α_H = 97.775%, α_L = 97%. In (a) with 2 ms time division, in (b) with 0.2 ms time division.

It is important to notice that in order to obtain a picture easier to understand, an offset equal to supply voltage (V_{IN}) is applied to this signal (V_{BUFF}), so that in this case it is ranging approximately between 2 V and 1.95 V.

In this test the current limitation was set to 1 mA, while threshold was set to 97% and 97.75%, respectively. The input current was monitored through a HP® 34401A multimeter in series with the power supply, showing an actual limited current I_{LIM} of 1.3 mA, which differs from the desired one due to the inaccurate value of the 100 nA external reference current used by the internal mirror to perform limitation. The relevant outcome is the effective limitation that can be achieved through the designed circuit, which is also confirmed by the linear charge of the buffer capacitor as depicted in Fig. 13. As a matter of fact, a 53 µF buffer capacitor is used with an input voltage V_{IN} of 2 V and an inductor of 100 µH. With these data, an actual ramp of $C_{buff} \cdot (\alpha_H - \alpha_L)V_{IN}/I_{LIM} = 610$ µs is expected, equal to the measured one. All other three limitation values (0.4, 5 and 15 mA) was tested too with similar results. Purple line represents the threshold comparator output, which is set high each time the buffer voltage V_{BUFF} exceeds the high threshold and returns to zero as soon as it drops below the low one. In this test, considering an input voltage of 2 V, thresholds are 1.955 V and 1.94 V, respectively. With reference to equation (xvi), the resulting efficiency of this block is nominally 97.375%.

Green line is the drain voltage of MOS *D*. During recharge phase it is grounded as MOS *D* is switched on, as well as during the ON phase while the inductor is charged. Then, during the subsequent OFF stage, starting on the negative edge of the *TH* signal, MOS *D* is switched off and its drain node is shorted to the output load through MOS *B*, so its drain voltage follows output voltage.

A more focused view is shown in Fig. 37 (a). It is worth noting that during the ON phase (*TH* signal high) the drain voltage slightly increases due to its parasitic on-resistance, which creates a drop proportional to the current flowing in it. Then, during the subsequent OFF phase the drain voltage is forced by the inductor to be higher than output voltage, just enough to allow the flow of current from inductor to output. As current decrease, the drain voltage gets closer and closer to the output voltage till current drops to zero and drain voltage is equal to output one, this ruling the end of the OFF phase.

Moreover, in Fig. 37 (b) waveform of drain voltage of MOS *C* is shown. Similarly to MOS *D*, during the recharge phase it is grounded as MOS *C* is switched on too. Conversely to MOS *D*, during ON phase MOS *C* is switched off, so its drain voltage follows the decreasing buffer capacitance voltage, whilst during OFF phase it is switched on and it consequently allows a flow of current from its source (connected to ground) through the inductor towards the output node. In this latter situation, the drain node if forced to be slightly below ground value, in order to allow a positive current from source to drain, as reflected in Fig. 37 (b).

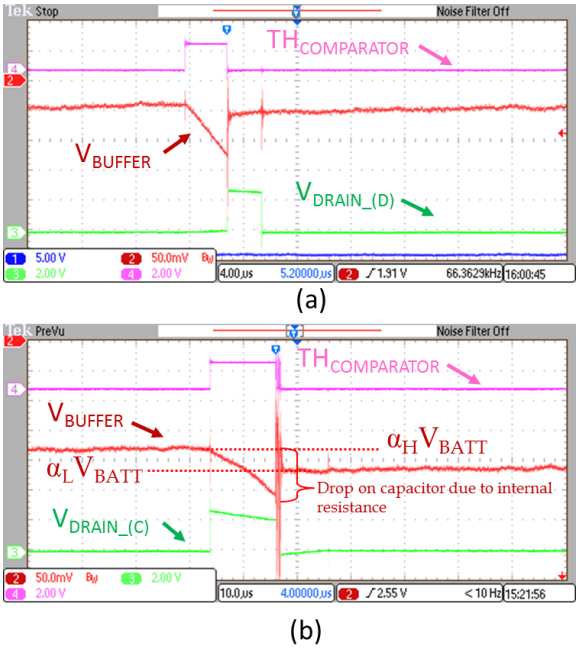

Fig. 37 Waveforms of switching signals of "adaptable limiter architecture" solution. Referring to block diagram in Fig. 13, respectively: buffer capacitor voltage (red), threshold comparator signal (purple). In (a): green line is drain voltage of MOS D, V_{IN} = 2 V; V_{OUT} = 2.77 V; C_{buff} = 10 µF; L = 100 µH; α_H = 98%, α_L = 97%. In (b): green line is drain voltage of MOS C, V_{IN} = 2 V; V_{OUT} = 2.77 V; C_{buff} = 53 µF; L = 100 µH; α_H = 91.25%, α_L = 89%.

Moreover, two different buffer capacitor C_{buff} were used to obtain results of Fig. 37 (a) and (b), being respectively 10 µF and 53 µF. As a consequence, peak currents are different and ON phases have different duration. Considering equations (xi), *(x)* and (xii), an estimated duration for the *ON phase* is respectively 12 µs (when using 55 µF) and 3.2 µs (when using 10 µF), confirmed by measured values. From the same equations we can therefore estimate the maximum current inside the inductor, which is respectively 215 mA (when using 55 µF) and 61 mA (when using 10 µF). The interesting thing is the voltage drop on the buffer capacitor, reasonably caused by its intrinsic resistance. Combining measured values with analytic equations, values of 0.3 Ω (when using 55 µF) and 1.2 Ω (when using 10 µF) are found for the parasitic resistances of capacitors, which in both cases leads to a transfer efficiency of about 96%, to be multiplied by efficiencies of other stages.

Efficiency of the overall DC/DC was measured by means of the ratio between output power and input power. Input power can be easily calculated since current is kept constant by the integrated circuit and was measured through an HP® 34401A multimeter in series with a constant voltage supply. On the output node, another constant voltage supply was connected in order to

emulate the capacitive load, which in a typical application can be for example a super-capacitor. Differently from input node, in output node the current shape is not flat but it has an impulsive triangular characteristic, so a low-pass filter was inserted in order to extract the average current, being R = 10 Ω and C = 10 mF, and its value was then measured with an Agilent® 34401A multimeter. With an output voltage of 2.77 V, efficiencies found are respectively 57% (when using 55 µF) and 62% (when using 10 µF), which is compatible with simulated results. The poor efficiency outcome in this case is due to the high parasitic resistances of the board and to the low input voltage (2 V), which is not sufficient to properly switch on the integrated n-MOS and p-MOS of DC/DC converters which therefore maintain a high on-resistance. Moreover, the higher is the buffer capacitor, than the higher is the maximum current and consequently the lower is the efficiency, as confirmed by measures. Efficiency results for different values of input voltage, output voltage and buffer capacitor are presented in Table 6.

2.6.2 Improved efficiency architecture

Further tests were performed on the *improved efficiency architecture*, with the insertion of an external clock source in order to implement the described stepwise energy transfer. In Fig. 38 waveforms of switching signals are shown, with two different time divisions. Red line is voltage of buffer capacitor, purple line is threshold comparator signal, green line is the drain voltage of MOS *D*, and blue line is the clock signal. It is evident the effect of the stepwise transfer as the discharge process is now divided into multiple sub-steps controlled by the external clock source at 125 kHz. General characteristics related to current limitation and recharge phases are not further analyzed in this section as they are the same as in the other solution already discussed since they share the same architecture, while the remarkable thing in this case is the verification of the stepwise procedure. As expected, a correct synchronization with the clock signal is accomplished at the beginning of the transfer phase – the first *ON phase* has a duration of at least one clock semi-period – and at the end of the transfer phase – one complete *ON-OFF phase* is always brought to an end –, as depicted in Fig. 38 (a). In Fig. 38 (b) a closer look on the interaction between clock signal and switching frequency is presented. The *ON phase* starts at the end of the previous OFF phase, and lasts till the subsequent useful clock edge, which is the positive one in this case.

During the *ON phase* the drain voltage of MOS *D* slightly increases due to the drop caused by the current flowing through the on-resistance of the MOS itself. Conversely, during the *OFF phase* the drain node is shorted to the output, so it follows its value, as already explained in previous solution. The measured waveforms are indeed compliant with the simulated one reported in Fig. 34. For what concerns efficiency values, considering an input voltage of 2 V, output voltage of 2.77 V and buffer capacitor of 10 µF, a value of 71.8% can be observed.

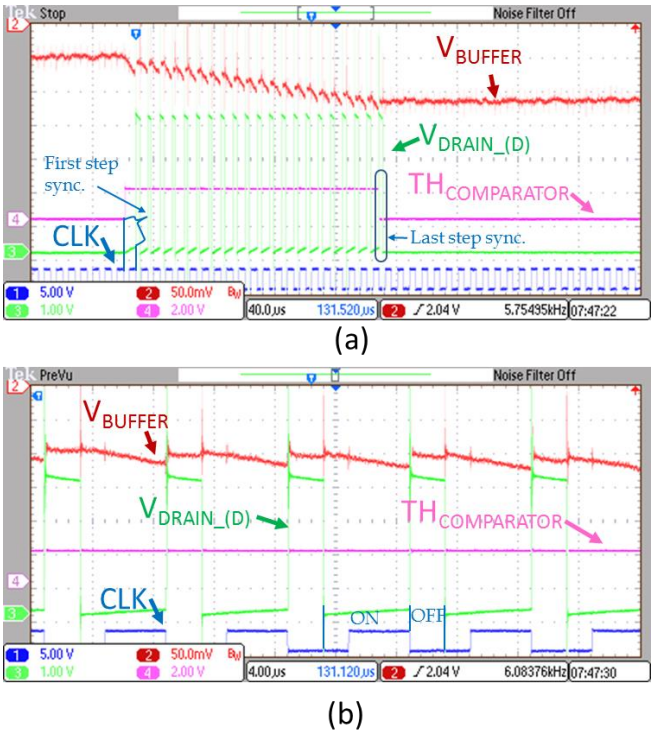

Fig. 38 Waveforms of switching signals of "improved efficiency architecture" solution. Referring to block diagram in Fig. 13, respectively: buffer capacitor voltage (red), threshold comparator signal (purple), drain voltage of MOS D (green), and clock signal (blue). V_{IN} = 2 V; V_{OUT} = 4 V; C_{buff} = 53 µF; L = 100 µH; α_H = 97.775%, α_L = 97%. In (a) with 40 µs time division, in (b) with 4 µs time division.

In the same condition, the first solution not implementing stepwise transfer has only 57% efficiency, this demonstrating that this advanced architecture can actually improve overall efficiency. Moreover, by increasing the clock frequency it is possible to control the number of steps of the transfer, with a further improvement in efficiency as expressed in equation (xxiv). As a matter of fact, passing from 125 kHz to 140 kHz produces an increase of 1.3% in efficiency from 71.8% to 72.1%. Complete results are shown in Table 6.

2.6.3 Ultra-low power architecture

Finally results related to the *ultra-low power architecture* are presented.

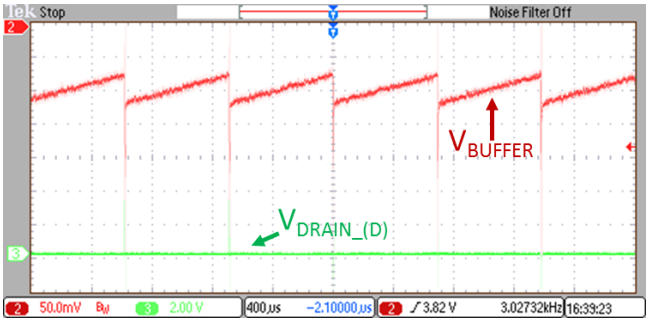

Fig. 39 Waveforms of switching signals of "ultra-low power architecture" solution. Referring to block diagram in Fig. 13, respectively: buffer capacitor voltage (red), drain voltage of MOS D (green). V_{IN} = 2 V; V_{OUT} = 4 V; C_{buff} = 10 µF; L = 100 µH; α_H = 97.775%, α_L = 97%.

In Fig. 39 an overview of the switching signals is presented. The first analyzed aspect is the quiescent current consumption, which was confirmed to be about 800 nA in line with simulated results. The test was performed at 1.8 V supply voltage with a HP® 34401A multimeter, while more exhaustive tests at higher voltages cannot be performed at the moment due to unexpected current losses in the I/O pad circuits that have already been identified and that will be fixed in a future release. Similarly, for what concerns current limitation circuit it was verified through a HP® 34401A multimeter in series with voltage supply, and it is also confirmed by the linear charge of buffer capacitor reported in Fig. 39. Moreover, values of sense resistors are compatible with analytic formulation (xix). Nevertheless, an unexpected dependence of the limitation threshold on the supply voltage can be observed, which is not directly attributable to the issue on I/O pad circuit and which must be further investigated.

For what concerns efficiency, measured results are in line with simulations and other two solution, in the range of 70%-72%, and a complete list is presented in Table 6.

2.6.4 Comparison and future work

A recap of performed tests is shown in Table 6, considering L = 100 µH; αH = 97.775%, αL = 97%.

From a general point of view, all three solutions have been tested and correct functionality was verified. Current limitation architecture has been proved to be a feasible approach in order to design advanced DC/DC converters which guarantee higher durability of supply batteries. Main open points regard measured efficiencies which are far away from expected ones, although specific simulations accomplished with more realistic values of parasitic resistances with respect to actual testing board implementation are compliant with obtained outcome. Moreover, by comparing the multi-step solution with the reference

one, the improvement in efficiency was verified too. Finally, quiescent current analysis and functional verification was performed for the ultra-low power solution, showing a consumption of less than 1 μA.

Nevertheless further tests are necessary in order to fully characterize the integrated design especially in terms of measured efficiency, by developing a dedicated PCB board for minimizing parasitic resistances of interconnection and passive elements, with particular attention to the buffer capacitor and to the inductor, which have to sustain the higher flow of current.

Moreover, more precise measurements have to be implemented on the actual dynamic profile of the current drawn by the battery, in order to effectively characterize the timing response of the limiting circuits, and to evaluate the spurious peaks which may be present during fast commutations between on and off stages of the DC/DC converter. On the other hand, the actual limitation capability outside the few nanoseconds window of fast commutations has been inferred by the linear charge of the buffer capacitance presented in previous sections. It is worth noting that since spurious peaks are in the order of few nanoseconds with slew rates of 20-30 mA/ns, then proper measurement techniques and instrumentation have to be carefully investigated in order to match such constraints.

Finally, considering Table 6, greyed-out results was obtained in similar conditions with similar values of external passive elements, and therefore they can be used to compare the three proposed solutions in terms of achievable efficiency.

Table 6 Recap of performed measures of three proposed solutions of an advanced DC/DC converter for improved battery durability

V_{IN} (V)	I_{IN} (mA)	V_{OUT} (V)	I_{OUT} (mA)	Efficiency (%)	Loss specific origin
adaptable limiter architecture					
C_{buff} = 10 µF					
5	1.373	4	1.190	69.3	Power dissipation on unoptimized breadboard
5	1.373	4.5	1.060	69.5	
5	1.373	4.7	1.013	69.3	
5	1.373	5	0.937	68.2	
2	1.300	2.770	0.585	62.3	High switches resistance due to low supply voltage
C_{buff} = 55 µF					
2	1.300	2.770	0.540	57.5	High switches resistance due to low supply voltage and high inductor current due to high C_{buff}
3	0.600	2.770	0.320	49.2	
improved efficiency architecture					
C_{buff} = 55 µF					
2	1.07	2.770	0.555 @ 125 kHz	71.8	High switches resistance due to low supply voltage and high inductor current due to high C_{buff}
2	1.07	2.770	0.565 @ 140 kHz	73.1	
ultra-low power architecture					
C_{buff} = 10 µF					
5	0.405	5	0.265	65.4	Power dissipation on unoptimized breadboard
4	0.650	4	0.460	70.7	
2	0.217	2.17	0.140	70.0	High switches resistance due to low supply voltage

Chapter 3

Robustness and durability aspects in the design of energy autonomous nodes

An Increasing interest in distributed sensor networks [55] and IoT applications has driven research into the scope of energy harvesting mechanisms towards a more precise field of application. The combination of smart nodes, able to interact with standard wireless communication infrastructures, and energy scavenging modules, which allow nodes to work in a standalone scenario, has proved crucial for the development of both technologies [56].

Since autonomous nodes are expected to operate in very dissimilar surroundings with different energy sources and power densities, the importance of finding efficient ways to exploit available energy is evident, as in many cases the power available from the environment is in the order of microwatts [57] or less.

In terms of robustness and durability two remarkable aspects can be noted

- The absence of the battery source in favor of locally scavenged energy, or even the joint combination of both, can by itself dramatically increase the device lifetime, as battery end-of-life is a common issue for this kind of devices and in many cases it can represent the bottleneck for the reliability for entire system [16].
- Increasing the maximum operative range can guarantee a better mean time between failures in nominal condition so simultaneously improving system robustness too [58].
- Studying solutions with modular communication interfaces or configurable digital control may be an alternative way to improve device usability and extend operative ranges in different environmental framework.

3.1 State-of-the-art solutions

In this context, radio-frequency power harvesting [59, 60] represents both a fascinating solution, due to the opportunity of selectively providing energy through dedicated RF energy showers augmented by smart power beaming techniques [61, 62], and a tough challenge because of the limitations imposed by regulations causing very low voltage and power levels as the distance from the source increases. A comprehensive perspective on RF harvesting techniques

specifically devoted to wireless sensor nodes can be found in [57]. In this field of application most solutions concentrate the greatest effort in optimization of the harvesting module [62, 63], while other studies are proposed to define advanced algorithms to find most efficient transmission rates in complex scenarios [64, 65].

Concerning integrated RF-to-DC converters, an interesting solution is presented in [66] with a 65% efficiency at −20 dBm in UHF band and output voltage up to 1.6 V. Another notable solution is presented in [63], where 1.0 V output is obtained at 27 m distance. The nano-power design of an integrated 1 μW – to 5 mW power management circuit is shown in [67]. The DC/DC converter proposed achieves a peak conversion efficiency of 77% and a minimum start-up voltage of 223 mV. The trend for quiescent power consumption of commercial and academic PMIC implementation is shown in [68].

Furthermore, regardless the adopted energy source, new perspectives are gaining interest, introducing the concept of adaptive behavior of the node accordingly to the available power, for example by dynamically modulating the transmission data-rate in order to best fit the actual power budget. If the node becomes capable of reducing autonomously its power consumption or entering specific idle or sleep states, operation is guaranteed over a wider range of operating conditions, resulting in increased robustness. For example, in [61] a simple adaptive solution is adopted, with solely two possible transmission data-rates and a solar cell as harvesting source. Advanced adaptive solutions are studied in [69], for a general-purpose sensor node in a multi-antenna power transfer scenario. These solutions lie on the development of complex recursive algorithms based on the knowledge of the evolution of stored energy in time, which implies the use of additional power-consuming electronics incompatible with micro-power scenarios. In fact, experimental results demonstrate just a 5-m operative range. A similar approach is used in [65], with an accurate analysis of harvest-and-use and harvest-store-use schemes. Again, the resulting optimization algorithm requires the development of dedicated energy meters interacting with the node MCU to estimate the correct transmission rate. Both solutions are based on an adaptive estimation of best data-rate accomplished by the MCU on the basis of complex monitoring of available energy. Although standard communication protocols – e.g. DASH7 – may perform a communication range up to 5 km, they are also widely used for indoor applications and, in combination with RF harvesting, they can provide an optimum solution for enclosed sensors like smart meters placed inside walls or generic structures.

A complete solution with harvesting module and sensing node is proposed in [70], showing an operative range of 5 m with −8 dBm input power. The block diagram of this solution is presented in Fig. 40, and it is useful to understand some general aspects related to robustness and durability issues in the design of autonomous RF harvesting nodes.

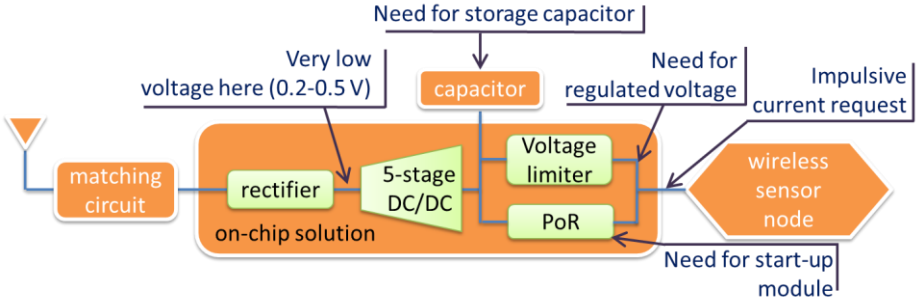

Fig. 40 Block diagram of a state-of-the-art solution of an IoT node with RF harvesting techniques (Y. Syed, B. G. Hegde, T. V. Prabhakar, M. Manjunath and K. J. Vinoy, "RF energy harvesting chip powered sensor node")

Most relevant design aspects are:

- Voltage levels involved in RF harvesting are relatively low, in the order of 200-500 mV [57], so we need aggressive step-up and DC/DC converters in order to rise these levels to acceptable one by the main circuitry of the node.
- Storage elements are required for different reasons. Since harvesting sources are intrinsically discontinuous and energy requested from sensing and communication modules is typically far higher than energy provided by the harvesting module and it also has usually an impulsive shape, then it is necessary to gather energy for a certain period of time before activating the node. Moreover, the dimensioning of such storage element, i.e. typically a capacitor, is not trivial: Big capacitors provides a more stable voltage source, but on the other hand they requires larger areas and extended recharge times; small capacitors are faster but require higher voltage levels in order to store the necessary energy.
- Since supply voltage is provided by a storage element, i.e. a capacitor, then its value is variable in time, especially during activation period when battery is discharged due to the power demand from the node. Hence, voltage regulators may be necessary to provide a suitable value to the electronics of the node.
- Specific modules must be designed to detect the amount of stored energy in the capacitor and to switch-on the sensing module only when energy is enough to perform a complete cycle of sensing and data transmission.

Extending these concepts to other harvesting sources, similar constraints can be considered for example for indoor photovoltaic panels [71, 72, 73] or thermoelectric generators (TEG) [74, 75]. In both cases, and similarly to the RF sources, output voltages involved are in the range of few hundreds of millivolts, with an available power ranging from tens of microwatts for TEGs to hundreds of microwatts for photovoltaic panel. As a consequence, innovative power

management solutions presented in this chapter, which particularly refer to an RF harvesting node, can nevertheless be effectively applied to other harvesting scenarios always in the field of low-power applications.

Generally speaking, a wide range of different applications related to energy harvesting techniques can be considered, which are gaining increasing interest. For example in the development of IoT nodes with embedded wake-up-radio management and localization capabilities [76], the challenge is to design efficient power converters in order to maximize the operative range of the node and implement advanced strategies to perform addressing operation in an ultra-low power scenario. Another widespread approach is to fully integrate the IoT node embedding for example sensing and localization capabilities [77], in order to reduce quiescent currents associated to discrete solutions. This approach implies the development of smart power management to efficiently distribute supply to different blocks of the system (sensing, elaboration, communication, etc.) and potentially switching on blocks in a selective way. Moreover, great focus is shifting to the development of smart nodes with IoT standard compatible communication interfaces [78] [79]. The possibility to easily insert a node in a pre-existing infrastructure, which is also potentially already connected to an Internet gateway, is certainly a significant added value. In this case, from a power management point of view, the development of adaptive algorithms able to dynamically change the behavior of the node (e.g. its data-rate) accordingly to the actual environmental conditions (e.g. the available power), is a promising approach to extend lifetime and durability of the node.

In any case, the development of dedicated power management units and advanced digital control modules is essential to achieve adequate efficiency rates which guarantee the desired operative ranges and lifetime.

3.2 Studied solution: adaptive approach to energy harvesting

As a matter of fact, the most prohibitive obstacle to the diffusion of energy harvesting nodes is the lack of dedicated power converters able to operate with extremely low levels of input power and voltage. However, simply developing more effective power converters or designing more efficient energy transducers is not in general sufficient: power management must go hand in hand not only with obvious requirements in terms of ultra-low power, but also with the development of specific policies for adjusting the behavior of the node according to the availability of energy. Active interaction between the power module and smart node is a promising approach to achieving this target and to developing integrated applications.

Thus, a holistic approach can best tackle this type of issue. On the one hand, circuit design aims at minimizing the power consumption of electronic devices

and, on the other hand, optimized behavioral policies for active node modules need investigating with a view to exploiting the available energy at its best.

3.2.1 IoT standard communication node with feedback power management

The proposed approach consists in enhancing power management of conventional IoT nodes. The aim in this case is to tackle the power conversion problem by using innovative DC/DC converter integrated circuits and by developing advanced management techniques at different levels in order to extend operative ranges of device with consequent benefits for robustness and durability.

As a case study of the previously mentioned technique, a demonstrator system was designed with an ultra-low power approach, with the introduction of

- A custom energy transducer, namely a rectifying antenna – developed by a parallel design team [57]–.
- An existing nano-power DC/DC converter designed to operate down to 250 mV and 1 μW [67].
- A multi-sensor node with a low-power profile and adopting a standard wireless communication protocol for IoT – developed ad-hoc for this solution in collaboration with another design team –.
- The introduction of novel interface circuits between the power management sub-system and the node, which provide real-time feedback on the actual level of available power.

Power management aims at optimizing the extraction and the use of energy at different levels. At hardware level, the power converters performs MPPT and adapts its behavior to the effective level of available power. Additionally, a series of new dedicated circuits extracts information on the level of available power and provides it on a series of digital signals. At software level, the node can use the information provided by the power management sub-system in order to dynamically adapt its behavior, e.g. selecting the transmission data-rate, or selecting the most appropriate sleep or stand-by mode, etc.

The aim of this project is to efficiently combine these different elements by adding a power management section able to fruitfully exploit RF energy harvesting.

As mentioned above, in order to implement the necessary interactions between the power management subsection and the active sensor node, specific circuitry has been designed, for dynamically changing the behavior of the system according to different scenarios of available environmental energy. The peculiar achievement obtained through such active interaction is the possibility to modulate the transmission data-rate as a consequence of variations in the power

harvested, so that a higher amount of power causes an automatic increase in the data-rate and vice-versa, in such a way that the highest feasible data-rate is always obtained. Such an outcome may have a considerable rebound on those applications where high transmission rates are not strictly indispensable but can help in building a more extensive information database and therefore a more precise behavioral model for the monitored system.

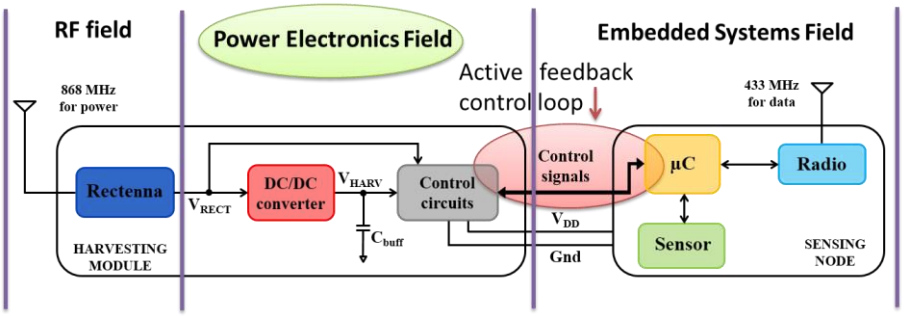

Fig. 41 Block diagram of the architecture of the proposed IoT node with feedback power management

In Fig. 41 the architecture of the case study is presented: two sub-systems are present, respectively an energy harvesting module and a sensing node. The interaction presented is obtained through specific control signals exchanged between the power module and the microcontroller, designed to provide information about the current state of the harvesting module, e.g., the voltage level and the amount of power and energy extracted. Based on this, the microcontroller can adapt its behavior in order to optimize the transmission rate.

In this specific case, two different operating frequencies are used for harvesting and communication channels (868 MHz and 433 MHz respectively). On the other hand, using two different antennas for harvesting and communication allows optimization of the harvesting antenna to best fit the DC/DC specifications, at the expense of a reasonable increase in area. Using a single antenna would be more complicated and would result in worse harvesting performance, mainly because of the losses introduced by the multiplexing circuitry. We remark that our solution is still general purpose, and then the adopted solution also allows to seamlessly replace the RF energy transducer with alternatives such as photovoltaic cells, thermoelectric generators, etc.

The introduction of smart voltage supervisors allows the harvesting module to adaptively configure the data transmission period of the node, and to accordingly change the sleep policy.

3.2.2 DC/DC conversion

The DC/DC converter used in the system features an ultra-low power buck-boost converter designed in a 0.32 µm CMOS microelectronic technology and previously developed within the research team [67].

The overall architecture can be divided into two main blocks:

- A start-up circuit, which allows for IC bootstrap with RF input sources typically providing low voltages.
- The main DC/DC converter which also provides a fractional open-circuit voltage (FOCV) MPPT algorithm in order to adapt to the best power transfer condition.

The IC dynamically decides whether to route power to the load or to a small self-supply capacitor C_{conv}: this achieves very fast activation times even in the presence of large buffer capacitors at the load output port. When C_{conv} is sufficiently charged, all power is routed to the load. Should C_{conv} get excessively discharged, all power is routed here to replenish it before the integrated circuits fails. A block diagram of the circuit module is reported in Fig. 42.

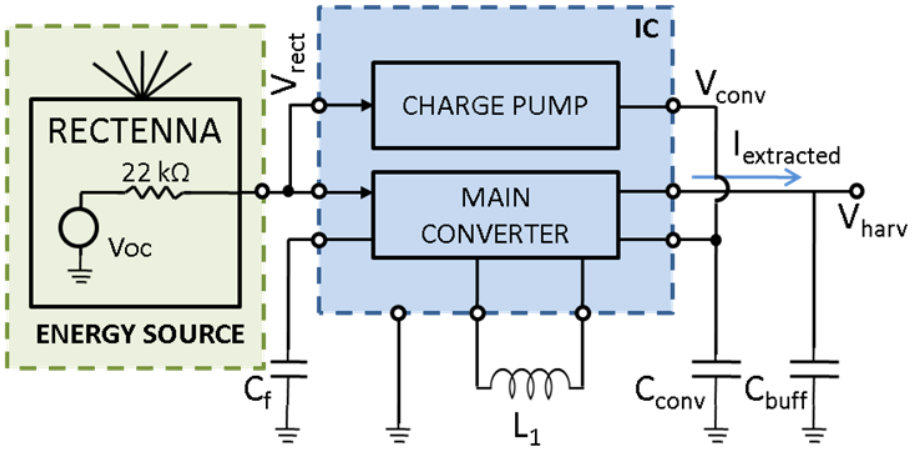

Fig. 42 Block diagram of the architecture of the DC/DC converter used in the power management module of proposed IoT node

The start-up module consists of a 16-stage charge pump implemented with low-threshold MOSFETs and driven by an internal oscillator. A minimum voltage of approximately 250 mV from V_{rect} is required to keep it operating. During the start-up phase, when the input voltage (i.e., the rectifying antenna output voltage) approaches 250 mV, the charge pump circuit starts working, and the output voltage on the self-supply capacitor C_{conv} is boosted. However,

internal devices are not fully switched on until the output voltage gets to 600 mV, so that the output charging rate is initially limited by the sub-threshold state of the system.

As soon as the generated voltage reaches 0.6 V the start-up circuit becomes fully operational and the charge pump improves its charging rate until the output exceeds 1.36 V, which is the minimum operating voltage of the main DC/DC converter. At this point the charge pump is disabled and power conversion occurs through the buck-boost DC/DC converter. Although the overall efficiency of the start-up stage settles between 5% and 15%, its sole purpose is to initially bootstrap the main DC/DC converter, so that its impact on operative efficiency can be considered negligible.

Once the 1.36 V threshold is reached, an in-rush current of about 11 µA is absorbed from the energy source by the module for a short time to complete bootstrapping the converter functionalities.

After this, the module can be sustained with an input power of just 935 nW showing a quiescent current of 121 nA.

The different functional modes are summarized with the corresponding supply voltages in Table 7. It is worth recalling that these values refer to the voltage on the self-supply capacitor V_{conv}. Another aspect worth consideration is the high output resistance of the rectifying antenna, which causes significant voltage drops on its output node as the current increases.

Table 7 Operative modes and related voltage ranges of the proposed DC/DC converter

<table>
<tr><td>V_{rect}</td><td>0V-0.250V</td><td colspan="3">0.250V-1.6V</td></tr>
<tr><td>V_{conv}</td><td></td><td>0V-0.600V</td><td>0.600V-1.36V</td><td>>1.36V</td></tr>
<tr><td rowspan="2">mode</td><td rowspan="2">Switched off</td><td rowspan="2">Charge pump (limited efficiency)</td><td rowspan="2">Charge pump (fully functional)</td><td>DC/DC converter fully functional
121nA quiescent current
935nW minimum input power</td></tr>
<tr><td>11 µA in-rush current from source needed to bootstrap converter</td></tr>
</table>

In order to extract the maximum power from the source, the converter adopts a FOCV MPPT technique (see section 1.5).

The input source is kept at 50% of the open-circuit voltage of the rectifying antenna, which actually represents the maximum power transfer condition for the system. The open-circuit voltage is sampled for 2 µs every 8 conversion cycles of the DC/DC converter. The buck-boost DC/DC converter operates in discontinuous current conduction mode (see section 1.5), and it is switched when the source voltage crosses the reference MPPT voltage. The overall efficiency is highly affected by source impedance and open-circuit voltage.

Thereafter, a full analysis was performed with the aim of obtaining an exhaustive characterization of the DC/DC converter in the specific running conditions of the system proposed. An equivalent model of the rectifying antenna was extracted from the static voltage-current characteristics and used for characterization. This consists in a DC voltage source (V_{OC}) with a 22 kΩ series resistance. The output voltage V_{harv} of the DC/DC is set at 2.3 V, which is the chosen maximum operating voltage of the sensing node. During operation, the variations on V_{harv} will be limited to a few hundred mV as the worst case. A 10 MΩ load was connected to V_{harv}. Results show that when the open-circuit voltage of the rectifying antenna V_{OC} ranges from 0.32 V to 1.4 V, the related efficiency grows from 35% to 73%, with a plateau reached early on at 0.8 V. The whole characterization is reported in Fig. 43, including a polynomial interpolation, and will be used to predict the available power in operating conditions different from the characterized data points.

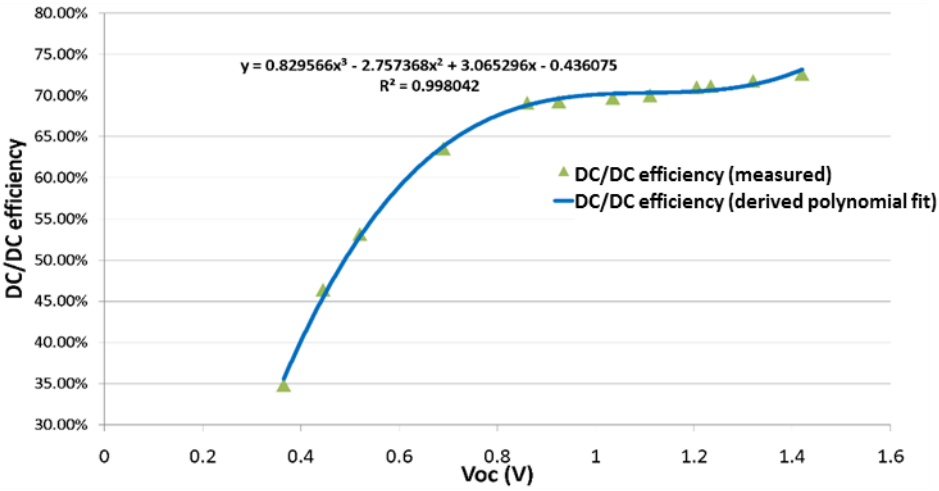

Fig. 43 Efficiency characterization of proposed DC/DC converter

3.2.3 The active node

The sensing and communication node, whose internal architecture is shown in Fig. 44, includes a temperature and relative humidity sensor, a low-power microcontroller and a sub-GHz radio device for data communication. STMicroelectronics HTS221 is an ultra-compact sensor based on a planar capacitance technology that integrates humidity and temperature sensing with a mixed signal ASIC to provide data measured through standard digital serial interfaces. The ultra-low power STMicroelectronics STM32L1 microcontroller, based on the ARM Cortex-M3 core, interfaces with the sensor for data acquisition and manages communication with the STMicroelectronics SPIRIT1 module, a low-power sub-GHz RF transceiver.

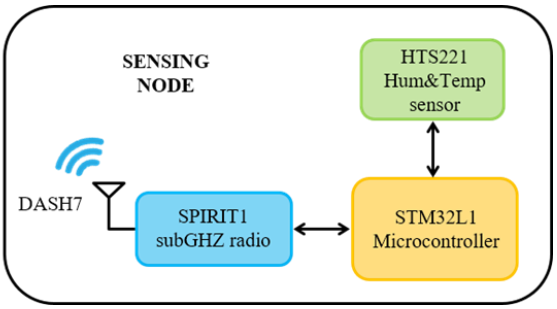

Fig. 44 Block diagram of the active module of the proposed IoT node

Wireless communication is based on DASH7 [80], an open source Wireless Sensor and Actuator Network (WSAN) protocol; the microcontroller implements OpenTag, a DASH7 protocol stack and a minimal Real-Time Operating System (RTOS) designed to be light and compact and targeted to run on resource-constrained microcontrollers.

The DASH7 network architecture has a star structure where all the nodes, which are typically low-power devices able to transmit and receive data, communicate only with a gateway that is never offline and connects the DASH7 network to other networks and to the web.

DASH7 supports two communication models: pull and push [81]. The pull model consists of a request-response mechanism initiated by the gateway; it uses an advertising protocol for rapid ad-hoc node synchronization before sending an addressed request to a node and waiting for the response [81]. The data transfer to the gateway initiated by the nodes is based on the push model (e.g., beaconing); this approach is implemented as an automated message or beacon that is sent at specific time intervals.

In the proposed solution, the beaconing approach is used to send the temperature and humidity data from the sensor node to the gateway; this method is the least power hungry and the node can send the message as soon as the harvesting module provides enough power to power-up the node or wake up it from a deep sleep state.

The node can be supplied with a voltage ranging from 1.8 V to 3.6 V, and it is programmed to perform two different stop policies: off-mode and standby-mode. The policy is selected by the harvesting module, as will be explained in the following section.

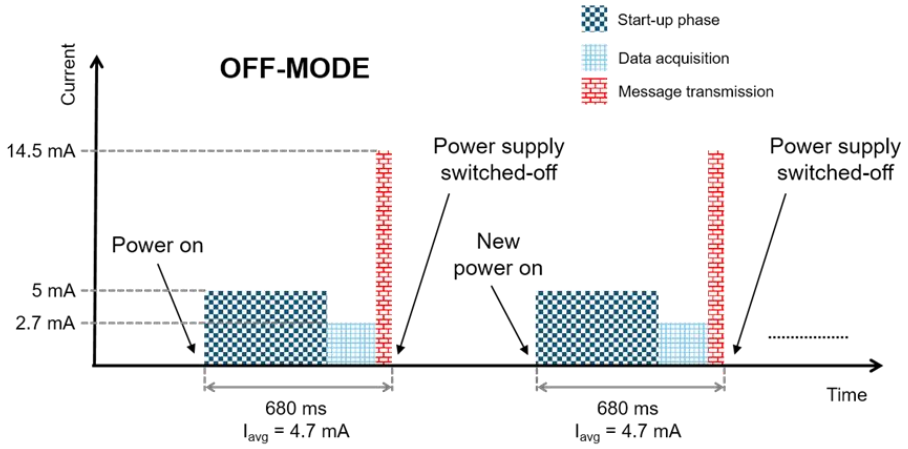

Fig. 45 Power consumption of proposed solution when operating in OFF-Mode

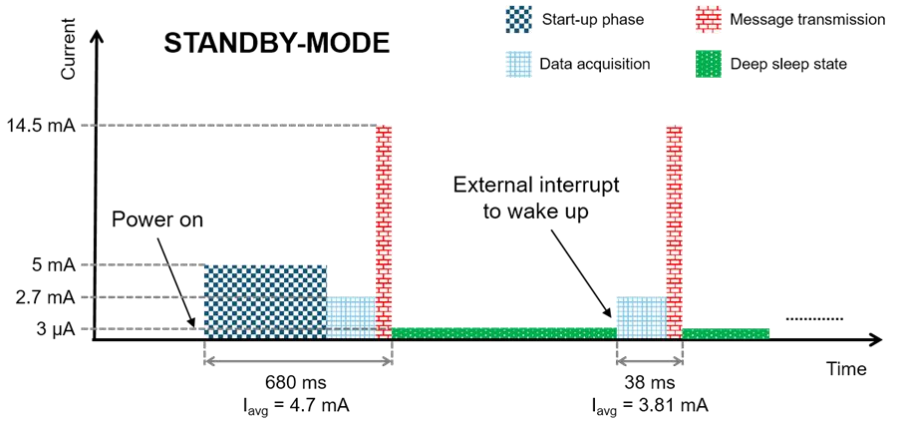

Fig. 46 Power consumption of proposed solution when operating in STANDBY-Mode

As it can be seen in Fig. 45 and Fig. 46, the two modes behave in the same way at power on, when, after the start-up phase, the node acquires data from the sensor and transmits them to the gateway. Afterwards, if off-mode is selected, the node generates a signal for the harvesting module to inform it that the power supply can be switched-off. When the power supply is once more provided, the node will perform a new start-up phase, data acquisition and message transmission.

This phase is associated with a significant energy overhead. Fig. 45 shows a schematic of the current consumption of the node and its behavior in off-mode indicating the average current in each of the three phases (start-up, data

acquisition and transmission); the overall activation phase lasts 680 ms and the average current consumption over this time is 4.7 mA at 1.9 V.

On the contrary, if the standby-mode is selected, after the first start-up phase and message transmission, the node informs the harvesting module that transmission is completed and that it is entering a deep sleep state in which its current consumption is 3 µA. The node then waits for an external interrupt, generated by the harvesting module, to wake up and perform a new data acquisition and message transmission. In standby-mode, therefore, the power supply is never switched-off, and the overhead consists in constant power consumption. The schematic of the node's current consumption and its behavior in standby-mode is shown in Fig. 46. In this configuration, with the exception of the first power-on in which the current consumption is the same as each activation in off-mode, the start-up phase does not have to be repeated for each activation phase because the power supply is never switched-off.

As can be seen in Fig. 46, in standby-mode each activation phase following the first one lasts 38 ms, and the average current consumption during this time is 3.81 mA at 1.9 V. In standby-mode, the charge consumption for each data acquisition and message transmission is much less than in off-mode, but a current of 3 µA has to be guaranteed to keep the node alive in the deep sleep state.

The selection between off-mode and standby-mode has a significant impact on the power budget. The off-mode is associated with a constant energy overhead, consisting in the energy consumed for starting the system. By contrast, the standby-mode is associated with a constant power overhead. Hence, which of the two modes costs less will depend on the frequency of activation. For frequent activation, the stand-by mode consumes less energy. Furthermore, the frequency of activations strictly depends on the harvested power.

Finally, Fig. 47 shows the realized PCB prototype of the sensor node connected to the harvesting module.

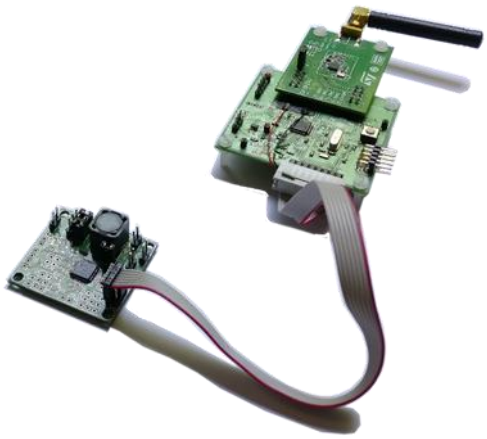

Fig. 47 PCB prototype of proposed IoT node with adaptive power management

3.2.4 Circuits for detecting the actual input power level

In this section, the proposed adaptive feature is described in detail, as well as the architectural choices and dimensioning of control circuits shown in Fig. 48. The interface between the harvesting module and the active node is implemented through four control signals connected to the microcontroller (*Policy*, *Reset_VDD*, *Start* and *Reset_Start*), besides the ground and positive supply (*VDD*).

The Policy signal selects one of the two stop policies of the active node (off-mode and standby-mode).

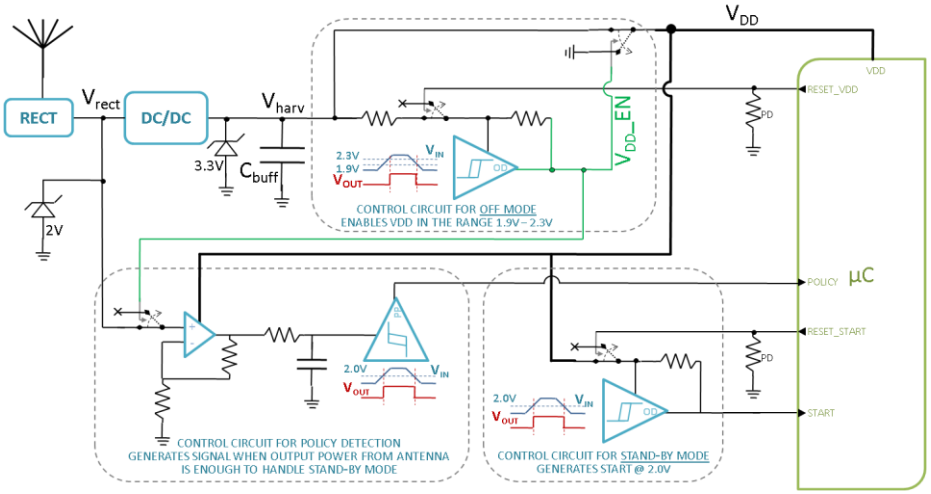

Fig. 48 Adaptive power management architecture of proposed IoT node

The first factor to be analyzed is the buffer capacitance C_{buff}, which plays the role of energy storage needed by the system to offset the total power request of the node during its active phase. Such requests are summarized in Table 8, which integrates the current absorbed by the node when switching into active mode from each of the other two modes.

Table 8 Power requests by proposed node in both OFF-Mode and STANDBY_Mode

Mode	Charge (µC)	Operating Voltage (V)
OFF	3196	2.3–1.9
STANDBY	145	~2

To have a voltage drop of about 0.4 V, the resulting C_{buff} must be at least

$$C_{buff} = \frac{Charge(OFF)}{\Delta V} = \frac{3196\,\mu C}{0.4\,V} = 7990\,\mu F \cong 8\,mF \quad (xxv)$$

where the voltage drop was chosen as a trade-off between system power consumption and wake-up time. In this instance, a lower bound of 1.9 V was chosen by considering a 100 mV margin to the minimum 1.8 V supply voltage required by the node to operate, while the upper bound was chosen by considering that a lower voltage implies lower power consumption, though at the same time it requires a larger buffer capacitance which causes a longer start-up time when the system has to be booted for the first time. Hence a maximum operating voltage of 2.3 V was chosen and, as a result, an 8 mF C_{buff} must be considered.

Three control circuits are necessary to generate the correct control signals for the micro-controller (Fig. 48).

- The first one is the **Control circuit for OFF mode**.
  This block has the task of monitoring the voltage across C_{buff} capacitance voltage and consequently to provide power supply to the sensing node only when voltage is in the acceptable range (1.9 V–2.3 V). In this way, the sensing module is only switched on when V_{DD} exceeds 2.3 V, i.e., when the buffer capacitance has sufficient energy to sustain at least one complete data transmission. Likewise, power supply is taken off as soon as V_{DD} drops below 1.9 V, as the sensing module cannot work at lower voltages.
  During off-mode, a reset signal (*Reset_VDD*) must be issued by the microcontroller at the end of each transmission stage, so that power supply is simultaneously turned off. This behavior ensures that the next transmission will only be held when the buffer capacitance is fully recharged, i.e., when it reaches 2.3 V again. A NCP303 low-power voltage supervisor was used to implement the block, along with two AS11P2 analog switches and two resistors in order to obtain the desired hysteresis, respectively 2.4 MΩ and 500 kΩ. The total quiescent current of the block is 500 nA, mostly due to the NCP303 supervisor.

- The second one is the **Control circuit for STANDBY mode**.
  This block has the task of monitoring the capacitance voltage and consequently providing the start signal only when voltage is above 2.0 V. During standby-mode, the sensing node is always powered, and subsequent transmissions are regulated by the start signal, so that it must only be issued when the buffer capacitance is storing enough energy to sustain transmission. Actually, the expected voltage drop due to a single transmission in standby-node is a mere 18 mV as explained in following equation

$$\Delta V(STANDBY) = \frac{Charge(STANDBY)}{C_{buff}} = \frac{145\ \mu C}{7990\ \mu F} = 18\ mV \qquad (xxvi)$$

so a threshold voltage of 1.9 V + ΔV = 1.918 V could be enough to sustain standby-mode, but a safer margin of 2.0 V − 1.9 V = 100 mV was chosen for this condition.
A reset signal (*Reset_Start*) from the microcontroller is also requested at the end of each transmission in order to force the start signal to a low level, even if the related capacitance voltage drop has not been sufficient to trigger the voltage supervisor. This happens because the microcontroller is sensitive to a positive start signal edge, so that a low-to-high transaction is always required to awaken the sensing node. An NCP303 low-power voltage supervisor was used to implement the block, along with one AS11P2 analog switch and a pull-up resistor of 2.4 MΩ. The total quiescent current of the block is 400 nA, mostly due to the NCP303 supervisor.

- The third one is the **Control circuit for policy detection**.
  This block has the task of correctly identifying the available power and consequently evaluate if it is either above or below a predefined threshold, and communicating this to the microcontroller through the policy signal. As a matter of fact, it exists a precise value of extracted power below which it is more efficient to completely switch-off the micro between wake-ups, and above which it is more efficient to use a stand-by state.
  Since the correct relationship between the power received by the rectifying antenna and the power extracted by the DC/DC has been fully investigated, the least power-consuming solution to evaluate available power is to simply monitor the average voltage at the rectifying antenna output. This value is solely related to the extracted current through the efficiencies of the interposed stages, and it can be fairly used to estimate the usable power.
  The interesting point is then to compute the exact threshold value to use for discerning between the two sleep modes.

The ability to dynamically select whether to operate in off-mode or standby-mode is a crucial aspect of the solution presented, as it enables the system to fully exploit the available environmental energy under any circumstance without human intervention. In both cases the minimum transmission period is obtained, as the microcontroller is either supplied (off-mode) or awoken (standby-mode) as soon as the buffer capacitance has recovered the energy lost, but depending on the variable amount of extracted energy, one solution can be less advantageous than the other, if not altogether unfeasible. Transmission Period (TP) is defined as the time interval between two consecutive transmissions and can be calculated as:

(xxvii)
$$TP = \frac{Q_{needed}}{(I_{extracted} - Iq_{harv} - Iq_{node})}$$

where Q_{needed} is the charge lost during each transmission, $I_{extracted}$ is the current provided by the DC/DC converter, Iq_{harv} is the quiescent current of the harvesting module that is directly supplied by V_{HARV} while Iq_{node} is the quiescent current of the rest of the system supplied by V_{DD}. These values differ between the two operative modes, and are summarized in Table 9.

Table 9 Recap of required charge and quiescent currents of proposed node in OFF-Mode and STANDBY-Mode

	Q_{needed} (µC)	I_{qharv}(µA)	I_{qnode}(µA)		
		Control circuit OFF-mode	Control circuit STANDBY-mode	Control circuit Policy detection	Sensor node
OFF	**3196**	**0.5**	switched-off	switched-off	switched-off
			switched-off		
		0.5			
STANDBY	**145**	**0.5**	0.4	0.6	3
			4		
		4.5			

The most significant difference is that in off-mode the charge needed is significantly higher than in standby-mode, but the total quiescent current is only 500 nA, since all the other modules are switched off during recharge periods. As a consequence, in off-mode nearly all the current from the power converter can be used to recharge the buffer capacitance.

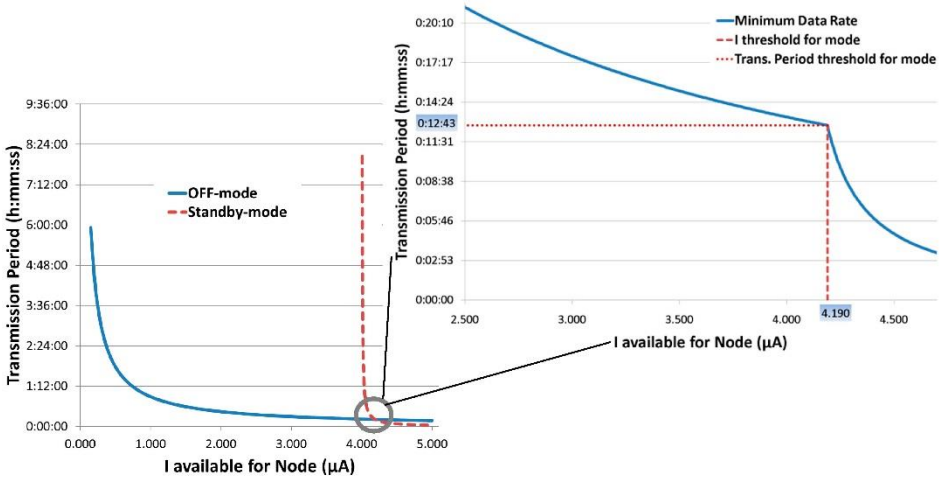

Fig. 49 Detailed graph of transmission data rates versus extracted currents of proposed node in OFF-Mode (blue) and STANDBY-Mode (red)

Thus, this last mode proves more suitable when the extracted current is relatively low, whereas the standby-mode becomes more cost effective at higher

extracted currents, when its lower value of activation charge becomes predominant. A detailed graph of transmission data rates versus extracted currents is shown in Fig. 49, analytically obtained through equation (xxvii).

The available current is defined as the effective current that can be used by the active part of the system or, in other words, the whole extracted current subtracted by Iq_{harv}, which is always drawn from the DC/DC converter ($I_{available} = I_{extracted} - Iq_{harv}$). As shown in the graphs, as the available current rises above 4.190 µA, standby-mode becomes the best choice in terms of minimum data rates, and the related threshold value is about 13 min.

With this assumption, the **Control circuit for policy detection** has the task of correctly identifying whether the current available is either above or below the threshold value of 4.190 µA by monitoring the average voltage available at the rectifying antenna output, and experimental results show that a value ≥585 mV for V_{RECT} is required to obtain such value.

Since the low-power voltage supervisor NCP303 has a threshold value of 2 V, a dedicated low-power voltage amplifier with a 2 V / 0.585 V = 3.42 gain was added, composed of an LPV521 op-amp and two resistors of 20 MΩ and 4 MΩ. Moreover, a simple RC filter was inserted with τ = 100 ms, in order to reject the periodic fluctuations caused by the FOCV algorithm of the DC/DC converter, which actually disconnect the rectifying antenna for about 4 µs every 8 extraction cycles. The overall quiescent current of the block is 600 nA, as already reported in Table 9.

3.2.5 Results

Operative ranges

The available energy is mainly affected by two factors: the transmission power and the distance between transmission and receiving antennas. For the former, two different transmitter powers were selected to be compliant with the RFID standard [82], respectively 0.5 W ERP and 2.0 W ERP.

A specific graph reporting the available power versus node distance is presented in Fig. 50. The available power is the total power extracted from the DC/DC converter. It also accounts for losses on the capacitor and on instrumentation.

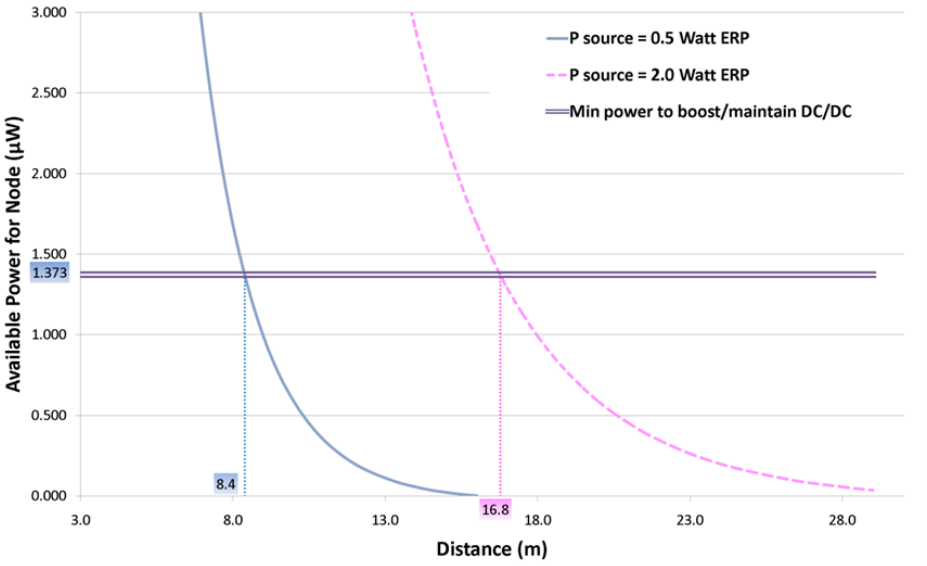

Fig. 50 Available power versus node distance with 0.5 W ERP transmitted (blue) and 2.0 W ERP transmitted (pink) – analytical model

The graph shows two different curves for 0.5 W ERP and 2.0 W ERP, which intersect at threshold values. The value of 1.373 µW is the threshold value at which the system presented can be considered self-sustained, as it can successfully supply the minimum actual load of the system, which is the control circuit for off-mode described in Fig. 48.

The far from inconsiderable result obtained is that with a transmitted power of just 0.5 W ERP the system presented can start at 8.4 m, while with 2.0 W ERP the distance can rise up to 16.8 m.

Minimum distance of 8.4 m with 0.5 W ERP transmitted power was verified through a dedicated experiment.

When the system starts from a completely discharged situation, an initial startup time is required to charge the 8-mF buffer capacitance whose value depends on the harvested current. Once booted, the node is automatically configured to operate in the best operating mode, providing the shortest transmission period. A detailed graph of startup and transmission times is reported in Fig. 51.

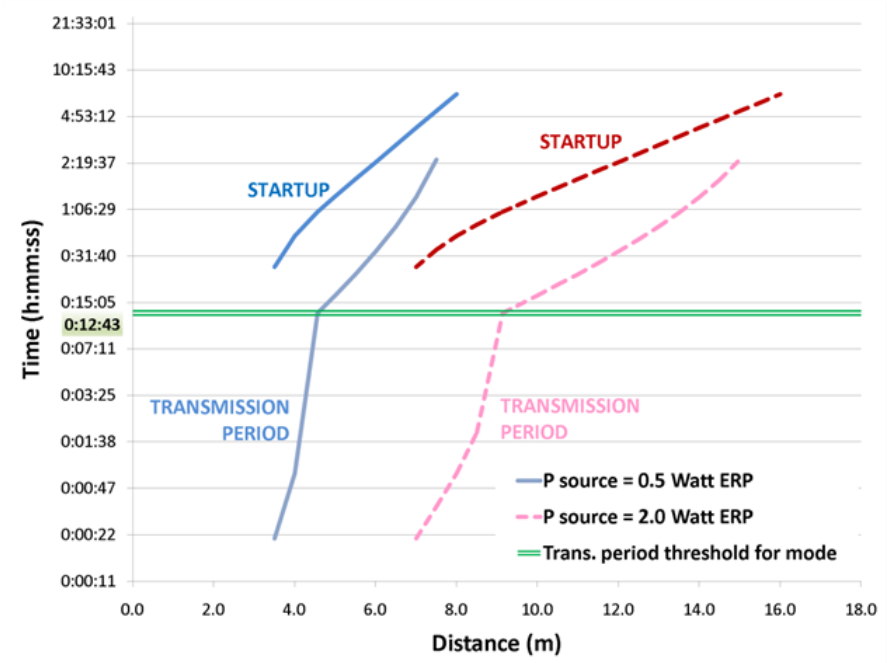

Fig. 51 Detailed graph of startup and transmission times) – analytical model

Analytic results show that the minimum transmission period is about 21 s, corresponding to an extracted power of 26.5 µW obtained with an antenna open circuit voltage of 1.650 V. Similarly, the operating mode is switched from off-mode to standby-mode according to Figure 13 when the extracted power is 11.011 µW (open circuit voltage 1.170 V), with a period of 12′43″.

Data rates

Fig. 52 shows the relationship between node distance, power extracted from DC/DC and obtainable transmission periods. Starting from distance (bottom horizontal axis), the blue-dotted line represents extracted power when the source is 0.5 W ERP, while the pink-dotted line is extracted power when the source is 2.0 W ERP. Once the available power is known, the obtainable period can be found on the dotted green line, whose values are reported along the top horizontal axis. Moreover, three operative regions of extracted power are identifiable: a turn off region where the node cannot be switched on, an off-mode operating region and a standby-mode one. Finally, on distance axis two values are underlined for both 0.5 W ERP and 2.0 W ERP transmitted. The first one matches the intersection between the switched-off region and the off-mode region, which also represents the maximum operative distance. The second one

matches the intersection between off-mode and stanby-mode, and it represents the distance at which it is convenient to switch between the two modes.

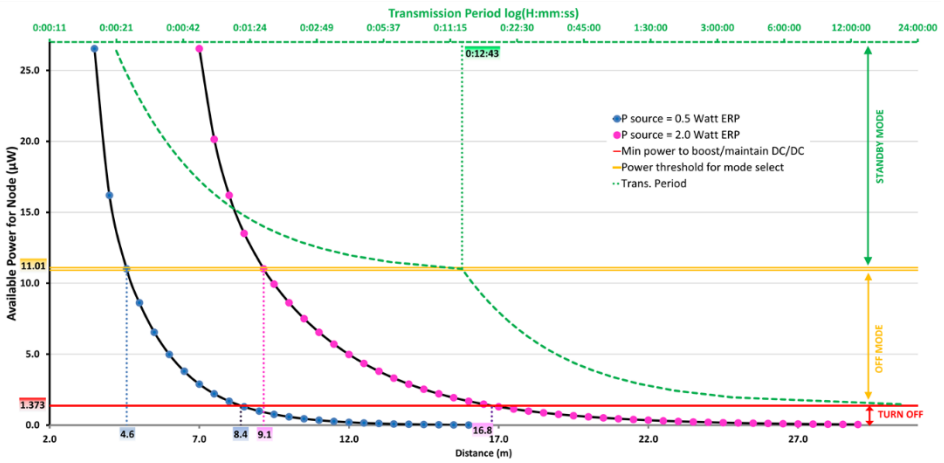

Fig. 52 Relationship between distance, power extracted and obtainable data rates) – analytical model

Table 10 summarizes the threshold values shown in Fig. 52.

Table 10 Recap of the maximum operative distances related to available input power / voltage and associated with best obtainable data rate

	Antenna V_{oc} (V)	**Extracted Power (µW)**	**Transmission Period**	**Distance (m)**	
				0.5 W ERP	**2.0 W ERP**
Switch-on	0.490	1.373	→ ∞	8.4	16.8
Policy threshold	1.170	11.011	0:12:43	4.6	9.1
Min. trans period	1.650	26.531	0:00:21	3.5	7.0

Communication

The effective operation of the DASH7 node was tested, in terms of power consumption, transmission capability and adaptive data rate. Fig. 53 (a) shows waveforms of signals related to off-mode operation. Supply V_{DD} decreases as expected from 2.3 V to 1.9 V over a time interval of about 680 ms, which correspond to a single transmission. With reference to Fig. 45, this time accounts for the microcontroller start-up phase, the data acquisition and finally data transmission. The reset signal (*Reset_VDD*) is activated at the end of each transmission. Similarly, in Fig. 53 (b) the control signals for standby-mode are shown. Voltage drop is about 20 mV as expected, while in this mode the *Reset_Start* signal is activated instead of *Reset_VDD* at the end of transmission.

Fig. 53 Tested waveform of respectively: storage voltage (orange), enable/start signal (green), reset signal (purple) and received data trigger (pink) during normal operation, for OFF-Mode (a) and STANDBY-Mode (b)

Transmitted data are then received by a dedicated gateway, which displays data directly onto a PC terminal. Fig. 54 shows the received data bytes with different sensor values.

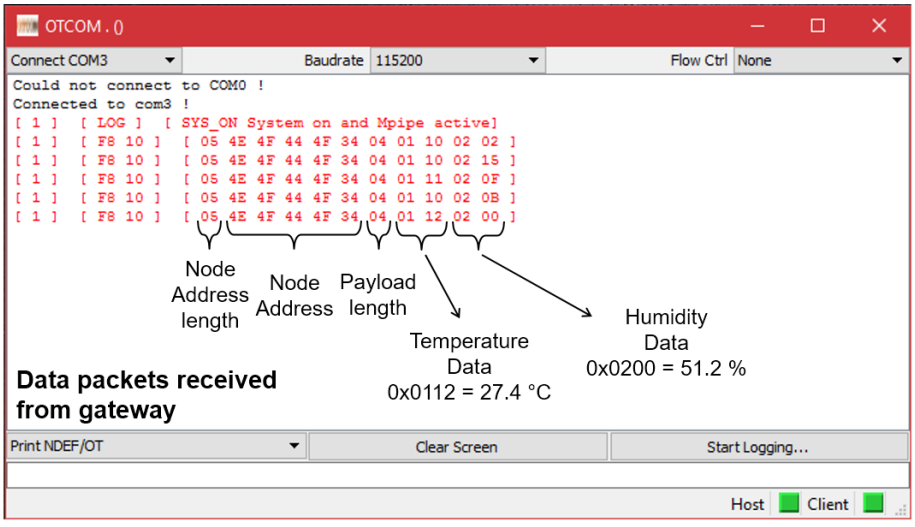

Fig. 54 Screenshot of data acquisition graphical interface with received data

Adaptive power management

Finally, power optimization circuits for policy selection were tested. In Fig. 55 control signals behavior can be observed with respect to DC/DC output voltage V_{HARV}. Considering signals reported in Fig. 48, V_{HARV} is initially below the activation threshold of 2.3 V, so all other signals are disabled. As soon as

V_{HARV} exceeds 2.3 V, the node can be enabled so V_{DD} (= V_{HARV}) is provided, and other supervisors are supplied through V_{DD} too. Start signal is high, as V_{HARV} is above 2.0 V, while policy is also high as V_{OC} is kept above 1.170 V in this stage (see Table 10). As RF source is switched off, the buffer voltage V_{HARV} begins to decrease, and policy is immediately forced low. Then start signal goes low when V_{HARV} falls below 2.0 V as expected, while supply voltage V_{DD} is disconnected when V_{HARV} goes below 1.9 V.

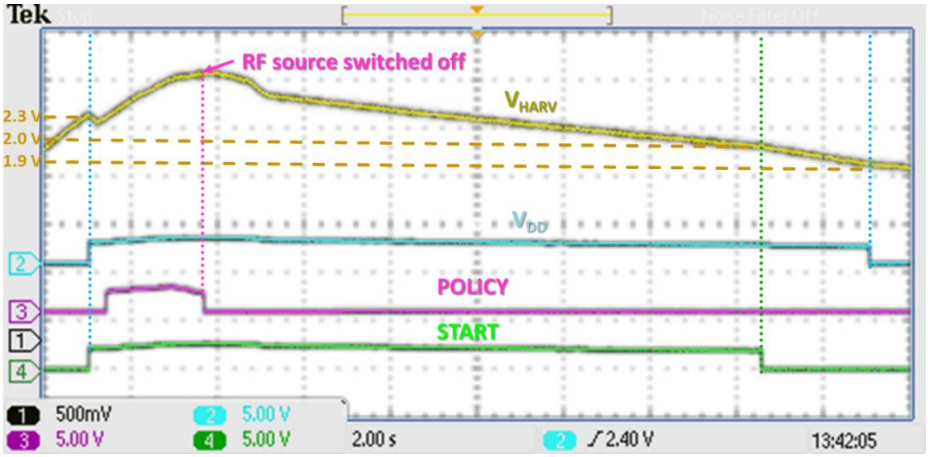

Fig. 55 Tested waveform of respectively: DC/DC output voltage on storage element (yellow), node voltage supply (blue), policy control signal (purple), start control signal (green) during normal operation in the case when RF source initially provides sufficient energy to operate in STANDBY-Mode and then is switched off. Policy is then correctly adapted through control signal

The proposed solution is also described in detail in [83].

3.3 Discussion

Main purpose of this work regards the study and development of the power management unit, with the introduction of the feedback architecture and the deployment of an advanced prototype of DC/DC converter. Deep analysis of power consumption profiles of the node was accomplished in order to find the best solution for sleep policy. The choice and dimensioning of discrete components was carefully implemented too, altogether in order to minimize the dissipation of such elements. As a matter of fact primary aim was to reduce power consumption of the node as much as possible to obtain the higher possible operative distance along with the higher possible transmission rate for any distance.

Chapter 4

Robustness and durability aspects in maximum power point tracking algorithms

In many low-power energy harvesting transducers such as rectennas, photovoltaic cells (PV) or thermoelectric generators (TEG), with power available in the order of up to hundreds of microwatts, load matching is generally required to achieve maximum power transfer thanks to Maximum Power Point Tracking (MPPT) algorithms.

Many MPPT techniques have been proposed in literature [84]. In high power systems, such as outdoor PV panels, where DC/DC converter power consumption contribution is negligible, closed looped and computational intensive MPPT algorithms are used because of the significantly lower impact on extracted power. Differently, in low-power applications, such as those based on indoor PV panels or thermoelectric modules, DC/DC converters with open-loop MPPT techniques such as Fractional Open-Circuit Voltage (FOCV) are usually preferred [85] as a generally accepted trade-off. The FOCV algorithm assumes a simplified linear dependence between the voltage corresponding to the Maximum Power Point (MPP) and the open-circuit voltage (V_{OC}) of the transducer. Then, V_{OC} is periodically sampled to track variations in available power, and a constant scaling factor (k) is programmed once and for all at the DC/DC converter input, depending on the application. An incorrect choice of the parameter k results in a loss of efficiency of the harvesting system, especially since its value is actually slightly dependent on the source intensity [86].

For what concerns robustness and durability aspects, the ability to keep the input source to a predefined maximum power point may decay over time due to malfunctions in the DC/DC converter electronics or natural drifts of passive elements which are usually adopted in order to set the precise ratio with respect to the open circuit voltage. Therefore it would be of great interest to have an efficient method to periodically check the real maximum power point of the panel and compare it with the actual working point of the converter. Moreover, it would be useful to have a non-invasive method which could be applied to different kind of DC/DC converter without the need to redesign the converter itself. By monitoring the difference between the target maximum power point and the actual one it is possible to estimate the state of health of the MPPT circuit and eventually correct or compensate possible malfunctions.

4.1 Studied solution: A novel approach to MPPT maintenance in photo-voltaic applications

The proposed system relies on an algorithm to reconstruct the complete PV cell Power versus Voltage (P-V) characteristic without requiring the value of panel short-circuit current, as in [87, 88], but only the values of voltages and currents at the transducer output during normal operation of a system implementing the FOCV-MPPT technique. In this way, verifying MPPT efficiency does not require dedicated power-consuming circuitry to be added to the original harvesting system, nor power loss due to short-circuit current measurement, but only the possibility of inserting an external measuring unit between the panel and the DC/DC converter. During normal operation the transducer is directly connected at the DC/DC converter input, while during the debug phase the external measuring board is connected in series between the transducers and the DC/DC converter input and allows one to measure voltage and current (V, I) values minimizing voltage drop (Fig. 56).

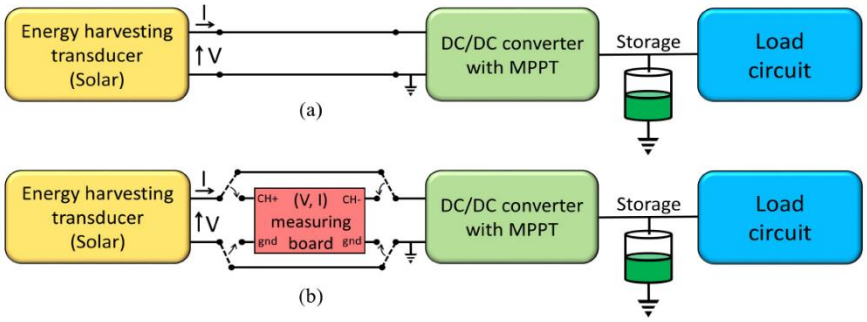

Fig. 56 Deployment scenario of proposed method for monitoring FOCV MPPT algorithm efficiency over time: (a) standard architecture, (b) enhanced architecture with measuring system for efficiency tracking

The proposed method aims at verifying the efficiency of low-power harvesting systems based on PV cells for indoor applications; the efficiency is verified only during the installation or debugging phases and not run-time as proposed in other works, for example in [89]. The method is applied to indoor PV harvesting systems in which the light intensity levels are usually rated in terms of photometric units (lx); as an example, in the case of standard global AM 1.5 spectrum, an illuminance of 500 lx corresponds to an irradiance of 500 µW/cm2 [90]. The indoor illumination levels range from 100 lx to 1000 lx: a range of 100-300 lx is typical of home lighting, the range 400-800 lx is typical of office and meeting rooms, while near the window the illuminance level will reach 1000 lx. Moreover, in indoor environments the temperature excursions are modest so the temperature dependence of the PV cell characteristic can be ignored.

Differently from other already described harvesting sources, like RF or TEGs, which have an almost resistive characteristic, in photovoltaic cells the relationship between voltage and current is not linear, and corresponding P-V curve is shown in Fig. 57 for a fixed illuminance level.

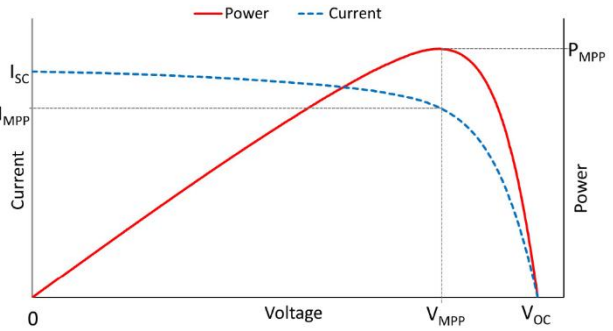

Fig. 57 Typical photovoltaic cell P-V and I-V curves. Voltage V_{MPP} and current I_{MPP}

As a consequence, established that in FVOC techniques the operating voltage V_M which guarantee the maximum power transfer is found as a fraction k of the open circuit voltage V_{OC} following:

(xxviii) $$V_M = k \cdot V_{OC}$$

then the value of the multiplying factor k must be chosen according to the physical characteristics of the transducers. If for resistive transducer (RF, TEG) typical value is ~ 0.5 [91], for photovoltaic cells more realistic values are ~ 0.7-0.8 [85, 86] and, more important, actual value differs between panels and may also vary accordingly to irradiance level. Hence, particular techniques are required to obtain a correct value of k in photovoltaic applications. By way of example, typical waveforms associated to a FOCV algorithm are presented in Fig. 58.

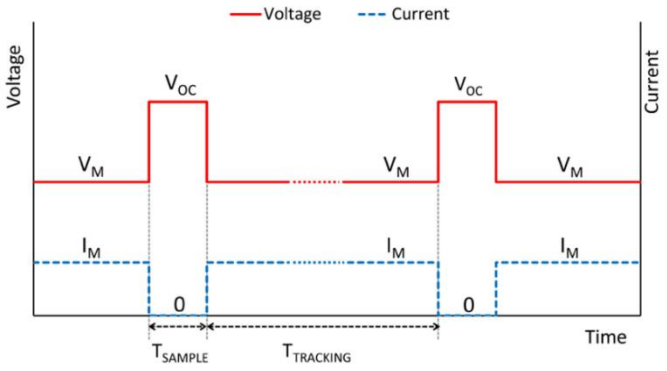

Fig. 58 Sketch, not in scale, of voltage (top) and current (bottom) waveforms at the transducer output of the harvesting system based on the FOCV-MPPT technique

4.1.1 System Implementation

In order to design a system based on indoor PV cells and an FOCV-MPPT technique, a developer needs to set the k factor according to the panel characteristics. Two voltage values are needed: the value in open-circuit (V_{OC}) and in maximum power transfer (V_{MPP}) operating points at the same illuminance level. If not available from the transducer datasheet, V_{OC} can easily be measured by disconnecting the panel, while V_{MPP} can only be determined by sampling the full P-V (or I-V) characteristic, as shown in Fig. 57, changing the panel load until the maximum output power is obtained. Given these measurements, $k = V_{MPP} / V_{OC}$ can be set in the DC/DC converter, and in common implementations this value is considered accurate for all illuminance values. However, the k factor is a function of panel fabrication process, illuminance and temperature values in operating conditions. As discussed in section 4.1, in indoor applications, the temperature dependence can be ignored since the temperature variations are limited, and panel temperature can be considered always equal to ambient temperature in first approximation. On the contrary, illuminance levels in indoor environments range from 100 lx to 1000 lx. In order to define the value of the k factor optimizing power transfer of the specific panel under analysis, complete PV curve characterization would therefore be required for a number of illuminance levels, but PV panel manufacturers often do not include these characterizations in datasheets and specific equipment is required for full panel characterization on site.

To overcome the problem, analytic-based MPPT techniques are proposed: from experimental measurement of V_{OC} and short-circuit current (I_{SC}), techniques for analytical calculation of the *MPP* of a photovoltaic array are suggested in [87, 88].

Implementing these MPPT techniques in a DC/DC converter still requires integration of additional power-consuming circuitry to measure I_{SC} and to compute V_{MPP}, which is not well suited to low-power applications. Unlike the previous technique, the proposed method allows reconstruction of the P-V curve without requiring measurement of I_{SC}, but only the values (V_M, I_M) and (V_{OC}, 0) corresponding to normal FOCV-MPPT operation, as sketched in Fig. 58. The only additions to the original harvesting system are a few passive components (switch and connector) to allow insertion of a measuring board between the transducer and the DC/DC converter (Fig. 56 (a)) whenever the efficiency of the power transfer has to be monitored. The acquired data are sent to a PC where the reconstruction algorithm is executed.

Comparison between the working point (V_M, I_M) and the optimal one (V_{MPP}, I_{MPP}) corresponding to maximum power P_{MPP} calculated from the reconstructed characteristic gives an estimate of the efficiency of the MPPT algorithm and allows one to modify the value of the multiplying k factor accordingly.

4.1.2 Photovoltaic cell model: interpolation problem

The conventionally adopted PV cell model is described in [92] and refers to an amorphous panel, as shown in Fig. 59

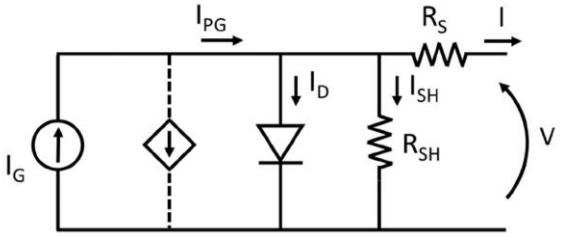

Fig. 59 Amorphous PV panel equivalent model

which leads to the following equation:

(xxix) $$I = I_{PG} - I_D - I_{SH} = I_G\left(1 - \frac{b_1}{b_2 - V - R_S I}\right) - I_0\left(e^{\frac{V+R_S I}{n_s a V_T}} - 1\right) - \frac{V + R_S I}{R_{SH}}$$

I_G is the photo-generated current proportional to light irradiation. In crystalline cells this term is independent of the operating point. In amorphous cells, such as those used in the system analyzed, there is an additional recombination current loss proportional to I_G and dependent on the operating point, modeled with the corrective terms (b_1, b_2) on I_G: the effective photo-generated current is therefore $I_{PG} < I_G$. The PV panel, being composed of a series of p-n junctions, has a dark current component I_D which must be subtracted from I_{PG}. In the I_D model, I_0 is the diodes dark saturation current, n_s the number of cells in series, $V_T = k \cdot T/q$ the thermal voltage and a (a real number between 1 and 2) the diode non-ideality factor related to additional recombination effects. The illuminance is assumed uniform on all the n_s cells. Along with these core parameters, additional cell losses are modeled with resistors: R_{SH} is the shunt resistance related to manufacturing defect losses in the device; R_S is the series resistance related to ohmic paths in the junction and metal contacts.

To reconstruct the I-V curve, the value of the parameters in (xxix) are required. It is worth noting that at first approximation the unknown parameters can be divided in two groups:

- a, R_{SH}, b_1, b_2 have a very limited dependency on the degree of illuminance and therefore can be calculated off-line just once, using dedicated algorithms potentially exploiting advanced machine learning algorithms.
- I_G, R_S, I_0 have a deep correlation with illuminance and must be calculated on-the-fly.

Hence, from a mathematical perspective there it should be necessary to know 3 working points in order to solve this 2-unknowns problem.

The main panel characteristics provided by PV cell manufacturers are (V, I) values for one or a few illuminance levels at three operating points: open-circuit (V_{OC}, 0), maximum power (V_{MPP}, I_{MPP}) and short-circuit (0, I_{SC}). It has been shown [10] that it is possible to interpolate a complete I-V curve at a fixed illuminance from these three operating points. Moreover, other studies [93] show how it is possible to reconstruct the whole I-V characteristic starting from just two points, maximum power (V_{MPP}, I_{MPP}) and short-circuit (0, I_{SC}), thanks to some weighted approximations. Unfortunately short circuit I_{SC} value is not easily obtained in common systems though, unless you consider to radically change the architecture of the DC/DC converter. Conversely, it is very easy to know the open-circuit voltage V_{OC}, since it is periodically estimated within the implemented FOCV MPPT algorithm, without changing DC/DC behavior or adding supplementary circuitry. Hence it would be of great interest to find a methodology to interpolate the I-V curve starting from V_{OC}.

As a consequence, an original algorithm has been studied able to reconstruct the I-V (P-V) curve from the only two operating points: the first being the operative point of the DC/DC converter, potentially close to MPP (V_M, I_M), and the open-circuit point (V_{OC}, 0).

4.1.3 Reconstruction algorithm

First of all a method to estimate the values of constant parameters a, R_{SH}, b_1, b_2 is proposed.

The ***characterization algorithm*** was developed in MATLAB© and aims to find the values of constant parameters which best fit equation (xxix) with a set of experimental I-V panel curves. An offline full P-V panel characterization using ad-hoc testing devices or available through datasheets provided by manufacturers is therefore still required in the proposed technique as in common implementation of FOCV-MPPT systems, but only for a subset of illuminance curves: these parameters will then be used to reconstruct curves for all illuminance levels.

The resulting quadruple of parameter is the one that minimizes the error function:

$$e = \sqrt{\sum_{V_i} \sum_{L_j} \left\| I_{m,ij} - I_{c,ij} \right\|^2_{V_i,L_j}} \qquad (xxx)$$

defined as the root mean square of the distance between all measured points ($I_{m,ij}$) at different voltage points (V_i) and illuminance levels (L_j) as compared to calculated ones ($I_{c,ij}$) using the *reconstruction algorithm* described below in this section.

A minimum for that function is sought through the search method [94] offered in MATLAB©, a direct search method that does not use numerical or analytic gradients, while initial guess for parameters a, R_{SH}, b_1, b_2 was taken from literature [92] (b_1 = 0.1 V, b_2 = 0.9 V, whereas a = 1.5 and R_{SH} = 2.5 MΩ).

It is worth noting that the obtained values of a, R_{SH}, b_1, b_2, are the result of the optimization phase: they act therefore as fitting parameters and may assume values that are not physically acceptable, such as in the case of the parameter a which can in some cases be found slightly greater than 2.

Starting from those constant parameters a ***reconstruction algorithm*** is developed.

To solve the system for I_G, I_0 and R_s three equations are needed. The first two equations are obtained by substituting in (xxix) the values (V_M, I_M) and (V_{OC}, 0) measured in the two operating phases (DC/DC conversion and open-circuit measuring) of a system implementing an FOCV-MPPT technique. To find the third equation an approximation must be introduced.

It can be shown that, in a short-circuit (SC) case, the derivative of (xxix) can be approximated as

(xxxi)
$$\left.\frac{dI}{dV}\right|_{SC} \approx -\frac{1}{R_{SH}}$$

which is derived in [95] and is based on the assumption that $R_S \cdot I_{SC} << a \cdot n_S \cdot V_T$. This equation cannot be used in the proposed method because I_{SC} is not known from measurement; the third equation is therefore derived following an approach similar to that in [95] but analyzing the derivative of (xxix) at the open-circuit (OC) point. Even if (xxix) is a nonlinear implicit function, its derivative can be calculated analytically using implicit partial derivatives. Calculation of the derivative in (V_{OC}, 0) leads to:

(xxxii)
$$\left.\frac{dI}{dV}\right|_{OC} = -\frac{A}{1+R_S A};\quad A = \frac{I_0}{a n_S V_T} e^{\frac{V_{OC}}{a n_S V_T}} + \frac{1}{R_{SH}} + I_G \frac{b_1}{(b_2 - V_{OC})^2}$$

Typical values for the first term of A are in the order of 10^{-4} S. The third term of A can be ignored because it relates to a corrective term of I_G and is an order of magnitude smaller than other terms (a typical value is in the order of 10^{-7} S). The second term of A can also be ignored in all cases where shunt losses are small (for R_{SH} > 10 KΩ, it is < 10^{-5} S).

A can therefore be approximated with its dominant first term. Series resistance R_S, as a parasitic parameter, is usually less than 100 Ω and this ensures that $R_S \cdot A << 1$ (10^{-2}), leading to:

(xxxiii)
$$\left.\frac{dI}{dV}\right|_{OC} \approx -\frac{I_0}{a n_S V_T} e^{\frac{V_{OC}}{a n_S V_T}}$$

Now we can equate (xxxiii) to (xxxii), obtaining the third system equation:

$$\frac{A}{1+R_S A} = \frac{I_0}{a n_S V_T} e^{\frac{V_{OC}}{a n_S V_T}} \qquad (xxxiv)$$

From a mathematical point of view, this means that since we know from the physics of photovoltaic devices that some terms of (xxxii) are negligible, than we can in first approximation force those terms to be zero, by equalizing the original and the reduced form, so obtaining an additional equation.

The final equation system to obtain I_G, I_0 and R_s is therefore:

$$\begin{cases} I_M = f(V_M) \\ 0 = f(V_{OC}) \\ \text{(xxxiv)} \end{cases} \qquad (xxxv)$$

Solving (xxxv) for R_S leads to an implicit nonlinear equation that cannot be solved analytically. However, this equation can be solved by numerical methods (its derivative can be calculated analytically, again with partial implicit derivatives, so Newton-Raphson [96] may be used). The R_S value obtained can be substituted in the first two equations to solve for I_0, I_G.

Once all PV panel parameters are known for a given illuminance value, the I-V curve can be calculated from (xxix). Given that this equation is implicit and nonlinear, it must be solved numerically (again by Newton-Raphson [96]) for every point needed. From the calculated I-V curve, it is possible to obtain the P-V curve and MPP, which can be used to verify the DC/DC converter MPPT efficiency.

From a computational point of view, the Newton-Raphson method time complexity of calculating a root of a function $f(x)$ with n-digit precision, provided that a good initial approximation is known, is $O(\log_2(n) \cdot F(n))$ where $F(n)$ is the cost of calculating $f(x)/f'(x)$, with n-digit precision. In this case, $F(n)$ can be roughly estimated to take less than 100 sums and multiplications, so that this method turns out to be very low demanding in terms of computational time. Moreover, although this algorithm is intended to be an on-line method, its refresh rate can be set in the range of hertzes or millihertzes, rather than megahertzes, since it is related to changes in the environmental illuminance. Therefore no particular constraints have to be matched for what concerns computational time.

4.2 Results and discussion

The implemented prototype is shown in Fig. 60, including a sensor node with an indoor photovoltaic harvesting module and a measuring board connected in series with the DC/DC converter as depicted in Fig. 56 (b).

Fig. 60 PCB prototype of proposed solution of a novel architecture to reconstruct I-V photovoltaic panel characteristic on-the-fly in a solar harvesting scenario

The transducer is composed of two AM-1801 [97] PV panels while module SPV1050 [98], especially devoted to ultra-low energy harvesting applications, implements the FOCV-MPPT function and integrates a buck-bust DC/DC converter. A resistor divider at the SPV1050 input allows one to program the multiplying factor *k* value in (xxviii).

The set of panel P-V curves required as input for the *characterization algorithm* was obtained by measuring the AM-1801 PV panel at six values of illuminance level: 160 lx, 300 lx, 600 lx, 900 lx, 1200 lx and 1500 lx. For each illuminance level, the P-V curves were plotted and reported in Fig. 61.

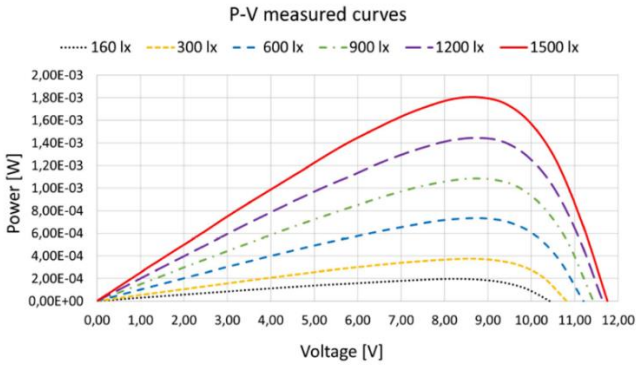

Fig. 61 Sanyo AM-1801 Panel P-V measured curves at various different illuminance levels

Considering extracted curves, a value of 0.8 is a reasonable choice for *k* factor.

Fig. 62 shows the measured (solid line) versus reconstructed (dashed line) P-V curve at an illuminance level of 450 lx, one of the illuminance levels used for

the optimization phase. The two points used for curve reconstruction are indicated: (V_M, $P_M = V_M \cdot I_M$) and (V_{OC}, 0).

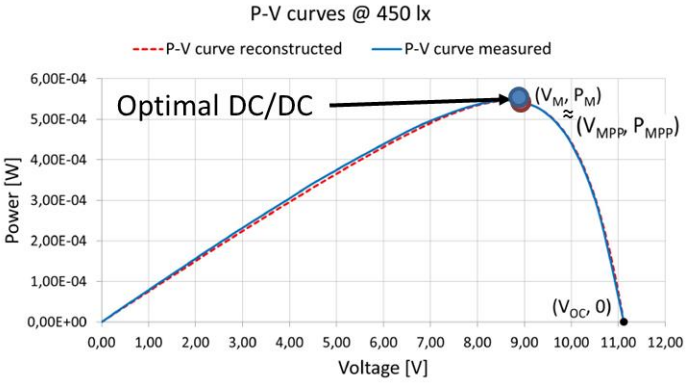

Fig. 62 Measured vs reconstructed P-V curve at 450 lx. (V_M, P_M) and (V_{OC}, 0) sampled when k = 0.8 (optimal condition)

The two curves are in good agreement and the error between the measured PMPP and the reconstructed one is 0.23 %. The error is defined as:

$$P_{MPP\_err} = \frac{\left|P_{MPP\_meas} - P_{MPP\_reconstr}\right|}{P_{MPP\ meas}} \cdot 100 \qquad (xxxvi)$$

Table 11 shows, for different illuminance levels, the two points used for reconstruction (V_{OC} and V_M/P_M), the MPP of the measured and reconstructed curves (V_{MPP}/P_{MPP} meas. and V_{MPP}/P_{MPP} reconstruct.) and, in the last column, the error between the maximum power points (P_{MPP_err}), defined in (xxxvi).

Table 11 MPP errors between measured and reconstructed curves ((V_M, I_M) and (V_{OC}, 0) sampled with k = 0.8)

Lux	**V_{OC} [V]**	**V_M/P_M [V/W]**	**V_{MPP}/P_{MPP} meas. [V/W]**	**V_{MPP}/P_{MPP} reconstr. [V/W]**	**P_{MPP_err} [%]**
160	10.42	8.34 / (1.9673·10-4)	8.34 / (1.9673·10-4)	8.18 / (1.9714·10-4)	0.2
300	10.81	8.65 / (3.7619·10-4)	8.65 / (3.7619·10-4)	8.46 / (3.7721·10-4)	0.27
600	11.2	8.96 / (7.3203·10-4)	8.96 / (7.3203·10-4)	8.68 / (7.3567·10-4)	0.5
900	11.42	9.14 / (1.0744·10-3)	8.57 / (1.0843·10-3)	8.76 / (1.0835·10-3)	0.08
1200	11.64	9.31 / (1.4154·10-3)	8.73 / (1.4448·10-3)	8.79 / (1.4399·10-3)	0.34
1500	11.75	9.40 / (1.7484·10-3)	8.81 / (1.8048·10-3)	8.75 / (1.7961·10-3)	0.48
450	11.12	8.90 / (5.4355·10-4)	8.34 / (5.4460·10-4)	8.65 / (5.4586·10-4)	0.23
750	11.39	9.11 / (9.0118·10-4)	8.54 / (9.1319·10-4)	8.77 / (9.0819·10-4)	0.55

The highlighted rows display the illuminance levels not included in the measured set of P-V curves used for reconstruction. In all cases tested the error between measured and calculated P_{MPP} is lower than 0.55 %. The difference between measured and reconstructed VMPP is in all cases lower than 0.3 V; note that the V_{MPP} difference results in such a low error in estimated MPP since around this point the derivative of the power curve is low.

Once verified the correct behavior of the method when DC/DC is working with an appropriate k factor, further analysis have been accomplished in order to evaluate the algorithm when DC/DC is suffering from some kind of malfunction in the MPPT mechanism, and therefore it is operating at a wrong k factor. To do so, the system was forced to work with $k = 0.6$, far lower than correct value of 0.8, in order to simulate a degradation in MPPT algorithm.

Fig. 63 show the reconstructed curve at 450 lx with a degraded k factor = 0.6. It can be observed that even if the operating point in this case is far away from the MPP, the reconstructed curve is still a good approximation of the measured one. The error in the estimated P_{MPP} is larger than in the previous cases but less than 2 % while the V_{MPP} difference is still in the same order (0.3 V). It can easily be observed that the operating point V_M is lower than the optimum one V_{MPP}, which enables one to state that $k = V_M / V_{OC}$ is lower than optimum and suggests the correcting action of increasing k by acting on the voltage divider at the DC/DC converter input. Similar results were obtained for different illuminance levels and programmed k values, showing that the proposed technique allows an accurate estimate of MPPT efficiency to be made without requiring a scan of the full PV panel characteristic.

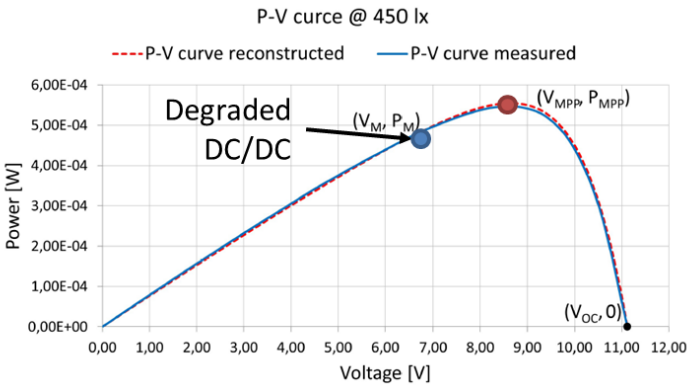

Fig. 63 Measured vs reconstructed P-V curve at 450 lx. (V_M, P_M) and (V_{OC}, 0) sampled when k = 0.6 (degraded condition)

Ultimately, the proposed method allows to reconstruct the characteristic when the PV cell is integrated in a harvesting system composed of the cell itself and a DC/DC converter implementing an FOCV-MPPT technique without additional dedicated power-consuming circuitry or power loss due to short-circuit current measuring. The algorithm combined with an external

measurement unit, connected during the debug phase in series between the transducer and the DC/DC converter, is applied so as to verify the efficiency of the MPP tracking technique in a prototype energy harvesting system composed of indoor PV panels. Experimental results prove that the error between the measured and reconstructed curves in the MPP point to be evaluated is less than 1 % if the measured point used to reconstruct the curve is near the MPP. This error increases (less than 2 %) if it is far away from the MPP, but the difference in the estimated V_{MPP} remains in the same range (0.3 V). The difference between the calculated V_{MPP} and the transducer operating point V_M is a clear indicator if the k factor is not optimum for maximizing power transfer; by observing the reconstructed characteristic, one can easily understand the corrective action to be taken on the multiplying k factor.

Chapter 5

Robustness and durability aspects due to Hot Carrier Degradation in switching devices

Another important aspect related to the concepts of robustness and durability is the one regarding the health and degradation rate of the single transistors which are the basis of the integrated circuits for power management. As widely explained in section 1.5 and 2, the specific waveform in a common DC/DC converter has an impulsive shape, since one or more integrated switches, typically n-MOS or p-MOS transistors, are periodically switched on and off in order to control the flow of current from input source to output load. In this scenario, a typical situation is the one occurring during the commutation transient time between ON and OFF state, when transistors are simultaneously subjected to high values of gate-source voltage and drain source voltage.

Referring to Fig. 7, if we consider n-MOS *D*, during the *OFF phase* it is switched off and its drain node is shorted to the output load through the p-MOS *B*, making its voltage possibly equal to the input source or even more in boost devices. When transition between *OFF phase* and *ON phase* occurs, then n-MOS *D* is switched on and its drain voltage drops approximately to ground, yet during this transition the voltages of gate and drain are found to be high at the same time for a brief transient time interval. As a matter of fact, this transition starts with the gate node driven high (i.e. brought to the supply voltage) in order to switch on the n-MOS, and after that the drain node starts to discharge till it reaches approximately ground, with a time constant depending on associated RC parasitic elements. Similar considerations may be made for other MOS switches involved in the DC/DC conversion too. A typical waveform showing this situation is reported in Fig. 64, being the red line the drain voltage while the blue line the gate voltage.

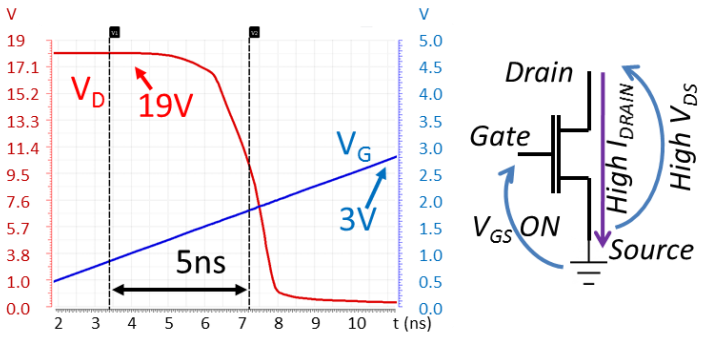

Fig. 64 Typical switching condition in DC/DC MOS elements

This condition is proven to be the major cause for single MOS degradation due to hot carrier effect in lateral double-diffused MOS (LDMOS) power transistors [99]. Indeed, in the presence of a high voltage drop between source and drain, the electric field is much stronger on the source side than on the drain side, and the voltage drop due to the channel current is concentrated on the drain side. As a consequence, carriers traveling from the source to the drain can gain a considerable amount of energy, becoming the so called *hot carriers*. If the acquired energy is sufficient, some of these carriers may be able to surmount the energy barrier at the Si/SiO_2 interface and be injected into the oxide. Then, they can be eventually permanently trapped in the oxide or break some binds in the oxide or at the SiO_2 interface, producing the effect of hot carrier degradation (HCD) [100].

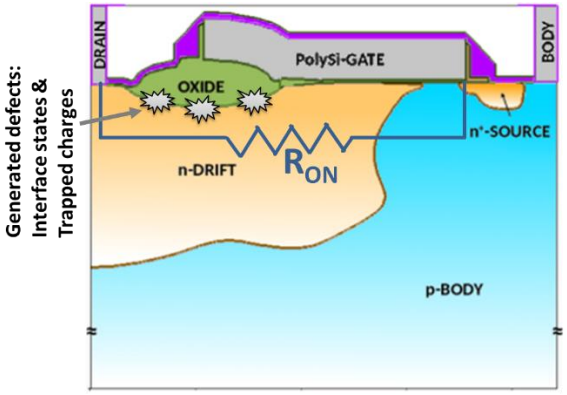

Fig. 65 Schematic of the medium rated voltage N-drift LDMOS with customized thick oxide realized on 200-mm silicon wafer. "A. N. Tallarico et al., "Investigation of the hot carrier degradation in power LDMOS transistors with customized thick oxide" in Microelectronics Reliability. vol. 76-77, pp. 475-479, Sep. 2017"

In Fig. 65 a section of an N-drift LDMOS is presented, which shows the generated traps and interface states due to hot carrier degradation. Moreover, the intrinsic on-resistance of the device is depicted too, which represents the actual resistance of the device while working in ON-state regime. The remarkable thing is that the R_{ON} value has a strong correlation with the HCD, in the sense that this kind of degradation produces an increase in the on-resistance of the device [101], which is depicted in Fig. 66.

Graph presented in Fig. 66 clearly shows the relationship between the degradation rate, evaluated as the stress time applied to the device, and the correspondent on-resistance.

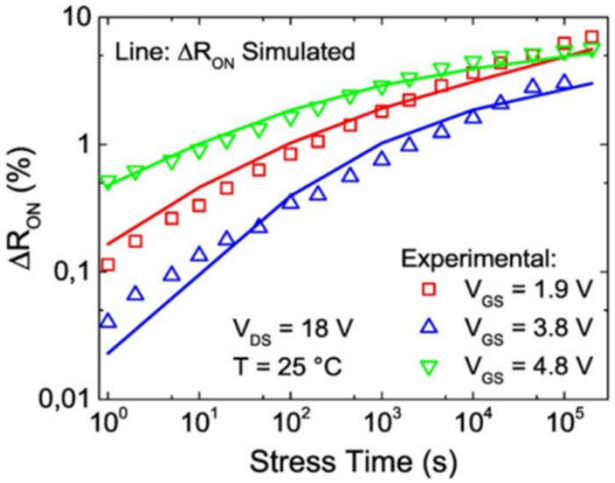

Fig. 66 Experimental (symbols) and simulated (line) R_{ON} degradation as a function of different stress conditions. "A. N. Tallarico et al., "Investigation of the hot carrier degradation in power LDMOS transistors with customized thick oxide" in Microelectronics Reliability. vol. 76-77, pp. 475-479, Sep. 2017"

Moreover we can also state that higher V_{GS} voltages produce higher degradation values, especially in the early period, and that the actual on-resistance of the device can be a good estimator for the overall degradation state. As a consequence, while obviously reducing the lifetime of the device by introducing reliability issues, HCD has also a negative impact on the efficiency of the overall DC/DC converter. For this reason, several studies have been proposed in order to model, predict and prevent this mechanism.

5.1 State-of-the-art solutions

Several models of HCD mechanisms have been recently proposed in order to perform effective predictions of the degradation level, both in terms of analytical expressions to be solved through a mathematical approach and physical representations of devices to be simulated through technology computer-aided design (TCAD) tools [102, 103, 104, 101].

On the other hand, in order to tackle HCD problem by reducing the probability of generating defects on the SiO_2 interface, advanced physical layouts are being studied which are less susceptible to the effect of hot carrier generation. In this direction [105] proposes a novel architecture of a lateral DMOS transistor with multiple floating poly-gate field plates and a modified recessed poly-gate structure which guarantee a reduction of the degradation ratio of about 36%.

Working at circuit level, other solutions are proposed aiming at smoothing or shifting the commutation edges in order to avoid the concomitant presence of high gate-source and drain-source voltages [106, 107, 108, 109]. Several different architectures are presented with different levels of complexity, all of them sharing the basic idea of adding a switching element possibly in combination with other passives (diodes, inductors, capacitors), which through a proper synchronization can both reduce the gradient or the flowing current during transitions and space edges of drain and gate nodes, for example by bringing the drain voltage to zero before the MOS is switched into an ON state. Although these kind of architectures are usually developed to solve efficiency and electromagnetic interference problems, they can also be adopted in the field of hot-carrier degradation [110], at the cost of increased design complexity.

A constant interest is also observed in developing solutions able to monitor the degradation state due to hot-carrier effect [111, 112, 113, 114], including both on-line and off-line architectures. The chance to know the degradation level of one on more devices inside an integrated circuit is obviously an effective way to predict the lifetime of the entire system in a reliability perspective, but it can also be useful in an efficiency perspective, for example by including additional circuitry which would be possibly able to compensate the increase of power losses due to the higher values of MOS on-resistance associated with HCD. In this scope a novel architecture has been studied and implemented in order to monitor the degradation status of a MOS switch in a DC/DC converter for power management.

5.2 Studied solution: monitoring HCD in DC/DC converters

Considering specific issues of developing a monitoring system for HCD in DC/DC converters, some aspects should be taken into account:

- DC/DC converters are circuits that serve the overall system by providing power supply to all other block, so a reasonable approach is to develop an on-line methodology which would be able constantly monitor HCD at runtime without halting the converter.
- As explained in section 5, the actual value of on-resistance R_{ON} is a good predictor for the MOS degradation. Nevertheless in order to know the value of R_{ON}, both drain voltage and current must be known at the same time, which introduces some challenges especially for what concern the current measurement. As a matter of fact, typical current sensing architectures include a sense resistor on the current path [115, 116], but as already discussed in chapter 2, the introduction of any resistive path has a strong negative impact on the efficiency of the system. Thus the current sensing architecture should be carefully designed in order to consider such aspect.

Starting from these considerations, a dedicated design was implemented for a boost DC/DC converter with on-the-fly embedded hot-carrier degradation monitoring through a sensing mechanism of the on-resistance of the MOS under observation. The project was developed in association with STMicroelectronics within the European project *R2Power300* and *ECSEL joint undertaking* group, for the continuous technological innovation on smart-power technology and design.

As a reference, a conventional DC/DC boost architecture is presented in Fig. 67, which clearly identifies the n-MOS device that may be subjected to hot-carrier degradation. Taking this schematic as basis for developing the monitoring system, the main challenge is to efficiently measure the voltage at drain node *D* and the corresponding current I_{DRAIN} in order to evaluate the value of the on-resistance R_{ON}, accordingly to Ohm's law. Moreover, from a practical point of view, this means that it would be necessary to provide an additional mechanism to calculate the resulting resistance as the ratio between the monitored voltages and currents, being sure to correctly synchronize the two signals. The required mechanism could be either integrated within the DC/DC converter or external, and in the first case the circuit would directly provide the value of resistance, while in the second case it should provide two different vales for voltage and current.

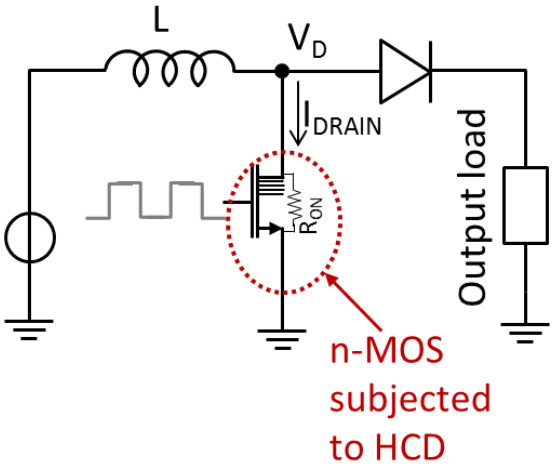

Fig. 67 Typical architecture of a boost DC/DC converter

In any case, a degradation in the observed MOS would produce an increase in the R_{ON} resistance and, as a consequence, an increase of the drain voltage V_D for the same current flowing. In other words, a percentage variation of R_{ON} ($\%\Delta R_{ON}$) produces an equal percentage variation of V_D ($\%\Delta V_D$), while in absolute terms we have:

$$\Delta V_D = \Delta R_{ON} \cdot I_D; \quad \%\Delta R_{ON} = \%\Delta V_D \quad @\ fixed\ I_D \qquad (xxxvii)$$

It is clear from (xxxvii) that if we also take into account possible noise or errors in the measurement of ΔV_D, then the best signal-to-noise-ratio is obtained at the highest current flowing I_D. In addition to that, since the current flowing into the observed MOS has typically a saw-tooth shape as described in section 1.5, the maximum obtainable current always occurs on the threshold between the *ON phase* and the *OFF phase*, i.e. just before the MOS is switched off.

5.2.1 A reliability aware DC/DC converter

Starting from these considerations, a simplified approach can be investigated, instead of constantly monitoring both current and voltage values. The proposed idea is to fix the maximum current flowing in the observed MOS at the end of the *ON phase* and then to sample the drain voltage V_D exactly when maximum current is reached just before switching off the MOS: in this way the comparison on V_D is always performed at the same flowing current so the percentage variation of R_{ON} can be directly obtained from the percentage variation of V_D, and furthermore the comparison is always performed when current is at its maximum, so improving measurements precision.

The architecture of the proposed solution is shown in Fig. 68.

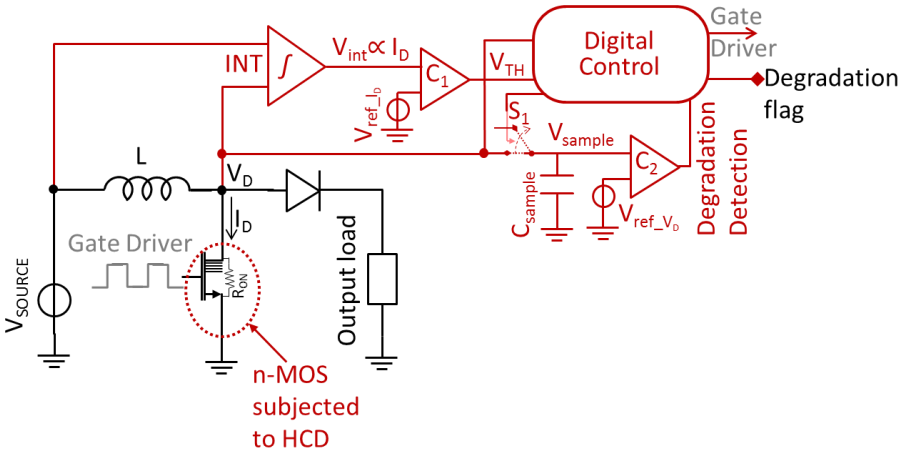

Fig. 68 Proposed architecture of a boost DC/DC converter with embedded detection of degradation level

The combination of the integrator circuit *INT* and the comparator circuit C_1 is used to set the maximum current inside the monitored MOS; the sampling circuit composed by the switch S_1, the sampling capacitor C_{sample} and the comparator circuit C_2 are used to store the information about the RON variation and possibly generate a flag signal if the detected variation is above a predefined

threshold; a digital control circuit is designed which generates the gate signal of the switching element. The chosen technology for implementation is a 90 nm BCD process.

5.2.2 Functional overview

In order to control the flowing current without introducing any resistive element, the relationship between voltage and current of inductor L is exploited. Starting from the general equation of the inductor it is possible to state that:

$$V = L\frac{dI}{dt} \xrightarrow{yields} I = \frac{1}{L}\int V + I_{init} \qquad (xxxviii)$$

The integrator *INT* generates a signal V_{INT}, which is obtained by integrating the voltage drop across the inductor, which is therefore proportional to the current I_D during the *ON phase*, when the MOS is switched on. The value of the maximum current is then set by means of an external reference voltage V_{ref_ID}, which must be chosen following:

$$V_{ref\_I_D} = \alpha \cdot L \cdot I_{MAX}; \qquad I_{MAX} = \frac{V_{ref\_I_D}}{\alpha \cdot L} \qquad (xxxix)$$

being α a proportional coefficient related to the specific implementation of the integrating circuit, explained in detail in section 5.2.3. During this phase, the sampling switch S_1 is closed, so that V_{sample} follows the value of V_D.

Once the maximum predefined current I_{MAX} is reached, the control signal V_{TH} is raised, this meaning that the drain voltage V_D is ready to be sampled. As a consequence the digital control block opens the sampling switch S_1 and drives the gate driver low, so determining the end of the *ON phase* and the consequent beginning of the *OFF phase*. In this way, C_{sample} stores the value of V_D when a precisely known current I_{MAX} was flowing through the drain of the observed MOS. Consequently the value of V_{sample} can be directly used to estimate the on-resistance of the MOS and it can optionally be compared with a reference value through the comparator C_2. For example, the value of V_{sample} for a fresh device V_{sample_fresh} can be considered, then a relative value of 105% of V_{sample_fresh} can be used for the reference value of V_{ref_VD}. In this way, since the percentage degradation of the R_{ON} is equal to the percentage degradation of V_D as explained in (xxxvii), then a specific flag is raised if the degradation exceeds 5%.

The sampling procedure is necessary in order to relax the timing constraints of the comparator C_2 and of the digital control block, since with this architecture they have a period of time equal to the whole duration of the *OFF phase* in order to complete the comparison and potentially raise the flag signal. From an operative point of view, the behavior of the system can be recapped as follows:

- A specific value of V_{ref_ID} must be chosen, which sets the exact value of the peak current through the observed MOS at the end of the *ON phase*. The precise relationship between V_{ref_ID} and I_{MAX} is reported in section 5.2.3.
- The DC/DC converter is then operated at time zero, i.e. with a fresh device, and the value of V_{sample} is observed. This value V_{sample_fresh} represents the reference value associated with the initial R_{ON} of the device.
- A custom maximum relative degradation value is taken into account and used to set V_{ref_VD}. For example if the maximum acceptable degradation for the device is 5%, then a value equal to 105% of V_{sample_fresh} should be chosen for V_{ref_VD}.
- During normal operation, the *ON phase* always lasts exactly the time needed for the current to reach the peak value I_{MAX}. The subsequent *OFF phase* lasts the time needed to bring the current back to zero, which means that the inductor is always completely discharged every transition, so the converter actually works on the threshold between continuous and discontinuous mode (see section 1.5). This behavior is helpful as in this way the initial current at the beginning of the *ON phase* is always null, which simplifies the implementation of the integration circuit. As a matter of fact, the integration signal V_{INT} is proportional to the variation of the flowing current, so the initial value I_{init} should be taken into account, if not zero (xxxviii).
- Initially, the value of V_{sample} is equal to V_{sample_fresh}, so no exception is raised.
- Over time, R_{ON} resistance degrades, this producing a constant detectable increase in the value of V_{sample}, till it optionally reaches the V_{ref_VD} value, in which case a degradation flag is raised from the digital block.
- In order to speed-up the degradation of the observed MOS, a specific mode is provided controlled by an external pin. In this mode, the observed MOS is always switched on, while its gate and drain voltages can be set from the outside without affecting the rest of the electronics.

It is worth noting that since the comparison of different values of V_D is made when the maximum available current is flowing, then it is also guaranteed that the best measure precision is obtained too (xxxvii).

As explained, both the *ON* and *OFF phases* are regulated by the associated current flowing inside the inductor *L*. The first one ends when current is equal to I_{MAX}, the second one when the current drops to zero. It is clear therefore that in this architecture there is no active feedback between the output node and the duty cycle of the converter. As a consequence, the output voltage cannot be regulated by the modulation of the duty cycle. For this reason an additional comparator is provided which monitors the output voltage and which switches off the entire converter as soon as the desired output voltage is reached. Then, the hysteresis of such comparator guarantees that voltage remains close to the desired one, i.e. the converter is switched on again if output voltage drops below the desired value minus hysteresis. This approach is actually the same already explained for solutions in section 2.2. Accordingly, the output voltage is

subjected to two different kinds of ripple. The first one is associated to the normal switching activity of the converter and therefore its peak-to-peak value is related to the maximum output current and to the output by-pass capacitance, while its frequency is equal to the switching frequency of the converter. On the other hand, another ripple is observable which is caused by the described on-off regulation, whose peak-to-peak value is therefore equal to the hysteresis of the control comparator which monitors the output voltage. Consequently, this second ripple can be regulated by tuning the hysteresis of the comparator, and its frequency depends on the hysteresis itself, the output by-pass capacitance and the current load, assumed that it would be clearly lower than switching frequency of the converter.

As a consequence, the value of I_{MAX} should be chosen accordingly to the power request of the connected load, since the average extracted power from the source should be higher than the required one in order to achieve successful operation.

Finally, considering temperature variations of R_{ON}, no temperature compensation has been studied for this solution, since the objective was to verify the feasibility and the effectiveness of degradation monitoring. In order to overcome this issue in the present implementation, an external sensor could be considered to be placed on the testing board, in order to monitor the temperature of the device. With this information available, the obtained V_{sample} could be accordingly compensated if a reliable model of the dependence of R_{ON} over temperature is available.

Expected waveforms are presented in Fig. 69.

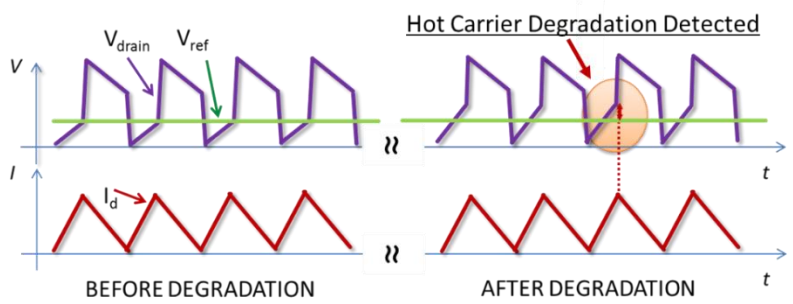

Fig. 69 Expected waveforms of respectively: V_{drain} (violet), V_{ref_VD} (green) and I_{drain} (red), before and after degradation

5.2.3 Maximum current regulation: integration block

In order to set the precise maximum current I_{MAX}, an integration approach is used. The objective of the integration block is to integrate the voltage drop across the inductor L in order to obtain an output signal proportional to the flowing current, as already mentioned in (xxxviii) and (xxxix). Furthermore, as explained

in 5.2.2, the initial current is always zero, so it is not necessary to consider the value of I_{init} in (xxxviii).

A typical integration architecture is presented in Fig. 70.

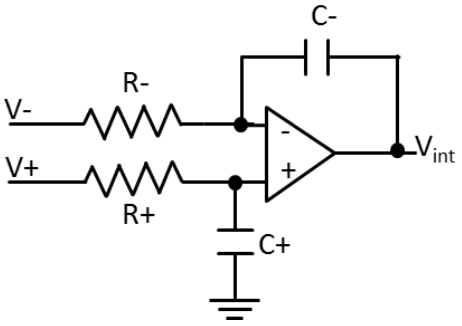

Fig. 70 Typical architecture of an integrator circuit with two coupled capacitors

In order to obtain a reliable integration, values of *C+*, *C-*, *R+* and *R-* should be correctly matched and, more important, they should be independent of any variation of the applied voltages. As obvious parasitic elements should be taken into account when considering matching, which are particularly critical in the adopted 90 nm BCD technology. As a matter of fact, the resulting structure with parasitic is presented in Fig. 71.

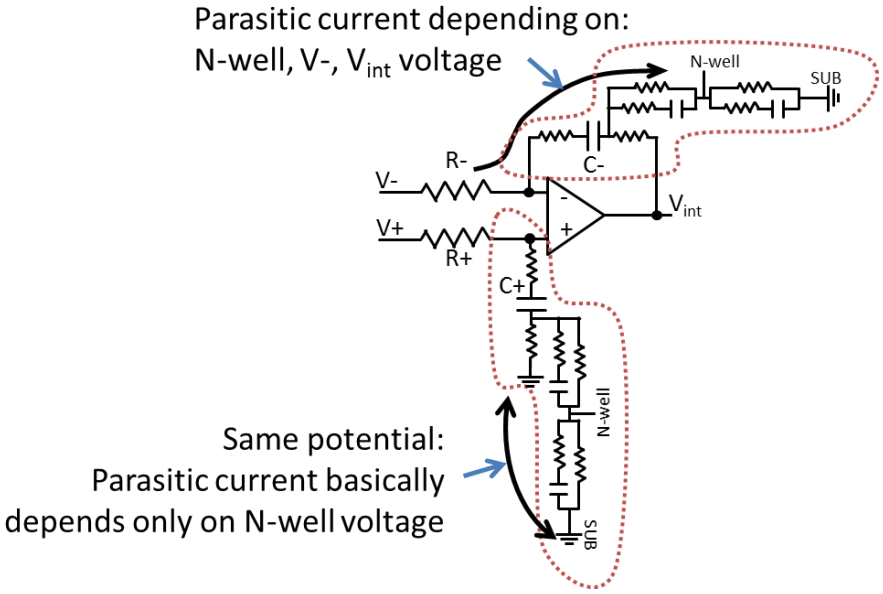

Fig. 71 Typical architecture of an integrator circuit with two coupled capacitors and parasitic elements exposed

The resulting effect is that parasitic currents flow in the two capacitive branch is present, which partially depend on the voltages of n-well and substrate nodes. Even worst, they depend on input and output voltages (V-, V+, V_{int}), and therefore they are not equal in the two branches and they vary accordingly to the working point of the circuit, so they cannot be easily compensated. As a consequence, the conversion factor α used to determine I_{MAX} (xxxix) is not constant.

In order to overcome this problem, an alternative structure is proposed, shown in Fig. 72.

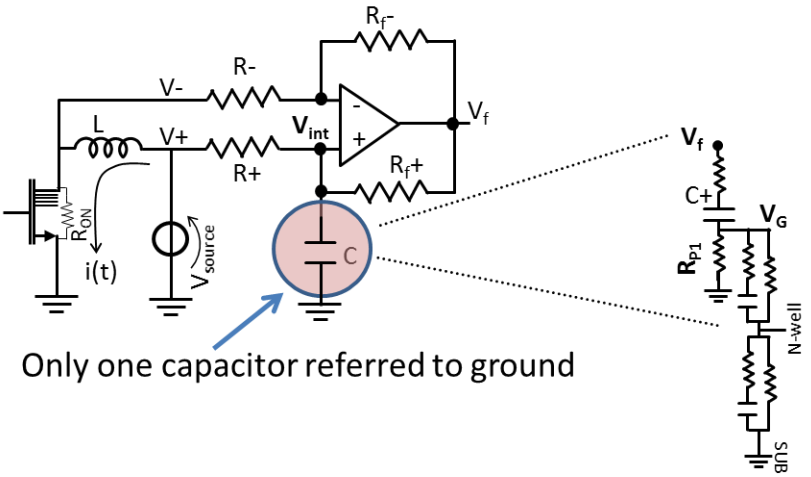

Fig. 72 Adopted architecture of the integrator circuit, with parasitic exposed and a unique capacitor element connected to ground.

With this solution, a unique capacitor is adopted connected to ground. Since substrate and N-well are at fixed values, then the resulting effect due to parasitic is to simply increase the value of C, plus a minor resistive effect depending on the value of R_{P1}, which can be neglected in first approximation. The resulting transfer function between flowing current $i(t)$ and integration signal $V_{int}(t)$ is therefore:

(xl)

$$\begin{cases} V_{int}(s) = \dfrac{L}{R^+ \cdot C} \cdot i(s) \cdot \dfrac{\delta s}{s + \dfrac{1-\delta}{R^+ \cdot C}} - \dfrac{V_{source}}{R^+ \cdot C} \cdot \dfrac{1-\delta}{s + \dfrac{1-\delta}{R^+ \cdot C}};\ \delta = \dfrac{R_f{}^- R^+}{R_f{}^+ R^-} & \textit{Laplace domain} \\ V_{int}(t) = \dfrac{L}{R^+ \cdot C} \cdot i(t) * \dfrac{\delta - 1}{R^+ \cdot C} \cdot e^{\frac{\delta-1}{R^+ C}t} - \dfrac{V_{source}}{R^+ \cdot C} \cdot e^{\frac{\delta-1}{R^+ C}t};\ \delta = \dfrac{R_f{}^- R^+}{R_f{}^+ R^-} & \textit{Time domain} \end{cases}$$

which can be simplified for δ = 1 as:

(xli) $$V_{int}(t) = \frac{L}{R^+C} \cdot i(t); \quad \begin{cases} \delta = \dfrac{R_f{}^- R^+}{R_f{}^+ R^-} = 1 \\ R^+ = \dfrac{L}{V_{ref\_I_D} C} \cdot I_{MAX} \\ R_f{}^+ = R^+ \cdot \dfrac{R_f{}^-}{R^-} \end{cases}$$

Another interesting aspect of this architecture is that it is possible to add any arbitrary capacitance to nodes V_{int} and V_f, without affecting the behavior of the integrator circuit, but only changing the conversion factor α. Thanks to this property, R_f+ and R+ can be placed outside the integrated chip and properly chosen in order to match the ratio δ = 1. As a further consequence, it is possible to also place the capacitor C outside the integrated circuit.

From a practical point of view, provided that δ = 1, then the value of $V_{ref\_I_D}$ should be chosen following the formula:

(xlii) $$V_{ref\_I_D} = \frac{L}{R^+C} \cdot I_{MAX}$$

Finally, operating frequency can be approximate as following:

(xliii) $$f_{SW} = \frac{1}{2} \cdot \frac{1}{-ln\left[\left(1 - \frac{I_{MAX} R_{ON}}{V_{IN}}\right)^{\frac{L}{R_{ON}}}\right]}$$

5.2.4 Comparison circuits

Referring to figure Fig. 68, two comparison circuits are provided in order to implement comparators C_1 and C_2. Input voltages associated with these circuits are relatively low with respect to the maximum driving operative range of the used MOS (5V), and the adopted architecture is almost equal to the one presented in Fig. 14, section 2.2.4, and it is not further analyzed in this section.

On the other hand, considering the behavior of the proposed converter explained in section 5.2.2, two other comparators should be included, as depicted in Fig. 73. The first one, $Comp_{ZCS}$, is used to detect when the current flowing inside the inductor L towards the output load drops to zero, so determining the end of the *OFF phase*. From an operative point of view, during the *OFF phase* the drain voltage V_D is forced to be higher than input voltage in order to allow the flow of current through the diode D. As soon as the current is nullified, V_D falls again below V_{SOURCE} so determining the commutation of the comparator.

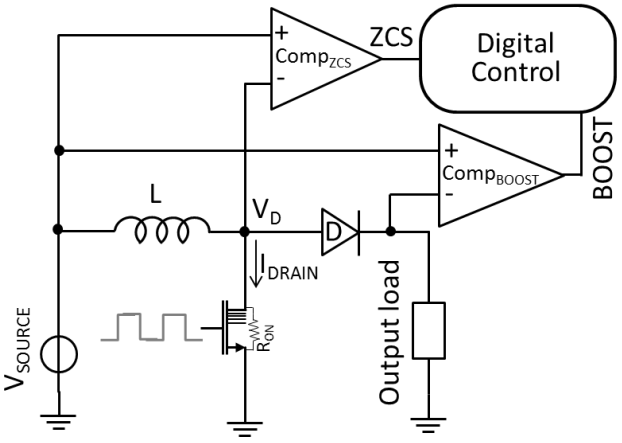

Fig. 73 Block diagram of additional control signal of proposed DC/DC converter with associated comparators

The second one, $Comp_{BOOST}$, is necessary to monitor when output node exceeds input source, this meaning the converter should actually start to operate as a boost converter. As a matter of fact, till output voltage remains above input source, a positive flow of current is always allowed from input to output through the series of inductor L and diode D, so no switching operation is necessary.

As both these two comparators are connected to high voltage nodes (both V_{SOURCE} and V_{OUT} can assume values above the maximum driving operating voltage of adopted MOS (5V)), then a dedicated design must be provided.

A simple approach is to use a dual architecture of the one proposed in Fig. 16 (a), but in this case a constant bias current would always be drawn from the V- node, which is connected to the output node in the proposed structure. This is particularly unfavorable as it may result in an unwanted discharge of the output node when converter is in idle mode. As a consequence, a new architecture is proposed in Fig. 74.

In this solution, a bias current of approximately 6 nA is drawn from V+ node, which is actually connected to input source in this configuration and which therefore doesn't affect the output node, while causing a negligible impact on the quiescent current of the overall system. LM_F, LM_H and LM_L are power LDMOS, which can accept up to 20 V as drain-source voltage with a maximum gate-source / gate-drain drop of 5V. When V- is higher than V+, than LM_H is switched off, so no flow of current is allowed and node V_d is brought slightly above V+ node. At the same time, differential amplifier DOA tries to compensate this variation by decreasing feedback signal V_f, so partially switching off MOS LM_F. Because of that, current flowing inside LM_F is erased, and as a consequence node V_g exactly follows the value of V- (more precisely V- minus the characteristic threshold value of MOS LM_L and LM_H). In this way, a proper V_{GS} (< 5V) is always present across LM_L and LM_H, while the main drop (V- - V+) is applied to drain-source nodes, as desirable.

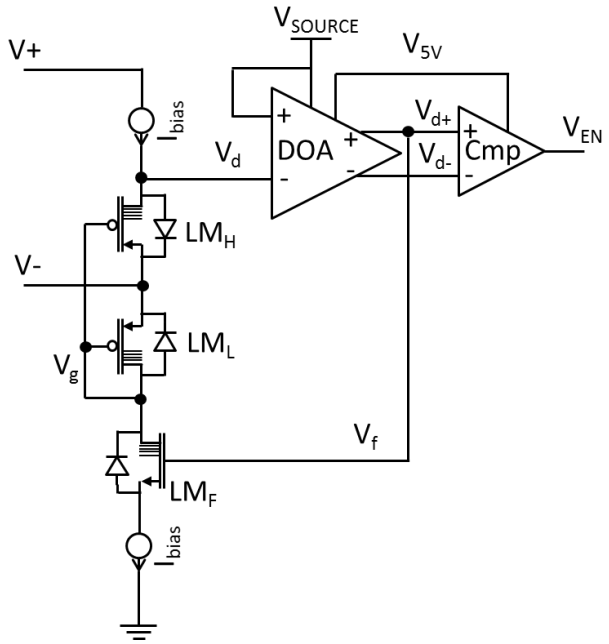

Fig. 74 Schematic of a novel comparator with wide input voltage range adopted to generate additional control signal

Conversely, when *V-* falls below *V+*, bias current is allowed to flow through LM_H and V_d drops below V_{SOURCE}. Hence, *DOA* increases feedback signal V_f, so switching on LM_F. In this case, bias current is also allowed to flow inside LM_F, whose value is almost equal to the one in LM_H. Consequently, feedback action forces the node V_g to assume a value which allows the flow of a current equal to I_{BIAS} through both LM_H and LM_L. As in previous case, gate-source voltage is always below maximum operating range of 5V for all considered MOS. Moreover, the current drawn from node *V-* is only the difference between the two bias currents, which mainly depends on layout mismatches between current sources.

Simulated results prove that a total current < 1 nA is statically drawn from node *V-* in both cases.

Finally, comparator *Comp* transforms the differential information into a rail-to-rail signal suitable for digital logic.

For the sake of completeness, the schematic of the differential operation amplifier *OPA* is reported in Fig. 74. The interesting thing is the presence of a double supply, as the first stage needs to handle signals in the range of the supply voltage up to 12 V, while the output stage needs to provide a signal which is suitable for the subsequent circuits operating at 5 V. Furthermore, in the first stage of the circuit, a series of high voltage LDMOS is used in order to decouple the high voltage section of the circuit, connected to V_{SOURCE}, to the low voltage

section of the circuit, connected to ground. Thanks to this architecture, when V_{SOURCE} rises above 5 V, all the exceeding voltage drop is applied to the decoupling MOS, thus guaranteeing a safe operating area for all other devices. Furthermore, this structure is self-biased, in the sense the gate voltage Vg is directly set trough the combination of bias current I_{BIAS} and LD_1 in diode-configuration.

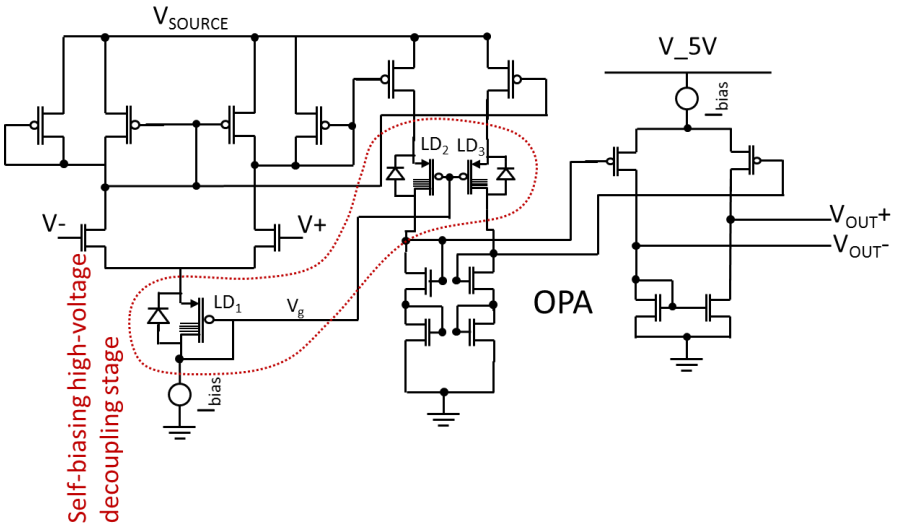

Fig. 75 Schematic of a dual-supply fully differential operation amplifier with wide input voltage range

For what concerns the architecture of comparator *Cmp* in Fig. 74, it is the exact dual structure of the one showed in Fig. 14, so no further analysis is presented in this section.

5.2.5 Delay aspects in I_{MAX} comparator

With reference to Fig. 68, a critical aspect may be the delay associated with comparator *C1*, which is used to determine the maximum flowing current. Considering the proposed architecture, a precise and stable control of the maximum current is mandatory in order to obtain reliable values of degradation status.

From a general point of view, if the gradient of the monitored current would always be the same in any condition, then a possible delay in comparator *C1* should only cause a constant offset in the maximum current. This situation is substantially harmless, since the crucial point is that the current should always be the same, regardless of its actual value. Unfortunately this is not the case, since the slew rate of the current depends on the input voltage V_{SOURCE}, as shown in Fig. 76.

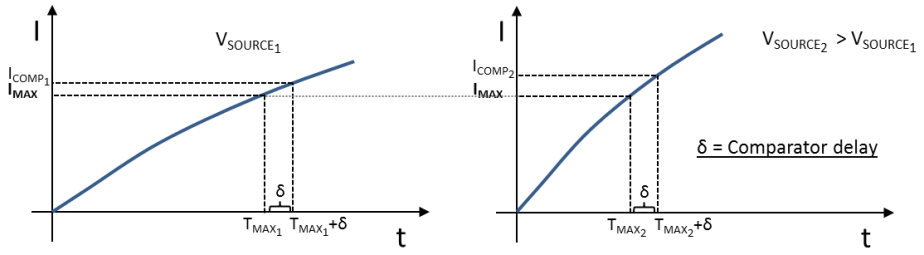

Fig. 76 Description of the effects of a potential commutation delay of designed comparators with respect to the actual value of the maximum current obtained at the end of the ON phase

Being I_{MAX} the expected value of maximum current, and δ the comparator delay, then two different actual values of maximum current (I_{COMP1} and I_{COMP2}) are obtained. From an analytical point of view, we can state that:

(xliv)
$$I_{comp} = \left(1 - e^{-\delta\frac{R_{on}}{L}}\right)\left(\frac{V_{SOURCE}}{R_{ON}} - I_{MAX}\right) + I_{MAX}$$

Consequently, if the maximum acceptable percentage error is ε, it can be argued that:

(xlv)
$$\frac{I_{comp_{max}} - I_{comp_{min}}}{I_{MAX}} < \varepsilon$$

Being $I_{compmax}$ and $I_{compmin}$ the minimum and the maximum values of I_{MAX} corresponding to the minimum and maximum acceptable values of V_{SOURCE}. Starting from (xlv), the maximum delay associated to comparator *C1* can therefore be expressed as:

(xlvi)
$$\delta_{MAX} < -\frac{L}{R_{ON}} ln\left(1 - \varepsilon \cdot \frac{I_{MAX}R_{ON}}{V_{SUP_{max}} - V_{SUP_{min}}}\right)$$

which for design values reported in Table 12 is approximately 70 ns for a 3% error, compatible with the designed solution.

5.2.6 Reference voltage circuit

An evolution of the bandgap circuit presented in section 2.4.1, and its schematic is shown in Fig. 77.

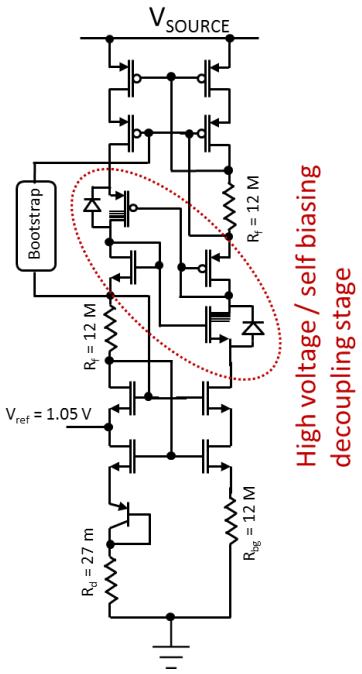

Fig. 77 Schematic of proposed bandgap reference with wide supply voltage range

The rejection to supply voltage is increased through the double-cascoded current mirror configuration, biased via resistors R_f, which guarantees a higher output impedance of the mirror stage. Moreover, the insertion of the decoupling stage allows this circuit to be suitable for supply voltages up to 12 V. In fact, as already explained in section 5.2.4, the role of the two LDMOS is to decouple the high voltage section of the circuit (above the decoupling stage) and the low voltage section (below the decoupling stage). Any voltage drop higher than 5 V is applied to the LDMOS, so that other two section always operate within safe operating conditions. Moreover, this structure is self-biased, as gate node of the two LDMOS is polarized through the associated coupled MOS in diode-configuration. Simulated overall current consumption of the module is less than 10 nA.

5.2.7 Simulated waveforms

In Fig. 78 simulated waveforms of described signals are shown.

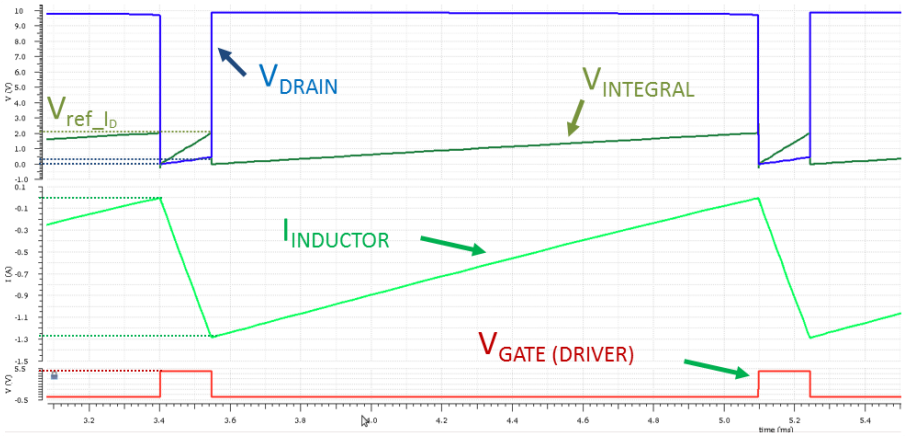

Fig. 78 Simulated waveforms of switching signal of proposed solution. In detail: drain voltage of observe MOS (blue), integrated voltage V_{int} (dark green), current flowing inside inductor (light green, negative by convention), and gate driver (red)

Simulated waveforms match expected behavior as described in Fig. 69. More precisely, during the *ON phase*, i.e. when gate driver is high, the inductor L is charged and its current (green) grows almost linearly, since it has been ideally connected to a constant voltage source V_{source} (notice that in the graph the current $I_{INDUCTOR}$ is negative by convention). During this phase V_{drain} increases accordingly to its intrinsic R_{ON} resistance, as well as the integral signal $V_{INTEGRAL}$ which follows the increasing current. As soon as it reaches V_{ref_ID} the *OFF phase* is started by bringing the gate driver to zero and switching off the connected MOS.

During the *OFF phase* the inductor L is discharged towards the output load and, as a consequence, the integrating signal $V_{INTEGRAL}$ increases accordingly, although it is not considered during this phase. It is worth noting that a reset circuit was added to the structure in Fig. 72, which shortens the capacitor C to ground at the end of each *ON-OFF phase*. Thanks to that signal $V_{INTEGRAL}$ always starts from zero so avoiding residual errors due to subsequent integration processes.

A more detailed simulation is presented in Fig. 79, with shown signals referring to Fig. 68.

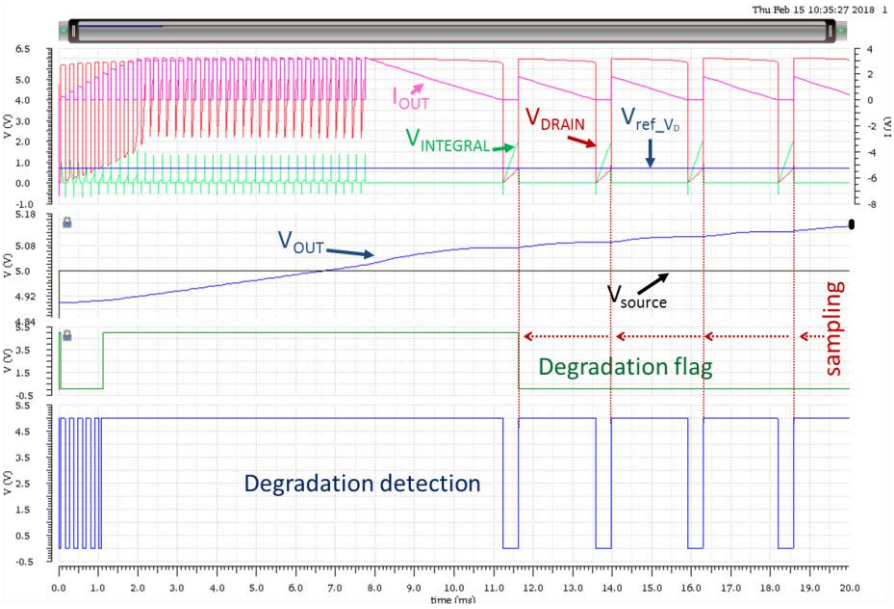

Fig. 79 Simulated waveforms of switching signal of proposed solution in detail – before degradation. First strip: drain voltage of observe MOS (red), integrated voltage V_{int} (green), current flowing towards output load (purple), reference value V_{ref_ID} (blue). Second strip: out voltage (blue), source voltage (black). Third strip: degradation flag (green). Fourth strip: degradation detection signal, out of comparator C_2 (blue). Dotted vertical red lines represents the instant of time when degradation detection signal is sampled to potentially generate the degradation flag

This simulation refers to a precise condition when the drain voltage V_{DRAIN} is equal to the corresponding V_{ref_VD}. During the *ON phase*, the *degradation detection* signal is low, so it is correctly evaluated as zero at the end of the *ON phase* by the digital block, so no flag is raised as expected. Other signals follows the behavior already explained in Fig. 78. In this case, simulated R_{ON} is 400 mΩ with a peak current of 1.7 A and a reference voltage of 680 mV.

On the contrary, if R_{ON} exceeds 400 mΩ due to degradation the expected V_{DRAIN} is higher than the reference voltage V_{ref_VD}, this causing the flag event. This situation is reported in Fig. 80, where a R_{ON} of 590 mΩ is adopted. It is clear that in this case at the end of the *ON phase* the value of V_{DRAIN} is about 1 V, and since it is greater than 680 mV, then when sampling occurs the *degradation detection* signal is high and degradation flag is asserted.

In both cases, $V_{INTEGRAL}$ signal is significant only during the *ON phase* when it is actually used, while it is set to zero in every other situation through a dedicated circuit. This adjustment guarantees that its initial value is always zero at the beginning of the ON phase, so eliminating any incremental error which would otherwise affect the integration measure. As a matter of fact, in an

unconditioned integrator circuit the measure error is generally summed over time, so rapidly diverging.

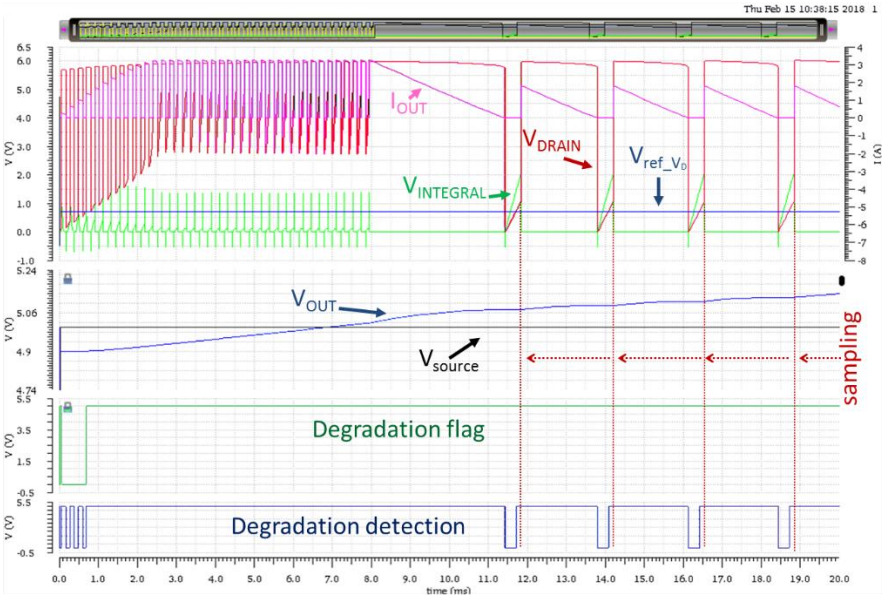

Fig. 80 Simulated waveforms of switching signal of proposed solution in detail – after degradation. First strip: drain voltage of observe MOS (red), integrated voltage V_{int} (green), current flowing towards output load (purple), reference value V_{ref_ID} (blue). Second strip: out voltage (blue), source voltage (black). Third strip: degradation flag (green). Fourth strip: degradation detection signal, out of comparator C_2 (blue). Dotted vertical red lines represents the instant of time when degradation detection signal is sampled to potentially generate the degradation flag

5.2.8 Specifications

The proposed solution was implemented in a 90 nm BCD technology in a 0.312 mm² area, using an LDMOS 20V-tolerant as switching element. Layout of integrated circuit is presented in Fig. 81.

The dimensioning of the switching MOS was particularly critic, due to the need to force its degradation through a dedicated procedure. As already mentioned a specific mode is provided which allows to directly drive the voltages of gate and drain of the observed MOS, in order to stress it and speed up its degradation. This specific procedure implies to apply high voltages to both gate and drain, with typical values of 3-5 V for gate and 12-15 V for drain, which can potentially lead to high values of flowing current with high level of produced heat due to Joule effect. Considering that the proposed package for the test chip has a thermal resistance of about 25 °C/W, the maximum acceptable dissipated power is about 5W. The width of the LDMOS has then been chosen accordingly and an associated nominal on-resistance of about 7.34 Ω.

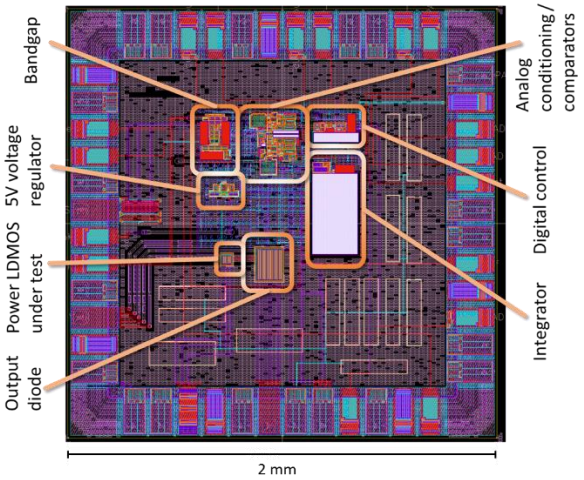

Fig. 81 Layout of the proposed solution of a boost DC/DC converter with embedded detection of degradation level, with different blocks highlighted

The reference voltage V_{ref_ID} is generated internally through a bandgap circuit, which also provides bias currents for the other analog blocks of the circuit. Its value is set to 1.05 V and it should be used to compute the value of $R+$ accordingly to (xlii). Considering that capacitance C is already integrated in the circuit and it has a value of 63 pF, then for example for an external inductor of 340 µF and a maximum current of 57 mA a value of 309 kΩ should be chosen for $R+$. Furthermore, taking into account a maximum current of 57 mA, the initial reference value V_{sample_fresh} is 418 mV, so guessing a maximum acceptable degradation of about 10% then a value of $410 \cdot 1.1 \approx 460$ mV for V_{ref_VD}

A summary of the simulated values is reported in Table 12.

Finally, a simulated efficiency of about 91.5% was observed for V_{source} = 9 V and V_{out} = 18V, while concerning degradation monitoring, simulated results show that a variation of 7% in R_{ON}, corresponding to a voltage variation of about 25 mV, can be correctly detected.

Table 12 Summary table of different dimensioning and operating conditions of proposed solution

Parameter	Value	Unit
Operating conditions		
Input voltage range	3-12	V
Output voltage range	0-20	V
Maximum power dissipation	5	W
Maximum current	~60	mA
Switching frequency	68-290	kHz
Size		
Core area	0.312	mm^2
Internal dimensioning		
V_{ref_ID}	1.25	V
R-	10	MΩ
R_f-	10	kΩ
C	63	pF
External dimensioning		
R+	309	kΩ
R_f+	309	Ω
V_{ref_VD}	460	mV
L	340	µH

5.3 Results and discussion

Preliminary tests were performed on a produced prototype with a ceramic dual-in-line package (DIP) and a dedicated breadboard. The schematic of the designed testing board is reported in Fig. 82. Components highlighted in red represent the integrated circuit under evaluation, while black components are discrete elements mounted on board. Dedicated test point (marked *TP* in picture) was included in final layout of the test-chip in order to easily monitor internal nodes, for both low-impedance nodes (e.g. comparator outputs) and high impedance nodes (e.g. bandgap voltage reference). Specifically for high-impedance nodes, specific buffers were added on board by mean of Analog® AD823 operation amplifiers (B_1, B_2, B_3), in order to avoid any disruption of the monitored signals. Considering the output load, a 1 mF capacitor is adopted, combined with an optional Zener Diode in order to limit maximum output voltage so preventing accidental breakdowns.

Concerning inductor L and feedback resistances R1 and R2, two sets of values was used, specifically 470 µH, 309 Ω, 309 kΩ and 10 mH, 6.2 kΩ, 6.2 MΩ. With these two sets, the maximum current inside the inductor is kept constant, while switching frequency is reduced of an approximated factor 20.

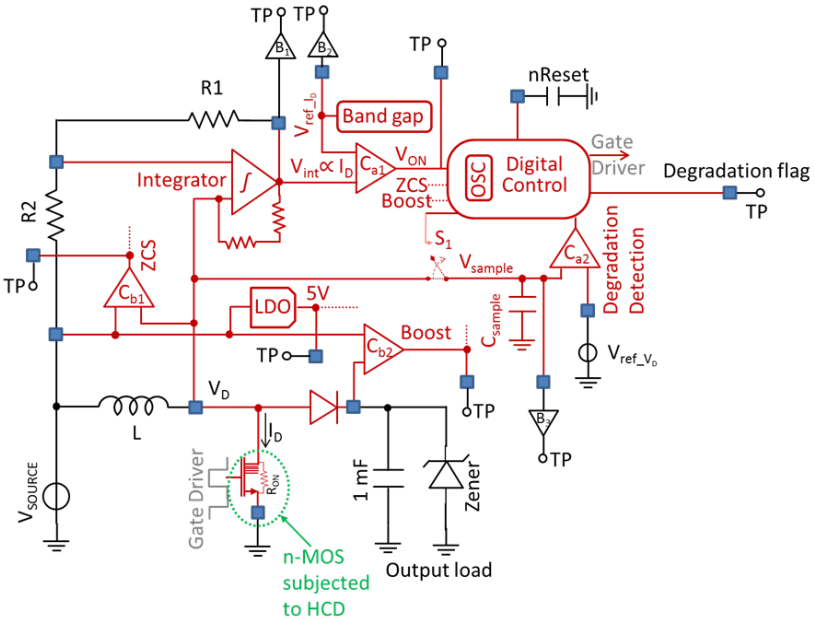

Fig. 82 Schematic overview of the testing board for the proposed solution of a boost DC/DC converter with embedded detection of degradation level

A first analysis was performed on critical elements of the system, more precisely on modules which are connected to high voltage nodes (> 5V), which requires dedicated structures as described in section 5.2.4.

High voltage comparators $Comp_{ZCS}$ and $Comp_{BOOST}$ (namely C_{b1} and C_{b2} in Fig. 82) was tested by directly applying different voltages on their input pins which are accessible through dedicated test points. Measured results are presented in Fig. 83.

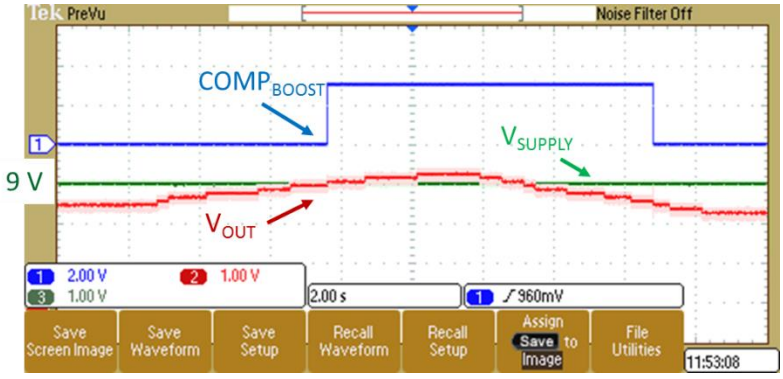

Fig. 83 Waveforms of tested high-voltage comparator. Respectively: supply voltage and comparator negative input (green), output voltage of DC/DC converter and comparator positive input (red), comparator output (blue)

Referring to Fig. 83, tested circuit is $Comp_{BOOST}$ described in 5.2.4. The green signal is the supply voltage which is also the negative input of the comparator, the red signal is output voltage of the DC/DC converter which is also the positive input of the comparator, while the blue line is the output of comparator. The circuit properly detects the voltage crossing between the two inputs, as soon as output voltage rises above supply voltage which is set to 9 V. Moreover, a hysteresis of about 500 mV can be noted, which was purposely added in the design through an additional feedback circuit applied to the comparator, in order to avoid possible ringing of comparator signal since output voltage has typically low slew-rates.

Specific tests were performed on the bandgap voltage reference described in section 5.2.6. The generated reference voltage versus input voltage is presented in Fig. 84.

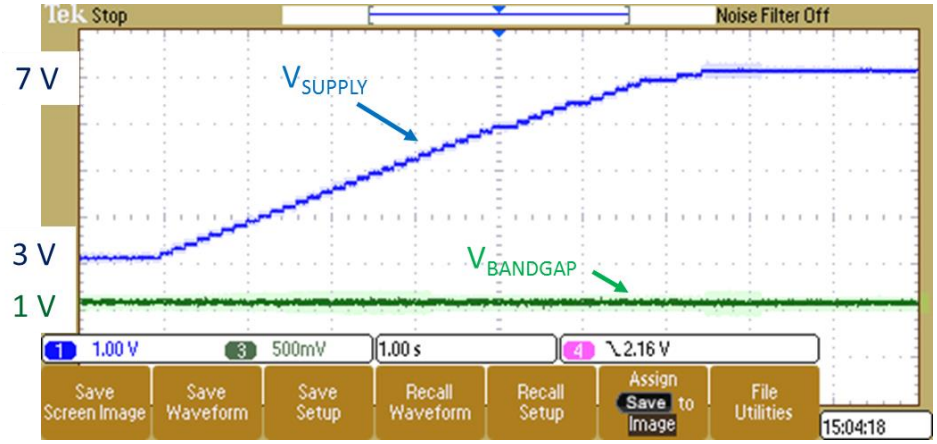

Fig. 84 Waveforms of tested bandgap voltage reference. Respectively: supply voltage (blue), voltage reference output (green)

Referring to Fig. 84, the blue signal is the power supply, while the green signal is the bandgap output. Supply voltage is dynamically varied from 3 to 7 Volt, while bandgap voltage is proved to keep a constant value of 1.05 Volt as expected, in line with schematic simulations. Correct behavior from 7 Volt to 12 Volt power supply was verified as well.

After a preliminary analysis of specific sub-circuits, the overall functionality of the DC/DC converter with degradation detection capability was tested. Referring to architecture described in Fig. 68 and Fig. 82, integration and sampling procedures are verified using a 470 µH inductor and two resistors of 390 Ω and 309 kΩ for respectively *R1* and *R2*. Measured waveforms are presented in Fig. 85.

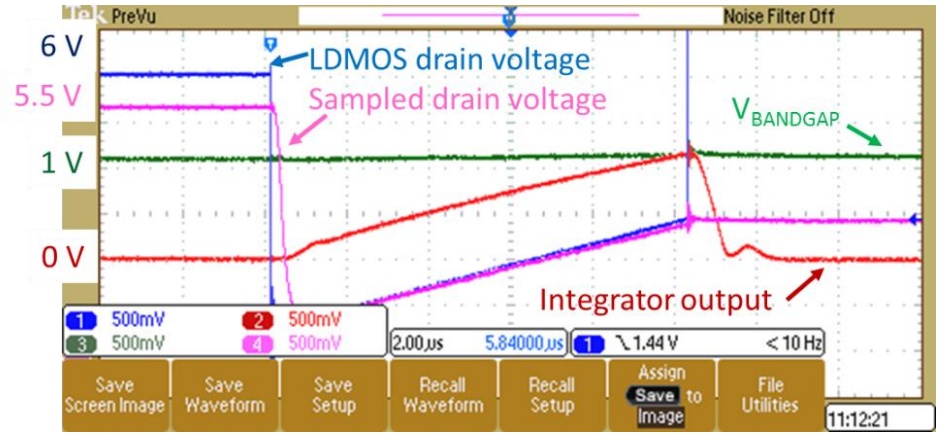

Fig. 85 Waveforms of tested monitoring circuit for degradation detection. Respectively: bandgap voltage reference (green), integration circuit output (red), drain voltage of monitored LDMOS (blue), sampled value of monitored LDMOS drain voltage (pink) to be compared with predefined reference

Referring to Fig. 85, the blue signal is the drain voltage of power MOS, the pink signal is the sampled value of the drain voltage of power MOS, which is used to detect degradation, the red signal is the integrator output while the green line is bandgap reference.

As expected, the integration signal linearly increases till it reaches a predefined threshold, which is generated through the internal bandgap reference. In this phase an increasing current is flowing inside the power MOS so that its drain voltage linearly increases due to its intrinsic on-resistance. At the same time, the sampling value follows the drain voltage value. When integration signal is equal to bandgap reference, a known current is flowing in the power MOS (about 50 mA in this test case), and power MOS is switched off. Simultaneously, the value of its drain voltage is correctly sampled and held and is available for evaluation. With the adopted values of external resistances and inductor, a switching frequency of about 65 kHz is obtained with a power supply of 3 Volt, while output voltage clamped at 5.6 Volt by Zener diode.

Waveforms related to control signals using a 10 mH inductor and two resistors of 6.2 kΩ and 6.2 MΩ for respectively R1 and R2 are shown in Fig. 86. Blue signal is drain voltage of power MOS, green signal is the output of zero crossing comparator ($Comp_{ZCS}$ in Fig. 73, C_{b1} in Fig. 82) and red signal is the output of integration comparator (C_1 in Fig. 68, C_{a1} in Fig. 82).

As expected, the *ON phase* during which the inductor is charged starts exactly when comparator C_{b1} (green) rises to logic value one, this meaning that current inside inductor is approximately zero. On the contrary, *ON phase* ends when comparator C_{a1} (red) is asserted, this meaning that desired current is actually flowing inside power MOS. Referring to Fig. 85, this happens as soon as integration signal reaches the bandgap reference value. In this case, a switching

frequency of about 2 kHz is obtained with a power supply of 3 Volt, while output voltage clamped at 5.6 Volt by Zener diode.

Additional tests were performed with different input and output voltages, including supply voltages up to 8 Volt, and output voltages up to 20 Volt (without Zener diode)

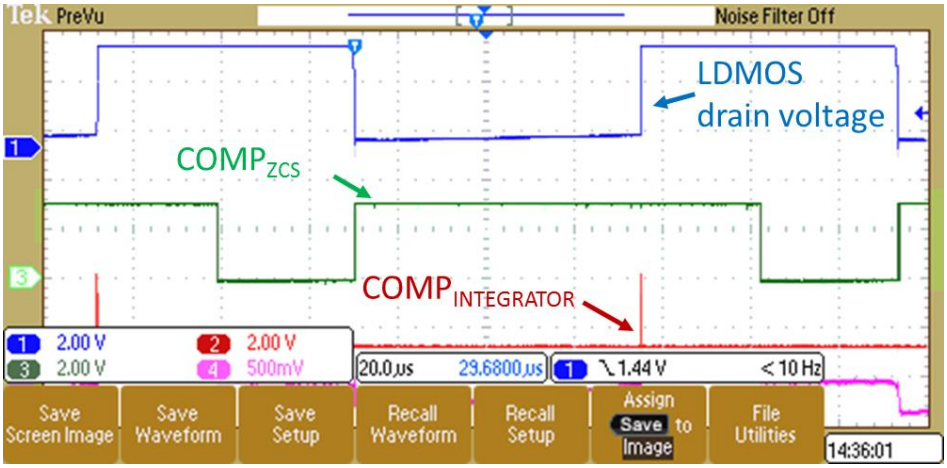

Fig. 86 Waveforms of control signals of proposed DC/DC converter. Respectively: drain voltage of monitored LDMOS (blue), output of ZCS comparator (green), output of integrator comparator (red)

In summary, dedicated tests were performed on specific elements of design and on overall behavior of DC/DC converter, along with circuits for degradation monitoring. Measured results are mainly compliant with simulated ones, and expected functioning was verified.

More precisely, measurements performed on single blocks of design are in line with simulated results, especially for what concerns the bandgap voltage reference and the digital control. Referring to high voltage regulators, an unexpected delay in high-to-low transition is observed, which can impact on the maximum switching frequency of the converter. Nevertheless, the transition sensed by the digital block to drive the switching activity is the low-to-high transition, which on the contrary has a correct timing. As a consequence, main functionality of DC/DC converter and degradation monitoring is not substantially affected by this delay.

Besides targeted tests on single sub-blocks, the overall functionality of prototype was verified. Normal operation was tested with two different subsets of values of external passive components, verifying correct operation at different switching frequencies. Moreover, the architecture proposed for sensing the degradation level of power MOS was validated too. DC/DC converter is properly instructed to switch the MOS at a predefined level of flowing current, by comparing the output of the embedded integrator with a reference value. On

the other hand, sampling circuit is proved to hold the actual value of the drain voltage of power MOS in the correct time window, so that it can be compared with a reference value in order to evaluate the degradation by mean of the variation of its on-resistance. Finally, all tests was performed at different input voltages, ranging from 3 to 12 Volt, in order to verify the design of the high voltage modules.

Chapter 6

Conclusions

With the evolving of new scenarios in the development of Internet of Things (IoT) nodes, new needs are emerging in the field of power management architectures, especially for what concerns lifetime, durability and robustness. High-efficiency converters are necessary in order to effectively extract power from different energy sources, which can be either harvesting sources (e.g. RF, photovoltaic, thermoelectric, etc.) or storage elements (e.g. electrochemical cells etc.) so improving system lifetime. Equally important, developing dedicated circuits which are able to overcome durability issues associated with specific sources is another key aspect to be investigated. For example, electrochemical cells suffer from high impulsive discharging profiles, which are commonly generated in switching DC/DC converters. Differently, if degrading conditions cannot be avoided, monitor techniques can be successfully adopted, in order to provide a suitable information about the state of health of the system, which can be potentially used to compensate the effects of degradations.

This thesis aimed at studying these different aspects of lifetime, durability and robustness in IoT power management, and to provide specific solutions in this field of research.

As a first contribution, three different integrated converters are proposed, implementing a unique idea with different architectures. The objective of this work was to design a DC/DC converter with enhanced reliability for battery-supplied systems. Current researches show how highly impulsive current discharge profiles can be detrimental to the end-of-life of electrochemical cells, being such profiles typical of common switching converters. In the presented solution, with the introduction of a decoupling stage between the input source (i.e. the battery) and the actual switching stage, the profile of the current drawn from the battery is effectively regulated, so that a constant, flat value is always required without any peak, with an improvement of the battery lifetime. In a first implementation, a programmable current regulation is designed, in order to provide a flexible solution able to adapt to different levels of power requirements from the connected load. In a second implementation, a more efficient solution is proposed, with same current shaping capability but featuring a stepwise energy transfer between the decoupling stage and the output load. Thanks to this stepwise implementation, a higher transfer efficiency can be obtained, following the concept of adiabatic capacitor charging. A third solution is presented, which implements the same architecture in an ultra-low power scenario, with specific circuit solution, like for example dynamic biasing, in order to obtain a quiescent current consumption below one microampere. All three solution were designed and physically implemented, and preliminary tests proves the correct functionality of the proposed architecture.

Concerning high-performing IoT nodes, an advanced solution is presented of a fully autonomous node with radio-frequency (RF) energy harvesting and standard communication protocol. An innovative adaptive power management section was designed, able to constantly monitor the amount of energy actually available and to dynamically change the behavior of the node (i.e. data-rate, sleep policy of microcontroller, etc.), in order to obtain high operative ranges while always providing the best feasible data-rate. Solution was proven to operate at up to 17 meters and adaptive mechanism was successfully tested.

In the field of monitoring circuits for lifetime and durability of IoT systems, a first contribution regards the development of a specific algorithm for detecting the efficiency of a maximum-power-point-tracking (MPPT) in indoor photovoltaic applications. In this scenario, fractional-open-circuit-voltage (FOCV) mechanism is commonly used to implement MPPT, relying on the idea that maximum power point is a precise fraction of the open circuit voltage of the panel. The proposed algorithm is able to reconstruct the actual characteristics of the panel by means of the signal already available within the normal operation of the DC/DC converter, and to detect if the MPPT mechanism is either working properly or has degraded for any reason, and to report this information to the user

A further solution is presented of a reliability-aware DC/DC converter architecture, which is capable to monitor the actual state of health of power switches, which are commonly subject to various aging effects and in particular to hot-carrier degradation (HCD). The principal side effect that can be observed due to this kind of degradation is the increasing of the on-resistance of the power switches over time. In the proposed architecture, additional circuits are provided which constantly monitor the on-resistance during normal operations in a runtime scenario, without affecting the performances of the DC/DC converter. Thanks to this information, compensatory action may also be taken into account in order to counterbalance the augmented power losses due to the increased resistance.

The proposed work opens several perspectives in the research field of power management for IoT applications. Concepts like autonomous harvested nodes, adaptive systems, maintenance-free devices, have just become a consolidated reality in the world of electronics, while new challenges concern the improvement of lifetime, durability and robustness of such systems. The emerging aspect of this research is that a successful approach is to combine on one hand dedicated architectures to enhance durability of specific elements of IoT systems (e.g. batteries, DC/DC converters, etc.), and on the other hand to improve overall efficiency, which is always a crucial point especially with regard to harvesting systems. Designing solutions able to achieve both those goals is a promising research field which has been investigated in this thesis and which offers interesting prospects for future works.

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