Alma Mater Studiorum – Università di Bologna

DOTTORATO DI RICERCA IN INGEGNERIA ELETTROTECNICA
XXIX CICLO

Settore Concorsuale di afferenza: SC 09/E1 – Elettrotecnica
Settore Scientifico disciplinare: SSD ING-IND/31 – Elettrotecnica

Theoretical and Experimental Analysis of Output Power Quality in Single-Phase Cascaded H-Bridge Multilevel Inverters

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Esame finale anno 2017

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Acknowledgement

It is my uttermost honour to express my gratitude to all people who have been the part of my research during the PhD studies at the University of Bologna.

First of all, my huge gratitude goes to my family who has been endlessly and constantly supporting and encouraging me since I started my education, sharing with me all my nice and less nice moments. Without their strong and altruistic support I would not have been able to successfully complete my PhD research work.

My deepest gratitude goes to my supervisor, Professor Gabriele Grandi, who has straightforwardly supported me with my research ideas, selflessly helped me with all issues we have had during my studies and humanly encouraged me during weak moments to overcome them and to powerfully and decisively carry on. His supervision at the high academic level together with his immense technical knowledge has been extremely appreciable and useful. The results obtained during my research work should be also addressed to his patient and professional supervision and our strong scientific cooperation. I am looking forward to continuing our collaboration at the high academic and professional level in the future.

I would like to thank my PhD coordinator Professor Domenico Casadei who has been with us PhD students all the time and who has always given many technical comments on my work and evaluated it as the good one. Also, I would like to thank Professor Claudio Rossi for sharing his technical knowledge and for providing the laboratory facilities for the experimental purposes.

I would like to thank Professor Alexander Ruderman and Professor Yakov L. Familiant from the Power Electronics Research Laboratory, Nazarbayev University, Kazakhstan, and Professor Boris Reznikov, General Satellite Corporation, Saint Petersburg, Russia, for a thorough and professional cooperation, support and help with detailed and enormous analytical and numerical developments in our research field.

I would like to thank Professors Vanja Ambrožič and Peter Zajec from the Faculty of Electrical Engineering, Department of Mechatronics, University of Ljubljana, Slovenia, for accepting me as a visiting PhD student, for hosting me during my three-months research period abroad at their Department and for supporting and working with me on a specific power configuration.

I wish to thank two department technicians, electrical engineers Marco Landini and Matteo Marano for sharing with me their technical experience and advising me for specific technical issues that I have faced realizing and designing different power electronics configurations.

One big thank goes to Dr. Jelena Lončarski from the Department of Engineering Sciences, Division of Electricity, Uppsala University, Sweden, for helping me with some issues at my first steps in Bologna and for sharing a scientific knowledge and cooperating with my research group considering different research topics.

I wish to express my sincere appreciation for the support I have received during my PhD studies as a fellow of the Institute of the Advanced Studies (ISA). Its coordinator Dr. Barbara Cimatti is a compassionate and responsible person who has been cooperating with all students at the Institute at a high professional and academic level. The hospitality of the ISA Institute has been positively far-reaching and useful for me from academic, professional and personal points of view. Having such an institution at the University of Bologna is a real privilege.

All in all, it has been a huge privilege to be with the Department of Electrical, Electronic and Information Engineering ‘‘Guglielmo Marconi’’, University of Bologna. Collaborating with all professors and colleagues, and sharing the same willingness have been priceless for me.

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Abstract

In this thesis simple closed-form asymptotic solutions for estimating the output power quality in single-phase cascaded H-bridge multilevel inverters are presented for staircase modulation technique and pulse-width modulation (PWM) technique. The analysis is carried out in the time domain considering the whole harmonic content and being used for an arbitrary inverter level count.

In case of the staircase modulation technique, the voltage and current ripple normalized means square (NMS) expressions are obtained in time domain considering the fundamental period. Voltage and current total harmonic distortions (THDs) as a function of the corresponding NMS values are defined as constrained optimization ones. Optimizing the voltage and current THDs determines the voltage and current optimal switching angles over the modulation index range. The current THD is understood as voltage frequency weighted THD that assumes a pure inductive load, but it is practically accurate for inductively dominant *RL*-loads. The same approach for estimating the current quality is given for a grid-connected inverter.

In the case of the PWM technique, the voltage and current THDs are estimated supposing that the ratio between switching and fundamental frequencies is (infinitely) large (asymptotic assumption). The voltage and current ripple normalized mean square (NMS) values are obtained in time domain by double integration of their normalized squared ripples over the switching and fundamental periods. They present piecewise continuously differentiable analytical solutions with only elementary functions and can be understood as the time-domain equivalent of the frequency-domain double Fourier transformation. The direct relation between the voltage and current NMS values and their qualities is presented. Considering the same approach, the current THD evaluation in case of a grid-connected system is presented.

Besides analytical developments, simulation and experimental verifications for three-level (one H-bridge), five-level (two cascaded H-bridges) and seven-level (three cascaded H-bridges) single-phase inverters are analysed, presented and compared in details.

Preface

My background

During my bachelor and master studies at the Department of Power Systems, School of Electrical Engineering, University of Belgrade, I was always a philomath trying to theoretically understand, practically experience and efficiently learn new topics related to the field of electrical engineering as well as to some other fields. Every new subject came as a challenge for me to discover and learn something new. Doing so, I was one of inquisitive students. Meanwhile, my desire to be involved in research appeared and the first research steps competed in my eclecticism towards different topics where I would try to approach each study problem from different aspects. As time was going by, my research interests were gradually tapering towards renewable energy and power systems due to some interesting subjects and lectures carried out at the Department. This helped me choose the subjects for my bachelor and master thesis that I successfully defended in July 2011 and September 2012, respectively. Both were based on the aforementioned topics where I improved my academic and research skills, and so I received the title Master Engineer of Electrical Engineering and Computer Science.

My devotion to science helped me make one step more and I came to the University of Bologna, at the Department of Electronic, Electrical and Information Engineering ‘‘Guglielmo Marconi’’, where I started working with my supervisor Professor Gabriele Grandi in the field of Power Electronics. I found the Department as a perfectly suitable place to carry out my research activities, to extend my knowledge and to gain a new international and academic experience. Apart from this, living in a new place and meeting new people from different countries and different fields have put my international, social and interdisciplinary skills at a higher level.

Spending many hours theoretically analyzing developments in my field, simulating different problems, trying to experimentally implement our research ideas and to prove the correctness and effectiveness of them successfully helped me to write my doctoral dissertation and to give a contribution, locally to my specific research area and globally to the field of electrical engineering.

Motivation for research

Nowadays, new and up-and-coming technologies exponentially bring new requirements from many points of view. This trend specially affects the field of electrical engineering and furthermore the field of power electronics in terms of reliability, flexibility and general possibilities to meet all needs that are supposed to be efficiently and unmistakably provided. Among a variety of specific subparts inside the field of power electronics, the energy conversion plays a very important role. In order to properly, efficiently and precisely convert one kind of electrical energy into another one, specific power electronic topologies are used. What kind of topology should be used mainly depends on an application which it is applied for. If the control of three-phase ac motor is needed, a three-phase inverter, which converts dc voltage into the ac one, can be used, or if there is a PV panel with its dc output voltage, then the single-phase structure such as an H-bridge inverter can be considered.

Using power electronic configurations brings some significant cons which must be considered as well. The common mismatch between desired and real waveforms, usually voltages and currents, comes from the fact that the relevant parameters with their defined waveforms are not as perfect as they are theoretically supposed to be. This means that, regarding the standard electrical grid, voltages and currents should be sinusoidal with as less as possible additional disturbances and distortions. In case of the presence of some distortions, the connected power electronic configurations ‘‘dirties’’ the electrical grid increasing the total harmonic distortion (THD) and overall losses in the grid and in the configuration itself. This phenomenon generally competes in power quality. If we consider ac motors in terms of their proper supply and control, distortions of voltages and currents increase losses inside them and additionally heat them up. This is usually the case for every power conversion independently of the rated power. All aforementioned facts require appropriate systems, able to provide output power with low harmonic contents, keeping at the same time all characteristics, which define the efficiency and reliability of them, at standard levels. Multilevel inverters have taken increasing scientific attention in the last years due to their positive feedback on those requirements.

This thesis deals with the analysis of single-phase multilevel inverters. Single-phase multilevel inverters have many practical advantages which are used in many real applications such as renewable energy sources (photovoltaic, wind, fuel cells), or applications which the reactive power compensation is needed for. Their modularity brings the possibility of increasing the number of the output voltage levels having several isolated dc bus voltages. Having more output voltage levels means that the voltage excursion in between those levels is smaller compared with an inverter with the same maximum output voltage but less output voltage levels.

As a result, this brings some main pros: the voltage THD, which refers to the fundamental component of the voltage compared to the full voltage waveform, is significantly reduced, power switches can be designed to withstand lover voltage stresses, the total power of the system is increased and in some cases transformers and synchronizing switching devices can be omitted. One drawback of this structure is that the dc bus voltages must be completely isolated without sharing the common ground connection. The output current is fully affected by the output voltage which means that having smaller steps in between voltage levels causes smaller current switching variations, so-called current ripples, and therefore reducing the total current harmonic distortion.

In other words, analysing single-phase multilevel inverters in terms of power quality presents an important challenge and issue due to many requirements given by new technologies and developments. It also presents a basis for analysing three- and more phase systems, since a single-phase inverter can be seen as one phase of a multiphase structure.

Research objectives

The main objective of this dissertation is the detailed theoretical analysis of the power quality in single-phase multilevel inverters considering the whole harmonic content, and regarding different modulation techniques and different power configurations. Apart from that, simulation and experimental verifications as a proof of the analytical correctness, numerical effectiveness and practical applicability of the proposed analysis represent the essential parts as well.

More precisely, the objectives are focused on the following:

1) Detailed analysis of single-phase multilevel H-bridge inverters in terms of power configuration and different modulation techniques – staircase modulation technique and pulse-width modulation (PWM) technique;
2) Design and realization of the experimental setup for a single-phase multilevel H-bridge inverter in the laboratory, controlled by two modulation techniques and supplying different loads;
3) Analytical developments of output voltage and output current ripples based on their normalized mean square values in case of the staircase modulation technique. Definition of voltage and current optimal switching angles and their direct correlation with voltage and current total harmonic distortions (THDs) for an arbitrary inverter level count with the inductively dominant load. Current quality in case of a grid-connected inverter;
4) Analytical developments of the output voltage and output current ripples based on their normalized mean square values in case of the unipolar PWM technique using the constant (dc) and sinusoidal (ac) modulating signals. Estimations of the voltage and current total harmonic distortions (THDs) and their direct correlation with corresponding NMS values in case of the sinusoidal modulating signal, for a single-phase n-level inverter connected to the inductively dominant load. Current quality in case of a grid-connected inverter;
5) Simulation analyses of different H-bridge configurations in terms of modulation technique, number of cascaded H-bridges and kind of load;
6) Comprehensive analysis and comparison of all analytical, simulation and experimental results for both modulation techniques.

1 Introduction

1.1 Multilevel inverters

Using renewable energy is increasing due to environmental difficulties with other kinds of energy sources and especially due to the lack of fossil fuels. On the other hand, the need for different kinds of energies is increasing rapidly as well as the number of devices which efficiently need them. Considering this, the research society pays high attention to multilevel inverters and their efficient usage. One multilevel inverter usually presents a system consisting of power semi-conductors properly connected in order to provide the specific required electrical and electromagnetic characteristics. Due to aforementioned facts multilevel inverters are widely used for medium/high voltage applications. They are capable of generating voltage and current waveforms with improved quality, providing a nominal power increase and having a modular structure, therefore they are applicable to many practical applications such as transport (powering trains, ships, automobiles and other drives), energy conversion (wind, solar), manufacturing and mining [1.1]–[1.3]. There are many different topologies of multilevel inverters that can be used regarding what they are supposed to meet and which application they should be used for. Amongst them the most popular ones are diode-clamped (neutral-point clamped), capacitor-clamped (flying capacitor) and cascaded ones with isolated input dc voltage sources [1.4]–[1.9].

In general, multilevel converters have some advantages compared to their conventional counterparts. Some of them compete in generating output voltages with very low distortion and decreasing *dv*/*dt* stress, thereby electromagnetic disturbances are reduced. This is specially emphasised in case of pulse-width modulated multilevel inverters. Input and output currents of this kind of inverter are with lower distortions as well. Apart from this, multilevel inverters produce a smaller common-mode voltage therefore the stress in motor bearings can be diminished and in some cases it can be eliminated using some modulation strategies. They can operate at fundamental and high switching frequency, taking into account that the higher switching frequency is, the higher switching losses are and the lower the efficiency is. Nevertheless, multilevel inverters have some disadvantages such as an increased number of power switching components and an increased number of gate drive circuits. In this case the complexity of the overall system is higher as well as the total cost of it [1.10].

Diode-clamped inverters consist of power switches and diodes properly connected and supplied by dc voltage divided into smaller ones. In *n*-level diode-clamped inverters a capacitor balance issue represents one of the most important requirements.

The total dc-bus voltage is divided into smaller voltage levels using (n−1) capacitors connected in series to generate stepped output waveforms [1.11]. In this case an unequal voltage sharing among the clamping diodes can appear. This is specially emphasized in high-voltage applications where an unequal voltage distribution in the capacitors can damage diodes and power switches, and also generate output voltage harmonics [1.7]. This phenomenon represents a main challenge which can be solved by using an isolating transformer or introducing some additional circuits [1.12], but these solutions increase the complexity of the system. One suggested solution was presented in [1.13] where a space vector modulation (SVM), based voltage balancing strategy for a new five-level multiple-pole multilevel diode-clamped inverter topology, is used to eliminate the voltage drift phenomena. Diode-clamped inverters can be controlled by using a space vector PWM modulation which can help balance dc bus voltages and improve output voltage [1.14]. Another possible technique is a carrier-based PWM technique. In case of three-phase system with a higher power, it is possible to inject a common ninth harmonic zero-sequence voltage on each of the three-phase reference voltages in a low-modulation-index region to mitigate magnetic-flux fluctuation on the input side of the inverter and to make uniform power losses [1.15]. One advantage of this kind of topology is sharing a common dc bus among all phases, which minimizes the capacitance requirements of the converter. For this reason, a back-to-back topology is not only possible but also practical for uses such as a high-voltage back-to-back interconnection or an adjustable speed drive. Apart from this, the capacitors can be pre-charged as a group and the efficiency is high for fundamental frequency switching. Disadvantages compete in the fact that the real-power flow is difficult for a single inverter because the intermediate dc levels will tend to overcharge or discharge without precise monitoring and control. The number of clamping diodes required is quadratically related to the number of levels, which can be cumbersome for units with a high number of levels [1.10].

Capacitor-clamped inverters consist of power switches and capacitors properly connected and supplied by dc voltage divided into smaller ones. They present important parts in many different applications. One of them is a power factor correction in single-phase ac/dc/ac inverters to achieve a power factor correction in the ac/dc side and to generate a sinusoidal voltage in the dc/ac side to the load [1.16], [1.17]. In wind power systems a capacitor-clamped inverter together with super capacitors operating under variable voltage conditions can be used to mitigate short term power fluctuations [1.18]. In this case the overall efficiency is increased taking into account the super capacitor voltage variations. For azimuth thrusters, capacitor clamped inverters can be used to absorb load transients and thereby to prevent the transient propagation onto the shipboard power systems.

By using a modified space-vector PWM techniques it is possible to provide a desired current at the output current and keep the THD level at the low level under unbalanced conditions [1.19]. Flying-capacitor-clamped five-level inverter was presented in [1.20] with the switched-capacitor circuit with dc-dc boosting conversion ability being controlled by the optimized carrier-based phase disposition pulse width modulation method. In this case the number of switches and capacitors is decreased compared to the conventional cascade multilevel inverter due to the special composite structure, the voltage of dc-link capacitor can be self-balanced under the proposed control strategy and the switching losses are reduced. An improvement in the output voltage quality was presented in [1.21] using a hybrid multilevel inverter consisting of a three-phase three-level diode-clamped inverter and H-bridge cells controlled by staircase and PWM techniques together. Advantages of this kind of inverter are phase redundancies which are available for balancing the voltage levels of the capacitors, controllable active and reactive power flow and the large number of capacitors enables the inverter to work during short duration outages and deep voltage sags. Disadvantages present the facts that the control to track the voltage levels for all capacitors and pre-charging all of them to the same voltage level is complicated, switching utilization and efficiency are poor for real power transmissions and the large number of capacitors are both more expensive and bulky than clamping diodes in multilevel diode clamped converters. In this concern, packaging is also more difficult in inverters with a high number of levels [1.10].

Cascaded H-bridge multilevel inverters are used in a relatively same way as the previous two topologies. Each H-bridge cell of one cascaded multilevel inverter has its own isolated dc bus voltage supply V_{dc}. In this case it is able to provide three voltage levels at the output ($+V_{dc}$, 0, $-V_{dc}$), therefore N H-bridges provides $n=2N+1$ output voltage levels. The number of output voltage levels is always odd due to the presence of the zero level. Thanks to the modularity of this kind of inverter voltage stress on power switches is decreased, the excursion between adjacent levels of the output voltage is lower, the maximum output voltage is increased and therefore the power quality is improved. Cascaded H-bridge inverters can operate as a standalone single-phase system or as one phase of a multiphase system. For every number of phases different load can be considered, while in case of grid-connected systems single and three-phase inverters are used. An improved cascaded configuration with a maximum of nine-level output voltage waveform with a reduced number of power components was presented in [1.22]. This topology, controlled by PWM technique, was compared with classical cascaded H-bridge inverters and some other multilevel topologies over a wide modulation index range where the improvement of the output voltage quality was shown.

Another modified cascaded topology suitable for a grid-connected photovoltaic system was presented in [1.23] together with experimental verifications, with a wide operation range, low grid current total harmonic distortion and high efficiency. It operates in inverter mode when the output voltage and power of the photovoltaic system are low, and transforms into H-bridge mode when the same output voltage and power are high. This possibility is provided using a bidirectional power switch.

A five-level staircase modulated single-phase inverter interfacing with photovoltaic modules with five power switches and reduced total harmonic distortion and electromagnetic interference was presented in [1.24]. A multitask asymmetrical cascaded three-phase H-bridge multilevel inverter suitable for micro-grid systems possibly supplying unbalanced and non-linear load is given in [1.25]. The main advantage of this inverter was the possibility to produce a staircase output voltage having unequal dc bus voltage such as a voltage coming from photovoltaic cells. A flexible control strategy based on a frequency response for following the reference commands was successfully demonstrated. Advantage of this topology is the fact that the number of possible output voltage levels is more than double than the number of dc isolated supplies while the series of H-bridges brings a high modular feature. On the other side, separate dc sources are required for each H-bridge and it can limit its applicability to products that already have multiple dc isolated sources readily available [1.10].

1.2 Outlines and original contribution of dissertation

This dissertation is divided into the following major chapters and the original contribution is provided by chapters 2–4:

Chapter 2: A general overview of cascaded single- and three-phase multilevel H-bridge inverters is given considering their use in real applications depending on the purpose, rated power and working conditions. Circuit topologies for single-phase cascaded H-bridge inverters are introduced presenting their basic characteristics such as the number of output voltage levels. Experimental design and implementation of three topologies consisting of one H-bridge, two and three cascaded H-bridges is described in detail considering all parts of the complete experimental setup.

Chapter 3: The staircase modulation technique for controlling single-phase cascaded multilevel inverters is given. Theoretical considerations and time-domain analytical calculations of optimal output voltage and current total harmonic distortions based on the normalized mean square (NMS) ripple values are presented. NMS values are calculated using the optimal voltage and current switching angles (Matlab/*fmincon* optimization function) for each modulation index m. An inductively dominant passive *RL*-load and a grid-connected system considering all switching harmonics are taken into account, being supplied by an n-level single-phase inverter. Detailed comparison between the simulation (Matlab/Simulink), analytical, and experimental results for the voltage and current qualities are presented in case of passive *RL*-load. In case of grid connection the current quality is considered comparing analytical and simulation results. All comparisons show the correctness of the proposed method.

Chapter 4: The pulse-width modulation technique (PWM) for controlling single-phase cascaded multilevel inverters is presented. Based on the normalized mean square ripple values calculated in the time domain over the switching and fundamental periods and following an assumption of using an inductively dominant load, closed-form piecewise analytical solutions of output voltage and current total harmonic distortions of a single-phase n-level inverter are presented considering all switching harmonics. The voltage THD as a function of inverter level count n and modulation index m is derived as well as the current THD including additionally the load parameters. Apart from the inductively dominant passive *RL*-load, the current THD is evaluated in case of a grid-connected system. A comparison between the simulation (Matlab/Simulink) and the analytical results is presented in case of grid connection, and together with experimental results in case of the passive *RL*-load, for three different configurations. Simulation and experimental results show the correctness of the analytical developments.

1.3 References

[1.1] J. Rodríguez , L.G. Franquelo, S. Kouro, J. I. Leon, R. C. Potrillo, M. Á. M. Prats and M. A. Péres, "Multilevel Converters : An Enabling Technology for High-Power Applications," *Proc. IEEE*, vol. 97, no. 11, pp. 1786–1817 2009.

[1.2] H. Abu-rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-Voltage Multilevel Converters – State of the Industrial Applications," *IEEE Trans. Ind. App.*, vol. 57, no. 8, pp. 2581-2596, 2010.

[1.3] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Pérez, and J. I. Leon, "Recent Advances and Industrial Applications of Multilevel Converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, 2010.

[1.4] J. Rodríguez, J. Lai, and F. Z. Peng, "Multilevel Inverters : A Survey of Topologies , Controls , and Applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, 2002.

[1.5] J. Rodríguez, S. Bernet, B. Wu, J. O. Pontt, S. Kouro, "Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, 2007.

[1.6] L.G. Franquelo , J. Rodríguez, J. I. Leon, S. Kouro, R. Portillo, and M. Á. M. Prats, "The Age of Multilevel Converters Arrives," *IEEE Ind. Electron. Mag.*, vol. 2 , no. 2, pp. 28–39, 2008.

[1.7] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A Survey on Neutral-Point-Clamped Inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219–2230, 2010.

[1.8] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Pérez, "A Survey on Cascaded Multilevel Inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2197–2206, 2010.

[1.9] D. G. Holmes and T. A. Lipo, Pulse Width Modulation for Power Converters: Principles and Practice. Hoboken, NJ: Wiley, 2003.

[1.10] M. H. Rashid, "Multilevel Power Converters," in *Power Electronics*, 3rd ed., Amsterdam, the Netherlands, Elsevier, 2011, ch. 17, pp. 455–486.

[1.11] A. Nabae, I. Takahashi, and H. Akagi, "A New Neutral-Point-Clamped PWM Inverter," *IEEE Trans. Ind. App.*, vol. IA-17, no. 5, pp. 518–523, 1981.

[1.12] T. Ito, Y. Sato, M. Kamaga, H. Ohashi "An Investigation of Voltage Balancing Circuit for DC Capacitors in Diode-Clamped Multilevel Inverters to Realize High Output Power Density Converters," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, Atlanta, GA, USA, 2010 pp. 3675–3682.

[1.13] P. H. Raj, A. I. Maswood, G. H. P. Ooi, and Z. Lim, "Voltage balancing technique in a space vector modulated 5-level multiple-pole multilevel diode clamped inverter," *IET Power Electron.*, vol. 8, no. 7, pp. 1263–1272, 2015.

[1.14] G. P. Adam, S. J. Finney, O. Ojo, and B. W. Williams, "Quasi-two-level and three-level operation of a diode-clamped multilevel inverter using space vector modulation," *IET Power Electron.*, vol. 5, no. 5, pp. 542–551, 2012.

[1.15] K. Hasegawa, and H. Akagi, "Low-Modulation-Index Operation of a Five-Level Diode-Clamped PWM Inverter With a DC-Voltage-Balancing Circuit for a Motor Drive*," IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3495–3504, 2012.

[1.16] B. Lin and C. Huang, "Single-phase AC / DC / AC converter based on capacitor clamped topology," *IEE Proc. – Electric Power App.*, vol. 152, no. 3, pp. 464–472, 2005.

[1.17] B. Lin and C. Huang, "Single-Phase Converter with Flying Capacitor Topology," in *IEEE Region 10 Conference (TENCON)*, Chiang Mai, Thailand 2004, pp. 73–76.

[1.18] S. D. G. Jayasinghe, D. M. Vilathgamuwa, and U. K. Madawala, "An Analysis on the Possibility of Using Capacitors of a Three-Level Capacitor Clamped Inverter as Power Smoothing Elements for Wind Power Systems," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, Phoenix, AZ, USA, 2001, pp. 2963–2970.

[1.19] S. G. Jayasinghe, D. Mohammadi, and M. Vilathgamuwa, "Capacitor-Clamped Inverter Based Transient Suppression Method for Azimuth Thruster Drives," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, USA pp. 2813–2820, 2016.

[1.20] L. He and C. Cheng, "A Flying-Capacitor-Clamped Five-Level Inverter Based on Bridge Modular Switched-Capacitor Topology," *IEEE Trans. Ind. Electron.*, vol. 63, no. 12, pp. 7814–7822, 2016.

[1.21] H. Sepahvand, M. Ferdowsi, M. Khazraei, K. Corzine, "A Hybrid Multilevel Inverter with Both Staircase and PWM Switching Schemes," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, Atlanta, GA, USA, 2010, pp. 4364–4367.

[1.22] C. I. Odeh, E. S. Obe, and O. Ojo, "Topology for cascaded multilevel inverter," *IET Power Electron.*, vol. 9, no. 5, pp. 921–929, 2016.

[1.23] F. Wu, X. Li, F. Feng, and H. B. Gooi, "Modified Cascaded Multilevel Grid-Connected Inverter to Enhance European Efficiency and Several Extended Topologies," *IEEE Trans. Ind. Informat.*, vol. 11, no. 6, pp. 1358–1365, 2015.

[1.24] V. S. K. Devi, R. H. Patrao, P. S. Sreekanth, G. Ramole, and A. Sreekumar, "Implementation of Staircase Modulation on a Five Level Cascaded H-Bridge Multilevel Inverter and Interfacing with Photovoltaic Modules," in *International Conference on Power and Advanced Control Engineering (ICPACE)*, Bangalore, India, 2015, pp. 185–190.

[1.25] A. Mortazaei, M. G. Simões, A.S. Bu Bshait, T. D. Curi Busarello, F. P. Marafão, and A. Al Durra "Multifuncional Control Strategy for Asymmetrical Cascaded H-bridge Inverter in Microgrid Applications," in *IEEE Industry Applications Society Annual Meeting (IAS)*, Dallas, TX, USA, 2015, pp. 1–8.

2 Single-phase cascaded H-bridge multilevel inverters

2.1 Introduction

Single-phase and three-phase cascaded H-bridge multilevel inverters are extensively used in many different applications due to their modular and power characteristics. Single-phase cascaded inverters can be used for single-phase controlled rectifiers in railway traction drive systems where with a proper control and calculations overall performances can be improved including an enlarged operation range and a more precise estimation of the instantaneous active and reactive power [2.1]. For grid-connected applications a single-phase H-bridge voltage source is used where the average current control technique brings the maximum power point tracking and a possibility of having a low distortion and high power output current factor [2.2]. H-bridge inverters are found in uninterruptible power supply (UPS) systems use as well. They are used for critical loads in telecommunication, data storage and life support systems. Using UPSs, it is important to follow the references and to have a good immunity for load disturbances. In this case, optimal feedback controls, which have to comply with IEC 62040-3 Standard, has been studied bringing new technical solutions and improvements in order to always have an uninterruptable power flow [2.3].
For grid-connected and stand-alone transformerless photovoltaic systems, applying different PWM techniques to cascaded multilevel inverters minimizes a problem of having a PV array leakage current as well as common mode voltages [2.4]. Thanks to the PWM technique, electromagnetic interferences requirements are satisfied as well.

Three-phase multilevel inverters, controlled by different PWM techniques where its each phase consists of properly cascaded H-bridges or a similar configuration can be used in electrical drives with a higher power [2.5], [2.6]. In case of renewable energy sources, specifically for photovoltaic systems (PV) connected to the electrical grid, three-phase cascaded multilevel inverters are used. Some modular hybrid configurations with a staircase modulation technique can reduce the number of power switches, total losses and switch voltage stress [2.7]. Connecting one PV system as a three-phase one to the electrical grid brings a possible leakage current between three phases, which can be reduced properly handling the common mode voltage with a relation to the leakage current using the PWM technique. This presents an important issue [2.8].

In the next section a circuit topology of a single-phase cascaded H-bridge inverter will be presented since it is the main configuration considered in this thesis.

2.2 Circuit topology of a single-phase cascaded H-bridge inverter

The basic well-known topology of a single-phase dc/ac converter, consisting of one H-bridge with four power transistors (switches) and dc voltage supply V_{dc}, with a passive *RL*-load and a possible connection to the electrical grid is presented in Figure 2.1. Parameters *R* and *L* present the load resistive and reactive parts and v_g presents the sinusoidal grid voltage. In case of the grid connection *R* and *L* would present a liking inductance with its inner resistance. Note that this structure is supposed to be used in relatively high-voltage and low-current applications, at switching frequencies no higher than 20 kHz, therefore insulated-gate bipolar transistors (IGBTs) are depicted.

Using this configuration and applying the proper gate signals to the power transistors, a desired three-level output voltage V_{AB} (voltage levels: $+V_{dc}$, 0 and $-V_{dc}$) can be obtained and applied across the load. The simplest way to control one H-bridge is to provide to its power switches square control signals with a proper duration. Switches which belong to one leg work alternately with one control signal and its opposite counterpart, while another leg has the same control behaviour just the signal is delayed by the time which corresponds to the half of the selected fundamental period. The duration of one pulse is defined by the parameter so-called duty-cycle δ which represents the switch on-time in per unit. It can be transformed into an angle scale, so one pulse is defined by the switching angle α when it changes its state from 0 to 1. In case of $\alpha=0$, the output voltage has only two voltage levels $\pm V_{dc}$ while in all other cases when $\alpha\neq 0$ there are three output voltage levels. Output voltages of one H-bridge for two different cases $\alpha=0$ and $\alpha=\pi/4$ over three fundamental periods (3T=60ms) are presented in Figure 2.2.(a) and (b) respectively. According to those two waveforms, the limit of switching angle α is evidently $\pi/2$. It must be noted that V_{dc} voltage is set to 200V and the fundamental frequency is 50Hz therefore a switching angle $\alpha=\pi/4$ corresponds to the time t=2.5ms.

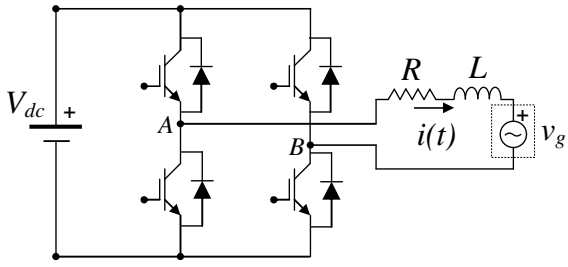


Figure 2.1. Single-phase three-level H-bridge dc/ac inverter with a passive *RL*-load and a possible load voltage v_g (grid connection).

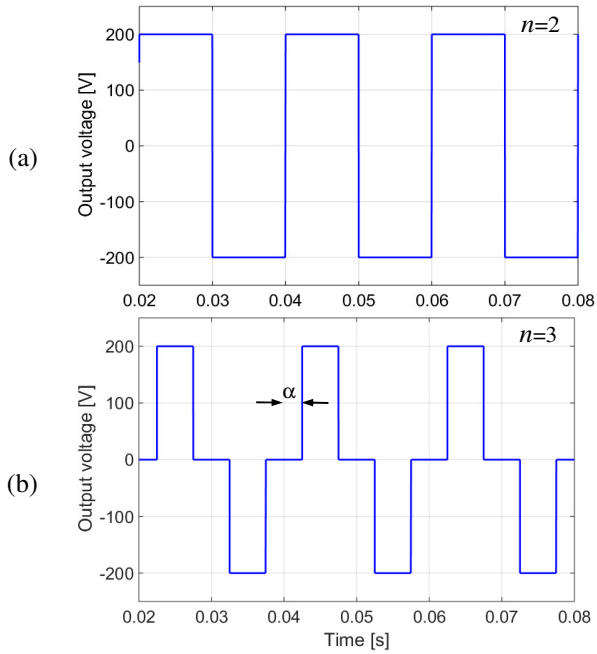


Figure 2.2. Output voltage of a single-phase inverter in case of switching angles (**a**) $\alpha=0$ ($n=2$) and (**b**) $\alpha=\pi/4$ ($n=3$), for $V_{dc}=200V$ and f=50Hz.

Note that in this chapter the configuration of the single-phase cascaded H-bridge multilevel inverter is presented with its basic output characteristics considering the basic control technique. Detailed control techniques, including the well-known pulse-width modulation (PWM) technique, will be presented in other chapters.

Apart from a single-phase three-level H-bridge which provides the output voltage that has by default three different levels $+V_{dc}$, 0 and $-V_{dc}$, it is possible to use this configuration as a basic building block in order to realise an n-level cascaded single-phase inverter. This configuration is shown in Figure 2.3.(a). It consists of N H-bridges connected in a way that every middle point of the first (second) leg of one H-bridge is connected to the middle point of the second (first) leg of another H-bridge and at the end two terminals of the whole cascaded configuration remain and are used for the load or grid connection. An important ability of this kind of configuration is its modularity which provides a possibility of increasing the total output voltage having more properly insulated dc bus voltages. In this case, the maximum number of output voltage levels equals $n=2N+1$ (N positive and N negative voltage levels, and one zero level), where N presents the number of cascaded H-bridges, as well as the number of needed isolated dc bus supplies. In case of one H-bridge N equals 1.

Using the advantage of the modularity, lower excursions of the output voltage in between all voltage levels is provided, as well as an improvement of the output voltage and current qualities. In Figure 2.3.(b) and (c) output voltages in case of two (n=5) and three (n=7) cascaded H-bridges are presented over three fundamental periods (3T=60ms) where each dc bus voltage is V_{dc}=200V. Fundamental frequency is set to 50 Hz and switching angles are $\alpha_1 = \pi/6$ (t_1=1.67ms) and $\alpha_2 = \pi/4$ (t_2=2.5ms) in the first case and in the second case an additional switching angle $\alpha_3 = \pi/3$ (t_3=3.33ms) is added. As it can be noticed that, in case of n=5, the maximum output voltage V_{max} is 400V which is two times the dc bus voltage and in case of n=3 V_{max} is 600V i.e. three times the dc bus voltage. This shows the important modular characteristic of this inverter where the output voltage increases proportionally with number of H-bridges N.

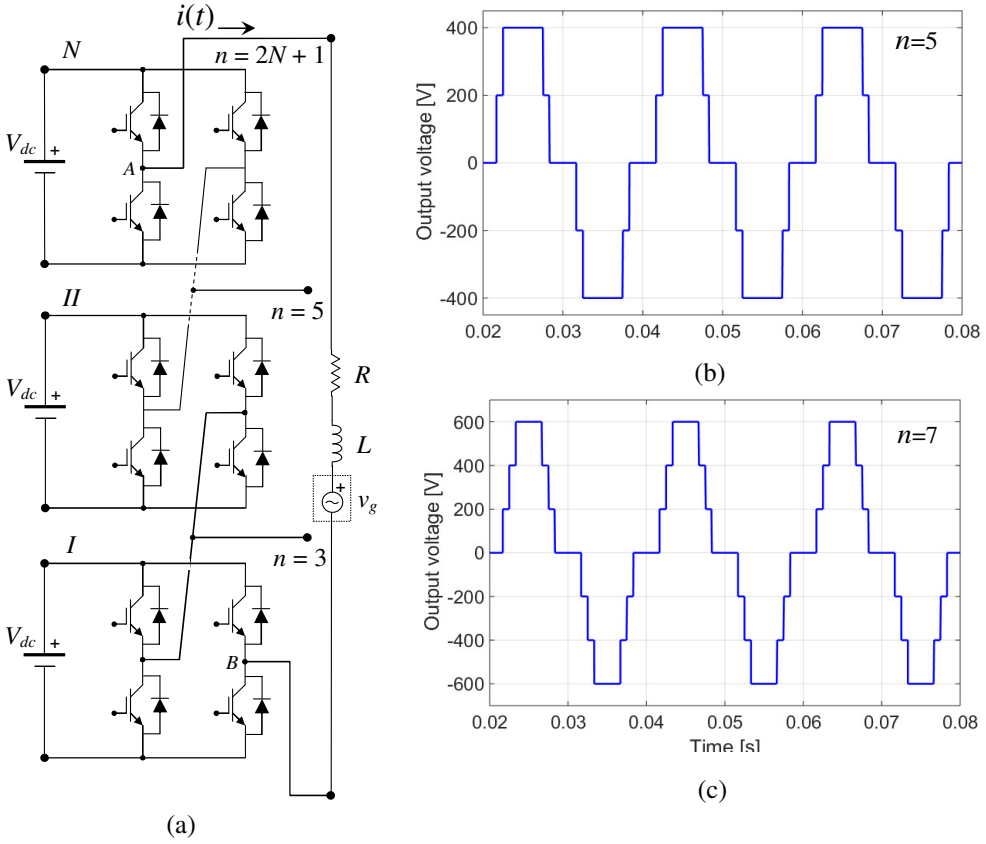
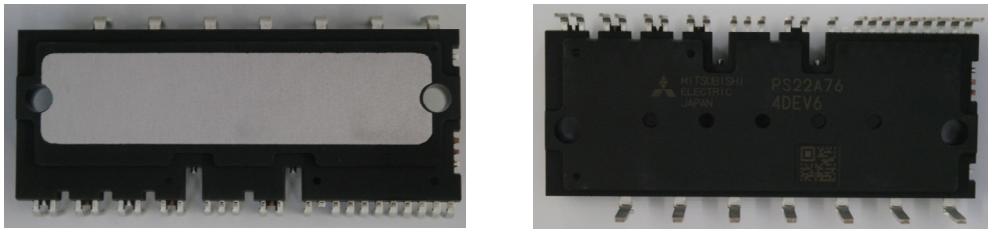


Figure 2.3. (**a**) Single-phase n-level inverter with a passive *RL*-load and a possible load voltage v_g (grid connection), and the output voltage in case of (V_{dc}=200V, f=50Hz):
(**b**) n=5 and switching angles $\alpha_1 = \pi/6$ and $\alpha_2 = \pi/4$ and,
(**c**) n=7 and switching angles $\alpha_1 = \pi/6$, $\alpha_2 = \pi/4$, and $\alpha_3 = \pi/3$.

2.3 Experimental implementation of a single-phase cascaded H-bridge inverter

In this chapter the experimental implementation of the previously explained *n*-level single-phase cascaded H-bridge inverter will be described in detail for the configuration up to three cascaded H-bridges. All experimental activities related to the design and practical realization of the mentioned configurations were carried out in the laboratory ‘‘SUN-Lab’’ at the department of Electrical, Electronic and Information Engineering ‘‘Guglielmo Marconi’’, University of Bologna and headed by Professor Gabriele Grandi. Experiments are an essentially important part of every research since each analytical and simulation solution has to be transferred from ‘the paper’ to ‘the real world’ by doing experiments and showing the proper results.

As a first step of the experimental implementation it is important to select a proper power module, suitable for the proposed configuration, considering its characteristics such as a power range, rated voltage and current, number of power switches, maximum switching frequency, control signal voltage level and etc. The selected power module is a three-phase Mitsubishi PS22A76 intelligent power IGBT dc/ac inverter. Its basic characteristics are: power range application 0.2-3.7kW, rated voltage and current 1200V and 25A, maximum switching frequency 20kHz and control signal voltage level up to 20.5V. The top and bottom sides of the selected inverter are presented in Figure 2.4. The power side has seven pins of which one pin is reserved for the dc bus voltage, three pins are used as the middle point connections of three inverter legs and the next three pins as their ground connections. The control side has much more pins for supplying the control part of each leg, for driving all six switches and for the fault state.

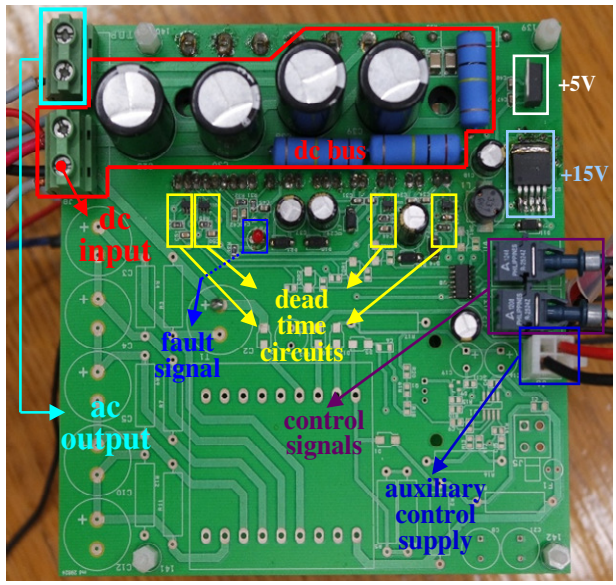


(a) (b)

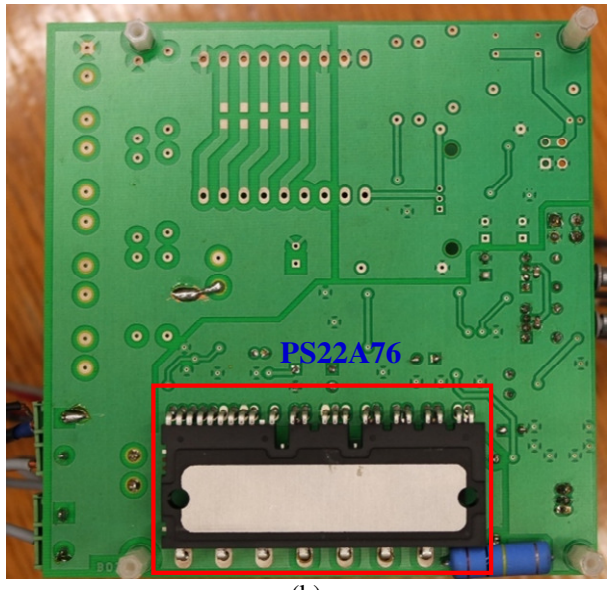
Figure 2.4. Mitsubishi PS22A76 intelligent power IGBT three-phase inverter (1200V, 25A) (**a**) top side and (**b**) bottom side.

The custom-made PCB board with the IGBT power module and its control and power parts is presented in Figure 2.5.(a) and (b) - top and bottom sides. On the top side the dc bus voltage connection is marked together with a load connection, dead-times circuits, fault signal, control signal connections, auxiliary control supply for the control part and two dc/dc converters. On the bottom side the inverter is displayed.

It is important to note that since the H-bridge structure is needed and the power module is the three-phase one, the third inverter leg is not connected to the main circuit and is properly grounded in order to avoid some circulating or leakage currents. Detailed scheme of the PCB board connections together with all components is given in Appendix 1.



(a)



(b)

Figure 2.5. Custom-made PCB board with a three-phase Mitsubishi PS22A76 intelligent power IGBT dc/ac inverter-power and control parts: (**a**) top side and (**b**) bottom side.

2.3.1 Control side implementation

In order to have the control of the inverter properly working, it has to be supplied by the 15V dc voltage as recommended by the manufacturer. In order to keep this voltage perfectly constant a dc/dc converter is used (marked as +15V in Figure 2.5.(a)) and supplied by the dc auxiliary supply Tenma 728345A (36V, 3A). The input voltage of this dc/dc converter is set to 17.23V, thereby it gives the required stable 15V dc at its output. In case of having a cascaded configuration consisting of more H-bridges, each one must have an own auxiliary dc supply, electrically and mutually isolated in order to avoid a common circulating current between the control parts. This requirement is provided by using small isolating single-phase transformers (230V-24V, 4.6A, 200VA). Each auxiliary supply is preceded by two isolating transformers providing the total voltage ratio (230V-24V-230V). In this case every possible common connection is avoided. Connecting all dc supplies directly to the electrical grid would mean that they share the same ground connection and the isolating feature is lost. The simple scheme presenting the auxiliary control dc supplies for three cascaded H-bridges is depicted in Figure 2.6.

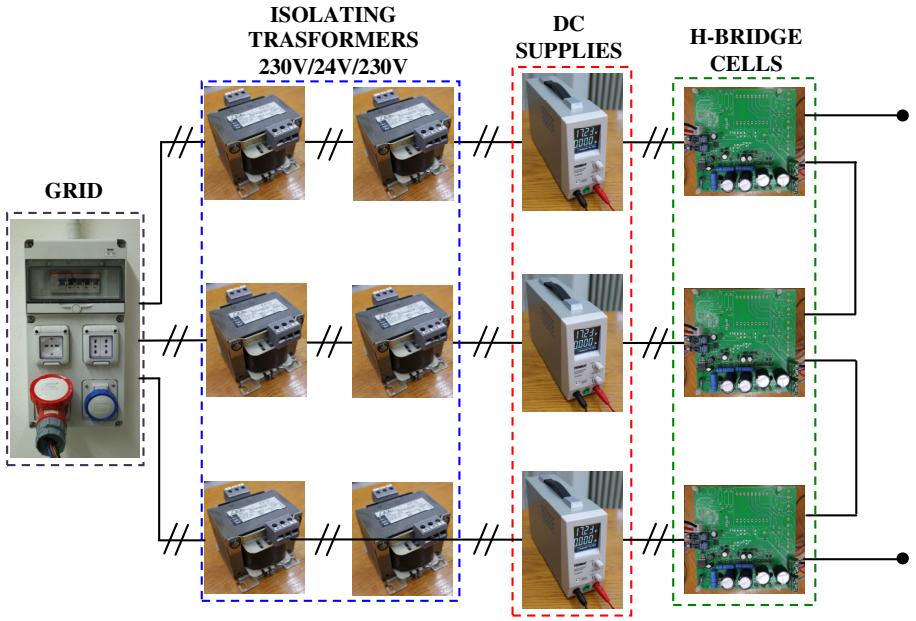


Figure 2.6. Experimental setup for providing three mutually isolated dc auxiliary supplies for the control side of a single-phase seven-level inverter (n=7) with three cascaded H-bridges.

Apart from the auxiliary supplies, the control gate signals have to be provided to properly control a single-phase multilevel inverter.

For this propose the Arduino DUE microcontroller board based on 84-MHz Atmel SAM3X83 ARM Cortex-M3 CPU is selected as a microcontroller which is powerful enough to generate control signals with desired waveforms and frequencies working in open loop. Using the Arduino platform, a C++ program code should be written and uploaded into the processor which generates all programmed control signals. The Arudino DUE platform is capable of generating eight (PWM) control signals at its output controlled independently. Basic characteristics of the microcontroller, together with some schemes are described in Appendix 1.

All control signals have to be sent to an interface board before transferring them to the inverter control pins. Two interface control boards were designed in the exactly same way (same components and same working principles) to decrease every possible noise and disturbance as much as possible and to adjust the voltage level of the control signals to be suitable for the power module. Note that only one interface board is enough (details given in Appendix 1), but there are two as a backup in case of some faults or a need of having more control signals generated by another microcontroller. The path of the control signals from the C++ program code to the inverter with three cascaded H-bridges is presented in Figure 2.7.

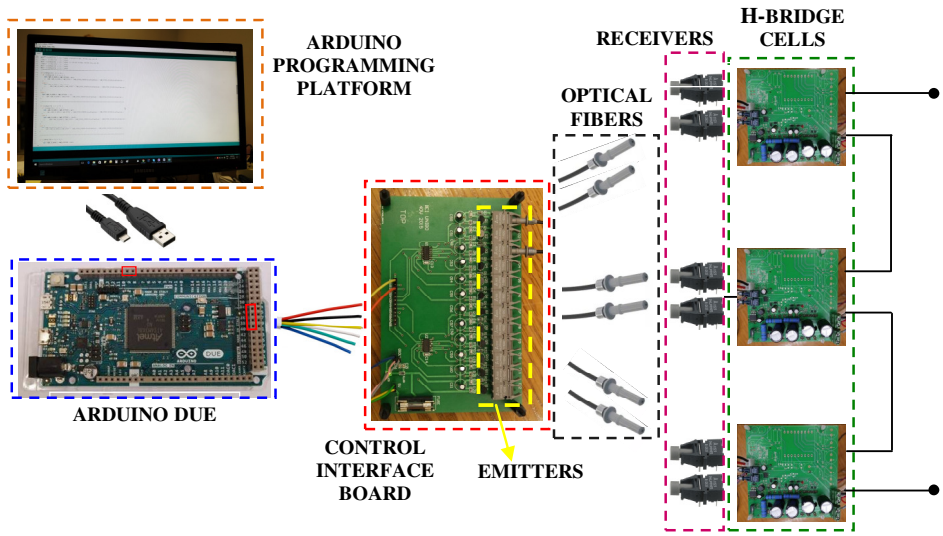


Figure 2.7. Scheme for providing control signals to a single-phase seven-level inverter (n=7) with three cascaded H-bridges.

As mentioned before, all control signals have to be programmed using the Arduino programming platform. The program code is sent to the microcontroller, via standard USB connector, which takes all commands and generates the signals which go to the control interface board through simple thin wire connections. After that the signals are transferred to the optical emitters.

The optical emitters are connected with the optical receivers, located on the PCB board, using the optical fibers. The receivers forward the control signals to small electronic circuits which lead directly to the control pins of the inverter. For each H-bridge there are supposed to be two control signals which correspond to the upper switches of two legs. Two other control signals for two lower inverter switches are generated directly on the board using proper electronic components. It should be noted that the supply for the Arduino DUE microcontroller evaluation board comes from the USB connector which is used for data transferring as well, therefore an additional supply is not needed. On the other hand, it can be supplied externally with the recommended voltage range 7-12V by plugging a 2.1mm center-positive plug into the power jack located near the USB connection on the board, in case that it is a more flexible solution.

An important parameter for all control signals and for the inverter itself is the dead time which provides safe operating conditions. It is simply possible to implement the dead time in the program code of the microcontroller, while generating two signals for one leg. In case of the presented H-bridges the dead time is implemented directly on the board using a simple electronic circuit for delaying signals as it is marked in Figure 2.5.(a). The suggested dead time for the PS22A76 IGBT inverter is 3μs therefore the adjusted dead time is 3.5μs to ensure safety. Taking into account that switching frequencies experimentally used for driving the inverter should not be higher than 20 kHz, the effect of the dead time is supposed to have a negligible effect on the output voltage and current.

2.3.2 Power circuit implementation

The power side of the experimental implementation mainly assumes properly and safely providing a dc voltage at the inverter input terminals. Maximum dc bus voltage of the power module is 1200V, but considering the voltage limit of other components of the experimental setup, it is supposed to be limited at 600V to ensure safety. In order to have a possibility to manually and continuously regulate the dc bus voltage within the proposed voltage limits a three-phase autotransformer (0-380V, 15A, 9900VA) is connected to the electrical grid. The autotransformer supplies three three-phase isolating transformers with the voltage ratio 400T/420Δ, rated current 1.44A and rated power 1000VA. They are used for the same reason as it was for the control side, to avoid common ground connection between all dc bus voltages. The three-phase outputs of the isolating transformers are connected to the three diode rectifiers (800V, 25A) which give three rectified voltages at their outputs with a frequency 300Hz that is six times the grid frequency 50Hz.

Each of these three voltages is supposed to be connected to the dc bus of one H-bridge and additionally rectified using dc bus capacitors. It should be noted that all three dc bus voltages have the same value and using the proposed autotransformer they cannot be regulated independently. The setup for providing three continuously controllable mutually isolated dc bus voltages is presented in Figure 2.8.

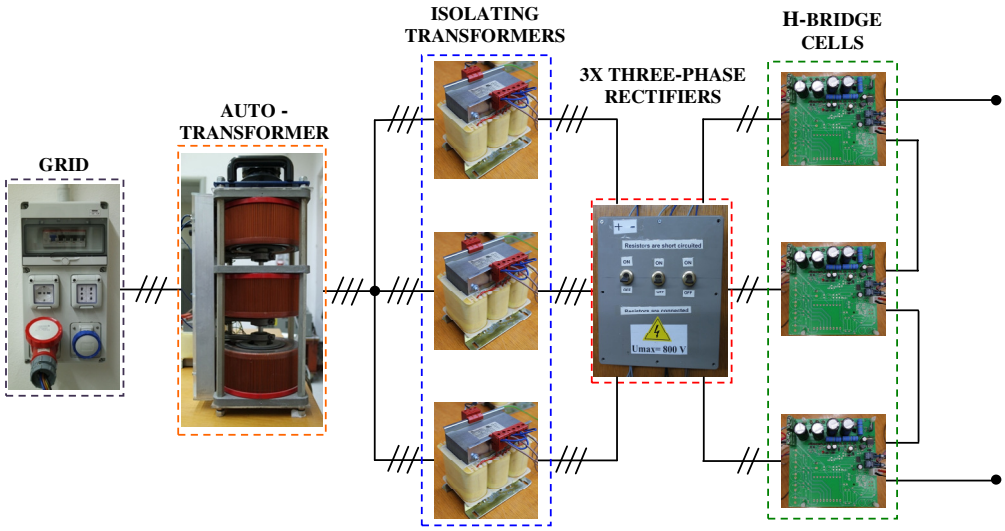


Figure 2.8. Experimental setup for providing three mutually isolated dc supplies for the power side of a single-phase seven-level (n=7) inverter with three cascaded H-bridges.

2.3.3 Measuring equipment

In order to measure all required parameters such as a voltage and current, different probes are used. Considering the characteristics of the implemented single-phase inverter, for voltage measuring a suitable voltage probe is a PICO TA057 differential probe (25MHz, ±1400V, ±2%) used with its two different possible attenuation ratios 1/20 and 1/200. For current measuring a LEM PR30 current probe (dc to 20kHz, ±20A, ±1%) is used. The current probe resolution is enough for current values that are supposed to be measured. To display everything what is measured and to do all necessary calculations in real time a Yokogawa DLM 2024 oscilloscope with its built-in advanced mathematical functions is considered. The voltage and current probes and the oscilloscope are presented in Figure 2.9.(a), (b) and (c), respectively.

It is important to note that regarding the fact that this thesis is mainly based on the output power quality, therefore calculating voltage and current THDs in real time using the proposed oscilloscope and its advanced functions bring a better and more precise verification of all analytical calculations and simulation results.

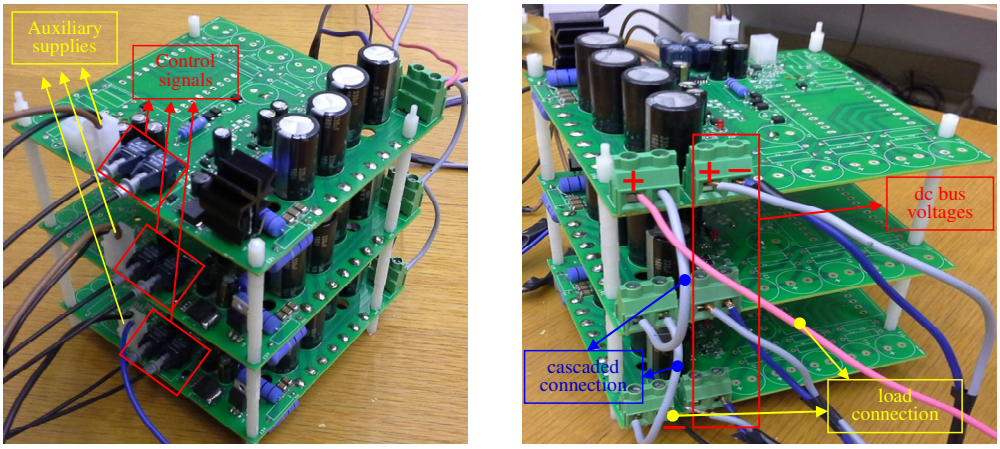
Due to oscilloscope's ability many different parameters, can be measured and evaluated while having the single-phase configuration working. Also, downloading all waveforms in a time-sample form with a high resolution take more time and increases the possibility of introducing unnecessarily additional errors.

(a) (b) (c)

Figure 2.9. Measuring equipment: (**a**) PICO TA057 differential voltage probe, (**b**) LEM PR30 current probe and (**c**) Yokogawa DLM 2024 oscilloscope

2.3.4 Complete experimental setup

The complete experimental setup of a single-phase seven-level inverter with three cascaded H-bridges together with dc bus supplies, auxiliary supplies and control signals is presented in Figure 2.10.(a) and (b).



(a) (b)

Figure 2.10. Three cascaded H-bridges properly connected: (**a**) control side and (**b**) power side

This setup can be used as only one H-bridge or two cascaded H-bridges simply avoiding sending control gate signals to the H-bridge that is not needed. In both cases, although two H-bridges or one H-bridge do not commutate, they produce voltage drops on their switches because the current circulates. The order of the current amplitude is supposed to be no higher than 5A-6A, therefore the voltage drops can be neglected. Considering this it can be said that, for example, the configuration of three cascaded H-bridges when one H-bridge does not commutate has the same behaviour as the configuration with only two cascaded H-bridges.

The full setup arrangement with all power, control and measuring components is presented in Figure 2.11.

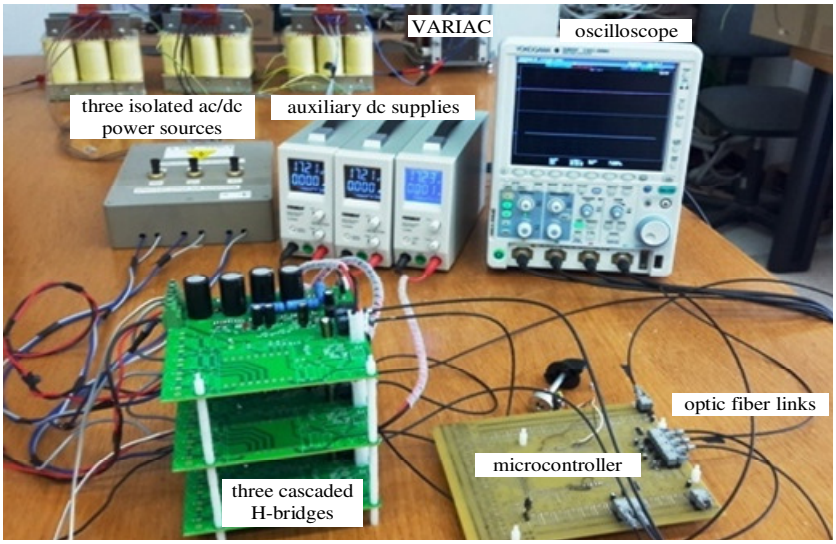


Figure 2.11. Complete experimental setup

2.4 References

[2.1] J. Ma, W. Song, S. Jiao, J. Zhao, and X. Feng, “Power Calculation for Direct Power Control of Single-Phase Three-Level Rectifiers,” *IEEE Trans. Ind. Electron.,* vol. 63, no. 5, pp. 2871–2882, 2016.

[2.2] F. C. Mattos, V. S. Lacerda, R. L. Valle, A. A. Ferreira, P. G. Barbosa, and H. A. C. Braga, “Contribution to the Study of a Single-Phase Single-Stage Photovoltaic System,” *IEEE Latin America Trans.*, vol. 13, no. 5, pp. 1265–1271, 2015.

[2.3] S. P. Ribas, L. Antonio, M. Jr, H. Pinheiro, R. C. L. F. Oliviera, and V. F. Montagner, “Design and implementation of a discrete-time H -infinity controller for uninterruptible power supply systems,” *IET Power Electron.*, vol. 7, no. 9, pp. 2233–2241, 2014.

[2.4] V. Sonti, S. Jain, and S. Bhattacharya, “Analysis of the Modulation Strategy for the Minimization of the Leakage Current in the PV Grid-Connected Cascaded Multilevel Inverter,” *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1156–1169, 2017.

[2.5] G. Waltrich and I. Barbi, “Three-Phase Cascaded Multilevel Inverter Using Power Cells With Two Inverter Legs in Series,” *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2605–2612, 2010.

[2.6] G. Waltrich and I. Barbi, “Three-Phase Cascaded Multilevel Inverter Using Power Cells with Two Inverter Legs in Series,” in *IEEE Energy Conversion Congress and Exposition (ECCE)*, San Jose, CA, USA, 2009, pp. 3085–3092.

[2.7] R. R. Karasani, V. B. Borghate, P. M. Meshram, H. M. Suryawanshi, and S. Sabyasachi, “A Three-Phase Hybrid Cascaded Modular Multilevel Inverter for Renewable Energy Environment,” *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1070–1087, 2017.

[2.8] X. Guo, R. He, X. Jia, and C. A. Rojas, “Leakage Current Reduction of Transformerless Three-Phase Cascaded Multilevel PV Inverter,” in *IEEE 24th International Symposium on Industrial Electronics (ISIE)*, Bùzios, Rio de Janeiro, Brazil, 2015, pp. 1110–1114.

3 Power quality evaluation of a single-phase cascaded multilevel inverter with staircase modulation technique

3.1 Introduction

In last decades, multilevel inverters have been widely used for medium- and high-voltage/power applications, such as different industrial and grid connected systems [3.1]–[3.4]. There are many papers on this subject dealing with the evaluation of either voltage or current total harmonic distortion (THD), typically based on voltage/current frequency spectra calculations or measurements (FFT).

In particular, the power electronics research community has recently increased its interest in voltage and current THD analysis for the staircase modulation technique. The analytical calculations for voltage THD of multilevel PWM single- and three-phase inverters have been obtained in [3.5] in case of a high ratio between switching and fundamental frequencies (i.e. so-called asymptotic approximation). Considering a pure inductive load, the current THD actually becomes voltage frequency weighted THD (WTHD). This approximation is practically very accurate for inductively dominant *RL*-loads, meaning that the load time constant (L/R) is much larger than switching interval durations (in the order of half fundamental period divided by the number of levels) [3.6]. The same approach can be applied in case of the staircase modulation and multilevel inverters.

Much work has been done on selective harmonics elimination (SHE) techniques, described in [3.7]–[3.10]. However, although SHE techniques can totally eliminate certain low-order harmonics, they do not have a minimization impact on either voltage or current THD, taking into account the whole harmonic content. To evaluate and optimize multilevel power quality, the research community typically uses a limited harmonics count (51, as recommended by Institute of Electrical and Electronics Engineers (IEEE) Standard 519 [3.11] or others, like 101) that can result in underestimating it [3.12], [3.13].

Recently, there have not been so many developments where the infinite harmonic content is taken into account for the power estimation in multilevel inverters. One reason may be a generally high complexity of a possible mathematical approach or the fact that sometimes there is no practical need to consider infinitely many harmonics. Recent publications have shown that it is quite feasible to consider an infinite harmonic content for the voltage THD when making multilevel voltage waveform analysis in the time domain [3.14]–[3.16].

Optimal switching angles that minimize multilevel inverter voltage THD for a given level count are presented in [3.15] for the single-phase configuration that the new manner of using Matlab to determine optimal switching angles was introduced for. In [3.16], the method of using asymmetrical dc bus voltages in order to achieve the minimum voltage THD was proposed, with a difficulty of the experimental implementation. In both cases, the corresponding modulation index was not explicitly indicated. A parallel implementation of the genetic algorithm on graphical processing unit was proposed in [3.17] in order to accelerate the computation of the optimal switching angles, which is usually a computationally demanding method and cannot be used easily for real-time control in case of multilevel inverters with varying dc sources.

In this thesis the theoretical analysis, simulation and experimental verifications of voltage and current THD minimization problems for a single-phase multilevel inverter are presented considering the whole modulation index range and using the time-domain problem formulations. The breakthrough of the proposed method is a power quality optimization and minimization for multilevel single-phase inverters using the time-domain (W)THD taking into consideration all possible switching harmonics [3.18].

Comparing the proposed time-domain (W)THD method with the standard frequency-domain THD minimization for voltage and current brings some advantages, such as results equivalent to unlimited harmonics content, avoiding Fourier trigonometric calculation of large number of harmonic magnitudes, reduced processor time, and reduced accumulated numerical errors. In this case, the only calculation based on the frequency domain is the Fourier calculation applied to determine the amplitude of the fundamental component (i.e. so-called the modulation index m), which is unavoidable.

Following the proposed method of minimizing the voltage and current THDs, general expressions for fundamental voltage and current mean square approximation errors and THDs are derived. Voltage and current THD minimization problems are formulated as time-domain constrained optimization ones and their solutions are obtained numerically. Inductively dominant *RL*-load is considered while in case of the current THD the grid connection is analysed as well. The verification of the theoretical developments is carried out by Matlab/Simulink simulations and detailed laboratory experiments.

3.2 Staircase modulation technique

The staircase modulation technique is a basic kind of modulation technique used for providing all gate signals for power switches. It is usually represented by different switching angles which define the output voltage and therefore the output current as well. For the single-phase H-bridge inverter presented in Figure 3.1.(a), which consists of four power switches, two different control signals must be provided in order to properly control two inverter legs. In Figure 3.1.(b) two control signals for two upper switches of the mentioned three-level single-phase inverter are presented over three fundamental periods (3T=60ms) considering the same switching angles $\alpha=\pi/4$ (t=2.5ms). In general, switching angles present delays of control signals compared with the full pulse. Note that the control signals for lower switches are the same just inverted, therefore they are not presented here.

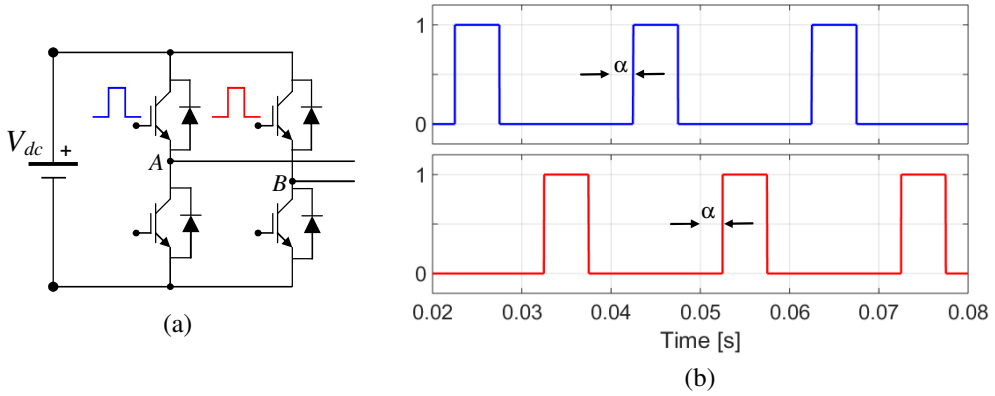


Figure 3.1. Single-phase three-level H-bridge dc/ac inverter:
(**a**) electrical circuit and (**b**) control signals for two upper switches for $\alpha=\pi/4$.

The three-level output voltage V_{AB} of one H-bridge inverter is presented in Figure 3.2. over three fundamental periods (3T=60ms), with the dc bus voltage V_{dc}=200V and fundamental frequency 50Hz. The general harmonic content given by the proposed modulation technique is relatively high. In order to improve it some optimal switching angles can be selected. In this case, the switching angle $\alpha=\pi/4$ is arbitrarily selected for the sake of explaining the modulation technique without any optimization impact on voltage or current quality. Selecting switching angles has a higher impact when there are more cascaded H-bridges. In this case a possibility of selecting optimized switching angles to obtain an improved power quality brings a higher contribution.

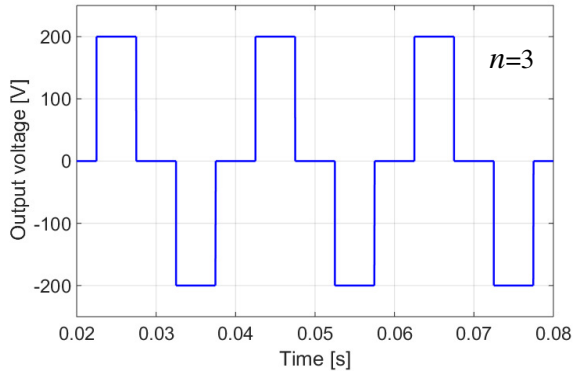


Figure 3.2. Output voltage of a single-phase three-level inverter (one H-bridge) with V_{dc}=200V, f=50Hz and switching angle $\alpha=\pi/4$.

In Figure 3.3. a single-phase seven-level inverter with three cascaded H-bridges (a) and switching-angle dependent control signals (b) are presented. The values of the angles are: $\alpha_1=\pi/6$ (t_1=1.67ms), $\alpha_2=\pi/4$ (t_2=2.5ms) and $\alpha_3=\pi/3$ (t_3=3.33ms). As mentioned previously, the selection of the switching angles is arbitrary at this step, as it would be the case for an n-level single-phase inverter where $(n-1)/2$ switching angles were selected.

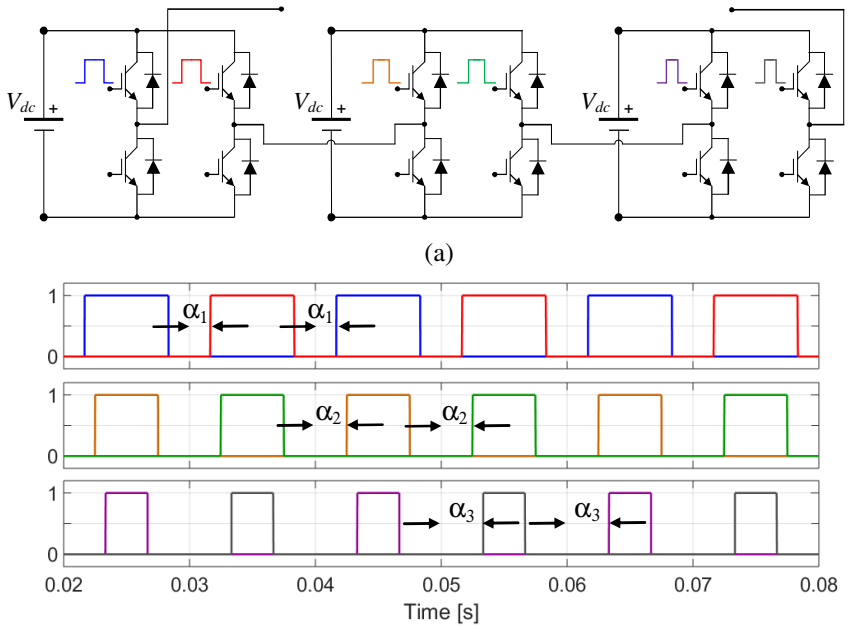


Figure 3.3. (**a**) Single-phase cascaded seven-level inverter (three H-bridges) and (**b**) control signals for six upper switches with switching angles $\alpha_1=\pi/6$, $\alpha_2=\pi/4$ and $\alpha_3=\pi/3$.

The output voltage over three fundamental periods (3T=60ms) is presented in Figure 3.4. with the dc bus voltage 200V of each H-bridge. It must be noted that the output current is not presented here because it strictly depends on the load which is not specifically described here. It will be done later on.

According to Figure 3.4., it can be noticed that with increasing the number of cascaded H-bridges, the voltage waveform becomes more similar to the sinusoidal waveform, but still yields a relatively high value of the total harmonic distortion. Also, three dc bus voltages are summed and the maximum output voltage reaches the value of 600V which corresponds to the modular characteristic of cascaded inverters.

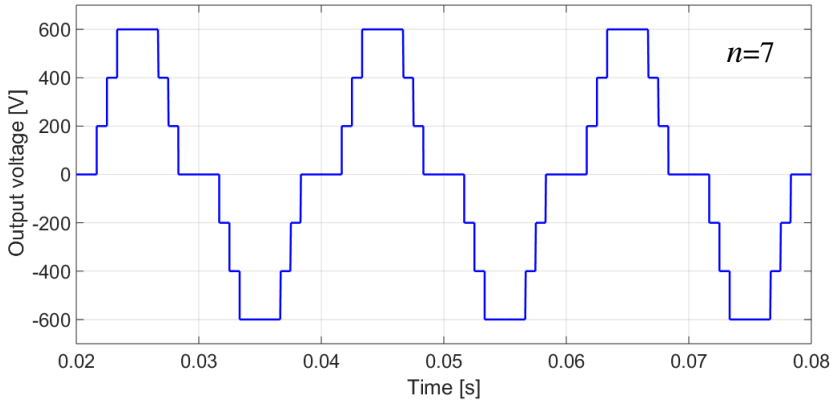


Figure 3.4. Output voltage of a single-phase seven-level inverter (three cascaded H-bridges) with V_{dc}=200V, f=50Hz and switching angles $\alpha_1=\pi/6$, $\alpha_2=\pi/4$ and $\alpha_3=\pi/3$.

An important parameter related to the proposed modulation techniques that directly affects the output voltage is the so-called modulation index *m.* It presents the ratio between the amplitude of the fundamental output voltage component (50Hz) $V_{1,\max}$ and the dc bus voltage V_{dc} of one H-bridge:

$$m = \frac{V_{1,\max}}{V_{dc}}. \tag{3.1}$$

In order to calculate the value of *m* for the first harmonic knowing all switching angles for one cascaded configuration, it is enough to use the Fourier series:

$$m = \frac{2}{T}\int_0^T v \sin(2\pi f t k)\, dt = \frac{2}{T}\int_0^T v \sin(\omega t)\, dt\ , \tag{3.2}$$

where T presents the fundamental period, f is the fundamental frequency and ω its angular frequency being k=1 for the first harmonic.

In order to present (3.2) in the angle domain, a simple equality can be introduced:

$$d\alpha = d(\omega t) = \omega\, dt = \frac{2\pi}{T} dt \longrightarrow dt = d\alpha \frac{T}{2\pi}. \tag{3.3}$$

Following (3.3), the expression for calculating the modulation index *m* for the first harmonic becomes:

$$m = 2\frac{1}{2\pi}\int_{0}^{2\pi} v\sin(\alpha)\,d\alpha\,. \tag{3.4}$$

Considering that the quarter-wave symmetry can be easily noticed in Figures 3.2. and 3.4., (3.4) can be written as:

$$m = 2\frac{1}{\pi/2}\int_{0}^{\pi/2} v\sin(\alpha)\,d\alpha = \frac{4}{\pi}\int_{0}^{\pi/2} v\sin(\alpha)\,d\alpha\,. \tag{3.5}$$

In case of having a single-phase *n*-level cascaded inverter with the switching angles $\alpha_1,\alpha_2,\ldots,\alpha_{(n-1)/2}$, the formula for calculating the modulation index *m* becomes:

$$m = \frac{4}{\pi}\left[\int_{\alpha_1}^{\alpha_2} 1\cdot\sin(\alpha)\,d\alpha + \int_{\alpha_2}^{\alpha 3} 2\cdot\sin(\alpha)\,d\alpha + \cdots + \int_{\alpha_{\frac{n-1}{2}}}^{\pi/2} \frac{n-1}{2}\cdot\sin(\alpha)\,d\alpha\right]. \tag{3.6}$$

Solving all integrals in (3.6) and summing them, the final expression for the modulation index *m* as a function of the inverter voltage level *n* is:

$$m = \frac{4}{\pi}\left[\cos(\alpha_1)+\cos(\alpha_2)+\cdots\cos\left(\alpha_{\frac{n-1}{2}}\right)\right] = \frac{4}{\pi}\sum_{i=1}^{k}\cos(\alpha_i)\,,\ k=\frac{n-1}{2}\,. \tag{3.7}$$

It must be noted that all equations are expressed as a function of different switching angles and the inverter voltage level *n* for the sake of easier following and calculating all relevant parameters.

3.3 Voltage and current quality time-domain problem formulation

In order to obtain minimal output voltage and output current THDs (hereinafter voltage and current), it is necessary to find optimal switching angles for a given modulation index *m*. The problem formulation in the frequency domain, as a general optimization that considers a limited harmonic count, is a possible source of inaccuracy [3.12], [3.13], [3.17]. In order to find an optimal solution that considers all harmonics, the optimization problem must be formulated in the time domain and as a constrained optimization one.

One way of estimating optimal switching angles is properly defining precise closed-form expressions for output voltage and output current ripple approximation error normalized mean square (hereinafter voltage and current ripple) and minimizing them. To do so, different analyses will be presented for single-phase three-, five-, and seven-level inverters, which means a configuration up to three cascaded H-bridges.

Based on these analyses, general expressions for voltage and current NMS values as well as their THD calculations will be given as a function of the inverter voltage level *n*, and voltage and current switching angles.

3.3.1 Voltage ripple NMS and total harmonic distortion

In order to carry out an analysis of the voltage ripple normalized mean square (NMS) and to derive a formula for the voltage total harmonic distortion (THD) as a function of NMS, a single-phase cascaded configuration is considered with up to three cascaded H-bridges which means an inverter with maximum seven output voltage levels.

In Figure 3.5. one cascaded configuration is presented as well as three normalized voltage half-waveforms in case of *n*=3, 5, and 7. All voltages are normalized by the dc bus voltage V_{dc} of one H-bridge.

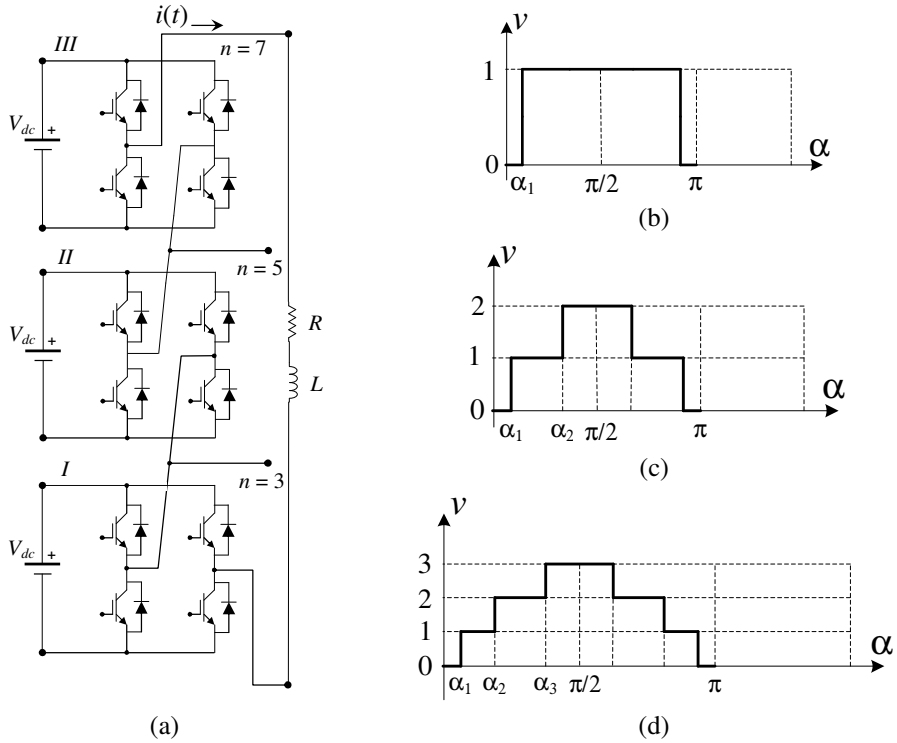


Figure 3.5. (**a**) Cascaded H-bridge inverter (*n*=3, 5, 7): voltage half-waves (p.u.) for the staircase modulation in case of (**b**) three, (**c**) five and (**d**) seven output voltage levels.

Switching angles for each configuration are properly depicted. Regarding the maximum number of switching angles and a level count of the given configuration, there are switching angles from α_1 to α_3, correspondingly.

Before evaluating the voltage ripple NMS, it is important to define the switching angle limits for the general case as a function of *n*. In order to do it, a fundamental component of a seven-level inverter normalized by V_{dc} is presented in Figure 3.6. over the half fundamental period 10ms which corresponds to π rad in the angle domain. The selected switching angles are $\alpha_1=\pi/6$, $\alpha_2=\pi/4$ and $\alpha_3=\pi/3$. Following equation (3.7), the maximum normalized value of the fundamental component, i.e. the modulation *m,* is 2.64. Limits of two switching angles are labelled as α_{1max} and α_{2max}, while the maximum of the third switching angle α_3 approaches the angle $\pi/2$.

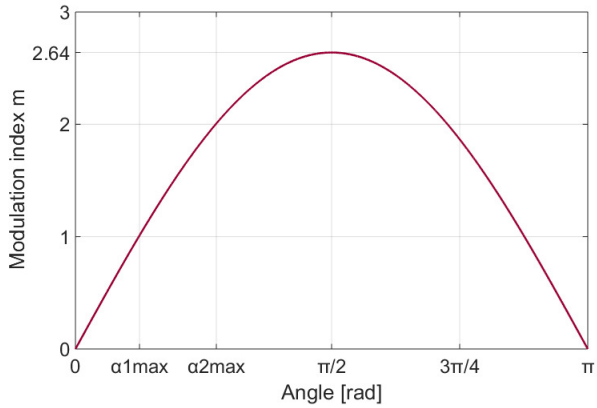


Figure 3.6. Normalized fundamental component of a single-phase seven-level inverter over the half fundamental period with the switching angles $\alpha_1=\pi/6$, $\alpha_2=\pi/4$ and $\alpha_3=\pi/3$.

According to Figure 3.6. two simple identities can be written:

$$m\sin(\alpha_{1\max}) = 1 \longrightarrow \alpha_{1\max} = \arcsin\left(\frac{1}{m}\right), \tag{3.8}$$

$$m\sin(\alpha_{2\max}) = 2 \longrightarrow \alpha_{2\max} = \arcsin\left(\frac{2}{m}\right). \tag{3.9}$$

Following this, the limits for all three switching angles α_1, α_2 and α_3 are:

$$0 \le \alpha_1 < \arcsin\left(\frac{1}{m}\right), \tag{3.10}$$

$$\arcsin\left(\frac{1}{m}\right) \le \alpha_2 < \arcsin\left(\frac{2}{m}\right), \tag{3.11}$$

$$\arcsin\left(\frac{2}{m}\right) \le \alpha_3 \le \frac{\pi}{2}. \tag{3.12}$$

It is possible to write a general form for the limits of one switching angle when the modulation index *m* is between two adjacent levels. This directly depends on the inverter voltage level *n*.

In this way the last defined switching angle is excluded. This exclusion completely considers the case for n=3 since the angle range is between 0 and $\pi/2$. Accordingly, the limits when m is between two adjacent levels are:

$$\arcsin\left(\frac{i}{m}\right) \le \alpha_{i+1} < \arcsin\left(\frac{i+1}{m}\right), i = 0,1..., \frac{n-5}{2}, n \neq 3. \tag{3.13}$$

The limits of the last switching angle, including the case for n=3 are:

$$\arcsin\left(\frac{k}{m}\right) \le \alpha_{k+1} \le \frac{\pi}{2}, k = \frac{n-3}{2}. \tag{3.14}$$

Note that for n=3, the equation (3.14) presents the full angle range between 0 and $\pi/2$.

Voltage ripple NMS can be obtained as a difference between the NMS values of the instantaneous voltage and its average (fundamental) component. Considering this, a simple relation related to normalized mean square values of the instantaneous voltage, its fundamental component and its ripple as a general function of a switching angle α can be written symbolically as:

$$NMS_v(\alpha) = NMS_{V_1}(\alpha) + NMS_V(\alpha) \tag{3.15}$$

being $NMS_v(\alpha)$ as the normalized mean square value of the instantaneous voltage, $NMS_{V_1}(\alpha)$ as the normalized mean square of the voltage fundamental component and $NMS_V(\alpha)$ as the normalized mean square of the voltage ripple.

Writing the integral forms of the members in (3.15) by using the definition of normalized mean square function and taking into account the square-wave symmetry lead to:

$$\frac{2}{\pi}\int_0^{\pi/2} v^2\, d\alpha = \frac{2}{\pi}\int_0^{\pi/2} v_1^2\, d\alpha + \frac{2}{\pi}\int_0^{\pi/2} \Delta v^2\, d\alpha. \tag{3.16}$$

Considering (3.16), the voltage ripple NMS can be written as:

$$NMS_V(\alpha) = \frac{2}{\pi}\int_0^{\pi/2} \Delta v^2\, d\alpha = \frac{2}{\pi}\int_0^{\pi/2} v^2\, d\alpha - \frac{2}{\pi}\int_0^{\pi/2} v_1^2\, d\alpha. \tag{3.17}$$

For calculating the NMS value of the voltage fundamental component, the last integral form in (3.17) can be expressed as a function of the modulation index m:

$$NMS_{V_1}(m) = \frac{2}{\pi}\int_0^{\pi/2} v_1^2\, d\alpha = \frac{2}{\pi}\int_0^{\pi/2} m^2 \sin^2(\alpha) d\alpha = \frac{1}{2}m^2. \tag{3.18}$$

Thus, the voltage ripple NMS for a single-phase n-level H-bridge inverter is:

$$NMS_V^n(\alpha, m) = \frac{2}{\pi}\int_0^{\pi/2} v^2\, d\alpha - \frac{1}{2}m^2. \tag{3.19}$$

Before delivering a general expression for the voltage ripple NMS calculation, its values for three-, five- and seven-level inverters can be written simply analytically, therefore the general dependence $NMS_V^n(\alpha, m)$ can be obtained.

Considering the aforementioned, the voltage NMS analytical forms for three different cases *n*=3, 5, 7 are:

$$NMS_V^3(\alpha_1, m) = \frac{2}{\pi}\int_{\alpha_1}^{\pi/2} d\alpha - \frac{1}{2}m^2 = 1 - \frac{2}{\pi}\alpha_1 - \frac{1}{2}m^2,\ 0 \le \alpha_1 \le \frac{\pi}{2}. \tag{3.20}$$

$$NMS_V^5(\alpha_1, \alpha_2, m) = \frac{2}{\pi}\int_{\alpha_1}^{\alpha_2} d\alpha + \frac{2}{\pi}\int_{\alpha_2}^{\pi/2} 2^2 \cdot d\alpha - \frac{1}{2}m^2 = 4 - \frac{2}{\pi}(\alpha_1 + 3\alpha_2) - \frac{1}{2}m^2,$$
$$0 \le \alpha_1 < \arcsin\left(\frac{1}{m}\right),\ \arcsin\left(\frac{1}{m}\right) \le \alpha_2 \le \frac{\pi}{2}. \tag{3.21}$$

$$NMS_V^7(\alpha_1, \alpha_2, \alpha_3, m) = \frac{2}{\pi}\int_{\alpha_1}^{\alpha_2} d\alpha + \frac{2}{\pi}\int_{\alpha_2}^{\alpha_3} 2^2 \cdot d\alpha + \frac{2}{\pi}\int_{\alpha_3}^{\pi/2} 3^2 \cdot d\alpha - \frac{1}{2}m^2 =$$
$$= 9 - \frac{2}{\pi}(\alpha_1 + 3\alpha_2 + 5\alpha_3) - \frac{1}{2}m^2, \tag{3.22}$$
$$0 \le \alpha_1 < \arcsin\left(\frac{1}{m}\right),\ \arcsin\left(\frac{1}{m}\right) \le \alpha_2 < \arcsin\left(\frac{2}{m}\right),\ \arcsin\left(\frac{2}{m}\right) \le \alpha_3 \le \frac{\pi}{2}.$$

Noticing a common rule of each of the previous expressions, the general form for the voltage ripple NMS for a single-phase *n*-level inverter controlled by the staircase modulation can be described as:

$$NMS_V^n\left(\alpha_1, \alpha_2, ..., \alpha_{\frac{n-1}{2}}, m\right) = k^2 - \frac{2}{\pi}\sum_{i=1}^{k}(2i-1)\alpha_i - \frac{1}{2}m^2,\ k = \frac{n-1}{2},$$
$$0 \le \alpha_1 < \arcsin\left(\frac{1}{m}\right),\ \arcsin\left(\frac{1}{m}\right) \le \alpha_2 < \arcsin\left(\frac{2}{m}\right), ..., \arcsin\left(\frac{n-3}{2m}\right) \le \alpha_{\frac{n-1}{2}} \le \frac{\pi}{2}. \tag{3.23}$$

After defining the voltage NMS criterion, it is important to derive a voltage THD form using the voltage NMS criterion. For this purpose simple mathematical calculations can be introduced. Every signal can be expressed as a sum of its fundamental component and other harmonic components, as it is given by (3.24).

$$x(t) = x_1(t) + \sum_k x_k(t). \tag{3.24}$$

Taking into account the Parseval's theorem (Rayleigh energy theorem), which says that the sum (or integral) of the square of a function is equal to the sum (or integral) of the square of its transform, the square of the total rms of one signal $x(t)$ can be presented as:

$$X_{rsm}^2 = \frac{1}{T}\int_0^T \left(x_1(t) + \sum_k x_k(t) \right)^2 = X_{1,rsm}^2 + X_{rms,dist}^2 \,. \tag{3.25}$$

Considering (3.25), the formula for the total harmonic distortion of the signal $x(t)$ becomes:

$$THD_x = \frac{X_{rms,dist}}{X_{1,rsm}} \,. \tag{3.26}$$

In case of the voltage ripple NMS of a single-phase n-level inverter, its normalized rms value is:

$$v_{rms}^n(m) = \sqrt{NMS_V^n\left(\alpha_1, \alpha_2, ..., \alpha_{\frac{n-1}{2}}, m \right)} \,. \tag{3.27}$$

Taking into account (3.26) and (3.27), the voltage THD formula can be written as the square root of the normalized mean square voltage ripple divided by the normalized fundamental component of the voltage:

$$THD_V^n(\%) = \frac{\sqrt{NMS_V^n\left(\alpha_1, \alpha_2, ..., \alpha_{\frac{n-1}{2}}, m \right)}}{V_{1,rms,norm}} \cdot 100 \,. \tag{3.28}$$

Defining the normalized fundamental component of the voltage as:

$$V_{1,rms,norm} = \frac{mV_{dc}}{\sqrt{2}} \frac{1}{V_{dc}} = \frac{m}{\sqrt{2}} \,, \tag{3.29}$$

the equation (3.28) becomes:

$$THD_V^n(\%) = \frac{\sqrt{2NMS_V^n\left(\alpha_1, \alpha_2, ..., \alpha_{\frac{n-1}{2}}, m \right)}}{m} \cdot 100 \,. \tag{3.30}$$

For a given modulation index m, the voltage THD optimization problem is formulated as a constrained optimization one with THD in equation (3.30) (NMS in equation (3.23)) as a target function to be minimized. This includes the modulation index m in equation (3.7) as an equality constraint and staircase modulation-imposed limitations on switching angles similar to equations (3.13) and (3.14) as inequality constraints.

3.3.2 Current ripple NMS and total harmonic distortion

In order to evaluate the current ripple NMS it is important to define the current waveform for a single-phase *n*-level inverter according to the corresponding voltage. Assuming the configuration described in the previous chapter with one H-bridge, and two and three-cascaded H-bridges, in Figure 3.7.(a), (b) and (c) three current half-waves with the corresponding voltages are depicted.

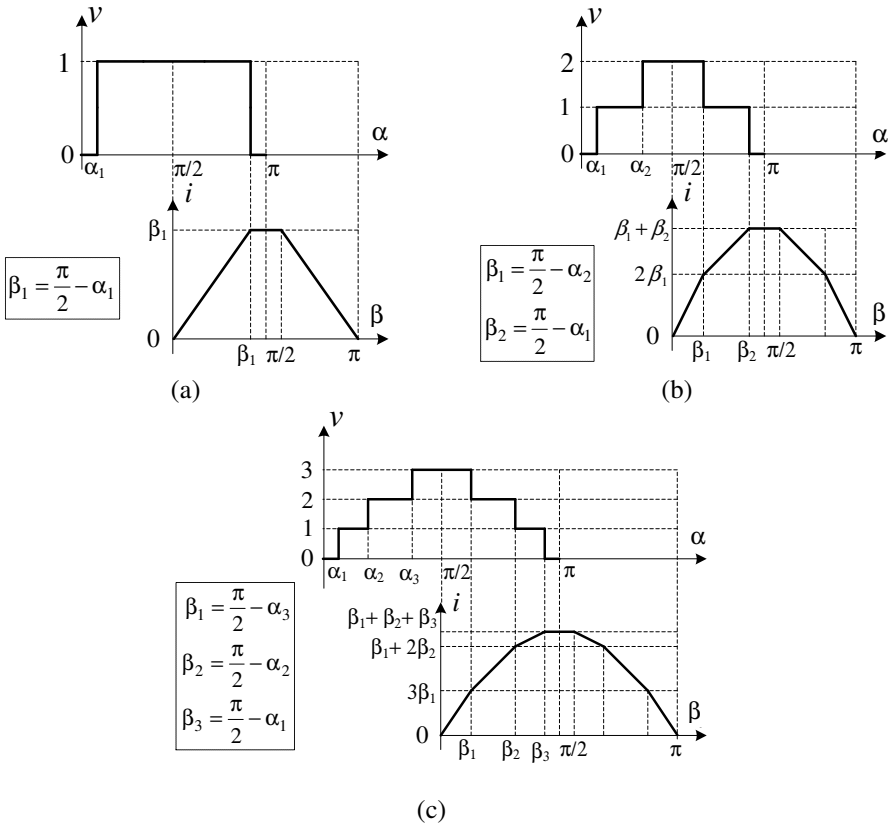


Figure 3.7. Voltage and current half-waves (p.u.) for staircase modulation in case of a (**a**) three-level, (**b**) five-level and (**c**) seven-level single-phase inverter.

Current waveforms are obtained by the time integration of the voltage that assumes pure inductive (or inductively dominant) load. For each inverter level count, the normalized current within different angle regions can be written as an integral form depending on the position of the current switching angle β. It must be noted that every current switching angle β is directly connected to a voltage switching angle α considering the shift π/2. Near each of the above waveforms the relations between voltage and current switching angles are written. According to this, in case of a three-level inverter the normalized current is given by (3.31).

$$i^{n=3}(0 \le \beta \le \beta_1) = \int_0^{\beta} u(\beta)\, d\beta = \int_0^{\beta} 1 \cdot d\beta = \beta\,. \tag{3.31}$$

The same calculation for a single-phase five-level inverter with two possible switching angles is:

$$i^{n=5}(0 \le \beta \le \beta_1) = \int_0^{\beta} u(\beta)\, d\beta = \int_0^{\beta} 2 \cdot d\beta = 2\beta\,. \tag{3.32}$$

$$i^{n=5}(0 \le \beta \le \beta_2) = \int_0^{\beta} u(\beta)\, d\beta = \int_0^{\beta_1} 2 \cdot d\beta + \int_{\beta_1}^{\beta} 1 \cdot d\beta = \beta_1 + \beta\,. \tag{3.33}$$

After this calculation the limits of the current switching angles must be defined, since in case of a three-level inverter there is only one angle which follows the whole quarter-wave symmetry range. According to Figure 3.7.(b), and taking into account the pure inductive load and the relation between voltage and current angles for a five-level inverter, the current switching angle limits can be written as:

$$0 \le \beta_1 < \frac{\pi}{2} - \arcsin\left(\frac{1}{m}\right), \frac{\pi}{2} - \arcsin\left(\frac{1}{m}\right) \le \beta_2 \le \frac{\pi}{2}\,. \tag{3.34}$$

Normalized current values within different angle regions for a single-phase seven-level inverter are:

$$i^{n=7}(0 \le \beta \le \beta_1) = \int_0^{\beta} u(\beta)\, d\beta = \int_0^{\beta} 3 \cdot d\beta = 3\beta\,. \tag{3.35}$$

$$i^{n=7}(0 \le \beta \le \beta_2) = \int_0^{\beta} u(\beta)\, d\beta = \int_0^{\beta_1} 3 \cdot d\beta + \int_{\beta_1}^{\beta} 2 \cdot d\beta = \beta_1 + 2\beta\,. \tag{3.36}$$

$$i^{n=7}(0 \le \beta \le \beta_3) = \int_0^{\beta} u(\beta)\, d\beta = \int_0^{\beta_1} 3 \cdot d\beta + \int_{\beta_1}^{\beta_2} 2 \cdot d\beta + \int_{\beta_2}^{\beta} 1 \cdot d\beta = \beta_1 + \beta_2 + \beta\,. \tag{3.37}$$

Following the previous explanation, the current angle limits in case of n=7 are:

$$\begin{aligned} &0 \le \beta_1 < \frac{\pi}{2} - \arcsin\left(\frac{2}{m}\right), \frac{\pi}{2} - \arcsin\left(\frac{2}{m}\right) \le \beta_2 < \frac{\pi}{2} - \arcsin\left(\frac{1}{m}\right), \\ &\frac{\pi}{2} - \arcsin\left(\frac{2}{m}\right) \le \beta_3 \le \frac{\pi}{2}\,. \end{aligned} \tag{3.38}$$

For Figure 3.7., the normalized current analysis for the pure inductive load, which assumes both the normalized fundamental angular frequency and the load inductance equal unity, the fundamental current harmonic magnitude equals voltage modulation index m.

Taking this into account, the current ripple NMS may be calculated, similarly to (3.19), by averaging the (normalized) squared current waveform on a quarter-wave interval. Considering the mentioned statement, for a single-phase *n*-level H-bridge inverter the current ripple NMS is found as:

$$NMS_I^n(\beta, m) = \frac{2}{\pi}\int_0^{\pi/2} i^2\, d\beta - \frac{1}{2}m^2 . \tag{3.39}$$

According to (3.39), for a single-phase three-level inverter with one switching angle β_1 (Figure 3.7.(a)) by direct current mean square value computation, the current ripple NMS is:

$$NMS_I^3(\beta_1, m) = \frac{2}{\pi}\left(\int_0^{\beta_1}\beta^2\, d\beta + \int_{\beta_1}^{\pi/2}\beta_1^2\, d\beta\right) - \frac{1}{2}m^2 = \beta_1^2 - \frac{4}{3\pi}\beta_1^3 - \frac{1}{2}m^2 \;,\; \beta_1 = \frac{\pi}{2} - \alpha_1 . \tag{3.40}$$

For a single-phase five-level inverter with two switching angles β_1 and β_2 (Figure 3.7.(b)), the current ripple NMS is:

$$NMS_I^5(\beta_1, \beta_2, m) = \frac{2}{\pi}\left(\int_0^{\beta_1}(2\beta)^2\, d\beta + \int_{\beta_1}^{\beta_2}(\beta_1+\beta)^2\, d\beta + \int_{\beta_2}^{\pi/2}(\beta_1+\beta_2)^2\, d\beta\right) - \frac{1}{2}m^2 . \tag{3.41}$$

Detailed calculation steps of (3.41) are presented in Appendix 2, here the final solution is given:

$$\begin{aligned} &NMS_I^5(\beta_1, \beta_2, m) = (\beta_1+\beta_2)^2 - \frac{\frac{6}{3}\beta_1^3 + \frac{6}{3}\beta_1\beta_2^2 + \frac{4}{3}\beta_2^3}{\pi} - \frac{1}{2}m^2 , \\ &\beta_1 = \frac{\pi}{2} - \alpha_2 \;,\; \beta_2 = \frac{\pi}{2} - \alpha_1 . \end{aligned} \tag{3.42}$$

Applying the same approach for a single-phase seven-level inverter with three switching angles β_1, β_2 and β_3 (Figure 3.7.(c)) gives:

$$NMS_I^7(\beta_1, \beta_2, \beta_3, m) = \frac{2}{\pi}\left(\begin{array}{l}\displaystyle\int_0^{\beta_1}(3\beta)^2\, d\beta + \int_{\beta_1}^{\beta_2}(\beta_1+2\beta)^2\, d\beta + \\ \displaystyle + \int_{\beta_2}^{\beta_3}(\beta_1+\beta_2+\beta)^2\, d\beta + \int_{\beta_3}^{\pi/2}(\beta_1+\beta_2+\beta_3)^2\, d\beta\end{array}\right) - \frac{1}{2}m^2 . \tag{3.43}$$

Detailed calculation steps of (3.43) are presented in Appendix 2, the final solution is given by (3.44).

$$NMS_I^7(\beta_1,\beta_2,\beta_3,m)=$$
$$=(\beta_1+\beta_2+\beta_3)^2-\frac{\frac{8}{3}\beta_1^3+\frac{6}{3}\beta_2^3+\frac{4}{3}\beta_3^3+2\left(\beta_1\beta_2^2+\beta_1\beta_3^2+\beta_2\beta_3^2\right)}{\pi}-\frac{1}{2}m^2\,, \tag{3.44}$$
$$\beta_1=\frac{\pi}{2}-\alpha_3\,,\ \beta_2=\frac{\pi}{2}-\alpha_2\,,\ \beta_3=\frac{\pi}{2}-\alpha_1\,.$$

For an arbitrary level count *n* according to the previous equations, the general current NMS formula becomes:

$$NMS_I^n\left(\beta_1,\beta_2,...,\beta_{\frac{n-1}{2}},m\right)=\left(\sum_{k=1}^{(n-1)/2}\beta_k\right)^2-\frac{2}{\pi}\left(\begin{array}{l}\frac{1}{3}\sum_{k=1}^{(n-1)/2}\left(\frac{n-1}{2}+2-k\right)\beta_k^3+\\+\sum_{k=1}^{(n-3)/2}\left(\beta_k\sum_{i=k+1}^{(n-1)/2}\beta_i^2\right)\end{array}\right)-\frac{1}{2}m^2, \tag{3.45}$$

$$\beta_k=\frac{\pi}{2}-\alpha_{\frac{n+1}{2}-k}\,,\ k=1,2,...,(n-1)/2\,.$$

The challenge of a time-domain current THD analysis in pure inductive load approximation (voltage WTHD) is expressed by (3.46) [3.20].

$$WTHD_V(m),\%=THD_I(m),\%=\frac{\sqrt{\sum_{k=2}^{\infty}\left(\frac{V_k}{k}\right)^2}}{V_1}\cdot 100 \tag{3.46}$$

This equation presents a closed-form expression for current approximation mean square error for piecewise linear (normalized) current waveforms obtained by time integration of their respective voltage waveforms (Figure 3.7.(a), (b) and (c)). Considering this, the current THD formula becomes:

$$THD_I^n(\%)=\frac{\sqrt{2NMS_I^n\left(\beta_1,\beta_2,...,\beta_{\frac{n-1}{2}},m\right)}}{m}\cdot 100\,. \tag{3.47}$$

3.4 Minimized voltage and current total harmonic distortions

3.4.1 Optimal voltage and current THDs solutions

The constrained THD (NMS) minimization problems with modulation index equality and switching angles inequality constraints described in the previous section 3.3. are effectively solved by means of Matlab function *fmincon*.

Voltage and current optimization solutions for a single-phase five-cell multilevel inverter (up to five switching angles and n=11) are shown in Figures 3.8., 3.9., 3.10., 3.11, 3.12. and 3.13.

In Figures 3.8. and 3.9. voltage and current optimal switching angles vs. modulation index m are presented, taking into account that the current optimal angles are labelled with α. It is done due to easier comparison between the current and voltage optimal switching angles and finding optimal working points considering both possible optimizations. For each value of the modulation index m, the proper relation between current angle α and β (depending on the inverter level) defined in the previous chapter exists. Each colour presents a different switching angle, corresponding to the inverter level count. The current switching angles are smoother compared with the voltage ones.

Voltage and current optimal switching angles may be considerably different. Over each inter-level interval, there are two points at which voltage THD optimal angles and current THD (voltage WTHD) optimal angles are identical, having the same modulation index m. Regarding the aforesaid, for the selected modulation indexes the voltage and current THDs are minimal.

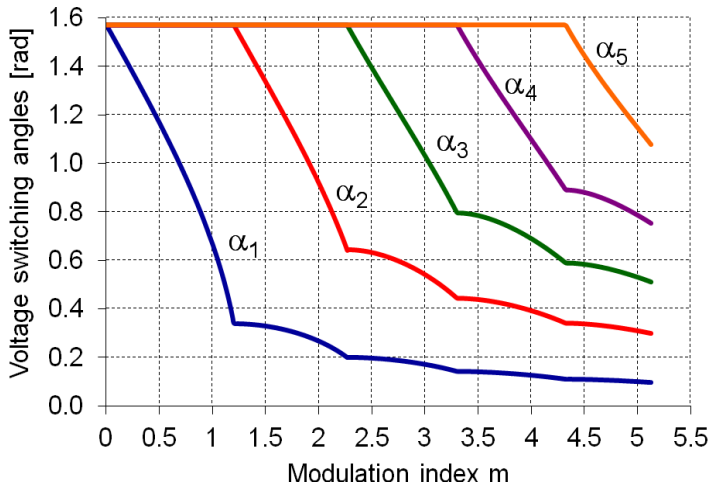


Figure 3.8. Voltage optimal switching angles vs. modulation index m for n = 11 (up to five cascaded H-bridges).

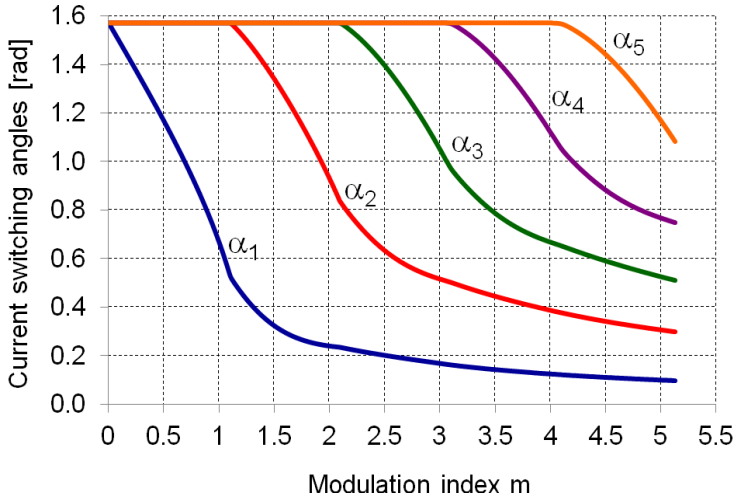


Figure 3.9. Current optimal switching angles vs. modulation index *m* for *n* = 11 (up to five cascaded H-bridges).

Based on the previously presented voltage and current optimal switching angles, the corresponding normalized mean squares values are presented in Figures 3.10. and 3.11., following the same colour representation over the modulation index range.

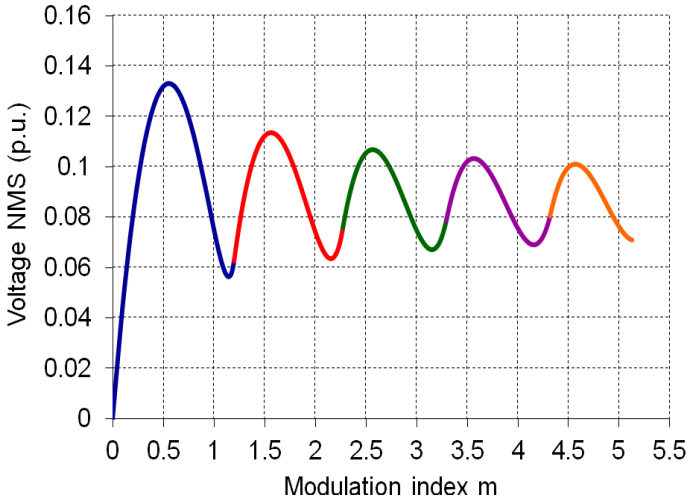


Figure 3.10. Voltage normalized mean square calculated using optimal voltage switching angles vs. modulation index *m* for *n* = 11 (up to five cascaded H-bridges).

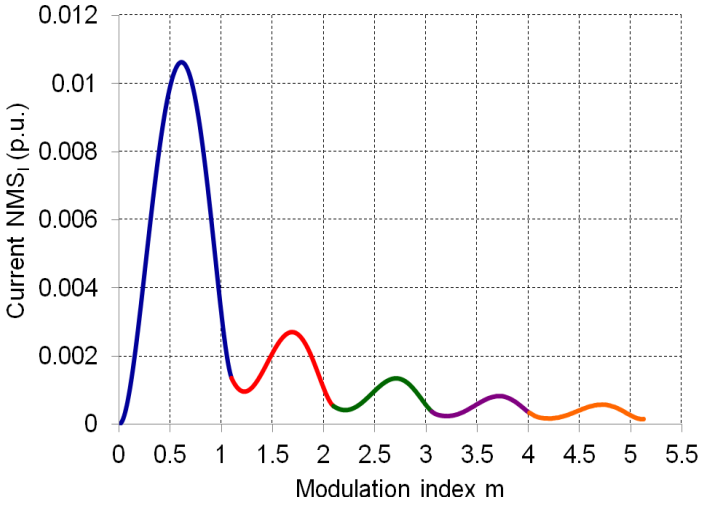


Figure 3.11. Current normalized mean square calculated using optimal current switching angles vs. modulation index m for $n = 11$ (up to five cascaded H-bridges).

Voltage and current THDs calculated by (3.30) and (3.47) using their optimal switching angles are presented in Figures 3.12. and 3.13. Over the inter-level modulation index intervals 1–2, 2–3, 3–4, 4–5, voltage and current quadratic approximation error (NMS/THD) local minima and maxima appear. Global voltage THD minima found in [15] and [16] for up to 6–7 switching angles, without explicitly indicating the modulation indices, are, in fact, local minima of the voltage THD curve in Figure 3.12.

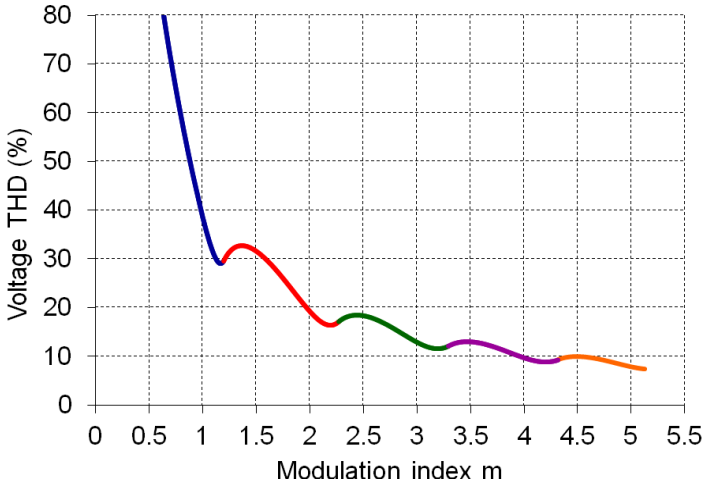


Figure 3.12. Minimal voltage total harmonic distortion (THD) vs. modulation index m for $n = 11$ (up to five cascaded H-bridges).

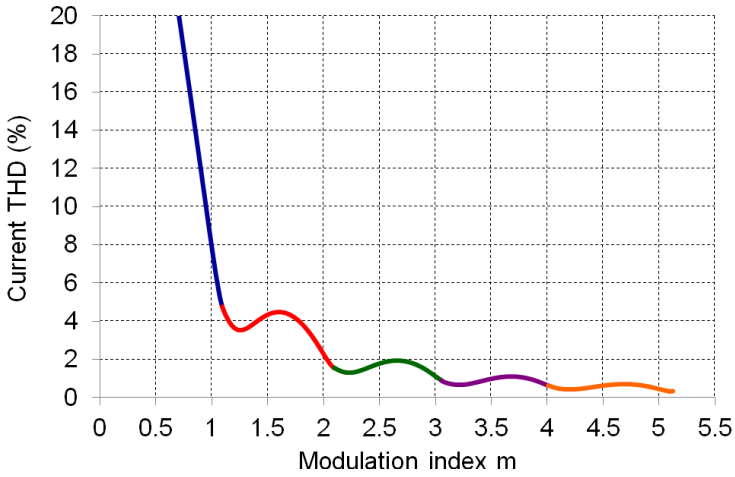


Figure 3.13. Minimal current total harmonic distortion (THD) vs. modulation index m for $n = 11$ (up to five cascaded H-bridges).

Study of sensitivity shows that optimal current THD is much more susceptible to switching angles variations compared with optimal voltage THD. This happens because a supposed fine piecewise linear optimal approximation (compared to a coarse piecewise constant one) is more susceptible in terms of possibly being affected by some disturbances. The low susceptibility to angle variations of optimal voltage THD is known from the previous study [3.12], [3.13]. On the whole, a coarse piecewise constant optimal approximation is very robust in terms of possible disturbances point of view, such as angle/level variations and rounding errors.

The comparison between optimal voltage and current THD (Figures 3.12. and 3.13.), shows that the current THD curve ripple is much larger considering the noticeable difference between adjacent maxima and minima in the order of 100%. As a result, current THD may be essentially reduced only by selecting a proper converter working point (modulation index) selection. On the contrary, there may be a significant current THD increase as a penalty for a detuned operation.

Regarding these figures, the curve of THD average trend can be approximated by simple hyperbolic approximations [3.19].

3.4.2 Optimal voltage and current working points

After defining the optimal THD solution for the voltage and current, it is important to define specific optimal working (test) points which will be considered in the simulation and experimental analyses.

Since these two analyses will consider a single-phase seven-level inverter, which means up to three cascaded H-bridges, the optimal working points will be within the corresponding modulation index range.

Minimal voltage and current THD curves within the modulation index range for the configuration consisting of three cascaded H-bridges (n = 7) are shown in Figures 3.14. and 3.15. together with selected optimal working points (a)-(d) having the modulation index $2<m<3$.

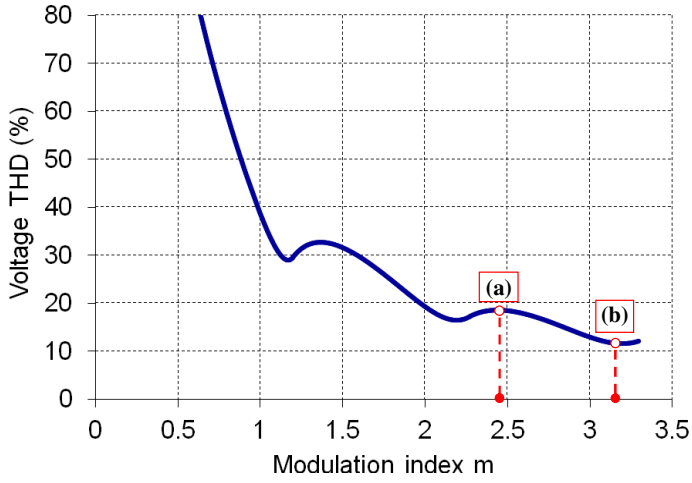


Figure 3.14. Minimal voltage THD vs. modulation index m for n=7 (up to three cascaded H-bridges) and two optimal working points for m=2.459 (a) and m=3.193 (b).

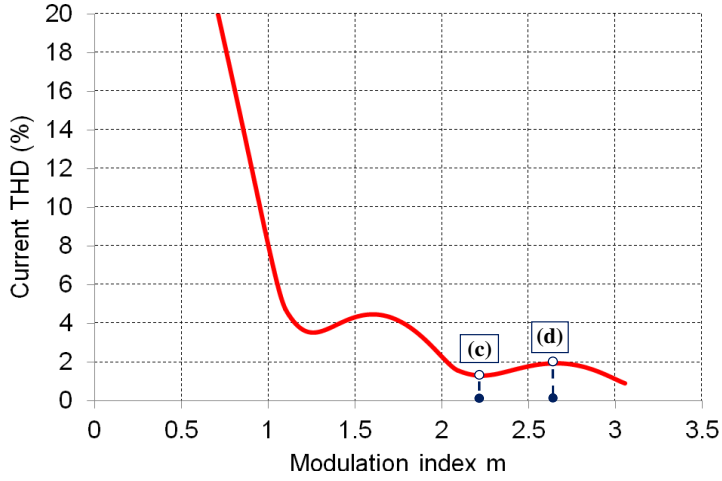


Figure 3.15. Minimal current THD vs. modulation index m for n=7 (up to three cascaded H-bridges) and two optimal working points for m=2.221 (c) and m=2.663 (d).

Voltage and current optimal switching angles are shown together in Figure 3.16. (current angle curves are the smoother ones). It is clearly visible that there are points in common where both voltage and current THDs have the optimal value considering the same modulation index *m* (*m*=2.494 (e), *m*=3.144 (f)), i.e. having the same switching angles.

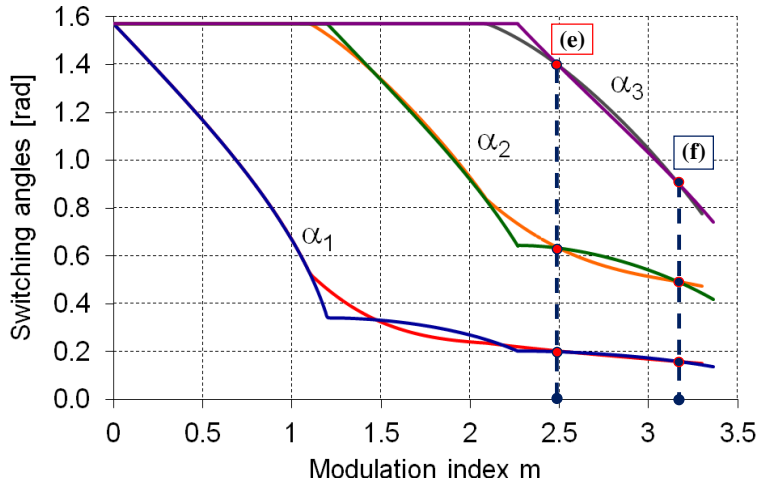


Figure 3.16. Voltage and current optimal switching angles vs. modulation index *m* for *n*=7 (up to three cascaded H-bridges) and two optimal working points in common: *m*=2.494 (e) and m=3.144 (f).

Considering these figures, the six test points indicated by dots are chosen for the simulation and experiments. In particular, four test points are selected for minimum and maximum values of voltage ((a) and (b)) and current ((c) and (d)) THDs over the modulation index range corresponding to a single-phase seven-level inverter, (Figures 3.14. and 3.15). Furthermore, another two test points (e) and (f) are selected corresponding to the so-called twice modulation index *m* when both voltage and current THDs are optimal having the same three switching angles (Figure 3.16). In table 3.1. the selected test points (a)-(f) are presented with the corresponding modulation indexes and switching angles α_1, α_2 and α_3.

Table 3.1. Six selected test points corresponding to a single-phase seven-level inverter

Test point	Modulation index *m*	Switching angles [rad]		
		α_1	α_2	α_3
(a)	2.459	0.199	0.635	1.424
(b)	3.193	0.155	0.482	0.884
(c)	2.221	0.224	0.758	1.527
(d)	2.663	0.190	0.580	1.294
(e)	2.494	0.202	0.633	1.397
(f)	3.144	0.160	0.495	0.925

3.5 Simulation

In order to validate the correctness of the analytical approach while estimating the power quality of a single-phase multilevel inverter controlled by the staircase modulation technique, Matlab/Simulink simulations were carried out. The configuration with three cascaded H-bridges (single-phase seven-level inverter) was implemented and is shown in Figure 3.17.

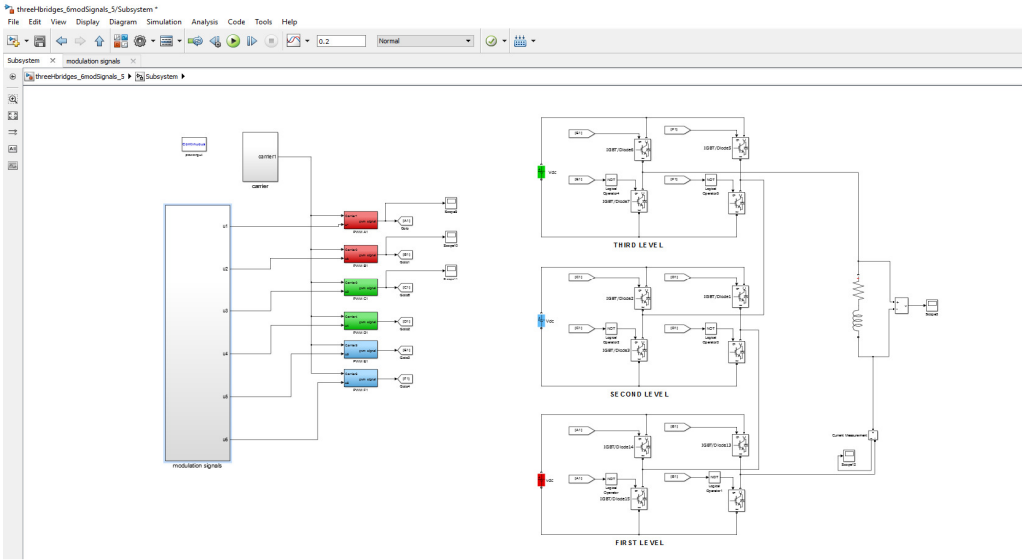


Figure 3.17. Matlab/Simulink model of a single-phase seven-level inverter with three cascaded H-bridges controlled by the staircase modulation technique

The left side of the figure represents the control part, while on the right side three H-bridges and the passive *RL*-load are shown. The control part, which is supposed to provide proper staircase modulation signals, consists of six modulation signals (each modulation signal corresponds to one H-bridge leg) and one carrier signal. The implementation of the control signals is quite simple and it is shortly presented in the following.

The idea of implementing the control signals follows the 100Hz carrier and switching-angle depending constant modulation signal with the same frequency. The amplitude of the modulation signal is directly proportional to the switching angle. In this case, assuming that the maximum value of the modulation signal m_m is 1 which is supposed to represent the angle $\pi/2$, introducing a simple relation (3.48):

$$m_m = 1 - \frac{\alpha[rad]}{\pi/2}, \tag{3.48}$$

the switching angle α is converted into the amplitude of the modulation signal.

This principle is presented in Figure 3.18. for two legs of one H-bridge where the set switching angle is π/4, which results in the modulation signal amplitude 0.5.

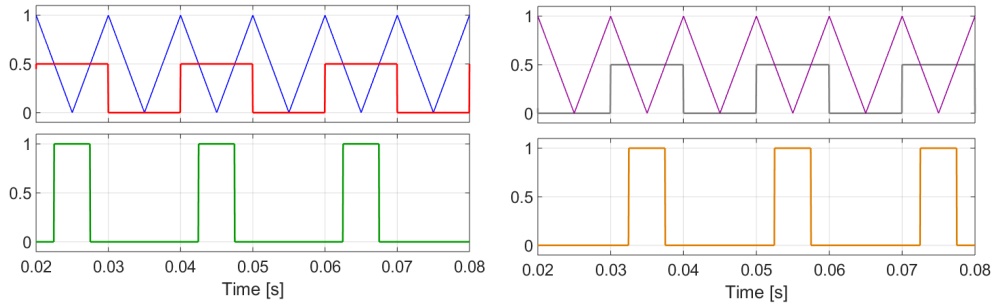


Figure 3.18. Control signals for two legs of one H-bridge with the staircase modulation: (**a**) carrier (blue trace), modulation signal (red trace) and gate signal (green trace); (**b**) carrier (purple trace), modulation signal (grey trace) and gate signal (orange trace).

It must be noticed that the frequency of the carrier is deliberately set at 100Hz although the fundamental frequency is 50 Hz. During the first half period of the carrier (Figure 3.18.(a)), the modulating signal is 0.5, while in the second half period it is zero. It is similarly presented in Figure 3.18.(b) for the second H-bridge leg. In this case, the shift of π rad between the gate signals of two H-bridge legs is provided. Two gate signals (green and orange ones) are obtained by comparing the carrier with the modulating signal. When the carrier is lower than the modulation signal, the comparison gives 1 at the output, otherwise the output is 0.

It is possible to attain the voltage and current THDs by using Matlab/Simulink with the built-in Matlab function called ‘‘FFT analysis’’. It is a simple tool which provides a THD value of one parameter corresponding to the selected fundamental frequency, additionally giving the amplitude of the fundamental component. The load must be inductively dominant as it was theoretically assumed. The chosen load parameters *R* and *L*, based on a real air-core inductor, are R=24.5Ω and L=480.7mH, measured by an RLC meter. The dc voltage of each H-bridge is set to 200V and the fundamental frequency is set at 50Hz.

In doing so, the voltage and current for the test point (a) as well as the results for all six defined test points (a)-(f) in chapter 3.4.2, using the Matlab/FFT tool, are presented in Figures 3.19., 3.20., 3.21 and 3.22.

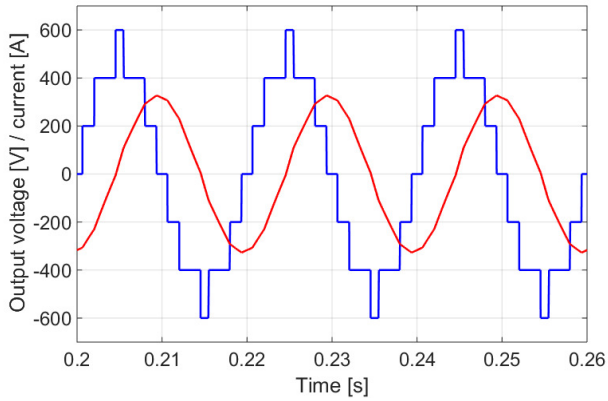
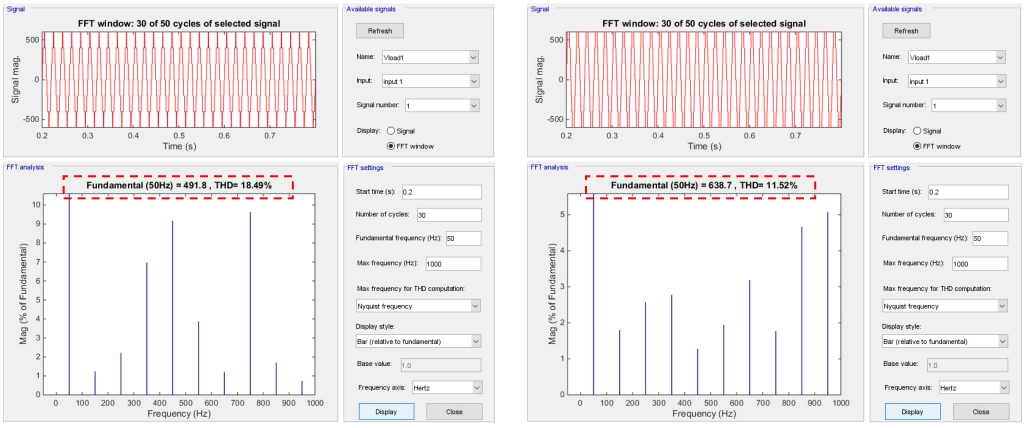


Figure 3.19. Voltage (blue) and current (red, x100) obtained by Matlab simulation for a single-phase seven-level inverter (three cascaded H-bridges) with respect to Figure 3.14.:
test point (a) - m = 2.459 (α_1 = 0.199, α_2 = 0.635, α_3 = 1.424),
for Vdc=200V, R=24.5Ω, L=480.7mH and f_f=50Hz.

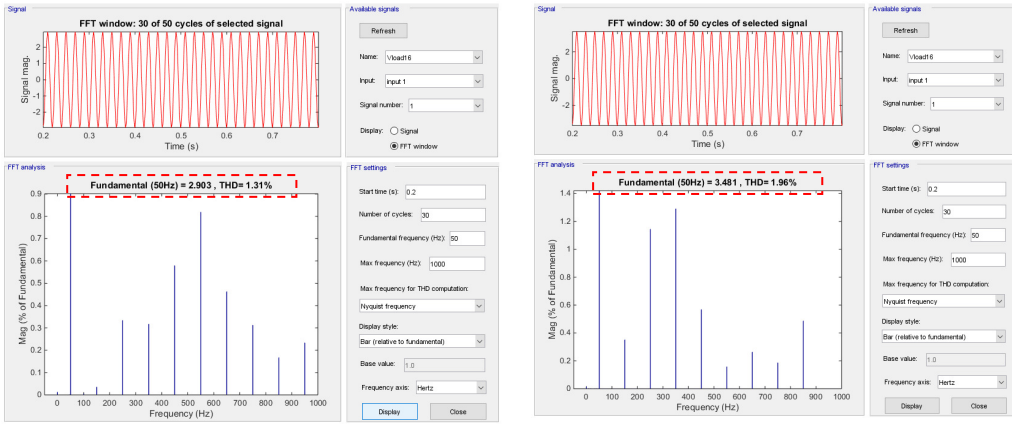


(a) (b)

Figure 3.20. Voltage THD obtained by Matlab simulation for a single-phase seven-level inverter (three cascaded H-bridges) with respect to Figure 3.14.:
(**a**) test point (a) - m = 2.459 (α_1 = 0.199, α_2 = 0.635, α_3 = 1.424);
(**b**) test point (b) - m = 3.193 (α_1 = 0.155, α_2 = 0.482, α_3 = 0.884).

Calculating the voltage and current THDs for each value of the modulation index m considers thirty fundamental periods of 20ms and starts at the time scale 200ms in order to steer clear of a possibly short transient period at the beginning of the simulation.

The fundamental voltage component as well as its THD value are emphasised with the red rectangle. The same applies for all selected test points.



(a) (b)

Figure 3.21. Current THD obtained by Matlab simulation for a single-phase seven-level inverter (three cascaded H-bridges) with respect to Figure 3.15.:
(**a**) test point (c) - $m = 2.221$ ($\alpha_1 = 0.224$, $\alpha_2 = 0.758$, $\alpha_3 = 1.527$);
(**b**) test point (d) - $m = 2.663$ ($\alpha_1 = 0.190$, $\alpha_2 = 0.580$, $\alpha_3 = 1.294$).

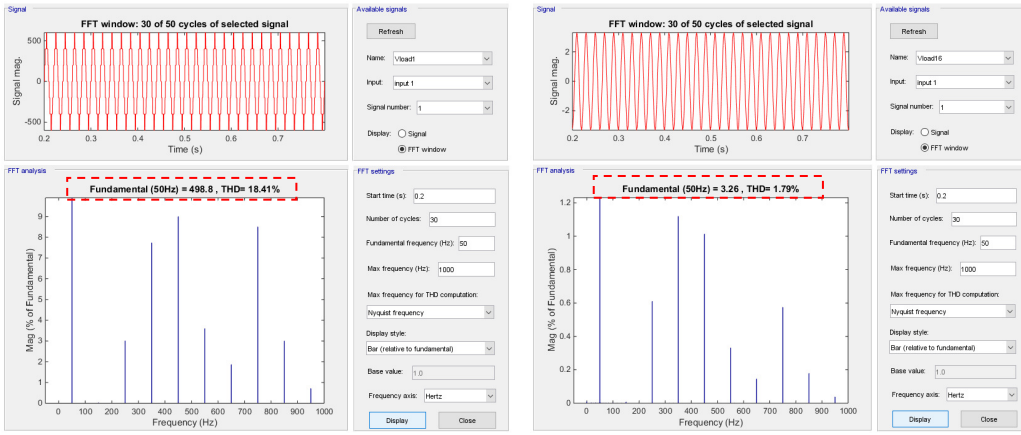


Figure 3.22.(a) Minimal voltage (left) and current (right) THDs obtained by Matlab simulation for a single-phase seven-level inverter (three cascaded H-bridges) with respect to Figure 3.16.: test point (e) - $m = 2.494$ ($\alpha_1 = 0.202$, $\alpha_2 = 0.633$, $\alpha_3 = 1.397$);

Note that Figure 3.22 is divided into two figures (a) and (b) due to better space arrangement and better resolution of the figures, which clearly shows the calculated parameters.

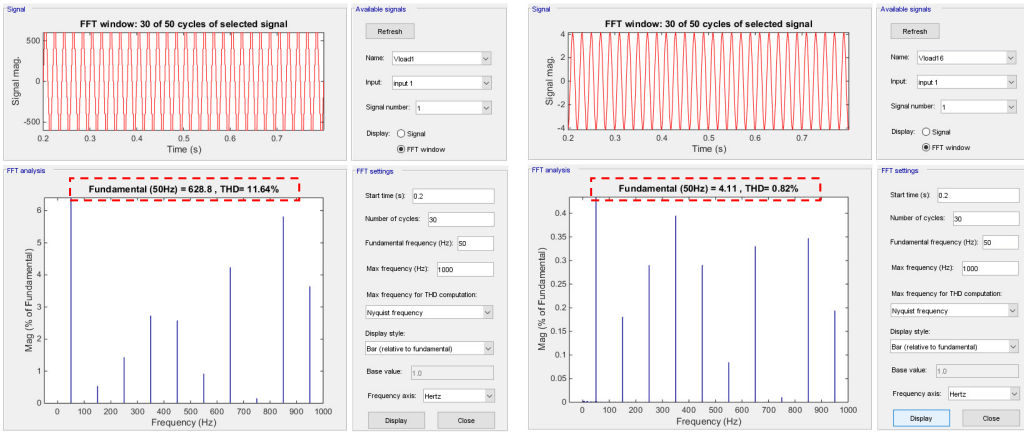


Figure 3.22.(b) Minimal voltage (left) and current (right) THDs obtained by Matlab simulation for a single-phase seven-level inverter (three cascaded H-bridges) with respect to Figure 3.16.: test point (f) - m = 3.144 (α_1 = 0.160, α_2 = 0.495, α_3 = 0.925).

Considering the selected minima and maxima within the modulation index range for a single-phase seven-level inverter as well as the optimal solutions in common for the voltage and current, the obtained THD values for the test points (a)-(f) are presented in the following table:

Table 3.2. Voltage and current THDs for six selected test points obtained by the simulation

Test Point	**Minimized THD_V (%)**	**Test Point**	**Minimized THD_I (%)**	**Test Point**	**Minimized THD_V (%)**	**Minimized THD_I (%)**
(a)	18.49	(c)	1.31	(e)	18.41	1.79
(b)	11.52	(d)	1.96	(f)	11.64	0.82

3.6 Laboratory experiments

Experimental verifications were performed for a single-phase inverter with one H-bridge, and two and three H-bridges (n_{max}=7), with the individual dc bus voltage V_{dc}=200V. Note that the detailed explanation of the experimental realization of the mentioned configuration is given in chapter 2.3. A simple circuit scheme of the experimental setup is shown in Figure 3.23.

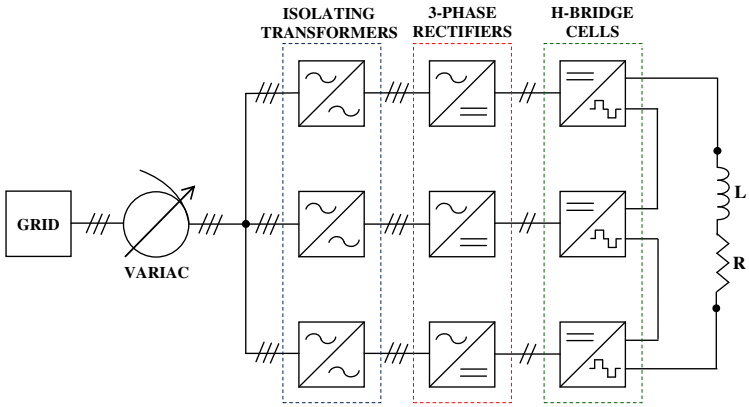
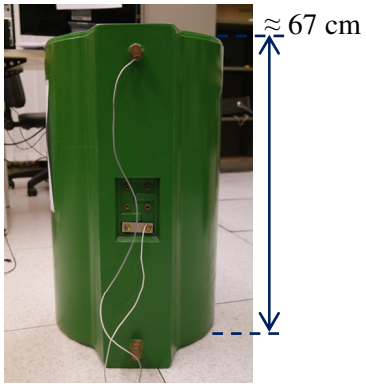


Figure 3.23. Circuit scheme of the experimental setup.

As it was considered in the simulation part, a real inductor with its resistive and inductive parts R=24.5Ω and L=480.7mH was used for the experimental tests. In Figure 3.24. the inductor with a side view together with the display of LCR meter measuring its parameter is presented.



(a)

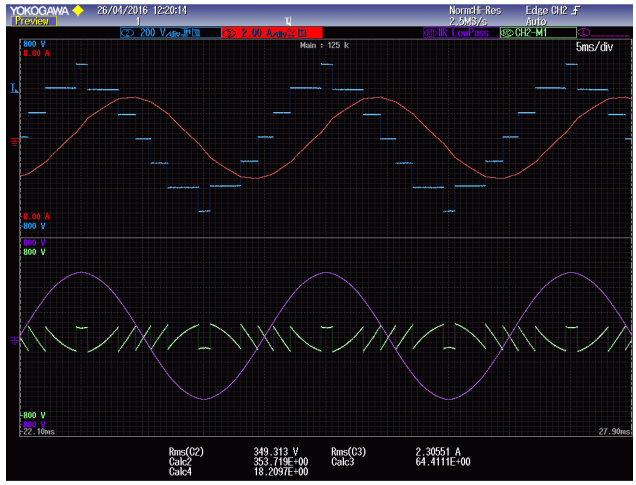
(b)

Figure 3.24. An inductor with its parameters R=24.5Ω and L=480.7mH:
(**a**) side view, (**b**) R and L measured by LCR meter.

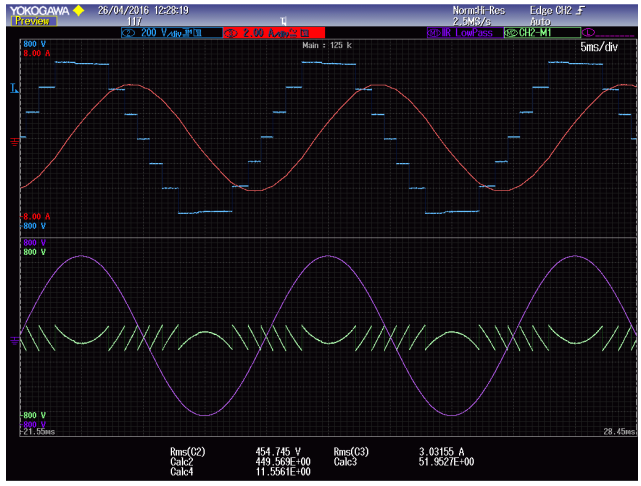
The control signals for all three H-bridges are provided by the Arduino DUE microcontroller. The modulating principle is similar to that one explained in chapter 3.6, therefore the program code with a brief explanation is given in Appendix 3.

In order to be able to properly and precisely compare the analytical results for the voltage and current THDs together with the simulation and experimental ones, the same six selected test points are considered for the experimental part.

In Figures 3.25., 3.26. and 3.27., the corresponding experimental results are presented, showing the test points (a)-(f). All figures depict the waveforms over the 2.5 fundamental periods (2.5T=50ms).



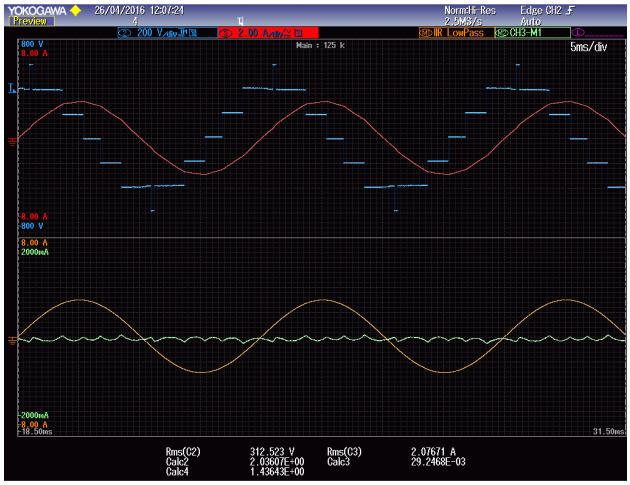
(a)



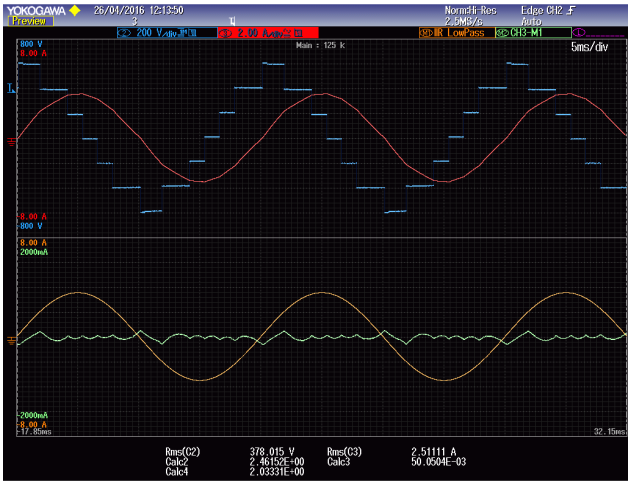
(b)

Figure 3.25. Voltage THD experimentally obtained for a single-phase seven-level inverter (three cascaded H-bridges) with respect to Figure 3.14.:
(**a**) test point (a) - $m = 2.459$ ($\alpha_1 = 0.199$, $\alpha_2 = 0.635$, $\alpha_3 = 1.424$);
(**b**) test point (b) - $m = 3.193$ ($\alpha_1 = 0.155$, $\alpha_2 = 0.482$, $\alpha_3 = 0.884$).

Figure 3.25. presents two cases for local maximum and minimum values of the voltage THD over the considered modulation index range. Figure 3.25.(a) corresponds to the voltage THD local maximum for $m = 2.459$ ($\alpha_1 = 0.119$, $\alpha_2 = 0.635$, $\alpha_3 = 1.424$), while Figure 3.25.(b) corresponds to the voltage THD local minimum for $m = 3.194$ ($\alpha_1 = 0.155$, $\alpha_2 = 0.482$, $\alpha_3 = 0.884$).



(a)



(b)

Figure 3.26. Current THD experimentally obtained for a single-phase seven-level inverter (three cascaded H-bridges) with respect to Figure 3.15.:
(**a**) test point (c) - m = 2.221 (α_1 = 0.224, α_2 = 0.758, α_3 = 1.527);
(**b**) test point (d) - m = 2.663 (α_1 = 0.190, α_2 = 0.580, α_3 = 1.294).

Figure 3.26. presents two cases for local minimum and maximum values of the current THD over the considered modulation index range. Figure 3.26.(a) to the current THD local maximum for m = 2.221 (α_1 = 0.224, α_2 = 0.758, α_3 = 1.527), while Figure 3.26.(b) corresponds to the current THD local minimum for m = 2.663 (α_1 = 0.190, α_2 = 0.580, α_3 = 1.294).

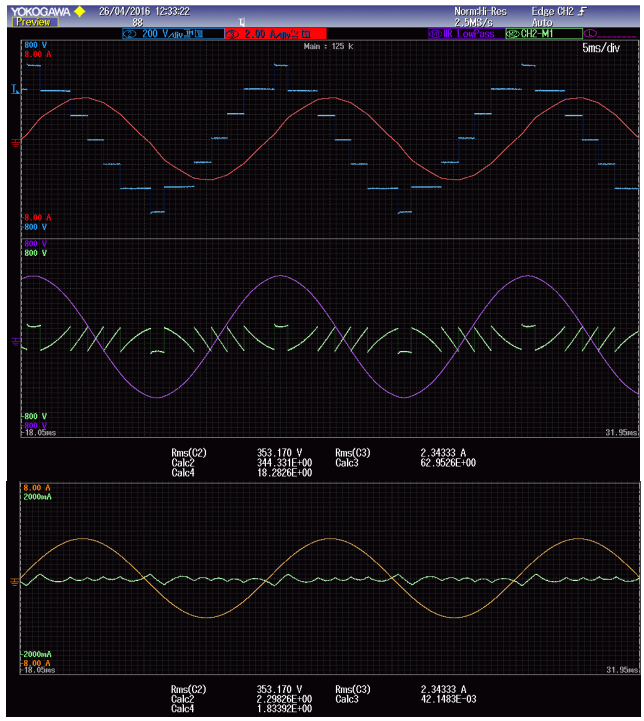


Figure 3.27. (a) Minimized voltage and current THDs experimentally obtained for a single-phase seven-level inverter (three cascaded H-bridges) with respect to Figure 3.16.: test point (e) - $m = 2.494$ ($\alpha_1 = 0.202$, $\alpha_2 = 0.633$, $\alpha_3 = 1.397$);

Figure 3.27. considers the cases of two modulation indices where the optimal voltage THD and the optimal current THD occur for the same switching angles, over the considered modulation index range. Figure 3.27.(a) corresponds to the case $m = 2.494$ ($\alpha_1 = 0.202$, $\alpha_2 = 0.633$, $\alpha_3 = 1.397$), while Figure 3.27.(b) corresponds to the case $m = 3.144$ ($\alpha_1 = 0.160$, $\alpha_2 = 0.495$, $\alpha_3 = 0.925$).

Figure 3.27. is divided into two figures for the same reason as it is done in case of Figure 3.22. due to better space arrangement and better resolution of the figures.

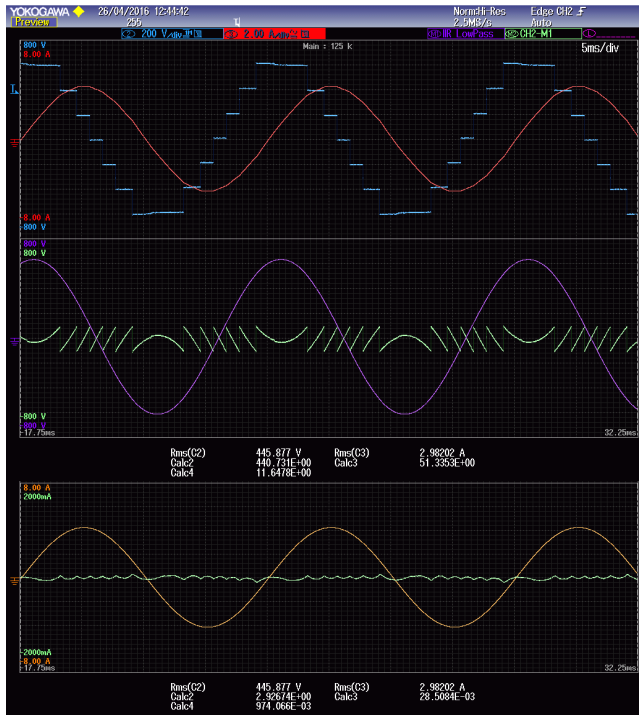


Figure 3.27 (b). Minimized voltage and current THDs experimentally obtained for a single-phase seven-level inverter (three cascaded H-bridges) with respect to Figure 3.16.: test point (f) - $m = 3.144$ ($\alpha_1 = 0.160$, $\alpha_2 = 0.495$, $\alpha_3 = 0.925$).

Considering the oscilloscope screenshots which present the experimental results, it can be noticed that on the top of each screenshot the scales of waveforms are displayed in the colours which correspond to the waveform colours. Also, on the left side of all screenshots there are full-range scales with the same colours. The description of those waveforms is given in the first half of Table 3.3.: load voltage (blue trace) - scope channel 2, labelled C2 (CH2), load current (red trace) - scope channel 3, labelled C3 (CH3), the top half screen; fundamental of load voltage (purple trace), labelled M1, and voltage ripple (green trace), labelled M2: CH2−M1, are depicted in the bottom half-screen of Figures 3.27. and 3.29; fundamental of load current (orange trace), labelled M1 and current ripple (green trace, magnified by 4), labelled M2: CH3−M1, are depicted in the bottom half-screen of Figures 3.28. and 3.29. It must be noted that while calculating the voltage THD, mathematical functions M1 and M2 are applied to the voltage waveform, while, instead, calculating the current THD they are applied to the current waveform.

Table 3.3. Waveforms' parameters calculated by the scope built-in advanced mathematical functions. RMS: root mean square.

Label	Description	Signal waveforms and calculated parameters
C2	Scope channel 2, CH2	Load voltage
C3	Scope channel 3, CH3	Load current
M1	Math function 1: IIR low pass filter	Fundamental voltage (current)
M2	Math function 2: CH2(CH3)−M1	Ripple voltage (current)
Rms(C2)	Math function RMS on CH2	Total voltage *RMS*
Rms(C3)	Math function RMS on CH3	Total current *RMS*
Calc2	Built-in math calculation 2	Fundamental voltage (current) *RMS*
Calc3	Built-in math calculation 3	Ripple voltage (current) *RMS*
Calc4	Built-in math calculation 4	Voltage (current) THD(%) calculated as: $THD_{V(I)}(\%)=\frac{V(I)_{rms,ripple}}{V(I)_{rms,fund}}\cdot 100=\frac{Rms(\mathrm{M2})}{Rms(\mathrm{M1})}\cdot 100$

Fundamental components were determined by built-in scope infinite impulse response (IIR) filter function (M1), and ripple components were calculated as the difference between the instantaneous waveforms and the corresponding fundamental components (M2 = CH2(3)−M1). THDs are determined as the ratio between the ripple root mean square (RMS) and the fundamental RMS. Specific calculation of RMS and THD for all voltage and current waveforms were carried out by the scope built-in advanced mathematical functions in real time and displayed on the bottom lines of the scope screen. Corresponding designations with the calculation of voltage (current) THD are presented in the second part of Table 3.3.

Summary of the experimental tests regarding voltage and current THD is given in Table 3.4.

Table 3.4. Voltage and current THDs for six selected test points obtained by experiments

Test Point	Minimized THD_V (%)	Test Point	Minimized THD_I (%)	Test Point	Minimized THD_V (%)	Minimized THD_I (%)
(a)	18.21	(c)	1.43	(e)	18.28	1.83
(b)	11.55	(d)	2.03	(f)	11.65	0.97

3.7 Comparison of analytical, simulation and experimental results

Analytical calculations of the voltage and current THDs must be compared with simulation and experimental results in order to present their correctness.

The experimental results (*Exp.*) are summarized in Tables 3.5., 3.6. and 3.7., and compared with both theoretical calculations (*Calc.*) and simulation results (*Sim.*) obtained by Matlab/Simulink.

Table 3.5. Minimized voltage THD - specific cases.

Test Point	Minimized THD_V (%)			
	m	***Calc.***	***Sim.***	***Exp.***
(a)	2.459	18.50	18.49	18.21
(b)	3.193	11.53	11.52	11.55

Table 3.6. Minimized current THD - specific cases.

Test Point	Minimized THD_I (%)			
	m	***Calc.***	***Sim.***	***Exp.***
(c)	2.221	1.29	1.31	1.43
(d)	2.663	1.93	1.96	2.03

Table 3.7. Minimized voltage and current *THD*s - same switching angles.

Test Point	***m***	Minimized THD_V (%)			Minimized THD_I (%)		
		Calc.	***Sim.***	***Exp.***	***Calc.***	***Sim.***	***Exp.***
(e)	2.494	18.43	18.41	18.28	1.54	1.79	1.83
(f)	3.144	11.65	11.64	11.65	0.81	0.82	0.97

Tables 3.5. and 3.6. present four cases corresponding to Figures 3.25. and 3.26. It is noticeable that calculated, simulated, and experimental *THD*(%) values match well in the case of the minimized voltage THD (Table 3.5.). In the case of the minimized current THD (Table 3.6.), calculated and simulation values match well, and the experimental values are slightly higher due to the very small current ripple, that emphasizes the measuring errors such as current probe errors and inverter nonlinearities (switching losses, dead-time, etc). Corresponding slight errors have been observed introducing similar nonidealities in the simulation tests.

Table 3.7. presents two cases (e) and (f) (Figure 3.27.), where the same three switching angles result in optimizing both the voltage and the current THDs, corresponding to the same modulation index, as shown in Figure 3.16. As expected, the experimental voltage THD results match almost perfectly both theoretical and simulated results, while the current THD results have slightly higher values, due to similar aforementioned reasons.

In general, the very slight difference between (ideal) simulations and calculated theoretical results in case of current THD can be justified considering that the *RL*-load is not purely inductive. In the specific test cases, the load impedance angle is about 81°, slightly lower than the theoretical angle of 90°. This difference introduces an acceptably small error due to the high current THD sensitivity, proving the effectiveness of the assumption of inductively dominant load. On the whole, simulation and experimental results match the theoretical ones in a satisfactory way.

3.8 Grid-connected single-phase multilevel inverter

3.8.1 Grid current THD evaluation

The previous analysis aims at calculating the current THD for pure inductive loads (voltage WTHD) and the results are practically applicable to inductively dominant *RL* loads. A similar analysis can be carried out for a grid-connected inverter application as well, considering a link inductor *L* with its inner resistance *R*. One grid-connected single-phase configuration is presented in Figure 3.28.

In order to obtain the maximum transferred power to the electrical grid at a given magnitude of the grid current, the current must be in phase with the corresponding grid voltage, as it is shown in the phasor diagram in Figure 3.29.

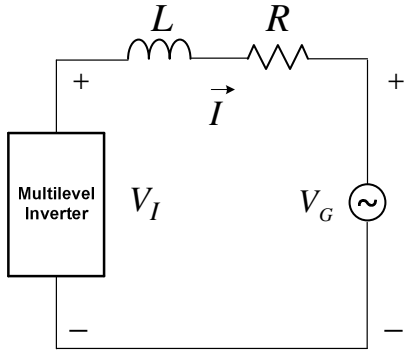


Figure 3.28. Single-phase multilevel inverter connected to the single-phase grid by a link inductor.

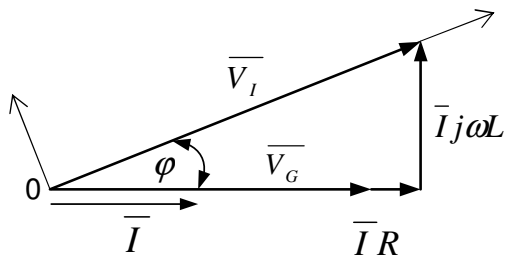


Figure 3.29. Phasor diagram for maximum transferred power.

According to Figure 3.29., the inverter voltage parameters are:

$$V_I = \sqrt{(V_G + RI)^2 + (\omega LI)^2} \ . \tag{3.49}$$

$$\varphi = -\arctan\left(\frac{\omega LI}{V_G + RI}\right). \tag{3.50}$$

For the link inductor, the resistive part in equations (3.49) and (3.50) can be neglected (i.e. $\omega L >> R$), leading to:

$$V_I = \sqrt{{V_G}^2 + (\omega LI)^2} \,. \tag{3.51}$$

$$\varphi = -\arctan\left(\frac{\omega LI}{V_G}\right). \tag{3.52}$$

For grid-connected applications, the voltage modulation index for zero current can be defined as:

$$m_G = \frac{V_G}{V_{dc}}. \tag{3.53}$$

According to (3.51) and (3.53), the modulation index m is:

$$m = \sqrt{m_G^2 + \left(\frac{\omega LI}{V_{dc}}\right)^2} \,, \tag{3.54}$$

where V_{dc} is the converter dc bus voltage, and V_G and I are the grid voltage and grid current amplitudes, respectively. Accordingly, the current THD becomes:

$$THD_{I,grid}^{n}(\%) = \sqrt{\frac{2NMS_I^n\left(\beta_1,\beta_2,...,\beta_{\frac{n-1}{2}},m\right)}{m^2 - m_G^2}} \cdot 100 \,. \tag{3.55}$$

Introducing (3.54) into (3.55) gives the current THD formula for a grid-connected single-phase n-level inverter:

$$\begin{aligned} THD_{I,grid}^{n}(\%) &= \frac{V_{dc}}{\omega LI}\sqrt{2NMS_I^n\left(\beta_1,\beta_2,...,\beta_{\frac{n-1}{2}},m\right)} \cdot 100 \approx \\ &\approx \frac{V_{dc}}{\omega LI}\sqrt{2NMS_I^n\left(\beta_1,\beta_2,...,\beta_{\frac{n-1}{2}},m_G\right)} \cdot 100 \,. \end{aligned} \tag{3.56}$$

Introducing the optimal current switching angles, used in the previous chapter, it is possible to present the current THD over the whole modulation index range with up to five cascaded H-bridges. Selecting R and L as 0.5Ω and 43.3mH, respectively, the dc bus voltage 200V and the fundamental amplitude current 5A (fundamental frequency f_f=50Hz), the grid current THD value calculated by (3.56) over the modulation index range is presented in Figure 3.30.

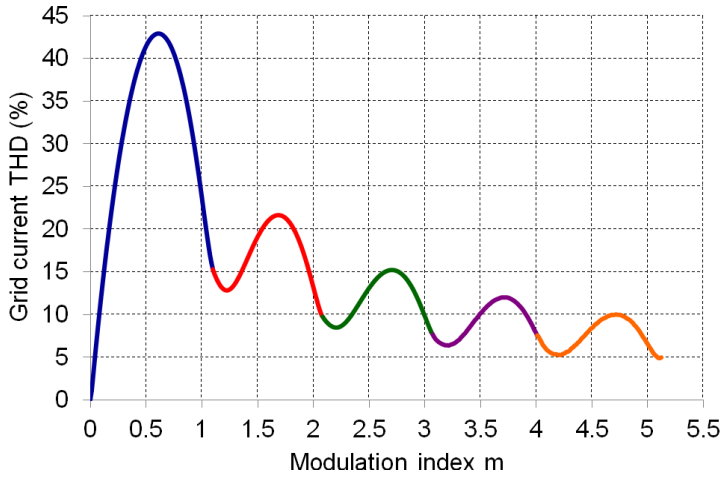


Figure 3.30. Optimized grid current total harmonic distortion (THD) vs. modulation index *m* for *n* = 11 (up to five cascaded H-bridges).

According to Figure 3.30. it can be noticed that for every inter-level modulation index range (0-1, 1-2, ...) the grid current THD has a local minimum value within the first half of the mentioned range, and its maximum within the second half.

Three different values of the modulation index *m* can be chosen following three different configurations – one H-bridge, two cascaded H-bridges and three cascaded H-bridges. In this case, obtained results for the grid current THD can be compared with the simulation ones in the next subchapter. For one H-bridge the modulation index which corresponds to the maximum grid current THD is *m*=0.608. For two cascaded H-bridges the value of *m* which belongs to the half grid current THD range can be one test point i.e. *m*=1.432, and for the third configuration when *m*=2.215 the minimum grid current THD appears.

These points with their characteristics are presented in Table 3.8.

Table 3.8. Grid-connected single-phase inverter – specific cases

Case	***m***	α_1 [rad]	α_2 [rad]	α_3 [rad]	$THD_{I,grid}$ (%)
I	0.608	1.073	/	/	42.90
II	1.432	0.347	1.385	/	17.27
III	2.215	0.225	0.766	1.533	8.43

3.8.2 Simulation of a grid-connected single-phase multilevel inverter

In order to verify the analytical expression for calculating the grid current THD, Matlab/Simulink simulations were carried out. Three previously selected values of the modulation index m are implemented using Matlab/Simulink. Apart from this it is important to define the grid parameters with respect to the selected working points - amplitude of the grid voltage V_G and its phase angle φ. The definition of these parameters is based on the necessity of the grid voltage being in phase with the grid current. Following the phasor diagram presented in Figure 3.29., simple relations between the inverter voltage fundamental component, grid voltage and angle φ can be written.
The amplitude of the inverter output voltage is:

$$V_I = mV_{dc}. \tag{3.57}$$

The angle φ can be calculated using a simple trigonometric relation leading to:

$$\varphi = -\arcsin\left(\frac{\omega LI}{mV_{dc}}\right). \tag{3.58}$$

Calculating φ and taking into account the voltage drop on the resistor R, the required amplitude of the grid voltage fundamental component is:

$$V_G = mV_{dc}\cos(\varphi) - RI. \tag{3.59}$$

Using the parameters set previously, three selected cases for three different H-bridges configurations together with the corresponding calculations are given in Table 3.9.

Table 3.9. Grid-connected single-phase inverter – selected cases for the simulation verification.

Case	*m*	α_1 [rad]	α_2 [rad]	α_3 [rad]	V_I [V]	φ [rad]	V_G [V]
I	0.608	1.073	/	/	121.6	- 0.593	98.30
II	1.432	0.347	1.385	/	286.4	- 0.240	275.70
III	2.215	0.225	0.766	1.533	443	- 0.154	435.21

The implemented configuration with three cascaded H-bridges (single-phase seven-level inverter) in Matlab/Simulink is presented in Figure 3.31.

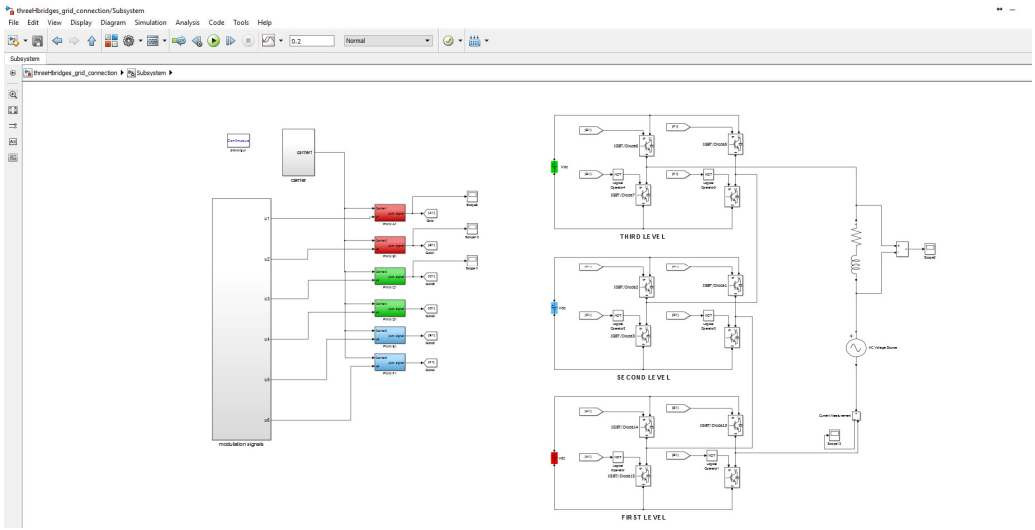


Figure 3.31. Matlab/Simulink model of a single-phase seven-level inverter with three cascaded H-bridges controlled by the staircase modulation technique and connected to the electrical grid.

Grid voltage together with the grid current is presented in Figure 3.32. for case III. For other cases graphical representations are similar, therefore they are not presented here.

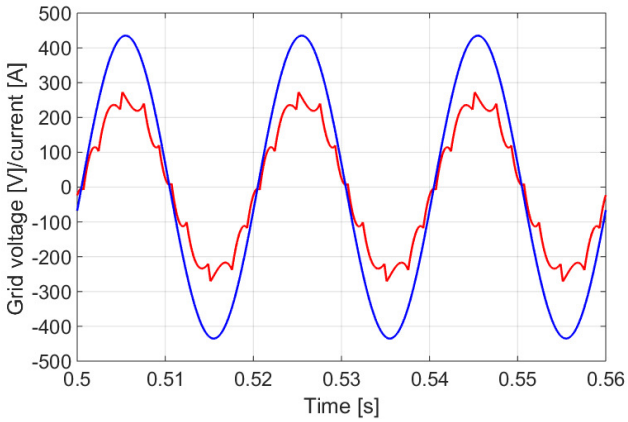
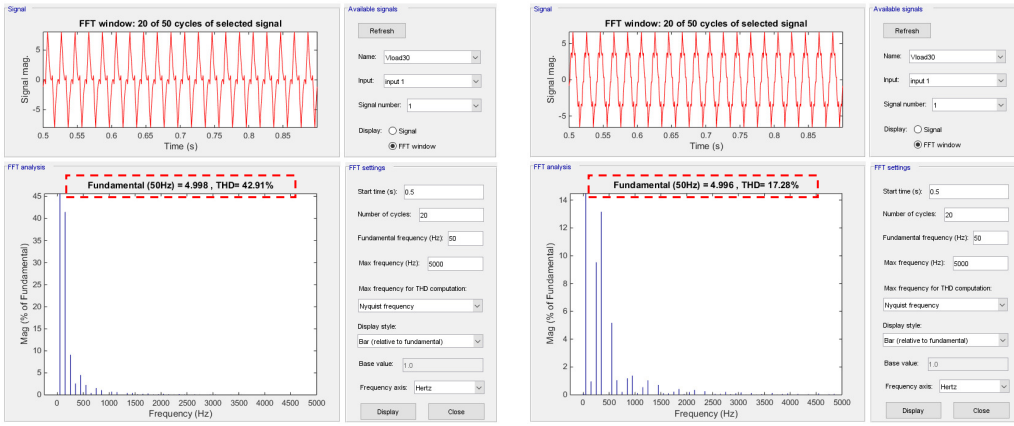


Figure 3.32. Grid voltage (blue) and current (50x, red) obtained by Matlab simulation for a single-phase seven-level inverter (three H-bridges) with respect to Figure 3.30.: m = 2.215, and α_1 = 0.225, α_2 = 0.766 and α_3 = 1.533.

Running the simulation and applying the FTT analysis for the grid current in all three selected cases (m=0.608, 1.432 and 2.215) give the simulation evaluation of the grid current THDs. These results are presented in Figure 3.33. and emphasised with the red rectangle.



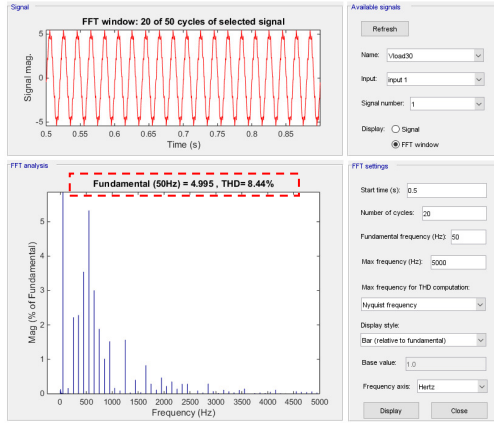


Figure 3.33. Grid current THD obtained by Matlab simulation for a single-phase three-, five- and seven-level inverter (up to three cascaded H-bridges) with respect to Figure 3.30.:
(**a**) $m = 0.608$ ($\alpha_1 = 1.073$, $\alpha_2 = 1.571$, $\alpha_3 = 1.571$);
(**b**) $m = 1.432$ ($\alpha_1 = 0.347$, $\alpha_2 = 1.385$, $\alpha_3 = 1.571$);
(**c**) $m = 2.215$ ($\alpha_1 = 0.225$, $\alpha_2 = 0.766$, $\alpha_3 = 1.533$).

Every simulation comprises 50 fundamental periods and 20 of them are taken for the grid current THD evaluation starting after 25 periods in order to avoid the current transient at the beginning of the simulation process.

3.8.3 Comparison of analytical and simulation results for a grid connected single-phase inverter

In order to prove the correctness of the analytical approach, the comparison between analytical (*Calc.*) and simulation (*Sim.*) results was carried out and presented in Table 3.10.

Table 3.10. Grid current THD – analytical and simulation results.

Case	*m*	$THD_{I,grid}$ (%)	
		Calc.	*Sim.*
I	0.608	42.90	42.91
II	1.432	17.27	17.28
III	2.215	8.43	8.44

Following those results, it can be seen that the analytical and simulation results almost perfectly match each other without any particular deviation which would introduce an error.

3.9 Discussion

Minimal voltage and current THDs for a single-phase multilevel inverter with uniformly distributed voltage levels are formulated as constrained optimization ones in time the domain, considering all switching harmonics. The current THD is considered in a pure inductive load approximation (corresponding to voltage frequency weighted THD, WTHD). Comparing with minimal voltage THD time-domain problem formulations reported previously, the minimal current THD time-domain problem formulation is a novel one. It becomes feasible due to analytical closed-form symbolic calculations of piecewise linear current waveform mean squares.

The numerical solutions establish theoretical calculation of voltage and current THD lower bounds for a single-phase multilevel inverter with a staircase modulation. Optimal switching angles and minimal voltage and current THDs were reported for different multilevel inverter cell numbers (different voltage level counts) and overall modulation index dynamic range. All calculations for optimal switching angles are quite simple and require a negligible processor time because they can be easily calculated offline and called from the microcontroller memory. Also, every microcontroller can perform a simple linear interpolation, thus high accuracy of the modulation index is not needed and, therefore, neither is its real-time calculation.

Over every inter-level modulation index interval, there are two working points which represent the set of switching angles where the optimal voltage and current THD are achieved. Modulation indexes which correspond to those two working points are the so-called twice-optimal modulation indices.

It is shown that optimal voltage THD solutions have relatively low sensitivity to switching angles variations and other disturbances. On the other hand, sensitivity of current optimal solutions is relatively high due to a fine piecewise linear optimal approximation which is much more susceptible to possible disturbances compared with a coarse piecewise constant optimal approximation.

In the case of grid-connected applications, the normalized current fundamental component is typically about 10 times smaller than the voltage modulation index. Accordingly, the THD value of the grid-connected current increases in the same proportion (due to the inverse proportion between the current THD and the normalized current magnitude), comparing with the case when there is an inductively dominant load. This comparison is valid for the same modulation indexes for both practical cases. It is shown that only about 10% of modulation index variations may cause around 100% of current THD changes. Considering this, there is a possibility for precisely defining the optimal working points where the current THD is minimal and controlling in parallel the dc bus and grid voltage variations.

Theoretical findings are followed by computer simulations, in case of the passive *RL*-load and the grid connection, and a wide set of laboratory verification. Experimental results confirm the correctness of the proposed mathematical approach for pure inductively dominant load for voltage and current THD calculations.

3.10 References

[3.1] J. Rodríguez, S. Bernet, B. Wu, J. O. Pontt, S. Kouro, "Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, 2007.

[3.2] G. Buticchi, D. Barater, E. Lorenzani, C. Concari, and G. Franceschini, "A Nine-Level Grid-Connected Converter Topology for Single-Phase Transformerless PV Systems," *IEEE Trans. Ind. Electron.*, vol. 61, no. 8, pp. 3951–3960, 2014.

[3.3] L. Tarisciotti, P. Zanchetta, A. Watson, S. Bifaretti, and J. C. Clare, "Modulated Model Predictive Control for a Seven-Level Cascaded H-Bridge Back-to-Back Converter," *IEEE Trans. Ind. Electron.*, vol. 61, no. 10, pp. 5375–5383, 2014.

[3.4] A. Mora, P. Lezana, and J. Juliet, "Control Scheme for an Induction Motor Fed by a Cascade Multicell Converter Under Internal Fault," *IEEE Trans. Ind. Electron.*, vol. 61, no. 11, pp. 5948–5955, 2014.

[3.5] A. Ruderman, B. Reznikov, and S. Busquets-Monge, "Asymptotic Time Domain Evaluation of a Multilevel Multiphase PWM Converter Voltage Quality," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1999–2009, 2013.

[3.6] D. G. Holmes and T. A. Lipo, Pulse Width Modulation for Power Converters: Principles and Practice. Hoboken, NJ: Wiley, 2003.

[3.7] J. N. Chiasson, L. M. Tolbert, K. J. Mckenzie, and Z. Du, "Elimination of Harmonics in a Multilevel Converter Using the Theory of Symmetric Polynomials and Resultants," *IEEE Trans. Control System Technol.*, vol. 13, no. 2, pp. 216–223, 2005.

[3.8] Z. Du, L. M. Tolbert, J. N. Chiasson, and B. Ozpineci, "Reduced Switching-Frequency Active Harmonic Elimination for Multilevel Converters," *IEEE Trans. Ind. Electron.*, vol. 55, no. 4, pp. 1761–1770, 2008.

[3.9] C. Buccella, C. Cecati, M. G. Cimoroni, and K. Razi, "Analytical Method for Pattern Generation in Selective Harmonic Elimination," *IEEE Trans. Ind. Electron.*, vol. 61, no. 11, pp. 5811–5819, 2014.

[3.10] M. S. A. Dahidah, G. Konstantinou, and V. G. Agelidis, "A Review of Multilevel Selective Harmonic Elimination PWM : Formulations, Solving Algorithms , Implementation and Applications," *IEEE Trans. Power. Electron.*, vol. 30, no. 8, pp. 4091–4106, 2015.

[3.11] *IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems*, IEEE Standard 519-1992, 2004.

[3.12] B. Diong, "THD-Optimal Staircase Modulation of Single-Phase Multilevel Inverters," in *Proc. IEEE Region 5 Conference*, San Antonio, TX, USA, April 2006. pp. 275–279.

[3.13] B. Diong, H. Sepahvand, and K. A. Corzine, "Harmonic Distortion Optimization of Cascaded H-Bridge Inverters Considering Device Voltage Drops and Noninteger DC Voltage Ratios," *IEEE Trans. Ind. Electron.*, vol. 60, no. 8, pp. 3106–3114, 2013.

[3.14] C.A.L. Espinosa, I. Portocarrero, and M. Izquierdo, "Minimization of THD and angles calculation for multilevel inverters," *Int. Journal of Eng. and Technology IJET-IJENS*, vol. 12, no. 5, pp. 83-86, Oct. 2012.

[3.15] F. L. Luo "Investigation on Best Switching Angles to Obtain Lowest THD for Multilevel DC/AC Inverters," in *IEEE 8th Conference on Industrial Electronics and Applications (ICIEA)*, Melbourne, Australia, 2013, pp. 1814–1818, 2013.

[3.16] E. E. Espinosa, J. R. Espinoza, P. E. Melín, R. O. Ramírez, F. Villarroel, J. A. Muñoz, and L. Morán, "A New Modulation Method for a 13-Level Asymmetric Inverter Toward Minimum THD," *IEEE Trans. Ind. App.*, vol. 50, no. 3, pp. 1924–1933, 2014.

[3.17] V. Roberge, M. Tarbouchi, and F. Okou, "Strategies to Accelerate Harmonic Minimization in Multilevel Inverters Using a Parallel Genetic Algorithm on Graphical Processing Unit," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5087–5090, 2014.

[3.18] M. Srndovic, Y. Familiant, G. Grandi and A. Ruderman: "Time Domain Minimization of Voltage and Current Total Harmonic Distortion for a Single-Phase Multilevel Inverter with a Staircase Modulation," *Energies*, vol. 9, no. 10, p. 815, 2016.

[3.19] K. Koishybay, Y. L. Familiant, and A. Ruderman, "Minimization of Voltage and Current Total Harmonic Distortion for a Single-Phase Multilevel Inverter Staircase Modulation," in *9th International Conference on Power Electronics (ICPE-ECCE Asia)*, Soeul, South Korea, 2015 pp. 1203–1208.

[3.20] T. A. Lipo, "An Improved Weighted Total Harmonic Distortion Index for Induction Motor Drives,". in *Aegean Conference on Electrical Machines & Power Electronics,* Brasov, Romania, 2000, pp. 311-322.

4 Power quality evaluation of a single-phase cascaded multilevel inverter with PWM technique

4.1 Introduction

Multilevel inverters are widely used for medium and high voltage applications. They are capable of generating voltage and current waveforms of improved quality, providing a nominal power increase and having a modular structure, therefore they are relevant to many practical applications such as transport (powering trains, ships, automobiles and other drives), energy conversion (wind, solar), manufacturing and mining [4.1]–[4.3]. There are many different topologies of multilevel inverters that can be used regarding what there are supposed to meet and which application they should be used for. Among them, the most popular ones are diode-clamped (neutral-point clamped), capacitor-clamped (flying capacitor) and cascaded inverters with isolated input dc sources [4.4]–[4.9]. Every mentioned topology can be controlled by many different modulation techniques [4.10]–[4.12].

Over the past 20 years, power electronics researchers have shown a significant interest in total voltage and current distortions (THDs) analysis of multilevel inverters. Many recent publications deal with voltage and current THD evaluations following the analytical frequency domain approach [4.13]–[4.16], which does not bring relatively simple closed-form mathematical expressions and therefore requires mathematically heavy numerical calculations [4.9], [4.16], [4.17]. Additionally, the previous works mostly considered a PWM current harmonic content in harmonic distortion factor (HDF)/additional PWM-induced copper loss analytical calculation context.

A simple closed-form voltage quality approach of multilevel multiphase converters is presented in [4.18]. Derivations of an analytical formula for voltage quality for any number of levels of a PWM multilevel inverter considering the leg voltage is presented in [4.19]. Derivations are based on the integration of the power of the PWM signal in a single switching period over the fundamental period of the signal for an ideal sinusoidal reference leg voltage. Two-level single- and three-phase PWM current quality and related normalized harmonic copper loss (current harmonic loss or harmonic distortion factor) time-domain analyses are presented in [4.9] and originated from [4.20] that assumed pure inductive (inductively dominant) load and almost constant PWM current ripple over a switching period (large ratio between the switching and fundamental frequencies).

For a three-phase case, current harmonic distortion is higher due to zero-sequence voltage presence in line-to-line voltages and varies for different modulation strategies/zero sequences [4.9].

The same type of analysis for two-level multiphase inverters was carried out in [4.21] and [4.22]. Along with PWM converter current distortion factor (THD), researchers are interested in peak-to-peak PWM current ripple characteristics. While peak-to-peak PWM current ripple envelope calculation for a single-phase multilevel inverter is almost simple, it becomes more complex for three- and multiphase ones due to the voltage zero-sequence presence. For a two-level three-phase inverter, peak-to-peak PWM current ripple envelope was first reported in [4.23]. The same for three-phase multilevel inverters was presented in [4.24] and [4.25]. Current ripple comparison for single and dual three-phase inverters used in electrical vehicles is presented in [4.26], while current ripple evaluation in dual three-phase inverter for open-end winding drives is presented in [4.27]. Apart from the output inverter side, researchers are interested in the dc input side evaluating the dc voltage ripple in single-phase inverters [4.28].

In this chapter the simple closed-form asymptotic formulae for estimating the voltage and current qualities, applied to a single-phase multilevel inverter, are presented, taking into account the whole harmonic content and being used for an arbitrary inverter level count. The analysis is carried out in the time domain considering that the ratio between switching and fundamental frequencies is supposed to be (infinitely) large (asymptotic assumption). In fact, asymptotic formulae are practically very accurate for ratios higher than 25-30. In line of principle, the formulae initially obtained for a single-phase inverter are valid for three-phase and multiphase inverters as well because the line-to-line voltage quality is invariable to zero sequence voltage insertion (variation) unless nearest level (nearest virtual space vector) switching is not distorted.

Developed mathematical approach applied to the voltage quality is evaluated in the time domain using the voltage ripple normalized mean squared (NMS) criterion. It is a piecewise continuously differentiable analytical solution and employs only elementary function. This solution is asymptotic in terms of having the ratio between switching and fundamental frequencies infinitely large, as mentioned before. The voltage ripple NMS is obtained by double integration over time of a normalized voltage ripple square - integrations over the switching period and over the fundamental period. This can be roughly understood as the time-domain equivalent of the frequency-domain double Fourier transformation. The same approach is applied to the current quality; its NMS value is obtained by double integration of a normalized current ripple square over the switching and fundamental periods. The current NMS value over the switching period is obtained by integrating the corresponding voltage applied to the load. NMS voltage and current calculations can be easily converted into analytical forms representing their total harmonic distortions (THDs) [4.29], [4.30]. It must be noted that voltage THD, based on the time integration, only depends on the modulation index *m*.

The modulation index represents the ratio between the amplitude of the fundamental component of the output voltage and the input dc voltage of one H-bridge within the cascaded configuration.

In case of grid-connected inverter applications the grid current quality is analytically evaluated following the same approach, and the final expression for the current THD is given depending on the switching frequency, linking grid inductance and grid current amplitude.

The verification of all theoretical developments is carried out by Matlab/Simulink simulations and detailed laboratory experiments.

4.2 Pulse-width modulation technique - PWM

Nowadays, power inverters in many applications are controlled by using carrier-based pulse-width modulation techniques (CB-PWMs). They are quite simple regarding different microcontrollers and have a constant or even variable switching frequency which allows a better control of switching losses. Additionally, there is a possibility of improving the voltage and current harmonic spectra applying different modulation strategies [4.31]–[4.34]. The basic principle of CB-PWMs is based on comparing proper modulating signals with one or more carriers providing the gate signals for power switches.

Modulating signals can be different from one application to another depending on the purpose and requirements of the system. Applying specifically optimized and modified modulation signals, the fundamental output voltage component can be higher compared with the classical sinusoidal modulation using the same configuration in case of continuous PWM [4.35]. Improvement of the current quality in terms of minimizing the current ripple can be achieved in case of discontinuous PWM as well alternatively using different modulating signals [4.36].

The modulating signal is represented by its waveform, frequency and amplitude so-called modulation index m. The waveform of the modulating signal represents the reference of the output voltage fundamental component. It depends on the control technique that is applied to one configuration and can differ significantly, while its frequency usually corresponds to the fundamental frequency of the electrical grid i.e. 50Hz. The modulation index m generally defines the amplitude of the modulating signal, but regarding the output voltage it is the ratio between the amplitude of output voltage fundamental component V_1 and dc bus voltage V_{dc}, defined as:

$$m = \frac{V_1}{V_{dc}}. \tag{4.1}$$

Roughly defining, the maximum value of the modulation index equals the number of H-bridges N in one cascaded configuration, therefore its limits are $0 \le m \le N$.

All power switches turn on and turn off at a speed that is usually defined by the carrier. This is represented by the parameter so-called switching frequency f_s. Considering this, over one switching period every switch turns on and turns off depending on the duty cycle given by the intersection of the modulating signal and the carrier. The general rule says that when the modulating signal is higher than the carrier, the output signal has a logical value 1, otherwise it is 0. Depending on the modulation technique and strategy, this rule can vary as well.

The simplest way of controlling one H-bridge (Figure 4.1.(a)) with the carrier-based PWM technique is presented in Figure 4.1.(b) with the carrier frequency f_s=3kHz, fundamental frequency f_f=50Hz and modulation index m=0.75. This ubiquitous modulation technique is the so-called bipolar PWM technique. In Figure 4.1.(c), a detail of the intersections between the carrier and the modulation signal, emphasised in Figure 4.1.(b), is presented giving a control signal which is supposed to be a gate signal of two diagonal switches. The two others are controlled by the opposite control signal.

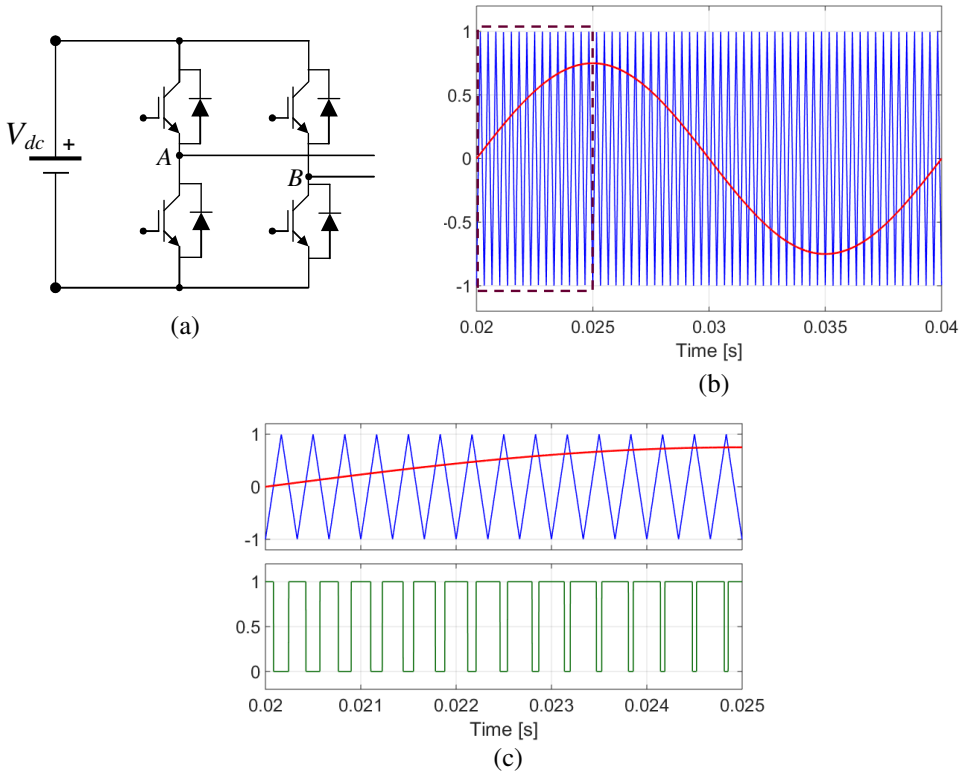


Figure 4.1. (**a**) H-bridge inverter , (**b**) bipolar PWM technique with one 3kHz carrier (blue), one 50Hz modulation signal (red) with m=0.75, and (**c**) a detail of the standard PWM working principle with the corresponding gate signal (green).

Using this modulation technique the output inverter voltage has two levels $\pm V_{dc}$. Since the voltage excursion is relatively high, the total voltage distortion is high as well. In Figure 4.2. the output inverter voltage over one fundamental period (T=20ms) in case of one H-bridge controlled by the bipolar PWM modulation technique is shown. The dc bus voltage is set to V_{dc}=200V, the fundamental and switching frequencies are 50Hz and 3kHz, respectively, and the modulation index is m=0.75.

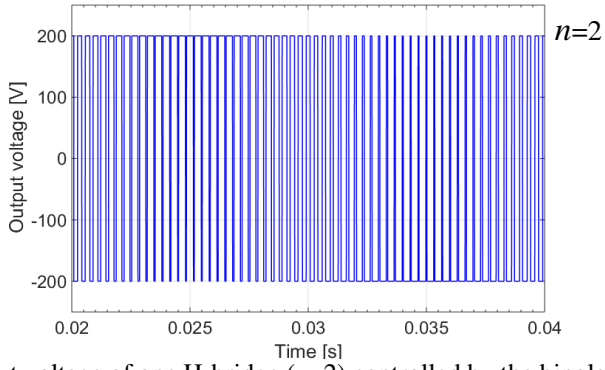


Figure 4.2. Output voltage of one H-bridge (n=2) controlled by the bipolar PWM technique: V_{dc}=200V, f_f=50Hz, f_s=3kHz and m=0.75.

Another ubiquitous modulation technique is the so-called unipolar PWM technique. In case of one H-Bridge, this technique consists of two carriers and one modulating signal, where each carrier corresponds to one H-bridge leg. Considering the same parameters as in the previous case, but introducing one more carrier, the control principle is presented in Figure 4.3., while the inverter output voltage over one fundamental period (T=20ms) is shown in Figure 4.4.

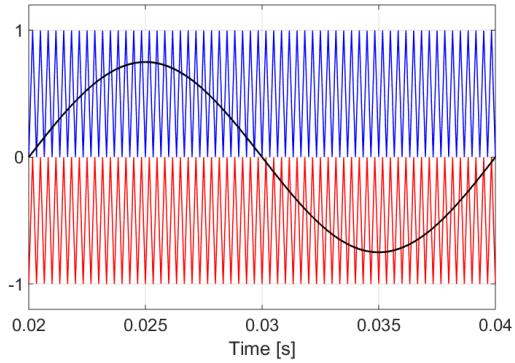


Figure 4.3. Unipolar PWM technique with two carriers and one modulating signal: f_f=50Hz, f_s=3kHz and m=0.75.

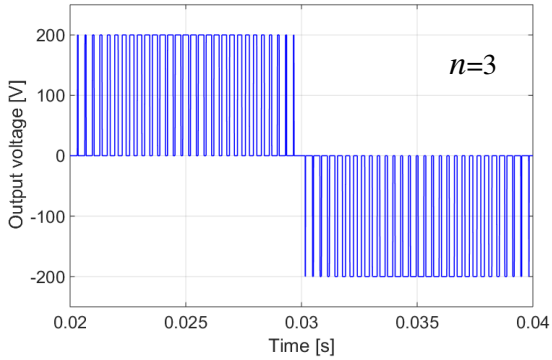


Figure 4.4. Output voltage of one H-bridge (n=3) controlled by the unipolar PWM technique: V_{dc}=200V, f_f=50Hz, f_s=3kHz and m=0.75.

According to Figure 4.4. it can be noticed that the output voltage has three levels 0 and $\pm V_{dc}$. The voltage excursion is lower for this modulation technique leading to better voltage quality. In general, for one H-bridge i.e. three-level inverter, two carriers and one modulation signal are needed, therefore n-1 carriers and one modulation signal are required for properly controlling a single-phase n-level inverter.

In Figures 4.5. and 4.6. the unipolar PWM technique for a single-phase seven-level inverter (0, $\pm V_{dc}$, $\pm 2V_{dc}$, $\pm 3V_{dc}$) with three cascaded H-bridges and its output voltage over three fundamental periods (3T=60ms) are presented. In this case there are six carriers and one modulating. All parameters are the same as previously but the modulation index m is 2.5.

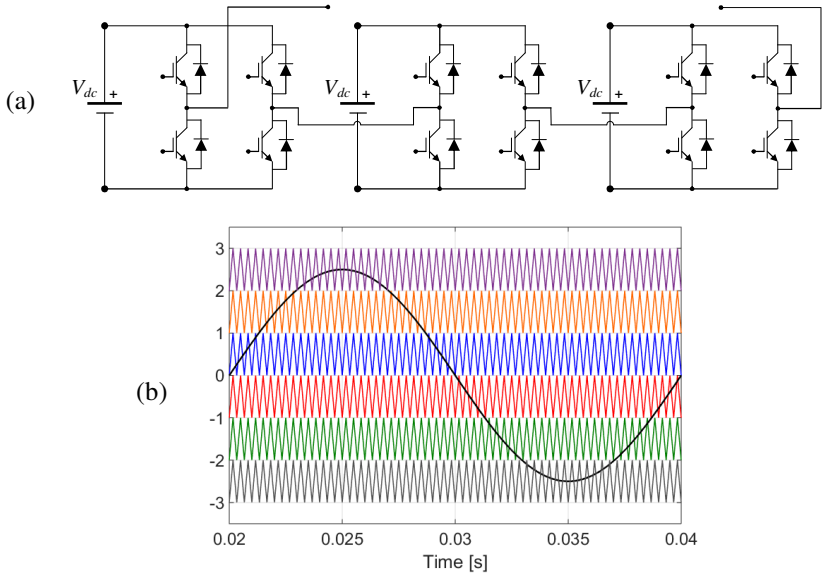


Figure 4.5. (**a**) Single-phase seven-level inverter and (**b**) unipolar PWM technique with six carriers and one modulating signal: f_f=50Hz, f_s=3kHz and m=2.5.

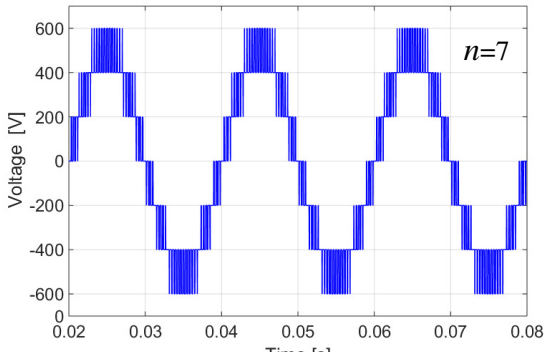


Figure 4.6. Output voltage of three cascaded H-bridges (n=7) over three fundamental periods controlled by the unipolar PWM technique: V_{dc}=200V, f_f=50Hz, f_s=3kHz and m=2.5.

4.3 Voltage and current quality time-domain problem formulation

Ripple analysis of output voltage and output current (hereinafter voltage and current) that is turned into the total harmonic distortion (THD) expression is theoretically based on the assumption that the ratio between switching and fundamental frequencies is infinitely large, as mentioned in the introduction. On the whole, the analysis is divided into two parts for both voltage and current THDs. The first part considers the so-called DC-PWM with constant modulating signal over time and therefore the duty cycle δ lasts equally every equidistant switching period. The second part takes the results obtained by using the DC-PWM and assuming the sinusoidal modulating signal over the fundamental period represents the so-called AC-PWM. In this case the duty cycle δ does not last equally every switching period, but nevertheless, due to the aforementioned assumption it is assumed that the modulation signal has a constant value over a switching period. Both DC and AC-PWM analyses consider the voltage and current normalized mean square (NMS) criteria applied to their ripples and used for estimating their qualities.

All final mathematical expressions are given for an arbitrary number of voltage levels n of a single-phase inverter, considering all harmonics. For calculating either output voltage or output current ripple NMS (hereinafter voltage ripple and current ripple), it is important to distinguish the level number of a single-phase inverter as well as the constant value of the modulating signal (constant duty cycle) (DC-PWM) or the modulation index m (AC-PWM). For example, in case of a single-phase seven-level inverter controlled by AC-PWM with the modulation index m=2.5, the ac voltage/current ripple NMS is calculated for three cases when m is between 0-1, 1-2 and 2-2.5.

Note that the maximum value of m for this kind of inverter using the adopted PWM technique is 3. In general, for a single-phase n-level inverter the maximum possible modulation index $m=(n-1)/2$.

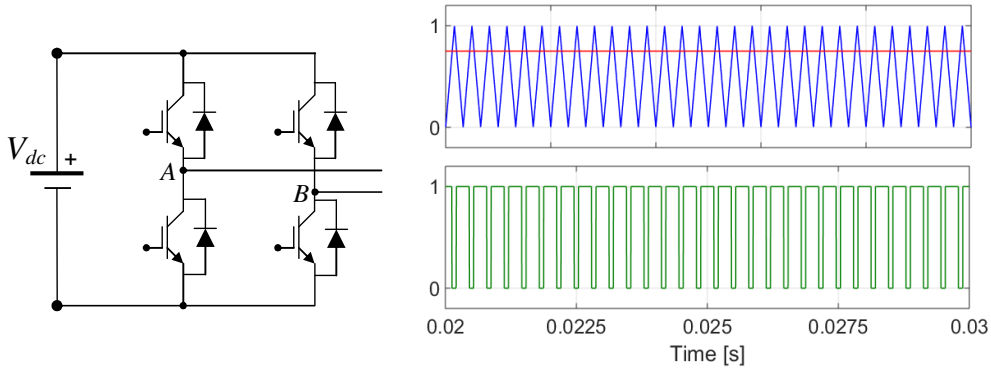
In this case the voltage/current ripple AC-NMS is calculated for each sub-level where $i<m<i+1$, $i=0,\ldots,(n-3)/2$ and summed to get its total value. It is important to mention that when changing the modulation index m, if its maximum belongs to one sub-level which is not the highest possible one, the ac voltage/current ripple NMS is calculated until the last voltage level where the maximum of modulating signal takes part considering the contribution of all preceding sub-levels. Following this, some of H-bridges do not work due to the lack of gate signals.

4.3.1 Voltage ripple NMS criterion and corresponding THD analysis

4.3.1.1 Analytical calculations of DC-PWM NMS voltage ripple

The main aim of analytically estimating the DC-PWM NMS output voltage ripple is to obtain a formula which can be extended to sinusoidal AC-PWM NMS voltage ripple, since in real applications sinusoidal signals are dominant.

The analytical approach starts with the basic single-phase three-level H-bridge inverter controlled by using a simple modulation technique with the constant modulating signal over time, which means that the duty cycle δ lasts equally every switching period. In Figure 4.7.(a), a single-phase three-level inverter is presented. Figure 4.7.(b) shows the suggested modulation technique with the constant modulating signal m=0.75 p.u (red trace), the carrier with frequency f_s set at 3kHz (blue trace) and corresponding gate signal (green trace).



(a) (b)

Figure 4.7. (**a**) Single-phase three-level inverter and (**b**) basic modulation technique with the constant modulating signal m=0.75(red), carrier with f_s=3kHz (blue), and corresponding gate signal (green).

Following the previous configuration, the normalized voltage over one switching period (normalized by the dc bus input voltage V_{dc}) and its corresponding voltage ripple are presented in Figure 4.8.(a) and 4.8.(b), respectively.
It must be noted that the (normalized) voltage ripple is obtained by subtracting the instantaneous (normalized) voltage and its average value i.e. δ.

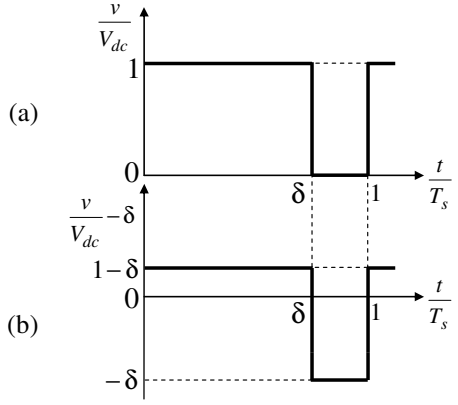


Figure 4.8. (**a**) Normalized voltage over one switching period and (**b**) corresponding normalized voltage ripple for a single-phase three-level inverter in case $0 \le \delta < 1$.

According to Figure 4.8., the voltage ripple DC-NMS criterion for this level voltage count inverter can be calculated by definition as:

$$NMS^{3}_{V,dc} = \frac{1}{T_S}\int_{0}^{T_S}\left(\frac{v^{n=3}}{V_{dc}} - \delta\right)^2 dt\,. \tag{4.2}$$

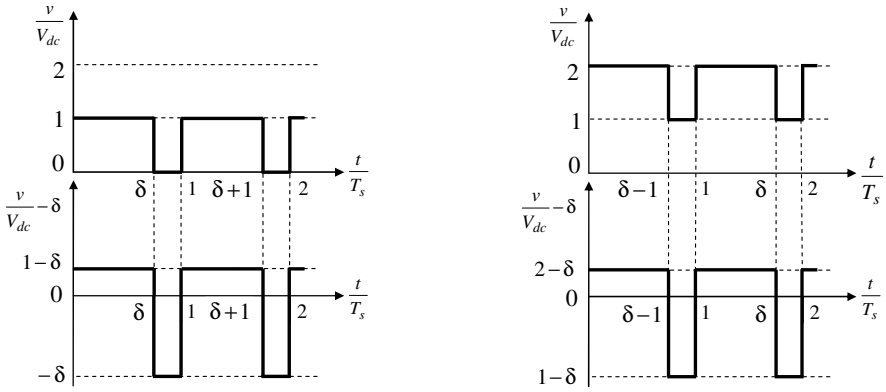
It can be noticed that equation 4.2. presents a squared rms value of the dc voltage ripple. Normalizing (4.2) by T_S, it gives:

$$NMS^{3}_{V,dc} = \int_{0}^{\delta}(1-\delta)^2\,d\delta + \int_{\delta}^{1}(-\delta)^2\,d\delta = \delta(1-\delta),\ 0 \le \delta \le 1\,. \tag{4.3}$$

It must be noted that the parameter δ represents a duty cycle of a single-phase three-level inverter as well as the value of the constant modulating signal (p.u.) using the DC-PWM technique.

The dc normalized voltage ripple over one switching period and its corresponding normalized voltage ripple for a single-phase five-level inverter (two cascaded H-bridges) are presented in Figure 4.9.(a) and (b). In this case there are two possible regions where the NMS value of the dc voltage ripple can be calculated, depending on the value of the constant modulating signal. In the first case, when $0 \le \delta < 1$, it means that the constant modulation signal has a value within those limits and the duty cycle δ, regarding the first H-bridge, is in agreement with them.

In the second case $1 \leq \delta \leq 2$, therefore the constant modulation signal has a value within the limits 1 and 2 and the duty cycle δ, regarding the second H-bridge, lays within them as well. This is important to note because in line of principle the duty cycle cannot have a value higher than 1 that corresponds to 100% of the duration of control signal pulses, but it is defined in the aforementioned way for the analytical developments.



(a) (b)

Figure 4.9. Normalized voltage over one switching period and corresponding normalized voltage ripple for a single-phase five-level inverter in case:
(**a**) $0 \leq \delta < 1$ and (**b**) $1 \leq \delta \leq 2$.

In general, the dc NMS criterion of the voltage ripple in case of a five-level inverter can be expressed as:

$$NMS_{V,dc}^{5} = \frac{1}{T_S} \int_0^{T_S} \left(\frac{v^{n=5}}{V_{dc}} - \delta \right)^2 dt \,. \tag{4.4}$$

If $0 \leq \delta < 1$, Figure 4.9.(a), normalizing (4.4) by T_S and integrating this over one switching period, the dc voltage ripple NMS becomes:

$$NMS_{V,dc}^{5}(0 \leq \delta < 1) = \int_0^{\delta} (1-\delta)^2 \, d\delta + \int_{\delta}^{1} (-\delta)^2 \, d\delta = \delta(1-\delta). \tag{4.5}$$

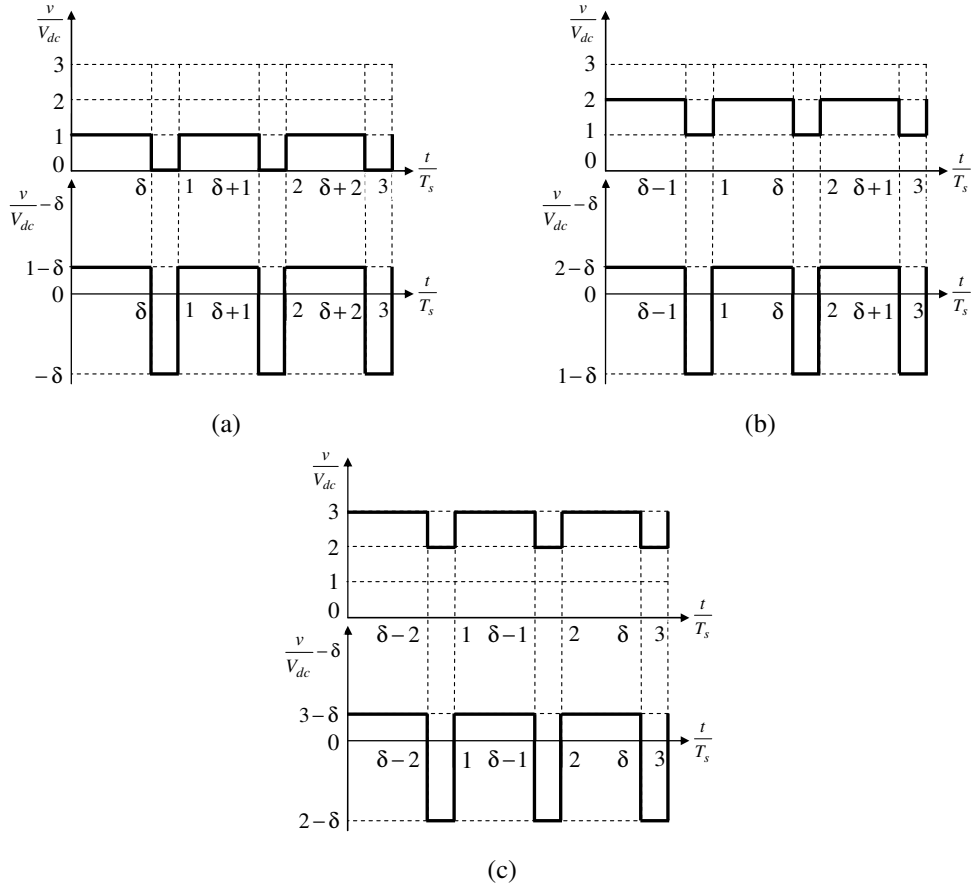
If $1 \leq \delta \leq 2$ (Figure 4.4.(b)), following the same approach, the dc voltage ripple NMS is:

$$NMS_{V,dc}^{5}(1 \leq \delta \leq 2) = \int_1^{\delta} (2-\delta)^2 \, d\delta + \int_{\delta}^{2} (1-\delta)^2 \, d\delta = (\delta-1)(2-\delta). \tag{4.6}$$

According to the previous results, $NMS_{V,dc}^{5}(\delta)$ for a single-phase five-level inverter is:

$$NMS_{V,dc}^{5}(\delta) = \left\{ \begin{matrix} \delta(1-\delta), 0 \leq \delta < 1 \\ (\delta-1)(2-\delta), 1 \leq \delta \leq 2 \end{matrix} \right\}. \tag{4.7}$$

In order to make a general expression of the normalized mean square voltage ripple for an *n*-level inverter, Figure 4.10. presents the case of a single-phase seven-level inverter (three cascaded H-bridges).



(a) (b)

(c)

Figure 4.10. Normalized voltage over one switching period and corresponding normalized voltage ripple for a single-phase seven-level inverter in case:
(**a**) $0 \le \delta < 1$, (**b**) $1 \le \delta < 2$ and (**c**) $2 \le \delta \le 3$.

Considering this inverter, if $0 \le \delta < 1$, (Figure 4.10.(a)), normalizing by T_S, and integrating over one switching period the dc voltage ripple NMS becomes:

$$NMS_{V,dc}^{7}(0 \le \delta < 1) = \int_{0}^{\delta} (1-\delta)^2 \, d\delta + \int_{\delta}^{1} (-\delta)^2 \, d\delta = \delta(1-\delta). \tag{4.8}$$

If $1 \le \delta < 2$, then the corresponding expression is:

$$NMS_{V,dc}^{7}(1 \le \delta < 2) = \int_{1}^{\delta} (2-\delta)^2 \, d\delta + \int_{\delta}^{2} (1-\delta)^2 \, d\delta = (\delta-1)(2-\delta). \tag{4.9}$$

And the last possible case, where the modulating signal corresponds to $2 \le \delta \le 3$, it results in:

$$NMS_{V,dc}^{7}(2 \le \delta \le 3) = \int_{2}^{\delta} (3-\delta)^2 \, d\delta + \int_{\delta}^{3} (2-\delta)^2 \, d\delta = (\delta-2)(3-\delta). \tag{4.10}$$

According to the previous results, for a single-phase single-level inverter the dc voltage ripple $NMS_{V,dc}(\delta)$ becomes:

$$NMS_{V,dc}^{7}(\delta) = \begin{Bmatrix} \delta(1-\delta), & 0 \le \delta < 1 \\ (\delta-1)(2-\delta), & 1 \le \delta < 2 \\ (\delta-2)(3-\delta), & 1 \le \delta \le 3 \end{Bmatrix}. \tag{4.11}$$

Noticing a common rule of $NMS_{V,dc}(\delta)$ depending on the number of H-bridges and therefore the inverter level count, an expression for the normalized mean square dc voltage ripple of a single-phase *n*-level inverter can be written as:

$$NMS_{V,dc}^{n}(\delta) = (\delta - i)((i+1)-\delta), \;\; i = 0, 1, 2, ..., (n-3)/2, \;\; i \le \delta \le i+1. \tag{4.12}$$

4.3.1.2 Analytical calculations of AC-PWM NMS voltage ripple

As mentioned before, in many real applications the sinusoidal or quasi-sinusoidal PWM techniques are used for controlling multilevel inverters. Regarding this point, the results obtained in the previous chapter can be properly extended in order to calculate the voltage quality of a single-phase multilevel inverter controlled by the PWM technique.

At the first step, it is important to define a duty-cycle δ introducing its sinusoidal function over time:

$$\delta(\theta) = m \sin(\theta). \tag{4.13}$$

In (4.13), $\theta=\omega t$ is the electrical angle and *m* is the modulation index. Depending on the inverter voltage level *n*, the maximum value of *m* is (*n*-1)/2.

According to the previous definition it can be said that the duty cycle will, theoretically, no longer have a constant value over every switching period. It will be changeable following the sinusoidal behaviour of the modulating signal. On the other hand, taking into account the assumption that the carrier (switching) frequency is much higher than the fundamental frequency, the function $\delta(\theta)$ is assumed predominantly constant over the switching period.

In this case, the ac voltage ripple NMS can be obtained by averaging the squared rms voltage ripple over one fundamental period, taking into account (4.12). The calculation of the ac voltage ripple NMS is given by (4.14).

$$NMS_{V,ac}^{n}(t)=\frac{1}{T}\int_{0}^{T}\left(m\sin(\omega t)-i\right)\left((i+1)-m\sin(\omega t)\right)dt,$$
$$i=0,\,1,\,2,\ldots,(n-3)/2,\; i\le m\le i+1. \tag{4.14}$$

In order to have (4.14) given in the angle domain, a simple equality can be written:

$$d\theta=d(\omega t)=\omega\,dt=\frac{2\pi}{T}dt\longrightarrow dt=d\theta\frac{T}{2\pi}. \tag{4.15}$$

Notice that parameters ω and T are given for the fundamental harmonic of the voltage which usually corresponds to the frequency 50Hz, but the index "1" as a subscript is intentionally omitted in order to avoid many subscripts in equations. Introducing the angle domain, the ac voltage ripple NMS can be calculated as:

$$NMS_{V,ac}^{n}(\theta)=\frac{1}{2\pi}\int_{0}^{2\pi}\left(m\sin(\theta)-i\right)\left((i+1)-m\sin(\theta)\right)d\theta,$$
$$i=0,\,1,\,2,\ldots,(n-3)/2,\; i\le m\le i+1. \tag{4.16}$$

The previous equation is integrated over the whole fundamental period. Following the PWM control technique and ac voltage ripple presented in Figure 4.11. for the case of three cascaded H-bridges with single dc bus voltages 200V, it can be noticed that this function has a quarter-wave symmetry. Modulation index is set to m=2.5.

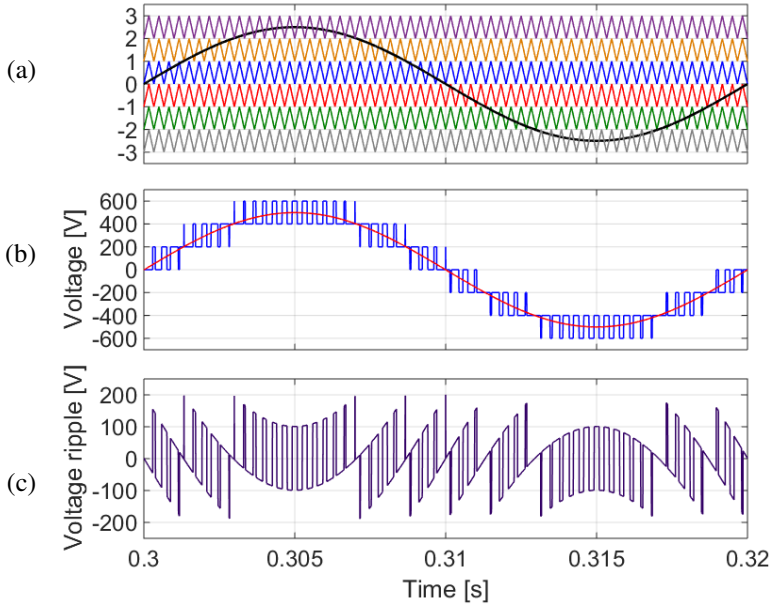


Figure 4.11. (**a**) PWM control technique, (**b**) instantaneous voltage (blue) and its fundamental component (red), (**c**) and instantaneous ac voltage ripple (purple) of a single-phase seven-level inverter with V_{dc}=200V, f_f=50Hz, f_s=3kHz and m=2.5.

Considering the aforementioned symmetry, the expression for the ac voltage ripple NMS can be written as:

$$NMS_{V,ac}^{n}(\theta)=\frac{2}{\pi}\int_{0}^{\pi/2}(m\sin(\theta)-i)\left((i+1)-m\sin(\theta)\right)d\theta, \quad i=0,\,1,\,2,\ldots,(n-3)/2,\; i\le m\le i+1. \tag{4.17}$$

Considering the case of single-phase multilevel inverters and the possibility of having the modulation index m between different (voltage) levels, we can define a generic property of one function $y(x)$, which says that the function has a specific value if some of its parameters are within defined limits, otherwise it has a zero value:

$$y(x)=\left\{\begin{array}{l}(x-x_1)(x_2-x),\; x\in[x_1,x_2]\\ 0,\; x\notin[x_1,x_2]\end{array}\right\}, \quad x_1=0,\,1,\,2,\ldots,(n-3)/2,\; x_2=1,\,2,\ldots,(n-1)/2. \tag{4.18}$$

Limits for the parameters x_1 and x_2 are defined considering the previously derived analytical approach taking into account the inverter voltage level n. Having defined this generic function, it can be said that the expression for calculating $NMS_{V,ac}$ can be divided into two main ones.

One expression considers the case when the modulation index m is between two adjacent (voltage) levels. This case is described by the parameters x_1 and x_2, and none of them presents the maximum possible level considering the full cascaded H-bridges configuration. Another expression presents the case when m is between the maximum possible (voltage) level and the penultimate one. This means that for every two adjacent levels the integral form (4.17) is calculated separately and at the end all in-between-voltage level contributions are summed to get the final value of the ac voltage ripple NMS. Each sub-integral form must have its limits that can be easily defined following Figure 4.12.

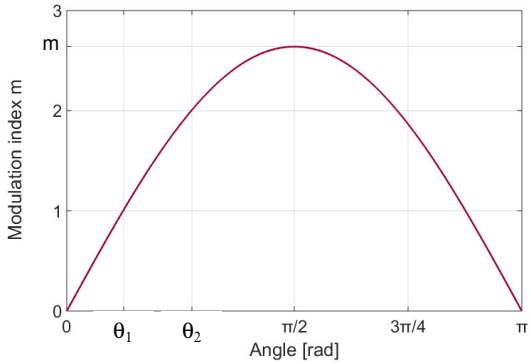


Figure 4.12. Half-fundamental period of the modulating signal (50Hz) defining the limits between adjacent (voltage) levels for a single-phase seven-level inverter and modulation index *m*.

As it can been seen, there are two angles θ_1 and θ_2 which define the proper limits. For this kind of inverter, there are three sub-integral forms that must be calculated in order to get the final ac voltage NMS value. The first one which considers the angle range between 0 and θ_1, the second one with the angle range between θ_1 and θ_2 and the third one with angles θ_2 and $\pi/2$. The first two can be joined into one form introducing a proper variable, while the third one must be calculated separately.

The modulation index *m* is selected arbitrarily between values 2 and 3 in order to explain the proposed algorithm. According to Figure 4.12., it can be written:

$$m\sin(\theta_1)=1\rightarrow\theta_1=\arcsin\left(\frac{1}{m}\right),\ m\sin(\theta_2)=2\rightarrow\theta_2=\arcsin\left(\frac{2}{m}\right). \tag{4.19}$$

For the general case of a single-phase *n*-level inverter, the equation (4.19) becomes:

$$m\sin(\theta_i)=i\rightarrow\theta_i=\arcsin\left(\frac{i}{m}\right),\ m\sin(\theta_{i+1})=i+1\rightarrow\theta_{i+1}=\arcsin\left(\frac{i+1}{m}\right), \tag{4.20}$$
$$i=0,\ 1,\ 2,...,\ (n-5)/2\ .$$

Considering (4.20) and defined limits for the parameter *i*, it must be mentioned that for a single-phase three-level inverter its modulation index *m* is within the range 0-1., Therefore this calculation is not only applicable for this case since there are no sub-voltage levels which contribute to the ac voltage ripple NMS. The same applies in the following equations.

In order to calculate the ac voltage ripple NMS between two adjacent voltage levels, the integral form (4.17) labelled as $a_V^n(m)$ is:

$$a_V^n(m)=NMS_{V,ac}^n(\theta_i\le\theta\le\theta_{i+1})=\frac{2}{\pi}\int_{\theta_i=\arcsin\left(\frac{i}{m}\right)}^{\theta_{i+1}=\arcsin\left(\frac{i+1}{m}\right)}(m\sin(\theta)-i)\left((i+1)-m\sin(\theta)\right)d\theta, \tag{4.21}$$
$$i=0,\ 1,\ 2,...,\ (n-5)/2\ ,\ i\le m\le i+1\ .$$

All steps of the calculation of this integral are given in Appendix 4. The final result of (4.21) is:

$$a_V^n(m)=\frac{3i+2}{\pi}\sqrt{m^2-i^2}-\frac{3i+1}{\pi}\sqrt{m^2-(i+1)^2}+\frac{1}{\pi}\left(\begin{array}{l}\left(2i(i+1)+m^2\right)\cdot\\ \left(\arcsin\left(\frac{i}{m}\right)-\arcsin\left(\frac{i+1}{m}\right)\right)\end{array}\right), \tag{4.22}$$
$$i=0,\ 1,\ 2,...,\ (n-5)/2\ ,\ i\le m\le i+1\ .$$

On the other hand, when the contribution to the ac voltage ripple NMS value comes from the last voltage level, the integral form, labelled as $b_V^n(m)$, becomes:

$$b_V^n(m) = NMS_{V,ac}^n\left(\theta_k \le \theta \le \frac{\pi}{2}\right) = \frac{2}{\pi}\int_{\theta_k=\arcsin\left(\frac{k}{m}\right)}^{\frac{\pi}{2}} (m\sin(\theta)-k)\left((k+1)-m\sin(\theta)\right)d\theta, \tag{4.23}$$

$k = (n-3)/2$, $k \le m \le k+1$.

Solving (4.23) results in:

$$b_V^n(m) = \frac{1}{\pi}(3k+2)\sqrt{m^2-k^2} + \frac{1}{\pi}\left(2k(k+1)+m^2\right)\left(\arcsin\left(\frac{k}{\pi}\right)-\frac{\pi}{2}\right) \tag{4.24}$$

$k = (n-3)/2$, $k \le m \le k+1$.

Detailed steps of solution of (4.24) are given in Appendix 4. It must be noted that the parameter *k* strictly depends on the level count *n* and has only one value because it refers to the last voltage level of one *n*-level single-phase H-bridge inverter. This case is applicable to the single-phase three-level inverter as well. In order to get the final value of the ac voltage ripple NMS, it is needed to properly sum equations (4.22) and (4.24). The proper sum of both equations is:

$$NMS_{V,ac}^n(m) = \sum_{i=0}^{(n-5)/2} a_V^n(m) + b_V^n(m) = \sum_{i=0}^{k-1} a_V^n(m) + b_V^n(m),\ k = (n-3)/2 \tag{4.25}$$

Introducing (4.22) and (4.24) into (4.25) results in:

$$\begin{aligned} NMS_{V,ac}^n(m) = &\sum_{i=0}^{k-1}\left(\frac{3i+2}{\pi}\sqrt{m^2-i^2} - \frac{3i+1}{\pi}\sqrt{m^2-(i+1)^2} + \right.\\ &\left.\frac{1}{\pi}\left(2i(i+1)+m^2\right)\left(\arcsin\left(\frac{i}{m}\right)-\arcsin\left(\frac{i+1}{m}\right)\right)\right)\\ &+\frac{1}{\pi}(3k+2)\sqrt{m^2-k^2} + \frac{1}{\pi}\left(2k(k+1)+m^2\right)\left(\arcsin\left(\frac{k}{\pi}\right)-\frac{\pi}{2}\right),\\ &i = 0, 1, 2, \ldots, (n-5)/2,\ k = (n-3)/2,\ i \le m \le i+1. \end{aligned} \tag{4.26}$$

Detailed solving and grouping steps of (4.26) are given in Appendix 4. The final result of the ac voltage ripple NMS considering all possible inverter voltage levels is:

$$NMS_{V,ac}^n(m) = \begin{cases} -\frac{1}{2}m^2 + \frac{2}{\pi}m,\ 0 \le m \le 1 \\ \frac{4}{\pi}\sum_{i=1}^{k}\left(i\arcsin\left(\frac{i}{m}\right)\right) + \frac{4}{\pi}\sum_{i=1}^{k}\left(\sqrt{m^2-i^2}\right) - \frac{1}{2}m^2 + \frac{2}{\pi}m - k(k+1), \\ i = 1, 2, \ldots, (n-3)/2,\ k = (n-3)/2,\ i \le m \le i+1. \end{cases} \tag{4.27}$$

Setting the parameter k=0 in (4.27) (or in (4.24)), the ac voltage ripple NMS in case of a single-phase three-level inverter with $0 \leq m \leq 1$ is easily obtained. The ac normalized mean square voltage ripple, with respect to the equation (4.27) for the configuration up to five cascaded H-bridges (n=11), is presented in Figure 4.13.

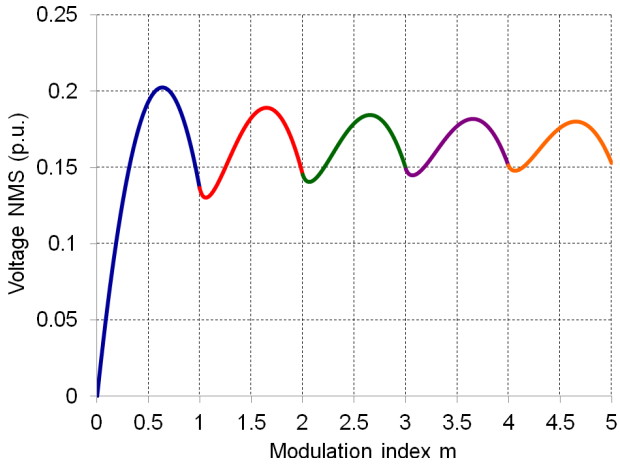


Figure 4.13. Ac voltage ripple normalized mean square for the configuration up to five cascaded H-bridges –single-phase eleven-level inverter (equation (4.27)).

4.3.1.3 Voltage THD as a function of ac voltage ripple NMS criterion

In order to calculate the voltage THD using the ac voltage NMS criterion, simple mathematical calculations can be introduced. Every signal can be expressed as a sum of its fundamental component and other harmonic components:

$$x(t) = x_1(t) + \sum_k x_k(t). \tag{4.28}$$

The total rms square value of the signal $x(t)$ can be written as (Parseval's theorem):

$$X_{rsm}^2 = \frac{1}{T}\int_0^T \left(x_1(t) + \sum_k x_k(t) \right)^2 = X_{1,rsm}^2 + X_{rms,dist}^2 \ . \tag{4.29}$$

Considering (4.29), the formula for the total harmonic distortion of the signal $x(t)$ is:

$$THD_x = \frac{X_{rms,dist}}{X_{1,rsm}}. \tag{4.30}$$

In case of the normalized ac voltage ripple NMS of a single-phase n-level inverter, its normalized rms value is:

$$v_{rms}^n(m) = \sqrt{NMS_{V,ac}^n(m)}. \tag{4.31}$$

Taking into account (4.30) and (4.31), the voltage THD formula can be written as the square root of the normalized ac voltage ripple divided by the normalized fundamental component of the voltage:

$$THD_V^n(\%) = \frac{\sqrt{NMS_{V,ac}^n(m)}}{V_{1,rms,norm}} \cdot 100 = \frac{\sqrt{NMS_{V,ac}^n(m)}}{\frac{mV_{dc}}{\sqrt{2}}\frac{1}{V_{dc}}} \cdot 100 = \frac{\sqrt{2NMS_{V,ac}^n(m)}}{m} \cdot 100\,, \quad (4.32)$$

where $NMS_{V,ac}^n(m)$ is the ac voltage ripple NMS, V_{dc} is the dc bus voltage of each single H-bridge and m is the modulation index.

The voltage THD expression does not depend on any frequency ratio, and it does only depend on the modulation index m and the level count n of a single-phase multilevel inverter. In Figure 4.14., the voltage THD as a function of the modulation index m is presented, considering the configuration up to five cascaded H-bridges, i.e. eleven-level single-phase inverter.

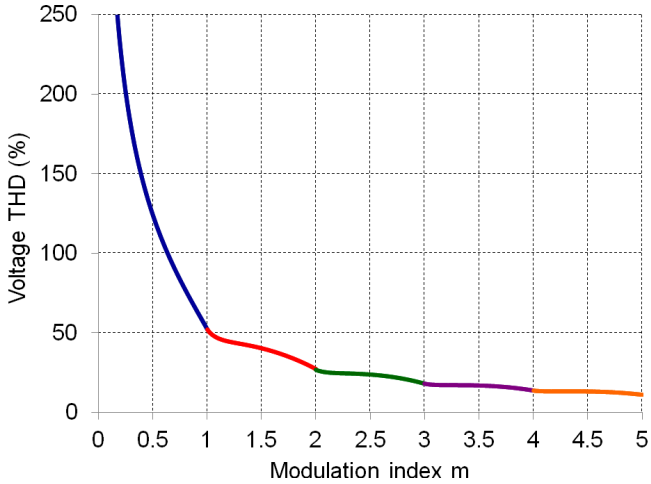


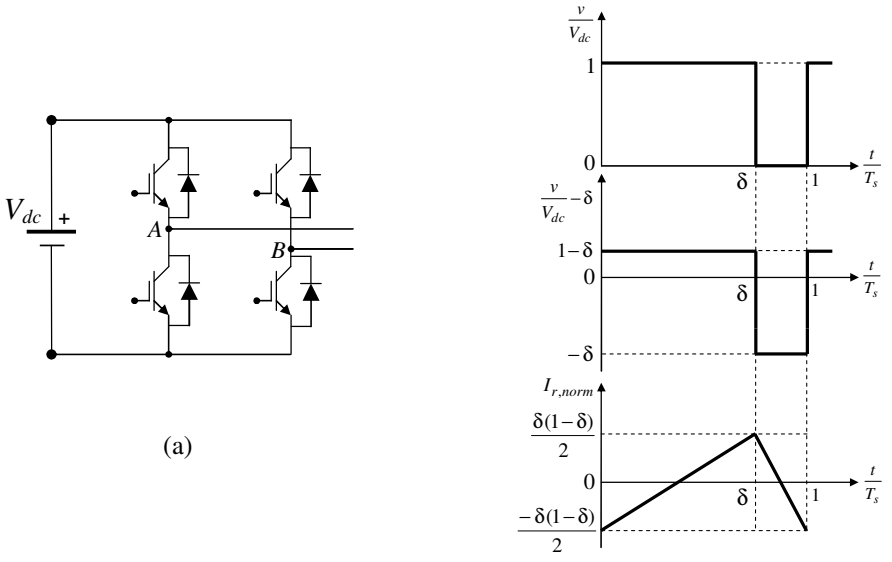
Figure 4.14. Voltage THD(%) as a function of the modulation index m (equation (4.32)) for the configuration up to five cascaded H-bridges – single-phase eleven-level inverter.

4.3.2 Current ripple NMS criterion and corresponding THD analysis

4.3.2.1 Analytical calculations of DC-PWM NMS current ripple

Analytical calculations of DC-PWM NMS current ripple can be performed in a similar way as it is done for the voltage calculations. The normalized dc voltage ripple voltage is applied over the load in order to calculate the corresponding current parameters.

The analytical approach is firstly carried out for the basic single-phase three-level H-bridge inverter, presented in Figure 4.15.(a), controlled by the constant duty cycle over every switching period. In Figure 4.15.(b), normalized voltage over one switching period, corresponding normalized voltage ripple and normalized current ripple are presented.



(a) (b)

Figure 4.15. (**a**) Single-phase three-level inverter and (**b**) normalized voltage over one switching period, corresponding normalized voltage ripple and normalized current ripple for $0 \leq \delta \leq 1$.

The normalized voltage and normalized current ripple are presented in Figure 4.16., with the duty cycle δ=0.75 in correspondence with the ongoing analytical approach. The switching period corresponds to the frequency f_s=3kHz.

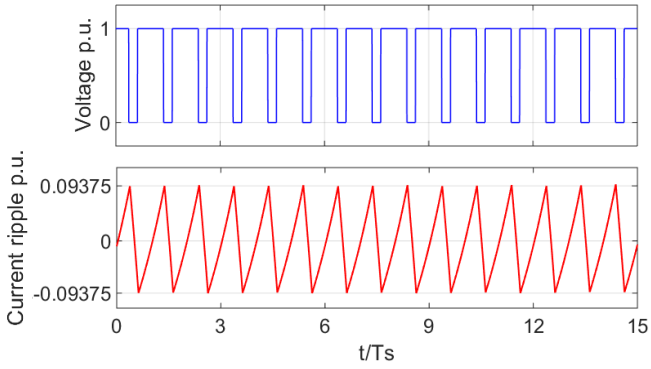


Figure 4.16. Normalized voltage and current ripple of a single-phase three-level inverter with the constant duty cycle δ=0.75 and switching frequency f_s=3kHz.

In general, there are two ways of calculating the ac current ripple NMS. One is an analytical way directly following the diagrams in Figure 4.15.(b), and the other one is the standard way starting from the voltage expression of one inductor.

Using the first way, by time integrating the normalized voltage ripple and adjusting the zero voltage, rms value of the current ripple of a single-phase three-level inverter can be written as:

$$I_{r,rms}^{3} = \frac{\delta(1-\delta)}{2\sqrt{3}}, \tag{4.33}$$

where δ represents the duty cycle and the square root of three results from obtaining the rms value of one triangular signal by dividing its amplitude with this number. Generally, the NMS criterion presents the square of the rms value of one signal, therefore the dc current ripple NMS of the single-phase three-level inverter is:

$$NMS_{I,dc}^{3} = \left(I_{r,rms}^{3}\right)^2 = \frac{\delta^2 (1-\delta)^2}{12}. \tag{4.34}$$

In the second case, the general formula for the instantaneous current ripple of one inductor L over one switching period T_s is:

$$i_{rip}(t) = \frac{1}{L}\int_0^{T_S} v(t)dt = \frac{1}{L}\int_0^{t_{on}} v(t)\,dt + \frac{1}{L}\int_{t_{on}}^{T_S} v(t)\,dt\,, \tag{4.35}$$

where t_{on} represents the duty cycle in the time domain while T_s is the switching period.

In order to estimate the peak-to-peak value of the current ripple, the first part of (4.35) can be taken into account considering that $v(t)=V_{dc}-v^*$, where v^* presents the reference voltage which defines the constant duty cycle. Introducing $v(t)=V_{dc}-v^*$ results in:

$$I_{pp}\left(i_{rip}(t)\right) = \frac{1}{L}\int_0^{t_{on}} \left(V_{dc} - v^*\right)dt = \frac{1}{L}\left(V_{dc} - v^*\right)t_{on}\,. \tag{4.36}$$

The equation (4.36) can be rewritten to obtain the peak-to-peak value of the current ripple as a function of δ:

$$I_{pp}\left(i_{rip}(t)\right) = \frac{V_{dc}}{L}\left(1 - \frac{v^*}{V_{dc}}\right) t_{on}\,\frac{T_s}{T_s} = \frac{V_{dc}\,T_s}{L}\,\delta(1-\delta). \tag{4.37}$$

Equation (4.37) has to be divided by two in order to get the amplitude of the current ripple:

$$\max\left(i_{rip}(t)\right) = \frac{V_{dc}\,T_s}{2L}\,\delta(1-\delta). \tag{4.38}$$

As it was done in the previous case, to get the rms value of the current ripple, here (4.38) is divided by square root of three. This is presented in (4.39).

$$I_{rip,rms}(\delta) = \frac{\max\left(i_{rip}(t)\right)}{\sqrt{3}} = \frac{V_{dc}\,T_s}{2\sqrt{3}\,L}\,\delta(1-\delta). \tag{4.39}$$

According to this, the dc mean square criterion for the current ripple can be written as:

$$MS^{3}_{I,dc} = \left(I_{rip,rms}(\delta)\right)^2 = \left(\frac{V_{dc}\,T_s}{L}\right)^2 \frac{1}{12}\,\delta^2\,(1-\delta)^2\,. \tag{4.40}$$

Normalizing (4.40), the dc current ripple NMS value for a single-phase three-level inverter becomes as in (4.34):

$$NMS^{3}_{I,dc} = \frac{\delta^2\,(1-\delta)^2}{12}\,. \tag{4.41}$$

Since the first approach is easier than the second one, the first one will be considered in the following calculations. Figure 4.17 shows corresponding waveforms in case of a single-phase five-level inverter. The dc current ripple NMS value can be estimated considering two different regions. According to Figure 4.17. we can distinguish both regions where the duty cycle δ is either $0 \le \delta < 1$ or $1 \le \delta \le 2$, as it was similarly done for the dc voltage ripple NMS.

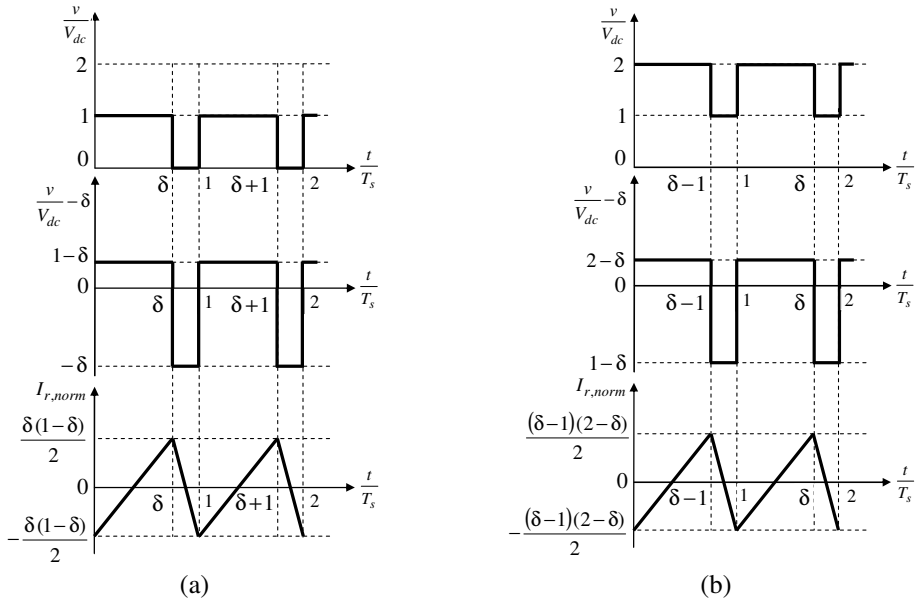


Figure 4.17. Normalized voltage over one switching period, corresponding normalized voltage ripple and normalized current ripple of a single phase five-level inverter when (**a**) $0 \le \delta < 1$, (**b**) $1 \le \delta \le 2$.

In both cases different voltage ripple values are applied over the load and, adjusting the zero average of the dc voltage ripple NMS as it is labelled, two different expressions (4.42) for the dc current ripple NMS as a function of δ can be written.

$$NMS_{I,dc}^{5}(\delta)=\left\{\begin{array}{l}\dfrac{\delta^2(1-\delta)^2}{12},\ 0\le\delta<1\\ \dfrac{(\delta-1)^2(2-\delta)^2}{12},\ 1\le\delta\le 2\end{array}\right\}. \tag{4.42}$$

For a single-phase seven-level inverter corresponding waveforms are shown in Figure 4.18.

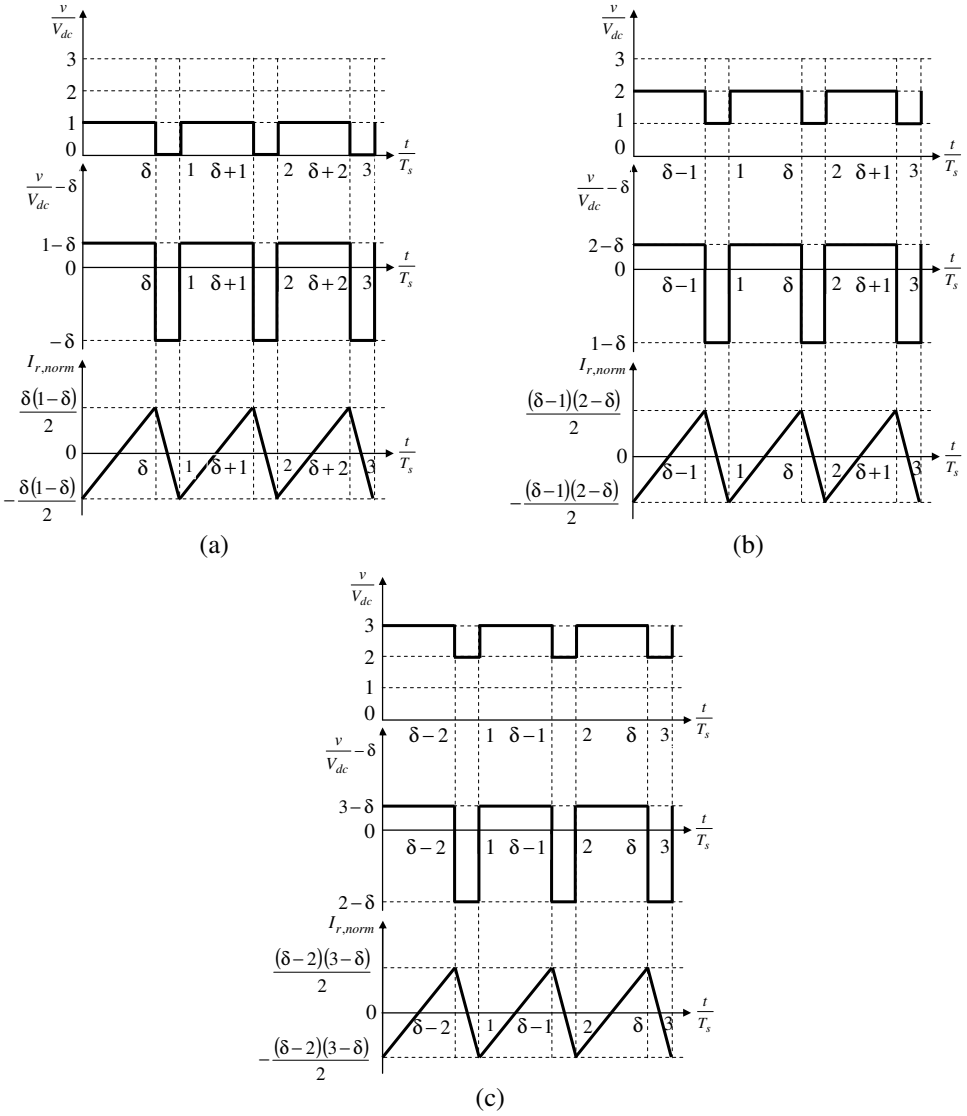


Figure 4.18. Normalized voltage over one switching period, corresponding normalized voltage ripple and normalized current ripple of a single phase seven-level inverter when (**a**) $0 \le \delta < 1$, (**b**) $1 \le \delta < 2$ and (**c**) $2 \le \delta \le 3$.

In order to calculate the dc current ripple NMS the same approach can be used. In this case there are three regions depending on the value of the duty cycle δ. The final expression for all cases is:

$$NMS_{I,dc}^{7}(\delta)=\left\{\begin{array}{l}\dfrac{\delta^2(1-\delta)^2}{12},\ 0\le\delta<1\\ \dfrac{(\delta-1)^2(2-\delta)^2}{12},\ 1\le\delta<2\\ \dfrac{(\delta-2)^2(3-\delta)^2}{12},\ 2\le\delta\le 3\end{array}\right\}. \tag{4.43}$$

Considering the presented cases for the single phase three-, five- and seven-level inverters, a general form for the dc current ripple NMS for a single-phase *n*-level inverter can be written as:

$$NMS_{I,dc}^{n}(\delta)=\frac{(\delta-i)^2\left((i+1)-\delta\right)^2}{12},\ i=0,\,1,\,2,...,\,(n-3)/2,\ i\le\delta<i+1. \tag{4.44}$$

4.3.2.2 Analytical calculations of AC-PWM NMS current ripple

In order to calculate the ac current ripple NMS, a non-constant reference voltage has to be considered. The sinusoidal reference voltage was used for the ac voltage ripple NMS, therefore the same will be assumed now. Within every switching period, the duty cycle δ as a function of the angle θ can be expressed as:

$$\delta(\theta)=m\sin(\theta), \tag{4.45}$$

with θ=ωt and *m* is the defined modulation index representing the ratio between the amplitude of the voltage fundamental component and the inverter dc input voltage. It must be mentioned that the switching frequency is theoretically assumed infinitely larger than the fundamental frequency therefore the results of the dc current ripple NMS can be used for calculating the ac current ripple NMS with the same statement that δ(θ) is predominantly constant over one switching period. Doing so, the ac current ripple NMS can be obtained by averaging the squared current ripple over one fundamental period. The corresponding expression in the time domain is:

$$\begin{aligned}&NMS_{I,ac}^{n}(t)=\frac{1}{12}\frac{1}{T}\int_0^T\left(m\sin(\omega t)-i\right)^2\left((i+1)-m\sin(\omega t)\right)^2\,dt,\\ &i=0,\,1,\,2,...,\,(n-3)/2,\ i\le m\le i+1.\end{aligned} \tag{4.46}$$

In order to have (4.46) given in the angle domain, a simple equality can be written:

$$d\theta=d(\omega t)=\omega dt=\frac{2\pi}{T}dt\longrightarrow dt=d\theta\frac{T}{2\pi}. \tag{4.47}$$

Parameters ω and T are given for the fundamental harmonic of the current that is 50Hz, but the index "1" as a subscript is intentionally omitted. According to this, the ac current ripple NMS can be calculated as:

$$NMS_{I,ac}^{n}(\theta)=\frac{1}{12}\frac{1}{2\pi}\int_{0}^{2\pi}(m\sin(\theta)-i)^{2}\left((i+1)-m\sin(\theta)\right)^{2}d\theta, \qquad (4.48)$$
$$i=0,\ 1,\ 2,...,\ (n-3)/2,\ i\le m\le i+1.$$

The previous integral form considers the whole fundamental period. Figure 4.13. shows a quarter-wave symmetry of the current ripple. The control technique together with the instantaneous current with its fundamental component and instantaneous ac current ripple are presented for the case of three-cascaded H-bridges with single dc bus voltages V_{dc}=200V, switching frequency f_s=3kHz, fundamental frequency f_f=50Hz and load parameters R=64.6Ω and L=36.2mH. Modulation index is set to m=2.5.

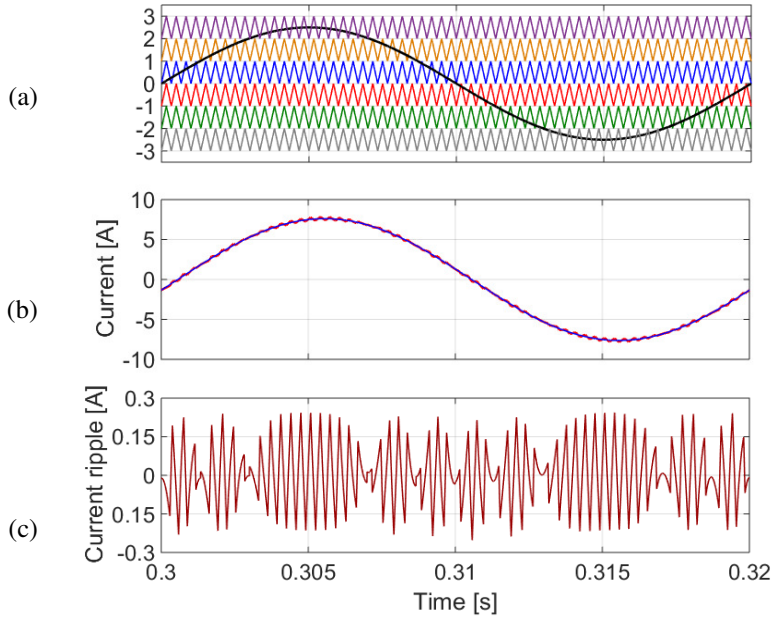


Figure 4.19. (**a**) PWM control technique , (**b**) instantaneous current (red) and its fundamental component (blue), (**c**) and instantaneous current ripple (maroon) over one fundamental period (T=20ms) of a single-phase seven-level inverter with V_{dc}=200V, load parameters R=64.6Ω and L=36.2mH, f_f=50Hz, f_s=3kHz and m=2.5.

Taking into account this symmetry, the ac current ripple NMS can be written as:

$$NMS_{I,ac}^{n}(\theta)=\frac{1}{12}\frac{2}{\pi}\int_{0}^{\pi/2}(m\sin(\theta)-i)^{2}\left((i+1)-m\sin(\theta)\right)^{2}\ d\theta, \qquad (4.49)$$
$$i=0,\ 1,\ 2,...,\ (n-3)/2,\ i\le m\le i+1.$$

As it was done for the ac voltage NMS the same generic property of one function $y(x)$ can be defined, which says that the function has a specific value if some of its parameters are within defined limits, otherwise it has a zero value:

$$y(x)=\left\{\begin{array}{l}(x-x_1)(x_2-x),\ x\in[x_1,x_2]\\ 0,\ x\notin[x_1,x_2]\end{array}\right\},\qquad (4.50)$$
$$x_1=0,\ 1,\ 2,\ldots,\ (n-3)/2\ ,\ x_2=1,\ 2,\ldots,\ (n-1)/2\ .$$

Limits x_1 and x_2 are given on the basis of the studied single-phase n-level inverter.

After defining this function, the expression for calculating $NMS_{I,ac}$ can be divided into two main parts. One part represents the case when the modulation index m takes part between two adjacent (voltage) levels defined by the parameters x_1 and x_2, and none of them presents the maximum possible level considering all N cascaded H-bridges. Another part represents the case when m is between the maximum possible (voltage) level and the penultimate one. This means that for every two adjacent levels the integral form (4.49) is calculated separately and at the end all in-between-level contributions are summed to get the final value of the ac current ripple NMS value. Each sub-integral form must have its limits that can be easily defined as it was done in case of the voltage evaluation. The same approach will be repeated here for a single-phase seven level inverter, according to Figure 4.20.

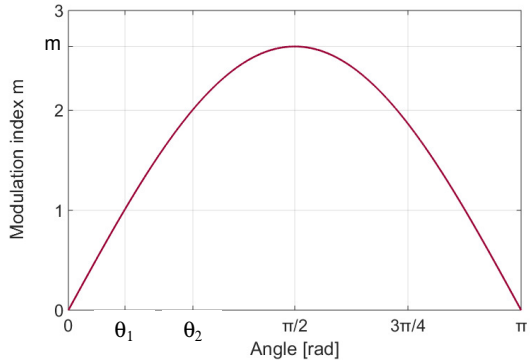


Figure 4.20. Half-fundamental period of the modulating signal (50Hz) defining the limits between adjacent (voltage) levels for a single-phase seven-level inverter and modulation index m.

It can be seen that there are two angles θ_1 and θ_2 which define the proper limits. There sub-integral forms must be calculated get the final ac voltage NMS value. The first one between angles 0 and θ_1, the second one between angles θ_1 and θ_2, and the third one between angles θ_2 and $\pi/2$. The first two can be joined into one form introducing a proper variable, while the third one must be calculated for itself. The

modulation index m is arbitrarily selected between values 2 and 3 in order to explain the suggested algorithm.

According to Figure 4.14. and considering the previous explanation for the voltage ripple NMS, the corresponding angle limits can be written as:

$$m\sin(\theta_1)=1\rightarrow\theta_1=\arcsin\left(\frac{1}{m}\right),\ m\sin(\theta_2)=2\rightarrow\theta_1=\arcsin\left(\frac{2}{m}\right). \tag{4.51}$$

For the general case of a single-phase n-level inverter, the equation (4.51) becomes:

$$m\sin(\theta_i)=i\rightarrow\theta_i=\arcsin\left(\frac{i}{m}\right),\ m\sin(\theta_{i+1})=i+1\rightarrow\theta_{i+1}=\arcsin\left(\frac{i+1}{m}\right), \tag{4.52}$$
$$i=0,\ 1,\ 2,...,(n-5)/2.$$

Equation (4.52) does not include the case for n=3 because there is only one region where m takes place. In order to calculate the ac current ripple NMS between two adjacent levels according to the previously defined angle limits, the integral form labelled as $a_I^n(m)$ becomes:

$$a_I^n(m)=NMS_{I,ac}^n(\theta_i\le\theta\le\theta_{i+1})=\frac{1}{12}\frac{2}{\pi}\int_{\theta_i=\arcsin\left(\frac{i}{m}\right)}^{\theta_{i+1}=\arcsin\left(\frac{i+1}{m}\right)}(m\sin(\theta)-i)^2\left((i+1)-m\sin(\theta)\right)^2\,d\theta, \tag{4.53}$$

$i=0,\ 1,\ 2,...,(n-5)/2$, $i\le m\le i+1$.

All steps related to the calculation of this integral are given in Appendix 5. The final result of (4.53) is:

$$a_I^n(m)==\frac{1}{12}\left(\begin{array}{l}\frac{1}{12\pi}\sqrt{m^2-(i+1)^2}\left(2(i+1)\left(25i^2+6i-1\right)+(23+55i)m^2\right)+\\-\frac{1}{12\pi}\sqrt{m^2-i^2}\left(2i\left(25i^2+44i+18\right)+(32+55i)m^2\right)+\\+\frac{1}{\pi}\left(2i^2(i+1)^2+\left(6i^2+6i+1\right)m^2+\frac{3}{4}m^4\right)\left(\arcsin\left(\frac{i+1}{m}\right)-\arcsin\left(\frac{i}{m}\right)\right)\end{array}\right) \tag{4.54}$$

$i=0,\ 1,\ 2,...,(n-5)/2$, $i\le m\le i+1$.

When the contribution of the ac current ripple NMS comes from the last voltage level, the integral form labelled as $b_I^n(m)$ is given by (4.55).

$$b_I^n(m)=NMS_{I,ac}^n\left(\theta_k\le\theta\le\frac{\pi}{2}\right)=\frac{1}{12}\frac{2}{\pi}\int_{\theta_k=\arcsin\left(\frac{k}{m}\right)}^{\frac{\pi}{2}}(m\sin(\theta)-k)^2\left((k+1)-m\sin(\theta)\right)^2\,d\theta, \tag{4.55}$$

$k=(n-3)/2$, $k\le m\le k+1$.

Solving (4.55) results in:

$$b_I^n(m)=\frac{1}{12}\left(\begin{array}{l}\arcsin\left(\frac{k}{m}\right)\left(-\frac{1}{\pi}\left(2k^2(1+k)^2+\left(6k^2+6k+1\right)m^2+\frac{3}{4}m^4\right)\right)+\\+\sqrt{m^2-k^2}\left(-\frac{1}{12\pi}\left(m^2(32+55k)+2k\left(25k^2+44k+18\right)\right)\right)+\\+\left[k^2(1+k)^2+\left(6k^2+6k+1\right)\frac{m^2}{2}+\frac{3}{8}m^4\right]\end{array}\right) \tag{4.56}$$

$k=(n-3)/2$, $k\le m\le k+1$.

Detailed solving steps of (4.55) are given in Appendix 5. It must be noted that the parameter k strictly depends on the level number n and has only one value because it refers to the last voltage level of one single-phase n-level H-bridge inverter. Apart from this, setting k=0, the ac current ripple NMS in case of n=3 can be obtained. In order to get the final value of the ac current ripple NMS, it is needed to sum (4.54) and (4.56) in a proper way. The proper sum of both equations is:

$$NMS_{I,ac}^n(m)=\sum_{i=0}^{(n-5)/2}a_I^n(m)+b_I^n(m)=\sum_{i=0}^{k-1}a_I^n(m)+b_I^n(m),\ k=(n-3)/2. \tag{4.57}$$

Introducing (4.54) and (4.56) into (4.57) results in:

$$NMS_{I,ac}^n(m)=\frac{1}{12}\left(\begin{array}{l}\left(\begin{array}{l}\sum_{i=0}^{k-1}\left(\begin{array}{l}\frac{1}{12\pi}\sqrt{m^2-(i+1)^2}\left(\begin{array}{l}2(i+1)\left(25i^2+6i-1\right)+\\+(23+55i)m^2\end{array}\right)+\\-\frac{1}{12\pi}\sqrt{m^2-i^2}\left(\begin{array}{l}2i\left(25i^2+44i+18\right)+\\+(32+55i)m^2\end{array}\right)+\\+\frac{1}{\pi}\left(2i^2(i+1)^2+\left(6i^2+6i+1\right)m^2+\frac{3}{4}m^4\right)\cdot\\\cdot\left(\arcsin\left(\frac{i+1}{m}\right)-\arcsin\left(\frac{i}{m}\right)\right)\end{array}\right)\end{array}\right)+\\+\arcsin\left(\frac{k}{m}\right)\left[-\frac{1}{\pi}\left(\begin{array}{l}2k^2(1+k)^2+\\+\left(6k^2+6k+1\right)m^2+\frac{3}{4}m^4\end{array}\right)\right]+\\+\sqrt{m^2-k^2}\left[-\frac{1}{12\pi}\left(m^2(32+55k)+2k\left(25k^2+44k+18\right)\right)\right]+\\+\left(k^2(1+k)^2+\frac{3}{8}m^4+\frac{\left(6k^2+6k+1\right)}{2}m^2\right)\end{array}\right). \tag{4.58}$$

Detailed solving and grouping steps of (4.58) are given in Appendix 5. The final result of the ac current ripple NMS for a single-phase n-level inverter considering all possible voltage levels is given by (4.59).

$$NMS_{I,ac}^{n}(m)=\begin{cases}\dfrac{1}{32}m^4-\dfrac{2}{9\pi}m^3+\dfrac{1}{24}m^2\ ,\ 0\le m\le 1;\\ -\dfrac{1}{3\pi}\sum_{i=1}^{k}\left(i\left(2i^2+3m^2\right)\arcsin\left(\dfrac{i}{m}\right)\right)-\dfrac{1}{9\pi}\sum_{i=1}^{k}\left(\sqrt{m^2-i^2}\left(11i^2+4m^2\right)\right)\\ +\dfrac{k^2(k+1)^2}{12}+\dfrac{1}{32}m^4-\dfrac{2}{9\pi}m^3+\dfrac{\left(6k^2+6k+1\right)}{24}m^2\ ,\\ i=1,\,2,\ldots,(n-3)/2\ ,\ i\le m\le i+1\ ,\ k=(n-3)/2.\end{cases}\qquad(4.59)$$

Setting the parameter k=0 in (4.59), the ac current ripple NMS in case of a single-phase three-level inverter with $0\le m\le 1$ is easily obtained.

The ac normalized mean square current ripple, with respect to the equation (4.59), for the configuration up to five H-bridges presenting a possible single-phase eleven-level inverter is presented in Figure 4.21.

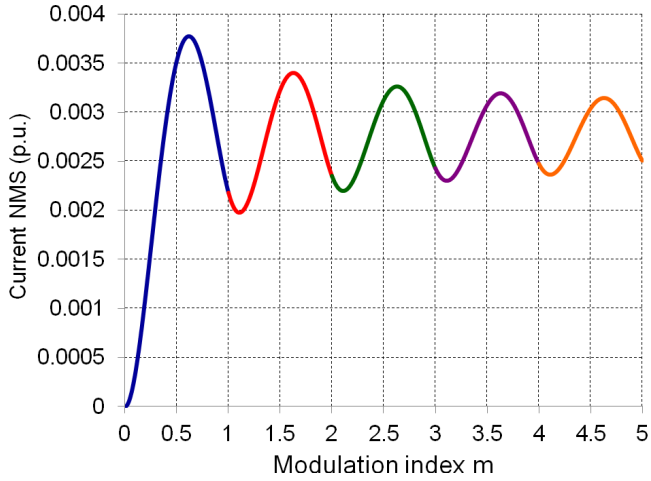


Figure 4.21. Ac current ripple normalized mean square for the configuration up to five H-bridges – eleven-level single-phase inverter (equation (4.59))

4.3.2.3 Current THD as a function of ac current ripple NMS criterion

In order to calculate the current THD using the current ripple NMS criterion, a simple mathematical calculation used for the voltage THD can be considered as well. In that case, the current THD form, using non-normalized parameters, is:

$$THD_I^n=\frac{I_{rms,dist}}{I_{1,rsm}}.\qquad(4.60)$$

The current ripple rms value $I_{rms,dist}$ can be written as a function of $NMS_{I,ac}^{n}(m)$ de-normalized with the proper coefficient evaluated in (4.40). Following this gives:

$$I_{rms,dist} = \sqrt{NMS_{I,ac}^{n}(m)\left(\frac{V_{dc}T_s}{L}\right)^2} = \sqrt{NMS_{I,ac}^{n}(m)}\frac{V_{dc}}{f_s L}. \tag{4.61}$$

The fundamental current component is:

$$I_{1,rsm} = \frac{mV_{dc}}{\sqrt{2}\sqrt{R^2 + (2\pi f_f L)^2}} = \frac{mV_{dc}}{2\sqrt{2}\pi f_f L\sqrt{1+\left(\frac{R}{2\pi f_f L}\right)^2}}. \tag{4.62}$$

By substituting (4.61) and (4.62) into (4.60), the current THD form becomes:

$$THD_I^n(\%) = \frac{2\pi\sqrt{2NMS_{I,ac}^{n}(m)}}{m}\frac{f_f}{f_s}\sqrt{1+\left(\frac{R}{2\pi f_f L}\right)^2}\cdot 100\%. \tag{4.63}$$

In Figure 4.22, the current THD as a function of the modulation index m is presented, considering the configuration up to five cascaded H-bridges, single-phase eleven-level inverter. Parameters used for the current THD are: f_f =50Hz, f_s=3kHz, R=64.6Ω and L=36mH.

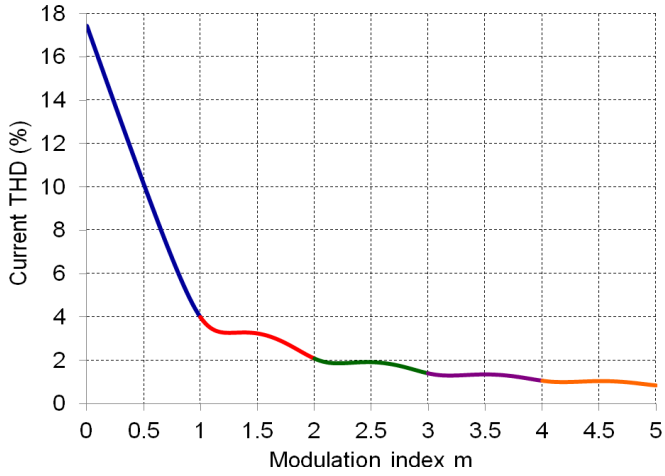


Figure 4.22. Current THD(%) as a function of the modulation index m (equation (4.63)) for the configuration up to five cascaded H-bridges – single-phase eleven-level inverter with R=64.6Ω, L=36.2mH, f_f=50Hz and f_s=3kHz.

4.4 Simulation

In order to estimate the correctness of the analytical approach while calculating the output power quality of a single-phase multilevel inverter controlled by PWM technique, Matlab/Simulink simulations were carried out. Three different configurations are analysed: one H-bridge, and two and three cascaded H–bridges. It must be noted that these configurations are intentionally selected because the same configurations will be experimentally used. The Simulink scheme with three cascaded H-bridges (seven-level single-phase inverter) is presented in Figure 4.23.

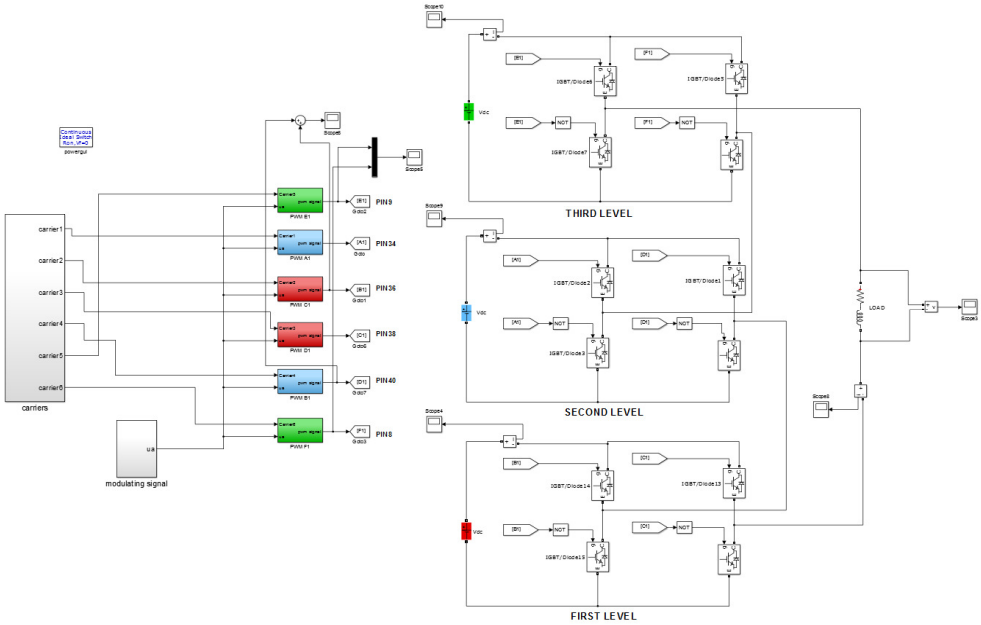


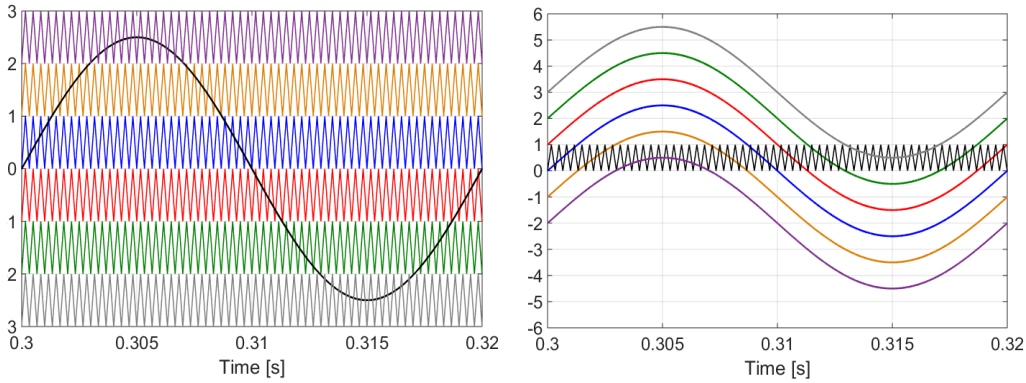
Figure 4.23. Matlab/Simulink model of a single-phase seven-level inverter with three cascaded H-bridges.

Generally, six carriers and one modulating signal are needed to control three cascaded H-bridges. Considering an *n*-level inverter *n*-1 carriers and one modulating signal are needed in order to properly control the whole configuration. On the other hand, the control strategy of a single-phase *n*-level inverter can be performed using only one carrier and *n*-1 modulating signals, as a completely equivalent solution. In this case every modulating signal has a shift of +/−1 with respect to the value of the modulation index *m*.

The second kind of the PWM technique is introduced because the microcontroller used in all experiments is capable of providing only one carrier and multiple modulating signals. This feature of the microcontroller will be explained in the experimental part of this chapter.

The important fact is that both ways of implementing the PWM technique work exactly in the same way and give identical results.

For three cascaded H-bridges the standard unipolar PWM technique with six carriers and one modulating signal, and the equivalent one with one carrier and six modulating signals are presented in Figure 4.24.(a) and (b), respectively. The frequency of all carriers is 3 kHz and the frequency of all modulating signals is 50 Hz. It must be noted that the colours of all carriers in Figure 4.24.(a) intentionally correspond to the colours of the modulating signals in Figure 4.24.(b), therefore each carrier has a connection with the corresponding modulating signal which provides exactly the same control signal. The chosen modulation index is m=2.5.



(a) (b)

Figure 4.24. Unipolar equivalent PWM techniques (**a**) with six carriers and one modulating signal and (**b**) with one carrier and six modulating signals for f_f=50Hz, f_s=3kHz and m=2.5.

In order to estimate the output power quality of the proposed single-phase configuration, it is important to define the passive load parameters R and L, since the current THD adheres to them. Those two parameters are based on a real custom-made air core inductance (measured with an RLC meter) and its values are R=64.6Ω and L=36.2mH. The same load parameters were used in the previous chapter and will be considered for the experimental work as well.

Scrutinizing the previously presented single-phase configuration, the modulation index range starts with 0 and ends with 3. This means that only one H-bridge works, if the inverter works with the modulation index which belongs to its first range i.e. from 0 to 1. If two H-bridges work it means that the modulation index takes place within the range 1-2. The same applies if three H-bridges contribute to the voltage and current, and m is between 2 and 3. According to this, nine different values of the modulation index m are chosen (three values for each of three different configurations) in order to attain the voltage and current THDs using the built-in Matlab function called ‘‘FFT analysis’’.

Apart from the THD value of one parameter this function gives its amplitude for the fundamental harmonic as well. The nine selected values of the modulation index *m* are: 0.3, 0.6, 0.9, 1.3, 1.6, 1.9, 2.3, 2.6, and 2.9.

In Figure 4.25. the voltage (blue) and current (red, scaled 50 times) are presented over three fundamental periods (3T=60ms) for the modulation index *m*=2.5 (intentionally deferent modulation index compared with the nine selected ones) as one representation of the analysed configuration.

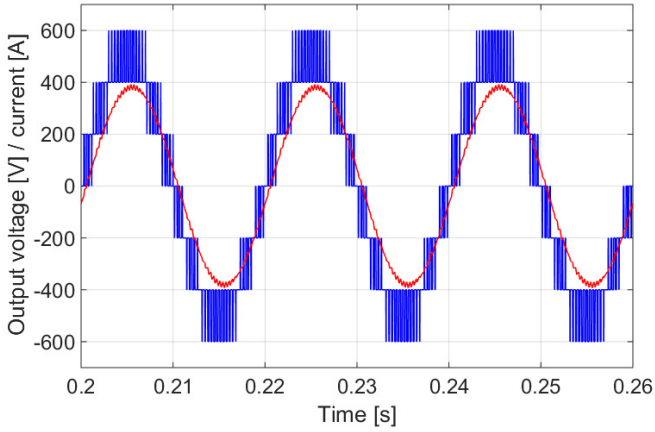


Figure 4.25. Voltage and current (50x) obtained by Matlab simulation for a single-phase seven-level inverter (three cascaded H-bridges):
V_{dc}=200V, R=64.6Ω, L=36.2mH, f_f =50Hz, f_s=3kHz and *m*=2.5.

In Figures 4.26., 4.27. and 4.28. all nine selected cases for the voltage and current THD estimations as results of the FFT analysis are presented. Each figure presents a screenshot of the Matlab/Simulink simulation, where the voltage and current THDs are displayed together with their fundamental amplitudes (emphasised with the red rectangle). Calculating the voltage and current THDs for each value of the modulation index *m* considers ten fundamental periods of 20ms and starts at the time scale 20ms in order to steer clear of a possibly short transient period at the beginning of the simulation and to get the desired values as precise as possible. The switching frequency is set to 3kHz, thereby harmonics appear around it and its multiples 6kHz and 9kHz. The frequency scale ends at 10kHz in order to make the dominating harmonics visible. All harmonics after the frequency 10kHz have lower amplitudes.

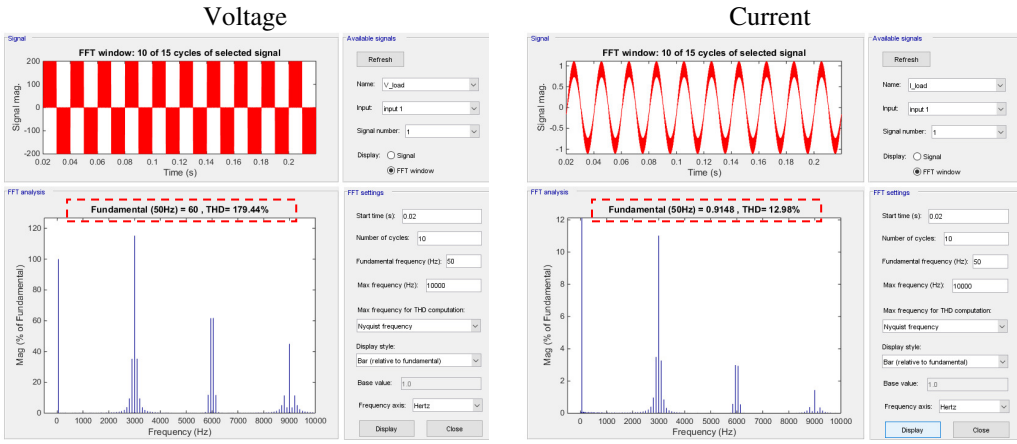


Figure 4.26. Voltage (left) and current (right) FFT analyses for a single-phase three-level inverter: (**a**) m=0.3, (**b**) m=0.6, (**c**) m=0.9, for V_{dc}=200V, R=64.6Ω, L=36.2mH, f_f=50Hz and f_s=3kHz.

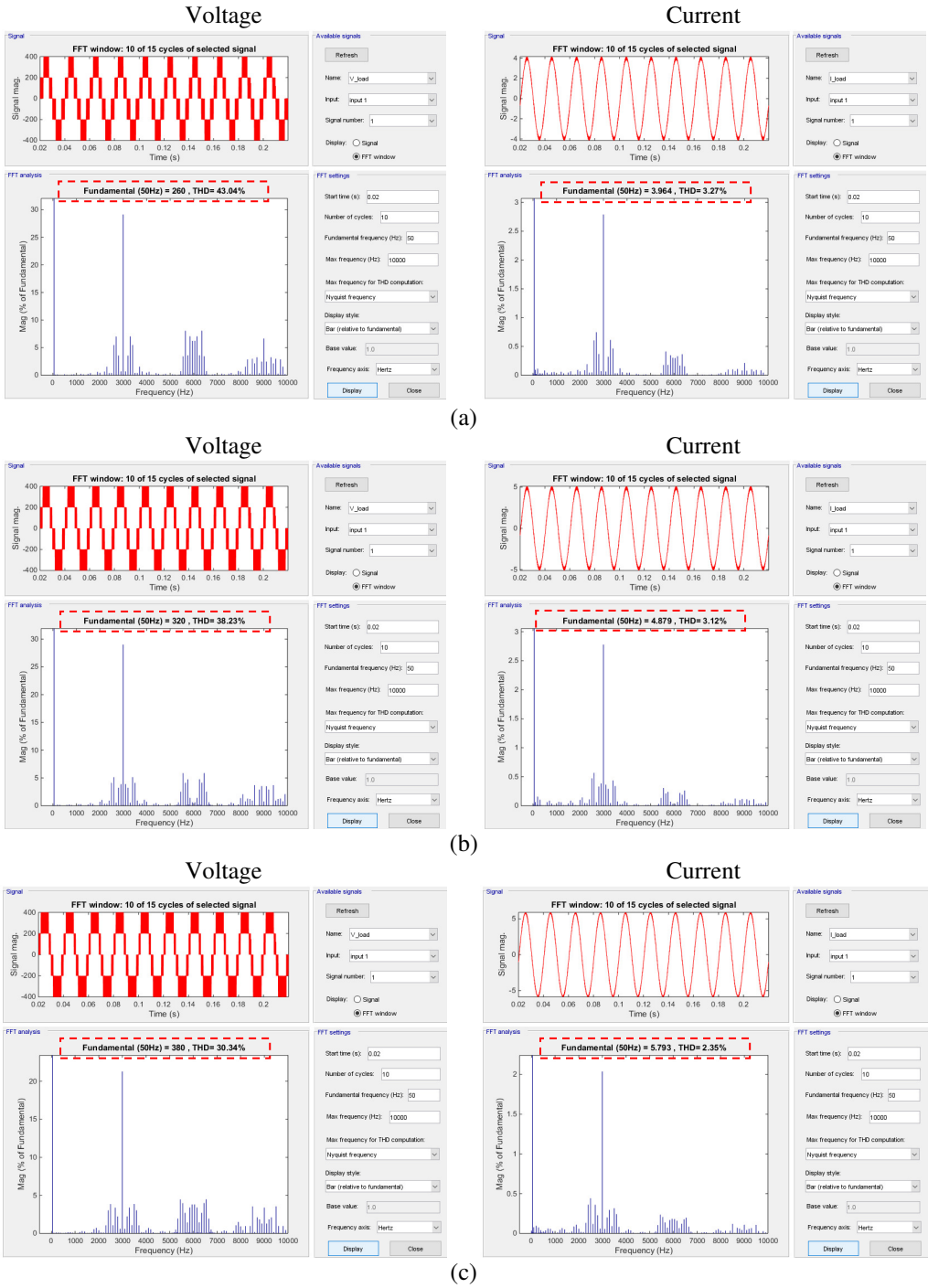
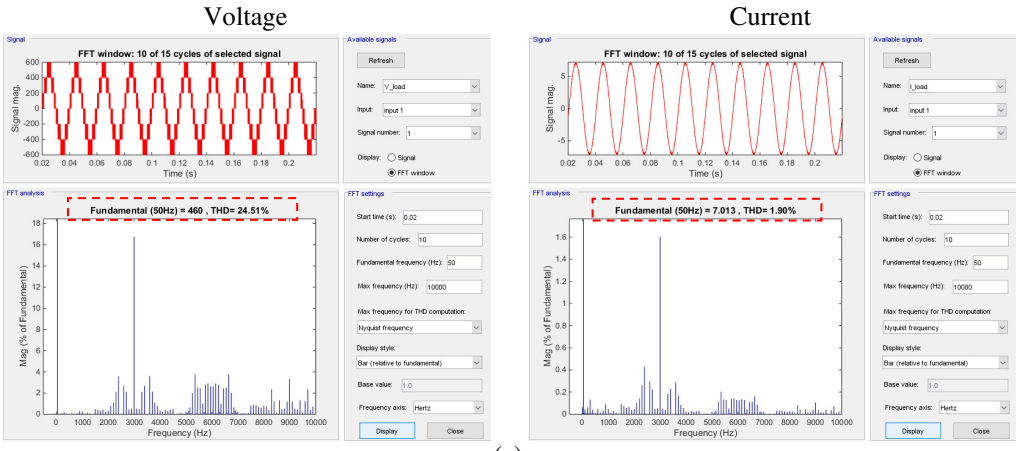
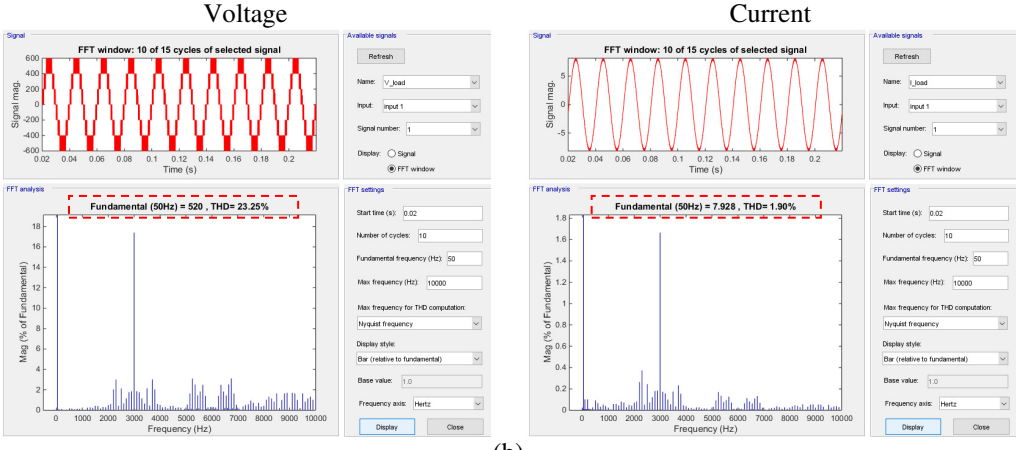


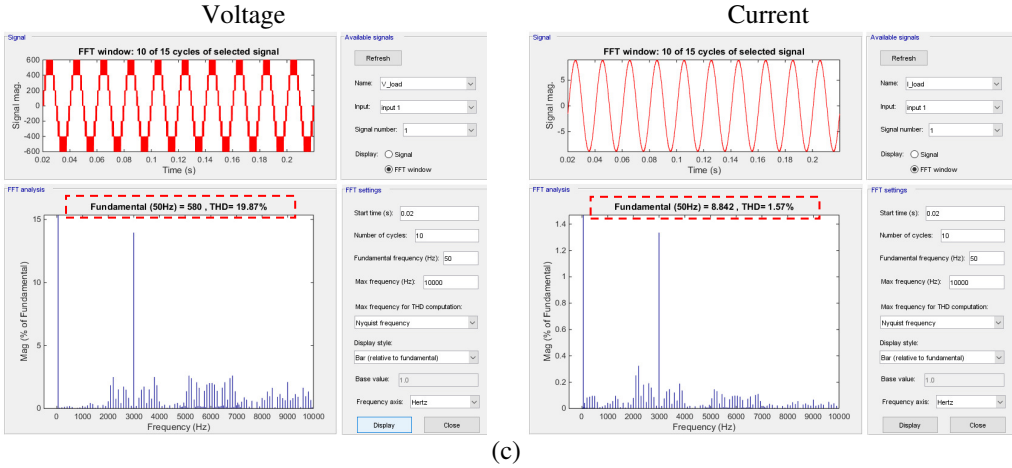
Figure 4.27. Voltage (left) and current (right) FFT analyses for a single-phase five-level inverter: (**a**) *m*=1.3, (**b**) *m*=1.6, (**c**) *m*=1.9, for V_{dc}=200V, R=64.6Ω, L=36.2mH, f_f=50Hz and f_s=3kHz.



(a)



(b)



(c)

Figure 4.28. Voltage (left) and current (right) FFT analyses for a single-phase seven-level inverter: (**a**) m=2.3, (**b**) m=2.6, (**c**) m=2.9, for V_{dc}=200V, R=64.6Ω, L=36.2mH, f_f=50Hz and f_s=3kHz.

The results obtained by using the simulations are summarized in Table 4.1. for a better overview.

Table 4.1. Voltage and current THDs for nine selected cases obtained by simulations

Configuration	Modulation index *m*	THD_V (%)	THD_I (%)
One H-bridge three-level inverter	0.3	179.44	12.98
	0.6	105.64	8.71
	0.9	64.18	4.91
Two cascaded H-bridges five-level inverter	1.3	43.04	3.27
	1.6	38.23	3.12
	1.9	30.34	2.35
Three cascaded H-bridges seven-level inverter	2.3	24.51	1.90
	2.6	23.25	1.90
	2.9	19.87	1.57

It can be noticed that by increasing the modulation index *m*, which also means involving more H-bridges in the configuration, the output power quality improves. After presenting the experimental results, the full comparison between analytically calculated, simulation and experimental results will be tabulated and graphically presented.

4.5 Laboratory experiments

Experimental verifications were performed for a single-phase inverter with one H-bridge, and two and three H-bridges, maximum seven voltage levels. The dc bus voltage of each H-bridge is V_{dc}=200V. Note that the detailed explanation of the experimental realization of the mentioned inverer is given in chapter 2.3. A simple circuit scheme of the experimental setup is presented in Figure 4.29.

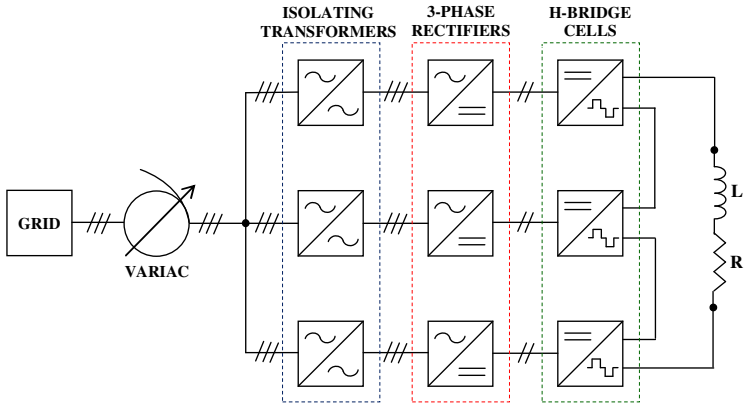
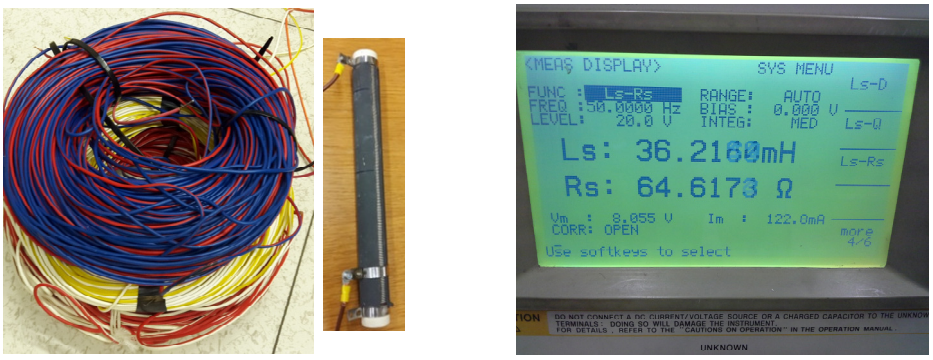


Figure 4.29. Circuit scheme of the experimental setup.

As it was considered in the previous analyses in this chapter, an air-core inductor with its resistive and inductive parts R=64.6Ω and L=36.2mH is used for the experimental tests. Figure 4.27. shows the inductor together with the display of the RLC meter measuring its parameters.



(a) (b)

Figure 4.30. (**a**) Air-core inductor used as a load and (**b**) measuring its parameters *R* and *L* with the RLC meter

The control signals for all three H-bridges are provided by the Arduino DUE microcontroller. The modulating principle is similar to that one explained in the chapter 3.6, therefore in Appendix 6 the program code is given with a short explanation. This kind of microcontroller has only one carrier consisting of clock counts starting at zero and finishing at an exact value which defines the switching frequency. The type of the carrier used in the program code is the so-called canter-aligned carrier. The same carrier was used in the simulation part. Generating proper sinusoidal modulation signals and comparing them with the carrier give control gate signals for the proposed configuration. It can be noted that for three cascaded H-bridges six modulating signals are generated by the microcontroller.

For the experimental verifications nine different values of the modulation index *m* are selected according to the correspondence with the simulation. Those values are 0.3, 0.6, 0.9, 1.3, 1.6, 1.9, 2.3, 2.6, and 2.9. In case of using only one H-bridge, two modulating signals are used, therefore the amplitudes of the other four modulating signals are set to 0. The same applies for two H-bridges where two modulating signals have the modulation index 0.

Doing so, a full comparison between analytical, simulation and experimental results can be made. Thanks to the oscilloscope advanced functions, each experimental case is presented with a screenshot of the signals together with their real time calculations. The experimental results are presented in Figures 4.31., 4.32., and 4.33.

(a)

(b)

(c)

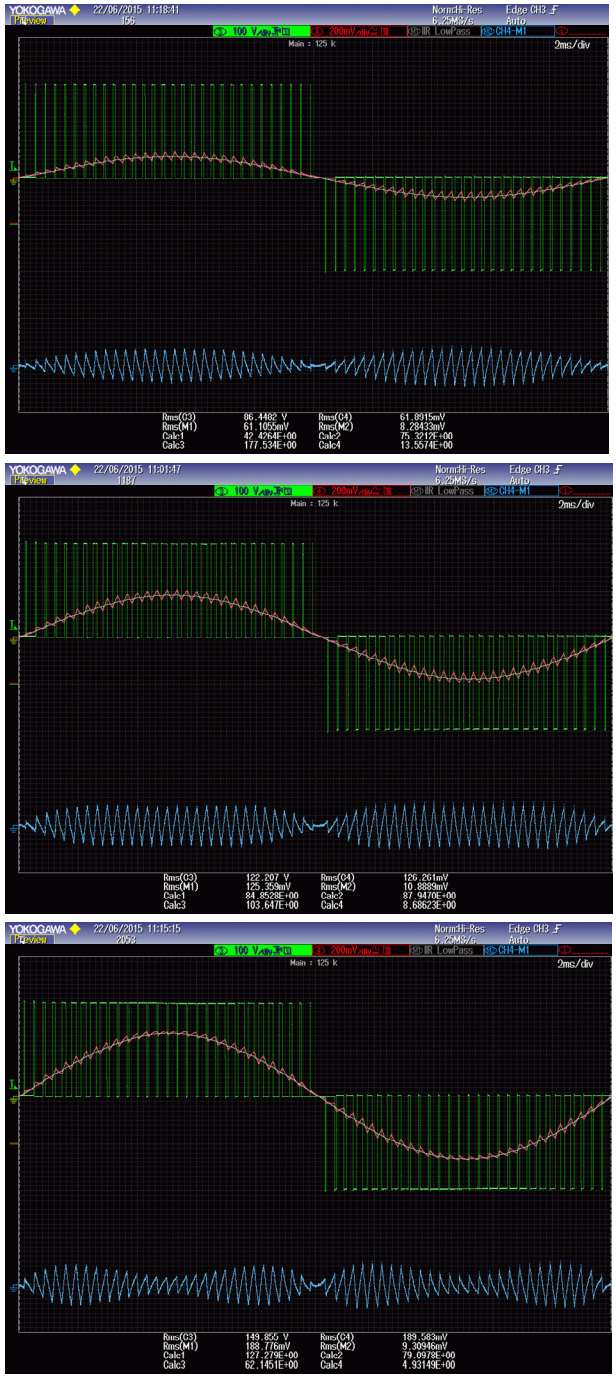


Figure 4.31. Measured voltage (green trace), current (red trace), fundamental current (grey trace) and current ripple (5x, blue trace) for (**a**) m =0.3; (**b**) m =0.6; (**c**) m =0.9, for V_{dc}=200V, R=64.6Ω, L=36.2mH, f_f =50Hz and f_s=3kHz.

(a)

(b)

(c)

Figure 4.32. Measured voltage (green trace), current (red trace), fundamental current (grey trace) and current ripple (5x, blue trace) for (**a**) m =1.3; (**b**) m =1.6; (**c**) m =1.9, for V_{dc}=200V, R=64.6Ω, L=36.2mH, f_f =50Hz and f_s=3kHz.

(a)

(b)

(c)

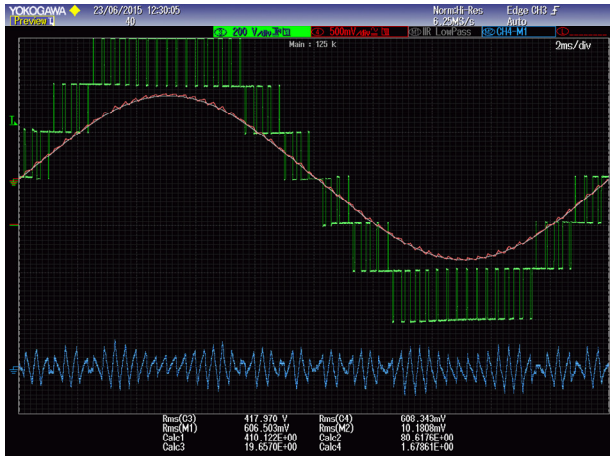


Figure 4.33. Measured voltage (green trace), current (red trace), fundamental current (grey trace) and current ripple (5x, blue trace) for (**a**) m =2.3; (**b**) m =2.6; (**c**) m =2.9, for V_{dc}=200V, R=64.6Ω, L=36.2mH, f_f =50Hz and f_s=3kHz.

Each screenshot shows four different waveforms, displayed over one fundamental period 20ms, presented in the first half of Table 4.2.: output (load) voltage (green trace) – oscilloscope channel 3, labelled C3; output (load) current (red trace) – oscilloscope channel 4, labelled C4; fundamental component of the current obtained by using the IIR low pass filter (grey trace) – labelled M1 and the current ripple obtained as a difference between the current and its fundamental component (blue trace, scaled 5 times) – labelled M2:C4-M1. It must be noted that on the top of each screenshot the scales of waveforms are displayed with the colours which correspond to the waveform colours. Due to the real size of the current ripple, it must be scaled by five in order to make it visible. The scaling factor does not affect any calculation.

Calculations used for estimating the output power quality under the specific working conditions are carried out by using the infinite impulse infrared (IIR) filter and built-in advanced mathematical functions of the oscilloscope working in real time. This is an important feature of the oscilloscope, considering that real time calculations take into account all characteristics of signals without some mid-steps such as downloading signals with a proper sample resolution and handling them with software. In this case possible conversion errors are avoided, all steps are less complex and experimental results are well and precisely presented. Eight different calculations, which are presented in the second half of Table 4.2., are shown at the bottom of each screenshot (Figures 4.31., 4.32. and 4.33.).

Table 4.2. Waveforms and their parameters calculated by the scope built-in advanced mathematical functions. RMS: root mean square.

Label	Description	Signal waveforms and calculated parameters
C3	Scope channel 3, CH3	Load voltage
C4	Scope channel 4, CH4	Load current
M1	Math function 1: IIR low pass filter	Fundamental current
M2	Math function 2: CH4−M1	Ripple current
Rms(C3)	Math function RMS on CH3	Total voltage rms V_{rms}
Rms(C4)	Math function RMS on CH4	Total current rms I_{rms}
Rms(M1)	Math function RMS on M1	Total fundamental current rms $I_{rms,fund}$
Rms(M2)	Math function RMS on M2=CH4−M1	Total current ripple rms $I_{rms,ripple}$
Calc1	Built-in math calculation 1	Fundamental voltage rms $V_{rms,fund}=\frac{m\,V_{dc}}{\sqrt{2}}$
Calc2	Built-in math calculation 2	Voltage ripple rms $V_{rms,ripple}=\sqrt{(V_{rms})^2-\left(m\,V_{dc}/\sqrt{2}\right)^2}=\sqrt{(Rms(C3))^2-(Calc1)^2}$
Calc3	Built-in math calculation 3	Voltage THD(%) $THD_I(\%)=\frac{V_{rms,ripple}}{V_{rms,fund}}\cdot 100=\frac{Calc2}{Calc1}\cdot 100$
Calc4	Built-in math calculation 4	Current THD(%) $THD_I(\%)=\frac{I_{rms,ripple}}{I_{rms,fund}}\cdot 100=\frac{Rms(M2)}{Rms(M1)}\cdot 100$

According to the previous calculations, the voltage and current THDs experimentally obtained can be easily tabulated in Table 4.3.

Table 4.3. Experimentally obtained voltage and current THDs

Configuration	Modulation index *m*	THD_V (%)	THD_I (%)
One H-bridge three-level inverter	0.3	177.53	13.56
	0.6	103.65	8.69
	0.9	62.14	4.93
Two cascaded H-bridges five-level inverter	1.3	42.61	3.48
	1.6	38.46	3.25
	1.9	29.20	2.45
Three cascaded H-bridges seven-level inverter	2.3	22.49	1.98
	2.6	23.58	2.01
	2.9	19.66	1.68

4.6 Comparison of analytical, simulation and experimental results

Experimentally obtained results (*Exp.*) which define the output power quality of single-phase three-, five- and seven-level inverters have to be compared with the analytical (*Calc.*) and simulation (*Sim.*) ones in order to verify the matching between different approaches and to prove the correctness of the mathematical developments. For selected modulation indexes three different sets of results for voltage and current THDs are compared in Table 4.4.

Table 4.4. Analytically calculated, simulation and experimental voltage and current THDs

	THD_V (%)			THD_I (%)		
Modulation index *m*	***Calc.***	***Sim.***	***Exp.***	***Calc.***	***Sim.***	***Exp.***
0.3	180.11	179.44	177.53	13.03	12.98	13.56
0.6	105.93	105.64	103.65	8.74	8.71	8.69
0.9	64.4	64.18	62.14	4.92	4.91	4.93
1.3	43.2	43.04	42.61	3.27	3.27	3.48
1.6	38.37	38.23	38.46	3.11	3.12	3.25
1.9	30.44	30.34	29.20	2.34	2.35	2.45
2.3	24.60	24.51	22.49	1.86	1.90	1.98
2.6	23.32	23.25	23.58	1.87	1.90	2.01
2.9	19.93	19.87	19.66	1.54	1.57	1.68

It can be noticed that all three different approaches lead to almost the same results with an acceptably small error. In case of higher values of the modulation index *m*, the current THD error becomes noticeable due to really small THD values and due to the sensitivity of the current probe. The comparison between those results for the voltage and current THDs are graphically presented in Figures 4.34. and 4.35.

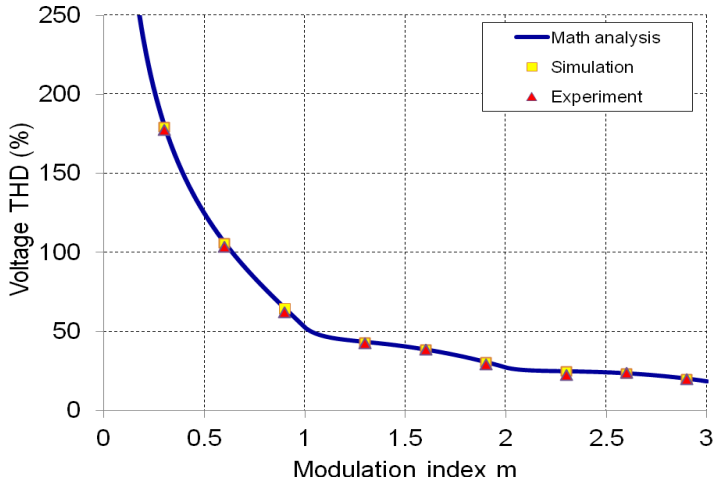


Figure 4.34. Comparison between analytically calculated, simulation and experimental values of the voltage THD considering nine different values of the modulation index *m*.

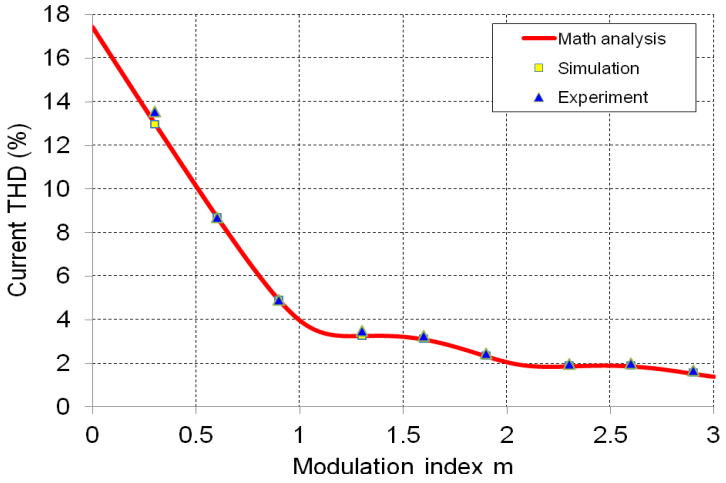


Figure 4.35. Comparison between analytically calculated, simulation and experimental values of the current THD considering nine different values of the modulation index *m*.

4.7 Grid-connected single-phase multilevel inverter

4.7.1 Grid current THD evaluation

A single-phase multilevel inverter connected to the electrical grid via coupling inductor is shown in Figure 4.36. For the maximum power transferred to the grid considering the given grid current amplitude, the current must be in phase with the corresponding grid voltage, as it is depicted by the phasor diagram in Figure 4.19.

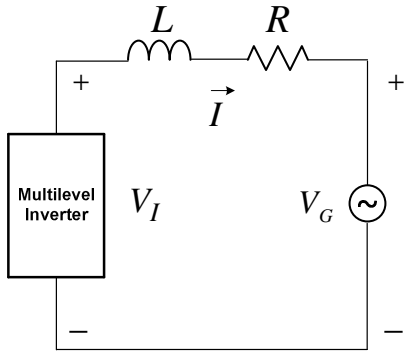


Figure 4.36. Single-phase multilevel inverter connected to the single-phase grid by a link inductor.

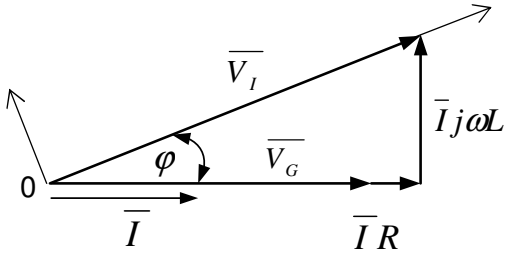


Figure 4.37. Phasor diagram for maximum transferred power.

Using an elementary geometry, according to Figure 4.37., inverter voltage parameters become:

$$V_I = \sqrt{(V_G + RI)^2 + (\omega LI)^2} \,. \tag{4.64}$$

$$\varphi = -\arctan\left(\frac{\omega LI}{V_G + RI}\right). \tag{4.65}$$

For the link inductor, the resistive part in equations (4.64) and (4.65) can be neglected (i.e. $\omega L >> R$), leading to:

$$V_I = \sqrt{V_G{}^2 + (\omega LI)^2} \,. \tag{4.66}$$

$$\varphi = -\arctan\left(\frac{\omega LI}{V_G}\right). \tag{4.67}$$

For grid-connected applications, the voltage modulation index for zero current can be defined as:

$$m_G = \frac{V_G}{V_{dc}}, \tag{4.68}$$

with V_{dc} as the converter dc bus voltage of each H-bridge and V_G the grid voltage.

According to (4.66) and (4.68), the modulation index m is:

$$m = \sqrt{m_G^2 + \left(\frac{\omega L I}{V_{dc}}\right)^2} \approx m_G \,, \tag{4.69}$$

where I is the grid current magnitude.
Taking into account (4.61), the normalized current ripple rms is:

$$I_{rms,dist} = \sqrt{NMS^{\,n}_{I,ac}(m)}\,\frac{V_{dc}}{f_s L}\,. \tag{4.70}$$

Introducing the grid current, the current THD becomes:

$$THD^{\,n}_{I,grid} = \frac{I_{rms,dist}}{I_{grid}} = \sqrt{2NMS^{\,n}_{I,ac}(m)}\,\frac{V_{dc}}{f_s L\, I_{grid}}\,. \tag{4.71}$$

Fundamental inverter voltage due to the voltage modulation index (4.68) will just compensate for the grid voltage, so that the fundamental grid current will be zero. For a unity power factor operation (Figure 4.37.), the required modulation index will be slightly larger but it can be considered the same as suggested by (4.69). This is because the coupling inductor voltage drop is practically of the order of 0.05–0.10 p.u. or less.

In order to graphically present the grid voltage THD given by (4.71), proper parameters have to be defined: dc bus voltage 200V, fundamental amplitude current 5A with the fundamental frequency 50 Hz, switching frequency 3 kHz, and linking inductance 43.3mH with its inner resistance 0.5 Ω. Introducing all these parameters into (4.71) results in Figure 4.38., where the grid current THD is presented over the modulation index range which considers up to five cascaded H-bridges (n=11).

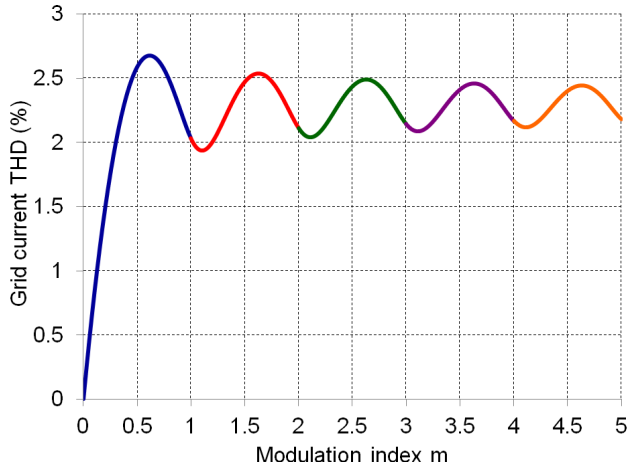


Figure 4.38. Grid current total harmonic distortion (THD) vs. modulation index m for n = 11 (up to five cascaded H-bridges).

Three values of the modulation index *m* can be chosen regarding three different configurations with one, two and three cascaded H-bridges in order to compare them with the simulation. For one H-bridge, the maximum value of the current THD can be selected what corresponds to the modulation index *m*=0.615 (Figure 4.38.). For two cascaded H-bridges the value of *m*, which belongs to the half grid current THD range, is one test point i.e. *m*=1.385, and for the third configuration one test point is *m*=2.11 corresponding to the minimum grid current THD. The selected test points are summarized in Table 4.5.

Table 4.5. Grid-connected single-phase inverter – selected test points

Case	*m*	$THD_{I,grid}(\%)$
I	0.615	2.68
II	1.385	2.32
II	2.110	2.04

4.7.2 Simulation of a grid-connected single-phase multilevel inverter

Verifying the analytical development of calculating the grid current THD by simulation, Matlab/Simulink is used. In the previous subchapter three test points were selected and based on them the grid parameters have to be calculated in order to have the grid voltage in phase with the grid current. Those grid parameters are the grid voltage amplitude V_G and its phase angle φ. The amplitude of the fundamental component of the inverter voltage is:

$$V_I = mV_{dc}. \tag{4.72}$$

The angle φ is calculated using a simple trigonometric relation leading to:

$$\varphi = -\arcsin\left(\frac{\omega LI}{mV_{dc}}\right). \tag{4.73}$$

Calculating φ, the required amplitude of the fundamental of the grid voltage which takes into account the voltage drop on the resistor *R* is:

$$V_G = mV_{dc}\cos(\varphi) - RI. \tag{4.74}$$

Using the parameters set previously, three selected cases for three different H-bridges configurations together with the proposed calculations are given in Table 4.6.

Table 4.6. Grid-connected single-phase inverter – selected cases for the simulation verification.

Case	*m*	$\mathbf{V_I}$ [V]	φ [rad]	$\mathbf{V_G}$ [V]
I	0.615	123	- 0.586	99.98
II	1.385	277	- 0.248	266.02
III	2.110	422	- 0.162	413.98

The implemented configuration with three cascaded H-bridges using Matlab/Simulink is presented in Figure 4.39.

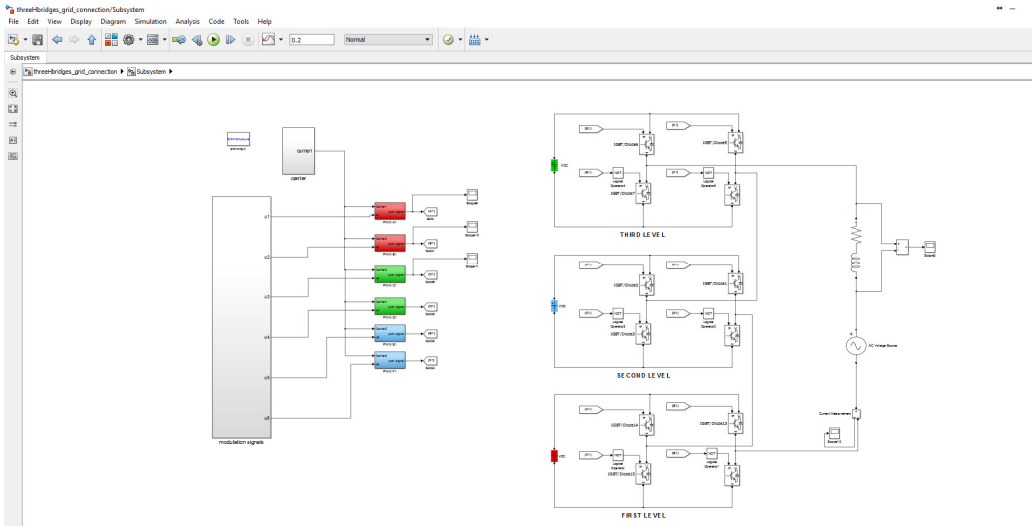


Figure 4.39. Matlab/Simulink model of a single-phase seven-level inverter with three cascaded H-bridges controlled by PWM technique and connected to the electrical grid.

One of three selected cases (case III) is presented in Figure 4.40. regarding the grid voltage and current, and it can be seen that they are in phase what confirms the analytical calculations presented in Table 4.6. For other cases voltage and current waveforms are similar, therefore they are not presented here.

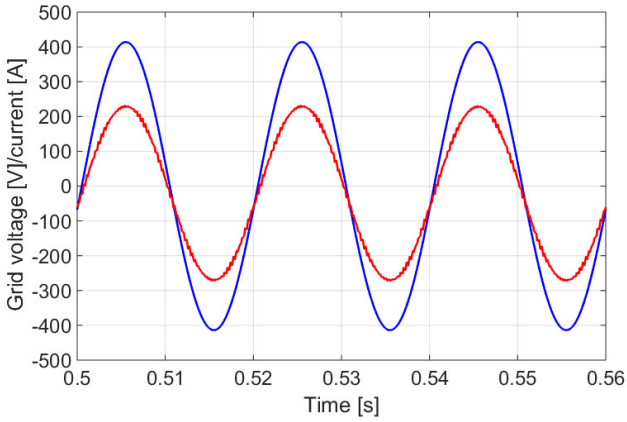


Figure 4.40. Grid voltage (blue) and current (50x, red) obtained by Matlab simulation for a single-phase seven-level inverter (three H-bridges) with respect to Figure 4.38.: V_{dc}=200V, R=0.5Ω, L=43.3mH, f_f=50Hz, f_s=3kHz, and m = 2.110.

Running the simulation and applying the FTT analysis for the grid current in all three proposed cases give the simulation evaluation of the grid current THDs. These results are presented in Figure 4.41.(a), (b) and (c) and emphasised with the red rectangle.

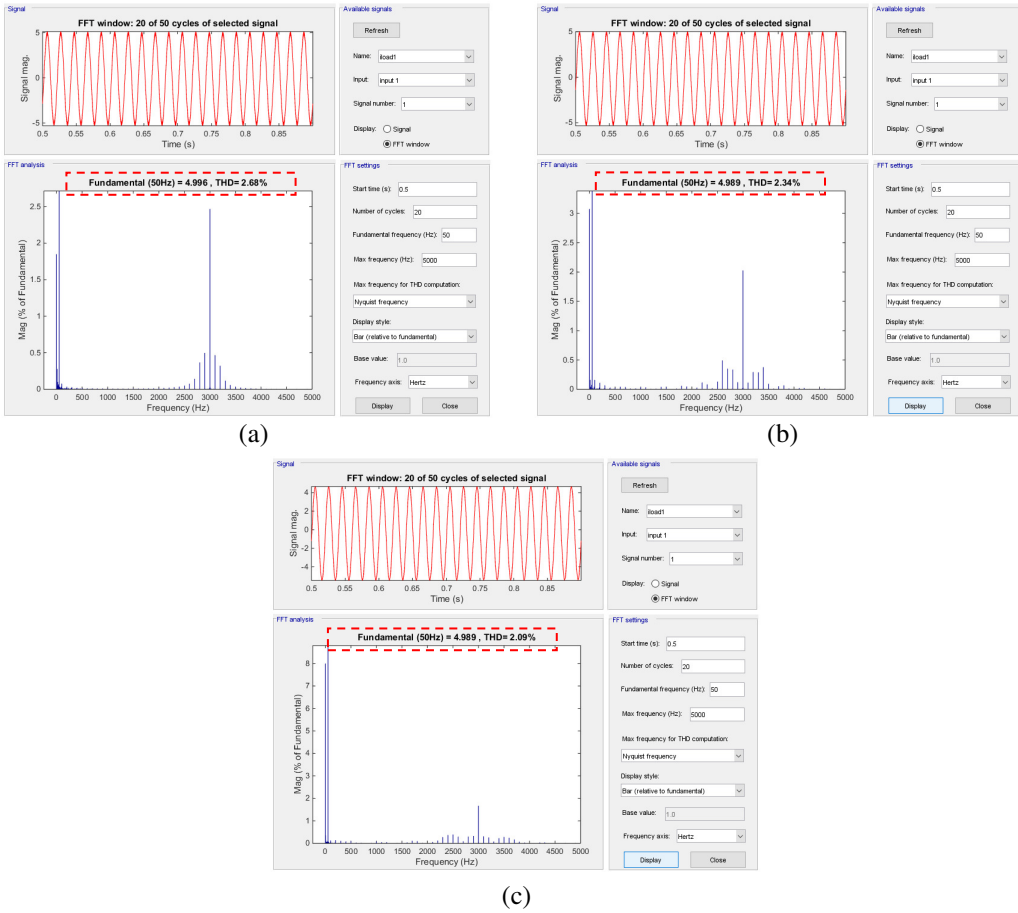


Figure 4.41. Grid current THD obtained by Matlab/Simulink simulation for single-phase three-, five- and seven-level inverters (up to three cascaded H-bridges) with respect to Figure 4.38.: (**a**) m = 0.615, (**b**) m = 1.385, (**c**) m = 2.110, for V_{dc}=200V, R=0.5Ω. L=43.3mH, f_f=50Hz and f_s=3kHz.

Every simulation comprises 50 fundamental periods and 20 of them are taken for the grid current THD evaluation starting after 25 periods in order to avoid the current transient at the beginning of the simulation process.

4.7.3 Comparison of analytical and simulation results for a grid-connected single-phase inverter

In order to prove the correctness of the analytical approach, the comparison between analytical (*Calc.*) and simulation (*Sim.*) results is presented in Table 4.7.

Table 4.7. Grid current THD – analytical and simulation results.

Case	*m*	$THD_{I,grid}$ (%)	
		Calc.	*Sim.*
I	0.615	2.68	2.68
II	1.385	2.32	2.34
III	2.110	2.04	2.09

Regarding this comparison, it can be said that simulation results match the analytical ones without any particular deviation which would introduce an error.

4.8 Discussion

The previously presented mathematical developments, using an asymptotic time-domain methodology for precisely evaluating the voltage and current THDs of single-phase multilevel inverters, delivers closed-form piecewise analytical solutions that consists of only elementary functions. On the contrary, the accepted frequency-domain approach for the same kind of analysis with relatively high switching frequency does not deliver simple closed-form analytical expressions and requires time-consuming numerical calculations. The ratio between the switching frequency and the fundamental frequency is theoretically supposed to be infinitely large and the load is supposed to be an inductively dominant one.

The voltage and current ripple are obtained by properly integrating their NMS values over one switching period and over the fundamental period what can be roughly understood as double Fourier series. In the first case the modulating signal is constant over time (DC-PWM), while in the second case it has a sinusoidal behaviour (AC-PWM) which can be assumed constant within one switching period due to the specifically defined load. This brings precise and efficient expressions for estimating the output power quality without following complex mathematical transformations.

The suggested methodology is asymptotic in the sense that the ratio of switching and fundamental frequencies is initially assumed infinitely large. This assumption may be interpreted as quasi-static in the time domain meaning that the PWM current ripple is supposed steady state on a switching period. For ratios larger than 25-30 the presented approach works accurately.

This claim is supported by frequency-domain current ripple calculations for single-phase multilevel PWM inverters for different switching and fundamental frequency ratios.

Originally derived for inductance-dominated load, current THD formulas are easily modified to cover a grid-connected single-phase PWM inverter with unity power factor using an appropriate phasor diagram.

Theoretical results are fully supported by detailed Matlab/Simulink simulations and laboratory experiments. Full comparison between theory, simulations and experiments is given proving the correctness of the proposed developments.

4.9 References

[4.1] J. Rodríguez , L.G. Franquelo, S. Kouro, J. I. Leon, R. C. Potrillo, M. Á. M. Prats and M. A. Péres, "Multilevel Converters : An Enabling Technology for High-Power Applications," *Proc. IEEE*, vol. 97, no. 11, pp. 1786-1817 2009.

[4.2] H. Abu-rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-Voltage Multilevel Converters − State of the Industrial Applications," *IEEE Trans. Ind. App.*, vol. 57, no. 8, pp. 2581-2596, 2010.

[4.3] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Pérez, and J. I. Leon, "Recent Advances and Industrial Applications of Multilevel Converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553-2580, 2010.

[4.4] J. Rodríguez, J. Lai, and F. Z. Peng, "Multilevel Inverters : A Survey of Topologies , Controls , and Applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724-738, 2002.

[4.5] J. Rodríguez, S. Bernet, B. Wu, J. O. Pontt, S. Kouro, "Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930-2945, 2007.

[4.6] L.G. Franquelo , J. Rodríguez, J. I. Leon, S. Kouro, R. Portillo, and M. Á. M. Prats, "The Age of Multilevel Converters Arrives," *IEEE Ind. Electron. Mag.*, vol. 2 , no. 2, pp. 28-39, 2008.

[4.7] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A Survey on Neutral-Point-Clamped Inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219-2230, 2010.

[4.8] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Pérez, "A Survey on Cascaded Multilevel Inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2197-2206, 2010.

[4.9] D. G. Holmes and T. A. Lipo, Pulse Width Modulation for Power Converters: Principles and Practice. Hoboken, NJ: Wiley, 2003.

[4.10] F. Wu, J. Duan, and F. Feng, "Modified single-carrier multilevel sinusoidal pulse width modulation for asymmetrical insulated gate bipolar transistor-clamped grid-connected inverter," *IET Power Electron.*, vol. 8, no. 8, pp. 1531–1541, 2015.

[4.11] E. Kabalci, Y. Kabalci, R. Canbaz, and G. Gokkus, “Single Phase Multilevel String Inverter for Solar Applications,” in *International Conference on Renewable Energy Research and Applications (ICRERA)*, Palermo, Italy, 2015, pp. 109–114.

[4.12] J. C. Kartick, B. K. Sujit, and K. Suparna, “Dual reference phase shifted pulse width modulation technique for a N -level inverter based grid connected solar photovoltaic system,” *IET Renewable Power Gen.*, vol. 10, no. 7, pp. 928–935, 2016.

[4.13] N. A. Rahim, K. Chaniago, and J. Selvaraj, “Single-Phase Seven-Level Grid-Connected Inverter for Photovoltaic System,” *IEEE Trans. Ind. Electron.*, vol. 58, no. 6, pp. 2435–2443, 2011.

[4.14] K. K. Gupta and S. Jain, “A Novel Multilevel Inverter Based on Switched DC Sources,” *IEEE Trans. Ind. Electron.*, vol. 61, no. 7, pp. 3269–3278, 2014.

[4.15] J. Choi and F. Kang, “Seven-Level PWM Inverter Employing Series-Connected Capacitors Paralleled to a Single DC Voltage Source,” *IEEE Trans. Ind. Electron.*, vol. 62, no. 6, pp. 3448–3459, 2015.

[4.16] J. I. Leon, L. G. Franquelo, E. Galvan, M. M. Prats, and J. M. Carrasco “Generalized Analytical Approach of the CalcuIation of the Harmonic Effects of Single Phase Multilevel PWM Inverters,” in *30th Annual Conference of IEEE Industrial Electronics Society (IECON)*, Busan, South Korea, 2004, pp. 1658–1663.

[4.17] H. W. van der Broeck, “Analytical calculation of the harmonic effects of single phase multilevel PWM inverters,” in *29th Annual Conference of IEEE Industrial Electronics Society (IECON)*, Roanoke, VA, USA, 2003, pp. 243–248.

[4.18] A. Ruderman, B. Reznikov, and S. Busquets-monge, “Asymptotic Time Domain Evaluation of a Multilevel Multiphase PWM Converter Voltage Quality,” *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1999–2009, 2013.

[4.19] O. Dordevic, M. Jones, and E. Levi, “Analytical formula for leg voltage THD of a PWM multilevel inverter,” in *7th IET International Conference on Power Electronics, Machines and Drives (PEMD)*, Manchester, UK, 2014, pp. 1–6.

[4.20] H. W. van der Broeck; H. -C. Skudelny; G. V. Stanke, “Analysis and Realization of a Pulsewidth Modulator Based on Voltage Space Vectors,” *IEEE Trans. Ind. App.*, vol. 24, no. 1, pp. 142–150, 1988.

[4.21] D. Dujic, M. Jones, and E. Levi, "Analysis of Output Current-Ripple RMS in Multiphase Drives Using Polygon Approach," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1838–1849, 2010.

[4.22] O. Dordevic, M. Jones, and E. Levi, "Analytical Formulas for Phase Voltage RMS Squared and THD in PWM Multiphase Systems," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1645–1656, 2015.

[4.23] A. Ruderman, "Understanding PWM current ripple in star-connected AC motor drive," *IEEE Power Electron. Soc. Newslett.*, vol. 21, no. 2, pp. 14–17, Apr. 2009.

[4.24] G. Grandi, J. Loncarski, and O. Dordevic, "Analytical evaluation of output current ripple amplitude in three-phase three-level inverters," *IET Power Electron.*, vol. 7, no. 9 pp. 2258–2268, 2014.

[4.25] G. Grandi, J. Loncarski, and O. Dordevic, "Analysis and Comparison of Peak-to-Peak Current Ripple in Two-Level and Multilevel PWM Inverters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 2721–2730, 2015.

[4.26] J. Loncarski, M. Leijon, M. Srndovic, C. Rossi, and G. Grandi, "Comparison of output current ripple in single and dual three-phase inverters for electric vehicle motor drives," *Energies*, vol. 8, no. 5, pp. 3832–3848, 2015.

[4.27] J. Loncarski, M. Leijon, C. Rossi, M. Srndovic and G. Grandi, "Current Ripple Evaluation in Dual Three-Phase Inverters for Open-End Winding EV Drives," in *IEEE 3rd International Conference on Connected Vehicles and Expo (ICCVE)*, Vienna, Austria, 2014, pp. 507-513.

[4.28] M. Vujacic, M. Srndovic, M. Hammami and G. Grandi, "Evaluation of DC Voltage Ripple in Single-Phase H-Bridge PWM Inverters," in *42nd Annual Conference of IEEE Industrial Electronics Society (IECON)*, Florence, Italy, 2016, pp. 3235-3240.

[4.29] Boris Reznikov, Gabriele Grandi, Milan Srndovic, Yakov L. Familiant and Alex Ruderman, "Simple Time Averaging Current Quality Evaluation of a Single-Phase Multilevel PWM Inverter," ," *IEEE Trans. Ind. Electron.*, vol. 63, no. 5, pp. 3605–3615, 2016.

[4.30] B. Reznikov, M. Srndovic, G. Grandi, B. Rakhim, Y. Familiant and A.Ruderman, "Asymptotic Time Domain Evaluation of a Single-Phase Multilevel PWM Inverter Current Quality," in *18th International Conference on Electrical Drives and Power electronics (EDPE)*, Tatranska Lomnica, Slovakia, 2015, pp. 42-47.

[4.31] E. Hassan, E. Aboadla, S. Khan, M. H. Habaebi, T. Gunawan, B. A. Hamidah, and M. Bin Yaacob, "Effect of Modulation Index of Pulse Width Modulation Inverter on Total Harmonic Distortion for Sinusoidal," in *International Conference on Intelligent Systems Engineering (ICISE)*, Islamabad, Pakistan 2016. pp. 192–196.

[4.32] D. Park, N. Ku, and R. Kim, "A Novel Switching Loss Minimization Method for Single-phase Flying-Capacitor Multilevel Inverter," in *IEEE 2nd International Future Energy Electronics Conference (IFEEC)*, Taipei, Taiwan, 2015, pp. 1–6.

[4.33] Y. Xia and R. Ayyanar, "Optimal Variable Switching Frequency Scheme to Reduce Combined Switching Loss and Inductor Core Loss of Single Phase Grid Connected Inverter," in *IEEE Energy Conversion Congress and Exposition (ECCE),* Montreal, Canada, 2015, pp. 1534–1540.

[4.34] F. Wu, X. Li, F. Feng, and H. Gooi, "Modified Cascaded Multilevel Grid-Connected Inverter to Enhance European Efficiency and Several Extended Topologies," *IEEE Trans. Ind. Informat.*, vol. 11, no. 6, pp. 1358–1365, 2015.

[4.35] G. Grandi and J. Loncarski "Implementation of Carrier-Based Optimized Centered PWM in Three-Phase Three-Level Inverters," in *International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM)*, Ischia, Italy, 2014, pp. 758–763.

[4.36] G. Grandi, J. Loncarski, and M. Srndovic, "Analysis and Minimization of Output Current Ripple for Discontinuous Pulse-Width Modulation Techniques in Three-Phase Inverters," *Energies*, vol. 9, no. 5, p. 380, 2016.

5. Final discussion

5.1 General conclusion

This thesis deals with the detailed time-domain analysis of the output power quality (output voltage and current total harmonic distortions) in single-phase cascaded H-bridge multilevel inverters considering different modulation techniques, different kinds of load and different number of voltage levels.

Firstly, a single-phase *n*-level inverter controlled by the staircase modulation technique is theoretically analysed providing the optimal voltage and current switching angles using the normalized mean square criteria with the help of Matlab/*fmincon* function. These criteria are applied to output voltage and current ripples for the pure inductive load and optimized in a way that for each value of the modulation index *m* the optimal switching angles are found. The sensitivity of voltage and current THDs to switching angles is presented and twice-optimal modulation indexes are estimated providing the working points where the voltage and current have the minimum THD. Apart from this, the current THD in case of a grid-connected system is evaluated and calculated based on the mentioned optimization.

Secondly, the same power configuration controlled by pulse-width modulation technique (PWM) is theoretically analysed revealing closed-form piecewise analytical solutions for the output power quality estimation. The estimation is based on the asymptotic assumption that the ratio between the switching and fundamental frequencies is infinitely large therefore the sinusoidal modulating signal is considered constant over one switching period. Evaluating the output voltage and current ripples over switching and fundamental periods defines their normalized mean squares values which are turned into THD expressions. Apart from this, the current THD in case of a grid-connected system is evaluated and calculated based on the mentioned approach.

All analytical developments are supported by the detailed simulations using Matlab/Simulink and by a full set of laboratory experiments. Comprehensive comparisons of analytical, simulation and experimental results prove the correctness, effectiveness and applicability of the presented developments.

5.2 Future developments

Developments presented in this thesis leave a large space for further research work in spite of its educational significance and research extensiveness. Some of them are listed here, as possible directions for future work:

- experiments in case of a single-phase multilevel grid-connected inverter;
- investigation of a single-phase multilevel inverter controlled by staircase and pulse-width modulation techniques with non-uniform dc bus voltages;
- extension of analytical developments to three- and multiphase inverters.

Authored publications

The authored publication list related to the subject of the thesis is given in the following. The list includes national meetings, international conferences and international journals.

National meetings:

[A1.1] G. Grandi, J. Loncarski and **M. Srndovic**, "Analisi teorica e sperimentale di inverter multilivello"*, XXX Riunione Nazionale dei Ricercatori Elettrotecnica (ET 2014)*, Sorento, 19-20 Giugno, 2014.

[A1.2] G. Grandi and **M. Srndovic**, "Analisi comparativa del ripple di corrente e delleprestazioni di inverter multilivello"*, XXX Riunione Nazionale dei Ricercatori Elettrotecnica (ET 2015)*, Genova, 17-19 Giugno, 2015.

[A1.3] G. Grandi and **M. Srndovic**, "Tecniche di modulazione ed analisi della distorsione armonica per inverter multilivello mono e multifase", *XXXII Riunione Annuale dei Ricercatori di Elettrotecnica (ET16),* Palermo, 15-17 Giugno, 2016.

[A1.4] G. Grandi, **M. Srndovic**, M. Hammami and M. Vujacic, "Analisi di tensione e corrente in ingresso ad inverter monofase H-bridge per applicazioni fotovoltaiche", *XXXII Riunione Annuale dei Ricercatori di Elettrotecnica (ET16),* Palermo, 15-17 Giugno, 2016.

International conferences:

[A1.5] J. Loncarski, M. Leijon, C. Rossi, **M. Srndovic** and G. Grandi, "Current Ripple Evaluation in Dual Three-Phase Inverters for Open-End Winding EV Drives," in *IEEE 3rd International Conference on Connected Vehicles and Expo (ICCVE)*, Vienna, Austria, 2014, pp. 507-513.

[A1.6] B. Reznikov, **M. Srndovic**, G. Grandi, B. Rakhim, Y. Familiant and A.Ruderman, "Asymptotic Time Domain Evaluation of a Single-Phase Multilevel PWM Inverter Current Quality," in *18th International Conference on Electrical Drives and Power electronics (EDPE)*, Tatranska Lomnica, Slovakia, 2015, pp. 42-47.

[A1.7] M. Vujacic, **M. Srndovic**, M. Hammami and G. Grandi, "Evaluation of DC Voltage Ripple in Single-Phase H-Bridge PWM Inverters," in *42nd Annual Conference of IEEE Industrial Electronics Society (IECON)*, Florence, Italy, 2016, pp. 3235-3240.

International journals:

[A1.8] J. Loncarski, M. Leijon, **M. Srndovic**, C. Rossi, and G. Grandi, "Comparison of output current ripple in single and dual three-phase inverters for electric vehicle motor drives," *Energies*, vol. 8, no. 5, pp. 3832–3848, 2015.

[A1.9] G. Grandi, J. Loncarski and **M. Srndovic**, "Analysis and Minimization of Output Current Ripple for Discontinuous Pulse-Width Modulation Techniques in Three- Phase Inverters," *Energies*, vol. 9, no. 5, p. 380, 2016.

[A1.10] Boris Reznikov, Gabriele Grandi, **Milan Srndovic**, Yakov L. Familiant and Alex Ruderman, "Simple Time Averaging Current Quality Evaluation of a Single-Phase Multilevel PWM Inverter," ," *IEEE Trans. Ind. Electron.*, vol. 63, no. 5, pp. 3605–3615, 2016.

[A1.11] **M. Srndovic**, Y. Familiant, G. Grandi and A. Ruderman: "Time Domain Minimization of Voltage and Current Total Harmonic Distortion for a Single-Phase Multilevel Inverter with a Staircase Modulation," *Energies*, vol. 9, no. 10, p. 815, 2016.

Appendix 1

In this appendix the H-bridge power board, Arduino DUE microcontroller board and interface control board are shortly described focusing on their main characteristics and design. For designing all PCB boards the Altium software was used, therefore the corresponding schemes are presented.

Appendix 1.1

The H-bridge inverter used for all experiments was designed by using the Altium software with the help of some department technicians and master students. Since a three-phase power component is used, only two legs are connected on the PCB board, while the third one is properly grounded. The main characteristic of the power board are explained in the chapter related to the experimental part (2.3), so here a designed scheme with some details from the Altium program is given in Figure A1.1.1.

The scheme shows control and power parts of the power module. On the control side there are two control signals going into two optical receivers (green dashed rectangle). They are transferred through the dead-time circuits (red dashed rectangle) to the four power switches of a PS22A76 IGBT power module. All components that are between the dead-line circuits and power switches are chosen according to the data sheet of the power module and an application note. Apart from control signals, there is one pin which a small current goes through in case of a fault in the power module. This current lights a led diode as a fault sign. It is emphasized with an orange rectangle. All components of the control side are designed to withstand the maximum dc voltage of +15V or +5V and the current in order of 0.5A.

On the power side (blue dashed rectangle) there is a dc bus connection and two outputs, two middle points of two inverters legs, together with a common ground connection. Four dc electrolytic capacitors are connected in series, each one with the rated voltage 150V, in total 600V. There are also three small smd capacitors to balance the voltage overshoots and high frequency current ripples during switching commutations. In case of the power side the maximum voltage and current are 600V and 25A, respectively.

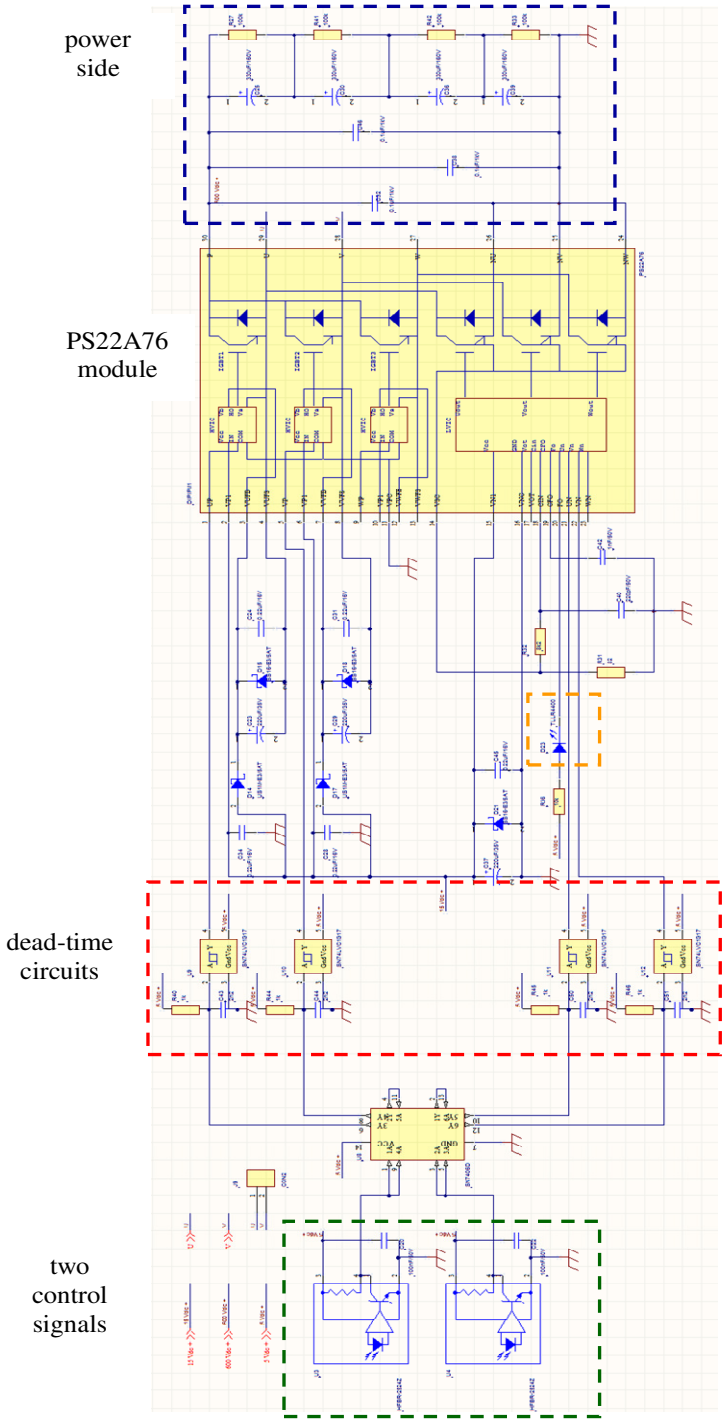


Figure A1.1.1. Scheme of the H-bridge PCB board made in Altium (horizontal view)

Appendix 1.2

An Arduino DUE microcontroller board (based on 84-MHz Atmel SAM3X83 ARM Cortex-M3 CPU) was used for generating the control signals for all experiments. In Figure A1.2.1. the board is presented with emphasized pins used as PWM outputs: 8, 9, 34, 36, 38 and 40. In the program code those pins are selected for generating the control signals.

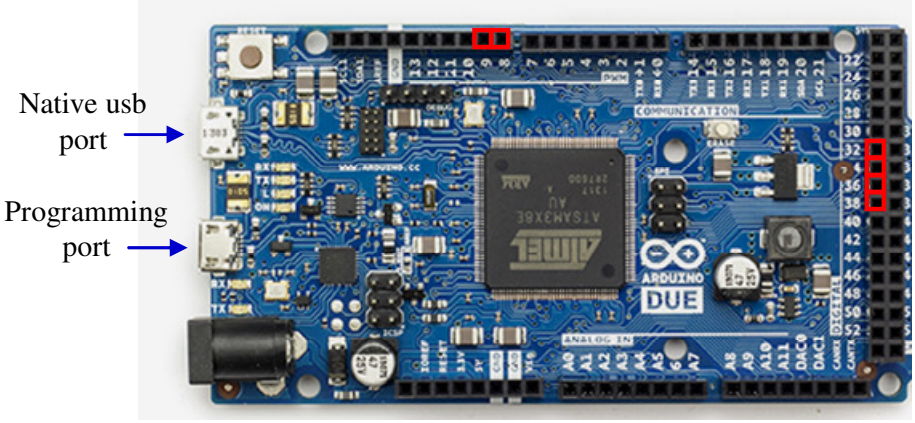


Figure A1.2.1. Arduino DUE evaluation board

Apart from this, in Figure A1.2.2. the Arduino DUE pinout diagram is presented with all available channels on the microcontroller board. The PWM channels 0, 1, 2, 3, 4 and 5 used for experiments are emphasized in red. In general, each channel has *low* (*L*) and *high* (*H*) parts in order to provide two complementary signals when it is needed. For the experimental purposes, only the *low* channels are used, since for each inverter leg only one signal is required (the opposite one is directly provided on the inverter PCB board). Those channels are PWML0-PWML5 where *L* stands for a *low* channel.

As it can be noticed, this microcontroller evaluation board has a variety of pins for different uses. The voltage limit of each pin is 3.3V, so applying a voltage over the limit can cause an irreversible damage to the circuitry on the board including the Atmel processor. The main board supply is provided with a standard 2.1mm plug having 7-12V. Using a usb connector via programming port or via native usb port can provide a proper board supply as well as a communication with the C program code.

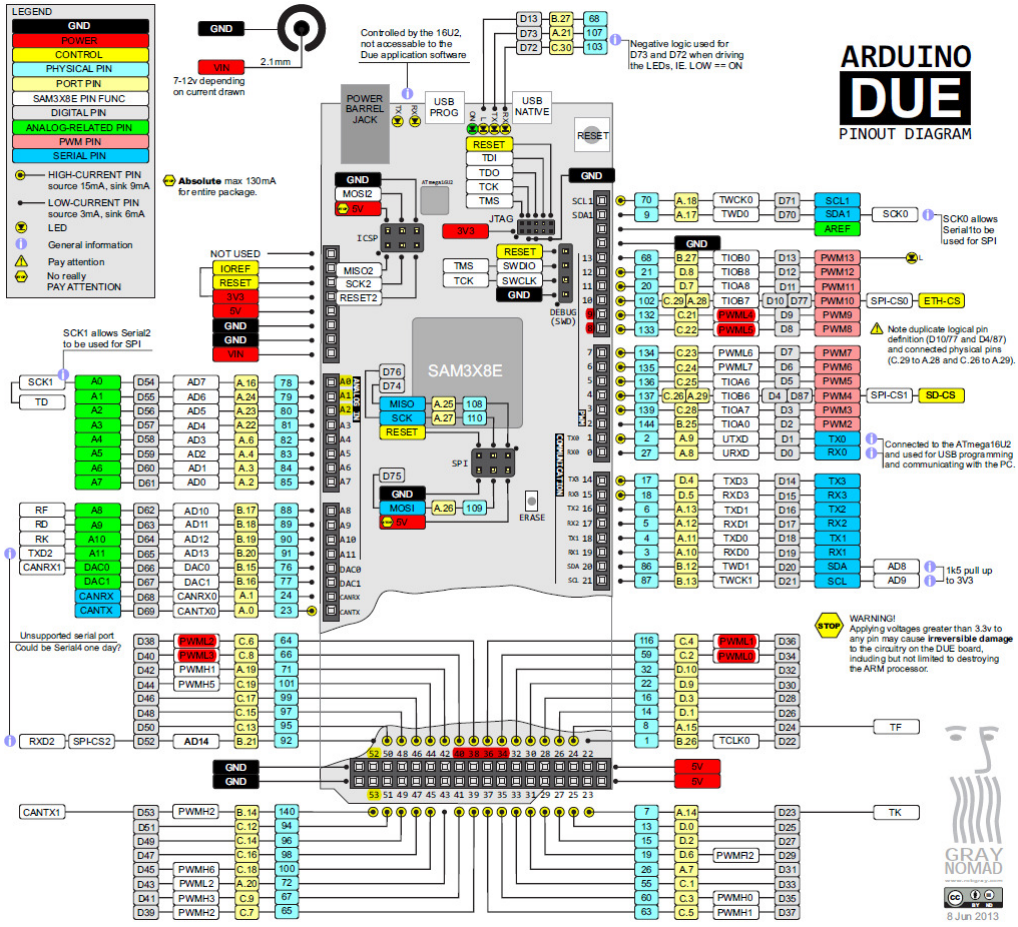


Figure A1.2.2. Arduino DUE pinout diagram

Appendix 1.3

The interface control board, already mentioned in the experimental part of the thesis (2.3), is used to transfer control signals from the microcontroller to power switches. Using this board, the control signal voltage levels are adjusted to ones required for the power switches and some possible disturbances while transferring signals are diminished. In Figure A1.3.1. the interface board scheme made in Altium software is presented. The design is made in a way that there are twelve channels for independently transferring control signals. Each channel has one corresponding pin which is connected to the microcontroller. At the end of the board there are twelve optical emitters used for the optical fiber connections for further signal transfer.

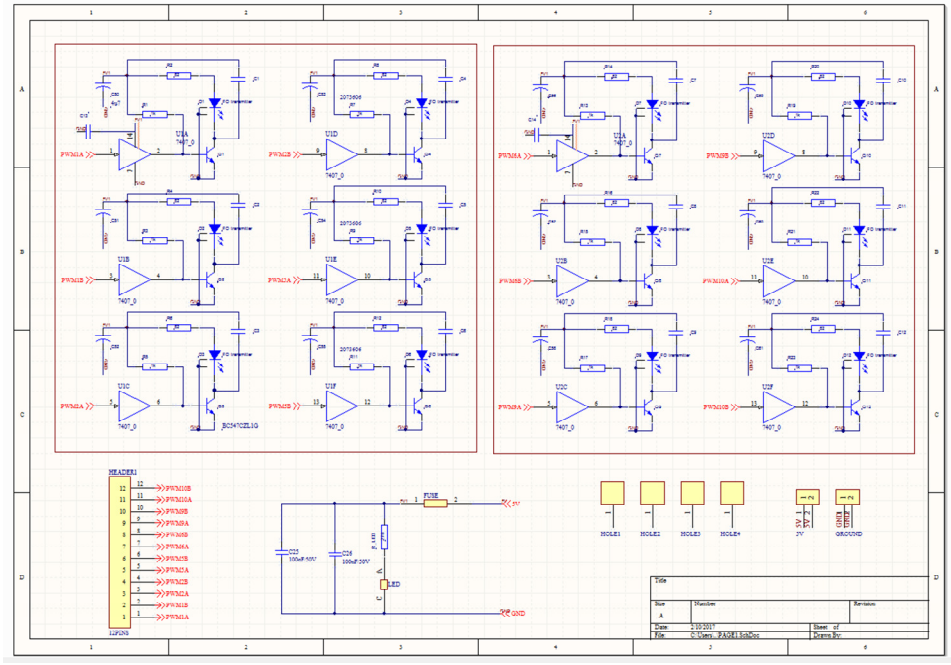


Figure A1.3.1. Scheme of the interface control board made in Altium

In Figure A1.3.2., 2D and 3D models of the board are presented where all connections can be seen together will all components. Apart from this, the printed PCB board used in the experiments is presented in Figure A1.3.3. The board is designed to be supplied by +5V dc voltage having the current around 0.5A when all twelve channels are working. As a protection one fuse is installed on the + side of the input voltage with a possibility of replicating it easily in case of a fault. One led diode with a nominal current 20mA is put close to the main supply in order to have a feedback when the board is connected.

(a)

(b)

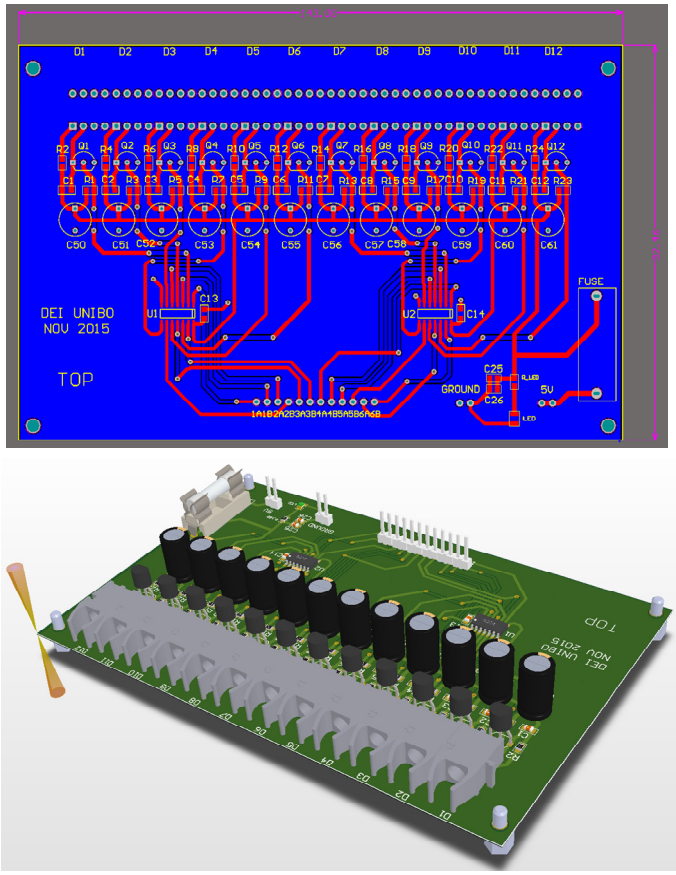


Figure A1.3.2. Interface control board designed in Altium: (a) 2D view and (b) 3D view.

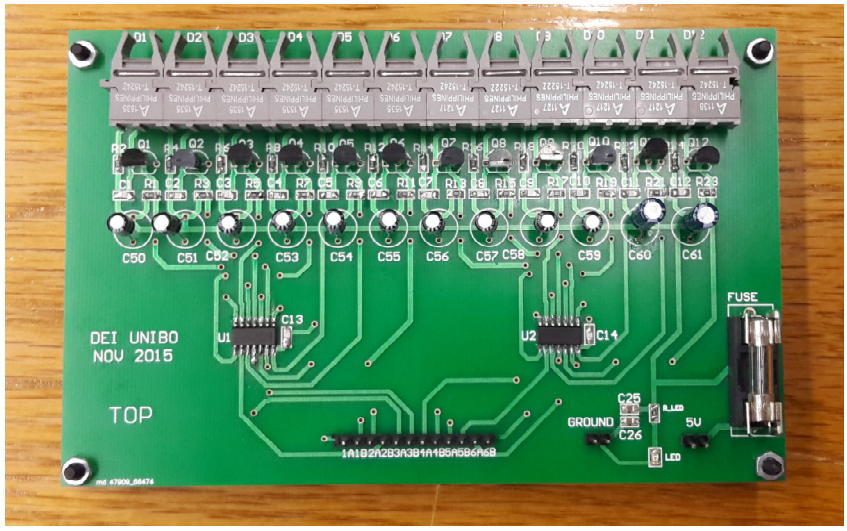


Figure A1.3.3. Printed PCB interface control board

Appendix 2

For a single-phase *n*-level H-bridge inverter controlled by the staircase modulation technique, the current ripple NMS is found as:

$$NMS_I^n(\beta,m)=\frac{2}{\pi}\int_0^{\pi/2} i^2\,d\beta-\frac{1}{2}m^2\,. \tag{A2.1}$$

Adjusting (A2.1) to a single-phase five-level inverter with two switching angles β_1 and β_2, the current ripple NMS is:

$$NMS_I^5(\beta_1,\beta_2,m)=\frac{2}{\pi}\left(\int_0^{\beta_1}(2\beta)^2\,d\beta+\int_{\beta_1}^{\beta_2}(\beta_1+\beta)^2\,d\beta+\int_{\beta_2}^{\pi/2}(\beta_1+\beta_2)^2\,d\beta\right)-\frac{1}{2}m^2\,. \tag{A2.2}$$

In (A2.2) there are three integral forms that can be separately calculated. Their solutions are:

$$I=\frac{2}{\pi}\int_0^{\beta_1}(2\beta)^2\,d\beta=\frac{4}{3\pi}\beta_1^3\,. \tag{A2.3}$$

$$II=\frac{2}{\pi}\int_{\beta_1}^{\beta_2}(\beta_1+\beta)^2\,d\beta=-\frac{2}{3\pi}\left((\beta_1+\beta_2)^3-8\beta_1^3\right)=-\frac{2}{3\pi}\left(7\beta_1^3-3\beta_1^2\beta_2-3\beta_1\beta_2^2-\beta_2^3\right). \tag{A2.4}$$

$$III=\frac{2}{\pi}\int_{\beta_2}^{\pi/2}(\beta_1+\beta_2)^2 d\beta=(\beta_1+\beta_2)^2\left(\frac{\pi}{2}-\beta_2\right). \tag{A2.5}$$

Summing all three integral forms and subtracting the normalized mean square of the current fundamental component, the current ripple NMS value for a single-phase five-level inverter becomes:

$$\begin{aligned} &NMS_I^5(\beta_1,\beta_2,m)=(\beta_1+\beta_2)^2-\frac{\frac{6}{3}\beta_1^3+\frac{6}{3}\beta_1\beta_2^2+\frac{4}{3}\beta_2^3}{\pi}-\frac{1}{2}m^2\,,\\ &\beta_1=\frac{\pi}{2}-\alpha_2\,,\ \beta_2=\frac{\pi}{2}-\alpha_1\,. \end{aligned} \tag{A2.6}$$

For a single-phase seven-level inverter with three switching angles β_1, β_2 and β_3, properly adjusting (A2.1), the current ripple NMS is:

$$NMS_I^7(\beta_1,\beta_2,\beta_3,m)=\frac{2}{\pi}\left(\begin{array}{l}\displaystyle\int_0^{\beta_1}(3\beta)^2\,d\beta+\int_{\beta_1}^{\beta_2}(\beta_1+2\beta)^2\,d\beta+\int_{\beta_2}^{\beta_3}(\beta_1+\beta_2+\beta)^2\,d\beta\\ \displaystyle+\int_{\beta_3}^{\pi/2}(\beta_1+\beta_2+\beta_3)^2\,d\beta\end{array}\right)-\frac{1}{2}m^2\,. \tag{A2.7}$$

In (A2.7) there are four integral forms that can be separately calculated. Their solutions are:

$$I = \frac{2}{\pi}\int_{0}^{\beta_1} (3\beta)^2\, d\beta = \frac{2}{\pi} 3\beta_1^3 . \tag{A2.8}$$

$$II = \frac{2}{\pi}\int_{\beta_1}^{\beta_2} (\beta_1 + 2\beta)^2\, d\beta = \frac{2}{\pi}\left(-\frac{13}{3}\beta_1^3 + \beta_1^2\,\beta_2 + 2\beta_1\,\beta_2^3 + \frac{4}{3}\beta_2^3 \right). \tag{A2.9}$$

$$III = \frac{2}{\pi}\int_{\beta_2}^{\beta_3} (\beta_1 + \beta_2 + \beta)^2\, d\beta = \frac{2}{\pi}\left(\begin{array}{l} -\beta_1^2\,\beta_2 - 3\beta_1\beta_2^2 - \frac{7}{3}\beta_2^3 + \\ +\left(\beta_1^2\beta_3 + 2\beta_1\beta_2\beta_3 + \beta_2^2\beta_3 + \beta_1\beta_3^2 + \beta_2\beta_3^2\right) + \frac{1}{3}\beta_3^3 \end{array} \right). \tag{A2.10}$$

$$\begin{aligned} IV &= \frac{2}{\pi}\int_{\beta_3}^{\pi/2} (\beta_1 + \beta_2 + \beta_3)^2\, d\beta = \\ &= (\beta_1 + \beta_2 + \beta_3)^2 - \frac{2}{\pi}\left(\beta_1^2\beta_3 + 2\beta_1\beta_2\beta_3 + 2\beta_1\beta_3^2 + \beta_2^2\beta_3 + 2\beta_2\beta_3^2 + \beta_3^3\right). \end{aligned} \tag{A2.11}$$

Summing all four integral forms and subtracting the normalized mean square of the current fundamental component, the current ripple NMS value for a seven-level single-phase inverter becomes:

$$\begin{aligned} &NMS_I^7(\beta_1,\beta_2,\beta_3,m) = \\ &= (\beta_1 + \beta_2 + \beta_3)^2 - \frac{\frac{8}{3}\beta_1^3 + \frac{6}{3}\beta_2^3 + \frac{4}{3}\beta_3^3 + 2\left(\beta_1\beta_2^2 + \beta_1\beta_3^2 + \beta_2\beta_3^2\right)}{\pi} - \frac{1}{2}m^2 . \end{aligned} \tag{A2.12}$$

For an arbitrary level count n following the rule in common of the previous equations for single-phase five- and seven-level inverters, the general current NMS formula becomes:

$$NMS_I^n\left(\beta_1,\beta_2,...,\beta_{\frac{n-1}{2}},m\right) = \left(\sum_{k=1}^{(n-1)/2}\beta_k\right)^2 - \frac{2}{\pi}\left(\begin{array}{l} \frac{1}{3}\sum_{k=1}^{(n-1)/2}\left(\frac{n-1}{2}+2-k\right)\beta_k^3 + \\ +\sum_{k=1}^{(n-3)/2}\left(\beta_k\sum_{i=k+1}^{(n-1)/2}\beta_i^2\right) \end{array} \right) - \frac{1}{2}m^2, \tag{A2.13}$$

$$\beta_k = \frac{\pi}{2} - \alpha_{\frac{n+1}{2}-k}\ ,\ k = 1,2,...,(n-1)/2 .$$

Appendix 3

The Arduino DUE program code for the staircase modulation with three cascaded H-bridges and three different switching angles is presented in the following. A brief explanation of the code steps is given at the end, focusing on the main characteristics and principles.

Program code:

```
**************************************************************************
const float pi = 3.1415;
int k = 0; // constant
float carrierfreq = 1600;
int clkfreq = 83999999;
float cprd = (clkfreq / (carrierfreq * 2)); // defining the carrier frequency
float m1 = 0; // modulation index, first H-BRIDGE
float m2 = 0; // modulation index, second H-BRIDGE
float m3 = 0; // modulation index, third H-BRIDGE
float alpha1 = pi / 8; // first angle
float alpha2 = pi / 4; // second angle
float alpha3 = pi / 3; // third angle

void PWM_Handler(void)
{
 PWM->PWM_ISR2;

 // First 10 ms

 if ( k < 1) {
  // First bridge, first leg, pin 34,
  PWM->PWM_CH_NUM[0].PWM_CDTYUPD = (alpha1 / (pi / 2)) * cprd;
  // First bridge, second leg, pin 36
  PWM->PWM_CH_NUM[1].PWM_CDTYUPD = cprd;
  // Second bridge, first leg, pin 38
  PWM->PWM_CH_NUM[2].PWM_CDTYUPD = (alpha2 / (pi / 2)) * cprd;
  // Second bridge, second leg, pin 40
  PWM->PWM_CH_NUM[3].PWM_CDTYUPD = cprd;
  // Third bridge, first leg, pin 9
  PWM->PWM_CH_NUM[4].PWM_CDTYUPD = (alpha3 / (pi / 2)) * cprd;
  // Third bridge, second leg, pin 8
  PWM->PWM_CH_NUM[5].PWM_CDTYUPD = cprd;

 }
 //Second 10 ms
 else {
  // First bridge, first leg, pin 34,
  PWM->PWM_CH_NUM[0].PWM_CDTYUPD = cprd;
  // First bridge, second leg, pin 36
```

```
    PWM->PWM_CH_NUM[1].PWM_CDTYUPD = (alpha1 / (pi / 2)) * cprd;
    // Second bridge, first leg, pin 38
    PWM->PWM_CH_NUM[2].PWM_CDTYUPD = cprd;
    // Second bridge, second leg, pin 40
    PWM->PWM_CH_NUM[3].PWM_CDTYUPD = (alpha2 / (pi / 2)) * cprd;
    // Third bridge, first leg, pin 9
    PWM->PWM_CH_NUM[4].PWM_CDTYUPD = cprd;
    // Third bridge, second leg, pin 8
    PWM->PWM_CH_NUM[5].PWM_CDTYUPD = (alpha3 / (pi / 2)) * cprd;
   }

   m1 = (alpha1 / (pi / 2)) * cprd;
   m2 = (alpha2 / (pi / 2)) * cprd;
   m3 = (alpha3 / (pi / 2)) * cprd;

   if (k < 1) {
    k++;
   }
   else {
    k = 0;
   }
}

void setPWMpin(uint32_t pin) {
  PIO_Configure(g_APinDescription[pin].pPort,
                PIO_PERIPH_B,
                g_APinDescription[pin].ulPin,
                g_APinDescription[pin].ulPinConfiguration);
}

void setup() {

  setPWMpin(34);
  setPWMpin(35);
  setPWMpin(36);
  setPWMpin(37);
  setPWMpin(38);
  setPWMpin(39);
  setPWMpin(40);
  setPWMpin(41);
  setPWMpin(8);
  setPWMpin(9);
  pmc_enable_periph_clk(ID_PWM);
  PWMC_DisableChannel(PWM, 0);
  PWMC_DisableChannel(PWM, 1);
  PWMC_DisableChannel(PWM, 2);
  PWMC_DisableChannel(PWM, 3);
  PWMC_DisableChannel(PWM, 4);
  PWMC_DisableChannel(PWM, 5);
```

```
PWMC_ConfigureClocks(clkfreq, 0, VARIANT_MCK);

 PWMC_ConfigureSyncChannel (PWM, PWM_SCM_SYNC0 | PWM_SCM_SYNC1 |
PWM_SCM_SYNC2 | PWM_SCM_SYNC3 | PWM_SCM_SYNC4 | PWM_SCM_SYNC5 |
PWM_SCM_SYNC6 | PWM_SCM_SYNC7 , PWM_SCM_UPDM_MODE1, 0, 0);

  // Configuring channel 0
  PWMC_ConfigureChannelExt(PWM,0,
                    PWM_CMR_CPRE_CLKA,
                    PWM_CMR_CALG,
                    PWM_CMR_CPOL,
                    PWM_CMR_CES,
                    PWM_CMR_DTE,
                    0,0);
  PWMC_SetPeriod(PWM, 0, cprd);
  PWMC_SetDutyCycle(PWM, 0, m1);

  // Configuring channel 1
  PWMC_ConfigureChannelExt(PWM,1,
                    PWM_CMR_CPRE_CLKA,
                    PWM_CMR_CALG,
                    PWM_CMR_CPOL,
                    PWM_CMR_CES,
                    PWM_CMR_DTE,
                    0,0);
  PWMC_SetPeriod(PWM, 1, cprd);
  PWMC_SetDutyCycle(PWM, 1, m1);

  // Configuring channel 2
  PWMC_ConfigureChannelExt(PWM,2,
                    PWM_CMR_CPRE_CLKA,
                    PWM_CMR_CALG,
                    PWM_CMR_CPOL,
                    PWM_CMR_CES,
                    PWM_CMR_DTE,
                    0,0);
  PWMC_SetPeriod(PWM, 2, cprd);
  PWMC_SetDutyCycle(PWM, 2, m2);

  // Configuring channel 3
  PWMC_ConfigureChannelExt(PWM,3,
                    PWM_CMR_CPRE_CLKA,
                    PWM_CMR_CALG,
                    PWM_CMR_CPOL,
                    PWM_CMR_CES,
                    PWM_CMR_DTE,
                    0,0);
  PWMC_SetPeriod(PWM, 3, cprd);
  PWMC_SetDutyCycle(PWM, 3, m2);
```

```
  // Configuring channel 4
  PWMC_ConfigureChannelExt(PWM,4,
                           PWM_CMR_CPRE_CLKA,
                           PWM_CMR_CALG,
                           PWM_CMR_CPOL,
                           PWM_CMR_CES,
                           PWM_CMR_DTE,
                           0,0);
  PWMC_SetPeriod(PWM, 4, cprd);
  PWMC_SetDutyCycle(PWM, 4, m3);

  // Configuring channel 5
  PWMC_ConfigureChannelExt(PWM,5,
                           PWM_CMR_CPRE_CLKA,
                           PWM_CMR_CALG,
                           PWM_CMR_CPOL,
                           PWM_CMR_CES,
                           PWM_CMR_DTE,
                           0,0);
  PWMC_SetPeriod(PWM, 5, cprd);
  PWMC_SetDutyCycle(PWM, 5, m3);

  PWMC_EnableChannel(PWM, 0);
  PWMC_EnableChannel(PWM, 1);
  PWMC_EnableChannel(PWM, 2);
  PWMC_EnableChannel(PWM, 3);
  PWMC_EnableChannel(PWM, 4);
  PWMC_EnableChannel(PWM, 5);


  NVIC_DisableIRQ(PWM_IRQn);
  NVIC_ClearPendingIRQ(PWM_IRQn);
  NVIC_SetPriority(PWM_IRQn, 0);
  NVIC_EnableIRQ(PWM_IRQn);
  PWMC_EnableIt(PWM, 0, PWM_IER2_WRDY);

}

void loop() {
}
*****************************************************************************
```

Short code description:

The main parameters are initially defined at the beginning of the code. Two parameters *carrierfreq* and *clkreq* are used to define the proper carrier frequency calculating the parameter *cprd*. This presents the maximum of the microcontroller clock which starts from zero and reaches this value. The centre-aligned carrier frequency is set at 100Hz in this case. Since there are three H-bridges, each one has its modulation index, therefore there are three modulation indexes defined as m_1, m_2 and m_3. Apart from this there are three angles labelled as $alpha_1$, $alpha_2$ and $alpha_3$ which can be set as chosen switching angles for the given configuration.

In the next part of the code there is a parameter called *k* which counts 0 and 1, therefore there are two cycles in the loop which give control signals properly comparing three modulating signals and one carrier. Since the carrier frequency is 100Hz, every 10ms there is a comparison between the modulation signals, which define the switching angles, and the carrier. Doing so, three control signals with the fundamental frequency of 50Hz are provided. The comparison is done using the instruction PWM->PWM_CH_NUM[*x*].PWM_CDTYUPD, where *x* presents the number of a microcontroller channel.

In the first cycle when *k*=0, the comparison between the modulating signals and the carrier is provided for channels 0, 2 and 4 following the rule explained in chapter 3.5. In this way, three control signals (each one for one H-bridge leg) are provided while for other legs the modulation signal equals *cprd*. Setting the modulation signal *cprd* gives the control signal equals zero since in the program code it is set by the instruction PWM_CMR_CPOL. In the second cycle the procedure is vice versa. It should be noted once again that for one H-bridge leg, the control signal for one switch of the inverter leg is given by the microcontroller while its counterpart is created directly on the PCB board using proper electronic components.

Another part of the code presents basic instructions for setting all channels, synchronizing them, defining all parameters of one PWM channel and some additional instructions that are required by the data sheet in order to properly use all channels.

Appendix 4

In case of a single phase *n*-level inverter, in order to calculate the ac voltage ripple NMS between two adjacent voltage levels, the integral form, defined as $a_V^n(m)$, is:

$$a_V^n(m) = NMS_{V,ac}^n(\theta_i \le \theta \le \theta_{i+1}) = \frac{2}{\pi} \int_{\theta_1=\arcsin\left(\frac{i}{m}\right)}^{\theta_{i+1}=\arcsin\left(\frac{i+1}{m}\right)} (m\sin(\theta)-i)((i+1)-m\sin(\theta))\,d\theta, \tag{A4.1}$$

$i = 0, 1, 2, ..., (n-5)/2$, $i \le m \le i+1$.

Solving the previous integral results:

$$\begin{aligned} a_V^n(m) &= -\frac{1}{\pi}\left(\begin{array}{l} -(3i+2)\sqrt{m^2-i^2} + (3i+1)\sqrt{m^2-(i+1)^2} + \\ -\left(2i(i+1)+m^2\right)\arcsin\left(\frac{i}{m}\right) + \left(2i(i+1)+m^2\right)\arcsin\left(\frac{i+1}{m}\right) \end{array}\right) = \\ &= \frac{3i+2}{\pi}\sqrt{m^2-i^2} - \frac{3i+1}{\pi}\sqrt{m^2-(i+1)^2} + \\ &+ \frac{1}{\pi}\left(2i(i+1)+m^2\right)\left[\arcsin\left(\frac{i}{m}\right) - \arcsin\left(\frac{i+1}{m}\right)\right], \\ &i = 0, 1, 2, ..., (n-5)/2,\ i \le m \le i+1. \end{aligned} \tag{A4.2}$$

When the contribution to the ac voltage ripple NMS value comes from the last voltage level, the integral form, defined as $b_V^n(m)$, becomes:

$$b_V^n(m) = NMS_{V,ac}^n\left(\theta_k \le \theta \le \frac{\pi}{2}\right) = \frac{2}{\pi} \int_{\theta_k=\arcsin\left(\frac{k}{m}\right)}^{\frac{\pi}{2}} (m\sin(\theta)-k)((k+1)-m\sin(\theta))\,d\theta, \tag{A4.3}$$

$k = (n-3)/2$, $k \le m \le k+1$.

Solving (A4.3) results:

$$\begin{aligned} b_V^n(m) &= \frac{1}{\pi}(3k+2)\sqrt{m^2-i^2} + \frac{1}{\pi}\left(2k(k+1)+m^2\right)\left(\arcsin\left(\frac{k}{m}\right) - \frac{\pi}{2}\right), \\ &k = (n-3)/2,\ k \le m \le k+1. \end{aligned} \tag{A4.4}$$

To get the final value of the ac voltage ripple NMS, it is needed to sum together (A4.2) and (A4.4) in a proper way:

$$NMS_{V,ac}^n(m) = \sum_{i=0}^{(n-5)/2} a_V^n(m) + b_V^n(m) = \sum_{i=0}^{k-1} a_V^n(m) + b_V^n(m),\ k = \frac{n-3}{2}. \tag{A4.5}$$

Writing (A4.5) in a full form becomes:

$$NMS_{V,ac}^{n}(m)=\sum_{i=0}^{k-1}\left(\begin{array}{l}\dfrac{3i+2}{\pi}\sqrt{m^2-i^2}-\dfrac{3i+1}{\pi}\sqrt{m^2-(i+1)^2}+\\ +\dfrac{1}{\pi}\left(2i(i+1)+m^2\right)\left[\arcsin\left(\dfrac{i}{m}\right)-\arcsin\left(\dfrac{i+1}{m}\right)\right]\end{array}\right)+$$
$$+\frac{1}{\pi}(3k+2)\sqrt{m^2-i^2}+\frac{1}{\pi}\left(2k(k+1)+m^2\right)\left(\arcsin\left(\frac{k}{m}\right)-\frac{\pi}{2}\right). \tag{A4.6}$$

Equation (A4.6) can be divided into four parts:

$$NMS_{V,ac}^{n}(m)=\sum_{i=0}^{k-1}\left(\frac{1}{\pi}\left(2i(i+1)+m^2\right)\arcsin\left(\frac{i}{m}\right)+\frac{3i+2}{\pi}\sqrt{m^2-i^2}\right)+$$
$$+\sum_{i=0}^{k-1}\left(\left(-\frac{1}{\pi}\right)\left(2i(i+1)+m^2\right)\arcsin\left(\frac{i+1}{m}\right)-\frac{3i+1}{\pi}\sqrt{m^2-(i+1)^2}\right)+ \tag{A4.7}$$
$$+\left(\frac{1}{\pi}(3k+2)\sqrt{m^2-i^2}+\frac{1}{\pi}\left(2k(k+1)+m^2\right)\arcsin\left(\frac{k}{m}\right)\right)-\left(\frac{1}{\pi}\left(2k(k+1)+m^2\right)\frac{\pi}{2}\right).$$

Considering that (A4.7) consists of four parts, each part can be rearranged separately in order to get the final compact form of the ac normalized voltage ripple. The first part of (A4.7) can be written in a way that the sum is split into two parts for i=0 and for i starting from 1. In this case, this part becomes:

$$NMS_{V,ac}^{n}(m)^1=\sum_{i=0}^{k-1}\left(\frac{1}{\pi}\left(2i(i+1)+m^2\right)\arcsin\left(\frac{i}{m}\right)+\frac{3i+2}{\pi}\sqrt{m^2-i^2}\right)=$$
$$=\sum_{i=0}\left(\frac{1}{\pi}\left(2i(i+1)+m^2\right)\arcsin\left(\frac{i}{m}\right)+\frac{3i+2}{\pi}\sqrt{m^2-i^2}\right)+$$
$$+\sum_{i=1}^{k-1}\left(\frac{1}{\pi}\left(2i(i+1)+m^2\right)\arcsin\left(\frac{i}{m}\right)+\frac{3i+2}{\pi}\sqrt{m^2-i^2}\right)= \tag{A4.8}$$
$$=\frac{2}{\pi}m+\sum_{i=1}^{k-1}\left(\frac{1}{\pi}\left(2i(i+1)+m^2\right)\arcsin\left(\frac{i}{m}\right)+\frac{3i+2}{\pi}\sqrt{m^2-i^2}\right).$$

The second part can be rewritten in a following way:

$$NMS_{V,ac}^{n}(m)^2=\sum_{i=0}^{k-1}\left(\left(-\frac{1}{\pi}\right)\left(2i(i+1)+m^2\right)\arcsin\left(\frac{i+1}{m}\right)-\frac{3i+1}{\pi}\sqrt{m^2-(i+1)^2}\right)=$$
$$=\sum_{i=1}^{k}\left(\left(-\frac{1}{\pi}\right)\left(2i(i-1)+m^2\right)\arcsin\left(\frac{i}{m}\right)-\frac{3i-2}{\pi}\sqrt{m^2-i^2}\right). \tag{A4.9}$$

The third and fourth parts of (7) are:

$$NMS_{V,ac}^{n}(m)^3=\frac{1}{\pi}(3k+2)\sqrt{m^2-i^2}+\frac{1}{\pi}\left(2k(k+1)+m^2\right)\arcsin\left(\frac{k}{m}\right). \tag{A4.10}$$

$$NMS_{V,ac}^{n}(m)^{4} = -\frac{1}{\pi}\left(2k(k+1)+m^{2}\right)\frac{\pi}{2}. \tag{A4.11}$$

It must be noticed that the third part presents the sum defined in (A4.8) for the case k=1. Combining it with (A4.8) results:

$$\begin{aligned} &NMS_{V,ac}^{n}(m)^{3} + \frac{2}{\pi}m + \sum_{i=1}^{k-1}\left(\frac{1}{\pi}\left(2i(i+1)+m^{2}\right)\arcsin\left(\frac{i}{m}\right)+\frac{3i+2}{\pi}\sqrt{m^{2}-i^{2}}\right) = \\ &= \frac{2}{\pi}m + \sum_{i=1}^{k}\left(\frac{1}{\pi}\left(2i(i+1)+m^{2}\right)\arcsin\left(\frac{i}{m}\right)+\frac{3i+2}{\pi}\sqrt{m^{2}-i^{2}}\right). \end{aligned} \tag{A4.12}$$

Connecting (A4.9), (A4.11) and (A4.12), the ac normalized voltage ripple can be written as:

$$\begin{aligned} &NMS_{V,ac}^{n}(m) = \sum_{i=1}^{k}\left(\frac{1}{\pi}\left(2i(i+1)+m^{2}\right)\arcsin\left(\frac{i}{m}\right)+\frac{3i+2}{\pi}\sqrt{m^{2}-i^{2}}\right) + \\ &+\sum_{i=1}^{k}\left(\left(-\frac{1}{\pi}\right)\left(2i(i-1)+m^{2}\right)\arcsin\left(\frac{i}{m}\right)-\frac{3i-2}{\pi}\sqrt{m^{2}-i^{2}}\right) - k(k+1) - \frac{1}{2}m^{2} + \frac{2}{\pi}m. \end{aligned} \tag{A4.13}$$

Arranging (A4.13) in a way that all is collected within one sum results in:

$$\begin{aligned} NMS_{V,ac}^{n}(m) = \sum_{i=1}^{k}&\left(\begin{array}{l} \frac{2i^{2}}{\pi}\arcsin\left(\frac{i}{m}\right)+\frac{2i}{\pi}\arcsin\left(\frac{i}{m}\right)+\frac{m^{2}}{\pi}\arcsin\left(\frac{i}{m}\right)+ \\ +\frac{3i}{\pi}\sqrt{m^{2}-i^{2}}+\frac{2}{\pi}\sqrt{m^{2}-i^{2}}-\frac{2i^{2}}{\pi}\arcsin\left(\frac{i}{m}\right)+ \\ +\frac{2i}{\pi}\arcsin\left(\frac{i}{m}\right)-\frac{m^{2}}{\pi}\arcsin\left(\frac{i}{m}\right)-\frac{3i}{\pi}\sqrt{m^{2}-i^{2}}+ \\ +\frac{2}{\pi}\sqrt{m^{2}-i^{2}} \end{array}\right) + \\ &-k(k+1)+\frac{1}{2}m^{2}-\frac{2}{\pi}m. \end{aligned} \tag{A4.14}$$

Annulling exact members in (A4.14), the full form becomes:

$$NMS_{V,ac}^{n}(m) = \frac{4}{\pi}\sum_{i=1}^{k}\left(i\arcsin\left(\frac{i}{m}\right)\right)+\frac{4}{\pi}\sum_{i=1}^{k}\left(\sqrt{m^{2}-i^{2}}\right)-k(k+1)-\frac{1}{2}m^{2}+\frac{2}{\pi}m. \tag{A4.15}$$

In case of $0 \le m \le 1$ in (A4.15) we can set k=0 which brings:

$$NMS_{V,ac}^{n}(0 \le m \le 1, k=0) = -\frac{1}{2}m^{2}+\frac{2}{\pi}m. \tag{A4.16}$$

Considering (A4.15) and (A4.16), the final form of the ac normalized voltage ripple is:

$$NMS_{V,ac}^{n}(m)=\left\{\begin{array}{l}-\frac{1}{2}m^2+\frac{2}{\pi}m\ ,\ 0\le m\le 1\\ \frac{4}{\pi}\sum_{i=1}^{k}\left(i\ \arcsin\left(\frac{i}{m}\right)\right)+\frac{4}{\pi}\sum_{i=1}^{k}\left(\sqrt{m^2-i^2}\right)+\frac{2}{\pi}m-\frac{m^2}{2}-k(k+1),\\ i=1,\ 2,...,\ (n-3)/2\ ,\ k=(n-3)/2\ ,\ i\le m\le i+1\ .\end{array}\right\}. \quad \text{(A4.17)}$$

Appendix 5

In case of a single phase *n*-level inverter, in order to calculate the ac current ripple NMS between two adjacent levels the integral form, defined as $a_I^n(m)$, is:

$$a_I^n(m) = NMS_{I,ac}^n(\theta_i \le \theta \le \theta_{i+1}) = \frac{1}{12}\frac{2}{\pi}\int_{\theta_i=\arcsin\left(\frac{i}{m}\right)}^{\theta_{i+1}=\arcsin\left(\frac{i+1}{m}\right)} (m\sin(\theta)-i)^2((i+1)-m\sin(\theta))^2 d\theta, \tag{A5.1}$$

$i = 0, 1, 2,..., (n-5)/2$, $i \le m \le i+1$.

The first solving step of (A5.1) results in:

$$a_I^n(m) = \frac{1}{12}\frac{1}{48\pi}\left[\begin{array}{l} -48(1+2i)(4i^2+4i+3m^2)\sqrt{m^2-i^2}+ \\ 48(1+2i)(4i^2+4i+3m^2)\sqrt{m^2-(i+1)^2}+ \\ +16(1+2i)m^3\cos\left(3\arcsin\left(\frac{i}{m}\right)\right)+ \\ -16(1+2i)m^3\cos\left(3\arcsin\left(\frac{i+1}{m}\right)\right)+ \\ -3\left(\begin{array}{l} 4\left(\begin{array}{l} 16i^3+8i^4+24im^2+8i^2(1+3m^2)+ \\ +m^2(4+3m^2) \end{array}\right)\arcsin\left(\frac{i}{m}\right)- \\ -2m^2(4+24i+26i^2+3m^2)\sin\left(2\arcsin\left(\frac{i}{m}\right)\right) \end{array}\right)+ \\ +3\left(\begin{array}{l} 4\left(\begin{array}{l} 16i^3+8i^4+24im^2+8i^2(1+3m^2)+ \\ +m^2(4+3m^2) \end{array}\right)\arcsin\left(\frac{i+1}{m}\right)+ \\ -8m^2(1+6i+6i^2+m^2)\sin\left(2\arcsin\left(\frac{i+1}{m}\right)\right)+ \\ +m^4\sin\left(4\arcsin\left(\frac{i+1}{m}\right)\right) \end{array}\right) \end{array}\right]. \tag{A5.2}$$

Grouping the members of (A5.2) gives:

$$a_I^n(m)=\frac{1}{12}\frac{1}{48\pi}\left[\begin{array}{l}-48(1+2i)\,(4i^2+4i+3m^2)\sqrt{m^2-i^2}+\\+48(1+2i)\,(4i^2+4i+3m^2)\sqrt{m^2-(i+1)^2}+\\-12\left(8i^2(1+i)^2+4(1+6i(1+i))m^2+3m^4\right)\arcsin\left(\frac{i}{m}\right)+\\-12(1+i)\left(6+28i+26i^2+3m^2\right)\sqrt{m^2-(i+1)^2}+\\+12\left(8i^2(1+i)^2+4(1+6i(1+i))m^2+3m^4\right)\arcsin\left(\frac{i+1}{m}\right)+\\+16(1+2i)\,m^3\cos\left(3\arcsin\left(\frac{i}{m}\right)\right)+\\+16(1+2i)\,m^3\sin\left(3\arccos\left(\frac{i+1}{m}\right)\right)+\\+6m^2\left(4+24i+26i^2+3m^2\right)\sin\left(2\arccos\left(\frac{i}{m}\right)\right)\end{array}\right]. \qquad \text{(A5.3)}$$

In order to better adjust the equation (A5.3), some identities can be introduced:

$$\sin\left(2\arcsin\left(\frac{i}{m}\right)\right)=\frac{1}{m^2}2i\sqrt{m^2-i^2} \qquad \text{(A5.4)}$$

$$\cos\left(3\arcsin\left(\frac{i}{m}\right)\right)=\frac{1}{m^3}\left(m^2-4i^2\right)\sqrt{m^2-i^2} \qquad \text{(A5.5)}$$

$$\sin\left(3\arccos\left(\frac{i+1}{m}\right)\right)=\frac{1}{m^3}\left(4i^2+8i+4-m^2\right)\sqrt{m^2-(i+1)^2} \qquad \text{(A5.6)}$$

Introducing (A5.4), (A5.5) and (A5.6) into (A5.3) gives (A5.7).

$$a_I^n(m)=\frac{1}{48\pi}\left[\begin{array}{l}
-48(1+2i)\,(4i^2+4i+3m^2)\sqrt{m^2-i^2}+\\
+48(1+2i)(4i^2+4i+3m^2)\sqrt{m^2-(i+1)^2}+\\
-12\left(8i^2(1+i)^2+4(1+6i(1+i))m^2+3m^4\right)\arcsin\left(\frac{i}{m}\right)+\\
-12(1+i)\left(6+28i+26i^2+3m^2\right)\sqrt{m^2-(i+1)^2}+\\
+12\left(8i^2(1+i)^2+4(1+6i(1+i))m^2+3m^4\right)\arcsin\left(\frac{i+1}{m}\right)+\\
+16(1+2i)m^3\,\frac{1}{m^3}\left(m^2-4i^2\right)\sqrt{m^2-i^2}+\\
+16(1+2i)m^3\,\frac{1}{m^3}\left(4i^2+8i+4-m^2\right)\sqrt{m^2-(i+1)^2}+\\
+6m^2\left(4+24i+26i^2+3m^2\right)\frac{1}{m^2}\,2i\sqrt{m^2-i^2}
\end{array}\right]. \qquad \text{(A5.7)}$$

Grouping the member of (A5.7) results in:

$$a_I^n(m)=\frac{1}{12\pi}\left[\begin{array}{l}
-2\sqrt{m^2-(i+1)^2}+50\,i^3\left(\sqrt{m^2-(i+1)^2}-\sqrt{m^2-i^2}\right)+\\
+m^2\left(23\sqrt{m^2-(i+1)^2}-32\sqrt{m^2-i^2}\right)+\\
+i^2\left(62\sqrt{m^2-(i+1)^2}-88\sqrt{m^2-i^2}\right)+\\
+i\left(\begin{array}{l}10\sqrt{m^2-(i+1)^2}-36\sqrt{m^2-i^2}+\\ 55m^2\left(\sqrt{m^2-(i+1)^2}-\sqrt{m^2-i^2}\right)\end{array}\right)+\\
+3\left(8i^2(i+1)^2+4(1+6i(i+1))m^2+3m^4\right)\cdot\\
\cdot\left(\arcsin\left(\frac{i+1}{m}\right)-\arcsin\left(\frac{i}{m}\right)\right)
\end{array}\right]. \qquad \text{(A5.8)}$$

Following the equation (A5.8), the final form of the ac current ripple NMS between two adjacent levels is given in (A5.9).

$$a_I^n(m)=\frac{1}{12}\left[\begin{array}{l}\frac{1}{12\pi}\sqrt{m^2-(i+1)^2}\left(\begin{array}{l}2(i+1)\left(25i^2+6i-1\right)+\\+(23+55i)m^2\end{array}\right)+\\-\frac{1}{12\pi}\sqrt{m^2-i^2}\left(2i\left(25i^2+44i+18\right)+(32+55i)m^2\right)+\\+\frac{1}{\pi}\left(\begin{array}{l}2i^2(i+1)^2+\\+\left(6i^2+6i+1\right)m^2+\frac{3}{4}m^4\end{array}\right)\left(\arcsin\left(\frac{i+1}{m}\right)-\arcsin\left(\frac{i}{m}\right)\right)\end{array}\right] \quad \text{(A5.9)}$$

$i=0,1,2,...,(n-5)/2$, $i\le m\le i+1$

When the contribution to the ac current ripple NMS value comes from the last voltage level, the integral form, defined as $b_I^n(m)$, becomes:

$$b_I^n(m)=NMS_{I,ac}^n\left(\theta_k\le\theta\le\frac{\pi}{2}\right)=\frac{1}{12}\frac{2}{\pi}\int_{\theta_k=\arcsin\left(\frac{k}{m}\right)}^{\frac{\pi}{2}}(m\sin(\theta)-k)^2\left((k+1)-m\sin(\theta)\right)^2 d\theta, \quad \text{(A5.10)}$$

$k=(n-3)/2$, $k\le m\le k+1$.

Solving (A5.10) results in:

$$b_I^n(m)=\frac{1}{12}\frac{1}{48\pi}\left[\begin{array}{l}6\left(8k^2(1+k)^2+4\left(1+6k(1+a)\right)m^2+3m^4\right)\left(\pi-2\arcsin\left(\frac{k}{m}\right)\right)+\\-48(1+2k)m\left(4k(1+k)+3m^2\right)\cos\left(\arcsin\left(\frac{k}{m}\right)\right)+\\+16(1+2k)m^3\cos\left(3\arcsin\left(\frac{k}{m}\right)\right)+\\+24m^2\left(1+6k(1+k)+m^2\right)\sin\left(\arcsin\left(\frac{k}{m}\right)\right)+\\-3m^4\sin\left(4\arcsin\left(\frac{k}{m}\right)\right)\end{array}\right]. \quad \text{(A5.11)}$$

It is important to introduce some identities in order to group the members of (A5.11). Those identities are:

$$\cos\left(\arcsin\left(\frac{k}{m}\right)\right)=\frac{1}{m}\sqrt{m^2-k^2}\,. \quad \text{(A5.12)}$$

$$\sin\left(2\arcsin\left(\frac{k}{m}\right)\right)=\frac{1}{m^2}\sqrt{m^2-k^2}\,2k\,. \quad \text{(A5.13)}$$

$$\cos\left(3\arcsin\left(\frac{k}{m}\right)\right)=\frac{1}{m^3}\sqrt{m^2-k^2}\left(m^2-4k^2\right). \tag{A5.14}$$

$$\sin\left(4\arcsin\left(\frac{k}{m}\right)\right)=\frac{1}{m^4}\sqrt{m^2-k^2}\,4k\left(m^2-2k^2\right). \tag{A5.15}$$

Introducing (A5.12), (A5.13), (A5.14) and (A5.15) into (A5.11) gives:

$$b_I^n(m)=\frac{1}{12}\frac{1}{48\pi}\left[\begin{array}{l}\left(16(1+2k)\left(-4k^2+m^2\right)\right)\sqrt{m^2-k^2}+\\-12k\left(-2k^2+m^2\right)\sqrt{m^2-k^2}+\\+48k\left(1+6k(1+k)+m^2\right)\sqrt{m^2-k^2}+\\-48(1+2k)\left(4k(1+k)+3m^2\right)\sqrt{m^2-k^2}+\\+6\left(\begin{array}{l}8k^2(1+k)^2+\\+4(1+6k(1+k))m^2+3m^4\end{array}\right)\left(\pi-2\arcsin\left(\frac{k}{m}\right)\right)\end{array}\right]. \tag{A5.16}$$

Rearranging the members of (A5.16) gives:

$$\begin{aligned}b_I^n(m)&=\frac{1}{12}\frac{1}{48\pi}\left[\begin{array}{l}\sqrt{m^2-k^2}\left(-8k(18+k(44+25k))-4(32+55k)m^2\right)+\\+\left(\begin{array}{l}48k^2(1+k)^2+\\+24(1+6k(1+k))m^2+3m^4\end{array}\right)\left(\pi-2\arcsin\left(\frac{k}{m}\right)\right)\end{array}\right]=\\&=\frac{1}{12}\frac{1}{\pi}\left[\begin{array}{l}\frac{1}{12}\sqrt{m^2-k^2}\left(-2k(18+k(44+25k))-4(32+55k)m^2\right)+\\+\frac{1}{8}\left(8k^2(1+k)^2+4(1+6k(1+k))m^2+3m^4\right)\left(\pi-2\arcsin\left(\frac{k}{m}\right)\right)\end{array}\right].\end{aligned} \tag{A5.17}$$

In (A5.17), three members can be analysed separately and later joined in order to have a compacter equation. In this case, the members can be written as:

$$\begin{aligned}b_I^n(m)^1&=\frac{1}{12}\frac{1}{12\pi}\sqrt{m^2-k^2}\left(-2k(18+k(44+25k))-4(32+55k)m^2\right)=\\&=-\frac{1}{12}\frac{1}{12\pi}\sqrt{m^2-k^2}\left(m^2(32+55k)+2k\left(25k^2+44k+18\right)\right).\end{aligned} \tag{A5.18}$$

$$\begin{aligned}b_I^n(m)^2&=\frac{1}{12}\frac{1}{\pi}\frac{1}{8}\left(8k^2(1+k)^2+4(1+6k(1+k))m^2+18m^4\right)\pi=\\&=\frac{1}{12}\left(k^2(1+k)^2+\left(6k^2+6k+1\right)\frac{m^2}{2}+\frac{3}{8}m^4\right).\end{aligned} \tag{A5.19}$$

$$b_I^n(m)^3 = -\frac{1}{12}\frac{1}{\pi}\frac{1}{8}2\arcsin\left(\frac{k}{m}\right)\left(8k^2(1+k)^2 + 4(1+6k(1+k))m^2 + 18m^4\right) = \\ = -\frac{1}{12}\frac{1}{\pi}\arcsin\left(\frac{k}{m}\right)\left(2k^2(1+k)^2 + \frac{3}{4}m^4 + \left(6k^2+6k+1\right)m^2\right). \quad \text{(A5.20)}$$

Collecting the three previous equations, the expression of the ac current ripple normalized mean square coming from the last voltage level becomes:

$$b_I^n(m) = \frac{1}{12}\left[\begin{array}{l} \arcsin\left(\frac{k}{m}\right)\left[-\frac{1}{\pi}\left(2k^2(1+k)^2 + \left(6k^2+6k+1\right)m^2 + \frac{3}{4}m^4\right)\right] + \\ + \sqrt{m^2-k^2}\left(-\frac{1}{12\pi}\left(m^2(32+55k) + 2k\left(25k^2+44k+18\right)\right)\right) + \\ + \left(k^2(1+k)^2 + \frac{3}{8}m^4 + \frac{\left(6k^2+6k+1\right)}{2}m^2\right) \end{array}\right] \quad \text{(A5.21)}$$

$k = (n-3)/2$, $k \le m \le k+1$

To get the final value of the ac current ripple NMS, it is needed to sum together (A5.9) and (A5.21) in a proper way:

$$NMS_{I,ac}^n(m) = \sum_{i=0}^{(n-5)/2} a_I^n(m) + b_I^n(m) = \sum_{i=0}^{k-1} a_I^n(m) + b_I^n(m),\ k = \frac{n-3}{2}. \quad \text{(A5.22)}$$

Doing so results in:

$$NMS_{I,ac}^n(m) = \frac{1}{12}\left[\begin{array}{l} \left(\sum_{i=0}^{k-1}\left[\begin{array}{l} \frac{1}{12\pi}\sqrt{m^2-(i+1)^2}\left(\begin{array}{l} 2(i+1)\left(25i^2+6i-1\right)+ \\ +(23+55i)m^2 \end{array}\right) + \\ -\frac{1}{12\pi}\sqrt{m^2-i^2}\left(\begin{array}{l} 2i\left(25i^2+44i+18\right)+ \\ +(32+55i)m^2 \end{array}\right) + \\ +\frac{1}{\pi}\left(2i^2(i+1)^2 + \left(6i^2+6i+1\right)m^2 + \frac{3}{4}m^4\right)\cdot \\ \cdot\left(\arcsin\left(\frac{i+1}{m}\right) - \arcsin\left(\frac{i}{m}\right)\right) \end{array}\right]\right) + \\ + \arcsin\left(\frac{k}{m}\right)\left[-\frac{1}{\pi}\left(\begin{array}{l} 2k^2(1+k)^2 + \\ +\left(6k^2+6k+1\right)m^2 + \frac{3}{4}m^4 \end{array}\right)\right] + \\ + \sqrt{m^2-k^2}\left[-\frac{1}{12\pi}\left(m^2(32+55k) + 2k\left(25k^2+44k+18\right)\right)\right] + \\ + \left(k^2(1+k)^2 + \frac{3}{8}m^4 + \frac{\left(6k^2+6k+1\right)}{2}m^2\right) \end{array}\right]. \quad \text{(A5.23)}$$

In (A5.23) it can be noticed that the two members with the coefficient k can be put within the same sum assuming that as a case when $i=k$. These two members, named as I and II, are:

$$I = \frac{1}{12}\left(\arcsin\left(\frac{k}{m}\right)\left(-\frac{1}{\pi}\left(2k^2(1+k)^2+\left(6k^2+6k+1\right)m^2+\frac{3}{4}m^4\right)\right)\right)= \\ \frac{1}{12}\sum_{i=k}\left(\arcsin\left(\frac{i}{m}\right)\left(-\frac{1}{\pi}\left(2i^2(1+i)^2+\left(6i^2+6i+1\right)m^2+\frac{3}{4}m^4\right)\right)\right). \tag{A5.24}$$

$$II = \frac{1}{12}\left(\sqrt{m^2-k^2}\left(-\frac{1}{12\pi}\left(m^2(32+55k)+2k\left(25k^2+44k+18\right)\right)\right)\right)= \\ \frac{1}{12}\sum_{i=k}\left(\sqrt{m^2-i^2}\left(-\frac{1}{12\pi}\left(m^2(32+55i)+2i\left(25i^2+44i+18\right)\right)\right)\right). \tag{A5.25}$$

Introducing (A5.24) and (A5.25) into (A5.23) gives:

$$NMS_{I,ac}^{n}(m) = \frac{1}{12}\sum_{i=0}^{k}\left(\begin{array}{l}-\frac{1}{\pi}\left(2i^2(i+1)^2+\left(6i^2+6i+1\right)m^2+\frac{3}{4}m^4\right)\arcsin\left(\frac{i}{m}\right)+\\ -\frac{1}{12\pi}\sqrt{m^2-i^2}\left(2i\left(25i^2+44i+18\right)+(32+55i)m^2\right)\end{array}\right)+ \\ +\frac{1}{12}\sum_{i=0}^{k-1}\left(\frac{1}{\pi}\left(2i^2(i+1)^2+\left(6i^2+6i+1\right)m^2+\frac{3}{4}m^4\right)\arcsin\left(\frac{i+1}{m}\right)\right)+ \\ +\frac{1}{12}\sum_{i=0}^{k-1}\left(\frac{1}{12\pi}\sqrt{m^2-(i+1)^2}\left(2(i+1)\left(25i^2+6i-1\right)+(23+55i)m^2\right)\right)+ \\ +\frac{1}{12}\left(k^2(1+k)^2+\left(6k^2+6k+1\right)\frac{m^2}{2}+\frac{3}{8}m^4\right). \tag{A5.26}$$

Rearranging (A5.26) gives:

$$NMS_{I,ac}^{n}(m) = -\frac{1}{12\pi}\sum_{i=0}^{k}\left(2i^2(i+1)^2+\left(6i^2+6i+1\right)m^2+\frac{3}{4}m^4\right)\arcsin\left(\frac{i}{m}\right)+ \\ +\frac{1}{12}\sum_{i=0}^{k}-\frac{1}{12\pi}\left(\sqrt{m^2-i^2}\left(2i\left(25i^2+44i+18\right)+(32+55i)m^2\right)\right)+ \\ +\frac{1}{12}\sum_{i=0}^{k-1}\left(\frac{1}{\pi}\left(2i^2(i+1)^2+\left(6i^2+6i+1\right)m^2+\frac{3}{4}m^4\right)\arcsin\left(\frac{i+1}{m}\right)\right)+ \\ +\frac{1}{12}\sum_{i=0}^{k-1}\left(\frac{1}{12\pi}\sqrt{m^2-(i+1)^2}\left(2(i+1)\left(25i^2+6i-1\right)+(23+55i)m^2\right)\right)+ \\ +\frac{1}{12}\left(k^2(1+k)^2+\left(6k^2+6k+1\right)\frac{m^2}{2}+\frac{3}{8}m^4\right). \tag{A5.27}$$

In (A5.27) five members can be analysed separately and later joined in order to get compacter form. Those five members are:

$$NMS^{n}_{I,ac}(m)^{1} = -\frac{1}{12\pi}\sum_{i=0}^{k}\left(2i^2(i+1)^2+\left(6i^2+6i+1\right)m^2+\frac{3}{4}m^4\right)\arcsin\left(\frac{i}{m}\right)= \\ -\frac{1}{12\pi}\sum_{i=1}^{k}\left(2i^2(i+1)^2+\left(6i^2+6i+1\right)m^2+\frac{3}{4}m^4\right)\arcsin\left(\frac{i}{m}\right)+0\left(\sum for\, i=0\right). \tag{A5.28}$$

$$NMS^{n}_{I,ac}(m)^{2} = \frac{1}{12}\sum_{i=0}^{k}-\frac{1}{12\pi}\sqrt{m^2-i^2}\left(2i\left(25i^2+44i+18\right)+\left(32+55i\right)m^2\right)= \\ =\frac{1}{12}\sum_{i=1}^{k}\left(-\frac{1}{12\pi}\sqrt{m^2-i^2}\left(2i\left(25i^2+44i+18\right)+\left(32+55i\right)m^2\right)\right)+ \\ +\frac{1}{12}\left(-\frac{1}{12\pi}\right)32m^3\left(\sum for\, i=0\right). \tag{A5.29}$$

$$NMS^{n}_{I,ac}(m)^{3} = \frac{1}{12}\sum_{i=0}^{k-1}\left(\frac{1}{\pi}\left(2i^2(i+1)^2+\left(6i^2+6i+1\right)m^2+\frac{3}{4}m^4\right)\arcsin\left(\frac{i+1}{m}\right)\right)= \\ =\frac{1}{12}\sum_{i=1}^{k}\left(\frac{1}{\pi}\left(2(i-1)^2i^2+\left(6(i-1)^2+6(i-1)+1\right)m^2+\frac{3}{4}m^4\right)\arcsin\left(\frac{i}{m}\right)\right). \tag{A5.30}$$

$$NMS^{n}_{I,ac}(m)^{4} = \frac{1}{12}\sum_{i=0}^{k-1}\left(\frac{1}{12\pi}\sqrt{m^2-(i+1)^2}\begin{pmatrix}2(i+1)\left(25i^2+6i-1\right)+\\+\left(23+55i\right)m^2\end{pmatrix}\right)= \\ =\frac{1}{12}\sum_{i=1}^{k}\left(\frac{1}{12\pi}\sqrt{m^2-i^2}\left(2i\left(25(i-1)^2+6(i-1)-1\right)+\left(23+55\left(i-1\right)\right)m^2\right)\right). \tag{A5.31}$$

$$NMS^{n}_{I,ac}(m)^{5} = \frac{1}{12}\left(k^2(1+k)^2+\left(6k^2+6k+1\right)\frac{m^2}{2}+\frac{3}{8}m^4\right). \tag{A5.32}$$

After selecting those members, some of them can be collected considering the parts in common. Collecting together (A5.28) and (A5.30) gives:

$$NMS^{n}_{I,ac}(m)^{1}+NMS^{n}_{I,ac}(m)^{3}= \\ =\frac{1}{12\pi}\sum_{i=1}^{k}\left(\begin{pmatrix}-\left(2i^2(i+1)^2+\left(6i^2+6i+1\right)m^2+\frac{3}{4}m^4\right)+\\+\left(2i^2(i-1)^2+\left(6(i-1)^2+6(i-1)+1\right)m^2+\frac{3}{4}m^4\right)\end{pmatrix}\arcsin\left(\frac{i}{m}\right)\right)= \\ =-\frac{1}{12\pi}\sum_{i=1}^{k}\left(i\left(8i^2+12m^2\right)\arcsin\left(\frac{i}{m}\right)\right)=-\frac{1}{3\pi}\sum_{i=1}^{k}\left(i\left(2i^2+3m^2\right)\arcsin\left(\frac{i}{m}\right)\right). \tag{A5.33}$$

Collecting together (A5.29) without the part for i=0 and (A5.31) gives:

$$\begin{aligned} &NMS_{I,ac}^{n}(m)^{2}-\left(\sum for\, i=0\right)+NMS_{I,ac}^{n}(m)^{4}= \\ &=\frac{1}{12}\sum_{i=1}^{k}\frac{1}{12\pi}\sqrt{m^2-i^2}\begin{pmatrix}-\left(2i\left(25i^2+44i+18\right)+\left(32+55i\right)m^2\right)+\\ +\left(2i\left(25(i-1)^2+6(i-1)-1\right)+\left(23+55(i-1)\right)m^2\right)\end{pmatrix}= \\ &=\frac{1}{12}\sum_{i=1}^{k}\frac{1}{12\pi}\sqrt{m^2-i^2}\left(-16\right)\left(11i^2+4m^2\right)=-\frac{1}{9\pi}\sum_{i=1}^{k}\left(\sqrt{m^2-i^2}\left(11i^2+4m^2\right)\right). \end{aligned} \tag{A5.34}$$

Collecting together the part of (A5.29) for i=0 and (A5.32) gives:

$$\begin{aligned} &NMS_{I,ac}^{n}(m)^{2}\left(\sum for\, i=0\right)+NMS_{I,ac}^{n}(m)^{5}= \\ &-\frac{1}{144\pi}32m^3+\frac{1}{12}\left(k^2(1+k)^2+\left(6k^2+6k+1\right)\frac{1}{2}m^2+\frac{3}{8}m^4\right)= \\ &=\frac{k^2(k+1)^2}{12}+\frac{1}{32}m^4-\frac{2}{9\pi}m^3+\frac{\left(6k^2+6k+1\right)}{24}m^2 . \end{aligned} \tag{A5.35}$$

Collecting equations (A5.33), (A5.34) and (A5.35) gives the final form of the ac current ripple NMS:

$$\begin{aligned} &NMS_{I,ac}^{n}(m)=-\frac{1}{\pi}\sum_{i=1}^{k}\left(i\left(\frac{2}{3}i^2+m^2\right)\arcsin\left(\frac{i}{m}\right)\right)-\frac{1}{9\pi}\sum_{i=1}^{k}\left(\sqrt{m^2-i^2}\left(11i^2+4m^2\right)\right)+ \\ &+\frac{k^2(k+1)^2}{12}+\frac{1}{32}m^4-\frac{2}{9\pi}m^3+\frac{\left(6k^2+6k+1\right)}{24}m^2 . \end{aligned} \tag{A5.36}$$

In order to get the expression for the ac current ripple NMS in case of $0\le m\le 1$, parameter k should be set to 0:

$$NMS_{I,ac}^{n}\left(0\le m\le 1\right)=\frac{1}{32}m^4-\frac{2}{9\pi}m^3+\frac{1}{24}m^2 \tag{A5.37}$$

Considering this, the ac current ripple NMS can be finally written as:

$$NMS_{I,ac}^{n}(m)=\left\{\begin{array}{l} \frac{1}{32}m^4-\frac{2}{9\pi}m^3+\frac{1}{24}m^2 ,\ 0\le m\le 1 \\ -\frac{1}{3\pi}\sum_{i=1}^{k}\left(i\left(2i^2+3m^2\right)\arcsin\left(\frac{i}{m}\right)\right)+ \\ -\frac{1}{9\pi}\sum_{i=1}^{k}\left(\sqrt{m^2-i^2}\left(11i^2+4m^2\right)\right)+ \\ +\frac{k^2(k+1)^2}{12}+\frac{1}{32}m^4-\frac{2}{9\pi}m^3+\frac{\left(6k^2+6k+1\right)}{24}m^2 , \\ i=1,2,...,(n-3)/2 ,\ i\le m\le i+1 ,\ k=(n-3)/2 . \end{array}\right\}. \tag{A5.38}$$

Appendix 6

The Arduino DUE program code for the PWM modulation with three cascaded H-bridges using one carrier and six modulating signals is presented in the following. A brief explanation of the code steps is given at the end focusing on the main characteristics and principles.

Program code:

```
**************************************************************************
float x = 0; // argument of the sine function
const float pi = 3.1415;
int i = 0; // constant
int k = 0; // constant
float carrierfreq = 3000; // Carrier frequency
float modfreq = 50; // Modulation frequency
float ris = carrierfreq / modfreq; // points where the sine function is divided
float lookup1[2500];
float lookup2[2500];
float lookup3[2500];
float lookup4[2500];
float lookup5[2500];
float lookup6[2500];
int clkfreq = 83999999;
float cprd = (clkfreq / (carrierfreq * 2));
float m = 0;
float m1 = 0;
float m2 = 0;
float m3 = 0;
float m4 = 0;
float m5 = 0;
float m6 = 0;

void lookuptable() {
  for (i = 0; i <= ris; i++) {
    lookup1[i] = m * sin(x);
    lookup2[i] = m * sin(x) - 1;
    lookup3[i] = m * sin(x) + 1;
    lookup4[i] = m * sin(x) + 2;
    lookup5[i] = m * sin(x) - 2;
    lookup6[i] = m * sin(x) + 3;
    x = x + 2 * pi / ris;
  }
}
void PWM_Handler(void)
{
   PWM->PWM_ISR2;
```

```
m = 1;
m1 = (lookup1[k + 1]) * cprd;
m2 = (lookup2[k + 1]) * cprd;
m3 = (lookup3[k + 1]) * cprd;
m4 = (lookup4[k + 1]) * cprd;
m5 = (lookup5[k + 1]) * cprd;
m6 = (lookup6[k + 1]) * cprd;

if (lookup1[k + 1] >= 0) {
  if (lookup1[k + 1] <= 1) {
    PWM->PWM_CH_NUM[0].PWM_CDTYUPD = m1;
  } else {
    PWM->PWM_CH_NUM[0].PWM_CDTYUPD = (cprd);
  }
} else {
  PWM->PWM_CH_NUM[0].PWM_CDTYUPD = (0);
}
if (lookup2[k + 1] >= 0) {
  if (lookup2[k + 1] <= 1) {
    PWM->PWM_CH_NUM[1].PWM_CDTYUPD = m2;
  } else {
    PWM->PWM_CH_NUM[1].PWM_CDTYUPD = (cprd);
  }
} else {
  PWM->PWM_CH_NUM[1].PWM_CDTYUPD = (0);
}
if (lookup3[k + 1] <= 1) {
  if (lookup3[k + 1] > 0) {
    PWM->PWM_CH_NUM[2].PWM_CDTYUPD = m3;
  } else {
    PWM->PWM_CH_NUM[2].PWM_CDTYUPD = (0);
  }
} else {
  PWM->PWM_CH_NUM[2].PWM_CDTYUPD = cprd;
}
if (lookup4[k + 1] >= 0) {
  if (lookup4[k + 1] <= 1) {
    PWM->PWM_CH_NUM[3].PWM_CDTYUPD = m4;
  } else {
    PWM->PWM_CH_NUM[3].PWM_CDTYUPD = (cprd);
  }
} else {
  PWM->PWM_CH_NUM[3].PWM_CDTYUPD = (0);
}
if (lookup5[k + 1] > 0) {
  if (lookup5[k + 1] <= 1) {
    PWM->PWM_CH_NUM[4].PWM_CDTYUPD = m5;
  }
```

```
else {
      PWM->PWM_CH_NUM[4].PWM_CDTYUPD = (cprd);
    }
  } else {
    PWM->PWM_CH_NUM[4].PWM_CDTYUPD = 0;
  }
if (lookup6[k + 1] <= 1) {
    if (lookup6[k + 1] > 0) {
      PWM->PWM_CH_NUM[5].PWM_CDTYUPD = m6;
    } else {
      PWM->PWM_CH_NUM[5].PWM_CDTYUPD = (0);
    }
  } else {
    PWM->PWM_CH_NUM[5].PWM_CDTYUPD = cprd;
  }
  if ((k + 1) < ris) {
    k++;
  } else {
    k = 0;
  }
}
void setPWMpin(uint32_t pin) {
  PIO_Configure(g_APinDescription[pin].pPort,
                PIO_PERIPH_B,
                g_APinDescription[pin].ulPin,
                g_APinDescription[pin].ulPinConfiguration);
}
void setup() {
  lookuptable();
  setPWMpin(34);
  setPWMpin(35);
  setPWMpin(36);
  setPWMpin(37);
  setPWMpin(38);
  setPWMpin(39);
  setPWMpin(40);
  setPWMpin(41);
  setPWMpin(9);
  setPWMpin(8);
  pmc_enable_periph_clk(ID_PWM);

  PWMC_DisableChannel(PWM, 0);
  PWMC_DisableChannel(PWM, 1);
  PWMC_DisableChannel(PWM, 2);
  PWMC_DisableChannel(PWM, 3);
  PWMC_DisableChannel(PWM, 4);
  PWMC_DisableChannel(PWM, 5);

  PWMC_ConfigureClocks(clkfreq, 0, VARIANT_MCK);
```

```
PWMC_ConfigureSyncChannel (PWM, PWM_SCM_SYNC0 | PWM_SCM_SYNC1 |
PWM_SCM_SYNC2 | PWM_SCM_SYNC3 | PWM_SCM_SYNC4 | PWM_SCM_SYNC5,
PWM_SCM_UPDM_MODE1, 0, 0);

 // Configuring channel 0
 PWMC_ConfigureChannelExt(PWM,0,
                  PWM_CMR_CPRE_CLKA,
                  PWM_CMR_CALG,
                  0,
                  PWM_CMR_CES,
                  PWM_CMR_DTE,
                  0,0);
 PWMC_SetPeriod(PWM, 0, cprd);
 PWMC_SetDutyCycle(PWM, 0, m1);

 // Configuring channel 1
 PWMC_ConfigureChannelExt(PWM,1,
                  PWM_CMR_CPRE_CLKA,
                  PWM_CMR_CALG,
                  0,
                  PWM_CMR_CES,
                  PWM_CMR_DTE,
                  0,0);
 PWMC_SetPeriod(PWM, 1, cprd);
 PWMC_SetDutyCycle(PWM, 1, m2);

 // Configuring channel 2
 PWMC_ConfigureChannelExt(PWM,2,
                  PWM_CMR_CPRE_CLKA,
                  PWM_CMR_CALG,
                  0,
                  PWM_CMR_CES,
                  PWM_CMR_DTE,
                  0,0);
 PWMC_SetPeriod(PWM, 2, cprd);
 PWMC_SetDutyCycle(PWM, 2, m3);

 // Configuring channel 3
 PWMC_ConfigureChannelExt(PWM,3,
                  PWM_CMR_CPRE_CLKA,
                  PWM_CMR_CALG,
                  0,
                  PWM_CMR_CES,
                  PWM_CMR_DTE,
                  0,0);
 PWMC_SetPeriod(PWM, 3, cprd);
 PWMC_SetDutyCycle(PWM, 3, m4);
```

```
// Configuring channel 4
 PWMC_ConfigureChannelExt(PWM,4,
                          PWM_CMR_CPRE_CLKA,
                          PWM_CMR_CALG,
                          0,
                          PWM_CMR_CES,
                          PWM_CMR_DTE,
                          0,0);
 PWMC_SetPeriod(PWM, 4, cprd);
 PWMC_SetDutyCycle(PWM, 4, m5);

 // Configuring channel 5
 PWMC_ConfigureChannelExt(PWM,5,
                          PWM_CMR_CPRE_CLKA,
                          PWM_CMR_CALG,
                          0,
                          PWM_CMR_CES,
                          PWM_CMR_DTE,
                          0,0);
 PWMC_SetPeriod(PWM, 5, cprd);
 PWMC_SetDutyCycle(PWM, 5, m6);

 PWMC_EnableChannel(PWM, 0);
 PWMC_EnableChannel(PWM, 1);
 PWMC_EnableChannel(PWM, 2);
 PWMC_EnableChannel(PWM, 3);
 PWMC_EnableChannel(PWM, 4);
 PWMC_EnableChannel(PWM, 5);
 NVIC_DisableIRQ(PWM_IRQn);
 NVIC_ClearPendingIRQ(PWM_IRQn);
 NVIC_SetPriority(PWM_IRQn, 0);
 NVIC_EnableIRQ(PWM_IRQn);
 PWMC_EnableIt(PWM, 0, PWM_IER2_WRDY);

}

void loop() {
}
*****************************************************************************
```

Short code description:

The main parameters are initially defined at the beginning of the code. Two parameters *carrierfreq* and *clkreq* are used to define the proper carrier frequency calculating the parameter *cprd*. This presents the maximum of the microcontroller clock which starts from zero and reaches this value. The centre-aligned carrier frequency is set at 3kHz in this case. Since there are three H-bridges, six carriers are provided with their modulating signals *m*1-*m*6, following the way explained in chapter 4.4.

In the next part of the code the function *lookuptable* defines six arrays *lookup*1-*lookup*6 which store the samples memorizing the modulating signals. The sample resolution of the modulating signals corresponds to the number of samples over one fundamental period with respect to the switching frequency. This is provided with a parameter named *ris*.

Entering the loop with *ris* steps and properly comparing the modulating signals with the carrier, the gate signals for all switches are provided. Considering that all modulating signals have a shift compared with the value of the modulation index, some limits in the code have to be put in order to distinguish the right position when one modulation signal intersects the carrier. When the modulating signal is out of the carrier range, the output is set 0 or 1 depending on its current position. This is provided using two *if* conditions within every microcontroller channel. In general, a comparison between the carrier and one modulating signals is done using the instruction PWM->PWM_CH_NUM[*x*].PWM_CDTYUPD, where *x* presents the number of the microcontroller channel.

It must be noted that for one H-bridge, the control signal for one switch of the inverter leg is given by the microcontroller while its counterpart is created directly on the PCB board using proper electronic components.

Another part of the code presents basic instructions for setting all channels, synchronizing them, defining all parameters of one PWM channel and some additional instructions that are required by the data sheet in order to properly use all channels.