Alma Mater Studiorum – Università di Bologna

DOTTORATO DI RICERCA IN

Ingegneria Elettronica, delle Telecomunicazioni e Tecnologie dell'Informazione

Ciclo XXVIII

Settore Concorsuale di afferenza: 09/E3 - ELETTRONICA

Settore Scientifico disciplinare: ING-INF/01 – ELETTRONICA

TITOLO TESI

GENERAL-PURPOSE DATA ACQUISITION CARDS BASED ON FPGAS AND HIGH SPEED SERIAL PROTOCOLS

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Esame finale anno 2016

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Introduction

In our fully connected society, where digital communications of any type are growing at very high rates in terms of bandwidths, data volumes, people to be reached, parameters like speed, flexibility and performance are very important requirements of electronic components devoted to data communication. Nowadays, fast configurable-logic devices like FPGAs, equipped with high speed dedicated ports are taking a growing role in these fields of application. In several circumstances, they are the preferred components due to their extreme flexibility that allows to reach faster the production phase reducing therefore the time to market, a crucial parameter for any commercial product. Sometimes the flexibility characterizing these devices is so advantageous that it allows to use the same hardware architecture in evolving applications. This happens for both the commercial products and the custom electronics developed for research purposes. As an example the current FPGA technology is improving so fast and has become so feature-rich that in the last years it has been adopted in many large high energy experiments like those operating at the LHC for Data Acquisition (DAQ) systems and it is used in many commercial measuring systems. Big steps have been done as well in the direction of lowering power consumption, giving the opportunity to use FPGA devices in several other applications not strictly related to custom application for particle physics intent. On the other hand, configurable devices, used in high-energy collision experiments, usually find their field of application in the front end readout infrastructure.

This thesis exhibits the result of my PhD Apprenticeship Program, during which I worked at the "Marposs S.p.a." firm, in the electronic research division, and at the Department of Physics and Astronomy of the Bologna University, in the INFN's electronics laboratories of the ATLAS group.

During the three years PhD period I worked on the development and realization of two electronic data acquisition boards designed to be applied in several contexts, which share the use of high performance FPGAs and high-speed serial communications. The thesis describes the successful application of high-speed configurable electronic devices to two different fields, firstly developed in the particle physics scenario, and then exported to the industrial measurement of mechanical pieces, fulfilling in this way the main goal of the PhD Apprenticeship Program.

The first part of this thesis is dedicated to the development of a smart electronic system designed for luminosity measurements in the A Toroidal LHC apparatuS (ATLAS) experiment, located at CERN Large Hadron Collider (LHC). The acquisition boards are based on FPGAs (Field Programmable Gate Array) and they were designed, firmware included, at the Department of Physics and Astronomy at Bologna University. The first chapter contains a description of LHC, the world largest particle accelerator, inside

which two beams, each one organized in bunches, are accelerated in opposite directions. In four regions along the accelerator, the two beams collide every 25 ns (40 MHz). The collision originates thousands of particles, producing tracks in the detectors. The largest part of the traces belongs to well known phenomena, whereas ATLAS experiment is dedicated to those rare events which are not studied in detail yet and might indicate the need of new physics to be explained. One of the most important parameter of a particle collider, as LHC, is a machine running parameter called luminosity. The second chapter describes in detail the meaning and the importance of this physical quantity and the different strategy used in ATLAS fot its determination. The third Chapter describes LUCID detector, that represents the main online and offline monitor for luminosity in ATLAS. This detector has undergone an important upgrade both for the sensors and for electronic equipment during my PhD, in order to cope with the expected increasing luminosity after the last LHC machine upgrade. The luminosity boost will determine an increased number of traces requiring higher data transmission and elaboration performances. In the fourth chapter, the new read-out system of the LUCID detector, called LUCROD (LUCid ReadOut Driver) board, is described. It is the central element of detector acquisition system upgrade; it is composed by several FPGAs managing data reception, digitalization and transmission of PMT signals via optical links. In the fifth chapter the board devoted to the luminosity measurement, called LUMAT (LUminosity and Trigger MoniToring), is presented. It is fundamental for the data elaboration system devoted to the determination of luminosity values, used by the ATLAS experiment, through different algorithms implemented in the board. The fourth and fifth chapters include: descriptions of projects I developed in VHDL code; detailed overview of components mapped on FPGAs, their functions and criteria of implementation for luminosity calculation algorithms. These chapters contain also a description on the whole system testing phase with both hardware and software instruments, and some plots of the results obtained during physics runs.

The second part of the thesis, starting from the sixth chapter, illustrates features and peculiarities of the Apprenticeship Programme at Marposs. Marposs is a worldwide leader in precision equipment for measurement and control in the production environment: it produces electronics workshop systems designed to perform dimensional, geometrical and surface checks on mechanical pieces and systems for monitoring machines and tools during working cycles.

The seventh chapter is dedicated to an overview of a physics principle called "shadow cast", which lies at the basis of the optical measurement system. I designed, produced and tested a customer board based on FPGA. The eighth chapter overviews on peculiar features of the electronic system I designed to interface the linear sensor and its own elaborator via a Gigabit Ethernet connection. The electrical features and VHDL projects that I developed are then described, emphasizing on hardware mapped components. Since the developed product is meant to define a standard in the automotive sector for high precision contactless measurements, most of the details of this work have been intentionally omitted to protect the Marposs intellectual property. Currently the

developed system is entering the beta-test phase where selected costumers can use it in advance before the final commercialization, foreseen for next year.

Chapter 1

The ATLAS Experiment at the LHC

1.1 LHC: The Large Hadron Collider

The Large Hardon Collider (LHC) [1] is the largest particle accelerator in the world and it has been built at CERN research center in Geneva. It is located beneath the border of France and Switzerland, in the underground tunnel used to host the former Large Electron-Positron (LEP) Collider. The tunnel has a circumference of 27 km and lies at about 100 m below the surface. The LHC was built in collaboration with over 10,000 scientists and engineers from over 100 countries, as well as hundreds of universities and laboratories [2]. It represents the most powerful particles accelerator in the world.

LHC is designed to accelerate two independent beams circulating into different directions and can work in two different modes of operation: as a proton-proton collider with a design center-of-mass energy of 14 TeV, as a lead ion collider, accelerating fully ionized lead atoms. In this later operating condition, beams have a design energy of 2.76 TeV/nucleon, yielding a center-of-mass energy of 1150 TeV.

The peak luminosity for p-p collisions has varied widely from the first runs in 2010 at $\sqrt{s}$=7 TeV, reaching a peak value of L_{peak} = 7,73 x 10^{33} cm^{-2} s^{-1} in the last runs in 2012. During the recent shut-down period, the machine has been updated, reaching now a luminosity peak of 3 x 10^{34} cm^{-2} s^{-1} for a center-of-mass energy of 13 TeV.

The underground structure of the LHC is shown in Figure 1.
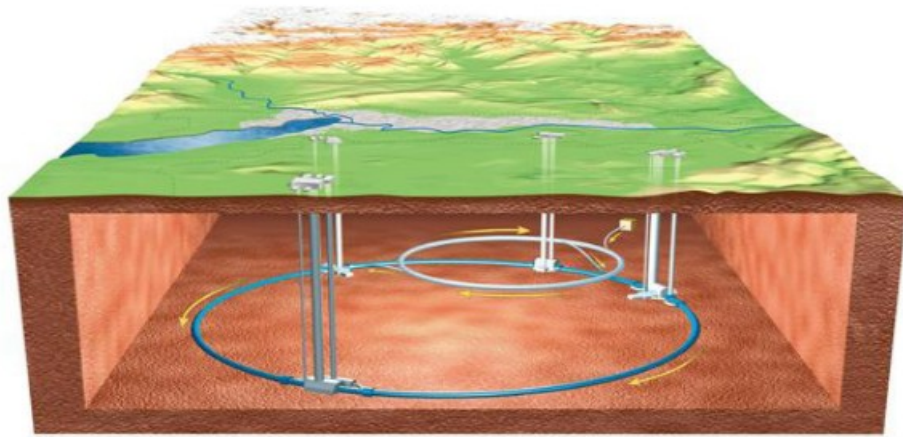
Figure 1: The underground structure of the LHC.

The Injection Chain

To reach the final design center-of-mass energy, the beams are accelerated through different stages performed using a chain of different accelerators (an overview of CERN accelerator layout is presented in Figure 2).
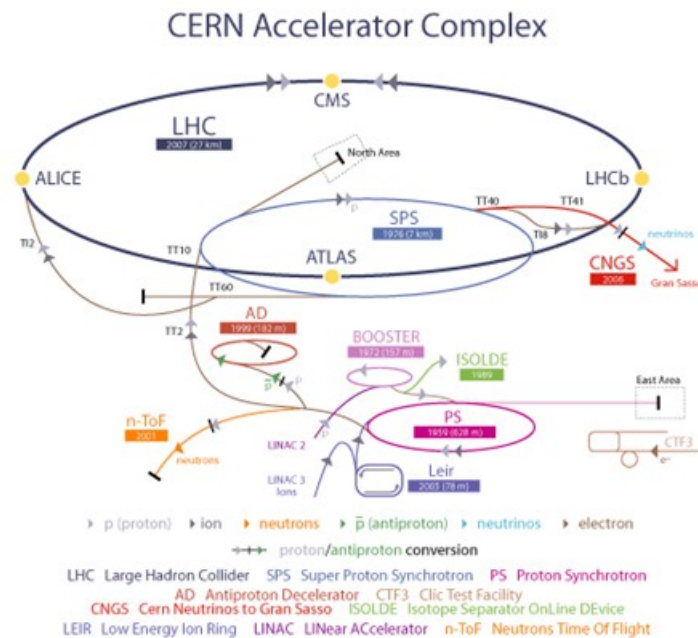
Figure 2: Overview of CERN acclerator layout.

The different chain stages schematically described in Figure 3 LHC are:

- **Linac2:** It is a linear accelerator used as starting point for protons and ions. It injects beams of 50 MeV in the following accelerator with a rate of 1 Hz. The

proton source is a bottle of hydrogen gas at one end of Linac2. The hydrogen passes through an electric field to strip off its electrons, leaving only protons to enter in the accelerator. The proton beams are pulsed from the hydrogen bottle impulses from 20 µs to 150 µs depending on the number of required protons. The pulses are repeated until enough protons are produced.

- **Proton Synchrotron Booster (PSB):** It speeds up the beams coming from Linac2 to an energy of 1.4 GeV. The accelerator is composed of four superimposed rings. In each ring, protons are collected in well defined packets or "bunches". They are them focused and sent through a magnet deflector into a single line to be injectied into the next accelerating element.

- **Proton Synchrotron (PS):** It is a key component in CERN accelerator complex. It usually accelerates either protons delivered by the Proton Synchrotron Booster or heavy ions from the Low Energy Ion Ring (LEIR). The PS has a circumference of 628 metres and hosts 277 conventional electromagnets, including 100 dipoles, to bend the beams round the ring. PS accelerates protons up to an energy of 25 GeV. It has been set to separate the bunches by 25 ns, providing a bunch collision rate of 40 MHz.

- **Super Proton Synchrotron (SPS):** It is the second-largest machine in CERN accelerator complex. Measuring nearly seven kilometres in circumference, it takes particles from the Proton Synchrotron and accelerates them to provide beams for the Large Hadron Collide. It has 1317 conventional electromagnets, including 744 dipoles to bend the beams round the ring. SPS is used as final injector for protons and heavy ions to LHC bringing the energy from 28 GeV to 450 GeV.

After the pre-acceleration stage the two beams are injected in the LHC ring at 450 GeV.

Protons are them accelerated up to the design energy according the different periods of data taking.
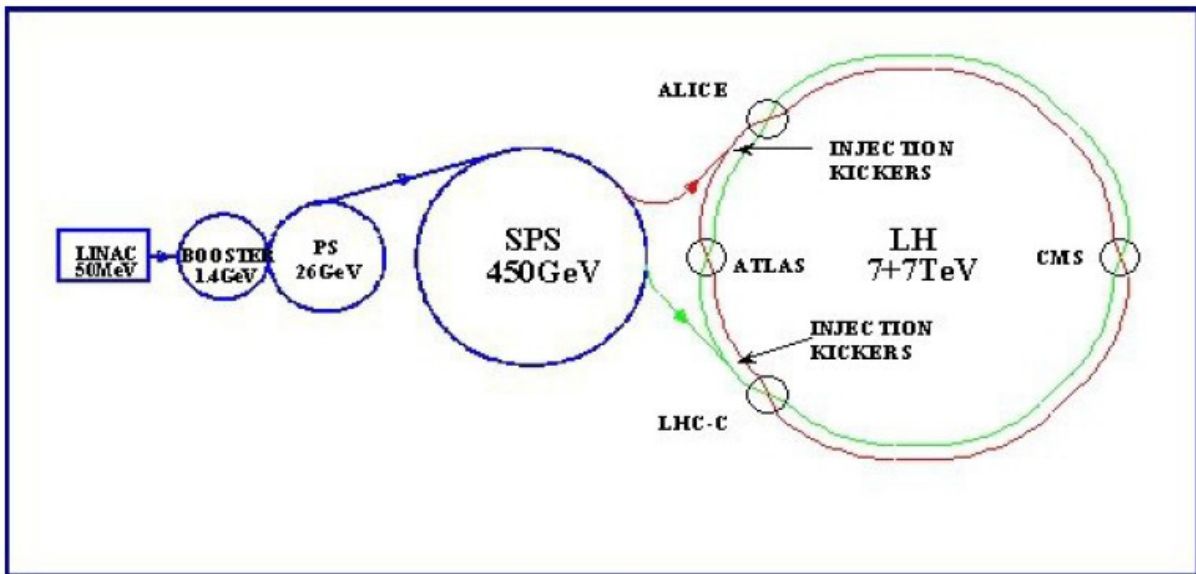
Figure 3: Different injection chain stages for LHC.

LHC sheds light on an energy region almost unexplored yet. Most of the design parameters are therefore close to the technical limits.
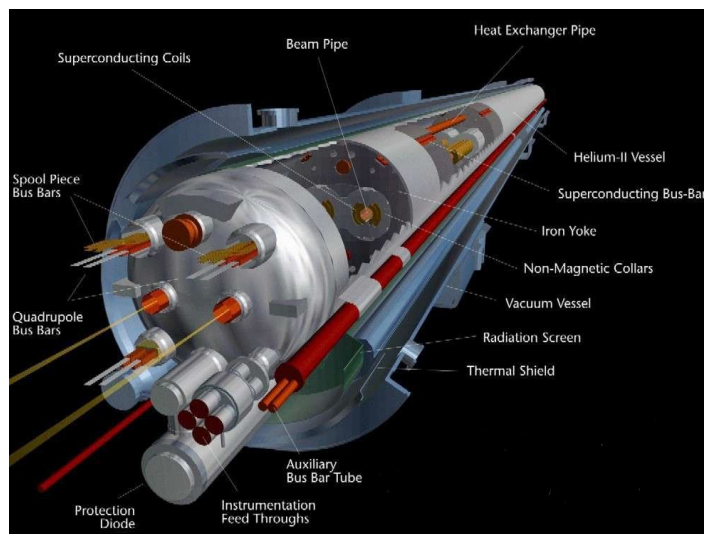
Figure 4: The key element of LHC accelerator: the 1232 dipoles bend the beam around the 27 km of circumference.

The two beams circulate into two separate ultrahigh vacuum chambers at a pressure of 10^{-10} Torr. The beams are labelled 1 and 2, where the former circulates clockwise and the latter in the opposite direction.

To curve the beam trajectories and keep them inside the accelerator, 1232 superconducting dipole magnets are displaced along the track. Pictorial view of the

magnets is visible in Figure 4. They are based on the Nb-Ti superconductor, working at a current of 11.85 kA and a temperature of 1.9 K, maintained by a liquid-helium refrigerating system, generating a magnetic field of up to 8.4 T. Other 392 superconducting quadrupole magnets producing a field of 6.8 T are necessary to focalize the beams.

The most important parameters of LHC in 2015 data taking are reported in Table 1.

LHC parameters	
Maximum collision energy	7 TeV
Injection energy	450 GeV
Dipole field 7 TeV	8.33 T
Internal coil diameter	56 mm
Peak luminosity	$10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$
Mean current	0.584 A
Bunch separation	24.95 ns, 7.5 m
Number of particles per bunch	$1.67 \cdot 10^{11}$
Crossing angle	300 µrad
Life time of beam	10 h
Energy lost per revolution (for proton)	7 keV
Total power radiated by the beam	3.7 kW

Table 1: Main parameters of LHC during 2015 data taking.

Beam Structure

The two beams circulating in the accelerator are not continuous but they are structured in 3564 evenly spaced bunch slots, separated in time by 25 ns each. An identification number (ID) is assigned to every slot (filled or empty). When two bunch slots with the same ID are filled in the two different beams, they can collide at special interaction points along the LHC tunnel. This is referred to as a bunch crossing (BC) and every event can be associated with a Bunch Crossing ID (BCID) for timing purposes.

Depending on the operational status of LHC, different filling schemes are foreseen. At the designed luminosity each beam will contain 2808 filled bunches. The bunches will be

gathered in trains of 80, (72 filled and 8 empty), separated by 30 empty bunches. Each bunch will contain $1{,}15 \times 10^{11}$ protons per bunch at the start of nominal fill and will be 7.55 cm long. The same bunch structure is used for heavy ion data taking.

Assuming a total proton-proton cross section of $10^{-25}\,\text{cm}^{-2}$ [3], there will be 10^9 events per second (or about 25 per BC). Elastic and anelastic collisions prevent the proton flows to circulate in the beam pipe in phase with the original bunches. A side effect of these collisions is that the beam luminosity degrades over time. The decay is exponential with an expected time constant $t = 14.9$ h, taking all loss mechanisms into account. Usually the beam can circulate for hours before a refill is needed. Measuring the luminosity is the task of various luminosity monitor detectors (see chapter 2).

1.1.2 LHC Experiments

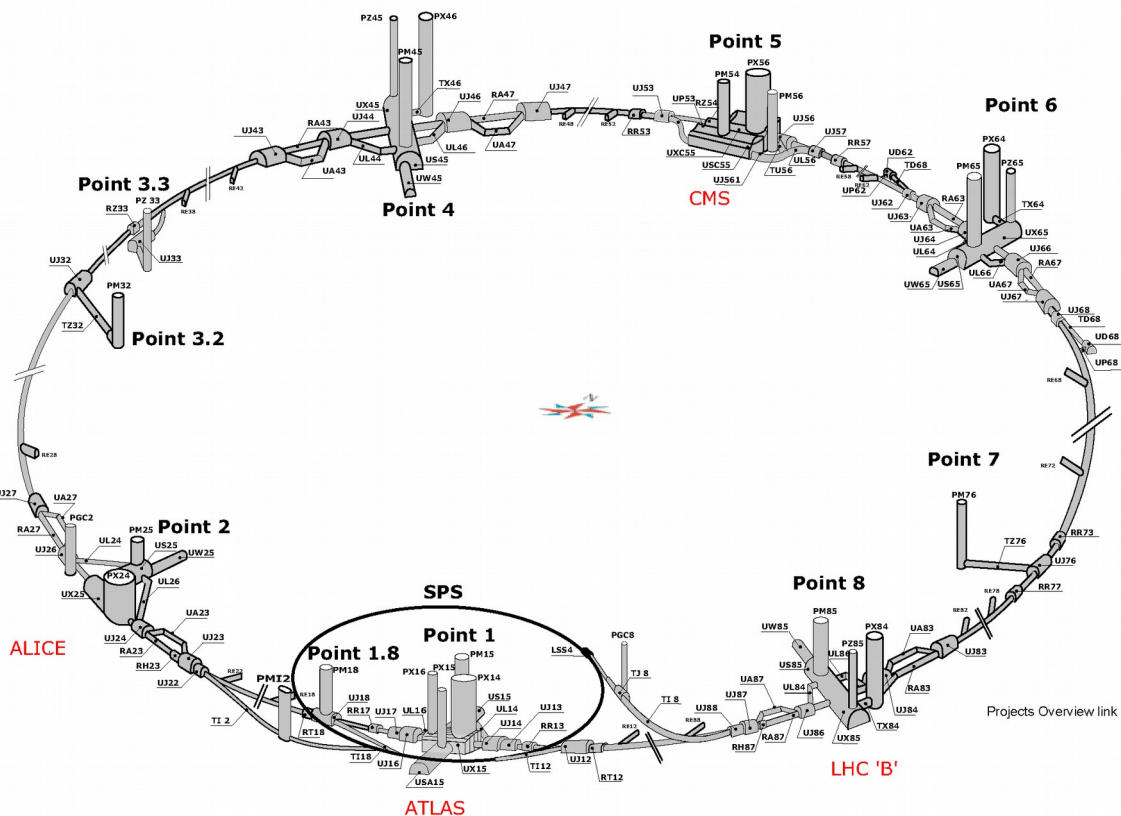Four experiments are installed along the LHC tunnel, see Figure 5 for a schematic view.

Figure 5: Interaction points at LHC in each of which the different experiments are installed.

- **A Toroidal LHC ApparatuS (ATLAS):** it is a multi-purpose detector which works at high luminosity. It has been designed to discover the Higgs boson as well as signatures of new phenomena in particle physics.

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- **Compact Muon Solenoid (CMS):** it is another multi-purpose detector designed to work at high luminosity with the same intents of ATLAS, but implemented with different and complementary technologies.

- **LHCb:** is the most specific experiment, it performs accurate measurements in the flavour physics of the B-mesons, for example CP violation. Since the production and the decay vertices of B-mesons are difficult to reconstruct when there is more than one interaction per bunch crossing, LHCb works at a luminosity lower than the one designed for ATLAS and CMS, using proton beams less focused near the interaction point.

- **A Large Ion Collider Experiment (ALICE):** it is built mainly to study a condensed status of the matter, called quark-gluon plasma, by detecting particles that are produced in heavy ion collisions. Due to the high nucleus-nucleus cross section, the higher track density per collision, ALICE can work up to luminosities $L = 10^{27}$ cm^{-2} s^{-1}.

Other two experiments are installed along the tunnel:

- **LHCf:** it measures γ and Π spectra in the very forward region at luminosity of $L = 10^{29}$ cm^{-2} s^{-1}. The aim is the calibration of Monte Carlo generators in cosmic rays studies. This detector was installed in 2009 and worked during the data taking at 900 GeV. It will be reinstalled once the design center of mass energy will be reached.

- **Total Cross Section, Elastic Scattering and Diffraction Dissociation at the LHC (TOTEM):** it is designed to measure the total pp cross section at a luminosity of $L = 10^{29}$ cm^{-2} s^{-1}. It is installed along the beam pipe near CMS.

1.1.3 LHC Schedule

The Large Hadron Collider has started its second three-years run (RUN 2). Cool down of the vast machine has finished and LHC started again to run after a long technical stop weeded to prepare the machine for running with superior energy.

In Figure 6 the schedule, more or less detailed, to 2035 is shown.
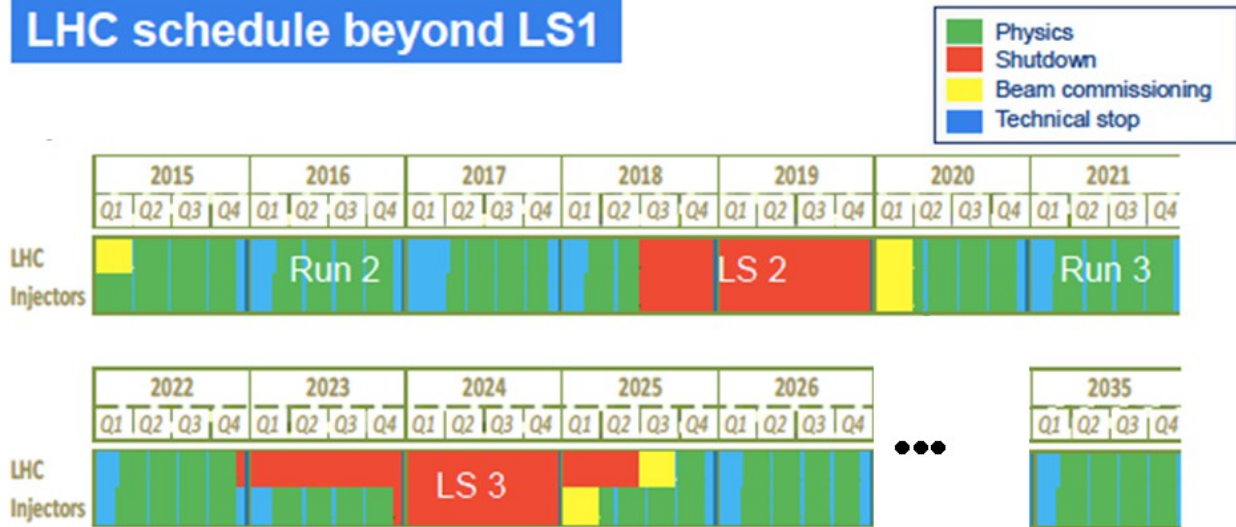
Figure 6: Schedule for LHC from 2015 to 2035.

The accelerator chain, that supplies the LHC particle beams, was restarted. During the shut down period finished at the beginning of 2015, LHC and all the CERN accelerator complex had a major programme of maintenance and upgrading. Before to collide beams again, a long and careful testing has been done to check all functions of the machine.

The aim of new data taking is to run the physics programme at 13 TeV in these years (from the beginning of 2015). The discovery of a Higgs boson is just the beginning of LHC journey. The increased energy opens the door to a whole new potential discovery, allowing further studies on the Higgs boson and potentially addressing unsolved mysteries such the dark matter.

1.2 The ATLAS Experiment

The ATLAS experiment is one of two general-purpose and a multi-purpose particle detectors, for physics studies, installed at the interaction point 1 of LHC, around 100 m underground. It probes a wide range of physics, from the search for the Higgs boson (discovery made public officially on 4 July 2012) to extra dimensions and dark matter particles. Although it has the same scientific goals as the CMS experiment, it uses different technical solutions and different magnet-system design.

The relative positions of the ATLAS experiment at Point 1 as well as its coordinates are shown in Figure 7.
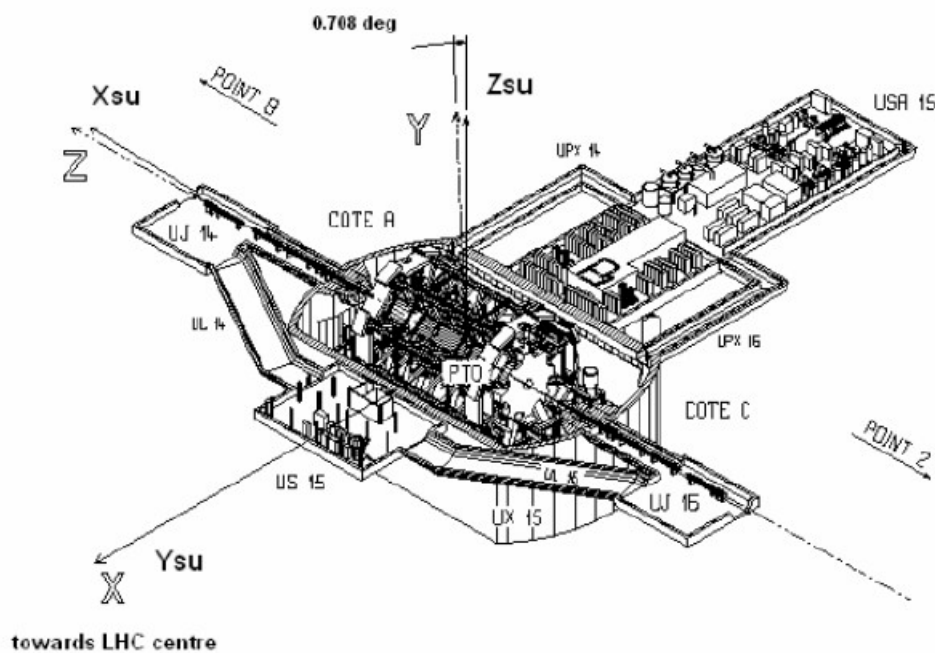
Figure 7: Schema of underground facility where ATLAS is installed. The ATLAS coordinates are shown as well.

The origin of the ATLAS coordinate system is defined as the nominal interaction point. The beam direction defines the z-axis and the x-y plane, transverse to the beam direction. The positive x-axis is defined as pointing from the interaction point to the center of the LHC ring. The positive y-axis is defined as pointing upwards. The A-side (C-side) of the detector is defined as the side with positive (negative) z. ATLAS is nominally forward-backward symmetric with respect to the interaction point [4].

ATLAS covers the full 2 π angle around the beam axis, in the polar ø coordinate, and an almost complete π coverage in the angle transverse to the beam axis.

The detector is cylindrically symmetric, with a total length of 42 m and a diameter of 22 m [4]. With its 7000-tonnes, the ATLAS detector is the largest volume particle detector ever constructed. The detector is organized in a central barrel and two end-caps that close either ends. In the barrel, the active detector elements form cylindrical layers around the beam pipe while in the end-caps they are organized in wheel layers.

The cross sections of the most interesting new-physics phenomena are very small, if compared to the total cross section of the p-p interactions, for both the 8 TeV center of mass energy reached in the 2012 and the 13 TeV of 2015. A high luminosity is essential to produce copiously of these rare events and high precision detectors are necessary to measure the properties of particles produced at each interaction.

The ATLAS detector is composed by a large number of sub-detectors, and electronic components, that can be regrouped as:

- a Magnetic System composed of a central super-conducting magnet and three toroidal magnets to bend the particle trajectories;
- an Inner Detector that provides the particle tracking close to the interaction point;
- a Calorimeter System divided in electromagnetic and hadron calorimeter;
- a Muon System that tracks muons in the outer layers of the detector;
- Luminosity Monitors that provide online luminosity;
- a Triggering System that selects bunch crossing containing interesting events and stores only data with interesting physics signature;
- a System for data acquisition and distributed analysis.

1.2.1 The ATLAS Detector

The human eye is the most essential component of our visual perception ability and thus the main input for the analysis process that takes place in the human brain. It perceives light, photons, in a limited range of frequencies, making it fairly inapt at detecting fundamental particles in all possible energy ranges [5] [6] [7]. Detectors transform particles into visible inputs and to do this they exploit the different ways in which particles interact with matter.

An overview of the ATLAS detector is shown in Figure 8.
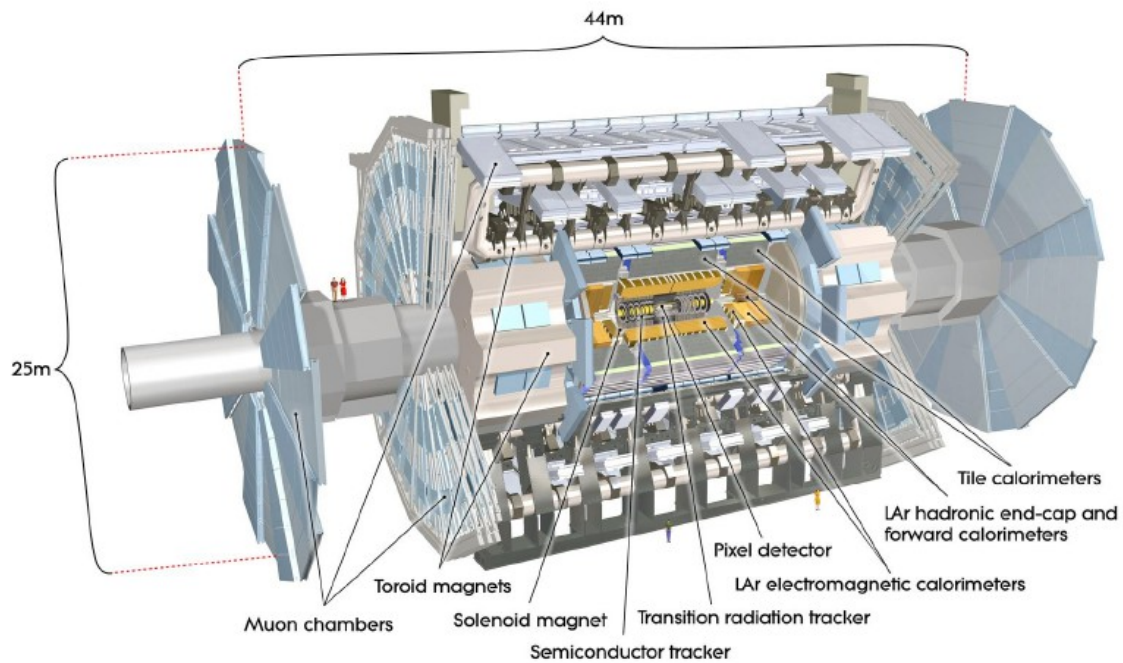
Figure 8: The ATLAS detector schema.

ATLAS is composed of several subsystems, each designed for specific purposes.

Particles produced in collisions normally travel in straight lines, but in presence of a magnetic field their paths become curved. Electromagnets installed around the beam pipe generate magnetic fields to exploit this effect. Physicists can calculate the momentum of a particle – a clue to its identity – from the curvature of its path: particles with high momentum travel in almost straight lines, whereas those with very low momentum move forward in tight spirals inside the detector.

In Figure 9 scheme of the Barrel Toroids and of the End-Cap Toroid magnets (in red) installed in ATLAS are shown; the blue cylinder is the calorimeter.
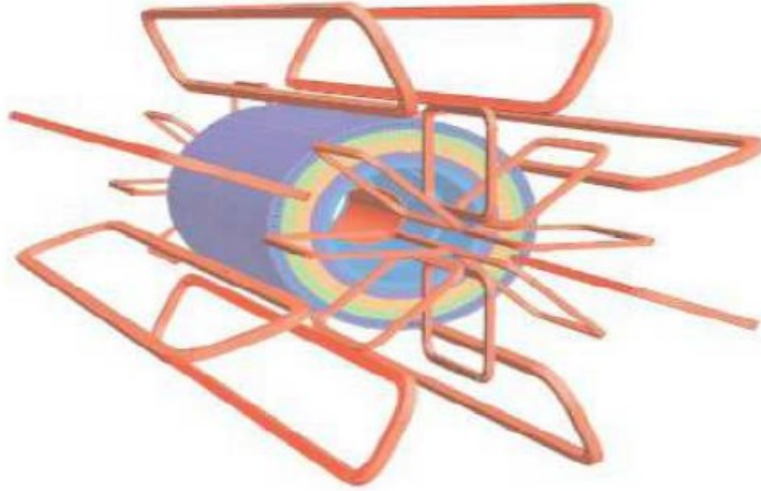
Figure 9: Scheme of the Barrel Toroids and End-Cap Toroid magnets (red). The blue cylinder is the calorimeter.

The magnetic system of the ATLAS experiment is characterized by three different magnetic field systems, each of which is composed by superconductive magnets kept at a temperature of 4.8 K:

- **Central Solenoid (CS)**: is designed to provide a 2T strong magnetic field in the central tracking volume. It is a superconducting solenoid based on a thin-walled construction for minimum thickness to decrease particle scattering effects. In order to reduce material build-up and enhance particle transparency, the solenoid shares its cryostat with the liquid argon calorimeter (LAr). The superconducting solenoid installed around the Inner Detector cavity is 5.3 m long with a bore of 2.4 m, has a thickness of 45 millimeters, a weight of almost six tonnes and operates at a current of 7,600 A. The energy absorption of the solenoid is minimized through the use of a very thin coil and the sharing of the same vacuum vessel with the LAr calorimeter, in order not to alter significantly the performance of the calorimeters themselves. In Figure 10 a picture of the CS is shown.

Figure 10: Scheme of the Central Solenoid (CS) in ATLAS.

- **Barrel Toroid (BT)**: it consists of 8 rectangular coils arranged in cylindrical configuration, super-conducting and air-core, with an open structure to minimize the multiple scattering effects. The total length is 25 m, with an inner diameter of 9.4 m and an outer diameter of 20.1 m. It is installed just outside the calorimeters. It provides a magnetic field of 1.5 T. In Figure 11 the BT of ATLAS is shown.
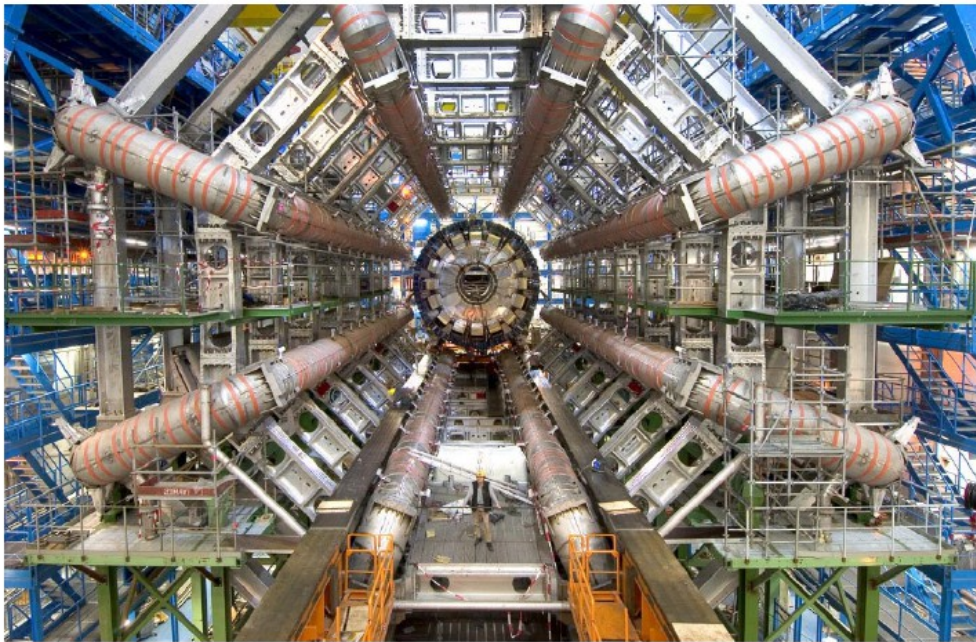
Figure 11: Scheme of the Barrel Toroid (BT) in ATLAS.

- **End-Cap Toroid (ECT)**: it is composed by 8 rectangular coils arranged in a single cylindrical vessel. The total lenght is 5 m, with an outer diameter of 10.7 m and an inner one of 1.65 m. The vessel is mounted at the ends of ATLAS in order to close the magnetic field lines produced by the Barrel Toroid. With this configuration the magnetic field is orthogonal to the beam axis and has a value of 2 T.

Inner Detector (ID)

The Inner Detector (ID) is the inner part of ATLAS, near the beam pipe and closest to the interaction point. It contributes to particle identification and gives essential information to identify rapidly decaying particles. In Figure 12 a section of the ID is shown: it is constituted mainly of successive layers of subdetectors placed in a cylindical configuration around the beam pipe.
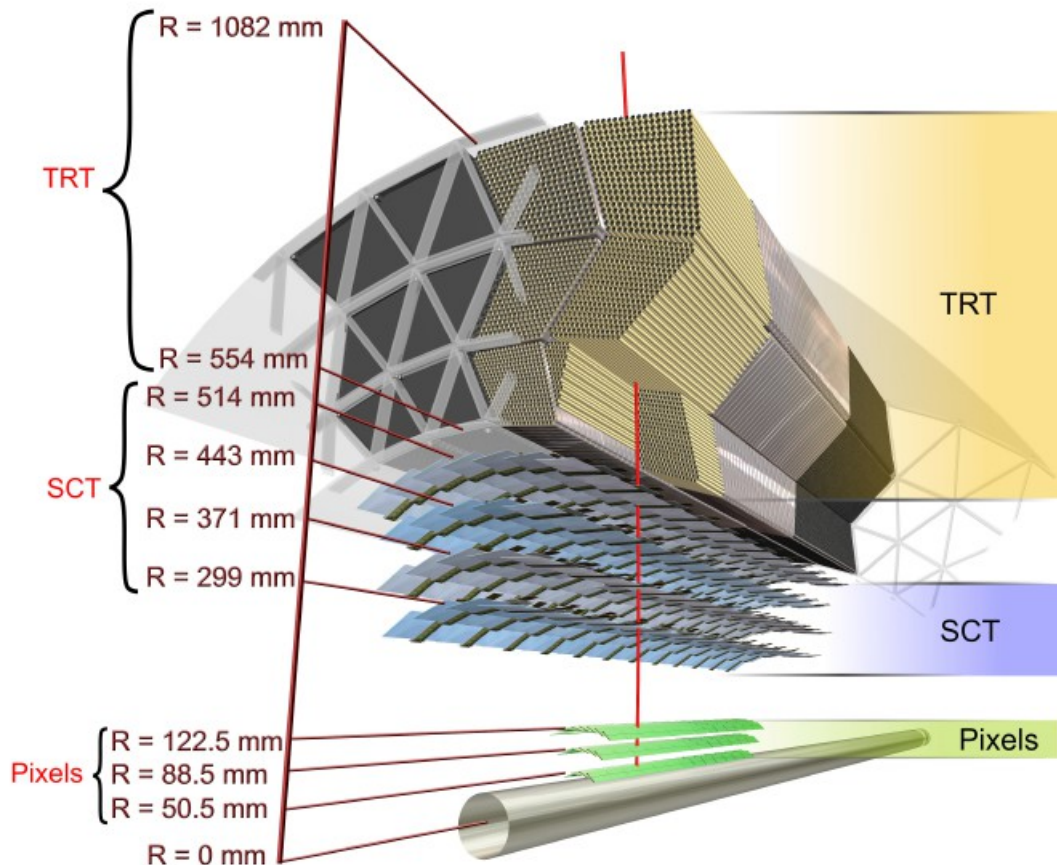
Figure 12: Section of the Inner Detector (ID) in ATLAS.

Approximately 1000 particles are expected to be produced every 25 ns for a luminosity of about L = 10^{34} cm^{-2} s^{-1} within the ID volume [7], creating a very large track density in the detector.

The charge and direction of each track is measured, as well as the impact parameter, defined as the distance of closest approach to the beamline. The ID is also responsible for reconstructing both primary and secondary vertices, which are needed to identify B-mesons and converted photons. The ID is immersed in a 2T magnetic field. By measuring the curvature of the tracks, the momentum of the particles can be determined.

The layout of the ID is presented in Figure 13.
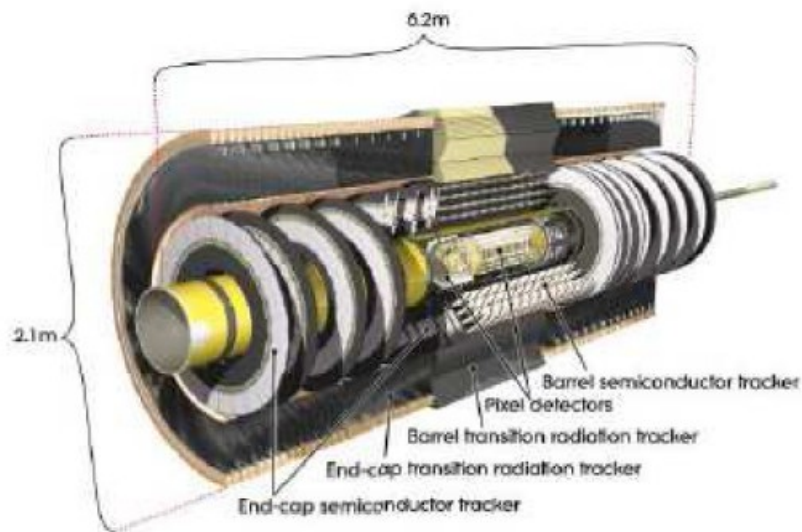
Figure 13: Layout of Inner Detector (ID) in ATLAS.

Its structure is divided in three parts. A barrel section of ± 80 cm extending along the beam axis, closed at the extremities by two identical end-caps. In the barrel region high precision detector layers are arranged in concentrical cylinders around the beam axis while the end-cap detectors are mounted on disks perpendicular to the z-axis.

Given the very large track density expected at LHC the momentum and vertex resolution targets impose high-precision measurements to be achieved with fine-granularity detectors (usually semiconductor pixel).

The ATLAS Pixel Detector shown in Figure 14 provides a very high granularity, high precision set of measurements as close to the interaction point as possible. The system provides three precision measurements over the full acceptance, and mostly determines the impact parameter resolution and the ability of the Inner Detector to find short lived particles such as B-Hadrons. The system consists of three barrels at average radii of ~ 5 cm, 9 cm, and 12 cm (1456 modules), and three disks on each side, between radii of 9 and 15 cm (288 modules). Each module is 62.4 mm long and 21.4 mm wide, with 46080 pixel elements read out by 16 chips, each serving an array of 18 by 160 pixel. The 80 million pixel cover an area of 1.7 m^2. The readout chips must withstand over 300 kGy of ionising radiation and over $5x10^{14}$ neutrons per cm^2 over ten years of operation. The modules are overlapped on the support structure to give hermetic coverage. The

thickness of each layer is expected to be about 2.5% of a radiation length at normal incidence. Typically three pixel layers are crossed by each track.

The pixel detector can be installed independently of the other components of the ID.
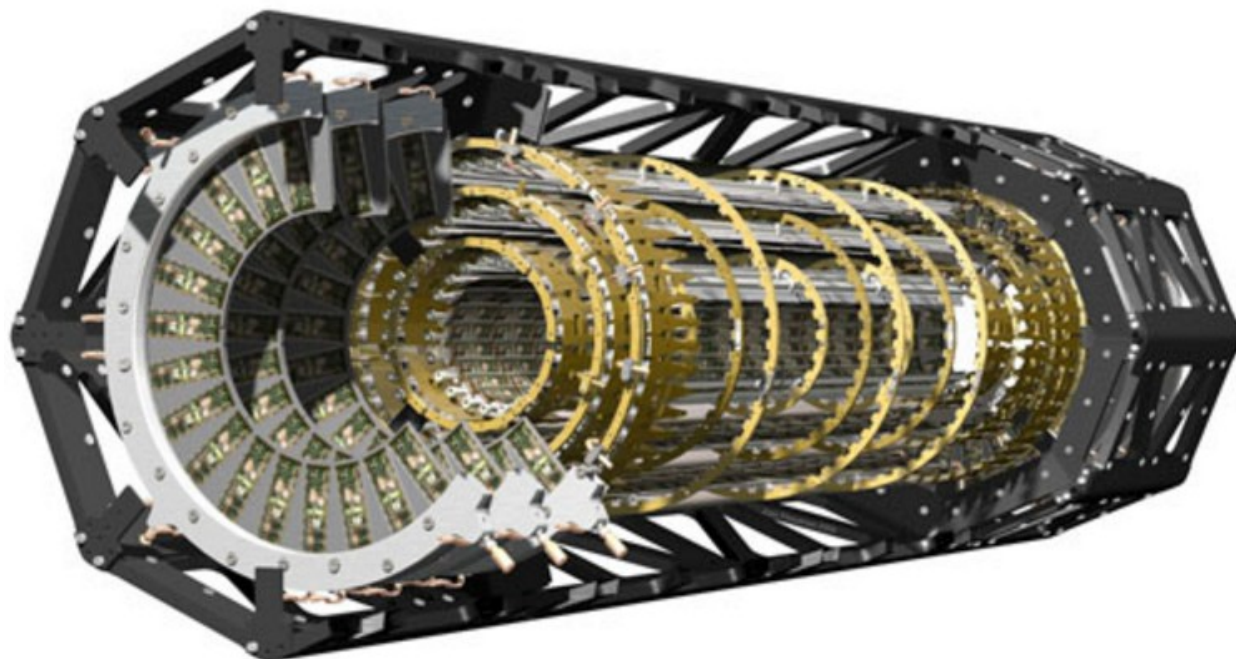
Figure 14: Pixel in the Inner Detector section.

During the long shutdown between RUN 1 and RUN 2, an additional layer, called "b-layer" was inserted between the old Pixel Detector and the beam pipe.

In the intermediate radial range a SemiConductor Tracker (SCT) provides precise reconstruction of tracks as well as measurements of momentum, impact parameter and vertex positions, providing also good pattern recognition thanks to its high granularity.

The barrel SCT shown in Figure 15 uses eight layers of silicon microstrips detectors to provide precision points in the coordinates. Each silicon detector is 6.36×6.60 cm^2 with 768 readout strips of 80 µm pitch. Each module consists of four single-sided p-on-n silicon detectors. On each side of the module, two detectors are wire-bounded together to form 12.8 cm long strips. The readout is accomplished by discriminator and a front-end amplifier, followed by a binary pipeline to store the hits above threshold, waiting for the Level 1 trigger decision (see section 1.2.3).
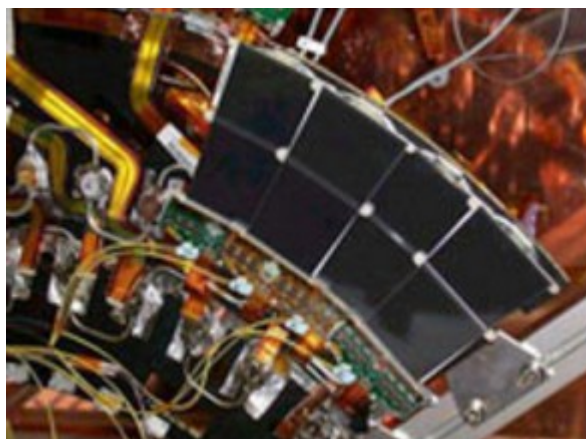
Figure 15: Photo of the barrel SCT.

The end-cap modules are very similarly assembled, but they use tapered strips, with one set aligned radially. The detector contains 61 m^2 of silicon detectors, read out by 6.2 million channels. Its high granularity is important for the pattern recognition.

The outermost component of the ID is the Transition Radiation Traker (TRT), is a combination of a straw detectors and a transition radiation detector, that can operate at the very high rates required by LHC. Electron identification is provided using xenon gas that becomes ionized when a charged particle passes through. This technique is intrinsically radiation hard and allows a large number of measurements, it is not as precise as those for the other two detectors, but it was necessary to reduce the cost of covering a larger volume and to have transition radiation detection capability.

Each straw is 4 mm in diameter for a maximum straw lenght of 144 cm in the barrel. The tubes are arranged in to 36 layers. A gold-plated tungsten wire in the middle of each tube collects the signal. Each layer is interspersed with a radiator to stimulate transition radiation from ultrarelativistic particles. The spatial resolution is about 200 µm.[4]

The barrel contains about 50000 straws, each divided in two at the center, with read-out at each end; the end-caps contain 320000 radial straws, with the read-out at the outer radius. The total number of electronic channels is 420000, providing drift-time measurements, with a spatial resolution of 170 µm per straw, and two independent thresholds, to discriminate between tracking hits and transition-radiation hits.

The Calorimetric System

Calorimeters in ATLAS are situated outside the solenoidal magnet that surrounds the Inner Detector. Their purpose is to measure the energy from particles by absorbing them. They detect also missing transverse energy by summing up all the measured energy deposits. A signal output in voltage or current proportional to the released energy is read out by front-end electronics and processed to recontruct the initial energy value.

The ATLAS calorimetric system is composed by two different calorimeters which cover different ranges of pseudo-rapidity. A pictorial view of the whole system is shown in Figure 16.
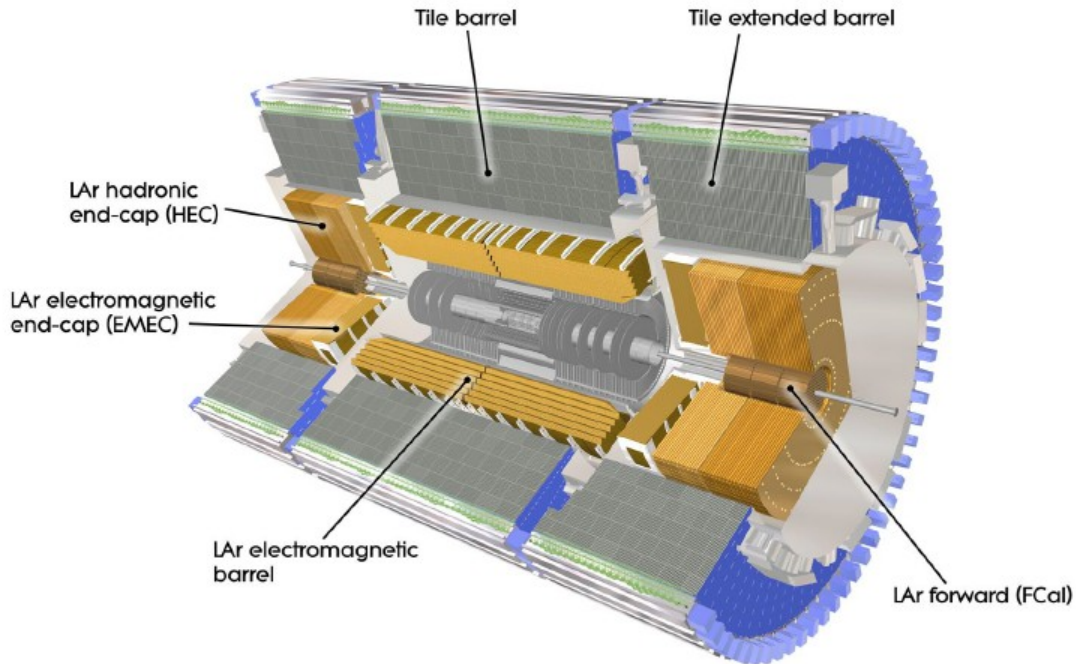
Figure 16: Calorimetric System in ATLAS.

The **Electromagnetic Calorimeter** (EM Cal) is divided into a barrel part and two end-cap components. It is specifically designed to absorb and measure the energy from particles interacting electromagnetically, which include charged particles and photons.

The EM calorimeter is composed by liquid argon as active material, with accordion-shaped kapton electrodes, and lead absorber plates as passive medium. When a particle traverses the liquid argon gap, it creates charge by ionization. Then the signal is collected on readout electrodes. The barrel component covers a region in pseudo-rapidity $|\eta| <$ 1.475 while the two end-cap elements cover the range $1.375 < |\eta| < 3.2$. The total thickness of the EM calorimeter is > 24 radiation lengths (X_0) in the barrel and > 26 X_0 in the end caps. The EM calorimeter must be able to identify electrons and photons with energy between 5 GeV and 5 TeV.

The energy measurements do not have to deviate from linearity more than 0.5% to provide good resolution [4].

The **Hadronic Calorimeters** are designed to absorb and measure energy from particles that pass through the EM calorimeter, but do interact via the strong force; these particles are primarily hadrons.

They are divided in different sections, the Hadronic Tile Calorimeter (HTC) is made of iron and plastic scintillator in the barrel region ($|\eta| < 1.7$), the second region is covered by a liquid argon calorimeter in the end-caps (Hadronic End-Caps Calorimeter, HEC) for $1.5 < |\eta| < 3.2$ coverage, and two frontal Forward Calorimeters (FCAL), very close to the beam pipe, made of liquid argon, iron and tungsten, that covers the region of $3,2 < |\eta| < 5$. The thicknesses of the calorimeters have to be tuned in order to contain all the hadronic shower, to minimize the punch-through into the muon system and to provide a good resolution for high energy jets. The energy resolutions of the different sections have been measured in beam tests using pions and electrons.

Muon chambers

The muon spectrometer in ATLAS has been designed to be efficient in the muon detection and, in principle, should be able to measure the momentum without the help of the Inner Detector.

The muon chamber system, with its outer diameter of 22 m, represents the extreme outer layer of the ATLAS detector. The muon system is instrumented with separate trigger and high-precision tracking chambers for excellent momentum resolution.

The tracking chambers are Monitor Drift Tube (MDTs) chambers and Chatode Strip chambers (CSCs). The MDT chambers provide precise muon tracking over most of the pseudo-rapidity range. The tubes are made of aluminum and have a diameter of 30 mm. The resolution on the drift distance is about 80 μm [8]. The CSCs cover the pseudo-rapidity range of $1 < |\eta| < 2.7$. They are multi-wire proportional chambers with cathodes segmented into strips. The spatial resolution on the coordinate is about 60 μm [8].

The trigger system covers the range $|\eta| < 2.4$. Resistive Plate Chambers (RPCs) are used in the barrel and Thin Gap Chambers (TGCs) in the end-caps. The trigger chambers (RPC and TGC) have a three-fold purpose:

- measurements of the second coordinate in the direction orthogonal to that measured by the precision chambers, with a resolution 5-10 mm.

- bunch-crossing identification, separating events with a time resolution better than 25 ns;

- trigger with well defined p_T threshold requiring a granularity of the order of 1 cm.

The structure of the Muon Spectrometer is shown in Figure 17.
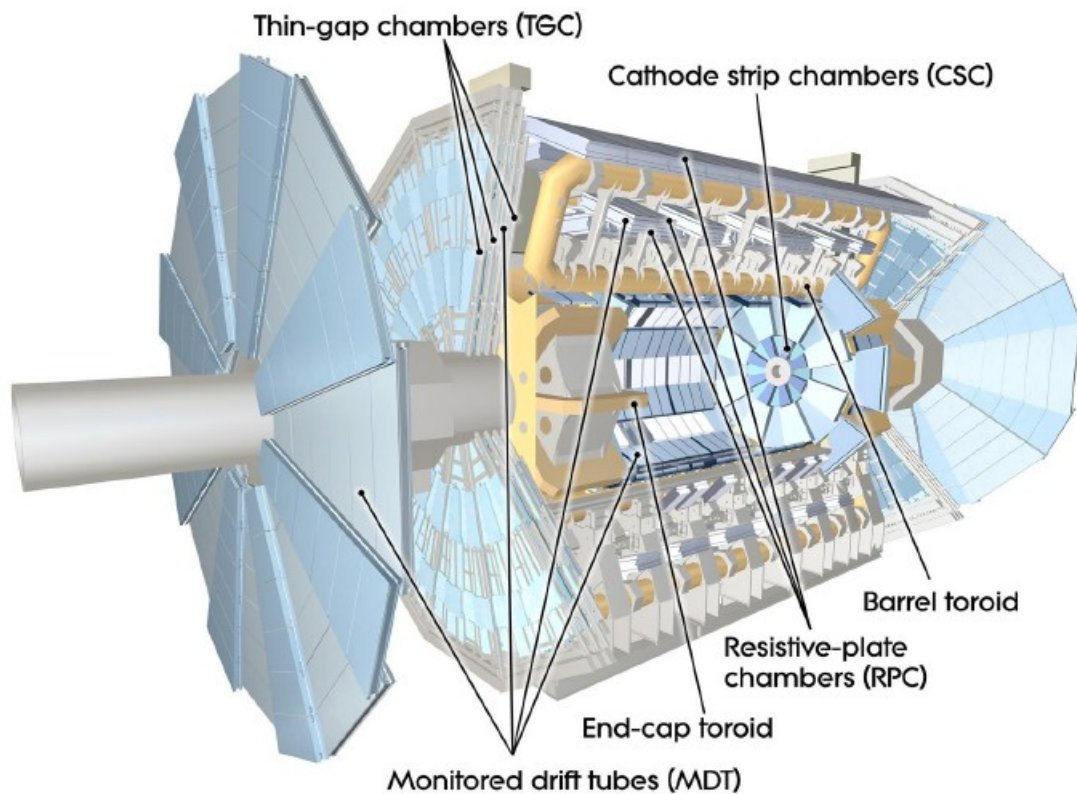
Figure 17: Scheme of the Muon Spectrometer in ATLAS.

Only in a small fraction of pp collisions, high pT events can be found for standard model processes, and an even smaller fraction of events is expected to correspond to new physics. Muons at high pT or isolated ones are more common in interesting events than in background and provide thus an important signature used by the trigger system.

1.2.2 ATLAS Physics

LHC will give the chance to study a wide range of physical phenomena, to measure with high precision the parameters of Standard Model and to seek out details of the Higgs boson or new physics (e.g. supersymmetric events or dark matter).

To study the most fundamental laws of nature it is necessary to achieve very high energies [1] [9].

In the Standard Model, the mass is generated by the so-called Higgs mechanism, regulated by the interaction of each particle with Higgs field that provides at the same time the well-known Higgs boson.

The Higgs boson, elementary particle and massive scalar, was observed in the previous data taking period (RUN 1) but the Standard Model mechanisms have to be still understood. The Higgs boson has a fundamental role in the model: it explains why the

photon has no mass, while the W and Z bosons are very heavy. In electroweak theory, the Higgs generates the masses of the leptons (electron, muon, and tau) and quarks.

The predictions of the standard model agree very well with the results of all experiments performed so far, sometimes with a remarkable accuracy, but there are hints that it cannot be a complete theory. It is unclear if it can describe correctly the processes happening at very high energies and it does not explain some important features of our universe: most notably the matter-antimatter asymmetry and the dark matter/dark energy already observed in cosmological studies.

Supersymmetry is an extension of the Standard Model aimed to fill some gaps. Supersymmetry is the physical theory that correlates bosonic particles (that have integer spin) with the fermionic particles (which have half-integer spin). According to supersymmetry every fermion has a bosonic superpartner and every boson has a fermionic superpartner. These new particles would solve a major problem with the Standard Model – fixing the mass of the Higgs boson. If the theory is correct, supersymmetric particles should appear in collisions at the LHC.

Finally, in many theories scientists predict the lighest supersymmetric particle to be stable and electrically neutral and to interact weakly with the particles of the Standard Model. These are exactly the characteristics required for dark matter. The Standard Model alone does not provide an explanation for dark matter. Supersymmetry is a framework that builds upon the Standard Model strong foundation to create a more comprehensive picture of our world.

1.2.3 ATLAS Trigger and Data Acquisition System

ATLAS would produce about 1 Petabyte/second of raw data if all the pp collisions were recorded, at design luminosity. However, most of the data come from common, well-known processes that after the first studies, are not of interest for the experiment.. The purpose of a trigger system is to select just the rare, interesting events while rejecting everything else.

The ATLAS experiment relies on a complex and highly distributed Trigger and Data Acquisition (TDAQ) system to gather and select particle collision data at unprecedented energy and rates. The TDAQ is composed of three levels, which reduces the event rate from the design bunch-crossing rate of 40 MHz to an average event recording rate of about 200 Hz.

The acquisition system is the most composite subsystem present in the ATLAS experiment. Its issue includes all features associated with the transport of the physical data recorded by the various detectors in the experiment, the final storage of selected data, all devices needed to operate with the suitable custom electronics.

Infrastructure acquisition is made of several elements:

- electronics on the detector: so-called the "front-end electronics". Each detector has a specific electronics, mainly analogic, that read out the raw data from the detector and send them to the next stage,

- transport electronics: the detector is placed 100 meters in the underground, in a highly radioactive environment where there are strong magnetic fields; high flows of particles damage the performance of the more sensitive electronics. For these reasons the majority of the detectors have a custom board electronics to digitalize the signals directly for the cavern and to sent them far from the radioactive area;

- electronics data collection: the main task of these elements is to collect the raw data, to digitize analog signals, to build data packets for each subdetector and to prepare them for the final phase of the acquisition. Such electronics are located in a protected environment at controlled temperature;

- electronics processing in situ: the data organized in packets and arranged for sub-detector are subsequently selected through different levels of trigger and assembled to construct an ATLAS event. At this stage the data travel mainly over optic fiber and / or ethernet network-gigabit. Finally they leave the ATLAS experiment towards large calculus centers;

- off-site electronics processing: the first data collection center (called Tier) is at CERN, the second in order of importance is in Bologna (Tier 1 of CNAF). These are large processing systems consisting of thousands of CPU server and organized in rack in which users can connect to perform the data analysis.

The Trigger System

The Trigger System [10] selects events containing interesting interactions among the huge amount of data produced at each interaction.

At the design luminosity there are about 25 interactions per bunch crossing leading to an interaction rate of about 10^9 Hz. The online triggering system must be able to select interesting physics signatures reducing the acquisition rate to approximately 200 Hz, the upper limit for the data storage. The goal is achieved with different trigger levels which successively refine the selection process: Level 1 Trigger (LVL1), Level 2 Trigger (LVL2) and Level 3 Trigger (LVL3) also called Event Filter. The differents levels of the trigger system is shown in Figure 18.
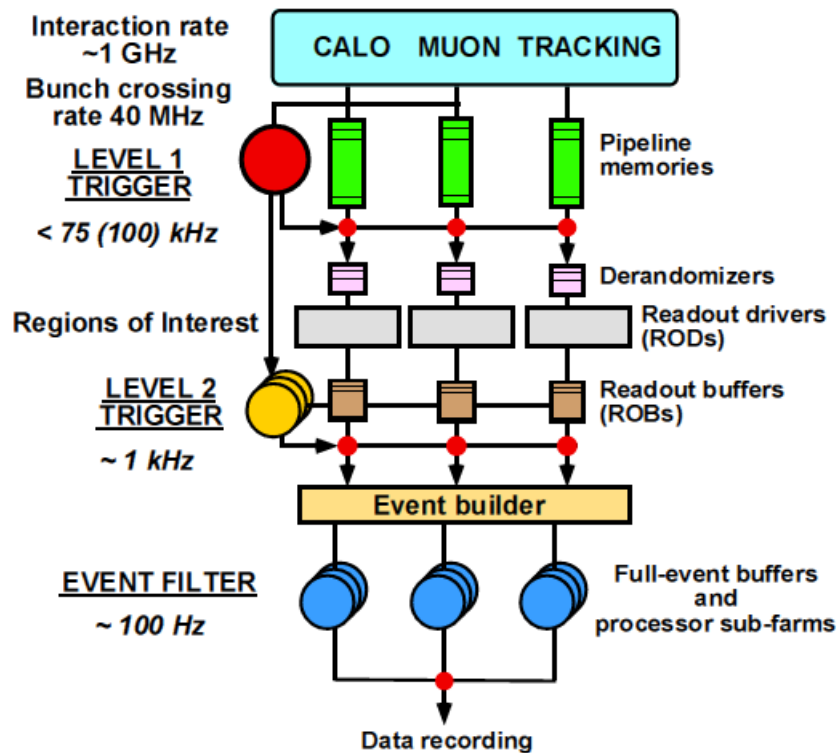
Figure 18: Scheme of the ATLAS trigger system.

- **Level 1 Trigger:** all the subdetectors in ATLAS work at the full LHC bunch-crossing rate. The trigger electronics has to provide a decision on the data temporarily buffered in pipe line at the rate of 40 MHz. The LVL1 trigger uses reduced granularity data from only a subset of detectors, muon chambers and calorimeters, plus prescaled contributions from luminosity monitors. Then the LVL1 decides if one event can be stored or it has to be rejected. The time to form and to distribute the trigger decision, called latency, is 2 μs and the maximum rate is limited to 100 kHz by the capabilities of the LVL2 trigger input band width. During the LVL1 processing, the data from all subdetectors are held in pipeline memories in the front-end electronics. The LVL1 trigger must identify unambiguously the bunch crossing containing the interaction of interest introducing negligible dead-time.

- **Level 2 Trigger**: the LVL2 trigger reduces the accepted rate from 100 kHz to 1 kHz, with a latency ranging from 1 ms to 10 ms depending on the event. Events passing the LVL1 trigger are held in so-called Read Out Buffers (ROBs) until the LVL2 trigger takes the decision to either discard the event or accept it. After an event is accepted, the full data are sent to the Event Filter processor via the Event Builder. In order to reduce the data transfer bandwidth from the ROBs to the LVL2 trigger processors, the LVL2 algorithms work on subsets of the detector data called Region of Interest (RoI) and defined in the LVL1.

- **Event Filter** the Event Filter trigger uses the full event data together with the latest available calibration and alignment constants to make the final selection of events for permanent storage. At LVL3 a complete event reconstruction is possible, with a total latency of about 1 s. The Event Filter must achieve a data storage of 10-100 MB/s by reducing both the event rate and the event size.

LV2 trigger and Event Filter are called together High Level Trigger (HLT).

Data Acquisition System

The Data Acquisition System (DAQ) is the framework in which the Trigger System operates. It receives and buffers the data from the detector-specific read out, called Read Out Drivers (RODs), at the Level 1 trigger rate, and trasmits the data to the Level 2 trigger if requested. If an event fulfills the Level 2 selection criteria, the DAQ is responsible for building the event and moving it to the Event Filter. Finally, the DAQ forwards the final selected events to mass storage.

In addition to moving data down to the trigger selection chain, the DAQ provides an interface for configuration, control and monitoring of all the ATLAS detectors during data taking. Supervision of the detector hardware, such as gas system and power supply voltages, is handled by a separate framework called the Detector Control System (DCS). Moreover, the DCS is responsible for alert and handling archiving.

System of Synchronization

The syncronization of the LHC experiments to the collisions is necessary to guarantee the quality of recorded data. LHC provides beam related timing signals to the experiments via optical fibers that are several kilometers long. The phase of the clock signals can drift (e.g due to temperature fluctuation, causing front-end electronics to sample at non optimal working points). The syncronization at ATLAS is provided by the Beam Precision Monitor for Timing Purposes (BPTX) system [11]. The BPTX stations are composed by of electrostatic button pick-up detectors, located at 175 m from the IP along the beam pipe on both side of ATLAS. BPTX are used to monitor the phase between collisions and clock with high accuracy in order to guarantee a stable phase relationship for optimal signal sampling in the subdetectors front-end electronics. In principle, the bunch structure of the beams as well as the number of particles in each bunch can be measured by the BPTX system, but the accuracy on the number of particles is not high enough for a reliable luminosity measurement.

Measurements of Bunch Currents

Two complementary systems are used in ATLAS to evaluate the bunch currents with the precision required by luminosity measurements: the Fast Bunch-Current Transformers (FBCT) and the Direct-Current Current Transformers (DCCT).

The Fast Bunch-Current Transformers (FBCT) are AC-coupled, high-bandwidth devices which use gated electronics to perform continuous measurements of individual bunch charges for each beam. The Direct-Current Current Transformers (DCCT) measure the total circulating intensity in each of the two beams irrespective of their underlying time structure. The DCCT have intrinsically better accuracy, but require averaging over tens of seconds to achieve the needed precision.

The relative bunch-to-bunch currents are based on the FBCT measurements.

The absolute scale of the bunch intensities is determined by rescaling the total circulating charge measured by the FBCT to more accurate DCCT measurements.

Chapter 2

Luminosity Measurements

2.1 Introduction

The most important parameter when hadron-hadron collisions are studied is the energy available at the center of mass that can be transformed into particles. The LHC accelerator has been designed to reach a center-of-mass energy of 14 TeV (the highest world record) in order to have access to final states containing possibly the Higgs boson and other exotic particles. Since these processes are very rare and happen once every 10^9 interactions, it is important to produce as many events as possible at each collision. The machine parameter that is related to the yield of interaction is called instantaneous luminosity. The interaction rate is given by the product of the luminosity and the total inelastic cross section.

In any accelerator luminosity depends on several parameters, among which there are: number of particles circulating in the beam, the beam size in the plane transverse to the beam direction and the overlap of the two beams at the interaction point. For two perfectly head-on beams, the higher is the number of particles and the smaller is the beam size, the higher is the luminosity and hence the collision rate.

When the packets in the beam colide, the particles interact with eletromagnetic fields due to the presence of other protons. This process is well-known as beam-beam effect and it reduce the beam lifetime. During standard operation the packets remain inside the accelerator for about 10-20 hour. Beam-beam effect and interactions of protons with residual particles in the beam pipe degrade the number of particles in the packets, causing a continuous decrease of instantaneous luminosity.

The definitions of luminosity and its importance will be presented in section 2.2. The different methods used at LHC to measure the luminosity will be presented in section 2.3, with particular attention to ATLAS strategy.

2.2 Luminosity Overview

2.2.1 Istantaneous Luminosity

The instantaneous luminosity $\mathscr{L}$ in a collider is defined as the ratio between the total interaction rate R of any processand its cross section σ. It is expressed in $cm^{-2}\,s^{-1}$ and it is independent of the process itself.

$$\mathscr{L} = \frac{R}{\sigma}$$

The instantaneous luminosity can be inferred from the machine parameters: if the two beams are made of identical bunches, they are Gaussian in shape and overlap perfectly without crossing angle, the luminosity is given by:

$$\mathscr{L} = f_r n_b \frac{N_1 N_2}{4 \Pi \sigma_x \sigma_y}$$

Detectors in ATLAS are generally able to determine only relative luminosity, mean an observable quantity related to the absolute luminosity through a calibration constant.

$$\mathscr{L} = \frac{\mu \, n_b f_r}{\sigma_{inel}} = \frac{(\frac{\mu^{vis}}{\varepsilon}) n_b f_r}{\sigma_{inel}} = \frac{\mu^{vis} n_b f_r}{\varepsilon \, \sigma_{inel}} = \frac{\mu^{vis} n_b f_r}{\sigma_{vis}}$$

where:

μ is the average number of interactions per bunch crossing (BC),

σ_{inel} the inelastic cross section,

ε is the efficiency of the luminosity algorithm (including the acceptance) for a certain detector,

$\mu^{vis} = \mu\,\varepsilon$ is the average number of interaction per BC as recorded by a particular luminosity monitor;

$\sigma_{vis} = \sigma\,\varepsilon$ is the detector calibration constant, referred to as the detector normalization.

The absolute luminosity at LHC can be expressed in terms of colliding beam parameters in the transverse plane and, for zero crossing angle, it is given by the equation (1):

$$\mathscr{L} = n_b f_r I_1 I_2 \int \rho_1(x,y)\rho_2(x,y)\,dx\,dy \quad (1)$$

where:

I is the intensity of beam,

$\rho_1(x,y)$ $\rho_2(x,y)$ are the particle densities in the transverse plane of the beam 1 and 2 respectively,

dx, dy infinite elements of surface.

At LHC, due to beam losses of various origin, the instantaneous luminosity decreases by 1% every ten minutes according to the power law:

$$\mathscr{L} = \mathscr{L}_0 \, e^{-\frac{t}{\tau}}$$

where $\tau \simeq 14$ h.

2.2.2 Integrated Luminosity

The integrated luminosity L is obtained by integrating the instantaneous luminosity over a certain time interval (t) and is expressed in cm^{-2}:

$$L = \int_0^t \mathscr{L}(t')\,dt'$$

The integrated luminosity L provided information on the total number of events collected in a certain period of time.

2.2.3 Delivered and Recorded Luminosities

The luminosity defined previously is called "machine luminosity" or the "delivered luminosity": it is the luminosity provided by the accelerator at a given interaction point. Since the physical analyses deal with recorded events, it is necessary to introduce another type of luminosity to take into account the data taking efficiency in order to keep

the proportionality between the events recorded and the physical cross section.

The recorded luminosity is defined summing up the delivered instantaneous luminosity for all periods of time when the apparatus was ready to take data. Obviously when the detector is switched off or not taking data the recorded luminosity is zero. During data taking there might be very short moments where the detector is not able to record data. These periods, called collectively dead-time, are usually originated by what happens just after a trigger is given or when the data taking system is momentarily busy. The recorded luminosity is therefore defined with respect to a trigger chain and refers to the fraction of time when the trigger chain was active. Bunch-crossing that occurs during dead-time are for example excluded.

The delivered luminosity is evaluated before any trigger decision and therefore does not test the dead-time of the data acquisition system. Since all datasets used for analysis are exposed to dead-time, the final goal is to find the recorded luminosity corresponding to the data-set in question: the delivered luminosity needs to be transformed into recorded luminosity by correcting for dead-time.

precise luminosity measurement are needed not only for offline physical analysis, but also online both for beam and data quality monitoring. Reliable real-time measurements of the instantaneous luminosity are a key ingredient for a successful data taking: these measurements provided to the LHC control room can be used to maximize the luminosity delivered at ATLAS.

2.2.4 Luminosity Monitor for Beam Tuning

In order to reach record luminosities, the LHC accelerator group has to accurately tune thousand of superconducting magnets making a single proton to circle billions of times before it collides with another proton. The accurate knowledge of the particle trajectories in the accelerator is ensured by several sensors along the accelerator and by what is recorded at the interaction points. To reach the optimal conditions for the highest delivered luminosity mini scans are used to center the beams on each other in the transverse plane at the beginning of each fill in LHC. Mini lumi-scans consist in active closed-orbit bumps around the IP, which modify the position of both beams by $\pm 1\sigma$ in opposite directions, either horizontally or vertically. A closed orbit bump is a local distortion of the beam orbit that is implemented using pairs of steering dipoles located on either side of the affected region. In this particular case, these bumps are tuned to translate either beam parallel to itself at the IP, in either horizontal or vertical direction. The relative positions of the two beams are then adjusted, in each plane, to achieve the optimum transverse overlap, as inferred from the measurement of the interaction rate.

2.3 Luminosity Measurements in ATLAS

Luminosity measurements in ATLAS are designed to reach three goals.

- Providing final absolute integrated luminosity values for offline analyses, for the full data sample as well as for selected periods. In addition, measurements of the average luminosity over small time intervals, called Luminosity Block (LB), and for individual bunch crossings are required. The LB is defined as a time interval in which the luminosity can be considered constant. As a consequence, the LB must be smaller than the decay time of the beam. The luminosity must be provided for each LB. In physics analyses, in fact, data are used only if some quality criteria, provided LB by LB, are satisfied. To avoid discarting too many data, short LB are needed. Typical values of LB lenght are thus of the order of 1-2 minutes, to balance all the aspects mentioned before. Each LB is identify by a number which uniquely tags it within a run.

- Providing fast online luminosity monitoring, as required for efficient beam steering: machine optimization, as for example beam centering through miniscans, as well as efficient use of the trigger. The fraction of recorded data, called prescale, in fact, can be changed according to the beam degradation in order to optimize at each time the data acquisition band width. A statistical precision of about 5% per few seconds and systematic uncertainties below 20% are desirable for the online luminosity.

- Fast checking of running conditions such as monitoring the structure of the beam and beam-related backgrounds.

Since there is no single experimental technique which can full fill all the above requirements, a number of complementary measurements and detectors have to be considered: parallel measurements of absolute and relative luminosity are mandatory.

2.3.1 ATLAS Running Conditions in RUN 2

During the RUN-1 period between 2009 and early 2013, the ATLAS trigger system [7] operated very successfully. It selected events with high efficiency at centre-of-mass energies up to 8 TeV, for a wide range of physics processes including minimum-bias physics and TeV-scale particle searches.

During the foreseen RUN-2 period between 2015 and 2018, the LHC running conditions,

as summarised in *Table* 2 are expected to be challenging to the trigger system: trigger rates for a RUN-1-like system are expected to increase by a factor of roughly five in total.

A factor of two increase is expected from the increase of energy up to 13 TeV, and will be even higher for high p_T jets. The additional factor of 2.5 originates from the peak-luminosity increase from 8×10^{33} cm^{-2} s^{-1} to $1\text{-}2 \times 10^{34}$ cm^{-2} s^{-1}.

In addition, the peak number of interactions per bunch crossing (μ_{peak}), which was 40 during the 2012 run, is expected to go up to 50.

The bunch spacing reduction from 50 ns to 25 ns, while helping to control the increase in in-time pile-up (interactions occurring in the same bunch-crossing as the collision of interest), will nevertheless increase both the out-of-time pile-up (interactions occurring in bunch-crossings just before and after the collision of interest) and beam-induced fake trigger rates, particularly in the muon system.

-	Year	Energy	$L_{peak}(10^{33}cm^{-2}s^{-1})$	peak $< \mu >_{LB}$	$L_{int}(fb^{-1})$
Run I	2010	$7\,TeV$	0.2	~ 5	0.047
-	2011	$7\,TeV$	3.6	~ 20	5.5
-	2012	$8\,TeV$	7.7	~ 40	22.7
Run II	2015	$13\,TeV$	5	~ 35	4.2
-	2016-2018	$13\,TeV$	exp. ~ 20	exp ~ 60	exp. ~ 100

Table 2: The luminosity acquired by the ATLAS experiment during RUN 1 and the expected RUN 2 luminosity.

2.3.2 Relative Luminosity Measurements at ATLAS

As already mentioned, all ATLAS luminosity detectors can measure only a quality wich is proportional to the absolute luminosity, providing thus a "relative" luminosity measurements.

The luminosity monitors provide the measurements of the instantaneous luminosity at two different frequencies. First, the luminosity monitors evaluate the instantaneous luminosity at the frequency of about 1-2 Hz. These fast measurements are typically averaged over all bunch crossing in an LHC beam revolution (orbit). At least one of these measurements is communicated to the LHC for machine operations. Second, the instantaneous luminosity is provided LB per LB on bunch-by-bunch basis. These measurements are used for physics analysis.

In summary, the luminosity is provided both integrated over all the bunch crossings and on bunch-by-bunch basis.

The response of a luminosity monitor ought to be linear over a large dynamic range, fast,

stable in time and stable under different beam conditions. The main goal of these luminosity monitor detectors is to reach a stability better than 2%.

The detectors that can provide luminosity measurements (at different accuracy levels and pseudorapidities) during RUN 2 are:

- Beam Condition Monitor BCM: it covers $|\eta| \sim 4.2$ and provides precise information on the condition of the beams and is thus used to calculate both integrated and bunch-by-bunch luminosity.

- Luminosity Cherenkov Integrating Detector LUCID: it covers $5.6 < |\eta| < 5.9$ and it was designed to sustain a high event rate and high radiation doses. It can work at design luminosity, and can provide both LB integrated and bunch-by-bunch measurements.;

- Hadronic Forward Calorimeters FCAL: is made of rod shaple electrodes inserted inside a tungsten matrix. The FCAL provides electromagnetic as well as hadronic coverage in the very forward region $3.2 < |\eta| < 4.9$. It can provide only LB integrated luminosity.

- Eletromagnetic End-Cap Calorimeter EMEC: consists of two wheels located on either sides of the barrel. The outer wheel covers the region $1.375 < |\eta| < 2.5$ while the inner wheel covers the region $2.5 < |\eta| < 3.2$. It provides estimation of LB integrated luminosity.

- Tile Calorimeter TileCal: consist of alternating layers of plastic scintillator and iron. It is a sampling hadronic calorimeter covering the pseudorapidity region $-1.7 < |\eta| < 1.7$. It provides LB integrated luminosity indirectly, monitoring the current drawn by the sensors.

In left plot of Figure 19, the integrated luminosities during stable-beam runs in 2011/2012 are shown: the LHC delivered luminosity is compared with the overall recorded luminosity at ATLAS and with the final luminosity recovered in perfect functioning conditions of the detectors (labelled "Good for Physics"). The losses of the delivered luminosity (for any reason) is around 10%.

In right plot of Figure 19 different evaluations of the instantaneous luminosity during a single run is shown for three of the luminosity monitors used in 2010 before any fine tuning correction. The decrease of the beam quality is clearly visible.
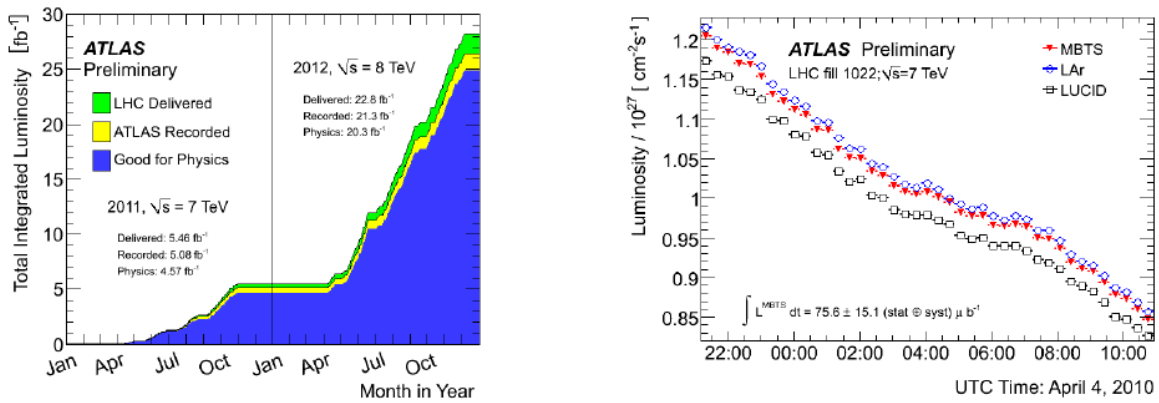
Figure 19: Integrated luminosity registered during runs in 2011/2012 and luminosity registered during the 2010 tests.

Relative luminosity must be calibrated through several methods, that exploit beam characteristics and known physics processes. The first and most used calibration technique is performed using beam conditions in a van der Meer scan [12].

At the LHC the method consists in moving the beams transversely with respect to each others while recording the counting rate by all the available luminosity monitors. Separation scan are performed in both vertical and horizontal directions. The position of maximum rate is thus found and the absolute luminosity is inferred from the measured beam overlap. This kind of calibration has an uncertainty that depends on beam parameter uncertainty (beam current in particular) and on the extrapolation to the higher luminosity regimes; thanking to the improvement an that method during RUN 1 data taking, the final uncertainty of 1,9% has been reached in 2015 [13]. Calibration through physics channels, in particular the W and Z bosons, yields an uncertainty that depends on the limited knowledge of the parton distribution functions (PDF) [14], a value that has improved over the run and is now $\sim$ 3%, depending on the process used. Finally, calibration through a dedicated detector (ALFA) [15] that measures the flux of protons scattered elastically should lower the uncertainty down to $\sim$ 2%.

Chapter 3

The LUCID Detector

3.1 Introduction

The main topic of this thesis is to study the electronic system of the main luminosity monitor in ATLAS called LUCID (Luminosity measurements Using Cherenkov Integrating Detector).

The measurement of luminosity is essential in any high-energy physics experiment for cross-section evaluation. In ATLAS, luminosity is measured on several levels and at different steps of the data-taking and data re-processing:

- online luminosity monitoring (performed by dedicated detectors), integrating signal over the short time-span $\Delta t = 2s$; only the fast hardware response of the electronics used by dedicated detectors can provide this measurement without significant delay;

- lumi-block by lumi-block luminosity, integrated over a period of time in which the instantaneous luminosity is estimated to vary by less than 1%; this process allows Δt to vary between 30 s and 10 min, with an average value of 60 s;

- offline luminosity, measured by reprocessing data in a more refined way; this measurement can be performed using a great number of detectors and algorithms, providing a redundant approach.

Since the start of data taking at the Large Hadron Collider, LUCID has been the only dedicated luminosity monitor in the ATLAS experiment [16] [12], although other detectors have been used to compute luminosity algorithms, as shown in chapter 2. The intrinsically fast response of the Cherenkov detectors and the dedicated readout electronics make it ideal to measure the number of interactions at each bunch crossing.

During the shutdown period between RUN 1 and RUN 2 (called long shutdown 1) a heavy upgrade of both detector and readout electronics have been necessary, to cope with

new LHC data taking conditions.

The solution to those problems was found by reducing the detector granularity and dimension. The reduced acceptance help LUCID to cape with the increased occupancy due to the higher center of mass energy and number of interaction per bunch crossing.

The original version of the detector ("old LUCID" [17]) is described in [ATLAS collaboration. JINST 3, S08003 (2008)] it took data providing luminosity values as main detector, in ATLAS during years 2009-2010 [18] and in combination with other detectors in years from 2011 to 2013.

In this chapter the "new LUCID" design will be presented with particular attention on the architecture of the sensors developed by the LUCID collaboration and especially on their read-out electronics based on Field Programmable Gate Array (FPGA).

3.2 Photo Multiplier Tubes

The Photo Multiplier Tubes (PMTs) are the sensitive part of the experiment and for this reason they take an important part in the R&D of the detector.

A photomultiplier is an instrument to measure and detect a light signal, in the visible or near ultraviolet range, converting it into electric current. Figure 20 shows the structure of PMT.
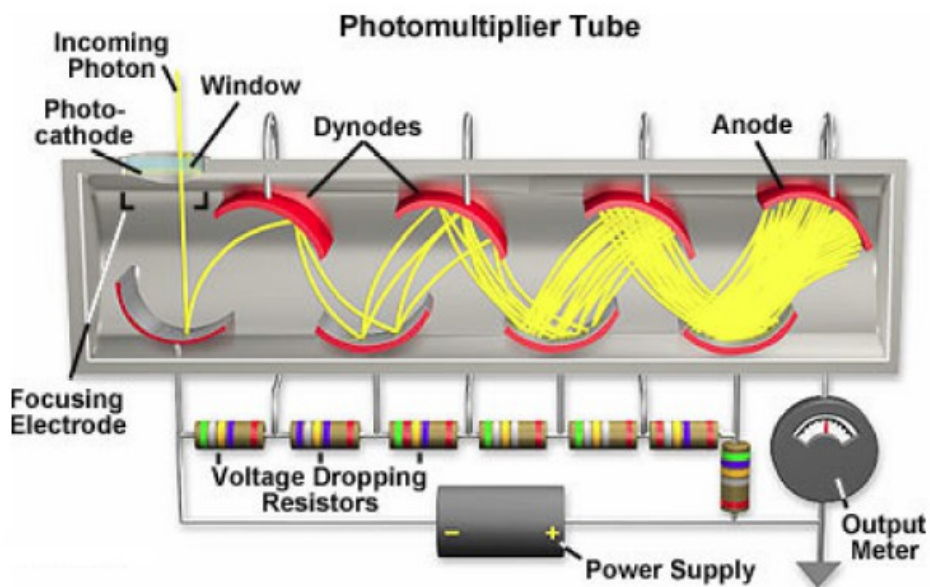

Figure 20: PMT structure

A PMT is constituted by a vacuum tube with an inlet window as much transparent as possible, a photocathode, a focussing electrode, a dynode chain in which a difference of potential is applied to collect and accelerate the electrons produced in the photocathode and an anode to collect current in output.

The operating principle of a photomultiplier is the photoelectric effect: the light incident on the photocathode produces electrons in quantity which is proportional to the incident light. The electrons are thus accelerated, by an the electric field, towards the first dynode, in which they are multiplied due to secondary emission. The procedure is repeated for a serie of dynodes and the final current is read out by the anode.

The most important components of PMT are thus:

- input window: since it is the first component encountered by incident photons, in order to make photons detected, it has to be transparent with respect to the wavelength of the photons. According on the material used for the window, PMTs will have different lowest detectable wavelength. More over the chosen material has to be radiation hard if the PMTs have to operate in a strongly radioactive area as for example at LHC;

- photocathode is the plate on which the incident photons convert into electrons (called photo-electrons) due to the photoelectric effect. The main parameter to be optimized is the energy estraction that has to be small in order to make easy the extraction of electrons by photons. The spectral response of the photocathode is the spectral response of the PMT and contains the information of the lowest and highest wavelength that photocathode can detect;

- dynodes: in order to produce a detectable signal even in case of very few incident photons, the photoelectrons produced by the photocathode are accelerated through a chain of dynodes. At each stage the electrons are accelerated toward a dynode where, due to the acquired kinetic energy, they impinge and are able to extract 2-4 electrons that can be accelerated toward the next dynode. Several dynodes in sequence provide the multiplication chain needed to amplify the tiny signal of a single electron to a measurable electronic pulse. Normally a PMT uses 8 or 12 dynodes, arranged in a geometric configuration that permits to maximize the efficiency collection. The ratio between the number of electrons produced by the photocathode and the charge collected by the anode is called gain. The gain is related to the number of dynodes and to the voltage supply.

Two models of PMT have been used to replace the one installed in LUCID in RUN 1 (Hamamatsu R762), both of them with reduced window:

- Hamamatsu R760: window of 10 mm of diameter, ten dynodes, and a quartz

window of constant thickness of 1.2 mm, photocathode composed by bialcali.

- Hamamatsu R760 modified: as a previous one but modified by the constructors with one part of the active window aluminized in order to further reduce the effective area to a diameter of 7 mm (shown in Figure 21).

Figure 21: Image of the R760 PMT in its modified form, showing the circular aluminium layer that reduces the active area and, thus, the acceptance.

3.3 Upgrade for RUN 2

The LUCID Detector worked in a strongly radioactive environment for a long time (more than three years). These working conditions caused ageing and performance degradation of LUCID. The main reasons of degradation are:

- Absorbed radiation: dosimeters, placed close to LUCID detector, measured a radiation dose at LUCID position in agreement with expectations. The main source of radiation is gamma rays and, secondary, neutrons. A long exposure to radiation produced an internal radioactivity that caused an increase of the PMT anodic current even in absence of external light, called dark current. Its level was kept under control in order not to not invalidate the measurements.

- Current consumption: it is caused by the continuous hitting of the multiplied electrons on the dynode metals. This degradates the dynodes by consumption (in particular the one closer to the anode, where the current impinging is higher). In

RUN 1, the total luminosity has been 25 fb^{-1} and PMTs have been crossed by a total charge of about 750C, close to the PMT maximum limit of 900 C. Instead, for RUN 2, it is forecasting a total luminosity of around 50 fb^{-1} per year and an accumulated charge of 2500C.

Therefore, the reasons for a substantial redesign of the detector and its electronics for RUN 2 are:

- The total integrated luminosity expected for 2015-2018 will produce a large collected change in the PMTs used for the detection of particles in LUCID, resulting in a fast ageing;

- the 25 ns bunch-spacing impose stringent limits to the electronic performances;

- the increased particle fluxes result in the saturation of the counting algorithms used for luminosity determination.

These reasons brought us to the replacement of photomultipliers with reduced acceptance to cope with the increased occupancy and particle flux and to a redesign of the readout electronics.

LUCID detector improvements are:

- old PMTs have replaced will the smaller ones described in previous section in which the active window it self will be used as Cherenkov radiator. All the PMTs have been calibrated, using a *Bi-207* source placed on the surface of the quartz window or led and equalized to the same working point in order for LUCID to work properly as luminosity monitor;

- a new board called LUCROD with integrated FADC has been designed to digitalize the signal next to the interaction point and avoid the broadening of analog signals, amplification and shaping. The LUCROD board records the signal above a fixed threshold and count events happening during an ATLAS LB.

3.4 Design and Principle of Detector

The main goal of LUCID is to monitor the inelastic collision rate with sufficient efficiency and low sensitivity to the background. The idea is to count the mean number of inelestic pp collisions through the number of charged particles that are produced in each collision within the LUCID acceptance.

The LUCID [19] apparatus is places around the beam-pipe on both forward ends of ATLAS, symmetric at about 17 m placed far from the interaction point (IP) as is shown in Figure 22 and it is composed by two identical arms (shown in Figure 23).
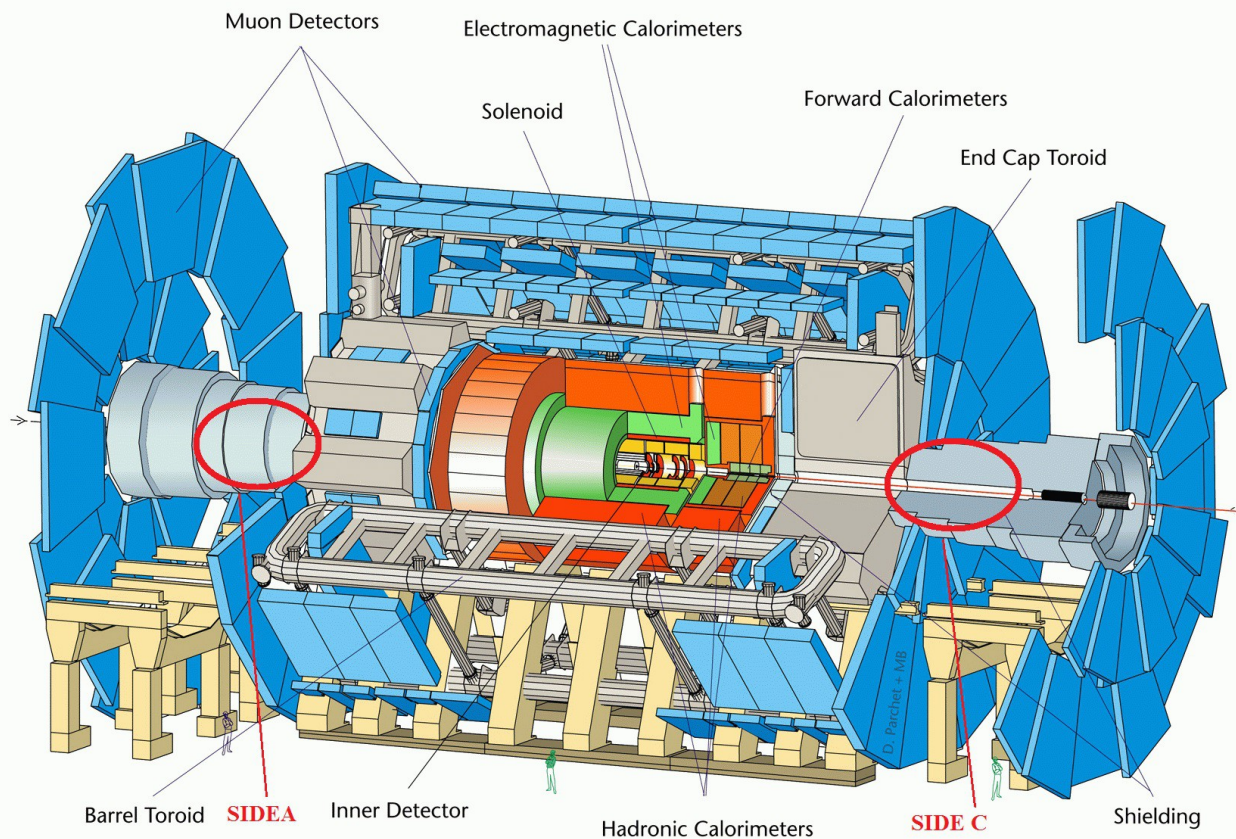
Figure 22: Position of LUCID modules inside the ATLAS experiment

Each detector is composed by 16 photomultipliers and four quartz fibre bundles, which carry the light produced in them to further PMTs, placed far away from the interaction region [20]. As already mentioned, the detecting medium is the quartz window of the PMT itself acting as Cherenkov radiator medium.

When a charged particle traverses a medium with a speed higher than the light in the same medium, it emits photons of a broad range of wavelenghts in the forward direction. These photons produced directly in the quartz window of the PMT easily reach the photocathode where they produce photoelectrons and give rise to a fast electronic signal.
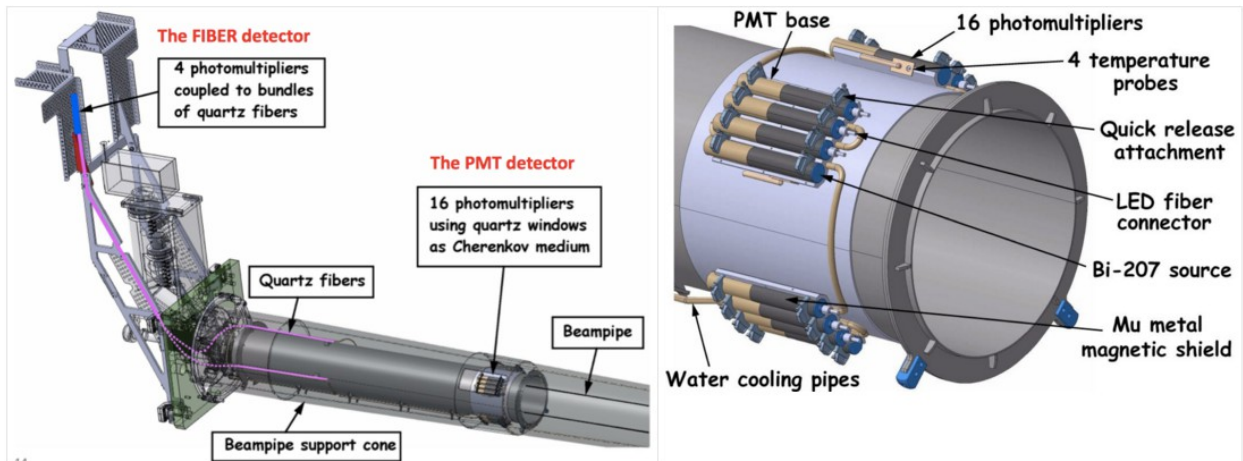
Figure 23: One arm of the LUCID detector

Each arm of LUCID is equipped will four different type of sensors:

- 4 photomultipliers of standard R760 type called VDM PMTs ;
- 4 photomultipliers of standard R760 type with reduced acceptance called Mod PMTs;
- 4 photomultipliers of standard R760 type equipped with *Bi-207* sources for calibration called *Bi-207* PMTs;
- 4 photomultipliers of standard R760 type as spares.

These sensors use quartz window as Cherenkov medium. The four extra fibers are read out by:

- 4 photomultipliers of standard R760 type.

The detector was assembled from June to August 2014. Some photos of the assembly phase are shown in Figure 24.
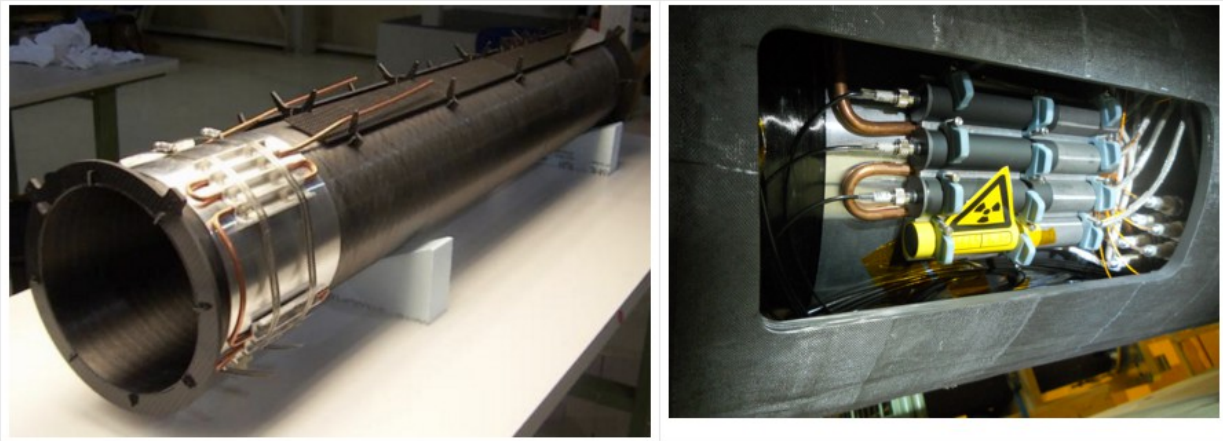
Figure 24: The LUCID detector during the assembly phase

The electronic signal produced by the PMTs is carried on 1.5 m long coaxial low noise cables to the front-end electronics. In every bunch crossing, PMT signals are shaped by the acquisition system and converted in digital hits by a Fast Analog-to-Digital Converter (FADC) on each channel. If signals overcome a fixed threshold (equivalent on average to 15 photoelectrons) a Hit is defined; then, the event is defined from specific hit configurations.

To measure the bunch-per-bunch luminosity, LUCID exploits event-algorithms or hit-algorithms [21]; additionally another method has been developed for the RUN 2 using change for luminosity algorithm. This new method has several advantages since it has a simple direct proportionality to the luminosity, it is free from statistical uncertainty, but it is strongly dependent on the stability of the PMT gain.

From March 2015, the LHC center-of-mass energy is 13 TeV and the average number of bunch crossings is increased up to 40. These conditions imply a large collected charge in the PMTs, due to a greater number of particles passing through the detector, resulting in a faster PMT ageing. The increasing particle fluxes originate a strong anodic current, which causes the PMT saturation (i.e. the loss of linearity of the PMT gain).

Each side of the LUCID detector is equipped with two LUCid ReadOut Driver (LUCROD) boards:

one LUCROD receives the signals form the VDM PMTs, the *Bi-207* PMTs and the spare ones; the second board receives the signals from the Mod PMTs and the fibers.

The hit pattern generated by the four LUCRODs are then sent to two Luminosity And Trigger (LUMAT) boards, each of which receives the hits from the same kind of sensors from the two sides in order to perform combinational algorithms (as shown in Figure 25).

LUCROD boards are near each side of LUCID in the experimental HALL (called UX15) while the LUMAT boards are in the counting room, called USA15), that is 100 m away from UX15, roughy at the same depth in the ground (about 100 m from surface).

The whole LUCID system is synchronized using the signals produced by TTC board (presented in section 5.6.5). The TTC board is able to send synchronized signals to boards located at different distance with a margin of error lower than 1ns. For example LUMAT is close to TTC (about 10 m) but LUCROD is 100 m far from TTC.
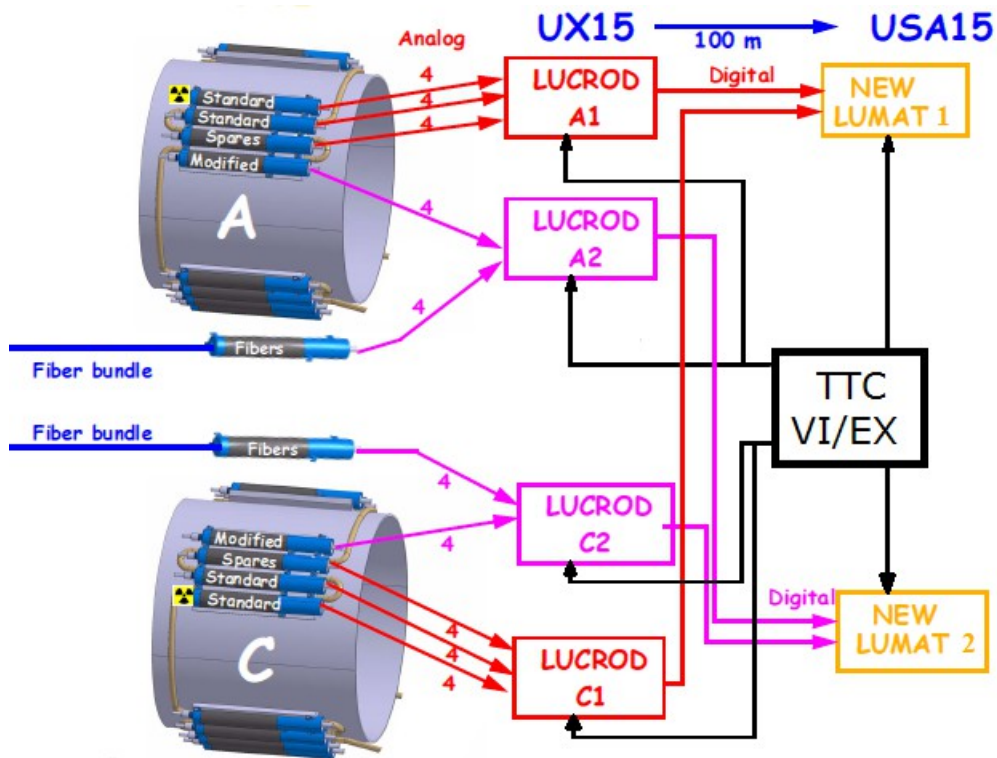
Figure 25: Block diagram of the LUCID detector electronics and readout system.

In Figure 26, it is possible to see a scheme of the new luminosity acquisition system. In the experiment there are two of these systems. Data are digitalized by LUCROD Analog-to-Digital Converter (ADC) and sent to a Field Programmable Gate Array (FPGA). The FPGA manages and sends data to the elaboration board through the fiber link.
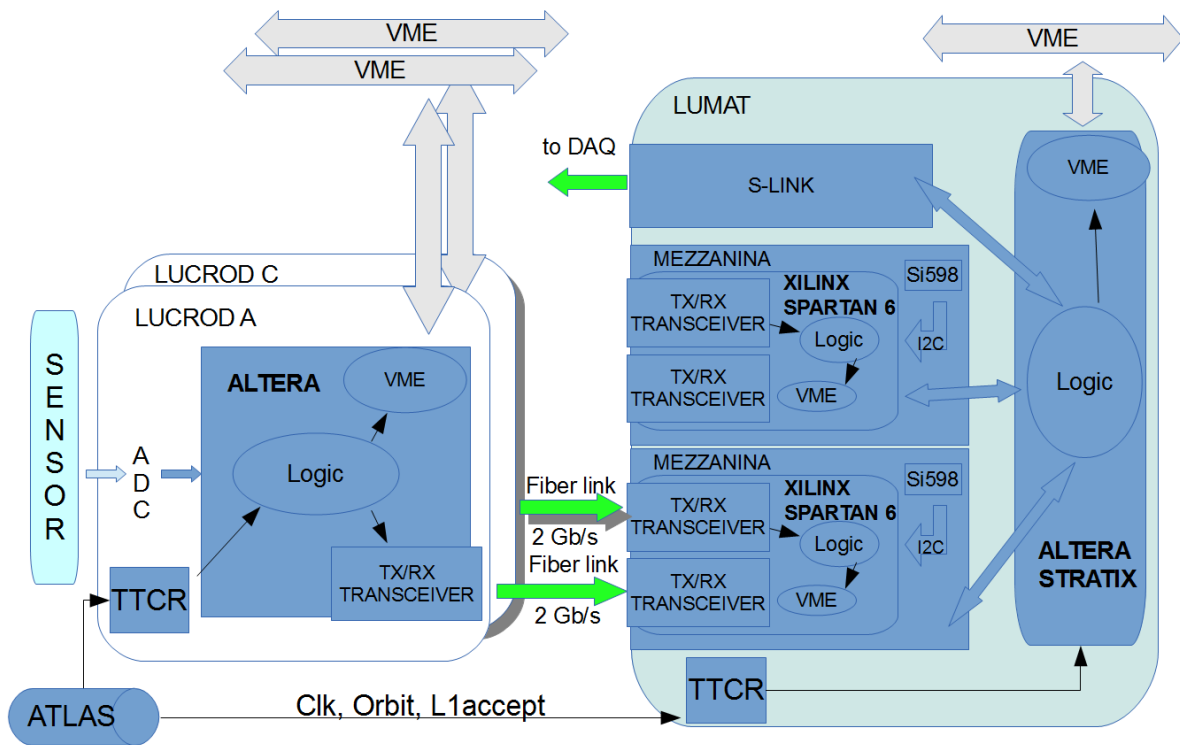
Figure 26: Scheme of the new electronic acquisition system.

LUMAT board receives data through the mezzanine card and sends them to the mezzanine Stratix board to elaborate the result sent to TDAQ software through the mezzanine s-link card and VME bus [22]. All boards are controlled by the VME bus. The details of these boards will be described in the following paragraphs.

3.5 The Field Programmable Gate Array

The Field Programable Gate Array (FPGA) is a modern programmable logic device, whose flexibility has been exploited for the realization of a custom readout architecture [23]. Part of the work realized for my PhD activity concerned the physical integration of all boards and the realization of several optimized firmware components for the FPGA devices located on the LUCID acquisition boards.

In the following chapter the custom firmware of the LUCROD and the LUMAT boards will be presented, discussing the management of the external components and the implementation of the data transmission protocol discussed.

The main digital element of the board is the FPGA. This technology is diffusing more and more in the high-tech scenarios for its low cost per logic-cell and its great flexibility. This programmable device descended from the Programmable Logic Array (PAL) and the subsequent Complex Programmable Logic Device (CPLD) families. Its most powerful characteristic is the possibility to re-arrange its logic elements in order to represent almost any possible digital architecture. In case of a microprocessor or a micro-controller the hardware architecture is static. It is designed to execute a well defined set of instructions. The programming code is then a sequence of these instructions. Instead, FPGA has not a defined architecture but a set of logic elements, which should be configured and interconnected at will to realize a well defined structure, that in principle could be a microprocessor as well. The firmware which is loaded inside an FPGA, is not a sequence of instructions but a topological description of the configuration and interconnections of the basic logic elements. These basic elements are called Configurable Logic Blocks (CLB), mainly made up of a programmable combinatorial net called Look Up Table (LUT) and a relative array of registers (D-type Flip Flop). Any sequential logic machine can be realized with the suitable interconnection of these two elements.

Depending on the manufacturer, the model and the dimension, an FPGA can have a different number of CLBs and each CLB can count on different slices (the minimum logic element).
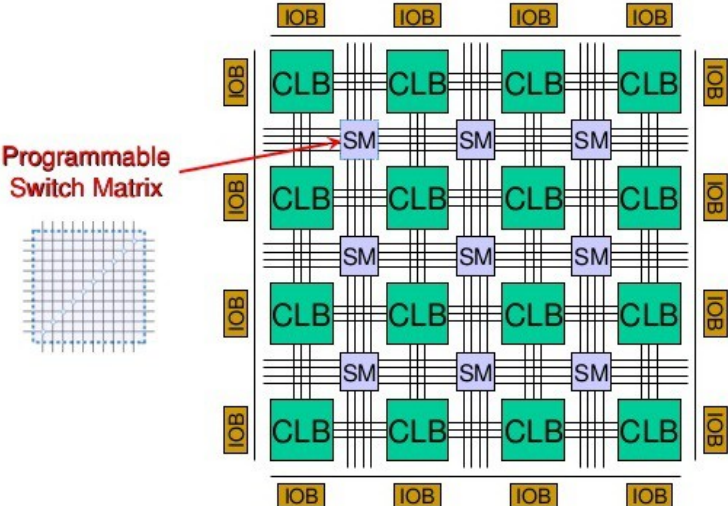

Figure 27: Basic logic elements of a Spartan six FPGA.

Each CLB is made up of four slices and each slice is composed by two LUTs and two registers. Each LUT is equivalent to a digital Multiplexer (Mux) with a 4-bit selector, therefore it can implement any logical function $y = f(x0 ; x1 ; x2 ; x3)$.

Downloading the configuration to the FPGA means that the 16 input lines of the MUX

have been tied to GND or Vdd, defining a specific logical function f. At runtime, "user signals" will be the four selectors of the MUX (x0 ; x1 ; x2 ; x3) and y will be the result of the combinatorial Sum of Products (SOP) operation feeding the output register of the LUT. The slice architecture is represented: the LUTs and the output registers have been described above, while the other components are auxiliary elements allowing the cascading of different slices for the realization of more complex logic. A LUT can also be configured as a block of distributed memory, where 16 bits of information are stored and which can be randomly accessed via the 4-bit selector. A set of distributed memory blocks is known as distributed RAM and it is suited for buffering small amount of data anywhere along signal paths.

An alternative to distributed RAM is Block RAM, which provides a more suitable solution in case of larger amount of data.

This is a real RAM device embedded in silicon together with the programmable logic. The main features of this component are the dual port technology, which allows two independent accesses to the common block of RAM, and the configurable port aspect ratio, that allows different widths between the input and output data ports.

Blocks of RAM are usually used extensively in the firmware architectures for the realization of FIFOs and shift registers.

Like the Block RAM, there are many other devices that are deployed in the silicon chip to support the mere programmable logic. For example, there is a dedicated clock infrastructure and DCMs (Digital Clock Managers), which are appointed to frequency division/multiplication and phase adjustments.

The master clock provided by the experiment is multiplied by an external programmable Phase Locked Loop (PLL).

The chip has several I/O pads even if not all of them are available to the user application, for example the configuration interface has a set of dedicated pads and so have the power-supply rails as well. On the other hand, all the remainder user pins are available to bring in and carry out each signal of the programmed logic. Another useful feature of the FPGAs (that deserves to be pointed out) is the possibility to assign several I/O standards to different groups of pin. In the FPGA device, the programmable I/O blocks are the elements between the core logic and the user I/O pins, a wide choice of digital standards is available (CMOS, LVTTL etc.). Some differential standards are also supported, for example LVDS and LVPECL, in this case I/O pairs are defined for predefined couples of pins.

All the user input/output pins are grouped into areas called I/O banks, each bank shares the same communication standard and the same $V_{CCO,}$ pin. Each bank has a dedicated $V_{CCO,}$ which is used as a voltage reference for the programmed I/O standard on that bank. The allowed voltage references depend on the supported standards and they are: 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V and 3.3 V.

The boards based on FPGA use the Joint Test Action Group (JTAG) or Boundary Scan protocol. It is a standard developed to debug purposes and to load the firmware. This

communication interface foresees a daisy chain interconnection of devices, terminated on the master controller that accesses the slave's registers. In a nutshell, there is a simple serial protocol, which allows to investigate chips behavior during their duty, exploiting very few control pins.

Providing a very simple and almost costless way to access chip registers in read and also write mode, JTAG interface can be exploited for programming purposes as well. Programmable devices had once to be first installed on a programmer system for configuration and then mounted on suitable sockets on their printed circuit boards into a programmer to be configured and then mounted; using JTAG interface that is no more necessary because it is possible to perform the so called In-System Programming (ISP). In other words, a programmable chip can be soldered to the PCB and, then, programmed directly inside its environment. The signal required to drive a JTAG chain are:

- TDI: the serial input line of a chip.
- TDO: the serial output line towards the next chip of the daisy chain.
- TMS: the state machine control signal.
- TCK: the clock of transmission.
- TRST: reset the TAP controller (this is an optional signal).
- TMS and TCK are connected in a star configuration to all the chips of the chain.

Chapter 4

The LUCROD Board

4.1 Introduction

To cope with the stringent requirements of LHC data taking in RUN 2 described in previous section, the INFN section of Bologna started a study on a different front-end architecture based on early digitization of the analog signals generated by the PMTs in LUCID. It was proposed, and successively realized, a new full-custom smart board called LUCid ReadOut Driver (LUCROD) for multichannel analog acquisition of the PMT signals. The LUCROD board is a 9U VME custom board placed in the detector hall.

This choice was mainly caused/justified by the need to cope with the planned change of minimum distance between bunches, which in 2015 has decreased from 50 ns to 25 ns. The transimission via 100 m long wires that were used in the past gave a significant signal shape distortion that was not possible to compensate completely at the receiving end. The baseline restoration in these conditions (reverting to zero of baseline value before next impulse) was optimizad within the 50 ns BC interval as was in RUN 1, but not within the current interval of 25 ns. Therefore the new LUCROD boards have been placed close to the detector and the analog signals have to travel from the PMT to the LUCOD boards only for 15 m.

Before the development of the final configuration with the INFN electronic group (section of Bologna) I started to work for the realization of a demonstrative board integrating the analog acquisition technology and a digital control environment on a basic prototype of LUCROD.

It is possible to subdivide the new smart board into three sections:

1. the analog data acquisition electronics, characterized mainly by a fast ADC which

samples the PMT signal after an anti-aliasing filter. It will be discussed in section 4.2,

2. the digital elaboration electronics, characterized mainly by an FPGA which manages the Fast ADC and manages the sincronization between input data and control signals provided by the experiment. It will be discussed in section 4.2,

3. The communication electronics for the delivery of "hit" data to another custom VME board, sitting 100 m away (LUMAT): in practice we use an FPGA to managing a serial transmission protocol based on 8b/10b. AnFPGA is used to manage the optical transceiver [24]. The configuration of the comunication system is controlled via the VME control bus.

This work was developed in a collaboration between the INFN section of Bologna and the LUCID Group: it formerly led to the production of a prototype board and then to the production of a final board fully compliant with the specification of the ATLAS requirements.

The following paragraphs refer to a final version of the LUCROD board. In Figure 28 a block diagram of the board is shown.
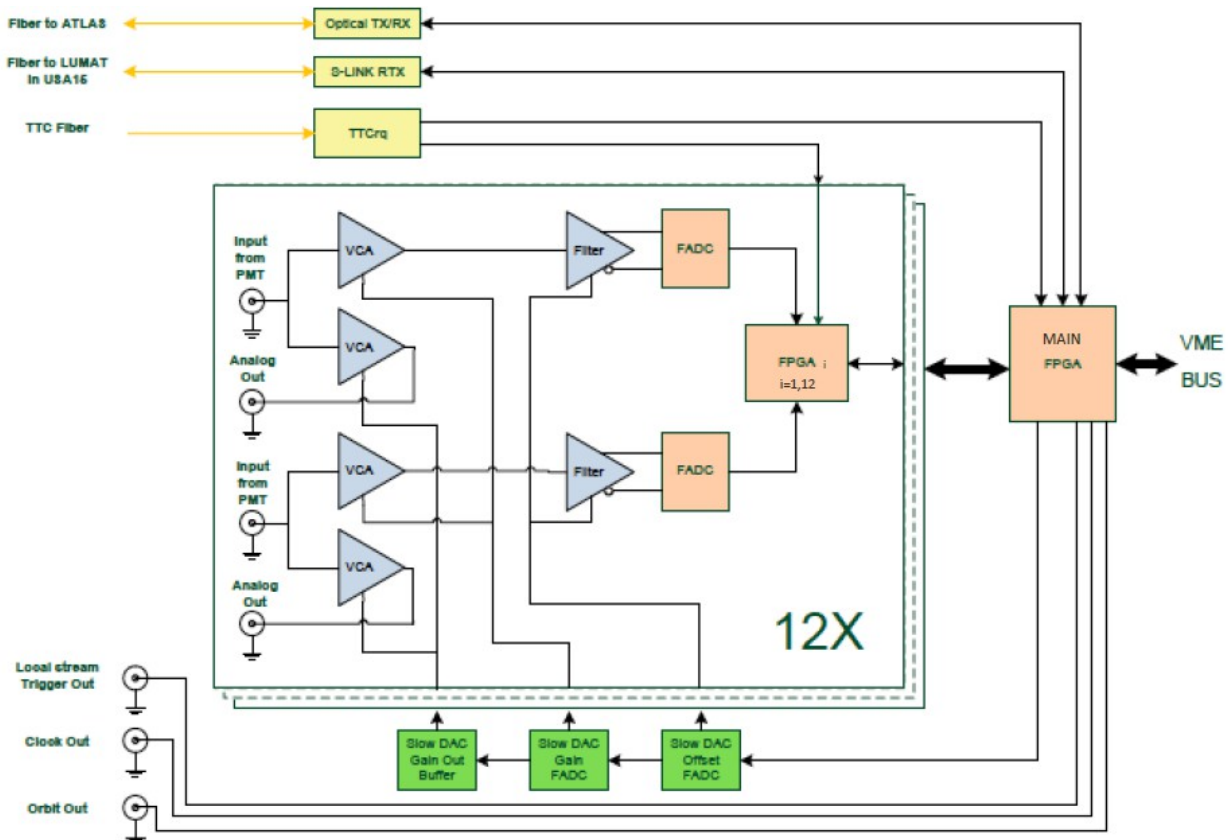

Figure 28: LUCROD's blocks diagram

4.2 The analog processing section

The board has several input/output signals, part of them are electronic signals, part are convoyed on fibers.

The most important input signals are of course the 16 analog input cannels connected to the PMT anode. In addition there are four digital input/output connectors for debugging purposes. All these signals are available on the front panel by means of Lemo connectors.

Each PMT signal is managed by two sections, both used for charge integration, and for discriminating a "hit":

- each on-board channel is amplified by a low noise Variable Gain Amplifier (VGA), single-ended and linear-in-dB. Amplified signals are replicated in output for testing purposes and for backward compatibility with the previous data-acquisition system,

- an anti-aliasing filter with a −3 dB bandwidth of 320 MHz, delivering a differential signal with low harmonic distortion. The internal feed-back circuit also minimizes any gain error that would be associated with the mismatches in the external gain setting resistors. After the filter, signals are processed by a Flash Analog to Digital Convert (FADC) sampling at 380 MSPS.

A key element of the acquisition chain is the Digital Converter. The device chosen is the AD9434 [25], shown in Figure 29. It is a 12-bit monolithic sampling analog-to-digital converter (ADC) optimized for high performance and low power consumption. This component operates at up to 500 MSPS conversion rate and it is optimized for outstanding dynamic performance in wideband carrier and broadband systems.

The ADC requires a 1.8 V analog voltage supply (obtained by a linear regulator from the main tension) and a differential clock for full performance operation. The digital outputs are LVDS compatible and support twos complement, offset binary format, or Gray code.

Eight Cyclone IV [26] FPGAs (one every two input channels) receive the digitized input signals and perform several tasks:

- charge accumulation per BCID: for each Luminosity Block charge is evaluated as the integral of the digitalized signal over one BCID period (which is 25 ns or 8/12 samples) with a dynamic range of 12 bits for a 1.5 V full scale signal;

- hit discrimination: the dedicated logic determines whether the signal acquired from PMTs is a "hit" or not, thanks to a comparator, which verifies whether a prefixed and modifiable threshold is exceeded or not.

- hit counting, per BCID, over each Luminosity Block, a "hit" counter is incremented;

- storage of the digitized signal waveform in 64-sample deep FIFOs, readable via VME, for signal shape monitoring.
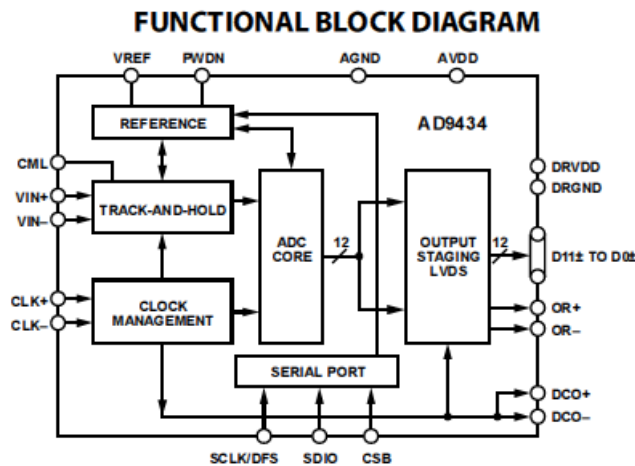
Figure 29: AD9434 Analog-to-Digital Converter function block diagram

Independent threshold and amplification factors are set for each input channel in order to reduce the noise and to optimize the dynamic range. The FPGA for communication purposes send a pattern of the over-threshold PMT signals for each BCID (the so called "hit PMTs" or just "hits") to the LUMAT board by the optical links. The LUCROD board is shown in Figure 30.
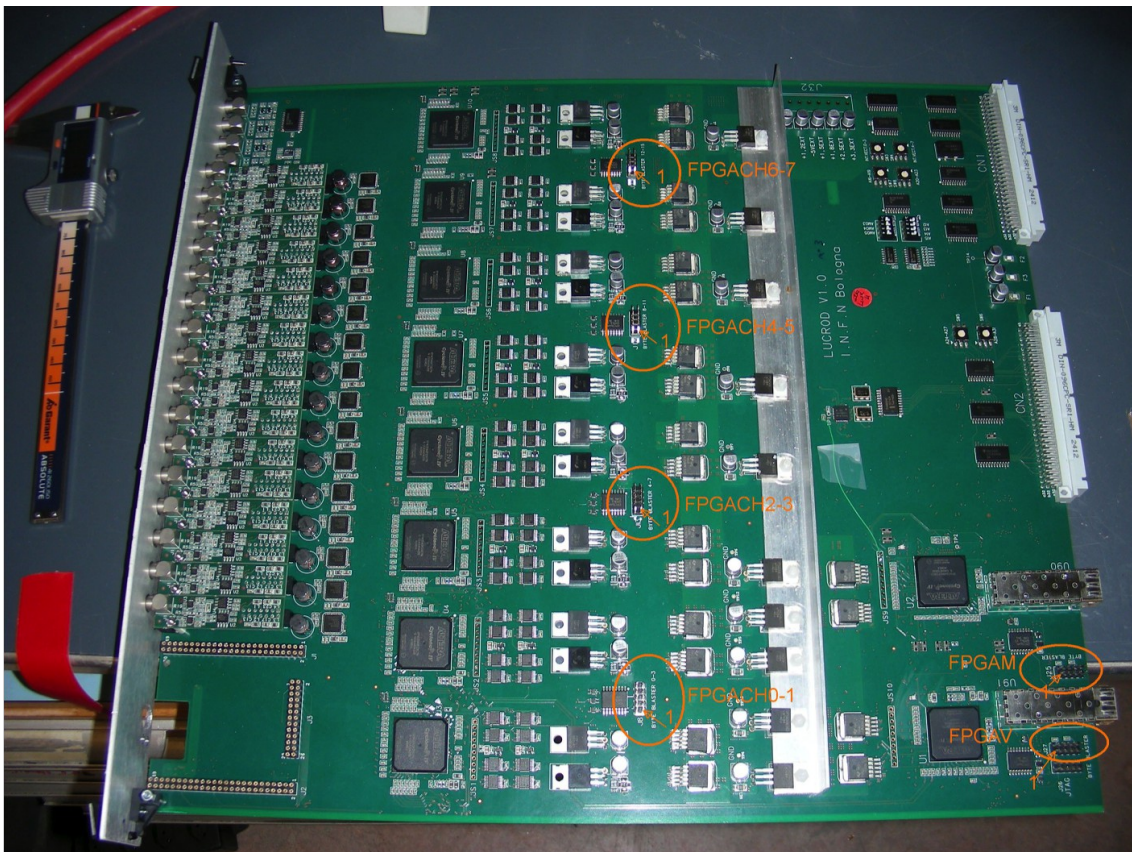
Figure 30: Final version of the LUCROD board

All the FPGAs operate at the 40 MHz LHC clock rate, except for the section dedicated to the acquisition of the FADCs.

The hits and the charge measured for each bunch crossing are used for a quick and partial evaluation of the luminosity. Since each LUCROD collects data from one side of ATLAS only, the luminosity evaluated will be subject to an higher level of background with respect to what is possible to obtain combining data from two sides, as done in the LUMAT board. Nevertheless the luminosity data from the LUCROD are important for monitoring and debugging purposes. The two most important luminosity algorithms performed in the LUCROD board are the collection of hit counts and the accumulation of the measured charge for each PMT and for each BCID. The accumulated patterns collected withing a luminosity block (LB, as described in chapter 3) are readout via the VME bus and stored for lumiosity conversion.

Figure 31 shows two of the luminosity algorithms performed by the LUCROD board: single-channel hit counting (left) and total charge integration (right) recorded during a typical pp runs. The two plots refer to the *Bi-207* sensors (see section LUCID).

From the hit/charge pattern the filling scheme of LHC beams (filled/empty bunches) is well visible.
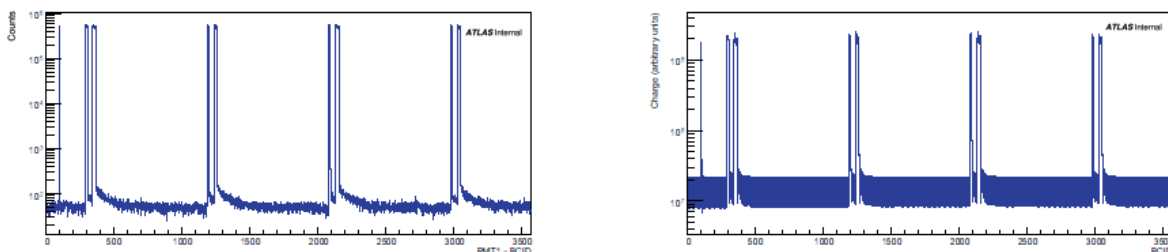
Figure 31: LUCROD PMT hit counts (left) and integrated charge (right) for a single PMT equipped with Bi-207 source (see section LUCID) in a typical LB of a pp physics run in 2015. From the hit/charge pattern the filling scheme of LHC beams (filled/empty bunches) is well visible. The constant bunch ground level in both plots is due to the irreducible source activity.

4.3 8b/10b protocol

Before starting to describe the firmware implemented on the main FPGA of the LUCROD and on the receiving end in the LUMAT, as it is strictly related to the used transmission protocols, a general overview of the functions and of the protocol used is given here.

The LUCROD board features two data output channels managed by two different ALTERA Cyclone IV FPGAs:

- the VME bus, using Single data and Block transfer protocols;
- the optical link transceivers, that send the "hit" patterns to the LUMAT board for combinatorial algorithms.

Due to the presence of a serial link with clock recovering on the receiving part, a modulation must be introduced to avoid the presence of DC and low frequency components.

For this purpose a digital modulation protocol called 8b/10b has been adopted. It brings mainly two significant advantages: it transmits a DC-free signal and it introduces redundancy, that is used for error detection and transmission of special control characters.

The 8b/10b coding scheme was initially proposed by Albert X. Widmer and Peter A. Franaszek of IBM Corporation in 1983 [27]. The encoder, on the transmitter side, maps the 8-bit parallel input to a 10-bit output. This 10-bit output is then shifted out through a high-speed serializer (Parallel-in Serial-out 10-bit Shift Register). The serial data stream is transmitted through the transmission media to the receiver.

The high-speed deserializer (Serial-in Parallel-out 10-bit Shift Register) on the receiver side converts the received serial data stream from serial to parallel. The decoder then re-maps thus the 10-bit data back to the original 8-bit form (see Figure 32 for a pictorial view of the deserialize and decoder 8b/10b).

Figure 32: Deserializer and decoder 8b/10b

When the 8b/10b coding scheme is used, the serial data stream is DC-balanced: DC-balanced means that it keeps almost the same number of 0's and 1's on the stream. Another quantitative parameter which is kept low, is the Run Length, defined as the maximum number of contiguous 0's or 1's.
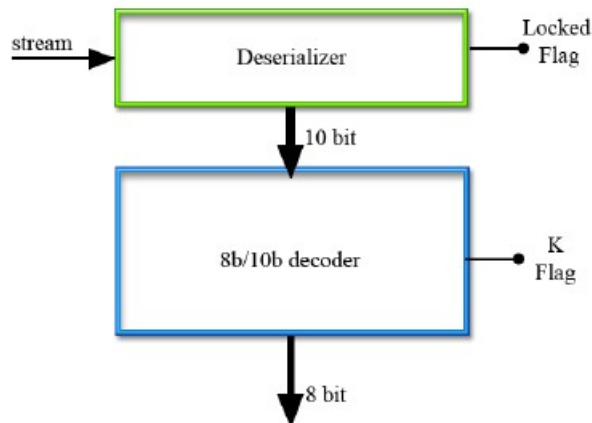
The 8b/10b encoder converts 8-bit codes into 10-bit codes. The encoded symbols include

256 data characters, named Dx.y, and 12 control characters named Kx.y.

The coding scheme breaks the original 8-bit data into two blocks, three most significant bits (y) and five least significant bits (x). Bits from the most significant one to the least significant one are named H, G, F and E, D, C, B, A. The 3-bit block is encoded into 4 bits named j, h, g, f. The 5-bit block is encoded into 6 bits named i, e, d, c, b, a as it is shown in Figure 33. The 4-bit and 6-bit blocks, also called sub-codes, are then recombined into a 10-bit encoded value.
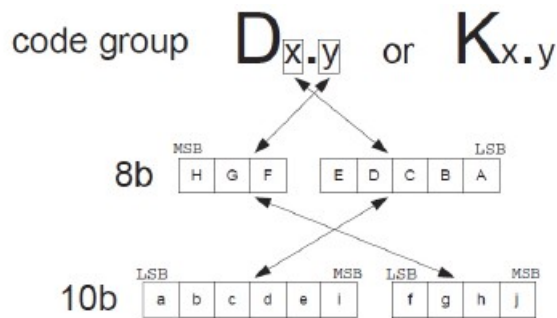
Figure 33: Conversion scheme in the 8b/10b modulation algorithm.

In order to create a DC-balanced data stream, the concept of Block Disparity is used to balance the number of 0's and 1's. The disparity of a block is calculated by the number of 1's minus the number of 0's. The value of a block that has a zero disparity is called disparity neutral.

Running Disparity (RD) is the sum of disparities of all the previous characters. It is tracked during transmission in order to keep the line balanced. Having the characters a maximum modulus of disparity equal to 2, the RD will be confined between two values, at most distant 2, if a wise sequence of the encoded words is generated.

In order to do that, every byte is associated to two 10-bit character encodings: the RD+ and the RD- representation. Encodings with disparity either +2 or 0 (disparity neutral) belongs to the RD- group while the RD+ values are the encodings with a disparity either -2 or 0. When the Running Disparity is maximum the RD+ encoding of a byte will be chosen, having a negative or null disparity it will keep the RD confined in the allowed range.

The dynamic evolution of disparity, for every bit transmitted on the serial line, is called Digital Sum Variation (DSV), and in the particular case of the 8b/10b code it is limited between +/-3.

In addition to the RD+ and RD- encodings for the 256 bytes (the D-codes), there are also 12 RD+ and 12 RD- codes that still allow to respect a run length of five and a DSV = +/- 3 on the data stream.

These are choses as the Control Characters used for the implementation of line services,

usually refer to as K-codes. The RD+ and RD- representations of the K-codes are shown in Table 3

	8bit code	RD-	RD+
K28.0	000 11100	001111 0100	110000 1011
K28.1	001 11100	001111 1001	110000 0110
K28.2	010 11100	001111 0101	110000 1010
K28.3	011 11100	001111 0011	110000 1100
K28.4	100 11100	001111 0010	110000 1101
K28.5	101 11100	001111 1010	110000 0101
K28.6	110 11100	001111 0110	110000 1001
K28.7	111 11100	001111 1000	110000 0111
K23.7	111 10111	111010 1000	000101 0111
K27.7	111 11011	110110 1000	001001 0111
K29.7	111 11101	101110 1000	010001 0111
K30.7	111 11110	011110 1000	100001 0111

Table 3: Control characters coding

When a control character is received, the decoder informs the upper protocol that the decoded value is a control code and not a data byte.

Control codes are useful during the link negotiation phase, for data-packets delimitation and, in our specific case, they are employed to transmit also real-time commands.

When the transmitter is powered up, the transmitter starts to send a sequence of comma characters (K28.5) and the receiver tries to lock on it. The sequence of successive K28.5 codes in the RD+ and RD- form, allows to univocally delimitate the beginning of a character as no possible overlapping subset corresponds to any valid symbol.

All the invalid characters received generate an error flag on the decoder. Redundancy is then exploited for the detection of communication errors which can generate invalid codes or violations in the Running Disparity. In case of a RD violation, the error occurred not necessarily in the last character received. Therefore the standard impose to consider invalid all the last three characters received. The upper protocol is informed of such errors by dedicate flags, in case, it must be programmed to take the appropriate measures.

4.4 FPGA firmware

The main task of the digital logic on the ALTERA Cyclone IV FPGA is managing the

acquisition process and the data transmission.

The whole firmware project has been developed using VHDL code, a hardware description language widely used to program FPGAs. This kind of language could seem similar to a procedural programming code at first sight, but the basic concept is though very different. VHDL is meant to describe parallel logical operations that can be synthesized into a hardware port netlist. On the contrary, a programming code like C, generates sequence of instructions for a specific hardware.

The software environment used for the firmware development is Quartus II by ALTERA, a tool provided by the same FPGA manufacturer. This environment includes mainly a source code manager, the code editor and a graphical user interface for the implementation programs. When the synthesis takes place, formerly the high level language is compiled and transposed into a netlist of abstract logical ports which perform the required operations. The synthesized netlist is then used to implement the design into a specific target device. The implementation phase is subdivided into three main parts: map, place and route, and generation of the configuration file.

Mapping basically creates a 1 to 1 correspondence from the gates required by the netlist and the physical resources of the device (LUTS and registers). Afterwards these elements have to be placed in a convenient way in order to ease the interconnection between them and to optimize path delays; this is what happens during the place and route phase. The last step in the implementation procedure is the condensation of the programming information into a binary configuration file, which is the sequence of bits that will be physically shifted into the configuration memory of the device.

The main operation that the FPGA connected to the optical link has to perform is to send the pattern of hit PMTs every 25 ns to the LUMAT board with some additional information. The main difficulty related to this task is that there is a countinuous flow of data without any interruption and that the data coming from two different LUCROD have to be synchronized at the receiving end and still be in sync with the LHC clock.

For this reason in the FPGA it has been developed an entity called "OPTO LINK INTERFACE" which receives the pattern of hit PMTs and information from the LHC beam clock and status and codes all the information on the fiber. To cope with the synchronization problem specific solutions have been implemented in the FPGA that are not usually employed in serial communications.

In order to check the proper functionality of all the data chain several debugging features are present.

The reference image that schematize the whole firmware is presented in Figure 34 in order to help the reader during the description of the blocks.
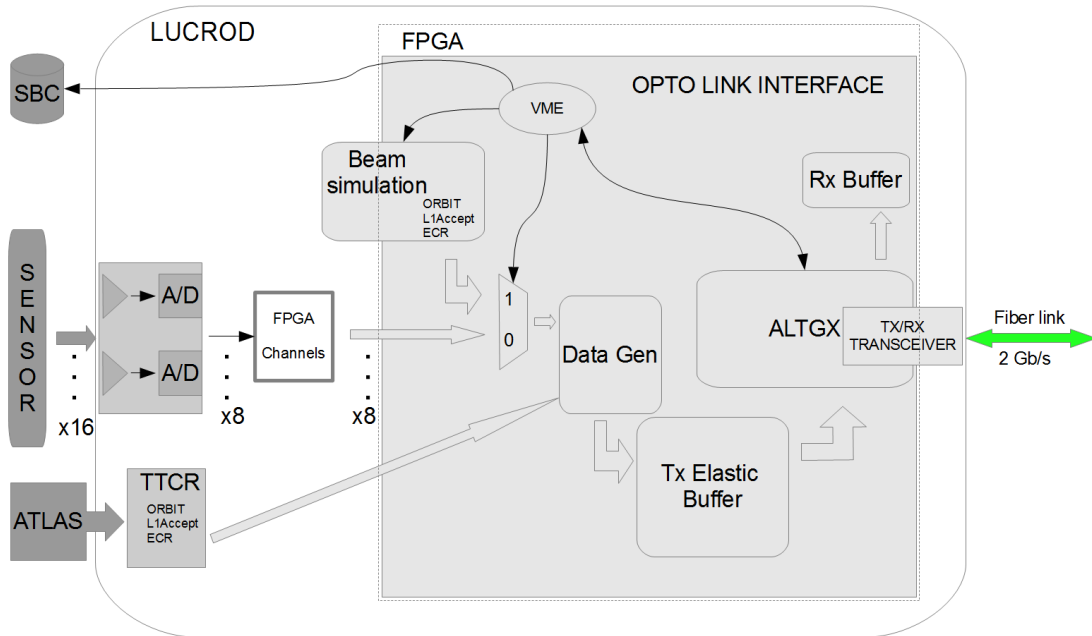
Figure 34: Firmware's block diagram of LUCROD

The top "optolink_interface" entity, shown in Figure 35, includes all the sub-entities for data transmission on the LUCROD side of the link.

```
1    entity optolink_interface is
2      port(
3        reset                  : in std_logic;-- main reset
4        XC_clk                 : in std_logic;-- Quartz osc. for GX
5        SYS_clk                : in std_logic;-- System CLK, LHC 40 MHz clock.
6        -- R/W Registers
7        RWReg0                 : in std_logic_vector(15 downto 0);
8        RWReg1                 : in std_logic_vector(15 downto 0);
9        RWReg2                 : in std_logic_vector(15 downto 0);
10       RWReg3                 : in std_logic_vector(15 downto 0);
11       RWReg4                 : in std_logic_vector(15 downto 0);
12       RWReg5                 : in std_logic_vector(15 downto 0);
13       RWReg6                 : in std_logic_vector(15 downto 0);
14       RWReg7                 : in std_logic_vector(15 downto 0);
15       -- ReadOnly Registers
16       ROReg0                 : out std_logic_vector(15 downto 0);
17       ROReg1                 : out std_logic_vector(15 downto 0);
18       ROReg2                 : out std_logic_vector(15 downto 0);
19       ROReg3                 : out std_logic_vector(15 downto 0);
20       ROReg4                 : out std_logic_vector(15 downto 0);
21       ROReg5                 : out std_logic_vector(15 downto 0);
22       ROReg6                 : out std_logic_vector(15 downto 0);
23       ROReg7                 : out std_logic_vector(15 downto 0);
24       --RX
25       RX_datavalid           : out std_logic;
26       RX_dataout             : out std_logic_vector(31 downto 0);
27       --TX
28       TX_push                : in std_logic;
29       TX_datain              : in std_logic_vector(31 downto 0);
30       -- Serial Link
31       RX_datain              : in std_logic;
32       TX_dataout             : out std_logic
33     );
34   end optolink_interface;
```

Figure 35: Input/output port of "optical_interface"

RWReg and ROReg from 0 to 7 are connected with the LUCROD configuration registers driven by the VME bus, in order to manage logic-controlled signals.

The PMT signals, amplified and converted, are connected in input to the top entity through the "TX_datain" bus, and "TX_push" corresponds to the data valid bit.

In the top entity it is possible to select between real data from the sensors or simulated data coming from a beam and PMT response simulator (described in 5.6.6).

The selected signals are then sent together with a signal marking the BCID number 0, called "Orbit" signal, "data valid", and other control signals to the sub-entity called "TX_elasticBuffer" (see Figure 36)

The role of this entity is to let data cross two asynchronous frequency domains.

```
1   entity TX_elasticBuffer is
2      generic(
3         EB_HF_ASSERT_TH    : integer := 32;        -- elastic buffer half full assert threshold
4         EB_HF_NEGATE_TH    : integer := 32;        -- elastic buffer half full negate threshold
5         -- elastic buffer clock correction 32 bit sequence
6         EB_CC_D_SEQ        : std_logic_vector(31 downto 0):= x"000000bc";
7         EB_CC_k_SEQ        : std_logic_vector(3 downto 0) := "0001"
8      );
9      port(
10        sync_reset    : in std_logic;                    -- synchr. reset: MUST BE SYNC TO SLOWEST CLOCK: int_dp_clk
11        wr_clk        : in std_logic;                    -- input data path clock @40 MHz
12        wr_en         : in std_logic;
13        data_in       : in std_logic_vector(31 downto 0);  -- 32 bit @ 40 MHz
14        int_dp_clk    : in std_logic;                    -- Internal Data Path clock @50 MHz
15        rd_clk        : in std_logic;                    -- output data path clock @100 MHz
16        data_out      : out std_logic_vector(15 downto 0); -- 16 bit @ 100 MHz with K-padding
17        k_out         : out std_logic_vector(1 downto 0)
18     );
19  end TX_elasticBuffer;
```

Figure 36: Input/output port of "TX_elasticBuffer"

The elastic buffer entity receives three clock signals:

- sys_clk   : the main 40 MHz clock of the experiment;
- GX_clk_50   : a 50 MHz clock generated from the transceiver PLL;
- GX_clk_100 : a 100 MHz clock derived as 2 x GX_clk_50.

32-bit input data are written synchronous with the main experiment clock (40 MHz) inside a true dual-port FIFO [28].

With a higher frequency clock "GX_clk_50", data are extracted from the fifo. In order to balance the read/write clock slack, an almost-empty/-full logic introduces special padding words starting with a k28.5 character (a special control sequence of the 8b/10b protocol, see Table 3). The 8b/10 control sequences placed in the data flow are also used to align the byte boundaries on the receiver counterpart.

The built-in transceiver is able to manage words with a maximum width of 16 bits, so a word chopper is used running at twice the elastic buffer read clock speed. "GX_clk_100" is provided in order to send the 32-bit elastic buffer output in groups of 16-bit words at double the speed. The "Data_out" bus, running at 100 MHz, moves data from this entity towards the sub-entity called "ALTGX0". The latter is responsible of data serialization and it directly drives the optical transceiver towards the LUMAT board.

In the following Figure 37 is shown the whole data path across several clock domains inside both LUCROD and LUMAT (see the chapter below).
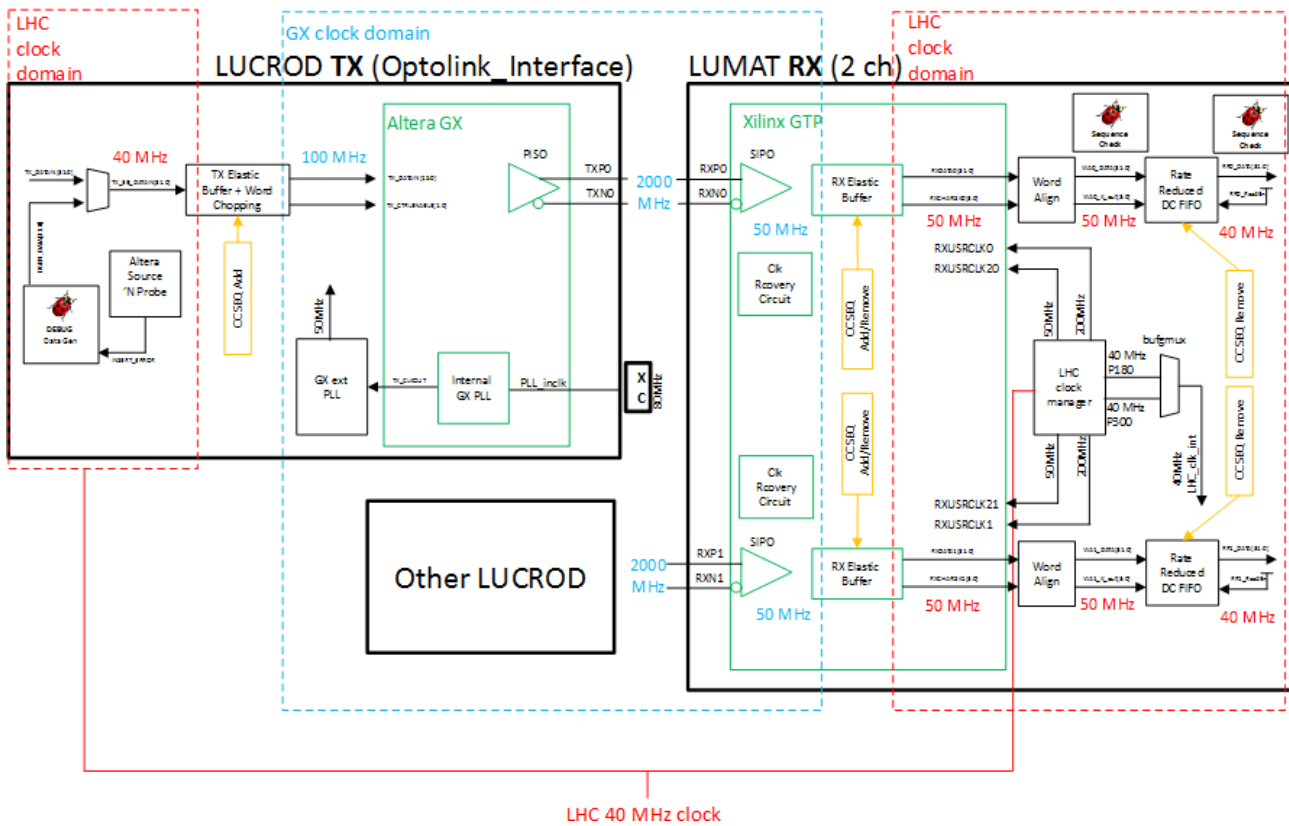
Figure 37: Scheme of logic managed the connection between the two board

LUCROD board sends incoming data from the sensors thanks to the logic described above serialized on the optical fiber link with a speed of 2 Gbit/s (40 bits @50 MHz).

Considering the data transmission link as a whole, for the sake of clarity, VHDL blocks used in the receiver mezzanine are described here below, in the LUCROD section, though being part of the LUMAT board.

An elastic buffer is implemented inside the "GTP" entity, its aim is to keep up the data flow despite its read/write asynchronous clocks by means of adding/removing the padding words included in the protocol.

Input data from the optical link are synchronous with the 50 MHz LUCROD transceiver's PLL and they come out of the "GTP" entity synchronous with the 50 MHz clock derived, on the LUMAT board, from the 40 MHz main LHC clock. This operation is realized removing (if the buffer is almost full) or putting (if the buffer is almost empty) the special padding words. 32-bit deserialized data, outgoing the gtp block, are sent to the "WordAlign" entity, who's role is to find the word edge. Aligning words (containing k-word and zeros) are used for this operation.

At the end, data after word alignment are sent to the "RateReduced" entity, where all the padding words are permanently removed and data rate is reduced back to its original frequency of 40 MHz.

The stream obtained is again synchronous with the main LHC clock at 40 MHz, and now it can be sent to the decoding and elaborating logics for the luminosity measurements as described in the following paragraphs.

Chapter 5

The LUMAT Board

5.1 Introduction

The Lumat board has been produced by INFN Research Group in Bologna. It is a large 9U board, designed to be located in an VME crate, characterized by five mezzanine (Figure 38) and described as follows:

1) A 9U motherboard, constituted by connectors for VME bus and FPGA, used to manage the bus communication protocol.

2) A main mezzanine based on FPGA Stratix II (Altera) [29] with 1508 pins, placed in the central part of the board, aimed to manage both incoming data from the receiver mezzanine and communication of subsequent elaboration stages. This board is the most important part during the elaboration process of sensors signals. The 18-layer structure of the board is due to the copious amount of FPGA pins. Six high-density connectors have been used, each connector features more than 180 pins. This mezzanine is the main responsible for luminosity measurements. In the following table (Table 4) are listed FPGA's characteristics:

Characteristics	EP2S130
ALMs	53.016
Adaptive look-up tables (ALUTs)	106.032
Equivalent LEs	132.540
M512 RAM blocks	699
M4K RAM blocks	609
M-RAM blocks	6
Total RAM bits	6.747.840
DSP blocks	63
18-bit x 18-bit multipliers	252
Enhanced PLLs	4
Fast PLLs	8
Maximum user I/O pins	1.126

Table 4: FPGA's characteristics

3) Two mezzanine boards, called receiver mezzanines, host two FPGA Spartan VI (Xilinx) [30] each, which manage bidirectional optical channels (described in paragraph 5.2). These boards are used to receive data sent from the LUCROD board (described in the previous chapter). The main role of these FPGAs is to implement the optical fiber communication based on the 8b/10b protocol (see paragraph 4.3). The input connectors of the board are four SFPs for the optical transceiver modules [31]. Each channel is capable of 2 Gbit/s, allowing a total bandwidth of 8 Gbit/s for each mezzanine.

4) An S-Link LSC (Link Source Card) mezzanine is used both to transmit elaborated data towards subsequent PC acquisition stages to allow recording of data on disk. Using a base clock of 40 MHz the link data rate is 160 Mbyte/s.

5) An acquisition system based on signal from TTC-rq board (described in paragraph 5.6.5) characterized by 40 MHz clocks signals and able to correct phase using an external signal from the ATLAS.
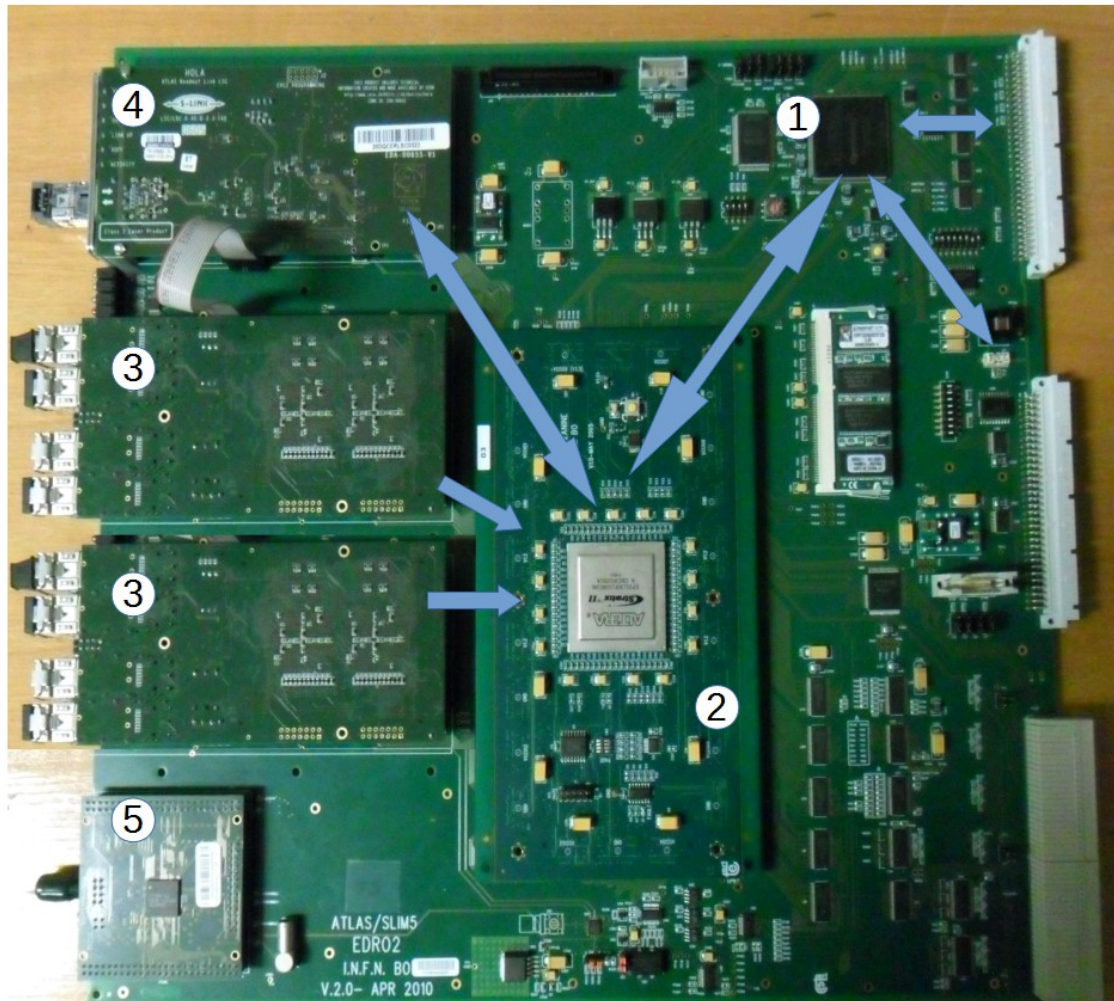
Figure 38: LUMAT board

5.2 Design features

The ATLAS experiment has been designed to last at least 20 years and several upgrades of its detectors have been and will take place to cope with the increasing collision energy and increasing luminosity delivered by LHC. For this reason, most of the electronics in ATLAS is composed by modular elements that can be easily replaced without the need to change the system alltogether. This allows a continuous improvement of the system at a small overall cost but requires a design phase that takes possible extensions and flexibility into consideration.

During the board planning stage, simple and easy methods have been chosen to manage and up-grade the project; FPGA devices are actually quite easy to manage, and they have been chosen because they are easily reprogrammable. They have been put on interconnected boards, so it is possible to change only non-functional boards in case of system damage.

Low-speed series ports have been used where transmission velocity is not essential, while optical fibers in series connections (with high efficiency and low failure rate) have been used where a high speed and high bandwidth is required [32].

Series resistors have been used in parallel buses both to avoid problems related to signal reflections in the conductive medium, and to access signals with the probe of an oscilloscope. All signal paths interconnecting the receiver mezzanine, the Stratix II FPGA (240 trails) and the S-link (42 trails) have been treated in this way.

Instead, signals incoming from the differential optical links interface (LVDS) have been treated to be very insensitive to noise. Signals are transformed into single ended on the receiver mezzanine board.

Triggers and control signals from the ATLAS experiment are distributed to the DAQ boards like LUMAT through a dedicated optical fiber. The fiber receiver is another mezzanine board, produced by CERN and called TTCRQ (described in 5.6.5), that through impedance controlled traces and controlled skew, distributes trigger and timing controls to each FPGA on board.

5.3 System development workflow

The development of the luminosity measurement system has been done in several steps, most of which performed in Bologna during my PhD. Since the whole system is quite complex and has to be tested extensively before the final installation on the ATLAS detector, a significant ammount of time has been invested in providing debugging and monitoring features on the boards and in performing long-lasting lab tests.

During my PhD I've been involved in the realization of the firmware on the LUMAT board, the comunication firmware on the LUCROD board and on system tests in Bologna and at CERN.

Validating the electronics consists in the whole assembly and test phase.

The system is made of a LUMAT board in a VME crate, connected to a LUCROD board and to computers for boards management and data storage on disk.

In the crate there is an VME bus through which the boards can communicate both ways.

The bus is also connected to a Linux-based Single Board Computer (SBC), accessible via Ethernet interface.

The SBC allows to write and read the board's registries through VME and to interact with Stratix, receiver mezzanine and the LUCROD firmware.

During my PhD activity, I dealt with the assembly of various parts composing the system, with FPGAs' firmware programming, developing the several communication protocols in use, and the necessary VHDL logics, with the testing and putting in place of the electronic system and with the installation of the boards within the ATLAS experiment.

Since the validation phase took place away from the LHC, the firmware needed to be designed with an algorithm core and a data or signals simulation part, otherwise not available during testing phase.

During an advanced test phase, we realized the need for a generator of pattern hits constantly operating. A random generator has been created as a hardware simulator in the receiver mezzanine, much faster than the preceding one and with several parameters, such as the rate configuration.

In the code there have been included software configurable VME registries, that allow to choose between functioning, depending on LUCROD's presence and on real or simulated data.

Operating modes are:

- simulation (debug)
    - text files acquisition (only used during first phase)
    - random generator in the board
- real data (physics)

Subsequently, I worked on the whole FPGA management code.

Code and algorithms features will be presented in the following paragraphs.

5.4 LUMAT board's Firmware

As I said in the previous chapters, LUCID system on Atlas experiment has been designed to track on hardware PMTs sensors data, located on the far ends of the experiment.

Data are produced by sensors and then digitalized and organized within the LUCROD board, that sends data on fiber via optical link to the LUMAT board (as seen in chapter 4).

The LUMAT board is entitled with the task of combining data from the two detector sides to produce on-line and off-line luminosity measurements. The resulting patterns are sent to the main FPGA mounted on the board, a Stratix II, for luminosity algorithm implementation.

In the receiver mezzanines the serial data are sent to the two (one is for backup) Xilinx Spartan six FPGA's, where the deserialization and word alignment described in paragraph 4.4 is performed.

After the boards' firmware development phase (described in the following paragraphs), and after developing a consistent and strong code, there was the testing phase for the whole system. Tests were performed in lab, both at INFN in Bologna and CERN.

The project consisted in manufacturing a LUMAT board able to receive data at high speed from LUCROD board, to elaborate them quickly and to provide useful information for future elaboration.

5.5 Receiver mezzanine

The mezzanine called receiver mezzanine (shown in Figure 41) is equipped with two Spartan VI FPGA (Xilinx), each one manages two optical channels. Only one channel in each mezzanine is used (one FPGA and two optical links), receiving incoming data from side A and from side C, while the remaining channel is spare, in case of problems on first channel.

The FPGA firmware is organized into several entities, as shown in the Figure 39 and Figure 40.

The GTP entity is described in the 4.4 paragraph.

Link Version: R00[15:8]
Firmware Version: R00[7:0]
Debug counter: R03[31:0]   (General Purpose Counter)

SA Hist reset : RW1[10]
SA Hist Freeze: RW1[9]
SA Hist Address : RW1[8:0]
SA Hist Data out: R02[19:0]

Spy Hist

LUCROD A

Serial Ch0

GTP

Data stream recovery logic

LUCROD data

Beam Sim

0
1

Stream Aligner

Sim Soglia = RW2[31:16]
Mask Sim Soglia = RW2[15:0]
Sim Parametri A = RW3[31:0]
Sim Parametri B = RW4[23:0]

Delay= RW4[28:25]

Select Data: RW4[24]

LUCROD C

Serial Ch1

Data stream recovery logic

LUCROD data

Beam Sim

Orbit Delay

1
0

SA Orbit Phase: R05[11:0]
SA Aligned: R05[12]
SA First Ch : R05[17:16]

ByteAligned1: R04[22]
ByteAligned0: R04[21]
PLL Locked: R04[20]
RX buffer status1: R04[19:17]

RX buffer status0: R04[16:14]
RR1 track data: R04[13]
RR0 track data: R04[12]
WA1 realign cnt: R04[11:8]

WA0 realign cnt: R04[7:4]
WA1 aligned: R04[3]
WA0 aligned: R04[2]
SFP Loss Of Sync: R04[1:0]

Figure 39: Firmware's Block diagram of receiver mezzanine

Orbit Counter

Count = R06[31:0]

Hamming Encoder

Stratix Core

Stream Aligner

Hamming Encoder

Orbit Counter

Count = R07[31:0]

Counter Reset = RW1[11]

Realign Counter

SA Realign cnt: R05[23:20]

I2C Reset: RW0[25]
Wr enable: RW0[24]
Read/Write : RW0[23]
Slave Address: RW0[22:16]
Slave Register: RW0[15:8]
Data in: RW0[7:0]

I2C interface
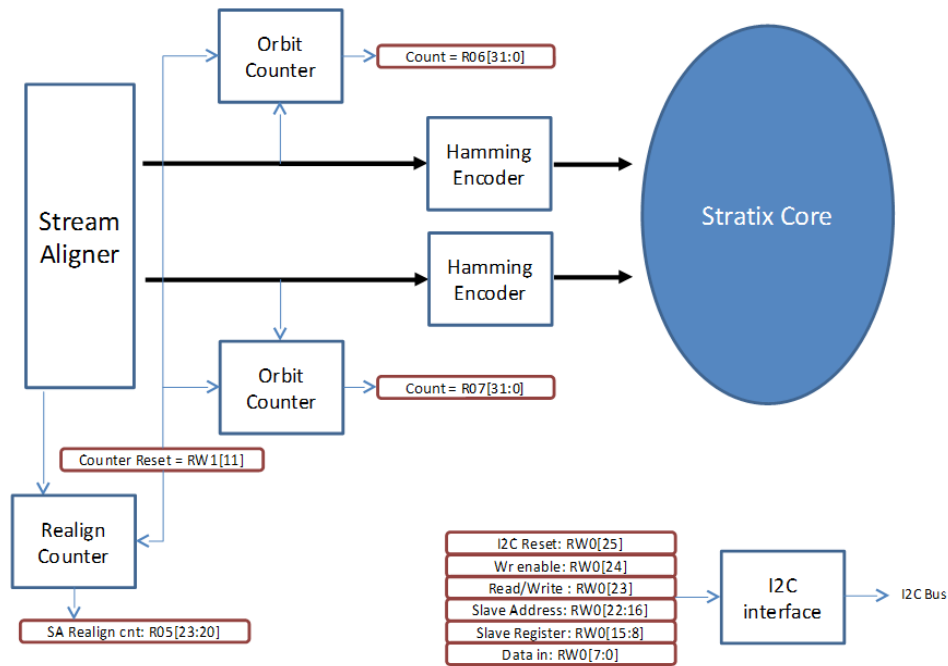
I2C Bus

Figure 40: Firmware's Block diagram of receiver mezzanine

Data arrive from the optical transceiver in the GTP entity, that manages the deserialization process. As seen in paragraph 4.3, this entity receives two channel data at 2 Gbps, decodes them in two streams of data and codes at 50 MHz and then sends the PMT data at 40 MHz at the next entity.

Data are sent at the 40 MHz LHC clock to the stream aligner entity, that recognizes the delay between two channels and aligns data from side A and side C.

A set of quality-check and debug words is stored in the VME registers, counting the number of successful and failed alignments, as well as the BCID distance between the "orbit" signals from the two sides, ensuring accurate quality assessment and quick problem solving.

Since LHC beam is not always available to have the or even the two LUCRODs an important part of the FPGA code consists in a random hit pattern generator, which is configured through VME registers to reproduce particular beam structures and for variable degrees of intensity and randomization. This entity called "beam_sim" described in paragraph 5.6.6), is essential to test new features and components without the necessity for detector input, that is available mostly during physics runs that cannot be disrupted by hardware tests.

Every entity is also managed by registers connected to the VME bus.

After the stream aligner the data are in principle ready to be sent to the Stratix II FPGA for use in luminosity algorithms. Since this comunication is done with parallel lines running thought two connectors and three different PCB boards (the mezzanine, the main LUCID board and the Stratix board), before sending data out they have been coded through a Hamming code that ensures single error correction and double error detection.

Therefore, after realignment, data are sent to the Hamming encoder entity, to be encoded with Hamming code. Then data are sent to Stratix mezzanine, where after a Hamming decoder entity, special algorithms are applied to obtain the luminosity measures.
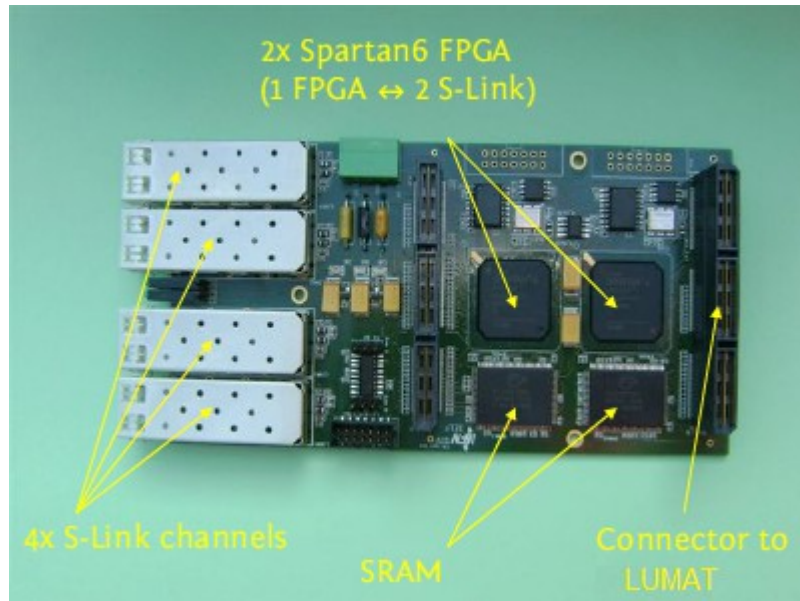
Figure 41: Receiver mezzanine

For a proper operation of all entities, a reset signal is needed in order to synchronize at the beginning all entities, to load default configuration parameter and to clean all the fifos and registers.

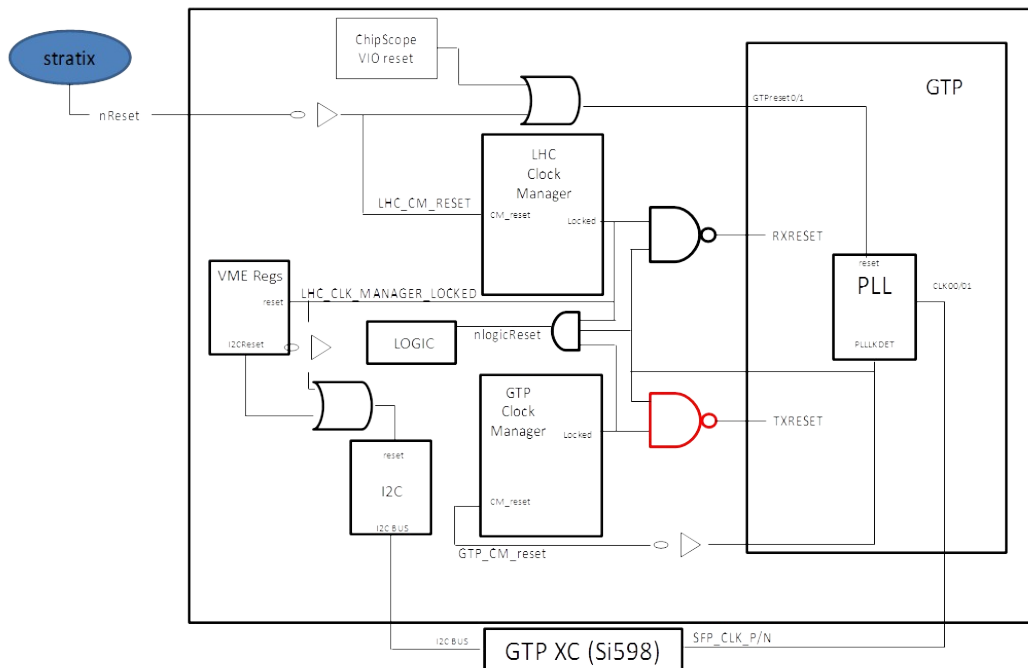The board's reset logic is designed as shown in the Figure 42

Figure 42: Block diagram of Reset way

Incoming reset signal from the Stratix mezzanine is provided in input to all entities.

In addition to the external signal, it is possible to reset the receiver mezzanine logic through a JTAG entity managed by the Xilinx Chipscope software (for debug purposes).

It takes about 1 ms after a reset signal for the PLLs to be stable.

5.6 Stratix scheme

Stratix board is LUMAT's central mezzanine, to which the digital signals coming from receive mezzanine or simulator arrive; it represents the system's actual "elaborator".

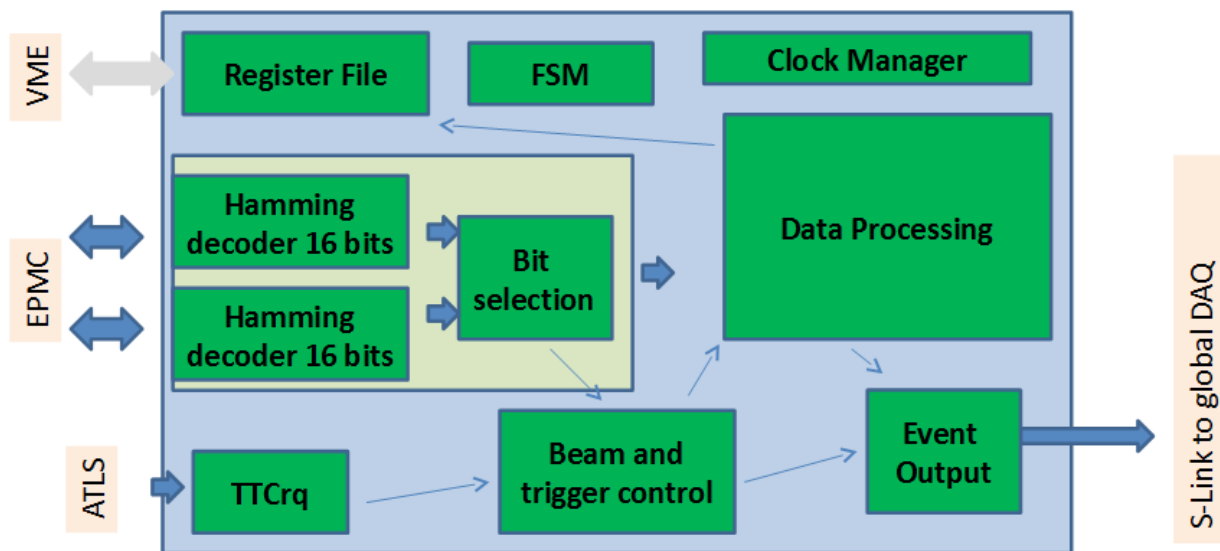The block diagram of Stratix firmware project, developed in VHDL, code is shown in Figure 43.

Figure 43: Block diagram of Stratix's firmware

The development of the project is quite linear; its entities are outlined below:

- Main FSM;
- Beam and trigger control;
- Bit selection:
  - Hamming decoder,
  - FourBitSelection,
  - Spy Buffer;

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- ◦ Data Processing:
- ◦ DelayHitsSignal,
- Event out;
- Register file;
- Clock manager.

Their details will be described in following paragraphs.

The main Stratix II FPGA decodes the incoming hit and control patterns and selects the stream coming from the appropriate receiver mezzanine and FPGA, since a total of four input streams are connected to it.

5.6.1 Main FSM

The entity "Main FSM" contains the Finite State Machine that sets the function global state of the whole system. The state decision depends on the value of several signals ("nReset", "RunningBit", "l1accept"and "ECR") shown in Figure 44. The values of these signals are set using the registers in the entity "RegisterFile".

```vhdl
entity MainFSM is
  port (
    clk                 : in std_logic;
    nReset              : in std_logic;
    RunningBit          : in std_logic;
    l1accept            : in std_logic;
    EventCounterReset   : in std_logic;
    EnableOutputBit     : in std_logic;
    L1ID                : out L1ID_t;
    EnableOutput        : out std_logic;
    State               : out std_logic_vector(1 downto 0)
    );
end MainFSM;
```

Figure 44: Main FSM Entity

The "Main FSM" decides the state transition, changing it from the configuration state to Runnig data and vice versa.

The "Main FSM" output is a signal called "State" (representing the state of the system), and its values are shown in the following Table 5

State	Value
00	Idle
01	Running
10	Stopping

Table 5: Main FSM state

5.6.2 Bit Selections

The VHDL entity "HitSelection" is shown in Figure 45 and its main role is to receive and decode data sending from receive mezzanine boards.

```vhdl
1  entity HitSelection is
2    port (
3      clk                 : in std_logic;
4      nReset              : in std_logic;
5      -- configuration from register file
6      EpmcSelection       : in std_logic;
7      FPGASelection       : in std_logic;
8      SpyBufReg           : in SpyBufReg_t;
9      -- running information (for spybuffer)
10     MonitoringBit       : in std_logic;
11     LBStart             : in std_logic;
12     -- All Hits from all EPMC outputs
13     HitsIn              : in Hit_v;
14     --     -- selected 4 pmts
15     PmtA4Out            : out std_logic_vector(3 downto 0);
16     PmtC4Out            : out std_logic_vector(3 downto 0);
17     -- selected 4 fibre
18     FibreA4Out          : out std_logic_vector(3 downto 0);
19     FibreC4Out          : out std_logic_vector(3 downto 0);
20     Orbit               : out std_logic;
21     L1Accept            : out std_logic;
22     ECR                 : out std_logic;
23     -- Spy Buffer output
24     SpyBufferOut        : out Hit_t;
25     errorCounters       : out errorCounters_v
26   );
27 end entity HitSelection;
```

Figure 45: HitSelection entity

The input data "HitsIn" contain all possible sources of data while in practice only one FPGA in one of the input mezzanine will be active. The data from the active mezzanine FPGA will be selected in this entity and the data will be divided in data from side A and

side C (Figure 46).

```vhdl
1   process(clk,nReset) is
2    begin
3      if nReset='0' then
4          HitsIn_int <=(others=>(others=>'0'));
5      elsif rising_edge(clk) then
6          HitsIn_int <= HitsIn;
7      end if;
8    end process;
9    selectionA <= EpmcSelection & FPGASelection;
10   selectionC <= EpmcSelection & FPGASelection;
11   with (selectionA) select
12       CodedHitA <= HitsIn_int(0)(hit_size-2 downto 1) when "00",
13                    HitsIn_int(2)(hit_size-2 downto 1) when "01",
14                    HitsIn_int(4)(hit_size-2 downto 1) when "10",
15                    HitsIn_int(6)(hit_size-2 downto 1) when "11";
16   with (selectionC) select
17       CodedHitC <= HitsIn_int(1)(hit_size-2 downto 1) when "00",
18                    HitsIn_int(3)(hit_size-2 downto 1) when "01",
19                    HitsIn_int(5)(hit_size-2 downto 1) when "10",
20                    HitsIn_int(7)(hit_size-2 downto 1) when "11";
```

Figure 46: Input signal selector

The signal values of "selectionA" and "selectionC" depends on the recorded values "EpmcSelection" and "FPGASelection"set by VME bus at the address "A_PMTSEL" (0x830) bit 16 and 17. The last two allow to select receiver mezzanine and FPGA from which is possible to sample the incoming data from optical link.

The selected data "CodedHitA" and "CodedHitC" are sent to another entity that decodes the Hamming Code.

VHDL entity "secded_decoder", is recalled for each channels referring to the side A and side C of the detector as shown in Figure 47

The main jobs of VHDL entity "secded_decoder" are to decode and correct eventual mistakes on the incoming data from the receiver mezzanine boards ("CodedHitA" e "CodedHitC"). The error signals "errorA" and "errorC" are connected to a registers in the entity "RegisterFile".

```
 1      DecodeA: secded_decoder
 2  ⊟       port map (
 3              clock        => clk,
 4              nReset       => nReset,
 5              datain       => CodedHitA,
 6              decodedData  => HitA16,
 7              syndrome     => syndromeA,
 8              error        => errorA
 9          );
10      DecodeC: secded_decoder
11  ⊟       port map (
12              clock        => clk,
13              nReset       => nReset,
14              datain       => CodedHitC,
15              decodedData  => HitC16,
16              syndrome     => syndromeC,
17              error        => errorC
18          );
```

Figure 47: Port map of secded_decoder for side A and C

The decoded output signals "HitA16" and "HitC16" contain:

- bits 0 to 11 values of PMT or Fiber sensors (only 8 are actually used in a given LUCROD);
- bit 12 control signal "Orbit";
- bit 13 control signal "L1Accept";
- bit 14 control signal "ECR".

Twelve bits on PMTs or Fibers side A and Side C are sent in input to another VHDL entity "FourBitSelection", shown in Figure 48.

The entity "FourBitSelection" is replicated four times (twice for the PMT signal and twice for the Fiber signals). Its main role is to select four input bits ("SelectedPMTHits") among twelve, based on the mask set on signal "BitSelection".

PMTs output signals are"PmtA4Out" and "PmtC4Out" and for Fibers are "FibreA4Out" and "FibreC4Out".

```
1   entity fourBitSelection is
2     port (
3       clk    : in std_logic;
4       nReset : in std_logic;
5       -- Configuration from register file
6       BitSelection : in std_logic;
7       -- All 12 bits from upper level
8       AllPMTHits   : in std_logic_vector(11 downto 0);
9       -- Selected 4 pmts
10      SelectedPMTHits : out std_logic_vector(3 downto 0)
11    );
12   end entity fourBitSelection;
```

Figure 48: FourBitSelection entity

Furthermore, an important component called "Spy-buffer" is defined in "HitSelection". It is used to control data flow of different entities in output during the debug. A SpyBuffer entity stores the last hit patterns received making them accessible for VME read-out. A random access addressing is required to access the memory. SpyBuffer allows to get an immediate feedback of the hit patterns behavior.

It is a component based on a group of Dual Port Ram, and it allows to store the input stream of data in a circular buffer when instructed by a VME command register. The storage can be frozen at any time and the data can be extracted to inspect the actual data flow and to allow for a debugging of the components preceding or after the HitSelection. The freeze command can also be triggered in case of errors detected by the VHDL logic allowing further debugging possibilities.

5.6.3 Data Processing

VHDL entity "DataProcessing" shown in Figure 49 is the main elaboration entity for the Stratix board, it is composed by the several sub-entities shown below.

```
 1  ⊟entity DataProcessing is
 2  ⊟  port (
 3        clk                 : in std_logic;
 4        nReset              : in std_logic;
 5        -- Configuration from Registers
 6        ConfigReg        : in ConfigReg_t;
 7        HitsDelay        : in Delay_t;
 8        BCIdtoRead       : in BCId_t;
 9        HistIndex        : in HistoIndeces_t;
10        --input control signals
11        MonitoringBit    : in std_logic;
12        Orbit            : in std_logic;
13        BCid             : in BCid_t;
14        LBStart          : in std_logic;
15        localLBStart     : in std_logic;
16        -- input hits
17        PMTselectedA     : in std_logic_vector(3 downto 0);
18        PMTselectedC     : in std_logic_vector(3 downto 0);
19        FIBselectedA     : in std_logic_vector(3 downto 0);
20        FIBselectedC     : in std_logic_vector(3 downto 0);
21        BitSelection       : in std_logic;
22        SelectAlgorithm    : in std_logic;
23        -- Data Output
24        PmtInfo            : out DetData_t;
25        -- All Luminosity counters
26        AllPmtLumi       : out LumiCounters_rec;
27        histCountA       : out lumiCounter_t;
28        histCountC       : out lumiCounter_t
29      );
```
Figure 49: DataProcessing entity

Stratix input data are sent to another entity called "DelayHitsSignal", after the decoding and selection of needed signals.

The "DelayHitsSignal" are repeated twice, one for PMTs and one for Fibers. The PMTs receive in input the signals "input_4PmtA"and "input_4PmtC", while Fibers receive in input the signals "input_4FibA" and "input_4FibC".

The entities "DelayHitsSignal" added a programmable delay to the input data streams and produce the output signals called respectively "delayed_4PmtA", "delayed_4PmtC", "delayed_4FibA" and "delayed_4FibC".

The delayed signals of PMTs and Fiber are sent in input to the sub-entities "HitsCounter".

These sub-entities count the number of active bits between two rising edges of the input signal "LumiBlockStart". The output signals "PmtCountA", "PmtCountC", "FibreCountA" and "FibreCountC" of the entity contain a number of active PMTs and Fibers of previous lumi block.

Finally, counting values and delayed input signals are sent to a fundamental entity called "algoritmi" shown in Figure 50.

```vhdl
1   entity algoritmi is
2     port (
3       clk                : in std_logic;
4       nReset             : in std_logic;
5       -- differential configuration
6       raddress           : in BCid_t;
7       enableHistogr      : in std_logic;
8       histBin            : in natural range 0 to 48;
9       histType           : in natural range 0 to 7;
10      -- input data to process
11      LBStart            : in std_logic;
12      myLBStart          : in std_logic;
13      PMTselectedA       : in std_logic_vector(3 downto 0); -- delayed_4PmtA
14      PMTselectedC       : in std_logic_vector(3 downto 0); -- delayed_4PmtC
15      FIBselectedA       : in std_logic_vector(3 downto 0); -- delayed_4FibA
16      FIBselectedC       : in std_logic_vector(3 downto 0); -- delayed_4FibC
17      na_Pmt             : in HitCount_t; -- to_integer(unsigned(PmtCountA))
18      nc_Pmt             : in HitCount_t; -- to_integer(unsigned(PmtCountC))
19      na_Fib             : in HitCount_t; -- to_integer(unsigned(FibreCountA))
20      nc_Fib             : in HitCount_t; -- to_integer(unsigned(FibreCountC))
21      BitSelection       : in std_logic;
22      SelectAlgorithm    : in std_logic;
23      bcid               : in BCid_t;
24      LumiOut            : out LumiCounter_a;
25      counts             : out lumiCounter_t;
26      myLumiOut          : out LumiCounter_a;
27      myCounts           : out lumiCounter_t;
28      diffLumiCounts     : out lumiDiffCounter_a;
29      histCountA         : out lumiCounter_t;
30      histCountC         : out lumiCounter_t
31    );
32  end entity algoritmi;
```

Figure 50: Algoritmi entity

Then, its Firmware include declaration and connection of several sub-entities to calculate the values of luminosity with the integral and differential algorithms.

The main activity of this entity is to provide a proportional value of luminosity without calibration. As written in the previous chapters, in a particle accelerator luminosity is a fundamental parameter to characterize the machine performance and the stability conditions of the colliding beams.

Twelve different algorithms are performed in the Algorithm entity using the hit patterns received from the LUCROD boards, six per PMT type (two types) received by each LUMAT board, with sixteen additional single-channel algorithms available for debugging and specific measurements through VME configuration, as shown in Table 6. The used set of algorithms is established through database configuration at the beginning of a data taking phase.

Every algorithm is performed as a function of the BCID and is processed in parallel at every clock tick, storing it in the FPGA RAM blocks thanks to the operation pipelining: read the old value for plot data on an istogram bin,increment it if necessary, then store

the updated value.

Algorithm	Function	Hits
EventOR	OR	$\geq 1/\text{side}$
EventAND	AND	$\geq 1/\text{side}$
EventORA	OR	≥ 1 on side A
EventORC	OR	≥ 1 on side C
HitOR	OR	sum hits on any side
HitAND	OR	sum hits on any side
Single Channel	-	-

Table 6: The SM Higgs boson production cross sections or mH = 125 GeV in pp collisions, as a function of the centre of mass energy, √s [33]

In this way each bin is integrated over the LB duration. Actually two memory blocks are alternatively used for each algorithm: one is used to update the values measured in a LB, while the other contains the data collected in the previous LB that can be read through the VME interface. When a LB ends the ram block used till that moment is frozen and made available for VME reading and the other ram block is cleaned up and used to collect data for the next LB. This switch between the two ram blocks happens without any loss of a single hit clock. Each algorithm also has a version integrated over both all BCID's and the LB and another version integrated over BCID's but only on a shorter Δt = 2 s. This latter measurement is sent to the ATLAS and LHC control rooms and provides a first and quick online luminosity monitoring. An example of the luminosity algorithm histograms produced by the LUMAT board is displayed in Figure 51, taken from a 2015 physics run.
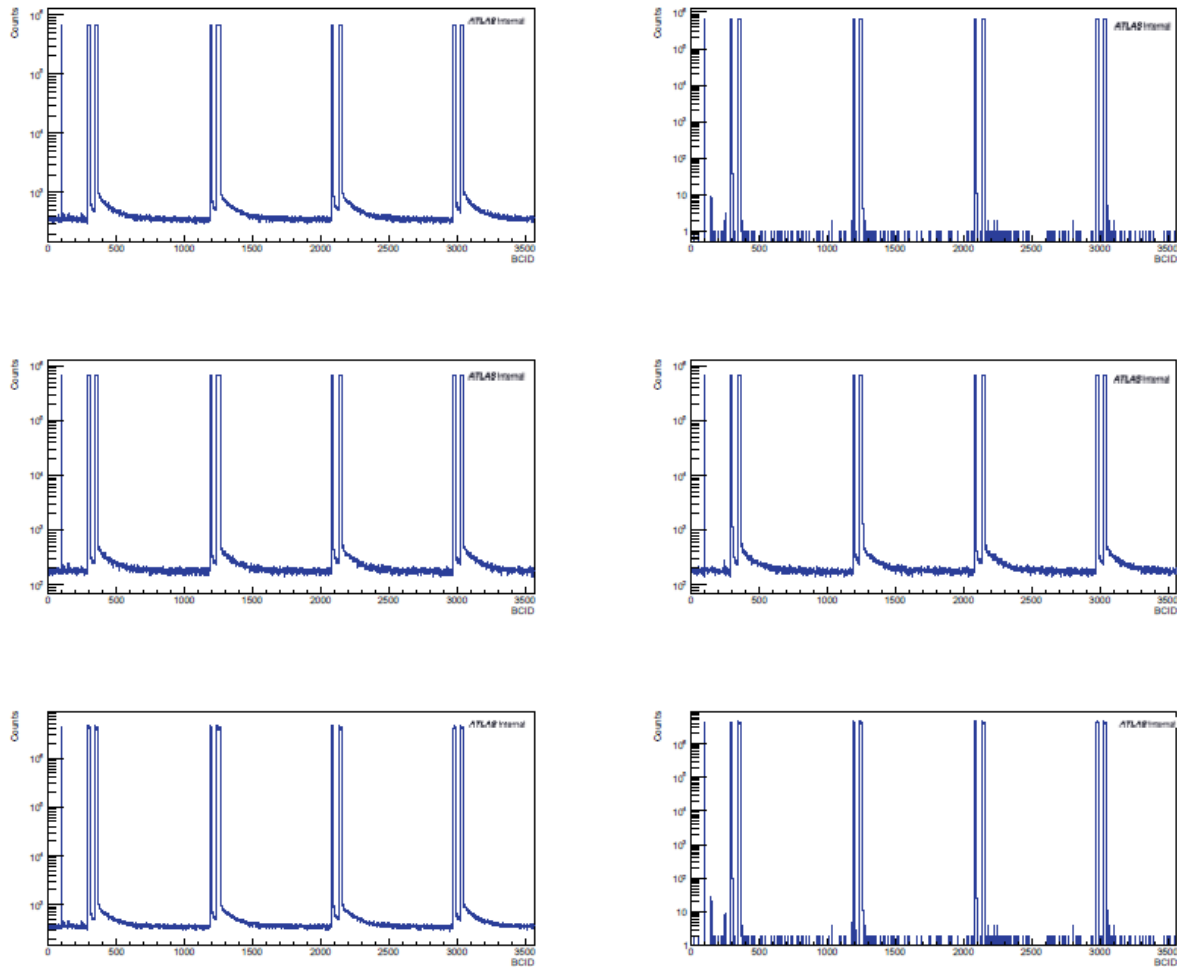
Figure 51: The output of the luminosity algorithms detailed in table six, in the same order, for the LUCID Bi-207 PMT's. The counts are measured as a function of the BCID number inside the same LB.

5.6.4 RegisterFile

The entity "RegisterFile" is developed to keep configuration parameters of the board and to monitor the board status. The Entity contains both read/write registers and read only registers that can be analyzed using the 32bit VME bus.

The most important registers are:

- "0000000" A_IOCONFIG to define the starting configuration of the LUMAT board;
- "0000001" A_LUMITIME to define lumiBlockPeriod and heartBeatPeriod;
- "0000010" A_DELAYS to define a delay for Hits, L1accept, Lumy Bloch and Orbit;
- "0000011" A_SLINKTTCRQ to define a configuration signals for TTCrq board;

- "0000101" A_SPYBUFFER to define configuretion and to read "SpyBuffer" component;
- "0000110" A_DetectorID;
- "0000111" A_RunNumber;
- "0001000" A_TriggerType;
- "0001001" A_FSM to define to set global state in "MainFSM" entity;
- "0001010" A_BCID;
- "0001011" A_PMTIDX;
- "0001100" A_PMTSEL mask registers to select data input in HitSelection.
- "0010000" A_VERSION to read the number vertion of Firmware;
- "0010001" A_DAQSPY to read information on acquisition state;
- "0010100" A_SPYBUF output register for Spy Buffer entity;
- "0010110" A_TRGS number of trigger receive;
- "0011100" A_L1ACCEPT number of l1accept receive;
- "0011110" A_LASTL1ID the number of last L1ID analyzed;
- "0011111" A_LASTBCIDS the number of last BCID analyzed;

The following list contains the registers to see the result of different algorithms:
- "0100000"A_Lumi0;
- "0100001"A_Lumi1;
- "0100010"A_MSB_0_1;
- "0100011"A_Lumi2;
- "0100100"A_Lumi3;
- "0100101"A_MSB_2_3;
- "0100110"A_Lumi4;
- "0100111"A_Lumi5;
- "0101000"A_MSB_4_5;
- "0101001"A_Lumi6;
- "0101010"A_Lumi7;
- "0101011"A_MSB_6_7;
- "0101100"A_Lumi8;
- "0101101"A_Lumi9;
- "0101110"A_MSB_8_9;

- "0101111"A_Lumi10;

The luminosity data consist of a total of 12 differential luminosity values for each BCID (3564 different sets of data) plus 12 LB integrated value and 12 integrated values for the quick monitoring of the beam. The data actually present in the registers depend on the values written in the read-only register A_BCID. Differential values are 32 bit words stored on single registers, while integral values are 48 bit words stored in pairs on three 32-bit registers.

5.6.5 TTC-RQ

VHDL entity "TTCrq" shown in Figure 52 is responsible of the interface between firmware and hardware mezzanine card called TTC-RQ (Time, Trigger and Control Receiver) [34] board.

```vhdl
entity TTCrq is
  port (
    Clk           : in  std_logic;        -- master clock
    nReset        : in  std_logic;        -- general reset
    -- To TTC
    toTTC         : out TTCReg_t;
    fromTTC       : in  TTCInfo_t;
    -- The following signals are copies of the  TTCRQ ones
    TTCData       : out  TTCInfo_t;
    TTCSpy0       : out std_logic_vector(31 downto 0);
    TTCSpy1       : out std_logic_vector(31 downto 0);
    -- The following signals go to/come from the main building blocks
    TTCReg        : in TTCReg_t
  );
end entity TTCrq;
```

Figure 52: TTCrq entity

A mezzanine card (TTCrq Figure 53) contains the TTCrx and the QPLL developed by the CERN microelectronics group.

Figure 53: TTCrq board

The main features are:

The on-board QPLL can be used as a jitter filter for the TTCrx clock or any external signal operating at the LHC frequency;

It can be mounted on a standard VME unit without imposing restrictions on the spacing between two VME modules;

Connectors J1 and J2 are fully pin compatible with those of the TTCrm (old board);

A third connector (J3) has been added to control the operation of the QPLL and for added functionality.

The board receives the 40 MHz main clock, diagnostic signals, trigger signal (L1accept) and control signals from ATLAS on optical fiber. The most important signal is "ID Bunch", it contains the identification number of Bunch used in the differential algorithms and "Orbit" that indicates the start beam.

5.6.6 Simulator

The system to manage the signal in input works when incoming data from PMTs arrive on front-end electronics. Input signals had to be simulated on the other end in order to test the board when real signals were not available, for example in debug state and during the shutdown period.

A component made to simulate the effects of the LHC collisions on the LUCID sensors has been created to test system and to detect eventual errors in the logic or in the connections.

The entity "RandomBit" simulates a single signal from a PMT, providing a zero or one value, based on a random number and a preset threshold value. The top Entity "beam_sim", renamed "RandomBit" entity several times, can generate signals compatible with the detector signals.

The beam of LHC is organized in 3564 bunch (Figure 54) that can be filled of protons or not. Two trains of bunches circulate in the accelerator in opposite directions. Every 25 ns two bunches collide head-on in the Atlas experiment, if both bunches are filled with protons, new particles can be produced rising the instantaneous luminosity.
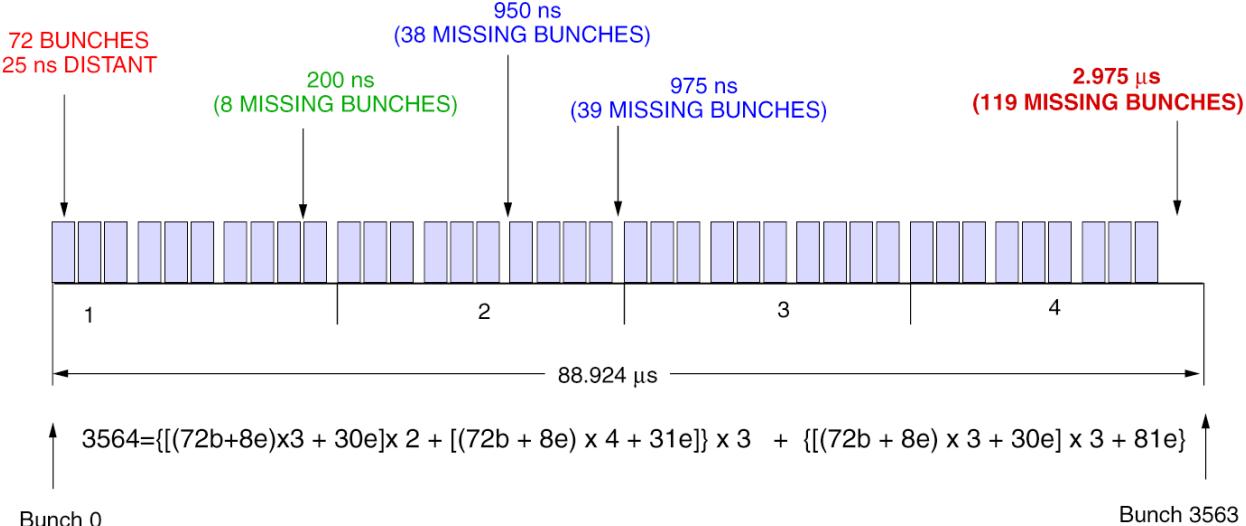

Figure 54: Beam LHC structure

Groups of filled bunches are interleaved with empty bunches in an aperiodic way. At the end of a structure there is an surplus of empty bunches that are used to identify the end of LHC cycle.

The simulator reproduces this situation with a little approximation, producing a hit sensor only when a filled bunch occurs or, *viceversa*, sending zero hit.

Furthermore, it is generated a signal called "Orbit" that indicates the start of a new cycle of beams in the simulated accelerator.

5.7 From counts to luminosities

The measurement of the luminosity with an accuracy at a level of few percent requires a detailed analysis of all the different elements that enter into the measurement and in order to convert the counts recorded by the LUMAT board into a luminosity.

By the definition the istantaneous luminosity links the interaction rate with the inelastic proton-proton cross section:

$$R = \mathscr{L}\,\sigma_{inel}$$

Since the instantaneous luminosity in an accelerator can be defined even for very short

period of times, it is possible to define it at a bunch crossing level, i.e. for periods of length, providing in this way the istantaneous luminosity of a specific BCID. During the turning of the LHC beam it is possible to observe that each BCID has a specific luminosity depending on the number of particles in the colliding bunches and on the lateral sizes. The number of interactions (Ni) that happened in a specific BCID during a given luminosity block LB composed by Nturns of the beam can be evaluated as:

$$N_i = N_{turns} \mathscr{L}_i \sigma_{inel} \Delta t$$

where $\mathscr{L}_i$ is the istantaneous luminosity of the BCID number i. On average at every turn of the beam during the bunch crossing there are $\mu_i = N_i / N_{turns}$ collisions in the detector. If a fraction ϵ of the collisions give rise to a recorded event in LUCID, it is possible to count the recorded events N_i^{rec} in a LB and relate them to the average number of interactions as:

$$N_i = N_i^{rec} / \epsilon$$

and from this extract the number of average number of collisions per BC and the luminosity:

$$\mu_i = N_i^{rec} / (N_{turns} \epsilon)$$

$$\mathscr{L}_i = N_i / (N_{turns} \sigma_{inel} \Delta t) = \mu_i / (\sigma_{inel} \Delta t) = N_i^{rec} / (\epsilon N_{turns} \sigma_{inel} \Delta t)$$

Once the luminosities in each bunch crossing have been evaluated, it is possible to have the beam averaged istantaneous luminosity over all the 3564 bunches:

$$\mathscr{L} = (\Sigma_i \mathscr{L}_i) / N_{bunches}$$

and at the end the integrated luminosity in an LB:

$$L = \int_0^t \mathscr{L}(t') dt' = N_{turns} (\Sigma_i \mathscr{L}_i) \Delta t \quad .$$

The different algorithms developed for measuring the luminosity contains different definition of what is a recorded event. From the different definitions it is possible to

extract luminosity estimations with different level of background or accuracy.

The most straitforward way to measure the luminosity is to rely on the so called *zero-counting* method which foresee to count empty events. If in a detector an average of μ events are expected at each bunch crossing, the probability of counting exactly 0 events is given by the poisson distribution and is

$$P(0) = \frac{N_0}{N_{tot}} = e^{-\mu\varepsilon} \rightarrow \mu = -\ln\left(\frac{N_0}{N_{turns}}\right)/\varepsilon$$

so simply by counting the empty events in a given BCID in a sample of Nturns of the beam it it possible to evaluate the μ value (knowing the efficiency) and from that the luminosity.

Since there are two independent sides of the LUCID detector, called A and C, it is possible to count empty events separately in side A and C and then to combine them. This is done for example with the *zero_and* method where asking for no hit in the A side and no hit in the C side, we can evaluate the fraction of empty events and hence their mu value as:

$$P(0) = e^{-\mu_A\varepsilon_A} e^{-\mu_C\varepsilon_A} \approx e^{-2\mu\varepsilon} \rightarrow \mu = -1/2\ln(N_0/N_{turn})/\varepsilon$$

which holds only in the limit where the two sides have approximately the same efficiencies and acceptances. This method, working on the coincidence of two far away detectors is practically background free.

Another method employed is the so called *hit_or* one where it is asked that at least one of the sides sees an empty event. In this case, with similar definition of all symbols, the fraction of empty events and the average number of interactions are given by:

$$P(0) = e^{-\mu_A\varepsilon_A} + e^{-\mu_C\varepsilon_C} - e^{-\mu_A\varepsilon_A} e^{-\mu_C\varepsilon_C} \approx 2e^{-\mu\varepsilon} - e^{-2\mu\varepsilon} \rightarrow \mu = -\ln\left(1 - \sqrt{1 - \frac{N_0}{N_{turns}}}\right)/\varepsilon$$

The three previous methods rely on the fraction of empty events and can be usable if there are enough empty events to make the measurement statistically significant. When the luminosity reaches the peak of the RUN 2 foreseen conditions and the average number of interactions is above 30, we enter in a so-called *zero starvation regime*, where there are so few empty events in a LB that the methods above are not usable. In this case we rely on the *hit counting method*, i.e. Counting the PMTs that have been hit by a charged particle. The average number of hit PMTs is proportional to the average number of collisions happened in a given BCID and hence to its luminosity. The proportionality

coefficients are evaluated via a Monte Carlo simulation and checked with special runs, called van der Meer scans.

5.8 Result and LUCID calibration

The LHC was turned on after the shut-down period in April and LUCID successfully registered the first events, showing its capability of measuring the luminosity on a bunch-by-bunch basis. In August 2015 took place the luminosity calibration using the van der Meer scans technique: two opposite bunches are initially non-colliding and are overlapped by small increments till the maximum superimposition is achieved. Figure 55 shows the scan shape as measured by the LUCID detector, together with the background processes involved.
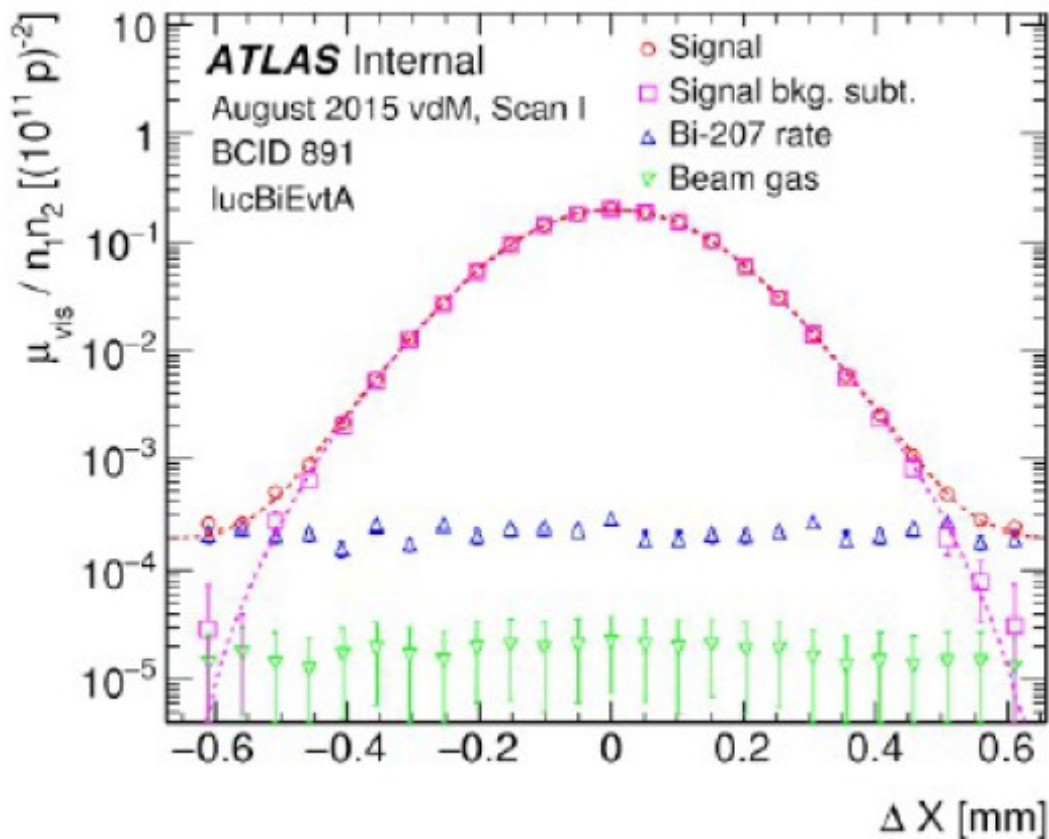

Figure 55: Visible interaction rate for the LUCID algorithm LUCORD Bi-207 Event AND, that provides the ATLAS luminosity, in one bunch crossing and per unit bunch population, versus nominal beam separation during horizontal scan 1 in the August 2015 luminosity-calibration session. The background is dominated by random counts from the radioactive Bismuth source used for phototube gain calibration (blue triangles), as estimated from the rate measured in the preceding unfilled bunch slot. The background subtracted rate is fitted by a Gaussian multiplied by a sixth-order polynomial (dashed curve). The error bars are statistical only.

The calibration is the main component of the uncertainties in luminosity determination: Table 6 summarizes the main contribution to the systematic uncertainty on luminosity measurements. A 3.8% uncertainty is assigned to the van der Meer calibration based on the August 2015 scans. The largest contributions arise from the precision of the length scale calibration determined by measuring the displacement of collision vertices reconstructed in the inner detector, the estimation of potential non-factorization biases during beam-separation scans, the scan-to-scan reproducibility of the visible cross sections of the LUCID algorithms, orbit drifts measured by the beam position monitors during the scans and corrections for beam-beam effects. Sources of uncertainties leading to sub-percent errors, such as the bunch population product (0.3%) are not listed in the table, but are included in the total uncertainty. A 3.2% uncertainty is assigned to the luminosity monitoring throughout the data taking. This error is dominated by the run-to-run consistency of luminosity measurements comparing LUCID bunch-by-bunch rates, bunch-average particle flux monitoring in the calorimeters and track counting in the inner detector. Another significant component is the estimated upper limit on the calibration transfer correction, i.e. the change of the LUCID response between the low-luminosity regime of van der Meer scans and the high-luminosity data taking conditions.

Source	Uncertainty [%]
van der Meer calibration	3.8
Dominant components:	
Length scale calibration	2.1
Non-factorisation effects	2.0
Scan-to-scan reproducibility	1.4
Orbit drifts	1.2
Beam-beam effects	1.0
Luminosity monitoring	3.2
Dominant components:	
Run-to-run consistency	2.5
Calibration transfer	2.0
Total luminosity uncertainty	5.0

Figure 56: Total uncertainty on the preliminary luminosity determination inthe 2015 proton-proton dataset at √s = 13 TeV.

The integrated luminosity measured by the LUCID detector is compared with the measurement of other detectors to test the stability of all luminometers in 2015. The calorimeter (Tile, FCal, EMEC) and track counting algorithms are cross-calibrated to a

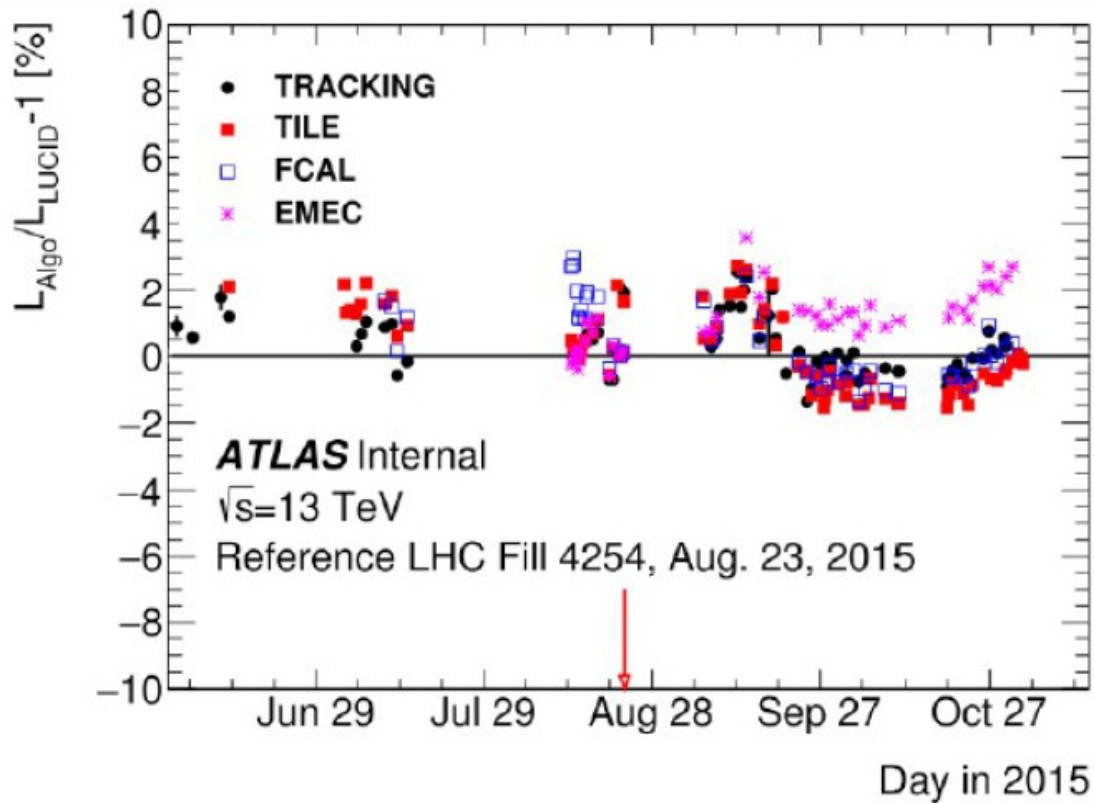LUCID measurement of the integrated luminosity in a reference fill, as shown in Figure 57

Figure 57: Run-to-run stability of ATLAS luminometers for the 2015 proton-proton dataset at √s = 13 TeV, excluding dedicated low luminosity data taking periods

Each point shown in Figure 57 is the mean fractional difference in integrated luminosity for a single ATLAS run, between the indicated algorithm and the reference LUCID luminosity algorithm.

The main features of the LUCID detector are fully functional and have already proven to be working correctly. New features and improvements are under development to provide better linearity of the luminosity measurements and additional information to the ATLAS detector.

Since the start of the 2015 data-taking, LUCID has been the official ATLAS luminosity monitor, thanks to its precise measurements, its fast response and its reliability, obtained through an intrinsically fast and redundant system, continuous calibration, fast electronics and functional control systems. We expect it to remain essential throughout the whole RUNII data-taking thanks to the continuous work put into it by the LUCID team.

The second part of my PhD activity took place at Marposs company. Marposs produces a large amount of measurement and process control solutions. My research activity concerned the optical metrology field.

Chapter 6

MARPOSS

6.1 Company

Marposs was established in Bologna in 1952 by Mr Mario Possati (1922-1990) [35].

The firm's concept was to innovate electronic gauging equipment's production for grinding.

New technologies and electronics allowed a massive improvement in performance when compared to existing products.

Research and testing phases were needed to ensure the demanded overall reliability, but soon after the end product fulfilled expectations and was successfully introduced in the market.

In the early sixties, as well as consolidating its sales presence, Marposs acquired the necessary structural strength to confidently look at future developments.

Then as now, Italy still exports a huge quantity of machine tools, making Marposs become even more committed to guarantee technical and after-sales support directly within the importing countries.

Therefore the company established offices in a number of foreign countries, as Germany (1962), Switzerland (1963) and United States (1963), reaching Japan and the Asian market in 1970.

These countries still represent, along with China, the company's most important markets.

Since its establishment, Marposs has been producing standard and custom systems for industrial measurement as dimensions, geometries and surface quality control of mechanical components, and for production's process monitoring. Marposs engineers relate to both end users and machine tool makers, from the project's development stage through implementation and long-term service support. Application solutions are obtained with standard or engineered products and cover all requirements, from the immediate control of the machine tool, to the final inspection of the final pieces and to the collection and statistical interpretation of the measurement data.

Marposs is a world leader with global capabilities in Research & Development, Production, Marketing, Sales, Customer Training and After-Sales Service.

Marposs adheres to Quality principles and is committed to the continuous improvement of procedures and methods, as well as the adoption of new and most suitable methods for the analysis, engineering, production, control and assistance of all its products and services.

Marposs' expertise allows its customers to reach their goals in product quality, efficiency, flexibility, productivity, reliability and maintainability of the manufacturing process, regardless of their company size.

Figure 58: Marposs S.P.A

6.2 Mission and philosophy

Marposs' mission is to provide precision metrology equipment designed for the workshop environment during and after machining operations.

Marposs supplies several types of products ranging from individual gauging component to turnkey machines or fully automated lines to provide global solutions to customers' needs, supplying the metrology equipment in association with non-destructive testing, leak testing and a wide variety of sensors and machine tool controls.

The company has become a world leader in measurement technology by offering its customers a combination of advanced products, market knowledge and commitment to long-term global partnerships. Building on these foundations, Marposs has created an international organization able to deliver application, design and service support virtually anywhere in the world.

Marposs pays the utmost attention to customer satisfaction. The company deploys economic and human resources and carries out its best commitment to offer top quality innovative products and applications, all developed in close cooperation and in simultaneous engineering with its customers.

Figure 59: Marposs applications

6.2 Worldwide organization

Marposs now boasts its own Sales and Technical Support companies in twenty-four countries with eighty offices. A further nine countries benefit from dedicated networks of Agents and Dealers.
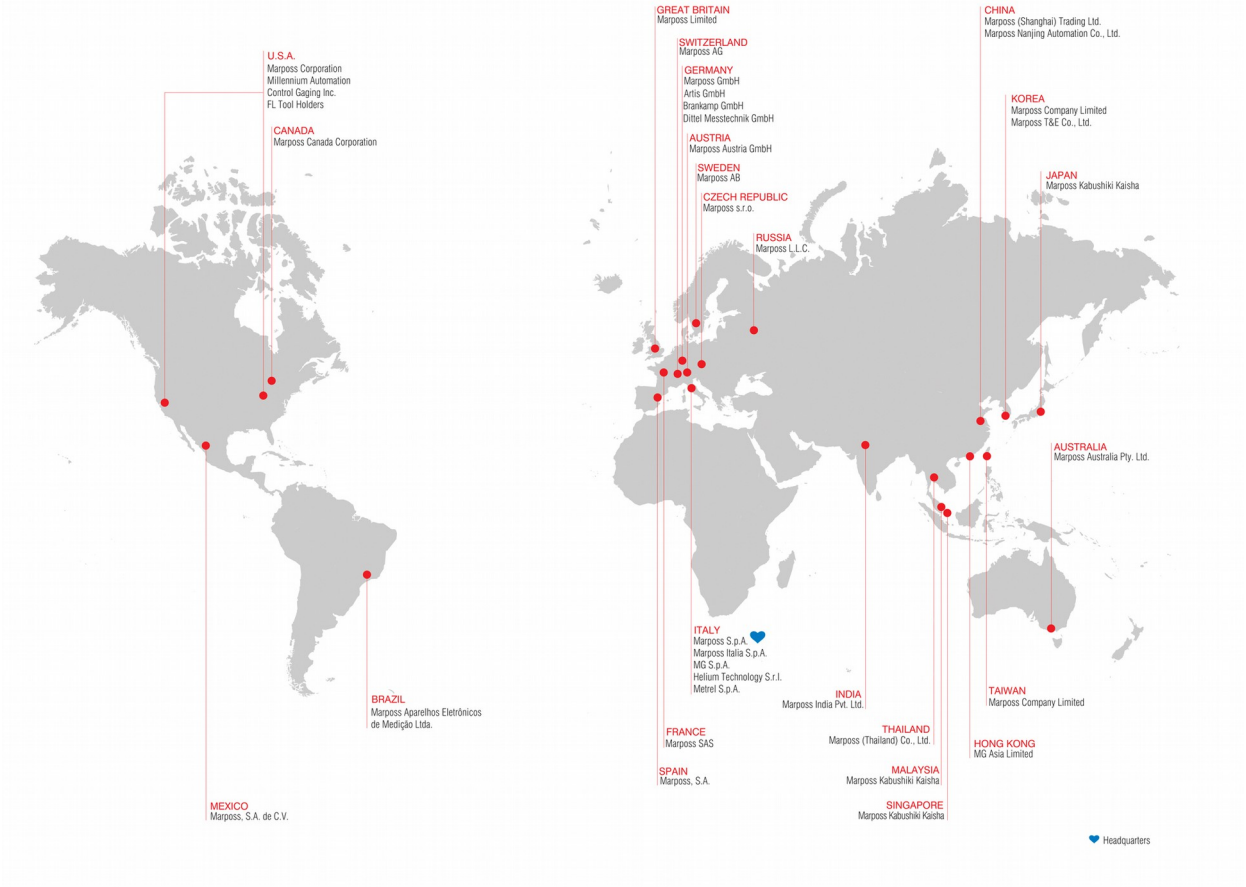

Figure 60: Wordwide organization

6.3 Market segments

Marposs supplies precision gauging equipment to industries worldwide.

About 94% of the production is intended for export purposes, mostly, but not only, to countries with a solid technological tradition of their own.

Main customers are:

- Machine tool makers selling machines already equipped with gauging systems
- Gauge makers
- End users:
  - AUTOMOTIVE AND SUPPLIERS: engine & transmission car body;
  - OTHER MANUFACTURING: bearing & gear compressor electric motor;
  - INJECTION: sub-micron applications;
  - GLASS: automotive, architectural & furniture, food & beverage and cosmetics & pharmaceutical;
  - AEROSPACE;
  - ENERGY: renewable energy and oil drilling;
  - HI-TECH: computer, hard disk and mobile;
  - BIOMEDICAL: orthopedic.

Products and applications:

- MACHINE TOOL APPLICATIONS:
  - In-process and post-process part inspection
  - Machine tool control and process monitoring
  - Part and tool probing
  - Tool setting and monitoring
- GAUGING COMPONENTS:
  - Mechanical and electronic components
  - Modular benches made up of components
  - Embedded and industrial computers
  - Data acquisition systems and SPC software
  - Masters

- MANUAL AND SEMI-AUTOMATIC GAUGES
  - Hand held gauges
  - Benches
  - Gauges by attributes (go - no go)
  - Fixtures
  - Dog-house gauges
- AUTOMATIC MACHINES
  - Dimensional and geometric inspection
  - Gauging for assembly
  - Non-destructive testing
  - Leak testing and functional checks

Figure 61: Optoquick SET

6.4 Corporate structure

The headquarters facilities are in Bentivoglio, about ten kilometers north of Bologna, Italy.

The headquarters consists of three factories set side by side (showed in the Figure 62), plus other service buildings (an internal restaurant and technological centers).

Figure 62: Headquarters of Marposs

The total covered space measures 38 000 sq.m., surrounded by 30 000 sq.m. of gardens plus yards and parking lot.

Internal to the main facility are 14 green, open-air atriums that are each 100 sq.m. in size. These areas work to enlighten and decorate the office area.

The working area is an open architecture without fixed dividing walls. This concept facilitates easier area reconfiguration according to changing needs.

The manufacturing organization in the headquarters has two major components:

- the Product Manufacturing Center which produces standard equipment;
- the Special Application Manufacturing Center, which produces customized systems to be integrated into customers' facilities.

Both Manufacturing Centers work in close cooperation with the R&D department (where I performed my PhD activity) and with the three commercial divisions:

- the Machine Tool Division operates in the world of measurement and control on machine tools

- the Standard Products Division works in the field of standard gauges and components for the gauge makers

- the Special Applications Division covers the area of customized gauging stations (manual benches and automatic machines) tailored to the specific customers' requests.

Research and development are the lifeblood of the constant technological innovation that characterizes today's global manufacturing community.

Recognizing this, Marposs invests approximately 10% of its revenue in Research and Development and participates with a number of partners in international research programs.

My PhD thesis shows how the company's investment policy in highly qualified and specialized human capital can have a positive and substantial impact on advanced academic learning.

The productivity of these efforts is enhanced by many years of real-world experience which help Marposs to identify and pursue efficiently the most promising new technologies.

Marposs' Research and Development Centers synthesize the knowledge gained from both customer applications and Marposs' own internal operations and apply it to the ongoing basic research.

All Marposs gauging solutions (mechanical, air-electronic, contact-electronic, optical) have their origins in the Research and Development Centers, and so will the advanced new technologies which eventually will replace them.

This continuous improvement is necessary to allow Marposs to maintain its leadership in the world for gauging systems engineering.

Marposs also benefits from its unique laboratories:

Test lab (Figure 63): Testing of extreme environmental conditions, life test and material verifications are performed to ensure and improve the product quality. The Marposs Test Laboratory is qualified by the presence of a skilled staff, controlled environmental conditions and a variety of equipment like a scanning electron microscope (SEM) with EDS probe, several benches for endurance test (shakers) and reliability test (life test), climatic rooms for thermal and humidity

tests, a chamber for resistance to corrosion test and more specific systems.

Figure 63: Test lab

- **EMC test lab** (Figure 64): The electromagnetic compatibility (EMC) test lab can check the compliance with national and international standards and legal requirements. The lab is equipped with an anechoic room that allows compliance verifications at all the stages of a product development, especially during the design and production monitoring. Furthermore the lab cooperates with several certification organizations for what concerns radio emitting device validation.
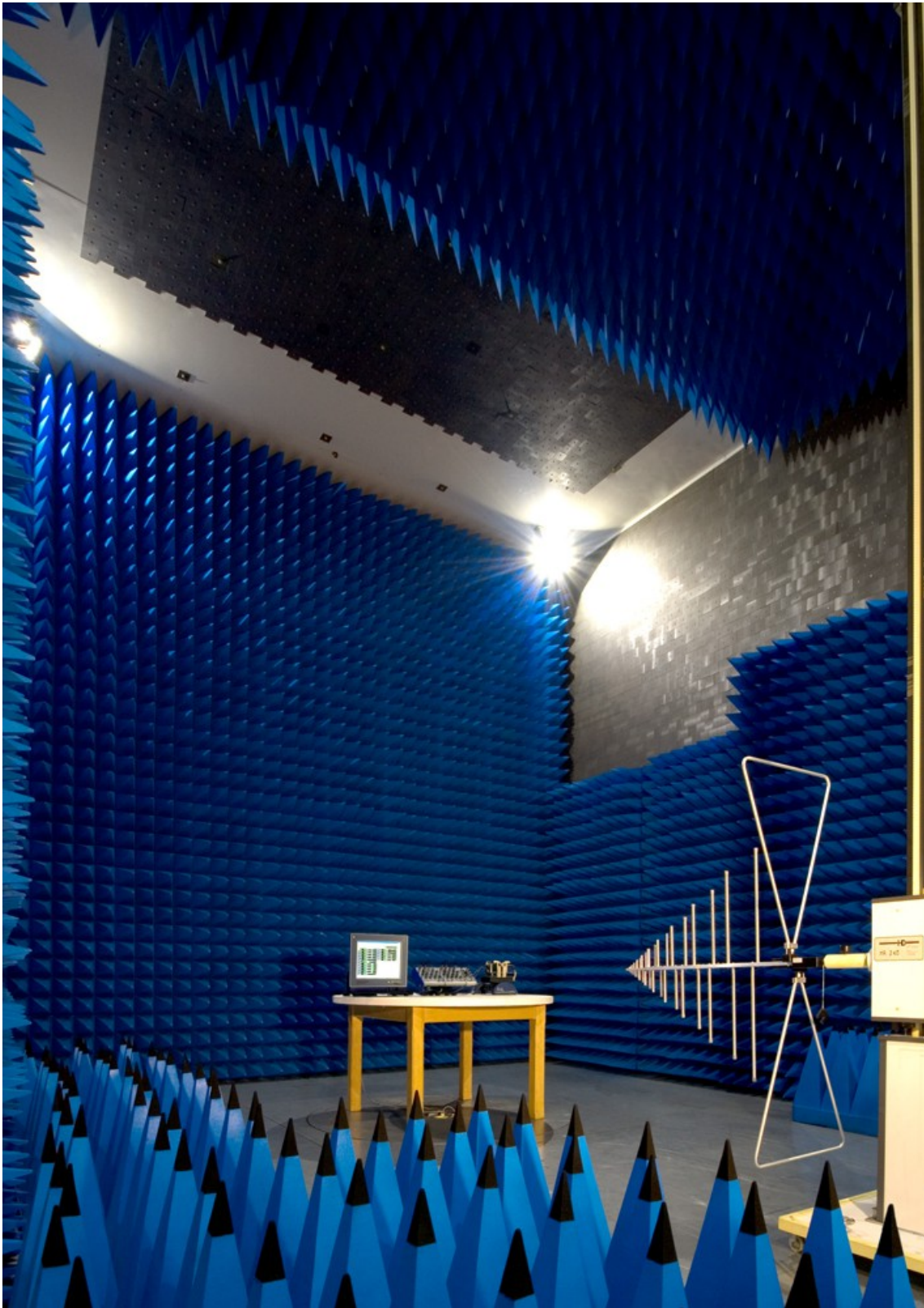
Figure 64: EMC test lab

- **Metrology labs** (Figure 65)**:** In its manufacturing sites Marposs has several metrology laboratories, accredited as calibration centers: the most important labs are in Marposs headquarters in Bentivoglio (150 sq. m.) and in MG manufacturing center in Brescia (three labs for a total of 440 sq. m.); also the recently established MNA manufacturing center in Nanjing has a well equipped 110 sq. m. lab. All the room floors are separated from the rest of the building and/or lay on anti-vibration bearings; the rooms are in a slight overpressure to keep dust out and are controlled within 20°C ± 0.3°C (or even ± 0.2°C in some labs) and relative humidity 50% ± 10%. The labs are equipped with 3D CMM's, height gauges, Abbe universal length measuring machines, roundness and shape measuring machines, CMM gear testing machines, master scanners, roughness and surface testers, durometers and other high precision instruments, all used to certify:

  ○ Reference standards (masters) used to calibrate Marposs gauges,

  ○ Sample parts used for metrological tests during the gauge run off,

  ○ Thread gauges, spline and master gears sold for go - no go checks.

Figure 65: Metrology labs

The provision for maintenance and maintenance support is a key element in ensuring the

dependability of items (products, equipment and systems) throughout their life cycle.

Intended functionality, capability and dependability performance are achieved by providing the necessary maintenance and maintenance support in conjunction with appropriate design (in terms of functionality, reliability and maintainability), quality manufacturing and sound operating practices.

Marposs after-sales organization is present all over the world in about 80 centers to be conveniently close to the customers' plants to minimize downtime of production lines; it accounts for approx 300 service engineers, mostly native, to assure the best possible understanding of customers' needs, qualified to provide the maintenance and maintenance support required.

Chapter 7

Optical measurement principles

7.1 Optical metrology

Automation is an increasingly important instrument for industrial process. Marposs offers innovative solutions that enable companies the perfect integration of optical metrology in their automatized processes.

Complete optical metrology automation ensures the following benefits:

- Greater efficiency in quality control

- Higher productivity

- Higher precision

- Significant cost reduction

Marposs offers the ideal automation solution to satisfy the highest quality control standards in the industrial field. Our solutions include reliable industrial hardware, process security software, and precise, effortless integration for every industrial area.

Today the megatrend in metrology is optical. This includes any non contact metrology device that uses light, laser, and sensing devices. In this period the automotive manufacturers face uncertain production volumes with roller coaster demand, up one year, down the next. There are also shorter production runs along with faster product development cycles. With part runs dropping into the 100,000s today from millions in the old days, manufacturers are striving to make their lines as flexible as possible. At the same time, there is a push for tighter tolerances, driven by everything from aesthetics for bodywork to better fuel efficiency in engines. Automotive manufacturers are competing on quality more than ever, driving advances in production metrology.

Marposs produces several types of optical metrology machines, used for measurement of several types of mechanical parts.

The advantages of optical metrology are many, for example:

- High speed of execution,

- no contact on the workpiece, so that it is possible to measure delicate pieces,

- possibility of differently shaped pieces' measurement.

However, the flexibility and speed of optical gauging offers an unparalleled tool for quality measurement and evaluation of complex parts as well as for manufacturing process control.

With systems based on optical metrology the following types of measurements can be performed:

- diameters (static or dynamic) of main bearings, pin bearings, flanges and their taper and roundness;

- distances and widths;

- check of grooves (minimum groove diameter, radius, width, position);

- radial TIR with respect to a mechanical or electrical axis;

- stroke;

- index.

By using a contact LVDT probe (optional), it is possible to perform an axial TIR check with respect to a mechanical or electrical axis.

The measurement of parts does require that they are in a clean and dry condition.

With Marposs' metrological solutions, the whole process chain analysis becomes an integral part of quality guarantee in production processes.

During my PhD activity at Marposs, I took part to a new FPGA-based linear camera's designing process, that I will describe in chapter 8.

The measuring principle is based on the shadow projection (described in the next paragraph) to detect and measure the outline of the piece. Camera, illuminator and synchronization system have been designed to measure long, round workpieces such as crankshafts, camshafts, and drive shafts.

These systems operate directly on the production field. In the Figure 66 are shown several examples of measured pieces:
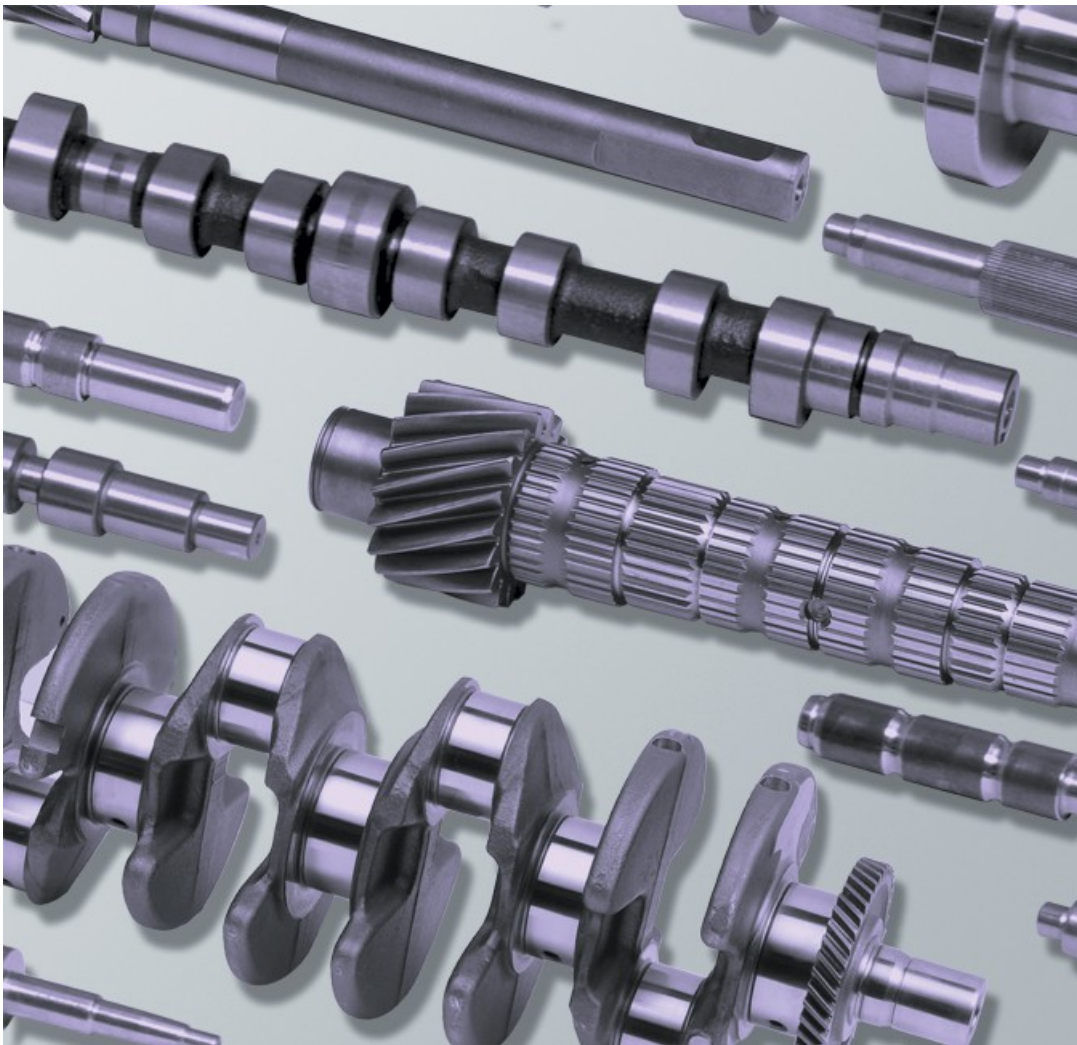
Figure 66: Example of measured pieces

One or more receiver-emitter couples are installed on several industrial applications with different purposes. Depending on the kind of pieces, cameras can be combined with several kinds of traditional contact and non-contact gauges to obtain an independent automatic system.

Optical sensors provide data of part and component geometries, as well as of three-dimensional displacements and deformations. Static and dynamic deformations are determined on the basis of individual points as well as entire surfaces.

With this data, manufacturers can evaluate part safety and functioning, while also optimizing their simulation and design processes at the same time. As a result, product development can be noticeably accelerated.

7.2 Shadow cast

The operating principle consists of projecting the shadow of the edges of the part to be measured onto a linear array of photodiodes (CCD) by means of a precisely aligned light beam [36]. The darkness-to-light and light-to-darkness transitions are located on the CCD sensor with subpixel resolution and correlated with the dimensional value of the dark area.

Effects from background environmental noise are eliminated by an optical filter accomplished by positioning a pinhole on the focal plane of the receiving lens [37].

Positions of edges are localized on darkness light transition of the projected luminous profile with a 0,1 µm resolution, as showed in the Figure 67
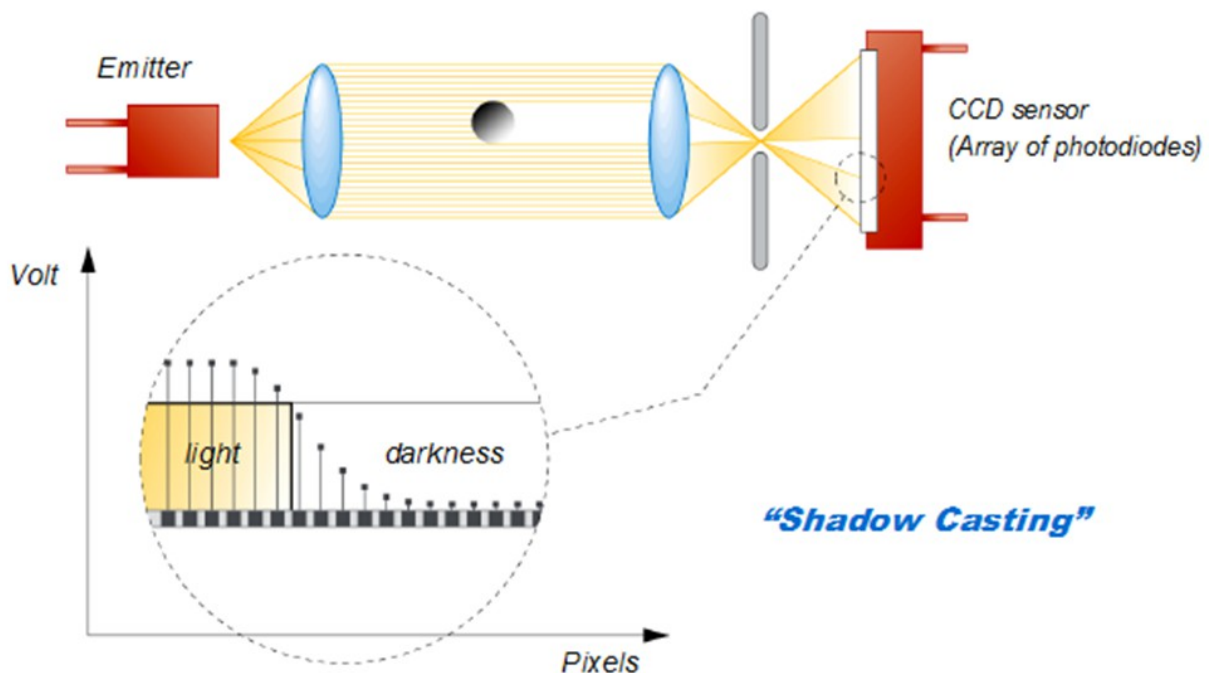
Figure 67: Shadow cast

A CCD probe is made of a receiver-emitter couple.The emitter includes the optical system that turns the almost hemispherical source into an almost parallel light beam. The beam intercepts the piece, casting a shadow on the receiver, as shown in the picture.

The receiver filters wavelength and non-parallel beams, recreating the image on a plane, where the CCD sensor converts light signals into electric signals, destined to a further processing.
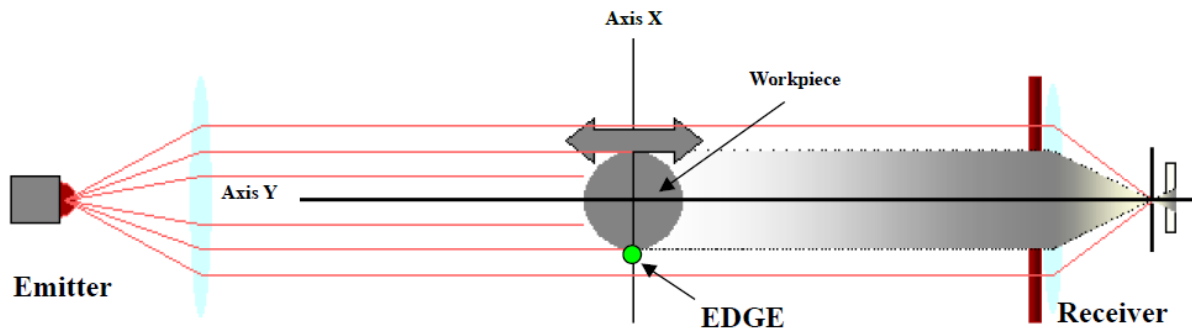
Figure 68: Axis of system

The receiver is made of a linear CCD of approximately 8200 pixel, each sized 7 μm, corresponding to about 8 μm on the X focal plane of direction.

In the image every visible edge will be located exactly along borders between neighboring pixel. After interpolating the edge profile, the likeliest of the true edge position is given by the inflection point of the interation function

The position of light intensity transition **(EDGE)** is determined with sub-pixel algorithms [38] with a resolution of a twentieth of a pixel.
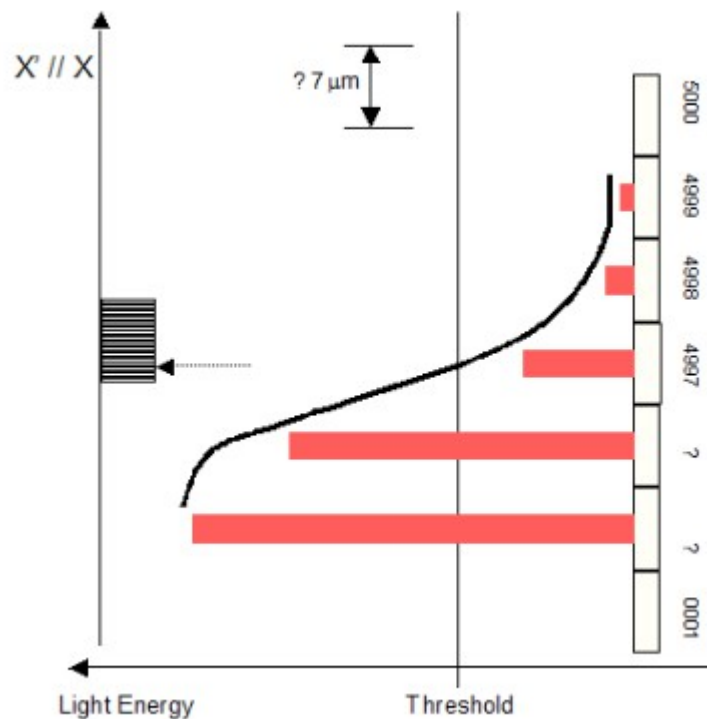
Figure 69: Example of edge profile

In fact, the sensor can be described as an "optical ruler" which allows the piece's diameter measurement; it can also be compared to a plain probe measuring in axis X direction.

7.3 Setup system

As shown in Figure 70 with a single system composed of emitter and camera it is possible to measure small diametered pieces, up to 55 mm using multiple cameras as shown in Figure 71 it's possible to measure larger pieces up to 200 mm.
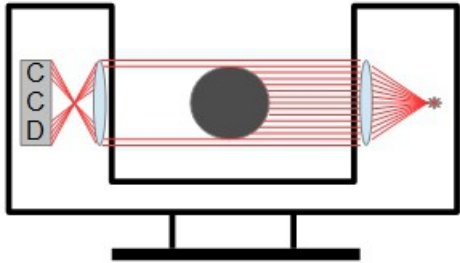

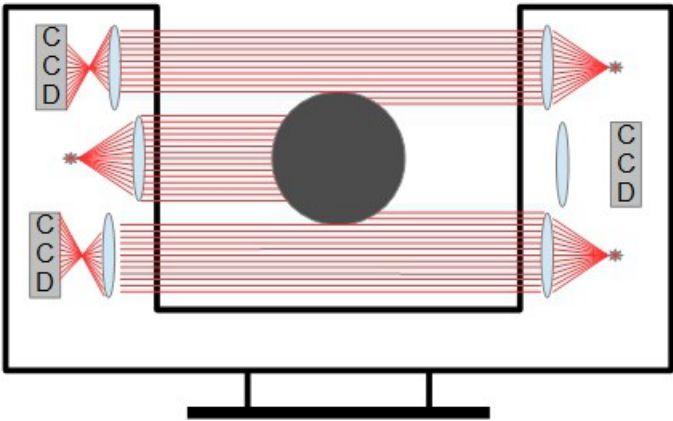*Figure 70: Single system emitter and camera*

Figure 71: Multiple cameras

The problem using multiple cameras is that this system requires a synchronization. Synchronization is provided by the Gagepod OQS external device.

The scanning can be activated by time-based or space-based triggers by Gagepod OQS source, that synchronizes the cameras and the incremental optical transducers, which control the movement axis of the measuring machine.

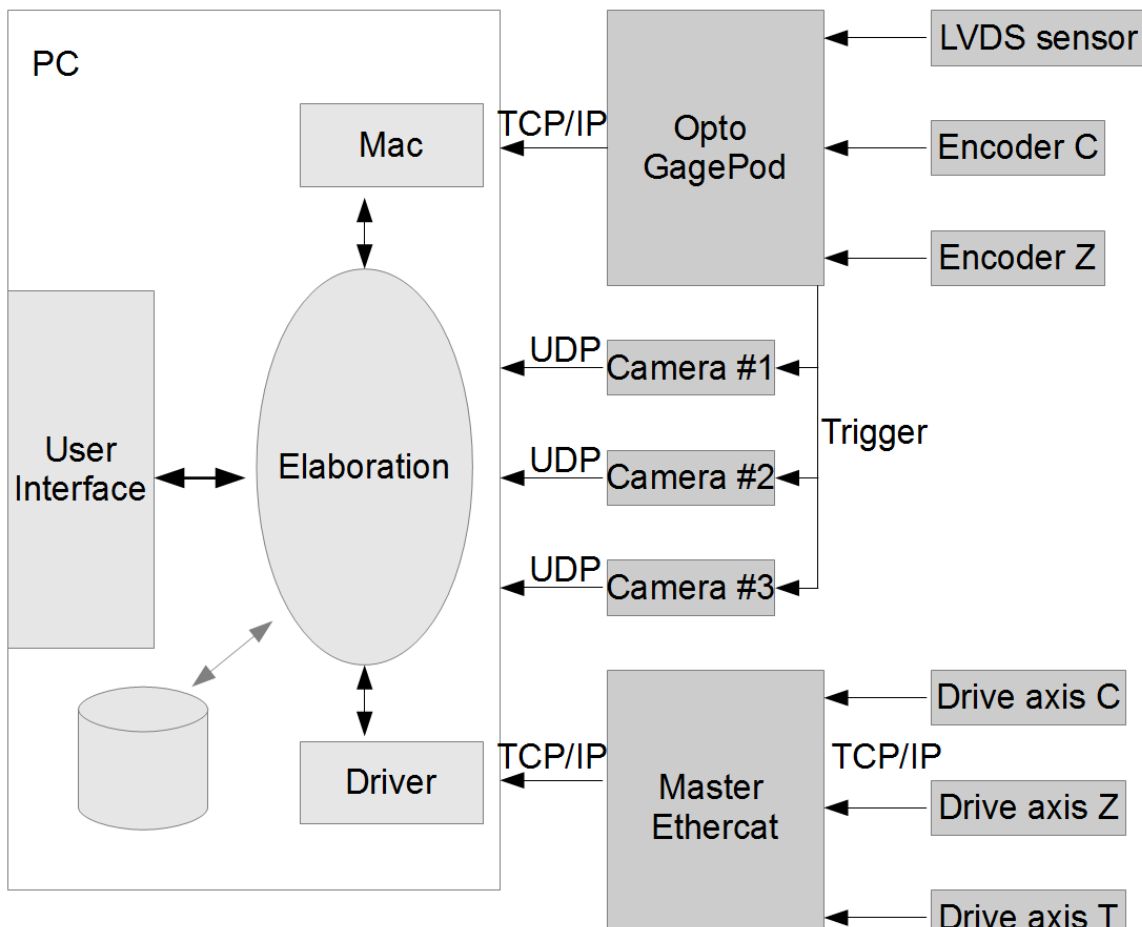An overview on the whole system is shown in Figure 72.

Figure 72: Scheme of whole acquisition system

There are two types of synchronizaton:

- time based in which the external device sends triggers periodically.
- space-based in which the external device sends triggers synchronized with the optical transducers that control the machine's movement.

This external device implements a new board of GagePod system designed to interface

this one to cameras on optical System. This board has to be connected to CPU board of GagePod and together realize the function needed for the application.

The interface connectors are located on the front panel:

- n. 2 connectors M12 female 8 pins for the cameras interface
- n. 4 connectors D-Sub male 9 pins for encoders interface
- n. 1 connector Lumberg female 5 pins for analog output
- n. 1 connector Lumberg female 7 pins for analog input

On the front panel there are also 10 LEDs for detailed information.

The main features of this board are:

- to manage four incremental encoders for positioning information or to generate a spatial synchronism;
- to deliver the power supply to two cameras and transfer the synchronism to them or from them;
- to manage a driver with the analog output (voltage/current);
- to acquire an analog source (voltage/current) with the analog input.

These functions are controlled by the CPU motherboard but they're managed by a FPGA inside this board.

All features of the board are controlled by the FPGA. At startup, it loads automatically the configuration bitstream from its boot memory (reading the data from the SPI interface).

The CPU board can access (with a parallel data bus) the FPGA directly to a file register to read and write data, commands, etc.

Inside the FPGA there are some blocks:

- "File register" that stores configuration of all other blocks; with this block the CPU also reads the counters, the analog input, etc.
- "FIFO", needed to store incoming data from the encoders and the analog input.
- "Encoder control and counter" manages the four encoder inputs, stores the counter value when the hold signal is active; if properly configured, it can generate a spatial synchronism. For the analog encoders, this module manages the A/D conversion units.
- "Encoder diagnostic" to manage errors and alarm signals, with the "File register" module.
- "Synchronism control" manages the connection matrix to route the input/output synchronism signals; this module is software-configurable.

- "Interrupt control"

- "External synchronism" from/to the M12 connectors. If programmed as output, this synchronism may be repeated (under SW control) up to 8 times at programmed time intervals. In every case, it is active for 1μs or 2μs (under SW control to indicate the start event).

- "Analog output control and dedicated memory" permits to create a V/I DC value or a repetitive waveform on the analog output. The software can setup the period, the shape (this is stored into a dedicated memory) of the output signal. The software can also configure if the output will be repeated indefinitely or one-shot.

- "Analog input control" acquires the dedicated A/D converter values and stores it into the FIFO like an encoder channel.

- "SPI master" can read or write the boot memory; this module can also control the IC driver of analog output using another chip select signal.

- "LED" module controls the LED of the encoders and of the synchronisms.

- "FPGA services" like startup, clock generator etc.

The board has a JTAG interface, connected to this FPGA, in order to run the boundary-scan test, to program and to debug the device.

Chapter 8

Marposs probe design

8.1 Technical features

During my PhD activity, I developed and realized the electronic boards shown in Figure 73, and I collaborated to the assembly of various components of the system, by programming the FPGA's firmware and developing different protocols used and the necessary vhdl logics. I also tested and put in place the electronic system, for which I created the software managing the essential function that I developed for the debug.
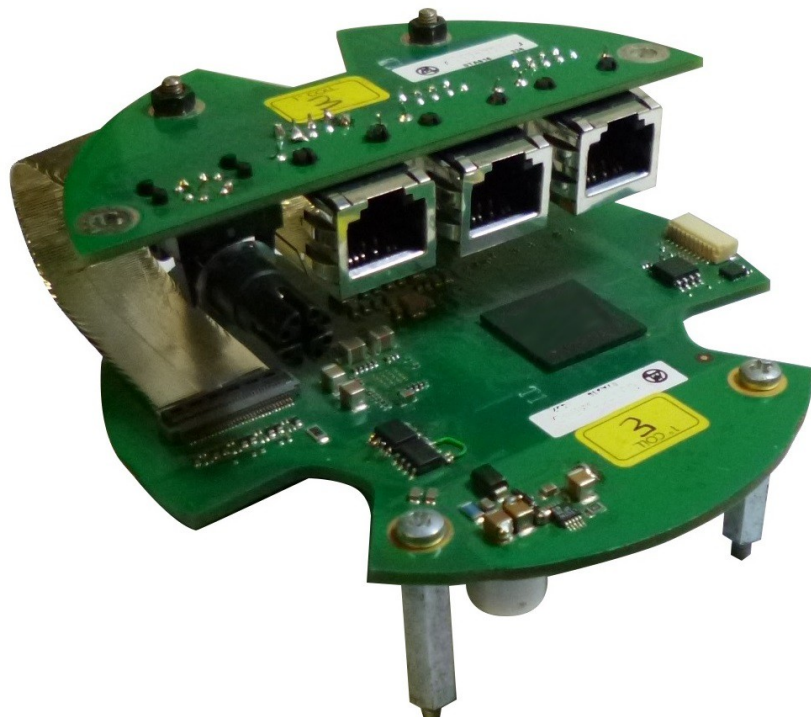

Figure 73: Marposs electronic boards

The electronic multi-board system manages an approximately 8200 pixel linear sensor and its illuminator. The interface is controlled by a Gigabit Ethernet line with point-to-point connection, while trigger and power supply are provided by a separate daisy-chain wire designed for multi-sensor systems.

The following technical features shown in Table 7 concern a single receiver probe, equipped with boards of interconnecting.

Power Supply	19.2 - 30 Vdc
Absorption current	< 150 mA at 24 V with illuminator
Ethernet Interface	10/100/1000 Mbit/s Ethernet interface MAC and IP, UDP, ARP and ICMP protocols are hardware implemented on FPGA
Sensor	8 digital synchronized bus, approximately 1000 pixel each, sized 7 μm
Frame	4 kHz maximum sampling frequency pixel data: 12 bit UDP data transmission: 12 packets/frames Approximately 700 pixel per frame, the first frame includes the status of the illuminator and the sensor and illuminator accelerometers
Performances	4 kHz maximum scanning frequency 556 Mbit/sec transmission speed
Diagnostics	Illuminator status Tri-axial accelerometer for testing vibrations on the probe Temperature variation on the probe Tri-axial accelerometer for testing vibrations on the illuminator Temperature variation on the illuminator
Non-volatile Memory	32 Mbit external dataflash, of which: 8 Mbit for FPGA bitstream 24 Mbit (3 Mbyte) available for mapping tables

Table 7: Technical features

8.2 Eletrical interface

The receiver probe (Figure 74) is connected to the PC via Gigabit Ethernet link. The connector is an M12 model certified for Gigabit networks (cat 6A, IP67).

RJ45 connectors are used to receive and trasmit power supply and trigger to the network of cameras, and also to connect to the illuminator.
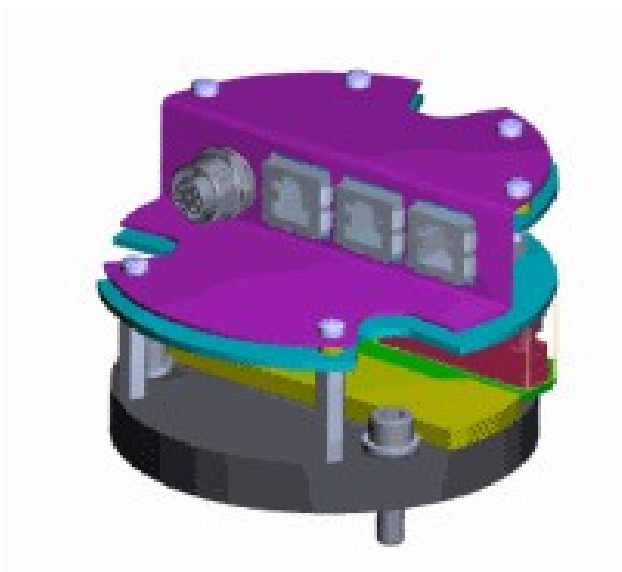

Figure 74: Receiver group

8.3 Linear sensor

The sensor chosen to equip the new linear cameras for OptoQuick and OptoFlex applications is a CMOS linear sensor featuring approximately 8200 in line pixel, 7 μm transversal dimension with completely integrated analogic interface electronics, implementing a 12 bit (ADC) converter for each pixel.

The converter is secured to the camera's chassis and connected to the reading electronics with a custom electronic board.

The sensor is divided into 8 arrays of approximately 1000 pixel each, organized in four consecutive sections.

Each array has its own 12 bit parallel bus to read collected data.

In addition to the 8200 pixel, there are about 30 more pixel designed for diagnostic functions and compensation value of darkness level.

Each one of the four sections is equipped with an SPI independent interface designed to program internal registers.

Collected data reading is sequential, with a 'read' command and a flag indicating valid data on the bus.

8.4 Design and Principle of electronic boards

The sensor interface electronics is made of three interconnected boards:

- One containing power supply, interface circuits to the sensor and the Gigabit FPGA implemented link,

- One connecting to the sensor (containing bypass capacitor and not active functions),

- One connecting outwards, containing ESD protections and output connectors

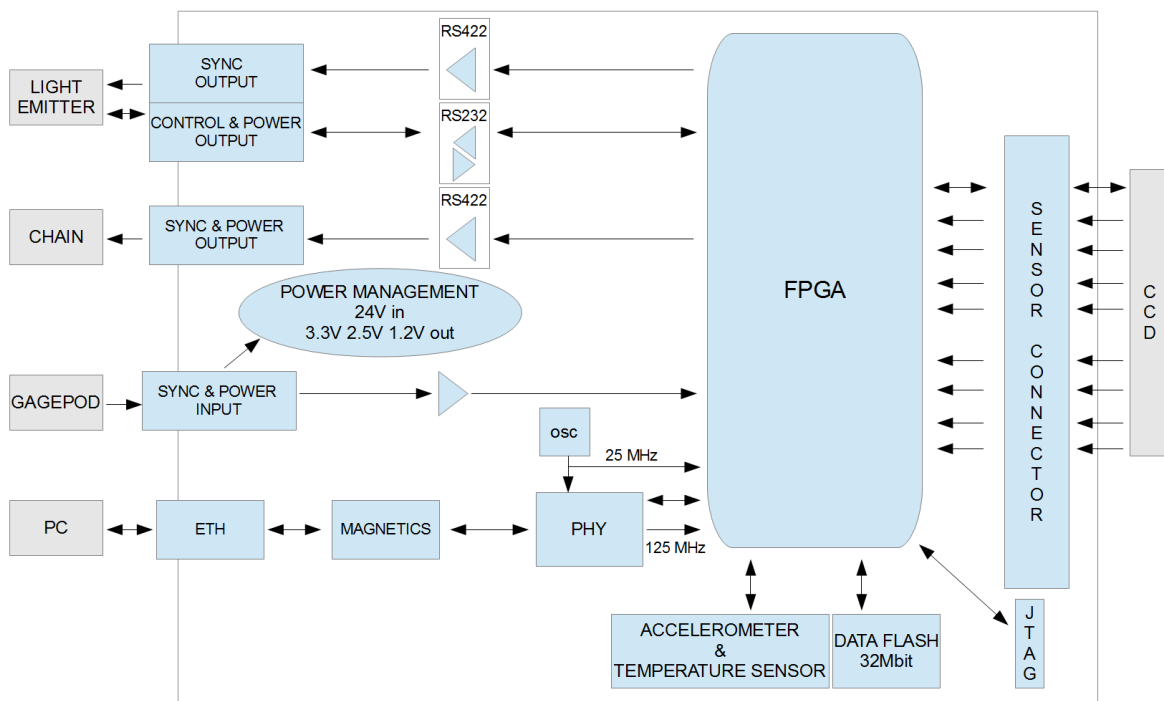General block diagram is showed in Figure 75

Figure 75: General diagram block

The circuit is designed to generate signals and timing necessary to control the sensor, and to send collected data via Gigabit Ethernet link.

Each scanning generates a frame, made of approximately 8200 12 bit words, each one relative to one sensor's pixel.

Each frame is splitted into 12 packets, containing about 700 pixel each (except for the first one, that contains less pixel to make space for temperature and accelerometers' data).

Scanning can be time-activated or trigger-activated by an external source.

The probe sends the trigger also to the illuminator to synchronize the illumination and the sensor's integration period.

The probe is also equipped with a mass storage (DataFlash), partly used for FPGA's firmware (8 MBit) and partly for probe mapping data (24 MBit).

The board is also provided with a triaxial accelerometer [39] for diagnostic purposes, which enables the monitoring of acceleration and vibration during the scanning process. It also enables the circuit's temperature variation measurement.

Communication with host PC occurs via Gigabit Ethernet link. It is physically managed by Micrel KSZ9031 [40] component, which communicates with MAC (FPGA implemented) through RGMII interface.

FPGA implements Ethernet MAC 10/100/1000 in hardware. It manages also (in hardware) the layer link and the UDP/IP protocol, allowing access to transmission channel with a simple buffer interface. The buffers, two for transmission and two for receiving, are designed to contain a whole Ethernet packet each, and are managed in pipeline (one is transmitted while another is received).

ARP and ICMP (ping command) protocols are also managed and completely implemented in hardware, without any intervention of local logics.

A second logic communication channel has been included (on a secondary UDP port), which enables the board's parameterization and management.

The channel implements an underprotocol which enables the access to ports and devices through a 16 bit parallel interface with 32 bit of address.

Arbitration between pixel transmission channel and control channel is automatically managed, prioritizing control channel.

On FPGA's inner, control bus has been implemented an SPI master interface for communication with the external DataFlash and the accelerometer, and an asynchronous serial interface (RS232) for remote illuminator control.

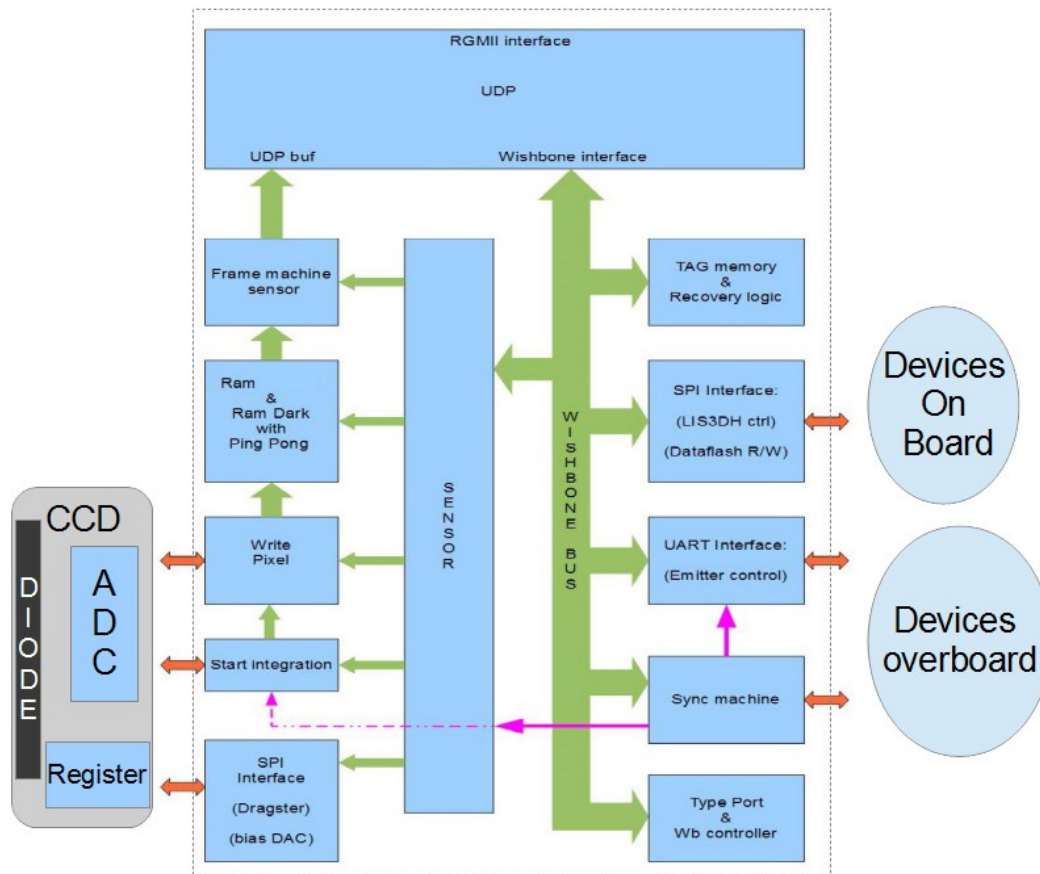The board and FPGA's structure are showed in Figure 76

Figure 76: Board and FPGA's structure

8.5 Details of the control logic

The system is designed specifically to manage the sensor directly from the PC, with no required dedicated interface hardware. The only external hardware signal is actually the trigger controlling the synchronization of multiple sensors and incremental optical transducers, that manages the measurement machine's movement axes.

The required transmission bandwidth can be easily calculated, given the sensor's features and the desired frame rate. Assuming 12 bit per pixel provided in transmission by the sensor with 16 bit words and a 4000 scannings per second goal, the obtained bandwidth is 8224 x 16 x 4000 = 526.3 Mbit/sec.

The Gigabit Ethernet transmission was therefore opted for, because it offers enough bandwidth and its use is largely spread for this kind of applications.

The local hardware implementation on FPGA of the whole communication logic and sensor management showed in the picture, has allowed the development of a highly performing board without a microcontroller.

Besides the fundamental data collection and transmission function, FPGA provides also the logic which allows for the peripherals remote control by the PC, as showed in the Figure 77
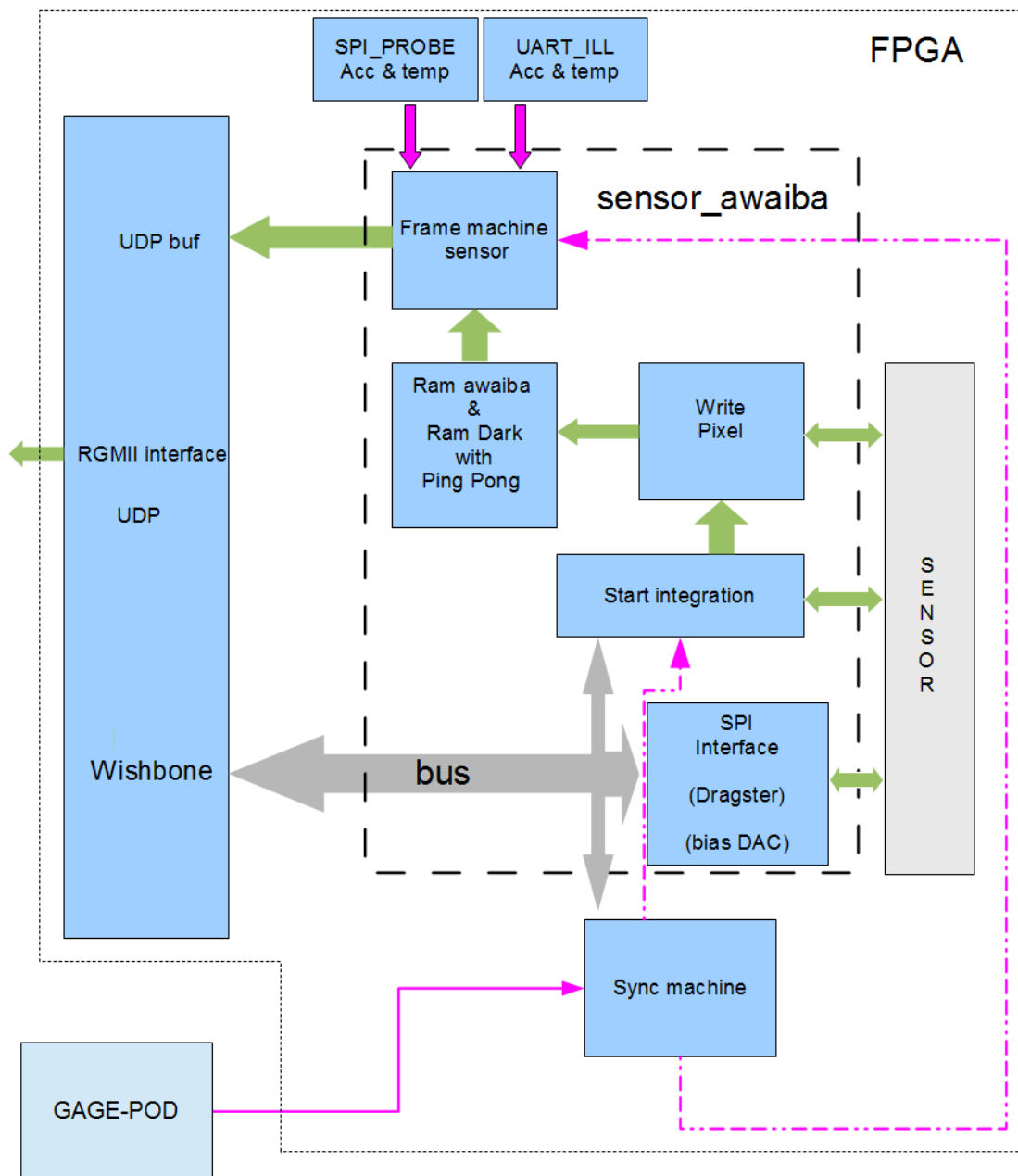

Figure 77: FPGA scheme

As far as the Ethernet is concerned, the probe has its own MAC address and IP static address, which can be programmed within a little storage on FPGA (probes will be provided with a default address to be reconfigured by software if necessary).

Data are transferred from PC to probe using UDP/IP protocol: it is therefore necessary to assign two ports, whose identifier can be programmed as the IP address in the FPGA storage. The first port is dedicated to frame transmission from probe to PC, the second controls and allows access to the probe's configuration and management registries.

The interface to the sensor is quite complex. As said before, the sensor is made of 8 approximately 1000 pixel arrays, interlaced in couples (the even pixel belong to an array, the odd ones belong to another).

The sensor has an A/D converter for each pixel, so that the acquisition is simultaneous for each pixel. Every array has its own 12 bit bus, synchronized to the clock signal, through which the FPGA downloads in sequence the pixel data.

The sensor's internal registers are programmed by eight SPI separate interfaces, managed by only one CLOCK and one MOSI, while MISO and Chip Select are specific. It is therefore possible to write on every array at the same time while you can read only one at a time. In addition, to control the array's exposition and conversion some logical signals are used.

The probe's Gigabit Ethernet interface can be used also as a means of transmission for the illuminator's remote control. The illuminator board shown in Figure 78, provided with a local CPU, is located on a dedicated board connected to the probe via RS232 interface. The probe routes on the serial channel the control bus accesses that allow the PC to access the registries that can program the illuminator's functionality.
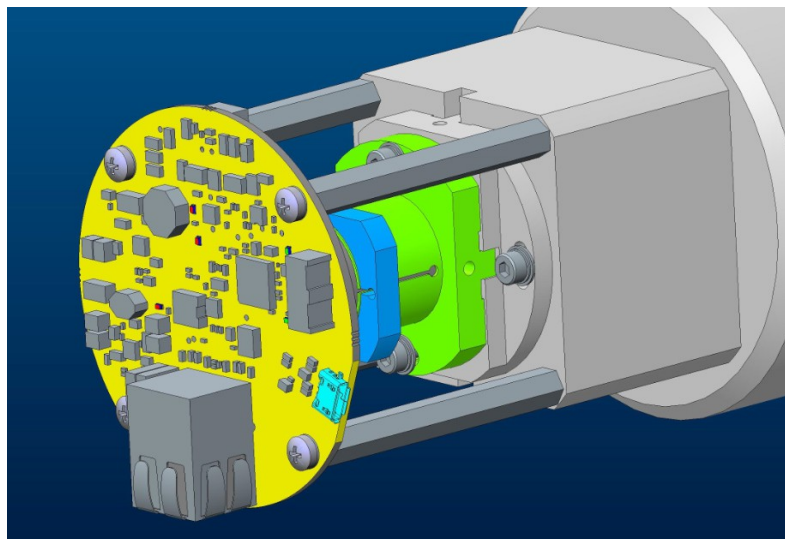

Figure 78: Emitter group

On the probe are also located two peripherals devices: an accelerometer and a 32 Mbit DataFlash serial storage. Both can be managed remotely by PC via dedicated SPI

interface.

The power supply section completes the design. 24 V external voltage is sent to a first DC/DC, based on +3.3 V voltage generating regulator, by which, through LDOs and switchings, are generated the voltages required by PHY Gigabit, FPGA, sensor and all the devices located on the board.

Established consumption is approximately 150 mW for the camera assembly and illuminator electronics, excluding LED.

8.6 Features of FPGA

Before describing in detail the several functional blocks, it is appropriate to describe general features of the implemented FPGA logic.

On the board is located an oscillator, providing the clock signal for the synchronization of the devices, and a reset generator, establishing the starting default values. After a hardware reset, part of the logic is kept in reset mode for the period necessary for the logic to read custom addresses (MAC, IP, UDP) used for communication.

Different parts of the board use different clock frequencies, obtained dividing the main clock signal. This was necessary because of the FPGA's internal delay time, which did not allow to have the same frequency for the whole logic.

This configuration needed the implementation of a bridge module, designed to connect and ensure the correct synchronization of all parts of the board.

The scanning data storage section uses the signal clock sensor to guarantee a synchronous data sampling. The reading, packing and transmission section, on the other hand, uses the clock signal in common with PHY Ethernet part.

FPGA contains a flash storage for programming bitstream, but it is also possible to access an external DataFlash, from which it is possible to upload a specific bitstream. In the application, a first version firmware is uploaded in internal flash, only to use in case of external storage fault.

The external storage must therefore be the first from which the bitstream is uploaded. On the external flash, the bistream can be updated from PC via UDP Ethernet. The new bitstream will only be used with the next boot.

8.7 UDP (network interface)

Gigabit network interface is managed by FPGA, which interfaces with the probe's managing logic through two UDP independent channels of communication: the first one

is dedicated to acquire frame transmission to PC, called FMP (Frame Machine Protocol); the second manages control traffic, the remote access to registers and storages located on the probe.

To manage the two data streams, an access arbitration circuit has been implemented, assigning priority to channel control.

ARP and ICMP protocols (necessary to network negotiation), part of data traffic, are processed in the FPGA and transparent to the user.

Network interface requires MAC address and IP address definition assigned to the probe and UDP ports assigned to channels. The values can be modified through control channel and stored in non-volatile mode into a small sized storage located in the FPGA.

The probe's logic manages a recovery system using broadcast packets to access and restore an unknown IP probe.

The PC remotely manages sensor and other peripheral devices located on the board. In order to support this activity a second UDP channel is established (the channel uses a different port from the one dedicated to scanning data transmission). To facilitate the probe's file register access and to manage remote devices, FPGA converts network level exchanged data into access cycles to a 16 bit WISHBONE parallel bus [41].

The control bus is an open source hardware bus designed for communication between FPGA internal logic and the integrated devices. It is designed to function as a logic bus, so it does not establish electric levels. The bus does not goes out of the FPGA, but connects the PC to the modules implementing different interfaces. Control bus is configured according to "shared bus" topology, with one master located in the FPGA and nine slaves, reached through the following signals in according to scheme showed in Figure 79:

- RST: reset signal,

- CLK: clock signal

- ADR: address signals; they provide the register's address in writing or reading within a slave. In the implementation, there are 32 address bit available, allowing access to a maximum 4 Gbyte storage

- DAT: data signals; depending on the access type (W/R), they contain data to be written in the registry or in reading the data read from register.

- WE: "write enable" signal; if high, it indicates current writing access; if low, it indicates current reading access

- SEL: "valid data" signals; it indicates what transferred data bytes are valid

- STB: control signal; if high, it indicates that transferred address and data are stable

- ACK: acknowledge; the slave turns the signal up to indicate that the cycle can be completed; it allows to manage interfacing with different speed slave devices

- CYC: turned up by the master, it indicates the beginning of a reading or writing cycle, and remains the same during the whole cycle

- CTI: "number" access signals; Wishbone bus manages single accesses and "bursts"; they indicate the current access' number
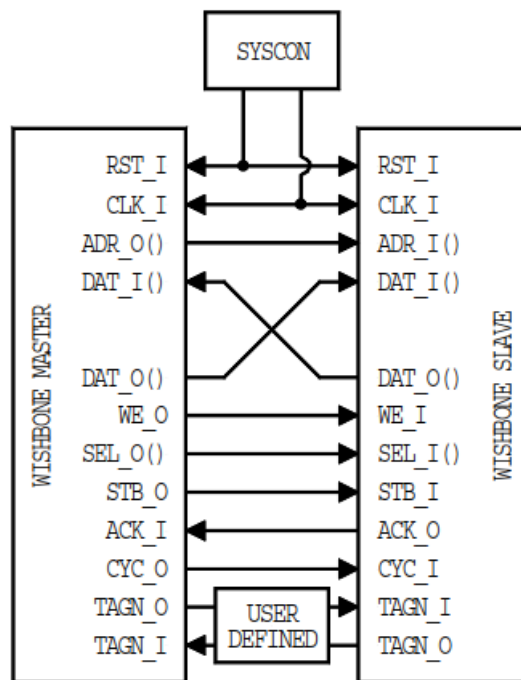

Figure 79: Standard connection master slave

Control protocol supports access in reading and writing mode; during writing cycles may show an "acknowledge" message sent by FPGA, indicating the cycle's complete execution on the bus. During burst cycles (during which more accesses are done at increasing addresses), the acknowledge signal is sent correspondingly to the last access.

During reading accesses, the acknowledge signal is not supposed to show, being implicitly intended in the return message with read data. Between the receiving of packets from FPGA and the sending of the answer packets, the communication channel is dedicated to UDP-control channel.

Sensor scanning data traffic remains on hold, that might determine some packets loss. This means that normally control activities must not take place during sensor scanning, especially with high frame-rate.

For this reason, status and diagnostic informations, used to validate the acquisition, have been included directly in the frame structure.

Slaves mapping into control bus' address space are shown in following Table 8

Address (0xXXXXXXXX)	SLAVE
0000 0000 to 0000 00FF	Sensor control
0100 0000 to 0100 0FFF	SPI master for DataFlash access
0200 0000 to 0200 00FF	Illuminator interface (UART)
0300 0000 to 0300 00FF	Internal storage
0500 0000 to 0500 00FF	Accelerometerautomatic read (SPI master)
0600 0000 to 0600 00FF	Synchronism management
0700 0000 to 0700 00FF	Watchdog
0900 0000 to 0900 00FF	Recovery
8000 0000 to 8000 00FF	Type port

Table 8: Slaves address mapping

At maximum frequency it is not possible to enter control accesses during acquisition, therefore software management includes only commands during non-operating acquisition.

ARP and ICMP accesses from PC are not directly manage by software, but because of their sporadic nature and their low payload they do not create packets loss.

8.7 FRAME structure

Frame acquisition from the sensor implies transmissions of more than 8200 12 bit words, corresponding to pixel plus control signals. To simplify the pixel collecting software task, it has been decided to send each pixel into a 16 bit word, instead of compacting them to reduce ethernet payload.

Besides, other managing data are added (camera and frame identifier) and also diagnostic information, allowing to monitor the probe assembly plus illuminator's functioning without making control access during scanning process.

With a 4 kHz frame rate, it is possible to get a 54% bandwidth typical on gigabit channel. Packets' sending takes place in sequence and takes approximately 140 μsec.

Allocation of control signals are static and are sent every first packet even when they are not updated by hardware.

8.8 Software

During my PhD activity, I developed a basic interface software called "Multi Camera Tester" (screenshot in Figure 81) to manage the essential functions I used to debug the board.

Figure 80: Basic interface software for debug

Final software for optoelectronic application (screenshot in Figure 81) is an add-on module integrated in the SPC Marposs software and it is quite complex because it must perform different functions: movement of axes motor or touch probes, management of cameras and illuminators, data acquisitions from different sensors, data elaboration and

extraction of features, showing of results and images, programming of different measure cycles, extraction of shaft's profile, etc.
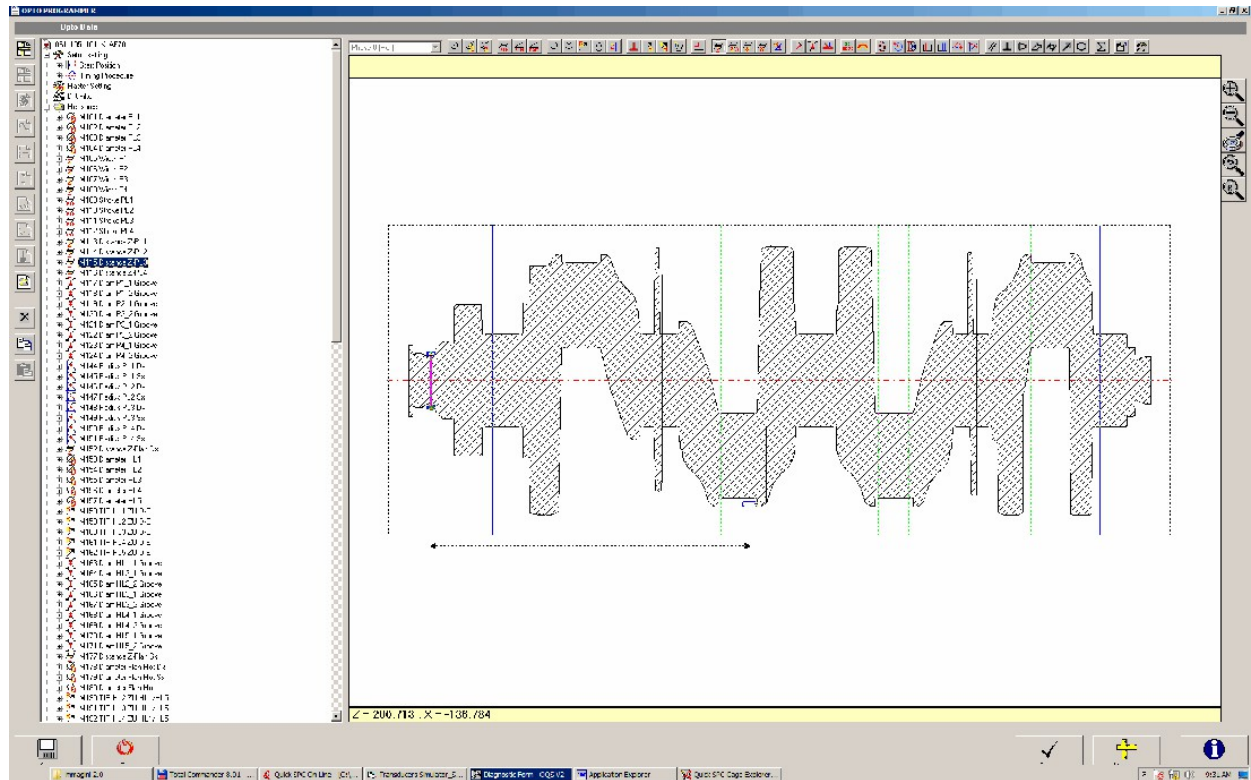

Figure 81: Programming display

For this reason, software is composed of many components, each of which executes a particular task; in this project new modules have been implemented to manage new cameras system and replace the old one based on E96 board.

Software must be able to transform a customer request in a series of movements and acquisitions, in order to provide the desidered measure (example in Figure 82).
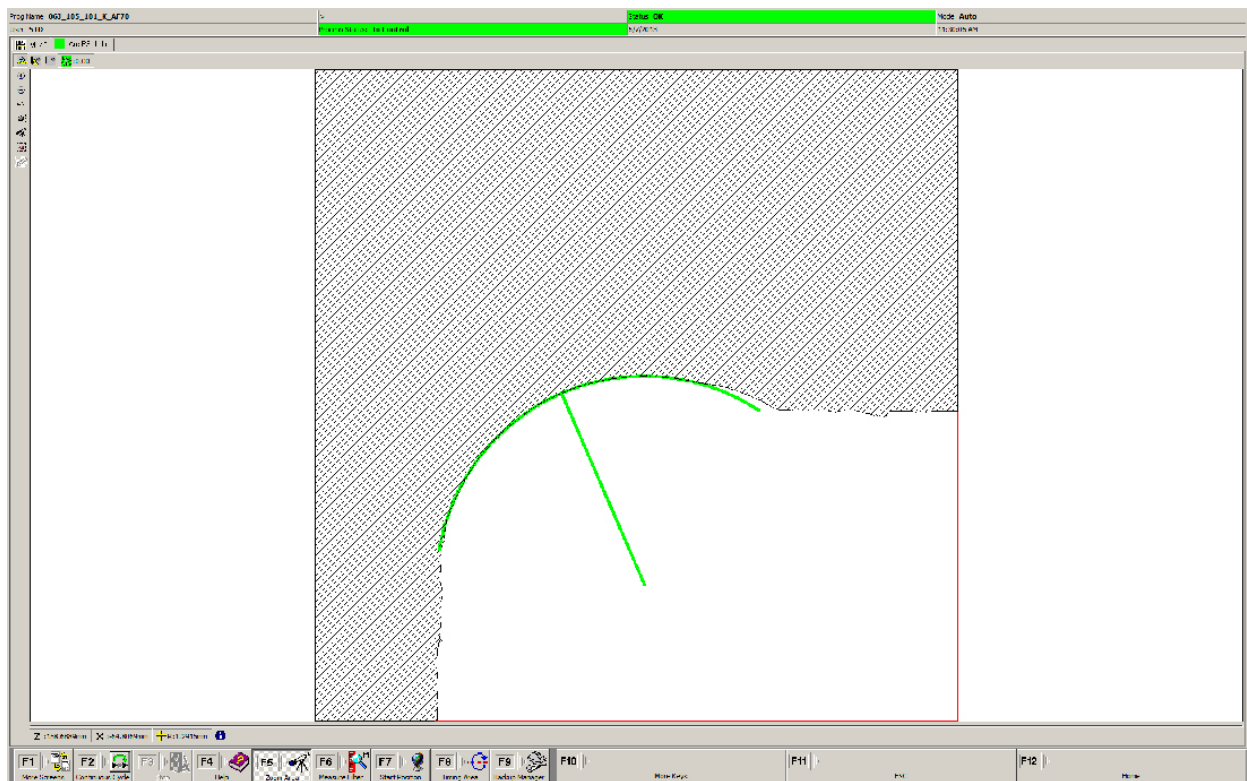
Figure 82: Software with a measure customer request

The element on which are based all kinds of measures is the calculation of the edge position, that is the transition of light intensity in the pixel array; this is found through an algorithm with subpixel resolution and so the resolution of the system can be under μm. In this way measures along X-axis are made, while the position along Z-axis is given by linear encoder. Many measures are made with the shaft in rotation; for this reason there is a rotary encoder which report the angular position.

A particular mapping procedure must be performed at the beginning of life of the system to compensate distortions of the optical system and temperature variations; mapping tables are so created and used in measure algorithms allowing high precision.

It is possible to use an immediate visualization (see Figure 83), in the user interface, that allows to see, rapidly, if the shaft put in the machine respects the imposed tolerance
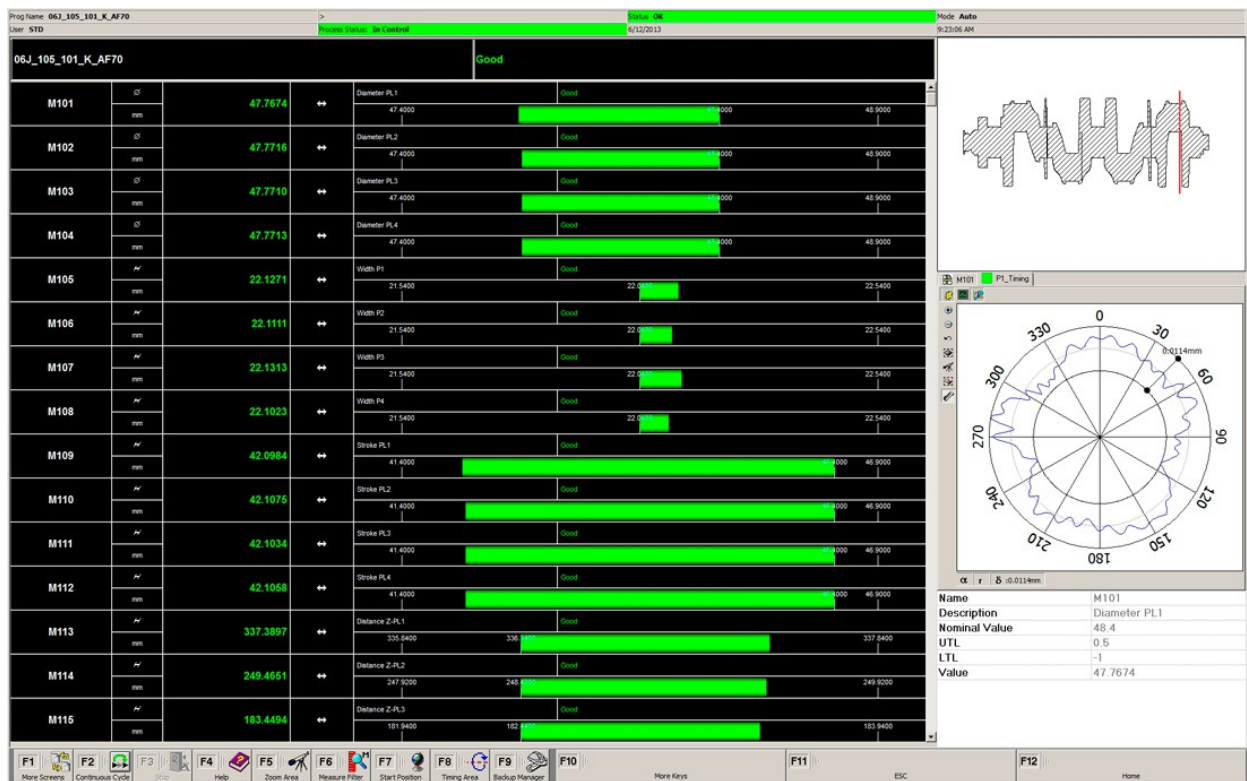
Figure 83: Immediate visualization in the user interface

Conclusions

My PhD activity is divided into two main parts, developed in different contexts of research: the first one in the field of high energy physics, and the other one is related to advanced technology for high-precision industrial equipment. The common denominator is the development of high speed electronics based on FPGAs for demanding data acquisition and data processing applications. This thesis is the synthesis of my work at the INFN section of Bologna and at the Marposs company during my PhD activity.

In the field of high energy physics I've participated to the research and development of a system for measuring the luminosity of the largest accelerator in the world: LHC. The luminosity monitor of the ATLAS experiment called LUCID, has been updated in 2014 and new electronic boards have been realized. The LUMAT and the LUCROD boards, subjects of my study, are smart acquisition boards able to produce and bring large input/output data bandwidth and large input/output data bandwidth at low bit error rate thanks to the transmission over optical fibers connections. Although they are developed to acquire data from the LUCID detector, they have been designed to keep a good degree of flexibility to allow their use for different applications. The boards and their sensors work together as a system specifically designed for hardware calculation of the luminosity at the ATLAS interaction point, one of the experiments installed at the Large Hadron Collider (LHC). The development of these boards allowed to achieve a high level of versatility on them, which are able to adapt to different configurations concerning the sensors and, in general, the data acquisition system. The LUCROD boards receive as input the data stream coming from PMTs exposed to the beam. After the elaboration, LUMAT boards provide to the ATLAS experiment the luminosity value with a precision which goes beyond the design specifications. I studied in details the logic of interesting events selection and acquisition, that make the LUCID system the benchmark detector for luminosity measurement in ATLAS. The firmware required for the communication between the LUMAT and LUCROD boards has been developed and then tested with the whole system. Communication is based on optical transceivers running at 2 Gbit/s which are directly driven by the FPGAs' ser-des. The firmware I developed, implements a custom communication protocol based on the 8b/10b line code allowing data exchange and real time monitoring of the link system. A feature of the LUCROD-LUMAT system required a serial synchronous communication where the data are sent at a continuous rate at 40 MHz without any single clock loss, without any idle time and without any jitter at the receiving end: three characteristics that required a carefully studied solution. The LUMAT board actually exchanges and manages 4 Gbit/s of data, though presenting a redundancy factor of x2 on the available raw data bandwidth. The test on the firmware has been completed and now the whole system is up and running since the real data taking phase has started since April 2015. The use of FPGA devices within the boards proved to be a crucial factor for the development and

the realization of the project. Several VHDL language entities have been created, resulting in thousands of code lines. The read out section system is completed and it represents the central element in the acquisition system of the experiment. It is designed to collect and send data to the ATLAS T-DAQ software for statistical analysis of results. From April 2015 to December 2015 the whole acquisition system has operated at full capacity, demonstrating good performances in luminosity measurement both online and offline, with a good stability over the data taking period.

The overall results of the activities performed at Marposs are also promising. I realized a system that is going to be used in a multiple-camera system designed for outline identification after machine tools working. Several boards have been designed and produced; firmware development and debug for the boards have been carried out during the first research phase. The following phase was the industrial production, adapting the system accordingly to production requirements. Nowadays the system is able to measure mechanical pieces with a 0,2-0,3 μm precision and a very high repeatability. Within a few months several optical gauges based on the multiple-camera system described in this thesis will be produced.

The Apprenticeship Program allowed me to continue my academic course in close contact with the work activity I started during my stage and thesis carried out during my master degree. It also allowed me to achieve a higher level in education and training in two different contexts of excellence, i.e. the industrial company and the academic research, where I could concretely learn the best technical knowledge.

The chance of bringing together two distant worlds was the most enthusiastic aspect of this PhD research. The worlds of industry and academic research faces similar problems with different points of view and goals. I had the opportunity to explore pure academic research, and also to apply my grew knowledge, learned in physics studies, to the industrial research.

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