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Interfacial interactions, charge transport and growth phenomena in Organic Field Effect Transistors

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Dedicated to my mother Luciana, Stefano and my beloved family

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Contents

Preface

Organic electronics is an emerging field with a vast number of applications having high potential for commercial success. Although an enormous progress has been made in this research area, many organic electronic applications such as organic opto-electronic devices, organic field effect transistors and organic bioelectronic devices still require further optimization to fulfill the requirements for successful commercialization. The main bottle neck that hinders large scale production of these devices is their performances and stability. The performance of the organic devices largely depends on the charge transport processes occurring at the interfaces of various material that it is composed of. As a result, the key ingredient needed for a successful improvement in the performance and stability of organic electronic devices is an in-depth knowledge of the interfacial interactions and the charge transport phenomena taking place at different interfaces.

The aim of this thesis is to address the role of the various interfaces between different material in determining the charge transport properties of organic devices. In this framework, I chose an Organic Field Effect Transistor (OFET) as a model system to carry out this study. An OFET offers various interfaces that can be investigated as it is made up of stacked layers of various material. Charge transport in OFETs takes place only in the first few monolayer residing adjacent to the dielectric. In order to probe the intrinsic properties that governs the charge transport, we have to be able to carry out thorough investigation of the interactions taking place down at the accumulation layer thickness. However, since organic materials are highly instable in ambient conditions, it becomes quite impossible to investigate the intrinsic properties of the material without the influence of extrinsic factors like air, moisture and light. For this reason, I have employed a technique called the *in situ* real-time electrical characterization technique which enables electrical characterization of the OFET during the growth of the semiconductor right from the early stages up to thicker films. Various scientific investigations of the processes taking place at the different kind of interfaces of the OFET have been carried out.

The thesis is organized as follows: **Chapter 1** gives a brief introduction of an OFET, the theory of charge transport in organic semiconducting materials and a highlight on the various interfaces which I have studied. An explanation on the relevance of the interfaces in determining the response of the OFET is discussed. In **Chapter 2** I describe the

different materials and methods that I have used for the experimental study and what are the parameters that I can extract from the experimental data analysis. In **Chapter 3** I address the role of the dielectric-semiconductor interface in determining the performance of a device. This interface is the core of the OFET as it is the place where charge transport occurs. Optimizing the charge transport along this channel is relevant in order to realize applications in flexible organic electronic devices and information technology. The work reported in this chapter deals with understanding of how disorders affect the performance of a device. A comparative study of the evolution of the charge transport characteristics as a function of film thickness of an OFET fabricated on an untreated SiO_2 and a SAM modified SiO_2 from sub-monolayer thickness to the multilayer regime is carried out. In addition, temperature dependent measurements was performed out in order to have a deeper insight into the charge transport phenomena taking place. In **Chapter 4**, I investigate the charge carrier accumulation and transport in sub-monolayer pentacene thin film transistor. The motive of this work was to quantify the amount of charges that accumulate in the semiconductor due to field effect.

Applications such as the organic opto-electronic devices are basically made up of an electron donor and an electron acceptor material. Charge transport in these devices largely depends on the energy alignment and molecular architecture of the heterojunction. With the aim to investigate the charge transport at the interface between a p-type semiconductor and an n-type semiconductor, I have carried out a study on the interaction and charge transfer at the heterojunction of pentacene (a p-type semiconductor and C_{60} an n-type semiconductor) reported in **Chapter 5**. The aim of this project is to examine the role of C_{60}/Pentacene interface morphology on the interfacial charge transfer phenomena occurring at the heterojunction by monitoring the electrical characteristics of ultra thin film of pentacene onto which C_{60} film is grown.

The next interface which I have addressed in this thesis is the electrolyte-semiconductor interface. This interface is central for organic biolectronics as the organic devices that has to interact with biological systems have to be operated in aqueous environment. In **Chapter 6** I have taken up the study of this interface by using the dual gated measurements of pentacene OFET. Using this protocol I was able to directly extract the capacitance of the double layer formed at the pentacene electrolyte interface. This is a relevant physical parameter needed for exploiting pentacene EGOFETs in biosensing

application. Moreover, moisture induced instability issues of OFETs is explored. The work which I report in this chapter has been done all *ex situ* after the fabrication of the OFET.

Due to a growing interest in neuro inspired devices based on new technology, the last chapter of this thesis concerns the understanding of charge transport processes at the interface between gold nanoparticles and pentacene in Nanoparticles Organic Memory Field Effect Transistor (NOMFET) devices. NOMFET was designed to mimic the feature of the human synapse known as 'synapse plasticity'. **Chapter 7** reports on the evolution of the electrical characteristics of pentacene grown on a dielectric functionalized with a network of gold nanoparticles.

Keywords

Organic field effect transistor

Organic semiconductors

Interface

Charge transport

Percolation

Disorders

Chapter 1 Interfaces in Organic Field Effect Transistor

1.1 Brief history of OFET

The concept of Field Effect Transistor (FET) was first proposed by Lilienfeld in 1930s.[1] A FET operates as a capacitor where one plate consists of a conducting channel between two ohmic contacts, the source and the drain and the second plate is the gate electrode. However it was only in 1960 that Kahng and Atalla fabricated the first silicon-based Metal-Oxide Semiconductor FET (MOSFET).[2] Nowadays, MOSFET has been the most prominent constituent of microelectronic devices. MOSFET are mainly fabricated with single crystalline silicon because of the excellent silicon-silicon oxide interface.

The metal-oxide-semiconductor capacitor using organic semiconductors was demonstrated by Ebisawa, Kurokawa, and Nara at NTT in 1982. The device was fabricated using polyacetylene as the semiconductor on a polysiloxane gate dielectric and used aluminum for the gate and gold for the source and drain electrodes.[3] The next significant milestone was the development of the first Organic Field Effect Transistor (OFET) with recognizable current gain by an *in situ* polymerized polythipohene transistor by Tsumura, Koezuka, and Ando of Mitsubishi Chemical in 1986.[4] Ever since this first FET was reported, interest in this field has risen steadily for both technological and scientific reasons. In the last two decades a significant number of studies on organic transistors have been reported. The interest in OFETs stems out due to the fact that they could serve as a main component in cheap and flexible electronic circuits. Major possible applications are Radio Frequency Identification (RFID) tags, flexible displays and recently organic-bioelectronic devices. Research efforts in optimizing the performances of these devices has been going on for the past decade of years. The main factor which is still preventing the commercialization of these devices is the mobility of the charge carriers and the sensitivity of the devices under air, moisture, and light exposure. The response of organic devices in general relies on the interfacial interactions that takes place between different materials that it is composed of.

1.2 Organic semiconductor

Organic semiconductors can be classified into two main classes

(i) Small molecules

(ii) Polymers

Carbon atoms (C-atom) in organic semiconductors form sp^2-hybridization (figure 1.1), where there are three sp^2-orbitals on the same plane (each with one electron) and a p_z-orbital perpendicular to this plane (with the fourth electron).

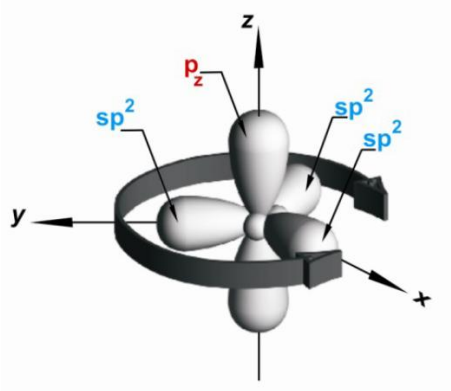

Fig. 1.1 *Carbon atom in its sp^2 hybridization form; 3 electrons are distributed in plane in sp2 orbital and an electron is positioned in the p_z orbital perpendicular to the sp2 plane.*

In an organic semiconductor, neighboring C-atoms present sp^2-hybridization, the overlap of sp^2- sp^2 orbitals forms a strong covalent σ-bond, whereas the overlap of two p_z-orbitals orthogonal to the plane of molecule yields a π-bond. In terms of energy, the σ-bonds (representing the backbone of the molecules) are stronger than the π -bonds. These kinds of molecules, termed π-conjugated molecules, exhibit an electronic structure dominated by the energy band gap between the HOMO (Highest Occupied Molecular Orbital) and LUMO (Lowest Unoccupied Molecular Orbital) levels. These are the most relevant molecular orbitals for the optical and electronic properties (Fig 1.2)

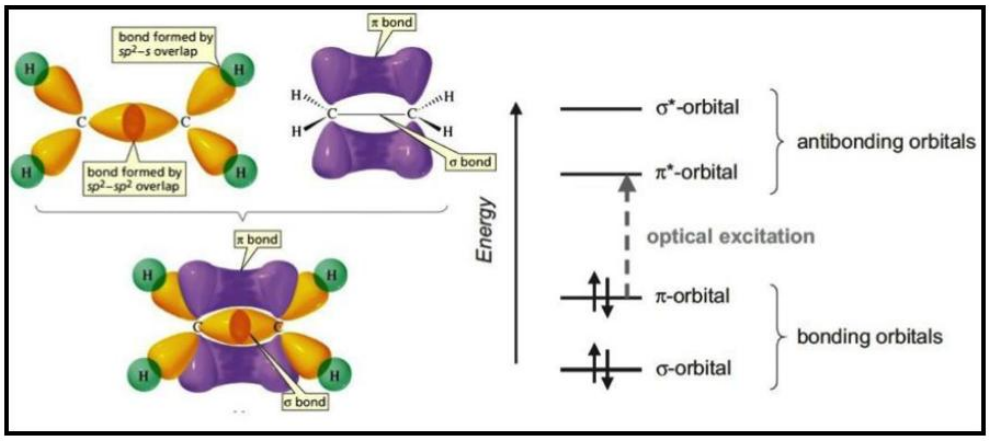

Fig. 1.2 *Ethylene molecule representations: Top view: sp^2 orbitals of C-atom (the p_z orbitals being perpendicular to the page, σ-bonds formed due to overlapping of sp^2 orbitals and π-bonds formed by the overlapping of p_z orbitals, bottom view: shows the whole hybridization ; right picture depicts the energy levels.*

In an isolated molecule, the energy levels are discrete and are a product of the combination of atomic orbitals. They are known as molecular orbitals. Due to the weaker nature of the π-bond compared to *σ*-bond, the *π*-electrons are involved in electronic transitions, named $\pi \rightarrow \pi^*$ transition between the HOMO and LUMO. As the conjugated network on a molecule becomes more spread out, the transition from HOMO to LUMO requires progressively lower energy (Fig. 1.3) and the energy band gap, dividing the bonding and the anti-bonding orbitals, becomes smaller.

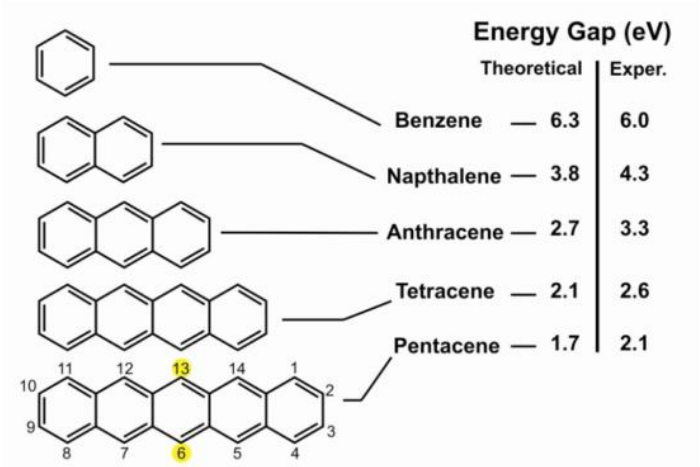

Fig. 1.3 *Molecular structure of the first five polyacenes and their HOMO-LUMO transitions (theoretical and experimental). Note that pentacene C-atom positions have been tagged. Positions 6-13 have been identified as they are most exposed to oxidation.*

1.3 What is an Organic Field Effect Transistor?

An Organic Field Effect Transistor (OFET) is a device which consist of three electrodes the Gate (G), the Source(S) and the Drain(D) , a dielectric and an organic semiconductor. It can be viewed as a parallel plate capacitor where one plate constitutes the gate electrode while the other plate consists of the semiconducting material bridging the source and drain electrodes. The source and drain electrodes of width *W* is separated by a distance *L* also known as the channel width and length respectively. The semiconductor layer in OFETs is usually vacuum sublimed , spin coated or drop casted depending on the semiconductor . The gate electrode is made up of a metal or a highly doped silicon serves as a gate electrode. The source and drain electrodes which inject charges into the semiconductor, are usually high work function metals like gold . The dielectric in our case is normally thermally grown silicon oxide or an electrolyte in the case of the electrolyte gated field effect transistor configuration.

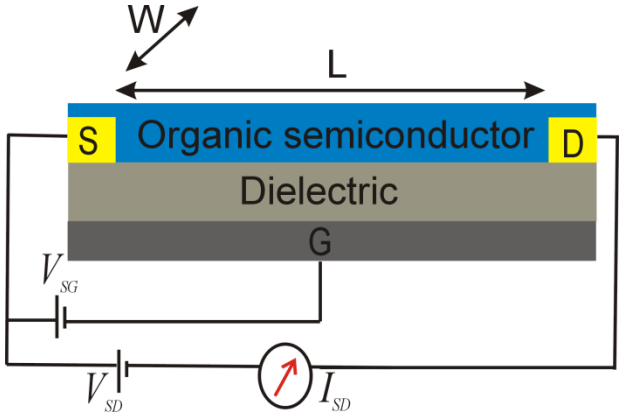

Fig. 1.4 *A schematic diagram of a field effect transistor and applied voltages. L and W are the channel length and width of the transistor. V_{SG} is the source gate voltage, V_{SD} is the source drain voltage and I_{SD} is the current flowing from the source to the drain.*

1.3.1 Device structures

There can be different device geometry depending on the position of the three electrodes with respect to the semiconducting material. The most commonly found structures (in relation to the substrate) are the bottom contact/top gate ,bottom contact/bottom gate and top contact/bottom gate structures.(Fig, 1.5). For most of the work in this thesis, the bottom gate/bottom contact configuration is used except for the experiments reported in Chapter 6.

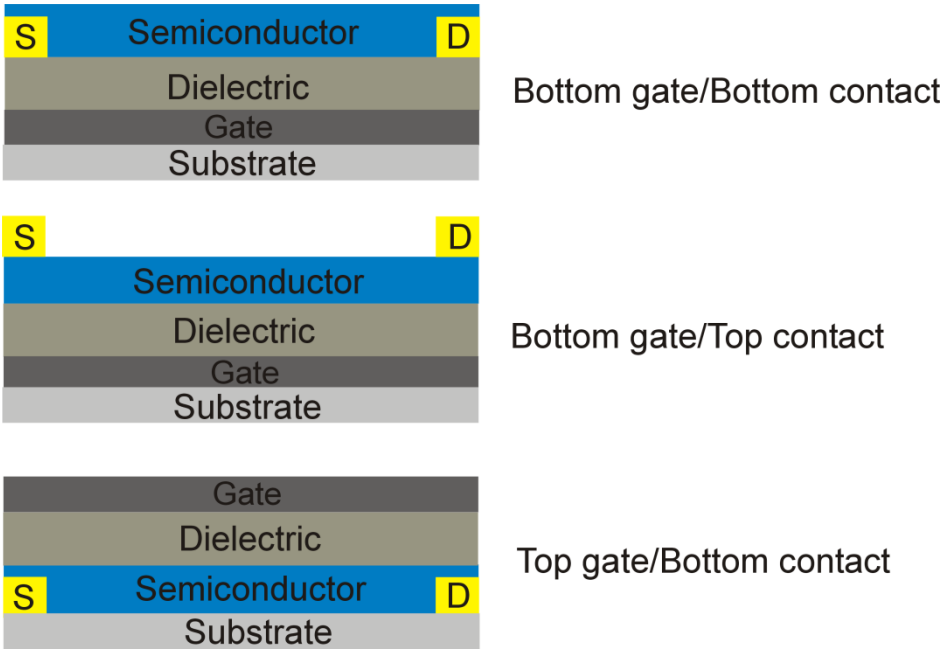

Fig. 1.5 *Common field-effect transistor configurations*

1.3.2 Basic Operation of an OFET

A potential is applied to the gate electrode V_G and drain electrode V_D while the source electrode is normally kept grounded. The potential difference between the source and the gate is just called the gate voltage V_{SG} while the potential difference between the source and drain is referred to source-drain voltage V_{SD}. The source inject charges as it is more negative when a positive gate is applied (electrons are injected) and more positive when a negative gate (holes are injected) is applied.[5]

A negative gate voltage will induce accumulation of positive charges (holes) at the semiconductor/dielectric interface and a positive gate voltage induces the accumulation of negative charges (electrons). The amount of charges accumulated is proportional to the gate voltage applied and as well to the capacitance of the dielectric. However not all of these charges are mobile and contribute to the source-drain current of the FET. Initially, deep traps has to be filled before the additional charges become mobile for charge transport. Therefore the concept of threshold voltage comes in. Threshold voltage V_{th} is the minimum gate voltage required to form a conducting channel . Therefore the effective gate voltage becomes (V_G-$V_{th.}$). When no drain voltage is applied the charge carriers concentration in the channel of the semiconductor is uniform. When a small potential V_D is applied such that V_D<<V_G-V_{th}, a linear gradient of charge carriers is created. This is normally called the *linear regime* because the current increases with increase in V_D.

However, when V_D is further increased such that $V_D=V_G-V_{th}$, the channel is pinched off and an even increasing V_D causes the channel to deplete. This mode of operation of the OFET where $V_D \geq (V_G-V_{th})$ is called the *saturation regime*.

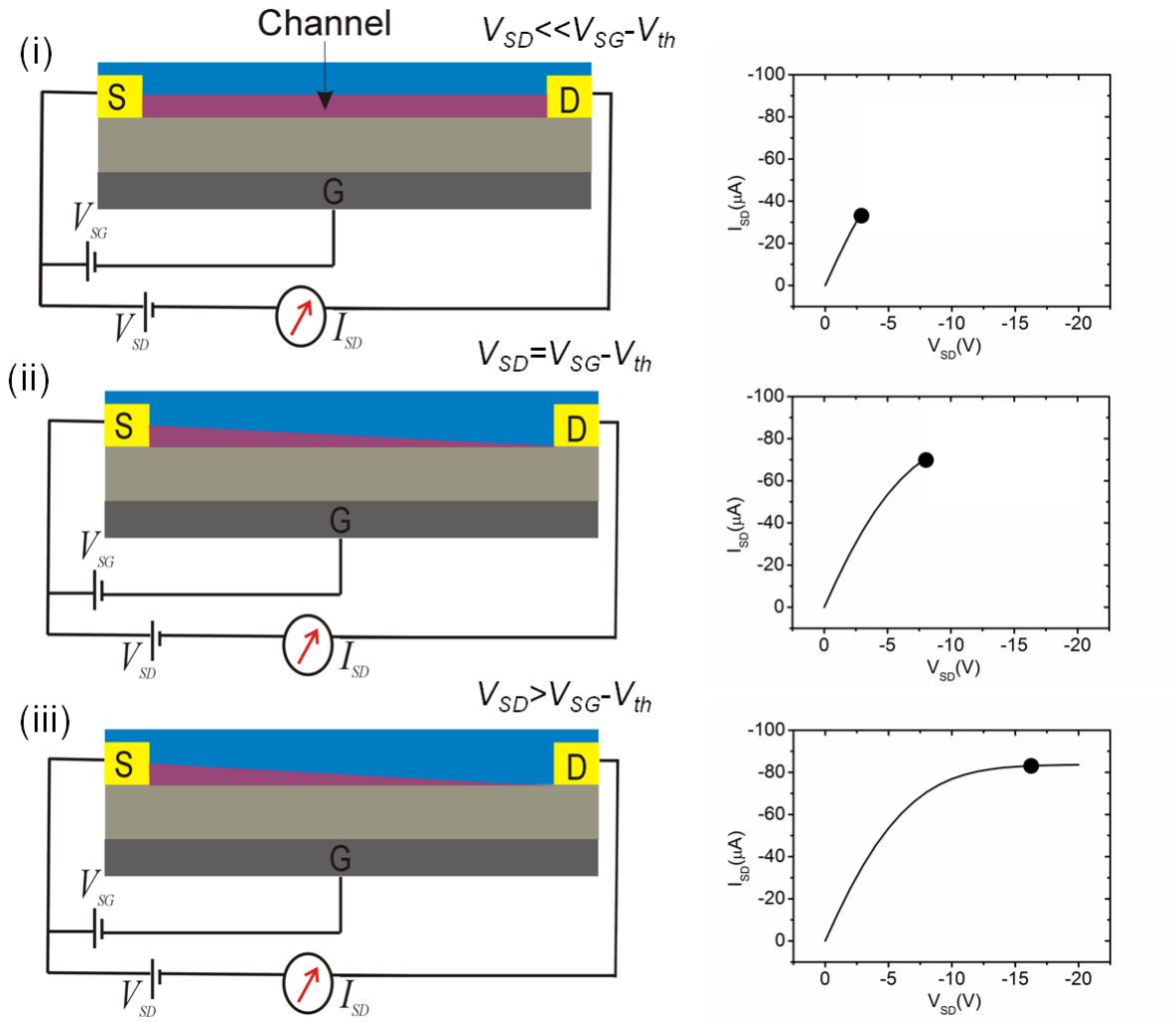

Fig. 1.6 *Illustrations of operating regime of an OFET. (i) linear regime (ii) At pinch off (iii) saturation regime.*

1.3.3 Current-voltage characteristics

The current voltage characteristics in different regimes can be described analytically using a gradual channel approximation. This implies that the gate field perpendicular to the current flow is much larger than the electric field parallel to the current flow created by the drain voltage.

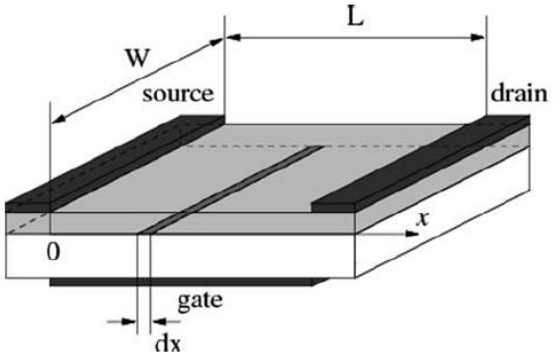

Fig. 1.7 *A schematic of an OFET for the derivation of the current.*[6]

When the gate voltage exceeds the threshold voltage V_{th}, the induced charge *dq* in an elemental strip *dx* is given by

$$dq = -C_i\left[V_G - V_{th} - V(x)\right] Wdx \tag{1.1}$$

Here, the potential $V(x)=0$ at source and $V(x)=V_D$ at the drain. C_i is the capacitance per unit are of the dielectric , *W* is the width of the channel and *Wdx* represents the area of the elemental strip.

Current I_D can be expressed as the amount of charge *dq* passing from source to drain at time dt is

$$I_D = \frac{dq}{dt} = \frac{dq}{dx}\frac{dx}{dt} \tag{1.2}$$

Mobility of charge carriers μ can be defined as the ratio between the mean velocity (*dx/dt*) of the charge carriers and the electric field $E = -dV/dx$. So $dx/dt = -\mu(dV/dx)$.

$$I_D dx = WC_i\mu\left[V_G - V_{th} - V(x)\right]dV \tag{1.3}$$

I_D is obtained by integrating I_D from source ($x=0, V(x)=0$) to drain ($x=L, V(x)=V_D$).

$$I_{D,lin} = \frac{W}{L}C_i\mu\left(V_G - V_{th} - \frac{V_D}{2}\right)V_D \tag{1.4}$$

Eq.(1.4) corresponds to *linear regime* where $V_D < V_G - V_{th}$

In *saturation regime* as described earlier, $V_D = V_G - V_{th}$. Therefore substituting this is eq. (1.4) we get

$$I_{D,sat} = \frac{W}{2L}C_i\mu(V_G - V_{th})^2 \tag{1.5}$$

1.4 Theory of charge transport in organic semiconductors

Band Transport

The mechanism of band transport occurs in crystalline inorganic solids like metals and semiconductors. In these solids energy bands form when a large number of interacting atoms are brought together. Their energy levels become so closely spaced that they become indistinct. However all of these bands are not filled with electrons. The probability of these bands being filled is given by the Fermi-Dirac statistics

$$f(E) = \left(1 + \exp\frac{E - E_F}{kT}\right)^{-1} \tag{1.6}$$

where k is the Boltzmann constant, T is the absolute temperature and E_F the Fermi energy. On this basis, solids can be classified as insulators, where the valence band (highest occupied band) is completely filled while the conduction band (lowest unoccupied band) is completely empty and metals in which the conduction band is partly filled. Semiconductors on the other hand has a small energy gap in between the valance band and conduction band such that at nonzero temperature, the smoothing of the Fermi Dirac distribution causes an appreciable number of states at the top of the valence band to be empty and an equivalent number of states at the bottom of the conduction band to be filled.

The earliest transport model for charge transport is the Drude model. This model assumes that the charge carriers are free to move under the influence of an electric field but are subject to damping forces due to collisions. This model is valid for semiconductors where the density of carriers is lower than the atomic density. Statistically the mean drift velocity v_x of the carriers in the direction of the field F_x can be written as

$$\langle v_x \rangle = \frac{q\tau}{m^*} F_x = \mu F_x \tag{1.7}$$

where q is the elementary charge, τ the relaxation time , m* is the effective mass and μ the mobility. It is important to note here that this model is valid only when the mean free path λ (the mean distance between two collisions) is much larger than the de Broglie length of the charge carrier (the distance between two atoms in the crystal). The mean free path is given as

$$\lambda = v_{th}\tau \tag{1.8}$$

where $v_{th} = \sqrt{3kT/m^*}$ is the electron thermal velocity. From eq. 1.7 and eq. 1.8 we can write

$$\mu = \frac{q\lambda}{m^* v_{th}} \tag{1.9}$$

The temperature dependence of mobility depends on the nature of scattering centers. However, it is found that the dependence follows a general behavior given by

$$\mu(T) \propto T^{-\alpha} \tag{1.10}$$

α is a positive number in most practical case so the mobility increases with decrease in temperature.

Polarons

The band model is not valid for charge transport in organic semiconductor because it fails to consider a crucial phenomenon in these material which is polarization. In organic solids, the molecular properties dominates that of the crystalline properties due to the weak van der Waals intermolecular interactions. This leads to a tendency of localization of charges on individual molecules. The localized charge , due to a typical residence time, manages to polarize the surrounding electronic and nuclear subsystems. Therefore charge carriers move in the solid not as free particles but they are "dressed" with a polarization cloud . Such entities are called "*polarons*". In other words, *polarons* are quasi-particles deriving from the electron-phonon coupling (or local coupling), i.e. interaction between electrons and quantized modes of vibrational energy arising from atoms' oscillations in the crystal (phonons). The charge carrier mobility of an organic material strongly depends on the electron-phonon coupling, other than on the electronic and phononic bandwidth and phonon energy.

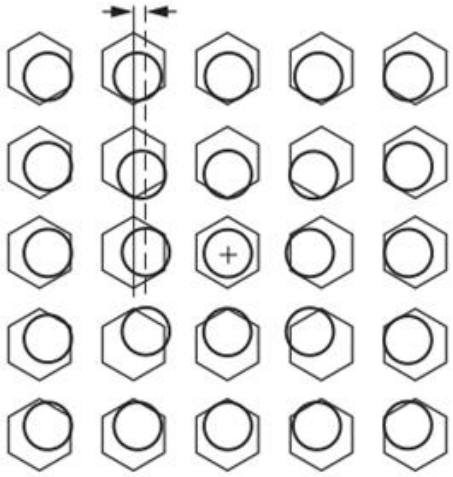

Fig. 1.8 *The figure is a schematic representation of the formation of a polaron when a positive charge is placed on a molecule in a conjugated organic solid. The hexagons symbolize the core of the nuclei, while the circles represent the delocalized π-electrons.*[7]

Hopping Transport

Charge transport in disordered organic semiconductors such as polymers is dominated by localized states. Charge carriers typically hop between these localized state leading to a diffusive, non-coherent transport with low mobility. Conwell and Mott suggested that in order to overcome the energy between two states the carrier absorbs or emits a phonon. In the case of a constant Density Of State (DOS) at low temperature, hopping over long distances becomes more energetically favorable than hopping to high energies. Hence the conductivity σ varies with temperature as

$$\sigma \propto \exp\left[-\left(T_0 / T\right)^{1/4}\right] \tag{1.11}$$

This is the well-known variable-range hopping model.

This model is based on the assumption that charges can hop a short distance with a high activation energy or a long distance with a low activation energy. The temperature dependence of charge transport in such systems is strongly dependent on the density of localized states. In OFETs, when a gate potential is applied, the channels begins to accumulate charge at the semiconductor-dielectric interface. As the charges fill the lower lying states, any additional charges will occupy higher energy states. Therefore these additional charges will require less activation energy to hop to a neighboring site. This

gives rise to a gate voltage dependent mobility. Based on this theory Vissenberg and Matters[8] developed a model based on percolation mechanisms. It assumes that transport is governed by the tail states of the Gaussian density of states (DOS) which is approximated by an exponential distribution:

$$N(E) = \frac{N_t}{kT_0} \exp\left(-\frac{E}{kT_0} \right) \tag{1.12}$$

where N_t is the total density of localized states, k the Boltzmann constant and T_0 is the width of the exponential distribution.

The resulting mobility gives the following expression

$$\mu = \frac{\sigma_0}{q} \left(\frac{\pi (T_0/T)^3}{(2\alpha)^3 B_C \Gamma(1 - T/T_0)\Gamma(1 + T/T_0)} \right)^{T_0/T} \left[\frac{C_i^2 (V_G - V_T)^2}{2kT_0 \varepsilon_s} \right]^{T_0/T - 1} \tag{1.13}$$

Vissenberg and Matters in Ref [8], used equation 1.13 in order to fit the temperature dependence mobility of pentacene and polythienylene vinylene (PTV) and found that the field effect mobility follows a simple Arrhenius behavior where

$$\mu_{FE} \propto \exp\left[\frac{-E_a}{kT} \right] \tag{1.14}$$

E_a is the activation energy which depends on the gate voltage V_G. It has been observed that E_a decreases with an increase in the gate potential V_G (negative) The decrease in E_a with increasing V_G is attributed to filling of charges at the lower-lying states. As a result, any additional charge carriers in the system will occupy sites with -on average- a higher energy and less energy will be required for the activated jumps to neighboring sites.

Multiple trapping and release

The multiple trapping and release (MTR) model is an alternative model which describes transport of charges along the localized levels in the vicinity a delocalized band edge. The basic assumption of this model is that the carriers arrive at a trap with a probability close to one and their release is controlled by thermally activated process. During their transit in the delocalized band, the charge carriers interact with the localized levels through trapping and thermal release (Fig. 1.9).

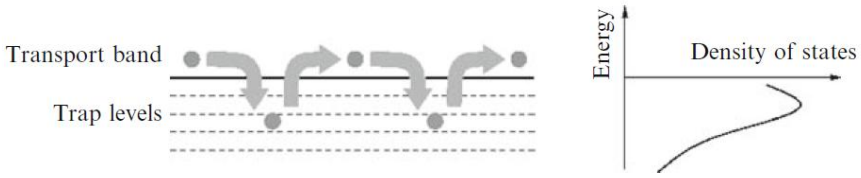

Fig. 1.9 *Principle of the multiple trapping and release limited charge transport*

The MTR model also predicts the dependence of mobility on gate voltage. When a potential is applied to the gate, a potential V_S is created at the dielectric-semiconductor interface. This results in the shift of the Fermi level towards the band edge, thus partly filling the DOS (Fig. 1.10). Hence, any additional charge carrier has its energy closer to the band edge which makes its thermal release easier and thus increases the mobility. The effective mobility is given by

$$\mu_{eff} = \mu_0 \frac{N_c}{N_t} \left(\frac{C_i (V_G - V_{th})}{qN_t} \right)^{T_0/T-1} \tag{1.15}$$

N_c is the effective DOS at the transport band edge.

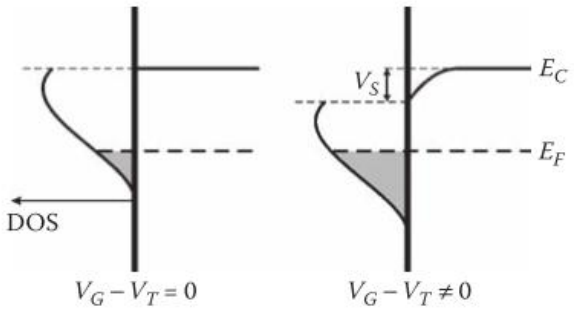

Fig. 1.10 *Gate voltage dependent mobility induced by an energy distributed density of traps.*

1.5 Relevance of interfaces in OFETs

Organic electronics has been heavily studied in the last decade due to its potential application in cheap, light-weighted flexible electronics and more recently in organic bioelectronics. Example of the state of the art organic electronic devices include Organic Photovoltaics (OPVs), Organic Light Emitting Diodes (OLEDs) , Organic Field Effect Transistors (OFETs) and Organic bioelectronic devices. These devices are basically fabricated by stacking together materials of various nature such as the organic

semiconductor, metal electrodes and the insulator. Interfaces plays a crucial role in determining their performances.[9] Their operation depends on specific interaction and charge transfer processes occurring at interfaces of various material. For instance, in the case of OPVs separation of charges occurs at the interface between the donor and acceptor layer. These charges, which are separated, are then transported through the semiconducting layers and finally collected by the electrodes. The efficiency of such devices relies on the quality of the interfaces.

The aim of this thesis is to investigate interactions and charge transfer at various interfaces in an OFET. I chose an OFET as a model system to study the various interfaces as it offers different interfaces and a pretty simple geometry and operation as compared to other organic electronic devices (Fig.1.11). From electrical characteristics of an OFET, I can extract relevant charge transport parameters.

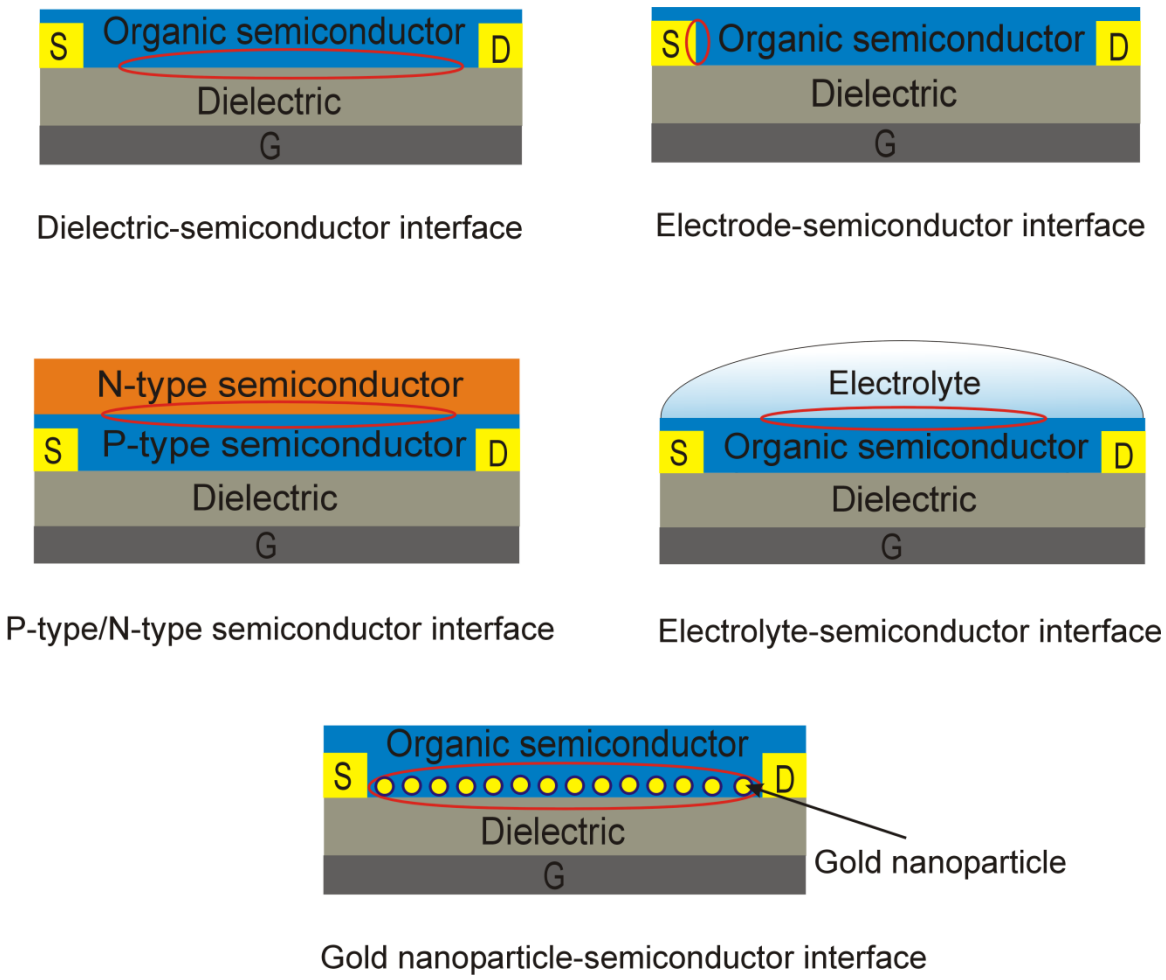

Fig. 1.11 *Interfaces that can be studied in an OFET.*

The **dielectric-semiconductor interface** is the most relevant interface in a transistor as the conducting channel where charges are transported from the source to the drain occurs at this interface.[10] Hence, charge transport is highly dependent on the quality of this interface. Its nature is however dependent on various factors such as the type of dielectric used and the morphology of the organic semiconductor deposited on the dielectric. In our case, for the bottom contact bottom gate configuration, the dielectric that I have used for most of the experiment is the thermal silicon oxide (SiO_2). Silicon oxide on the one hand is a technologically relevant substrate as it has proven to be a good quality dielectric having a low roughness of about 0.2 nm. Organic semiconductors such as pentacene and sexithiophene has shown well ordered growth on this substrate with a defined morphology. On the other hand, the oxide surface contains some defects such as the OH groups which acts as traps for the transport of charges. One way to optimize this, is to modify the surface using Self Assembled Monolayers SAMs such as Hexamethyldisiloxane (HMDS) or Octadecyltrichlorosilane (OTS)[11]–[13]. Apart from the interface between the dielectric and the semiconductor, another interface that comes into play is the one between adjacent organic semiconductor layers In the case of small molecule organic materials like pentacene or sexithiophene, the growth condition determines the morphological details of the thin film. Verlaak *et. al.* have shown how the rate deposition of the material and substrate temperature can determine the dimensionality of nucleation of the island.[14] The pentacene growth reported in this thesis follows a growth transition of 2D+3D which means that we have the first few monolayers growing in 2D and then the roughening starts after the second or third monolayer. In chapter 3 of this thesis, I have addressed the role of both the dielectric and the morphology of the semiconductor in the performance of an OFET. A comparative study on the evolution of electrical characteristics of an OFET fabricated on an untreated SiO_2 and HMDS treated SiO_2 was studied *in situ* real time during growth of the semiconductor (pentacene). Temperature dependent study was also performed in order to have a deeper insight into the transport phenomena taking place in the device. By fitting our data with a modified Vissenberg and Matters model, I was able to rationalize the dimensionality of the transport of charges and eventually characterized defects as a function of film thickness.

Another interface that has to be taken into account is the **electrode-semiconductor interface.** This interface determines the charge injection at the source and charge retrieval at the drain . In an ideal OFET, the source and drain contacts are ohmic. This means that

the contact resistance is negligibly small compared to the channel resistance or the electrical resistance of the channel. As depicted in Fig 1.10, the three resistances R_{source}, $R_{channel}$ and R_{drain} can be thought as three resistances in series. The resistance with injection and collection steps can be grouped as contact resistance R_c while the resistance associated with crossing the channel in the semiconductor is the channel resistance $R_{channel}$. For an ohmic contact $R_c << R_{channel}$. [7] Contact resistance depends not only on the electronic structure or band alignment at the electrode-semiconductor interface but also depends on the geometry of the device and the fabrication process.

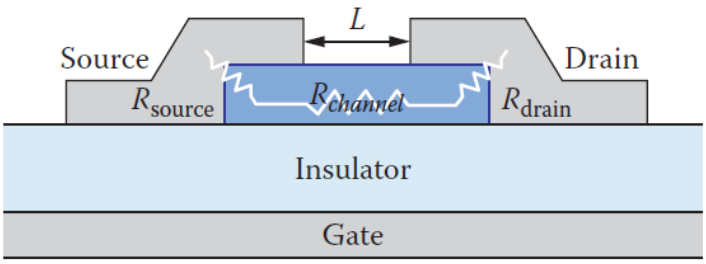

Fig. 1.12 *Schematic of an OFET showing the source contact resistance R_c, channel resistance $R_{channel}$ and the drain contact resistance R_{drain}.*

So far, I have spoken of a unipolar OFET where the semiconductor can transport just one type of charge i.e. electrons or holes which means that the semiconductor is either p-type or n-type. However, we can have a second type of OFET called the ambipolar OFET. An ambipolar OFET is one in which both electrons and holes can be accumulated in the channel of the transistor depending on the applied voltages. The semiconductor in this case can be either ambipolar in nature or it can be a combination of two layers where one layer is composed of an n-type semiconductor stacked together with a layer of a p-type semiconductor. Dodabalapur and co-workers first demonstrated organic heterostucture FET by combining layers of the hole-conducting α-hexathienylene (α-6T) and the electron conducting C60. [15] Since then, a lot of researchers have tried to explore other combination of p-type and n-type materials to obtain an ambipolar transistor and demonstrated that these device can be used as inverters.[16]–[18] Other applications such as OPVs and OLEDs have been realized by combining the p- and n-type semiconductor. The optimization and fine tuning of these device depends on the charge transport occurring at the **p-type-n-type semiconductor interface.** There are many factors that determine the quality of this interface such as the alignment of their energy levels, the

interface geometry and interface morphology. In Chapter 5, I will report our findings on the charge transport and percolation processes taking place at the heterojunction between pentacene (a p-type semiconductor) and C60 (an n-type semiconductor). Most importantly, I will demonstrate how the *in situ* real-time technique allows us to relate the interplay between the interface morphology to charge transport taking place at the p-n heterojunction.

The fourth interface that attracts the attention of most researchers today is the **electrolyte-semiconductor interface.** This interface is central for coupling organic electronics with biological systems. A new device architecture which I have employed to study this interface is the Electrolyte Gated Organic Field Effect Transistor (EGOFET). The basic operation of this type of transistor is similar to the traditional OFET except that for the dielectric. In this case, the electrolyte acts as a dielectric and a metal electrode immersed in the solution acts as a gate electrode. The large capacitive coupling between the ionic charges in the solution and the electric charges in the semiconductor give rise to the Debye Helmholtz (DL) layer . In Chapter 6 of this thesis, I will report the value of the capacitance of the DL layer in pentacene based-EGOFETs by employing the dual gate measurement technique.[19][20]. Furthermore I will discuss on the role of water in the instability of OFETs.

Due to an increasing interest in neuromorphic electronics based on new technology other than the traditional silicon CMOS , a new device called the Nanoparticle Organic Memory Field Effect Transistor (NOMFET) was developed. This device was designed to mimic the human synapse.[21], [22] Pentacene based NOMFETs works on the principle based on the charge trapping/detrapping in an array of gold NanoParticles (NPs) at the SiO_2/pentacene interface. Currently NOMFETS are limited to operation at high potentials (> 10 V) and at slow operation frequencies (< 50 Hz). Due this limitation, in Chapter 7 of this thesis, I studied the charge transport phenomena occurring at the **nanoparticle-semiconductor interface** in order to understand the transport limitations in NOMFET. A series of in situ experiments was carried out where electrical characterization was performed during the growth of pentacene on a network of nanoparticles.

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Chapter 2 Experimental techniques, materials and methods

This chapter includes a discussion on the materials used for the fabrication of the devices, the main experimental techniques and the characterization techniques carried out for the experimental work that is reported in this thesis.

2.1 Substrates and materials

The substrate used for the fabrication of OFETs for the work reported in this thesis is a test pattern manufactured by FBK (Fondazione Bruno Kessler, Trento, Italy).

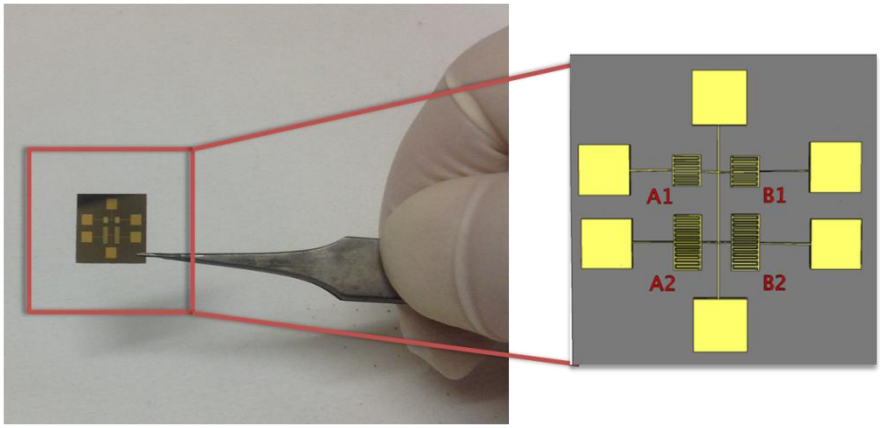


Fig. 2.1 *Trento test pattern (Left) depicts the photographic picture of the test-pattern and (right) shows a schematic drawing. A1,B1,A2 and B2 are the names given to the four transistors according to their geometry and position.*

The Test Patterns (TPs) as shown in Fig 2.1 were fabricated on a heavily doped Silicon wafer, 500 µm thick, with a resistivity of 0.01– 0.03 Ω*cm. 200 nm thick SiO_2 was thermally grown to make a dielectric layer. The capacitance of the dielectric is 17.25 nF/cm^2. Interdigitated Au electrodes (125 ± 25 nm thick) were photolithographically patterned onto the SiO_2 by using Chromium adhesive layer (3–5 nm). On each test pattern, there are four transistors consisting of different channel length *L*=20µm and 40µm and channel width *W*=11200µm and 22400µm respectively. The *W/L* ratio for all the four transistors is 560. A1, B1, A2 and B2 are the names assigned to the different transistors taking into account their geometry and position.

Prior to the fabrication of devices, the TPs were heavily cleaned by following a standard protocol. The protocol consists the following procedure:

i. We first rinse the TPs with acetone in order to remove the photoresistive layer , followed by blowing it with dry nitrogen.

ii. Then we dip the TPs in hot piranha (H_2SO_4:H_2O_2, 1:1) for 15 mins in order to remove organic contaminants. After that, the TPs are then rinsed de-ionised water and blowing with dry nitrogen.

iii. The last step consists in the etching of the silicon oxide by dipping it in HF(2%) solution for 5 seconds, followed by rinsing with de-ionised water and blowing with dry nitrogen.

iv. The TPs are then kept for 24 hours in a sealed petri-dish prior to the deposition of any organic material.

2.1.1 Surface modification

The performance of an OFET relies on the quality of the dielectric-semiconductor surface. The dielectric surface such as silicon oxide consists of terminated hydroxyl groups on the surface which acts as trap states that hinders the transport of charges. For this reason, we have modified the surface of the silicon oxide by a treatment with Hexamethyldisiloxane (HMDS). HMDS acts as a coupling reagent which reacts with OH-terminated SiO_2 and leaves $(CH_3)_3$-Si-terminated ones. Moreover the HMDS layer on the silicon oxide does not alter the morphology of the pentacene film growth.

The functionalization procedure of the silicon oxide surface with HMDS is done immediately after cleaning the substrate using the cleaning protocol discussed in Section 2.1. HMDS deposition was achieved by thermal evaporation of the molecule onto the substrate. Fig. 2.2a depicts the experimental set up for the functionalization process while fig. 2.2b and 2.2c show the surface of silicon oxide before and after the functionalization with HMDS repectively.

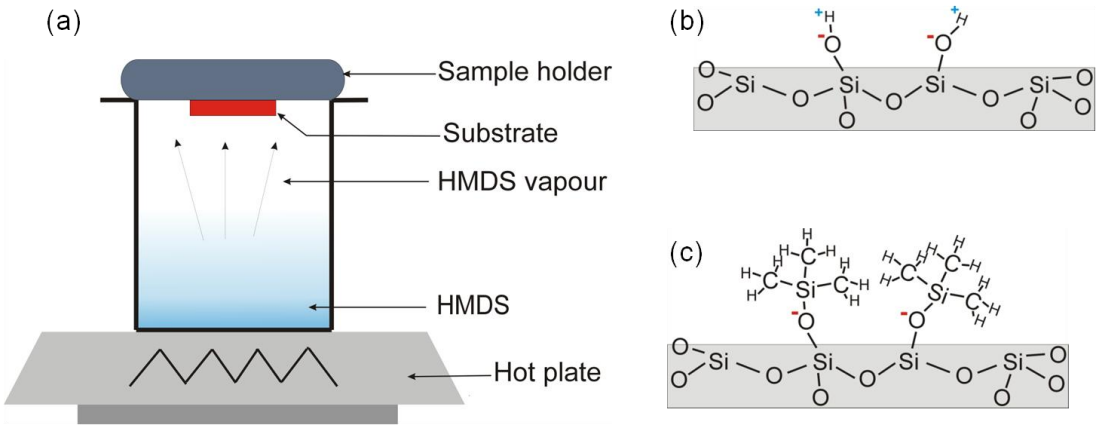


Fig. 2.2 *HMDS functionalisation of the substrate (SiO_2). (a) depicts the protocol used for functionalizing the SiO_2 surface (b) shows a chemical structure before the HMDS-functionalization and (c) shows the chemical structure where HMDS binds to the surface.*

2.2 Semiconductor deposition

The most crucial part in the OFET fabrication is the deposition of the organic semiconductor. The preparation of small molecule organic semiconductor such as Pentacene , C60 or PDI was done by high vacuum sublimation while in the case of polymers such as P3HT, the preparation was performed by spin coating.

2.2.1 High vacuum sublimation of small molecule organic semiconductors

In this section I will describe a system used for the growth of pentacene on the TPs for *ex situ* experiments described in chapter 6. A more sophisticated system which was used for most of my research activities which integrates growth and electrical characterization will be discussed later in Section 2.5.

The growth of organic molecules such as pentacene, sexithiophene or perylene was carried out on a high vacumm chamber which consists of a Knudsen cell, quartz crystal microbalance, shutter and sample-holder. A photographic image of the system is shown below in fig 2.3.

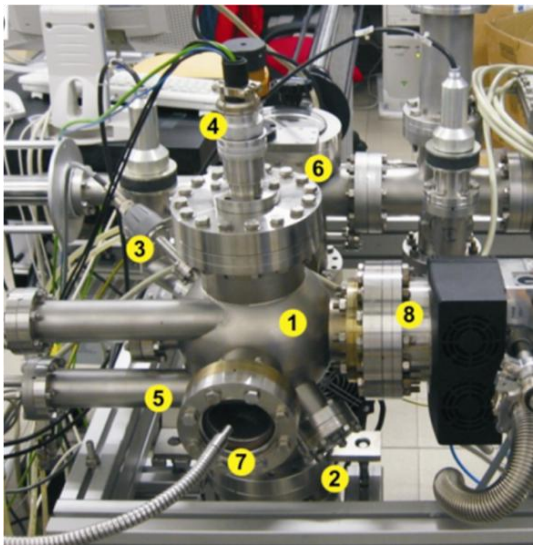


Fig. 2.3 *(a) HV sublimation chamber. The main elements are: (1) HV chamber; (2) Knudsen cell; (3)quartz crystal microbalance; (4) sample-holder manipulator; (5) shutter; (6) fast-entry; (7) viewport + light, for optical monitoring; (8) connections to turbomolecular and scroll pump*

Pentacene was purchased from Sigma-Aldrich. Once the material is filled into the knudsen cell , purification of organic materials is carried out in order to assure that the grown thin-film is reasonably free of impurities which may act as traps or dopants in an electronic device . There are several techniques for purification. The simplest technique is the outgassing, which is what we used . Outgassing consists of heating the organic material close to the sublimation point in HV for a few hours. This allows removal the traces of solvent and smaller oligomers or lighter precursors. Once outgassed, pentacene is kept under HV. Growth in a HV environment assures that a minimal density of impurities and defects will be incorporated into the film. The degree of impurities which may be deposited on the substrate depends on the quality of the vacuum .Vacuum sublimation of pentacene was carried out at a pressure of 10^{-8} mbar and at a growth constant rate of 7Å/min up to a desired thickness. The thickness of the layers is monitored using a calibrated quartz microbalance. After the growth of the semiconductor, the sample is then taken out of the HV chamber for electrical and surface characterization.

2.2.2 Spin coating

Polymers such as poly-(3-hexyl-thiophene) (P3HT) on the other hand require another fabrication technique known as spin coating. P3HT was purchased from Sigma Aldrich

and used without further purification. The molecular weight was between 15000 and 45000 g/mol and the regio-regularity was >98%. P3HT was spin-coated from dichlorobenzene, with a concentration of typically10mg/ml. The resulting film thickness was between 50 nm and 100nm depending on the concentration and spin-coating speed. The transistors were subsequently annealed at 150° for 1 hour, in order to remove any remaining solvent.

2.3 Electrical measurement set up

Electrical measurements of OFETs were performed both in air and in vacumm. The device structure that we have for most of our OFET measurement reported in this thesis is the bottom gate bottom contact configuration (except for the EGOFET measurements). A photographic image of the measurement set up system is shown below.

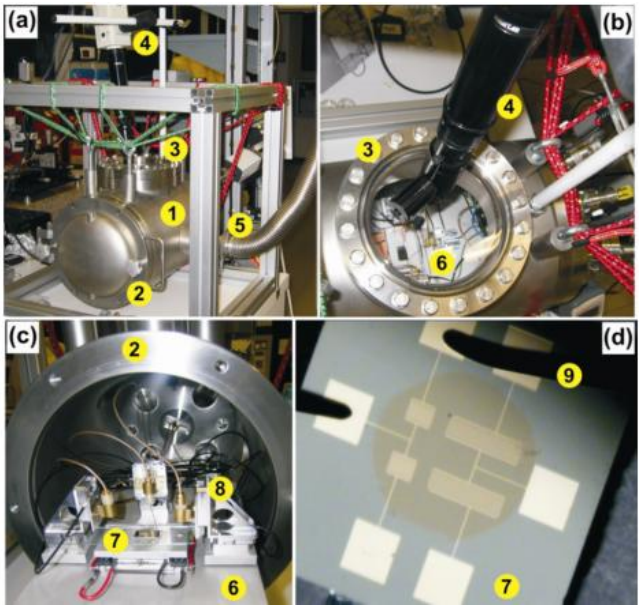


Fig. 2.4 *System for electrical measurements under controlled atmosphere. (a) Main view: (1)UHV chamber; (2) front entry; (3) viewport; (4) video camera; (5) pumping connection. (b) Top view. The sliding tray (6) is visible inside the HV chamber. (c) Interior view of the HV chamber showing the test pattern (7) and the piezoelectric motors (8). (d) View of a test pattern; the probes (9) which are connected to the piezoelectric motors are approached on the source and drain contacts by means of a video camera-assisted joystick which moves the piezoelectric motors.*

The system is shown in figure 2.4. It consists of a HV chamber (1) with front entry (2); a top viewport for optical monitoring (3) of the inside through a video camera (4); feedthroughs for gases (controlled by leak valves) and the electrical connections. Coaxial

cables are used for connecting the probes to the external measurement unit, in order to reduce environmental electrical noise. The measurement unit consists of a general purpose dual channel source/meter unit Keithley 2612, which is remotely controlled by a software as shown in fig. 2.6 The electrical connections of the three probes to the measurement unit are schematically shown below in fig. 2.5.

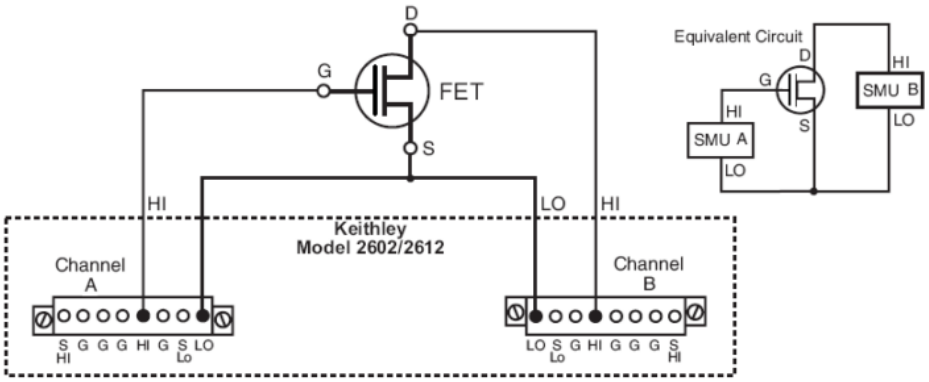


Fig. 2.5 *Connection of Keithley 2612 source/meter unit to the integral system for electrical measurements under controlled atmosphere. The gate probe is connected to the HI terminal of channel A, the drain probe is connected to HI terminal of channel B, and the source probe is connected to both LO terminals of channel A and channel B*

The measurement software as shown in Fig 2.6 is designed in such a way that it allows the user to perform different types of electrical measurements such as current-voltage characteristics of a transistor, output characteristics, capacitive current measurement, pulse measurement, current as a function of time and voltage as a function of time. The data curves are shown in the window of the program and it gives us the ability to plot the curve in logarithmic scale.

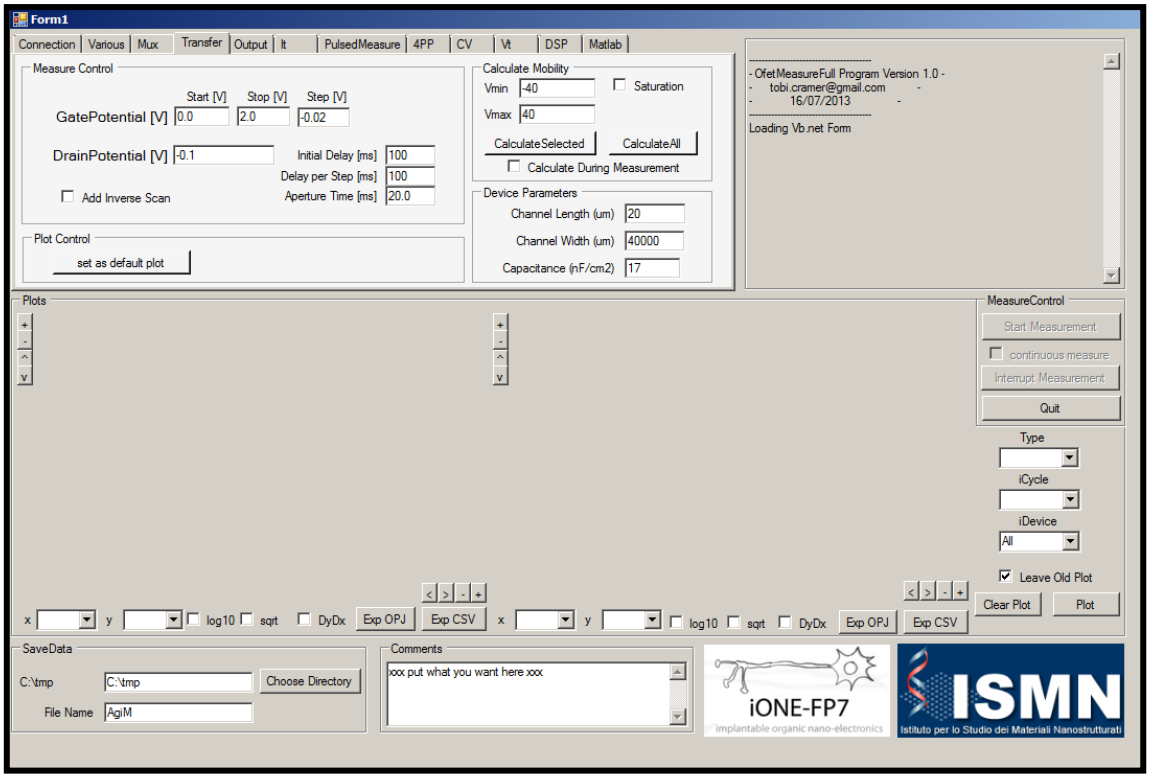


Fig. 2.6 *Software to control parameters and timing for the electrical measurement*

2.4 Electrical characterization and extraction of transport parameters

The evaluation of electrical performances of an OFET is carried out by performing standard electrical characterization which can be classified into:

i. Transfer characteristics

ii. Output characteristics

i. Transfer characteristics

An OFET is electrically characterized by measuring the current flowing from the source to the drain (I_{SD})when a voltage is applied to the gate (V_G). The source is normally grounded while a potential is applied to the drain. A plot of the current versus the gate voltage at a certain drain bias is called the transfer characteristics or the *I-V* curve. There are two operation regimes depending on the potential applied to the drain i.e linear regime and saturation regime.

For linear regime,

$$I_{DS} = \frac{W}{L} C_i \mu (V_{GS} - V_{th} - \frac{V_{DS}}{2}) V_{DS} \qquad for\ V_{DS} < V_{GS} - V_{th} \tag{2.1}$$

For saturation regime,

$$I_{DS} = \frac{W}{2L} C_i \mu (V_{GS} - V_{th})^2 \qquad for\ V_{DS} \geq V_{GS} - V_{th} \tag{2.2}$$

Where W and L are the width and length of the channel respectively, C_i is the capacitance (unit of F/cm^2) of the dielectric , μ is the charge carrier mobility and V_{th} is the threshold voltage.

For recording transfer characteristics in bottom gate bottom contact configuration

- We sweep the potential applied to the gate V_G from +30V to -30V
- Keep the drain potential V_D constant at either -1V or -30V (depending if the measurement is done in the linear or saturation regime)
- Measure the current flowing in the channel of the transistor from the source to the drain I_{DS}.

The resulting plot of I_{SD} versus V_G is called the transfer characteristic plot or the Current-voltage *I-V* curve of the transistor. From this *I-V* curve, relevant transport parameters can be extracted viz.

a) Charge carrier mobility μ

b) Threshold voltage V_{TH}

c) On/Off ratio $I_{ON/OFF}$

d) Pinch on voltage V_{ON}

e) Subthreshold slope SS

A typical characteristic transfer curve operated in the linear and saturation regime is shown in Fig 2.7. By analyzing the curve using eq. 2.1 for linear regime and eq. 2.2 for saturation regime, one can extract the value of mobility of charge carriers μ and the

threshold voltage $V_{th.}$. Charge carrier mobility can be expressed in simple words as the speed of the majority of charge carriers (holes/electrons) in which it is transported in the semiconductor material. It is extracted by taking the slope of the linear part of I_{DS} vs V_{GS} when measured in linear regime while in the case of saturation regime , it is taken from the slope of the linear part of sqrt(I_{DS}) vs V_{GS}.[1]The threshold voltage on the other hand is defined as the gate voltage potential at which the conduction channel is created in the organic semiconductor. It is extracted by taking the intersection of the extrapolated linear part of the transfer curve.

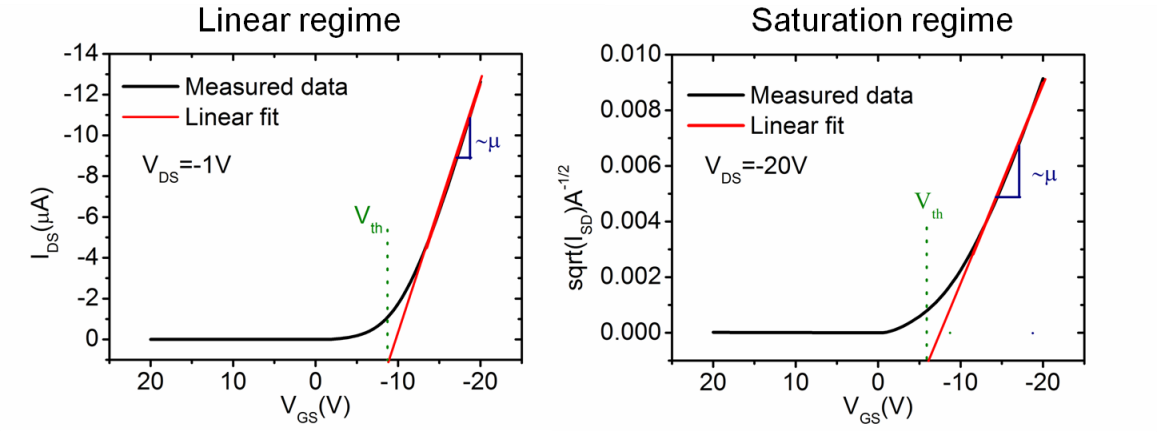


Fig. 2.7 *Typical transfer characteristics obtained for pentacene based OFETs. (Left) Measurements performed in the linear regime and (Right) measurements done in the saturation regime.*

The other parameters that can be extracted from the transfer curve in the semi-logarithmic plot is the Subthrehold slope SS, Pinch on voltage V_{ON} and the *ON/OFF* ratio.

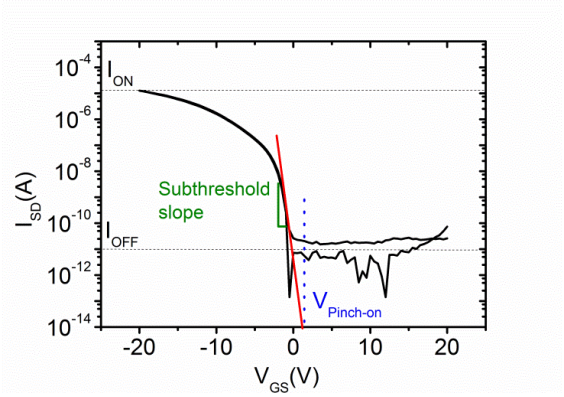


Fig. 2.8 *Transfer curve plotted in semi-log scale. The slope of the linear fit gives the subthreshold slope and the intercept yields the pinch on voltage*

The sub- threshold swing *SS* (expressed in mV/decade) is a measure of how rapidly the device switches from the off state to the on-state and is extracted from the steep region of the I_{DS} trend. V_{ON} is the voltage at which I_{DS} increases above the noise level of the off-current. On/off ratio between the maximum and minimum value of the current I_{DS} is an estimate of the amplification.

ii. Output characteristics

The output characteristics of an OFET is a measure of the source drain current as a function of the source drain voltage for different gate voltages. Fig. 2.9 shows a typical output curve of an OFET. In an output curve the linear and the saturation regime can be distinguished. Moreover, the shape of the output curve gives us an information of the contact resistance that is present/absent in our device.

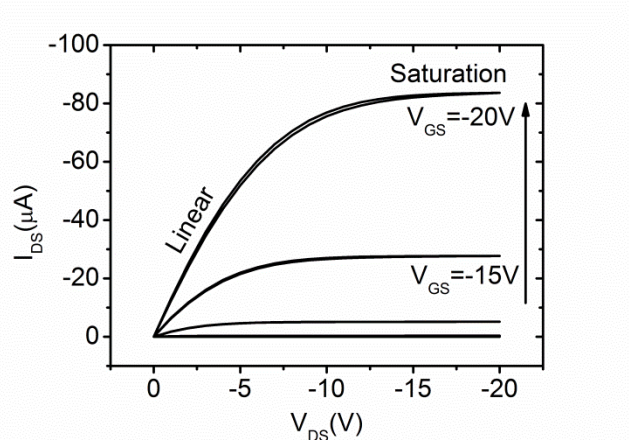


Fig. 2.9 *Typical output characteristics of a p-type OFET.*

2.5 *In situ* and real time electrical characterization

The *in situ* real time electrical characterization system is a home build system that allows us to carry out a complete electrical investigation of OFETs during semiconductor deposition (real-time), and after deposition by keeping the environmental parameters unchanged (*in situ*). [2]

The electrical response of a thin film transistor, on one hand depends on the growth conditions of the thin film (intrinsic properties), on the other hand, it is being influenced by environmental conditions (extrinsic effects) due to the sensitivity of organic thin films to oxygen, humidity, and light. For this reason, it is not simple to discriminate

the intrinsic and extrinsic effects on the electrical performance, especially when the thickness of the semiconductor is just a few molecular layers, as in ultrathin-film transistors used for sensing applications. A possible way to minimize the influence of extrinsic effects is the integration of the organic thin-film growth and the electrical characterization in the same high-vacuum system, *in situ*. For the case of small molecule semiconductors as in our case, the electrical properties of the OFET is strongly correlated to the morphology and thickness of the semiconductor. Due to this reason, real time electrical characterization of OFET during growth of the semiconductor is important for relating charge transport parameters vs film thickness.

Furthermore, the ability to carry out temperature dependent measurement of the electrical characteristics of the transistor *in situ* just after the deposition allows us extract information of how mobility of the charge carriers varies as a function of temperature. This information is important if we want to understand the charge transport phenomena such as band-like transport in the case of single crystals or hopping like transport in the case of organic semiconducting materials.

To sum up, the main advantages of the *in situ* and real-time electrical measurements can be listed below:

- The intrinsic electrical properties of the thin film transistor can be systematically investigated;
- The electrical properties of the OTFT can be measured as a function of the growth of the molecular layers;
- The growth phenomena of the semiconducting film forming the channel of the OFET can be directly correlated to its electrical performance
- Temperature -dependent measurements give a deeper insight into the charge transport processes taking place.

2.5.1 The experimental set-up

The *in situ* real time electrical characterization chamber consists of two stacked chambers pumped independently: the upper chamber and the lower chamber as shown in fig. 2.10. The two chambers are divided by a pneumatic gate valve connected through standard

ultrahigh-vacuum (UHV) CF63 stainless steel flanges. The sample-holder is mounted on the upper chamber, while the lower chamber is used to keep the organic material under High Vaccum (HV) condition. The upper chamber is pumped through a turbomolecular pump (Varian TV 81-M) via one multiport CF100 coupled to a tee CF40.

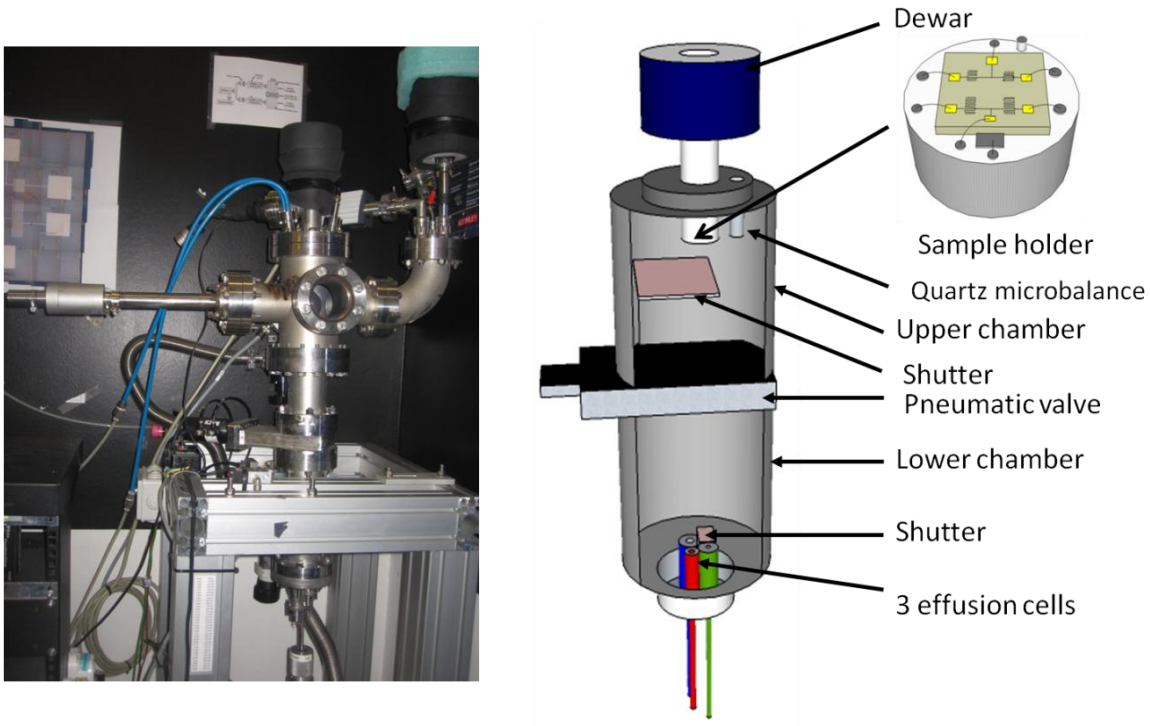


Fig. 2.10 *(Left) A photograph of the home built in situ real time system (Right) a schematic diagram depicting the different parts of the system.*

The sample holder is the unique part of this system as it allows electrical connection to the sample (Test Pattern) prior to the real time experiment. In addition the design of the sample holder allows us to vary the temperature of the substrate from ~-170°C to + 200°C. The cooling down of the sample is achieved by introducing liquid nitrogen onto the dewar which consists of a cold finger that is attached behind an insulating plate 'shapal' which has a good thermal conductivity. Likewise heating of the substrate is attained by a heater coil mounted in between as shown in fig. 2.11a.

Electrical connections from the sample holder to the test pattern is made by bonding the copper wires with a conductive silver paste as shown in Fig. 2.11b (left). A shadow mask is mounted over test pattern (fig. 2.11b (right)) in order to confine the area of pentacene

deposition on the channel of the transistors and also to avoid leakage current due to pentacene touching the edges of the silicon oxide.

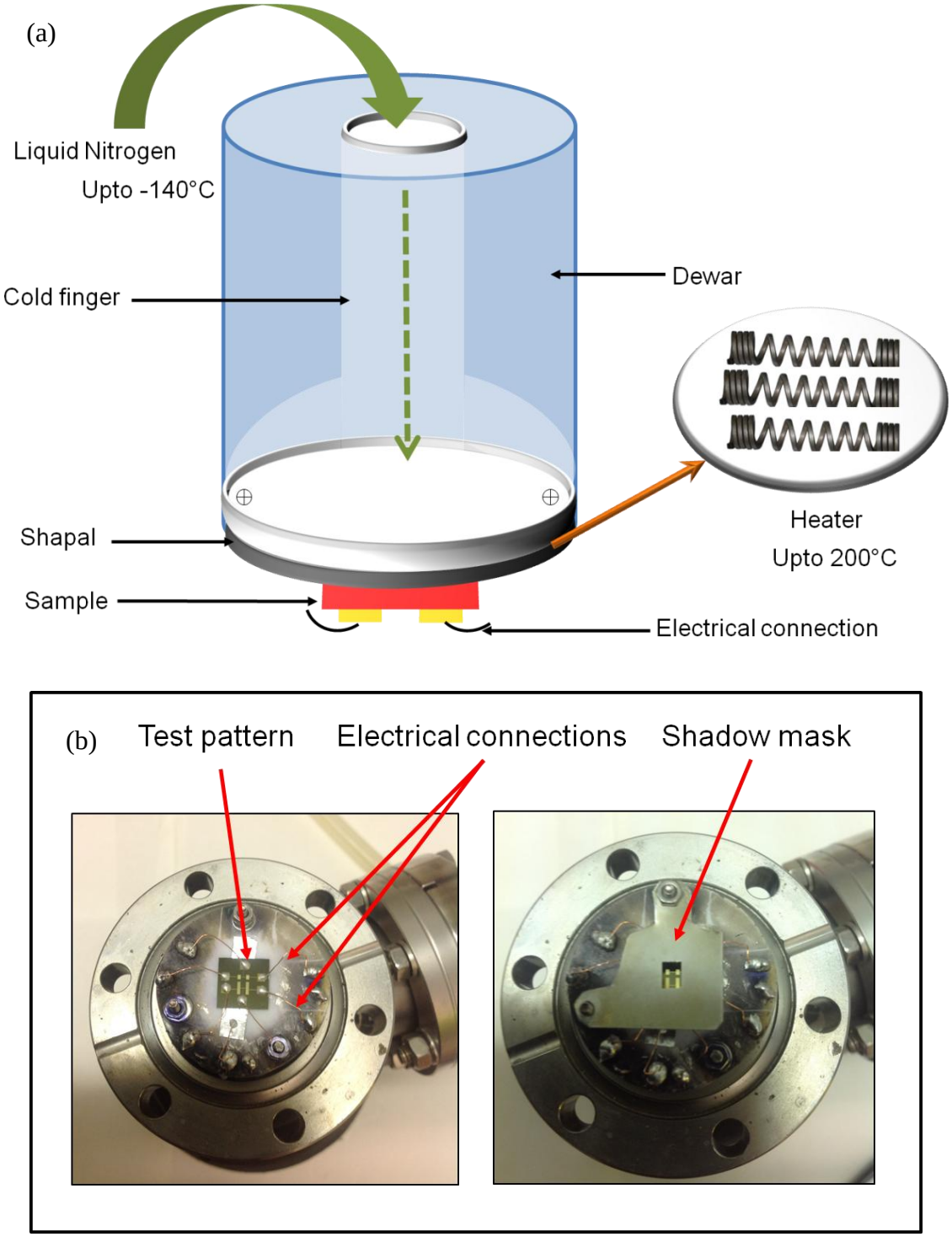


Fig. 2.11 *(a) A sketch of the sample holder showing the cold finger into which liquid nitrogen can be filled in order to cool down the sample and a heater for heating up the sample (b) Sample holder consisting of the test pattern into which electrical connections are made. On the right, the shadow masked is shown to be mounted on top of the test pattern for confining the area of the semiconducting film.*

The deposition rate and the thickness of the organic semiconductor is monitored using quartz crystal microbalance (QCM) (Sycon STM-100/MF). In order to increase the accuracy of the measurement and reduce the thermal drift, the temperature of the sensor is constantly kept at 20°C, through a cooling coil. The quartz sensor and its cooling coil are mounted on the multiport CF100 via CF16 feedthroughs. The shutter protects the sample from the subliming material and, coupled to a magnetic manipulator, is moved aside when deposition starts. The upper chamber pressure is measured by the ion gauge (Ionivac ITR90).

The lower chamber, connected to a turbomolecular pump (Pfeiffer TMU 071YP), contains the home-built effusion cell. There are three effusion cells in total. The effusion cells consist of a fused quartz crucible inside a structure made of boron nitride shrouded by a heating tantalum wire. An additional shutter is positioned over the crucible to mask the molecular beam.

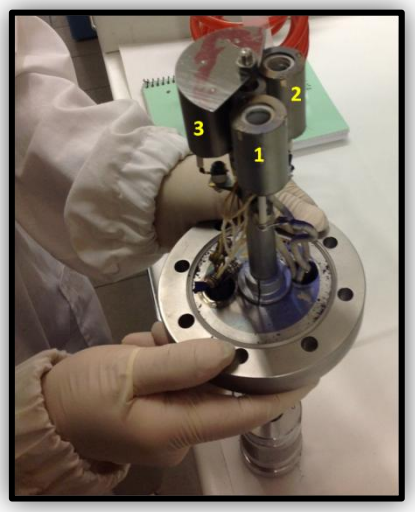


Fig. 2.12 *Three home built effusion cell mounted in the in situ system that can contain three different types of semiconductor.*

The three effusion cell temperature is monitored through their respective thermocouple (J-type) and is controlled by a proportional-integral- differential (PID) microcontroller. Good control of the effusion cell temperature ensures the stability of the deposition rate during growth. Once the crucibles are refilled, the lower chamber is kept under HV during all the time until the next refilling, in order to keep unchanged the physical–chemical properties of the organic semiconducting materials. Consequently, the

reproducibility of the growth conditions from run to run is improved, leading to good reproducibility of the electrical behavior. Both turbomolecular pumps are connected through manual valves to a dry scroll pump (Varian SH-1001) for the rough pumping. The system reaches a base pressure of 2×10^{-6} mbar after 5–6 h of pumping and 1×10^{-7} mbar after baking.

2.5.2 The electrical measurement set up

The TP electrodes are connected to the external source measuring units (SMU), in order to bias gate (G), drain (D) and source (S) and to measure the drain current I_D and gate current I_G. In total three transistors can be measured simultaneously at the same time. As shown in fig. 2.14, , two SMUs both Keithley 2612 were used for the measurements. A TSP link connector communicates the two SMUs together. While the gate bias is applied from the Channel A of SMU 1, the drain current of the three transistors is measured in channel B of SMU 1 , channel A SMU 2 and Channel B of SMU 2 respectively.

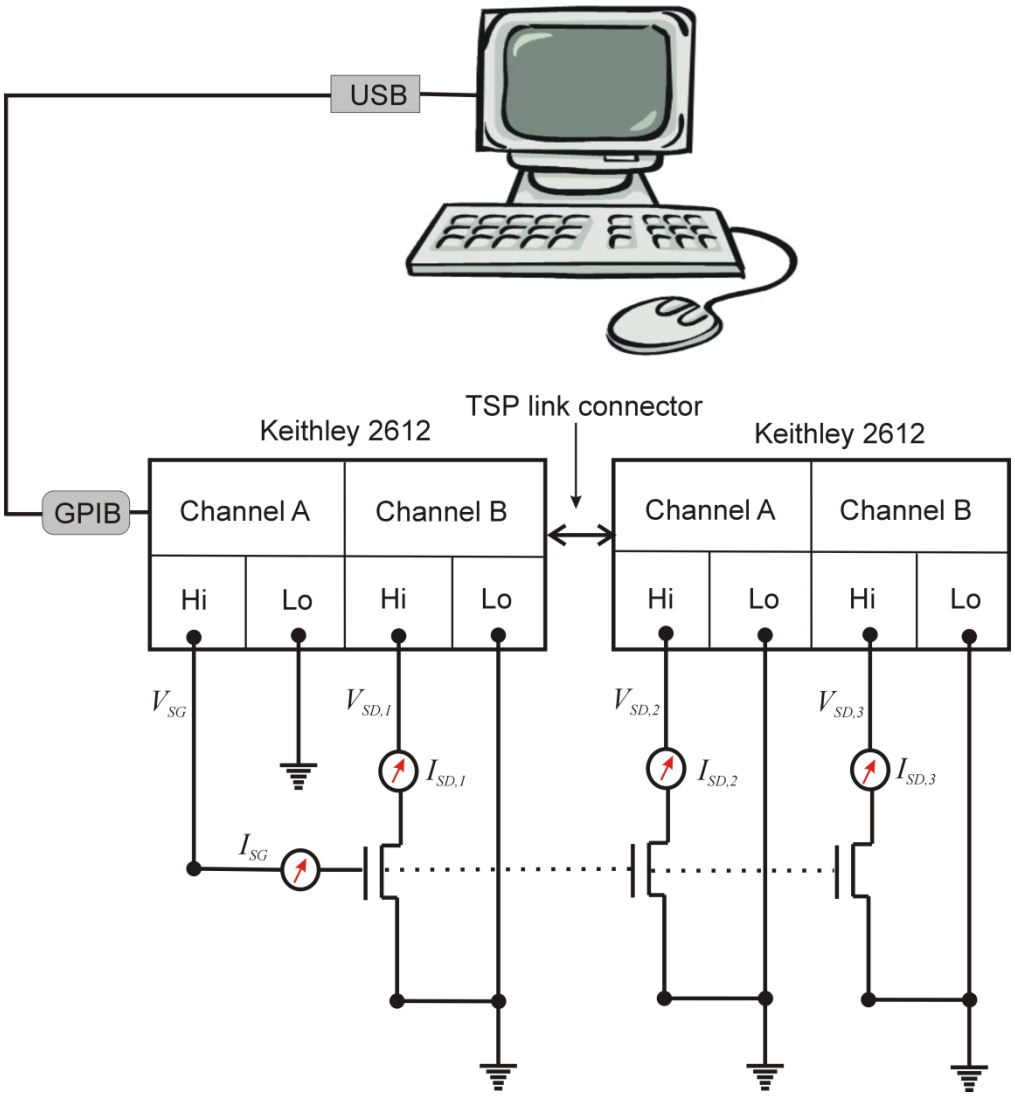


Fig. 2.13 *Schematic diagram of the main electrical connections to the Source measuring units and the computer.*

2.5.3 *In situ* real time experiment software

A sophisticated software was developed in order to synchronized two source measuring units (SMUs) and to control the parameters used for the *in situ* real-time experiments. Apart from the voltage parameters, the timing for recording the current voltage (IV) transfer characteristics is crucial. On one hand, real time measurements should be as fast as possible in order to record the electrical characteristics during every small changes in the film thickness during growth while on the other hand, fast measurement could lead to a higher noise level. Another factor that has to be taken into consideration while choosing the timing parameters is the mobility of the charges. For devices having low mobility, one has to take into consideration that an *I-V* measurement cannot be as fast as for the other

devices with a higher mobility. For pentacene based OFETs , we were able to record a reasonable *I-V* curve every 3 seconds. This implies that we performed electrical measurement every 0.4 Å when the deposition rate is 7 Å/min.

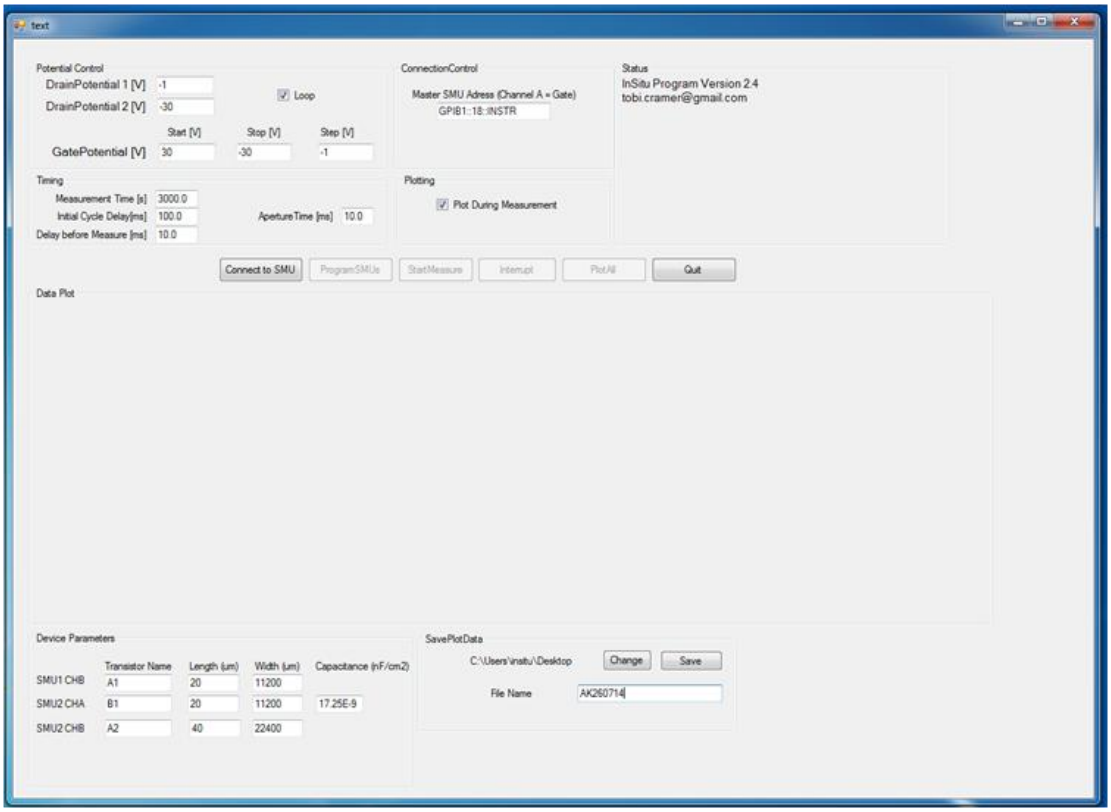


Fig. 2.14 *In situ real time program.*

The *in situ* real time program that I have used for controlling the measurements is shown in Fig. 2.15. For the potential control we have drain potential 1 and drain potential 2. This allows us to enter the different drain potential which we want to apply during the experiment. We can enter a drain potential for measuring in the linear regime and the other for measuring in the saturation regime. In this manner, we are able to record transfers simultaneously in linear and saturation regime during the growth of the semiconductor. In the gate potential window, we can enter the gate voltage scan for the measurement and it is possible to choose if we want to do the loop scan or not. Typical voltage parameters are : Gate potential sweep from +30V to -30V ; Drain potential -1V (for linear regime) and -30V (for saturation regime).

The other important parameter which is to be taken into account as mentioned earlier is the timing parameters. There are four different timing parameters viz. (1) Initial Cycle delay (2) Delay before measure (3) Aperture time.(4) Measurement time.

(1) Initial cycle delay is the time before the start of one measurement cycle or before sweeping a completer transfer scan. (~100 ms)

(2) Delay before measure is the given to the SMU when a potential is applied before taking the value of the current at that certain potential. (~10 ms, 20 ms and so on)

(3) Aperture time is the timing window during which the measurement point is recorded. (~10ms -20ms).

(4) Measurement time is the total time required to run the experiment.

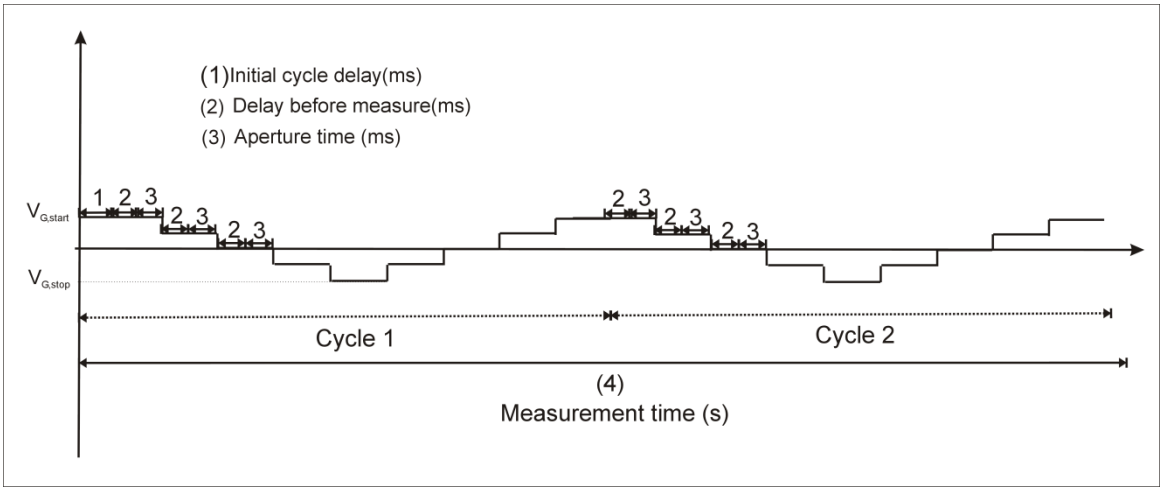


Fig. 2.15 *Timing parameters which control the in situ experiments*

At the bottom of the program (fig 2.12) there is window where we enter the device parameters. Here we can assign a name to the three different transistors and enter their respective channel geometry such as the width W and the length L . Moreover, we can enter also the capacitance of the dielectric in units of nF/cm^2.

2.5.4 *In situ* real-time data analysis

The in situ real time experiment requires that a transfer curve is recorded every 3 seconds during growth. The growth rate of the semiconductor that we have chosen is 0.6-0.7nm/min . For example, if we want to grow about 15nm of pentacene , we need to run the transfer scan for atleast 20-30 minutes. This will give rise to a huge number of transfer curves obtained for one *in situ* experiment. Hence the data analysis in order to extract relevant transport parameters such as mobility, threshold voltage , pinch on voltage and so on is done by MATLAB. The extracted values of the transport parameters

is then plotted as a function of film thickness. An example of the analysis of the data recorded during the growth of pentacene is shown in fig. 2.16.

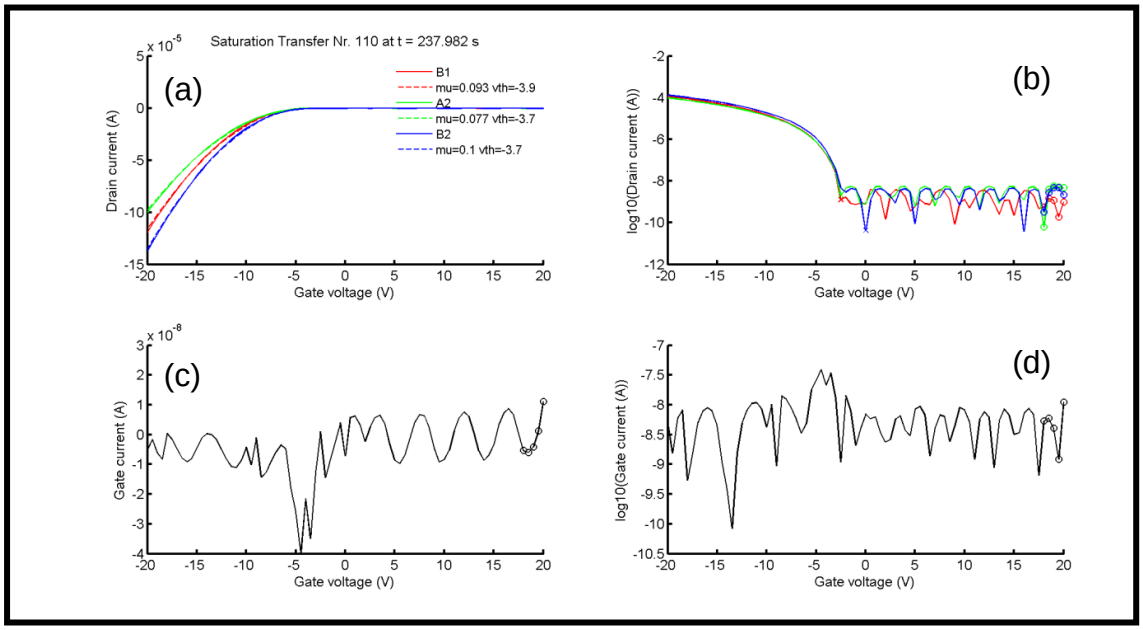


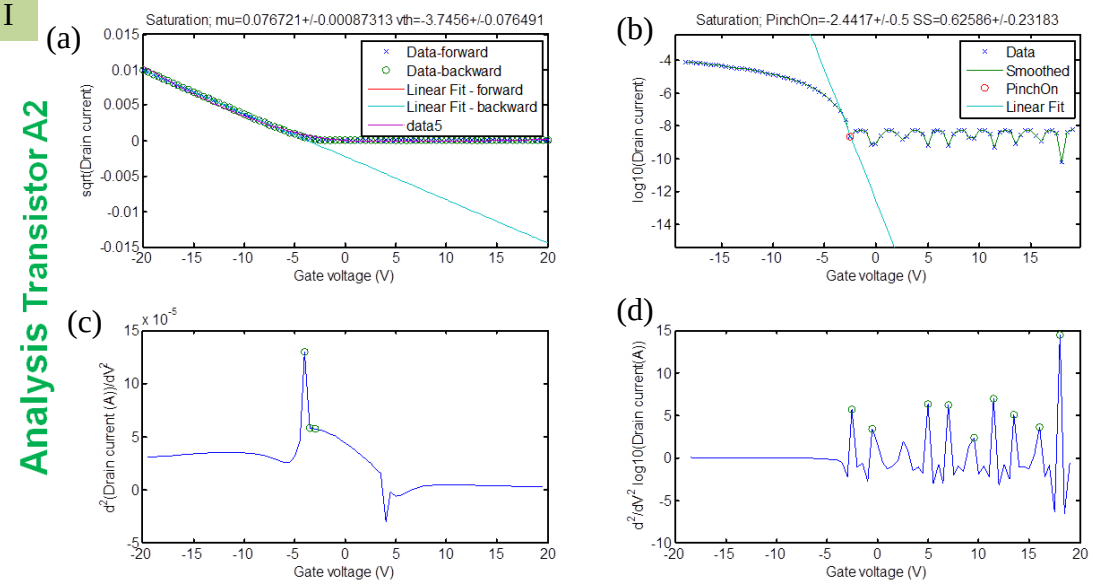
Fig. 2.16 *An example of an transfer characteristic curves recorded in real-time. (a) shows the transfer curves of the three transistorsB1, A2 and B2 and their respective mobility and threshold values depicted in the legend. (b) The transfer curve shown in (a) plotted in the semi-log scale (c) The gate/leakage current (d) the leakage current plotted in the semi-log scale.*

In Fig. 2.16, we can see the plot of the transfer characteristics of the three measured transistors (B1, A2, B2) plotted at t=237 seconds. The analysis of the transfer curves of each transistor is shown in the figure below. The most relevant transport parameters extracted is mobility μ, Threshold voltage V_{th}, Pinch ON voltage and subthreshold slope.

Mobility of the charge carriers is obtained from the linear fit of the smoothed transfer as depicted in Fig. 2.17a . Threshold voltage is obtained by taking the maxima of the second derivative of the transfer curve (Fig. 2.17 c). The Subthreshold slope is taken from the linear fit of the semi-logarithmic plot of the transfer (Fig.2.17b) and the pinch on is taken from the maxima of the second derivative of the semi-logarithmic curve (fig. 2.17d). This analysis is carried out for each transfer recorded during the whole experiment.

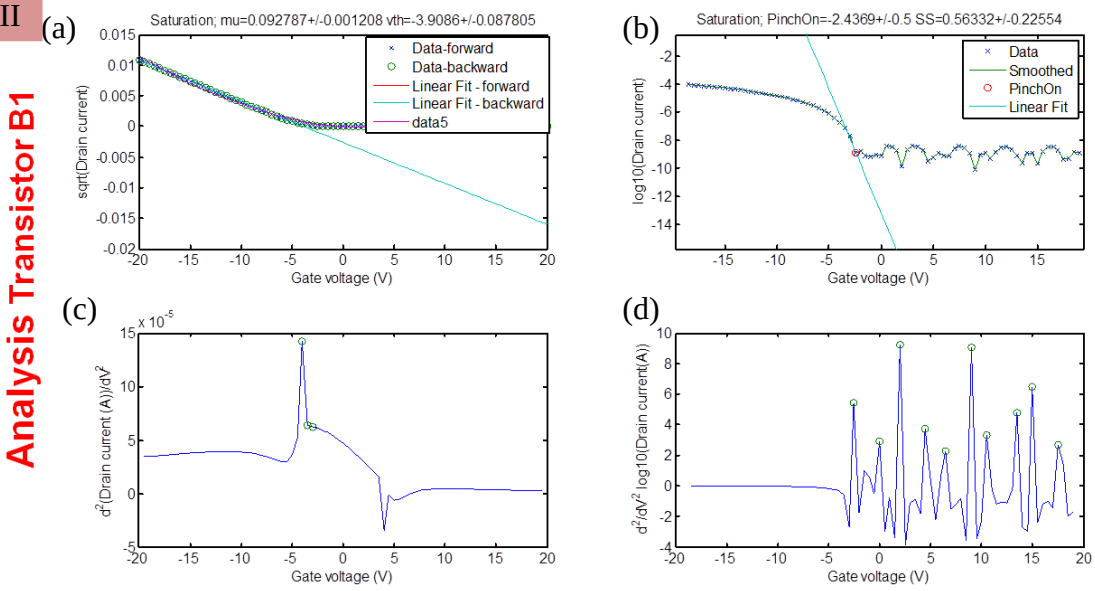
I

Analysis Transistor A2



II

Analysis Transistor B1



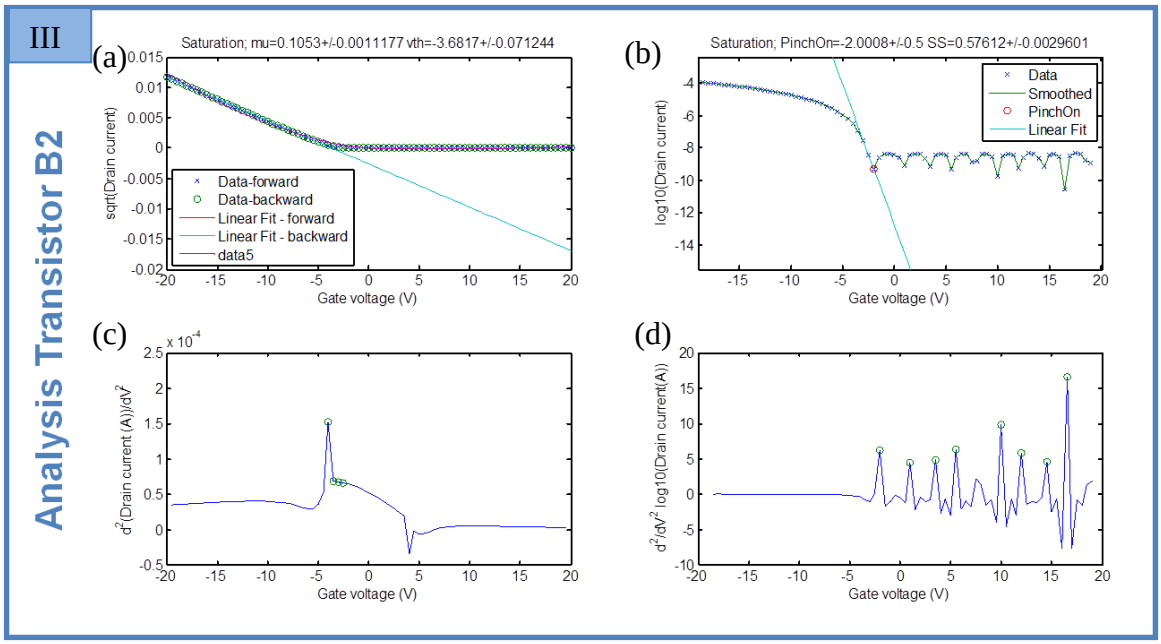


Fig. 2.17 *(I)-(III) : Example of analysis of the transfer curves (as shown in fig. 2.16) recorded in real time for three different transistors.*

Having obtained the values of the extracted parameters as a function of time, we can plot the mobility of the charge carriers from the very beginning of the growth of the semiconductor until the final thickness. Here I show the evolution of the main parameters i.e μ and V_{th} as a function of time. Since we know the deposition rate of the semiconductor or in other words the thickness of the semiconductor expressed in molecular layers versus time (fig. 2.18) we can obtained transport parameters versus film thickness.

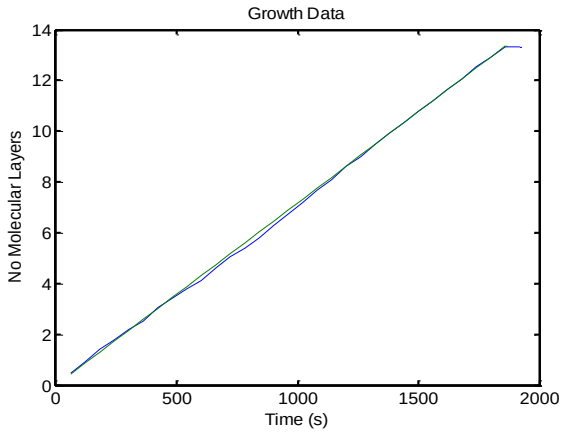


Fig. 2.18 *Thickness of the semiconducting material versus time*

Figure 2.19 shows an example a plot of mobility and threshold voltage versus thickness obtained after the analysis of the real time curves from beginning of the growth until the final thickness of the semiconductor.

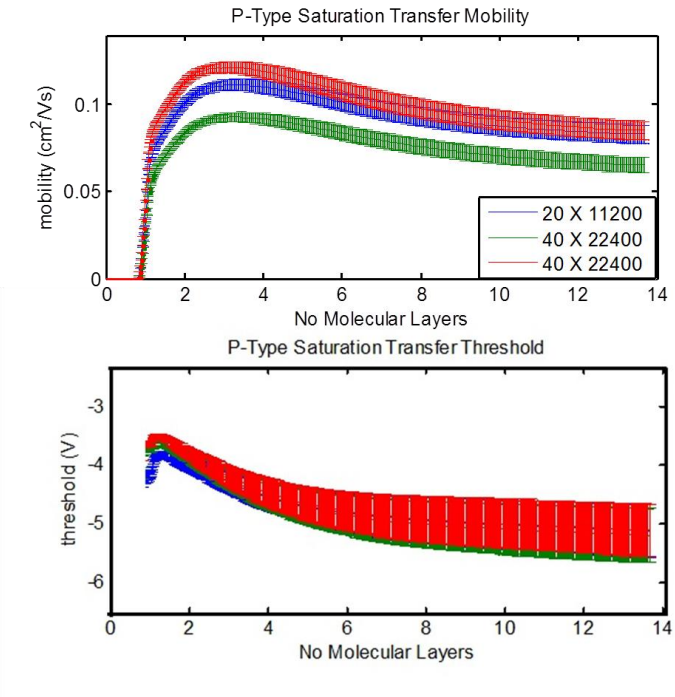


Fig. 2.19 *(top) mobility versus thickness expressed in number of molecular layers. (Bottom) Threshold voltage versus thickness. The three curves in each graph corresponds to the three different transistors with different geometries. Legend gives the information of the length and width of the channel of the transistor (L*x*W). The error bars is obtained from the standard deviation of linear fit for the case of mobility and from the standard deviation of the different values of the maxima of the curve for the case of threshold voltage.*

2.6 Atomic Force Microscopy

Atomic Force Microscopy (AFM) is a microscopy technique invented in 1986 that allows to see and measure surface structures with high resolution and accuracy. An AFM is quite different from other microscopes, because it does not create an image by focusing light or electrons onto a surface, like an optical or electron microscope. An AFM "feels" the surface atoms with a sharp probe, building up a map of the height of the sample's surface. A general picture of an AFM is shown in Fig. 2.20.

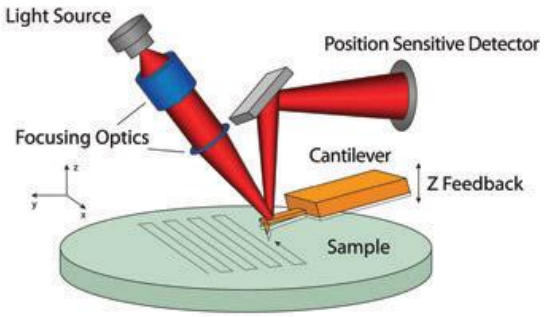


Fig. 2.20 *General schematics of an AFM*

2.6.1 AFM instrumentation

The main components of an AFM microscope are shown in Fig. 2.21: they can be gathered into the AFM stage, the control electronics and a computer to visualize the final surface image.

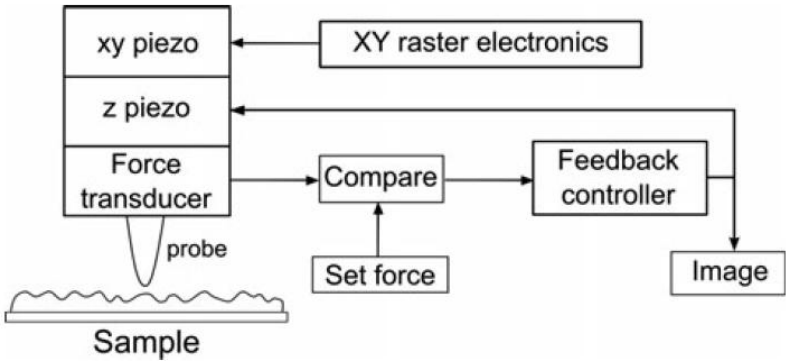


Fig. 2.21 *AFM block diagram*[3]

2.6.2 AFM stage

The microscope stage mainly contains the coarse approach mechanism, the x-y-z scanners (or piezos) and the force transducer.

An important challenge in AFM design is making a motion control system that allows the probe to approach the surface before scanning. This should happen without crashing the probe on the sample.

Coarse approach mechanism: In the AFM stage there are two separate motion generation mechanism in the z axis: the first is a stepper-motor-drive mechanism with a dynamic range of a centimeter and a resolution of a few microns. The second is the z scanner, which, together with the x and y scanner allows all the three motion of the tip with respect to the surface.

x-y-z scanners: these scanners are piezoelectric materials which convert electrical potentials in mechanical motion. Typically, the expansion coefficient is of the order of 0.1 nm/V. One possible configuration is a disk which gets longer and narrower when a voltage is applied. Another one is a tube, with electrodes inside and outside. Currently, the tube scanner is the most widely used as it is very compact and allows very precise movements.

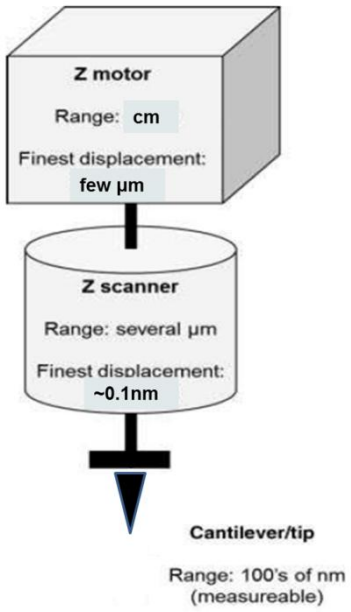


Fig. 2.22 *Series configuration of the z motor, the z piezo and the probe*[3]

Force sensor: the force between the AFM tip and the sample is measured by a force sensor. This tool is typically able to detect forces in the range of pN. The optical lever is the most widely used force sensor in AFMs. The principle of it is shown in Fig. 2.23.

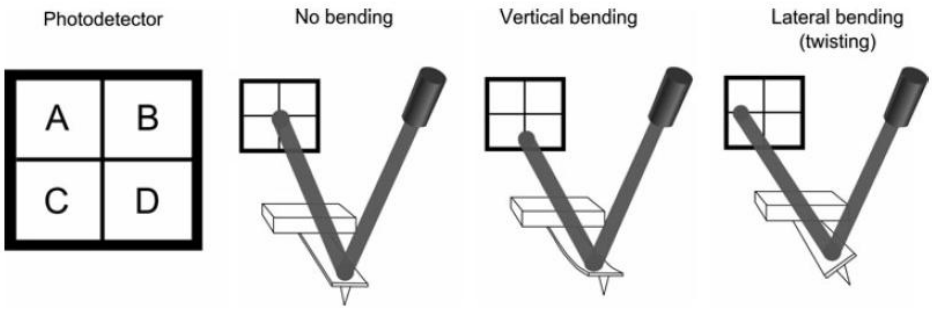


Fig. 2.23 *The optical lever sensor and an illustration of how the photodetector detects vertical and horizontal bending of the cantilever*[3]

This system consists of a laser focused to a spot on the back of a reflective cantilever, the beam is then reflected onto a split photodetector which measures the position of the laser spot. The optical lever magnifies a tiny movement of the cantilever to create a large movement at the photodiode.

If a probe, mounted on the front side of the cantilever interacts with the surface, the reflected light path will change. The force is then measured by monitoring the change in light detected by the four quadrants of the photodetector. Specifically, the difference in signal (A+B)-(C+D) gives the vertical deflection of the cantilever, while, (B+D)-(A+C) gives the lateral deflection.

2.6.3 AFM electronics

x-y raster pattern: the AFM electronics drive the x-y scanners in a type of raster pattern, as shown in Fig. 2.24. The x scanner moves across the first line of the scan and back. It then steps in the y direction to the second scan line, moves across it and back, then the third line, and so forth. AFM data are typically collected in only one direction, called the fast scan direction: the x axis in our case. The y direction is called, on the other hand, the slow scan direction.

While the x scanner is moving across a scan line, the image data are sampled digitally at equally spaced intervals. The spacing between the data points is called the step size which results in the full scan size divided by the number of pixels. The number of lines in a data set usually equals the number of points per line, thus, the typical data set is made up of a square grid.

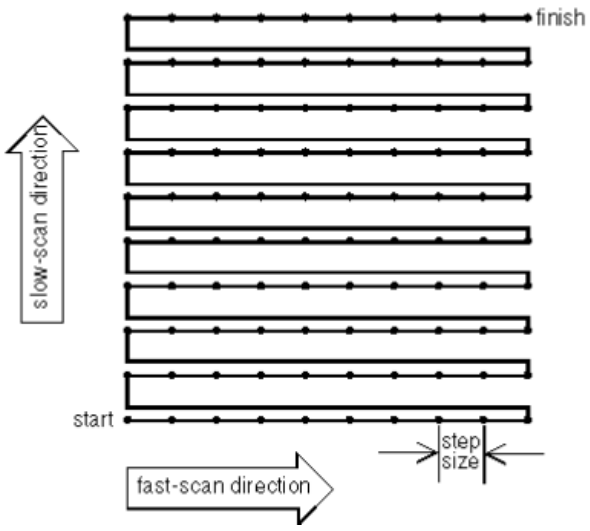


Fig. 2.24 *x-y scanner motion during data acquisition*

Feedback control: the feedback control is used to maintain a set force between the probe and the sample. The control electronics takes the signal from the force sensor and uses it to drive the z piezo so as to maintain the probe-sample distance, and thus the interaction force at a set level.

2.6.4 Interactions in AFM

The most common potential used to describe the interaction between the tip and the substrate is the Lennard-Jones potential, or "6-12" potential:

$$V_{LJ}(r) = \varepsilon[(\frac{\sigma}{r})^6 + (\frac{\sigma}{r})^{12}]$$

where ε is basically the depth of the potential well and σ is the finite distance at which the potential is zero.

This potential is the sum of two physical interactions between the tip and the substrate's atoms. One is an attractive contribution, commonly called van der Waals potential; this contribution is mainly relevant at big distances. The second part, instead, is a repulsive potential directly connected with the Pauli exclusion principle: this contribution has main effects at short distances.

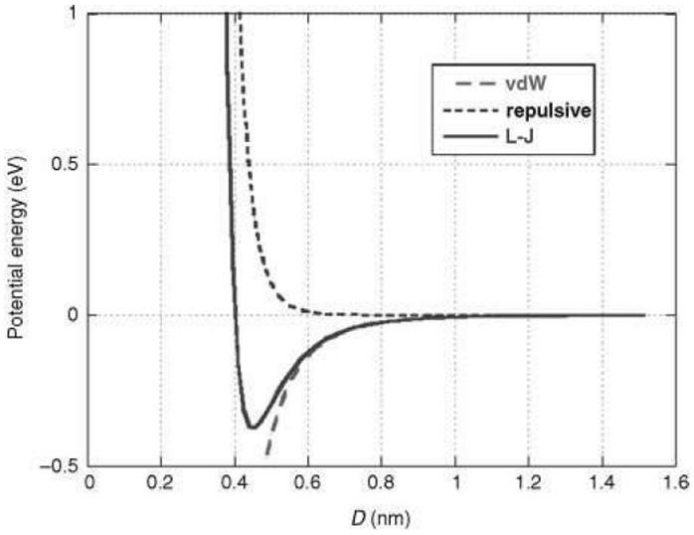


Fig. 2.25 *Distance dependence of the Lennard-Jones potential*

2.6.5 AFM modes

A very large number of possible modes of operation are nowadays used in AFM. Among them, contact mode and tapping mode are one of the most relevant.

1. Contact mode

Contact mode was the first mode developed for AFM. It is the simplest mode and the basis for the development of the later modes.

To understand this AFM mode, it is necessary to use the so called force-distance curve, like the one in Fig. 2.26.

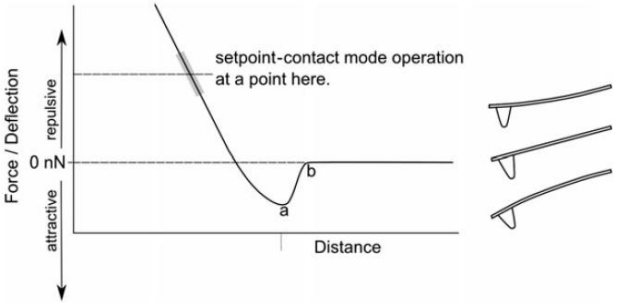


Fig. 2.26 *Simplified force-distance curve showing contact scanning regime (repulsive region). Right: illustration of probe bending in each regime: repulsive force regime, zero deflection regime and attractive force regime* [3]

Considering the approach curve in Fig. 2.26, when the tip is far from the sample, the cantilever is considered to have zero deflection. As the tip approaches the sample, it normally feels first an attractive force; as the instrument continues to push the cantilever towards the surface, the interaction moves into the repulsive regime. It is within the repulsive regime that contact mode imaging usually occurs. The basis of contact mode AFM is that the microscope feedback acts to keep the cantilever deflection at a certain value determined by the instrument operator. This point is known as set point and the correspondent imaging mode is called constant force contact mode AFM.

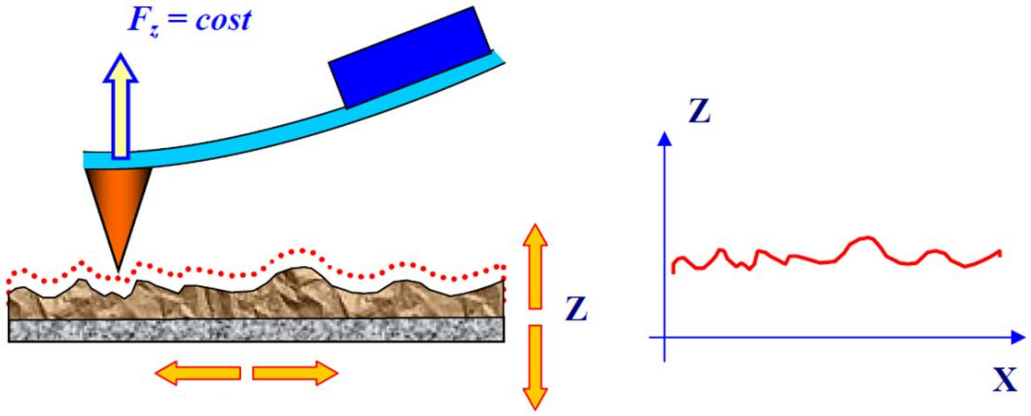


Fig. 2.27 *AFM image acquisition in constant force mode*

Probably the best reason to use this mode of operation is its high resolution and fast speed.

2. Tapping mode

If in contact mode the tip sample interaction is measured following the cantilever's deflection, in tapping mode, one of the possible dynamic mode of operation, the oscillation amplitude of the cantilever, the frequency and the phase shift may be recorded. This opens several channels for simultaneous data acquisition, each of them describing a different property of the sample. Moreover, since in tapping mode the cantilever is oscillating, the sample damage is substantially reduced.

Basically, in this AFM mode, the cantilever is oscillated, usually with an additional piezoelectric element, and typically at its resonance frequency. When the oscillating

probe approaches the sample surface, the oscillation changes due to the interaction between the tip and the surface itself. The effect is a damping of the cantilever oscillation, which leads to a reduction in the frequency and amplitude of oscillation. The oscillation is monitored by the force sensor and the z scanner adjusts the z height via the feedback loop to maintain the probe at a fixed distance from the sample.

The only real difference between the various oscillating modes are in the amplitude of oscillation applied to the probe. Using a small oscillation amplitude it is possible to maintain the cantilever only in the attractive regime, dominated by the van der Waals potential. This technique is known as non contact mode. On the other hand, it can be seen that if a large oscillation amplitude is applied, then the probe will move, during an oscillation, both in the attractive and repulsive regime. This technique is known as tapping mode AFM.

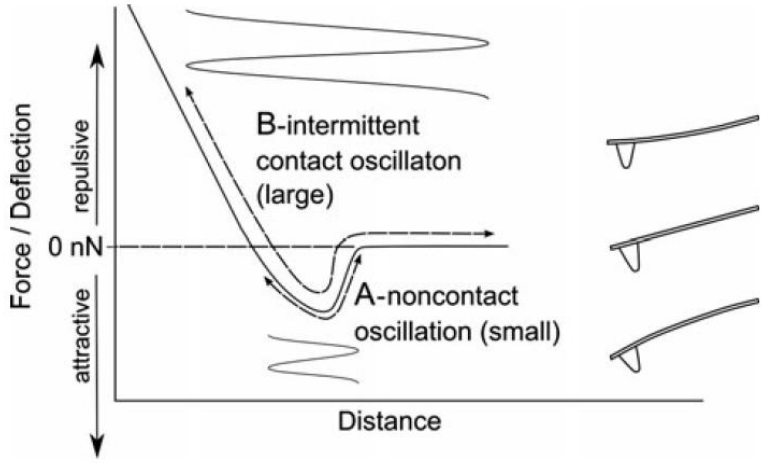


Fig. 2.28*: Different operating regimes for oscillating AFM modes. A: with a small amplitude of oscillation the probe can be kept in the attractive regime. B: with a larger oscillation the probe moves both in attractive and repulsive regime*

2.6.6 AFM Experimental setup

Throughout this thesis, the morphological investigations are based on AFM operating in semi-contact mode. We used a Smena (NT-MDT, Zelenograd, Russia) AFM consisting of standalone head with the piezo scanner positioned inside the head (Fig. 2.29).

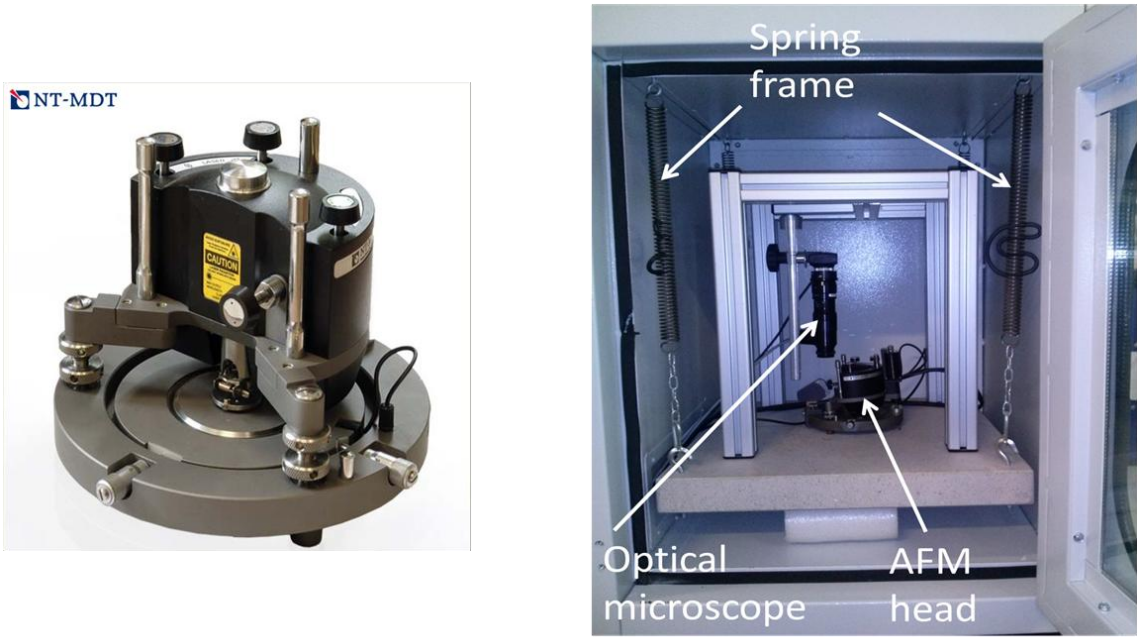


Fig. 2.29 *(Left) NT-MDT Standalone SMENA (Right) AFM set up used at the ISMN-CNR Bologna*

The sample is fixed on a special sample holder, and the head is the only moving part. The microscope is equipped with a camera and placed on an antivibration stage (Fig. 2.9). The tips are distributed by Molecular Devices and Tools for Nanotechnology (NTMDT) and their specifications are: chip size 3.6x1.6x0.4 mm; tip height: 10-15 μm; tip angle: ≤ 22°; tip curvature radius: 10 nm; and resonant frequency: 190-325 kHz and 115-190 kHz.

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Chapter 3 Band Broadening in Organic Thin Film Transistors: From the Sub-monolayer to the Multilayer Regime

3.1 Introduction

Charge transport (CT) in OFETs is governed by the field induced charge accumulation in an almost 2D confined layer adjacent to the interface with the gate dielectric. Optimizing the CT along this channel is relevant in order to realize applications in flexible organic electronic devices and information technology. Major challenges in this quest are the improvement of the electronic coupling along the pi-orbital transport path and the reduction of energetic disorder. While the former is intrinsically related to the molecular structure of the organic semiconductor, the latter is largely influenced by extrinsic factors related to processing conditions or device architecture. In order to arrive at the ultimate limits of molecularly controlled transport, energetic disorder and the consequential broadening of the transport band have to be minimized. Energetic disorders may arise due to various factors such as the defects or impurities of the dielectric, morphology of the semiconductor film or the nature of the molecular packing of the semiconductor. Experimentally, defects caused by the dipolar groups residing in the dielectric surface such as the silicon oxide can be reduced by modifying the surface of the dielectric surface such as silicon oxide with self assembled monolayer like Octadecyltrichlorosilane (OTS) or Hexamethyldisilazane **(**HMDS). These transistors have shown to have a better performance in terms of charge mobility in particular when they are compared to the ones fabricated on an untreated silicon oxide.[1] Another factor that contributes to the broadening of the transport band is the morphology of the semiconducting material. Mobility of the charges is strictly correlated to film thickness. Dinelli *et. al* has demonstrated that charge transport in the channel of the semiconductor takes place only in the first few layers[2]. However, depending on the growth conditions the thickness of the accumulation layer in the channel can be modulated by the film morphology and thickness.[3] Tello *et.al* have demonstrated how the inter grain regions between the pentacene island causes charge trapping in particular in particular in ultra thin film transistors.[4]Moreover Fiebig and co workers carried out an in situ study quantifying the number of traps as a function of film thickness[5]. The next question that arise is if we

can characterize the energetic disorders caused by defects as a function of film thickness and morphology. To study this we performed an in situ real time electrical characterization of an ultra thin film pentacene transistor fabricated on an untreated SiO_2 or HMDS modified SiO_2. Temperature dependent measurements were then performed in situ just after the real-time experiment.

A comparative study on the evolution of the electrical characteristics of the OFETs fabricated in the two different surfaces allows us to have a better insight on the interactions taking place at the dielectric-semiconductor interface. Fast electrical characterization allows us to study the field dependent transport during the growth of the active layer covering various thicknesses starting from percolation in the sub-monolayer regime .The measured transfer curves are analyzed in terms of a modified Vissenberg-Matters model which takes the 2D confined transport channel into account and reproduces temperature dependent measurements.[6] Fitting of the experimental data gives us a relation between band broadening and film thickness and morphology.

3.2 *In situ* real time experiment

In situ real time experiment was carried out in home built vacuum chamber[7] described earlier (section 2.5). Electrical characterization was carried out in real time during the growth of pentacene on the channel of the OFET. As substrates for the *in situ* experiments, we have used the standard TP consisting of a common gate made of highly doped n-type Si wafer with 200 nm thick layer of thermally grown silicon oxide (C_{ox} = 17.3 nF/cm^2) as gate dielectric. It consisted of interdigitated gold electrodes acting as source and drain contacts had channel length L = 20, 40 μm and width W = 11200, 22400 μm. The test patterns were cleaned by following a standardized protocol as discussed in Section 2.1.

For the experiment on bare SiO_2 , no chemical treatment was carried out after the cleaning procedure which for the HMDS-treated substrate, just after cleaning the TP, the oxide surface was functionalized with hexamethyldisilazane (HMDS) by thermal evaporation of HMDS over the cleaned substrate. (Sec. 2.1.1).

Pentacene was deposited by high vacuum sublimation at a rate of 7Å/min on the test pattern with transistor structures. Source-Drain current I_{SD} was measured in real time every 3 seconds upon sweeping the gate potential V_G from +20V to -20V while keeping the potential at the drain V_{SD} at -20V during the growth of the semiconductor. Three transistors were measured simultaneously.

At the end of the real time experiment, temperature dependent measurements were carried out *in situ*. The temperature of the substrate was cooled down up to about 100K. I-V characteristics were acquired as temperature rises up from 100K to 300K (ambient temperature).

Morphological characterization on the pentacene film grown on the two surfaces was carried out ex situ after the *in situ* real time experiment.

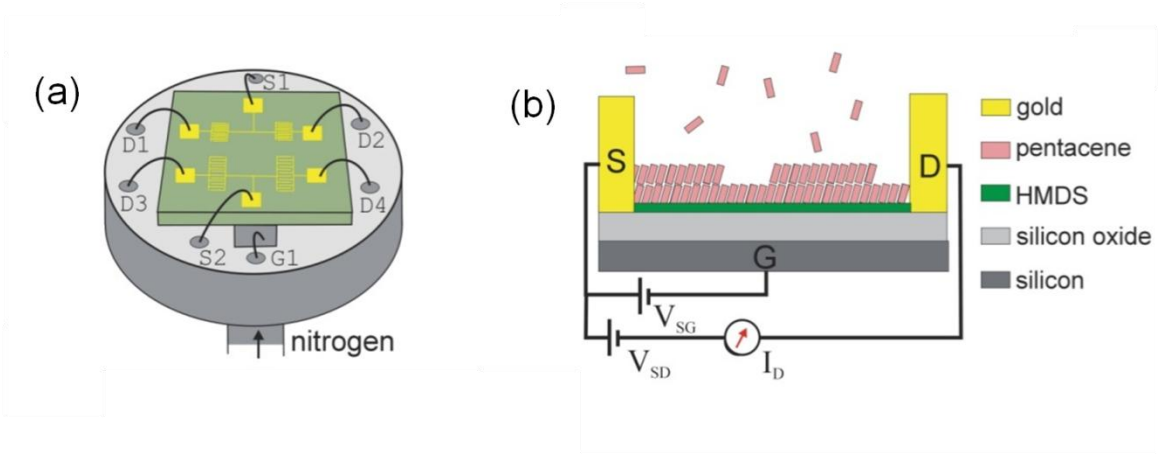

Fig. 3.1 *In-situ electrical characterization during the growth of an organic field effect transistor. (a) Scheme of the sample holder positioned the vacuum chamber showing the connections of a device with four inter-digitated transistors and one common gate. (b) Scheme showing the cross-section of a forming ultra-thin film transistor.*

3.3 Results

The electrical characteristics of the pentacene transistor fabricated on an untreated-Silicon oxide and on HMDS-treated silicon oxide is shown in Fig. 3.2. The current values plotted as a function of nominal film coverage corresponds to the on-current obtained from the transfer curves (at V_G=-20V, V_D=-20V). In both the transistors, percolation occurs at $\Theta_c \approx$ 0.7ML . Transistors fabricated on HMDS modified SiO_2 (Fig. 3.2 red curve) show a rapid increase in the transistor current I_D from percolation up to the completion of 1ML. Upon completion of the first monolayer, a kink is observed where we observe a slower increase in the current from the first to the second monolayer . The current reaches its maximum value after the completion of the third monolayer. In contrast, pentacene transistors fabricated on an un-treated SiO_2 show a relatively slower increase in I_D versus film thickness. The current saturates up to a final thickness of about 6MLs.

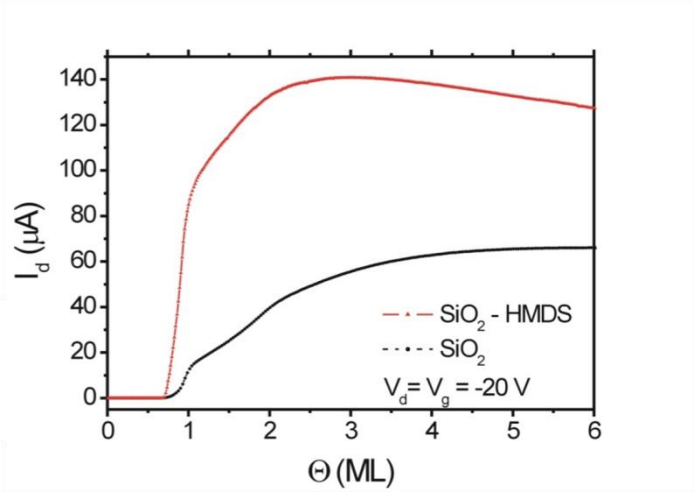

Fig. 3.2 *Plot of the drain current I_D as a function of the nominal thickness of pentacene expressed in number of molecular layers Θ for un-treated SiO2 surface and HMDS modified surface.*

In order to figure out the effect of HMDS on the known morphology of pentacene film on SiO_2, a comparative study was carried out on pentacene film grown on untreated SiO_2 versus HMDS SiO_2. The film morphology obtained by AFM imaging reveals that the morphology in both the cases is the same (Fig. 3.3). The pentacene film shows terraced islands stacked up together depicting the roughening transition of the film morphology from layer by layer 2D growth to 3D growth at higher thicknesses.

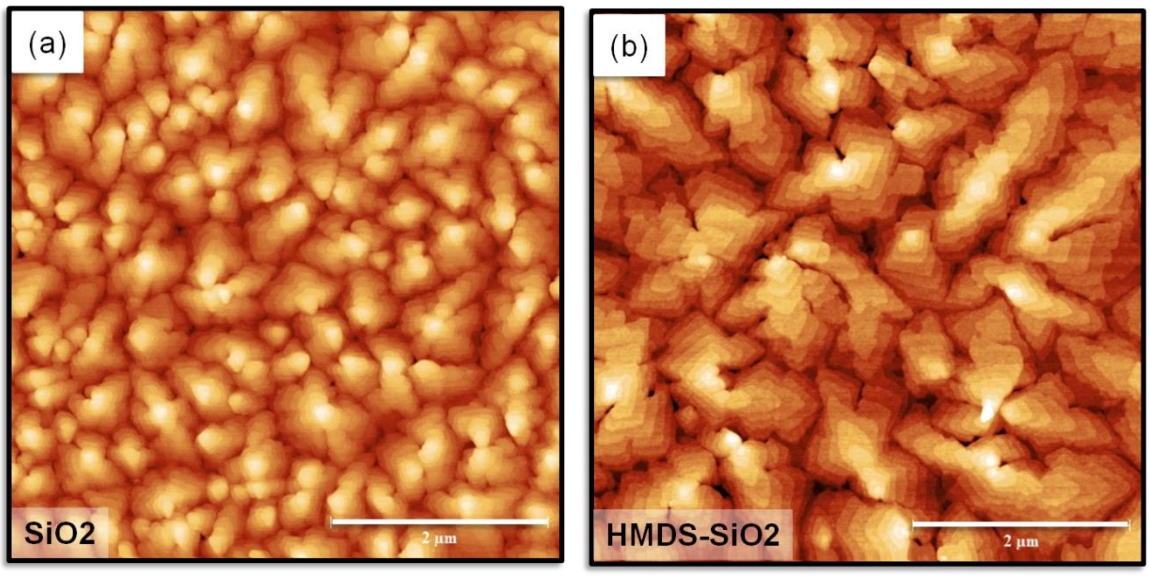

Fig. 3.3 *AFM image of 6ML thick pentacene film deposited on (a) Untreated silicon oxide and (b) HMDS treated silicon oxide.*

Moreover , output curves recorded *in situ* at the end of each experiment for both types of transistors (Fig. 3.4) evidence the absence of contact resistance in both the transistors irrespective of channel geometry.

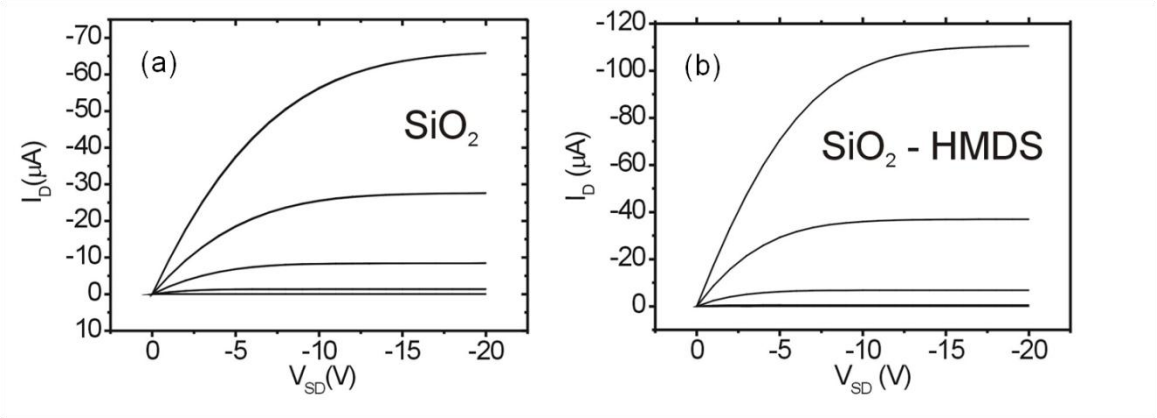

Fig. 3.4 *Transistor output characteristics*

To further investigate the charge transport phenomena, temperature dependent measurements were carried out. As temperature varies from 100K to 300K, I-V transfer curves were recorded. Each transfer curves were then fitted with a power law . Following the modified Vissenberg and Matter's model[8], we can write an expression for the drain current depending on the dimensionality of the charge transport as

$$I_D^{3D} \propto (V_{SG} - V_{th})^{\frac{2E_0}{kT}} - (V_{SG} - V_{th} - V_{SD})^{\frac{2E_0}{kT}} \tag{3.1}$$

and

$$I_D^{2D} \propto (V_{SG} - V_{th})^{\frac{E_0}{kT}+1} - (V_{SG} - V_{th} - V_{SD})^{\frac{E_0}{kT}+1} \tag{3.2}$$

where V_{SG}, V_{th} and V_{SD} are the source-gate voltage, threshold voltage and source-drain voltage respectively. E_o is the characteristic width of the exponential bandtail .

In the case of saturation regime where $V_{SD} \geq V_G - V_T$, equation 3.1 and 3.2 can be approximated as

$$I_D \propto (V_{SG} - V_{th})^{\gamma} \begin{Bmatrix} 3D: \gamma = 2E_0 / kT \\ 2D: \gamma = E_0 / kT + 1 \end{Bmatrix} \tag{3.3}$$

The transfer curves obtained as a function of temperature was fitted with equation 3.3. To obtain the gamma exponent, we take the derivative of $\frac{dI_d}{dV_g}$ and plot $\frac{I_d}{\left(dI_d / dV_g\right)}$ as a function of V_g. The linear fit of this plot (fig.3.5a) gives us γ *and* V_{th}.

Having obtained γ for each temperature, we plot γ as a function of 1/T as shown in Fig. 3.5b for both type of transistor. The extrapolated line crosses the exponent axis at 1, as predicted in equation 3.3 for 2D transport as $T \to \infty$. This confirms that transport of charges occurs in a spatially confined channel and obeys the 2D temperature dependence .

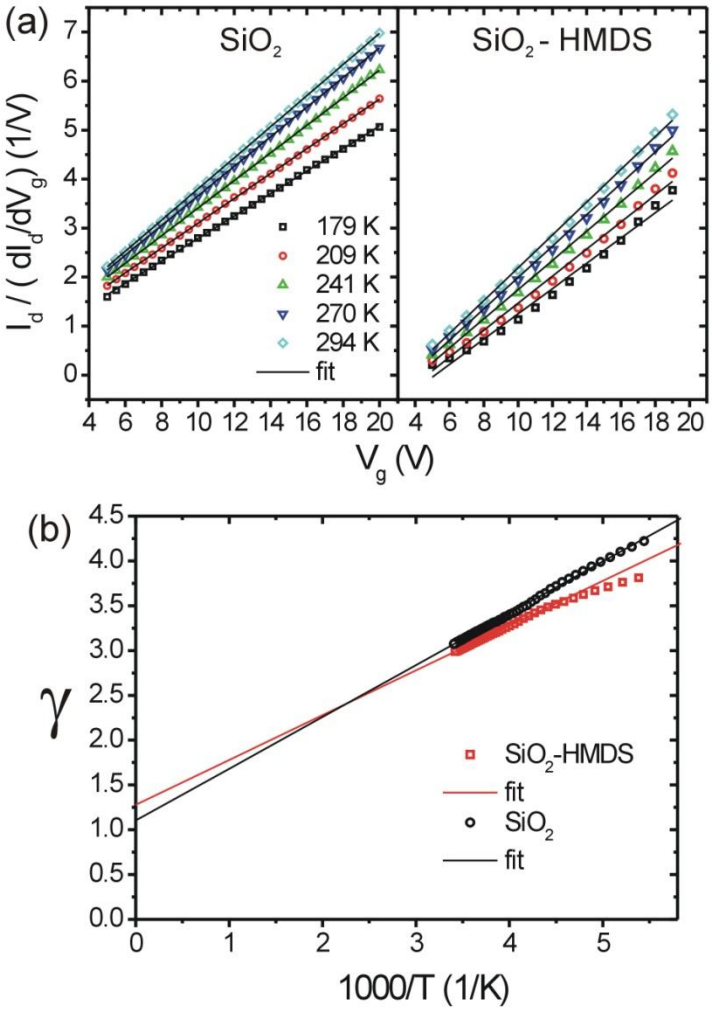

Fig. 3.5 *Experimental data from temperature dependent transfer measurements and fit to a powerlaw* $I_d \sim (V_g - V_{th})^{\gamma}$ *according to the Vissenberg Matters Model. In order to obtain the critical exponent* γ *and the threshold voltage* V_{th} *by a single linear fit, we plot* $\boldsymbol{I_d / \left(\frac{\partial I_d}{\partial V_g}\right)}$ *as a function of* V_g. *Power law exponent* γ *as obtained from transfer*

characteristics as a function of inverse temperature. The linear fit confirms hopping mediated transport in a confined, quasi two-dimensional charge carrier distribution.

Having know the charge transport model for our system, we used the 2D Vissenberg and Matters model to fit the transfer curves recorded in real time during the growth of the semiconductor. An example of the fit for the curves acquired at a certain thickness for both the transistors is depicted in Fig. 3.6. The power law fit yields an exponent gamma as a function of film thickness . As temperature of the substrate is kept constant during growth, by obtaining gamma, one can extract the value of the width of the band tail E_0 as a function of nominal film thickness.

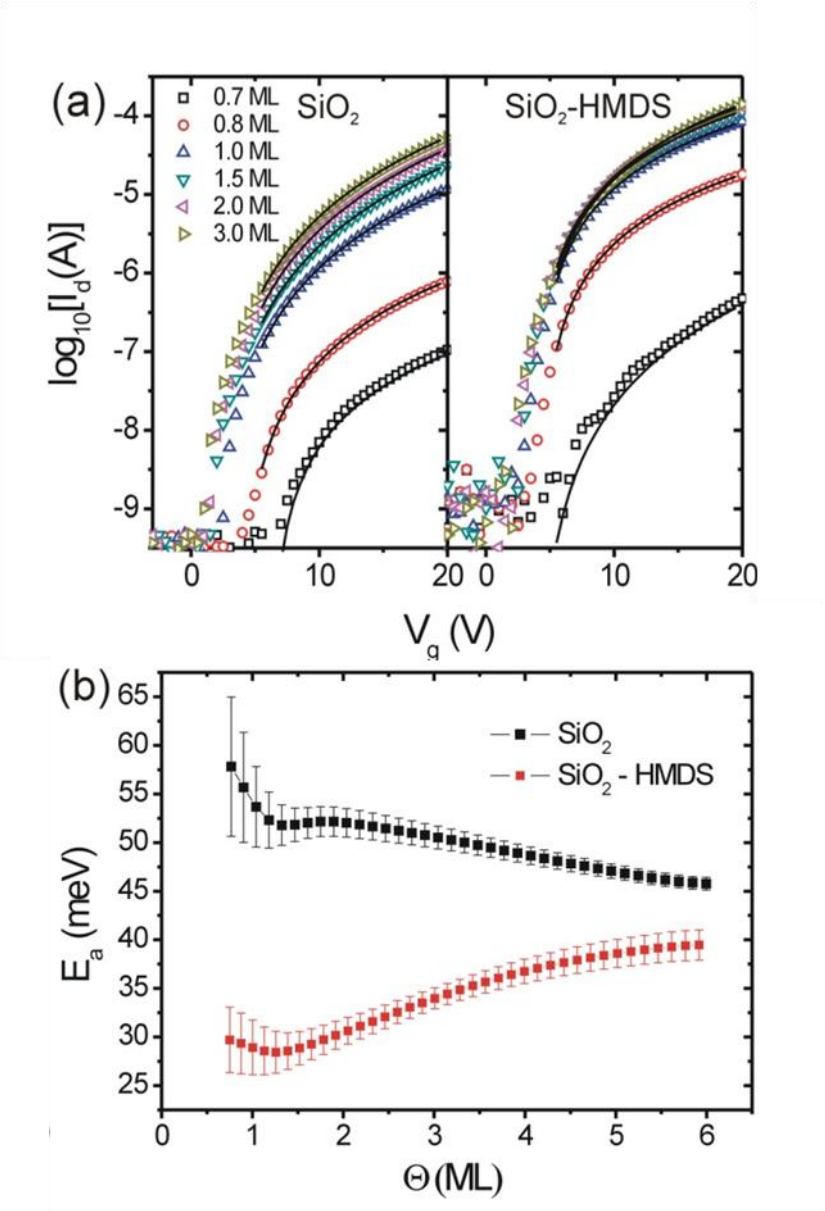

Fig. 3.6 *(a) Characteristic transfer curves obtained during the growth of a semiconducting pentacene film on bare or HMDS treated silicon oxide dielectric. The fit to the 2D confined hopping model is indicated by lines. (b) Characteristic width of the bandtail E_0 as a function of nominal layer thickness Θ for two types of dielectric surfaces.*

Fig. 3.6b shows the variation of E_0 as a function of nominal thickness Θ expressed in number of molecular layers (ML. For the unmodified dielectric surface, the disorder is highest at low layer thicknesses, when transport is confined close to the dielectric surface. Increasing the amount of semiconducting material reduces the width of the band tail. In contrast, on a modified silicon oxide surface, the disorder at the interface between the dielectric and the first layer of semiconductor is low as HMDS capping to the hydroxyl groups present in the surface reduces the defects at the SiO_2/pentacene interface.

However, at nominal thickness greater than 2 ML, the morphology of the film undergoes a roughening transition[9] leading to the introduction of defects and hence the band tail starts to broaden as a function of thickness.

3.4 Discussion

We rationalize the findings with two types of electric interactions which influence on the energetic disorder experienced by the charge carriers in the channel. First, dipolar disorder at the silicon oxide surface arises due to the presence of OH groups. This type of interaction is strongly distance dependent. With increasing film thickness the transfer path becomes optimized and the disorder reduces. For the case of the HMDS modified dielectric dipolar disorder is minimized due to the capping of OH groups. Second, polarization of the medium surrounding the charge carriers leads to a repulsion from the dielectric interface with the vacuum due to the difference in permittivity. The effect corresponds to an image charge effect. Here the interaction is repulsive as the charge resides in the medium with the higher permittivity. Quantitatively, the repulsion depends on the thickness of the pentacene layer And charges are more stabilized in thicker pentacene films. As a consequence, the increase of surface roughness after 2ML leads to an increase in energetic disorder, as observed for the case of the HMDS modified dielectric.

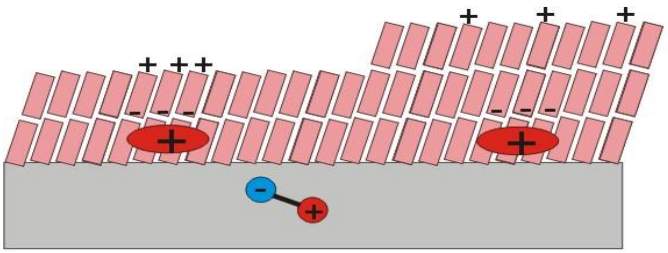

Fig. 3.7 *Scheme showing electrostatic interactions (image charge repulsion and dipolar disorder) relevant for energetic disorder experienced by hole charges at the pentacene dielectric interface.*

3.5 Conclusion

With the *in situ* real time experiment I was able to characterize the broadening of the transport band-tail as a function of layer thickness in pentacene transistors. The *in situ* real-time characterization permits to acquire data already at the very onset of percolation. On a dielectric with reduced dipolar disorder due to HMDS functionalization , I observe very low energetic disorder from the sub-monolayer to 2 ML regime. In particular from the transfer curves obtained during real time experiment, I observe that at pentacene thickness <2MLs, the mobility of the charges is independent of the charge carrier density. At larger thicknesses band broadening sets in due to surface roughening caused by the film morphology. In contrast on thermal SiO_2 dielectric disorder is present also in ultra thin films and is ascribed to the dipolar disorder.

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Chapter 4 Charge Density Increase in Sub-Monolayer Organic Field Effect Transistors

4.1 Introduction

In OFETs, strong electrostatic interactions of the charge carriers towards the gate results in the confinement of the charge density to a few layers of the semiconducting material lying adjacent to the dielectric.[1] Confinement of charge density can also arise due to a finite thickness of the semiconductor or by the lateral size of the semiconducting film caused by lithographic patterning or domain boundaries. Nano-scale spatial confinement has been exploited in order to optimize transport properties in organic thin film transistors with applications ranging from large area electronics[2], [3] and wearable electronics[4] to chemical and biological sensing [5]. The effects of confinement have been investigated in organic thin film transistor. Firstly, confining interfaces influence on polymorph selection and guide crystallization processes. This allows the optimization of charge transfer in the channel direction.[6], [7] Secondly, confinement at length scales in the order of the carrier localization changes the density of states and transport properties.[8] In OFETs a third contribution has to be considered when transport in confined channels is studied: lateral confinement that impacts on the capacitive coupling between the semiconductor and the gate electrode as it induces band bending in the dielectric layer. An understanding of this effect is necessary to obtain the correct charge density and analyze transport properties of the confined transistor channel.

Studies on charge transport in laterally confined systems assumed a carrier density in the accumulation layer that is independent of coverage. This holds true only when the lateral spacing between features largely exceeds the thickness of the dielectric. In this case transversal electric field can be treated as homogenous. If this is not the case bending of the electric field in the dielectric has to be taken into account and corrections for the calculation of transport properties has to be taken into consideration. Sub-monolayer OFETs represent a model system to study the effect because morphology varies depending on growth condition and coverage.

This work aims to investigate charge accumulation and transport in sub-monolayer transistors grown and characterized *in situ* in high vacuum. Displacement current

measurement was carried out in order to characterize the formation of the accumulation layer and charge density. I have demonstrated the dependence of charge density as a function of coverage in the sub-monolayer regime. The charge density have a maximum when coverage exceeds percolation threshold. The experimental result was explained using an analytical electrostatic model. Having known the charge density, I was able to extract mobility in the sub-monolayer regime and study transport close to the threshold of two dimensional percolation.

4.2 *In situ* real time characterization of pentacene transistor

Experiments were performed in the homebuilt set up described earlier in Section 2.5. Standard test pattern having a common gate as described in Sec 2.1 was used. The standard cleaning protocol for the test pattern was employed. This involves rinsing with acetone, followed by hot piranha solution for 15 minutes and hydrogen flouride (2%). The oxide surface was then functionalised with Hexamethylsilazane (HMDS) by thermal evaporation onto the cleaned surface. Electrical connections were made from the sample holder to the test pattern before putting the sample holder in the vacuum system. Pentacene was evaporated at a rate of 7Å/min through a mask exposing an area A_0=0.104 cm^2 (Fig. 2.11 of chapter 2). Three transistors were measured simultaneously using two synchronized Keithley B2612 source measure units. During pentacene growth, transfer characteristics were acquired by sweeping the gate potential V_{SG} from 20V to -20V while keeping the drain potential at V_{SD} = -20V. A fast sweep rate was applied in order to achieve a transfer measurement every 3 seconds.

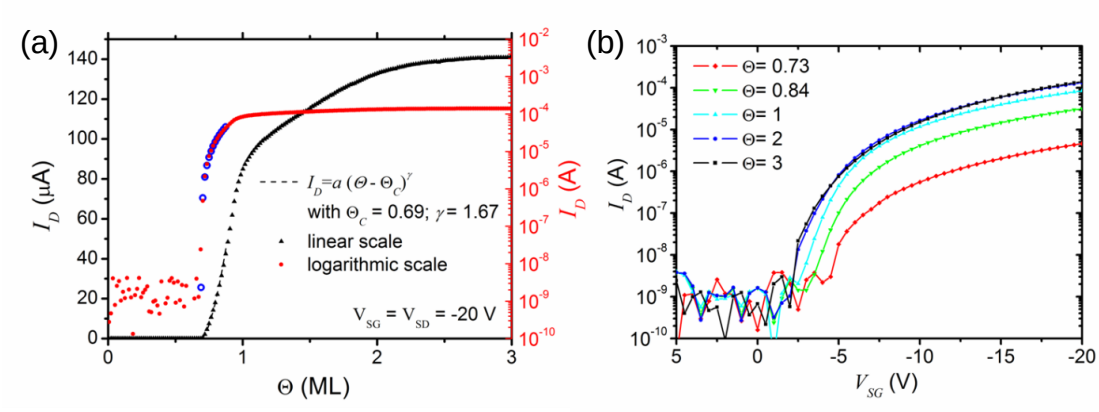

Fig. 4.1 *Evolution of current in pentacene transistor recorded in situ and in real-time during growth. (a) drain current I_D at V_{SG}=V_{SD}=-20 V as a function of nominal layer thickness Θ . The black curve corresponds to the linear scale while the red curve corresponds to the logarithmic scale of the current .The blue markers depict the power-law fit at percolation threshold; (b) Representative transfer curves at various Θ acquired at V_{SD} = -20 V. Each point in plot (a) corresponds to a full transfer characterization as shown in (b).*

Fig.4.1(a) shows the evolution of the source drain current I_D at V_{SG}= V_{SD}=-20V in the pentacene channel as function of pentacene layer thickness Θ expressed in monolayers (ML). Percolation of the semiconducting film occurs at a nominal layer thickness of Θ_C = 0.69 ML followed by orders of magnitude rise in the current. The current increases

substantially until the completion of the first monolayer. Upon completion of the first monolayer, the increase in the current (I_D vs Θ slows down) reflecting the layer-by-layer growth mode of pentacene thin films.[9] When the second layer is completed we see a further decrease of slope. At roughly three monolayers thickness, the transistor current is saturated, demonstrating the strong spatial confinement of the carrier accumulation zone to the first two to three monolayers.[10] This finding is consistent with the results reported earlier[11] and suggests that a decreased defect concentration at the silicon oxide surface is due to HMDS passivation[12], [13]. Fast sampling of I-V curves allows us to acquire transfer characteristics during film growth maintaining the same sampling frequency as for the single current measurements depicted in Fig. 4.1a. Representative I-V curves are shown in Fig. 4.1b. During the growth of the first two monolayers the shape of the transfer curves and its characteristic parameters such as pinch-off voltage, threshold voltage and mobility are in constant evolution. In order to analyze these curves quantitatively and extract the relevant transport parameters it is necessary to quantify the amount of charge that accumulates in the semiconductor due to field effect. The usual thin film approximation of assuming a planar capacitor geometry and calculating the capacitance from the dimensions of the oxide layer cannot be assumed to be valid in the sub-monolayer regime.

4.3 *In situ* real-time capacitive current measurement

In order to measure the capacitance and carrier accumulation during the growth of the pentacene layer we apply a triangular waveform to the potential V_{SG}, and sample the displacement current I_G.[14], [15] The source and drain electrodes were grounded to avoid any longitudinal electrostatic potential gradient in the charge distribution within the semiconducting film. In order to achieve fast sampling during pentacene growth, I apply a negative offset potential to ascertain operation in the accumulation regime of the p-type semiconductor, thus avoiding slow carrier injection or extraction processes from a depleted channel.[15]

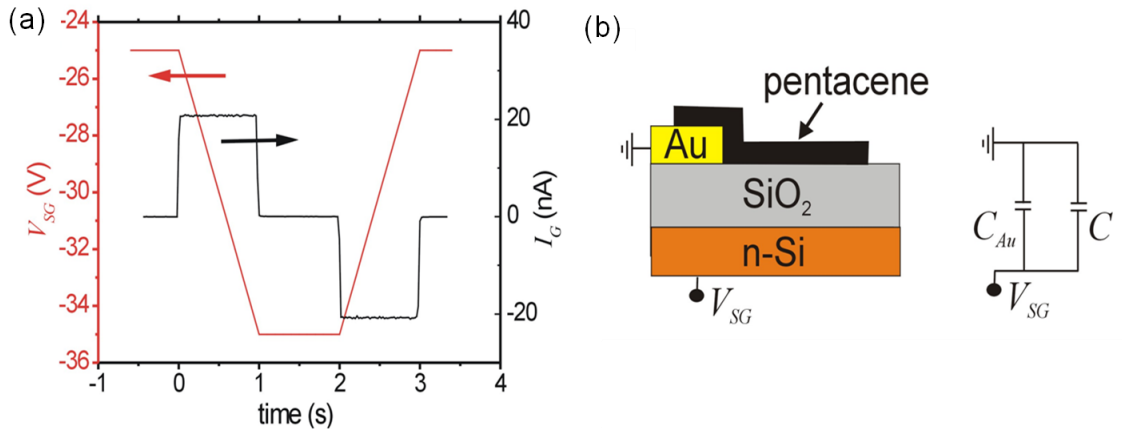

Fig. 4.2 *Experimental set up for measuring carrier accumulation in pentacene thin-film transistors: (a) potential waveform applied to V_{SG} and resulting displacement current I_G at 3 ML thickness (b) Schematic diagram depicting the two stacked capacitors connected in parallel.*

Details of the V_{SG} sweep and resulting I_G obtained in a device with 3 ML pentacene coverage are shown in Fig. 4.2a. The data allows to calculate the capacitances of the two layer stacks forming capacitors connected in parallel as depicted in Fig. 4.2b. The first stack contains the gold contacts, isolator and common gate and is denoted C_{Au}. The second stack regards the area which is not covered by gold and contains the pentacene layer, isolator and common gate and is referred by $C_{SC}(\Theta)$ which depends on coverage Θ. The following equation is used to extract the capacitances during the voltage sweep:

$$I_G = [C_{Au} + C_{SC}(\Theta)]\frac{dV_{SG}}{dt} \tag{4.1}$$

The capacitance containing the semiconducting layer can be further separated into two capacitances connected in series $C_{SC} = C_{OX}C_{Pen}/(C_{OX}+C_{Pen})$ which contain the contribution from the isolating oxide (C_{OX}) and a contribution from the pentacene layer C_{Pen} due to the spatial extension of the charge accumulation layer in the direction orthogonal to the interface. However the latter is typically neglected as $C_{OX} << C_{Pen}$.[15] Fig. 4.3 shows the measured displacement current as a function of the nominal layer thickness Θ of pentacene as measured *in situ*.

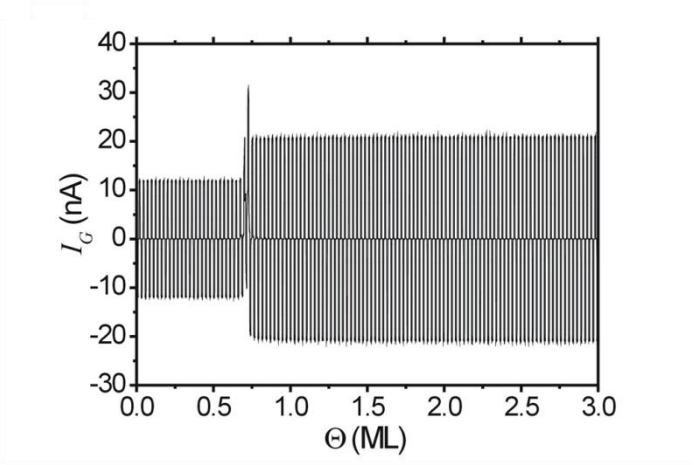

Fig. 4.3 *Displacement current measured during growth of pentacene film with a deposition rate of 0.47 ML/min applying continuously the described waveform. The displacement current before pentacene percolation (Θ=0.69 ML) results from the capacitance formed by gold source and drain electrodes*

In the initial phase the displacement current results from the capacitance that is formed between gold electrodes and the common gate. At the percolation threshold of the semiconducting film, the stable pattern of positive and negative displacement currents is perturbed. As the semiconductor percolates, the accumulation layer forms and charges enter the semiconductor resulting in a positive background peak of the displacement current. The superimposed variations of I_G are due to the continuously swept V_{SG}. After percolation the pattern of stable charging and discharging currents returns with larger amplitudes due to the increased capacitance.

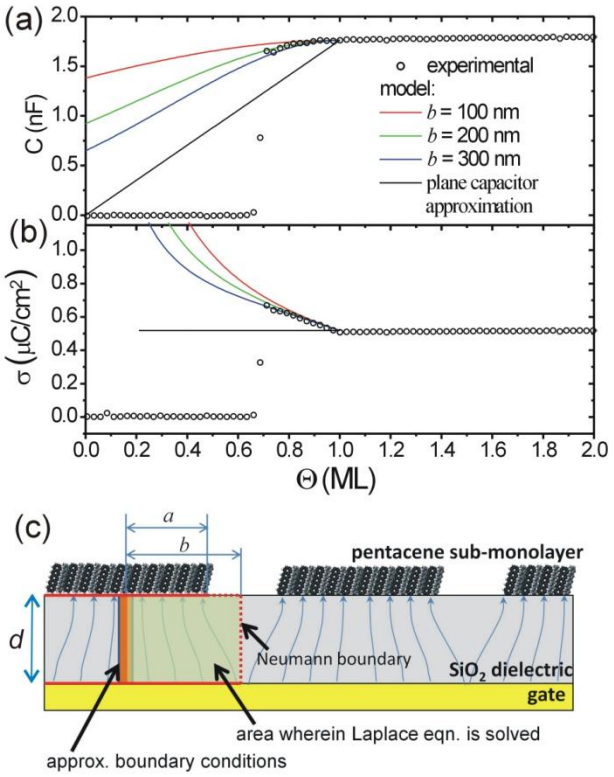

Fig. 4.4 *Capacitance C (a) and surface charge density σ (b) at V_{SG} = 30 V in the semiconducting film during growth as extracted from the displacement current measurements; (c) development of electrostatic model describing capacitance and charge density as a function of coverage in the sub-monolayer regime.*

The resulting values of C_{SC} are plotted in Fig. 4.4a. Before percolation, carriers cannot enter into the semiconducting film and C_{SC} ($\Theta < \Theta_C$)= 0. At percolation at Θ_C = 0.69 a sharp increase in C_{SC} occurs to reach almost immediately the maximum capacitance as determined by the oxide dielectric ($c_{SC} = C_{SC}/A_0$ = 17.3 nF/cm^2), which is reached upon completion of the first monolayer. Above 1 ML the capacitance remains constant, thus revealing that spatial confinement orthogonal to the interface has only minor impact on the charge density of the accumulation layer. This finding is in agreement with the small Debye length scale of 1-2 nm reported for organic semiconductors and confirms the usual approximation $C_{OX} << C_{PEN}$.[16] The initial sharp increase in C_{SC} demonstrates that already with the onset of percolation enough charges enter the semiconducting film to screen completely the gate field. This happens even if the dielectric surface is not completely covered by the semiconductor.

In order to rationalize the observed screening already at sub-monolayer coverage, a micro-electrostatic model of the capacitive coupling between interconnected semiconducting islands and gate electrode (Fig.4.4c) was derived. Sub-monolayer pentacene films were investigated by Atomic Force Microscopy to extract the geometric parameters describing the film morphology.

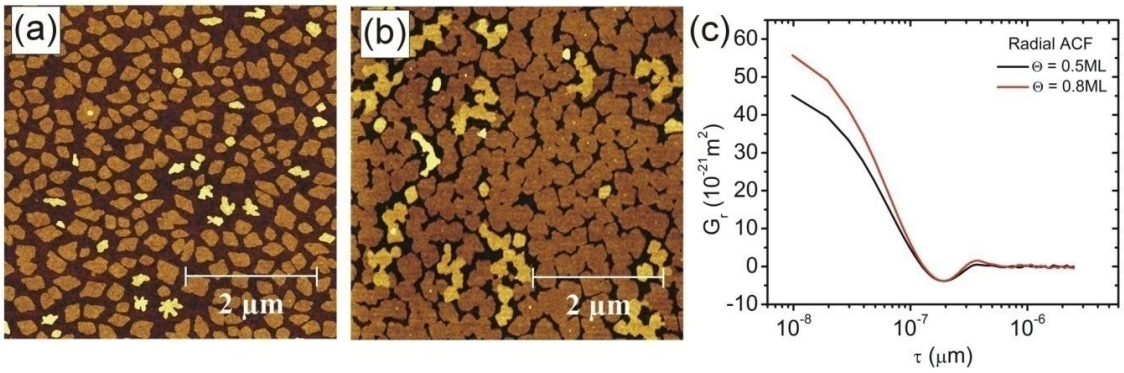

Fig. 4.5 *Morphology of sub-monolayer pentacene thin films: AFM topography at 0.5 ML (a) and 0.8 ML (b) coverage and corresponding height radial autocorrelation function in (c) showing a characteristic minima at 195 nm.*

Fig. 4.5a and 4.5b show the topography of two films obtained before and after percolation of semiconducting islands. Both images show a distribution of islands of varying lateral size and shape. The typical island height corresponds to a single pentacene monolayer. The characteristic length scale for island spacing is obtained by analyzing the radial height-autocorrelation function as plotted in Fig. 4.5c. For both coverages the minimum at b = 195 nm is equated to half the island spacing. The value is close to the thickness of the gate dielectric d = 200 nm. As a consequence the field lines exiting the dielectric bend slightly to re-enter in the pentacene-covered islands (Fig. 4.5b). A model for this behaviour was developed by means of a continuum electrostatic model that calculates the flux between the gate electrode and one half of a pentacene island by applying the conformal mapping technique to the two-dimensional Laplace equation.[17], [18] The periodic structure considered in the model is highlighted in green in Fig. 4.4c. Its two-dimensional geometry is described by the parameters b, d and a, the latter describing the island extension. In the 2D model an effective value for the island extension from the experimental coverage was calculated as $a = b\Theta$. As final result we obtain an analytic expression (see APPENDIX A) describing the capacitance $C_{SC}(\Theta,b)$ as a function of the geometric parameters.

$$C = A\frac{\epsilon_{ox}}{\mathrm{b}\,\pi}\left(\operatorname{arccosh}(u_4) - \operatorname{arccosh}(-1)\right) \tag{4.2}$$

Fig. 4.4a compares the theoretical results for the capacitance with the experimental findings. Using the observed island-spacing of $b \approx 200$ nm a good fit of the data was obtained despite the model's simplifications. The model allows to compare the impact of island spacing b on capacitance. Smaller b (equal to smaller characteristic feature size at constant coverage) lead to a reduction of bending of field lines until they become straight and capacitance becomes independent on coverage. Instead, increasing b leads to an increase of the bending of field-lines parting from uncovered areas. At very large island spacing ($b > 100\ d$) the contribution of bended field lines can be neglected and the plane capacitor approximation in which only areas covered by semiconductor are considered, starts to hold. As a consequence, the capacitance scales with the area covered by the semiconductor.

Charge transport through the transistor channel is governed by the surface charge density σ in the semiconductor. Knowing $C_{SC}(\Theta)$ σ was calculated as a function of Θ by using $\sigma(\Theta) = C_{SC}(\Theta)V_{SG}/A_P$ where $A_P = \Theta A_0$ at $\Theta < 1$ ML denotes the area covered by pentacene. A_0 is determined by the shadow-mask and gold electrode layout, here it amounts to $A_0 = 0.104$ cm^2. The result at $V_{SG} = 30$ V is plotted in Fig.4.4b. A maximum in σ is observed close to the percolation threshold. With increasing coverage, σ drops as the total constant charge distributes over an increasing area. At $\Theta > 1$ ML stability in σ is reached. The finding shows two competing effects which influence σ in the sub-monolayer regime: on the one hand, σ is reduced due to the partial coverage which leads to a small decrease in C_{SC} as field lines in the dielectric are bent. On the other hand σ rises as the accumulated charges become concentrated in the sub-monolayer covered area. The latter effect outperforms the former due to the close island spacing in the pentacene film and a maximum in σ is obtained close to the percolation threshold.

With the knowledge of $C_{SC}(\Theta)$, the transistor parameters such as mobility μ and threshold voltage V_t can be calculated from the transfer characteristics acquired during growth. The findings show that in the sub-monolayer regime a correction term has to be introduced to account for the increased carrier density due to lateral confinement in the uncompleted monolayer. The correction can be readily introduced into the standard equations for current in thin film transistors[10]

$$I_D = W[\sigma(x) - \sigma_t]\mu E(x) \tag{4.3}$$

where W being the width of the transistor channel, σ_t specifying the trap state density and μ the mobility, by introducing

$$\sigma(x) - \sigma_t = \frac{C_{SC}(\Theta)}{\Theta A_0}(V_{SG} - V_t - V(x)) \quad \text{for } \Theta < 1 \text{ ML} \tag{4.4}$$

with V_t being the threshold voltage. In order to analyze the acquired transfer characteristics in saturation regime ($V_{SD} > V_{SG} - V_t$), we integrate Eq. (4.3) to obtain

$$I_D = \frac{W}{2L}\frac{C_{SC}(\Theta)}{\Theta A_0}(V_{SG} - V_t)^2\,\mu\ , \tag{4.5}$$

L being the channel length. Fitting Eq. (4.5) to our dataset results in mobility μ and threshold voltage V_t as a function of Θ as depicted in Fig. 4.6.

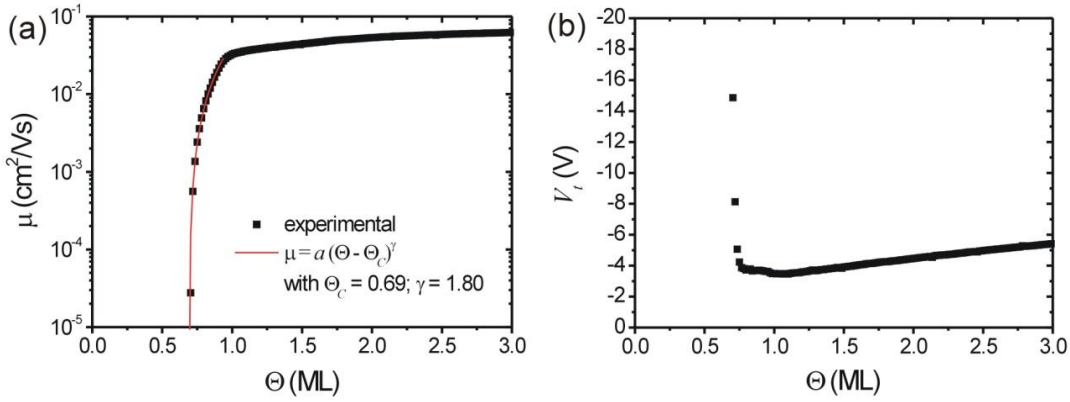

Fig. 4.6 *Mobility μ (a) and threshold voltage V_t (b) calculated from transfer characteristics acquired during growth of pentacene semiconducting layer at V_{SG} = -20 V and V_{SD} = -20 V. Correction for the increased charge density in the sub-monolayer regime has been included.*

At the onset of percolation several orders of magnitude increase in mobility exhibits a power law behaviour $\mu \propto (\Theta - \Theta_C)^t$. Here we find a percolation threshold of Θ_C = 0.69 and a critical exponent of t = 1.8 +/- 0.1. The increase of mobility follows the shape of the current increase as discussed above with characteristic kinks at Θ = 1 and 2 ML. The large increase in mobility during the growth of the first monolayer demonstrates its particular relevance for transistor performance. For the growth conditions chosen here, almost 60% of the final mobility is attained after the formation of the first monolayer. Addition of more than three monolayers do not further improve performance or can even

lead to a deterioration of properties.[19] The calculated threshold voltage V_t is shown in Fig. 4.6b. It starts right at percolation with a strongly negative value of V_t = -15 V but drops immediately to stabilize at Θ = 0.8 ML at a low value of around V_t = -4 V. The very negative initial value suggests an increased trap concentration at the onset of percolation. As an explanation we hypothesize that in the early percolation network the energy landscape experienced by carriers is strongly disturbed due the increased extension of confining interfaces where polarization interactions[20] are spatially varying and island interconnections may act as bottlenecks.

Further insight into transport in the sub-monolayer regime can be provided by comparing the values from the power-law fit of mobility to values from standard models of percolation theory.[21] In the initial phase of the monolayer, pentacene islands start to grow from nucleation sites that are almost randomly distributed over the surface. Percolation of randomly positioned objects is described in the literature by continuum models. The percolation threshold depends largely on the shape and anisotropy of the percolating objects. Close to the observed value of Θ_C = 0.69 is the percolation threshold of randomly positioned discs ($\Theta_{C,disc}$ = 0.67)[22] indicating a circular shape of the percolating pentacene islands. Several theoretical studies investigated the dependence of the critical exponent *t* of the electrical conductivity in systems composed of resistors and insulators (here corresponding to pentacene and bare dielectric) which are interconnected to form a resistor network.[21] Again the value of *t* depends on the dimensionality of the system and on the lattice geometry. Reported exponent values fall in the range of $t_{2D} \sim 1.3$ and $t_{3D} \sim 1.8$. Although for pentacene, the layer-by layer growth defines 2D percolation, the experimental finding for the percolation of the conducting pathway deviates and the exponent is larger and closer to the 3D behaviour. The increase in exponent results in a reduced slope in mobility at $\Theta = \Theta_C$. We postulate two possible causes for the non-ideality: (i) small deviations from the ideal layer-by-layer growth mode slow down the formation of additional conducting pathways at the initial percolation stage as material is used to form a second monolayer. Evidence for small deviations from layer-by-layer growth can be seen in the AFM topography as depicted in Fig. 4.5b where some pentacene islands contain already the second monolayer. (ii) The percolating resistor network model assumes constant local conductivity of the segments. For the pentacene film the local mobility is likely to be influenced by the morphology changes during the growth. In fact, Fig. 4.6a shows that the mobility continues to rise also after the

completion of the first monolayer, clearly demonstrating the relevance of other factors in addition to the geometric one.

Conclusion

In this study I have investigated carrier accumulation and transport in sub-monolayer pentacene transistors. In this model system charge transport is laterally confined within nanometer-sized islands forming a percolating network. I have demonstrated that the geometry of the network determines not only the percolation threshold and the critical exponent but also the density of charge carriers created by field effect. The latter effect was characterized in detail by displacement current measurements *in situ* during the formation of the semiconducting layer and by an analytical electrostatic model. Due to the nanostructured geometry with a characteristic island spacing similar to the size of the dielectric thickness, the gate field is only slightly bent in the dielectric and the capacitance governing carrier accumulation is almost independent of coverage once percolation threshold is exceeded. As a result, there is an increase in charge density in partially covered films. The experimentally determined capacitance allows us to analyze transfer characteristics acquired in the sub-monolayer regime and to extract mobility and trap state density. The findings are of general relevance for partially covered thin-film transistors where the plane capacitor model is not applicable due to nanoscale lateral confinement.

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Chapter 5 Charge Transfer and Percolation in C_{60}/Pentacene Field Effect Transistors

5.1 Introduction

The efficiency of charge transfer (CT) in organic electronic devices depends largely on specific interaction taking place at the interface between stacked layers of different materials. In opto-electronic devices such as Organic Photovoltaics (OPVs), Organic light emitting diodes (OLEDs) and organic light emitting transistors, CT processes, such as electron-hole separation or recombination, occur at interfaces between electron and hole transporting layers [1]–[4]. CT is driven by the alignment of their Fermi levels. The efficiency of CT depends on the alignment of the energy levels of molecules lying at the heterojunction, as well as on the molecular organization and the morphology of the interface[5]–[7]. In OPVs, CT results from the absorption of light whose outcome is an exciton. This exciton is able to diffuse in the layer where it was created. This process is largely controlled by the absorption spectra of the organic molecular layers, as well as their thickness and device architecture. The exciton can diffuse within an exciton diffusion length and dissociates into charge carriers that can be collected at the electrodes (Fig. 5.1) .[2] These processes depend on the morphology of the organic-organic heterojunction and of the p-and n-type layers and their charge carrier mobility.

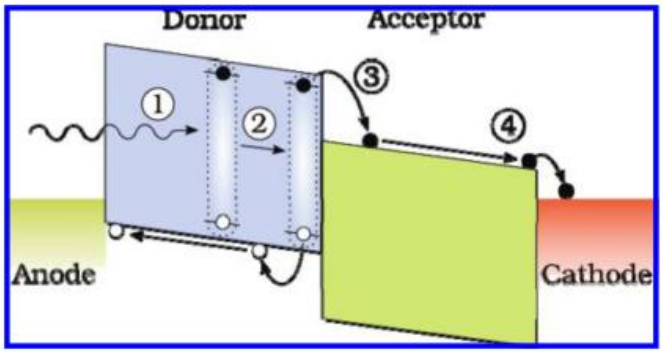


Fig. 5.1 *Energy diagram of an organic solar cell with a donor-acceptor interface. The four subsequent processes to generate photocurrent are (1) absorption of an incident photon to create an exciton, (2) diffusion of an exciton toward the donor-acceptor*

interface, (3) charge transfer of an exciton into an electron in the acceptor and hole in the donor, and (4) collection of charges at the contacts.[2]

In ambipolar transistors with stacked donor (p-type) and acceptor (n-type) thin films, it has been observed that the interface between the layers exhibits higher conductivity with respect to the individual layers. The enhanced source-drain current in ambipolar transistor [8]–[10] arises from CT between the two semiconductors, leading to accumulation of charge carriers at the heterojunction that. There have been several theoretical reports which discuss how the local morphology[6], [11] and the electrostatic interactions [12] determine the energy landscape where the separated carriers move, what is the role of molecular architecture[6], [13], interface geometry[14], polarization[15] and CT dipole moment[16]. Formation of a dual channel in fullerene C_{60}/pentacene ambipolar transistor was invoked by Noever *et. al* [17] to explain the shift in the threshold voltage upon increasing C_{60} thickness up to 6-7 monolayers (ML). The accumulation of mobile charges at the heterojunction formed by pentacene and C_{60} occurs after the percolation of C_{60}. However, since the morphology of thin films grown in non-equilibrium conditions undergoes roughening as thickness increases[18], [19], it is important to modulate the thickness of the donor and acceptor layer in order to understand the correlation between CT and morphology at an organic-organic heterojunction.

In this chapter, I will demonstrate the interplay between morphology and CT at the heterojunction by performing *in situ* real time electrical measurements of an ambipolar field effect transistor during the growth of the bilayer. We chose pentacene, as p-type, and C_{60}, as n-type materials, being a model donor-acceptor pair[20]. I study the charge transport phenomena at the heterojunction of the bilayer by monitoring in real time the electrical characteristics of an ultra thin film of pentacene during the growth of C_{60} on it. Pentacene grown by vacuum sublimation shows a 2D layer by layer growth for the first two molecular layers and then follows a roughening transition at higher thickness. Because of this growth phenomena, varying the thickness of the bottom pentacene layer would drastically change the morphology of the heterojunction between the pentacene and C60. With this motivation in mind, I performed thickness dependent study of the bilayer in order to correlate film morphology and thickness with CT processes.

5.2 *In situ* real time experiment

As substrates for the *in situ* experiments, I have used the standard test pattern consisting of a common gate made of highly doped n-type Si wafer with 200 nm thick layer of thermally grown silicon oxide (C_{ox} = 17.3 nF/cm^2) as gate dielectric. It consisted of interdigitated gold electrodes acting as source and drain contacts had channel length L = 20, 40 µm and width W = 11200, 22400 µm. The test patterns were cleaned by following a standardized protocol as discussed in Section 2.1 in Chapter 2 SiO_2 was functionalized with hexamethyldisilazane (HMDS) by thermal evaporation of HMDS over the cleaned substrate.

Pentacene and C_{60} (both by Sigma Aldrich) were grown by high vacuum sublimation at a rate of 6Å/min on the test pattern with transistor structures. First I grow an ultra-thin film of pentacene, then a C_{60} thin film on top (Fig. 5.2). In this manner the device is never exposed to air, thus avoiding accidental contamination of the interface. Source-Drain current I_{SD} was measured in real time every 3 seconds upon sweeping the gate potential V_G from +30V to -30V while keeping the potential at the drain V_{SD} at -30V during the growth of the bilayer. Three transistors were measured at the same time, and the extracted parameters averaged. During growth the electrical characteristics of the transistor were sampled at 50 Hz using a home-built setup described earlier [19], [21].

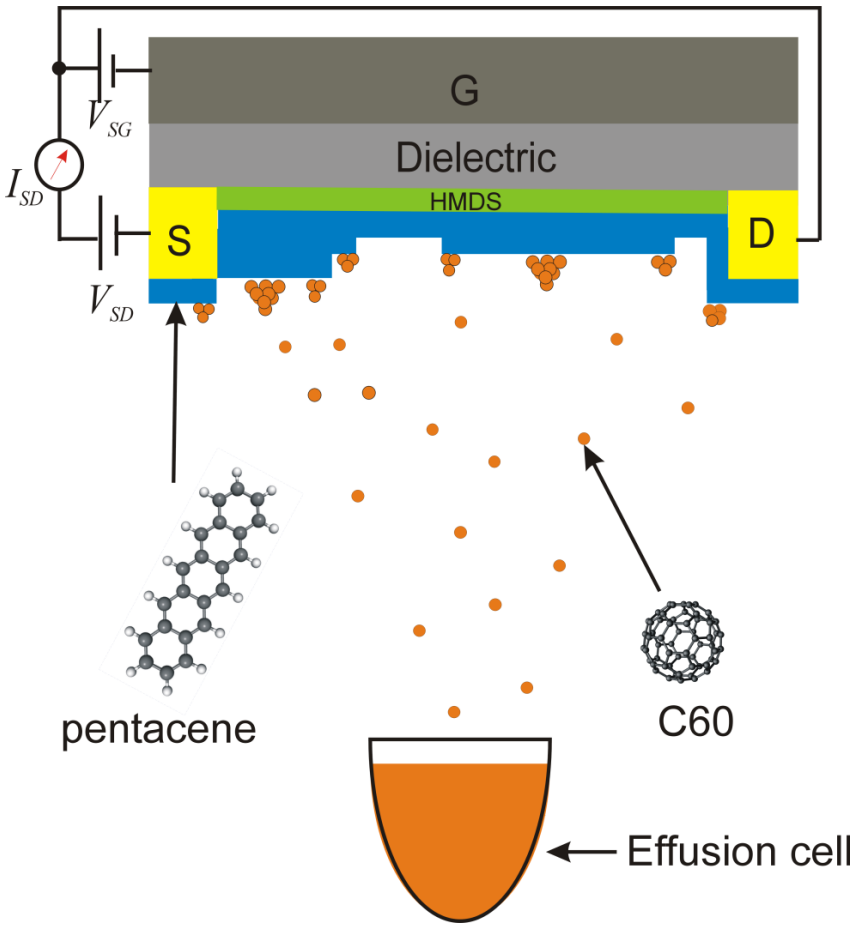
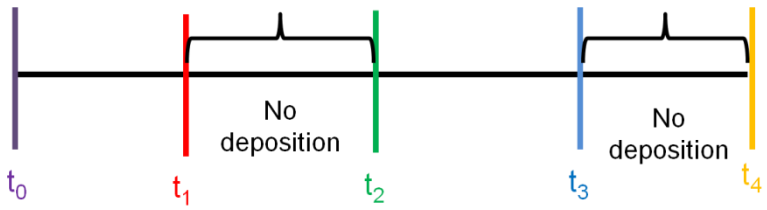


Fig. 5.2 *In situ real time experiment set up. The real time electrical characterization of the ultra thin of pentacene transistor during the deposition of C_{60}. V_{SG} and V_{SD} are the potential applied between the source and gate and between the source and drain respectively and I_{SD} is the source drain current being measured.*

The experimental procedure followed for deposition timings is shown in Fig. 5.3 For all the experiments the bottom layer consists of pentacene film onto which C60 is grown. At the very start of the *in situ* measurement i.e at $\mathbf{t_0}$, the *in situ* measurement program starts and the shutter of the sample holder is opened to allow pentacene growth on the substrate. The thickness of the film is monitored using a calibrated quartz microbalance. When the final thickness of pentacene film is reached at $\mathbf{t_1}$, the shutter is then closed. Electrical characterization is continuously being carried out in order to characterize only the underlying pentacene transistor as a function of time. This allows us to monitor the stability of the ultra thin film transistor. After about 10 minutes , i.e at $\mathbf{t_2}$, the sample holder shutter is open allowing the C_{60} deposition to start.



- t_0: Start measurement program and open shutter for pentacene
- t_1 : Close shuter pentacene
- t_2 : Open shutter C_{60}
- t_3 : Close shutter C_{60}
- t_4 : Close program

Fig. 5.3 *Sequence of timing followed during bilayer deposition of pentacene and C60.*

Care has to be taken that the time interval between $\mathbf{t_1}$ and $\mathbf{t_2}$ is not so long as the ultra thin film of pentacene deposited on HMDS treated surface is known to de-wet as a function of time [22]. Therefore I have made sure that $\mathbf{t_2}$-$\mathbf{t_1}$<10 minutes. When the final thickness of C_{60} is reached at $\mathbf{t_4}$, the sample shutter is closed and measurement continues until $\mathbf{t_4}$. At the end of the real time electrical characterization, post deposition *in situ* transfer curves were recorded.

The evolution of the bilayer morphology was carried out *ex-situ* using Atomic Force Microscopy (AFM Smena, NT-MDT, Moscow, Russia) measurement.

Moreover, structural characterization of the bilayer films were carried out. The 2D-GIXRD images were recorded at the XRD1 beamline at the Elettra synchrotron facility at Trieste (Italy) using a monochromatic beam with a wavelength of 1 Å. The incident angle of the X-ray beam, αi, was chosen close to the critical angle for total reflection of the organic film (i.e., 0.12°), in order to probe the whole film. The diffraction patterns were recorded using a 2D camera (Pilatus detector) placed normal to the incident beam direction. Specular XRD scans were performed using a SmartLab-Rigaku diffractometer equipped with a rotating anode (Cu Kα, λ = 1.54180 Å), followed by a parabolic mirror to collimate the incident beam, and a series of variable slits (placed before and after the sample position). The lateral and vertical crystalline domains size were evaluated from the peak width along q_{xy} and q_z directions, respectively, using the Scherrer-formula[23] and taking into account the resolution as described earlier[24].

5.3 Results and discussion

5.3.1 Morphology of the bilayer

Here, I will first start by discussing the growth evolution of the bilayer heterojunction. The device layout is shown in the schematics fig. 5.2 and fig. 5.3(a). The nominal thickness of each layer, measured with calibrated quartz microbalance, is expressed as the respective coverage in monolayers (ML). The conversion from coverage in ML to thickness in nm is based on the periodicity of the molecular planes of C_{60} and pentacene as measured on our samples with X-ray diffraction. We take the height of 1 ML C_{60} equivalent to the periodicity d=0.8 nm of the (111) stacking, and 1 ML pentacene equivalent to the periodicity h=1.5 nm of the (001) plane of the thin film phase of pentacene.[25] In our experiment, the final coverage of C_{60} (Θ_{C60}) film was held at 12.5 ML (10 nm), while the coverage of the bottom pentacene layer (Θ) was varied for different devices from 0, 1, 1.5, 2, 3, 4, 6 and 20 ML.

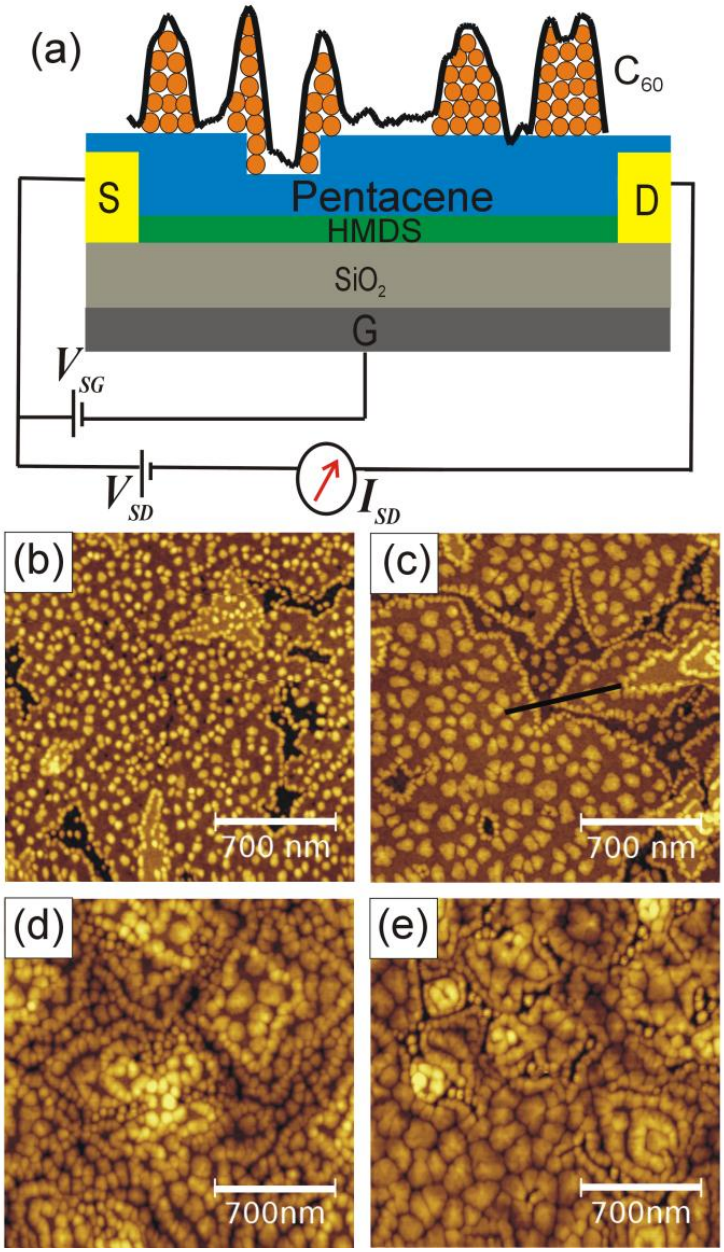


Fig. 5.4 *Morphology of C_{60}/ pentacene bilayer: (a) Schematic diagram of ambipolar C_{60}/pentacene FET. The profile drawn in Fig. 1c is displayed as the envelope of C_{60} molecules (represented as circles). (b-e) AFM topographical images at different C_{60} coverage on a 2 ML pentacene film: (b) 0.6 ML (0.5 nm) (c) 1.2 ML (1 nm) (d) 3 ML (2.5 nm) and (e) 6 ML (5 nm).*

Ex situ AFM imaging was performed on a set of bilayers comprising a Θ=2ML (3 nm) pentacene film at the bottom and a C_{60} film with Θ_{C60} increasing up to 12.5 ML (10 nm) on top. The morphological evolution is displayed in the AFM micrographs shown in fig. 5.4b-5.4e. C60 growth at the intial stage shows two distinct features: (i) C_{60} small grains

decorate step edges around pentacene islands, while (ii) larger C_{60} grains nucleate and grow on the basal plane of the island[26], [27]. The latter exhibit lower areal density. The line profile in fig. 5.4a (extracted along the line drawn on the AFM image in fig. 5.4c) suggests that C_{60} molecules are in intimate contact with pentacene at step edges. Fig. 5.4b,c display the early stage of C_{60} growth on pentacene film: terrace edges are decorated by strings of interconnected C_{60} grains ~30-60 nm wide and 2.6 nm (>3 ML) high, while C_{60} molecules nucleating on the basal plane form disc shape grains with average diameter 40-80 nm and height 1.6 nm (2 ML). As Θ_{C60} increases above 3 ML, the grains in the basal plane grow larger and coalesce into a connected percolation network across the pentacene layer (Fig. 5.4d,e).

This same growth phenomena is observed for various thickness of the underlying pentacene. The only difference is the number of terraces of pentacene islands increase with increase thickness. Or in other words, pentacene roughness increases with thickness. Fig. 5.5 shows another example of the morphology of the bilayer comprising of C_{60} and pentacene. In this case the thickness of pentacene Θ=3MLs and Θ_{C60} = 12.5MLs.

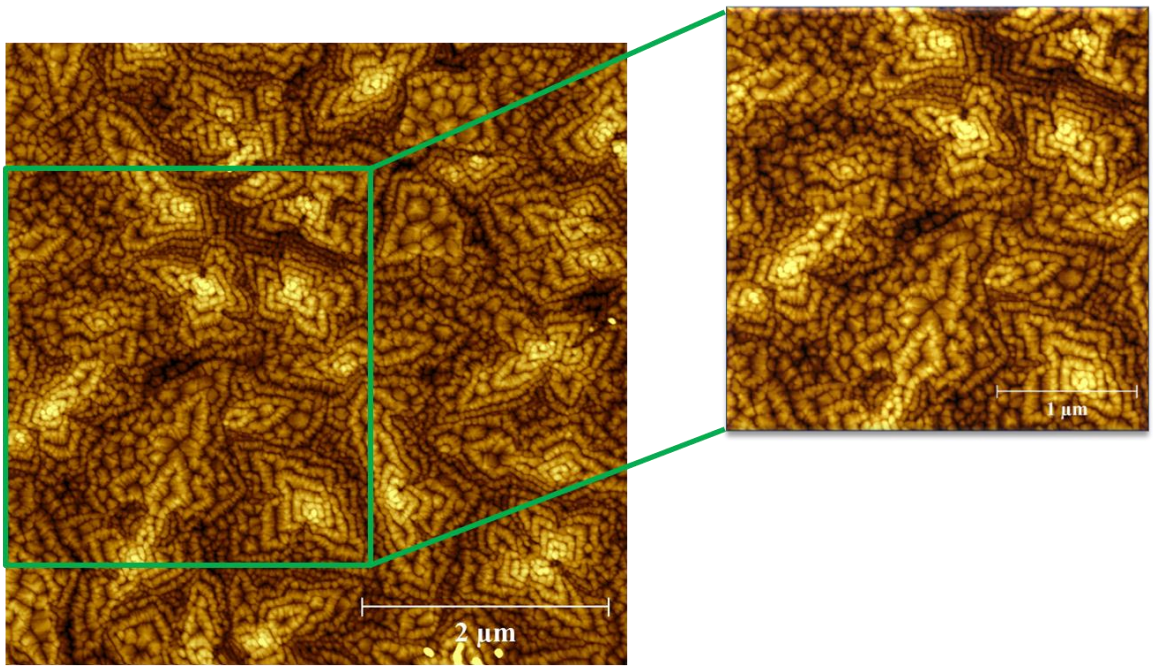


Fig. 5.5 *AFM image of a bilayer film comprising of Θ=3MLs and Θ_{C60} = 12.5MLs . On the left of size 5x5 um^2 and on the right an image obtained by zooming the depicted region(in green outline)*

5.3.2 In situ real-time electrical characterization.

Fig. 5.6a shows transfer characteristics recorded in real-time at different Θ_{C60} and Θ=2 ML. In the absence of C_{60}, there is not a detectable electron current at potential values greater than the turn-on voltage. The V-shaped transfer curve recorded as Θ_{C60} increases evidences the formation of the electron-conducting channel. Also the hole current in the pentacene layer increases and the turn-on voltage shifts to more positive values. The electron current increases by six decades at increasing $\Theta_{C60.}$ In fig. 5.6b the evolution of the maximum electron and hole currents extracted from the transfer curves as in fig. 5.6a is displayed. The plateau in the curve of the pentacene transistor before C_{60} deposition indicates that the charge transport channel is stable and bias stress is absent. As C_{60} film starts growing, the hole current increases less than 50% until it saturates at Θ_{C60} ≈4.5 ML.

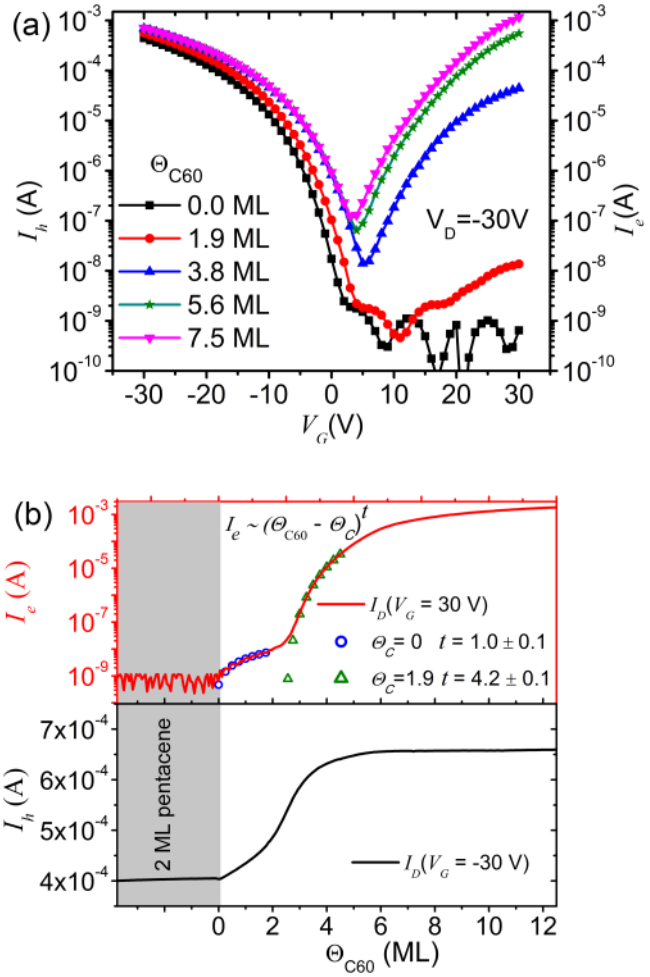


Fig. 5.6 *In situ real time electrical characterization (a) Representative transfer characteristics showing both hole current I_h and electron current I_e as recorded in real time during the growth of C_{60} on 2 ML pentacene transistor. Coverage of C_{60} film is shown in the legend together with applied drain bias. (b) Evolution of hole current (black solid line) and electron current (red solid line) during C_{60} growth on pentacene transistor. The values are extracted from the transfer curves recorded at V_G= -30V for hole current and V_G= +30V for electron current. Markers (blue circles and green triangles) on electron current curve are estimated from power law fit representing two distinctive percolative processes. Best-fit exponent t and critical coverage Θ_C are noted in the legend.*

The electron current shows a distinctive behavior. From the logarithmic plot in Fig. 5.6b, it is not possible to identify a percolation threshold at the onset of the electron current, because there is a significant current <10 nA above noise level (rms I=0.6±0.3nA) even at Θ_{C60} as low as 0.07 ML. The one order of magnitude rise of the electron current up to Θ_{C60} =2 ML indicates that electron transport occurs either along the interconnected C_{60} grains that decorate the step edges of the pentacene terraces or through pentacene (see

Fig. 5.4b). I fit the data in this range as $I_e \sim (\Theta_{C60} - \Theta_C)^t$. The best fit exponent t=1.0±0.1 supports the picture of 2D stick percolation, [28] that is also consistent with the observation of electron current at Θ_{C60} of a few percent ML. For Θ_{C60}>2 ML, the electron current very rapidly increases as a function of Θ_{C60}, following a power law scaling with t=4.2±0.1. This shows that percolation undergoes a transition from 2D-stick percolation to 2D-surface percolation above Θ_{C60}=2 ML. This interpretation is supported by the image in Fig. 5.4d at Θ_{C60}>2 ML where the interconnected network of C_{60} grains may enable percolation of electrons in 2D across the basal plane. The non-universal exponent t=4.2±0.1 suggests that transport of electrons involve tunneling injection between C60 grains.[29]

5.3.3 *In situ* characterization of the bilayer transistor after the real-time experiment

Without changing the environmental condition, post deposition transfer curves were obtained *in situ* after the real-time experiment. IV curves shown in fig. 5.7a shows the typical ambipolar transfer curve obtained which is similar to the ones depicted in fig 5.6a. Output curves (fig.5.6b and fig 5.6c) recorded in order to ensure the existence of the p-conducting channel and n-conducting channel. As we can see the, the p-type output shows negligible contact resistance as compared to the n-type output. The contact resistance observed is attributed to the poor charge injection in the n-channel as the work function of the gold electrode (~5eV) does not match perfectly with the LUMO level of C60(~3.8eV). The same is not observed in the p-type output as the work function of gold is very close to the HOMO level of pentacene. The superposition of the curves as seen in fig 5.6c is typical for ambipolar FETs because at high V_G we have a standard behavior for electron carrier and then we have a superlinear current increase for low V_G as we have also an injection of the opposite carrier.

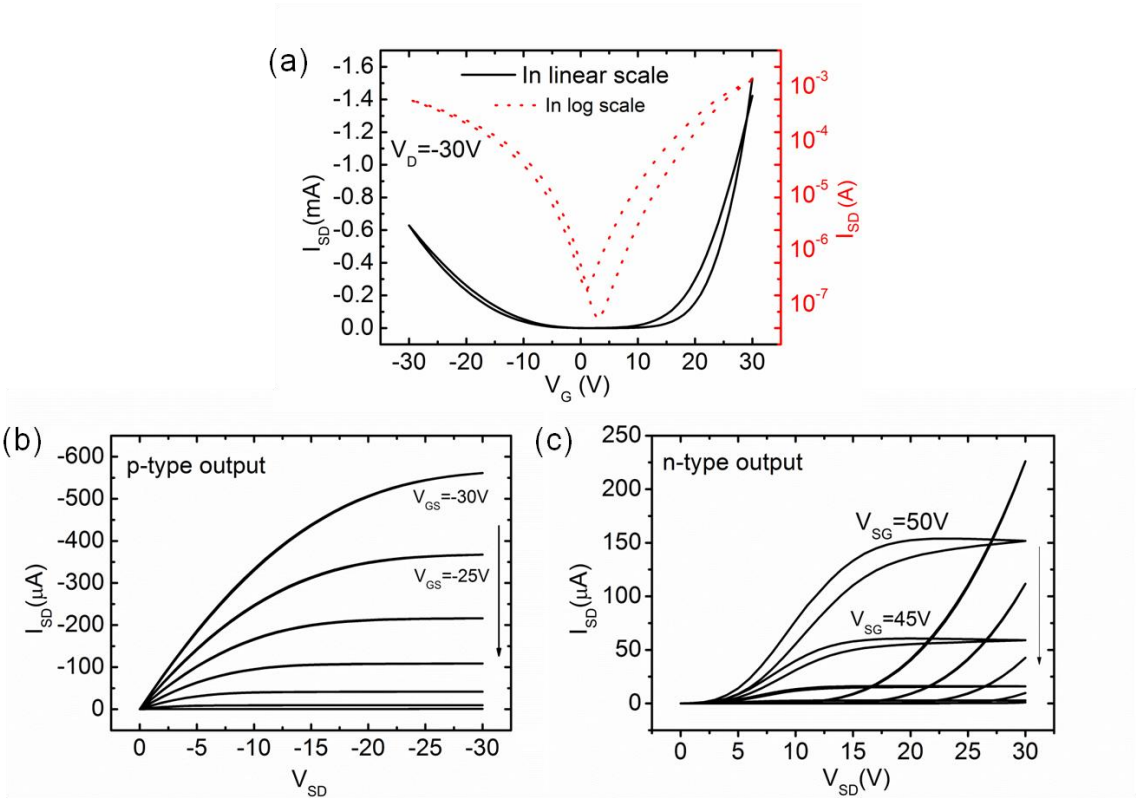


Fig. 5.7 *Post deposition transfer curves (a) plotted in the linear and logarithmic scale. (b) p-type output curve obtained for hole transport and (c) n-type output curve obtained for electron transport*

5.3.4 Structural characterization of the pentacene/C_{60} heterojunction.

Grazing Incidence X-Ray Diffraction (GIXRD) measurements (fig. 5.8) acquired at $\Theta_{C60}\approx$1.8 ML reveal the presence of high molecular order, with C_{60} grains (5 nm high and 20 nm wide, as calculated from the Full Width High Maximum (FWHM) of 22 rod and 111 peak, respectively) exhibiting [111] texturing (see Fig. 5.9). The same crystal structure is preserved during the C_{60} deposition up to 10 nm. This finding suggests a well ordered and oriented crystal packing already at the early stage of growth which allows the transport of charges through the grains formed at the terrace edges.

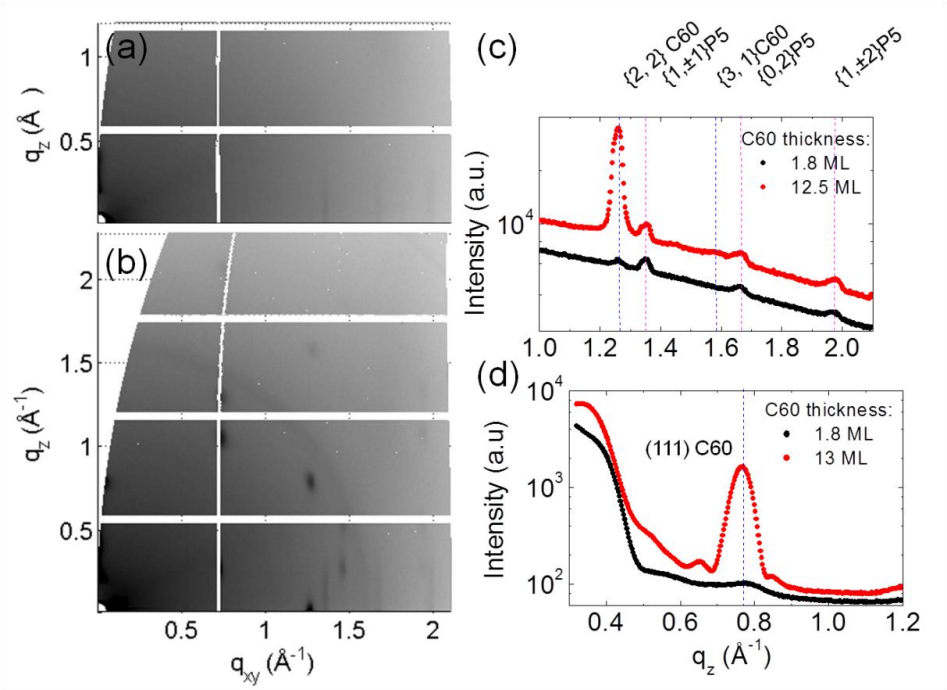


Fig. 5.8 *2D GIXD images of C_{60} on 2ML pentacene film (a) 1.8 ML of C_{60} and (b) 12.5 ML of C60 deposited on 2ML of pentacene film. (c) Scattering intensity integrated along the Yoneda(qz~0) of 2D-GIXRD images.(d) Specular XRD scans.*

5.4 Charge Transfer at the pentacene/C_{60} heterojunction.

The increase of the hole current upon C_{60} growth (Fig 5.6b black curve) is ascribed to two factors: i) the shift of the threshold voltage to more positive values, and ii) the increased mobility. Both of them are due to the additional density of charge carriers. The scenario is the following: i) CT across the heterojunction leads to accumulation of holes in pentacene and electrons in C_{60}; ii) a fraction of holes fills interfacial traps the rest being mobile; iii) electrons are mobile because an ordered and oriented C_{60} crystal packing provides efficient electron transport through the grains formed at the terrace edges at the early stages, and across the basal plane at later stages.

I extract from each transfer curve $I_{SD}(V_{GS})$ as in Fig. 5.6a the charge carrier mobility and the threshold voltage of both hole and electron current, from the equation

$$\mu_{sat} = \frac{2L}{WC_{ox}}\left(\frac{\sqrt{I_{SD}}}{V_{GS}-V_{th}}\right)^2 \qquad (5.1)$$

for the current in the saturation regime.

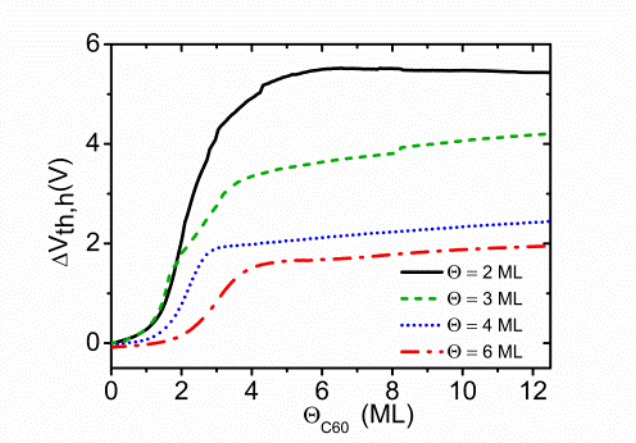


Fig. 5.9 *Characteristic shift in threshold voltage. Shift of threshold voltage of the hole current induced by the deposition of C_{60}. The legend shows the values of the pentacene coverage Θ of each device.*

In Fig 5.9 I show the threshold voltage shift of the hole current $\Delta V_{th,h}$ upon the deposition of C_{60}. For each pentacene coverage Θ, the reference value is the threshold voltage measured prior the deposition of C_{60} viz. at Θ_{C60}=0 ML. The correlation of the data shows the advantage of using *in situ* measurement since the chemistry of the interfaces is not altered by adventitious species. The onset of the shift $\Delta V_{th,h}$ occurs immediately upon deposition of C_{60}, and saturation is observed when $\Theta_{C60}\approx$4 ML. The slope in the rising section depends on the thickness of the pentacene film, decreasing at larger coverage. The positive shift of the threshold voltage by a few volts indicates that the pentacene layer is progressively "doped" by mobile holes due to CT from the donor (pentacene) to the acceptor (C_{60}) layer. CT adds mobile charge carriers in both hole and electron channels until the alignment of the Fermi level is attained. At this point the threshold voltage saturates.

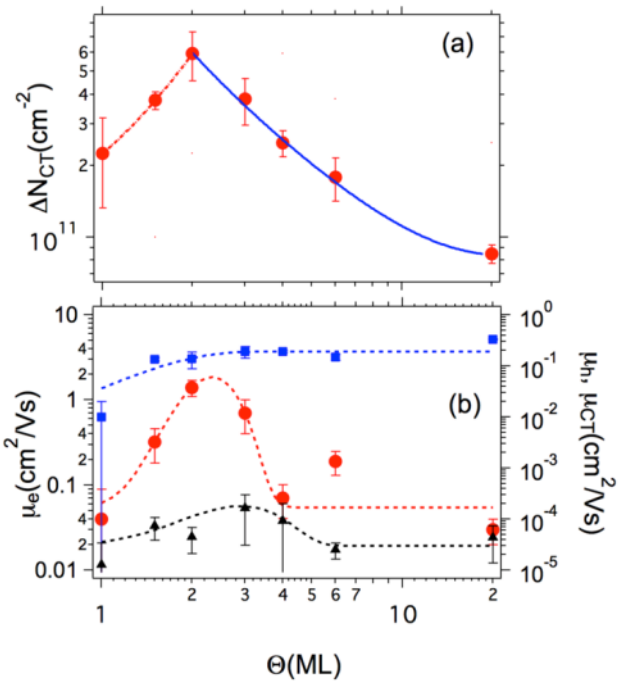


Fig. 5.10 *Charge transport parameters vs pentacene coverage in ML (a) Additional surface density of charges from eq. 1. Thickness of C_{60} was 12.5 ML. The best-fit lines with the functional eq. 6a (hyphen) and 6b (blue solid) are shown. (b) Charge carrier mobility from transistor transfer curves: electron mobility (left axis, red circles) and hole mobility (right axis, blue squares); mobility of CT charges as from eq. 7 (right axis, triangles). Dashed lines are guide-to-the-eye by phenomenological functionals.*

The additional charge number density generated by CT is given by:

$$\Delta N_{CT} = \Delta N_{hole} = \Delta N_{electrons} = \frac{C_{ox}\Delta V_{th,h}}{e} \tag{5.2}$$

where e is the elementary charge and C_{ox} is the capacitance of the silicon oxide gate dielectric.

Fig. 5.10a shows the trend of ΔN_{CT} as from equation (1) vs pentacene coverage Θ. ΔN_{CT} initially increases for coverage up to Θ=2 ML, that corresponds to the onset of the roughening transition of pentacene[18]. At Θ<2 ML CT states are not stabilized because of weak polarization due to an incomplete "bulk" milieu .[30] When Θ=2 ML the accumulation/charge transport layer is largely completed. [18], [19] At Θ>2 ML, ΔN_{CT} decreases monotonically. At larger coverage the roughness of the pentacene film increases due to a proliferation of terraced islands.[31] Pentacene roughening layers above the accumulation layer are largely disconnected and act as a polarizable dielectric

between holes in the accumulation layer and electrons at the C_{60}/pentacene interface. The weaker electrostatic coupling between the dielectric/pentacene interface and the C60/pentacene interface, leads to a decrease of ΔN_{CT} the heterojunction.

The above mentioned arguments can be translated into a simple electrostatic model to explain the data in Fig. 5.9 and 5.10(a). C_{60} adds an electrostatic (negative) potential $V_{C60,0}$ at the upper pentacene interface thus acting as a second top gate for the holes in the channel:

$$\Delta N_{CT} = \left[-\frac{C_{top}(\Theta) V_{C60,0}}{e} \right] \left[\frac{S_A(\Theta, \Theta_{C60})}{A} \Theta_{C60}^{\gamma} \right] \tag{5.3}$$

The exponent γ depends on the dimensionality and size distribution of C_{60} grains. C_{top} is the capacitance of pentacene growing above the accumulation layer. We define $\Theta_r \approx 2$ ML as the critical coverage at which the roughening transition of pentacene occurs.[19] For $\Theta < \Theta_r$ the growth mode is layer-by-layer, while for $\Theta > \Theta_r$ the growth mode proceeds by stacked terraces forming island on the second monolayer. The ratio S_A/A between the pentacene surface area S_A accessible to C_{60} grains and the geometrical area A of the transistor channel depends on the morphology of pentacene (modulated by Θ), and on Θ_{C60}:

$$\frac{S_A}{A} = (\Theta_{C60} - \theta) \cdot \sum_{n=1}^{N} \frac{(A_n - A_{n+1})}{A} + \theta \sum_{n=1}^{N} h \cdot \frac{P_n}{A} = (\Theta_{C60} - \theta) \cdot \Theta_1 + \left(\frac{k \cdot h}{A^{1-D/2}} \right) \cdot \theta \cdot \sum_{n=1}^{N} \Theta_n^{\frac{D}{2}} \tag{5.4}$$

Equation (5.4) embodies characteristic features of the pentacene morphology and its C_{60} adlayer: the stacked monolayer terraces (through the discrete index *n*), their "fractal shape" and roughness (through the self-affine relation perimeter P_n vs A_n [32] and the occupancies Θ_n) and the non-homogeneous partition of C_{60} between edges and basal plane through the fractional weight θ/Θ_{C60}. The first sum in equation (5.4) is the area of the basal plane (assuming the exposed pentacene terraces are wider than the diameter of C_{60} grains), being Θ_1 the coverage of the first monolayer in contact with the gate dielectric; the second term is the area of the terrace edges under the assumption that the coastline fractal dimension *D* (a number between 1 and 2) is the same for all terraces independently on the specific number of the stacking layer (i.e. the index n). This makes the relation $P_n = kA_n^{D/2}$ between perimeter P_n and area of the islands A_n to hold[33], [34], *k*

being a constant that imparts the proper physical dimensionality. The sum indices run to infinity, albeit is convenient to cut them off. The quantities S_A/A, D and θ are extracted from AFM images of pentacene films vs Θ. Here we fix the values for D according to the analysis of AFM images: D=1.08 for Θ<1 ML, and D=1.25-1.35 for Θ>2 ML depending on the estimation method (cube counting or perimeter vs area plot respectively). For Θ≥1 ML, i.e. the relevant range where the *in situ* real time characteristics are acquired, we propose a simple approximation to Equation (5.4):

$$\frac{S_A}{A} \approx \left(\Theta_{C60} - \theta\right) + \theta \cdot k_{eff} \Theta^{\frac{D}{2}} \tag{5.5}$$

This is a phenomenological extension of the exact expression for Θ≥1 ML. We assessed it by plugging analytical expressions for $\{\Theta_n\}$ from growth models[35], [36] to find that it underestimates the effective exponent by no more than 6%. The next step consists of introducing the rough morphology of the pentacene layer in the functional Equation (5.4). For $\Theta \leq \Theta_r$ C_{60} is in close proximity of the accumulation layer and our *ansatz* is:

$$C_{top}\left(\Theta\right) = \frac{\varepsilon_0 \varepsilon_{osc}}{\lambda_0} \tag{5.6}$$

whereas for $\Theta > \Theta_r$ the capacitance is ascribed to the effective thickness above the transport layer:

$$C_{top}(\Theta) = \frac{\varepsilon_0 \varepsilon_{osc}}{h(\Theta - \Theta_r) + \lambda_0} \tag{5.7}$$

Here ε_0 is the vacuum permittivity, ε_{OSC} the relative permittivity of pentacene ≈3.9±0.25 [37], λ_0 is pentacene Debye screening length ≈ 1 nm. The fitting functional is derived by plugging equations (5.5) and (5.6) into equation (2) for $\Theta < \Theta_r$ to yield:

$$\Delta N_{CT} = K_1 + K_2 \Theta^{\frac{D}{2}} \tag{5.8}$$

where $K_1 = [\Theta_{C60} - \theta]\left[\frac{-\varepsilon_0 \varepsilon_{OSC} V_{C60,0} \Theta_{C60}^{\gamma}}{e\lambda_0}\right]$,

$$K_2 = \left[\frac{-\varepsilon_0 \varepsilon_{OSC} V_{C60,0} \Theta_{C60}^{\gamma} \theta k_{eff}}{e\lambda_0}\right]$$

and equations (5.5) and (5.7) into equation (5.3) for $\Theta > \Theta_r$ to yield:

$$\Delta N_{CT} = \frac{K_3 + K_4 \Theta^{\frac{D}{2}}}{(\Theta - \Theta_r) + (\lambda_0 / h)} \tag{5.9}$$

where $K_3 = [\Theta_{C60} - \theta]\left[\frac{-\varepsilon_0 \varepsilon_{OSC} V_{C60,0} \Theta_{C60}^{\gamma}}{eh}\right]$,

$$K_4 = \left[\frac{-\varepsilon_0 \varepsilon_{OSC} V_{C60,0} \Theta_{C60}^{\gamma} \theta k_{eff}}{eh}\right]$$

Equation (5.8) predicts the additional charge density to scale as the power law of Θ with the exponent $D/2$ due to the increase of the accessible surface area; Equation (5.9) predicts that for $\Theta > \Theta_r$ the hole density decays as the inverse separation distance of C_{60} from the accumulation layer. We fix $D/2$=0.65 from the AFM value and set Θ_r=2 ML. Equation (6a) has two free parameters (K_1, K_2), whereas Equation (6b) has three (K_3, K_4, λ_0/h).

The best-fit curves are shown as continuous lines in Fig. 5.10(a). Based on the agreement of the data with Equation (5.9), I infer that the capacitive coupling of C_{60} with a single hole channel explains the data, differently from the dual channel invoked in ref.17. Moreover, I find the Debye length λ_0 to be on the order of 1-2 nm.

The charge mobility of the devices are modulated by the pentacene thickness. The trend of the modulation is shown in Fig. 5.10b. Hole mobility increases and saturates. Electron mobility exhibits a maximum value $\mu_e \approx 1.4$ cm^2/Vs at 2 ML pentacene coverage and 12.5 ML (10 nm) thickness of C_{60}. The maximum electron mobility coincides with the inflection point of the hole mobility *vs* Θ occurring at the completion of the second monolayer [19] whose value $\mu_h \approx 0.2$cm^2/Vs. The large value of the electron mobility to

two factors: the highest density of CT states in pentacene at the inflection point (maximum dI/dΘ) that maximizes the CT rate, and the high crystalline nature of C_{60} films deposited on few monolayers of pentacene [38], [39]. Our maximum μ_e value should be compared to μ_e=4.9 cm^2/Vs , viz. the highest reported for C_{60} [38].

To establish the correlation between electron and CT carriers, we estimate the charge mobility of the CT carriers from the increase of the off-current I_{off} of pentacene transistor during the C_{60} deposition:

$$\mu_{CT}(\Theta) = \left(\frac{L}{W} \cdot \frac{1}{eV_{SD}} \right) \cdot \frac{I_{off}(\Theta)}{\Delta N_{CT}(\Theta)} \tag{5.10}$$

The mobility of CT carriers vs Θ has a non-monotonic trend as shown in Fig. 5.10b.

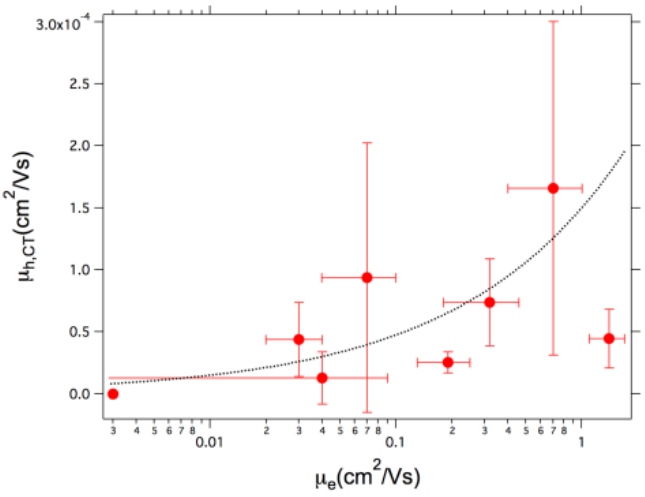


Fig. 5.11 *Correlation plot between CT mobility and electron mobility.*

Fig. 5.11 shows the positive (albeit non-linear) correlation between the mobility of electrons and that of CT carriers, the latter being about 1000 times less dense than the electrons generated by field-effect accumulation. These CT carriers move into an energy landscape characterized by interfacial disorder that introduces density of states, with dispersed spatial localization, in the HOMO-LUMO gap [40]. The fraction of charges generated by charge transfer from the HOMO state of pentacene to the LUMO state of C_{60} obeys Boltzmann statistics $\frac{\Delta N_{CT}}{N_0 + \Delta N_{CT}} = \exp(-\Delta E_{CT} / k_b T)$. Here ΔE_{CT} is the difference in energy between the CT states and the neutral states, whose density N_0 is

given by the number of pentacene molecules per unit area $N_0(\Theta)$ = $\rho/MM \cdot N_A \cdot h \cdot \Theta \approx 4 \cdot 10^{14} \cdot \Theta$, where ρ is the mass density, MM the molar weight, N_A Avogadro's constant. We neglect the population of mobile carriers (smaller than $N_0/1000$) that should be subtracted to N_0. Since CT occurs for molecules at the pentacene surface, whose number is comparable to those on the basal plane $N_0(\Theta=1\ ML) \approx 4 \cdot 10^{14}$, it turns out that:

$$\Delta E_{CT} \approx -k_b T \ln\left(\frac{\Delta N_{CT}}{4 \cdot 10^{14}}\right) \tag{5.11}$$

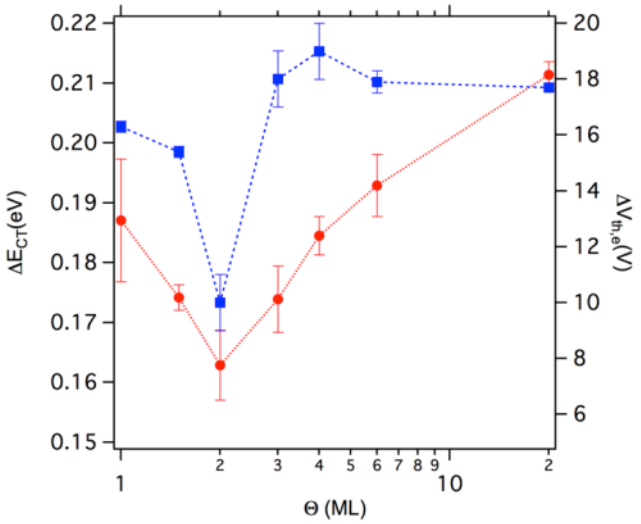


Fig. 5.12 *Energy gap and shift in electron current threshold voltage vs pentacene coverage (in ML) (left axis, circles): Energy gap as (from eq. 5.11) vs pentacene coverage Θ; (right axis, squares): shift of the electron current threshold voltage with respect to that of a 10 nm thick C_{60} field effect transistor (Θ=0). Error bars are estimated by error propagation.*

In fig. 5.12 left axis the values calculated from Equation (5.11) at room temperature are shown. The minimum value is $\Delta E_{CT,min} \approx 0.16$ eV at 2 ML pentacene and increases to about 0.20 eV for pentacene films of different thickness. These values are lower than 0.5eV expected from the unperturbed electronic structure of C_{60} and pentacene. These results suggest that interfacial CT involves intermediate states whose energy is strongly shifted with respect to the unperturbed HOMO and LUMO orbitals. The intermediate states or the density of states arise from coulombic interaction between the hole electron pairs (fig. 5.13)

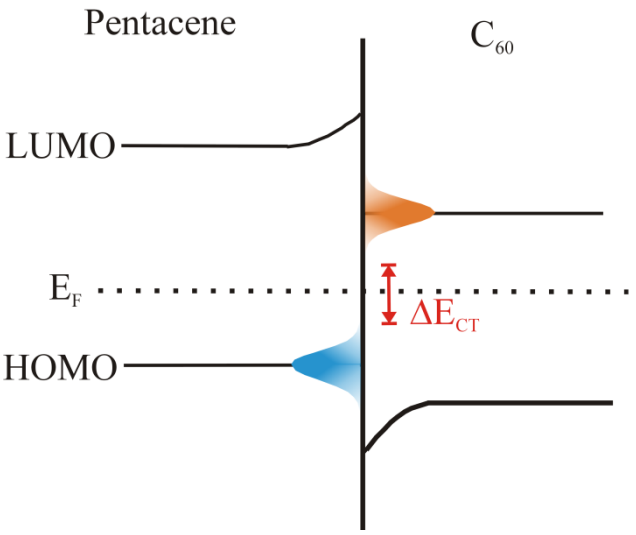


Fig. 5.13 *Energy diagram depicting the energy levels of for charge transfer. Blue and brown Gaussian curve represents the density of states present at the heterojunction. ΔE_{CT} is the energy difference of the charge transfer states.*

Fig. 5.12 right axis shows the corresponding threshold voltage shift for electron current $\Delta V_{th,e}$ (left axis) vs pentacene coverage for 10 nm C_{60}. The values are estimated subtracting the threshold voltage of the unipolar transistor with 10 nm C_{60} and no pentacene on it. The trend of $\Delta V_{th,e}$ is clearly correlated to that of the energy gap. At large pentacene coverage the threshold voltage shift saturates as the decreasing capacitance prevents additional CT. The data trend suggests that electrons are mostly transferred when the coverage of pentacene film is below 3 ML, hinting that CT at terrace edges, despite the higher transfer rate with respect to the basal plane [14], contributes less than the CT process on the basal plane because of its smaller cross section.

5.5 Conclusion

In conclusion, by performing *in situ* real time electrical characterization on C_{60}/pentacene ambipolar transistor, I was able to probe CT processes during the formation of an organic-organic heterojunction. *In situ* electrical measurements in combination with AFM reveal that charge transport of electrons follows two distinct percolation pathways: one along the edges of pentacene islands and the other across the basal plane. The observed positive shift in threshold voltage results in an increase in hole current from the beginning of C_{60} deposition. This evidence strongly hints to an initial "doping" due to CT at the edges of pentacene islands. The evolution of the ambipolar FET parameters is explained by the capacitive coupling between C_{60} and pentacene in the accumulation layer, which is

consistent with a single hole transport channel. The values of the hole and electron charge transport parameters evidence that the optimum charge transport with high mobilities of both hole and electrons occurs when the hole accumulation layer is either completed or has achieved highest density of charge carriers, else when the distance between hole accumulation/transport and electron accumulation/transport layers is minimum. Beyond the specific ambipolar device, the fundamental aspects discussed here are useful to understand the mechanisms by which an organic transistor responds to the interactions with the outer environment. This is central to the control of sensitivity and specificity of environmental and biomedical sensors based on organic semiconductors.

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Chapter 6 Double layer capacitance measured by organic field effect transistor operated in water

6.1 Introduction

As discussed in the earlier chapters, an OFET response strongly depends on the specific interactions taking place at the various interfaces. One of these interfaces is the electrolyte- semiconductor interface. Initially the interest on this interface stems out from the fact that devices based on organic semiconductor materials often show instabilities in their performances in particular in the presence of moisture.[1] The moisture induced instability is explained as a consequence of the interaction of charges in the semiconductor with polar molecules and solute ions of the electrolyte which thus changes the electrical response of the transistor.[2] Possible degradation processes include redox reactions involving water and oxygen [3], structural instabilities of the organic film and charge carrier scattering and trapping due to polar impurities.

Today, the electrolyte -semiconductor interface is gaining a lot of attention due to an increasing interest in applying organic electronic devices at the interface with life science also known as organic bioelectronics. The term "organic bioelectronics" was first coined by Berggren and Richter-Dahlfors.[4] [5] The field of Bioelectronics itself dates back in the 18th century with the experiments of Luigi Galvani, who applied a voltage and made the detached leg of a frog move. Since then, a variety of bioelectronic devices are available that offer improved healthcare. These include biosensors such as glucose monitors for diabetics, pacemakers/defibrillators and cochlear implants for restoration of lost or damaged physiological functions, and biomedical instruments that provide a deeper understanding of the how cells communicate with each other and with their environment. One of the main interest in employing organic materials as the active material for application in bioelectronics is because they are mechanically soft and foldable which makes them easy to interface with "soft" biological systems.

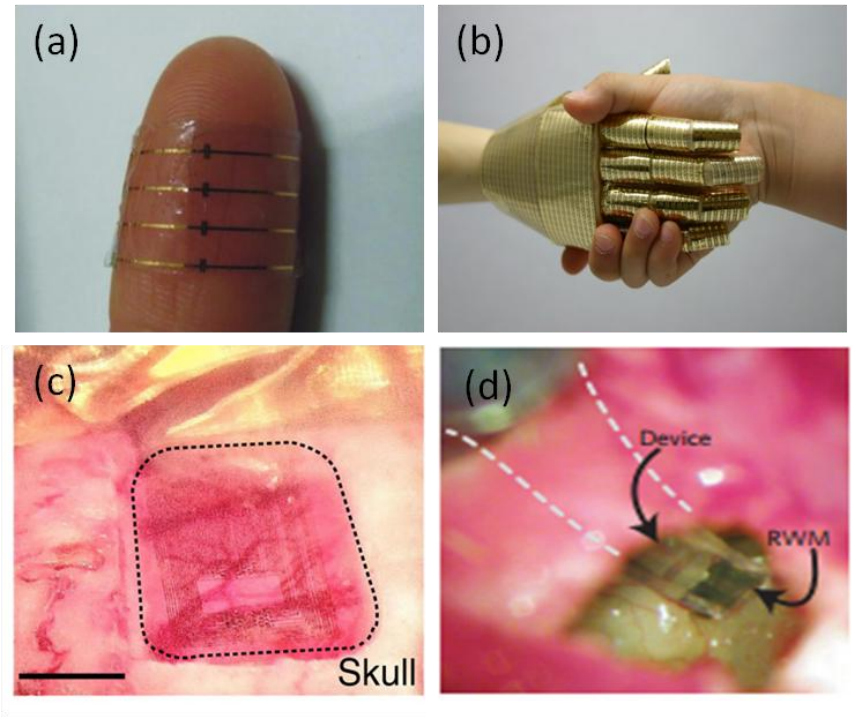

Fig. 6.1 *State of the art organic bioelectronic devices. (a) Electrocardiogram recording by means of electrochemical transistor fabricated on bioresorbable substrate [6]. Electronic skin made by grinding carbon nanotubes, with an ionic liquid and adding it to rubber.(c) Optical micrograph of the electrocorticography probe placed over the somatosensory cortex, with the craniotomy surrounded by dashed lines.[7] (d) Photograph of the organic electronic ion pumps mounted on the round window membrane of the cochleae, for controlled neurotransmitter release.* [8]

Organic bioelectronic devices include (i) flexible, low impedance organic microelectrode arrays (OMEAs) for neuronal recordings [9] (ii) organic electronic ion pumps (OEIPs) for controlled neurotransmitter release and (iii) organic electrochemical transistors (OECTs) for biosensing applications.[8], [10]–[12]. All of these devices have to interact with biological systems and thus have to be operated in a aqueous environment. A new architecture that is emerging recently in the field of bioelectronics is the Electrolyte Gated Field Effect Transistor (EGOFET). In these devices, the electrolyte-semiconductor interface is exploited.[13], [14] The difference between traditional bottom gate OFETs and EGOFETs is the dielectric. While in the former configuration, gating of the transistor is done via solid dielectrics, in the latter the gate is separated from the organic semiconductor by an electrolyte. The potential application of EGOFETs as biological sensors and transducers depends on the strong capacitive coupling between the electrolyte and the semiconductor, device stability and fast switching speeds.[15] A bias between

the gate electrode immersed in the electrolyte and the source-drain bias of the transistor gives rise to a difference in the electrostatic potential between the electrolyte and semiconductor. And as a results an electric double layer (EDL) is formed which constitutes the Debye Helmoltz layer in the electrolyte and the electrical charges in the semiconductor. This EDL has a large capacitance as its thickness is in the sub nm lengthscale. The electrostatic coupling that takes place at the interface between the organic semiconductor and the electrolyte and the amount of charges is modulated by the potential applied externally to the gate which is a metal electrode immersed in the solution.

EGOFET architectures have been realized by many organic semiconducting materials. Kergoat *et.al* have demonstrated the operation of ruberene and P3HT based EGOFETs gated by two different electrodes gold and platinum respectively.[15] The capacitive coupling has been investigated by impedance spectroscopy for semiconductors deposited on gold electrodes. The capacitance measured is of the range of 2-8μF/cm^2. [15]–[17] By exploiting the capacitive coupling in these devices, EGOFETs have also demonstrated to be an ideal device architecture for sensing applications. [18] Buth et al has illustrated the sensitivity of the transistor to the change in the pH of the solution which is manifested in the modulation of the threshold voltage.[17]

The work described in this chapter aims in understanding the origin of instability of pentacene based bottom gated OFET in the presence of water. Moreover , due to the increase interest in using EGOFETs as biosensors and transducer, I demonstrated a working pentacene based EGOFET device since pentacene based OFETs has already shown its potential application as a biological sensor even in the dry state.[19]. Most importantly I have established an experimental protocol which is the dual gate measurement that allows the direct extraction of the capacitance of the EDL formed at the interface between the electrolyte and pentacene.

6.2 Working principle of EGOFET

A schematic of the working principle of electrolyte-gated OFET is shown in Figure 6.2. Just as conventional bottom gated OFETs fabricated using more EGOFET operates in an accumulation mode, with the polarity of the applied gate bias (V_G) being opposite to that of the mobile charge carriers induced in the organic semiconductor at the

semiconductor/dielectric interface. An electrostatic, capacitive coupling of the gate bias across the dielectric layer to the semiconductor induces charge carriers in the semiconductor channel, and the source–drain bias (V_D) drives these carriers to obtain an output current. In fig. 6.2, a negative bias V_G applied to the gate electrode produces a negative surface charge on the metal electrode that attracts mobile cations in the electrolyte and forms an EDL at the gate/electrolyte interface. Anions are repelled from the gate and a layer of anionic charge is created at the opposite electrolyte/semiconductor interface. These anionic charges induce the holes in the semiconductor (p-type) which results in the formation of another EDL at the electrolyte semiconductor interface. The critical feature of the electrolyte-gated OFET, therefore, is the formation of these two EDLs in series, which are located at the gate/electrolyte and electrolyte/semiconductor interfaces with charge-neutral electrolyte between them. [20]

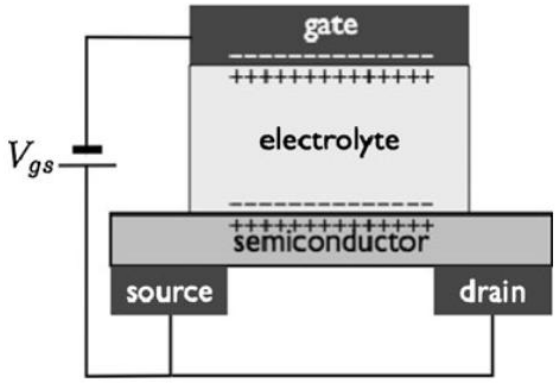

Fig. 6.2 *An electrolyte gated field effect transistor configuration. The conducting channel in the organic semiconductor is depicted. One can see the electric double layer formed at the semiconductor electrolyte interface and the gate-electrolyte interface.* [21]

In order to understand and optimize the working of an EGOFET, a closer look to the EDL structure is crucial. Due a sub-nm length scale, the EDL has a large capacitance and already small potential differences smaller than 0.1V leads to a sizable charge density in the semiconductor channel close to the interface. Therefore this interface is extremely effective for modulating the transistor current response.

6.3 Dual gate measurement setup

The dual gate configuration is shown in fig.6.3.

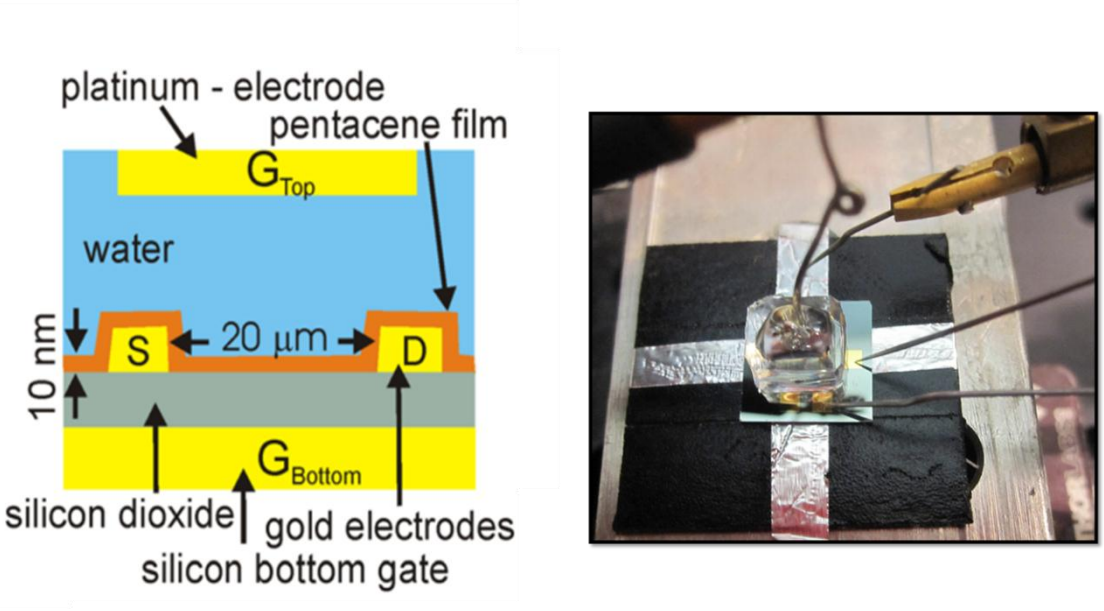

Fig. 6.3 *Dual gate transistor. (Left) Schematic diagram of the dual gate transistor layout* [22] *and (Right) a photograph of the dual gate measurement set up*

Dual gate pentacene EGOFETs are fabricated on a substrate which is made of highly doped n-type silicon wafer with a thermally grown 200nm thick layer of silicon oxide (C_{ox}=17.25nF/cm^2) acting as a dielectric and interdigitated gold electrodes acting as source and drain contacts which are photolithographically defined. In total there are 4 transistors in one substrate with two different geometries (L=20, 40 µm and W=11200 and 22400 µm respectively). The two gate electrodes comprise of the conventional bottom gate and the second one is the platinum wire immersed in the electrolyte.

Prior to the experiments, the substrate was cleaned thoroughly by first rinsing it with acetone, followed by dipping it in hot piranha (65 degrees for 15minutes) and then finally etched by dipping the substrate in hydrogen fluoride (HF 2%). Pentacene deposition was carried out in high vacuum chamber (Base pressure < 10^{-7}mBar). Deposition was performed by thermal sublimation of the semiconductor at a rate of 0.7nm/min. The average thickness of pentacene is 10nm and the thickness is monitored by a calibrated quartz microbalance. A drop of bi-distilled water / saline solution is confined by using a 100 µm thick Polydimethylsiloxane PDMS stamp which acts a pool

around the transistors. Electrical characterization was performed using the Keithley 2612 Source Measuring Unit .

6.4 Experimental results

The first attempt is to understand the stability of charge transport processes in traditional OFETs in the presence of water. IV measurements were performed where we apply a potential only to the conventional bottom gate while the top gate was kept grounded. The potential window applied to the bottom gate was from +40V to -40V while the drain voltage V_D was kept at low potential of -0.1V due to the presence of the electrolyte. The curve obtained is shown in fig. 6.4.

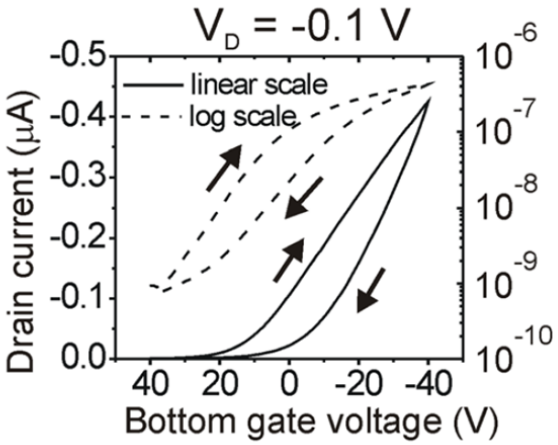

Fig. 6.4 *Transfer characteristics of pentacene based OFET in the presence of an electrolyte on top of the semiconductor. The arrows indicate the direction of the hysteresis both in the linear scale and log scale* [22]

Despite a direct contact of the few monolayers of the semiconductor (Pentacene) with water, both the transfer characteristics show on a linear as well as on a logarithmic scale the typical IV characteristics for p-type OFETs operated in linear regimes (Fig. 6.4). The on-off ratio is greater than 300. The transconductance of the curve is similar to the ones for devices operated in vacuum, however, the transfer curves shows a large hysteresis. This is a typical bias stress effect due to the presence of water . The reason for this bias stress effect is explained in the section of the discussion. This transistor however is not stable for a long time under continuous measurement. The instability of the pentacene transistors over prolonged times in water is attributed to proton migration through the oxide-dielectric at negative gate potentials. The transfer curve in fig. 6.5 shows a typical

transfer curve of a broken device. The characteristic feature shows a diode like behaviour of the leakage current. The source drain current is high as well due to the breakdown of the device.

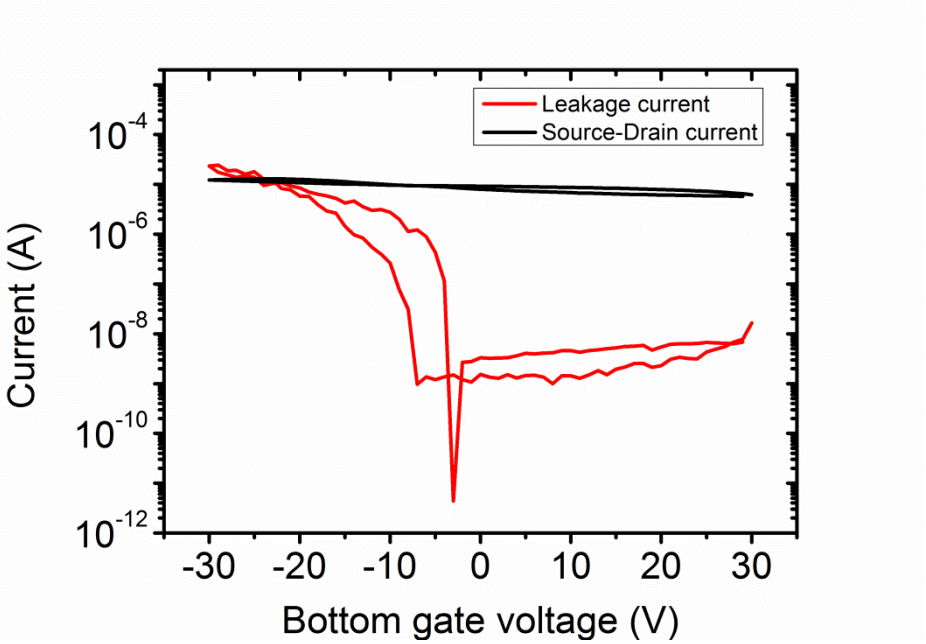

Fig. 6.5 *Typical transfer obtained of a broken pentacene transistor operated for a long time in the presence of water*

The next step was to operate the device in liquid by applying a potential only to the top gate while the bottom gate is grounded . The top gate is made up of a platinum wire which is immersed in the electrolyte. The electrolyte used was bi-distilled water or saline solution (0.1M NaCl). The potential applied to the top gate ranges from +0.4V to -0.4V in order to avoid electrochemical reactions. The drain potential was kept at -0.1V. The obtained transfer characteristic curve is shown in fig. 6.6.

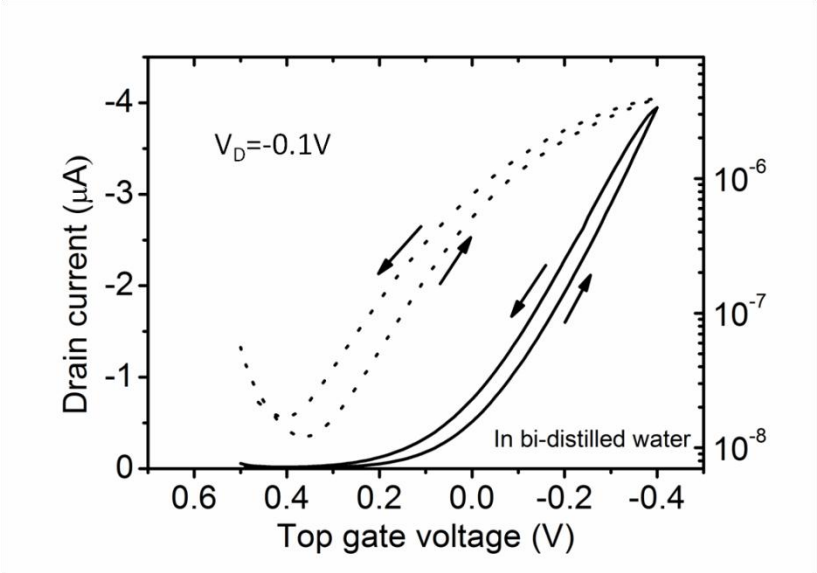

Fig. 6.6 *Transfer characteristics of pentacene based OFET gated by bi-distilled water*

Due to the large capacitive coupling in EGOFETs we observe a much larger transconductance. At the same time we observe an anti-clockwise hysteresis which indicates the absences of bias stress when the top gate is used. We also recorded an output characteristic curve for these transistors by sweeping V_D from 0V to -0.5V and varying V_G from 0V to -0.5V in steps of -0.1V. The obtained output characteristic curve is shown below where one can clearly see that it is a typical output curve of an OFET which has the two regimes viz. linear and saturation regime. This indicates that even when the transistors are operated in the EGOFET configuration, one can obtained a saturation regime operation.

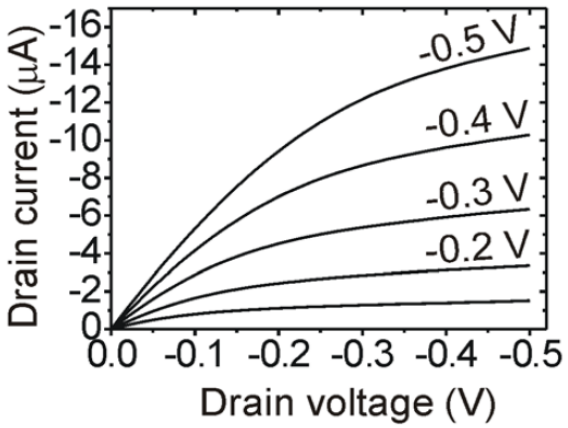

Fig. 6.7 *Output characteristics of the electrolyte gated field effect transistor.*[22]

Having obtained working transistors in the presence of an electrolyte both gated with the conventional bottom gate as well as the top gate, the next step was to combine the measurements with a voltage applied to both the gates in the dual measurement setup. The dual gate measurements were carried out by sweeping the bottom gate potential from +40V to -40V while keeping the potential applied to the top gate fixed. This measurement was performed for different top gate potential *i.e* 0.0V, -0.1V, -0.2V, -0.3V and -0.4V. The resulting transfer is shown in fig.6.8 for both bi-distilled water and saline solution as the electrolyte.

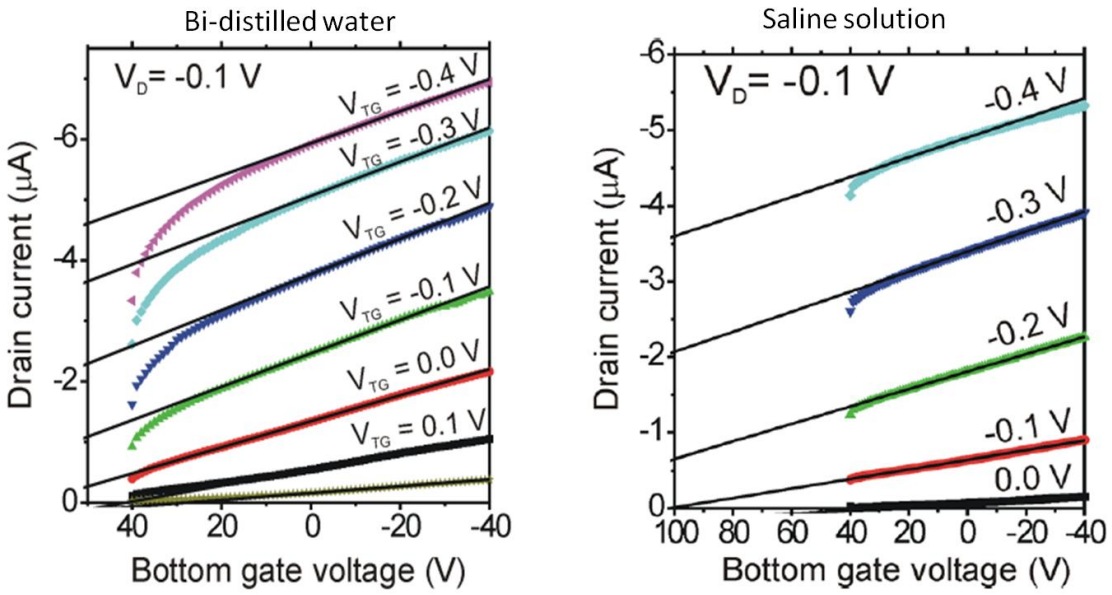

Fig. 6.8 *Dual gate measurements involving the conventional gate and the electrolyte top gate to extract the electric double layer capacitance. In both cases the VD =-0.1V while the bottom gate voltage sweeps from +40V to -40V. The curves with different colours correspond to the various transfer obtained while varying the potential of the electrolyte top gate. The line represents the linear extrapolation for extracting the mobility threshold voltage. In the left the electrolyte used is the bi-distilled water and in the right the electrolyte used is saline solution*[22]

If the electrolyte potential is negative, the charge accumulation in the semiconductor can be controlled by the potential applied to the bottom gate. As seen in the figure above the transistor shows an initial charging phase and then follows a linear dependence vs the bottom gate voltage. The measurement can be interpreted using a simple model for dual gated transistors.

$$I = \frac{W}{L}\mu(C_{DL}V_{TG} + C_{ox}V_{BG} + \sigma_i)V_D$$

$$= \frac{W}{L}\mu C_{ox}(V_{BG} - V_{th})V_D \quad (6.1)$$

where W and L are the width and length of the channel of the transistor. μ is the mobility of the charge carriers, C_{ox} is the capactance of the silicon oxide and C_{DL} is the capacitance of the electric double layer at the electrolyte-semiconductor interface. V_D, V_{TG} and V_{BG} are the voltages applied to the drain, top gate and bottom gate respectively. σ_i is the density of intrinsic charge carriers. Vth is the potential when the bottom gate potential when we have no current i.e $I = 0$ at $V_{BG}=V_{TH.}$

Therefore equation (6.1) becomes

$$V_{th} = -\frac{(C_{DL}V_{TG} + \sigma_i)}{C_{ox}} \quad (6.2)$$

Using equation (6.1) to fit the curves as depicted in fig 6.8 , I could extrapolate V_{th} as a function of V_{TG}. The extracted values of V_{th} vs V_{TG} is shown in fig. 6.9.

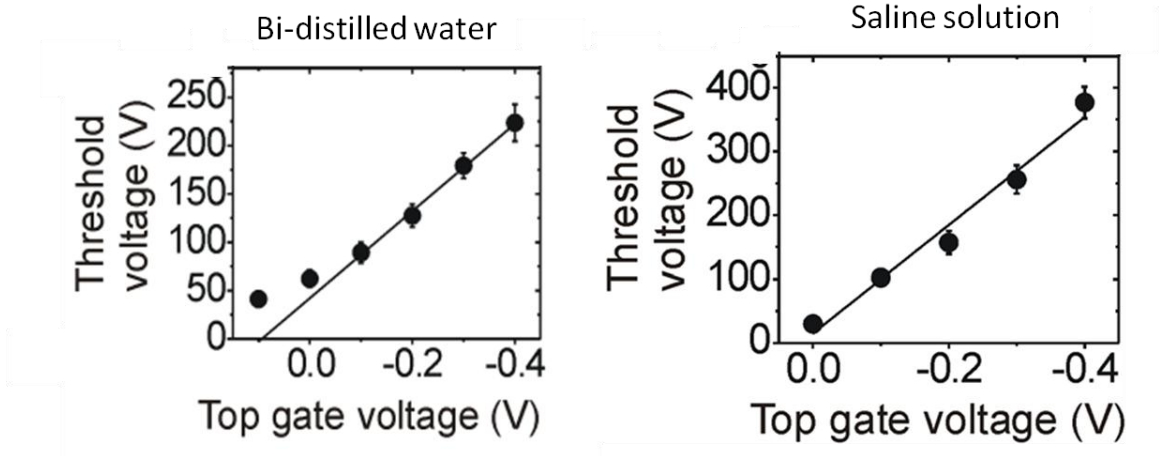

Fig. 6.9 *Threshold voltage obtained from the fit of the transfer scan depicted in fig. 6.6 as a function of top gate voltage* [22]

As can be seen from the above trend, V_{th} vs V_{TG} shows a linear behavior. This is in agreement with equation (6.2). Having known the capacitance of silicon oxide, a linear fit of the curve will give us the value of the capacitance of the electric double layer C_{DL}. The value of C_{DL} however depends on the ionic strength of the solution. For pure bi-

distilled water, I obtained a value of C_{DL}=7.8±0.8μF/cm^2. While in the case of saline solution (0.1M NaCl), I obtain a value of C_{DL}=14.6±2.0μF/cm^2.

Another relevant transport parameter that can be extracted from the slope of the transfer curves shown in fig 6.10 is the mobility of the charge carriers vs the top gate voltage.

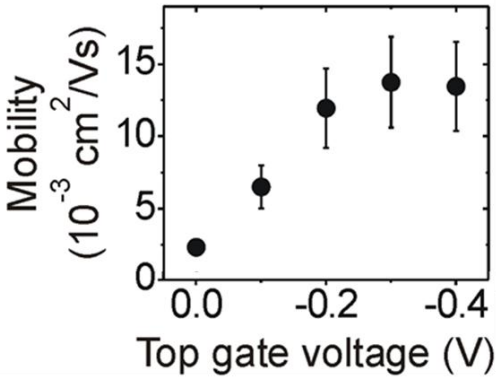

Fig. 6.10 *Mobility of charges as extracted from Fig. 6.6* [22]

The mobility increases with increase in V_{TG} and then begins to reach a saturation when V_{TG} is greater than 0.2V. The increase of mobility with charge carrier density is typical for OFETs because at lower charge density due to the presence of some trap states which reduces the mobility of the charge carriers. The mobility is comparable to that of other organic semiconductors gated with an electrolyte.

Another experiment performed on these devices is time dependent measurements. This enables us to investigate the switching time of our device. For this measurement, I apply a a potential to the top gate from -0.1V to -0.3V while the drain potential was kept constant at 0.02V. Figure 6.11 below shows how the drain current changes during the switching of the potential.

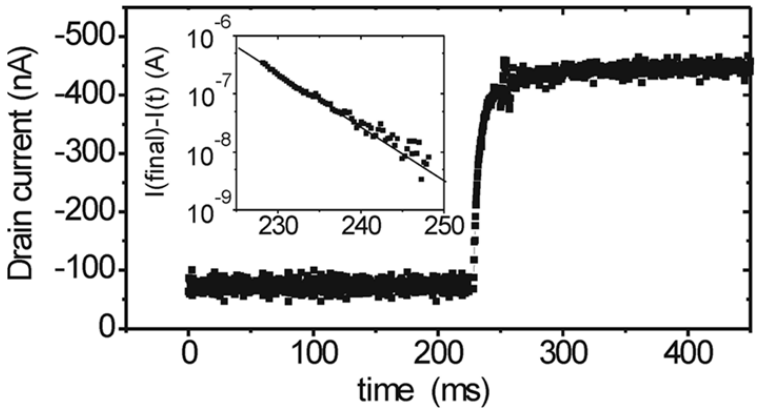

Fig. 6.11 *Determination of the switching time of the water gated organic field effect transistor: Drain current transient during a change in water gate voltage from -0.1 to -0.3V at a drain voltage of -0.02 V. The inset demonstrates the quality of the exponential fit with τ=4.6ms to the transient in the relevant time frame on a logarithmic scale.*[22]

After the switch the current stabilizes after few milliseconds following a fast exponential behaviour ID~-exp(-t/τ) with a characteristic time constant of 4.6ms. The fast dynamics strongly indicates that the ions do not diffuse into the semiconductor but forms a Debye helmoltz layer at the electrolyte semiconductor interface.

6.5 Discussion

I start by discussing the role of water in device stability. As reported in Fig. 6.4 and 6.6, the device shows a different hysteresis when gated by the conventional gate with respect to the electrolyte top gate configuration. A large clockwise hysteresis hinting bias stress effect is observed when the device is operated by the conventional gate while the effect is the opposite when operated by top gate. The explanation for former phenomena is based on the reversible redox reaction between hole charges in the pentacene layer and the water molecules in the electrolyte leading to the formation of protons and oxygen molecules.

$$2P^{+} + H_2O \leftrightarrow 2P + 2H^{+} + 1/2O_2$$

On biasing the gate, the protons are moved out of equilibrium as the electric field due to the gate attracts them to the dielectric . Therefore the charge density in the semiconductor is replaced by the protons being trapped at the interface between the gate and the semiconductor. Nevertheless, the same electrochemical reaction is also expected in EGOFET devices, but the difference here is that the protons do not replace the charge carriers as the electrolyte gate field does not allow the migration of the protons to the

dielectric. Instead the protons migrate in the electrolyte and this can be observed from the measure leakage current (<5nA). While in the case of saline solution (NaCl solution), sodium and chloride ions present in the electrolyte do not contribute to high leakage current The reduction and oxidation at the electrode or semiconductor interface can be excluded due to their high redox potentials. The chloride anions are expected to be a part of the negatively charged Debye-Helmoltz layer.

Morphological investigation on pentacene thin film was carried out by AFM imaging. Even after immersion in water, the pentacene film shows no degradation effects and this is in agreement with earlier reports.[23] Moreover, EGOFET devices could be stored for several hours in aqueous solution and they showed stable electrical performances.

For using EGOFETs as potentiometric sensors with application for extracellular recording of neurons , the sensitivity of the device is crucial. For operation in linear regime the detection limit for potential changes in the electrolyte is given by $\Delta V_{\lim} = s_{noise}/(C_{EDL}\mu V_D W/L)$. From the transfer characteristic fig. 6.4, I obtained a detection limit as low as $V_{\lim} = 50\mu V$ with a noise level of $s_{noise} \approx 1nA$. The high sensitivity originates from the high capacitance of the electric double layer. The sensitivity depends on two main factors (i) capacitance and (ii) mobility of the charge carriers. Since the capacitance that I obtained already reached the theoretical limit, there is room for improvement only in the mobility. Mobility of charge carriers is strongly dependent on film morphology and thickness.[24] Pentacene grows initially in a 2D layer by layer growth mode and then changes its growth mode to 3D following a roughening transition. Since in the EGOFET configuration, the pentacene layers in contact with the dielectric (which is electrolyte) is the upper layers, this means that the charge transport takes place in a rough interface due to the defective, poorly connected layers. If the thickness of the pentacene is thicker, the roughening increases and this hinders the mobility of the charge carriers and impacts on the reduction of device sensitivity.

6.6 Conclusion

In this work I have explained the cause of device instabilities in the presence of water when gated by the conventional bottom gate. I have demonstrated how the dual gate measurement allows the direct measurement of the EDL capacitance. The capacitance of the EDL depends on the ionic strength of the electrolyte. The capacitance measured for devices gated with bi-distilled water is C_{DL} = 7.8±0.8μF/cm^2 while when the electrolyte is saline solution, the capacitance is C_{DL}= 14.6±2.0μF/cm^2. Our experimental approach not only allows us to measure the capacitance of the EDL but at the same time allows us to measure the charge carrier mobility in the same device. The high capacitance allows the pentacene EGOFETs to work as potentiometric sensors (a few tens μV) with a response time of a few milliseconds. No bias stress effect is seen in EGOFET devices as protons do not migrate at the dielectric. The described properties of EGOFETs makes them promising candidates for biosensing applications like non-invasive recording or neuronal electrical activity.

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Chapter 7 Charge transport in Nanoparticle Organic Memory Field Effect Transistors (NOMFETs)

7.1 Introduction

There is a growing interest in neuro-inspired devices based on new technologies beyond the existing silicon CMOS implementation for artificial networks.[1], [2] Recently, a new device called NOMFET (Nanoparticle Organic Memory Field Effect Transistor) was designed to mimic the feature of the human synapse known as 'synapse plasticity'. In the nervous system, a synapse is a junction between two neurons, enabling the transmission of electric messages from one neuron to another and the adaptation of the message as a function of the nature of the incoming signal (plasticity) .The working principle of NOMFETs, is based on the charge trapping/detrapping in an array of gold nanoparticles (NPs) at the SiO_2/pentacene interface. NOMFETs have been initially designed for neuro-inspired computing architectures (artificial neural networks). This device which is memristor-like [3] mimics short-term plasticity (STP)[4] and temporal correlation plasticity (STDP, spike-timing dependent plasticity)[3] of biological spiking synapses, two "functions" at the basis of learning processes. The behavior of the device is obtained by virtue of the combination of two properties of the NOMFET: the transconductance gain of the transistor and the memory effect due to charges stored in the NPs. The NPs are used as nanoscale capacitors to store the electrical charges and they are embedded into an organic semiconductor . Currently NOMFETS are limited to operation at high potentials (> 10 V) and at slow operation frequencies (< 50 Hz). Goal of the research activity was to achieve an understanding of the transport limitations in NOMFET by a series of *in situ* experiments. Understanding charge transport at the interface between the NPs and the semiconductor would ultimately allow to optimize materials properties and to reach performances with potentials and frequencies in the range of the biological synapse (V~ 100 mV; f~ 3 kHz). In *in-situ* experiments I have studied the response of the device during the growth of the organic semiconductor thin film. I analyzed the relationship between the organic film morphology and the transport properties by measuring the current-voltage characteristic curves, *in-situ* and in real time, during the growth of the pentacene over the NP network. Temperature-dependent measurements of the charge carrier mobility allow us to assess the effect of NPs on charge transport properties.

7.3 Experimental section

7.3.1 Sample preparation

The NOMFETs were processed using a bottom-gate bottom contact configuration. The substrates used are the standard test patterns made up of highly doped n-type Si wafer with 200 nm thick layer of thermally grown silicon oxide as a dielectric. Interdigitated gold electrodes were photolithographically patterned in order to define the source and drain contacts. It consisted of four transistors with two different geometries W=11200, 22400 and L=20, 40 respectively. The test patterns were cleaned using the standard cleaning procedure described in Section 2.1.

7.3.2 Au NPs synthesis

Colloidal solutions of citrate-capped Au NP (10 ± 3 nm in diameter) were synthesize as follows.[5] Charge stabilized Au nanoparticles were synthesized by the reduction of chloroauric acid in water. To obtain a 100 mL aqueous solution of Au nanoparticles, a solution with 1 mL of HAuCl44H_2O (1% w/v) in 79 mL of H_2O was first prepared. A 20 mL reducing solution with 4 mL of trisodium citrate (1% w/v) and 80 μL of tannic acid (1% w/v) in 16 mL of H_2O was then added rapidly to the Au solution (all solutions at 60 °C). The mixed solution was boiled for 10 min before being cooled down to room temperature. A continuous stirring was applied throughout the process. The resulting reddish solution contained typically 10nm Au. The NP size (10 ± 3 nm in diameter) and density is calculated from SEM images of NPs arrays on the surface.

7.3.3 SiO_2 surface functionalization and NP deposition

Immediately after cleaning the TPs, the SiO_2 gate dielectric was functionalized by a SAM to anchor gold nanoparticles (NPs) on the surface.[6] The SiO_2 surface was functionalized by immersion in a solution of (3-aminopropyl)-trimethoxysilane (APTMS) molecules diluted in methanol at a concentration 1μL/mL for 1h.[7]. Excess, non-reacted, molecules were removed by rinsing in methanol under sonication. This sample was subsequently dried under nitrogen stream. Static water contact angle was 19°, a common value for hydrophilic NH2-terminated surfaces.[7] This sample was then immediately dipped in a colloidal solution of citrate-stabilized Au-NP for 24h. This procedure yields an array of NPs with a density of about 4-5x10^{10} NP/cm^2. The sample was then cleaned with de-

ionized water and isopropanol, and dried under a stream of dry nitrogen. The NPs deposited on SiO_2 do not form a continuous film or large clusters, rather they are adsorbed as individual entities. They do not coalesce, and they exhibit a characteristic length scales, i.e. a density, that we can adjust with the concentration of the Au NPs in the solution and the time of deposition.[4] Indeed, we have previously demonstrated that an optimized density of NPs for the NOMFETs is around $5x10^{10}$ NP/cm^2.[4]

7.3.4 OTS functionalization

Octadecyltricholorosilane (OTS) molecules were deposited using the reported protocol.[8][9]The silanization reaction was carried out in a glovebox under nitrogen atmosphere but non-anhydrous solvents were used to favor hydrolysis of -SiCl3 functions. The freshly cleaned substrate was immersed for 2h in a 10^{-3} M solution of OTS in a mixture of n-hexane and dichloromethane (70:30 v/v). The device was rinsed thoroughly by sonication in dichloromethane (2 times) then blown with dry nitrogen.

7.3.5 *In situ* real time experiments

Electrical characterization was carried out *in situ* real time during the growth of pentacene over the dielectric functionalized with the NPs. Pentacene was evaporated at a rate of 0.5ML/min(1 ML of pentacene ≈1.5 nm) .The substrate was kept at room temperature. Prior to the evaporation of pentacene, electrical connection was done on the samples before they were transferred in a home-built vacuum evaporation chamber[10], Characteristic transfer curves (I_D-V_G) were recorded in real time by sweeping V_G= 30V to -30V both in linear (V_D=-1V) and saturation regime (V_D=-30V) . When the final pentacene thickness reached about 20 MLs, deposition was stopped and temperature dependent measurements were carried out by recording I_D-V_G scans every 30 s while the temperature was varied from -160°C to RT. Hole mobility in linear and saturation regimes was extracted as usual from standard transistor equations. In total three transistors were measured simultaneously. Two keithley 2612 were used as the source measuring unit.

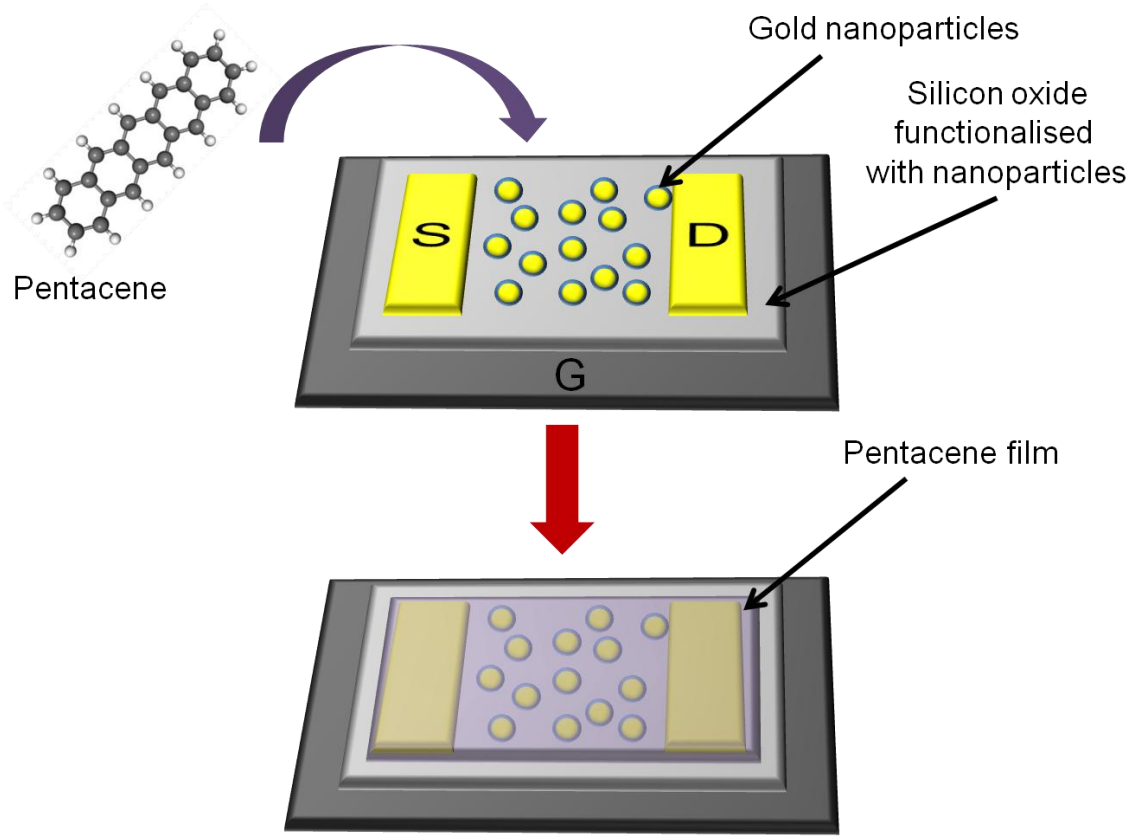

Fig. 7.1 *Schematic diagram depicting the device configuration. Top view shows a substrate which is functionalized with gold nanoparticles onto which pentacene is deposited and bottom view shows the gold nanoparticles embedded in the pentacene film. S,D,G refers to the source, drain and gate electrodes respectively.*

7.3 Results and discussion

As a reference sample, I first performed the *in situ* real-time experiment on pentacene growth on a dielectric surface functionalized by APTMS but without NPs. In pentacene transistors grown on a smooth dielectric interface, percolation is observed before the completion of the first monolayer ($\Theta_{C,2D}$ ~ 0.7 ML) following the theory of 2D percolation.[11], [12] Fig. 7.2 shows the evolution of the saturation mobility of the charge carriers as a function of the nominal pentacene layer thickness Θ (expressed in monolayers ML by taking into account 1ML of pentacene ≈ 1.5nm) during the *in-situ* experiment. While mobility in linear and saturation regimes are slightly different ($\mu_{sat} > \mu_{lin}$ by a factor of about 1.5-2), their evolution with pentacene thickness is the same. Without the NPs (Black triangle markers), the onset of mobility starts at about 0.7 monolayer (ML) of pentacene in agreement with previous work, corresponding to the

onset of the percolation path in 1st pentacene monolayer. The steep increase up to 2ML indicates the formation of the spatially confined channel where field effect induced carriers are generated. Then the slow increase of mobility reaching a plateau of 2-3x10^{-3} cm^2/Vs at about 15 ML depicts a 2D-3D growth transition.[12], [13]

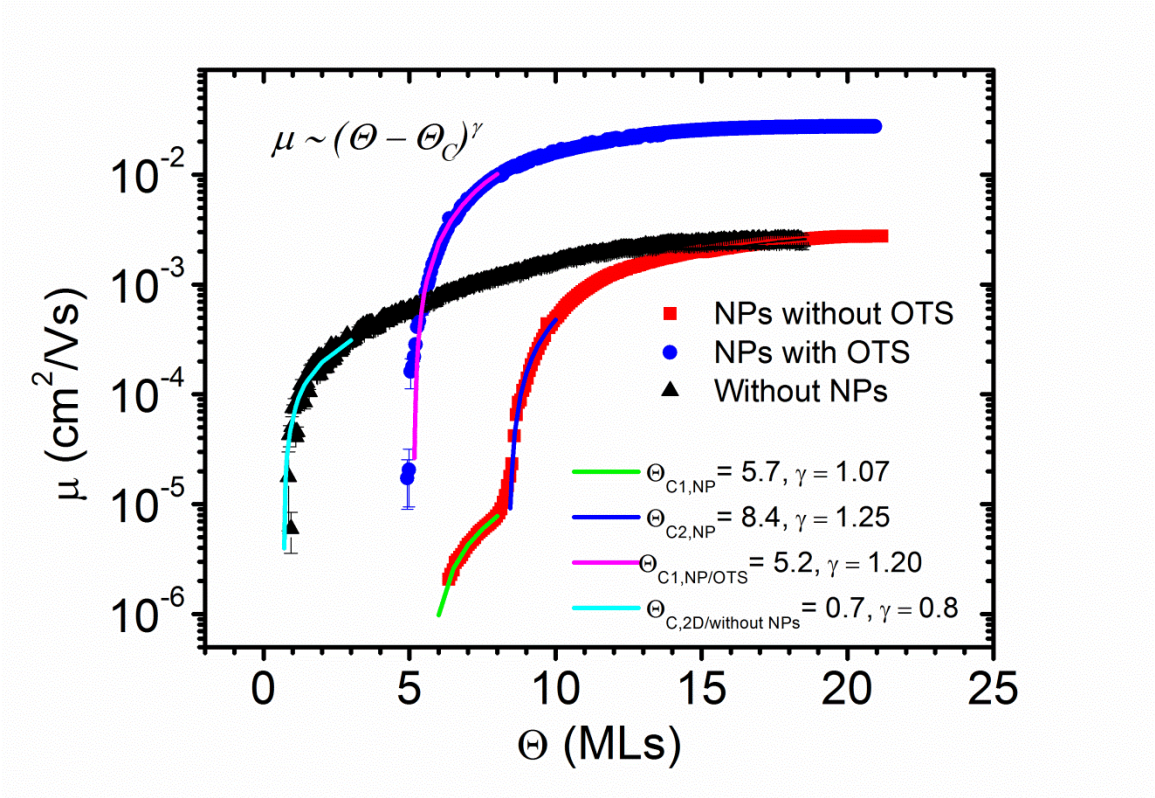

Fig. 7.2 *Mobility μ in saturation of pentacene NOMFETs as a function of nominal layer thickness Θ measured in situ during the deposition of the semiconducting film. The black triangle markers correspond to pentacene growth on substrate functionalized with APTMS but without nanoparticles. Both the blue circle markers and reds square markers were obtained on substrates functionalized with APTMS and 10 nm gold nanoparticles. The blue circle markers were measured using a substrate that had been made hydrophobic by a final OTS functionalization. The blue, green and pink and light blue lines indicate the power law fit to obtain the percolation threshold.*[14]

For the case of pentacene deposition on the NP functionalized substrates, I observed that below a critical thickness of $\Theta_{C1,NP}$ = 5.7 ML (red square markers, NOMFET without OTS treatment) no transistor current can be measured and the mobility cannot be extracted. At $\Theta_{C1,NP}$ percolation of conducting islands sets in and a first continuous pathway connects source and drain electrode.

The transfer characteristics measured during growth of pentacene allows us to extract the mobility μ as a function of $\Theta \geq \Theta_{C1,NP}$. With increase in pentacene thickness the transistor current and the mobility both increase rapidly over orders of magnitude. The increase does not follow a single power law but contains an inflection point at $\Theta_{C2,NP}$ = 8.4 ML beyond which a second phase of steep increase in mobility is observed. Both regions are fitted by a power law $\mu \sim(\Theta - \Theta_C)^{\gamma}$, with the critical coverage Θ_C indicating the creation of a percolation path between the electrodes, and the critical exponent γ related to the lattice geometry and dimensionality of the underlying conducting network. From the fit I found an increase in exponent from 1.1 in the first phase to 1.25 in the second phase of mobility increase, demonstrating a change in growth mode at Θ = 8.4 ML (*i.e.* about 12 nm) caused by the presence of NPs (diameter of about 10 nm). Finally, saturation of the curve is slowly attained at $\Theta \approx 20$ ML of deposited pentacene to yield a saturated charge mobility of $\mu = 3x10^{-3}$ cm^2/Vs. This mobility value is in agreement with the one I previously measured on NOMFET.[4] The observed evolution of the mobility with Θ clearly results from the more disordered organization of the semiconducting film grown on the NPs. Further complexity in the formation of additional transport paths leads to the formation of the inflection point. Only when the nominal thickness exceeds 8 ML a second critical regime emerges where an additional steep increase of mobility is observed. This second threshold happens at a thickness which exceeds the diameter of the citrate capped NPs (about 10 nm). This finding indicates that efficient transport paths are formed when the NPs start to get covered by the pentacene layer. Therefore, I infer that a more disordered pentacene film is obtained with NPs, as revealed by AFM images with smaller pentacene grain size for the NOMFET compare to pentacene transistor without NPs (Fig 7.3) .

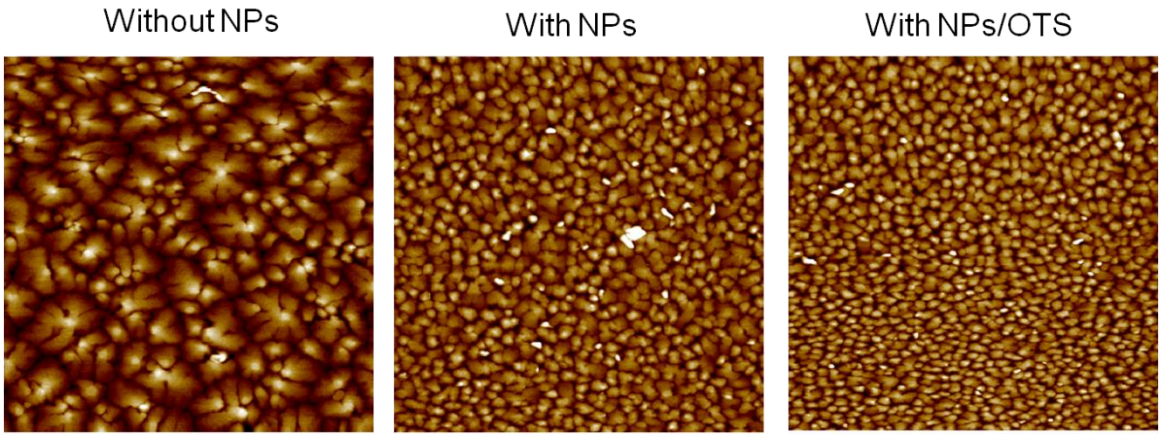

Fig. 7.3 *AFM images showing pentacene film grown on SiO_2 (a) without gold nanoparticles (b) with gold nanoparticles and (c) gold nanoparticles functionlized with OTS. The size of all images is 5 x 5µm^2.*

In order to have a deeper insight into the transport phenomena, temperature dependent characterization of the transistor was carried out *in situ* after the deposition of pentacene. Figure 7.4 shows the Arrhenius plot of mobility in saturation measured, *in situ*, at the end of the pentacene growth, *i.e.* for a film thickness of about 20 ML (30 nm). The Arrhenius plot shows strongly temperature activated behavior. The presence of NPs leads to an increase of the activation energy to E_A = 125 meV (red square markers) in contrast to E_A = 65 meV in pure pentacene films (black square markers). This latter value is in agreement with previous reports for pentacene OFET (in the range 20-80 meV). The increase in the activation energy due to the presence of NPs is attributed to the availability of trap states at the HOMO-LUMO gap, near the HOMO.[15]–[17] Extrapolation to infinite temperature yields a trap-free mobility of μ_0 = 0.26 cm^2/Vs.[15], [18], [19]

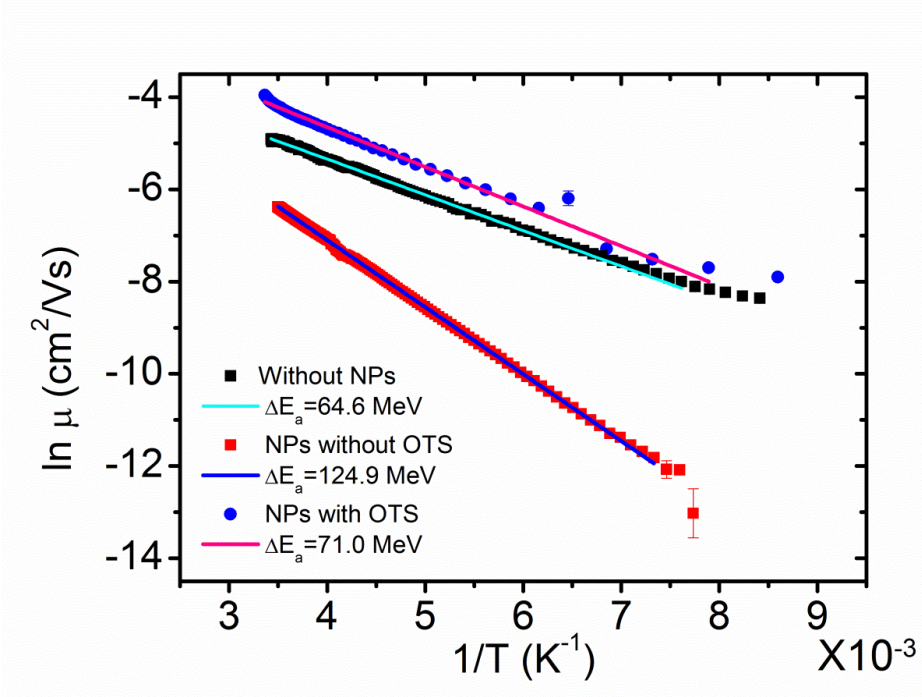

Fig. 7.4 *Arrhenius plot of temperature dependence of mobility in saturation* μ_{sat} *for pentacene NOMFETs grown on substrates without NPs (black markers) APTMS/NP (red) or APTMS/NP/OTS surface (blue). All the curves show a temperature activated behavior and follow the Arrhenius behavior. From the slope I determine activation energies as indicated in the plot.*[14]

Our findings point to two possible reasons for the weak performance of the NOMFET grown on citrate capped NPs. First, the pentacene morphology is disordered due to the presence of NPs, and only transport paths spanning at a distance from the dielectric interface can evolve. The electronic coupling and charge mobility are reduced along such a path. The extrapolated trap free mobility is an order of magnitude lower than typical values found in unperturbed pentacene transistors [20].

Second, deep trap states further reduce mobility and lead to activated transport behavior with higher energy barrier. In the NOMFETs, once a sufficiently thick pentacene film is deposited (above about 10 ML, Fig. 7.2), each nanoparticle is surrounded by pentacene, thus each NP acts as a "shallow trap" for charge carriers moving across the pentacene thin film, explaining the increased activation energy E_A with the NPs. Since low charge carrier mobility in NOMFET is the main cause of the slow dynamics of its synaptic behavior,[4] I modify the fabrication protocol adding a silanization treatment after the NPs deposition. The findings from the *in situ* experiment prompted this strategy. Reduced mobility was already observed in the APTMS modified dielectric without the presence of NPs.[21]

Therefore, both the surface chemistry that exposes the highly polarizable groups and the morphological changes of the semiconductor as induced by the presence of NPs (given that a sufficiently thick pentacene layer is deposited), contribute to the decrease of charge transfer velocity. Surface functionalization by molecules such as octadecyltrichlorosilane (OTS) is known to improve mobility in OFET as they bind to polar groups at the surface and form an oriented monolayer which exposes non-polar alkyl chains, thereby decreasing the surface energy.[22]–[24] I treated the NPs/APTMS substrates in a solution of OTS (see section 7.3.4) according to an established protocol.[8], [25], [26]Chlorosilane head groups of the OTS molecules are prone to react with both the terminal amine group of APTMS and the -OH and COO- groups of citrate capping the NPs.[27], [28] Moreover, OTS can polymerized laterally, though siloxane bonds, forming a capping layer over the surface and NPs. Evidence of the correct grafting of OTS is the observation of an increase of the water contact angle from ~30-40° for APTMS/NPs surface to ~90-100° after silanization. This latter value is consistent with 100-110° reported for OTS monolayer on a smooth surface (SiO_2), (I observe contact angles of 106-109° for APTMS/OTS bilayer on flat SiO_2). Now I compare the above results with *in situ* experiments performed after passivation of the NP surface with OTS. The increase of mobility as a function of Θ, as shown in Fig. 7.2 (blue circle markers), clearly confirms the improved performance. Percolation sets in earlier at $\Theta_{C1,NP/OTS}$ = 5.2 ML, but remains still beyond the sub-monolayer regime. Here the percolation process follows a simpler pattern that is described by a single power-law in the initial critical regime. The final increase in mobility saturates slowly and only at Θ = 18 ML a stable value of $\mu = 3 \times 10^{-2}$ cm^2/Vs is obtained which exceeds by more than an order of magnitude the non-OTS passivated device. Temperature dependent measurements demonstrate also for the OTS passivated NOMFET a thermally activated transport, but the activation barrier is clearly reduced to E_A = 71 meV, close to the one for pentacene transistor (Fig. 7.4). Extrapolation to infinite temperature results in μ_0 = 0.25 cm^2/Vs, as for the non-OTS passivated device. The comparison of the two types of NOMFETs provides a clear interpretation of the improvements in electrical performances. Most important, I achieved a smoothening of the trap states that limited transport in the non-OTS passivated device. The exposure of the polar citric acid groups at the NP surface leads to strong electrostatic interactions with carriers and consequently trapping. OTS reacts directly with these groups [28] making the NP surface hydrophobic by exposing the alkyl chain. As a consequence the mobility rises by more than one order of magnitude when operated at

room temperature. However, both kind of surfaces demonstrate critical limitations of transport when compared to transistors grown on smooth dielectric surfaces: the NPs perturb the morphology in the first monolayers and give rise to a hindered transport path with reduced electronic coupling. This finding is independent of the NP functionalization and in both investigated cases I find maximum "trap-free" mobilities $\mu_0 = 0.25$ cm^2/Vs by extrapolation.

7.4 Conclusion

In conclusion, I have successfully studied the charge transport processes taking place at the interface between NPs and pentacene in NOMFET devices. The morphology of pentacene grown on a network of NPs reveals that it forms smaller grain sizes as compared to the one grown on a SiO_2 without NPs. This disorder in the morphology of pentacene when grown on the NPs causes a delay in the percolation of the semiconductor to form a conductive path for the current to flow. The presence of NPs has shown to cause deep trap states reducing the mobility of the charge carriers and leads to activated transport behavior with higher energy barrier. However, when NPs is passivated with OTS the mobility of the charges is higher and the activation energy decreases. The improvements of the semiconducting behavior led ultimately to faster dynamics of the NOMFET device[14] .

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Final Conclusions

In this thesis I have explored the impact of interfaces and interface modifications on charge transport in Organic Field Effect Transistors. The first interface that I have investigated is the dielectric-semiconductor interface which is central for charge transport in OFETs. By utilizing the *in situ* real-time electrical characterization of an OFET during the growth of the semiconductor, I have demonstrated how defects residing at the dielectric/semiconductor interface can hinder transport of charge carriers. The comparative study of the electrical properties of pentacene transistors fabricated on untreated SiO_2 versus a SAM modified SiO_2 leads to two main results (i) Modifying the dielectric by capping the polar groups present in the SiO_2 improves the performance of the transistor. In particular, from the transfer characteristics obtained *in situ*, it has been observed that for pentacene OFETs fabricated on HMDS-SiO_2, the first two monolayers show disorder free transport. (ii) By fitting the temperature dependent measurement results with a Vissenberg and Matters model the dimensionality of the charge transport phenomena has been determined. Having a transport model in hand, transfer curves recorded in real time were then fitted in order to extract the value of the width of band broadening as a function of film thickness. This result is the first of its kind to demonstrate band broadening from sub-monolayer regime to multilayer regime. As the potential application of OFETs in large area flexible electronics, rely on the electrical performance of the devices, a fine tuning of this interface can impact largely on their optimization.

The second activity on the study of charge transport properties of sub-monolayer transistors is also related to the dielectric-semiconductor interface, however here the aim was to quantify the charge density as a function of film coverage. In a system where charge transport is laterally confined within nanometer-sized islands forming a percolation network, the geometry of the network not only determines the percolation phenomena but it also defines the density of charge carriers created by field effect. The capacitance measured from the displacement current measurement allows the extraction of mobility and threshold voltage of sub-monolayer transistors.

By investigating charge transport at the interface of a donor/acceptor layer (pentacene/C_{60}) I have elucidated the interplay between interface morphology and interfacial charge transport taking place at the heterojunction. From the electrical

characteristics acquired in real time during the formation of the bilayer, I have shown that at early stages of C_{60} growth, hole current in pentacene increases and electron current flows through C_{60} grains decorating the terrace edges of pentacene. At later stages, transition from stick- to surface-percolation in 2D yields a five-decade increase of electron current. Maximum charge mobility for electrons (μ_e=1.4±0.3cm^2/(Vs)) and holes (μ_h=0.14±0.05 cm^2/(Vs)) are observed as C_{60} is grown on two-monolayer pentacene film. The fraction of charges that are transferred from pentacene to C_{60} at the heterojunction is manifested by the shift in the threshold voltage of pentacene upon C_{60} deposition. Specifically I have demonstrated that amount of charges transferred at the heterojunction is modulated by film thickness and morphology. This result is relevant especially for opto-electronic devices as one of the key ingredient for efficient charge transfer is the understanding of how interface morphology plays a role in the interfacial interactions.

With the aim to study the electrolyte-semiconductor interface, I have established an experimental protocol which permits the extraction of the capacitance of the double layer formed at the interface between an electrolyte and the semiconductor (pentacene). The value of the capacitance extracted for pure water as an electrolyte is C_{DL}=7.8±0.8 µF/cm^2 while in the case of saline solution as an electrolyte, the capacitance measured C_{DL}=14.6±2.0 µF/cm^2.The high capacitance allows the pentacene EGOFETs to work as sensible potentiometric sensors with a response time in the range of a few milliseconds. Moreover I have demonstrated that in contrast to devices operated with a conventional silicon/silicon oxide gate, the EGOFETs electrical properties are stable. Bias stress is absent as proton migration and trapping at the gate dielectric do not happen. The described properties render the pentacene EGOFETs promising candidates for bio-sensing applications. In addition, these findings can be exploited for most applications of organic electronics in the field of bioelectronics.

Finally, charge transport process was investigated in Nanoparticles Organic Memory Field Effect Transistor (NOMFET) devices. From a series of *in situ* real time experiments, where electrical characterization was carried out during the growth of the pentacene over a network of gold nanoparticles (NPs), I have illustrated a relationship between the organic film morphology and the transport properties of these devices. A comparison between the electrical characteristics of a traditional OFET versus NOMFET shows that the presence of the NPs causes a disorder in the morphology of pentacene

leading to the formation of smaller grains pentacene islands. Moreover citrated capped NPs acts as traps for the transport of carriers. However, by functionalizing the NPs with a self assembled monolayer OTS (octadecyltrichlorosilane), the transport properties of the device is improved. Since NOMFET was designed to mimic the human synapse, the understanding of the charge transport at the interface between the NPs and the semiconductor would allow the optimization of the materials properties in order to reach performances with potentials and frequencies in the range of the biological synapse (V~ 100 mV; f~ 3 kHz).

APPENDIX A

To derive closed-form equations we consider a two-dimensional structure as shown in Fig. 4.4c of Chapter 4. The island size in the two dimensional model is described by the geometric parameters *b* and *a* whereas the thickness of the dielectric enters with parameter *d*. The experimental coverage enters into the model via $a = b\Theta$. Within this periodic structure the conformal mapping technique is applied to a 2-corner structure (highlighted in green) to keep mathematics manageable.

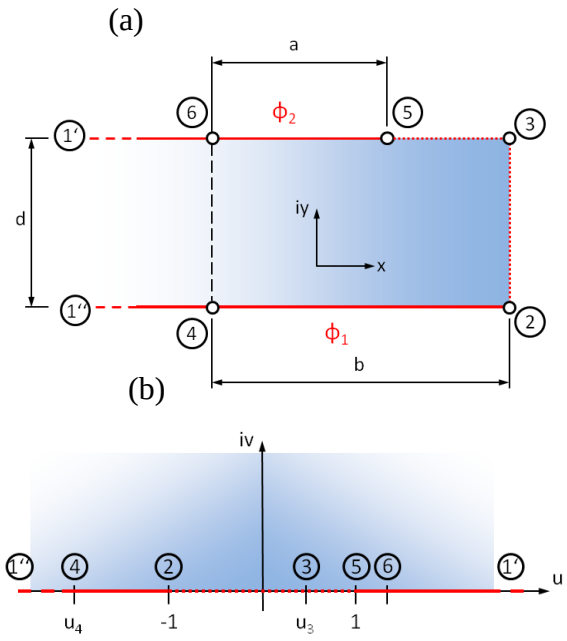

Fig. A1: *Conformal mapping technique applied to sub-monolayer pentacene film: The 2-corner structure in complex plane z wherein Laplace equation is analytically solved is shown in (a). The area of interest is mapped upon the upper half in plane w (b).*

Figure A1 shows this structure in complex plane z. The gate electrode is defined between points 2 and 4, the pentacene island between points 5 and 6. At the symmetry line within the gap (line between points 2 and 3) Neumann boundary is applied. Along the symmetry line in the centre of the pentacene island, the line connecting points 4 and 6, a Neumann boundary is approximated by extending both top and bottom electrode infinitely to point 1. This approximation holds if the influence of the fringing fields from the corner of the pentacene island upon the line between points 5 and 6 can be neglected, resulting in a nearly homogeneous field in this area. In the model structure that is the case for a

thickness d of the oxide which is less than the length of the pentacene islands. The 2-corner structure is mapped upon the upper half of a complex plane w (Fig. 6b). Following Schwarz-Christoffel transformation[33] the derivative of the mapping function is given by:

$$\frac{dz}{dw} = -\frac{d}{\pi}\frac{1}{\sqrt{u+1}\sqrt{u-u_3}}$$

Its integration yields:[34]

$$z = f(w) = -\frac{2d}{\pi}\log\left(\sqrt{w+1} + \sqrt{w-u_3}\right) + D$$

where the integration constant D defines the origin in z plane.

In w plane the boundary of the mapped region lies along the real axis. Points 2 and 5 are mapped upon w = -1 and w = +1, respectively. Parameter u_3 can be derived by equating the distance between points 3 and 5 in z plane to the difference b-a and results in:

$$u_3 = \frac{2}{\cosh^2\left(\frac{\pi(a-b)}{2d}\right)} - 1.$$

Applying a potential Φ_1 between points 1´´ and 2 and a potential Φ_2 between points 5 and 1´ the complex potential solution in the w plane reads:[4]

$$P(w) = \Phi(w) + i\Xi(w) = \Phi_2 + i\frac{\Phi_2-\Phi_1}{\pi}\operatorname{arccosh}(w).$$

The integral dielectric flux leaving in plane z the bottom electrode between points 2 and 4 is given by the difference of the imaginary parts of the complex potential at the corresponding points in plane w:

$$\int_{2\to4}\vec{D}\,d\vec{z} = \epsilon_{ox}\left(\Xi(u_4) - \Xi(-1)\right) = \epsilon_{ox}\frac{\Phi_2-\Phi_1}{\pi}\left(\operatorname{arccosh}(u_4) - \operatorname{arccosh}(-1)\right).$$

By solving the equation f(-1)-f(u_4) = b for u_4 one obtains:

$$u_4 = u_3 - (1+u_3)\cosh^2\left(\frac{\pi b}{2d}\right).$$

Finally the capacitance between gate electrodes and pentacene film of total area A can easily be calculated from

$$C = A\frac{\epsilon_{ox}}{b\,\pi}\left(\operatorname{arccosh}(u_4) - \operatorname{arccosh}(-1)\right) \qquad \text{(A1)}$$

List of Publications

1. S. Desbief, **A. Kyndiah**, D. Guérin, D. Gentili, M. Murgia, S. Lenfant, F. Alibart, T. Cramer, F. Biscarini, and D. Vuillaume, "Low voltage and low time constant organic synapse-transistor" , **2015,** *Organic Electronics* 21, 47-53
2. A.F Basile, T Cramer, **A Kyndiah**, F Biscarini, B Fraboni "Trap densities and transport properties of pentacene metal-oxide-semiconductor transistors. I. Analytical modeling of time-dependent characteristics", **2014**, *Journal of Applied Physics* 115 , 244504
3. A.F Basile, **A Kyndiah**, F Biscarini, B Fraboni ″Trap densities and transport properties of pentacene metal–oxide–semiconductor transistors: II—Numerical modeling of dc characteristics" **2014,** *Journal of Applied Physics* 115, 244505
4. T.Cramer, A.Campana, F.Leonardi, S.Casalini, **A. Kyndiah**, M.Murgia, F.Biscarini **2013,** *Journal of Materials Chemistry B* 1 (31), 3728-3741
5. T.Cramer, **A.Kyndiah**, M.Murgia, F.Leonardi, S.Casalini, F.Biscarini "Double layer capacitance measured by Organic field effect transistors operated in water" **2012** , *Applied Physics Letters* 100 (14), 143302
6. **A.Kyndiah**, T. Cramer, C. Albonetti, F. Liscio, S. Chiodini, M. Murgia, F. Biscarini "Charge transfer and percolation in ambipolar field effect transistors", **2014** *under revision Advanced Electronic Materials*
7. T. Cramer, **A. Kyndiah**, A. Kloes, M. Murgia, B. Fraboni, F. Biscarini "Charge Density Increase in Sub-Monolayer Organic Field-Effect Transistors", **2015** *submitted to Phy. Rev B*
8. T.Cramer, **A.Kyndiah**, M. Murgia, C. Albonetti, B. Fraboni , F. Biscarini "Band Broadening in Organic Thin Film Transistors: From the Submonolayer to the Multilayer Regime" *to be submitted.*

A person who never made a mistake never tried anything new.

"If we knew what it was we were doing, it would not be called research, would it?"

Albert Einstein