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DESIGN AND FABRICATION OF BOND WIRE MICRO-MAGNETICS

Presentata da: ENRICO MACRELLI

Relatori:

Prof. Ing. MARCO TARTAGNI

Prof. Ing. ALDO ROMANI

Coordinatore di dottorato:

Prof. CLAUDIO FIEGNA

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Abstract

This thesis presents a new approach for the design and fabrication of bond wire magnetics for power converter applications by using standard IC gold bonding wires and micro-machined magnetic cores. It shows a systematic design and characterization study for bond wire transformers with toroidal and race-track cores for both PCB and silicon substrates. Measurement results show that the use of ferrite cores increases the secondary self-inductance up to 315 µH with a Q-factor up to 24.5 at 100 kHz. Measurement results on LTCC core report an enhancement of the secondary self-inductance up to 23 µH with a Q-factor up to 10.5 at 1.4 MHz. A resonant DC-DC converter is designed in 0.32 µm BCD6s technology at STMicroelectronics with a depletion nmosfet and a bond wire micro-transformer for EH applications. Measures report that the circuit begins to oscillate from a TEG voltage of 280 mV while starts to convert from an input down to 330 mV to a rectified output of 0.8 V at an input of 400 mV. Bond wire magnetics is a cost-effective approach that enables a flexible design of inductors and transformers with high inductance and high turns ratio. Additionally, it supports the development of magnetics on top of the IC active circuitry for package and wafer level integrations, thus enabling the design of high density power components. This makes possible the evolution of PwrSiP and PwrSoC with reliable highly efficient magnetics.

Cycling around Iceland is strictly for masochists.

— Michiel Erens

Dedicata ad Arrigo Amadori.

Acknowledgements

It is arduous to sum up the life of three years in a brief number of lines. However, the first thanks goes to my advisor, Prof. Marco Tartagni. Thank you Marco for pointing me towards electronics and magnetics science. These meticulous fields of knowledge fascinated me, I hope to go in the right direction. Thank you to Prof. Aldo Romani as well, for all the support during these years and for all aspects of circuit design and microelectronic technologies. Thank you to Prof. Rudi P. Paganelli as well, for the support in the field of power electronics and micro-magnetics.

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Contents

Introduction

Significant efforts are recently devoted in developing high performance magnetic components compatible with Integrated Circuit (IC) processes. Air-core inductors and planar transformers shaped as spirals are implementable in standard IC processes, although it is difficult to achieve good efficiencies and high inductance values. In fact, an overall size reduction of magnetic components for power converters is a strategic issue, as well as the minimization of power losses. The ultimate market drivers are pushing the growth of new miniaturized platforms such as Power Supply in Package (PwrSiP) and Power Supply on Chip (PwrSoC) technologies. In PwrSiP the magnetics are co-packaged with the converter circuitry, while in PwrSoC the magnetics are integrated and, potentially lead to the realization of monolithically integrated power supplies. However, on-chip magnetics usually require complex and expensive deposition techniques which currently limit their market application.

The main goals in the design of power conversion circuits are high efficiency and reduced power losses. In order to develop highly efficient DC-DC converters, active semiconductor devices such as mosfets are used as switches, while passive components are required for temporarily storing energy and for filtering the periodic switching output pattern of DC-DC conversion in order to extract the DC component. Generally, the quality of such passive elements affects power dissipation losses. A modern challenge for the miniaturization of DC-DC converters is the integration of passive components achieving similar performance of discrete passives with a comparable footprint from 0.5 to 10 MHz. Recent progress in increasing the switching frequency in commercial DC-DC converters has enabled the use of smaller passive components. However, such advancements are restricted by structural limitations of magnetic materials related to magnetic saturation and internal power losses. A different approach is to remove completely the magnetics from the converters as in charge pumps which are based on a net of switches and capacitors; however this approach implies a significant energy loss due to the capacitor switches. Although the design of charge pump converters can minimize losses and achieve satisfactory efficiency, their application requires high complexity and it is limited to a small range of voltage conversion ratios. Actually, several power converters use transformers which can store energy as inductors allowing a wide-ranging conversion ratio with high efficiency.

Power inductors and transformers are generally fabricated by wounding a coil around a planar core as in solenoid and toroidal structures, or by enclosing the coils within a multilevel magnetic core as in spirals. The design of such devices must consider the current flowing in the coil which produces a magnetic field, in which the energy is stored. A good micro-inductor should achieve a high inductance with a low series resistance in a small footprint area. In cases where a magnetic core is used, the inductance increases proportionally to the relative permeability of the core. However, this can lead to the saturation of the core for low values of applied magnetic field, and

to high AC core losses.

Various integration techniques are available for reducing the size of power devices. For package level integration the magnetics are co-packaged side by side with the die and connected within the package, whilst for wafer level integration the magnetics are built into the substrate or on top of the die thus decreasing the overall device footprint area. A simple approach to form a power device is the use of IC bonding wires based on solid phase welding to enclose the magnetic core. This kind of devices, called bond wire magnetics, is a promising solution compared to Micro Electro-Mechanical System (MEMS) technology due to the standard process and the low resistivity of bonding wires which enables the realization of efficient power converters. Furthermore, bond wire magnetics with toroidal core facilitate high inductance to DC resistance ratios while reducing the overall footprint area. Beyond this, the performance of bond wire magnetics can be adjusted by varying wire loop height and core thickness, whilst a toroidal geometry produces a negligible external magnetic field over active ICs.

This thesis presents a new approach for realizing bond wire transformers for power converters by using conventional gold bonding wires and micro-machined cores. It shows a systematic design study and a fabrication technique for bond wire transformers with toroidal and race-track cores for both Printed Circuit Board (PCB) and silicon substrates. Furthermore, it demonstrates how this technique is suitable for integration of magnetics built on top of the substrate, thus enabling the design of high density power components. Experimental results report that the use of soft ferrite cores enhance the secondary self-inductance up to 315 µH with a Q-factor up to 24.5 at 100 kHz, which represent the actual state-of-the-art for bond wire toroidal magnetics. On the other hand, experimental results on LTCC core show an increase of the secondary self-inductance up to 23 µH with a Q-factor up to 10.5 at 1.4 MHz. This new methodology is cost-effective and enables a manageable design of inductors and transformers with high inductance and high turns ratio. Finally, a resonant DC-DC converter is designed in 0.32 µm BCD6s technology at STMicroelectronics with a depletion nmosfet and a bond wire micro-transformer. Measures report that the converter starts to oscillate from an input voltage down to 280 mV and begins to convert from an input down to 330 mV to a rectified output of 800 mV at an input of 400 mV. This circuit permits the development of battery-less and low input voltage DC-DC converters for Energy Harvester (EH)s.

This thesis is structured as follows. The first chapter describes a review of actual technology in the field of micro-magnetics and introduces the reader to the state-of-the-art in this area while showing the basic magnetic materials and structures.

The second chapter describes the fundamentals of wire bonding processes and techniques and explains the density limits for ball banding on silicon in order to determine the bonding capability and yield.

The third chapter defines the basic magnetic relationships for the design and the modeling of inductors and transformers in both low-frequency and high-frequency regions.

The fourth chapter shows in detail the design and fabrication of the toroidal and race-track bond wire magnetics realized on both PCB and silicon substrates and assembled with standard gold IC bonding wires. The characterization of the prototypes is reported together with the measurement results compared to air-core devices.

The last chapter illustrates a review of modern low-voltage DC-DC architectures for Thermo Electric Generator (TEG) sources and shows the design of a self-startup resonant DC-DC converter with a bond wire micro-transformer. Finally, small-signal and simulation results together with experimental measurements are reported.

Chapter 1

Micro-magnetics for power applications

1.1 Micro-magnetic materials for magnetic core

The growing demand for miniaturized and efficient micro-magnetics has produced the need for developing magnetic materials as magnetic core for power devices. Soft magnetic materials are usually employed in power components thus providing the desired inductance for micro-inductors and a high magnetizing inductance, as well as a good coupling between the windings, for micro-transformers. This section shows the basic magnetic materials along with the main properties and deposition techniques for the fabrication of the magnetic core.

1.1.1 Magnetic materials

Almost all materials are poor conductors of magnetic flux due to their low relative permeability. Hence the purpose of a magnetic core is to produce an easy path for the magnetic flux in magnetic circuits, similarly as the conductors carry electric currents in electronic circuits. Magnetic materials can be classified in two main categories: soft and hard. Soft magnetic materials can be easily magnetized and demagnetized, so that they can transfer or store magnetic energy in circuits with AC waveforms. Besides, hard magnetic materials are difficult to magnetize and demagnetize, thus making them attractive as permanent magnets in brushless and synchronous electric motors [45].

The major magnetic materials are: silicon steel, nickel-iron alloy (permalloy), cobalt-iron alloy (permendur), ferrites, amorphous metallic alloys, and iron powders. The role of the relative permeability is to give a measure of the enhancement of the magnetic flux concentration compared to air core devices. Furthermore, the presence of the core in magnetic circuits causes an increase in the inductance over the same air core circuit, thus resulting in a better capability to store magnetic energy.

The key properties which define a magnetic material are: relative permeability μ_{rc}, saturation magnetic flux density B_s (T), resistivity ρ_c (Ω m), and operating frequency f_{op} (Hz). The magnetic properties of a material are determined by the interaction of the magnetic dipoles of its atoms with an external magnetic field. These properties depend on the crystalline structure of the material. Hence, magnetic materials can

Table 1.1: Resistivity values of various ferromagnetic materials.

Material	Resistivity $\rho_c\,(\Omega\,\mathrm{cm})$
Co ferrite	10^7
Mg ferrite	10^7
NiZn ferrite	10^6
Cu ferrite	10^5
Mn ferrite	10^4
MnZn ferrite	$10^2 - 10^3$
Zn ferrite	10^2
Fe ferrite	$4 \cdot 10^{-3}$
Metallic glass	$125 \cdot 10^{-6}$
NiFe (permalloy)	$45 \cdot 10^{-6}$
SiFe (silicon steel, 2.5% Si)	$40 \cdot 10^{-6}$
Co alloy (50%)	$35 \cdot 10^{-6}$
SiFe (silicon iron, 1% Si)	$25 \cdot 10^{-6}$
SiFe (silicon iron, 0.25% Si)	$10 \cdot 10^{-6}$
Fe (iron)	$9.6 \cdot 10^{-6}$
Nanocrystalline	$1.2 \cdot 10^{-6}$

be classified in: ferromagnetics, paramagnetics, diamagnetics, antiferromagnetics, and superparamagnetics. Almost all the magnetic cores for power devices are made up of soft ferromagnetic materials due to the better capability of conduct magnetic flux and the larger relative permeability than any other magnetic materials. Popular alloy elements which act as a soft ferromagnetic materials are silicon (Si), aluminum (Al), manganese (Mn), zinc (Zn), and chromium (Cr). Tables 1.1, 1.2 on the next page, and 1.3 on page 4 give an overview, respectively, of the resistivity, saturation flux density, and relative permeability values of several ferromagnetic materials used for power devices [45].

Another parameter is the curie temperature $T_c\,(^\circ\mathrm{C})$ which defines the maximum temperature that disintegrates the ferromagnetic domains. Above the curie temperature, a ferromagnetic material becomes a paramagnetic material, while μ_{rc} drop to 1. Generally, T_c ranges from 120 to 1121 °C, however most of the magnetic cores work at temperature below 100 °C [45].

1.1.2 Properties of magnetic materials

The characteristics of a magnetic core for efficient and miniaturized magnetic components in the frequency range from 1 to 10 MHz can be summarized as: high resistivity, low coercivity, high saturation magnetic flux density, high relative permeability, high magnetic anisotropy field, and low core losses [45, 61].

High resistivity ρ_c leads to low eddy currents in the core which represent a dissipative loss of energy and define the maximum operating frequency f_{op} of the device. Furthermore, a high resistivity material has an increased skin depth $\delta_c\,(\mathrm{m})$ which ensures that the magnetic field intensity is constant within the core thickness $t_c\,(\mathrm{m})$. Low coercivity $H_c\,(\mathrm{A\,m^{-1}})$ allows to minimize hysteresis loss at high frequencies, whilst high saturation magnetic flux density B_s enhances current-handling capability of the device. Besides, high and stable relative permeability μ_{rc} permits to increase the inductance and to get stable performance at high frequency. High magnetic anisotropy

Table 1.2: Saturation flux density values of various ferromagnetic materials.

Material	Saturation flux density B_s (T) at $T = 20\,°C$
50% Co alloy	2.3
0.25% Si iron	2.2
2.5% Si steel	2
Metallic glass	1.6
78% NiFe alloy (permalloy)	1.5
78% NiFe alloy (supermalloy)	1.5
48% NiFe alloy	1.5
50% Ni, 50% Fe	$1.4 - 1.6$
Nanocrystalline	$1.2 - 1.5$
80% Ni, 4% Mo alloy	0.8
50% Ni, 50% Fe alloy	0.75
MnZn ferrite	$0.4 - 0.8$
NiZn ferrite	0.3

field H_k (A m^{-1}) increases the operating frequency and current-handling ability. Finally, core losses which include eddy current and hysteresis losses, can be minimized by using soft magnetic materials with high resistivity and low coercivity field. While resistivity and saturation flux density are intrinsic properties of a core material, permeability, coercivity and anisotropy field can vary depending on the deposition process and shape of the magnetic core.

1.1.3 Deposition techniques for on-chip magnetics

The most widespread deposition techniques for the fabrication of on-chip magnetics are: screen printing, sputtering, and electroplating [61]. Screen printing is generally used for deposition of nonmetallic thin films such as soft ferrites (NiZn and MnZn) because the core material is suspended in a polymer matrix for deposition. While screen printing proposes simple process together with deposition of high resistivity cores ($\rho_c > 1\,\Omega\,\mathrm{m}$), the high temperature annealing makes this technique inappropriate for standard silicon based MEMS technology.

Another approach is sputtering which is suitable for the deposition of a wide range of magnetic materials including alloys with high resistivity ($100 - 1000\,\mu\Omega\,\mathrm{cm}$) which reduce eddy current losses, while ensuring higher saturation flux density and higher permeability. Sputtering is a controlled deposition process compatible with low-temperature Complementary Metal-Oxide Semiconductor (CMOS) fabrication technology, however only films up to a thickness of few hundred nanometers can be deposited due to the expensiveness of the process. Different types of thin films have been sputtered in recent years including CoZrNb, FeCoBC, FeCoBN, high resistivity CoHfTaPd alloy, and nanocrystalline films such as CoZrO and $CoMgF_2$ [61].

Last option is electroplating which is suited for achieving deposition of thick films while maintaining compatibility with standard IC and MEMS fabrication. The most commonly electrodeposited materials are NiFe (permalloy) and NiFeMo (supermalloy) due to their high relative permeability, low hysteresis losses and widely established deposition technology from recording-head industry. Other electroplated materials are $Ni_{50}Fe_{50}$ (orthonol) and $Ni_{45}Fe_{55}$ thin films, especially the latter has higher saturation flux density, high anisotropy field and higher resistivity than standard $Ni_{80}Fe_{20}$

Table 1.3: Relative permeability values of various ferromagnetic materials.

Material	Relative permeability μ_{rc}
Powder	$10 - 60$
NiZn ferrite	150
Cobalt	250
Nickel	600
50% Ni, 50% Fe (orthonol)	2000
MnZn ferrite	$1000 - 4000$
0.25% Si iron	2700
48% Ni alloy	4000
2.5% Si steel	5000
4% Si steel	7000
50% Co alloy	10 000
Metallic glass	10 000
Nanocrystalline	$15\,000 - 150\,000$
80% Ni, 4% Mo alloy	50 000
Mumetal 75% Ni, 5% Cu, 2% Cr	100 000
99.96 % pure iron	280 000
79% Ni, 17% Fe, 4% Mo (permalloy)	$12\,000 - 100\,000$
79% Ni, 5% Mo (supermalloy)	1 000 000

permalloys [63]. Table 1.4 on the next page shows a review of several magnetic materials used as core for micro-magnetic structures [61].

1.1.4 Comparison of on-chip magnetic materials

The most employed integrated magnetic materials for power applications are: soft ferrites, metallic thin films, and nanocomposite thin films [61]. At low frequencies (< 1 MHz) soft ferrites such as NiZn and MnZn are the most widely used materials for power devices. Although they exhibit low saturation flux density and low permeability, thick films ($t_c \sim 500\,\mu$m) can be deposited due to their high resistivity using screen printing techniques. The main disadvantage is the high coercivity which leads to high hysteresis losses at higher frequencies and to an incompatibility with IC fabrication.

At higher frequencies (> 5 MHz) thin films such as permalloy with higher saturation flux density compared to ferrites and lower coercivity are more appropriate. These materials (as metallic alloys) have low resistivity thus limiting the core thickness, and they can be deposited with low temperature silicon technologies such as sputtering and electroplating. Higher composition of magnetic elements such as Fe, Ni, and Co and non-magnetic elements such as O and P is required to reach higher permeability, thus leading to a trade-off between saturation flux density and resistivity based on the application requirements.

For very high frequencies (> 100 MHz) the key property of magnetic thin films is the resistivity due to eddy current losses. The best solution is the lamination of the core with alternate layers of magnetic and dielectric films, to reduce eddy currents and to allow the deposition of thicker magnetic core. In recent times, new nanoengineered materials are emerging for integrated power applications such as nanogranular and nanocomposite ferromagnetic cores [89]. These materials consist of nanoparticles of metallic magnetic material separated by dielectric which allow an improvement in

Table 1.4: Review of core materials for micro-magnetics.

Material	Deposition technique	B_s (T)	μ_{rc}	ρ_c (µΩ cm)	t_c (µm)
NiZn [71]	Screen-printing	0.2	6	108	300
NiZnFeO [49]	Screen-printing	0.23	25	108	100
CoTaZr [51]	Sputtering	1.44	500	100	2.2
CoZrO [13]	Sputtering	0.9	80	2000	6
CoHfTaPd [44]	Sputtering	1	n.a.	170	9
CoZrTa [30]	Sputtering	1.52	300	99	2†
$Ni_{80}Fe_{20}$ [28]	Electroplating	0.8	2000	20	10
NiFeMo [72]	Electroplating	0.8	2500	n.a.	5
$Ni_{80}Fe_{20}$ [72]	Electroplating	1	1300	20	12
$Ni_{45}Fe_{55}$ [63]	Electroplating	1.5	280	45	$3.5-5$

n.a.: data not available.
†: laminated core (4 layers of 0.5 µm each).

Table 1.5: Frequency range values of several ferromagnetic materials.

Material	Frequency range
Iron alloys	$50-3000$ Hz
NiFe alloys	$50-20\,000$ Hz
CoFe alloys	$1-100$ kHz
Nanocrystalline	$0.4-150$ kHz
Amorphous alloys	$0.4-250$ kHz
MnZn ferrites	$10-2000$ kHz
Iron powders	$0.1-100$ MHz
NiZn ferrites	$0.2-100$ MHz

resistivity thus addressing the challenge for high operating frequency. Table 1.5 gives an overview of the frequency range values of different ferromagnetic materials for power devices [45].

1.1.5 Comparison of commercial magnetic materials

The mostly used commercial magnetic materials for power applications are: iron alloys (FeSi), nickel-iron alloys (NiFe), cobalt-nickel alloys (CoNi), ferrites (MnZn and NiZn), powders, ceramic tapes (Low Temperature Co-fired Ceramic (LTCC)), and amorphous (CoFeSi) or nanocrystalline alloys [45].

Iron alloy cores are made of iron and small amount of silicon and exhibit low resistivity ($> 10^{-7}\,\Omega\,\mathrm{m}$) comparable with that of good conductors, high relative permeability ($\sim 2500-5000$), high saturation flux density ($\sim 1.5-2$ T), and high eddy current and hysteresis losses. Generally, silicon is added and lamination is realized in order to reduce eddy currents and to improve the relative permeability. FeSi alloy cores are used at very low frequency (up to 5 kHz) in power transformers and electric motors.

Nickel-iron alloy cores, also called permalloy, are mainly composed by low-nickel or high-nickel alloys and have the highest relative permeability ($> 40\,000$), high satura-

tion flux density ($\sim 0.8-1.5\,\mathrm{T}$), and low resistivity ($> 5\cdot 10^{-7}\,\Omega\,\mathrm{m}$). These materials are sensitive to mechanical stress and are suitable for low frequency applications (up to 20 kHz).

Cobalt-nickel alloy cores have the highest saturation flux density (up to 2.4 T), high relative permeability ($> 10\,000$), low resistivity ($> 3.5\cdot 10^{-7}\,\Omega\,\mathrm{m}$), and same frequency range of NiFe alloys.

Ferrites are the most widespread soft materials in power electronics due to the low cost and low eddy current losses. Commercial ferrites exhibit high relative permeability ($\sim 100-10\,000$), low saturation flux density ($\sim 0.4-0.8\,\mathrm{T}$), and very high resistivity ($> 1-10^{7}\,\Omega\,\mathrm{m}$). They are brittle and sensitive to any shock and, as an insulator, they can be used in the high frequency range (up to 50 MHz). MnZn ferrites have higher permeability (> 1000), relatively low resistivity ($> 1\,\Omega\,\mathrm{m}$), and low operating frequency (up to 2 MHz), while NiZn ferrites have lower permeability (< 300), higher resistivity ($> 10^{3}-10^{7}\,\Omega\,\mathrm{m}$) and thus low losses, and high operating frequency (up to 50 MHz).

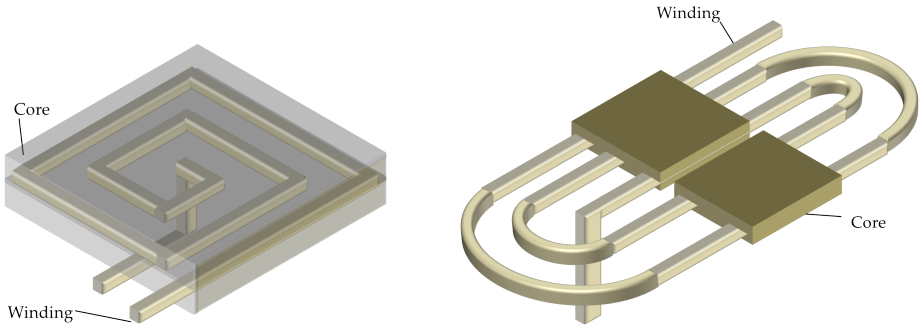
Powder cores are manufactured from pulverized iron alloys or permalloy by grinding the base material into fine particles (size from 5 to 200 µm) plus a coating with an inert insulating material. Powders have low relative permeability ($\sim 10-500$), relatively high saturation flux density ($\sim 0.5-1.3$ T), high resistivity ($\sim 1\,\Omega\,\mathrm{m}$), and find use in toroidal inductors for switched-mode power supplies in a wide range of frequencies (from 1 kHz to 10 MHz).

LTCC tapes are flexible films of magnetic powder designed to be fired at high temperature. These tapes have low relative permeability ($\sim 50-600$), very high resistivity ($\sim 10^{7}\,\Omega\,\mathrm{m}$), and can be used for high frequency applications.

Finally, nanocrystalline or amorphous alloys are thin films ($\sim 20\,\mu\mathrm{m}$) prepared from ultra-fine grains (size from 10 to 20 nm) with high saturation flux density ($\sim 1.2-1.5\,\mathrm{T}$), very high relative permeability ($\sim 15\,000-150\,000$), and fairly low resistivity ($\sim 10^{-6}-10^{-8}\,\Omega\,\mathrm{m}$). Nanocrystalline materials are usually laminated to reduce eddy current losses and to improve the operating frequency (up to 100 MHz).

1.2 Micro-magnetic structures for power devices

The choice of the magnetic structure is essential to achieve high-inductance, minimize resistive losses at high frequency, and to get the largest current available without saturating the core. Hence, power devices employ a magnetic core to increase the inductance value. Magnetic components represent one of the key challenges for the evolution of PwrSiP and PwrSoC platforms. The structure of a power device can be classified into two main approaches depending on the arrangement between conductors and magnetic core. In the first approach the planar coils are enclosed by a multilevel magnetic core. Typical models are spiral and strip-line inductors and transformers. In the second approach the conductors are wrapped around a planar magnetic core. Typical models are toroidal and solenoid inductors and transformers, as well as bond wire magnetics based on existing IC bonding wires. In order to characterize the performance of a magnetic structure in a fixed footprint area, several factors must be considered including: high inductance value per area, low DC resistance to get high current, and high quality Q-factor for high efficiency [52, 61]. This section outlines in detail the aforementioned structures together with the main DC and AC figures of merit.



(a) Square-shaped spiral inductor. **(b)** Race-track shaped spiral inductor.

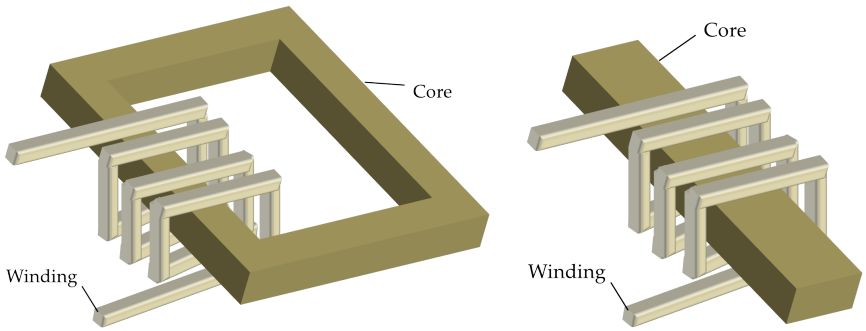
Figure 1.1: Examples of spiral micro-magnetics.

1.2.1 Spiral magnetics

The spiral type magnetics are the most appropriate structures to form a planar inductor or transformer due to their high inductance value, low DC resistance, and high Q-factor [1, 61]. Typical shapes of spiral magnetics are both square or circular [46, 67]. The spiral structure is obtained by enclosing the windings in a magnetic material to achieve the required inductance and to reduce ElectroMagnetic Interference (EMI). The main drawback of the spiral structure is the difficulty to induce anisotropy in the magnetic core during the deposition process. This compromises the ability to minimize core loss at high frequency and limits its application frequency. Typically, integrated spirals for power supplies are limited to switching frequency $< 10\,\text{MHz}$ with a current lower than 1 A.

A race-track shaped spiral inductor can be fabricated by stretching a circular loop thus resulting in an elongated form [63, 87]. Figure 1.1 shows a picture of a square-shaped (a) and race-track shaped (b) spiral micro-inductors. The core can be deposited in the presence of a magnetic field to induce a uniaxial anisotropy along the longitudinal direction, which generates a magnetic easy axis in the direction of current flow. In [7] a 0.9 µH race-track spiral transformer is reported with NiFe permalloy core capable of working up to 5 MHz with an efficiency of 40, whilst in [69] a 300 nH race-track inductor with NiFe core is suitable for use in high frequency, i.e. $> 10\,\text{MHz}$, with high efficiency. Another example of spiral structure is the inductor in [30] compatible with 90 nm CMOS process with inductance higher than 100 nH with a CoZrTa core. At high frequencies small sized air core inductors with small values of inductance are generally used, with the downside of higher power losses in coils due to Joule heating than magnetic core inductors, as many more turns are required to achieve a sufficient inductance. In [62] a comparison between 36 nH magnetic core and 36 nH air core spiral inductors designed to operate up to 100 MHz is reported, and shows that the performance of the magnetic core inductor is superior up to 50 MHz than the air core inductor. However, for higher frequencies lamination is essential to limit eddy currents. Besides, several race-track inductors have been realized in several buck converters at frequencies up to 100 MHz [98, 99].

Last option for developing high-power spirals is to embed the structure in the substrate, i.e. silicon [97] or PCB [102], thus getting low profile and increased packaging densities.



(a) Toroidal inductor. **(b)** Solenoid inductor.

Figure 1.2: Examples of toroidal micro-magnetics.

1.2.2 Toroidal magnetics

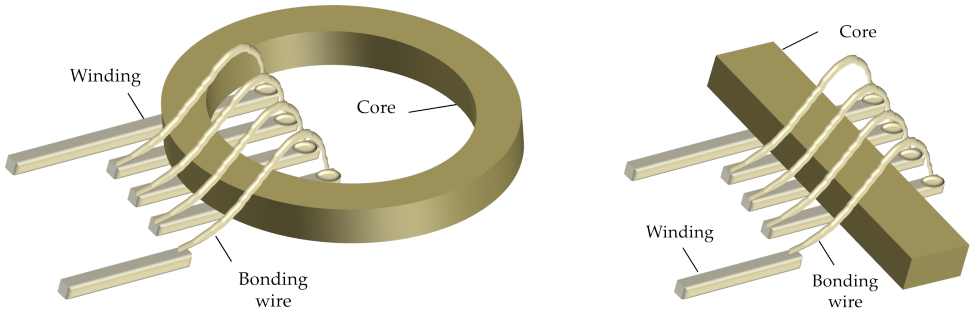
The toroidal type structure is another approach to realize micro-inductors and micro-transformers. This structure uses conductors wrapped around a magnetic core, and is more suitable for power supplies with switching frequency below 10 MHz. The main defects of toroidal magnetics are the difficulty to achieve an uniaxial anisotropy field, as for spirals, and the high process complexity due to the multilevel metalizations. A toroidal inductor design is implemented in [70] in a 5.6 mm x 5.6 mm device area with an inductance of 0.5 µH up to 10 MHz and a Q-factor up to 20. A race-track shaped toroidal magnetics can be obtained with a stretched version of the toroidal core, thus permitting an uniaxial anisotropy in the magnetic core useful for higher frequencies and allowing higher turns density. In [1] a toroidal micro-inductor with permalloy core is fabricated with an inductance of 0.4 µH at 10 kHz and a DC resistance of 300 mΩ, whilst [28] shows an inductor with inductance up to 120 µH and Q-factor up to 14 with Vitrovac and NiFe alloy cores.

Another form can be obtained by a solenoid structure which uses a bar core shaped magnetic core. Solenoid race-track shaped magnetics have been fabricated as shown in [51] with inductance above 70 nH in a footprint area below 1 mm^2. Figure 1.2 shows a picture of a toroidal (a) and solenoid (b) micro-inductors.

1.2.3 Bond wire magnetics

The bond wire type structure is a simple approach to fabricate a power device by using regular IC bonding wires technology to enclose the magnetic core as in toroidal magnetics. This construction has several advantages compared to MEMS technology as a post-processing step to realize the magnetics [56]. Firstly, the standard process and the low resistivity of bonding wires (aluminum or gold) compared to the metallic thin films, and the higher Q-factor. Secondly, the components realized with bonding wires can be integrated into the System on Chip (SoC) packaging process, thus making possible the realization of cost-effective and efficient power converters [57].

In addition, bond wire magnetics with toroidal core demonstrate high inductance to DC resistance ratio, which is a key parameter for evaluating the DC performance of magnetics, as well as a small footprint area [61, 70, 89]. Beyond this, the performance of bond wire magnetics can be optimized by varying the wire loop height and the core thickness. Moreover, the toroidal geometry produces very small EMI which is



(a) Toroidal bond wire inductor. **(b)** Solenoid bond wire inductor.

Figure 1.3: Examples of bond wire micro-magnetics.

distributed mainly outside the IC substrate due to the planar closed magnetic path, ergo reducing high frequency effects in the bulk [68, 88]. Figure 1.3 shows a picture of toroidal (a) and solenoid (b) bond wire micro-inductors. The structure of bond wire components allows to deposit magnetic materials by using sputtering or electroplating techniques [61].

Several examples of bond wire magnetics are reported in literature. In [55, 57] a solenoid bond wire 2 : 1 micro-transformer with 70 nH of inductance is described with MnZn ferrite epoxy core for PwrSoC applications. An improved version of solenoid bond wire inductor is reported in [56] with inductance up to 340 nH, whilst [42] shows an IC power converter built in a 0.5 µm CMOS process with 3-turn bond wire inductors. Other attractive devices are the on-chip magnetics proposed in [96] with gold bonding wires and inductances up to 2.7 µH at 1 MHz. These devices use very thin permalloy and ferrite layers as magnetic core with a thickness of 0.25 mm and race-track shaped toroidal geometry with electroplated gold metalization. Besides this, in [58, 59] several prototypes of bond wire 1 : 38 transformers with toroidal ferrite cores are presented with very high inductances up to 315 µH and high Q-factor up to 24.5 for both PCB and silicon substrates.

Table 1.6 on the next page shows a comparison of various power devices in the actual literature with several magnetic core structures including spiral, toroidal and bond wire magnetics.

1.2.4 Integration techniques

Since magnetic components are the largest part of power converters, the interest for reducing the size of power devices is highly increasing in recent years [52]. Several integration techniques are currently available for shrinking micro-magnetics which can be classified into: board level, package level, and wafer level.

For board level the magnetic devices are integrated in an organic-based Flame Retardant 4 (FR4) or ceramic-based LTCC substrates. The mechanical properties such as processing temperature of the organic substrate are not compatible with the silicon die, whilst ceramic substrate are generally suitable for silicon. For package level the magnetic devices are co-packaged side by side with the die and combined inside within the package. Finally, for wafer level the magnetic components are directly built

Table 1.6: Comparison of power devices in actual literature with different magnetic core structures.

Work	Device	Structure	Core material	Max inductance	Turns	Max Q-factor
[7]	Transformer	Spiral race-track	Permalloy	0.9 µH	4 : 2	n.a.
[69]	Inductor	Spiral race-track	NiFe alloy	300 nH	5	n.a.
[30]	Inductor	Spiral race-track	CoZrTa alloy	160 nH	6	8
[28]	Inductor	Toroidal race-track	Vitrovac and NiFe alloys	120 µH	33	14
[70]	Inductor	Toroidal	NiFe alloy	0.5 µH	12	20
[1]	Inductor	Toroidal race-track	Permalloy	0.4 µH	33	1.5
[51]	Inductor	Solenoid	CoTaZr film	70.4 nH	17	6
[57]	Transformer	Solenoid bond wire	MnZn ferrite epoxy	70 nH	2 : 1	n.a.
[56]	Inductor	Solenoid bond wire	MnZn ferrite epoxy	340 nH	10	28
[42]	Inductor	Solenoid bond wire	Ferrite epoxy	450 nH	3	n.a.
[96]	Inductor	Toroidal bond wire	Permalloy and ferrite	2.7 µH	35	n.a.
[58]	Transformer	Toroidal bond wire	MnZn and NiZn ferrites	315 µH	1 : 38	24.5

n.a.: data not available.

on the same IC or on top of the silicon die. For magnetics built on top, the power components are fabricated on top the active circuitry thus decreasing the overall device area. For magnetics fabricated in the die, the power inductors or transformers are built nearby the active part on the same die. Besides this, from low (board) to high (wafer) integration levels the output current is reduced while the operating frequency is improved [52].

Generally, air core spirals implemented directly in the substrate have been used in Radio Frequency (RF) circuits [3, 53], whilst spirals with magnetic core are generally developed for board [6] and wafer [97] level integrations. On the other hand, both bond wire and toroidal structures are suitable for integration into the PwrSiP and PwrSoC platforms for package and wafer level integrations.

1.3 Figures of merit for micro-magnetics

1.3.1 DC figures of merit

The main DC parameters for the design of a micro-inductor are: inductance $L\,(\mathrm{H})$, series DC resistance $R^{DC}\,(\Omega)$, number of turns n, saturation current $I_{sat}\,(\mathrm{A})$, and footprint area $A_r\,(\mathrm{mm}^2)$.

The inductance per unit DC resistance $L/R^{DC}\,(\mathrm{H}\,\Omega^{-1})$ is a useful figure of merit to evaluate the DC performance of micro-inductors [61]. For a given footprint area, L/R^{DC} can be improved in several ways by: increasing the number of turns, using a thicker core, and employing a higher permeability core. Adding more turns in a fixed device area implies the use of thinner conductor thus enlarging the R^{DC}. Core thickness can be improved until reaching the skin depth while a laminated core can be adopted, however this will increase the process complexity. Finally, a higher permeability core can be adopted, despite this limits the saturation current and operating frequency of the device.

A comparative performance of power micro-inductors can obtained by plotting the L/R^{DC} versus the energy density $E\,(\mathrm{J})$ defined by $E = L \cdot I^2/2 \cdot A_r\,(\mathrm{J\,m^{-2}})$ where $I\,(\mathrm{A})$ is the current of the inductor. Generally, E can be enhanced by reducing the relative permeability, this will decrease linearly the inductance while increasing quadratically the saturation current. Alternatively, the use of high permeability core improves the inductance but with lower energy density. Figure 1.4 on the following page shows a comparison of the L/R^{DC} versus E of several integrated and commercial micro-inductors.

Commercial ferrite, ferrite based, and bond wire inductors show quite high energy density with high L/R^{DC} due to the thick magnetic core employed, whilst micro-inductors which use magnetic core have higher inductance than air core inductors. Solenoid inductors lead to high L/R^{DC} with low energy density, because the larger number of turns which decreases the saturation current. Spiral inductors are considered as a structures which lead to high inductance at low energy density. Toroidal and race-track shaped inductors show a trade-off between L/R^{DC} and energy density, however they demonstrate similar performance to solenoid and spiral inductors [62]. Finally, air core devices show the lowest L/R^{DC} with different energy density. The most effective method for improving L/R^{DC} while maintaining high energy density is the use of a laminated core and the apply of thicker conductors [61].

1.3.2 AC figures of merit

The AC performance of micro-magnetic components can be evaluated by the Q-factor expressed as $Q = 2\,\pi\,f_{op}\,L/R$, which represents a measure of the AC losses within the magnetic structure at different frequency of operation. AC losses of a power device includes AC core loss determined by the core material, and AC winding loss determined by the conductors characteristics [61].

Core losses are primarily of two kinds: hysteresis loss and eddy-current loss [45]. Hysteresis loss represents the energy used for aligning and rotating magnetic moments of the core, due to the friction forces involved in changing the alignment of the magnetic domains. This energy is dissipated in the core thus producing heat. When using a power device in an AC circuit, the core material goes through the hysteresis loop the same number of times per second as the frequency of the applied current.

Eddy-current loss is produced by the eddy currents in the core which are generated

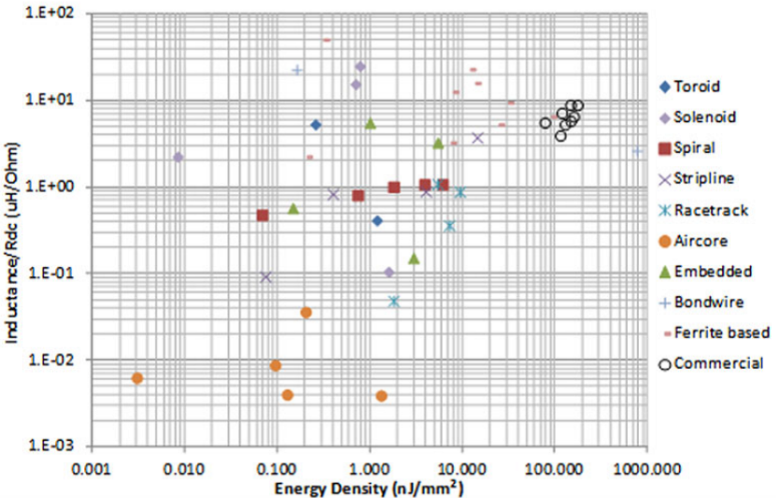


Figure 1.4: Comparison of inductance per unit DC resistance versus energy density of various micro-inductor structures [61].

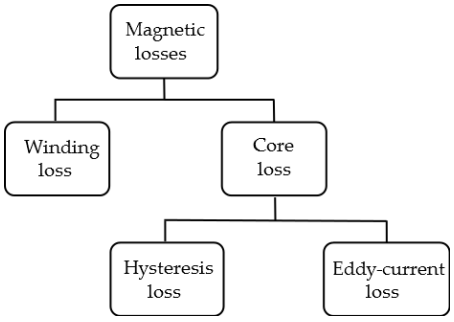


Figure 1.5: Classification of power losses in magnetic components.

from a time-varying magnetic field. These currents are induced every time there is a change in the magnetic field, and follow circular paths normal to the direction of the magnetic flux. The higher resistivity of the core material, the lower eddy-current loss. As for hysteresis loss, eddy currents cause heating of the core, hence they must be added at the total core losses. Similarly, winding loss is caused by eddy currents in the conductors which increase the series resistance at high frequency. Figure 1.5 shows a classification of power losses in micro-magnetic components.

Chapter 2

Fundamentals of wire bonding

Wire bonding is the most common chip interconnection technique in the packaging of semiconductor components [36, 65, 93]. All wire bonding processes are based on solid phase join where two materials are brought into close contact. This produces electron sharing and atom diffusions depending on the materials involved and process conditions, thus resulting in the formation of the bond. Generally, the wires are bonded one at a time using a special tool and a combination of several parameters such as heat, pressure, and ultrasonic energy. Figure 2.1 on the following page shows an example of a chip attached to a substrate which is placed in a package with wire bonds performed.

This chapter presents the major techniques and processes for wire bonding, analyzes the quality and reliability of wire bonds, and explains the density limits for ball bonding on-chip. Finally, the design and wire bond process optimizations are shown, and a comparison of chip interconnection techniques is reported.

2.1 Techniques and processes for wire bonding

Three major techniques are developed for wire bonding technology depending on the welding agents: Thermocompression (T/C) bonding, Ultrasonic (U/S) bonding, and Thermosonic (T/S) bonding [50, 65]. The shape of the bond wire is a direct consequence of the wire bonding method and tool (capillary or wedge) used. T/C and T/S bonding typically produce a ball-wedge bond because the first bond has a ball while the second has a wedge. This allows an easier manufacturing since after performing the first ball bond the wire may be moved in any direction without stress on the wire, while the second wedge bond lies on an arc about the first ball bond. Figure 2.2 on the next page shows two pictures of the basic form of the bond: ball bond (a) and wedge bond (b). On the other hand, U/S bonding produces a wedge-wedge bond because both bonds have wedges. In this case, the manufacturing is more difficult because the second wedge bond lies on the center line of the first wedge bond, while the loop height $H\,(\mathrm{m})$ is lower than in ball-wedge processes. Figure 2.3 on page 15 shows two pictures of the two main wire bonding formation: ball-wedge for T/C and T/S bonding (a) and wedge-wedge for U/S bonding (b); with $D\,(\mathrm{m})$ as the wire diameter.

In the T/C bonding the wire and the substrate are heated to high temperature ($300 - 500\,^{\circ}\mathrm{C}$) by mounting the substrate on a hot stage, while the intimate contact is performed in a controlled time, pressure and temperature cycle with a capillary

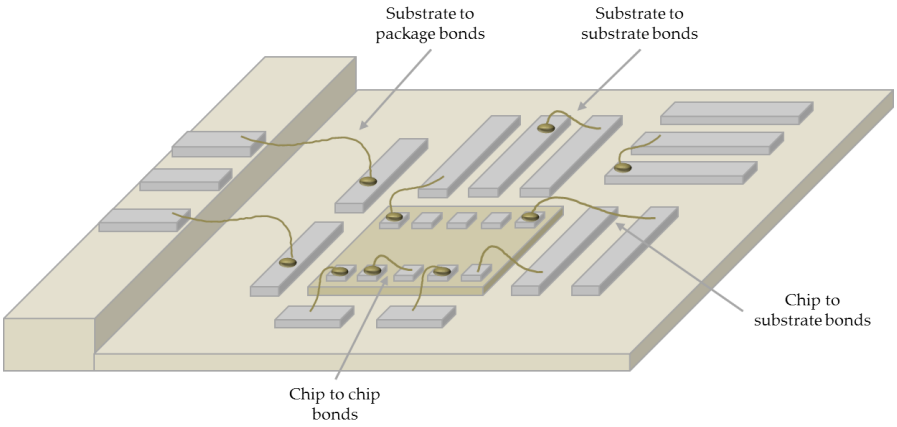
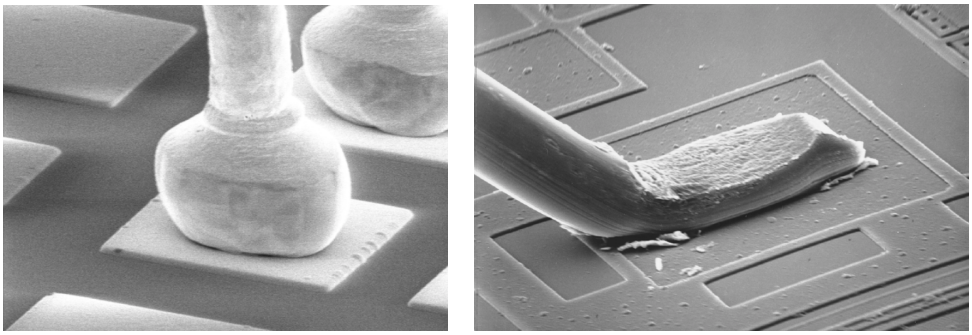


Figure 2.1: Example of a chip attached to a substrate placed in a package with wire bonds in place.



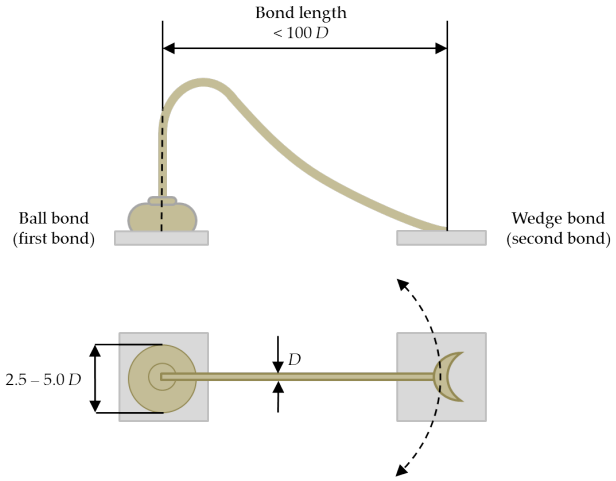
(a) Ball bond. **(b)** Wedge bond.

Figure 2.2: Pictures of the basic form of the bond.

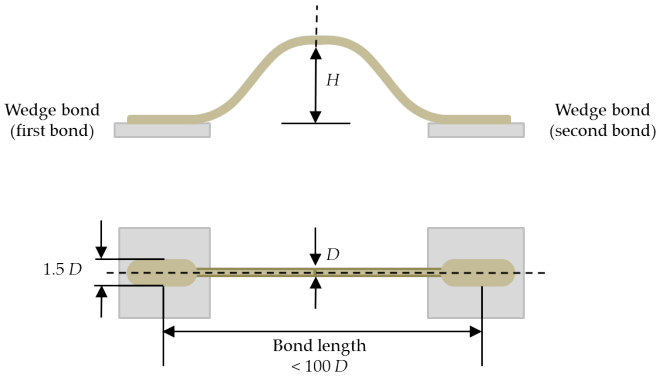
tool. Gold wire is commonly used since gold can be easily deformed under pressure at elevate temperature and resists oxidation while diffusing readily. Ball bonding is used in preference to wedge bonding since higher bonding rates can be obtained, while one disadvantage is the high temperature involved during die attach through high temperature solders.

In the U/S bonding the welding is achieved in a low-temperature process where the source of energy is a transducer vibrating the bonding wedge tool. The combination of pressure and ultrasonic vibration ($20-60\,\mathrm{kHz}$) produces the metallurgic weld (cold) while causing surface oxides and contaminants to disperse thus getting a smoothing interface. Aluminum or gold wires are generally used onto either aluminum or gold pads.

In the T/S bonding ultrasonic energy with the ball bonding technique of the T/C bonding are combined with lower temperature ($100-150\,^{\circ}\mathrm{C}$). Ultrasonic bursts of energy ($20-50\,\mathrm{ms}$) are generally used to produce the bond. Since the heat is applied through the substrate without affecting adhesive die attachments, T/S bonding has been used with gold wire onto gold or aluminum pads while reducing the risk of uncontrolled intermetallic growths. Table 2.1 shows the characteristics of the major



(a) Ball-wedge for Thermocompression (T/C) and Thermosonic (T/S) bonding.



(b) Wedge-wedge for Ultrasonic (U/S) bonding.

Figure 2.3: Characteristics of the main wire bonding formation techniques.

wire bonding methods used in modern IC.

2.2 Quality and reliability of wire bonds

Wire bonding quality is determined by many factors involved in the bonding process such as: bond placement accuracy, bond shape, loop shape and proximity, bond pull strength, and bond shear strength. While visual inspection and electrical test of bonds are usually carried out, there are two mechanical methods for testing wire bonds: pull strength test and shear strength test [95]. Pull strength test is a destructive mechanical testing based on a simple loop pull arrangement by placing a hook under the wire and by applying a normal upward force until the wire is pulled up while recording the load failure force. Pull test gives information about wire bond quality and its associated bonding process. Shear testing is a destructive test applicable to both ball and wedge bonds by moving a shear tool parallel to the bonded surface and by shearing the ball bond while measuring the shear strength. Shear test gives infor-

Table 2.1: Characteristics of the main processes for wire bonding technology.

Process	Pressure	Temperature	Ultrasonic energy	Wire material	Pad material
T/C	High	300 – 500 °C	No	Au	Au, Al
U/S	Low	25 °C	Yes	Au, Al	Au, Al
T/S	Low	100 – 150 °C	Yes	Au	Au, Al

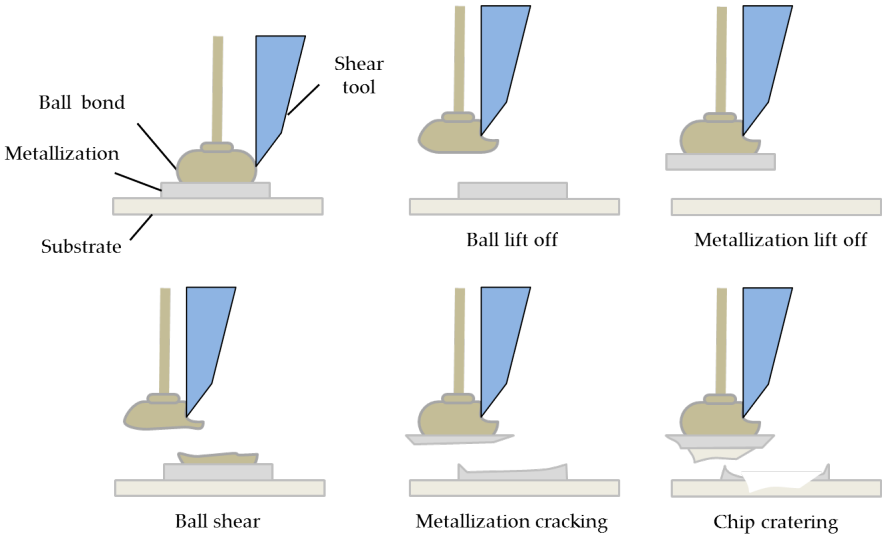


Figure 2.4: Examples of failure modes obtained with destructive shear strength test.

mation about the quality and the integrity of the ball (or wedge) bond to substrate. Figure 2.4 shows the major failure modes obtained with shear strength test.

Despite the reliability improvements and high yields per wire, many problems still take place in wire bonded interconnection systems [65]. Common complications include stress-strain matches, die attach media interactions, and wire breakage due to grain growth followed by stress-induced creep. This section shows the wires used and the metallurgical systems produced in wire bonding.

2.2.1 Wires used in wire bonding

Gold wire is used extensively for T/C and T/S bonding. Surface finish and cleanliness are the critical issue to ensure the formation of a strong bond to prevent bonding capillaries. Pure gold can be pulled to produce an adequate breaking strength and the proper elongation to be used as bonding wire. Ultra pure gold is very soft, but even extremely small amount of impurities, 5 to 10 ppm by weight or 30 to 100 ppm of Cu are added to make the gold wire workable [50, 65].

Pure aluminum is typically too soft to be pulled into a fine wire. Therefore, aluminum is often alloyed with 1% Si or 1% Mg to provide a reinforced mechanism. At room temperature 1% Si exceeds the solubility of silicon in aluminum by a factor of 50 which leads to silicon precipitation. The number and the size of the silicon precipitates are dependent on the cooling rate from higher temperatures. Al-1% Mg

(a) Gold-aluminum intermetallic growth around a gold ball bond on an aluminum pad.

(b) Gold-aluminum intermetallic consumed over a gold wedge bond on an aluminum pad.

Figure 2.5: Pictures of intermetallic compounds of an AuAl system [65].

alloy can be drawn into a fine wire that exhibits a breaking strength similar to that of Al-1% Si. The Al-1% Mg alloy wire bonds are superior to the Al-1% Si bonds in resistance to fatigue and to degradation of ultimate strength after exposure to high temperatures [50, 65].

Recently, copper wire has been used for bonding IC metalization with both T/C and T/S bonding due to their economy and resistance of the wire to move in the plane perpendicular to its length (sweep) during encapsulation. The major problem of copper wire is the bondability because copper is harder than gold and aluminum hence causing the cratering of the metalization aside [50, 65].

2.2.2 Metallurgical systems

In wire bonding process the reliability depends on the growth of intermetallic compounds between wire and pad metalization [50]. Intermetallic formation is the series of compounds which can be produced when gold wire and aluminum pad (or vice versa) are used. The exact compound depends on the process conditions including time, temperature, and amount of each element. Typical metallurgical systems are: AuAu, AuAl, AuCu, AuAg, AlAl, AlAg, AlNi, and CuAl.

Gold wire to gold pad (AuAu) is extremely reliable because the bond is not subjected to interface deterioration and intermetallic formation. Even a poorly welded gold-gold bond will increase in strength with time and temperature. Either T/C and T/S bonds are easily and reliable.

Gold to aluminum (AuAl) welding is the most commonly used in wire bonding processes, however this bonding can lead to the formation of intermetallic compounds such as purple plague $AuAl_2$ and white plague Au_5Al_2. These metallurgical systems are brittle materials unstable at high temperatures because Kirkendall voids tend to form due to different diffusion rates of Au and Al atoms [50, 65, 73]. This causes bond failure and increases the electrical resistance of the joint. Figure 2.5 shows two pictures of intermetallic compounds in a gold-aluminum system: intermetallic growth on a gold ball bond realized on an aluminum pad (a) intermetallic consumed on a gold wedge bond performed on an aluminum pad (b).

Gold wire to copper bond (AuCu) can cause the formation of three ductile intermetallic phases such as Cu_3Au, AuCu, and Au_3Cu. These compounds can decrease

the bond strength at higher temperature as a result of Kirkendall voiding. Generally cleanliness of the bonding surface is extremely important to ensure good bondability and reliability.

Gold to silver system (AuAg) is very reliable for very long times at high temperatures. This system does not form intermetallic compounds and interface corrosion, however bondability problems can arise from contaminants like sulfur.

Aluminum to aluminum system (AlAl) is highly reliable because it does not produce intermetallics and corrosion. Aluminum wire on aluminum metalization welds best with U/S bonding.

Aluminum bond to silver pad (AlAg) is often used in thick film hybrids. The phase diagram is very complex with many intermetallic phases, while Kirkendall voids can occur only at temperature higher than the operating range of electronic circuits.

Aluminum to nickel system (AlNi) is typically used with large diameter wires, i.e. $D > 75\,\mu m$, while aluminum wires are less predisposed to Kirkendall voiding and galvanic corrosion. This metallurgical system has used in high production on power devices and high temperature applications. The main problems when bonding to nickel is bondability rather than reliability due to nickel surface oxidation.

Copper wire to aluminum substrate (CuAl) can produce five different intermetallics similar to those of AuAl system, however the growth in the former is slower. The intermetallic growth in CuAl bonds does not result in Kirkendall voiding but lowers the shear strength at $150 - 200\,°C$ due to the growth of a brittle $CuAl_2$ phase. In the range $300 - 500\,°C$ bond strength significantly decreases with the increase of the total intermetallic thickness.

Finally, the major causes of bond failure which inhibit the intimate metal-to-metal contact are due to: short exposure to high temperature (few hours $> 300\,°C$), longer exposure to moderate temperature (hundreds of hours $> 150\,°C$), presence of moisture within the package, and presence of ionic contamination (Na^+, K^+, Cl^-). Ideally a monometallic bonding system should be used [65].

2.3 Density limits for ball bonding on-chip

Nowadays wire bonding has become the main chip interconnection technology, thus bringing to reduce pad dimension and wire diameter. Actually, wires as small as $18\,\mu m$ can be bonded using T/S process. As the density of chip interconnects has increased during last years, wire bonding has progressed to a fully automated process while T/S and U/S bonders have become the most widespread techniques. Automatic wire bonding uses patter recognition to locate marks on both the chip and the package, and, after alignment, the bonder automatically bonds all Input/Output (I/O) connections at a rate up to five bonds per second [65].

In order to validate the bonding capability several constraints have to be considered for ball bonding technique [93]. Figure 2.6 on the facing page shows the spacing limitations for ball bonding on-chip. The first constraint is the width of the bonding window (1) which should not overlap the passivation. As shown on the top scheme of Figure 2.3 on page 15, item (1) must be greater than the minimum ball spread which is comprised between 2.5 to 5.0 times the wire diameter D. The second limit is the distance between top of in-place ball and edge of capillary tip (2). The third limit is the distance between top of bonding loop and conical edge of capillary (3). Finally, the last constraint is the wire-to-wire spacing (4) or Bond Pad Pitch (BPP) which is restricted by items (1), (2), and (3). Common values of BPP range from $90\,\mu m$ to

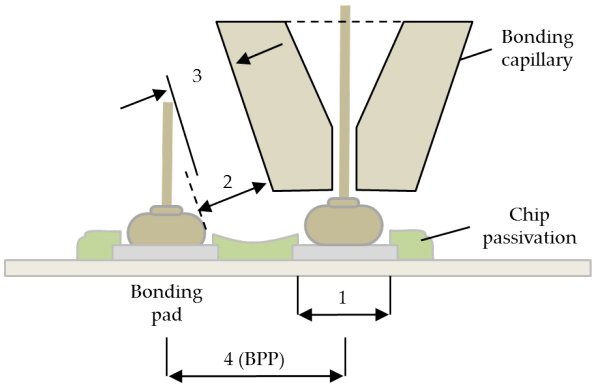


Figure 2.6: Spacing limitations for ball bonding on chip.

140 µm for wire diameters between 18 µm to 32 µm, respectively.

2.4 Design process optimization

Electrical and mechanical characteristics of the materials involved in the wire bonding process must be considered in the design process for achieving a reliable wire bond. The design process of wire bond connections includes the choice of: wire diameter and material, pad dimension and material, and wire aspect ratio [50]. The minimum allowable wire diameter is generally based on the maximum acceptable resistance per unit length, while the bond pad dimension, including the BPP, is used to evaluate the maximum number of wire bond connections. Critical wire material properties must be considered such as: wire resistivity, shear strength, tensile strength (yield and ultimate), Young's modulus, Poisson's ratio, hardness, and coefficient of thermal expansion. Besides this, the metalization material needs to be selected to match right the wire used. The main characteristics involved in the choice of the pad material are:

- pad resistivity;
- pad bondability;
- pad tendency to form intermetallic compounds;
- pad hardness;
- pad corrosion resistance;
- pad coefficient of thermal expansion.

Several points derived from the physics of failure models must be considered in the design process flow [50]:

- wire material must be a low resistivity metal to ensure signal integrity coming from the IC without deteriorating;
- wire diameter must not exceed 1/4 of the pad size in case of ball bonds and 1/3 of the pad size in case of wedge bonds;

- yield strength, ultimate tensile strength, and endurance limit of the wire must be greater than stresses produced in the wire during temperature cycles;
- bond materials should have interdiffusion constants which allow the formation of a strong bond while preventing excess intermetallics during the expected operational life (see subsection 2.2.2 on page 17);
- pad material should be free of impurities to ensure good bondabiity;
- wire and bond pad hardness should be reasonably matched because a wire harder than the pad would inhibits cratering by absorbing the energy during the bonding process; while a wire softer than the pad would dissipates the energy from the bonding process to the substrate.

The electrical and mechanical performance of a wire bonded package can be optimized if the designer knows the capabilities and limitations of the wire bond process [50]. The main constraints for a ball banding process as shown in Figure 2.3 on page 15 (a) are:

- ball size is approximately 2 to 3 times the wire diameter, 1.5 times for small ball applications with fine pitches, and 3 to 4 times for large bond pad application;
- bond size should not exceed 3/4 of the pad size, about 2.5 to 5 times the wire diameter, depending on the geometry and moving direction of capillary during bonding;
- loop heights of 150 mm are now common, but they depend on the wire diameter and on the application;
- loop length should be less than 100 times the wire diameter. However, in some cases such as high I/O connections wire lengths have to increase to more than 5 mm.

On the other hand, the main constraints for a wedge bonding process as shown in Figure 2.3 on page 15 (b) are:

- a high-strength wedge bond is possible even the bond is only $2-3\,\mu m$ wider than wire diameter;
- pad length must support the longitudinal dimension of the wedge bond as well as the tail;
- the pad's long axis should be oriented along the intended wire path;
- bond pad pitch must be designed to maintain consistent distance between wires.

2.5 Wire bond process optimization

2.5.1 Bonding parameters

Bonding parameters are of fundamental importance because they control the bonding yield and reliability of the entire bonding process [36]. The key variables involved in the wire bonding process, as discussed in the section 2.1 on page 13, are listed below:

- bonding force;
- bonding temperature;
- bonding time;
- ultrasonic frequency and power.

The force imposed on the wire holds the two surfaces in close contact with each other. The force must be strong enough to localize the ultrasonic energy onto the wire without causing excessive deformation, while too little force may result in skipping and cratering. Typical force values are $30-45\,\mathrm{g}$ for the first bond, while $70-90\,\mathrm{g}$ for the second bond.

Temperature is induced into the process either through a heated workholder or through the tool by a heated capillary. The action of the heat is twofold: dissipate any water vapour, and plasticize the wire. Typical temperature range depending on the adopted techniques are listed in table 2.1 on page 16.

Time is needed for the welding mechanism to fully take place. Typical values for time are $30-40\,\mathrm{ms}$ for the first bond, while $40-50\,\mathrm{ms}$ for the second bond. Any time over $50\,\mathrm{ms}$ is generally wasted because it produces overworking of the wire which will lead to metal fatigue, except for very thin wire applications where low power and long time are required to produce an acceptable bond.

Finally, ultrasonic energy results from a mechanical scrubbing action that: removes contaminants and irregularities from the bond junction, and helps diffusion of the metals by causing acoustic slippage in the crystal lattice. Typical values of ultrasonic frequency are $55-65\,\mathrm{kHz}$ depending on the bonding process. Ultrasonic power is needed also to improve the ultrasonics from values of $3\,\mathrm{W}$.

2.5.2 Optimization of parameters

Wire bonding optimization is a simple logical process in which the bonding parameters should be adjusted so that reproducibility is at a maximum whilst maintaining high full strength. These optimum conditions are further controlled by wire type, pad metalization, and device configuration. Hence, a series of bonding tests have to be performed by varying bonding parameters until reaching the optimum conditions [50].

Three sets of curves of bond pull strength versus power, time, or force can be obtained by varying one of these parameters while holding the other two constants at their optimum values. Each curve is similar to the curve of bond pull strength versus wire deformed width shows in Figure 2.7 on the next page. As each parameter is increased, the bond grows stronger in lift-off strength. At the same time, due to wire deformation, the transition from the wire into the bond becomes weaker. At maximum pull strength the failure mode changes from bond lift-off to wire breakage failure. We can deduce that lowest reproducibility is within the lift-off failure region and within the breakage failure region after the deformed width exceeds two times the wire diameter. Highest repeatability is within the breakage failure region, directly after the maximum pull strength. This is the optimum bonding region which produces maximum reproducibility consistent with high pull strength.

2.6 Comparison of chip interconnection methods

The electronic packaging industry is providing solutions to address the challenges posed by recent developments in silicon technology. Multi Chip Modules (MCM) is

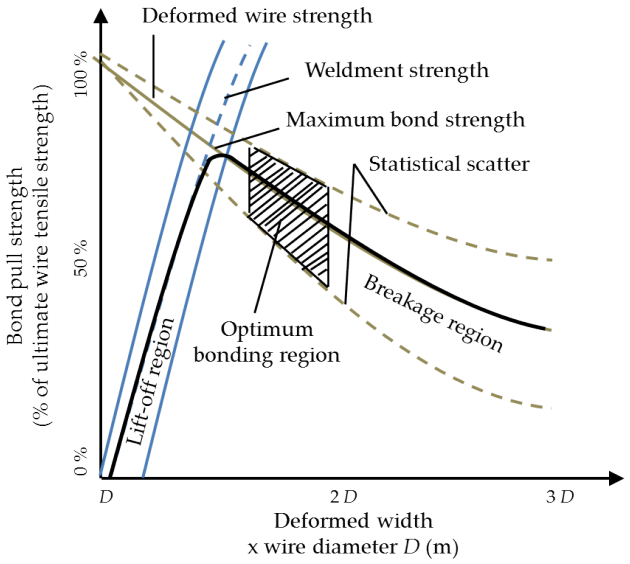


Figure 2.7: Curve of bond pull strength versus wire deformation width.

a promising solution where a package combines multiple ICs into a single system-level unit [50]. The resulting module is capable of handling an entire function. The components of an MCM are normally mounted encapsulated on a substrate where the bare dies are connected to the surface by wire bonding technology. MCM offers an impressive variety of advantages instead of mounting packaged components directly on the PCB such as:

- performance improvements: shorter interconnect lengths between die, lower power supply inductance, lower capacitance loading, less cross talk, and lower off-chip driver power;
- miniaturization capability: MCM results in a smaller overall package when compared to packaged components making the same function, hence resulting I/O to the system board is significantly reduced;
- low manufacturing cost silicon sweep allows the integration of mixed semiconductor technology;
- lower board complexity: several devices onto one package reduce the complexity and minimize the cost of PCBs;
- improved reliability: less number of interconnects between components and boards.

Three separate technologies are involved in the manufacturing of an MCM: substrate technology, die attach and bonding technology, and encapsulation technology [50]. Although wire bonding is a well proven method to provide interconnection to chips, other approaches are available nowadays in the microelectronics industry for chip packaging such as: Ribbon bonding, Tape Automated Bonding (TAB), and Flip-Chip (FC) bonding. This section reviews the most common interconnection technology for assembling an MCM.

2.6.1 Wire bonding

As discussed in Chapter 2 on page 13 wire bonding is the dominant chip to substrate connection method [50]. In wire bonding the chip is attached to the substrate with the pads facing away from the substrate, while bonding wires made of gold or aluminum are then attached by solid phase welding on the chip pads. The most common alternatives of the process are U/S wedge-wedge bonding of $18-32\,\mu m$ aluminum wire and T/S ball-wedge bonding of $18-32\,\mu m$ gold wire. Large wire diameters up to $500\,\mu m$ in aluminum are used to bond high power chips, while the minimum wire diameter is $7\,\mu m$ for manual bonding of microwave devices. Besides, the minimum wire diameter for automatic wire bonding determined by the lack of sensitivity in touch down sensors is $17.8\,\mu m$. The main advantages of wire bonding technology are:

- good yield method;
- well established technique;
- cost-effective for low to medium production process.

However, there are some drawbacks due to:

- slow process;
- movement of the bond-head restricted;
- high parasitic inductance limits high-frequency applications.

2.6.2 Ribbon bonding

Ribbon bonding is the same process as wedge-wedge U/S bonding with the exception that the bond wire is replaced by a rectangular section ribbon. The ribbon can be made of aluminum, silicon, or gold. Another difference between wire and ribbon bonding is the reduced material deformation in the latter (10%) compared to wire deformation ($50-220\%$).

2.6.3 Tape automated bonding

Tape Automated Bonding (TAB) is an interesting alternative to conventional wire bonding originally developed as a highly automatic technique for packaging large volume from low to high I/O devices [50, 93]. The TAB process involves bonding silicon chips to patterned metal on polymer tape using T/C bonding. Later processing is carried out in strip form through operations such as testing, encapsulation, and burn-in followed by excising of the individual packages from the tape and attachment to the substrate or board by outer lead bonding.

In TAB the chip is attached to a polymer tape prepared with copper conductors. This attachment, called the inner lead bond, is normally done at the wafer fabrication level. The copper wires are connected to the pre-bumped chips by T/C bonding, typically all in one go (gang bonding). However, this may cause cracks in the chip passivation and sometimes one and one lead is connected at the time to allow better control of the bonding.

In the assembly plant, the tape is cut is such way that the outer part of conductors (leads) is exposed. The chip assembly is then aligned and soldered (or glued) to the substrate using conductive adhesives. Normally, the cutting and bonding is done in one

operation with a tool specially designed for the chip assembly. The main advantages of TAB are:

- suited for high volume production;
- good electrical performance;
- possibility of pre-testing of chips attached to TAB frames prior to mounting into expensive packages;
- possibility to mount chips with fine pad pitch on a substrate with much larger pitch.

Furthermore, the robust nature of TAB should give consistently high bond strengths. However, there are disadvantages that are:

- expensive bonding tools;
- TAB film must be designed for every chip type;
- the chips need special bumping and metallurgy;
- cross-talk may occur at high frequency;
- high inductance of conductors;
- difficulty in maintaining satisfactory planarity.

2.6.4 Flip-chip bonding

Flip-Chip (FC) bonding comprises a range of similar interconnection techniques with in common the inverted status of the chip with respect to the substrate which have the same pad pattern as the chip [50]. This technique requires the formation of bumps onto the chip pads, which can be solder alloy balls or copper bumps in case of solder connections. Contact is made between substrate metalization and bond pad on the chip by means of a short path length of intermediary material such as solder, gold, or conductive adhesive. When solder or isotropic conductive adhesive is used, an underfill typically of epoxy is applied on two of the edges of the chip and flows under the chip by the capillary force. Figure 2.8 on the next page shows several examples of FC joints between chip and substrate.

The most widely used form of FC bonding are: T/C or T/S bonding of gold bumped chips electroplated or gold ball bumped, solder reflow by means of furnace or thermode heating, and adhesive bonding by means of either anisotropic and acrylic adhesive. The main advantages of this techniques are:

- very high I/O connections possible;
- cheap method;
- self alignment under reflow;
- suited for high-frequency devices due to the low inductance.

After all, there are some inconveniences due to:

- required extra metalizations on chips;
- fine pad pitch requires fine pitch boards;
- slow underfill process of epoxy.

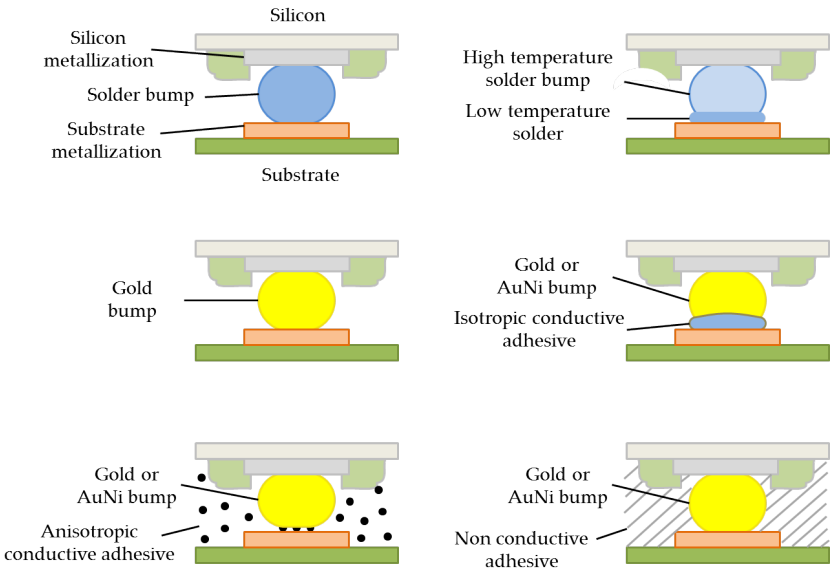


Figure 2.8: Examples of different FC joints between chip and substrate.

2.6.5 Density performance comparison

Actually, automated wire bonding technology is limited to 50 µm square bond pads at $80 - 100$ µm pitch with aluminum wedge-wedge bonding (25 µm wire). Depending upon chip size it is possible to bond to more that 240 sites around the periphery of the chip. Similar performance levels have been achieved with gold ball bonding techniques, however due to tooling and wire tolerances, the process is less tolerant of positioning errors.

Ribbon bonding is currently capable of being bonded to $40 - 50$ µm pads at 63 µm BPP using specialized bonding tools.

TAB is generally limited to an inner lead width of $40 - 75$ µm at $80 - 150$ µm BPP. Very high I/O counts are possible with area TAB although problems remain with planarity and bonding heat consistence.

Like area TAB, FC bonding offers very high interconnection density due to the arrangement of bonding pads across the whole surface of the chip. Solder bumps down to 100 µm at 200 µm BPP are in common use and work has been carried out on bumps down to 40 µm in diameter on pitches below 100 µm. However, micron bump technology is available to reduce pitches to 10 µm and devices with more than 2300 I/Os have been fabricated.

Chapter 3

Modeling of micro-magnetic components

Almost all electronic circuits require the use of inductors and transformers. These components are generally the largest, heaviest and expensive devices of a circuit. The main feature of an inductor is the capacity to store magnetic energy in the form of a magnetic field. On the other hand, the main abilities of a transformer are the capability to combine magnetic fluxes of different windings while transferring AC energy from the input to the output through the magnetic field, as well as to provide DC isolation while transmitting AC signals. The amount of energy transferred is determined by the operating frequency, flux density, and temperature. This chapter shows the basic magnetic relationships in order to analyze and design micro-magnetic components such as inductors and transformers.

3.1 Magnetic relationships

An inductor with n turns carrying an AC current $i\,(\mathrm{A})$ produces the MagnetoMotive Force (MMF) $(\mathrm{A}\,turns)$ given by:

$$\mathcal{F} = n\,i. \tag{3.1}$$

The *magnetic flux* $\phi\,(\mathrm{Wb})$ is forced to flow in a magnetic circuit by the MMF driving the magnetic circuit. The $\mathcal{F}$ is the analogous of the ElectroMotive Force (EMF) in electric circuits which causes a current circulation. Generally, the magnetic circuit is the space in which the magnetic flux flows around the coil. The *magnetic field intensity* $H\,(\mathrm{A\,m^{-1}})$ is given by:

$$H = \frac{\mathcal{F}}{l} = \frac{n\,i}{l}. \tag{3.2}$$

where $l\,(\mathrm{m})$ is the inductor length. The *magnetic flux density* $B\,(\mathrm{T})$ is given by:

$$B = \frac{\phi}{A}, \tag{3.3}$$

where $A(\mathrm{m^2})$ is the surface crossed perpendicularly by the magnetic flux ϕ. The relationship between the magnetic flux density B and the magnetic field intensity H is given by:

$$B = \mu\,H = \mu_0\,\mu_{rc}\,H, \tag{3.4}$$

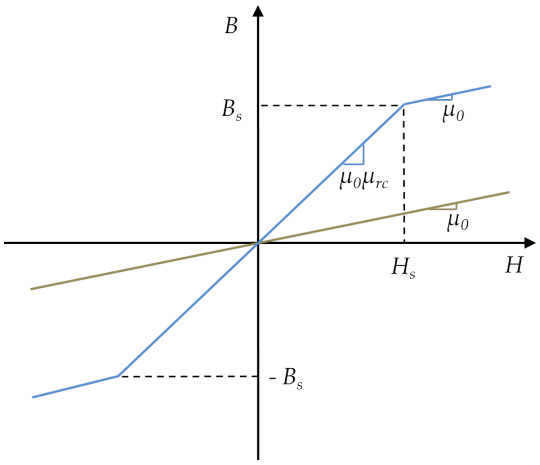


Figure 3.1: Example of $B-H$ curves for air core (linear) and magnetic core (piecewise linear approximation) micro-inductors.

where $\mu_0 = 4\,\pi \cdot 10^{-7}\,(\mathrm{H\,m^{-1}})$ is the free-space permeability, and μ_{rc} is the core relative permeability. For free space, insulators, and nonmagnetic conductors, $\mu_{rc} = 1$. For diamagnetic materials such as copper Cu, lead Pb, silver Ag, and gold Au, $\mu_{rc} \sim 1 - 10^{-5}$. However, for ferromagnetic materials such as iron Fe, cobalt Co, nickel Ni, and their alloys, $\mu_{rc} \sim 1 - 10^{6}$ [45]. The overall permeability $\mu = \mu_0\,\mu_{rc}\,(\mathrm{H\,m^{-1}})$ describes how simply a material can be magnetized because magnetic flux always follows the path with the highest permeability. For a large value of μ_{rc}, a small current produces a large flux density B.

For ferromagnetic materials, the association between B and H is non linear because the relative permeability μ_{rc} depends on H. Figure 3.1 shows two plots of the $B-H$ curve for air core and magnetic core inductors. The straight line which describes air core inductors has a constant slope μ_0, hence these inductors are linear. The piecewise linear approximation corresponds to magnetic core inductors, where $B_s\,(\mathrm{T})$ is the saturation flux density and $H_s = B_s/\mu\,(\mathrm{A\,m^{-1}})$ is the saturation field intensity. At low values of $B < B_s$, the relative permeability is high and also the slope of the $B-H$ curve $\mu_0\,\mu_{rc}$ is high, while at high values of $B > B_s$ the core saturates and $\mu_{rc} = 1$, thus reducing the slope of the $B-H$ curve to μ_0. The total peak magnetic flux density $B_{pk}\,(\mathrm{T})$ consists of both DC component $B^{DC}\,(\mathrm{T})$ and AC component $B_m\,(\mathrm{T})$ of the inductor, and should be lower than the saturation flux density B_s of a magnetic core at the highest operating temperature $T_{max}\,(^{\circ}\mathrm{C})$ as defined below:

$$B_{pk} = B^{DC} + B_m \;\leq\; B_s \quad (T_{max}), \tag{3.5}$$

where B^{DC} and B_m are given by:

$$B^{DC} = \frac{\mu\,n\,I_L}{l_c}, \tag{3.6}$$

$$B_m = \frac{\mu\,n\,I_m}{l_c}, \tag{3.7}$$

where $I_L\,(\mathrm{A})$ and $I_m\,(\mathrm{A})$ are the amplitudes of the DC and AC components of the inductor current, respectively, while $l_c(\mathrm{m})$ is the mean Magnetic Path Length (MPL)

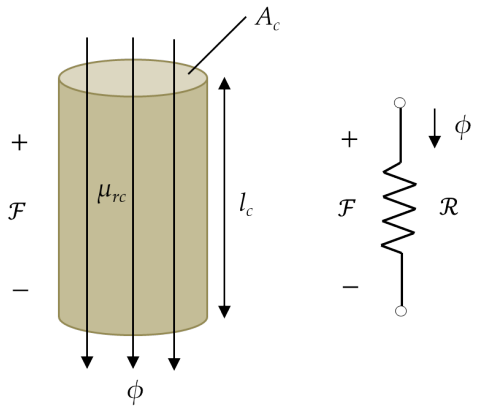


Figure 3.2: Basic magnetic element conducting magnetic flux (left) and equivalent magnetic circuit (right).

which is the mean length of the closed path that the magnetic flux flows around the magnetic circuit.

The *magnetic flux linkage* $\lambda\,(\mathrm{Wb}\,turns)$ is the sum of the flux contained by each turn of wire encompassing the magnetic core, and is described by:

$$\lambda = n\,\phi = n\,A_c\,B = n\,A_c\,\mu\,H = \frac{\mu\,A_c\,n^2\,i}{l_c}, \tag{3.8}$$

where $A_c(\mathrm{m}^2)$ is the cross-sectional area of the core crossed by the magnetic flux.

3.2 Reluctance definition

The inductance of an inductor depends on the winding geometry, core geometry, permeability of the core, and frequency of operation [25, 45]. The *reluctance* $\mathcal{R}$ $(turns/\mathrm{H})$ is the resistance of the core to the flow of the magnetic flux ϕ, similarly to the way in which the resistance $R\,(\Omega)$ opposes the electric current flow. The concept of reluctance can be expressed by Figure 3.2 which shows the basic magnetic element and the equivalent magnetic circuit. The reluctance of a basic magnetic element is given by:

$$\mathcal{R} = \frac{l_c}{\mu\,A_c}. \tag{3.9}$$

A poor conductor of magnetic flux has a high reluctance. The magnetic Ohm's law is expressed as:

$$\phi = \frac{\mathcal{F}}{\mathcal{R}} = \frac{\mu\,n\,i\,A_c}{l_c}. \tag{3.10}$$

Figure 3.3 on the following page shows an example of inductor and the corresponding equivalent magnetic circuit.

3.3 Core saturation

For a magnetic core inductor the saturation magnetic flux $\phi_s\,(\mathrm{Wb})$ is given by:

$$\phi_s = A_c\,B_s, \tag{3.11}$$

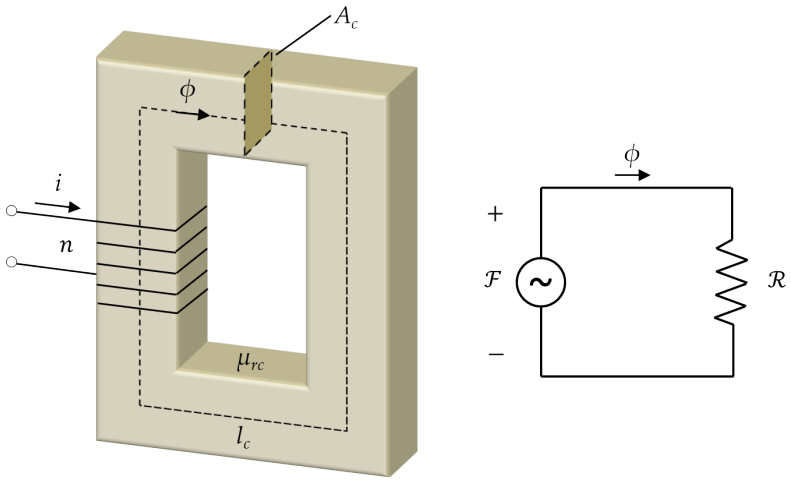


Figure 3.3: Example of inductor composed by a core and a coil (left) and equivalent magnetic circuit (right).

while the saturation flux density can be expressed as:

$$B_s = \mu\, H_s = \mu\, \frac{n\, I_{sat}}{l_c}, \tag{3.12}$$

where I_{sat} (A) is the maximum amplitude of the inductor current at which the core saturates [45]. Hence, in order to avoid core saturation the ampere-turn limit is extracted by:

$$(n\, I_{sat}) \leq B_s\, A_c\, \mathcal{R}. \tag{3.13}$$

Therefore, by considering a sinusoidal waveform $v_L = V_L \sin(2\,\pi\, f\, t)$ (V) applied to an inductor with maximum amplitude V_{Lmax} (V), the lowest frequency f_{min} (Hz) at which an inductor can operate without saturating the core is given by:

$$f_{min} = \frac{V_{Lmax}}{2\,\pi\, n\, A_c\, B_s}. \tag{3.14}$$

The minimum cross-sectional area A_{cmin} (m^2) of the core to avoid saturation is:

$$A_{cmin} = \frac{V_{Lmax}}{2\,\pi\, n\, f\, B_s}. \tag{3.15}$$

3.4 Design of inductors

A method for calculating the inductance L (H) of an inductor is the use of the core reluctance $\mathcal{R}$ as follows:

$$L = \frac{n^2}{\mathcal{R}} = \frac{\mu_0\, \mu_{rc}\, n^2\, A_c}{l_c}. \tag{3.16}$$

If the number of turns n is equal to 1, the inductance $L = 1/\mathcal{R}$. Moreover, by including (3.8) into (3.16) it follows:

$$L = \frac{\lambda}{i}. \tag{3.17}$$

The reluctance method allows to obtain several inductance expressions for various types of core.

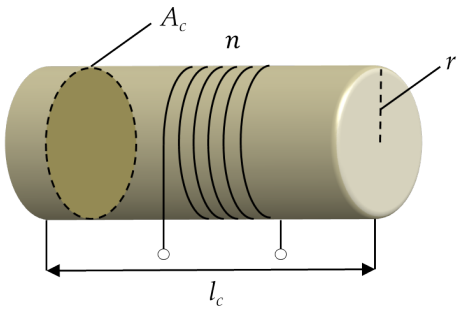


Figure 3.4: Example of short solenoid inductor.

3.4.1 Solenoid inductor

The inductance of a long solenoid L_∞ (H) at low frequencies is given by:

$$L_\infty = \frac{\mu_0\,\mu_{rc}\,n^2\,A_c}{l_c} = \frac{\mu_0\,\mu_{rc}\,n^2\,r^2\,\pi}{l_c} = \frac{n^2}{\mathcal{R}}, \tag{3.18}$$

where $A_c = \pi\,r^2$, r (m) is the mean coil radius, and l_c is the mean core length. On the other hand, the inductance L of a single-layer solenoid of length l_c can be estimated by the following expression [101] which is valid for $r/l_c < 1.25$:

$$L = \frac{L_\infty}{1 + 0.9\,\dfrac{r}{l_c}} = \frac{\mu_0\,\mu_{rc}\,n^2\,A_c}{l_c(1 + 0.9\,\dfrac{r}{l_c})} = \frac{\mu_0\,\mu_{rc}\,n^2\,r^2\,\pi}{l_c + 0.9\,r}, \quad \text{for} \quad r/l_c < 1.25. \tag{3.19}$$

The inductance of the short solenoid is smaller than that of the infinitely long round solenoid. As r/l_c increases, $K = L/L_\infty$ decreases. Figure 3.4 shows an example of a finite length solenoid.

3.4.2 Toroidal inductor

A toroidal inductor can be seen as a finite length solenoid closed on itself to form a toroid shape. The low-frequency inductance of a tightly wounded toroidal inductor with a round cross section can be described by [45]:

$$L = \frac{\mu_0\,\mu_{rc}\,n^2\,A_c}{l_c} = \frac{\mu_0\,\mu_{rc}\,n^2\,A_c}{2\,\pi\,r} = \frac{\mu_0\,\mu_{rc}\,n^2\,(D_o - D_i)^2}{8\,(D_o + D_i)} = \frac{n^2}{\mathcal{R}}, \tag{3.20}$$

where $r = (D_o + D_i)/4$ (m) is the mean radius of the core with D_o (m) and D_i (m) as the outer and inner core diameters, while $A_c = \pi\,(D_o - D_i)^2/16$ and $l_c = 2\,\pi\,r = \pi\,(D_o + D_i)/2$. Similarly, the inductance expression for a toroidal inductor with rectangular cross section is given by [45]:

$$L = \frac{\mu_0\,\mu_{rc}\,n^2\,A_c}{l_c} = \frac{\mu_0\,\mu_{rc}\,n^2\,A_c}{2\,\pi\,r} = \frac{\mu_0\,\mu_{rc}\,n^2\,t_c\,(D_o - D_i)}{\pi\,(D_o + D_i)} = \frac{n^2}{\mathcal{R}}, \tag{3.21}$$

where $A_c = t_c\,(D_o - D_i)/2$ with t_c (m) as the core thickness and $l_c = 2\,\pi\,r = \pi\,(D_o + D_i)/2$. Figure 3.5 on the following page shows an example of a toroidal inductor with rectangular cross section.

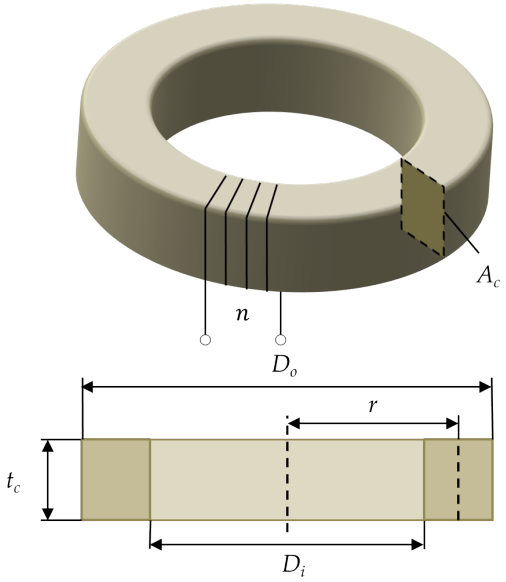


Figure 3.5: Example of toroidal inductor with rectangular cross section.

3.4.3 Air gap and inductance factor

The overall reluctance can be controlled by introducing an air gap in the core. In a gapped core, a small section of magnetic flux path is replaced by a nonmagnetic material such as air or nylon [45]. In fact, adding an air gap in a core is equivalent to include a large gap reluctance $\mathcal{R}_g$ $(turns/\mathrm{H})$ in the magnetic circuit shows in Figure 3.3 on page 30 in series with the core reluctance $\mathcal{R}_c$ $(turns/\mathrm{H})$. This is analogous to add a large series resistor in an electric circuit to reduce the magnitude of the current at a fixed source voltage. The low-frequency inductance of a coil with an air gap of length l_g (m) is given by [45]:

$$L = \frac{n^2}{\mathcal{R}} = \frac{n^2}{\mathcal{R}_g + \mathcal{R}_c} = \frac{n^2}{\dfrac{l_g}{\mu_0\, A_c} + \dfrac{l_c}{\mu_0\, \mu_{rc}\, A_c}} = \frac{\mu_0\, \mu_{rc}\, n^2\, A_c}{l_c + \mu_{rc}\, l_g} = \frac{\mu_0\, \mu_{rc}\, n^2\, A_c}{l_c\, F_g}, \tag{3.22}$$

where $\mathcal{R} = \mathcal{R}_c + \mathcal{R}_g$ is the overall reluctance composed by air gap $\mathcal{R}_g$ and core $\mathcal{R}_c$ reluctances expressed as:

$$\mathcal{R}_g = \frac{l_g}{\mu_0\, A_c}, \tag{3.23}$$

$$\mathcal{R}_c = \frac{l_c - l_g}{\mu_0\, \mu_{rc}\, A_c} \approx \frac{l_c}{\mu_0\, \mu_{rc}\, A_c}. \tag{3.24}$$

The air gap factor F_g can be defined as:

$$F_g = \frac{\mathcal{R}}{\mathcal{R}_c} = \frac{\mathcal{R}_c + \mathcal{R}_g}{\mathcal{R}_c} = 1 + \frac{\mathcal{R}_g}{\mathcal{R}_c} = 1 + \frac{\mu_{rc}\, l_g}{l_c}, \tag{3.25}$$

while the effective relative permeability μ_{re} of the core becomes:

$$\mu_{re} = \frac{\mu_{rc}}{1 + \frac{\mu_{rc}\, l_g}{l_c}} = \frac{\mu_{rc}}{F_g}. \tag{3.26}$$

An air gap causes a substantial decrease in the effective relative permeability, however it produces a more stable permeability and reluctance, resulting in a more predictable inductance.

The classic equation (3.16) can be rewritten as:

$$L = \frac{n^2}{\mathcal{R}} = \frac{\mu_0\, \mu_{rc}\, n^2\, A_c}{l_c} = A_L\, n^2, \tag{3.27}$$

where A_L (H/*turns*) is the core inductance factor defined by:

$$A_L = \frac{L}{n^2} = \frac{\mu_0\, \mu_{rc}\, A_c}{l_c} = \frac{1}{\mathcal{R}}. \tag{3.28}$$

Each core of different materials, shapes, and sizes have a unique value of A_L, thus it can be used to predict the desired inductance of an inductor from the core material characteristics [45].

3.5 Design of transformers

Transformers are widely used in power electronics to step down or step up the AC voltage to a level appropriate for low-voltage or high-voltage circuits, respectively. A transformer is a system of two or more reciprocally coupled coils, which share a common magnetic flux wounded on the same core. Generally, the main function of a transformer can be summarized as:

- modify the level of AC voltages and currents;
- reverse voltage or current waveforms;
- transform impedance;
- provide DC electrical isolation;
- store and transfer magnetic energy.

This section shows the basic relationships for the design and the modeling of transformers.

3.5.1 Ideal transformer

A two-winding transformer is realized by wrapping two coils on the same magnetic core [25, 45]. The first coil has n_1 turns and is referred as the *primary winding*, while the second coil has n_2 turns and is referred as the *secondary winding*. A time varying current i_1 (A) in the primary coil produces a magnetic flux in both windings, which induces a voltage v_2 (V) over the secondary winding. The polarity of the mutual induced voltage depends on the way the coils are wounded in relation to the reference direction of coil currents indicated by the dot convention. Hence, transformers can be

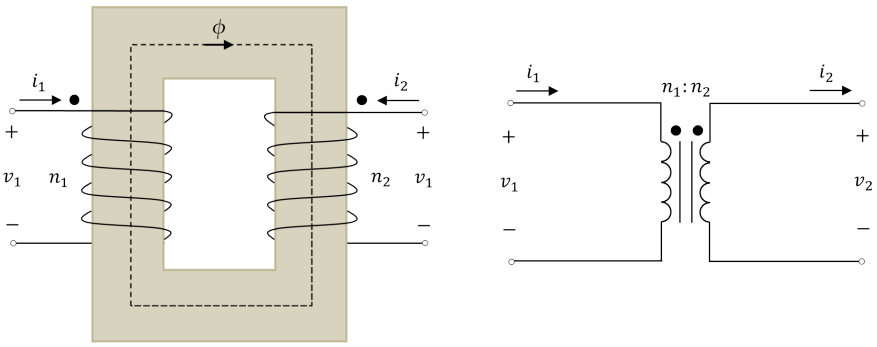


Figure 3.6: Example of non inverting two-winding transformer (left) and circuit symbol (right) with dot convention.

inverting and non inverting. Figure 3.6 shows an example of non inverting two-winding transformer with the corresponding circuit symbol.

For an ideal transformer, the core has infinite resistivity ($\rho_c \sim \infty$), infinite permeability ($\mu_{rc} \sim \infty$), zero core reluctance ($\mathcal{R} \sim 0$), infinite bandwidth, while the magnetic field is confined within the core and it is linked to both windings. The primary coil is usually connected to an AC voltage source v_1 (V) while the secondary coil is connected to a load resistor R_L (Ω). The input voltage v_1 generates the current i_1 in the primary coil, which establishes a magnetic flux ϕ. This magnetic flux is related to the input voltage v_1 by Faraday's law:

$$v_1 = n_1 \frac{d\,\phi}{dt}. \tag{3.29}$$

The variations in the magnetic flux induce an output voltage v_2 over the secondary coil again according to Faraday's law:

$$v_2 = n_2 \frac{d\,\phi}{dt}, \tag{3.30}$$

which causes the output current i_2 (A) equal to $i_2 = v_2/R_L$ to flow. The voltage transfer function of the transformer is equal to the *turns ratio* n_{12} given by:

$$n_{12} = \frac{v_2}{v_1} = \frac{n_2 \dfrac{d\,\phi}{dt}}{n_1 \dfrac{d\,\phi}{dt}} = \frac{n_2}{n_1}. \tag{3.31}$$

An ideal transformer is lossless and all of the instantaneous power provided by the input source $p_1 = i_1\, v_1$ (W) is delivered to the load resistor as the output instantaneous power $p_2 = i_2\, v_2$ (W), thus:

$$p_2 = i_2\, v_2 = p_1 = i_1\, v_1, \tag{3.32}$$

resulting in:

$$n_{12} = \frac{v_2}{v_1} = \frac{i_1}{i_2} = \frac{n_2}{n_1}. \tag{3.33}$$

Hence, we get the following set of equations using dependent voltage and current sources:

$$v_2 = n_{12}\, v_1, \tag{3.34}$$

$$i_1 = n_{12}\, i_2, \tag{3.35}$$

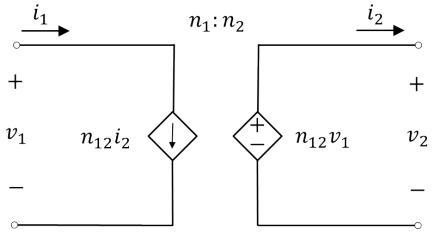


Figure 3.7: Circuit model of an ideal lossless transformer.

which represents the circuit model of an ideal lossless transformer, as shown in Figure 3.7. Since $v_2 = R_L\, i_2$, $v_1 = v_2/n_{12} = R_L\, i_2/n_{12}$, and $i_1 = n_{12}\, i_2$, the transformer input resistance $R_i\,(\Omega)$ is given by:

$$R_i = \frac{v_1}{i_1} = \frac{R_L\, i_2/n_{12}}{n_{12}\, i_2} = \frac{R_L}{n_{12}^2}. \tag{3.36}$$

Generally, a voltage transformer should never be used with a short circuit at the output. Referring to Figure 3.6 on the facing page, from Ampère's law the magnetic flux ϕ is given by:

$$\phi = \frac{n_1\, i_1 - n_2\, i_2}{\mathcal{R}}, \tag{3.37}$$

where the core reluctance $\mathcal{R}$ is:

$$\mathcal{R} = \frac{l_c}{\mu_0\, \mu_{rc}\, A_c}. \tag{3.38}$$

For an ideal transformer ($\mathcal{R} = 0$, $\mu_{rc} = \infty$), equation (3.37) becomes:

$$n_1\, i_1 - n_2\, i_2 = 0, \tag{3.39}$$

yielding the turns ratio $n = n_2/n_1 = i_1/i_2$ obtained in (3.33).

3.5.2 Real transformer

The total magnetic flux ϕ of a transformer consists of a *mutual flux* $\phi_m\,(\text{Wb})$ and a *leakage flux* $\phi_l\,(\text{Wb})$ expressed as:

$$\phi = \phi_m + \phi_l = \phi_m + \phi_{l1} + \phi_{l2}, \tag{3.40}$$

where $\phi_{l1}\,(\text{Wb})$ and $\phi_{l2}\,(\text{Wb})$ are the leakage fluxes on the primary and secondary side, respectively. The mutual flux ϕ_m of a two-winding transformer is the piece of the total flux which is common with both coils, while the leakage flux ϕ_l is the piece of the total flux which does not link both coils [45].

In order to analyze the behavior of a real lossy transformer, we start to consider a two-winding transformer driven by an AC current source i_1 with an open circuit at the output. The current through the secondary coil is zero ($i_2 = 0\,\text{A}$) and does not induce any magnetic flux. The AC current i_1 circulating in the primary induces a magnetic flux $\phi_{11}\,(\text{Wb})$ in the primary coil, which in turn induces an AC voltage v_1 over the primary coil. The magnetic flux produced by current i_1 consists of a *mutual flux* $\phi_{21}\,(\text{Wb})$ and a *primary leakage flux* $\phi_{l1}\,(\text{Wb})$, as shown below:

$$\phi_{11} = \phi_{l1} + \phi_{21}. \tag{3.41}$$

The mutual flux ϕ_{21} links both primary and secondary side, while the primary leakage flux ϕ_{l1} links only the turns of the primary coil. The flux linkage of the primary winding $\lambda_1\,(\mathrm{Wb}\,turns)$ is given by:

$$\lambda_1 = n_1\,\phi_{11} = L_{11}\,i_1, \tag{3.42}$$

where $L_{11} = n_1^2/\mathcal{R}\,(\mathrm{H})$ is the *self-inductance* of the primary winding, which can be expressed as:

$$L_{11} = \frac{\lambda_1}{i_1} = \frac{n_1\,\phi_{11}}{i_1} = \frac{n_1\,\phi_{l1}}{i_1} + \frac{n_1\,\phi_{21}}{i_1} = L_{l1} + M_{21}, \tag{3.43}$$

where $L_{l1}\,(\mathrm{H})$ is the *leakage inductance* of the primary coil, and $M_{21}\,(\mathrm{H})$ is the *mutual inductance* of the coupled coils. From Faraday's law the self-induced voltage at the primary side v_1 by current i_1 is:

$$v_1 = \frac{d\,\lambda_1}{dt} = \frac{d\,(L_{11}\,i_1)}{dt} = L_{11}\,\frac{d\,i_1}{dt}. \tag{3.44}$$

The flux linkage $\lambda_{21}\,(\mathrm{Wb}\,turns)$ of the secondary winding (in linear transformers) is equal to:

$$\lambda_{21} = n_2\,\phi_{21} = M_{21}\,i_1. \tag{3.45}$$

Hence, from Faraday's law the voltage across the secondary side v_2 is expressed as:

$$v_2 = \frac{d\,\lambda_{21}}{dt} = \frac{d\,(M_{21}\,i_1)}{dt} = M_{21}\,\frac{d\,i_1}{dt}. \tag{3.46}$$

Now we consider an AC current source i_2 in series with the secondary coil and an open circuit ($i_1 = 0\,\mathrm{A}$) across the primary winding. The AC current i_2 circulating in the secondary induces a magnetic flux $\phi_{22}\,(\mathrm{Wb})$ in the secondary coil, which in turn induces an AC voltage v_2. The magnetic flux ϕ_{22} is equal to the mutual flux $\phi_{12}\,(\mathrm{Wb})$ linking both primary and secondary side and the secondary leakage flux $\phi_{l2}\,(\mathrm{Wb})$ linking only the secondary coil, as shown below:

$$\phi_{22} = \phi_{l2} + \phi_{12}. \tag{3.47}$$

The flux linkage of the secondary winding $\lambda_2\,(\mathrm{Wb}\,turns)$ is given by:

$$\lambda_2 = n_2\,\phi_{22} = L_{22}\,i_2, \tag{3.48}$$

where $L_{22} = n_2^2/\mathcal{R}\,(\mathrm{H})$ is the *self-inductance* of the secondary winding, which can be expressed as:

$$L_{22} = \frac{\lambda_2}{i_2} = \frac{n_2\,\phi_{22}}{i_2} = \frac{n_2\,\phi_{l2}}{i_2} + \frac{n_2\,\phi_{12}}{i_2} = L_{l2} + M_{12}, \tag{3.49}$$

where $L_{l2}\,(\mathrm{H})$ is the *leakage inductance* of the secondary coil, and $M_{12}\,(\mathrm{H})$ is the *mutual inductance* of the coupled coils. Again from Faraday's law, the self-induced voltage at the secondary side v_2 by current i_2 is:

$$v_2 = \frac{d\,\lambda_2}{dt} = \frac{d\,(L_{22}\,i_2)}{dt} = L_{22}\,\frac{d\,i_2}{dt}. \tag{3.50}$$

The flux linkage $\lambda_{12}\,(\mathrm{Wb}\,turns)$ of the primary winding (in linear transformers) is equal to:

$$\lambda_{12} = n_1\,\phi_{12} = M_{12}\,i_2. \tag{3.51}$$

Hence, from Faraday's law the voltage across the primary side v_1 is:

$$v_1 = \frac{d\,\lambda_{12}}{dt} = \frac{d\,(M_{12}\,i_2)}{dt} = M_{12}\,\frac{d\,i_2}{dt}. \tag{3.52}$$

From the reciprocity principle, we can assume that:

$$\phi_{21} = \phi_{12} = \phi, \tag{3.53}$$

$$M_{21} = M_{12} = M. \tag{3.54}$$

Finally, we analyze a two-winding transformer with an AC current source i_1 linked to the primary side and an AC current source i_2 connected to the secondary side. From the superposition principle, we can extract the magnetic flux in the primary coil ϕ_1 (Wb) induced by currents i_1 and i_2 as:

$$\phi_1 = \phi_{l1} + \phi_{21} + \phi_{12} = \phi_{11} + \phi_{12}, \tag{3.55}$$

resulting in the flux linkage in the primary coil:

$$\lambda_1 = n_1\,\phi_1 = n_1\,\phi_{11} + n_1\,\phi_{12} = L_{11}\,i_1 + M_{12}\,i_2, \tag{3.56}$$

and the voltage across the primary coil:

$$v_1 = \frac{d\,\lambda_1}{dt} = n_1\,\frac{d\,\phi_{11}}{dt} + n_1\,\frac{d\,\phi_{12}}{dt} = L_{11}\,\frac{d\,i_1}{dt} + M\,\frac{d\,i_2}{dt}. \tag{3.57}$$

Hence, the voltage over the primary inductance is the sum of the voltage due to the primary winding self-inductance and the voltage due to the mutual inductance. Similarly, we can extract the magnetic flux in the secondary coil ϕ_2 (Wb) induced by currents i_1 and i_2 as:

$$\phi_2 = \phi_{l2} + \phi_{12} + \phi_{21} = \phi_{22} + \phi_{21}, \tag{3.58}$$

yielding the flux linkage in the secondary coil:

$$\lambda_2 = n_2\,\phi_2 = n_2\,\phi_{21} + n_2\,\phi_{22} = M_{21}\,i_1 + L_{22}\,i_2, \tag{3.59}$$

and the voltage across the secondary coil:

$$v_2 = \frac{d\,\lambda_2}{dt} = n_2\,\frac{d\,\phi_{22}}{dt} + n_2\,\frac{d\,\phi_{21}}{dt} = L_{22}\,\frac{d\,i_2}{dt} + M\,\frac{d\,i_1}{dt}. \tag{3.60}$$

Hence, the voltage across the secondary inductance is the sum of the voltage due to the secondary winding self-inductance and the voltage due to the mutual inductance. Figure 3.8 on the next page shows the circuit model of a real lossy transformer.

3.5.3 Mutual inductance

By assuming that the current i_1 circulates within the primary coil, while some of which passes across the secondary coil, the mutual inductance M (H) is given by:

$$M = \frac{\lambda_{21}}{i_1} = \frac{n_2\,\phi_{21}}{i_1} = \frac{\lambda_{12}}{i_2} = \frac{n_1\,\phi_{12}}{i_2}. \tag{3.61}$$

The mutual magnetic flux ϕ_{21} created by the current i_1 is expressed as:

$$\phi_{21} = \frac{\mu_0\,\mu_{rc}\,n_2\,A_c\,i_1}{l_c} = \frac{n_2\,i_1}{\mathcal{R}}, \tag{3.62}$$

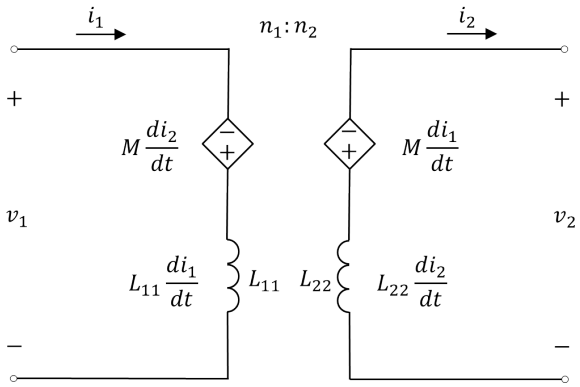


Figure 3.8: Circuit model of a real lossy transformer.

while the flux linkage λ_{21} is:

$$\lambda_{21} = n_1\,\phi_{21} = \frac{\mu_0\,\mu_{rc}\,n_1\,n_2\,A_c\,i_1}{l_c} = \frac{n_1\,n_2}{\mathcal{R}}\,i_1, \tag{3.63}$$

and the mutual inductance M_{21} between the windings is given by:

$$M_{21} = \frac{\lambda_{21}}{i_1} = \frac{n_1\,n_2}{\mathcal{R}}. \tag{3.64}$$

Similarly, the mutual magnetic flux ϕ_{12} generated by the current i_2 is expressed as:

$$\phi_{12} = \frac{\mu_0\,\mu_{rc}\,n_1\,A_c\,i_2}{l_c} = \frac{n_1\,i_2}{\mathcal{R}}, \tag{3.65}$$

while the flux linkage λ_{12} is:

$$\lambda_{12} = n_2\,\phi_{12} = \frac{\mu_0\,\mu_{rc}\,n_1\,n_2\,A_c\,i_2}{l_c} = \frac{n_1\,n_2}{\mathcal{R}}\,i_2, \tag{3.66}$$

and the mutual inductance M_{12} between the windings is given by:

$$M_{12} = \frac{\lambda_{12}}{i_2} = \frac{n_1\,n_2}{\mathcal{R}}. \tag{3.67}$$

Finally, by comparing (3.67) and (3.64) we obtain that $M_{12} = M_{21} = M$.

If we assume that $L_{l1} = 0$ and $L_{l2} = 0$, the self-inductances of both primary and secondary sides are given by:

$$L_{11} = \frac{\mu_0\,\mu_{rc}\,n_1^2\,A_c}{l_c} = \frac{n_1^2}{\mathcal{R}}, \tag{3.68}$$

$$L_{22} = \frac{\mu_0\,\mu_{rc}\,n_2^2\,A_c}{l_c} = \frac{n_2^2}{\mathcal{R}}. \tag{3.69}$$

Extracting n_1 and n_2 from (3.68) and (3.69), respectively, and substituting them into (3.67), we get:

$$M = \sqrt{L_{11}\,L_{22}} = \frac{n_1\,n_2}{\mathcal{R}}. \tag{3.70}$$

The mutual inductance is proportional to the geometric mean of the self-inductances. Now, if we combine (3.68) and (3.69), we obtain the turns ratio n_{12} of the two windings by:

$$n_{12} = \frac{n_2}{n_1} = \sqrt{\frac{L_{22}}{L_{11}}}. \tag{3.71}$$

3.5.4 Coupling coefficient

Generally, not all flux produced by the primary coil is combined to the secondary coil. In order to analyze this leakage the *coupling coefficient* of the primary winding k_1 can be defined by:

$$k_1 = \frac{\phi_{21}}{\phi_{11}} = \frac{\phi_{21}}{\phi_{l1} + \phi_{21}} = \frac{\dfrac{n_1\,\phi_{21}}{i_1}}{\dfrac{n_1\,\phi_{11}}{i_1}} = \frac{M_{21}}{L_{11}} = \frac{L_{11} - L_{l1}}{L_{11}}. \tag{3.72}$$

Hence, the leakage inductance of the primary coil L_{l1} is:

$$L_{l1} = (1 - k_1)\,L_{11}. \tag{3.73}$$

Similarly, the *coupling coefficient* of the secondary winding k_2 can be defined by:

$$k_2 = \frac{\phi_{12}}{\phi_{22}} = \frac{\phi_{12}}{\phi_{l2} + \phi_{12}} = \frac{\dfrac{n_2\,\phi_{12}}{i_2}}{\dfrac{n_2\,\phi_{22}}{i_2}} = \frac{M_{12}}{L_{22}} = \frac{L_{22} - L_{l2}}{L_{22}}. \tag{3.74}$$

Thus, the leakage inductance of the secondary coil L_{l2} is:

$$L_{l2} = (1 - k_2)\,L_{22}. \tag{3.75}$$

Since $M_{12} = M_{21} = M$, the coupling coefficient k of a transformer can be expressed as:

$$k = \sqrt{k_1\,k_2} = \sqrt{\frac{M_{21}}{L_{11}}\,\frac{M_{12}}{L_{22}}} = \frac{M}{\sqrt{L_{11}\,L_{22}}}. \tag{3.76}$$

Generally, if the windings have the same number of turns $k_1 = k_2 = k$, otherwise k_1 is not always equal to k_2. The coupling coefficient $k\,(0 \leq k \leq 1)$ is a measure of the magnetic coupling between the coils. When the two coils are tightly coupled $k = 1$, while if the windings are loosely coupled $k \ll 1$.

3.5.5 Magnetizing inductance

Consider a two-winding transformer with a perfect coupling between coils ($\phi_l = 0$), and a nonzero core reluctance ($\mathcal{R} > 0$, $\mu_{rc} < \infty$). Referring to Figure 3.6 on page 34, from Ampère's law the magnetic flux ϕ is given by:

$$\phi = \frac{n_1\,i_1 - n_2\,i_2}{\mathcal{R}} = \frac{n_1}{\mathcal{R}}\Big(i_1 - \frac{n_2\,i_2}{n_1}\Big) = \frac{n_1}{\mathcal{R}}\Big(i_1 - n_{12}\,i_2\Big). \tag{3.77}$$

Since $\lambda_1 = n_1\,\phi$, the primary voltage v_1 is:

$$v_1 = \frac{d\,\lambda_1}{dt} = n_1\,\frac{d\,\phi}{dt} = n_1\,\frac{d}{dt}\Big(\frac{n_1}{\mathcal{R}}\Big(i_1 - n_{12}\,i_2\Big)\Big) = \frac{n_1^2}{\mathcal{R}}\,\frac{d}{dt}\Big(i_1 - n_{12}\,i_2\Big) = L_m\,\frac{d\,i_{Lm}}{dt}, \tag{3.78}$$

where the *magnetizing inductance* on the primary side L_m (H) is:

$$L_m = \frac{n_1^2}{\mathcal{R}}, \tag{3.79}$$

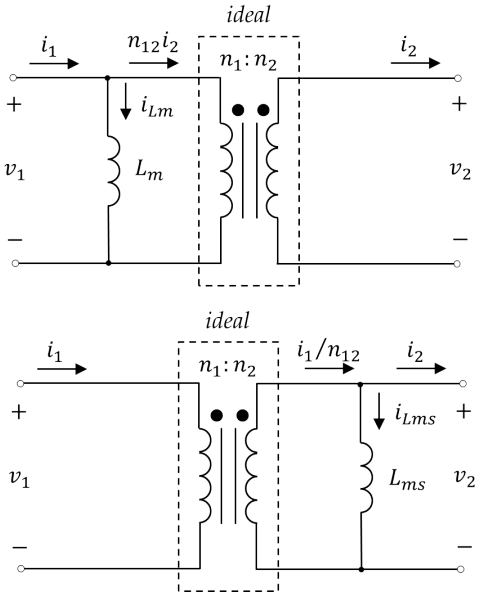


Figure 3.9: Circuit models of a transformer with perfect coupling and finite magnetizing inductance: referred to the primary side (top), and referred to the secondary side (bottom).

and the *magnetizing current* in the primary side i_{Lm} (A) is:

$$i_{Lm} = i_1 - n_{12}\, i_2. \tag{3.80}$$

The top circuit of Figure 3.9 shows the equivalent circuit of the transformer with the magnetizing inductance on the primary side. For an ideal transformer with a zero core reluctance, the magnetizing inductance approaches infinity ($L_m = \infty$).

Similarly, from Ampère's law the magnetic flux ϕ can also be expressed as:

$$\phi = \frac{n_1\, i_1 - n_2\, i_2}{\mathcal{R}} = \frac{n_2}{\mathcal{R}}\Big(\frac{n_1\, i_1}{n_2} - i_2\Big) = \frac{n_2}{\mathcal{R}}\Big(\frac{i_1}{n_{12}} - i_2\Big). \tag{3.81}$$

Since $\lambda_2 = n_2\, \phi$, the secondary voltage v_2 is:

$$\begin{aligned} v_2 = \frac{d\,\lambda_2}{dt} = n_2\,\frac{d\,\phi}{dt} = n_2\,\frac{d}{dt}\Big(\frac{n_2}{\mathcal{R}}\Big(\frac{i_1}{n_{12}} - i_2\Big)\Big) = \frac{n_2^2}{\mathcal{R}}\,\frac{d}{dt}\Big(\frac{i_1}{n_{12}} - i_2\Big) \\ = L_{ms}\,\frac{d\,i_{Lms}}{dt}, \end{aligned} \tag{3.82}$$

where the *magnetizing inductance* on the secondary side L_{ms} (H) is:

$$L_{ms} = \frac{n_2^2}{\mathcal{R}} = L_m\, n_{12}^2, \tag{3.83}$$

and the *magnetizing current* in the secondary side i_{Lms} (A) is:

$$i_{Lms} = \frac{i_1}{n_{12}} - i_2. \tag{3.84}$$

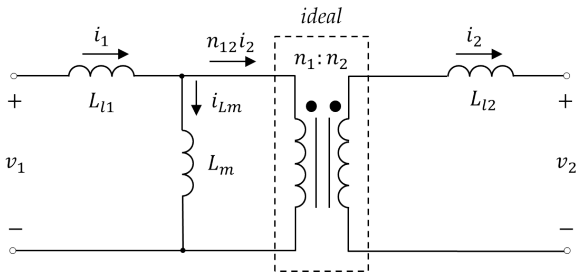


Figure 3.10: Circuit model of a real transformer with nonperfect coupling and finite magnetizing inductance on the primary side.

The bottom circuit of Figure 3.9 on the facing page shows the equivalent circuit of the transformer with the magnetizing inductance on the secondary side. Finally we can extract the mutual inductance M by combining (3.79) and (3.83) with equation (3.70) as:

$$M = \frac{n_1\, n_2}{\mathcal{R}} = L_m\, n_{12} = \frac{L_{ms}}{n_{12}}. \tag{3.85}$$

Therefore, we obtain the magnetizing inductances on the primary and secondary side, respectively, as follows:

$$L_m = \frac{M}{n_{12}}, \tag{3.86}$$

$$L_{ms} = M\, n_{12}. \tag{3.87}$$

3.5.6 Complete model

As discussed in subsection 3.5.4 on page 39, in a real transformer not all magnetic flux induced by one coil links the other coil ($\phi_l > 0$), hence $k < 1$. In fact, there is a magnetic flux induced by one coil in the space between the layers, in the space between the winding and the core, and within the conductors. This effect can be modeled by leakage inductances. Several methods allow to increase the coupling coefficient like the use of wide and flat coils with minimum insulation, and the use of interleaved windings. Furthermore the coils of toroidal inductors or transformers should cover almost the entire magnetic path [45]. In addition, as discussed in subsection 3.5.5 on page 39, in a real transformer the core reluctance in nonzero ($\mathcal{R} > 0$) depending on the value of the relative permeability ($\mu_{rc} < \infty$). Figure 3.10 shows the complete equivalent circuit of a real transformer with the magnetizing inductance on the primary side and the leakage inductances. The coupling coefficient is given by:

$$k = \frac{M}{\sqrt{L_{11}\, L_{22}}}, \tag{3.88}$$

where the self-inductances are:

$$L_{11} = L_{l1} + L_m, \tag{3.89}$$

$$L_{22} = L_{l2} + L_{ms}. \tag{3.90}$$

Hence, the leakage inductances are given by:

$$L_{l1} = L_{11}\,(1 - k), \tag{3.91}$$

$$L_{l2} = L_{22}\,(1 - k), \tag{3.92}$$

and the magnetizing inductances are:

$$L_m = k\,L_{11} = \frac{M}{n_{12}}, \tag{3.93}$$

$$L_{ms} = k\,L_{22} = M\,n_{12}, \tag{3.94}$$

where the turns ratio n_{12} is:

$$n_{12} = \frac{n_2}{n_1} = \sqrt{\frac{L_{22}}{L_{11}}}. \tag{3.95}$$

In order to get the voltages over the windings, the coupling coefficient k has to be taken into account in (3.95) thus getting the *effective turns ratio* n_e expressed as:

$$n_e = k\,n_{12} = k\sqrt{\frac{L_{22}}{L_{11}}}. \tag{3.96}$$

3.6 Losses and high-frequency design

This section describes the type of power losses in the core and the winding, and shows the high-frequency circuit models of inductors and transformers. Impedance measurement techniques are shown to calculate the main transformer parameters. Finally, the lamination of the magnetic core is analyzed to overcome high-frequency effects.

3.6.1 Core losses

Core losses are the major restrictions in the design of micro-magnetics at high frequency. They are of two types: *hysteresis loss* and *eddy-current loss*. Hysteresis loss represents the energy used to arrange and twist the magnetic moments of the core material. This energy is wasted in the core material as heat. A good magnetic material will have a large permeability, but a very narrow hysteresis loop. For instance, soft iron cores satisfy this condition thus resulting suitable for high-frequency applications, while hard steel cores have wider hysteresis loop which causes larger hysteresis loss. Eddy current loss is due to eddy currents because a time varying magnetic field induces a voltage which produces circulating currents. These currents follow circular paths normal to the direction of the magnetic flux, and produce a secondary magnetic field which opposes the original applied magnetic field. A higher resistivity core material has lower eddy current loss. Eddy-current loss, as hysteresis loss, causes heating of the core [45].

The *total power loss density in the core* $P_v\,(\mathrm{W\,cm^{-3}})$ due to both hysteresis and eddy-current losses, can be described by Steinmetz equation [84, 85] as follows:

$$P_v = P_h + P_{ev} = k_c\,f_{op}^{a}\,B_m^{b}, \tag{3.97}$$

where $P_h\,(\mathrm{W\,cm^{-3}})$ and $P_{ev}\,(\mathrm{W\,cm^{-3}})$ are the hysteresis and eddy-current power loss density, respectively, $B_m\,(\mathrm{T})$ is the amplitude of the AC component of the magnetic flux density, and $f_{op}\,(\mathrm{kHz})$ is the operating frequency. Generally $P_h \ll P_{ev}$. Finally k_c, a, and b are the loss constants for a supplied core material. The *total power loss in the core* $P_c\,(\mathrm{W})$ is given by:

$$P_c = P_v\,V_c = k_c\,f_{op}^{a}\,B_m^{b}\,V_c, \tag{3.98}$$

where $V_c = A_c\, l_c\,(\mathrm{cm}^3)$ is the core volume. Now if we consider a sinusoidal current $i_L\,(\mathrm{A})$ circulating through the coil of an inductor with magnetic core as follows:

$$i_L = I_L\, \sin(2\,\pi\, f_{op}\, t), \tag{3.99}$$

we can redefine the total power loss in the core of (3.98) in terms of:

$$P_c = R_c\, I_{Lrms}^2 = \frac{R_c\, I_L^2}{2}, \tag{3.100}$$

where $I_{Lrms} = I_L/\sqrt{2}\,(\mathrm{A})$ is the rms value of the current, while $R_c\,(\Omega)$ is the Equivalent Series Resistance (ESR) of the inductor due to core power loss [33, 45]. Therefore, we obtain:

$$R_c = \frac{2\,P_c}{I_{Lm}^2} = \frac{2\,k_c\, f_{op}^a\, B_m^b\, V_c}{I_{Lm}^2}. \tag{3.101}$$

3.6.2 Winding losses

Another kind of power loss arises from winding losses, which are caused by skin effect and proximity effects in conductors. The first type of winding loss is due to skin effect mechanism that emerges when an AC current flows in a conductor. Hence, a magnetic field is induced in the coil by its own current thus producing extra circulating currents in the winding. The second type of winding loss is due to the proximity effect which appears when AC currents flow in adjacent conductors. Therefore a magnetic field is induced in the coil by their nearby currents thus producing extra circulating currents as well. However, proximity effect is negligible when the conductor pitch is much greater than the conductor radius. These currents tend to flow near the surface of the winding causing the current density to decrease from the surface to the center of the conductor. As the frequency increases, the conductor's effective resistance increases, as well as the winding power loss. At low frequencies, the current follows the path of the lowest resistance, while at high frequencies the current takes the path of the lowest inductance. Winding losses are high-frequency phenomena and limit the capability of conductors to carry high-frequency currents [20, 45].

The frequency behavior of micro-magnetics can be analyzed by evaluating the *skin depth* of a metal conductor $\delta_m\,(\mathrm{m})$ defined as:

$$\delta_m = \sqrt{\frac{\rho_m}{\pi\,\mu_0\,\mu_{rm}\,f_{op}}}, \tag{3.102}$$

where μ_{rm} is the winding relative permeability, and $\rho_m\,(\Omega\,\mathrm{m})$ is the winding resistivity. The skin depth describes the degree of penetration of a conductor by the magnetic flux and eddy currents. The skin effect in the winding is negligible only if the conductor skin depth δ_m is much greater than the metal thickness $t_m\,(\mathrm{m})$, i.e. $\delta_m \gg t_m$. Table 3.1 on the following page shows different skin depth values for copper at several frequencies. Similarly, the *skin depth* can be defined also for a conductive magnetic core $\delta_c\,(\mathrm{m})$ as:

$$\delta_c = \sqrt{\frac{\rho_c}{\pi\,\mu_0\,\mu_{rc}\,f_{op}}}, \tag{3.103}$$

where ρ_c is the core resistivity. The skin effect in the core is negligible only if the core skin depth δ_c is much greater than the core thickness t_c, i.e. $\delta_c \gg t_c$.

Table 3.1: Skin depth values for copper at several frequencies.

Frequency	Skin depth δ_m (m) for copper at $T = 20\,^{\circ}\mathrm{C}$
60 Hz	8.53 mm
400 Hz	3.3 mm
1 kHz	2.53 mm
10 kHz	0.66 mm
20 kHz	0.467 mm
100 kHz	0.209 mm
1 MHz	0.066 mm
10 MHz	20.9 µm
100 MHz	6.6 µm
1 GHz	2.09 µm
2 GHz	1.478 µm
10 GHz	0.66 µm

The DC winding resistance $R_w^{DC}\,(\Omega)$ of a conductor is given by:

$$R_w^{DC} = \frac{\rho_m\, l_m}{A_m} = \frac{\rho_m\, l_m}{w_m\, t_m}, \tag{3.104}$$

where $w_m\,(\mathrm{m})$ and $t_m\,(\mathrm{m})$ are the conductor width and thickness, respectively, while $l_m\,(\mathrm{m})$ is the conductor length. The AC winding resistance $R_w\,(\Omega)$ can be expressed as:

$$R_w = F_R\, R_w^{DC} = F_R\, \frac{\rho_m\, l_m}{w_m\, t_m}, \tag{3.105}$$

where F_R is the *AC resistance factor* defined as:

$$F_R = \frac{R_w}{R_w^{DC}}, \tag{3.106}$$

which represents the AC-to-DC winding resistance ratio. At high frequency the current is assumed to flow uniformly over the skin depth only near both surfaces of a straight conductor, while it is zero in the middle [45]. Furthermore, the conductor thickness (generally the shorter dimension) is more affected by the skin effect than the conductor width. Therefore, if we consider the effective cross-sectional area of the current flow given by $A_e = 2\,\delta_m\, w_m\,(\mathrm{m}^2)$, the AC winding resistance R_w of a straight conductor becomes:

$$R_w = \frac{\rho_m\, l_m}{A_e} = \frac{\rho_m\, l_m}{2\,\delta_m\, w_m}, \tag{3.107}$$

while for a round conductor of diameter $d\,(\mathrm{m})$ the effective cross-section is given by $A_e = \pi\,\delta_m\,(d - \delta_m)$ thus obtaining:

$$R_w = \frac{\rho_m\, l_m}{A_e} = \frac{\rho_m\, l_m}{\pi\,\delta_m\,(d - \delta_m)}. \tag{3.108}$$

A wide conductor has a reduced DC resistance compared to that of a narrow conductor, however the AC resistance of the wider conductor will exceed at a certain frequency that of the narrower conductor. When an inductor or a transformer operate at low frequency, the DC power loss $P_w^{DC}\,(\mathrm{W})$ in the winding can be expressed by:

$$P_w^{DC} = R_w^{DC}\, I_{Lrms}^2 = \frac{R_w^{DC}\, I_L^2}{2}, \tag{3.109}$$

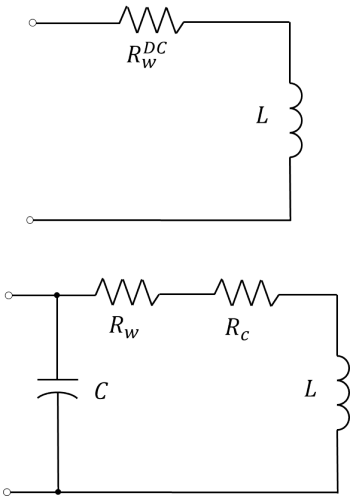


Figure 3.11: Circuit models of an inductor at low frequency (top) and at high frequency (bottom).

where I_{Lrms} is the rms value of the current through the inductor. When the operating frequency is high the current density is non uniform, hence the *AC power loss in the winding* P_w (W) is expressed as:

$$P_w = R_w\, I_{Lrms}^2 = F_R\, R_w^{DC}\, I_{Lrms}^2 = \frac{F_R\, R_w^{DC}\, I_L^2}{2}. \tag{3.110}$$

Hence the AC-to-DC power loss ratio is $F_R = P_w/P_w^{DC} = R_w/R_w^{DC}$.

Finally, the *total power loss* P_L (W) due to both core loss (hysteresis and eddy current losses) and winding loss can be calculated by summing (3.100) and (3.110) as [33]:

$$P_L = P_w + P_c = (R_w + R_c)\, I_{Lrms}^2 = \frac{(R_w + R_c)\, I_L^2}{2}. \tag{3.111}$$

3.6.3 High-frequency inductor model

The low-frequency model of an inductor can be represented by the inductance L in series with the DC series resistance R_w^{DC}. At high frequency the capacitance C (F) between each turn of the winding operates as a shunt capacitance (or self-capacitance) which depends on winding geometry, proximity of the core and turns, and eventually on the permittivity of the winding coating. Hence, the core and the winding should be coated to reduce, respectively, the core-to-winding capacitance and the turn-to-turn capacitance [45]. The high-frequency inductor model includes the AC winding resistance R_w, the core ESR R_c, and the self-capacitance C. Figure 3.11 shows the equivalent circuit models of an inductor at low frequency (top) and at high frequency (bottom). The total AC series resistance of an inductor R_s (Ω) is given by:

$$R_s = R_w + R_c. \tag{3.112}$$

The *quality factor* of a magnetic core inductor Q_L is given by:

$$Q_L = \frac{2\,\pi\, f_{op}\, L}{R_s} = \frac{2\,\pi\, f_{op}\, L}{R_w + R_c} \xrightarrow[R_c \ll R_w]{} \frac{2\,\pi\, f_{op}\, L}{R_w}. \tag{3.113}$$

The *first self-resonant frequency* f_r (Hz) of the parallel resonant circuit formed by the capacitance and the inductance is given by:

$$f_r = \frac{1}{2\,\pi\,\sqrt{L\,C_s}}, \tag{3.114}$$

where for $f < f_r$ the inductor impedance is inductive, while for $f > f_r$ the inductor impedance is capacitive. Generally, the useful frequency range of an inductor is from DC to approximately f_r. At low frequency ($\delta_m \gg t_m$, $\delta_c \gg t_c$) winding and core losses and self-capacitance can be neglected, hence $R_c = 0$, $R_w = R_w^{DC}$, and $R_s = R_w^{DC}$.

The bottom circuit in Figure 3.11 can be represented also by a high-frequency series equivalent circuit [4, 33, 45] with an equivalent AC series resistance $R_{s,eq}\,(\Omega)$ plus an equivalent AC inductance $L_{eq}\,(\mathrm{H})$ given by:

$$R_{s,eq} = \frac{R_s}{(1-\omega^2\,L\,C)^2 + (\omega\,C\,R_s)^2}, \tag{3.115}$$

$$L_{eq} = \frac{L\,(1-\omega^2\,L\,C - C\,R_s^2/L)}{(1-\omega^2\,L\,C)^2 + (\omega\,C\,R_s)^2}, \tag{3.116}$$

where $\omega = 2\,\pi\,f_{op}\,(\mathrm{rad})$. This equivalent model comprises the effect of the self-capacitance which is assumed to be independent of frequency. Finally, the *self-capacitance* can be extracted by (3.116) using the self-resonant frequency f_r defined as the frequency at which $X_{eq} = \omega\,L_{eq} = 0$, thus obtaining:

$$C = \frac{1}{(2\,\pi\,f_r)^2\,L(f_r) + R_s^2(f_r)/L(f_r)}. \tag{3.117}$$

3.6.4 High-frequency transformer model

The low-frequency model of a transformer can be obtained from the circuit in Figure 3.10 on page 41 by including the DC series resistances of primary $R_{w1}^{DC}\,(\Omega)$ and secondary $R_{w2}^{DC}\,(\Omega)$ coil. As for inductors, at high frequency the self-capacitances must be included which consist of turn-to-turn capacitance, core-to-winding capacitance, and winding-to-winding capacitance. The effects of the self-capacitances include resonant frequency, reduced bandwidth, and electrostatic coupling with other circuits [45]. Hence, the high-frequency model of a transformer must consider the AC series resistances of primary $R_{w1}\,(\Omega)$ and secondary $R_{w2}\,(\Omega)$ coil, the core ESR $R_c\,(\Omega)$ referred at the primary, and the self-capacitances of primary $C_1\,(\mathrm{F})$ and secondary $C_2\,(\mathrm{F})$ winding [31, 38]. The winding-to-winding capacitance is not included since it is usually negligible. Figure 3.12 on the facing page shows the equivalent circuit models of a transformer at low frequency (top) and at high frequency (bottom) both referred at the primary side. The AC series resistances of the primary $R_{s1}\,(\Omega)$ and secondary side $R_{s2}\,(\Omega)$ of a transformer are given by:

$$R_{s1} = R_{w1} + R_c, \tag{3.118}$$

$$R_{s2} = R_{w2} + R_c\,n_{12}^2. \tag{3.119}$$

The quality factors of the primary Q_{L1} and secondary Q_{L2} side are given by:

$$Q_{L1} = \frac{2\,\pi\,f_{op}\,(L_{l1}+L_m)}{R_{s1}} = \frac{2\,\pi\,f_{op}\,(L_{l1}+L_m)}{R_{w1}+R_c} \xrightarrow[R_c \ll R_{w1}]{} \frac{2\,\pi\,f_{op}\,(L_{l1}+L_m)}{R_{w1}}, \tag{3.120}$$

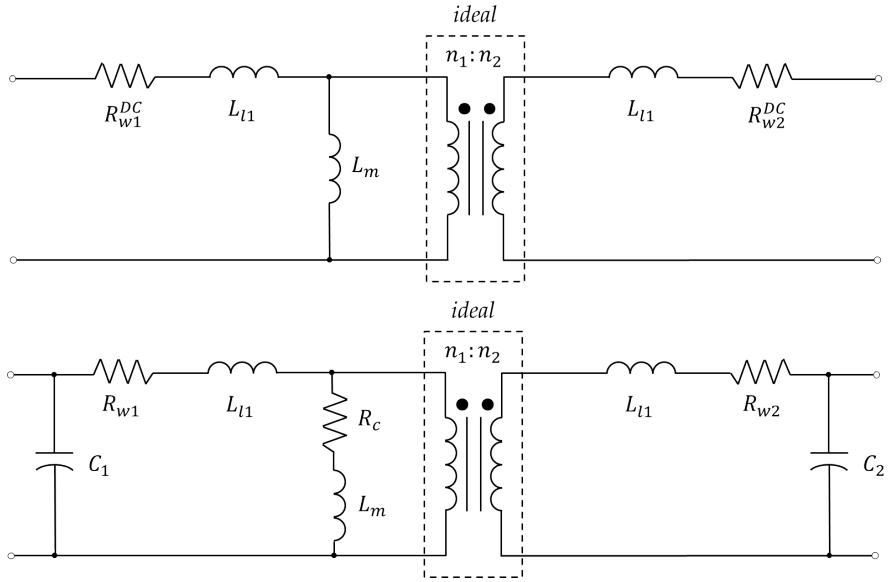


Figure 3.12: Circuit models of a transformer at low frequency (top) and at high frequency (bottom) referred at the primary side.

and:

$$Q_{L2} = \frac{2\,\pi\,f_{op}\,(L_{l2} + L_m\,n_{12}^2)}{R_{s2}} = \frac{2\,\pi\,f_{op}\,(L_{l2} + L_m\,n_{12}^2)}{R_{w2} + R_c\,n_{12}^2} \xrightarrow[R_c\,n_{12}^2 \ll R_{w2}]{} \frac{2\,\pi\,f_{op}\,(L_{l2} + L_m\,n_{12}^2)}{R_{w2}}. \quad (3.121)$$

At low frequency ($\delta_m \gg t_m$, $\delta_c \gg t_c$) winding and core losses and self-capacitances can be neglected, hence $R_c = 0$, $R_{s1} = R_{w1} = R_{w1}^{DC}$, and $R_{s2} = R_{w2} = R_{w2}^{DC}$.

As for an inductor, the primary coil of the bottom circuit in Figure 3.12 can be represented by a high-frequency series equivalent circuit [33] with an equivalent AC primary resistance $R_{s1,eq}\,(\Omega)$ plus an equivalent AC primary self-inductance $L_{11,eq}\,(\mathrm{H})$ given by:

$$R_{s1,eq} = \frac{R_{s1}}{(1 - \omega^2\,L_{11}\,C_1)^2 + (\omega\,C_1\,R_{s1})^2}, \quad (3.122)$$

$$L_{11,eq} = \frac{L_{11}\,(1 - \omega^2\,L_{11}\,C_1 - C_1\,R_{s1}^2/L_{11})}{(1 - \omega^2\,L_{11}\,C_1)^2 + (\omega\,C_1\,R_{s1})^2}, \quad (3.123)$$

where $\omega = 2\,\pi\,f_{op}$. Similarly, the secondary coil can be represented by an equivalent AC secondary resistance $R_{s2,eq}\,(\Omega)$ plus an equivalent AC secondary self-inductance $L_{22,eq}\,(\mathrm{H})$ as follows:

$$R_{s2,eq} = \frac{R_{s2}}{(1 - \omega^2\,L_{22}\,C_2)^2 + (\omega\,C_2\,R_{s2})^2}, \quad (3.124)$$

$$L_{22,eq} = \frac{L_{22}\,(1 - \omega^2\,L_{22}\,C_2 - C_2\,R_{s2}^2/L_{22})}{(1 - \omega^2\,L_{22}\,C_2)^2 + (\omega\,C_2\,R_{s2})^2}. \quad (3.125)$$

These equivalent models include the effect of the self-capacitances of both sides which are assumed to be independent of frequency.

3.6.5 Impedance measurements

The main parameters of a two-winding transformer can be extracted from the two-port network by performing Standard Open and Short circuit (SOS) tests and Extended Open and Short circuit (EOS) tests [38, 45, 83, 90]. In SOS tests the secondary coil is left open ($i_2 = 0\,\mathrm{A}$) while applying an AC voltage to the primary coil with frequency $f_{ac}\,(\mathrm{Hz})$. Measurements at the primary terminals give the primary impedance $Z_{11} = R_{11} + i\,L_{11}\,(\Omega)$, hence the primary self-inductance L_{11} and resistance $R_{11}\,(\Omega)$ are extracted by:

$$L_{11} = \frac{\Im(Z_{11})}{2\,\pi\,f_{ac}} = L_{l1} + L_m, \tag{3.126}$$

$$R_{11} = \Re(Z_{11}) = R_{w1} + R_c. \tag{3.127}$$

Similarly, the primary coil is left open ($i_1 = 0\,\mathrm{A}$) while applying an AC voltage to the secondary coil with frequency f_{ac}. Measurements at the secondary terminals give the secondary impedance $Z_{22} = R_{22} + i\,L_{22}\,(\Omega)$, hence the secondary self-inductance L_{22} and resistance $R_{22}\,(\Omega)$ are extracted by:

$$L_{22} = \frac{\Im(Z_{22})}{2\,\pi\,f_{ac}} = L_{l2} + L_m\,n_{12}^2, \tag{3.128}$$

$$R_{22} = \Re(Z_{22}) = R_{w2} + R_c\,n_{12}^2. \tag{3.129}$$

In EOS tests the secondary coil is short-circuited while applying an AC voltage to the primary coil. Measurements at the primary coil give the total leakage inductance $L_{lp}\,(\mathrm{H})$ referred at the primary side as:

$$L_{lp} = L_{l1} + \frac{L_{l2}}{n_{12}^2}. \tag{3.130}$$

In order to measure the coupling between the coils, the mutual inductance M is measured with series-coupling tests [38]. Firstly, the two windings are connected in series-aiding mode with the two minus terminals short-circuited. Measurements at the two plus terminals give the series-aiding inductance $L_a\,(\mathrm{H})$ as:

$$L_a = L_{11} + L_{22} + 2\,M. \tag{3.131}$$

Secondly, the two windings are connected in series-opposing mode with one plus and one minus terminal short-circuited. Measurements at the other terminals give the series-opposing inductance $L_b\,(\mathrm{H})$ as:

$$L_b = L_{11} + L_{22} - 2\,M. \tag{3.132}$$

Finally, the mutual inductance M is extracted by:

$$M = \frac{L_a - L_b}{4}. \tag{3.133}$$

The series-coupling tests combined with the SOS and EOS tests can be used to compute the transformer parameters only if the magnetizing flux density is common for all tests, establishing a constant value for L_m and R_c. However, the differential impedance varies little with excitation current thus providing results without errors [38].

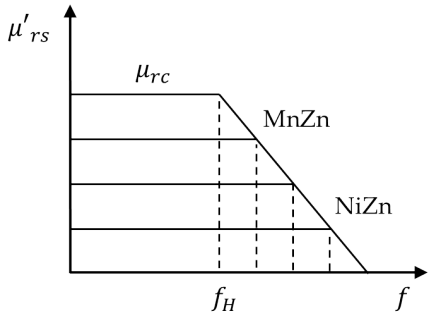


Figure 3.13: Plot of the inductive relative permeability as a function of frequency for ferrites.

3.6.6 Complex permeability

The permeability at high frequencies becomes complex and it may be used to represent all the type of core losses, especially for soft ferrites [35, 45]. The *series complex permeability* μ_s of a magnetic core is given by:

$$\mu_s = \mu'_s - i\,\mu''_s = \mu_0\,(\mu'_{rs} - i\,\mu''_{rs}), \tag{3.134}$$

where μ'_s is the inductive permeability, μ''_s is the resistive permeability, μ'_{rs} is the inductive relative permeability, μ''_{rs} is the resistive relative permeability. The inductive μ'_{rs} and resistive μ''_{rs} relative permeabilities can be approximated by the magnitude of the transfer function of a first-order and second order low pass filters, respectively, as shown below:

$$\mu'_{rs} = \frac{\mu_{rc}}{\sqrt{1 + \left(\dfrac{f}{f_H}\right)^2}}, \tag{3.135}$$

$$\mu''_{rs} = \frac{\mu_{rc}}{\sqrt{1 + Q^2\left(\dfrac{f}{f_H} - \dfrac{f_H}{f}\right)^2}}, \tag{3.136}$$

where μ_{rc} is the low-frequency relative permeability, f_H (Hz) is the -3dB frequency of the μ'_{rs} characteristic, while $Q = f_H/\Delta f$ is the quality factor with Δf (Hz) as the -3dB bandwidth of the μ''_{rs} characteristic.

Therefore, the inductance of an inductor at any frequency L (H) can be modeled as:

$$L = L_0^{DC}\,\mu'_{rs}, \tag{3.137}$$

where L_0^{DC} is the low-frequency inductance with $\mu_{rc} = 1$ obtained by (3.16). The ESR of an inductor $R_c\,(\Omega)$, which represents the core loss, can be modeled as:

$$R_c = 2\,\pi\,f\,L_0^{DC}\,\mu''_{rs}. \tag{3.138}$$

Commonly, MnZn ferrites have large μ_{rc} but low values of f_H, while NiZn ferrites have low μ_{rc} but high values of f_H. Figure 3.13 shows a plot of the inductive relative permeability as a function of frequency for ferrites. It is possible to obtain a parallel

complex permeability model where the parallel inductance at any frequency L_p (H) is the same of (3.137) as:

$$L_p \approx L_0^{DC}\,\mu'_{rs}, \tag{3.139}$$

while the parallel ESR R_p (Ω) is obtained by:

$$R_p = R_c\,[1 + (2\,\pi\,f\,L_p/R_c)^2]. \tag{3.140}$$

3.6.7 Laminated and anisotropic core

Eddy current loss can be reduced by using a high resistivity core. Another option is to split the core into n_l slices called laminations with thickness t_l (m). These sheets have to be electrically insulated from each other and stacked together to form a thick magnetic core [45]. If the core is laminated each layer has a little flux, hence the induced voltage decreases while the condition $\delta_c \gg t_l$ is satisfied. Furthermore, if the laminations are close enough to each other the total magnetic flux is equal to the sum of the fluxes in each sheet. Thus if we consider $t_c = n_l\,t_l$ the low-frequency inductance of an inductor with a laminated core can be obtained from (3.16) as follows:

$$L = \frac{\mu_0\,\mu_{rc}\,n^2\,t_c\,h}{l_c} = \frac{\mu_0\,\mu_{rc}\,n^2\,n_l\,t_l\,h}{l_c} = \frac{n^2}{\mathcal{R}}, \tag{3.141}$$

where h (m) is the height of the core.

For an anisotropic magnetic core, given the relative permeabilities in the hard μ_{rc}^{hard} and easy μ_{rc}^{easy} axis, and the MPLs in the hard l_c^{hard} (m) and easy l_c^{easy} (m) axis, equation (3.16) can be separated in two weighted contributions thus obtaining [27, 28]:

$$L = \frac{n^2}{\mathcal{R}^{tot}} = \frac{n^2}{\mathcal{R}^{easy} + \mathcal{R}^{hard}}, \tag{3.142}$$

where $\mathcal{R}^{easy}$ and $\mathcal{R}^{hard}$ are the reluctances of the easy and hard axis, respectively, given by:

$$\mathcal{R}^{easy} = \frac{2\,l_c^{easy}}{\mu_0\,\mu_{rc}^{easy}\,A_c}, \tag{3.143}$$

$$\mathcal{R}^{hard} = \frac{2\,l_c^{hard}}{\mu_0\,\mu_{rc}^{hard}\,A_c}. \tag{3.144}$$

Therefore equation (3.142) becomes:

$$L = \frac{n^2\,\mu_0\,\mu_{rc}^{easy}\,\mu_{rc}^{hard}\,A_c}{l_c^{easy}\,\mu_{rc}^{hard} + l_c^{hard}\,\mu_{rc}^{easy}}. \tag{3.145}$$

For a laminated core with total thickness $t_c = n_l\,t_l$ and $h \gg t_l$, the high-frequency inductance L can be obtained by:

$$L = \frac{L^{DC}\,\delta_c}{t_l}\,\frac{\sinh\left(\frac{t_l}{\delta_c}\right) + \sin\left(\frac{t_l}{\delta_c}\right)}{\cosh\left(\frac{t_l}{\delta_c}\right) + \cos\left(\frac{t_l}{\delta_c}\right)}, \tag{3.146}$$

where L^{DC} is the low-frequency inductance obtained by (3.16) or (3.141) or in case of an anisotropic core by (3.145). In addition, the ESR R_c can be expressed as:

$$R_c = \frac{2\,\pi\,f\,L^{DC}\,\delta_c}{t_l}\,\frac{\sinh\left(\frac{t_l}{\delta_c}\right) - \sin\left(\frac{t_l}{\delta_c}\right)}{\cosh\left(\frac{t_l}{\delta_c}\right) + \cos\left(\frac{t_l}{\delta_c}\right)}. \tag{3.147}$$

The use of a laminated core allows to reduce eddy-currents and so the corresponding power loss density P_{ev}, thus decreasing R_c.

Chapter 4

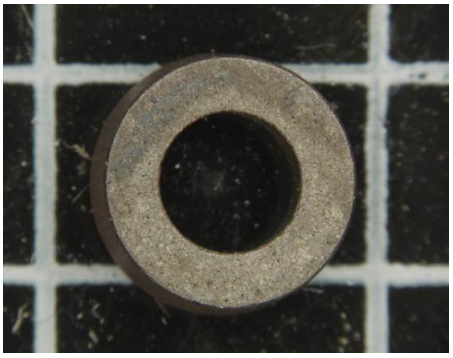
Design and fabrication of bond wire devices

Several micro-transformer prototypes with magnetic core and bonding wires are designed and fabricated with toroidal and race-track shapes first on PCB and later on silicon substrate. The core materials investigated are soft ferrite toroids, LTCC magnetic tapes, and Vitrovac thin films with precise micro-mechanical processing. Various core shapes and thickness are selected to maximize the number of turns in a fixed footprint area. The bonding wires designed are standard IC gold wires assembled in clean room environment. In order to characterize the micro-transformers, the devices are electrically and magnetically measured with LCR Meter and Shb Loop tracer, respectively. Impedance measurements show the realization of high inductance and high turns ratio transformers accordingly to analytical modeling. This chapter describes the fabrication steps of the magnetic cores. Later, the design of the devices on both PCB and silicon substrates is presented. Finally, the analytical modeling and the impedance measurements are reported.

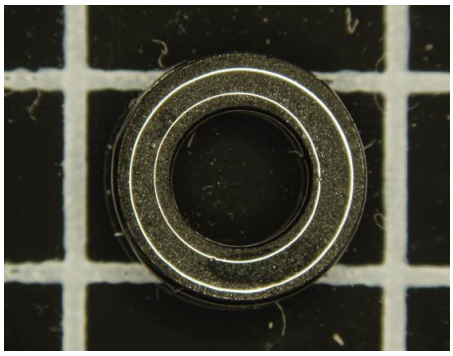
4.1 Fabrication of magnetic cores

4.1.1 Toroidal ferrites

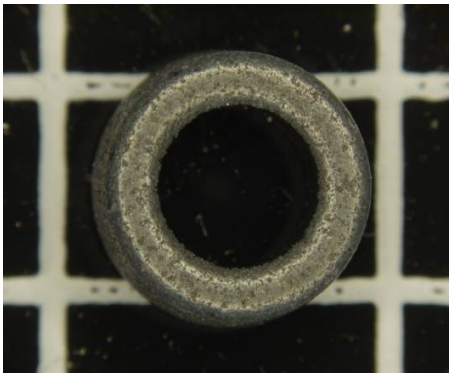
The first type of magnetic material used as core is the soft ferrite with toroidal shape. Several high-permeability toroids are investigated and characterized as core to increase the inductance and improve the coupling coefficient of the bond wire magnetics. The first part is Fair-Rite 5943000801 [14] which is a NiZn uncoated toroidal soft ferrite (43 material) with high resistivity $\rho_c = 10^5\,\Omega\,\mathrm{cm}$, medium relative permeability $\mu_{rc} = 800$, and low saturation flux density $B_s = 290\,\mathrm{mT}$, typically used for inductive applications. The second part is Fair-Rite 5975000801 [15] which is a MnZn uncoated toroidal soft ferrite (75 material) with medium resistivity $\rho_c = 3 \cdot 10^2\,\Omega\,\mathrm{cm}$, high relative permeability $\mu_{rc} = 5000$, and medium saturation flux density $B_s = 430\,\mathrm{mT}$, normally used for broadband transformer applications. The third part is Epcos B64290P36X830 [24] which is a MnZn coated toroidal soft ferrites ($N30$ material) with medium resistivity $\rho_c = 0.5 \cdot 10^2\,\Omega\,\mathrm{cm}$, high relative permeability $\mu_{rc} = 4300$, and medium saturation flux density $B_s = 380\,\mathrm{mT}$. Finally, the last part is an epoxy mold with the same dimension used to evaluate the improvements obtained



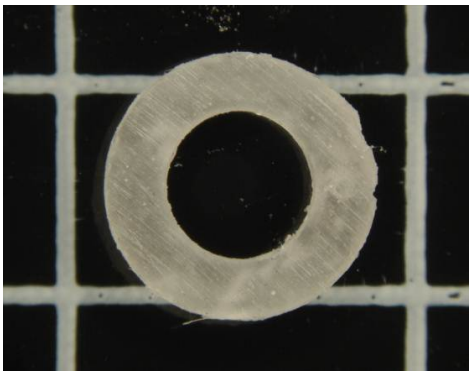
(a) Fair-Rite 5943000801 NiZn ferrite.



(b) Fair-Rite 5975000801 MnZn coated ferrite.



(c) Epcos B64290P36X830 MnZn ferrite.



(d) Dummy epoxy mold.

Figure 4.1: Microphotographs of the toroidal soft ferrites and epoxy mold used as core.

by the insertion of a magnetic core. Figure 4.1 shows four microphotographs of the ferrites and epoxy mold used as core for the bond wire magnetics. The electrical and magnetic properties of toroidal ferrites and dummy core are summarized in Table 4.1 on the next page, with B_r (T) as the residual flux density (or remanence) which represents the remanent magnetization for $H = 0\,\mathrm{A\,m^{-1}}$, and $H_c\,(\mathrm{A\,m^{-1}})$ as the core coercivity which denotes the magnetic field intensity required for reducing the flux density to $B = 0\,\mathrm{T}$.

Whilst miniaturized ferrites are available in commerce, IC packages and wire bonder capillary sizes impose restrictions on the maximum core thickness t_c usable [37, 65, 89]. Hence, the fabrication of the ferrites involves two micro-machining steps performed at the Tyndall National Institute, Cork (IRL) represented by thinning and coating. In the thinning step the core thickness is reduced to an height of $t_c \approx 0.5\,\mathrm{mm}$ with a polishing machine for which the bonder capillary has enough space to reach the inner bonding pads of the device. However t_c can be further reduced if necessary, hence decreasing the self-inductance. In the coating step, performed only for the 5975000801 core due to the lower resistivity, the thinned core is coated with an insulation film (63 Norland optical adhesive with UV curing) to prevent any conductive paths between core and coils. Figure 4.2 on the facing page shows the micro-fabrication steps of the toroidal ferrite cores.

Table 4.1: Electrical and magnetic properties of toroidal ferrites and dummy core.

Supplier	Fair-Rite	Fair-Rite	Epcos	n.a.
Part Number	5943000801	5975000801	B64290P36X830	Dummy
Material	NiZn	MnZn	MnZn	epoxy
D_o (mm)	3.95	3.95	4.00	3.92
D_i (mm)	2.15	2.15	2.40	2.12
h (mm)	1.40	1.40	1.60	0.50
μ_{rc}	800	5000	4300	1
f_H (MHz)	1.6	0.8	0.9	n.a.
Δf (MHz)	10	2.0	2.0	n.a.
ρ_c (Ω cm)	10^5	$3 \cdot 10^2$	$0.5 \cdot 10^2$	n.a.
H_c (A m^{-1})	35.8	12.7	12.0	n.a.
B_s (mT)	290	430	380	n.a.
B_r (mT)	130	140	n.a.	n.a.
k_c (100 °C, 100 kHz)	n.a.	$6.6 \cdot 10^{-8}$	n.a.	n.a.
a (100 °C, 100 kHz)	n.a.	1.52	n.a.	n.a.
b (100 °C, 100 kHz)	n.a.	2.19	n.a	n.a.

n.a.: data not available.

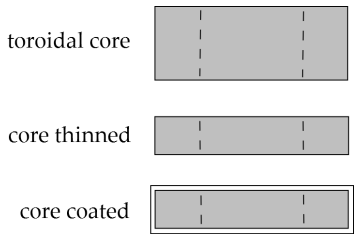
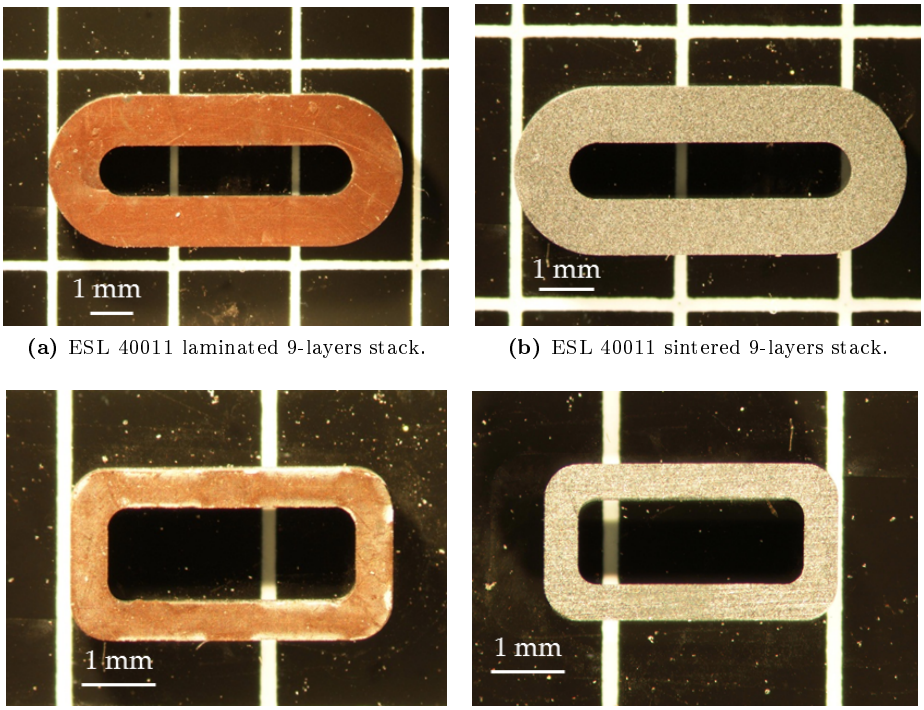


Figure 4.2: Micro-fabrication steps of the toroidal soft ferrite cores.

4.1.2 Race-track LTCCs

The second type of magnetic material used as core is the LTCC magnetic tape with race-track shaped toroid aspect. The ESL 40011 [21] and 40012 [22, 77, 82] are LTCC flexible cast films of magnetic powder. They are given in a green state and designed to be sintered at high temperature to give an isotropic ceramic body and get large grains thus achieving significant magnetic properties.

The fabrication of the tapes involves several micro-machining steps such as: lamination, cutting, and sintering. In the lamination step each layer (thickness $t_l = 60\,\mu$m) is stacked one above the other and laminated with a warm isostatic press (Jenoptik Hot Embosser) at the Tyndall National Institute, which applies first high pressure and then low temperature, thus getting a thick stack of n_l layers. Later the laminated stack is cut in a race-track shape with a laser equipment (Coherent AVIA Laser 355 nm 7 W) at the National Centre for Laser Applications (NCLA), Galway (IRL). Last step is the sintering (co-firing) of the sample at high temperature with slow firing ratio performed in an oven (Nannetti KL 20) at the National Research Council of Italy (CNR)-Institute of Science and Technology for Ceramics (ISTEC), Faenza (IT). During the firing step the sample contracts its dimensions due to frictional forces so



(a) ESL 40011 laminated 9-layers stack. **(b)** ESL 40011 sintered 9-layers stack.

(c) ESL 40012 laminated 9-layers stack. **(d)** ESL 40012 sintered 9-layers stack.

Figure 4.3: Microphotographs of 9-layers laminated stacks of LTCC with race-track shape before and after the sintering step.

it must be taken into account when designing the geometry. As discussed for ferrites, the core thickness is limited to $\approx 0.5\,\text{mm}$, hence $n_l = 9$ layers are chosen as a laminated stack with a total thickness of $t_c = n_l\, t_l \approx 0.54\,\text{mm}$. Figure 4.3 shows four microphotographs of 9-layers LTCC stacks with race-track shape before and after the sintering step.

The ESL 40011 is a green tape designed to be laminated at a combination of pressure/temperature of 10 MPa/70 °C and fired at a peak temperature of 915 °C for 3 hours, thus getting a magnetic tape with $\mu_{rc} = 200$. The sintering step includes several stages such as: from room temperature to 450 °C at 0.7 °C/minute, hold 450 °C for 1 hour, from 450 °C to 915 °C at 3.5 °C/minute, hold peak for 3 hours, from 915 °C to 550 °C at 6 °C/minute, and cooling down to room temperature ($\sim$ 3 °C/minute). The measured shrink percentage is about 19% in all directions. Hence, the total core thickness after sintering is $\approx 0.44\,\text{mm}$. The ESL 40012 is a green tape designed to be laminated at a pressure/temperature combination of 14 MPa/70 °C and fired at a peak temperature of 915 °C for 3 hours, thus getting a magnetic tape with $\mu_{rc} = 500$. Since the 40012 is more dense than 40011, the former requires higher peak temperature to get large grains and thus higher permeability. The sintering step comprises the following stages: from room temperature to 450 °C at 0.7 °C/minute, hold 450 °C for 1 hour, from 450 °C to 930 °C at 3.5 °C/minute, hold peak for 4 hours, from 930 °C to 550 °C at 6.3 °C/minute, and cooling down to room temperature ($\sim$ 3 °C/minute). Figure 4.4 on the next page shows the sintering stages of both ESL 40011 and 40012. The measured shrink percentage is about 17% in all directions. Hence, the total core

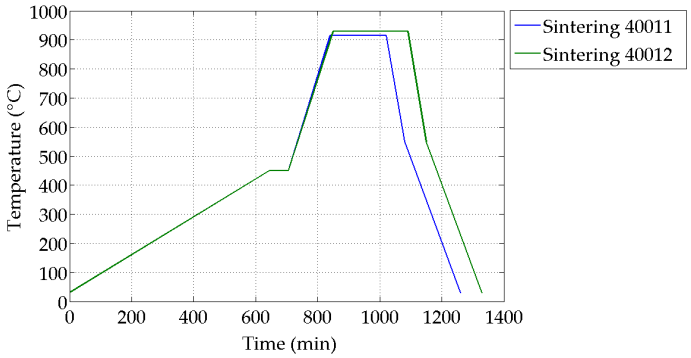


Figure 4.4: Sintering stages of the ESL 40011 and 40012 LTCCs.

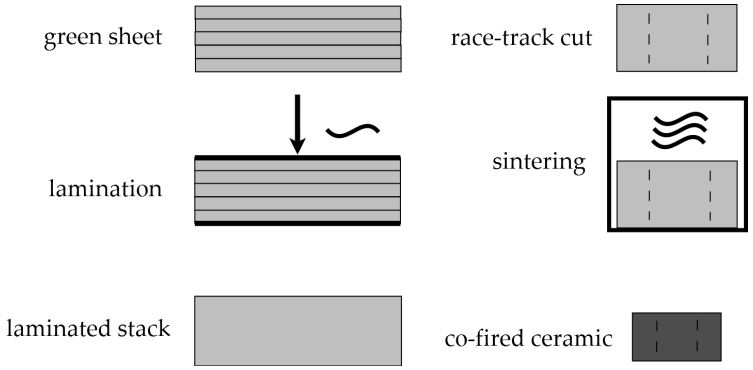


Figure 4.5: Micro-fabrication steps of the race-track LTCC magnetic tapes.

thickness after sintering is $\approx 0.45\,\mathrm{mm}$. The co-fired cores do not require any insulation coating due to the high resistivity ($\rho_c > 10^8\,\Omega\,\mathrm{cm}$) of the ceramic sample. Finally a dummy epoxy mold with the same dimension is used to compare the performance between magnetic and air core transformer. Figure 4.5 shows the micro-fabrication steps of the race-track LTCC magnetic tapes.

4.1.3 Race-track thin films

The Vacuumschmelze Vitrovac VC6155 U55 F [94] is a magnetostriction-free amorphous cobalt-based alloy with high permeability $\mu_{rc} = 1200$, low resistivity $\rho_c = 1.1 \cdot 10^{-4}\,\Omega\,\mathrm{cm}$, and flat hysteresis loop. The VC6155 U55 F exhibits low values for coercivity $H_c = 2\,\mathrm{A\,m^{-1}}$ and thus very low losses, anisotropy field, high saturation flux density $B_s = 1000\,\mathrm{mT}$, and magnetostriction close to zero [39]. The VC6155 U55 F is annealed below crystallization temperature ($\sim 350°\mathrm{C}$) under a magnetic field in a protective atmosphere for several hours. After annealing the material is shaped as a strip wound core with an insulation coating to form a semi-finished strip with thickness $t_l = 21\,\mu\mathrm{m}$. Vitrovac offers three different hysteresis loop: F (flat), Z (square), and R (round). Flat loops (F) require a magnetic field during annealing which is aligned across the strip making an uniaxial anisotropy field (easy axis). Flat loops (F) offer lower frequency dependence of losses showing the best reproducibility of the magnetic properties, while they are sensitive to mechanical stress. Square loops (Z)

Table 4.2: Electrical and magnetic properties of the LTCC magnetic tapes and Vitrovac thin films.

Supplier	ESL	ESL	Vacuumschmelze
Part Number	40011	40012	VC6155 U55 F
Material	LTCC	LTCC	Vitrovac
t_l (µm)	60	60	21
μ_{rc} (100 kHz)	200	500	1200 (easy axis)
ρ_c (Ω cm)	$> 10^8$	$> 10^8$	$1.1 \cdot 10^{-4}$
H_c (A m^{-1})	n.a.	330	2
B_s (mT)	300	350	1000
B_r (mT)	n.a.	250	n.a.

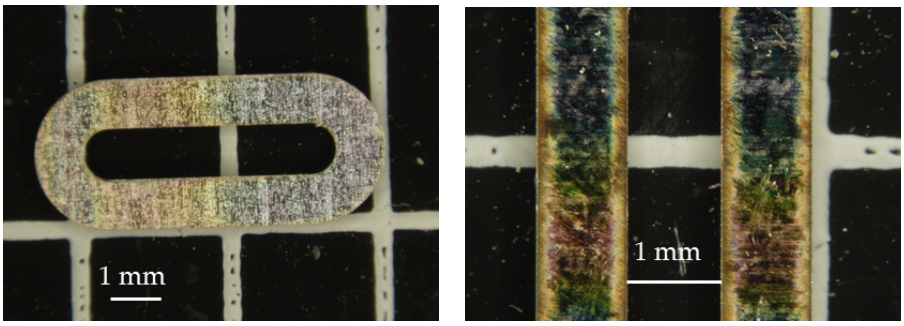
n.a.: data not available.

can be derived from magnetic field annealing along the circumferential direction of the core. Cores with Z-loops show higher scatter in the magnetic properties and higher magnetizing losses compared to F-loops, hence with rising frequency, coercivity and losses increase due to eddy currents. Finally round loops (R) are annealed without magnetic fields and reveal a broader scatter of magnetic properties. The electrical and magnetic properties of both LTCC tapes and Vitrovac thin films are summarized in Table 4.2.

The fabrication of the metallic VC6155 U55 F thin film involves several micro-machining steps such as: cutting, stacking, and coating. In the cutting step several layers of Vitrovac and dielectric films are cut in a race-track shape with a laser equipment (Coherent AVIA Laser 355 nm 7 W) at the NCLA, with the longer axis of the race-track as the easy axis of the Vitrovac thin film, thus obtaining n_l layers with thickness t_l. Figure 4.6 on the next page shows two microphotographs of a single layer of Vitrovac with race-track shape (left) and a zooming on the rear side (right). The right picture shows Heat-Affected Zone (HAZ)s at the edge due to heat intensive cutting laser operations which have modified the micro-structure of the Vitrovac at the weld interface hence reducing the insulation coating. However, HAZs can be avoided by using a short pulse fiber laser. In the stacking step a series of alternating layers of metallic and dielectric films are stacked and glued together in a thick stack with thickness $t_c = t_l\, n_l$. Later the core is coated with an insulation film (63 Norland optical adhesive with UV curing) to prevent any conductive paths between core and coils. Figure 4.7 on the facing page shows the micro-fabrication steps of the race-track Vitrovac thin film.

4.1.4 Magnetic characterization

The hysteresis loops of the ferrite cores are measured by a MESA-300 Loop tracer equipment produced by Shb instruments [41]. Figure 4.8 on page 60 shows the measured hysteresis curves of the toroidal ferrite cores. The hysteresis sweeps of both ferrites have narrow hysteresis loops, which reduce the hysteresis core loss (see section 3.6.1 on page 42) and make them promising magnetic materials for high-frequency applications. The loop tracer provides the data to evaluate the core magnetic properties such as saturation flux density B_s, remanence B_r, and coercivity H_c. Table 4.3 on the next page shows the ferrite core parameters measured from Figure 4.8. By com-



(a) VC6155 U55 F single layer cut with laser.

(b) Zooming on the rear to highlight the HAZs.

Figure 4.6: Microphotographs of a single layer of Vitrovac with race-track shape after laser cutting.

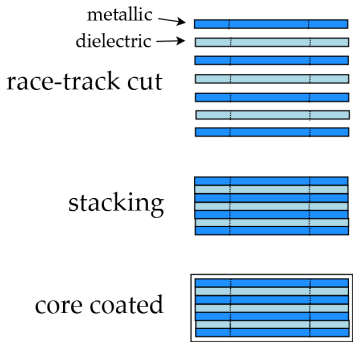


Figure 4.7: Micro-fabrication steps of the race-track Vitrovac thin film.

paring Table 4.3 and 4.1 on page 55 the measured saturation flux density is similar to that provided by manufacturers for all cores, while the measured coercivity is higher and the remanence is lower than that provided by producers for all cores.

4.2 Design and characterization of toroidal magnetics

This section describes the bonding wire tests performed at the Tyndall National Institute to evaluate the wire bonder yield. Later the layout design and the analytical modeling of the bond wire devices on both PCB and silicon substrates are discussed.

Table 4.3: Soft ferrite properties measured with a MESA-300 Loop tracer by Shb instruments.

Core	B_s (mT)	B_r (mT)	H_c (A m^{-1})
5943000801	300	3.6	162
5975000801	410	3.1	153

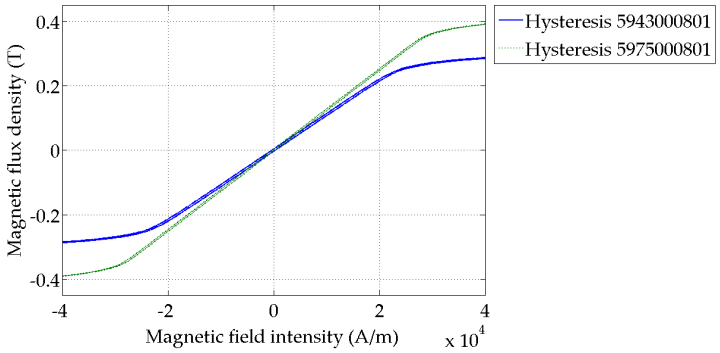


Figure 4.8: Hysteresis curves for 5943000801 core (blue line) and 5975000801 core (green dotted line) obtained with a MESA-300 Loop tracer equipment.

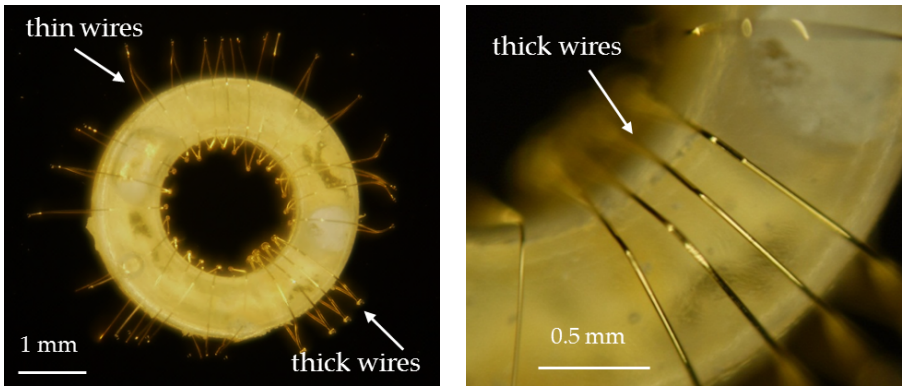
4.2.1 Bonding wire tests

A Kulicke & Soffa (K&S) 4524 gold wire bonder [54] with T/S ball-wedge bonding is used to enable closer wire placement thus leading to the fabrication of high turns ratio devices. Key design parameters in terms of bonding wires include wire diameter, material and minimum spacing [56]. Gold round wires are recommended due to the low resistivity of gold ($\rho_b = 2.44 \cdot 10^{-6}\,\Omega\,\mathrm{cm}$) which minimizes the series resistance. Furthermore, a small spacing between wires enhances the self-inductance and mutual inductance of the devices, thus improving the coupling coefficient. In order to analyze the wire bonder capability, several tests are performed with different gold wire diameter $d_b\,(\mathrm{m})$, ball spread, and BPP on blank silicon substrate coated with gold with epoxy molds mounted on-top. Additionally, a K&S 4700 ribbon bonder is used with ribbon wires characterized by a rectangular cross-section of width $w_b\,(\mathrm{m})$ and thickness $t_b\,(\mathrm{m})$, to compare the yield between round and ribbon wires.

The tests show that thick round wires ($d_b = 32\,\mu\mathrm{m}$) are more robust while the large diameter leads to a small series resistance ($\approx 80\,\mathrm{m}\Omega/\mathrm{wire}$). On the other hand, thin round wires ($d_b = 25\,\mu\mathrm{m}$) are fragile and more resistive ($\approx 130\,\mathrm{m}\Omega/\mathrm{wire}$) due to the smaller diameter, however they allow higher BPP. Besides this, ribbon wires ($w_b = 50\,\mu\mathrm{m}$, $t_b = 12\,\mu\mathrm{m}$) permit to reduce the series resistance ($\approx 60\,\mathrm{m}\Omega/\mathrm{wire}$), however they require greater inner-outer distances from the core. Figure 4.9 on the next page shows two microphotographs of wire bonding tests performed on a toroidal epoxy mold with gold round bonding wires. Figure 4.10 on the facing page shows two microphotographs of wire bonding tests performed on a race-track epoxy mold with gold round bonding wires. Figure 4.11 on page 62 shows two microphotographs of wire bonding tests performed on a race-track epoxy mold with gold ribbon wires. Table 4.4 provides an overview of the electrical and geometrical characteristics of gold bonding wires available at the Tyndall National Institute.

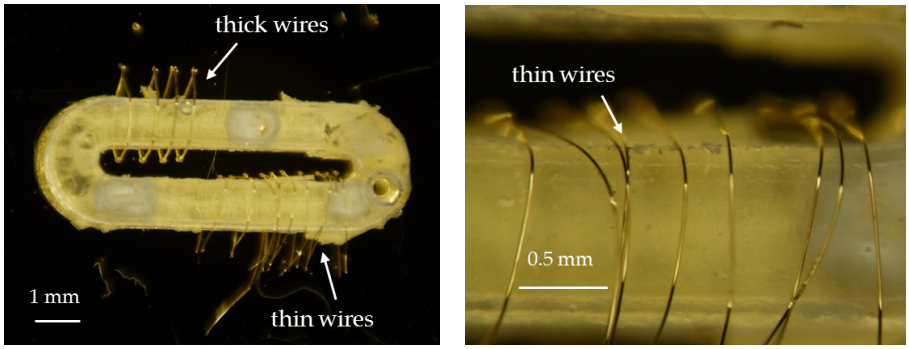
4.2.2 Layout design on PCB substrate

Several layouts are designed and fabricated on a single layer PCB substrate (370HR material) with ultra-thin technology (0.33 mm thick), copper conductor with thickness $t_m = 15\,\mu\mathrm{m}$ and resistivity $\rho_m = 1.68 \cdot 10^{-6}\,\Omega\,\mathrm{cm}$ plus a nichel-gold finish (1 µm). The prototypes are fabricated by Litho-Circuits, Cork (IRL). With the aim to evaluate the



(a) Thin and thick wires. **(b)** Zooming on thick wires.

Figure 4.9: Microphotographs of wire bonding tests on a toroidal epoxy mold with gold round wires.

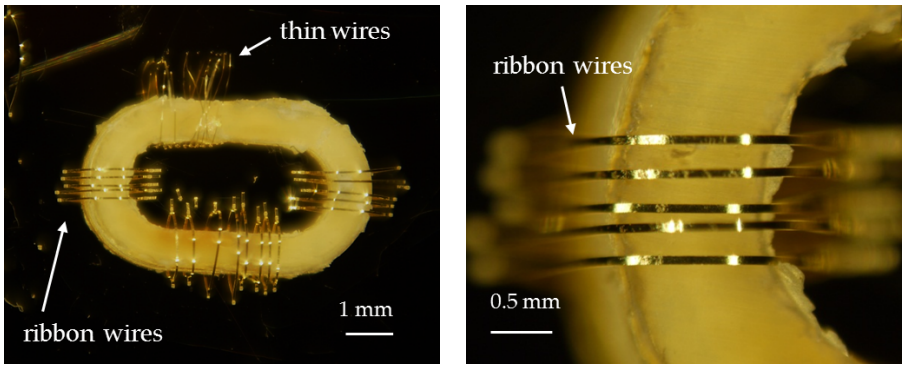


(a) Thin and thick wires. **(b)** Zooming on thin wires.

Figure 4.10: Microphotographs of wire bonding tests on a race-track epoxy mold with gold round wires.

bonding capacity and get the best performance in terms of n_{12} in a fixed footprint area A_r (m), one group of layouts is designed depending on the PCB technology parameters such as conductor width w_m (m) and minimum spacing s_{min} (m), and wire bonder constraints such as BPP and outer/inner d_{ext} (m)/d_{int} (m) pad distances from magnetic core.

The group indicated with $T_{1...4}$ is designed to be assembled with the toroidal ferrites described in section 4.1.1 on page 53 and gold thick bonding wires in a footprint area of $A_r = 4.95\,\text{mm} \cdot 4.95\,\text{mm}$. The first layout, indicated as T_1, is designed with small and narrow conductors thus allowing a higher turns ratio transformer. The second layout, indicated as T_2, is designed with the larger and wider conductors which allows better yield in wire bonding. The third layout, indicated as T_3, is designed with the wider inner pad distance from core thus admitting more space for the capillary insertion and permitting the mounting of thicker cores, however reducing n_2. The last layout T_4 has the same specification as the first layout T_1, but with two turns of primary winding instead of one. Figure 4.12 on page 63 shows the technology parameters and



(a) Thin and ribbon wires. **(b)** Zooming on ribbon wires.

Figure 4.11: Microphotographs of wire bonding tests on a race-track epoxy mold with gold ribbon wires.

Table 4.4: Electrical and geometrical characteristics of gold bonding wires available at the Tyndall National Institute.

Wire	d_b (µm)	w_b x t_b (µm)	Spread (µm)	BPP (µm)	K&S Platform
Ultra-thin	18	n.a.	45 – 90	95	4524
Thin	25	n.a.	65 – 125	112	4524
Thick	32	n.a.	80 – 160	130	4524
Ribbon	n.a.	50 x 12	60 – 70	130	4700

n.a.: data not available.

constraints for the design of toroidal micro-transformers. Table 4.5 shows a summary of the transformer layouts on PCB substrate for toroidal devices.

4.2.3 Assembly of toroidal devices

The micro-machined cores are assembled to the PCB substrate with a mixture of Araldite 15 ml glue (resin and hardener) in a clean room environment. Therefore, each device is bonded with a K&S 4524 wire bonder with thick gold wires from inner pads to outer pads. The devices are assembled with the wire bonder in manual mode with a full control of the bonding head and a work-holder temperature of about 100 °C.

The process parameters of K&S 4524 are loop height, search height, tail length, and ball size [54]. The loop height is the position of the loop after performing the

Table 4.5: Summary of the transformer layouts on PCB substrate for toroidal devices.

Layout	$n_1 : n_2$	w_m (µm)	s_{min} (µm)	BPP (µm)	d_{ext} (µm)/d_{int} (µm)
T_1	1 : 38	80	50	130	450 – 225
T_2	1 : 33	90	60	150	450 – 225
T_3	1 : 28	90	70	160	450 – 300
T_4	2 : 35	80	50	130	450 – 225

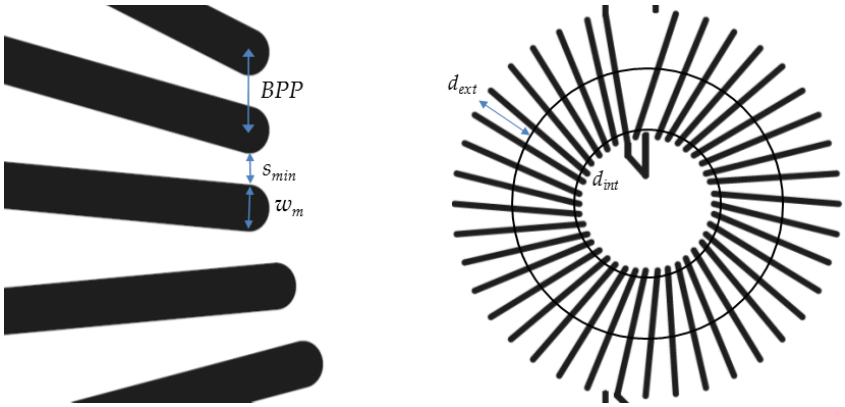


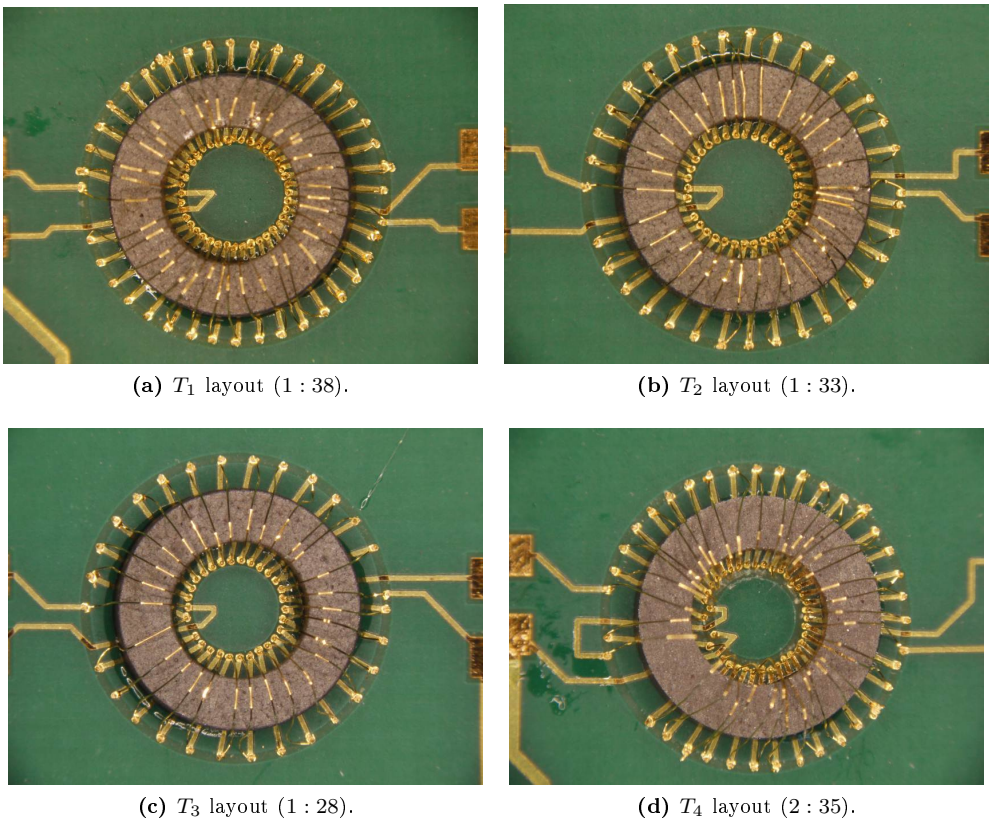
Figure 4.12: Technology parameters and constraints for the design of toroidal micro-transformers.

Table 4.6: Process and bonding parameters setting in the panel of K&S 4524 for gold thick wires on PCB substrate.

Parameter	Setting
Loop height	4.0
Search height (first bond)	5.1
Search height (second bond)	4.2
Ball size	4.6
Tail length	5.0
Power (first bond)	5.5
Power (second bond)	7.1
Time (first bond)	8.0
Time (second bond)	8.0
Force (first bond)	4.5
Force (second bond)	6.5

first bond. The search height is the position at which the bonding head stops above the bond site. The ball size should be set 2 to 3 times larger than the diameter of the wire, as discussed in 2.1 on page 13 and 2.4 on page 19. If the ball is too small, it can block up the capillary, while if the ball is too large it can cause a short-circuit between the wand and the wire. The tail is the length of the wire protruding from the capillary after performing the second bond. Wire bonding is a function of three main bonding parameters: power, time, and force. Bonding power is the amount of ultrasonic energy applied to the bond. Bonding time is the amount of time that the ultrasonic power and force are applied. Bonding force is applied to the wire while the ultrasonic energy is being applied. The process and bonding parameters setting regulated for gold thick wires are shown in Table 4.6.

The devices after micro-fabrication have the following characteristics: reduced core thickness $t_c \approx 0.45\,\text{mm}$, core cross-sectional area $A_c \approx 0.41\,\text{mm}^2$, core mean MPL $l_c \approx 9.6\,\text{mm}$, single turn metalization length $l_m \approx 1.6\,\text{mm}$, and single turn mean wire length $l_b \approx 2.6\,\text{mm}$. Figure 4.13 on the following page shows four microphotographs of the transformers assembled with thick gold bonding wires ($d_b = 32\,\mu\text{m}$) and 5943000801



(a) T_1 layout (1 : 38). **(b)** T_2 layout (1 : 33).

(c) T_3 layout (1 : 28). **(d)** T_4 layout (2 : 35).

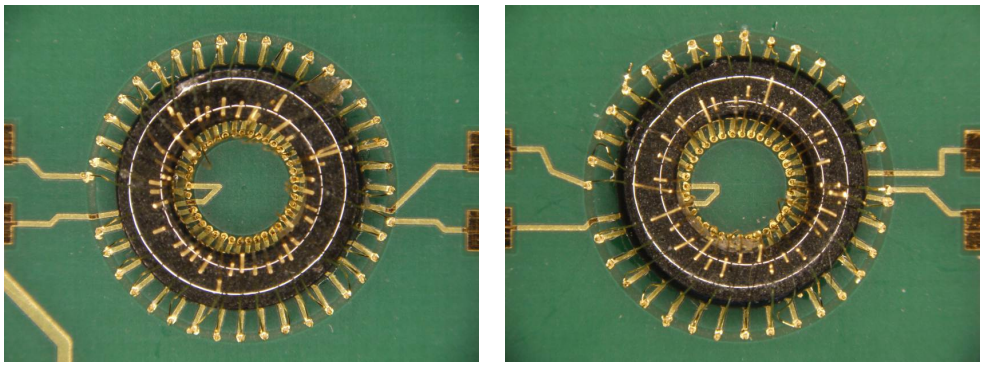
Figure 4.13: Microphotographs of the bond wire transformers assembled with thick gold bonding wires ($d_b = 32\,\mu m$) and 5943000801 ferrite core ($\mu_{rc} = 800$).

ferrite core ($\mu_{rc} = 800$) for all layouts $T_{1...4}$. Figure 4.14 on the next page shows four microphotographs of the transformers assembled with thick gold bonding wires ($d_b = 32\,\mu m$) and coated 5975000801 ferrite core ($\mu_{rc} = 5000$) for all layouts $T_{1...4}$. Figure 4.15 on page 66 shows four microphotographs of the transformers assembled with thick gold bonding wires ($d_b = 32\,\mu m$) and B64290P36X830 ferrite core ($\mu_{rc} = 4300$) for all layouts $T_{1...4}$. Figure 4.16 on page 67 shows four microphotographs of the transformers assembled with thick gold bonding wires ($d_b = 32\,\mu m$) and dummy epoxy mold ($\mu_{rc} = 1$) for all layouts $T_{1...4}$.

4.2.4 Analytical modeling of toroidal devices

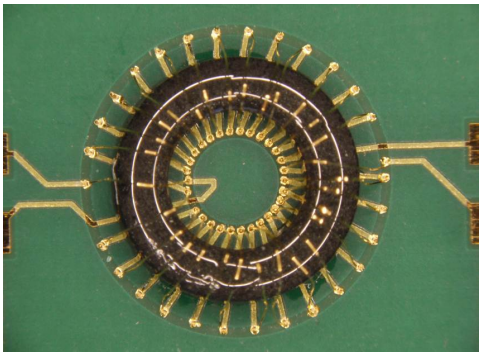
The bond wire transformer structure is composed by bonding wires as coils and soft ferrite as a magnetic core as depicted in Figure 4.17 on page 68. Loops around the magnetic core are performed with bonding wires and completed on the PCB metalization layer.

The devices are modeled by analytical means with equations presented in Chapter 3. The DC self-inductances of both windings L_{11}^{DC} (H) and L_{22}^{DC} (H) are evaluated from the inductance expression (3.21) for a tightly wounded inductor with toroidal

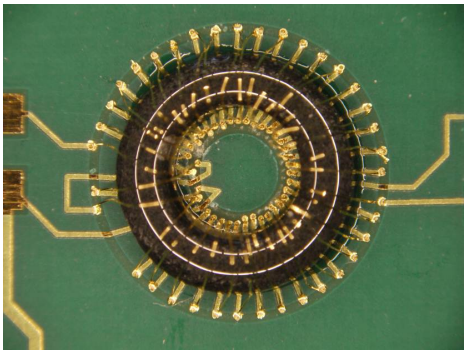


(a) T_1 layout $(1:38)$.

(b) T_2 layout $(1:33)$.



(c) T_3 layout $(1:28)$.



(d) T_4 layout $(2:35)$.

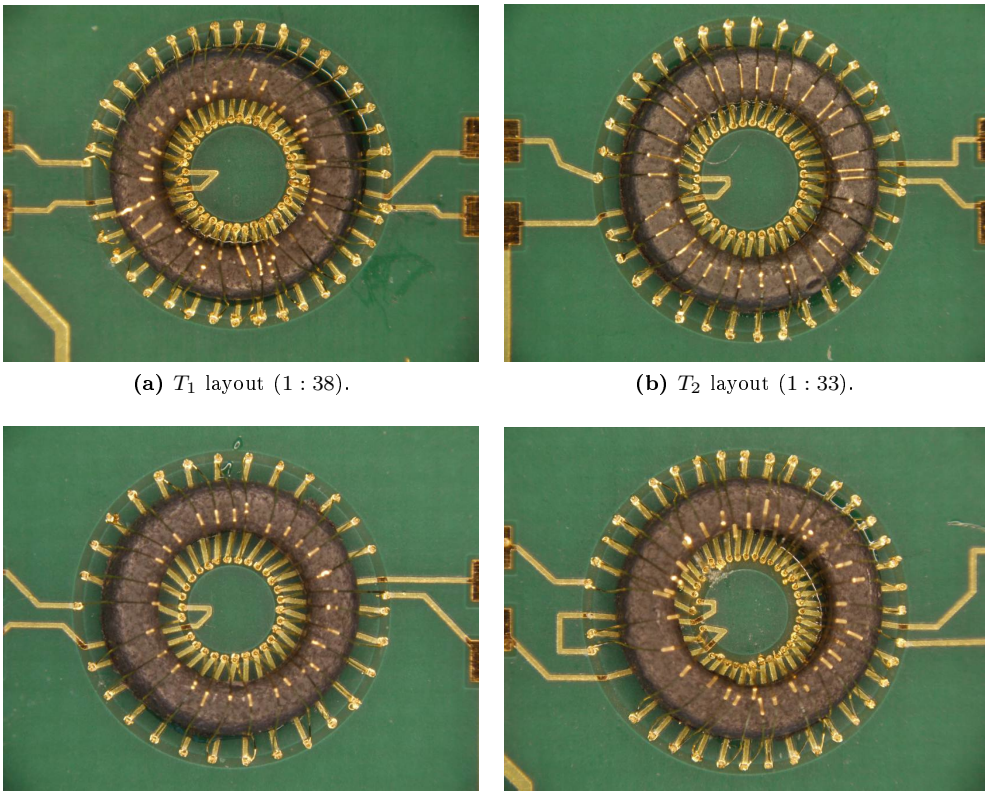
Figure 4.14: Microphotographs of the bond wire transformers assembled with thick gold bonding wires ($d_b = 32\,\mu\text{m}$) and coated 5975000801 ferrite core ($\mu_{rc} = 5000$).

core and rectangular cross-section briefly reported here:

$$L^{DC} = \frac{\mu_0\,\mu_{rc}\,n^2\,A_c}{l_c} = \frac{\mu_0\,\mu_{rc}\,n^2\,t_c\,(D_o - D_i)}{\pi\,(D_o + D_i)}, \tag{4.1}$$

where D_o, D_i, and μ_{rc} are shown in Table 4.1 on page 55 depending on the core type, n is the number of turns of each side shown in Table 4.5 on page 62 which depends on the transformer layout, while t_c is the reduced core thickness measured in section 4.2.3. Since (4.1) is described for strongly wounded inductors, it can lead to an overestimated value if we consider large wounded devices [59]. As discussed in section 3.4.3 on page 32 for the air gap, the equivalent magnetic circuit of a widely wounded inductor should comprises a large air reluctance in parallel with the core reluctance. However, if the relative permeability of the core is high (> 1000) the assumption of tightly wound can be considered true, thus allowing the use of the (4.1) correctly.

The DC series resistances of both windings $R_{w1}^{DC}\,(\Omega)$ and $R_{w2}^{DC}\,(\Omega)$ are obtained from the DC winding resistance expression (3.104) by summing the DC resistances of a single round bonding wire $R_b^{DC}\,(\Omega)$ and of a single PCB metalization $R_m^{DC}\,(\Omega)$,



(a) T_1 layout (1 : 38). **(b)** T_2 layout (1 : 33).

(c) T_3 layout (1 : 28). **(d)** T_4 layout (2 : 35).

Figure 4.15: Microphotographs of the bond wire transformers assembled with thick gold bonding wires ($d_b = 32\,\mu m$) and B64290P36X830 ferrite core ($\mu_{rc} = 4300$).

multiplied by the number of turns as:

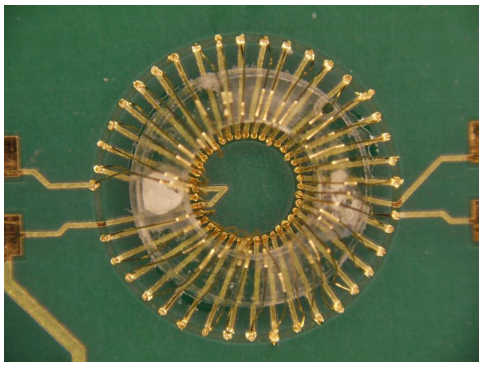
$$R_w^{DC} = n\,(R_b^{DC} + R_m^{DC}) = n\left(\frac{\rho_b\,l_b}{\pi(d_b/2)^2} + \frac{\rho_m\,l_m}{w_m\,t_m}\right), \tag{4.2}$$

where d_b is shown in Table 4.4 depending on the wire used, w_m is displayed in Table 4.5 which depends on the layout considered, l_b and l_m are exposed in section 4.2.3, ρ_m and t_m are shown in section 4.2.2, while ρ_b is displayed in section 4.2.1.

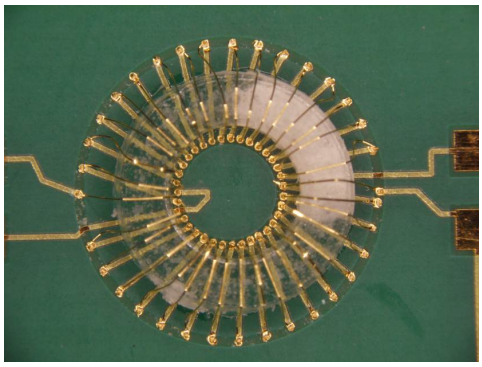
The equivalent saturation current $I_{max}\,(\mathrm{A})$ is estimated by the ampere-turn limit expression (3.13) rewritten for a transformer as:

$$(n_1\,I_1 + n_2\,I_2) \leq I_{max} = B_s\,A_c\,\mathcal{R}, \tag{4.3}$$

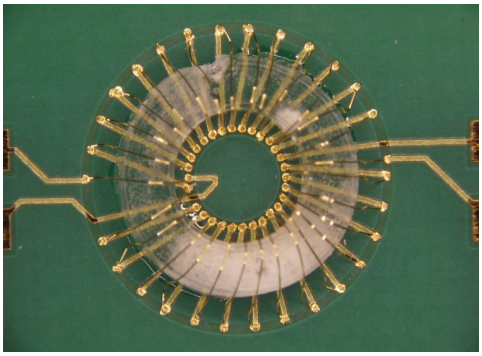
where $I_1\,(\mathrm{A})$ and $I_2\,(\mathrm{A})$ are the amplitudes of the currents in the primary and secondary coil, respectively, while A_c is calculated in section 4.2.3. A current flowing across a bonding wire converts electrical energy to thermal energy through a process called Joule heating, with its associated risk of wire fusing [81]. This effect can be estimated by a modified Preece equation [75] which takes into account of the length of the wire that changes dramatically the current-carrying capability. A typical value of maximum current for a gold bonding wire with $l_b = 2.6\,mm$ and $d_b = 32\,\mu m$ ranges from 0.665 to 0.97 A, hence I_1 and I_2 must comply with this limit.



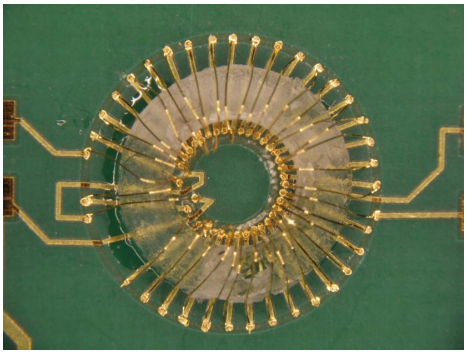
(a) T_1 layout $(1:38)$.



(b) T_2 layout $(1:33)$.



(c) T_3 layout $(1:28)$.



(d) T_4 layout $(2:35)$.

Figure 4.16: Microphotographs of the bond wire transformers assembled with thick gold bonding wires ($d_b = 32\,\mu\text{m}$) and dummy epoxy core ($\mu_{rc} = 1$).

The minimum frequency to avoid core saturation f_{min} (Hz) is evaluated by (3.14) on the primary winding concisely reported below:

$$f_{min} = \frac{V_{1max}}{2\,\pi\,n_1\,A_c\,B_s}, \tag{4.4}$$

where B_s is shown in Table 4.1, while V_{1max} (V) is the maximum amplitude of the sinusoidal voltage applied on the primary side.

The skin depth of metalization δ_m and core δ_c obtained from (3.102) and (3.103), respectively, represent the distances at which the amplitudes of the magnetic field intensity in the coil and core are reduced to $1/e = 0.37$ of their original values. While the low-frequency region is valid when $\delta_m \gg t_m$ and $\delta_c \gg t_c$, the maximum frequency of operation f_{max} (Hz) is defined as:

$$f_{max} \Big|\ \delta_m < 2\,d_b \,||\, \delta_c < 2\,t_c. \tag{4.5}$$

At frequency above f_{max} eddy-currents start to affect the device in both core and windings.

The AC power loss in the core P_c (mW) is estimated by the Steinmetz equation given in (3.98) here reported:

$$P_c = k_c\,f_{op}^{a}\,B_m^{b}\,V_c, \tag{4.6}$$

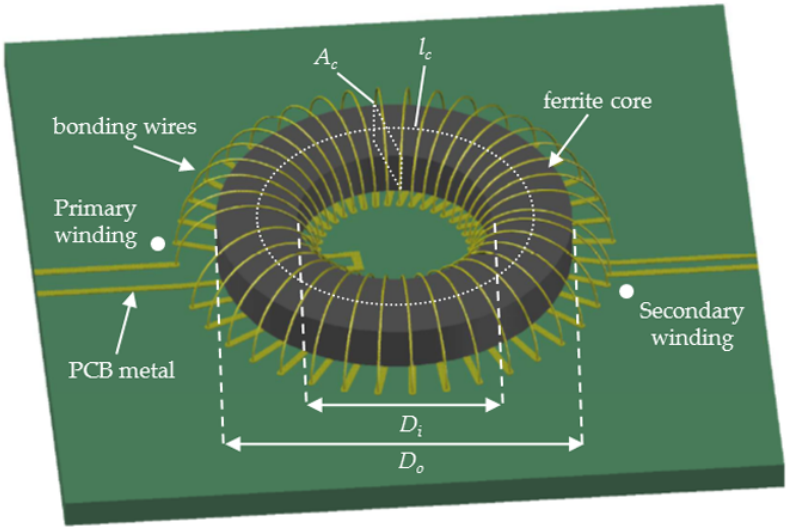


Figure 4.17: Structure of the bond wire transformer device with toroidal ferrite core and round bonding wires. Dimensions and dot convention associated with the core are included.

where B_m (T) is the AC component amplitude of the magnetic flux density, f_{op} (kHz) is the frequency of operation, while k_c, a, and b are the core loss constants given in Table 4.1. The AC power loss in the windings P_w (mW) is estimated by (3.110) here revived:

$$P_w = R_{w1}\, I_{1rms}^2 + R_{w2}\, I_{2rms}^2, \tag{4.7}$$

where I_{1rms} (A) and I_{2rms} (A) are the rms values of I_1 and I_2, respectively, while R_{w1} (Ω) and R_{w2} (Ω) are the AC winding resistances at high frequency estimated by (3.107) and (3.108) thus obtaining:

$$R_w \approx\ n\,(R_b + R_m) = n\left(\frac{\rho_b\, l_b}{\pi\,\delta_m\,(d_b - \delta_m)} + \frac{\rho_m\, l_m}{2\,\delta_m\, w_m}\right), \tag{4.8}$$

where R_b (Ω) and R_m (Ω) are the AC series resistances of a single round bonding wire and of a single PCB metal conductor, respectively.

The AC self-inductances of both coils L_{11} (H) and L_{22} (H) can be modeled by (3.137) as:

$$L = L_0^{DC}\,\mu'_{rs} = \frac{\mu_0\,\mu_{rc}\,n^2\,A_c}{l_c\sqrt{1 + \left(\dfrac{f_{op}}{f_H}\right)^2}}, \tag{4.9}$$

where μ'_{rs} is the inductive relative permeability given in (3.135), f_H (Hz) is the -3dB frequency of the μ'_{rs} characteristic provided in Table 4.1, while L_0^{DC} is the low-frequency inductance with $\mu_{rc} = 1$ obtained by (4.1). In order to characterize the AC core loss, the ESR R_c (Ω) can be modeled by (3.138) as:

$$R_c = 2\,\pi\, f_{op}\, L_0^{DC}\,\mu''_{rs} = \frac{2\,\pi\, f_{op}\,\mu_0\,\mu_{rc}\,n^2\,A_c}{l_c\sqrt{1 + Q^2\left(\dfrac{f_{op}}{f_H} - \dfrac{f_H}{f_{op}}\right)^2}}, \tag{4.10}$$

Table 4.7: Modeling results of DC self-inductances and resistances of the toroidal bond wire transformers.

	Core	5943000801	5975000801	B64290P36X830	Dummy
L_{11}^{DC} (µH)†	T_1	0.051	0.255	0.222	0.060 m
	T_2	0.051	0.255	0.222	0.060 m
	T_3	0.051	0.255	0.222	0.060 m
	T_4	0.185	0.998	0.867	0.238 m
L_{22}^{DC} (µH)†	T_1	60.8	339	294	0.086
	T_2	45.4	254	220	0.065
	T_3	32.4	181	157	0.047
	T_4	51.3	287	249	0.073
R_{w1}^{DC} (Ω)	T_1	0.10	0.10	0.10	0.10
	T_2	0.10	0.10	0.10	0.10
	T_3	0.10	0.10	0.10	0.10
	T_4	0.30	0.30	0.30	0.30
R_{w2}^{DC} (Ω)	T_1	3.8	3.8	3.8	3.8
	T_2	3.2	3.2	3.2	3.2
	T_3	2.7	2.7	2.7	2.7
	T_4	3.5	3.5	3.5	3.5

†: the toroidal inductance expression is described for strongly wounded inductors, hence it can leads to an overestimated inductance for widely wounded devices. However, as the permeability of the ferrites is > 1000 (except for 5943000801 core for which is slightly lower) while the height of the wire loop is lower than 0.7 mm, the assumption of tightly wound is considered true with good approximation [59].

where μ''_{rs} is the resistive relative permeability given in (3.136), while $Q = f_H/\Delta f_{op}$ with Δf_{op} (Hz) as the -3dB bandwidth of the μ''_{rs} characteristic given in Table 4.1. Finally, the AC series resistances R_{11} and R_{22} can be obtained by (3.118) and (3.119).

The modeling results of DC self-inductances and resistances of the toroidal magnetics are shown in Table 4.7. The primary self-inductance L_{11}^{DC} of the T_1 layout increases from 0.060 nH with dummy core to 0.051 µH with 5943000801 core. The other ferrites enable further increases from 0.051 µH to 0.255 µH with 5975000801 toroid. The secondary self-inductance L_{22}^{DC} of the T_1 layout increases from 0.086 µH with dummy core to 60.8 µH with 5943000801 core. The other ferrites enable further increments from 60.8 µH to 339 µH with 5975000801 ferrite. The primary series resistance R_{11}^{DC} of the $T_{1...3}$ layouts for all cores is equal to $\approx 0.10\,\Omega$, while for the T_4 layout is equal to $0.30\,\Omega$ for all cores due to the higher primary turns. The secondary series resistance R_{22}^{DC} ranges from $3.8\,\Omega$ for the T_1 layout for all cores to $2.7\,\Omega$ for the T_3 layout for all toroids.

The modeling results of saturation and AC analysis of the toroidal magnetics are shown in Table 4.8 on page 71. The equivalent saturation current I_{max} ranges from 2.76 A for the 5943000801 ferrite for $T_{1...4}$ to 0.656 A for the 5975000801 ferrite for layouts $T_{1...4}$, while for the epoxy mold there is no saturation. The minimum frequency f_{min} at $V_{1max} = 10$ mV ranges from 13 kHz for the 5943000801 ferrite for $T_{1...3}$ to

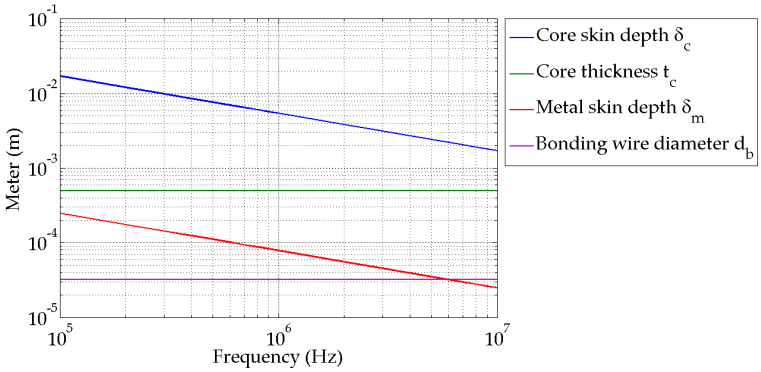


Figure 4.18: Core and metalization skin depths for the B64290P36X830 toroid.

9.8 kHz for the 5975000801 ferrite for $T_{1...3}$, while for the T_4 layout the frequency is half of the previous values due to the higher primary turns. The maximum frequency f_{max} is equal to 1.6 MHz for all layouts and cores mainly due to skin effect in bonding wires and PCB metalizations, while the core skin depth remains much greater than core thickness due to the high resistivity of the ferrites (except for the B64290P36X830 core). Figure 4.18 shows the core δ_c and metalization δ_m skin depths compared with core thickness and bonding wire diameter, respectively, for the B64290P36X830 ferrite. The power loss in the core P_c at $B_m = 0.1\,\mathrm{T}, f_{op} = 0.1\,\mathrm{MHz}$ is 1.04 mW for the 5975000801 core and all layouts. The power loss in the windings P_w at $I_{1rms} = 50\,\mathrm{mA}, I_{2rms} = 1\,\mathrm{mA}, f_{op} = 10\,\mathrm{MHz}$ is ≈ 0.70 mW for all devices except for T_4 layouts that is equal to 1.4 mW.

4.2.5 Measurement results of toroidal devices

The impedance measurements are performed by using a precision LCR Meter 4285A equipped with a test leads 16048A and a probe station [90]. First the LCR Meter is calibrated with open and short circuit tests (1 m cable length, single mode) to compensate the parasitic reactance of the cables, plus an AC voltage level set to 10 mV with no bias. However, the measures comprise the parasitic resistance and inductance of pads and wires which are estimated to be $\approx 0.2\,\Omega$ and ≈ 5 nH, respectively, for each coils for all devices. The devices are measured with equations presented in section 3.6.5 by SOS and series-coupling tests.

Firstly, the self-inductance L_{11} (H) and resistance R_{11} (Ω) of primary side are measured with SOS tests by (3.126) and (3.127) which are here reported:

$$L_{11} = \frac{\Im(Z_{11})}{2\,\pi\,f_{ac}}, \tag{4.11}$$

$$R_{11} = \Re(Z_{11}), \tag{4.12}$$

where Z_{11} (Ω) is the impedance of the primary side. Similarly, the self-inductance L_{22} (H) and resistance R_{22} (Ω) of secondary side are measured by (3.128) and (3.129) here reported:

$$L_{22} = \frac{\Im(Z_{22})}{2\,\pi\,f_{ac}}, \tag{4.13}$$

$$R_{22} = \Re(Z_{22}), \tag{4.14}$$

Table 4.8: Modeling results of saturation and AC analysis of the toroidal bond wire transformers.

	Core	5943000801	5975000801	B64290P36X830	Dummy
I_{max} (A)‡	T_1	2.76	0.656	0.707	lin*
	T_2	2.76	0.656	0.707	lin*
	T_3	2.76	0.656	0.707	lin*
	T_4	2.76	0.656	0.707	lin*
f_{min} (kHz)	T_1	13	9.8	10.5	lin*
	T_2	13	9.8	10.5	lin*
$V_{1max} = 10\,\text{mV}$	T_3	13	9.8	10.5	lin*
	T_4	6.5	4.9	5.2	lin*
f_{max} (MHz)◇	T_1	1.6	1.6	1.6	1.6
	T_2	1.6	1.6	1.6	1.6
	T_3	1.6	1.6	1.6	1.6
	T_4	1.6	1.6	1.6	1.6
P_c (mW)	T_1	n.a.	1.04	n.a.	lin*
$B_m = 0.1\,\text{T}$	T_2	n.a.	1.04	n.a.	lin*
$f_{op} = 0.1\,\text{MHz}$	T_3	n.a.	1.04	n.a.	lin*
	T_4	n.a.	1.04	n.a.	lin*
P_w (mW)	T_1	0.71	0.71	0.71	0.71
$I_{1rms} = 50\,\text{mA}$	T_2	0.70	0.70	0.70	0.70
$I_{2rms} = 1\,\text{mA}$	T_3	0.70	0.70	0.70	0.70
$f_{op} = 10\,\text{MHz}$	T_4	1.4	1.4	1.4	1.4

*: linear behavior of the $B-H$ curve due to the absence of the magnetic core as discussed in section 3.1 on page 27.
‡: while $(n_1\,I_1 + n_2\,I_2) \leq I_{max}$, the currents in the coils I_1 and I_2 are limited by the current-carrying capability of a bonding wire from the modified Preece equation [75, 81] giving a range of maximum current from 0.665 to 0.97 A for gold wires with diameter $d_b = 32\,\mu\text{m}$ and length $l_b = 2.6\,\text{mm}$.
◇: this parameter does not include capacitance effects.
n.a.: data not available.

where $Z_{22}\,(\Omega)$ is the impedance of the secondary side.

Secondly, the series-aiding L_a (H) and series-opposing L_b (H) inductances are measured with series-coupling tests [38] by (3.131) and (3.132), and subsequently the mutual inductance M (H) is extracted from (3.133). All the aforementioned equations are concisely reported below:

$$L_a = L_{11} + L_{22} + 2\,M, \tag{4.15}$$

$$L_b = L_{11} + L_{22} - 2\,M, \tag{4.16}$$

$$M = \frac{L_a - L_b}{4}. \tag{4.17}$$

The coupling coefficient k and the effective turns ratio n_e are extracted by (3.88) and (3.96) in section 3.5.6 on page 41 by assuming that $k_1 = k_2 = k$ (see section 3.5.4),

here concisely reviewed:

$$k = \frac{M}{\sqrt{L_{11}\, L_{22}}}, \tag{4.18}$$

$$n_e = k \sqrt{\frac{L_{22}}{L_{11}}}. \tag{4.19}$$

Finally, the quality factors of both side Q_{11} and Q_{22} are extracted by (3.120) and (3.121) in section 3.6.4 on page 46 here reported:

$$Q_{11} = \frac{\Im(Z_{11})}{R_{11}}, \tag{4.20}$$

$$Q_{22} = \frac{\Im(Z_{22})}{R_{22}}. \tag{4.21}$$

The measured self-inductances, coupling coefficient, and effective turns ratio of the 5943000801 ferrite ($\mu_{rc} = 800$) for all layouts $T_{1\ldots4}$ are shown in Figure 4.19 on page 74. The primary self-inductance L_{11} is enhanced from 0.05 µH with $T_{1\ldots3}$ layouts to 0.22 µH with T_4 layout due to the higher primary turns and the lower spacing between wires. The secondary self-inductance L_{22} is enhanced from 28 µH with T_3 layout to 59 µH with T_1 layouts due to the higher turns number and the lower BPP. However, the performance of the T_1 layout are similar to those of the T_4 layout because the former has two adjacent bonding wires short-circuited due to difficulties in the assembly step. The coupling coefficient k is improved from ≈ 0.7 with T_3 layout to ≈ 0.95 with T_4 layout due to the higher primary turns number which allows a better coupling between coils. The effective turns ratio n_e is increased from 15.5 with T_4 layout to ≈ 27 with T_1 layout due to the higher step-up ratio. Figure 4.20 on page 75 shows a comparison of the calculated and measured self-inductances and resistances of the 5943000801 core for layout T_1. The comparison results shows that the predicted self-inductances and resistances from analytical modeling are in good agreement with measurements. Moreover, Figure 4.20 indicates that the core loss impacts on the behavior of the micro-transformer starting from about 1 MHz due to eddy-currents while there are no capacitance effects in such range of frequency. The measured quality factors of the 5943000801 core for all layouts are reported in Figure 4.21 on page 76. The results show that the maximum secondary quality factor Q_{22} ranges from 12.5 at 500 kHz for T_2 layout to 19.5 at 500 kHz for T_1 layout.

The measured self-inductances, coupling coefficient, and effective turns ratio of the 5975000801 ferrite ($\mu_{rc} = 5000$) for all layouts $T_{1\ldots4}$ are shown in Figure 4.22 on page 77. The primary self-inductance L_{11} is enhanced from 0.21 µH with $T_{1\ldots3}$ layouts to 0.72 µH with T_4 layout due to the higher primary turns and the lower spacing between wires. The secondary self-inductance L_{22} is enhanced from 180 µH with T_3 layout to 315 µH with T_1 layout due to the higher secondary turns and the lower BPP. The coupling coefficient k is improved from ≈ 0.9 with T_3 layout to ≈ 0.95 with T_4 layout due to the higher turns of primary side which enhances the mutual coupling. The effective turns ratio n_e is increased from 17 with T_4 layout to ≈ 34 with T_1 layout due to the higher step-up ratio. Figure 4.23 on page 78 shows the calculated and measured self-inductances and resistances of the 5975000801 core for layout T_1. The comparison results shows that the predicted self-inductances and resistances are in good accordance with measurements obtained by SOS tests. Furthermore, Figure 4.23 indicates that the core loss affects the behavior of the micro-transformer starting from about 0.6 MHz for both coils while there are no self-capacitance effects. The measured

quality factors of the 5975000801 core for all layouts are shown in Figure 4.24 on page 79. The results show that the maximum secondary quality factor Q_{22} ranges from 10 at 70 kHz for T_2 layout to 21.5 at 100 kHz for T_1 layout.

The measured self-inductances, coupling coefficient, and effective turns ratio of the B64290P36X830 ferrite ($\mu_{rc} = 4300$) for all layouts $T_{1...4}$ are shown in Figure 4.25 on page 80. The primary self-inductance L_{11} is enhanced from 0.2 µH with $T_{1...3}$ layouts to 0.83 µH with T_4 layout due to the higher primary turns. The secondary self-inductance L_{22} is enhanced from 148 µH with T_3 layout to approximately 250 µH with $T_{1,2,4}$ layouts due to the higher turns number. The performance of the T_1 layout are similar to those of the $T_{2,4}$ layouts because the former has two adjacent bonding wires short-circuited due to complications in assembling the devices. The coupling coefficient k is approximately equal to 0.95 for all layouts. The effective turns ratio n_e is raised from 17 with T_4 layout to ≈ 32 with T_1 layout due to the higher step-up ratio. Figure 4.26 shows the calculated and measured self-inductances and resistances of the B64290P36X830 core for layout T_1. The results show that the analytically calculated self-inductances and resistances agree well with the measurements, especially the self-inductances. Moreover, Figure 4.26 indicates that the core loss influences the behavior of the micro-transformer starting from about 0.6 MHz for both windings, while there are no self-capacitance effects in that range of frequency. The measured quality factors of the B64290P36X830 ferrite for all layouts are displayed in Figure 4.27 on page 82. The results show that the maximum secondary quality factor Q_{22} ranges from 24.5 at 100 kHz for T_2 layout to 15.5 at 100 kHz for T_3 layout.

The measured self-inductances, coupling coefficient, and effective turns ratio of the epoxy mold ($\mu_{rc} = 1$) for all layouts $T_{1...4}$ are shown in Figure 4.37 on page 93. The primary self-inductance L_{11} is enhanced from 0.01 µH with T_1 layout to 0.03 µH with $T_{2,3}$ layouts. The secondary self-inductance L_{22} is enhanced from 0.2 µH with $T_{2,3}$ layouts to 0.3 µH with T_1 layout. The coupling coefficient k is below 0.2 except for the T_4 layout for which is $\approx 0.3 - 0.4$. The effective turns ratio n_e is below 1 except for the T_4 layout for which is ≈ 1.5. The calculated and measured self-inductances and resistances of the epoxy core for layout T_1 are shown in Figure 4.29 on page 84. The comparison results show poor agreement between analytical and measured self-inductances due to the absence of a magnetic core, while there are no high-frequency effects. The measured quality factors of the epoxy mold for all layouts are displayed in Figure 4.38 on page 94. The results show that the maximum quality factors of both coils are localized at high frequencies, hence the operating range of air-core devices is still higher than 2 MHz.

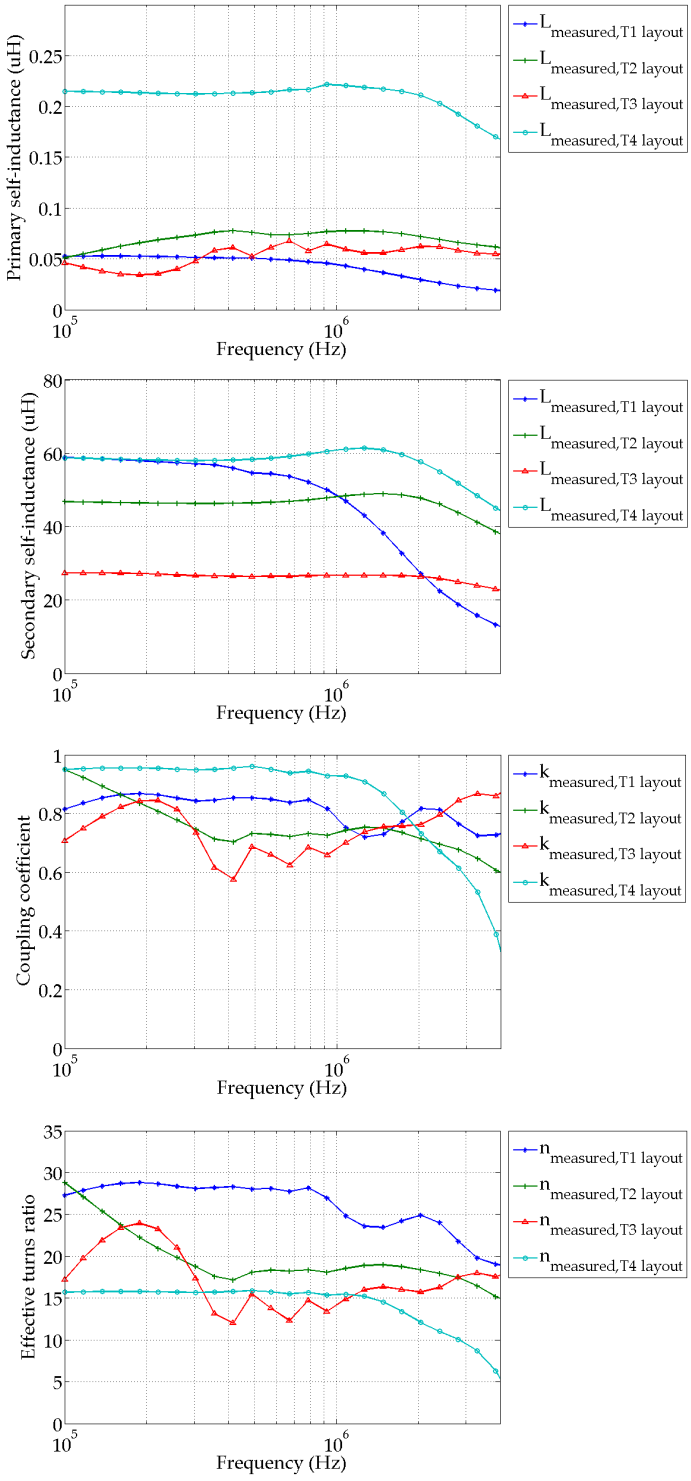


Figure 4.19: Measured self-inductances, coupling coefficient, and effective turns ratio of the devices assembled with 5943000801 core ($\mu_{rc} = 800$) and gold thick bonding wires ($d_b = 32\,\mu\text{m}$) for all layouts $T_{1\ldots4}$.

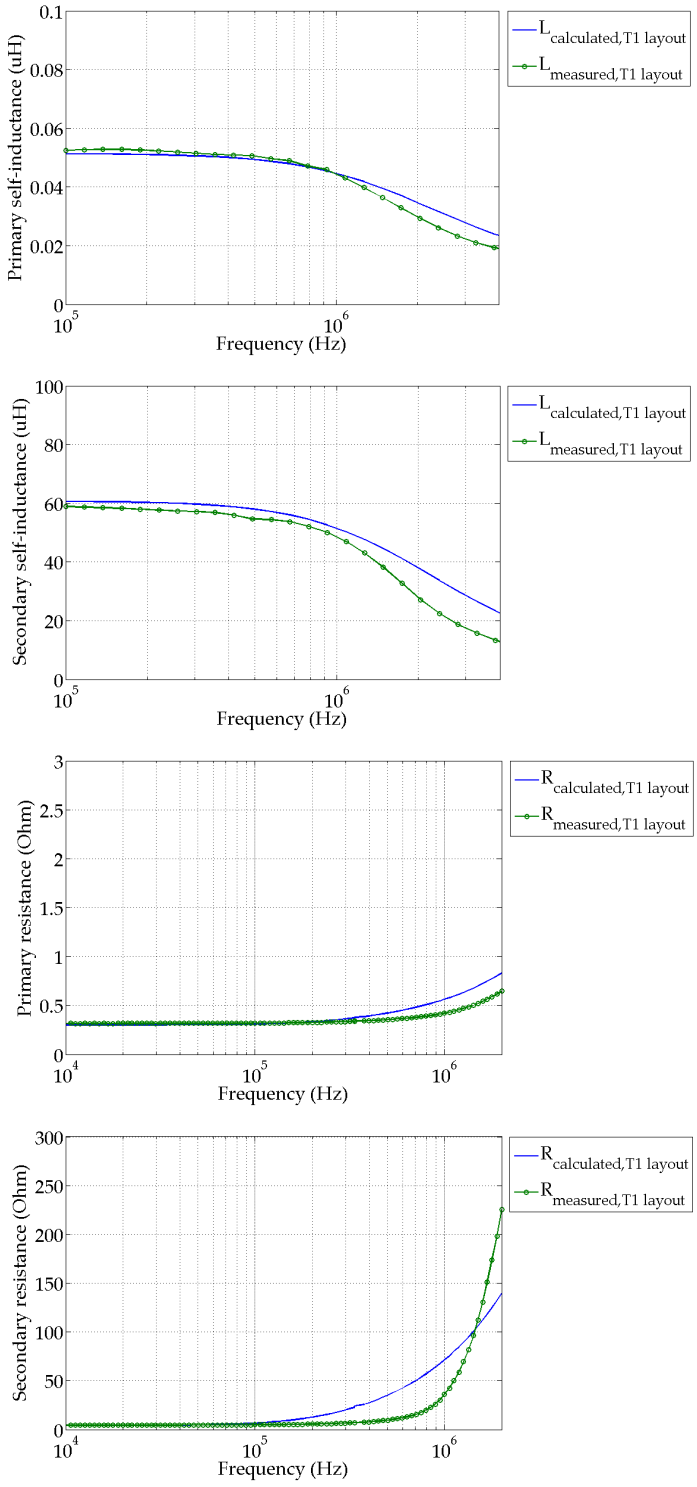


Figure 4.20: Comparison between calculated and measured self-inductances and resistances of the devices assembled with 5943000801 ($\mu_{rc} = 800$) core and gold thick bonding wires ($d_b = 32\,\mu m$) for layout T_1.

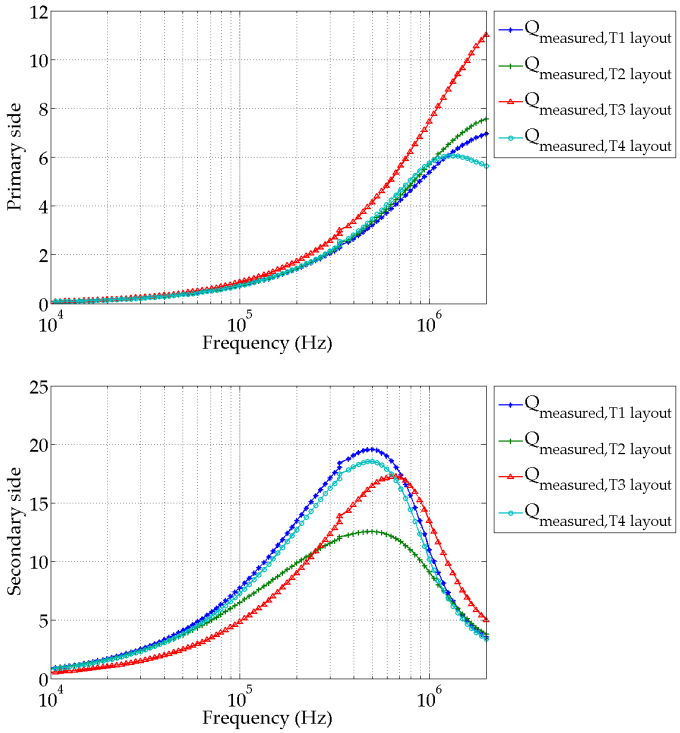


Figure 4.21: Measured quality factors of the devices assembled with 5943000801 core ($\mu_{rc} = 800$) and gold thick bonding wires ($d_b = 32\,\mu\text{m}$) for all layouts $T_{1\ldots4}$.

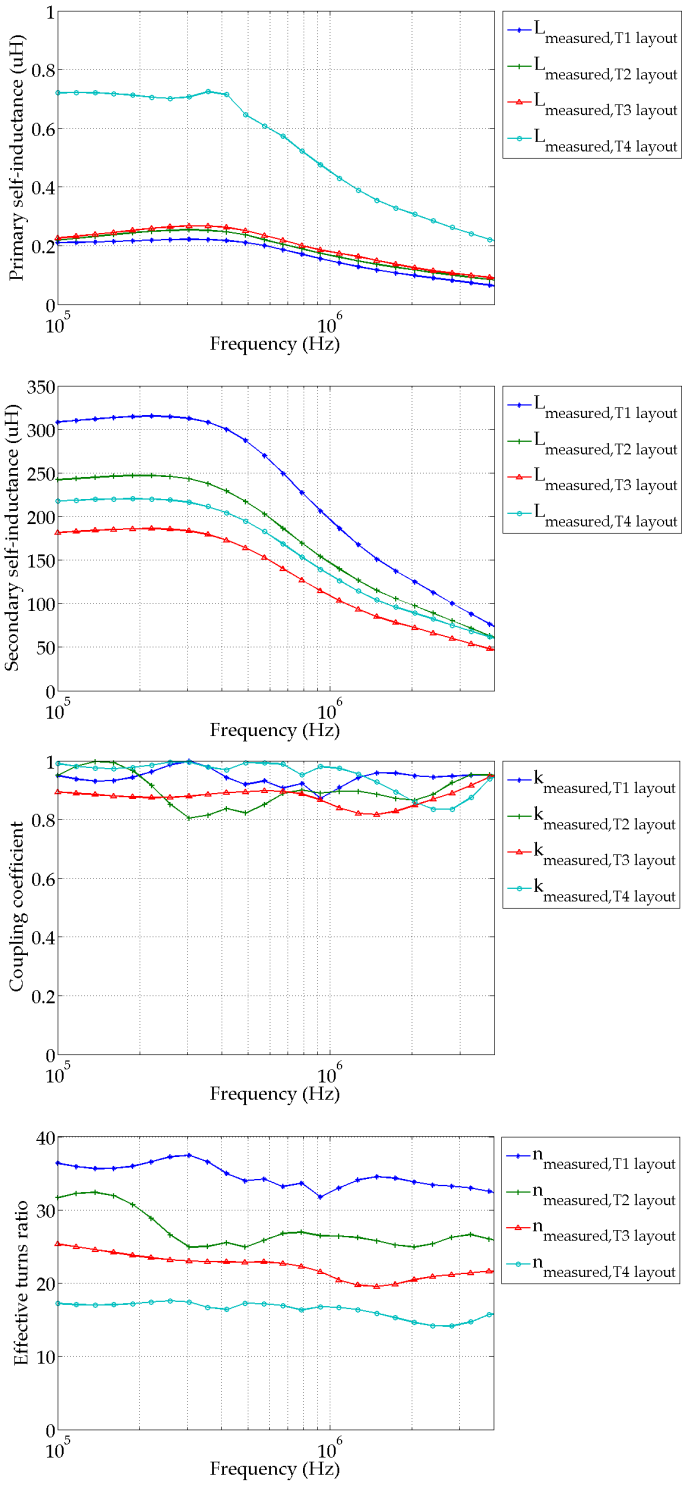


Figure 4.22: Measured self-inductances, coupling coefficient, and effective turns ratio of the devices assembled with 5975000801 core ($\mu_{rc} = 5000$) and gold thick bonding wires ($d_b = 32\,\mu m$) for all layouts $T_{1...4}$.

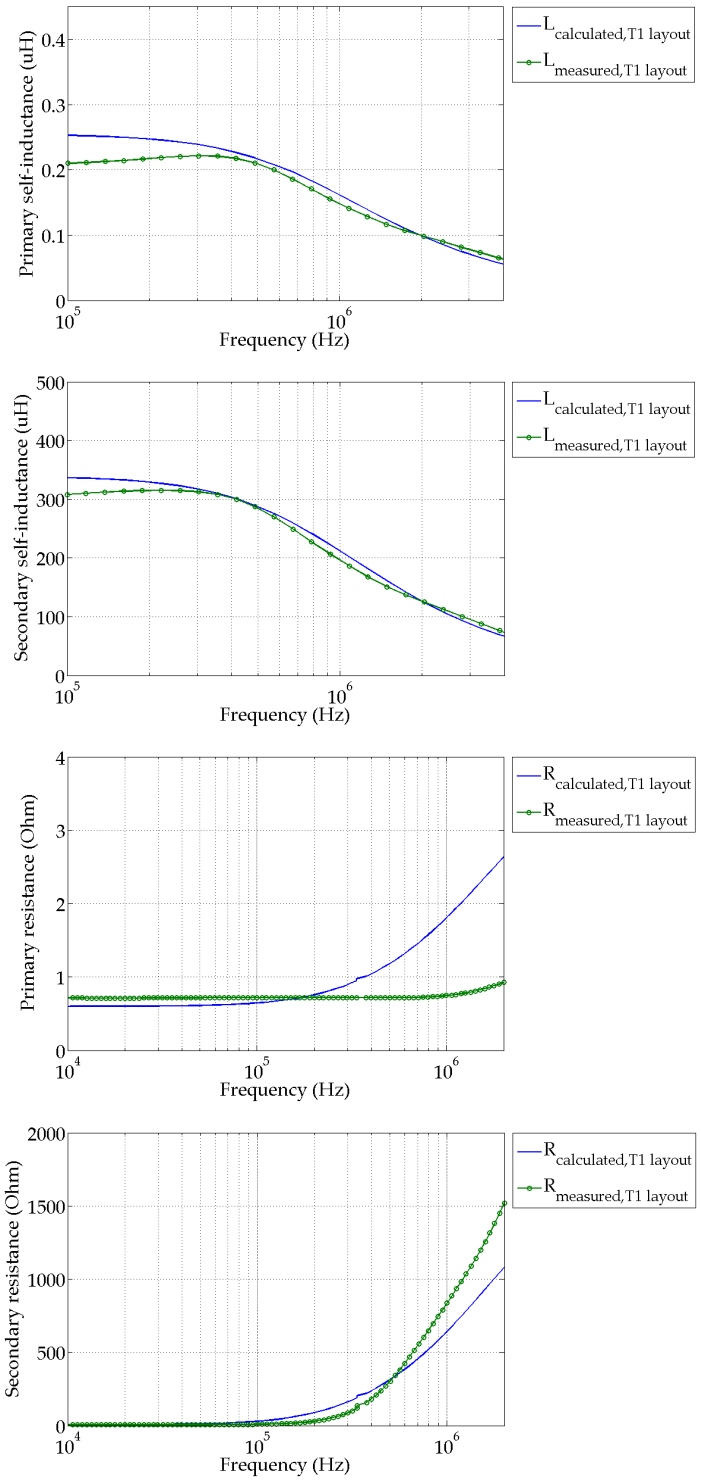


Figure 4.23: Comparison between calculated and measured self-inductances and resistances of the devices assembled with 5975000801 core ($\mu_{rc} = 5000$) and gold thick bonding wires ($d_b = 32\,\mu m$) for layout T_1.

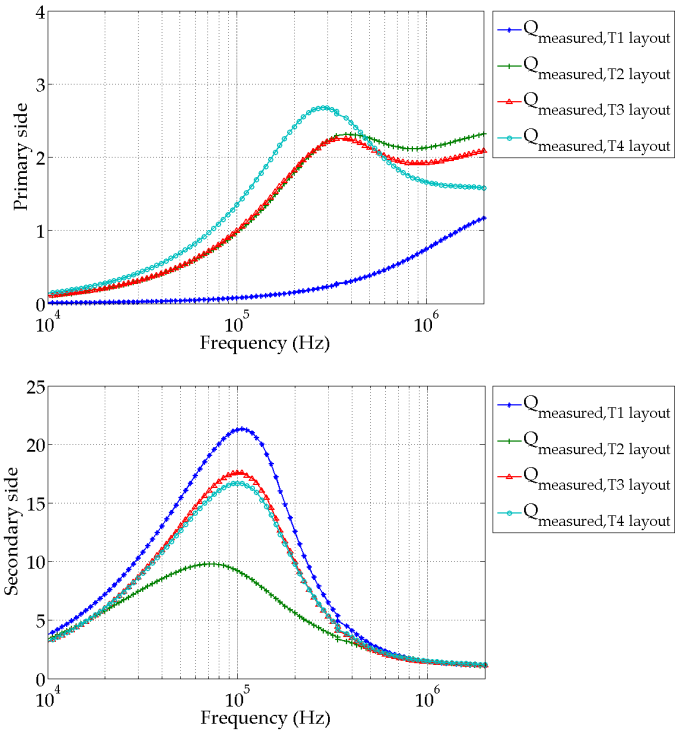


Figure 4.24: Measured quality factors of the devices assembled with 5975000801 core ($\mu_{rc} = 5000$) and gold thick bonding wires ($d_b = 32\,\mu m$) for all layouts $T_{1...4}$.

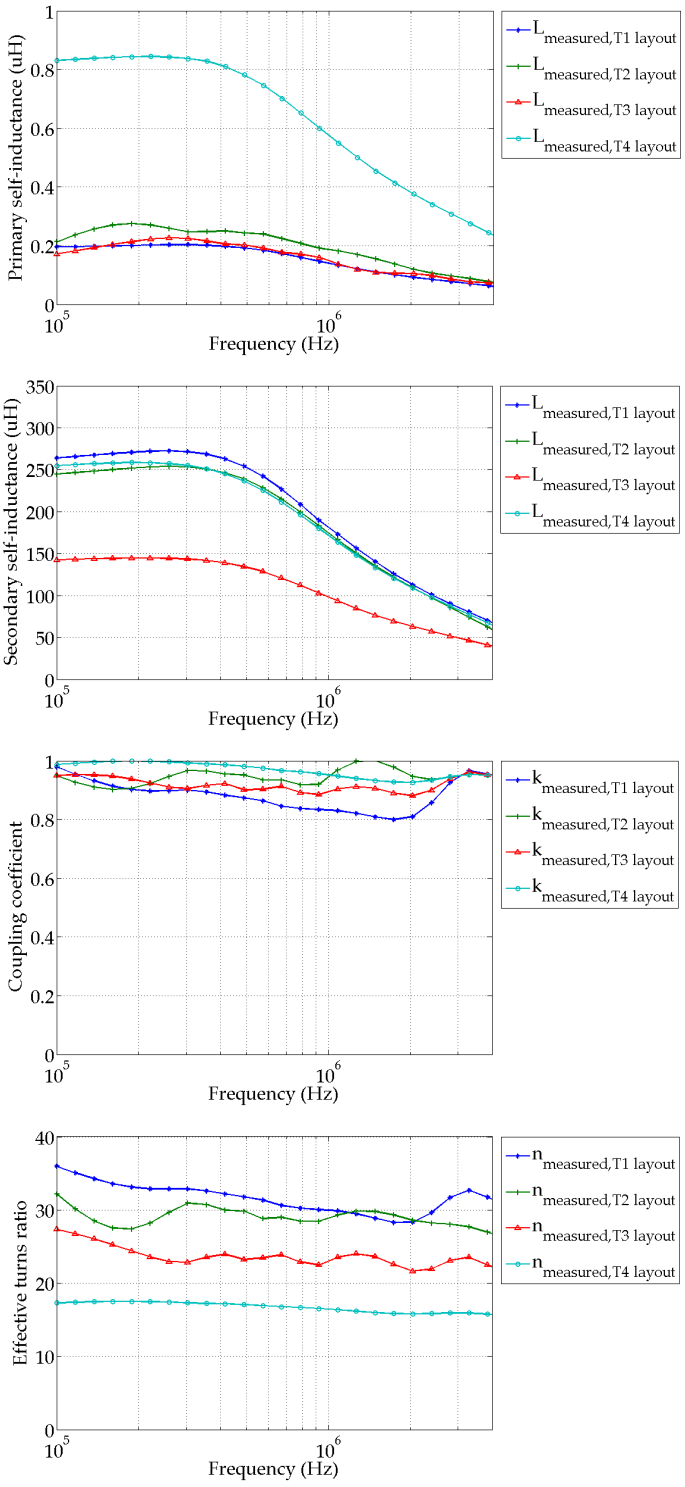


Figure 4.25: Measured self-inductances, coupling coefficient, and effective turns ratio of the devices assembled with B64290P36X830 core ($\mu_{rc} = 4300$) and gold thick bonding wires ($d_b = 32\,\mu m$) for all layouts $T_{1...4}$.

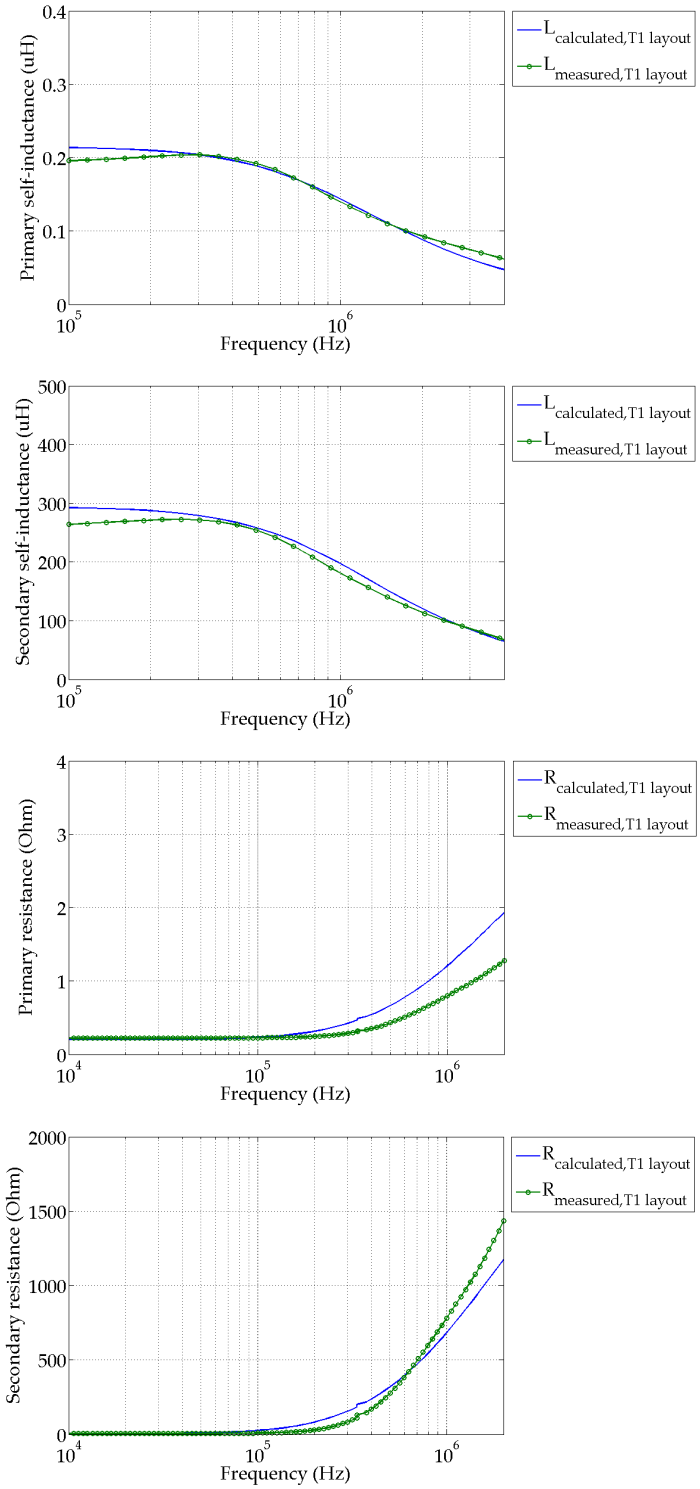


Figure 4.26: Comparison between calculated and measured self-inductances and resistances of the devices assembled with B64290P36X830 core ($\mu_{rc} = 4300$) and gold thick bonding wires ($d_b = 32\,\mu m$) for layout T_1.

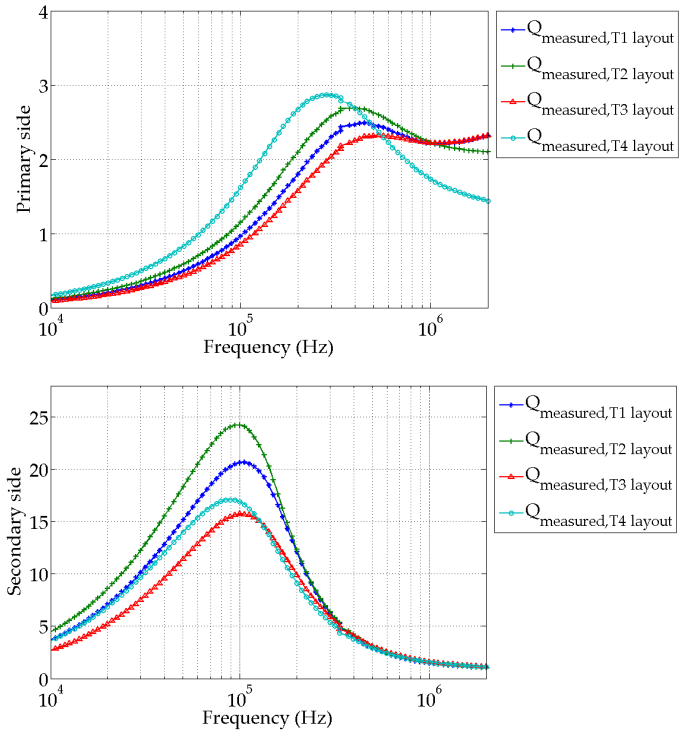


Figure 4.27: Measured quality factors of the devices assembled with B64290P36X830 core ($\mu_{rc} = 4300$) and gold thick bonding wires ($d_b = 32\,\mu\text{m}$) for all layouts $T_{1\ldots4}$.

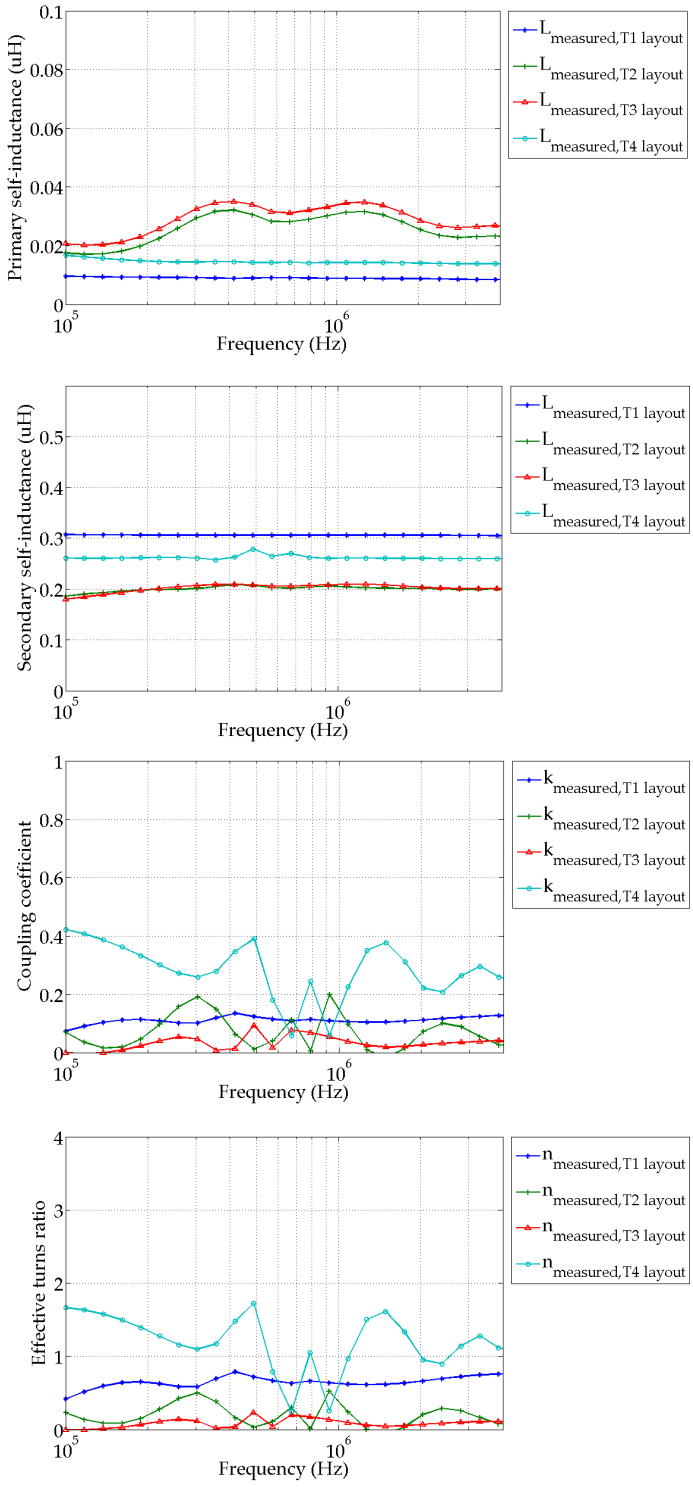


Figure 4.28: Measured self-inductances, coupling coefficient, and effective turns ratio of the devices assembled with epoxy mold ($\mu_{rc} = 1$) and gold thick bonding wires ($d_b = 32\,\mu m$) for all layouts $T_{1...4}$.

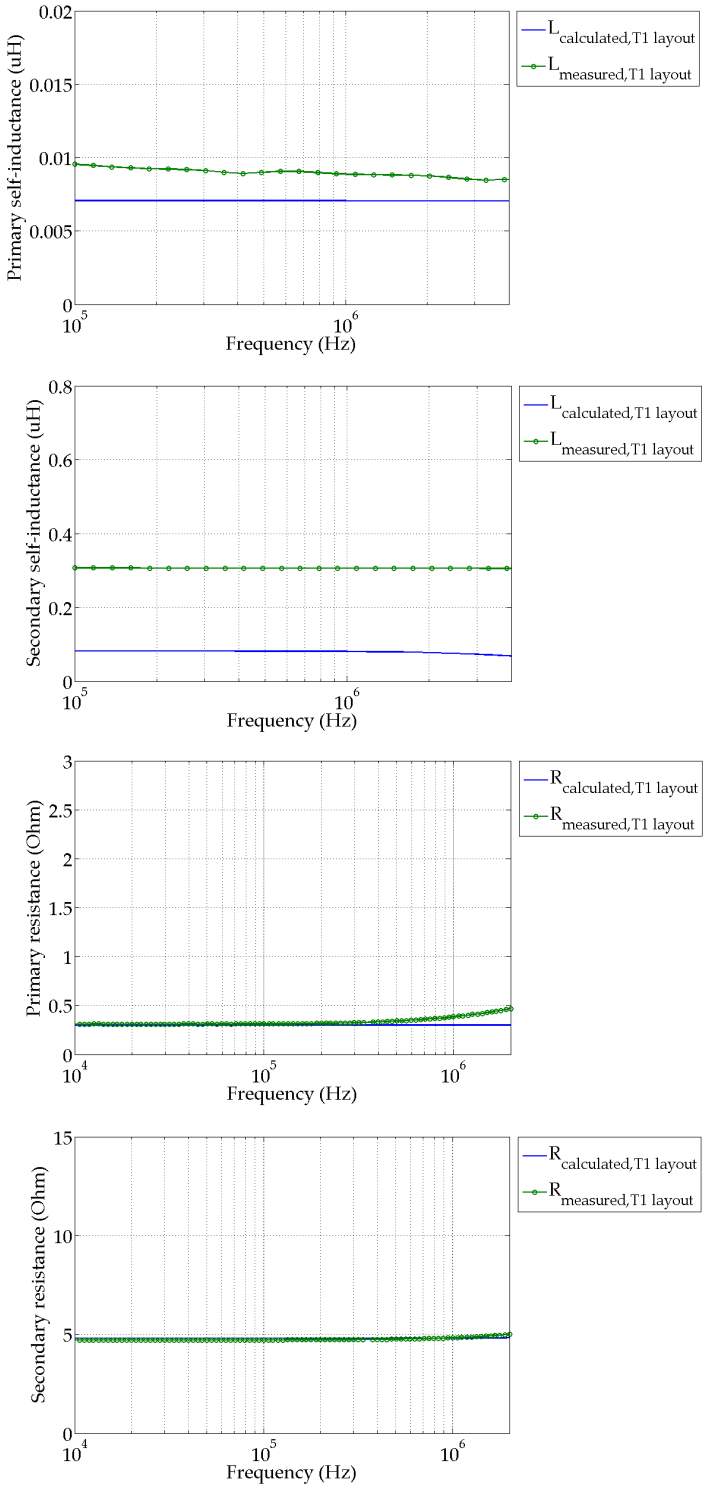


Figure 4.29: Comparison between calculated and measured self-inductances and resistances of the devices assembled with epoxy mold ($\mu_{rc} = 1$) and gold thick bonding wires ($d_b = 32\,\mu m$) for layout T_1.

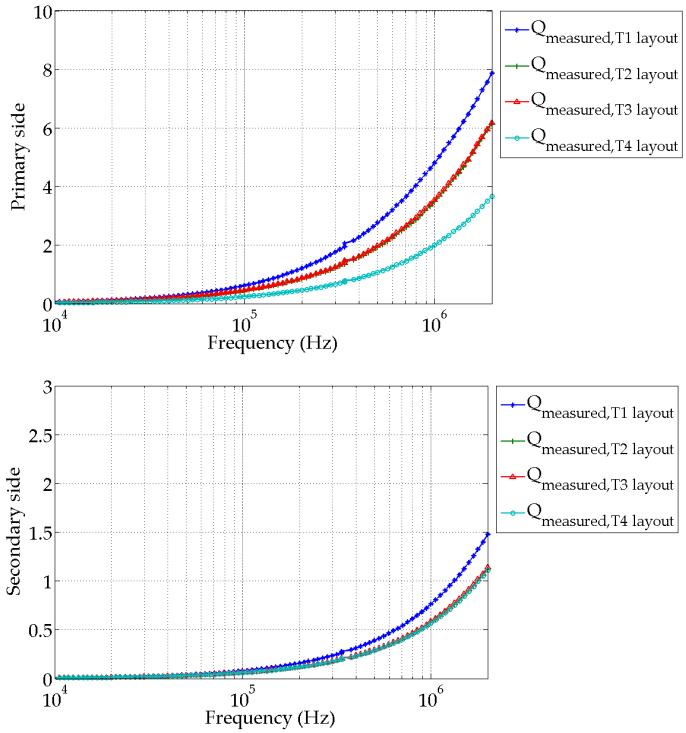


Figure 4.30: Measured quality factors of the devices assembled with epoxy mold ($\mu_{rc} = 1$) and gold thick bonding wires ($d_b = 32\,\mu\text{m}$) for all layouts $T_{1\ldots4}$.

4.3 Design and characterization of race-track magnetics

4.3.1 Layout design on silicon substrate

Several transformers are designed on a silicon die fabricated in 0.32 µm BCD6s technology at STMicroelectronics, Agrate Brianza (IT). The prototypes are realized on the last thick level of metalization (metal3tk) of the BCD6s process [86]. This layer is made of AlCu with thickness $t_m = 1.6\,\mu\text{m}$ and sheet resistance $R_{sheet} = 10\,\text{m}\Omega\,\text{sq}^{-1}$. The resistance of the metalization $R_m\,(\Omega)$ is calculated as:

$$R_m = R_{sheet}\,\frac{l_m}{w_m}, \tag{4.22}$$

where $l_m\,(\text{m})$ and $w_m\,(\text{m})$ are the length and width of the metalization, respectively. The resistivity of the metalization $\rho_m\,(\Omega\,\text{m})$ can be calculated as:

$$\rho_m = R_{sheet}\,t_m, \tag{4.23}$$

thus obtaining $\rho_m = 1.6 \cdot 10^{-6}\,\Omega\,\text{cm}$. The transformer layout is designed to maximize the turns ratio n_{12} in a fixed footprint area of $A_r = 3.93\,\text{mm}\cdot 3.81\,\text{mm}$ depending on the metalization width w_m and spacing $s_m\,(\text{m})$, and wire bonder limitations such as BPP and outer/inner $d_{ext}\,(\text{m})/d_{int}\,(\text{m})$ pad distances from magnetic core. The prototypes are designed to be assembled with the race-track shaped toroidal LTCC cores described in section 4.1.2 on page 55 and gold bonding wires with a gig-gag pad configuration [96] which allows to increase the turns ratio while complying with the minimum BPP. A dummy epoxy mold is used to evaluate the advancements obtained by the insertion of a magnetic core. Figure 4.31 on the facing page shows the technology parameters and constraints for the design of the race-track devices. Table 4.9 shows a summary of the layout parameters on silicon substrate for race-track transformers.

4.3.2 Assembly of race-track devices

Firstly, the silicon layout is placed in a CLCC68 package, and later the race-track cores are assembled to the silicon substrate with a mixture of glue in clean room environment. Figure 4.32 on page 88 shows two pictures of the BCD6s silicon layout on the left, and of the transformer with the 40012 LTCC core mounted on-top of the die on the right. The device with the LTCC core is bonded with a K&S 8208-PPS with thin gold wires at STMicroelectronics, while the device with epoxy core is bonded with a K&S 4524 with thick gold wires at the Tyndall National Institute, both from inner pads to outer pads in clean room environment. The devices after micro-fabrication have the following characteristics: core layers $n_l = 9$, fired layer thickness $t_l \approx 45\,\mu\text{m}$, fired core thickness $t_c = n_l\,t_l \approx 0.41\,\text{mm}$, core length $l = 3.8\,\text{mm}$, core depth $p = 2.0\,\text{mm}$, core width $w_c \approx 0.5\,\text{mm}$, core cross-sectional area $A_c \approx 0.20\,\text{mm}^2$,

Table 4.9: Summary of the layout parameters on silicon substrate for race-track micro-transformers.

$n_1 : n_2$	$w_m\,(\mu\text{m})$	$s_m\,(\mu\text{m})$	BPP (μm)	$d_{ext}\,(\mu\text{m})/d_{int}\,(\mu\text{m})$
1 : 50	90	20	112	450 – 225

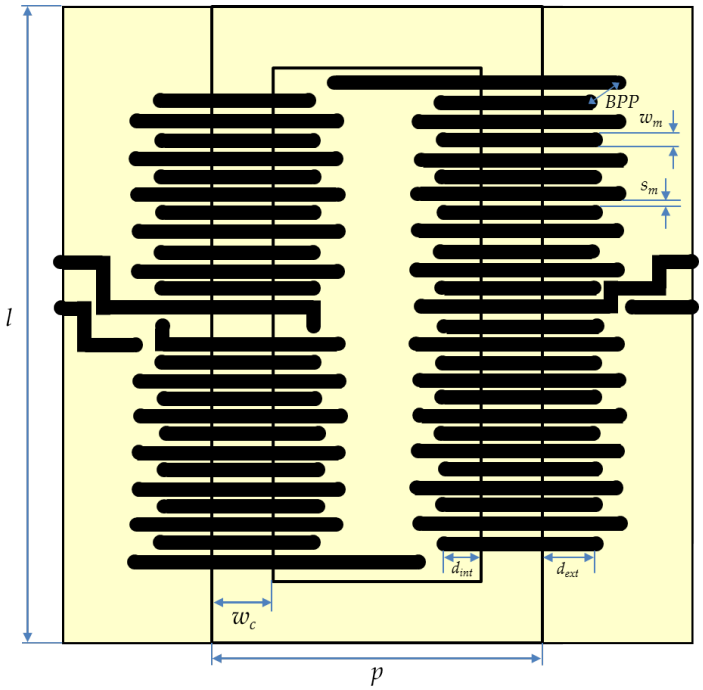


Figure 4.31: Technology parameters and constraints for the design of race-track micro-transformers.

core mean MPL $l_c \approx 9.6\,\text{mm}$, single turn metalization length $l_m \approx 1.32\,\text{mm}$, and single turn mean bonding wire length $l_b \approx 3.0\,\text{mm}$. Figure 4.33 on page 89 shows two microphotographs of the transformers assembled with 40012 LTCC core ($\mu_{rc} = 500$) and thin gold bonding wires ($d_b = 25\,\mu\text{m}$) on the left, and with epoxy mold core ($\mu_{rc} = 1$) and thick gold bonding wires ($d_b = 32\,\mu\text{m}$) on the right.

4.3.3 Analytical modeling of race-track devices

The bond wire transformer structure is composed by bonding wires as coils and LTCC as a magnetic core. Loops around the magnetic core are realized with bonding wires and completed on the last thick metal layer of the BCD6s silicon technology. As for the toroidal devices, the race-track components are analyzed by most of all equations presented in Chapter 3 on page 27 revisited in section 4.2.4 on page 64 for both DC, saturation and AC analysis. The only exceptions are the DC self-inductances of both coils L_{11}^{DC} (H) and L_{22}^{DC} (H) adapted for a race-track core as follows:

$$L^{DC} = \frac{\mu_0\,\mu_{rc}\,n^2\,A_c}{l_c} = \frac{\mu_0\,\mu_{rc}\,n^2\,t_c\,w_c}{2\,(l+p-2\,w_c)}, \tag{4.24}$$

where $A_c = t_c\,w_c$, $l_c = 2\,(l+p-2\,w_c)$, while n is the number of turns of the coil considered displayed in Table 4.9 on the facing page.

The modeling results of DC self-inductances and resistances, saturation, and AC analysis of the race-track magnetics are shown in Table 4.10 on page 90. The primary self-inductance L_{11}^{DC} increases from 0.027 nH with dummy mold to 0.014 µH with 40012 core, while the secondary self-inductance L_{22}^{DC} increases from 0.066 µH with dummy

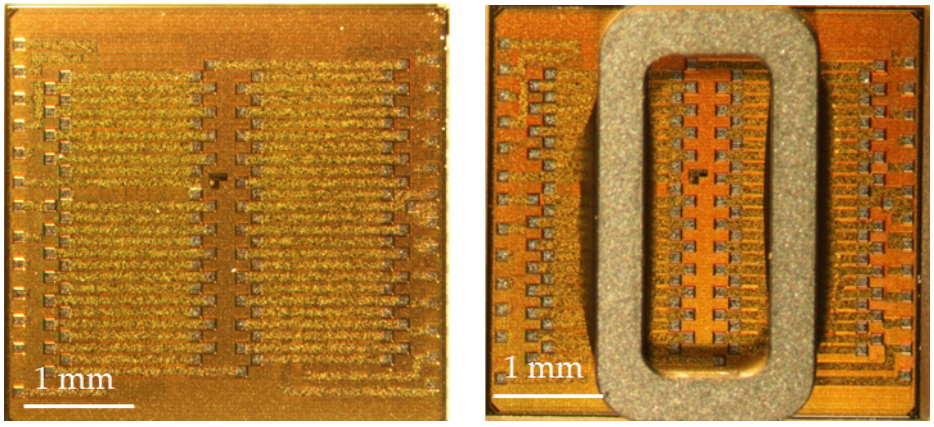


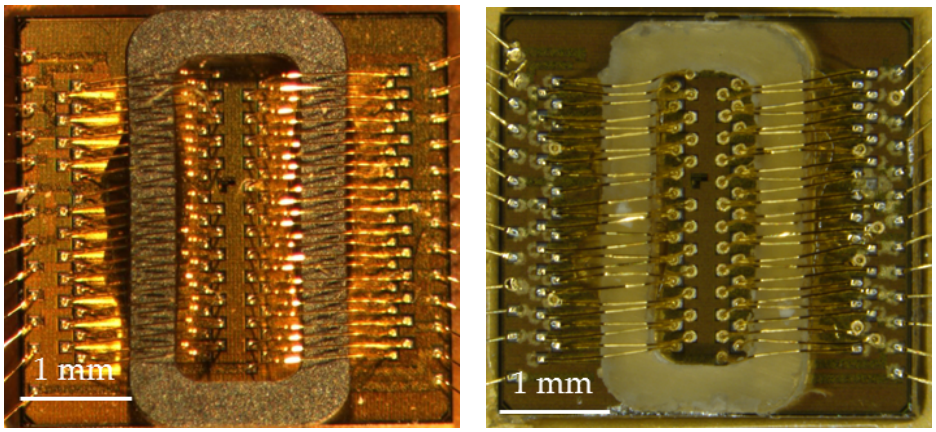
Figure 4.32: Microphotographs of the thick metal layout (on the left), and of the transformer with the 40012 LTCC core mounted on-top of the die (on the right).

mold to 31.8 µH with 40012 core. The primary series resistance R_{11}^{DC} ranges from 0.24 Ω for the epoxy mold to 0.30 Ω for the 40012 core, while the secondary series resistance R_{22}^{DC} ranges from 14.8 Ω for the 40012 core to 11.9 Ω for the epoxy mold. The equivalent saturation current I_{max} is equal to 4.89 A for the 40012 core while there is no saturation for the epoxy mold. The minimum operating frequency f_{min} at $V_{1max} =$ 10 mV is 24.6 kHz. The maximum operating frequency f_{max} ranges from 2.5 MHz for 40012 core to 1.6 MHz for the epoxy mold due to skin effect in bonding wires and silicon metalizations, while the core skin depth stays higher than core thickness due to the high resistivity of LTCCs. Figure 4.34 on the facing page shows the core δ_c and metalization δ_m skin depths compared with core thickness and bonding wire diameter, respectively, for the 40012 LTCC. The power loss in the core P_c are not available because the manufacturer does not provide any core loss constants. The power loss in the windings P_w at $I_{1rms} = 50$ mA, $I_{2rms} = 1$ mA, $f_{op} = 10.0$ MHz increases from 0.76 mW for the 40012 core to 1.10 mW for the epoxy mold due to the higher AC resistance.

4.3.4 Measurement results of race-track devices

The impedance measurements are performed by using a precision LCR Meter E4980A equipped with a test leads 16048D at the University of Bologna, Cesena (IT). The LCR Meter is calibrated with open and short circuit tests (1 m cable length, single mode) to compensate the parasitic reactance of the cables, plus an AC voltage level set to 10 mV with no bias [90]. However, the measures comprise the parasitic resistance and inductance of pads and wires from chip to package which are estimated to be $\approx 0.8\,\Omega$ and ≈ 20 nH, respectively, for each coils for both devices. The devices are measured with equations presented in section 3.6.5 on page 48 revisited in section 4.2.5 on page 70 with SOS and series-coupling tests.

Figure 4.35 on page 91 compares the measured and calculated (with $f_H = 6.6$ MHz, $\Delta f_{op} = 1.6$ MHz) self-inductances and resistances of the 40012 LTCC ($\mu_{rc} = 500$). The results shows good agreement between measured and analytically predicted inductances and resistances. The measured primary self-inductance L_{11} is equal to 0.17 µH while the predicted one is close to 0.05 µH. The measured secondary self-inductance L_{22} is equal to 23 µH compared to the predicted 32 µH. This overestimated analytical



(a) 40012 LTCC core ($\mu_{rc} = 500$) and thin gold bonding wires ($d_b = 25\,\mu m$).

(b) Epoxy mold core ($\mu_{rc} = 1$) and thick gold bonding wires ($d_b = 32\,\mu m$).

Figure 4.33: Microphotographs of the bond wire transformers assembled with gold bonding wires and race-track cores on silicon substrate.

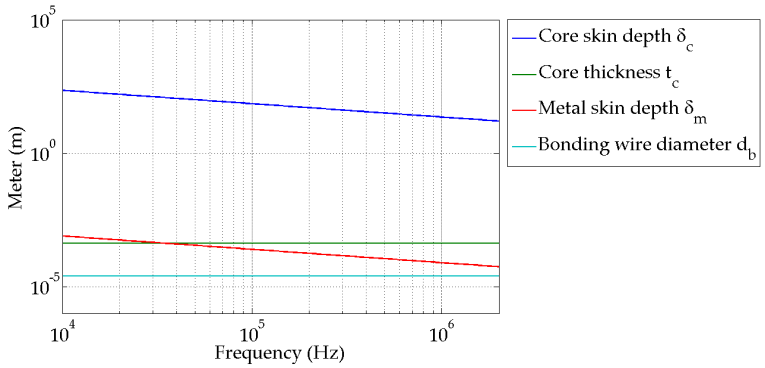


Figure 4.34: Core and metalization skin depths for the 40012 LTCC core.

inductance is due to the lack of the assumption of tightly wounded core because the lower permeability of 40012 (< 1000). The overall self-capacitances and eddy currents have no impact on the behavior of the micro-transformer in the range of frequency between 10 kHz and 2 MHz. The measured primary resistance R_{11} is equal to 1.1 Ω while the calculated one is close to 1.0 Ω. The measured secondary resistance R_{22} is equal to 13.0 Ω with respect to the calculated 15.0 Ω at low frequency. Figure 4.35 indicates further that the core loss affects the behavior of the device starting well above 1.0 MHz especially for the secondary side, while there are no self-capacitance effects in that range of frequency. The measured coupling coefficient, effective turns ratio, and quality factors of the 40012 core are reported in Figure 4.36 on page 92. The coupling coefficient k is ≈ 0.6, while the effective turns ratio n_e is ≈ 7.0. The low turns ratio is due to the parasitic inductance of pads and wires which is comparable with that of the primary winding, thus reducing the overall effective turns ratio gives in (3.96). The maximum secondary quality factor Q_{22} is 10.5 at 1.4 MHz.

Figure 4.37 on page 93 compares the measured and calculated self-inductances

Table 4.10: Modeling results of DC self-inductances and resistances, saturation, and AC analysis of the race-track bond wire transformers.

Core	40012	Dummy
L_{11}^{DC} (µH)	0.014	0.027m
L_{22}^{DC} (µH)	31.8	0.066
R_{w1}^{DC} (Ω)	0.30	0.24
R_{w2}^{DC} (Ω)	14.8	11.9
I_{max} (A)†	4.89	lin*
f_{min} (kHz) $V_{1max} = 10\,\text{mV}$	24.6	lin*
f_{max} (MHz)$^{\diamond}$	2.5	1.6
P_w (mW) $I_{1rms} = 50\,\text{mA}$ $I_{2rms} = 1\,\text{mA}$ $f_{op} = 10\,\text{MHz}$	0.76	1.10

*: linear behavior.
†: the currents in each coils are limited to 0.435 A for gold wires with diameter $d_b = 25\,\mu\text{m}$ and length $l_b = 3.0\,\text{mm}$ [81].
$^{\diamond}$: this parameter does not include capacitance effects.

and resistances of the epoxy mold ($\mu_{rc} = 1$). The measured primary self-inductance L_{11} is equal to 0.1 µH while the predicted one is close to 0.03 µH. The measured secondary self-inductance L_{22} is equal to 0.28 µH compared to the predicted 0.07 µH. The measured primary resistance R_{11} is equal to 1.0 Ω while the calculated one is 0.9 Ω. The measured secondary resistance R_{22} is equal to 11 Ω with respect to the calculated 12.0 Ω. The measured coupling coefficient, effective turns ratio, and quality factors of the epoxy mold are reported in Figure 4.38 on page 94. The coupling coefficient k and the effective turns ratio n_e are very low hence there is a poor coupling between coils. The maximum quality factors of both windings are localized at high frequencies, therefore the operating range of the air-core device is much higher than 2 MHz.

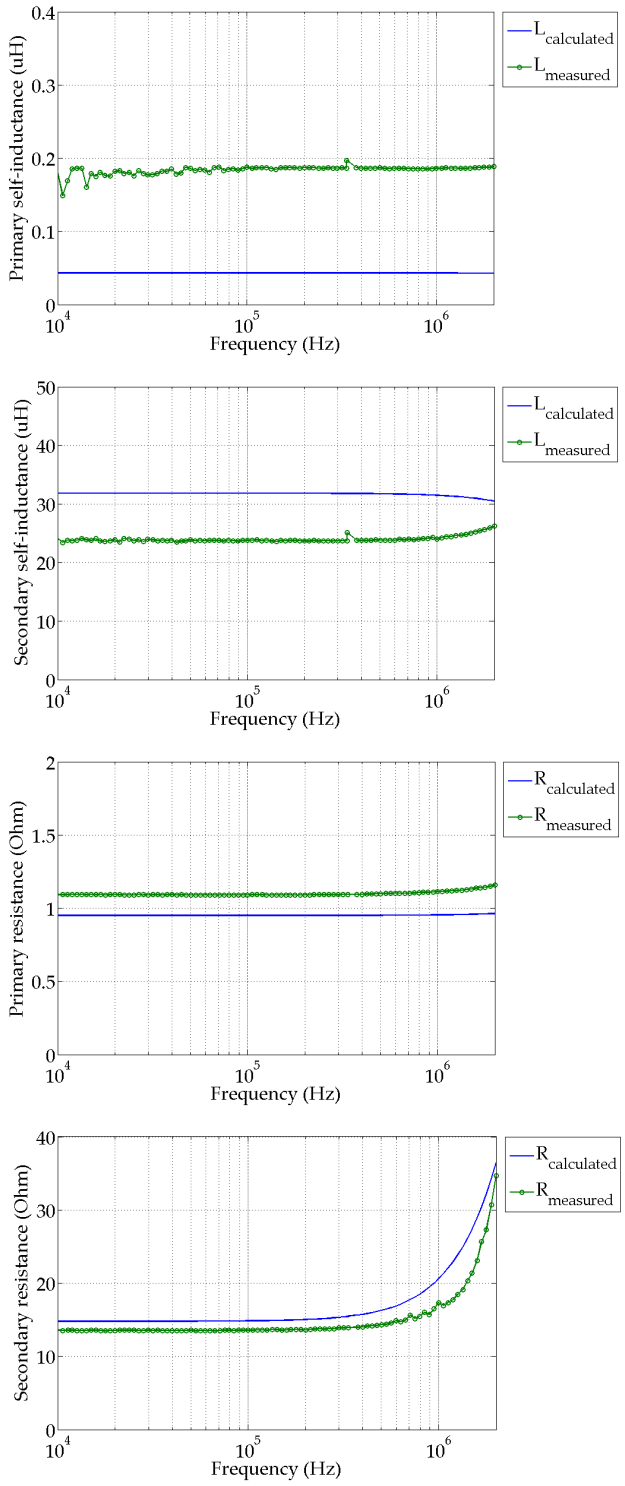


Figure 4.35: Measured and calculated self-inductances and resistances of the device assembled with 40012 core ($\mu_{rc} = 500$) and gold thin bonding wires ($d_b = 25\,\mu m$).

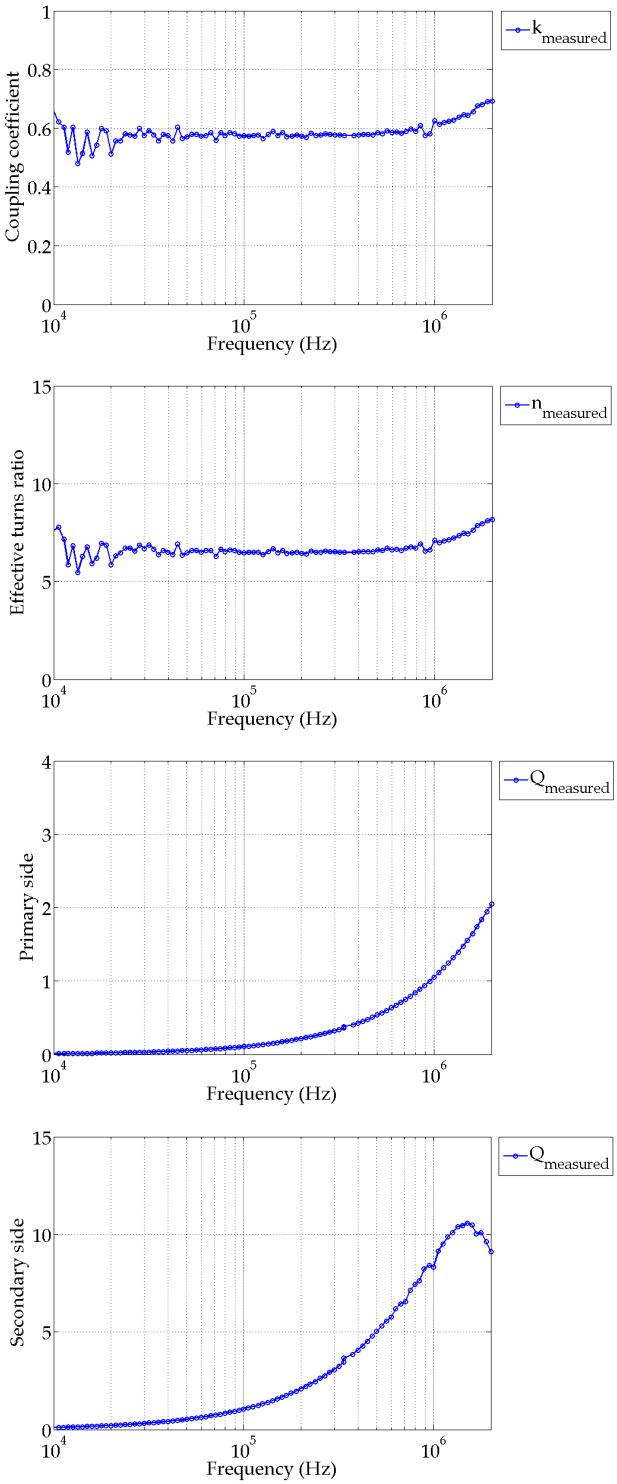


Figure 4.36: Measured coupling coefficient, effective turns ratio, and quality factors of the device assembled with 40012 core ($\mu_{rc} = 500$) and gold thin bonding wires ($d_b = 25\,\mu\text{m}$).

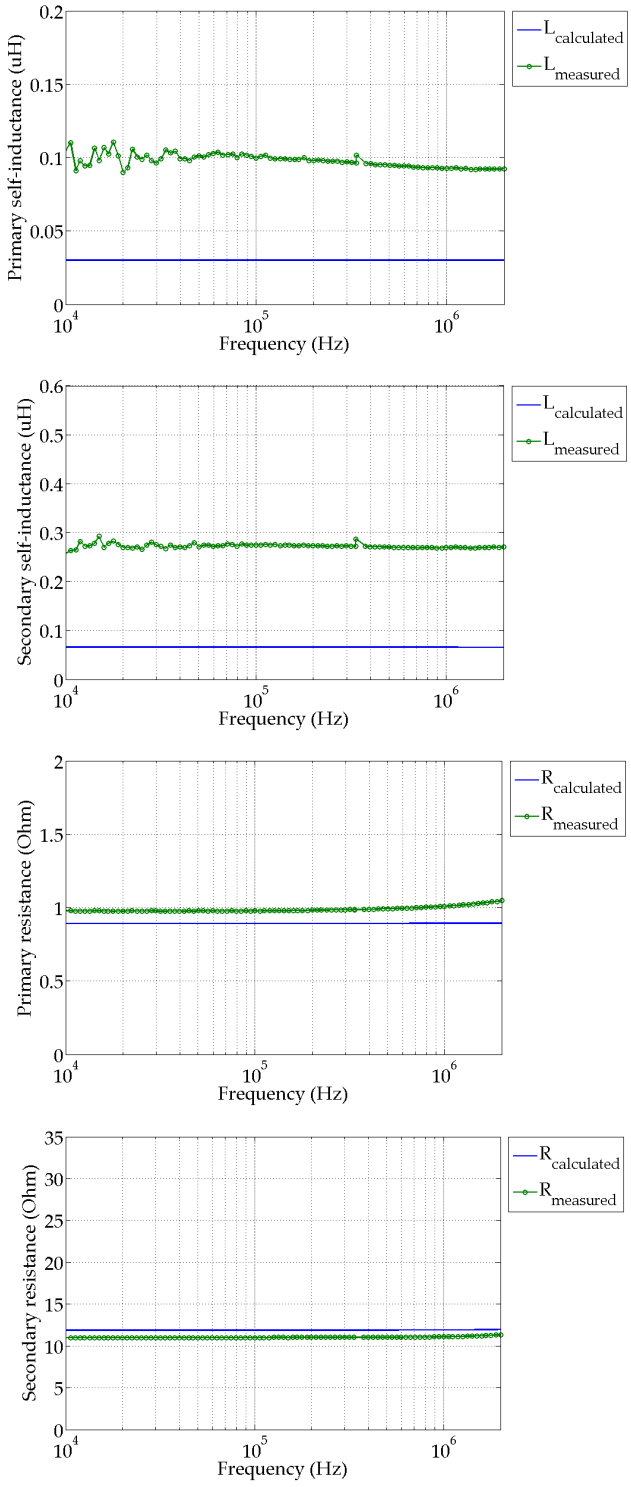


Figure 4.37: Measured and calculated self-inductances and resistances of the device assembled with epoxy mold core ($\mu_{rc} = 1$) and gold thick bonding wires ($d_b = 32\,\mu m$).

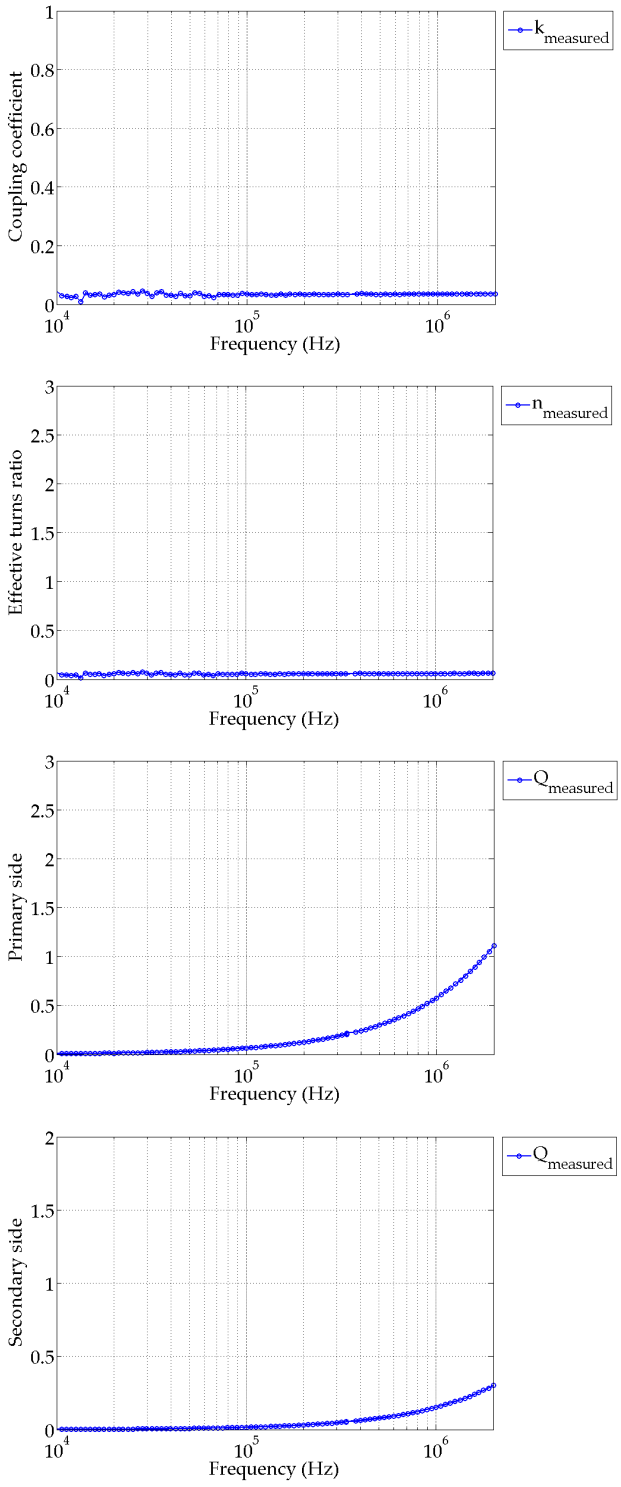


Figure 4.38: Measured coupling coefficient, effective turns ratio, and quality factors of the device assembled with epoxy mold core ($\mu_{rc} = 1$) and gold thick bonding wires ($d_b = 32\,\mu\text{m}$).

Chapter 5

Low power energy harvesting systems

5.1 Introduction

Energy harvesting is the process utilized to extract energy from the environment, store that energy, and use it to supply low power and low voltage circuits. TEGs provide a good solution for battery-less Wireless Sensor Nodes (WSN)s and EH applications. TEGs consist of arrays of thermocouples containing a p-type and n-type semiconductor connected electrically in series and thermally in parallel. Because of the Seebeck effect, the output voltage of a TEG is proportional to the number of thermocouples and to the temperature difference between cold and hot side [79]. TEGs with output voltages up to hundreds $\mathrm{mV\,K^{-1}}$ have been developed with microelectronic processes [5], which allow to integrate high numbers of miniaturized thermocouples, with overall electrical resistances in the order of hundreds Ω. However, TEGs generally deliver ultra-low voltage outputs in the range from 10 to $50\,\mathrm{mV\,K^{-1}}$ and present very low resistances usually lower than 1 Ω. Hence for body applications with a temperature gradient of 2 K between body and ambience, the expected output voltage is lower than 100 mV.

Generally, in standard CMOS technologies 100 mV is lower than the typical threshold voltage of a mosfet, and many design and efficiency issues would arise in power conversion in deep sub-threshold regions. Some circuits use external battery which improves the overall efficiency, but in fact since WSNs are generally located where maintenance is difficult, starting them manually and replacing the battery can be difficult, therefore they are not suitable for fully autonomous systems [78]. However, specific ultra-low voltage DC-DC converters are required in order to take advantage of the low voltages available from TEGs, to kick start battery-less electronic systems, and to produce functional higher output voltages appropriate for standard CMOS technologies and circuits.

5.2 Low voltage DC-DC architectures for TEG sources

In the actual state-of-the-art several architectures of low voltage DC-DC converters are implemented using TEG sources. As reported in [17], analog step-up oscillator architectures based on the Armstrong topology have been proposed. However, the

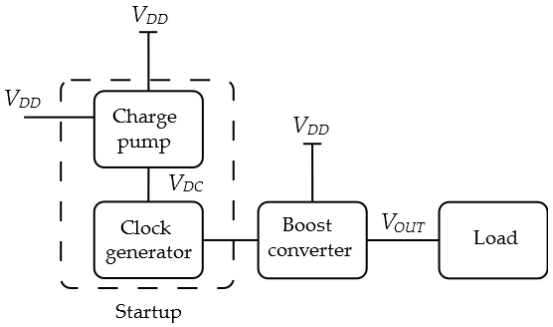


Figure 5.1: Boost converter circuit with a charge pump.

startup of this kind of circuits requires a normally-on device with a high resistance compared to the internal TEG resistance which represents a limitation in the achievable output power to levels far below the ideally available power. The first approach to overcome this issue is to realize the startup circuit separately from the main power conversion block, so that high efficiency classical DC-DC converter topologies can be used. The second option is to implement an unique solution with the startup circuit merged with the main DC-DC converter in order to decrease the number of devices thus limiting the cost and improving the reliability. The third approach is to design new architectures and circuits specifically developed for low voltage operations. The main architectures using the first approach are boost topologies implemented with charge pumps, mechanical switches, and analog transformer startup. The main structures using the second approach are generally based on synchronous boosts, flyback converters, and analog coupled inductors schemes. New architectures using the third approach are boost converters with transformer-reuse scheme and step-up oscillators with voltage doubler circuits. Besides this, a series of commercial devices is available on the market. In this context, low voltage and low power DC-DC converters for TEG sources require precise design consideration and key metrics such as: startup capability, high efficiency, minimum power consumption, Maximum Power Point Tracking (MPPT) capability, low minimum input voltage, high maximum output voltage, battery-less approach, and single-chip integration [17, 26, 48].

5.2.1 Startup and DC-DC converter separately

The charge pump is one of the most common architecture of boost topology. A first example is the 0.18 V input voltage charge pump reported in [9]. The proposed circuit uses a 3-stage charge pump based on voltage doubler structure with the addition of forward body biasing to every mosfets. The circuit is separately implemented with a clock generator to produce the clock signal with high duty cycle which drives the last boost converter stage. Figure 5.1 shows the overall architecture. A prototype is fabricated using a 65 nm standard CMOS process showing an output voltage of 0.74 V at 6 mA output current, with two off-chip capacitors. A second example is the 95 mV charge pump reported in [11]. The starter circuit is based on a threshold-tuned oscillator by fixed charge programming to compensate process variations, and on a 20-stage Dickson charge pump. The circuit implements an improved version of [9] by using a capacitor pass-on scheme capable to convert an input voltage down to 100 mV to 0.9 V output at 0.9 mA load current. A test chip is fabricated with 65 nm standard

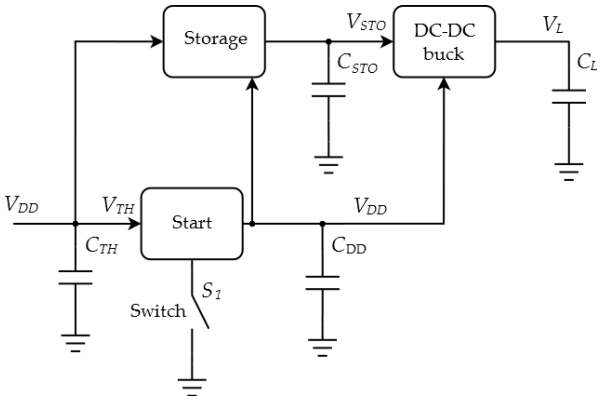


Figure 5.2: Harvesting circuit with a motion activated switch.

CMOS technology. Despite the very low voltage input, the circuit requires one off-chip capacitor and one off-chip inductor and an additional fabrication process which increases the cost. As a third example, charge pumps implemented in standard CMOS processes that operate with input voltages down to 120 mV have been reported. In [66] an 8-stage charge pump architecture with a clock oscillator and a buffer circuit supplies a 1.6 V output with a 300 mV input with low current and peak efficiency of 23%. A single-chip with no external component is implemented in a 0.18 µm UMC CMOS process and tested successful. Similar results have been reported with a 65 nm CMOS process in [10], with a higher efficiency up to 38.8%.

An alternative approach, with separate startup and power converter circuits, is to rely on mechanical vibration for the activation. An example is the 35 mV battery-less TEG harvesting circuit with the mechanically assisted startup scheme described in [76]. The energy required for the initial activation is extracted from the TEG by a mechanically actuated switch controlling a boost converter. The overall architecture, shown in Figure 5.2, is based a storage buffer circuit and a DC-DC converter with MPPT. A prototype is fabricated using a 0.35 µm CMOS process and generates a regulated output voltage of 1.8 V with a peak conversion efficiency of 58%.

The analog transformer is another typical structure of a boost topology. An example of startup and boost converter circuits based on a resonant transformer scheme capable of starting from 0.3 V is reported in [16]. The complete circuit is divided in several blocks: the starter circuit to initialize the conversion, the main circuit based on a modified boost converter which provides the output voltage with high efficiency, and two stages of switching and supply circuits. In prototype tests, the author claimed a peak efficiency of 76% and a maximum stable output voltage of 5 V for 131 mW output load.

5.2.2 Startup and DC-DC converter merged

Synchronous and flyback boost converters are example of merged architectures. An example of switched-mode boost converter is reported in [8] capable to step-up voltages between 20 and 250 mV to a controllable output voltage of 1 V at 10 µW load. The converter is fabricated with 0.13 µm CMOS process and has an efficiency of 75% for 100 mV input. However, the circuit needs a 600 mV minimum voltage for the startup and requires some off-chip components such as an inductor and two filter

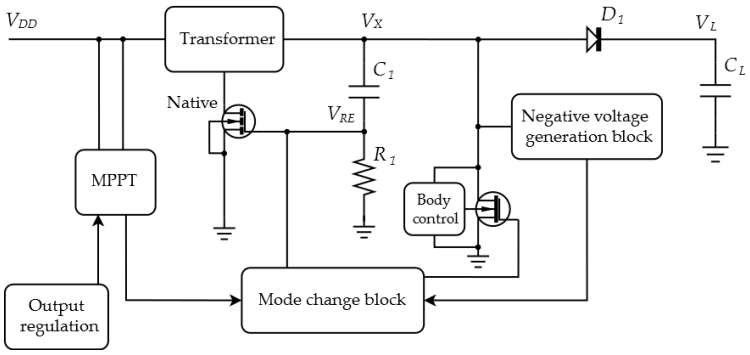


Figure 5.3: Harvesting circuit with transformer based oscillator and MPPT.

capacitors.

Another common architectures used for energy harvesting circuits are step-up oscillators based on cross-coupled inductors. A first example is the 116 mV step-up converter based on coupled inductors described in [60]. The circuit is based on analog transformer scheme and two parallel switching transistors: one used for the starting, and one used for steady state operation. The converter has an efficiency of about 70% for input voltages of 300 mV. A second example for up-converting low-voltages coming from TEGs is the 70 mV step-up converter described in [74]. The converter is characterized by an efficiency of 70% for an input voltage between 200 to 500 mV and an output voltage of 2 V, and is capable to deliver an output power of 5 mW with an input voltage of 300 mV. A small prototype is realized and tested with PCB process. A third example of 0.3 V converter based on coupled inductors is shown in [18] for harvesting energy from Microbial Electric Generator (MEG)s. The converter is adapted from a classical boost topology and includes an oscillating circuit and a simple analog MPPT regulation. The harvested power is 10 mW under a minimum input voltage of 0.3 V. A PCB prototype is realized with a measured efficiency of 74% and a maximum output voltage of about 2 V depending on load conditions.

5.2.3 Novel architectures

Recent approaches for energy harvesting from TEG sources are based on a modified versions of step-up oscillators which use voltage doubler circuits and transformer with boost converters. In [34] a startup converter is proposed capable to start from 6 mV and 82 µA input current and to achieve an output voltage of 1 V. The circuit uses seven cascade print transformers and a rectifier to startup the circuit with a maximum efficiency of 18%. The authors claim the implementation of a discrete prototype with an input voltage of 12 mV and a power consumption of 2.7 µW. Another interesting architecture presented in [40] is the transformer-reuse self-starting boost converter with low-power MPPT control for low-voltage TEG applications. Figure 5.3 shows the overall architecture. The minimum working voltage of the boost converter is 40 mV with oscillation through a positive feedback loop formed by a normally-on mosfet and a transformer. This work suggests a new boost converter architecture which utilizes a transformer for both self-startup function and high efficiency power transfer. A prototype chip is implemented in a 0.13 µm CMOS process, and it operates with an input voltage range from 40 to 300 mV while providing a maximum output power of 2.7 mW with a maximum efficiency of 61% at an output voltage of 2 V. However, the

converter requires an off-chip transformer and several external signals.

Another new architecture is the third circuit proposed in [17] which is a step-up oscillator with a Greinacher voltage-lift. The circuit is very similar to the [34] and starts from 0.3 V while providing an efficiency of 66.5% with an energy transfer both directly and indirectly to the load. A recent work is the fully eletrical 50 mV 3-stage stepping-up architecture proposed in [100]. The converter is composed by four functional blocks and is able to provide an output voltage of 1.2 V with a minimum input voltage of 50 mV and a measured peak efficiency of 73%. However, the converter uses some external smd inductors. A new battery management is reported in [43] with a cold start circuit based on a powered boost converter capable to start from 330 mV, while [19] shows an integrated charge pump realized with 0.35 µm standard CMOS process with very low power consumption and minimum input voltage of 0.6 V. However, the converter requires a 2 V battery for the startup. Finally, an innovative boost converter with Zero-Current Switching (ZCS) scheme is reported in [47] with MPPT and peak efficiency of 72%. On the other hand, the converter needs an external battery for the startup and an off-chip inductor.

5.2.4 Commercial products

Several solutions for low power and low voltage circuits are present in the market. A first solution is the LTC3108 [92] from Linear Technology. The LCT3108 uses a normally-on mosfet and a resonant oscillator scheme with an external step-up transformer (es. [12]) to convert from an ultra-low input voltage. This allows boosting input voltages as low as 20 mV using a transformer with a ratio of 1 : 100 while giving multiple regulated output voltages for powering other circuits. The startup oscillator is coupled with an external charge pump capacitor and a rectifier which act as a boost converter thus providing an output voltage from 2.35 to 5 V and high efficiency. LTC3108 can operate with varies voltage sources such as TEGs, thermopiles, and photovoltaic cells. A second solution is the S-882Z series [80] charge pump for the startup of step-up converters from Seiko. The charge pump differs from conventional ones since it utilizes fully depleted silicon on insulator technology thus enabling ultra-low voltage operations. The S-882Z is based on a charge pump and an oscillator circuit and is capable to start the conversion from input voltage of 0.3 V with an external startup capacitor and deliver from 1.8 to 2.4 V to the output. Another example is the step-up converter ECT 310 [23] from EnOcean designed for powering radio modules in sensors and actuators. ECT 310 can start from 20 to 50 mV input voltage relate to the typical output of a TEG module with 2 K temperature gradient, and deliver an output voltage between 3 to 4 V with an efficiency of 30%. The last solution is the Micropelt TE-Core module [64] capable to provide outputs between 1.8 and 4.5 V with high efficiency.

5.3 Design of DC-DC converters with micro-magnetics

The constant drive headed for reducing the size of electronic products, from portable to high-performance electronics, is one of the major challenges on power management platforms. The self-startup is one of the most critical issues for battery-less and low input voltage DC-DC converters for EHs [58].

The proposed circuit is a low-voltage DC-DC converter based on a resonant oscillator with a bond wire micro-transformer. The resonant oscillator part is composed

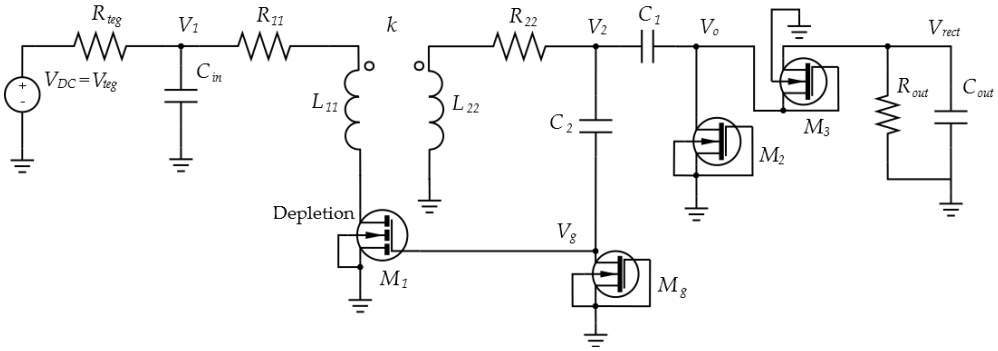


Figure 5.4: Circuit diagram of the first version of DC-DC converter with micro-transformer.

by a transformer and a depletion nmosfet, while the last stage is a voltage doubler. The converter has a self-startup capability from very low-voltage and is designed in 0.32 µm BCD6s technology at STMicroelectronics. This section shows the large-signal and small-signal analysis of the converter. The analytical analysis and static characterization are presented to evaluate the startup capability of the converter. Finally, the simulation and experimental results are discussed.

5.3.1 Large-signal analysis

The converter is based on a Meissner oscillator topology with a bond wire micro-transformer. Two different versions of oscillator are designed and fabricated on silicon substrate. Figure 5.4 shows the circuit diagram of the first version of the proposed DC-DC converter. The low-voltage source is represented by a TEG with a DC voltage $V_{DC} = V_{teg}$ (V) and an internal series resistance R_{teg} (Ω). A filter capacitor $C_{in} = 630$ pF is added to reduce the equivalent source impedance. The micro-transformer is modeled by the self-inductances L_{11} (H) and L_{22}(H), the series resistances R_{11}(Ω) and R_{22}(Ω), and the coupling coefficient k. The depletion nmos M_1 is designed with channel width $W = 2$ mm and length $L = 0.8$ µm, and is chosen due to its normally-on state and negative threshold voltage $V_{tn} = -0.882$ V compared to conventional enhancement nmosfets. The coupling capacitor $C_2 = 150$ pF and M_1 provide the positive feedback to the transformer, while the nmos diode-connected M_g with $W = 8$ µm, $L = 0.8$ µm and $V_{tn} = 0.65$ V behaves as a leakage to avoid charge building up on M_1 gate. Two depletion nmos and two coupling capacitors with same values can be added in parallel to M_1 and C_2, respectively, to improve the startup capability. In order to analyze the converter, the gate-source capacitance C_{gs} (F) of M_1 should be considered due to its effect on the startup condition.

Initially, the converter is connected to the DC source V_{DC} which increases the current I_1 (A) through the primary winding and the normally-on ($V_{gs} \approx 0$ V) nmos depletion. Hence, a positive voltage V_2 (V) is induced at the secondary winding, which gives a positive feedback over the coupling capacitor C_2 by rising the V_{gs} of M_1 ($V_{gs} > 0$ V). Once the current at the primary coil reaches saturation, the voltage V_2 starts to drop reducing the V_{gs} of M_1, which lowers the drain current I_1, thus decreasing again the V_2 and so on, by a loop until M_1 is driven near its off-state ($V_{gs} < 0$ V). Initial energy is delivered by the current stored in the primary winding which provides a positive current I_1 through M_1 [16]. Therefore, a positive voltage V_2 is induced at the secondary coil which increases the V_{gs} ($V_{gs} \approx 0$ V) causing M_1

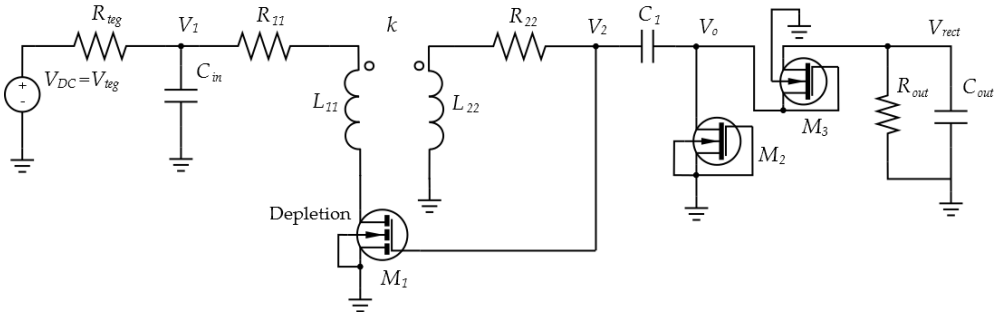


Figure 5.5: Circuit diagram of the second version of DC-DC converter with micro-transformer.

to become more conductive again, so that the oscillation process starts again. The nmos depletion acts as a controlled resistor switched between the on-state (low on-resistance) and off-state (high on-resistance), which modulates the current I_1 over the primary winding.

The last stage is a voltage doubler composed by the pump capacitor $C_1 = 150\,\text{pF}$ and the two diode-connected nmos M_2 and M_3 with $W = 8\,\mu\text{m}$, $L = 0.8\,\mu\text{m}$ and $V_{tn} = 0.65\,\text{V}$. Two pump capacitors with same values can be added in parallel to C_1 to improve the performance of the converter. However, too large value of C_1 can compromise performance when operating at low input voltages or with high source resistances R_{teg}. The load is composed by a storage capacitance $C_{out} = 22\,\text{nF}$ and a load resistance $R_{out} = 100\,\text{M}\Omega$.

The second version of the proposed DC-DC converter is shown in Figure 5.5. The main difference with the first version is the short of the coupling capacitor C_2 and the absence of the leakage nmos M_g. The large-signal analysis is the same of the first version.

5.3.2 Small-signal analysis

The active part of the oscillator is formed the depletion nmos M_1 while the passive part is represented by self-inductances L_{11} and L_{22} and capacitances C_1, C_2, and C_{gs}. Since M_1 is connected in series with the primary winding of the transformer, the drain-source voltage $V_{ds}\,(\text{V})$ has small values compared to $V_{ov} = V_{gs} - V_{tn}$. Therefore, M_1 works always in triode mode (linear region) as a controlled resistor for low V_{teg}. The drain current $I_{ds}\,(\text{A})$ in linear region is defined as follows:

$$I_{ds} = \beta_n \left[(V_{gs} - V_{tn})\, V_{ds} - \frac{V_{ds}^2}{2} \right], \tag{5.1}$$

where $\beta_n = \mu_n\, C_{ox}\, W/L\,(\text{A V}^{-2})$ is the beta factor with $\mu_n\,(\text{m}^2\,\text{V}^{-1}\,\text{s}^{-1})$ as the electron mobility, W/L is the form factor, and $C_{ox} = \epsilon_{ox}/t_{ox}\,(\text{F m}^{-2})$ is the gate-oxide capacitance. The term $\epsilon_{ox} = \epsilon_0 \cdot \epsilon_r\,(\text{F m}^{-1})$ is the overall permittivity with $\epsilon_0 = 8.86 \cdot 10^{-12}\,(\text{F m}^{-1})$ as the free-space permittivity and $\epsilon_r = 3.9$ as the oxide relative permittivity, while $t_{ox} = 1.83 \cdot 10^{-8}\,(\text{m})$ is the thickness of the gate oxide. The output transconductance $g_{ds}\,(\text{S})$ is extracted by making the derivative of (5.1) with respect to V_{ds} thus obtaining:

$$g_{ds} = \frac{d\, I_{ds}}{dV_{ds}} = \beta_n\, (V_{gs} - V_{tn} - V_{ds}), \tag{5.2}$$

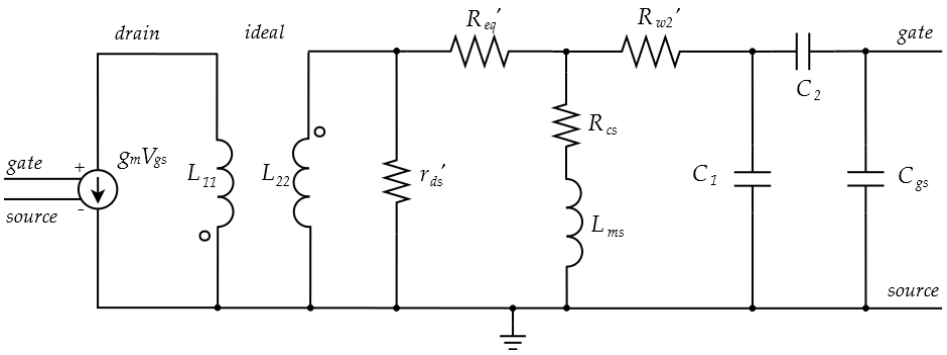


Figure 5.6: Small-signal circuit diagram of the resonant oscillator of the first version of DC-DC converter with series core loss.

while the nmos transconductance g_m (S) is evaluated by performing the derivative of (5.1) with respect to V_{gs} thus getting:

$$g_m = \frac{d\, I_{ds}}{dV_{gs}} = \beta_n\, V_{ds}. \tag{5.3}$$

Equation (5.3) shows that after fixing the intrinsic parameters such as μ_n, C_{ox}, and W/L, the transconductance g_m depends only on the V_{ds} value. The M_1 on-resistance r_{ds} (Ω) can be derived by computing the inverse of g_{ds} as:

$$r_{ds} = \frac{1}{g_{ds}}, \tag{5.4}$$

while the gate-source capacitance C_{gs} (F) in the triode mode is defined as:

$$C_{gs} = \frac{C_{ox}\, W\, L}{2}. \tag{5.5}$$

In order to analyze by small signals the resonant oscillator, the micro-transformer is modeled by L_{ms}, R_{w1}, R_{w2}, n_{12}, $R_{cs} = R_c\, n_{12}^2$, and k as discussed in section 3.5.6 on page 41 and 3.6.5 on page 48. The leakage inductances L_{l1} and L_{l2} are considered negligible compared to the other impedances, while the self-capacitances C_1 and C_2 are neglected. Figure 5.6 shows the small-signal circuit diagram of the resonant oscillator block with the V_0 node grounded of the first version of DC-DC converter with series core loss [2]. The total primary winding resistance R_{eq} (Ω) can be defined as:

$$R_{eq} = R_{teg} + R_{w1} + R_{con1}, \tag{5.6}$$

where R_{con1} (Ω) is the parasitic resistance of extra-connections. As shown in (3.36), R_{eq} can be referred at the secondary side thus getting R'_{eq} (Ω) defined by:

$$R'_{eq} = R_{eq}\, n_{12}^2. \tag{5.7}$$

Similarly, the total secondary winding resistance R'_{w2} (Ω) can be obtained as:

$$R'_{w2} = R_{w2} + R_{con2}, \tag{5.8}$$

where $R_{con2}\,(\Omega)$ is the parasitic resistance of extra-connections. The equivalent capacitance $C_{eq}\,(\mathrm{F})$ at the secondary side is defined as:

$$C_{eq} = C_1 + \frac{C_{gs}\,C_2}{C_{gs} + C_2}. \tag{5.9}$$

In addition the following capacitive ratio $C_k\,(\mathrm{F}^{-1})$ must be considered:

$$C_k = \frac{C_2}{C_{gs}\,C_2 + C_{gs}\,C_1 + C_1\,C_2}. \tag{5.10}$$

Finally, the on-resistance in (5.4) can be referred to the secondary side thus obtaining $r'_{ds}\,(\Omega)$ as:

$$r'_{ds} = r_{ds}\,n_{12}^2. \tag{5.11}$$

The startup requirements are calculated by considering the Barkhausen criterion which implies that the transfer function, formed by the product of the active part and passive part, must be equal to unity to reach and self-sustain the oscillation. This means further that the magnitude of the transfer function must be greater than 1 while its phase shift must be equal to 0 °C or a multiple of 360 °C [2, 32]. From the small-signal analysis, the oscillation frequency $f_0\,(\mathrm{Hz})$ of the converter is obtained as:

$$f_0 = \frac{1}{2\,\pi}\sqrt{\frac{L_{ms}\,(r'_{ds} + R'_{eq} + R_{cs}) - R_{cs}\,(C_{eq}\,R_t + L_{ms})}{L_{ms}^2\,C_{eq}\,(r'_{ds} + R'_{eq} + R'_{w2})}}, \tag{5.12}$$

where $R_t\,(\Omega^2)$ is given by:

$$R_t = R_{cs}\,r'_{ds} + R'_{w2}\,r'_{ds} + R_{cs}\,R'_{eq} + R'_{w2}\,R'_{eq} + R'_{w2}\,R_{cs}. \tag{5.13}$$

If $R_{22} \approx R'_{w2}$ hence $R_{cs} \ll R'_{w2}$ equation (5.12) can be simplified to:

$$f_0 = \frac{1}{2\,\pi}\sqrt{\frac{r'_{ds} + R'_{eq}}{L_{ms}\,C_{eq}\,(r'_{ds} + R'_{eq} + R'_{w2})}}. \tag{5.14}$$

If $r'_{ds} + R'_{eq} \gg R'_{w2}$ equation (5.14) can be reduced to the general expression of the resonant frequency of LC-circuits [32] as:

$$f_0 \approx \frac{1}{2\,\pi\,\sqrt{L_{ms}\,C_{eq}}}, \tag{5.15}$$

which depends on L_{ms} and on C_{eq}. The startup condition is obtained by evaluating the minimum nmos transconductance $g_{m0}\,(\mathrm{S})$ as follows:

$$g_{m0} = \frac{n_{12}}{C_k\,L_{ms}\,r'_{ds}\,C_{eq}} \cdot \frac{(C_{eq}R_t + L_{ms})[R_{cs}^2 L_{ms} C_{eq}(r'_{ds} + R'_{eq} + R'_{w2}) + L_{ms}(R'_{eq} + r'_{ds}) - R_{cs}C_{eq}R_t]}{L_{ms}(R'_{eq} + r'_{ds}) - R_{cs}C_{eq}R_t + C_{eq}R_{cs}^2(r'_{ds} + R'_{eq} + R'_{w2})}. \tag{5.16}$$

As for f_0, if $R_{cs} \ll R'_{w2}$ equation (5.16) can be condensed to:

$$g_{m0} = \frac{n_{12}}{C_k\,L_{ms}\,r'_{ds} C_{eq}} \cdot C_{eq}(R'_{eq}\,R'_{w2} + r'_{ds}R'_{w2}) + L_{ms}. \tag{5.17}$$

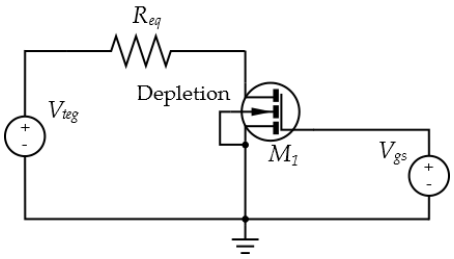


Figure 5.7: Circuit diagram for the static characterization of the depletion nmos.

If r'_{ds} is higher than the other impedances equation (5.17) can be simplified to:

$$g_{m0} \approx \frac{n_{12}\, R'_{w2}}{C_k\, L_{ms}}, \tag{5.18}$$

or in terms of minimum drain-source voltage V_{ds0} (V):

$$V_{ds0} = \frac{g_{m0}}{\beta_n}. \tag{5.19}$$

From (5.19) is possible to calculate the minimum source voltage V_{teg0} (V) as described below:

$$V_{teg0} = -V_{ds0}^2 \frac{R_{eq}\,\beta_n}{2} + V_{ds0}\,(1 - R_{eq}\,\beta_n\,V_{tn}), \tag{5.20}$$

hence, the Barkhausen criterion is fulfilled if:

$$g_m \geq g_{m0} \qquad \text{or} \qquad V_{ds} \geq V_{ds0}. \tag{5.21}$$

Equations (5.21) represent the startup condition to reach and maintain the oscillation. If $g_m \gg g_{m0}$ or $V_{ds} \gg V_{ds0}$ the converter starts to oscillate exponentially, while if $g_m \geq g_{m0}$ or $V_{ds} \geq V_{ds0}$ the converter starts to oscillate sinusoidally. The small-signal analysis of the second version of DC-DC converter is similar to that of the first one. Only equations (5.9) and (5.10) change by shorting the coupling capacitor ($C_2 \sim \infty$), thus getting:

$$C_{eq} = C_1 + C_{gs}, \tag{5.22}$$

$$C_k = \frac{1}{C_1 + C_{gs}} = \frac{1}{C_{eq}}. \tag{5.23}$$

5.3.3 Static characterization

The startup requirements depend on the nmos transconductance, hence a static analysis is performed with Cadence Design Systems to characterize M_1 for one and two parallel nmos. The simplified circuit diagram for the static analysis is shown in Figure 5.7. The source is represented by V_{teg} and R_{eq} obtained in (5.6). Figure 5.8 on the facing page shows the simulated V_{ds} of a single (top graph) and two parallel (bottom graph) nmos depletion for $V_{gs} = 0\,\text{V}$ as a function of V_{teg} which varies from 0 to 200 mV, with a parametric sweep on R_{eq} from 0.5 to 10 Ω.

Figure 5.9 on page 106 shows the simulated static curves of a single nmos depletion for $R_{eq} = 0\,\Omega$ as a function of V_{gs} which varies from −2 to 2 V. The top graph shows the drain current I_{ds} while the bottom graph shows the transconductance g_m shown

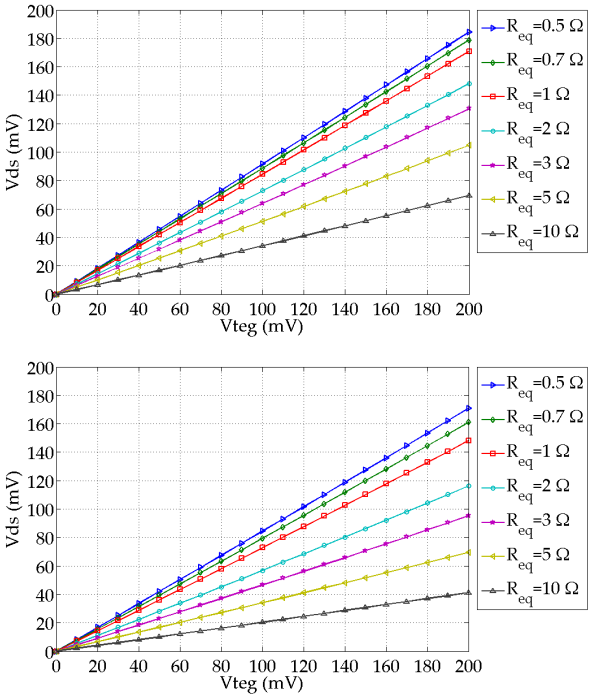


Figure 5.8: Simulated V_{ds} versus V_{teg} for single (top graph) and two parallel (bottom graph) nmos depletion for $V_{gs} = 0\,\text{V}$ with a parametric sweep on R_{eq}.

in (5.3), both with a parametric sweep on $V_{ds} = V_{teg}$ from 10 to 100 mV with a 10 mV step. For an input voltage of $V_{ds} = 40\,\text{mV}$, the bottom graph of Figure 5.9 shows that g_m reaches the maximum value of 7.0 mS at $V_{gs} = -0.45\,\text{V}$ (near cut-off), while for greater V_{gs} the transconductance decreases as the I_{ds} become stabilized. Figure 5.10 on page 107 shows the g_m of a single (top graph) and two parallel (bottom graph) nmos depletion with respect to the V_{teg} which varies from 10 to 100 mV, with a parametric sweep on R_{eq} from 0.5 to 10 Ω. The values are extracted by choosing the g_m values at $V_{gs} = 0\,\text{V}$ due to the DC behavior of the M_1 gate node connected to the leakage nmos M_g, as shown in Figure 5.4 on page 100, which holds the gate node close to ground voltage. The addition of one (or more) parallel nmos depletion allows to rise the g_m only for small values of R_{eq} due to the growth of the parasitic capacitance C_{gs}.

Figure 5.11 on page 107 shows the simulated static curves of a single nmos depletion for $R_{eq} = 0\,\Omega$ versus $V_{ds} = V_{teg}$ which varies from 10 to 100 mV. The top graph shows the drain current I_{ds} while the bottom graph shows the transconductance g_{ds} shown in (5.2), both with a parametric sweep on V_{gs} from −2 to 2 V with a 0.4 V step. The top graph of Figure 5.11 shows that M_1 is off until V_{gs} reaches the threshold voltage V_{tn}, while for greater V_{gs} it works always in the triode mode due to the reduced V_{ds} values, as shown in the bottom graph of Figure 5.11. Figure 5.12 on page 108 shows the g_{ds} of a single (top graph) and two parallel (bottom graph) nmos depletion as a function of the V_{teg} which varies from 10 to 100 mV, with a parametric sweep on R_{eq} from 0.5 to 10 Ω. The values are extracted by choosing the g_{ds} values for $V_{gs} = 0\,\text{V}$ as discussed before. The addition of one (or more) parallel nmos depletion allow to increase the g_{ds} thus reducing the on-resistance r_{ds}.

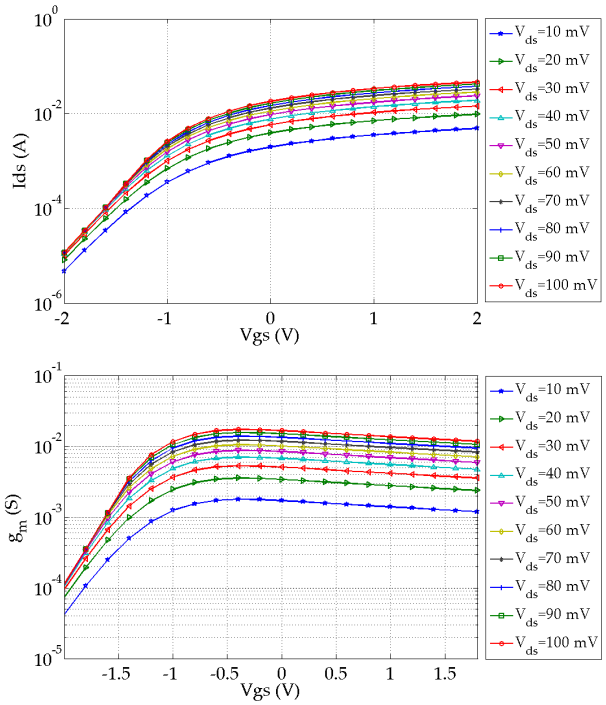


Figure 5.9: Simulated I_{ds} versus V_{gs} (top graph) and g_m versus V_{gs} (bottom graph) with a parametric sweep on $V_{ds} = V_{teg}$ of a single nmos depletion for $R_{eq} = 0\,\Omega$.

The static analysis allows to find the g_{ds} and g_m values of M_1 (single or two parallel). Later g_m can be compared with the minimum g_{m0} in (5.16) or (5.17), which satisfies the Barkhausen criterion accordingly to (5.21). Therefore, if $g_m \geq g_{m0}$ or equivalently $V_{ds} \geq V_{ds0}$, the converter reaches and maintains the oscillation at the resonant frequency f_0 given in (5.12) or (5.14).

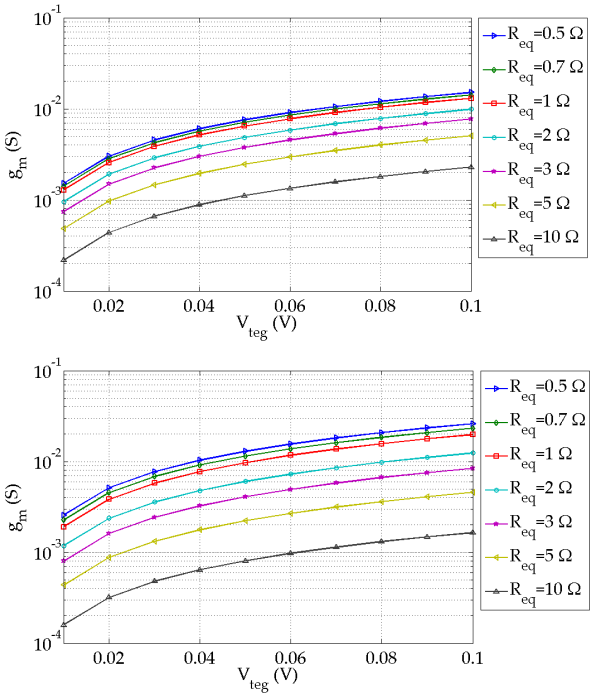


Figure 5.10: Simulated g_m at $V_{gs} = 0\,\mathrm{V}$ versus V_{teg} for single (top graph) and two parallel (bottom graph) nmos depletion with a parametric sweep on R_{eq}.

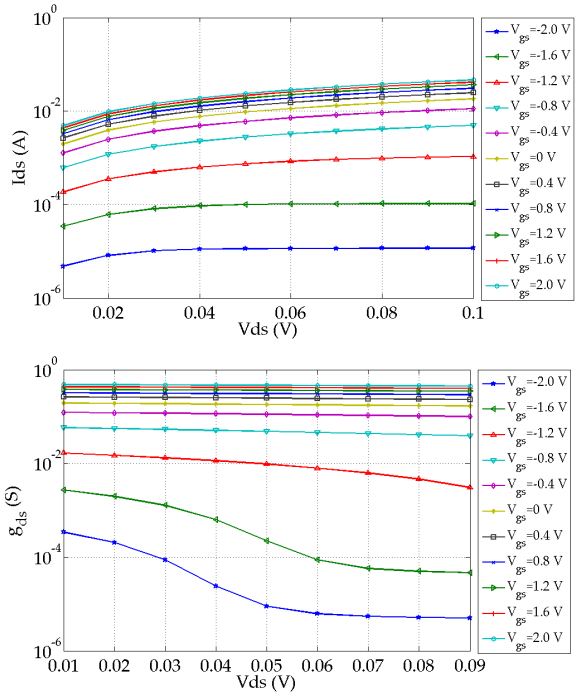


Figure 5.11: Simulated I_{ds} versus V_{ds} (top graph) and g_{ds} versus V_{ds} (bottom graph) with a parametric sweep on V_{gs} of a single nmos depletion for $R_{eq} = 0\,\Omega$.

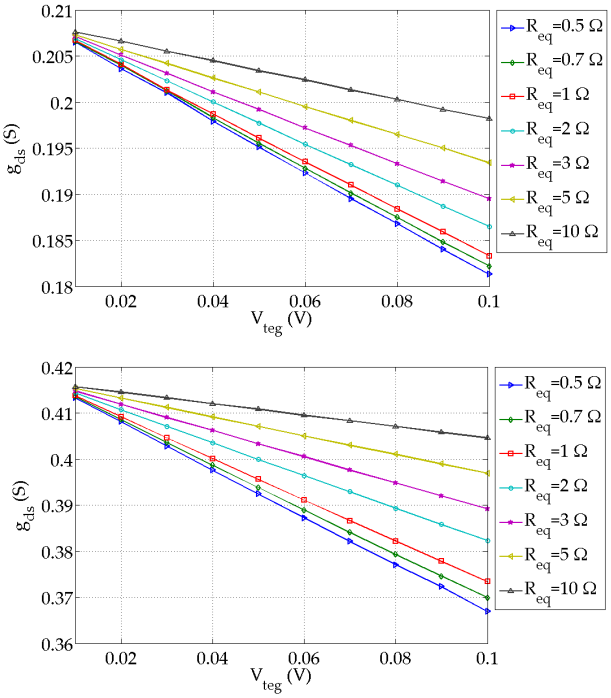


Figure 5.12: Simulated g_{ds} at $V_{gs} = 0\,\mathrm{V}$ versus V_{teg} for single (top graph) and two parallel (bottom graph) nmos depletion with a parametric sweep on R_{eq}.

5.3.4 Small-signal and simulation results

The transformer is modeled by using the measurement and analytical results of the device fabricated with 5975000801 ferrite ($\mu_{rc} = 5000$) and T_1 layout ($1:38$) on PCB shown in Figure 4.22 on page 77 and Figure 4.23 on page 78, respectively. This transformer has the highest secondary self-inductance and turns ratio which ensure maximum performance of the converter, however it has high secondary resistance. The results at $\approx 1.0\,\text{MHz}$ report $L_{11} = 0.15\,\mu\text{H}$, $L_{22} = 195\,\mu\text{H}$, $R_{w1} = 0.8\,\Omega$, $R_{w2} = 3.8\,\Omega$, $R_{cs} \approx 600\,\Omega$ and $k \approx 0.9$. The parasitic resistances of internal interconnections and gold bonding wires ($d_b = 25\,\mu\text{m}$) from chip to CLCC68 package (as discussed in section 4.2.1) are estimated to be $R_{con1} = 0.55 + 0.80 = 1.35\,\Omega$ and $R_{con2} = 1.13 + 0.80 = 1.93\,\Omega$ for the primary and secondary side, respectively.

The source is modeled with $V_{teg} = 40\,\text{mV}$, $R_{teg} = 0.43\,\Omega$ (from CP series TEG module [91]), while the nmos depletion M_1 is modeled at $V_{gs} \approx 0\,\text{V}$ with $C_{ox} = 0.0019\,\text{F m}^{-2}$, $W = 2\,\text{mm}$, $L = 8\,\mu\text{m}$, $\mu_n = 0.0451\,\text{m}^2\,\text{V}^{-1}\,\text{s}^{-1}$, $V_{tn} = -0.882\,\text{V}$ (from NMOS5VDEPL model [86]), while V_{ds} depends on R_{eq} as shown in Figure 5.8 on page 105. The self-startup capability is evaluated from the small-signal analysis combined with the static characterization by calculating the startup condition. The transformer equivalent parameters are calculated below:

$$
\begin{aligned}
L_{ms} &= k\,L_{22} = 176\,\mu\text{H},\\
n_{12} &= \sqrt{L_{22}/L_{11}} = 36.1,\\
R_{eq} &= R_{teg} + R_{w1} + R_{con1} = 2.58\,\Omega,\\
R'_{eq} &= R_{eq}\,n_{12}^2 = 3.35\,\text{k}\Omega,\\
R'_{w2} &= R_{w2} + R_{con2} = 5.73\,\Omega.
\end{aligned}
$$

Now we compute the capacitances:

$$
\begin{aligned}
C_{gs} &= C_{ox}\,W\,L/2 = 1.51\,\text{pF},\\
C_{eq} &= C_1 + C_{gs} \approx 152\,\text{pF},\\
C_k &= 1/C_{eq} = 6.58\cdot 10^9\,\text{F}^{-1}.
\end{aligned}
$$

and the nmos parameters:

$$
\begin{aligned}
\beta_n &= \mu_n\,C_{ox}\,W/L = 0.213\,\text{A V}^{-2},\\
g_{ds} &= \beta_n\,(V_{gs} - V_{tn} - V_{ds}) = 182\,\text{mS},\\
r_{ds} &= 1/g_{ds} = 5.50\,\Omega,\\
r'_{ds} &= r_{ds}\,n_{12}^2 = 7.15\,\text{k}\Omega,\\
g_m &= \beta_n\,V_{ds} = 6.0\,\text{mS}.
\end{aligned}
$$

where $V_{ds} = 28\,\text{mV}$ is estimated from Figure 5.8 depending on R_{eq}. The previously calculated values of g_m and g_{ds} are in good agreement with the values obtained by the static characterization shown in Figure 5.10 and 5.12. The startup requirements are calculated below (by comprising R_{cs}) as:

$$
\begin{aligned}
f_0 &= 0.82\,\text{MHz},\\
g_{m0} &= 22.6\,\text{mS},\\
V_{ds0} &= 106\,\text{mV},\\
V_{teg0} &= 154\,\text{mV}.
\end{aligned}
$$

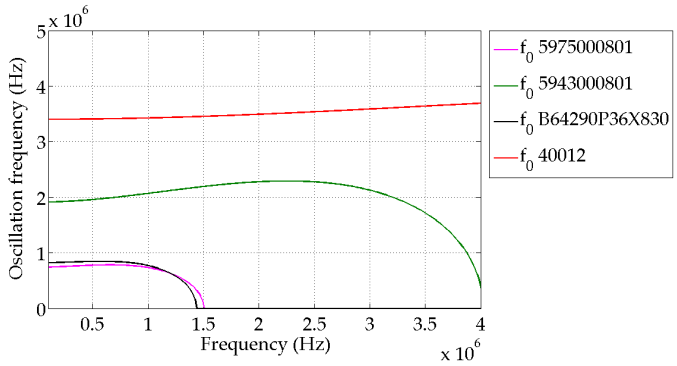


Figure 5.13: Oscillation frequency of the converter as a function of frequency for 5943000801, 5975000801, and BA64290P36X830 core with T_1 layout, and for the 40012 core.

The analytical results show that the minimum source voltage is $V_{teg0} = 154\,\text{mV}$. Since $g_m < g_{m0}$ and $V_{ds} < V_{ds0}$ the converter can not start to oscillate. This is mainly due to the high R_{cs} with 5975000801 ferrite at 1 MHz. However, g_m can be improved by adding one (or more) parallel nmos depletion but only for small values of R_{eq} due to the growth of g_{ds} which increases the g_{m0} from (5.17).

While (5.12) gives the static oscillation frequency of the converter, a more accurate expression for f_0 can be obtained by including the AC analytical model of the micro-transformer. This model comprises skin effects in the windings analyzed in section 3.6.2 on page 43 and the complex permeability presented in section 3.6.6 on page 49. Therefore, the self-inductances are modeled by (3.137), the winding resistances are modeled by (4.8), while the core ESR is modeled by (3.138). Figure 5.13 shows the oscillation frequency in (5.12) as a function of frequency for devices with 5943000801, 5975000801, and BA64290P36X830 core with T_1 layout fabricated on PCB substrate, and with the 40012 core fabricated on silicon substrate. Figure 5.13 allows to find the point at which the oscillation frequency f_0 equals the frequency of operation f_{op} of the devices. The results shows that this point is close to 2.3 MHz for 5943000801 core, 1.0 MHz for both 5975000801 and BA64290P36X830 cores, and 3.5 MHz for 40012 core. The modeling results for 5943000801 core ($\mu_{rc} = 800$) and T_1 layout ($1:38$) at $\approx 2.3\,\text{MHz}$ report $L_{11} = 0.025\,\mu\text{H}$, $L_{22} = 22\,\mu\text{H}$, $R_{w1} = 0.8\,\Omega$, $R_{w2} = 3.8\,\Omega$, $R_{cs} \approx 210\,\Omega$ and $k \approx 0.75$. The modeling results for BA64290P36X830 core ($\mu_{rc} = 4300$) and T_1 layout ($1:38$) at $\approx 1.0\,\text{MHz}$ report $L_{11} = 0.14\,\mu\text{H}$, $L_{22} = 190\,\mu\text{H}$, $R_{w1} = 0.8\,\Omega$, $R_{w2} = 3.8\,\Omega$, $R_{cs} \approx 530\,\Omega$ and $k \approx 0.85$. The modeling results for 40012 core ($\mu_{rc} = 500$ and $1:38$) at $\approx 3.5\,\text{MHz}$ report $L_{11} = 0.18\,\mu\text{H}$, $L_{22} = 20\,\mu\text{H}$, $R_{w1} = 1.2\,\Omega$, $R_{w2} = 14.8\,\Omega$, $R_{cs} \approx 50\,\Omega$ and $k \approx 0.62$. Table 5.1 on the facing page shows the startup conditions calculated at the optimum frequency $f_0 = f_{op}$ for the 5943000801, 5975000801, and BA64290P36X830 core with T_1 layout, and for the 40012 core.

The resonant oscillator of the second version of DC-DC converter is simulated with Cadence Design Systems with the V_0 node grounded (without load). The transformer is modeled with the measurements of the device with 5975000801 ferrite at 1 MHz. The trigger condition is obtained by adding noise sources at the beginning of each simulations. However, this does not affect the startup requirements which are imposed from (5.21). The simulations are performed with a transient (from 0

Table 5.1: Startup conditions evaluated at $f_0 = f_{op}$ for 5943000801, 5975000801, and BA64290P36X830 core with T_1 layout, and for the 40012 core.

Device	5943000801	5975000801	B64290P36X830	40012
L_{ms} (µH)	16.5	176	162	12.4
n_{12}	29.7	36.1	36.8	10.5
R_{eq} (Ω)	2.58	2.58	2.58	2.98
R'_{eq} (kΩ)	2.27	3.35	3.50	0.33
R'_{w2} (Ω)	5.73	5.73	5.73	16.7
r_{ds} (Ω)	5.50	5.50	5.50	5.50
r'_{ds} (kΩ)	4.84	7.15	7.46	0.61
f_0 (MHz)	2.40	0.82	0.88	3.56
g_m (mS)	6.0	6.0	6.0	6.0
g_{m0} (mS)	54.5	22.6	23.6	29.7
V_{ds0} (mV)	256	106	111	139
V_{teg0} (mV)	362	154	161	211

to 1 ms) and transient noise (from 0 to 1 ms) analyses with: noise bandwidth between 1 to 4 MHz, all mosfet noise sources (Flicker and Thermal), setup corners with typical global variations (TYP), very high accuracy tuning (VHIGH), and minimum conductance equal to $G_{min} = 10^{-21}$ S. Firstly, the transformer is simulated without core loss ($R_{cs} = 0\,\Omega$). In this case the analytical results show that the converter can start to oscillate from $g_{m0} = 5.3$ mS and $V_{teg0} = 37.0$ mV with an oscillation frequency equal to $f_0 = 0.97$ MHz. Hence, the transient analysis considers a source with $V_{teg} = 50$ mV resulted to be the minimum DC voltage, $R_{teg} = 430\,\text{m}\Omega$, and the device with $L_{11} = 0.15\,\mu\text{H}$, $L_{22} = 195\,\mu\text{H}$, $R_{w1} = 0.8\,\Omega$, $R_{w2} = 3.8\,\Omega$, $R_{cs} \approx 0\,\Omega$, $k \approx 0.9$, $R_{con1} = 1.35\,\Omega$ and $R_{con2} = 1.93\,\Omega$. Figure 5.14 on the next page shows the time responses from 0 to 0.1 ms of voltages and currents at both primary and secondary winding swithout core loss. Figure 5.14 shows that the converter starts to oscillate exponentially, while the simulated f_0 is 0.92 MHz.

Later, the transformer is simulated with core loss ($R_{cs} \approx 600\,\Omega$) with an equivalent parallel core loss resistor estimated from (3.140) to be $R_{ps} = R_{cs}[1+(2\,\pi\,f\,L_{ms}/R_{cs})^2] = 2.64\,\text{k}\Omega$ as discussed in section 3.6.6 on page 49. Figure 5.15 on the next page shows the small-signal circuit diagram of the resonant oscillator block of the first version of DC-DC converter with parallel core loss. The analytical results show that the converter can start to oscillate from $g_{m0} = 22.6$ mS and $V_{teg0} = 154$ mV with an oscillation frequency equal to $f_0 = 0.82$ MHz. Hence, the transient analysis considers a source with $V_{teg} = 220$ mV resulted to be the minimum DC voltage, $R_{teg} = 430\,\text{m}\Omega$, and the device with $L_{11} = 0.15\,\mu\text{H}$, $L_{22} = 195\,\mu\text{H}$, $R_{w1} = 0.8\,\Omega$, $R_{w2} = 3.8\,\Omega$, $R_{cs} \approx 600\,\Omega$, $k \approx 0.9$, $R_{con1} = 1.35\,\Omega$ and $R_{con2} = 1.93\,\Omega$. Figure 5.16 on page 113 shows the time responses from 0 to 0.1 ms of voltages and currents at both primary and secondary windings with core loss. Figure 5.16 shows that the converter starts to oscillate exponentially, while the simulated f_0 is 0.88 MHz.

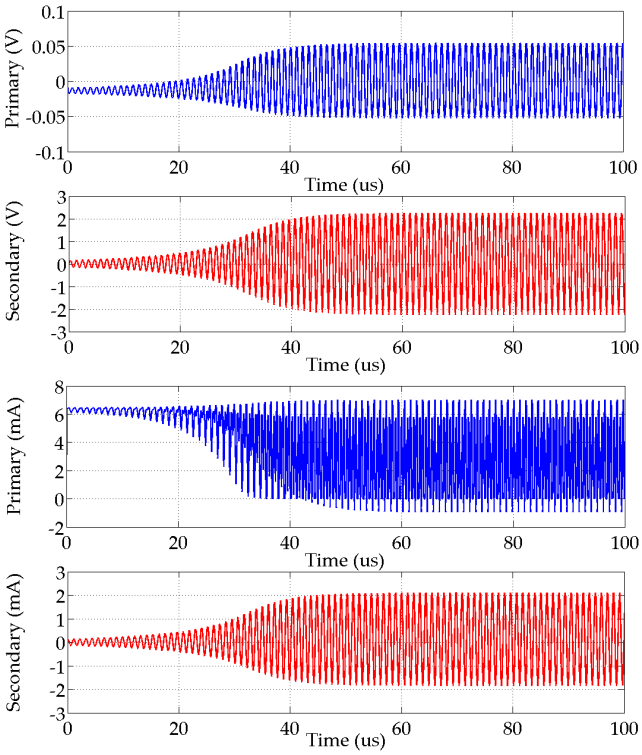


Figure 5.14: Simulation results without load: voltages (top figure) and currents (bottom figure) at the primary and secondary windings with 5975000801 ferrite without core loss and T_1 layout.

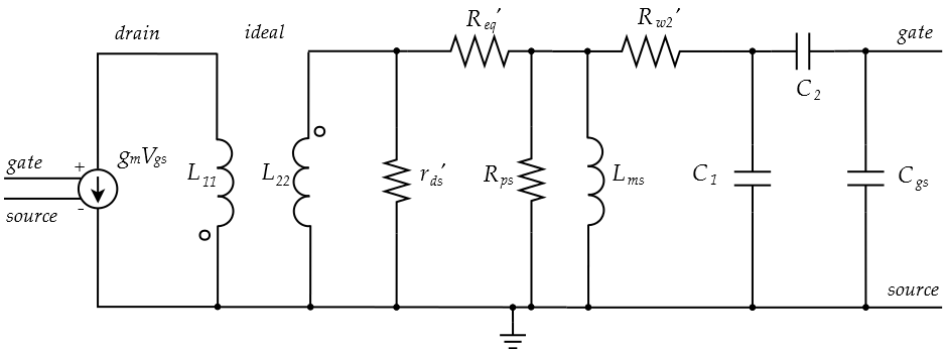


Figure 5.15: Small-signal circuit diagram of the resonant oscillator of the first version of DC-DC converter with parallel core loss.

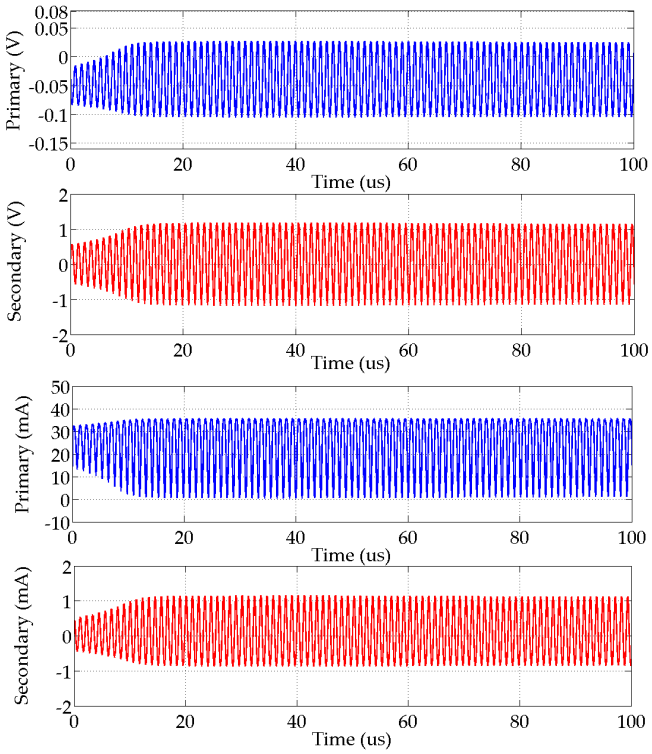


Figure 5.16: Simulation results without load: voltages (top figure) and currents (bottom figure) at the primary and secondary windings with 5975000801 ferrite with core loss and T_1 layout.

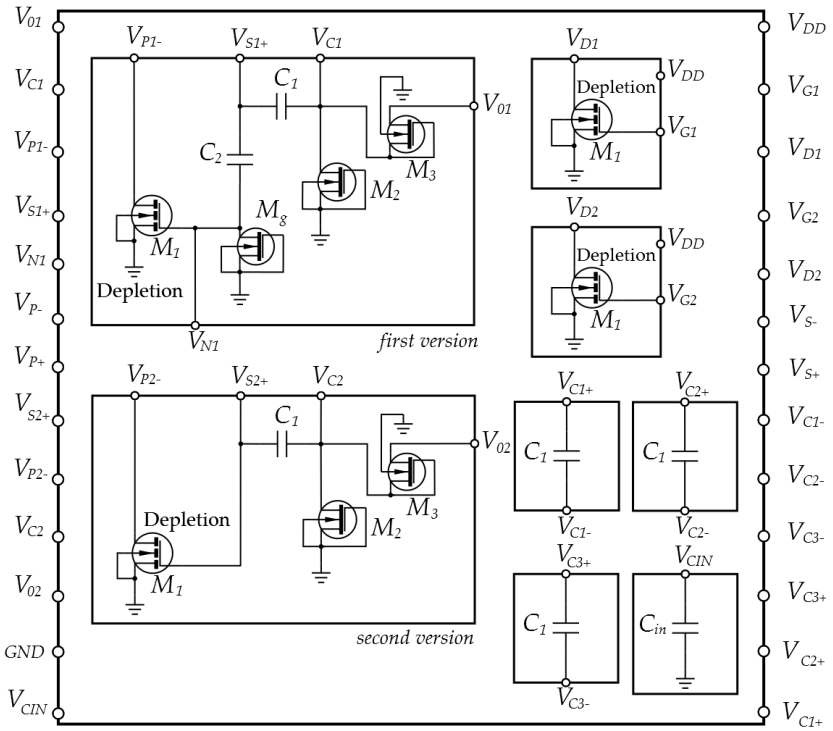


Figure 5.17: Schematic of the low-voltage IC DC-DC resonant converter.

5.3.5 Experimental results

The converter is fabricated in 0.32 µm BCD6s technology at STMicroelectronics. The overall schematic is presented in Figure 5.17. The left picture of Figure 4.32 on page 88 shows a microphotograph of the IC prototype. The top metalization is compatible with the mounting of magnetics on-top of the silicon die. However, the following results are obtained with devices fabricated on PCB substrate due to the higher inductance and turns ratio.

Measurements are realized on the second version of DC-DC converter (Figure 5.5 on page 101) with single M_1 and single C_1 combined with the transformer with 5975000801 core and T_1 layout. Measures with no C_{in} and no load report that the circuit starts to oscillate from $V_{teg0} = 0.28\,\text{V}$. This is in good agreement with small-signal and simulation results described in the previous section. However, the measured V_{teg0} is higher than the simulated value of 0.22 V due to a mismatch in the fabrication of the nmos depletion. In fact, M_1 results to have a higher threshold estimated to $V_{tn} \approx -0.80\,\text{V}$ that decreases the g_m at $V_{gs} = 0\,\text{V}$. Figure 5.18 on the facing page shows the experimental waveform without load at $V_{teg} = 0.36\,\text{V}$ with a measured f_0 equal to 0.6 MHz. Measures with $C_{out} = 22\,\text{nF}$ report that the prototype is capable to convert an input voltage down to $V_{teg} = 0.33\,\text{V}$ to a rectified output of $V_{rect} = 0.80\,\text{V}$ (at $V_{teg} = 0.40\,\text{V}$) greater than the typical threshold voltage of a mosfet. In addition, for an input of 0.59 V the circuit provides an output of 2.0 V. Figure 5.19 on the next page shows the experimental waveforms with load at $V_{teg} = 0.50\,\text{V}$ with a measured f_0 equal to 1.03 MHz and an output of $V_{rect} = 1.3\,\text{V}$. Finally, Figure 5.20 on the facing page shows the experimental startup waveforms with load at $V_{teg} = 0.37\,\text{V}$.

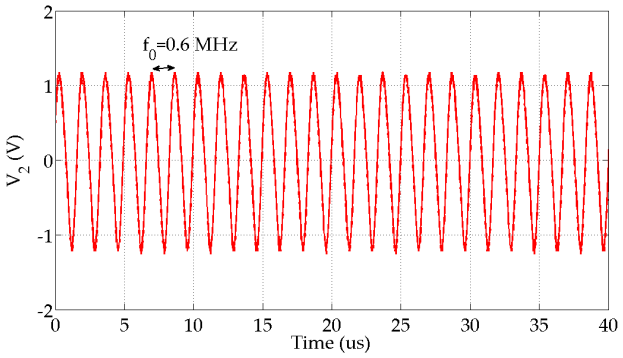


Figure 5.18: Experimental waveform without load at $V_{teg} = 0.36\,\mathrm{V}$: secondary winding voltage with 5975000801 ferrite and T_1 layout.

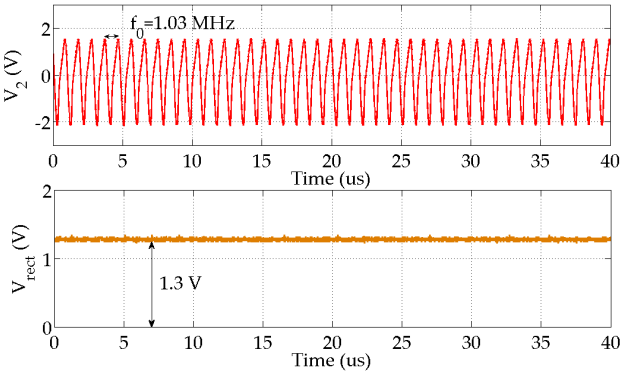


Figure 5.19: Experimental waveforms with load at $V_{teg} = 0.50\,\mathrm{V}$: secondary winding and rectified output voltages with 5975000801 ferrite and T_1 layout.

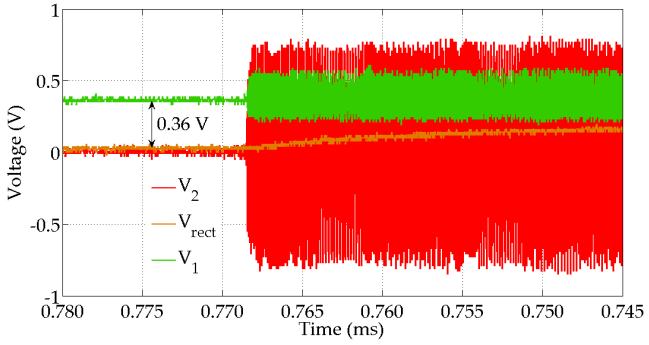


Figure 5.20: Experimental startup waveforms with load at $V_{teg} = 0.37\,\mathrm{V}$: secondary winding, rectified output, and input voltages with 5975000801 ferrite and T_1 layout.

Conclusions and future works

This thesis has investigated a new approach for realizing bond wire magnetics for power converter applications, thus enabling the development of new platforms denoted as PwrSiP and PwrSoC for package and wafer level integrations. Several prototypes of bond wire transformers with gold IC bonding wires have been modeled and designed in order to get high inductance and turns ratio in a small footprint area in a frequency range between 10 kHz and 5 MHz. The devices have been fabricated on both PCB and silicon substrates with toroidal and race-track shaped toroidal cores, and various layouts depending on minimum spacing, minimum bond pad pitch and metalization width.

Several high-permeability toroidal magnetic cores have been characterized and micro-machined with the intent to maximize the secondary self-inductance and number of turns based on a manufacturable and repeatable wire bonding technology on PCB substrate. Measurement results show that the use of ferrite cores with respect to air cores increases the secondary self-inductance up to 315 µH with low DC series resistance, and improves the coupling coefficient to ≈ 0.9 with an effective turns ratio of ≈ 35, which represent the actual state-of-the-art for highly efficient bond wire magnetics. In addition, the maximum Q-factor measured at the secondary side is 24.5 at 100 kHz.

An LTCC race-track magnetic core has been characterized and fabricated with the target of maximizing the secondary self-inductance and number of turns based on a repeatable wire bonding process on top of a 0.32 µm BCD6s silicon substrate fabricated at STMicroelectronics. Measurement results report that the use of the LTCC core with respect to the air core improves the secondary self-inductance up to 23 µH with low DC series resistance, and enhances the coupling coefficient to ≈ 0.6 with an effective turns ratio of ≈ 7.0. Finally, the maximum Q-factor measured at secondary side is 10.5 at 1.4 MHz.

A resonant DC-DC converter is designed and fabricated in 0.32 µm BCD6s silicon technology at STMicroelectronics with a depletion nmosfet and bond wire micro-transformer for EH applications. Experimental measures report that the circuit starts to oscillate from a TEG voltage down to 280 mV while begins to convert from an input voltage down to 330 mV to a rectified output voltage of 800 mV (at an input of 400 mV) higher than the conventional threshold voltage of a mosfet.

The approach proposed in this thesis for developing bond wire magnetics is cost-effective and enables a flexible design of inductors and transformers with adjustable performance by varying wire loop height and core thickness, and very small EMI due to the toroidal geometry. This makes possible the evolution of PwrSiP and PwrSoC with reliable highly efficient magnetics with high inductances and turns ratios compatible with IC designs.

At this moment, many works are in progress. Several LTCC and laminated

anisotropic Vitrovac race-track cores are being assembled by Foundation Bruno Kessler (FBK), Trento (IT) with gold IC bonding wires on PCB substrate in a footprint area of $7.0\,\text{mm} \cdot 4.1\,\text{mm}$, and on silicon substrate in a footprint area of $3.93\,\text{mm} \cdot 3.81\,\text{mm}$ with a smaller package to reduce the parasitic inductance. This new designs will allow the development of high turns and high inductance micro-magnetics. In addition, a new solution of resonant DC-DC converter is being fabricated in $0.32\,\mu\text{m}$ BCD6s technology at STMicroelectronics able to startup from ultra low-voltage down to $50\,\text{mV}$ with a bond wire transformer mounted on-top of the die.

Future works include further miniaturization such as the evolution of flip-chip bonded magnetics with reduced core thickness for tiny IC packages $< 0.2\,\text{mm}$ and standard FC bonders. Flip-chip magnetics can guarantee a better coupling compared to bond wire magnetics because the more compact structure. This enables the realization of high power density components with low cost production processes. Furthermore they allow to decrease the series resistance with electroplated metalizations and small solder bumps thus improving the overall Q-factor.

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Acronyms

BPP Bond Pad Pitch

CMOS Complementary Metal-Oxide Semiconductor

CNR National Research Council of Italy

EH Energy Harvester

EMF ElectroMotive Force

EMI ElectroMagnetic Interference

EOS Extended Open and Short circuit

ESR Equivalent Series Resistance

FBK Foundation Bruno Kessler

FC Flip-Chip

FR4 Flame Retardant 4

HAZ Heat-Affected Zone

IC Integrated Circuit

I/O Input/Output

ISTEC Institute of Science and Technology for Ceramics

K&S Kulicke & Soffa

LTCC Low Temperature Co-fired Ceramic

MCM Multi Chip Modules

MEG Microbial Electric Generator

MEMS Micro Electro-Mechanical System

MMF MagnetoMotive Force

MPL Magnetic Path Length

MPPT Maximum Power Point Tracking

NCLA National Centre for Laser Applications

PCB Printed Circuit Board

PwrSiP Power Supply in Package

PwrSoC Power Supply on Chip

RF Radio Frequency

SOS Standard Open and Short circuit

SoC System on Chip

TAB Tape Automated Bonding

TEG Thermo Electric Generator

T/C Thermocompression

T/S Thermosonic

U/S Ultrasonic

WSN Wireless Sensor Nodes

ZCS Zero-Current Switching

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