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MODELLING AND DESIGN OF ADVANCED RELIABLE CIRCUITS AND DEVICES FOR ENERGY EFFICIENCY

Tesi di Dottorato

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Abstract

Reliable electronic systems, namely a set of reliable electronic devices connected to each other and working correctly together for the same functionality, represent an essential ingredient for the large-scale commercial implementation of any technological advancement. Microelectronics technologies and new powerful integrated circuits provide noticeable improvements in performance and cost-effectiveness, and allow introducing electronic systems in increasingly diversified contexts. On the other hand, opening of new fields of application leads to new, unexplored reliability issues.

The development of semiconductor device models, and at the meantime the creation of electrical models (such as the well known SPICE models) able to describe the electrical behaviour of devices and circuits, is a useful means to simulate and analyse the functionality of new electronic architectures and new technologies. Moreover, it represents an effective way to point out the reliability issues due to the employment of advanced electronic systems in new application contexts. A fault analysis and modeling have always been important activities needed to improve quality and performance of electronic devices and circuits. In this thesis modeling and design of both advanced reliable circuits for general-purpose applications and devices for energy efficiency are considered.

More in details, analyzing different contexts, the following activities have been carried out: first, reliability issues in terms of security of standard communication protocols in wireless sensor networks are discussed. A new communication protocol is introduced, allows increasing the network security.

Second, a novel scheme for the on-die measurement of either clock jitter or process parameter variations is proposed. The developed scheme can be successfully used for an accurate evaluation of both jitter and process parameter variations at negligible area and power costs.

Then, reliability issues in the field of “energy scavenging systems” have been analyzed. Particularly, an accurate analysis and modeling of the effects of faults affecting circuit for energy harvesting from mechanical vibrations is performed. The results of the performed analyses have than driven the development of a solution able to make the circuit fault tolerance with respect to internal faults.

Finally, the problem of modeling the electrical and thermal behavior of photovoltaic (PV) cells under hot-spot condition is addressed. Two models have been developed during this activity: a distributed electrical network able to model the electrical behavior of a PV cell, and a thermal model based on the thermal properties of the materials used to manufacture the cells. The first model is useful to evaluate the electrical performance of the PV cell and to extract the power dissipated when it is under hot-spot. The second model allows estimating the temperature of the hot-spot area as a function of the time interval during which the PV cell is under hot-spot, taking as input the value of the power dissipation provided by the distributed electrical model.

Chapter 1

Introduction

In this short chapter, a brief overview about the main topics that will be analyzed in this thesis and shown in the next chapters is given. The emphasis is placed on the importance of modelling and design for reliability applied to advanced electronic systems and devices. Several applicative contexts are briefly descripted and, considering electronic circuits and devices used in these contexts, problems in terms of reliability are exposed. The exploration of faults, defects, and "failure conditions" of integrated circuits and devices for energy efficiency, through a circuital analysis, the development of models, and electrical simulations, has been the main motivation for this thesis.

1.1 Reliability and modelling for electronic systems

The emerging new technologies provide ever more challenges to assure the reliability of electronic devices. The increasing of even more high performance integrated circuits, with a lower cost, in a less space (weight), and at the meantime with a higher electronic circuits density in a single chip, it's leading to the possibility to use microelectronic technologies everywhere. This makes the reliability an even more important issue.

The reliability of electronic assemblies requires a definitive design effort that has to be carried out concurrently with the other design functions during the development phase of the product. While of course, consistent high quality manufacturing and all that its implies in term of design for assembly and design for testability is a necessary prerequisite to assure the reliability of the device, only a design for reliability (DfR) can assure that the design manufactured will be reliable in its intended application. It is well known that reliability is a requirement needed for any kind of electronic application. For example it is important for devices in the aerospace field, or at same time for biomedical applications. Not least it is important for "energy green" applications or general-purpose integrated circuits, where a very low fault rate is required and process variations due to the fabrication that can affect the device, must be analyzed and activated during the testing phase.

First, this requires an accurate analysis and modelling of each fault effect that can affect the components of the circuit considered, with particular emphasis to the faults impact on the device performance; then, a design of ad-hoc solutions through a preliminary development of models, in order to make the device high reliable.

There are many intrinsic factors that are increasing the necessity to give more attention to the DfR. As already mentioned, if increasing miniaturization and integration of microelectronic technologies with high design complexity, has provided substantial improvements in performance and cost-effectiveness for many applications, this means also that the presence of reliability concerns as those that can originate from the parameter variations occurring during fabrication, it is increasingly difficult to guarantee the availability of clock signals with sharp edges, limited skew and jitter [1-1]. As well known, the jitter on the clock signal is an undesired deviation with respect to the nominal behavior of the clock signal itself. An example of clock jitter is shown in Fig. 1.1. This undesirable effect may be caused by electromagnetic interference (EMI), noise on the bias voltage used to supply the integrated circuit, and

phenomena of crosstalk with carriers of other signals inside the microprocessor.

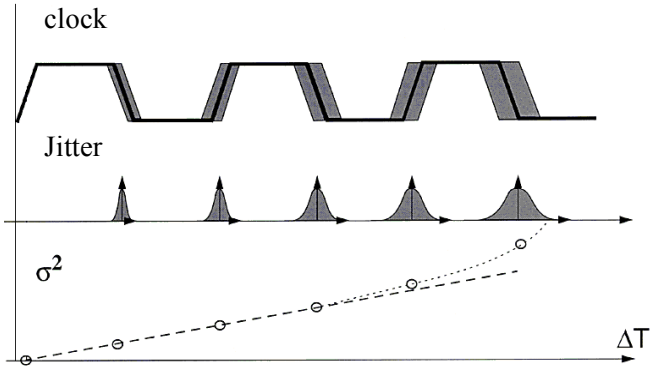

Figure 1.1: Temporal behavior of the clock signal affected by jitter.

In the latest digital electronic chips, this effect is one of the must important factors that must be kept in mind during the design, due to the negative impact on the electronic performance that it can introduce with its presence.

Reliability issues are also of interest for other applications, as for example the field of "energy scavenging systems". The last decade has shown an increased research interest in the development of electronic devices able to extract energy from the environment to supply electrical systems, and at the meantime the design of electronic systems able to generate electrical energy from different energy sources. The mechanical vibrations and sun power are two promising source of energy because of their widespread existence [1-2]. So far, not enough has been done in term of modeling and reliability design for this kind of systems. Energy-harvesting circuits (EHCs) are generally composed of many components that may fail during in-field operation because of material degradation or other effects [1-3]. An accurate modelling of faults in every component of the circuit, like diodes, transistors and capacitors, to make possible the analysis of their effects by simulations, it is an important step needed during the design, in order to make these circuits high reliable.

As well as for the EHCs, photovoltaic silicon solar cells are very sensitive to material impurities that can be present in their structure. Due to their large area,

the presence of these impurities is an intrinsic problem that cannot be eliminated during the fabrication process, but must be analyzed and mainly, its effect on the solar cell behavior could be modeled. Numerical TCAD simulators are useful to account for the impact of doping profiles, metal architectures or passivation schemes in silicon solar cells [1-4]. But due to the fact that this kind of simulators basically analyse an element of symmetry (a small repetitive portion of the solar cell) in order to reduce the computational effort, unfortunately, it is not possible to account for non-homogeneities in PV solar cell. On the other hand, circuit simulations of distributed electrical network (as the distributed electrical model presented in the chapter 6 of this thesis) allow analysing a larger area with a reduced computational time. As will be shown in the chapters 5 and 6 of this thesis, in some case, a shaded solar cell can be affected by an hot-spot condition due to the presence of impurity in its structure, that can really introduce permanent faults in the cell with drastically consequences on the whole photovoltaic system performance. A perfect way to simulate this phenomenon is the development of distributed models that can account for the whole solar cell. It is shown through simulation results confirmed by experimental date, that in situation like the above described, high voltage across the shaded cell results both high power dissipation and elevate temperature. Depending on the light current generated, the temperature above ambient of the shaded cell can be as high as 200 C°, implying potential safety issues.

Finally, reliability issues are also of interest in wireless applications. In these kinds of systems, due to the absence of a physical medium (wire) of the communication channel, the information can be exposed to various types of attacks that may try to violate the reliability of the network [1-5]. This is another issue that has been subject of this thesis. Defining a standard communication protocol useful to make sensor nodes in a correct and secure way to communicate each other, can be really tough in a wireless sensor network, because of all the possible situations have to be considered, simulated and classified including external attacks. Moreover, the analysis can became

very hard in cases of requirement of very low power consume to supply the sensor nodes. Due to the fact that the message traveling into the network is represented with a low number of bits, this makes more difficult the possibility to guaranty property of confidentiality, integrity or availability of the message.

Following the introduction above written, the body of this thesis is composed of the following chapters:

- *Chapter 2 Secure communication protocol for wireless sensor network:* The problem about the reliability of standard communication protocols in wireless sensor networks to guaranty a secure communication is discussed. The exposition of a new communication protocol allows to increase the security compared with standard communication protocols is the main part of this chapter.
- *Chapter 3 Measurement scheme for process parameter variation and clock jitter:* A novel scheme for the on-die measurement of either clock jitter or process parameter variations is proposed and analyzed. This type of scheme is needed during the test and debug phase of microprocessors, in order to validate the design and manufacturing process. It's part of the design for reliability concept needed to evaluate the possible need for design or process improvements.
- *Chapter 4 Faults affecting energy-harvesting circuits of self-powered wireless sensor:* An accurate analysis and modelling of fault effects affecting an integrated circuit performing energy harvesting from mechanical vibrations is exposed. Moreover, a possible solution to make the circuit fault tolerance from internal faults is also presented.
- *Chapter 5 Model for thermal behavior of shaded solar cell under hot spot condition:* In this chapter, the problem of modeling the thermal behavior of photovoltaic (PV) cells under hot-spot condition is addressed. Due to the combination of their being exposed to shading and localized crystal defects inside themself, PV cells may experience a dramatic temperature increase with consequent reduction of the provided power. A thermal model is also presented which allows

estimating the temperature of the hot-spot area as a function of the time interval during which the PV cell is under hot-spot condition.

- *Chapter 6 A distributed electrical network to model silicon solar cell:* From the activity done and exposed in the previous chapter, the idea to develop a distributed electrical network able to model in detail the behavior of silicon solar cells was born. The model developed is based on a network of repetitive elementary electrical units allows accounting for transport through the emitter, the fingers and the busbars. Moreover, electrical simulations done with the model considering cases of non-uniformities in the solar cell and partial shaded conditions will be discussed.
- Finally, in the last chapter conclusions are given with some suggestions for further work.

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Chapter 2

Secure communication protocol for wireless sensor networks

In the recent past, wireless sensor networks (WSN) have found their way into a wide variety of applications and systems with vastly varying requirements and characteristics. As a consequence, it is becoming increasingly difficult to discuss typical requirements regarding hardware issues and software support. Moreover, as already mentioned in the first chapter, associated to the design problems on which hardware an software are needed in order to implement an efficient system, an important issue for WSN, is their security, in terms of confidentiality, integrity, authenticity, availability [2-1]. In fact, differently from a wired network where the information transmitted among nodes is confined within a physical medium (a wire), in a wireless network the information is exchanged among nodes through electromagnetic waves that are broadcasted to the atmosphere. This makes them prone to various kinds of attacks that may try to violate the security of the network like for instance, the *Denial of Service* (*DoS*), the *Man-in-the-middle* (MITM), and the c*opy and repeat* (denoted also as *replay*) attacks [2-2, 2-3]. As consequence

especially in case of WSN employed within control systems for safety critical applications (e.g., chemical or nuclear industrial plants, aerospace vehicle platforms, etc.), it is of utmost importance to implement countermeasures to guarantee their security [2-3].

In order to provide a WSN with an adequate security level, it is essential that nodes exchanging information must be able to provide assurance on their identity, and that the exchanged information is authentic and integral [2-3].
The IEEE 802.15.4 standard and the ZigBee Alliance protocol provide the communication with some level of authenticity and integrity. In particular, they are able to prevent/limit the above-mentioned attacks on the messages transmitted from the transmitter (master) node (Tx) to receiver (slave) nodes (Rx) [2-4]. Reversely, they do not provide any protection to the acknowledgment (ACK) message [2-4], which is sent back by the Rx in order to confirm to the Tx that the message has been successfully received. The lack of protection for the ACK is a serious bug [2-1], possibly harming the security of the whole network. Moreover, in the IEEE 802.15.4 and the ZigBee protocols, the message freshness against possible *replay* attacks is guaranteed by a frame counter only.

Based on these considerations, in this short chapter is proposed a new, secure communication protocol for WPANs, that is able to guarantee message integrity, authenticity and freshness for both, sent messages and acknowledgment messages. Furthermore, the developed protocol prevents the *copy and repeats* attack by a different, and more secure approach, compared to the IEEE 802.15.4 and ZigBee protocols.

The rest of this chapter is organized as follows. In Section 1.2, some important security problems of standard WPAN protocols are discussed. In Section 1.3, the proposed protocol is illustrated. In Section 1.4 a possible hardware implementation of the proposed protocol is also given.

2.1 Security problems of standard protocols

As introduced, in standard IEEE 802.15.4 and ZigBee Alliance protocols, when the Rx receives the message (MSG), it verifies its validity (integrity, authenticity and freshness). If the message is valid, then the Rx sends an unprotected ACK to the Tx, which considers the communication successfully concluded upon its receipt, with no check upon the ACK authenticity (i.e., its coming from the expected Rx node) and freshness (i.e., its being a new ACK, and not an old ACK copied and repeated by a non authorized node). The lack of authentication and freshness verification on the ACK could seriously threaten the security of the whole network. For instance, let's consider the simple case of an attacker trying to avoid that a message arrives to the Rx, thus starting a MITM attack. It can first simply send an interference noise to the Rx at the same time as the Tx, thus preventing the Rx from properly receiving the MSG sent by Tx. Afterwards, the attacker can send a fake ACK to the Tx. This way, since the ACK is not protected, the Tx can be fooled that Rx successfully received the MSG. Another limit of standard protocols is that they verify the MSG freshness by checking a sequence number provided by a simple counter. They are consequently prone to DoS-like attacks [2-5]. In fact, as shown in [2-5], such an attack can be carried out by assembling a fake message that is compliant with the protocol format and by setting its sequence number equal to the maximum counting value. This way, the counter of the node receiving such a fake message will overflow. This will make the counters of the Tx and Rx no longer synchronous, so that the Rx will discard all following messages from Tx.

2.2 Proposed secure protocol

Here is proposed what has been developed to overcome the security

problems that have described in the previous section. As significant example, is considered the case of a master/slave network with one master node, acting also as network manager, and several slave nodes. However, the proposed protocol can be applied to any kind of WPAN by means of straightforward modifications. Similarly to the standard IEEE 802.15.4 and ZigBee protocols, this protocol guarantees authentication and integrity of the MSG by means of a Message Authentication Code (MAC) [2-4], that is generated by encrypting the message in clear text by an Advanced Encryption Standard (AES) algorithm [2-4]. Moreover, differently from the standard IEEE 802.15.4 and ZigBee protocols, the proposed protocol: i) guarantees the authenticity and freshness of the ACK, thus avoiding MITM attacks; ii) provides a new mechanism to guarantee the freshness of the MSG, that is able to protect the WPAN with respect to DoS-like attacks.

To guarantee the authenticity of the ACK, it is proposed to generate a MAC for the ACK, by encrypting the ACK in clear text by an AES algorithm [2-6]. To guarantee the freshness of the ACK and the MSG, as will be described later in this section, the proposed protocol embeds a rolling code sequence [2-7] (#seq) on both the ACK and MSG, and provides an original mechanism to synchronize the Tx and Rx. This makes the WPAN immune to DoS-like attacks. The general structure of the derived MSG or ACK is schematically shown in Fig. 2.1.

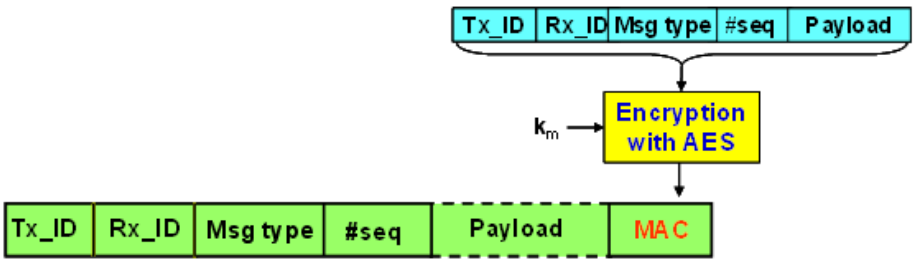

Figure 2.1: Structure of a MAC or ACK of the proposed protocol.

The fields Tx_ID and Rx_ID contain the identification codes (IDs) of the

transmitter Tx and receiver Rx, respectively. The Payload is the useful part of the message, containing data, commands or ACKs. The field Msg_type indicates the type of message (e.g., command, data, ACK, synchronization, etc.) included in the payload field. The field #seq contains the current sequence number of the rolling code of the node (Tx/Rx) sending the message. Finally, the MAC of the MSG or ACK is generated by encrypting the first part of the message (i.e., Tx_ID, Rx_ID, Msg_type, #seq and Payload) with the AES algorithm and a secret key k_m. As can be seen from Fig.2.1, the useful message (i.e., the whole message, but for the MAC) is sent in clear text. This allows to identify the Rx of the message and to verify the correctness of #seq without any decryption, thus reducing power consumption and the impact on communication latency. Of course, this approach can not be used if the message carries critical data, while it does not give rise to any security flow if the message consists of a simple command, as it is usually the case in WSNs.

Let's describe in details how the developed protocol guarantees the freshness of both the AKC and MSG. As for the adopted rolling code sequence, it can be a pseudo-random sequence, for instance generated by a *Linear Feedback Shift Register* [2-7]. The freshness of the ACK and MSG is verified when the rolling code sequences (#seq) in the master (Tx) and in the slave (Rx) nodes are synchronized. This is achieved in the following way.

Let's suppose, as an example, that the WSN is composed by one Tx node (N1), and three Rx nodes (N2, N3 and N4), as schematically represented in Fig. 2.2.

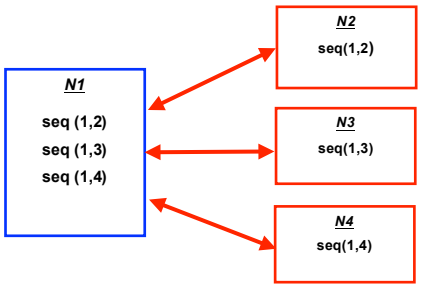

Figure 2.2: Sequences of the rolling code memorized on a master node (N1) and slave nodes (N2, N3, N4).

Tx must generate/memorize a different *#seq* for any Rx node. Thus, in a network of *n* nodes, Tx must generate *n-1* different sequences (*seq(1,i)*, *i=2..n*), while each Rx must generate only one *#seq* (the respective *seq(1,i)* sequence), as represented in Fig. 2.2. In the proposed protocol, the synchronism between the *#seq* of Tx and Rx is guaranteed by the ACK. When a Rx (Ni, with i=2, 3, 4) receives a message (MSG) from Tx, it verifies the authenticity and freshness of the received MSG and, in case these verifications are successful, it accepts the MSG, updates its *seq(1,i)* and sends back an ACK to Tx (N1). When Tx receives the ACK, it also updates its *seq(1,i)* that is specific to the Rx with which it was communicating. Therefore, upon conclusion of a successful communication, Tx and Rx are synchronized. If Rx (Tx) receives a MSG (ACK) with a *#seq* different from the expected one (e.g., due to an attack), Rx (Tx) discards the MSG (ACK) without updating its *#seq*. This way, the synchronization of the *#seq* of Tx and Rx is still guaranteed, and the Rx is ready to accept a possible new (valid) message from Tx. Additionally, the protocol provides a retransmission procedure that avoids the loss of synchronism also when Tx does not receive any ACK from Rx (e.g., if due to excessive noise in the channel, the MSG sent by Tx does not reach Rx, or the ACK sent by Rx does not reach Tx). After sending a MSG, Tx triggers a timer and waits for the arrival of the ACK for a proper time interval t_w. If after t_w Tx has not yet received the ACK, it sends again the MSG to Rx and triggers again the timer. The t_w is chosen large enough to allow the MSG to reach Rx and be processed by it, to permit Rx to elaborate the ACK, and the ACK to reach node Tx. Tx repeats this retransmission procedure till it receives the ACK from Rx, or till the maximum number of retransmissions (n_{max}) allowed by the proposed protocol is reached. If after n_{max} retransmissions Tx has not received any ACK, it labels Rx as “problematic” node. Retransmissions are managed by node Rx as follows. When Rx receives a MSG with a *#seq* equal to its previous *#seq*, then it compares the whole MGS with the last MSG received from Tx. If they match, then Rx recognizes it as a retransmitted message and sends again the ACK to Tx without increasing its *#seq*.

Finally, as for the Rx nodes that have been labeled as “problematic”, the protocol provides the following resynchronization procedure between Tx and Rx. Initially, the master Tx starts sending to Rx a synchronization MSG (which is built as shown in Fig. 2.1, but without any payload) with its current $\#seq_{TX}$. When Rx receives this kind of MSG, it makes its own sequence $\#seq_{RX}$ equal to $\#seq_{TX}$. Then, Rx sends and ACK to Tx with $\#seq_{RX}$ and increases its sequence by 1 (i.e., $\#seq_{RX}+1$). When Tx receives the ACK, it also increases its sequence by 1 (i.e., $\#seq_{TX}+1$) and sends an ACK with the updated sequence to Rx. Finally, when Rx receives the ACK, it verifies that $\#seq_{TX}+1 = \#seq_{RX}+1$. If they are the same, then Rx assumes that Tx is an authorized node of the network, thus accepting the new sequence. Otherwise, Rx keeps its old sequence number.

2.3 Implementation and validation

In order to verify the effectiveness of the illustrated protocol the Tx and Rx blocks have been designed implementing the protocol in Verilog. The nodes have been synthesized with Altera Quartus II [2-8].

As an example, here is exposed the case of a single master (Tx) node and three slave (Rx) nodes (Fig. 2.2). Moreover, it has been considered a field of 2 bits for the Tx ID, for the Rx ID and for the message type, while a field of 6 bits for the Payload. Additionally, and without loosing generality, it has been considered a rolling code implemented by a 3 bits counter. Finally, it has been used a 128 bits AES module (i.e., input message and secret key of 128 bits) to generate the message MAC. Thus, before the encryption of the message (to generate its MAC), the message is expanded to 128 bits by adding 0s. The implementation of the Tx node is schematically shown in Fig. 2.3. As for the Rx node, its structure is very similar and is not shown. Tx is divided in two functional blocks: i) Tx-part, which elaborates the MSGs to be sent to the Rx; ii) Rx-part, which controls the ACK messages received from Rx. As for the

Tx-part, it receives as input: i) the ID of the Rx (ID_Rx), ii) the message type (MsgT), iii) the Payload, iv) the current rolling code sequence number (My_RC) of the Tx generated by the 3 bit counter *RC_Gen*, v) the IDs of problematic Rx nodes (ID_PN), which are loaded during the initialization phase into a proper table within the block *Rx_Status*.

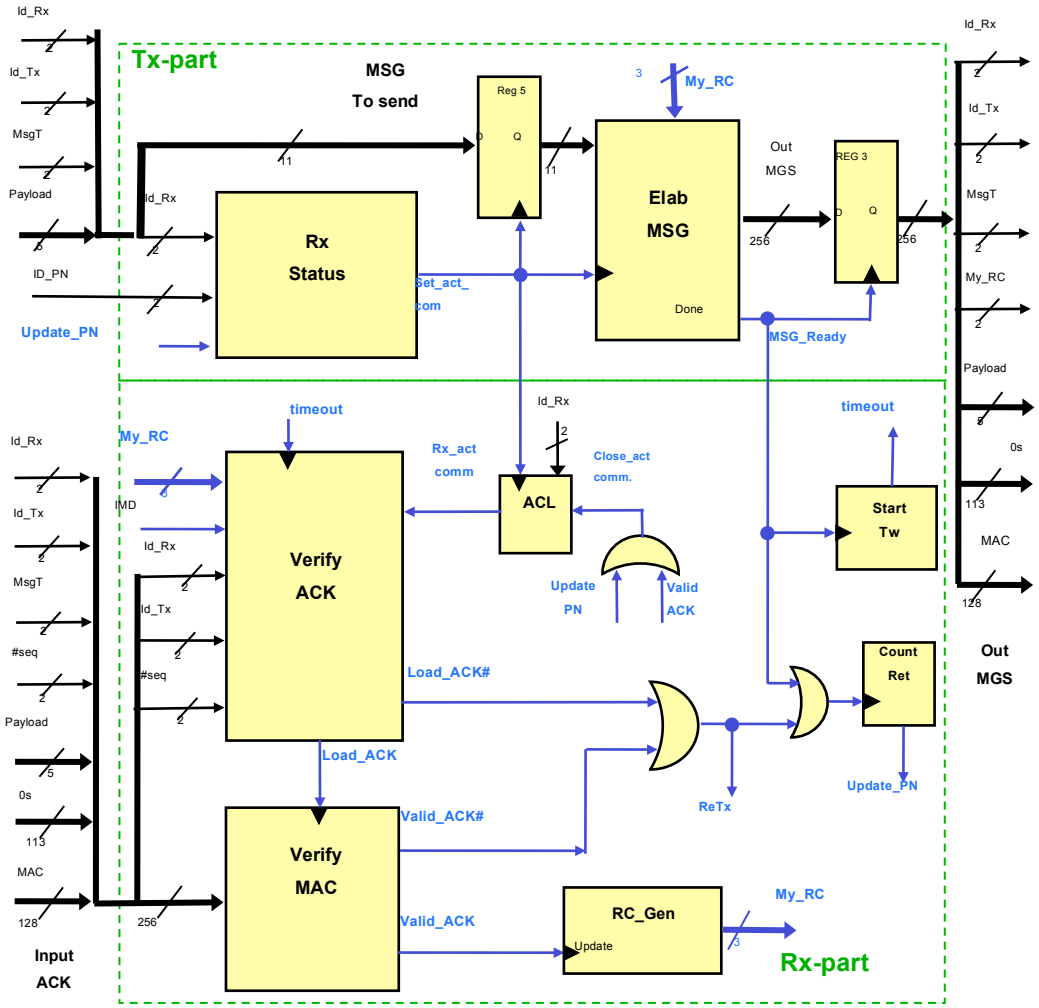

Figure 2.3: Block structure of a Tx node.

Before starting a communication with a Rx, *Rx_Status* verifies that Rx is not a problematic node. If Rx is not problematic, *Rx_Status* sets its output *Set_act_com* to 1, thus indicating to the *ACL* block (which keeps track of the Rx nodes with which Tx has active communications) to add the node Rx to the list of nodes with active communications. In addition, when *Set_act_com*=1,

Elab_MSG is enabled and starts elaborating the MSG to be sent (as in Fig. 2.1). Then, *Elab_MSG* sets *Msg_Ready* to 1, to indicate that the message given to its output (Out MSG), and loaded into the output register *reg 3*, is ready to be sent. Simultaneously, when *Msg_Ready*=1: i) the timer *Start_Tw* (which accounts for the maximum time that Tx waits for the arrival of the ACK from Rx) is enabled, and ii) the counter *Count_Ret* (which keeps track of the number of retransmissions) is incremented by one.

As for the Rx-part, its *Verify_ACK* block is enabled when *timeout*=1, which takes place when *Start_Tw* reaches its maximum count. The block *Verify_ACK* verifies the correctness of the Rx ID and the rolling code sequence (*#seq*) of the received ACK. If the Rx ID is correct and the *#seq* of the ACK is the same as the expected one (i.e., equal to *My_RC*), then *Verify_ACK* sets the signal *Load_ACK* to 1. When *Load_ACK*=1, *Verify_MAC* is enabled. This block regenerates the MAC from the clear text of the input ACK and compares it with the MAC received in the ACK. If both the received and the regenerated MACs are equal, then the input ACK is considered valid and *Verify_MAC* sets the signal *Valid_ACK* to 1. This indicates that the communication with Rx has been accomplished successfully. Then, Rx is removed from the list of nodes with active communications in *ACL*, and *RC_Gen* increases *My_RC* by 1.

Instead, if in the input ACK the IDs of the Rx or Tx are not valid, or the *#seq* is not equal to *My_RC*, then signal *Load_ACK*=0 (*Load_ACK#*=1) and the input ACK is discarded before analyzing its MAC. The input ACK is also discarded if its MAC is not correct. In this case it is *Valid_ACK* = 0 (*Valid_ACK#* = 1). When *Load_ACK#* or *Valid_ACK#* are set to 1, the signal ReTx is set to 1 and the *Out_MSG* is retransmitted to Rx. Then, *Start_Tw* is restarted, and the number of retransmissions is incremented by 1 in *Count_Ret*. If *Count_Ret* reaches n_{max}, it sets the signal *Update_PN* to 1, which labels the Rx as "problematic".

2.4 Summary

In this short chapter, a new communication protocol for wireless sensor networks has been developed allowing to make it secures with respect its most common attacks. As described in the Section 2.2, compared to the standard IEEE 802.15.4 and ZigBee protocols, the proposed protocol allows to increase security significantly, at negligible impact on node complexity. Finally, a possible hardware scheme to implement the protocol has been also shown in the Section 2.3.

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Chapter 3

Measurement scheme for process parameter variations and clock jitter

As known and briefly described in the first chapter of this thesis, with the continuous scaling of microelectronic technology, defects and parameter variations occurring during fabrication are becoming ever more likely and significant. In the case of high performance microprocessors, this is making increasingly difficult to guarantee the availability of clock signals with sharp edges, limited skew and jitter [3-1, 3-2, 3-3, 3-4].

Jitter affecting clock signals results in uncertainties on their period and rising/falling edges, thus forcing designers to either increase time margins (with consequent performance penalties), or face the possibility of operating malfunctions. None of these options are of course desirable for high performance microprocessors. Consequently, accurate on-die measurement of clock jitter is needed during the test and debug phase, to validate the design and manufacturing process, and evaluate the possible need for design or process improvements. Similarly, the continuous increase in process parameter

variations occurring during fabrication is creating uncertainties in the provided performance. In order to avoid increasing time margins, accurate on-die measurement of process parameter variations is needed during the test and debug phase. In order to cope with these problems, several proposed measurement schemes for clock jitter [3-4, 3-5, 3-6, 3-7, 3-8, 3-9] and process parameter variations [3-10, 3-11, 3-12] are based on the use of Ring Oscillators (ROs).

Based on these considerations, as well as on the widespread adoption (for high performance microprocessors) of RO based schemes for process variation measurement, in this chapter is proposed and analyzed a novel low cost scheme for the on-die measurement of either clock jitter, or process parameter variations. By re-using and properly modifying such ROs, the proposed scheme can be easily set in either the process parameter variation measurement mode, or the clock jitter measurement mode, by externally acting on the scheme control signal. This way, during the test or debug phase, clock jitter can also be measured at negligible area and power costs (6% and 1.4%, respectively) with respect to process parameter variation measurement only.

The rest of this chapter is organized as follows. In Section 3.1, it is briefly described the considered scheme for process parameter variation measurement, that has been properly re-used and modified to allow also clock jitter measurement. In Section 3.2, the proposed on-die measurement scheme is presented. Section 3.3 reports the results of the electrical level simulations performed to verify its accuracy in measuring clock jitter and process parameter variations. Finally, an evaluation about the costs of the proposed scheme and a comparison to those of the scheme in [3-10] for process parameter variation measurement is also shown.

3.1 Considered Measurement Scheme for Process Parameter Variation

As a general example, let refer to the process parameter variation measurement scheme in [3-10]. It consists of many Functional Unit Blocks (hereinafter referred to as a FUBs) that are properly distributed on the chip.

Each FUB presents the internal structure shown in Fig. 3.1 [3-10]. It consists of *q* ROs, each composed by *N* (usually N=99) NOTs. The number of ROs within a FUB and the number of FUBs on the chip depend on the available area and required measurement accuracy. The NOTs within each RO are equal to each other. Instead, the ROs within the same FUB are generally different. Particularly, several ROs are composed by min sized NOTs, several others by double min sized NOTs, several others by triple min sized NOTs, and so on. This allows achieving more accurate measurements of process parameter variations [3-10].

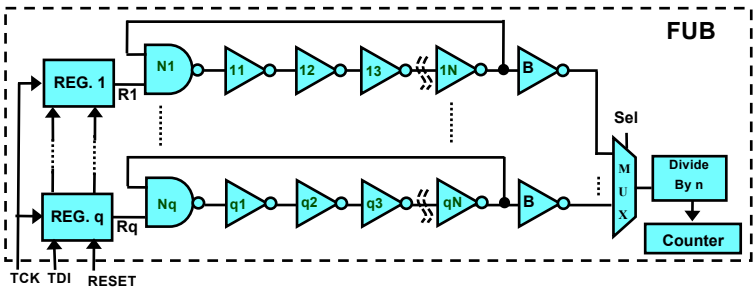


Figure 3.1: Internal structure of the FUBs in [3-10].

Each RO oscillates at a frequency that is a function of the average of the device parameter values at its location. Such a frequency is converted into a digital word (by a proper counter, Fig. 3.1), and then compared to the code expected under nominal values of process parameters. By back tracing the derived code difference to process parameter values, it is possible to get the measurement of the process parameter variations that occurred locally during fabrication. Moreover, by memorizing the oscillation frequency of each FUB, it is possible to map process parameter variations over the chip. The control signals (i.e., TCK, TDI and RESET in Fig. 3.1) for

the ROs may be configured via Test Access Port (TAP). Through these control signals, the REG *i* (*i=1..q*) registers are programmed to activate (by making Ri=1, *i=1..q*) only the RO required for the measurement. Then, a multiplexer (MUX in Fig. 3.1) selects the output of the RO that has been used for parameter variation measurement. Finally, a frequency divider (the Divide by n block in Fig. 3.1) reduces the oscillation frequency of the ROs, thus allowing to use a smaller counter.

3.2 Proposed On-Die Measurement Scheme

In this section, it is described how the previously described measurement scheme is re-used and properly modified in order to allow its adoption also for on-die clock jitter measurement. As for clock jitter measurement, it has been followed the well assessed and widely used approach of measuring the duration of the clock high or/and low phase/s over time, and comparing them to their expected duration for the case of jitter-free clock [3-9]. For the sake of brevity, it will be here considered the case of the clock high phase measurement only, which can however be extended to both clock phases' measurement by straightforward modifications. The proposed scheme is schematically shown in Fig. 3.2, for the case of jitter measurement resolution equal to a NOT input-output delay (t).

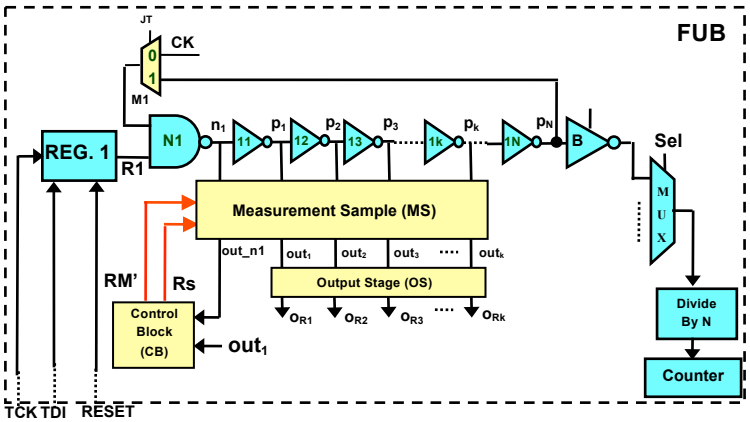
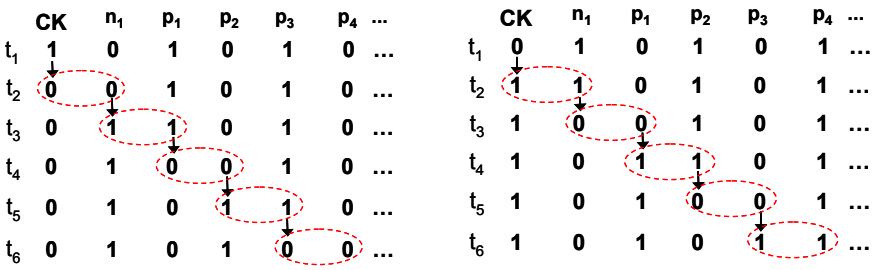


Figure. 3.2: Block structure of the proposed measurement scheme.

Since the global delay of the NOT chain used for jitter measurements should be long enough to cover the whole clock period (T_{CK}) [3-9], we re-used a number k of NOTs of the RO, such that $kt > T_{CK}$ (Fig. 3.2).

With respect to the scheme in Fig. 3.1, a multiplexer (M1 in Fig. 3.2) has been connected to the input of the N1 NAND. This way, by externally acting on the control signal JT, the proposed scheme can be easily set in either the process parameter variation measurement mode (JT=1), or the clock jitter measurement mode (JT=0). In fact, when JT =1, the proposed scheme is configured as in Fig. 3.1. Instead, when JT = 0, the input of the N1 NAND is connected to the input clock (CK), whose jitter has to be measured, so that the RO can be used to measure clock jitter, as described below in more details. When JT=0, the NOTs composing the RO, together with the N1 NAND, implement a delay line that delays signal CK (whose jitter has to be measured) by an amount of time. The output of the N1 NAND (n_1) is a delayed (by the NAND delay) and inverted version of CK. The outputs of the inverters p_i are progressively delayed (with a delay increasing with i), and inverted (for i even), versions of CK. The logic values simultaneously present on node n_1 and node p_i after a CK falling (rising) edge are reported in Fig. 3.3 (a) (Fig. 3.3(b)), in which each row represents the snap-shot at one specific instant of time, according to a vertical time axis.

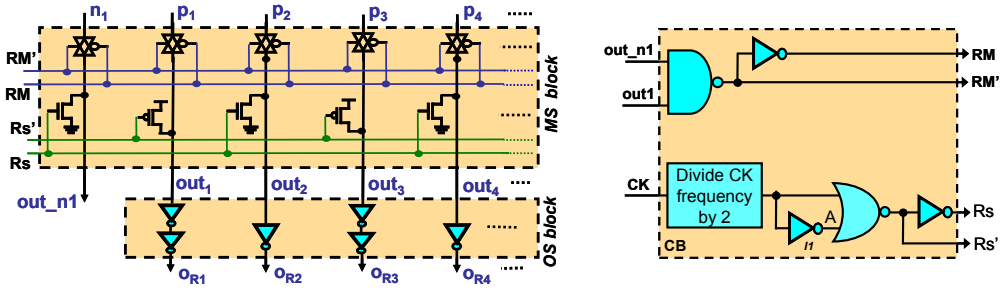


(a) (b)

Figure 3.3: (a) (b) Schematic representation of the propagation of the CK falling and rising edges, respectively, through the RO gates, when the proposed scheme is used to measure jitter.

The position of the CK falling (rising) edge is identified by the occurrence of two successive 0s, or two successive 1s, whose location moves progressively to the right. Therefore, but for the input NAND and MUX, when JT=0, the proposed scheme resembles the delay chain that is frequently adopted for clock jitter measurement [3-4, 3-5, 3-9].

As known, a major problem of clock jitter measurement schemes is to be able to make them insensitive to power supply noise [3-9]. To achieve this goal, similarly to [3-9], in the proposed scheme it is possible to sample the values present on the p_i signals (by asserting RM'=0) when the CK falling edge arrives to the input of the second element of the chain (i.e., to the input of the first NOT after the N1 NAND in Fig. 3.2), rather than when it arrives to the input of the first element of the chain (i.e., to the input of the N1 NAND). In fact, since power supply noise is most likely to occur upon clock edges (due to the simultaneous transition of all clock buffers, flip-flops, etc.), rather than at the middle or end of its period [3-13, 3-14, 3-15], and being the NOTs' behavior temporarily delayed because of such a power supply noise, it is possible to wait for the disappearance of such a temporary influence before sampling the values on p_i. Infact, the duration of the power supply noise is a random variable with a maximum value in the order of the rise time of the clock signal [3-15]. Therefore, the proposed scheme samples the values present on p_i (by asserting RM'=0) when $n_1=p_1=1$, that is at the time instant t_3 (Fig. 3.3 (a)). Then, the duration of the clock high phase is given by the number of NOTs within the chain that the CK rising edge has passed through before the CK falling edge arrives to the input of the chain. This can be identified by the Measurement Sample (MS) and Output Stage (OS) blocks in Fig. 3.2. They can be implemented as shown in Fig.3.4[3-9].



(a) (b)

Figure 3.4: Possible implementation of blocks MS and OS (a), and block CB (b) [3-9].

Similarly to the proposed scheme in [3-9], MS samples the values present on signals p_i ($i=1..k$) upon the falling edge of signal RM', which can be generated by the Control Block (CB) (Fig. 3.4 (b) [3-9]). The p_i ($i=1..k$) sampled values are given to signals out_i that, in the proposed scheme, are given to the OS block, which encodes them into a word belonging to the thermometer code (which is given on signals o_{Ri}). Then, the signal RM' remains low till reset (Rs), which is activated (Rs=1) by CB after a time interval long enough to allow to read the measurement. Afterwards, the circuit is ready to measure the duration of the next CK high phase. MS also samples the value of n_1 (i.e., output of the N1 NAND) on *out_n1*, which is used by the CB block to generate RM' and RM. The behavior of the MS, OS and CB blocks is the same as that of the same blocks in [3-9]. The produced output thermometer encoding allows to easily and quickly deriving the duration of clock jitter. As an example, the produced encoded o_{Ri} ($i=1..k$) word can be compared, by k parallel XORs, with that expected for the case of jitter-free clock, thus providing a k bit string with a number of 1s equal to the difference between the number of 0s in the produced encoded word and in the expected one (for the jitter-free case). Such a number of 1s can be easily counted. Jitter measurement can then be simply obtained by multiplying such a 1s count by the scheme resolution. It could be easily verified that the scheme in Fig. 3.2 has a resolution equal to a NOT delay (t). A higher measurement resolution can be easily achieved, by re-using

and properly modifying more ROs, rather than one. As an example, the scheme in Fig. 3.5 can be considered, which re-uses and properly modifies two ROs.

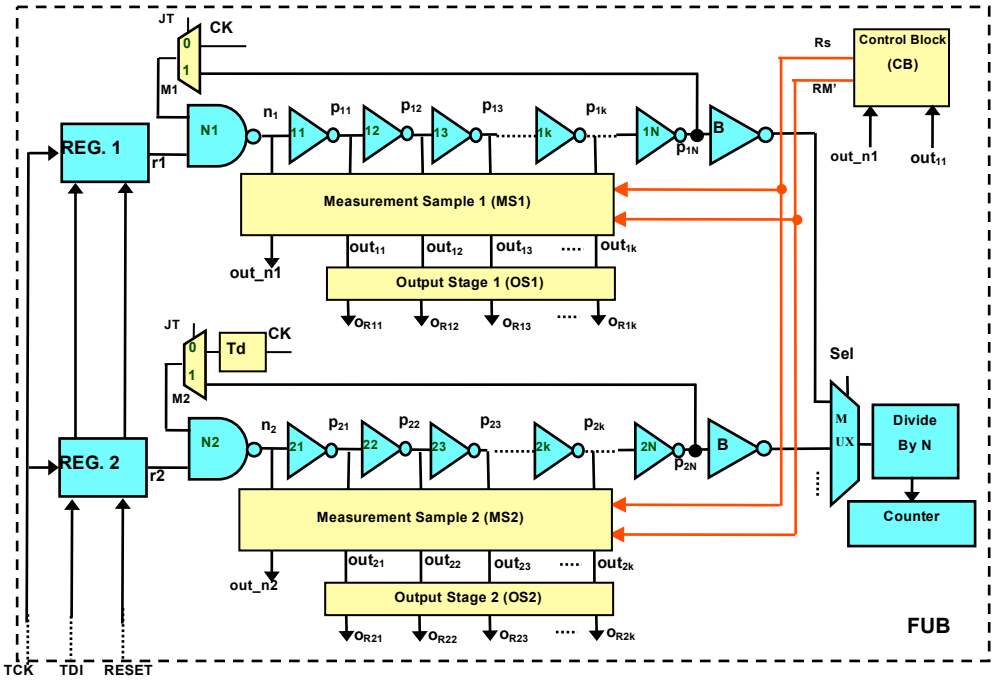


Figure 3.5: Block structure of the proposed scheme providing higher measurement resolution than that in Fig. 3.1.

This way, when the control signal JT=1 (i.e., in the process parameter variation measurement mode), the input of the N1 NAND is connected to p_{1N}, while the input of the N2 NAND is connected to p_{2N}. Instead, when JT = 0 (i.e., in the clock jitter measurement mode), the input of the N1 NAND is connected to CK, while the input of the N2 NAND is connected to the CK signal, properly delayed by a delay *Td* equal to half of the NOT input-output delay (*Td*=t/2). This way, as illustrated in Fig. 3.5, the outputs of the corresponding NOTs of the two chains (i.e., p_{1i} and p_{2i}) present a phase difference equal to t/2 (we here consider only the phase difference between signal edges, without addressing existing signal inversions, that will be accounted for by the OS block). Then, considering as output the alternated succession of the two NOT chains' outputs (i.e., p_{11}; p_{21}; p_{12}; p_{22}; p_{13}; p_{23}; etc., in Fig. 3.5), any two following outputs will

have a phase difference equal to t/2. Therefore, the scheme in Fig. 3.5 features a measurement resolution of half a min sized NOT input-output delay (i.e., t/2).

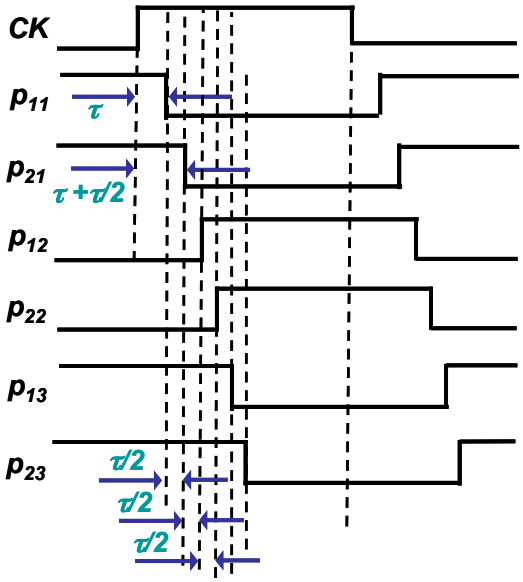


Figure 3.6: Schematic representation of the signals produced at the NOT outputs when the circuit is used to measure CK jitter.

In particular, MS1 (which is the same as the MS block in Fig. 3.2) receives the p_{1i} ($i=1..k$) signals from the NOTs of the upper RO, and produces k outputs out_{1i} ($i=1..k$). Similarly, MS2 (which is the same as the MS block in Fig. 3.2) receives the p_{2i} ($i=1..k$) signals from the NOTs of the lower RO, and produces k outputs out_{2i} ($i=1..k$). Thus, at the sampling instant, MS1 gives on signal out_{1i} the sampled value of p_{1i}, while MS2 gives on signal out_{2i} the sampled value of p_{2i} (Fig. 3.6). As for the case of one NOT chain, MS1 and MS2 sample the value of n_1 and n_2 on *out_n1* and *out_n2*, respectively. Signal *out_n1* is used by the CB block to generate RM and RM', while signal *out_n2* is discarded. Then, OS1 (which is the same as the OS block in Fig. 3.2) receives signal out_{1i} ($i=1..k$) from MS1, and produces the outputs o_{R1i} ($i=1..k$) encoded by a thermometer code. Analogously, OS2 receives signal out_{2i} ($i=1..k$) from MS2, and produces the outputs o_{R2i} ($i=1..k$) encoded by a thermometer code. Then, the jitter measurement is provided by the outputs of OS1 (o_{R1i}) and OS2 (o_{R2i}) , that is o_{R11}, o_{R21}, o_{R12}, o_{R22}, o_{R13}, o_{R23}, o_{R14}, o_{R24}, etc. Similarly to the proposed scheme in Fig. 3.2, in order to achieve low sensitivity to power supply noise, the values at the outputs of the

NOTs can be sampled by MS1 and MS2 when the CK falling edge arrives to the input of the first NOT of the upper RO (i.e., when $n_1=p_{11}=1$ in Fig. 3.6).

Similarly to [3-9], even higher resolutions in clock jitter measurement can be achieved by re-using *n* ROs of the FUB.

3.3 Measurement Accuracy

In order to compare the performance of the proposed model, it has been verified the capability of the scheme to measure process parameter variations as accurately as [3-10] (Fig. 3.1), and clock jitter as accurately as [3-9], by means of electrical simulations performed by HSPICE.

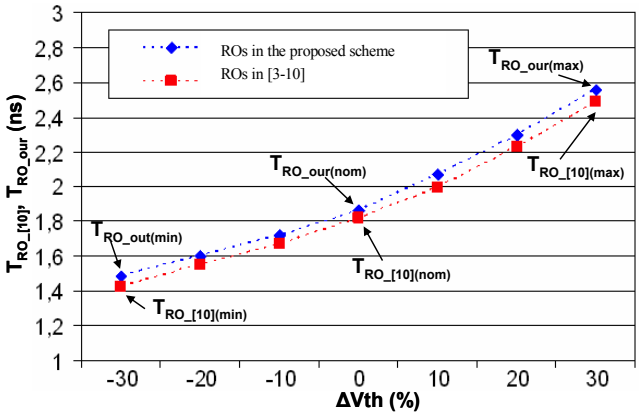
All schemes have been implemented by a standard 65 nm CMOS technology, with Vdd = 1.1V, and clock frequency of 3GHz. Moreover, the proposed scheme (Fig. 3.5), as well as that in [3-9], measures the CK high phase and allows a jitter measurement resolution of half the delay of a min sized NOT. In addition, as for the illustrated scheme (Fig. 3.5), as well as that in [3-10], it has been considered: i) 8 ROs, out of which 2 are composed by 99 min sized NOTs, 2 by 99 double min sized NOTs, 2 by 99 triple min sized NOTs, and 2 by 99 quad min sized NOTs; ii) a Div. by 16 block; iii) a 10 bit counter.

Let's start showing the ability of the proposed scheme to measure process parameter variations as accurately as the original scheme in [3-10].

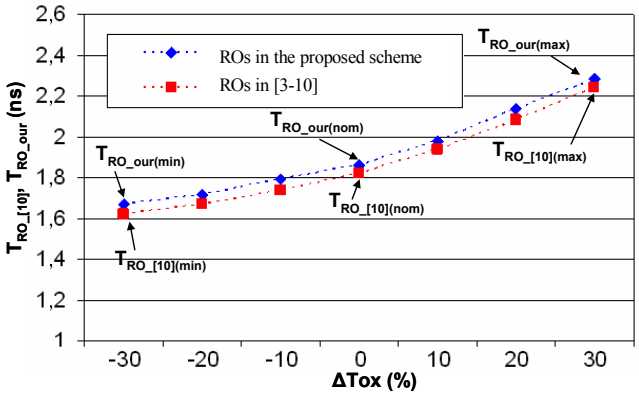
By means of Hspice simulations, the oscillation period (T_{RO}) of the ROs of the original scheme in [3-10] ($T_{RO\_[10]}$) has been compared with that of the ROs of the proposed scheme (T_{RO_our}), as a function of parameters Vth and Tox.

As an example, Fig. 3.7(a) shows $T_{RO\_[3\text{-}10]}$ and T_{RO_our} as a function of parameter Vth, varying of ±30% from its nominal value. Can be seen that, throughout the considered variation interval, the difference among the oscillation periods of the ROs of the proposed scheme and those of the ROs in [3-10] is always negligible (reaching a maximum difference of 4% with respect to the oscillation period of the ROs in [3-10]), thus allowing a measurement of possible Vth variations as accurate as that provided by [3-10].

Instead, Fig. 3.7(b) shows $T_{RO\_[3\text{-}10]}$ and T_{RO_our} as a function of parameter Tox, varying of ±30% from its nominal value. Throughout the considered variation interval, it has been verified that the difference among the oscillation periods of the ROs of the illustrated scheme and those of the ROs in [3-10] is always negligible (reaching a maximum difference of 3% with respect to the oscillation period of the scheme in [3-10]), thus allowing a measurement of possible Tox variations as accurate as that provided by [3-10]. Similar results have been achieved for variations of different process parameters. Therefore, the proposed modifications to the scheme in [3-10] to allow also clock jitter measurement do not impact the measurement accuracy for process parameter variations.



a)



b)

Figure 3.7: Oscillation periods of the ROs in [3-10] ($T_{RO\_[3\text{-}10]}$), and in the proposed scheme (T_{RO_our}), as a function of parameters Vth (a) and Tox (b).

Now let's show the ability of the illustrated scheme to measure clock jitter as accurately as the recently proposed scheme in [3-9]. For the considered implementation of the proposed scheme, all NOTs of the two re-used and properly modified ROs present an input-output delay $\tau \cong 12ps$, so that, similarly to the scheme in [3-9], the developed scheme (Fig. 3.5) should provide a clock jitter measurement resolution of $Res=\tau/2 \cong 6ps$. Since the chains need to cover a full T_{CK} (≅333ps), the number of NOTs within each RO should be $\geq T_{CK}/\tau = 28$. Therefore, for the scheme in Fig. 3.5, it is $k=29$.

As an example, Fig. 3.8 shows the simulation results obtained for nominal values of electrical parameters, considering the case of: i) no jitter affecting the first measured CK high phase (CK HP 1); ii) a jitter of 7ps widening the second measured CK high phase (CK HP 2).

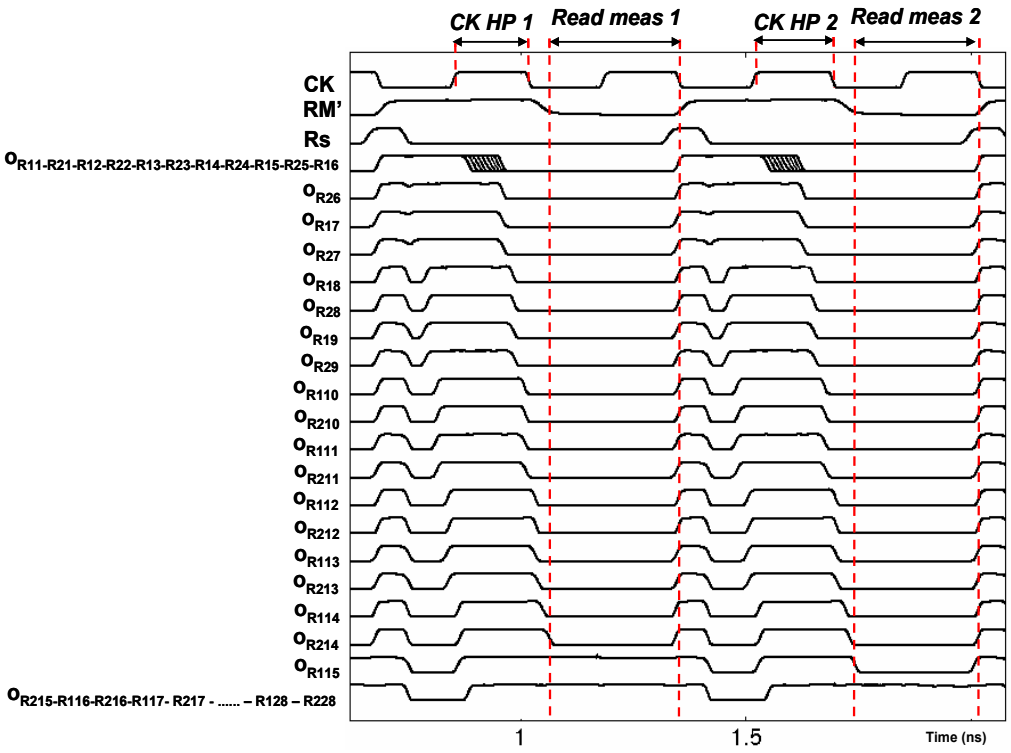


Figure 3.8. Simulation results for nominal values of electrical parameters and case of: i) no jitter (CK HP 1); ii) jitter of 7ps (CK HP 2).

As can be seen, when no jitter affects the CK high phase (CK HP 1), while

RM'=0 (Read meas 1 in Fig. 3.8), the proposed scheme gives to its outputs (o_{Ri}) a word encoded by the thermometer code with 28 zeros, as expected. With the proposed scheme it is possible to get the jitter measure expressed as the difference in the number of 0s between the produced output (=28) and the one expected for the jitter-free case (= $T_{CK}/2$ * 1/Res = 168 / 6 = 28) multiplied by the resolution of the proposed scheme (equal to 6ps). Of course, in this case it has been obtained a jitter measurement equal to 0ps, as it is actually the case. Instead, when for instance a jitter of 7ps affects the CK high phase (CK HP 2) while RM'=0 (Read meas 2 in Fig. 3.8), the scheme gives to its outputs (o_{Ri}) a word encoded by the thermometer code with 29 zeros. Therefore, in this case it has been obtained a measurement of jitter = 6ps. Therefore the developed scheme provides measurement accuracy as the scheme in [3-9].

Of course, the presence of local process parameter variations could affect the accuracy of the provided clock jitter measurement. However, through the possibilities to set the configuration of the proposed measurement scheme preliminarily in the process parameter variation measurement mode, and thank to the insensitivity of such provided measure to possible clock jitter, could allow to correct possible clock jitter measurement errors due to the presence of process parameter variations. In fact, by accurately measuring process parameter variations, their impact on the RO NOT delay ($\pm \Delta\tau$) can be evaluated. This, in turn, will impact the number of 0 given to the output of the proposed scheme, thus the derived clock jitter measurement. Particularly, denoting by *#0pv* (*#0pvf*) the number of 0s given to the output of the scheme in the presence (absence) of process parameter variations, it can be easily derived that:

$$\#0pv = (T_{CK}/2)*(n/(\tau \pm \Delta\tau)) \text{ and } \#0pvf = (T_{CK}/2)*(n/\tau) \quad (3.1)$$

where n denotes the number of ROs modified for jitter measurement, while τ is the NOT input-output delay expected in case of no process parameter variations. Therefore, once measured the possibly present parameter variations

and once derived their impact on the RO NOT delay (± Δτ), the clock jitter measurement provided by the proposed scheme can be corrected by adding to the obtained measurement a number of 0s equal to:

$$\#0pv - \#0pvf = (T_{CK} / 2) * (\pm n\Delta\tau / \tau (\tau \pm \Delta\tau)) \quad (3.2)$$

Of course, such process parameter variations will also impact the provided clock jitter measurement accuracy, which will become equal to $(\tau \pm \Delta\tau)/n$, where n is the number of ROs modified for jitter measurement, rather than being equal to a targeted *Res* value. This can be easily compensated by considering a proper number n of ROs, such that $n = (\tau \pm \Delta\tau) / Res$, where ± Δτ is derived from the performed process parameter measurement, τ is the value of the NOT input-output delay expected for the case of no process parameter variations, and *Res* is the target clock jitter measurement resolution.

Therefore, the proposed scheme allows obtaining an accurate measurement of clock jitter, despite the presence of process parameter variations, provided that process parameter variations are preliminary measured with respect to clock jitter.

3.3.1 Cost evaluation and comparison

Finally, the costs of the proposed approach have been evaluated the cost in terms of area overhead and power consumption. The proposed scheme has been implemented as described in the previous section.

Particularly, for simplicity, it has been considered each FUB composed by 8 ROs. However, it is worth noticing that usually the FUBs are composed by a number of ROs that is much higher than 8 [3-10]. Therefore, a pessimistic estimation of the area and power overhead of the illustrated scheme over [3-9] is provided.

As for area, it has been roughly estimated in squares, while power consumption has been evaluated by means of electrical simulations.

Tab. 3-I reports the costs of the scheme in [3-10] for process parameter

variation only, and those of the proposed scheme, allowing also clock jitter measurement.

TABLE 3-I. Area and power costs of the proposed scheme and that in [3-9].

Considered Scheme	Area (squares)	Area Overhead (%) $100 \cdot \frac{(A_{re-used\_FUB} - A_{orig\_FUB})}{A_{orig\_FUB}}$	Power Comp. (μW)	Power Overhead (%) $100 \cdot \frac{(P_{re-used\_FUB} - P_{orig\_FUB})}{P_{orig\_FUB}}$
Original FUB	9086	-	982	-
Re-used FUB	9656	+6%	996	+1.4%

As can be seen, the proposed modifications to the scheme in [3-10] allow achieving also clock jitter measurement at negligible relative increase in area overhead and power consumption, equal to 6% and 1.4%, respectively. Similar results are expected for other RO based process parameter variation measurement schemes.

3.4 Summary

As it has been described and shown in this chapter, a novel low cost scheme for the on-die measurement of either clock jitter, or process parameter variations has been proposed. By re-using and properly modifying the ring oscillators that are currently widely employed for process parameter variation measurement in high performance microprocessors, the proposed scheme can be easily set in either the process parameter variation measurement mode, or the clock jitter measurement mode, by acting on an external control signal. In particular, it has been shown that the proposed scheme allows to obtain clock jitter measurement at negligible relative increasing in area overhead and power consumption (6% and 1.4%, respectively) with respect to the frequently adopted scheme for process parameter variation measurement in [3-10].

Moreover, the developed scheme is scalable in the provided clock jitter measurement resolution, while allowing the same process parameter variation

measurement resolution as the ring oscillator based scheme in [3-10]. It should be noted that due to its allowing both process parameter variation and clock jitter measurements, the novel scheme developed features accurate clock jitter measurement, despite the possible presence of significant process parameter variations, provided that process parameter variations are preliminary measured with respect to clock jitter.

Finally, the proposed approach can be easily applied also to other process parameter variation measurement schemes by means of straightforward modification, for which similar results are expected.

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Chapter 4

Faults affecting energy harvesting circuits of self powered wireless sensors

Wireless sensing systems have recently gained a lot of interest, and their employment opens new possibilities in large scale, easy and low cost data capture. The main challenge in the use of such systems is associated with their power supply, today's still mainly provided by batteries. There is a tradeoff between the size of the energy storage element (i.e., the battery) and the lifetime of the device. Due to the required small size and frequent remote deployment, any servicing linked with battery replacement is impractical. Therefore, systems using ambient energy as additional energy source have recently gained a considerable interest. They employ a circuit that harvests energy from the environment in which they are embedded to obtain the required energy. Systems exploiting Energy Harvesting (EH) would also feature higher reliability than those using a fixed battery. In fact, they are less likely to suffer from common problems of depleted energy supply, and therefore limited lifetime. This is of great importance in case of powering

biomedical wearable sensors monitoring critical human vital parameters (e.g., breathing, heart activity, etc.). Although energy harvesting circuits (EHCs) could in principle be more reliable than fixed batteries, they are generally composed by many components (e.g., diodes, switching transistors, capacitors, inductors, etc.) that may fail during their in-field operation, due to material degradation, or electromagnetic interference [4-1, 4-2]. Up to now, many architectures for mechanical EH systems have been proposed [4-3, 4-7, 4-8] but none of them has yet considered the effects of faults possibly affecting its components. Based on these considerations, during the research activity, it has been analyzed the effects of faults affecting an integrated circuit performing energy harvesting from mechanical vibrations, and powering a wireless biomedical multisensor node. The EHCs is implemented by the same CMOS technology as the considered multisensor node, and have been analyzed the effects of all possible faults affecting the EHC. The obtained results are presented in this chapter. Particularly, it will be shown that they may make the EHC fail to produce the required supply voltage to the sensor node, with consequent dramatic impact on reliability.

The rest of this chapter is organized as follows. In Section 4.1, a description of the considered energy harvesting circuit used to power the biomedical multisensor node considered in this work, is given. In Section 4.2, the effects of faults possibly affecting the considered EHC are analyzed. In Section 4.3, a low cost circuit to monitor concurrently the power supply voltage provided by the EHC is proposed and the results of the electrical simulations that have been performed to verify the correct operation of the developed monitoring circuit are presented. In Section 4.4, the self-checking ability of the circuit proposed with respect to its possible internal faults, is reported. An evaluation of its costs is also given in the Section 4.5.

4.1 The self powered wearable multisensor considered

For this work, the wireless biomedical multisensor node described in [4-2] has been considered. It is designed to monitor human vital parameters (in particular, breathing and heart activity) and consists of the following components:

1) a multisensor;
2) a signal-conditioning block;
3) a microprocessor;
4) communication terminals;
5) a powering system [4-2].

The node features three different operating modes: i) the stand-by mode, in which it consumes a power of 3μW; ii) the data acquisition (DA) mode (for data collection, processing and storing), for which a power lower than 1mW is reported; iii) the radio transmission (TX) mode (for the wireless transmission of collected data), during which the power consumption reaches a value slightly lower than 10mW [4-2]. The node is in the data acquisition (DA) mode most of the time, with short periodic radio transmission (Tx) phases.

The considered multisensor node is self-powered by an EHC (exploiting human vibrations) along with a rechargeable battery. The EHC is shown in Fig.4.1. It employs a piezoelectric generator to convert the kinetic energy generated from human vibrations into electrical energy [4-8].

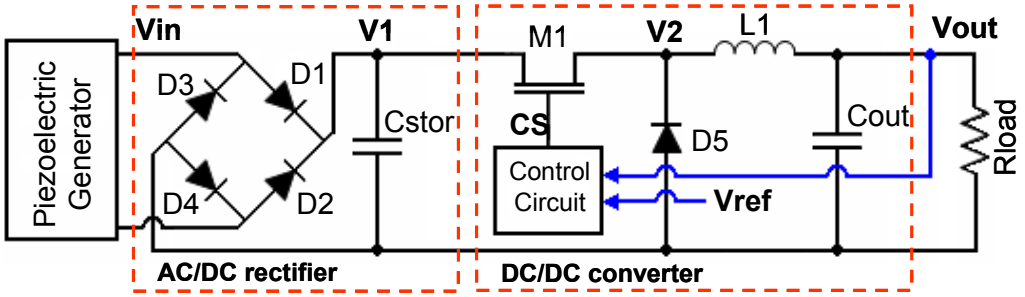


Figure 4.1: EHC used to power the considered multisensor node.

Such a piezoelectric generator is built using a cantilever beam with piezoelectric patches, as described in [4-9]. Since the voltage produced by the piezoelectric generator (V_{piezo}) is an AC voltage, it is converted into a DC voltage, in order to be exploited for powering the multisensor node, here represented by *Rload*. Particularly, first a full-wave AC/DC rectifier rectifies the AC voltage Vpiezo to a DC voltage, and then the produced DC voltage is regulated to a specific value by a step-down DC/DC converter (Fig. 4.1). The full-wave AC/DC rectifier consists of a diode bridge (D1-D4) and a storage capacitor (C_{stor}) that converts the AC voltage V_{piezo} into the DC voltage V1, which is maintained at the terminals of $C_{stor.}$ The DC voltage V1 is regulated to a lower, specific value (V_{out}) by the step-down DC/DC converter (Fig. 4.1), which also maintains constant such a V_{out} value (by its *Control Circuit* and M1 transistor), whichever the current absorbed by the powered sensor. Particularly, for the correct operation of the considered biomedical multisensor node, V_{out} should be kept in the [1.5V–2.1V] range [4-13, 4-14].

More in details, the DC/DC converter is composed of a transistor M1 and a diode D5 acting as switches and allowing to transfer the required amount of energy from the input (V_1) to the output (V_{out}). The inductor L1 and the capacitor C_{out} are used to filter out the oscillations on the voltage V_2, which can be induced by the commutation of M1 and D5. The *Control Circuit* generates a periodic control signal (V_{CS}) that turns the transistor M1 on and off, with a fixed frequency f_{CS}. This circuit compares the output voltage V_{out} with a reference voltage (V_{ref}), and based on such comparison result, it modifies the duty-cycle of signal V_{CS} (i.e., the time within $T=1/f_{CS}$ in which V_{CS} is 1) in order to make V_{out} equal to V_{ref}. The selection of the value of the frequency f_{CS} is based on design constrains of the discrete capacitors and inductors composing the EHC and does not affect the operation of the DC/DC converter. Typically, f_{CS} is selected within a range comprised between 1kHz and some tenths of kHz. The EHC in Fig. 4.1 has been implemented using the same 180*nm* standard CMOS technology as the considered multisensor node, and with discrete capacitors and inductors. In particular, all diodes (D1-D5) have

been implemented by MOS transistors with shorted drain – gate terminals, while the passive components are: $C_{storage}=180\mu F$, $C_{out}=500\mu F$ and $L1=22mH$. Based on the power absorbed by the multisensor node in the DA and Tx operating modes described above, and the required V_{out} value, *Rload* has been chosen equal to $5.3k\Omega$, in the DA mode, and to 530Ω, in the Tx mode. The described implementation guarantees a nominal V_{out} value of 2.1V, independently of the power consumed by the multisensor node.

4.2 Faults Affecting the Energy Harvesting Circuit and their Effects

Faults affecting the EHC in Fig.4.1 during its in field operation have been considered, and their produced impact on the provided V_{out} have been evaluated. For this analysis it has been supposed that the EHC is exhaustively tested after fabrication, thus it's fault-free at the beginning of its in field operation, with its capacitor C_{stor} properly charged. Particularly, all faults possibly affecting the EHC component sub-circuits (the AC/DC rectifier and the DC/DC converter) have been considered.

For each sub-circuit, the following all possible have been considered: i) node stuck-at 0 (SA0) [4-14]; ii) transistors stuck-on (SONs) [4-14]; iii) transistors stuck-open (SOP) [4-14]; iv) resistive bridgings (BFs), with realistic values of connecting resistance (R_{BF}) in the range]0..6kΩ] [4-14]. It is worth noticing that SA1 faults have not been considered, since they cannot realistically occur. In fact, in the EHC analyzed, any short between an internal node and the output V_{out} (which is the V_{dd} of the circuit itself) will produce a variation on the V_{out} voltage value, thus being more realistically modeled as a resistive bridge (with a value of the connecting resistance equal to 0), rather than as a stuck-at 1.

In addition, as usual to in-field concurrent detection, it has been assumed that faults occur one at a time in the field, and that the time elapsing between

the occurrence of two following faults is long enough to allow the application of all possible inputs [4-15].

As introduced before, for the reliable operation of the considered biomedical multisensor node, it is essential that such faults do not make V_{out} fall out of the required voltage range [1.5V – 2.1V]. However, this analysis applies also for different, possibly required voltage ranges. In order to evaluate the fault effects on the provided V_{out}, electrical simulations have been performed by means of HSPICE. The results of these analyses are reported in details in the following sub-sections.

4.2.1 Faults affecting the AC/DC rectifier and produced effects

In this subsection, the effects of all possible faults affecting the AC/DC rectifier of the EHC (Fig. 4.1) are analyzed.

A. Stuck-At-0 (SA0)

Let's start considering SA0s. They may affect the following nodes: i) V_{in}+; ii) V_{in}-; iii) V1. SA0 of kind i) is activated during the positive half-waves of V_{piezo} (Fig. 4.1), independently of the EHC operating mode. When the SA0 is activated, the AC/DC rectifier fails in rectifying the positive V_{piezo} half-waves, thus failing in charging C_{stor} (thus also C_{out}) to the expected value. Therefore, the provided V_{out} is lower than what expected under fault-free conditions. Moreover it has been verified that, due to its rapid drop to ground, the provided V_{out} does not suffice to the correct operation of the driven multisensor node, whichever the EHC operating mode. Therefore, the correct operation of the EHC, thus of the driven multisensor node, is compromised due to the considered SA0.

As for the SA0 of kind ii), it is activated during the negative half-waves of V_{piezo} (Fig. 4.1), independently of the EHC operating mode. When this SA0 is activated, the AC/DC rectifier fails in rectifying the negative V_{piezo} half-waves,

thus failing in charging C_{stor} up to the expected value. As a consequence, the DC/DC converter also fails in charging C_{out} to its expected value. Therefore, as for the SA0 of kind i), the voltage provided on V_{out} is lower than what expected under fault-free conditions and it does not suffice to the correct operation of the driven multisensor node, whichever the EHC operating mode. As a consequence, also in this case, the correct operation of the EHC, thus of the driven multisensor node, is compromised.

The SA0 of kind iii) is activated during the time intervals in which $|V_{piezo}| > |V_{Cstor}|$, independently of the EHC operating mode. When this SA is activated, the capacitor C_{stor} turns out to be not connected to the EHC, and the whole current produced by the piezoelectric generator flows to ground, being V1 SA0. Consequently, the capacitor C_{out} is quickly discharged and the voltage provided on V_{out} drops rapidly to ground. Therefore, also in this case, the correct operation of the EHC, thus of the driven multisensor node, may be compromised.

B. Transistor SONs / SOPs

Now let's consider SONs/SOPs that may affect the transistors implementing (Fig.4.1): i) diodes D1, D4; ii) diodes D2, D3.

As for SONs/SOPs of kind i), they are activated during the time intervals in which $|V_{piezo}| > |V_{Cstor}|$, and reduce the average current that charges the capacitor C_{stor}. As a consequence, the DC/DC converter does not receive as input the power required to keep V_{out} constant when the multisensor starts a transmission (i.e., during the TX operating mode), thus producing a temporary voltage drop that compromises the correct operation of the EHC and the driven multisensor node. As for SONs/SOPs of kind ii), they are activated during the time intervals in which $|V_{piezo}| < |V_{Cstor}|$. We have verified that these SONs/SOPs produce the same effects as SONs/SOPs of kind i) above, causing a temporary voltage drop during the TX operating mode, thus possibly compromising the correct operation of the EHC and the driven multisensor node.

C. Bridging Faults (BFs)

Now all possible BFs are analyzed, with realistic values of connecting resistance (R_{BF}) in the range]0..6kΩ] [4-14]. Their activating conditions, as well as their produced effects during both the DA and Tx operating modes are summarized in Table 4-I.

TABLE 4-I: Effects of BFs possibly affecting the AC/DC converter.

BF	Activating Condition	No Effect		Gradual Degradation to GND		Overshoot	
		DA	TX	DA	TX	DA	TX
V_{in}^{+} – GND	V_{piezo}>0V	]0,6kΩ]	--	--	]0,6kΩ]	--	--
V_{in}- – GND	V_{piezo}<0V	]0,6kΩ]	--	--	]0,6kΩ]	--	--
V_{in}^{+} – V_{in}-	V_{piezo}≠0V	]0,6kΩ]	--	--	]0,6kΩ]	--	--
V_{in}^{+} – V1	$\|V_{piezo}\|>\|V_{Cstor}\|$	]0,6kΩ]	--	--	]0,6kΩ]	--	--
V_{in}- – V1	$\|V_{piezo}\|>\|V_{Cstor}\|$	]0,6kΩ]	--	--	]0,6kΩ]	--	--
V_{in}^{+} – V_{out}	$V_{piezo} \neq 2.1V$	]0,6kΩ]	--	--	]0,6kΩ]	--	--
V_{in}- – V_{out}	$V_{piezo} \neq 2.1V$	]0,6kΩ]	--	--	]0,6kΩ]	--	--
V1 – V_{out}	$V_{Cstor} \neq 2.1V$	--	--	--	]0,6kΩ]	]0,6kΩ]	--
V1 – GND	$V_{Cstor} > 0$	--	--	]0,6kΩ]	]0,6kΩ]	--	--

Particularly, it has been verified that, when activated, each BF (but for the V1-V_{out} BFs discussed below) results in a V_{out} gradual voltage drop to ground, thus making the voltage provided on V_{out} not sufficient for the correct operation of the driven multisensor node, whose correct operation is consequently compromised. This situation is illustrated in Fig. 4.2, which reports, as an example, the results of the electrical simulation performed considering a BF between V_{in}+ and GND, with a value of connecting resistance R_{BF} = 1kΩ and the multisensor node operating in the DA mode for $t < t_1$, and in the TX mode for $t \geq t_1$.

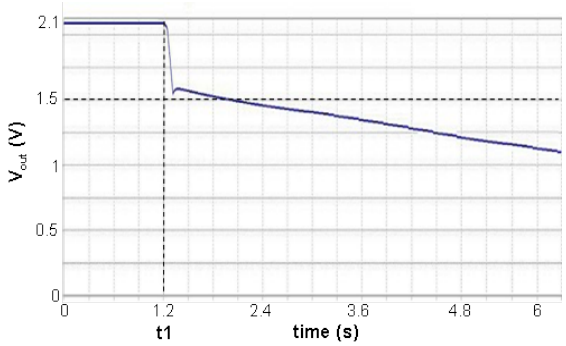


Figure 4.2: Variation of the voltage on V_{out} due to a BF (with R_{BF} = 1kΩ) between V_{in}+ and GND.

As can be seen from Fig. 4.2, after the multisensor enters the TX mode at t_1, the voltage V_{out} quickly drops to a value slightly higher than 1.5V, which is the minimum voltage value required by the multisensor node to operate correctly. Afterwards, it continues to drop gradually to ground, reaching 1.5V soon after t1. The BF between V1 and V_{out} is activated each time the voltage value on V1 (i.e., the voltage across C_{stor}) differs from the voltage value on V_{out} (i.e., 2.1V). In particular, this BF connects the positive terminals of C_{stor} and C_{out}, thus originating a charge distribution process between them. This situation is shown in Fig. 4.3.

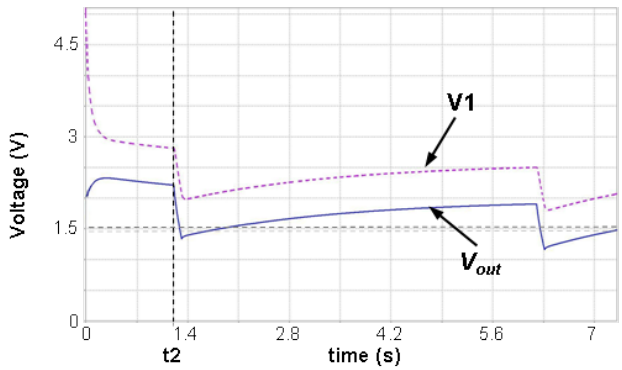


Figure 4.3: Variation of the voltage on nodes V_{out} (solid line) and V1 (dashed line) in case of a BF (with R_{BF} = 500Ω) between them.

As can be seen, this BF generates an initial voltage overshoot (for $t < t_2$) on V_{out}, which reaches approximately 2.4V (a value higher than the maximum tolerated voltage of 2.1V), while producing a reduction in the voltage value V1

across C_{stor}. This reduction is caused by a decrease in the charge stored on C_{stor}, which makes the EHC fail in keeping V_{out} above 1.5V when the multisensor node switches from the DA mode to the TX mode at time t2 (Fig. 4.3). Following commutations of the multisensor node from the DA mode to the TX mode reduce further the voltage value on V_{out}, which gradually decreases to GND. Therefore, also in this case, the correct operation of the EHC, thus of the driven multisensor node, may be compromised.

4.2.2 Faults affecting the DC/DC converter and produced effects

In this subsection, the effects of all possible faults of the DC/DC step-down converter of the EHC (Fig. 4.1) are analyzed.

A. Stuck-At-0 (SA0)

Let's start considering SA0s that may affect nodes (Fig. 4.1): i) V2; ii) V_{out}; iii) V_{cs}. It has been verified that the SA0 of kind i) is activated during the time intervals in which V_{cs} presents a high logic value (i.e., V_{cs}=2.1V) and the nMOS transistor M1 is conductive. This SA0 prevents the current coming from the AC/DC rectifier from flowing through the inductor L1. Consequently, the capacitor C_{out} is quickly discharged and the voltage V_{out} drops rapidly to ground. As a consequence, the correct operation of the EHC (thus, of the driven multisensor node) may be compromised. Similar results have been obtained for SA0s of kind ii) and iii).

B. Transistor SONs / SOPs

SONs/SOPs that may affect the following transistors (Fig.4.1): i) M1; ii) D5.

It has been verified that the SON of kind i) is activated during the time intervals in which V_{cs}=0V. This fault connects permanently nodes V1 and V2 (Fig. 4.1), and its effect on the output of the EHC is similar to that of a BF between nodes V1 – V_{out} described in the previous subsection and schematically represented in Fig. 4.3. Thus, a SON of kind i) produces an

initial overshoot on V_{out}. Then, after successive commutations of the multisensor node from the DA to the TX operating mode, it causes a gradual drop to ground of V_{out}. Therefore, the correct operation of EHC and the driven multisensor node may be compromised.

The SON of kind ii) is activated during the time intervals in which V_{cs}=0V (nMOS M1 off). This SON produces a permanent conductive path from node V2 (Fig. 1) to ground, thus not allowing charging the output capacitor C_{out}. As a consequence, V_{out} drops to ground after the next transmission of the multisensor node, and the correct operation of EHC, as well as that of the driven multisensor node, is compromised.

As for the SOP of kind i), it is activated during the time intervals in which V_{cs} presents a high logic value (i.e., V_{cs}=2.1V), and induces operating conditions similar to those previously described for the SA0 affecting node V2. Particularly, in this case, the DC/DC converter is disconnected from the AC/DC rectifier, since the transistor M1 is always off. Consequently, the capacitor C_{out} is quickly discharged and the voltage provided on V_{out} rapidly drops to ground. Similarly to the previous case, the correct operation of EHC and the driven multisensor node are compromised.

Finally, the SOP of kind ii) is activated during the time intervals in which V_{cs}=0V. Due to this SOP, the diode D5 is always off, and after V_{cs} flips to 0 switching off M1, no current flows through L1, as in the fault-free case. This prevents the DC/DC converter from charging C_{out} up to its expected value. Therefore, the voltage provided on V_{out} turns out to be lower than that expected under fault-free conditions, and it does not suffice to the correct operation of the multisensor node. Therefore, the correct operation of the EHC, and of the driven multisensor node, is compromised.

C. Bridging Faults (BFs)

Let's now consider all possible BFs, with realistic values of connecting resistance (R_{BF}) in the range]0..6kΩ] [4-14]. The activating conditions, as well as the produced effects during both the DA and the TX operating modes are summarized in Table 4-II.

TABLE 4-II: Effects of BFs possibly affecting the DC/DC converter

BF	Activating Condition	No Effect		Drop to GND		Gradual Degradation to GND	Overshoot
		DA	TX	DA	TX	TX	DA
V2-GND	Vcs = 2.1V	]0,6kΩ]	--	--	--	]0,6kΩ]	--
V1 - V_{CS}	Vcs = 0V	--	--	--	--	]0,6kΩ]	]0,6kΩ]
V1 - V2	Vcs = 2.1V	--	--	--	--	]0,6kΩ]	]0,6kΩ]
V_{CS} - V2	Vcs = 2.1V	--	--	]0,4kΩ]	--	]4k,6k]Ω	--
V_{out}-GND	$V_{out} \neq 0V$ (normal operation)	--	--	]0,6kΩ]	]0,6kΩ]	--	--
V_{CS}-GND	Vcs =2.1V	]0,6kΩ]	--	--	--	]0,6kΩ]	--
V_{CS}-V_{out}	Vcs = 0V	]0,6kΩ]	--	--	--	]0,6kΩ]	--
V_{ref} -V_{CS}	Vcs = 0V	]0,6kΩ]	--	--	--	]0,6kΩ]	--
V_{ref} -V_{out}	$V_{out} \neq V_{ref}$	]0,6kΩ]	]0,6kΩ]	--	--	--	--
V2 -V_{out}	$V2 \neq V_{out}$	]0,6kΩ]	]0,6kΩ]	--	--	--	--

Is it possible to observe that the BF between node V2 and ground affects the output voltage V_{out} only during the TX mode, resulting in a gradual degradation to ground for all bridging resistance values in the considered range. Therefore, this BF may compromise the correct operation of EHC and of the driven multisensor node. A similar behavior has been verified also for BFs between nodes V_{cs}- V_{out}, V_{cs}- GND, $V_{ref} - V_{cs}$, and V_{cs}- V2, the latter for values of connecting resistance in the range 4-6kΩ.

As for the BF between V1 and V_{cs}, it makes transistor M1 permanently ON. This BF produces similar effects to the BF between V1 and V_{out} described in the previous subsection for the AC/DC converter. Therefore, the correct operation of EHC and of the driven multisensor node may be compromised. Moreover, a similar behavior occurs also for the BF between V1 and V2. As for the BF between V_{out} and GND, it always affects V_{out} (Table 4-II). Fig. 4.4 shows the effects on voltage V_{out} after this BF occurs at time t3, with a bridging resistance R_{BF}=500Ω. As can be seen, this BF makes V_{out} quickly drop to

ground, thus compromising the correct operation of the driven multisensor node. It has been verified that a similar behavior occurs also for BFs between nodes V_{cs} and V2, for values of connecting resistance in the range 0-4kΩ.

Finally, the BF between V_{ref} and V_{out} is never activated, independently of the multisensor operating mode, since during the multisensor normal operation it is always $V_{ref} = V_{out} = 2.1V$. Therefore, this fault does not produce any effect on V_{out}. Moreover, has been verified that, if this fault is followed by any one of the faults analyzed before and making $V_{out} \neq 2.1V$, the resulting effect on V_{out} is the same as that generated by the second fault only, which has been analyzed before. A similar behavior is obtained also for the BF between nodes V2 and V_{out}.

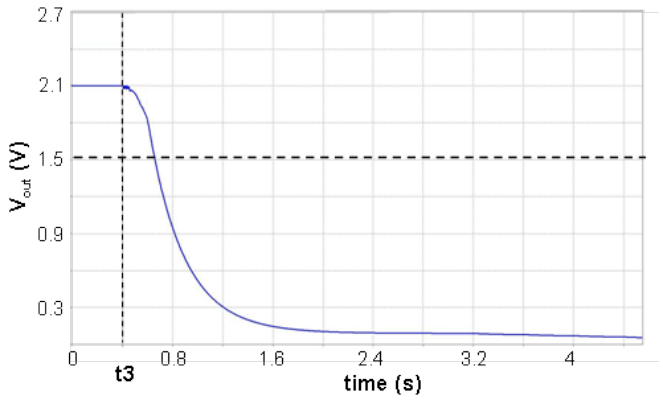


Figure 4.4: Simulation results showing the variation of the voltage on V_{out} due to a BF (with $R_{BF} = 500\Omega$) between V_{out} and GND**.**

4.3 Proposed Energy Harvesting Concurrent Monitoring Circuit

In order to monitor continuously, and concurrently with the system operation, the correctness of the voltage V_{out} provided by the EHC a monitoring circuit has been proposed and validated. The monitor generates an error message when V_{out} drops below 1.5V (that is, below the minimum voltage value required by the sensor to work properly), or when it is affected by internal faults (as will be shown in the next section). The proposed circuit is

schematically shown in Fig. 4.5. The pMOS M1 and the capacitor C1 generate an auxiliary voltage V_{aux}, which is used as power supply for our circuit. In fact, the circuit cannot use V_{out} as power supply, since it should provide an error indication when, in case of faults, V_{out} drops below the required voltage value. Under fault-free conditions, it is $V_{aux} \cong V_{out}$. Transistor M1 operates as a diode, allowing a current to flow from V_{out} to V_{aux} , thus charging C1, when $V_{out} > V_{aux}$ (i.e., when the circuit is turned on). Instead, transistor M1 avoids current to flow from V_{aux} to V_{out} when $V_{out}<V_{aux}$ due to a fault affecting the EHC, thus avoiding the discharge of C1.

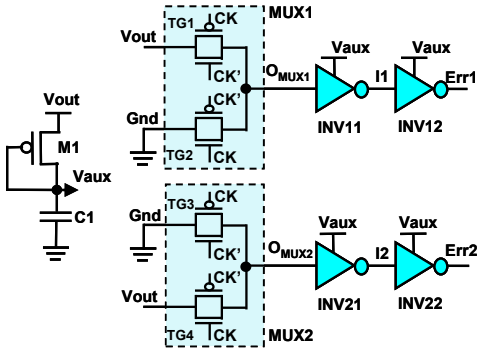


Figure 4.5: Proposed monitoring circuit

Therefore, after V_{out} drops due to a fault affecting the EHC, C1 allows to keep V_{aux} approximately constant for a chosen time interval (that is a function of the C1 value), thus allowing the circuit to provide an error indication. MUX1 and MUX2 receive V_{out} and ground (*GND*) as inputs, while the system clock (*CK*) acts as control signal. In particular, when *CK=0*, it is $O_{MUX}=V_{out}$ and $O_{MUX2}=0$, while when *CK=1,* it is $O_{MUX1}=0$ and $O_{MUX2}=V_{out}$. Each multiplexer has been implemented using two transfer gates (TGs). They are driven by the system clock (*CK*) and its complement (*CK'),* whose correct synchronization could be easily checked using a circuit of the kind in [4-9]. As for inverters INV11 and INV21, they are pMOS dominant, and designed to have a nominal logic threshold voltages (denoted as $V_{LT\text{-}PD}$) equal to the 72% of their power supply voltage (V_{aux}). Finally, INV12 and INV22 are minimum sized, symmetric inverters, employed to reshape the signals on nodes *I1* and *I2*.

Let's describe now in details the operation of the circuit proposed. First let's consider the fault-free case. Under this condition, the voltage V_{out} is approximately equal to V_{aux}. When CK=0, it is $O_{MUX1} = V_{out}$ ($\cong V_{aux}$), thus INV11 produces a low logic value ($I1=0$). Instead, since it is $O_{MUX2}=0$, INV21 produces a high logic value ($I2=1$). Therefore, when CK=0, the outputs of our circuit are ($Err1, Err2)=(1,0)$.

When $CK=1$, it is $O_{MUX1}=0$, so that INV11 produces a high logic value ($I1=1$). As for O_{MUX2}, it results $O_{MUX2}=V_{out}$ ($\cong V_{aux}$), thus it is $I2=0$. Therefore, when CK=1, the outputs of our circuit are $(Err1, Err2) = (0,1)$.

Therefore, on the whole, under fault-free conditions, the outputs of our monitor present always alternating and complementary logic values.

Now let's analyze the case of a fault affecting EHC, and making V_{out} drop below 1.5V. Let's refer to this value as V_{outmin}. In this case, V_{out} it is lower than the 72% of V_{aux}, which is maintained equal to 2.1V by C1. Since V_{aux} acts as power supply for inverters INV11 and INV21, it is $V_{outmin}=V_{LT\text{-}PD}=1.5V$, where $V_{LT\text{-}PD}$ denotes the logic threshold voltage of the two inverters.

When $CK=0$, it is $O_{MUX1}=V_{out}$. Since it is $V_{out} < V_{outmin} = V_{LT\text{-}PD}$, it is also $O_{MUX1} < V_{LT\text{-}PD}$. Consequently, INV11 produces a high logic value as output ($I1=1$). On the other hand, it is $O_{MUX2}=0$, so that also INV21 produces a high logic value ($I2=1$). Thus, when $CK=0$, the outputs of our monitor are $(Err1, Err2) = (0,0)$. When $CK=1$, it is $O_{MUX1}=0$, thus INV11 produces a high logic value ($I1=1$). Meanwhile, it is $O_{MUX2} =V_{out} < V_{outmin}=V_{LT\text{-}PD}$, so that $I2=1$. Therefore, also when $CK=1$, the outputs of our monitor are $(Err1, Err2)=(0,0)$.

This way, when V_{out} drops below 1.5V, the proposed monitor gives non-complementary values on $Err1$ and $Err2$ during the whole CK cycle. It is possible to assume that $(Err1, Err2) = (0,0)$ or $(1,1)$ are indications of either faults affecting EHC or, as shown in Sect. 4.4, faults affecting the proposed monitor. Instead, $(Err1, Err2) = (1,0)$ or $(0,1)$ are indications of fault-free operation.

4.3.1 Implementation and validation

The described monitoring circuit has been implemented considering a standard 0.18µm CMOS technology of the kind considered in [4-13] for the connected multisensor node. Particularly, it has been considered the following transistor aspect ratios and components for the circuit in Fig. 4.5: (i) *(W/L)=1* for the nMOS and *(W/L)=2* for the pMOS of the TGs; (ii) *(W/L)=1/20* for the nMOS and *(W/L)=50* for the pMOS of INV11 and INV21: (iii) *(W/L)=1* for the nMOS and *(W/L)=2* for the pMOS of INV12 and INV22; (iv) *(W/L)=20* for the pMOS M1; (v) C1=10µF. It is worth noticing that the value of C1 is high enough to guarantee the correct operation of circuit monitor for many seconds after V_{out} goes below 1.5V, thus allowing the activation of proper recovery approaches. The behavior of the implemented circuit monitoring has been analyzed by conventional and Monte Carlo electrical simulations, performed considering statistical variations (with uniform distribution) up to 20% of oxide thickness, transistor threshold voltage and electron/hole mobility.

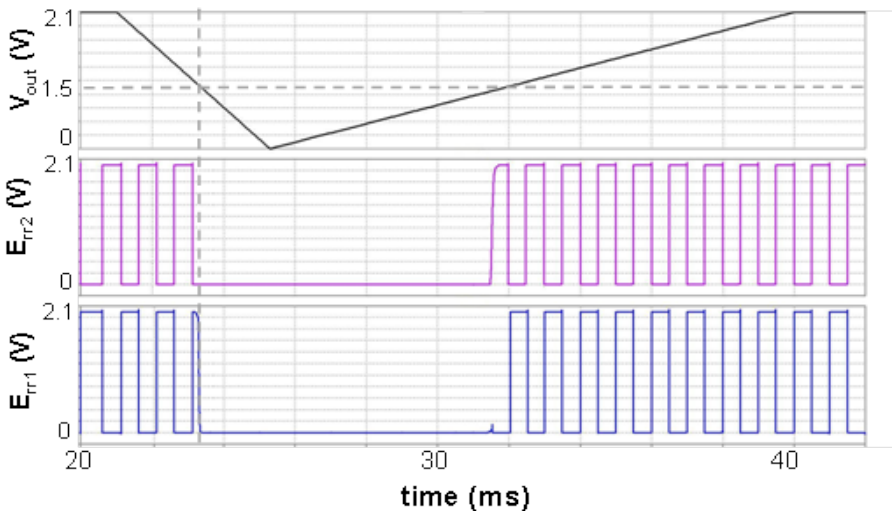


Figure 4.6: Simulation results obtained for nominal values of electrical parameters and temporary drop of V_{out} (due to faults) greater than the 28% of its nominal value**.**

Fig. 4.6 reports the simulation results obtained under nominal values of electrical parameters in case of faults making V_{out} temporary lower than V_{outmin}=1.5V. Is it possible to observe that, during the time interval in which V_{out} is lower than V_{outmin}, it is *(Err1, Err2) = (0,0)*, thus indicating the presence of an incorrect voltage value on V_{out}. Instead, Fig.4.7 shows some results of the Monte Carlo simulations that have been performed to analyze how parameter variations occurring during fabrication impact the V_{outmin} value, that is the minimum V_{out} value resulting in an error indication at the output of our monitor. As can be seen, V_{outmin} varies between 1.55V and 1.30V, thus changing with respect to the value expected by design (equal to 1.5V). Therefore, process parameter variations can make our monitor generate: i) false error indications (if V_{outmin} > 1.5V), or ii) false indications of correct operation (if V_{outmin} < 1.5V).

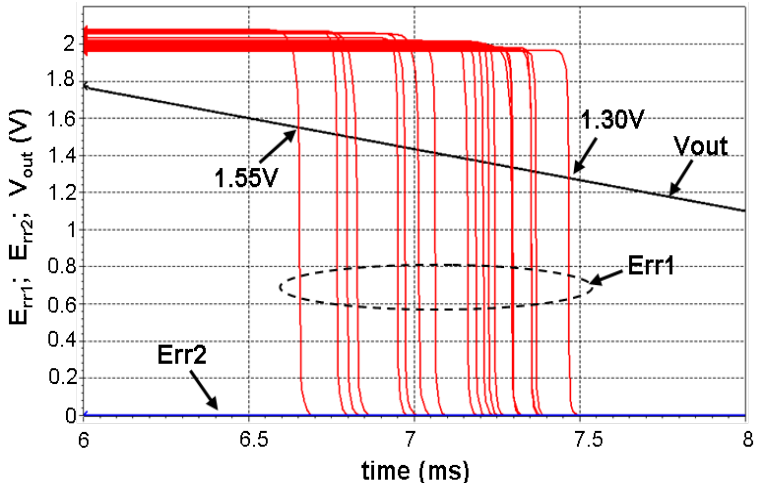


Figure 4.7: Monte Carlo simulations showing the minimum voltage value on V_{out} resulting in an error indication in case of statistical variations of electrical parameters up to 20%.

In order to avoid i) and ii) above, the inverters of the proposed monitor could be designed to allow the calibration of their logic thresholds after fabrication, for instance by adopting the approach in [4-17]. The derived inverter is shown in Fig. 4.8, where the programming signals Cpi (Cni) (i=1.3)

allows to choose the number of conductive pMOS (nMOS) in series with MP0 (MN0), thus allowing to calibrate the gate logic threshold. Of course, this implies an extra cost in area which, however, has a negligible impact the EHC area, as will be shown in Section 4.5.

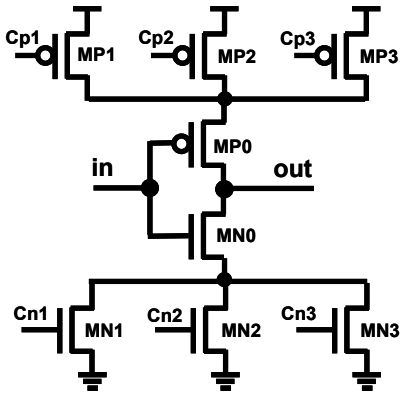


Figure 4.8: Inverter derived from [4-17] allowing logic threshold calibration after fabrication.

4.4 Self-checking ability

As previously discussed, the developed monitor may be itself affected by faults. To guarantee system high reliability, similarly to checkers of self-checking circuits (SCCs) [4-15], the described monitor should be able to check itself with respect to possible internal faults, and satisfy either the *Totally Self-Checking* (*TSC*) [4-15], or the *Strongly Code-Disjoint* (*SCD*) [4-18] property, with respect to such internal faults. As usual to self-checking circuits, it has been assumed that faults in the field occur one at a time, and that the time elapsing between the occurrences of two following faults is long enough to allow the application of all possible input code words (i.e., the correct V_{out} value) [4-15].

Moreover, the considered set of faults $\mathcal{F}$ possibly affecting the developed monitor is composed by all possible node stuck-ats (SAs), transistor stuck-opens (SOPs), transistor stuck-on (SONs) and resistive bridgings (BFs), with

realistic values of connecting resistance (R) in the range[0..6kΩ] [4-14]. Faults effects have been analyzed by means of logical and electrical simulations. The achieved results are summarized below.

A. Stuck-At-Faults (SAs)

Let's start considering node SAs 1/0. They may occur on nodes: i) O_{MUX1}, O_{MUX2}; ii) *I1*, *I2*; iii) *Err1*, *Err2*; iv) *CK*, *CK'*; v) V_{aux}. The activating conditions of the considered SAs 1/0 are summarized in Table 4-III.

TABLE 4-III: Activating conditions for the considered SAs possibly affecting the proposed monitor.

	Kind of SA								
	i		**ii**		**iii**		**iv**		**v**
	O_{MUX1}	**O_{MUX2}**	**I1**	**I2**	**E_{rr1}**	**E_{rr2}**	**CK**	**CK'**	**V_{aux}**
SA0	CK=0	CK=1	CK=0	CK=1	CK=1	CK=0	CK=1	CK=0	CK=0 or CK=1
SA1	CK=1	CK=0	CK=1	CK=0	CK=0	CK=1	CK=0	CK=1	-

As for SAs of kind i), it has been verified that before these faults are activated, they do not affect the correct operation of the proposed monitor. Additionally, when these faults are activated, an error indication is produced during one of the *CK* semi-periods (see Table 4-III), so that the circuit is *TSC* with respect to them. Analogous considerations hold true for SAs of kind ii), iii) and iv).

As for a SA0 affecting V_{aux}, it is activated immediately after its occurrence (i.e., it is activated with both CK=0 and CK=1), and it results in the generation of an error message. In fact, such a SA0 produces a logic 0 at the outputs of all inverters, thus resulting in the error indication *(Err1, Err2) = (0,0)*. The proposed circuit is therefore *TSC* with respect to such a fault.

Instead, a SA1 on V_{aux} is never activated, thus it does not result in the generation of any error message. Moreover, due to such a fault, the circuit is not able to indicate an incorrect voltage value on V_{out}. Thus, the implemented

circuit is neither *TSC,* nor *SCD* with respect to it. The occurrence of this fault should be avoided by properly designing the circuit layout [4-19].

B. Transistor Stuck-Open Faults (SOPs)

As for SOPs, they may affect the transistors of: i) MUX1, MUX2; ii) INV11, INV12, INV21 and INV22; iii) M1. As for SOPs of kind i), they may affect: i-a) the pMOS or nMOS of TG2 and TG3, or the nMOS of TG1 and TG4; i-b) the pMOS of TG1 and TG4. The activating conditions of the considered SOPs are summarized in Table 4-IV.

TABLE 4-IV: Activating conditions for the considered SOPs possibly affecting the proposed monitor.

Kind of SOP	Affected transistor	Activating Condition
i-a	nMOS – pMOS of TG2 and nMOS of TG4	CK=0 → CK=1
	nMOS – pMOS of TG3 and nMOS of TG1	CK=1 → CK=0
i-b	pMOS of TG1	CK=1 → CK=0
	pMOS of TG4	CK=0 → CK=1
ii	pMOS of INV11	CK=0 → CK=1
	nMOS of INV11	CK=1 → CK=0
	pMOS of INV21	CK=1 → CK=0
	nMOS of INV21	CK=0 → CK=1
	pMOS of INV12	CK=1 → CK=0
	nMOS of INV12	CK=0 → CK=1
	pMOS of INV22	CK=0 → CK=1
	nMOS of INV22	CK=1 → CK=0
iii	pMOS M1	CK=0 → CK=1 or CK=1 → CK=0

When activated, SOPs of kind i-a) do not result in the generation of an error message. However, in the presence of these SOPs, the circuit continues to detect incorrect voltage values on V_{out}. Moreover, it has been verified that, if such SOPs are followed by other faults in $\mathcal{F}$, the circuit continues to detect incorrect values of V_{out} before the following fault is activated, while it produces an error message after the following fault activation. Therefore, the proposed circuit is SCD with respect to SOPs of kind i-a).

As for SOPs of kind i-b), it has been verified that the correct operation of the developed monitor is not modified before their activation. Instead, their activation results in the generation of an error message, so that the circuit is *TSC* with respect to them. Similar considerations apply to SOPs of kind ii) and iii).

C. Transistor Stuck-On Faults (SONs)

As for SONs, they may affect: i) the transistors of MUX1, MUX2; ii) the pMOS of INV11 and INV21; iii) the nMOS of INV11 and INV21; iv) the nMOS and pMOS of INV12 and INV22; v) transistor M1. As for SONs of kind i), they may affect transistors of: i-a) TG1 or TG4; i-b) TG2 or TG3. The activating conditions of the considered SONs are summarized in Table 4-V.

SONs of kind i-a), even when activated, do not result in the generation of an error message. However, the circuit continues to detect incorrect voltage values on V_{out} even if it is affected by one of these SONs. Moreover, if SONs of this kind are followed by other faults in $\mathcal{F}$, the circuit continues to work properly and produces an error message when the following fault is activated. Therefore, the proposed circuit is *SCD* with respect to SONs of kind i-a).

Moreover, it has been verified that, if another fault in $\mathcal{F}$ occurs, the circuit continues to detect V_{out} incorrect voltage values before the following fault is activated, while it produces an error message after its activation. Therefore, our circuit is *SCD* with respect to SONs of kind iii).

TABLE 4-V: Activating conditions for the considered SONs possibly affecting the developed monitor.

Kind of SON	Affected transistor	Activating Condition
i-a	nMOS - pMOS of TG1	CK=1
	nMOS - pMOS of TG4	CK=0
i-b	nMOS - pMOS of TG2	CK=0
	nMOS - pMOS of TG3	CK=1
ii	pMOS of INV11	CK=0
	pMOS of INV21	CK=1
iii	nMOS of INV11	CK=1
	nMOS of INV21	CK=0
iv	pMOS of INV12	CK=1
	nMOS of INV12	CK=0
	pMOS of INV22	CK=0
	nMOS of INV22	CK=1

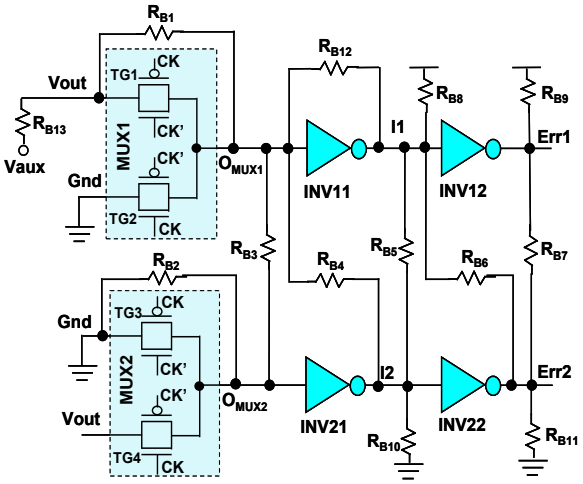
SONs of kind iv) do not alter the correct operation of our monitor before they are activated. When activated, instead, they result in the generation of an intermediate voltage value on *Err1* or *Err2* during one of the *CK* semi-periods. Depending on the logic threshold of the downstream logic, these faults may or may not result in an error indication. In the case of no error message generation, our circuit continues to work properly and, in particular, to detect the presence of incorrect voltage values on V_{out}. Moreover, if SONs of kind iv) are followed by other faults in $\mathcal{F}$, our circuit keeps on working correctly, producing an error message after the following fault is activated. Therefore, our circuit is *TSC* or *SCD* with respect to this kind of SONs.

Finally, as for a SON of kind v), it produces the same effect as the SA1 affecting node V_{aux}, so that the same considerations apply.

D. Bridging Faults (BFs)

All possible BFs affecting the monitoring circuit have been considered, as reported in Fig. 4.9(a). The maximum resistance value for which each BF results in an error message is reported in Fig.4.9 (b), along with the activation conditions. It has been verified that before the activation of the considered BFs, the monitor continues to indicate incorrect voltage values on V_{out}.

As for BFs with R_{max}=6kΩ, when they are activated, an error indication is produced during one of the *CK* semi-periods, so that the circuit is *TSC* with respect to them. Instead, BFs with resistances R_{B1}, R_{B3} and R_{B10} result in an error message for values of R lower than 3.6kΩ, 5.1 kΩ and 0.6kΩ, respectively. However, it has been verified that, for higher values of R, the proposed circuit continues to detect incorrect voltage values on V_{out}. Moreover, if such BFs are followed by other faults in F, the circuit: 1) continues to detect V_{out} incorrect voltage values before the following fault is activated, and 2) produces an error message after the following fault is activated. Therefore, the developed circuit is *SCD* with respect to them.



R_{Bi}	R_{max} (kΩ)	Activating condition
R_{B1}	3.6	CK=1
R_{B2}	6	CK=0
R_{B3}	5.1	CK=0 or 1
R_{B5}	6	CK=0 or 1
R_{B7}	6	CK=0 or 1
R_{B8}	6	CK=0
R_{B9}	6	CK=1
R_{B10}	0.6	CK=0
R_{B11}	6	CK=1
R_{B12}	6	CK=0 or 1

Figure 4.9: Considered BFs, and maximum R value for which they can be detected.

As for R_{B4}, R_{B6}, and R_{B13}, they are never activated, thus they do not result in an error indication. Due to these BFs, the proposed circuit is no longer able to

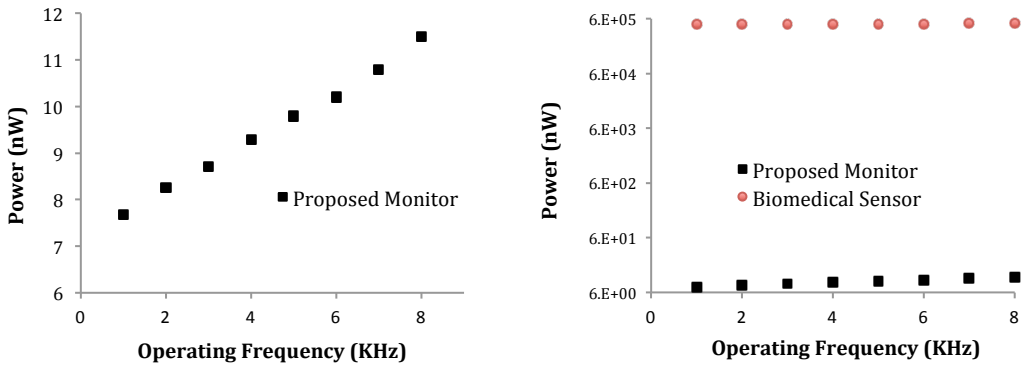
detect incorrect voltage values on V_{out}. Therefore, the occurrence of such faults should be avoided by properly designing the circuit layout [4-19].

To summarize, the proposed monitor satisfies the *TSC,* or the *SCD* property for all faults in F, but for a few faults, whose likelihood should be reduced by means of proper layout design.

4.5 Cost evaluation

An evaluation of the costs of the proposed monitor in terms of power consumption and area overhead has also been performed. As described in Section 4.3, the monitor has been implemented considering the inverters designed as shown in Fig. 4.8, thus allowing the calibration after fabrication of their logic threshold voltage values. The area and power required by the monitor has been compared to those of the considered EHC (Fig. 4.1), implemented as described in Section 4.1.

As for power consumption, it has been found that the power consumed by the proposed monitor increases linearly with its operating frequency (i.e., the frequency of its CK signal in Fig. 4.5), as depicted in Fig. 4.10 (a).



(a) (b)

Figure 4.10: (a) Power consumed by the proposed monitoring circuit as a function of its operating frequency. (b) Power consumed by EHC (squares pattern) and by the monitoring circuit (circle pattern), as a function of the frequency f_{CS} of the control signal V_{cs}.

As for the power consumed by EHC, it increases with the frequency f_{CS} of its control signal V_{CS}. However, as can be observed from Fig. 4.10(b), the power consumed by the monitor is considerably lower than the power consumed by EHC for all frequencies in the considered range (i.e., between 1kHz – 8kHz), which is a realistic range of operating frequencies for EHCs. More in details, Table 4-VI reports the power consumed by the monitor (P_{mon}) and that of EHC (P_{EHC}), as well as the relative power consumption increase required by the monitor over the power consumed by EHC for different values of their operating frequency (i.e. the frequency of the CK signal for our monitor and the frequency f_{CS} of the control signal V_{CS} of the EHC). From Table 4-VI, it is possible to observe that the increase in power consumption required by the developed monitor is negligible for all considered frequencies with respect to that of EHC.

TABLE 4-VI: Power consumed by the proposed monitor (P_{mon}) and by EHC (P_{EHC}), and relative power consumption increase required by the monitor ($\Delta P(\%)=100\cdot(P_{mon}/P_{EHC})$).

Monitor/EHC operating frequency (KHz)	Power consumption		
	EHC (μW)	monitor (nW)	ΔP (%)
1	480	7.68	0.0016
2	490	8.25	0.0016
3	490.8	8.7	0.0017
4	492	9.28	0.0018
5	492.2	9.79	0.0019
6	492.4	10.2	0.0020
7	492.7	10.8	0.0021
8	493	11.5	0.0023

As for area overhead, the proposed monitor requires 41 transistors and a capacitor C1 (Fig 4.9). According to the implementation in Section 4.3.1, the 41 transistors of the circuit require 500 squares, implying an area of approximately 16μm^2 for the considered 0.18μm CMOS technology. Considering that the AC/DC and DC/DC converters of EHC (Fig. 4.1) require 5920 squares and a die size of approximately 189μm^2 in a 0.18μm CMOS technology, it is possible to conclude that the area increase required by the proposed monitor is of approximately the 8.5%. As for the capacitor C1, it may be not integrated using the CMOS 0.18μm technology, because of its relatively large capacitance value (C1=10μF). Thus, the capacitor C1 may be implemented as a discrete capacitor, together with the discrete capacitors (i.e., C_{STOR} and C_{OUT}) and inductor L1 of EHC (Fig. 4.1). As shown in Section 4.2, the two capacitors of EHC are considerably larger than C1 (e.g., $C_{STOR}=180\mu F$ and $C_{OUT}=500\mu F$). As a consequence, the implementation of C1 in such a portion of EHC, which includes also the inductor L1, negligibly impacts its area overhead. Therefore, the developed monitoring circuit implies a very small area increase over the total area of the considered EHC.

4.6 Summary

In this chapter the problem of the concurrent detection of faults possibly affecting an EHC that powers a wearable biomedical sensor has been addressed. A brief description about the EHC analyzed has been shown in the first section. In the next sections, the effects of possible faults affecting the EHC have been analyzed, showing that they may make it fails in producing the required power supply voltage level for the sensor. To address this issue, a new low cost circuit has been developed to monitor continuously and concurrently with normal operation, the power supply voltage given to the output of the EHC. The circuit proposed gives an error indication if the provided power supply voltage falls below the minimum voltage value required by the sensor

to work properly, thus allowing the activation of proper recovery actions, to guarantee the correct powering of the sensor, despite such faults occurrence.

The monitor requires very low costs in terms of power consumption and area overhead. Moreover, it features self-checking ability with respect to its possible internal faults, but for a few faults, whose likelihood can be reduced by means of proper layout design.

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Chapter 5

Model for thermal behavior of shaded solar cells under hot spot condition

As already introduced in the first chapter, in a photovoltaic system, and in particular in a photovoltaic module, there is a failure condition that can lead to energy output losses, due to localized overheating (a phenomenon referred to as hotspot) in a single solar cell inside the module. Overheating can produce a permanent damage of the solar cell area involved, with a consequent drastic reduction of the provided power of the whole module. In order to improve the photovoltaic module reliability, an accurate analysis about phenomena that can cause efficiency degradation must be carried out. In this chapter, the problem of modeling the thermal behavior of photovoltaic (PV) cells is addressed. Due to the combination of their being exposed to shading and localized crystal defects inside themself, PV cells may experience a dramatic temperature increase with consequent reduction of the provided power. In particular, a thermal model is presented, which allows estimating the temperature of the hot-spot area as a function of the time interval during which the PV cell is under hot-spot condition. The rest of this chapter is organized as

follows. In Section 5.1, some preliminary on PV cell and hot-spot heating are given, with an introduction of terminologies and equivalent electrical circuit used to model the solar cell behavior [5-1][5-11]. In Section 5.2, the thermal model to estimate the temperature of a PV cell under hot-spot condition is presented and validated against experimental data. In Section 5.3, the thermal behavior of shaded PV cells undergoing hot-spot conditions obtained by applying the developed model is shown and a comparison between partial shading over full shading effects is proposed.

5.1 Preliminaries on a PV cell and PV cell hot spot heating

A photovoltaic solar cell can be modeled considering the simple electrical circuit as shown in Fig. 5.1 [5-10][5-11]:

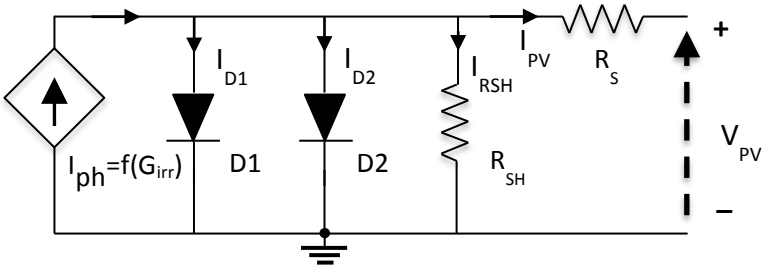


Figure 5.1: Two diode equivalent lumped model of a solar cell

When the PV cell is exposed to sunlight, it generates a photocurrent I_{ph} that is proportional to the solar irradiation G_{irr} [W/m^2] as indicated in Fig. 5.1[5-8, 5-10, 5-11]. The output current I_{PV} provided by the PV cell is:

$$I_{PV} = I_{ph} - I_{D1} - I_{D2} - I_{RSH} \quad (5.1).$$

The diodes D1 and D2 account for the saturation mechanisms in the PV cell. Particularly, the currents I_{D1} and I_{D2} are the saturation currents due to diffusion mechanism and the recombination in the space charge layer; they are given by:

$$I_{D1} = I_{01} \cdot [\exp(V_{PV} + I_{PV}R_s)/n_1 V_T - 1] \quad (5.2).$$

$$I_{D2} = I_{02} \cdot [\exp(V_{PV} + I_{PV}R_s)/n_2 V_T - 1] \quad (5.3).$$

where V_T is the thermal potential [5-1, 5-8], and n_1, n_2 the ideality factors . The current I_{RSH} represents the leakage current of the PV cell, which is accounted by a shunt resistor R_{sh} [5-2, 5-8]. The resistor R_S models the voltage drop across the PV cell produced by the current I_{PV} [5-8]. Additionally, the function $f(G_{irr})$ that provide the photocurrent I_{ph} is given by: $(J_{ph} \cdot A_{cell} \cdot G_{irr})/1000$ where G_{irr} is the value of the irradiance in W/m^2, A_{cell} is the area of the PV cell and the photocurrent density J_{ph} is given considering the standard conditions ($1000 W/m^2$, T_{cell}= 25C°) under which measurements are usually performed. Equation 5.1 can be used to show graphically the current-voltage dependence both in dark and under illumination condition.

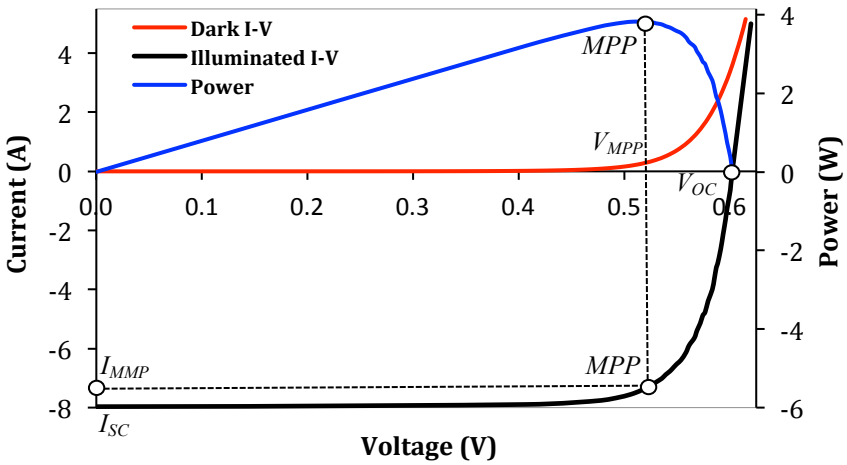


Figure 5.2: Dark and illuminated I-V, power curve, and basic solar cell parameters.

Fig. 5.2 shows the I-V curves of a solar cell in dark (red line) and illuminated (black line) conditions. Considering the curve I-V under illuminated condition, the voltage at which the current is equal to zero is called open circuit voltage (V_{OC}) while the current at which the voltage is zero is called short circuit current (I_{SC}). The blue line represents the generated power $P(V) = VI$. The

voltage at which the power has a maximum is called maximum power voltage (V_{MP}), and the corresponding current is called maximum power current (I_{MP}). The point corresponding (V_{MP}, I_{MP}) is called maximum power point (MPP) and it indicates the maximum power generated by the solar cell under illuminated condition. Two primary parameters about the solar cell are its efficency (η) and fill factor (FF). The fill factor FF is defined as:

$$FF\ (\%) = (V_{MP} * I_{MP})/(V_{OC} * I_{SC})\ \text{x}100\% \qquad (5.4).$$

Efficiency η is defined as:

$$\eta\ (\%) = ((V_{MP} * I_{MP})/P_{IN})\ \text{x}100\% = (FF * V_{OC} * I_{SC})/(P_{IN})\ \text{x}100\% \qquad (5.5).$$

where P_{IN} is the standard normally incident solar power [5-2].

The introduced model is able to describe the electrical behavior of the solar cell when it is forward biased and under different illumination conditions. However, when the cell is reverse biased and in particular, it works near the breakdown region, its behavior can be better modeled by adding to the model in fig. 5.1 a second current generator (I_{BR}), connected in series to the shunt resistance, whose produced current is controlled by the output voltage V_{pv} [5-2]. The schematic is shown in Fig.5.3

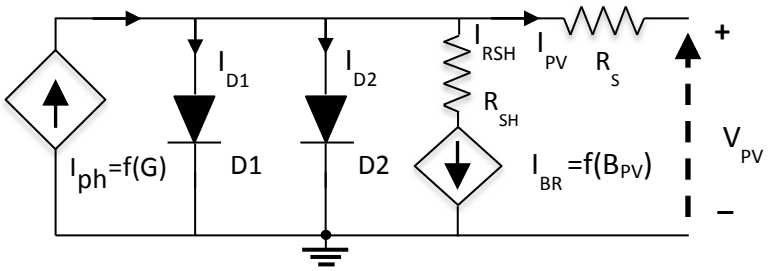


Figure 5.3: Two diode modified equivalent lumped model of a solar cell [5-2].

The current I_{br} is approximately equal to 0A for values of V_{pv} higher than the cell breakdown voltage (V_{br}). Instead, it is $I_{br} \cong \alpha \cdot V_{pv} \cdot (1-(V_{pv} / V_{br}))^{-m}$, for values of V_{PV} lower than V_{br} [5-2]. The parameters α and m are fitting parameters.

Fig. 5.4 shows the current I_{PV} as a function of V_{PV}, for a PV cell modeled with the circuit shown in Fig. 5.3, considering a solar irradiation $G_{irr}=500W/m^2$. The photocurrent generated is I_{ph} =4A, and three different values of the shunt resistance R_{sh} have been considered. It can be noticed that, when V_{pv} = 0V (i.e., the outputs of the PV cell are shorted), the current I_{PV} is equal to the photocurrent I_{ph} = 4A. This because, when V_{PV} = 0V, no current flows trough R_{sh} (I_{RSH}=0), and D1 and D2 are off ($I_{D1}=I_{D2}=0$). Additionally, it can be observed that also when $0 < V_{pv} < 0.5V$, it is $I_{PV} \approx I_{ph}$, since D1 and D2 are still off and I_{RSH} is very small. Instead, for $V_{PV} > 0.5V$, the current $I_{PV} = I_{ph}-I_{D1}-I_{D2}-I_{RSH}$ starts decreasing quickly as V_{PV} increases, since D1 and D2 become conductive, and I_{D1} and I_{D2} increase quickly as V_{PV} increases. From Fig. 5.4, it is possible also to observe that, when the PV cell is reverse biased ($V_{pv}<0$), the current I_{PV} increases as V_{PV} decreases. Moreover, the value of I_{PV} strongly depends on the value of the shunt resistance R_{sh}. In particular, I_{PV} increases faster when the value of R_{SH} decreases.

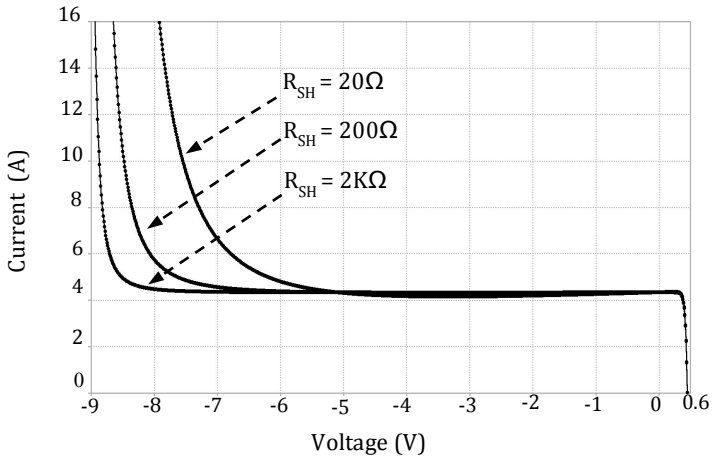


Figure 5.4: Solar cell current I_{PV} as a function of V_{PV} for a PV cell modeled with the circuit in Fig. 5.3 for the case of an irradiation $G_{irr}=500W/m^2$ producing an I_{PV}=4A and for three different values of the shunt resistance R_{SH}.

It is worth noticing that, when the PV cell is forward biased, V_{PV} is lower than 0.6V. Therefore, even for high values of I_{PV}, the power dissipated by the PV cell due to the shunt resistance R_{sh} ($P_{diss}= V_{pv}^2/R_{sh}$) is small [5-2]. Instead,

when the PV cell is reverse biased, the absolute value of V_{PV} can be as high as 10 V (depending on the PV cell breakdown voltage), so that the power dissipated by the PV cell can be very high [5-2], and the temperature of the PV cell can considerably increase.

Generally, when the PV cell is reverse biased, I_{PV} is non-homogeneously distributed throughout the cell area, and tends to concentrate in small regions (with an area or different areas approximately equal to $100\mu m^2$) of slightly higher conductivity, where the silicon presents a higher concentration of defects/impurities. These impurities create a filament-type shunt along grain boundaries that connect directly the back contact metal with the front, bypassing the p-n junction of the PV cell. Often the shunts are not random but occur preferably at the cell cusps and grain-boundary corners along cell edges due to physical chipping from the scribing procedure [5-18]. This physical phenomenon is taken into account in the value of shunt resistance R_{sh} in Fig. 5.2 and 5.3 [5-6, 5-18]. A low value of R_{sh} will originate a large value of I_{PV} when the cell is reverse biased, which in turn will produce high power dissipation on R_{sh}. If such a power dissipation is high enough, it will produce a considerable increase in the temperature of the regions of the PV cell that are close to the impurity centers, thus giving rise to hot-spot heating [5-6, 5-12]. Under hot-spot heating, the temperature of the heated regions can exceed the maximum value tolerated by the PV cell, with a possible consequent permanent damage to the cell [5-2]. From the above considerations, it is clear that, to enter a hot-spot condition, a PV cell must operate in its reverse bias region. This is likely to occur in typical PV arrays, where many PV cells are connected in series to obtain an adequate level of DC voltage [5-19]. In fact, if a PV cell within the series is (partially) shaded, it reduces its current and forces the current of the serially connected PV cells to diminish too [5-6]. However, the other cells of the series, which are fully irradiated, tend to produce a higher current than that imposed by the shaded cell. This condition forces the shaded cell to enter the reverse biased region [5-6], thus possibly giving rise to hot-spot. It must be pointed out that a solar cell with local shunt has also a negative

behavior in term of electrical performance, when it is biased in the forward region. In this last case the impact is not on the temperature that reaches locally until no critical values, but in term of fill factor and solar cell efficiency. In the next chapter, it will be shown how hot-spot regions in a solar cell due to local shunts, results in a degradation of the fill factor and thus of the overall power conversion efficiency.

5.2 Thermal model description and validation

As described in the previous section, when one PV cell within a series of PV cells is shaded, it starts operating in the reverse region, with the reverse current flowing mainly through small regions containing impurities [5-6]. The power generated by the reverse current of the cell is therefore dissipated in an area close to these impurity centers, which consequently undergoes a hot-spot condition.

In order to introduce the thermal model developed to analyze a hot-spot condition, it is important to give a brief description of the whole solar cell structure, when it is encapsulated in a PV module.

In practical, solar cells are encapsulated into a “sandwich” structure that typically consists of glass -ethylene vinyl acetate (EVA) - antireflection coating (ARC) - Silicon - Tedlar, as shown in Fig. 5.5 [5-20].

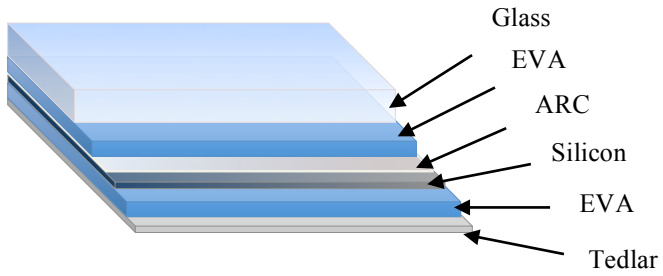


Figure 5.5: Cross-section of an encapsulated silicon solar cell (glass-EVA-ARC - Silicon-Tedlar) [5-20].

The sizes and the thermal properties of each layer in the encapsulated cell can differ case-by-case considering different photovoltaic technologies.

However, for a standard silicon solar cell, typical values are reported in Table 5-I [5-20].

TABLE 5-I: Size and thermal properties of each layer in an encapsulated silicon solar cell.

Layer	Thickness (mm)	Thermal Conductivity ($W/m^2/K$)
Glass	3	*0.98*
EVA	0.5	*0.23*
ARC	$0.6 \cdot 10^{-3}$	*1.38*
Silicon	0.18	*148*
Tedlar	0.1	*0.36*

Analyzing the sizes and the properties present in table 5-I it can be derived that, due to its highest thickness and low thermal conductivity, the glass is the main thermal resistive layer in the encapsulated solar cell. So the dissipated heat of the solar cell strongly depends on this layer. Therefore, for the performed thermal analysis, glass layer has only been considered in order to determine each parameter of the developed model shown in Fig.5.6a. The developed thermal model consists of two series thermal *RC* circuits. The lower *RC* circuit (composed by C_{THcell} and R_{THcell}) accounts for the temporal behavior of the PV cell temperature as a function of solar irradiation (T_{cell} in Fig. 5.6a) only. Instead, the upper thermal *RC* circuit (composed by $C_{TH\text{-}HS}$ and $R_{TH\text{-}HS}$) models the temporal behavior of the PV cell portion under hot-spot condition (area A_{HS}) as a function of the power dissipated (P_{diss}) on the shunt resistor R_{sh}. Particularly, P_{diss} has been estimated by Spice simulations as the power dissipated on the shunt resistance, that is: $P_{diss} = R_{SH} \cdot I_{SH}^2$ [W/m^2], where I_{SH} is the reverse bias current of the shaded PV cell.

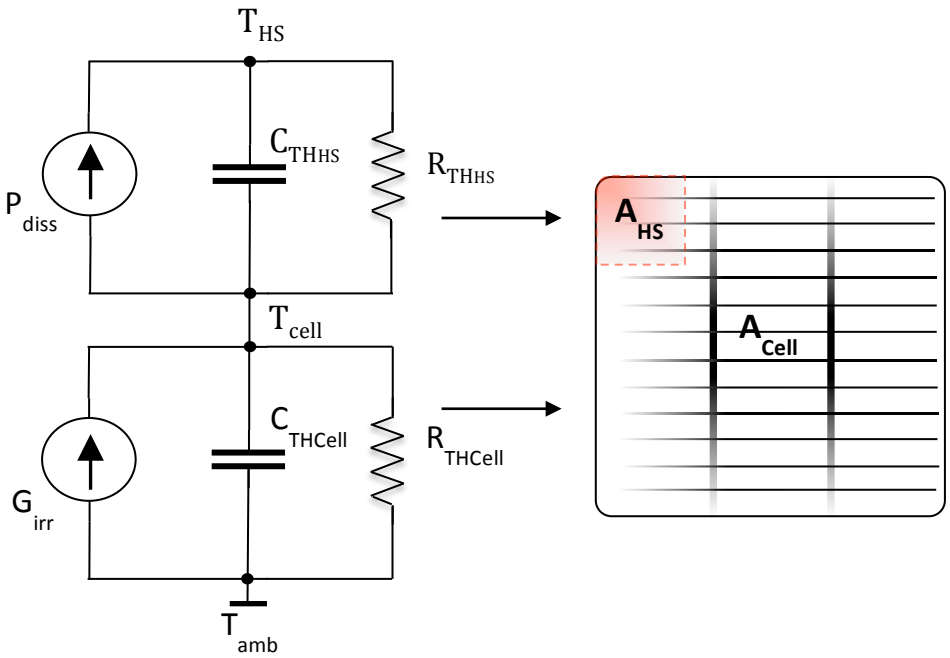


Figure 5.6: (a) Equivalent thermal model proposed to estimate the time dependence of the temperature of the portion of PV cell (A_{HS}) under hot-spot condition. (b) Schematic representation of a shaded PV cell considered here to build the model.

Fig. 5.6(b) shows a representation of the shaded PV cell that has been considered to develop the thermal model proposed. A_{Cell} denotes the area of the PV cell surface, while the area of the regions affected by hot-spot heating is denoted by A_{HS}. The value of A_{HS} depends on the PV cell fabrication process, and it has been experimentally determined to be in the range of 5%-10% of A_{Cell} [5-14]. As for the other parameters in Fig. 5.6(a), T_{HS} [˚C], R_{THHS} [˚C·m^2/W] and C_{THHS} [˚C· m^2·sec/W] are the temperature, thermal resistance and thermal capacitance, respectively, of the PV cell portion A_{HS}; T_{cell} [˚C], R_{THCell} [˚C·m^2/W] and C_{THCell} [˚C· m^2·sec/W] are the temperature, thermal resistance and thermal capacitance, respectively, of the remaining portion of the shaded PV cell that is not undergoing in a hot-spot condition; T_{amb} [˚C] is the ambient temperature; G_{irr} [W/m^2] is the solar radiation density illuminating

the PV cell. The values of the parameters R_{THHS}, R_{THCell}, C_{THHS} and C_{THCell} have been calculated as follows:

$$R_{THCell} = \frac{l}{K * A_{Cell}}; \qquad C_{THCell} = A_{Cell} * l * \rho * \varsigma \tag{5.6}$$

$$R_{THHS} = \frac{l}{K * A_{HS}}; \qquad C_{THHS} = A_{HS} * l * \rho * \varsigma \tag{5.7}$$

where l [m] is the thickness of the glass covering the PV cell; k is the glass thermal conductivity; ρ [Kg/m^3] is the glass density; ς [J/Kg·°C] is the glass specific heat capacity. From the thermal circuit in Fig. 5.6(a), it is possible to derive the behavior over time of the temperature T_{HS} in the area of the PV cell undergoing a hot-sport condition (at time t_{HS}) as follows:

$$T_{HS}(t) = \begin{cases} T_A + R_{THcell} G_{irr} & t < t_{HS} \quad (5.8) \\ T_A + R_{THcell} G_{irr} \left(\gamma + (1-\gamma) e^{-\left(\frac{t-t_{HS}}{R_{THcell} C_{THcell}}\right)} \right) + P_{diss} R_{TH-HS} \left(1 - e^{-\left(\frac{t-t_{HS}}{R_{TH-HS} C_{TH-HS}}\right)} \right) & t \geq t_{HS} \quad (5.9) \end{cases}$$

where $\gamma = G_{irr\text{-}shaded}/G_{irr}$ denotes the relative mismatch in the irradiation between the shaded ($G_{irr\text{-}shaded}$) and the non shaded (G_{irr}) cells of the PV array. Thus, a fully shaded PV cell will present a $\gamma = 0$, while for non-shaded PV cells it is $\gamma = 1$. From equations (5.8) and (5.9), it is possible to observe that, before entering a hot-spot condition (for $t < t_{HS}$), the temperature of the whole PV cell is constant and given by $T_{HS} = T_{cell} = T_A + R_{THcell} \cdot G_{irr}$. In this condition, in fact, the PV cell works with the same solar irradiation G_{irr} as the other PV cells in the panel, so that the PV cell is forward biased. Therefore, it is $P_{diss} \approx 0$, and the cell temperature turns out to depend only on the solar irradiation. On the other hand, after the PV cell is shaded (with an irradiation mismatch γ) and enters a hot-spot condition (for $t \geq t_{HS}$), there are two different phenomena determining the temperature of the PV cell: i) the contribution of the reduced solar irradiation (i.e., second term in (5.9) for $t \geq t_{HS}$), which tends to reduce the PV cell temperature with a time constant $\tau_{cell} = R_{TH\text{-}cell} \cdot C_{TH\text{-}cell} = l \cdot \rho \cdot \varsigma / k$ [sec]; ii) the contribution of the power dissipated by R_{sh} (P_{diss}) (i.e., third term in (5.9)

for $t \geq t_{HS}$), which tends to increase the PV cell temperature with a time constant $\tau_{HS} = R_{TH\text{-}HS} \cdot C_{TH\text{-}HS} = l \cdot \rho \cdot \varsigma / k$ [sec]. It is worth noticing that $\tau_{cell} = \tau_{HS}$; they depend only on the glass thickness (l), thermal conductivity (k), density (ρ) and specific heat capacity (ς), while they do not depend on the surface areas A_{cell} and A_{HS}. It is also interesting to note that, since it is $A_{cell} >> A_{HS}$, in (5.6) and (5.7) it is $R_{THcell} << R_{HT\text{-}HS}$. Thus, $G_{irr} \cdot R_{THcell} << P_{diss} \cdot R_{TH\text{-}HS}$ in (5.9). Therefore, even if $\tau_{cell} = \tau_{HS}$, the contribution of ii) to the temperature T_{HS} is considerably higher than the contribution of i). As a result, when a PV cell is shaded, its temperature T_{HS} tends to increase very quickly, as it will be shown in the next section. Additionally, for $0 < \gamma < 1$ (partial shaded cell), T_{HS} grows faster than for $\gamma = 0$ (fully shaded cell). From a physical point of view, this is due to the fact that, in the partial shaded cell, the operating temperature is higher than in the fully shaded cell, since part of the cell is still being fully irradiated.

The proposed thermal model can be simulated by means of any electrical simulation tool Spice-like. To fulfill this purpose, it is only needed to convert the units of the obtained voltages (currents) to units of temperature (power), so that, 1V (1A) in the simulated electrical circuit will correspond to 1˚C (1W) in the actual thermal circuit.

The proposed model allows to evaluate simply and quickly the maximum time interval in which a PV cell can remain under a hot-spot condition, without suffering from permanent damages due to excessive temperature. Such an evaluation is a preliminary step towards the development of shading tolerant techniques that, if activated in the field, could avoid PV cell damage in case of shading, thus avoiding the consequent efficiency loss of the whole PV array. The model has been validated by comparing its provided results against the experimental ones reported in [5-16, 5-17], considering the same operating conditions. Fig. 5.7 shows the temperature behavior of a shaded cell obtained by the thermal model.

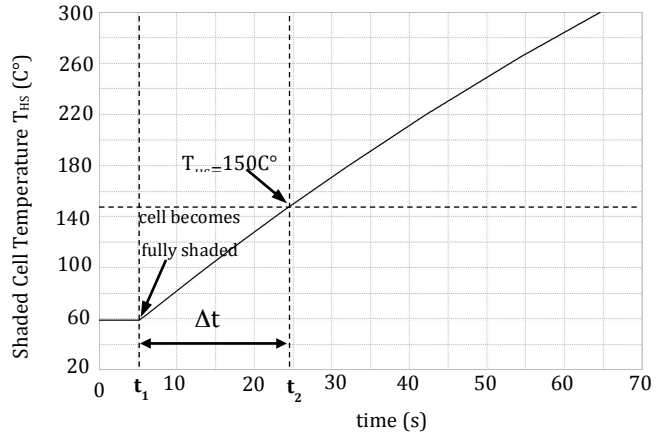


Figure 5.7: Temperature trend over time in solar cell, when it is fully shaded after t1 and for the operation conditions reported in [5-5].

As can be seen, before the cell is shaded at time t_1, it presents a constant operating temperature of 60˚C. This is in very good agreement with the operating temperature of a non-shaded PV cell reported in [5-16]. After the cell is shaded (at time t_1), the model estimates a time interval $\Delta t = t_1 - t_2 = 21.2s$ to rise by 90˚C, thus reaching a temperature of 150˚C. This result is in accordance with the experimental results reported in [5-17].

5.3 Solar Cell thermal behavior derived from the model

In this section, the results obtained when the model is applied to estimate the behavior of the temperature T_{HS} of a shaded PV cell undergoing a hot-spot condition are presented. As an example, a realistic PV array scheme has been considered and depicted in Fig. 5.8 [5-2]. It is composed by a series of 36 identical PV cells (PVi, *i=1..36*), with 2 bypass diodes (D_{BYPi}, *i=1, 2*), each connected in parallel to 18 PV cells [5-2]. It must be pointed out that the bypass diodes are used to counteract the detrimental effect of shading. The

adoption of bypass diodes connected in antiparallel with the solar cells has been proposed in [5-2, 5-4], and nowadays is a standard de facto. Particularly, bypass diodes limit the reverse voltage that can be applied to a PV cell, thus preventing it from reaching the breakdown voltage when it is shaded. Unfortunately, hot-spot condition on shaded PV cells can still arise, even if bypass diodes are employed within PV arrays [5-3]. This because, as previously described, some PV cells exhibit a large reverse current, even before reaching the reverse breakdown voltage and a dangerous hot-spot condition can still happen. For this analysis, it has been assumed that the cell PV36 has a localized low value of its shunt resistance and is either almost fully shaded ($\gamma = 0.01$), or partially shaded ($\gamma = 0.3$). Of course, similar results would have been obtained considering another PV cell in the array. The bypass diodes (D_{BYPi}, $i=1, 2$) avoid that a shaded PV cell, which is reverse biased, can enter its breakdown region. In fact, the reverse voltage of a shaded PV cell within the array in Fig. 5.8, equal to the sum of the forward voltages of the other 17 non shaded PV cells sharing the same bypass diode, is always lower than its breakdown voltage V_{br} (typically equal to -10V considering each solar cell working around its V_{OC}).

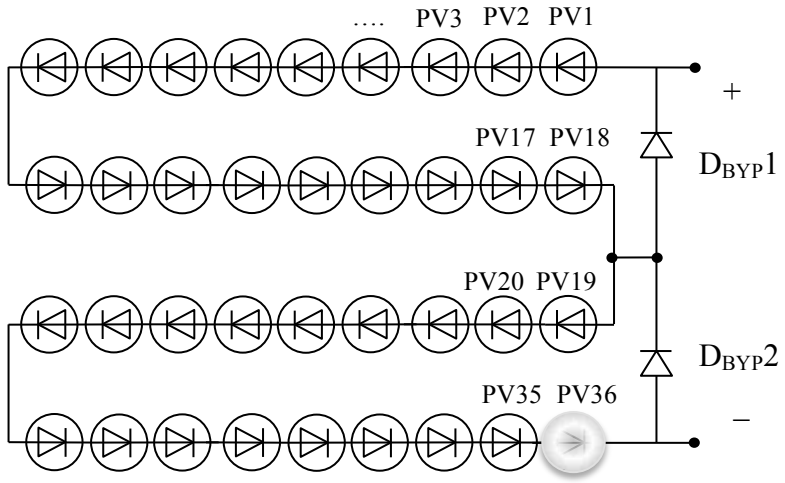


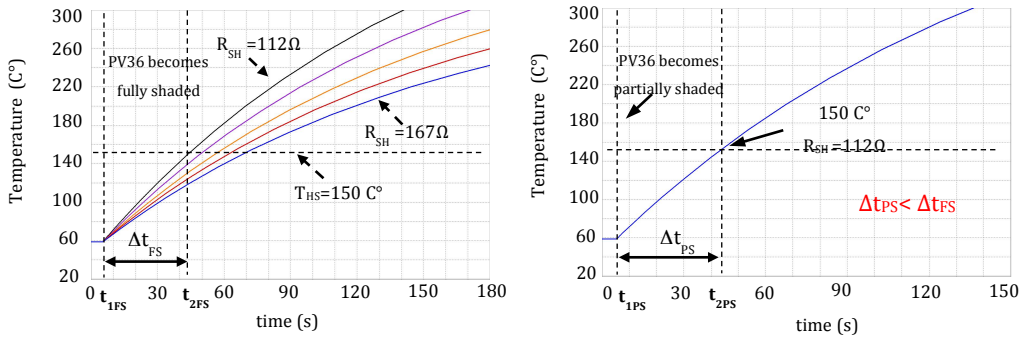
Figure 5.8: PV array scheme considered and used to analyze (by means of the proposed model) the temperature behavior in time of a shaded PV cell (PV36) undergoing a hot-spot condition.

The PV cells of the array have been modeled with the two diode lumped electrical model reported in Fig.5.3, considering the following values of the parameters [5-15]: V_{br} = -10V; α=1.93; m =1.10, R_{sh} =139.6Ω, R_S = 10mΩ. Additionally, it has been considered a typical cell area A_{cell} = 243 cm^2, with a A_{HS} = 14cm^2 (i.e., approximately 6% of A_{cell}). Then, from the equations in (5.6) (5.7) it is: R_{THcell} = 1.4°C/W; $R_{TH\text{-}HS}$ = 14°C/W; C_{THcell} = 65.5 W·s/°C; $C_{TH\text{-}HS}$ = 6.5 W·s/°C.

As a first step, by means of Spice electrical simulations, the power dissipation on the shunt resistance R_{sh} of the shaded PV cell (i.e., PV36) has been estimated for the two considered cases: 1) PV36 is almost fully shaded (γ *=0.01*); 2) PV36 is partially shaded (γ *=0.3*). The values obtained of dissipated power have then been employed in the thermal model (shown in Fig. 5.6(a) and eq.(5.9)) to evaluate the temperature T_{HS} of the shaded cell PV36, as a function of time. In particular, the model has been used to evaluate the time required by the temperature T_{HS} of PV36 to reach *150°C* (hereafter denoted by T_{150}) from the beginning of the partial/full shading. In fact, T_{150} is the minimum value of temperature that can cause permanent damage to the PV cell, in case of hot-spot heating [5-5]. Fig. 5.9(a) shows the results obtained in case of full shading (γ=0.01) of PV36, and for various values of its shunt resistance R_{sh}. Particularly, five different values of R_{sh} have been considered, with a ±20% variation with respect to its nominal value. In fact, as stated in Sect. 5.2, the shunt resistance may considerably vary for different impurity concentration and distribution within a PV cell [5-6, 5-12].

The initial irradiation is uniform for the whole array at the maximum value G_{irr}=1000W/m^2, and the produced temperature is T_{HS} = 60°C on all array cells. At instant t_{1FS}, the cell PV36 is completely shaded (G_{irr}=10W/m^2), while the other cells keep on being fully irradiated (thus obtaining γ=0.01). As can be seen, the time interval Δt_{FS} required by T_{HS} to reach the critical temperature T_{150} (at time t_{2FS}) strongly depends on the value of R_{sh}. In the worst case (represented by the lowest value of R_{SH} = 112Ω), it is: $\Delta t_{FS} = t_{2FS} - t_{1FS}$ = 40s.

For larger values of R_{SH}, Δt_{FS} decreases, being approximately Δt_{FS} = 65s for the highest value of R_{SH} = 167Ω. Similarly, Fig. 5.9(b) depicts the trend over time of the T_{HS} of PV36 when, starting from the time instant t_{1PS}, it is partially shaded (with G_{irr}=300W/m^2, thus γ=0.3), for R_{sh} = 112Ω (i.e., R_{sh} fixed at the lowest value considered in Fig. 5.9(a)). It is worth noticing that the temperature of the partially shaded cell PV36 increases faster than that of the fully shaded cell shown in Fig. 5.9(a). Particularly, it is T_{HS} reaches T_{150} after a time interval equal to Δt_{PS}= t_{2PS}−t_{1PS} =36s < Δt_{FS}. This counterintuitive behavior highlighted by the distributed model can be explained from a physical point of view by considering that, in the partially shaded cell, the full irradiation of part of the cell shortens the time needed to enter the hot-spot condition.



(a) (b)

Figure 5.9: Results obtained with the model for the temperature T_{HS} behavior of PV36 when: (a) PV36 becomes fully shaded after t_{1a} (γ=0.01) and for various values of R_{SH}; b) PV36 becomes partially shaded after t_{1b} (with γ=0.3) and with the lowest value of R_{SH} =112Ω (worst case from the cell temperature point of view).

Instead, Fig. 5.10(a) illustrates the results showing the temperature behavior over time of PV36 when it is fully shaded (with γ=0.01), and for several values of its reverse voltage. In fact, as shown in [5-10], the open circuit voltage of an irradiated cell can slightly vary as a function of the operating temperature, which depends on the ambient temperature and solar irradiation. Therefore, in

the considered case, the V_{PV} of the shaded cell turns out to vary slightly with temperature in the range -9.6V ÷ -9.1V. The shunt resistance R_{sh} has been assumed equal to its considered nominal values (R_{sh} =139.6Ω). As can be seen, the time interval $\Delta t_{FS} = t_{2FS} - t_{1FS}$ required to enter a hot-spot condition ($T_{HS} \geq T_{150}$) diminishes with the increase of the cell reverse voltage. In the considered worst-case scenario (lowest Δt_{FS}), which corresponds to V_{PV} = -9.6V, it is Δt_{FS} = 51s. Instead, for V_{pv} = -9.1V, T_{HS} does not reach T_{150} within the considered simulation time interval of 150s, at which it reaches 112°C. Similarly, Fig. 5.10(b) reports the trend over time obtained for the T_{HS} of PV36, when it is partially shaded after t_{1PS} (with G_{irr}=300W/m^2, thus γ=0.3), and for V_{pv} fixed at the lowest value of the considered reverse voltages (i.e., V_{PV} = -9.6V). As can be seen, the same behavior as in Fig. 5.9(b) has been obtained, but for $\Delta t_{PS} = t_{2PS} - t_{1PS}$ = 48s < Δt_{FS}, thus confirming that the T_{HS} of a partially shaded PV cell rises faster than that of a fully shaded cell.

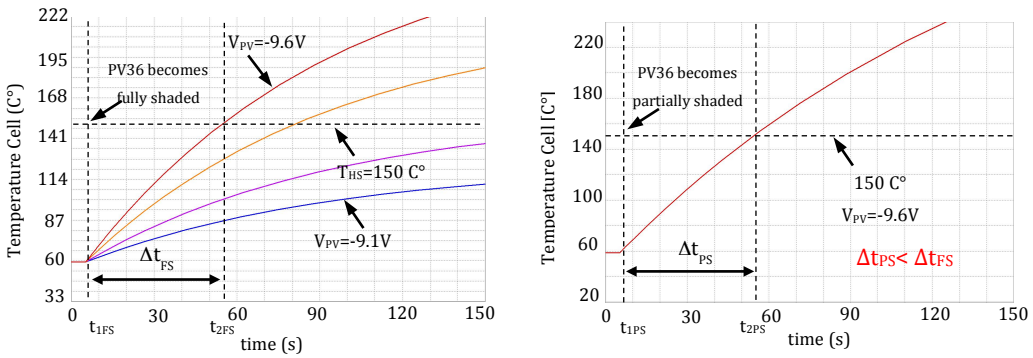


Figure 5.10: Results obtained with the thermal model for the temperature behavior of PV36 when: (a) PV36 becomes fully shaded after t_{1c} (γ=0.01) and for different values of its reverse voltage (V_{pv} varying from -9.1 to -9.6V); (b) PV36 becomes partially shaded after t_{1d} (γ=0.3) and with the lowest of the considered reverse voltages in Fig. 5.10(a) (worst case from the temperature point of view).

From the analysis shown in this section, it can be derived that the presence of localized defects inside the solar cell, generating a low shunt resistance in

terms of equivalent component, is the main factors contributing to the generation of a local overheating when the cell is under hot-spot condition. Moreover, it has been shown that, PV cells affected by defects can reach the temperature until a critical value very quickly, if the voltage applied is closest to its breakdown voltage. Finally, the described thermal model has highlighted that, differently from what may be expected, a partially shaded PV cell enters the hot-spot condition faster than a fully shaded PV cell, thus providing useful hints to PV array design.

5.4 Summary

In this chapter a model for the thermal behavior of a silicon solar cell under hot-spot condition has been introduced and validated. Some preliminary concept about a solar cell has been given in the first section, with the description of the electrical behavior of the cell and the discussion about the considered equivalent electrical model and hot-spot condition in a silicon solar cell. The developed thermal model has been presented and validated in Section 5.2, and a case study using the model has been analyzed in Section 5.3. Simulation results have shown that cells with low shunt resistance can be affected by local overheating when they are shaded thus reverse biased. The thermal model has highlighted that a partially shaded PV cell enters the hot-spot condition faster than a fully shaded PV cell. The results obtained, are in accordance with the experimental data shown in [5-16, 5-17].

By this work, it was born the interest to analyze the behavior of a PV cell with local shunt when forward biased. A possible solution to model a PV cell in a spatially distribution which could simulate the whole its structure was the goal. Must be pointed out in fact, that for the analysis shown in this chapter a lumped electrical model has been considered and a lumped thermal model has been presented accounting for the only behavior of the solar cell when reverse biased. In the next chapter a distributed electrical model able to account for the

non-uniformity in the solar cell will be shown and presented, in order to analyze the impact of the local shunting on the solar cell performance also when forward biased.

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Chapter 6

A distributed electrical network to model a silicon solar cell

In this chapter, the development of a three dimensional 3-D electrical network for modelling double side silicon solar cell is presented. The developed tool is based on a network of repetitive elementary units each one modeled by a two-diode electrical circuit and allows accounting for transport through the emitter, the fingers and the busbars. Moreover the tool is able to account for the non-uniformity in the solar cell. Partial shaded condition can be also simulated. In the section 6.1 a description about the type of elementary units of the distributed model is given. The method to extract the parameters in order to fit and sizing each electrical component of the network is shown in the section 6.2. Simulation results obtained by the tool and compared with experimental date are exposed in the section 6.3 in order to demonstrate the correct calibration of the model and the capability of the tool to characterize the electrical behavior of a double side solar cell. Finally in section 6.4, as case of study, hot-spot regions due to localized crystal defects inside the cell are modeled with the distributed electrical network in order to analyze the impact of the local shunting on the solar cell performance.

6.1 Description of distributed electrical network

The model developed represents a solar cell by means of a resistive network, which connect 2-diode equivalent circuits that represent its elementary units depending on their geometry and position in the solar cell (illuminated area or metallized area). The description about the 2-diode equivalent lumped model has been already shown in the previous chapter 5, so in this section will be reported just the description of the distributed model. In Fig. 6.1a and Fig. 6.1b are illustrated two types of elementary units. They allow modeling the solar cell properties under the metalized regions and under the non-metalized regions respectively.

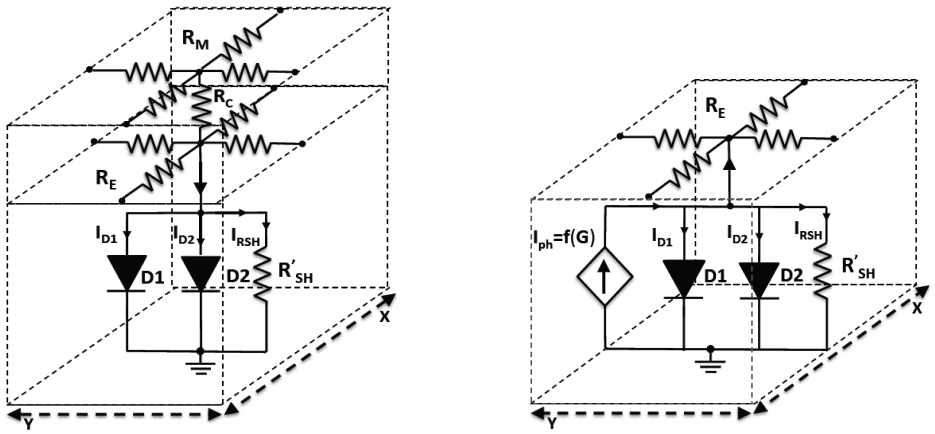


Figure 6.1: Elementary units implemented in the distributed electrical network. They are based on the 2-diode model. The elementary unit (a) is suitable to model the area under the fingers and the busbars. The elementary unit (b) allows modeling the area under non-metalized regions.

Both elementary units are composed by distributed resistances (R_E) to account for the transport through the emitter region, and by two diodes that, as explained in the section 5.1, describe the recombination currents of the *pn* junction. The shunt resistance R'_{SH} (obtained as the specific shunt resistance r_{sh} divided by the elementary unit area) is placed in parallel to the two diodes. In particularly, the currents I_{D1} and I_{D2} are given by:

$$I_{D1}(x,y) = A(x,y) \cdot J_{01} \cdot [\exp(V(x,y)/\eta_1 V_T - 1], \quad (6.1)$$

$$I_{D2}(x,y) = A(x,y) \cdot J_{02} \cdot [\exp(V(x,y)/\eta_2 V_T - 1], \quad (6.2)$$

where in this case A(x,y) is the area of the elementary unit. An ideal current source is implemented in order to account for the photogenerated current (I_{ph}), which is supposed to be proportional to the solar irradiation G [W/m^2]. The contact resistances of fingers and the busbars are modeled with the resistor R_C, while R_M represents the resistance due to the conduction through the metal structures (i.e. fingers and busbars). It is possible to understand that the above descripted electrical parameters, are almost the same as shown in the section 5.1 of the previous chapter except for the series resistance and for the dependence of each parameter of the position (X,Y) and area inside the solar cell. In table 6-I are summarized the resistances definition for the elementary units of the 3-D distributed model described.

TABLE 6-I: Resistance definition for the elementary units of the 3-D distributed model

Metal Resistance	$R_M = (r_{Msheet}) \cdot \frac{X/2}{Y/2} (\Omega)$ or $R_M = (r_{Msheet}) \cdot \frac{Y/2}{X/2} (\Omega)$ where r_{Msheet} is the metal sheet resistance
Emitter Lateral Resistance	$R_E = (r_{Esheet}) \cdot \frac{X/2}{Y/2} (\Omega)$ or $R_E = (r_{Esheet}) \cdot \frac{Y/2}{X/2} (\Omega)$ where r_{Esheet} is the emitter sheet resistance
Contact Resistance	$R_C = \rho_c / X \cdot Y (\Omega)$ where ρ_c is the specific contact resistance ($\Omega \cdot cm^2$)

It is worth noting that the elementary units are slightly modified on along the perimeter regions in order to account for the boundaries of the cell. Finally, the whole solar cell can be modeled by opportunely interconnecting the elementary units. The developed distributed network can be used to model the behavior of solar cell in both dark and illuminated conditions. In particularly, the dark analysis can be easily performed by forcing $I_{ph} = 0$. The figure 6.2 shows

how the complete solar cell can be modeled by connecting the different elementary units. The resulting circuit consists of thousands and thousands elementary units which have to be solved by a circuit simulator like Spice. In this thesis ELDO from MENTOR [6-17] was used.

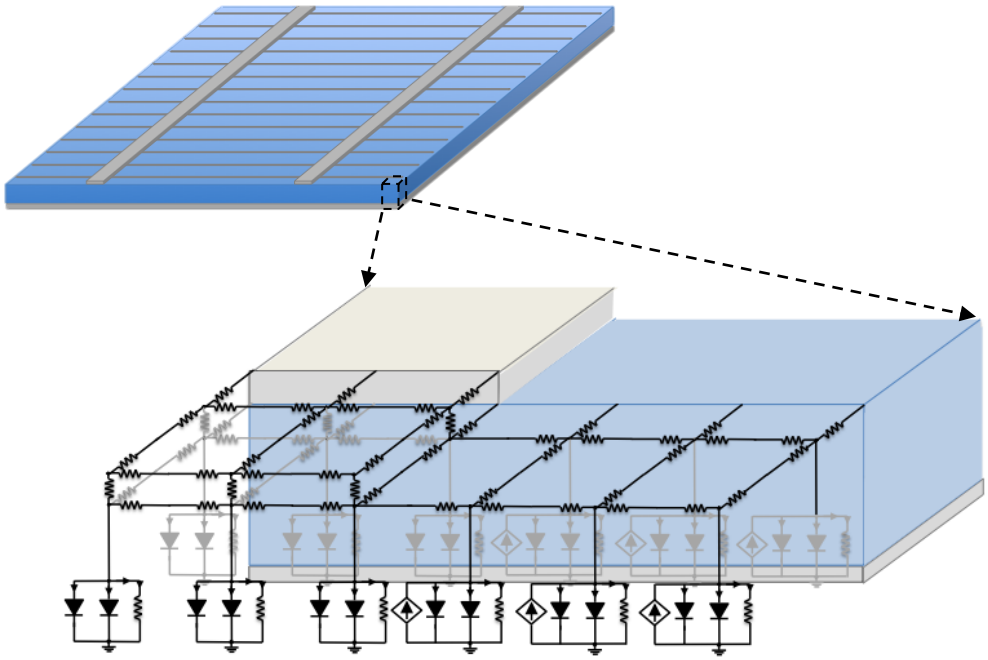


Figure 6.2: Distributed network model of a single junction silicon solar cell. The network describes the complete solar cell including busbars, fingers, illuminated areas as well as the perimeter.

6.1.1 Optimum size of the elementary units

The chosen geometry for the elementary units is one of the key aspect when tools able to model large area electronic devices like silicon solar cell are developed. Analysis with numerical TCAD simulators is useful to account for the impact of doping profiles, metal architectures or passivation schemes in silicon solar cells [6-2][6-3]. This type of simulation basically analyses an element of symmetry (a small repetitive portion of the solar cell) in order to reduce the computational effort. Unfortunately, in this way is not possible to account for non-homogeneities in silicon solar cell. On the other hand, circuit simulation of

distributed electrical network allows analyzing a larger area with a reduced computational time. About circuit simulation of distributed electrical network, the main compromise required in the elementary unit geometry assignation is between the simulation accuracy level and the CPU calculation time. Some simulations were carried out to detect the optimum size of the elementary units. Of course, as well as the accuracy of the simulation there are several size aspect that need to be taken into consideration. Mainly, the size of the unit cell for fingers and busbars must be smaller that the current transfer length L_T (see appendix A) in order to avoid the overestimation in the effective area under the contact, secondly the size of the non-metalized elementary units must be smaller than the minority carrier diffusion length in the emitter. Details about the elementary unit dimensions implemented in the developed model will be shown in the next sections.

6.2 Parameters extraction for the calibration of the distributed electrical model

In order to calibrate the distributed electrical network the knowledge of I_{ph}, I_{01}, I_{02}, n_1, n_2, R_{SH} is needed. These are the parameters, which characterize each electrical component of the model. The value of each mentioned parameter depends on the geometry and position inside the solar cell. About the total series resistance (as contribute of the emitter sheet resistance, metal sheet resistance and contact resistance) the value can be calculated according to the physical properties of metallization and emitter region. Based on the approaches presented in [6-18] the extraction of the parameters for the distributed electrical model get started from the analysis of a dark I-V curve of solar cell which can be estimated from experimental measurements. For this purpose a homogeneous distribution of the parameters in the whole solar cell is supposed. The analysis is now explained.

Considering the two exponential behaviors to model the dark cell I-V characteristic:

$$I_C = I_{01}\cdot[e^{(V_C - R_S * I_C)/\eta_1 V_T} - 1] + I_{02}\cdot[e^{(V_C - R_S * I_C)/\eta_2 V_T} - 1] + \frac{V_C - R_S * I_C}{R_{SH}} \qquad (6.3)$$

where I_C is the total output current of the solar cell, V_C the output voltage, R_{SH} and R_S the equivalent lumped shunt resistance and the equivalent lumped series resistance of the solar cell respectively, it is possible to separate the obtained curve in two parts as shown in figure 6.3.

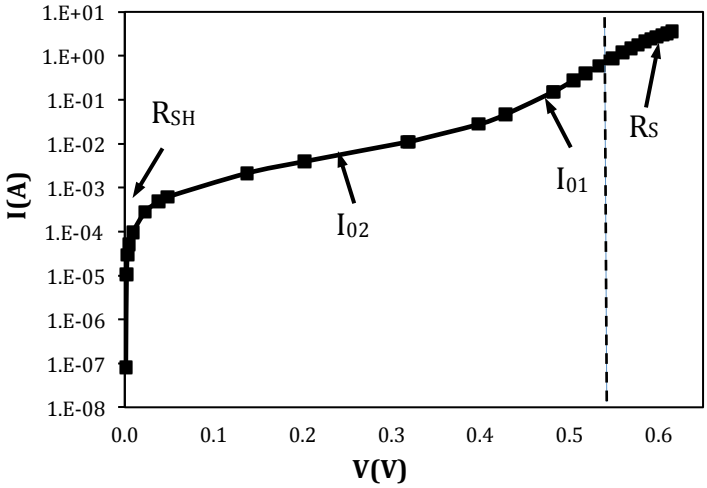


Figure 6.3: Dark I-V characteristic with two different regions.

The higher part includes the influence of the series resistance and the first exponential contribute; the lower part includes the shunt resistance impact and the second exponential behavior. Trough the development of a Matlab algorithm that minimizes the error by considering the mean root square (standard deviation) between the experimental date and the analytical model it is possible to extract the parameters. In particular, as first step looking at the experimental dark I-V curve between the range from 0 to 450mV, where the series resistance has no impact on the dark characteristic, and using the Matlab algorithm in this range with the only second exponential behavior and the shunt contribute of the analytical model, the shunt resistance R_{SH} and the second diode saturation-current I_{02} with the respective ideality factor n_2 can be extracted. As second step considering the remained dark I-V range (between 450mV and 650mV) the first diode saturation-current I_{01} is possible to obtain, holding a constant value of the ideality factor n_1 equal to one. About the total series resistance R_S, the distributed model takes into account separately the emitter, contact and metal series resistance and the value

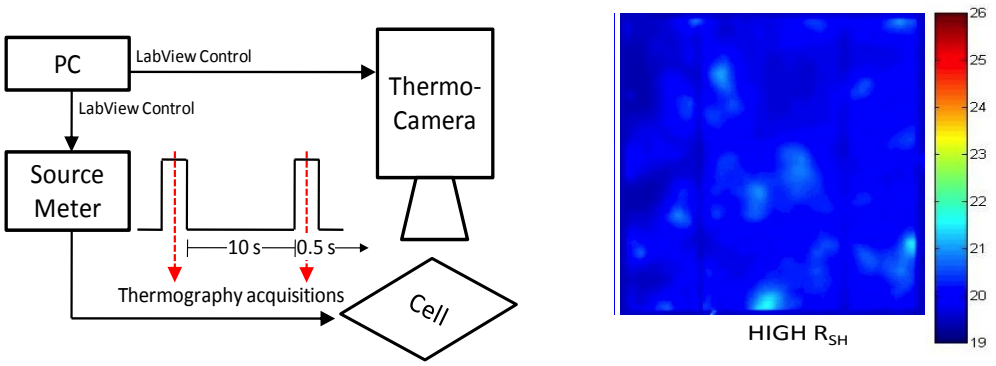
has been calculated accounting to the physical properties of metallization and emitter regions.

According with experimental measurements on a multicrystalline-silicon mc-Si solar cell, the parameters for the model have been extracted by using the above-described method and the distributed electrical model has been calibrated. In particular, trough the thermography analysis, a mc-Si solar cell without the presence of clustered defects inside the structure has been chosen in order to consider a uniform distribution of its electrical properties and use them for the calibration of the distributed electrical model. Moreover, a comparison with the results obtained by using the two-diode equivalent lumped model has been done. In the following sub-sections the procedure in detail is shown with an initial explanation of the thermographic characterization and dark I-V extraction of the solar cell sample used for the calibration of the distributed model.

6.2.1 Thermographic characterization of solar cell

Infrared thermography measurement of a silicon solar cell is a recent technique used in the photovoltaic field in order to evaluate the presence of hot-spot in the solar cell that usually appear in small region of the itself where clustered defects are present [6-1, 6-13, 6-14]. In conventional thermography setups, a dc bias is applied to the cell and a thermography image is acquired. The use of dc bias can have a detrimental effect on results of thermography measurements, since – due to the long measurement times – heat can spread on the cell area, negatively affecting the spatial resolution of the measurement. For the thermal measure of the mc-Si solar cell used as experimental sample for the calibration of the distributed electrical model, a setup for synchronous-pulsed thermal characterization has been realized that allows for a better spatial resolution without the need of a more expensive Lock-in thermography system [6-14]. Figure 6.4a shows a schematic block diagram of the measurements setup. A current pulse is applied on the cell for 500ms in reverse bias conditions and a spatially thermographic image is acquired immediately after the voltage on the

cell was stabilized. Then a zero current is applied for about ten seconds, to cool down the cell, and then another measurement can be taken. The final image is obtained as the average of over ten images in order to reduce noise. This kind of measurement setup is used to reduce self-heating of the cell during the measurements, thus increasing spatial resolution. In figure 6.4b the spatially resolved thermography of the cell is reported.



(a) (b)

Figure 6.4: (a) Schematic diagram of spatially resolved thermography measurement setup. (b) Synchronous-pulse thermography image of the analyzed cell.

The image shows that the cell presents a diffused heating of one or two degrees randomly distributed on device area, that means absence of clustered defects inside the solar cell and suggests the possibility to consider a uniform distribution of its electrical properties with good approximation.

6.2.2 Dark I-V measurement of solar cell

The dark I-V measurement of the solar cell was made using a source meter. The date were carried out with a four wire technique in order to minimize the effect of the parasitic impedance of the cables. In order to avoid a large current flow in reverse condition near the breakdown voltage, the characterization was stopped at -5 V. The dark I-V curve obtained is reported in figure 6.5. The very low current value measured in reverse condition of the cell, shows as the cell

present an high shunt resistance that it's in agreement with the thermal measurement shown in the previus section. This will be also confermed by the high solar cell performance meusered under different level of solar irradiation that will be shown in the next session.

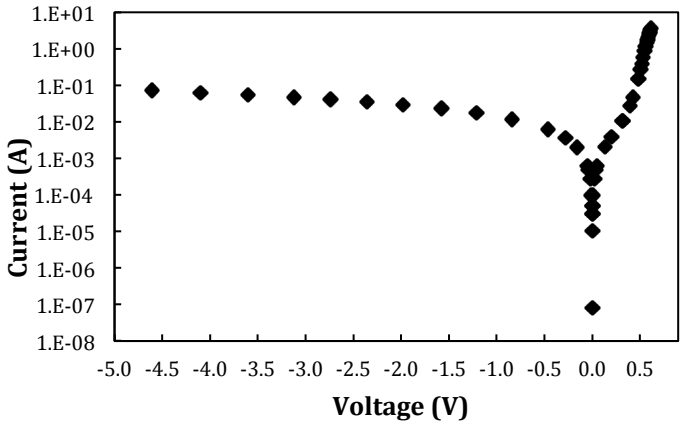


Figure 6.5: Dark I-V characteristic measured of the mc-Si solar cell.

6.2.3 Simulation results obtained with the distributed electrical model calibrated

As first step, the parameters of a two-diodes lumped elements model have been extracted. The results are reported in Table 6-II. It is worth noting that in this case the calculated series resistance includes the contribution of emitter, contact and metal resistances.

TABLE 6-II: Modelling parameters extracted from the experimental dark I-V curve.

CELL	J_{01} (A/cm^2)	η_1	J_{02} (A/cm^2)	η_2	R_{SH} (Ω)	R_S (Ω)
Sample	$1.02 \cdot 10^{-12}$	1	$2.1 \cdot 10^{-9}$	1.55	80	$5 \cdot 10^{-3}$

As second step, the parameters of the homogenous distributed electrical network have been extracted. To this purpose have been considered the same diode parameters and shunt resistances of Table 6-II. On the other hand, the resistive network (R_E, R_M, R_C) has been calculated according to the physical properties of metallization and emitter region reported in Table 6-III.

TABLE 6-III: Physical parameters of the considered mc-Si solar cell

Parameter	Value	Description
ρ_{Em} (Ω/□)	75	*Emitter sheet resistance*
ρ_M (Ω·cm)	$6 \cdot 10^{-6}$	*Resistivity of metallization*
ρ_C (Ω·cm^2)	$3 \cdot 10^{-3}$	*Contact Resistance*
A_F (μm^2)	1425	*Finger cross-section area*
W_{BB} (mm)	2	*Bus Bar width*
t_{BB} (μm)	23	*Bus Bar thickness*

By following this approach, it's possible to observe in Fig. 6.6 that same result of the 2-diodes lumped element model is achieved and that the distributed model is in good agreement with both the experimental date and lumped model.

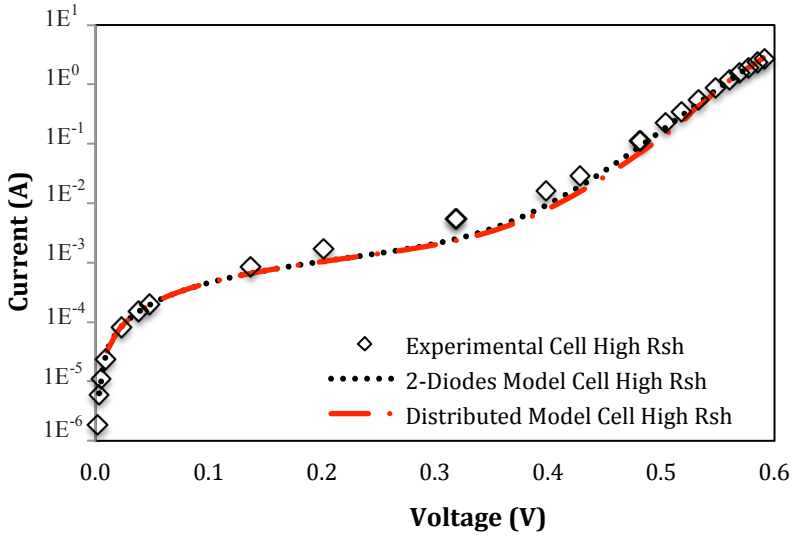


Figure 6.6: Comparison between experimental and simulated dark I-V curves.

Moreover, in Table 6-III it's possible to observe that the output electrical parameters of cell evaluated with the distributed network are very close to the one experimentally measured. This proves the accurate modelling of the resistive network and the proper operation of the distributed network.

TABLE 6-IV: Parameters obtained with the simulated model and with experimental measurements under 1.18 Sun.

Cell	E_{ff} (%)	V_{OC} (V)	I_{SC} (A)	FF (%)
Lumped Model	14.2	0.59	9.5	73.1
3-D Model	14.2	0.59	9.5	72.8
Experimental	14.4	0.59	9.5	73.4

In Fig. 6.7 are reported the simulated and measured I-V curves under different illumination levels. The simulated I-V curves are able to accurately account for the impact of the illumination level on the solar cell performance.

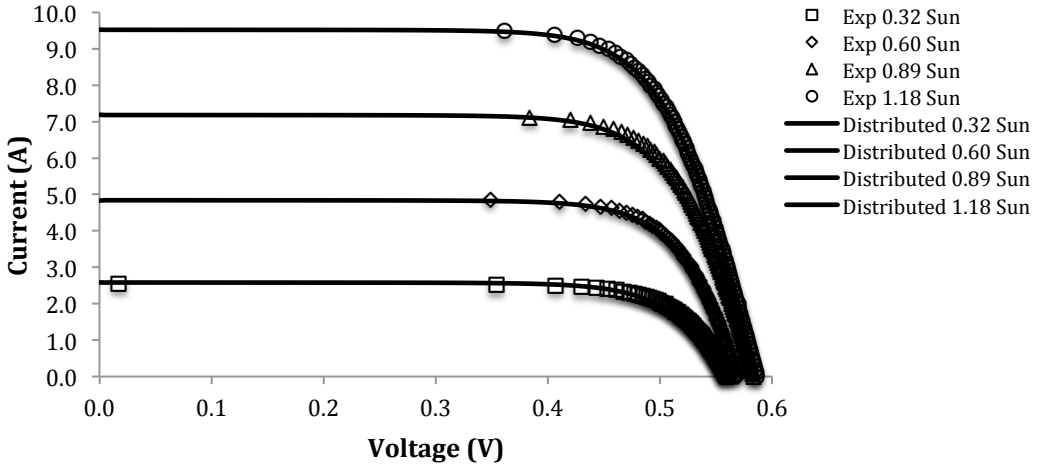
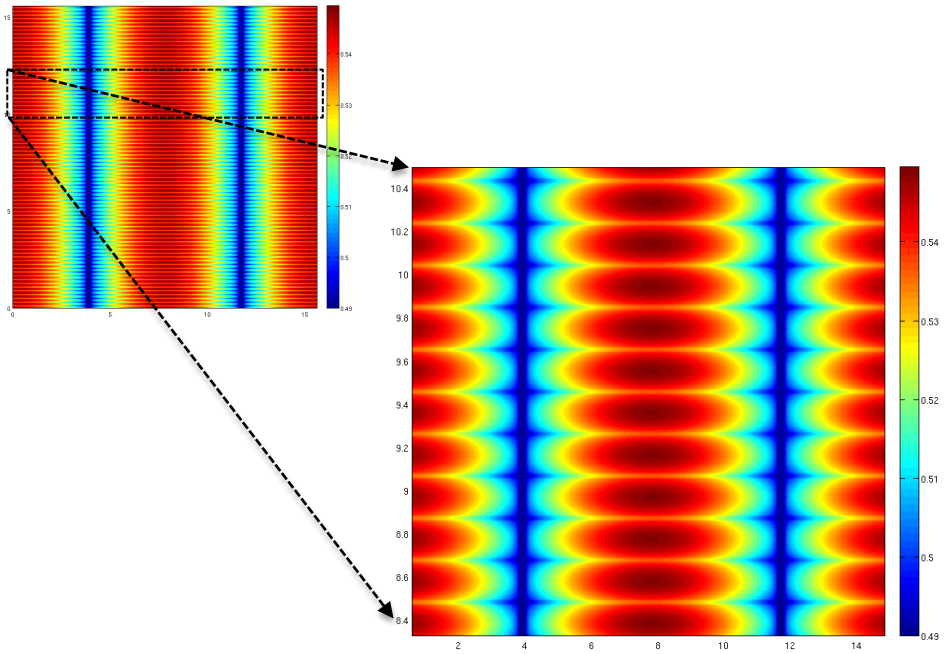


Figure 6.7: Experimental and simulated I-V curves under different illumination levels**.**

With the calibrated distributed model under different illumination levels, has been generated the voltage distribution under V_{OC} condition or around the maximum power point as well as the current density distribution across the whole solar cell. In Fig. 6.8 is shown a 2-D voltage distribution map of the solar cell, obtained with the cell forward biased around the maximum power point under a power irradiation of 1000W/m^2.

Looking at the zoom in of the 2-D voltage distribution map, it is possible to see that the local voltage is higher in the middle of each active area between two fingers and bus bars with a gradual decrease until the biased voltage value applied on the bus bars. This trend is due to the emitter sheet resistance that introduces a voltage drop when a photocurrent is generated and harvested through the metal.



(a) (b)

Figure 6.8: (a) 2-D Voltage distribution across the whole solar cell when a forward bias around the maximum power point is applied and under a power irradiation of 1000W/m^2. (b) Zoom in (not in scale) of the 2-D voltage distribution in a local region of the solar cell.

6.4 A case of study: effect of local shunts and its modeling in a silicon solar cell

In order to understand how the local shunt resistance is strongly correlated to the presence of localized defects that contribute to the generation of hot-spot, a second mc-Si solar cell has been analyzed and modeled. In this case a solar cell with lower performance respect the cell shown in the previous section has been chosen. Must be pointed out that both the cell come from the same fabrication process, and both were composed by two bus bars and eighty fingers in a total area of 243.36 cm^2 (15.6cm x 15.6 cm). In Fig. 6.9 is reported the spatially resolved thermography of the new cell. It's clearly visible a localized red region that highlights a high local temperature respect the remaining part of the solar cell. This effect is due to the presence of clustered defects in a small solar cell fragment that contributes to the generation of hot-spot [6-1][6-4].

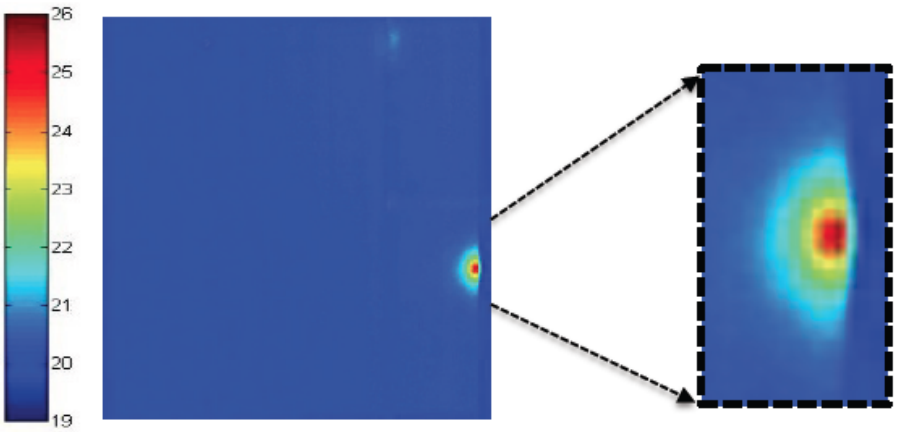


Figure 6.9: Synchronous-pulse thermography image of the analyzed shunted cell.

With the physical properties of metallization and emitter region already reported in Table 6-III and with the contribute of the above shown thermal image of the shunted solar cell, the distributed electrical model has been calibrated considering a non-uniform distribution of the shunt resistance. In particular, as first step and exactly in the same way as described for the previous solar cell modelling, the

parameters needed have been extracted considering a homogeneous distribution of the physical properties in the whole solar cell. In table 6-V are reported the parameters extracted for the analysed solar cell. In Fig. 6.10 a comparison between the experimental and simulated dark I-V with both distributed and lumped electrical model are also shown.

TABLE 6-V: Modelling parameters extracted from the experimental dark I-V curve

CELL	J_{01} (A/cm^2)	η_1	J_{02} (A/cm^2)	η_2	R_{SH} (Ω)	R_S (Ω)
Sample	$2 \cdot 10^{-12}$	1	$1.7 \cdot 10^{-9}$	1.51	0.26	$4 \cdot 10^{-3}$

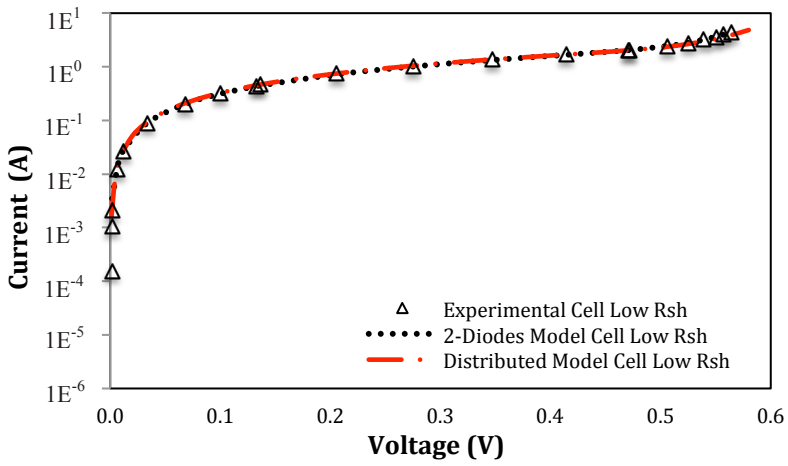


Figure 6.10: Comparison between experimental and simulated dark I-V curves for a shunted solar cell.

Again, as well as done for the previous solar cell analysed, simulations under different illumination levels have been carried out and compared with the experimental date. As it is possible to see in Fig. 6.11 where the results are reported, a reduction of the illumination level leads to a higher degradation of fill factor of the solar cell analyzed. This problem can influence the performance of the single cell and the functionality of the entire PV module (if the analyzed cell is inserted in a PV module) because in low illumination condition the shunt

resistance leads to a degradation of the fill factor and hence of the efficiency. Therefore the shunt resistance is a fundamental parameter to be considered in the "in-line" selection procedure of manufacturing production process.

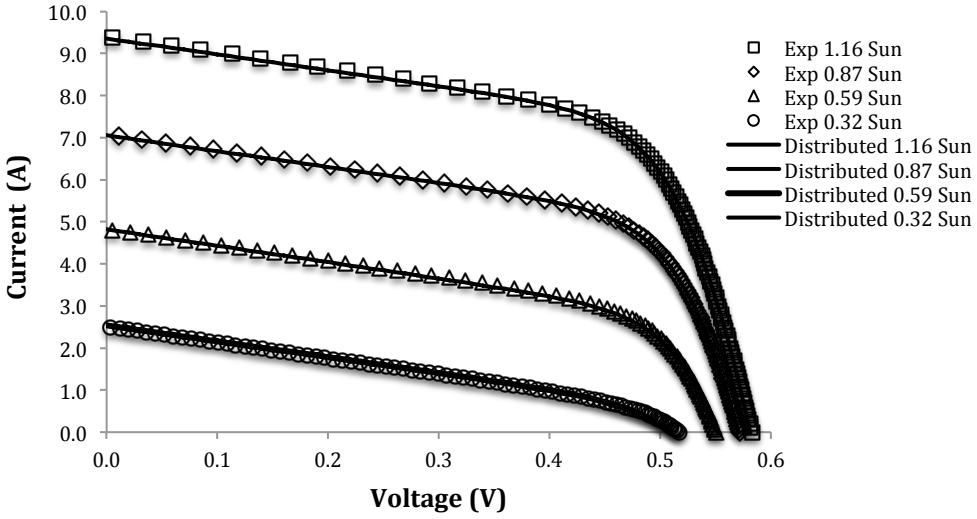


Figure 6.10: Experimental and simulated I-V curves under different illumination levels of the shunted solar cell.

As second step the distributed model has been calibrated to consider a non-uniform distribution of the shunt resistance. Based on the experimental thermography image of the cell with low shunt resistance, different values of shunt resistance have been introduced in two areas of the solar cell as shown in Fig.6.11 The small area in Fig.6.11, represents the hot-spot area (1.6 cm^2), hence a low value of shunt resistance is considered. The remaining part of the solar cell is modeled with a larger specific shunt resistance r_{sh} (around 20k$\Omega \cdot cm^2$). The other parameters are the same of Table 6-III and Table 6-V. For the specific shunt resistance in the small region of Fig. 6.11, three different cases have been considered: i) r_{sh}=0.417$\Omega \cdot cm^2$; ii) r_{sh}=1m$\Omega \cdot cm^2$; iii) r_{sh}<1m$\Omega \cdot cm^2$ (1e-4$\Omega \cdot cm^2$ or 1e-6 $\Omega \cdot cm^2$ 1e-8$\Omega \cdot cm^2$).

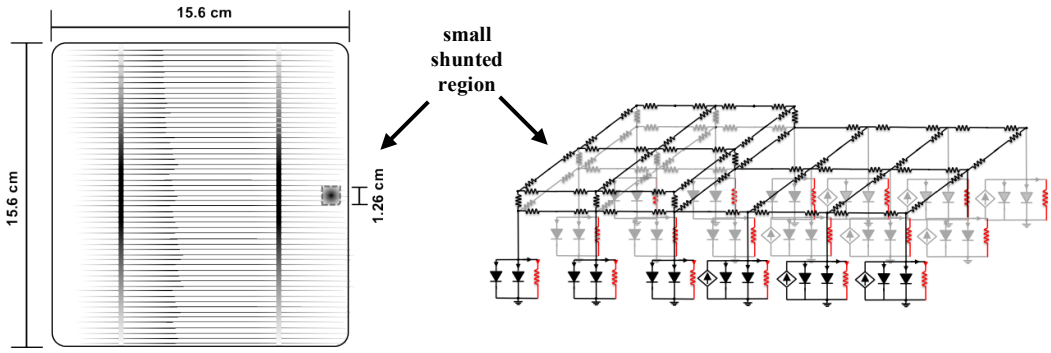


Figure 6.11: Schematic representation of the solar cell with the simulated hot-spot area. The highlighted shunt resistances in the distributed model represent the local region with a very low value of the resistance respect the remained solar cell.

The first value is calculated as the overall shunt resistance (0.26 Ω) times the hot-spot area (1.6 cm^2). Intuitively, this means that all the shunting effect is concentrated in the hot-spot area. However, simulation results, in table 6-VI and Fig.6.12 reveals that the I-V curves strongly deviate from the experimental measurements. Furthermore, the predicted FF is higher than the experimental value. Therefore, the analysis performed with the distributed network suggests that the local specific shunt resistance r_{sh} must be much lower than $0.417\Omega \cdot cm^2$. It is possible to observe in Table 6-VII that by considering a r_{sh} much lower than $1m\Omega \cdot cm^2$ a good agreement with experimental measurement is achieved. It is important to highlight that by using several values of the specific shunt resistance r_{sh}, 1e-4 $\Omega \cdot cm^2$ and 1e-6$\Omega \cdot cm^2$, the same value of efficiency is obtained. By increasing the r_{sh} up to $1m\Omega \cdot cm^2$, the output performances of the solar cell slightly change.

TABLE 6-V: Parameters obtained with the distributed network by considering different values of the specific shunt resistance in the hot-spot area (1.6 cm^2) and under 1.18 Sun.

Cell	E_{ff} (%)	V_{OC} (V)	I_{SC} (A)	FF (%)
Experimental	11.7	0.580	9.40	60.8
r_{sh}= 0.417 ($\Omega \cdot cm^2$)	12.98	0,582	9.43	67.9
r_{sh}= $1e^{-3}$ ($\Omega \cdot cm^2$)	11.8	0.580	9.40	61
r_{sh}= $1e^{-4}$, $1e^{-6}$, $1e^{-8}$ ($\Omega \cdot cm^2$)	11.7	0.578	9.38	60.7

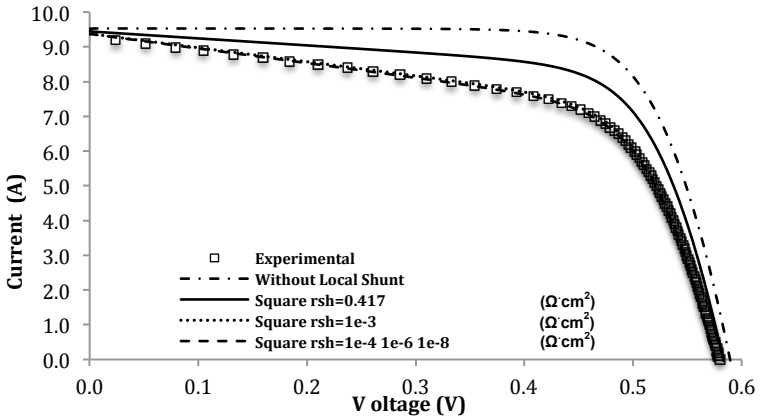


Figure 6.12: Experimental and simulated I-V curves obtained by considering different values of local specific shunt resistance in the hot-spot area (1.6 cm^2) under 1.18 Sun.

With this analysis appears clear that, by modelling the hot-spot area with a low specific shunt resistance obtained as the measured overall shunt resistance (0.26Ω) times the hot-spot area (1.6 cm^2), simulated results are strongly different from experimental measurements. In particular, higher value of fill factor and efficiency are found. Therefore, a lower value of specific shunt resistance must be considered. This means that the impact on the solar cell performance strongly depend by the hot-spot area. In fact, if the specific shunt resistance is kept constant and the hot-spot area is varied a different fill factor is observable. Moreover, by performing the analysis under different illumination conditions, it is

possible to see that the effect of a low shunt resistance is more relevant at low irradiation levels. To complete this analysis, the local dissipated power density on the shunted solar cell has been carried out in order to understand how much power locally the solar cell with shunt region can dissipate. As well as done for the analyzed cell shown in the previous section, with the calibrated distributed model, the voltage distribution and spatially current density maps in the whole solar cell have been generated. As shown in Fig. 6.12 where a solar cell voltage distribution around the maximum power point is simulated, a local shunt effect impacts on a biggest area in the solar cell compared to the effective area with a low shunt resistance (the blue region with almost 0V due to the very low value of the local shunt resistance). In this particular case, the impact reaches the bus bar closest to the hot-spot, making almost this entire region unavailable for the photocurrent generation.

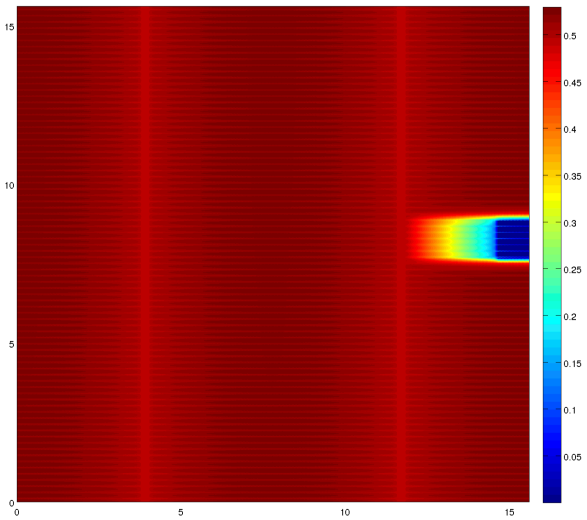


Figure 6.12: 2-D Voltage distribution across the whole solar cell with a low shunt resistance when a forward bias around the maximum power point is applied and under a power irradiation of 1000W/m^2.

In this way, it's easy to understand that a hot-spot can affects the solar cell performance with different impact, considering its different position into the solar cell. Of course this means that the impact can also be different if a highest number of fingers are involved in the hot-spot region, or a portion of bus bar is totally

shunted. As well as if the shunted region is localized on the edge or in the middle of the solar cell, the impact can be different. It's possible to conclude that the solar cell performance depends by the hot-spot area, hot-spot position, and number of hot-spot regions inside the cell. Another important information can be carried out from the analysis of the current density distribution and, consequently, from the dissipated power density map shown in Fig. 6.13 and Fig. 6.14 respectively. In both the maps shown, the electrical parameters are in a logarithmic scale in base 10.

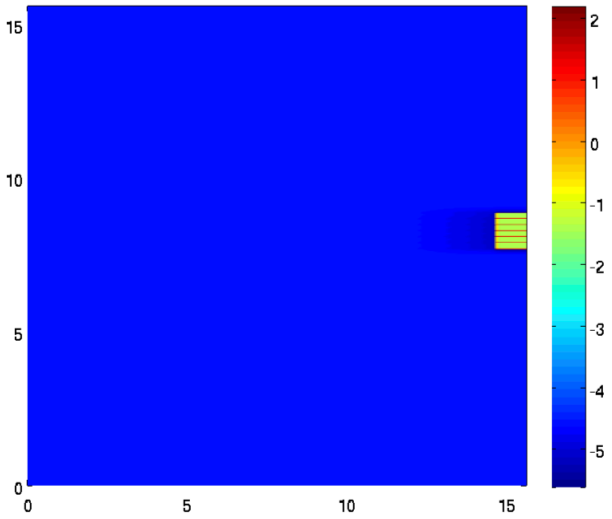


Figure 6.13: 2-D Current density distribution across the whole solar cell with local low shunt resistance when a forward bias around the maximum power point is applied under a power irradiation of 1000W/m^2.

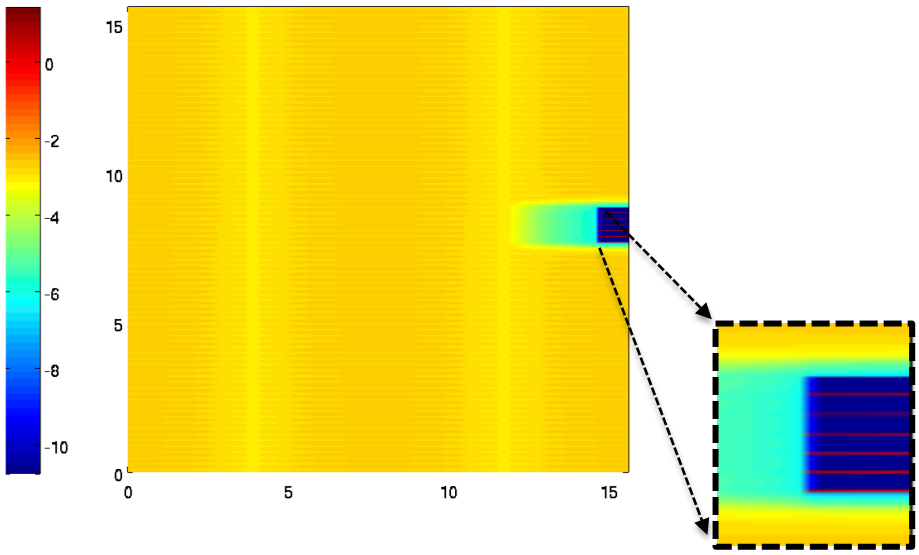


Figure 6.14: 2-D Dissipated power density distribution across the whole solar cell with local low shunt resistance when a forward bias around the maximum power point is applied under a power irradiation of 1000W/m^2. The zoomed region highlights how the dissipated power is closes just under the finger segments (red color due the highest power dissipated in this case).

As it is possible to see from the Fig. 6.13, although the entire hot-spot region has been modeled with an equal shunt resistance, almost all the current flows trough the shunt resistances under the fingers involved in this region. This means that most of the power dissipated is close in a very small region composed by the finger segments as shown in Fig. 6.14. As exposed in the previous chapter, considering that for standard photovoltaic applications usually solar cells are encapsulated in a module which is composed by different layers with low thermal conductivity [6-16, 6-19], the power dissipated in a so small region can cause a local increase of the temperature with a consequent overheating that can damage the cell permanently [6-19, 6-20].

6.5 Summary

In this chapter, the development of a three dimensional 3-D electrical network for modelling double side silicon solar cell has been presented and validated. Based on a network of repetitive elementary units each one modeled by a two-diode electrical circuit and allows accounting for transport through the emitter, the fingers and the busbars, the tool is able to account for the non-uniformity in the solar cell and to take into account for shaded condition with different irradiation levels. The presence of local shunting, due to localized crystal defects, has been analyzed and modeled with the tool. Both experimental and simulation results have shown how hot-spot regions results in a degradation of the fill factor and then of the overall power conversion efficiency.

Moreover, the developed distributed electrical model is exploited to understand how the different spatial distribution of local defects can impact on the solar cell performance.

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Conclusions

In this thesis, modeling and design of several advanced reliable circuits and devices for energy efficiency, have been considered. It has been shown that taking into account different applicative contexts, faults analysis and high reliability modeling are important activities needed to improve quality and performance of electronic devices.

In particular, discussing separately the applicative contexts considered, the problem about the reliability of standard communication protocols in wireless sensor networks to guaranty a secure communication has been discussed. A new communication protocol allows increasing the security compared with standard communication protocols it has also been presented.

In the chapter 3, a novel scheme for the on-die measurement of either clock jitter, or process parameter variations has been developed and analyzed. It has been shown that this type of scheme is needed during the test and debug phase of microprocessors, to validate the design and manufacturing process. It should be noted that due to its allowing both process parameter variation and clock jitter measurements, the developed scheme features accurate clock jitter measurement, despite the possible presence of significant process parameter variations, provided that process parameter variations are preliminary measured with respect to clock jitter.

In the field of energy scavenging systems, an accurate analysis on the effects of fault affecting an integrated circuit performing energy harvesting from mechanical vibrations has been carried out with the development of a possible solution to make it fault tolerance from internal faults.

For photovoltaic devices, the problem of modeling the thermal behavior of photovoltaic (PV) cells has been analyzed. It has been shown that, due to the combination of their being exposed to shading and localized crystal defects inside the cell, it may experience a dramatic temperature increase with consequent reduction of the provided power. The thermal model presented which allows estimating the temperature of the hot-spot area as a function of the time interval during which the PV cell is under hot-spot condition has been validated against experimental data, and constitutes a first preliminary step towards the development of shading-tolerant approach. Moreover, the model presented has highlighted that, differently from what may be expected, a partially shaded PV cell enters the hot-spot condition faster than a fully shaded PV cell, thus providing useful hints to PV array design. For instance, arrays composed by small cells could be preferred to arrays made of larger cells.

Finally, by the development of a distributed electrical network able to model in detail the behaviour of silicon solar cells, the effect of local shunting on mc-Si solar cell has been modelled. Associated with the thermal model presented in the chapter 5 and with an infrared thermography characterization of the solar cell, it has been clearly revealed how the shunt resistance is strongly correlated to the presence of localized defects that contribute to the generation of hot-spot. Moreover, with the distributed model has been shown how the different spatial distribution of local defects can impact on the solar cell performance in term of fill factor, efficiency and power dissipation.

Appendix A

Contact resistance calculation in a solar cell

In this appendix, details regarding the calculation of the contact resistance in a solar cell are given (Sect. A.1). A brief description on the technique used for its measurement with an analysis on trustworthiness of this technique when applied to measure a contact resistance in a solar cell is also discussed (Sect. A.2).

A.1 The "real value" of contact resistance in a solar cell

As well as in a generic integrated circuit where there is interaction between metal and semiconductor, in a photovoltaic solar cell the contact resistance refers to the resistance associated with the metal/semiconductor barrier at the interface between metal contact and semiconductor. For example, in a solar cell structure like that one shown in the previous chapter 6, the current travels through the emitter toward the fingers and passes in the interface before travelling in the metal [A-1]. The value of this contact resistance depends on many factors (semiconductor material, contact material, doping concentration an so on).

Without taking into account of the current mechanisms at the semiconductor/metal interface, a simple way to calculate the specific contact resistance is given by:

$$R_C = \rho_c / A \ (\Omega) \qquad (1.A)$$

where ρ_c is the specific contact resistivity of the metal considered and A is the surface area where metal/semiconductor interface is created. If the voltage across the metal/semiconductor is considered a constant value, the equation (1.A) could also be written as the ratio between the voltage V across the contact and current I that flows through the contact:

$$R_C = V/I \ (\Omega) \qquad (2.A)$$

Unfortunately (1.A) and (2.A) cannot be applied in a solar cell to calculate the contact resistance between metal and substrate. This because, the potential across the interface in contacts that collect lateral current such as the fingers in a solar cell, is maximal at the finger edge and minimal at the center due to the substrate sheet resistance (in this specific case the emitter sheet resistance R_{em}) below the finger. In this way the specific contact resistance is related not only to the specific contact resistivity ρ_c but also to the sheet resistance of the substrate R_{em} [A-1, A-2]. By these considerations and knowing that the contact resistivity ρ_c and the emitter sheet resistance ρ_{em} are of distributed nature, if V_0 is the maximal voltage on the metal edge, it is possible to observe that there is nearly exponential voltage decay under the contact, as shown in fig. A.1 [A-2].

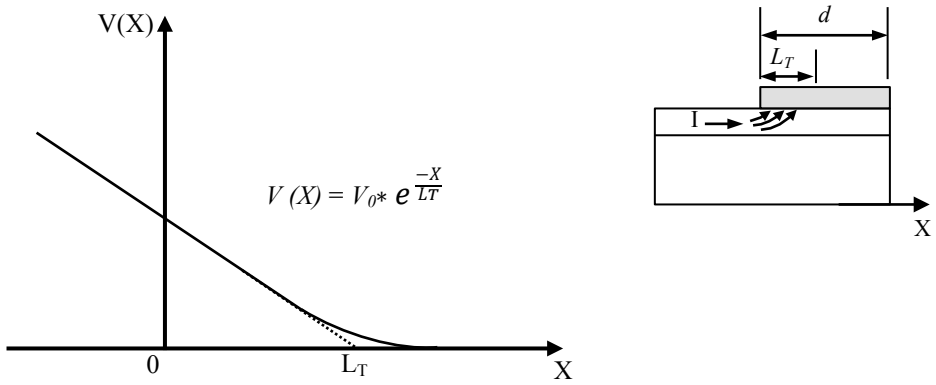


Figure A.1: Voltage decay under the contact and current transfer length representation in a solar cell.

As can be seen from the equation shown in fig. A.1, a new parameter is introduced and called "current transfer length" L_T that is expressed as $\sqrt[2]{\rho_c/R_{em}}$. Basically, by considering L_T that relates the voltage variation under the contact area to the distance over which the current transfers from the emitter to the metal, the contact resistance can be now expressed as:

$$R_C = \rho_c/(L_T * w)\ (\Omega) \tag{3.A}$$

where W is the length of the considered metal finger.
However, this equation can be true just in case of the contact width d of the metal is very long respect L_T ($d >> L_T$). As analyzed and derived by Shockley in [A-1], when this assumption cannot be done the contact resistance Rc is expressed as:

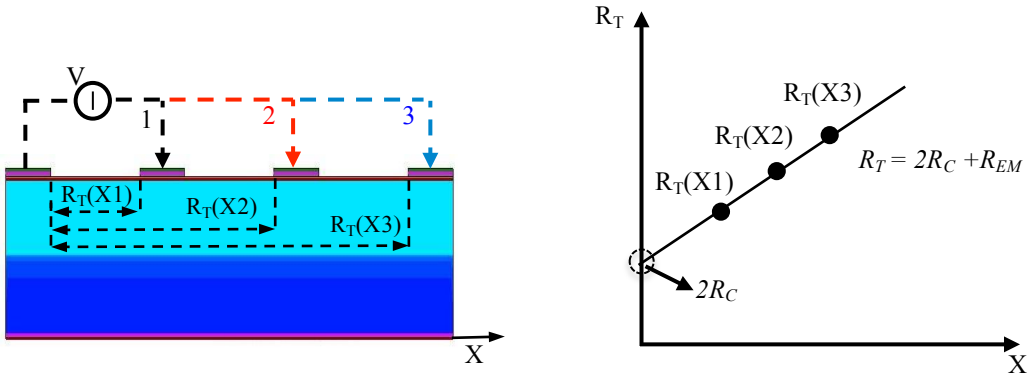
$$R_C = \frac{\rho c}{W * LT} * coth\left(\frac{d}{LT}\right) \tag{4.A}$$

In fact by knowing the trend of the hyperbolic cotangent can be easily derivable that for $d >> L_T$ the (4.A) becomes exactly the (3.A) vice versa when d it's almost closed to 0.5 L_T the (4.A) can be reduced to the (1.A).

A.2 Transmission Line Model applied to measure the contact resistance

The above-described calculation is used in a common method to quantify the real performance of ohmic contacts to semiconductor once manufactured the solar cell. This method is defined as Transmission Line Model (TLM). According to this method, a segment of solar cell involving several fingers is considered, and the total resistance R_T is measured between one finger and the others, in order to graph R_T against the distance variation between the fingers. In particular, as it is schematized in fig. A.2, a voltage is applied between two fingers and the current is measured. Changing finger and consequently the distance between themselves, a different current can be measured. Considering few fingers, when the contact

resistance is the same for each finger and the emitter sheet resistance is homogeneous, a straight line can be plotted.



(a) (b)

Figure A.2: (a) Schematic representation of the TLM applied to the solar cell segment in order to extract the contact resistivity. **(b)** Plot of total contact-to-contact resistance as a function of the distance X in order to obtain the current transfer length and the contact resistance.

The interception of the line with R_T axis can be used to calculate ρ_c considering that the value of R_c is equal to (4.A). Moreover, more information can be extracted from the straight-line equation. Writing it as:

$$R_T = 2 * \frac{\rho c}{W * LT} * coth\left(\frac{d}{LT}\right) + \frac{Rem * X}{W} \qquad (5.A)$$

It is possible to extract the value of the emitter sheet resistance because of the slope of the considered straight line. This means that by using this experimental method it is possible to measure the contact resistivity and the emitter sheet resistance which are two important parameters that must be knew in order to understand their contribute on the solar cell performance. Of course, for this method the busbars must be disconnected from the fingers to avoid parallel conduction. In practice, small samples must be cut from the cell.

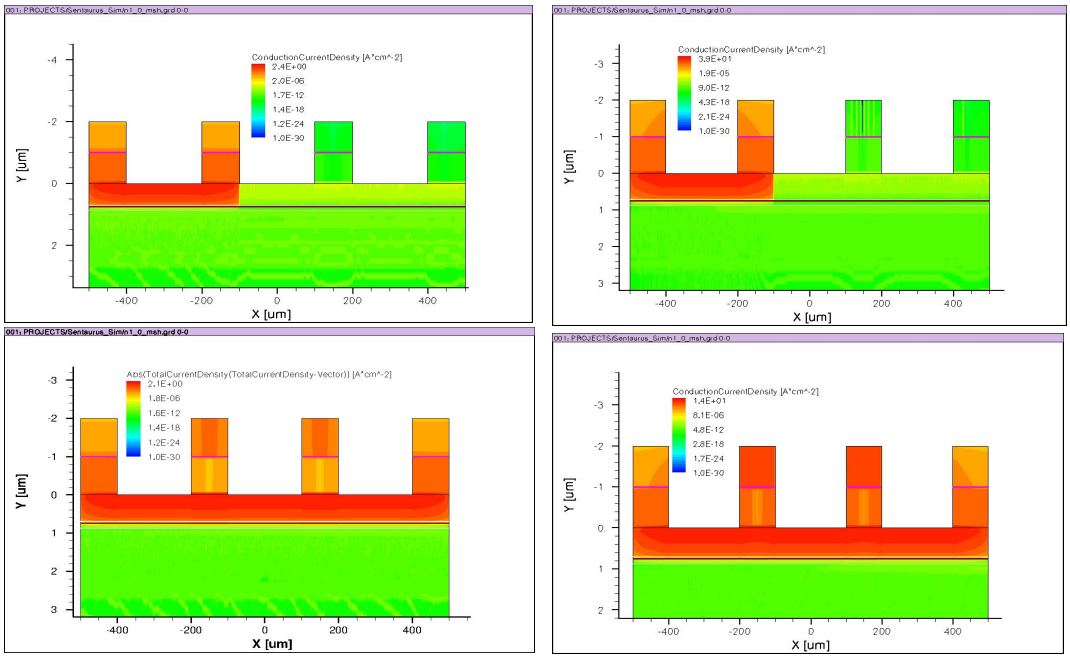
However, in term of model applied to solar cell devices this method presents several limitations:

1) Its only works when the contact resistance is exactly the same for each finger considered.

2) The emitter sheet resistance must be supposed equal in the whole substrate involved in the measure, without distinction between metal and non-metal interface area.
3) The negative contribute in term of measure affected by the metal of the fingers in the middle between two external fingers (considering for example the measure of R_T (X3)), is neglected.

Although the first two points can be assumed, by doing 2-D device simulations using TCAD Sentaurus [A-4], an analysis has been carried out, in order to quantify the error introduced considering negligible the third point listed above. Due to the low value of the contact resistivity used in recent silicon solar cells, when a voltage is applied between the two external fingers as in the case of R_T (X2) or R_T (X3), the current generated in the substrate, flows not only in the emitter, as supposed by the model, but also through the metal of the fingers that are in the middle. This means that the current path until the external finger is modified due to the presence of these metals. To emphasize this effect two different simulations have been done. By considering exactly the same structure for both the simulations, the first one had a low value of the contact resistivity that is very close to the real contact resistivity used for silicon solar cell devices; the second one with hundred times higher value of the contact resistivity respect the previous. For both the considered cases the TLM has been simulated in order to measure the total resistance R_T and to extract the contact resistivity ρ_c from the simulation results. In fig. A.3 a) and b) are shown respectively the simulations with high and low contact resistivity when a voltage generator is applied between two adjacent fingers (upper part of the figure) and when a voltage generator is applied between the two external terminal (lower part of the figure).

As can be seen on the lower right part in the picture, the current (indicated by a red colour) flows inside the emitter as well as in the metal of the fingers. This confirms that when a low value of contact resistivity is used the TLM cannot works correctly in order to extract the contact resistivity because of the above-mentioned motivations.



(a) (b)

Figure A.3: 2-D Simulation results of a simple solar cell segment composed by four fingers with a low value of ρ_c ($1e^{-3}$ Ω*cm^2) **(a)**, and with higher value of ρ_c ($1e^{-1}$ Ω*cm^2) **(b).** A voltage generator is applied between two adjacent fingers in the figure on the upper part of the picture, and between the two external fingers in the lower part of the picture.

Plotting the results obtained respect the nominal value of the contact resistivity used in the simulations, the error introduced by the TLM to extract the contact resistivity is displayed. In fig. A.4 the values of the contact resistivity extracted with the TLM from the simulation results are shown, respect their corresponding nominal values.

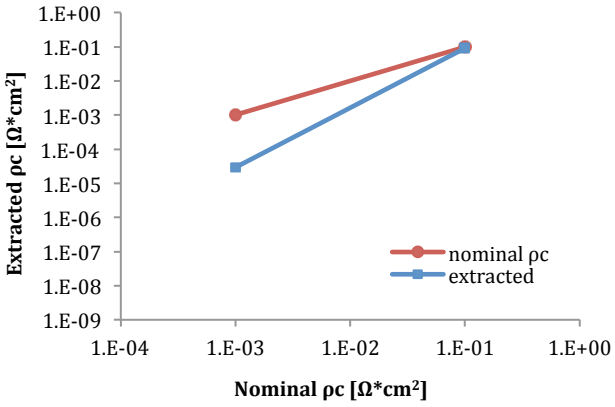


Figure A.4: Contact resistivity extracted with the TLM from the two different cases simulated (blue line), respect the nominal value used in the simulations (red line).

As can be seen, for high contact resistivity the value extracted with the TLM is very close to the nominal value considered. This because, due to the high contact resistivity, almost all the current generated in the substrate, flows just through the emitter without passing through the metal, and the TLM assumptions can be applied. Vice versa when the case of low contact resistivity is considered, the value extracted with TLM is totally different respect the nominal value (ρ_c extracted = 29.3 μΩ*cm^2 respect the ρ_c measured = 1 mΩ*cm^2).

However, with some mathematical consideration, and introducing in the TLM the contribute in term of current path added due to each metal presents in the segment, a convergence toward the correct contact resistivity can be also obtained when a its low value is used. In fact, as described in [A-1], the total resistance extracted from each measurement can be written as:

$$R_T = \frac{Rem*X}{W} + 2 * \frac{\rho c}{W*LT} * coth\left(\frac{d}{LT}\right) + 2 * \frac{\rho c}{W*LT} * tanh\left(\frac{d}{LT}\right) * (N-2) \qquad (6.A)$$

where N is the total number of fingers between the terminals of the voltage generator applied for the measure, and $(2 * \frac{\rho c}{W*LT} * tanh\left(\frac{d}{LT}\right))$ is the corresponding value determined for each one of those fingers. As can be seen in fig. A.5, where

the extracted contact resistivity is plotted using the new model, the results obtained now are in good agreement for both, low and high contact resistivity.

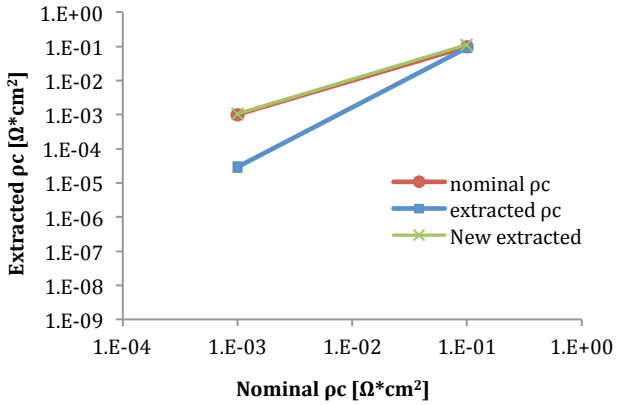


Figure A.5: contact resistivity extracted with the TLM from the two different cases simulated (blue line) and with the modified model (green line) respect the nominal value used in the simulations (red line).

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Curriculum Vitae

Daniele Giaffreda was born in Bologna, Italy, on June 19, 1981. He received his 1-st and 2-nd level Master Degree in Electronic Engineering in 2006 and 2009, respectively. In 2009, he joined the ARCES research center, University of Bologna, Bologna, starting the Ph.D. program in Information Technology. From February 2012 to May 2012 he was visiting student at Applied Materials (AMAT), Santa Clara, California (USA). From November 2012 to January 2013 he was visiting student at the IMEC research center, Leuven, Belgium. He is currently working with the ARCES photovoltaic devices modelling and simulation group.

List of Publications

[1] M. Omana, D. Giaffreda, C. Metra, TM Mak, S. Tam A, Rahman, "*On-Die Ring Oscillator Based Measurement Scheme for Process Variations and Clock Jitter*", IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), 2010.

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Twenty years from now you will be more disappointed
by the things that you didn't do than by the ones you did do.
So throw off the bowlines. Sail away from the safe harbour.
Catch the trade winds in your sails. Explore, Dream, Discover…
Mark Twain