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ADVANCED CMOS INTERFACES FOR BIO-NANOSENSORS

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Advanced CMOS interfaces for bio-nanosensors

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To Deborah,

for being my muse.

Abstract

The improvement of devices provided by Nanotechnology has put forward new classes of sensors, called bio-nanosensors, which are very promising for the detection of biochemical molecules in a large variety of applications. Their use in lab-on-a-chip could gives rise to new opportunities in many fields, from health-care and bio-warfare to environmental and high-throughput screening for pharmaceutical industry. Bio-nanosensors have great advantages in terms of cost, performance, and parallelization. Indeed, they require very low quantities of reagents and improve the overall signal-to-noise-ratio due to increase of binding signal variations vs. area and reduction of stray capacitances. Additionally, they give rise to new challenges, such as the need to design high-performance low-noise integrated electronic interfaces.

This thesis is related to the design of high-performance advanced CMOS interfaces for electrochemical bio-nanosensors. The main focus of the thesis is: 1) critical analysis of noise in sensing interfaces, 2) devising new techniques for noise reduction in discrete-time approaches, 3) developing new architectures for low-noise, low-power sensing interfaces. The manuscript reports a multi-project activity focusing on low-noise design and presents two developed integrated circuits (ICs) as examples of advanced CMOS interfaces for bio-nanosensors.

The first project concerns low-noise current-sensing interface for DC and transient measurements of electrophysiological signals, such as those used for ion channel applications. The focus of this research activity is on the noise optimization of the electronic interface. A new noise reduction technique has been developed so as to realize an integrated CMOS interfaces with performance comparable with state-of-the-art instrumentations. One CMOS chip prototype has been realized and is now in fabrication.

The second project intends to realize a stand-alone, high-accuracy electrochemical impedance spectroscopy interface. The system is tailored for

conductivity-temperature-depth sensors in environmental applications, as well as for bio-nanosensors. It is based on a band-pass delta-sigma technique and combines low-noise performance with low-power requirements. As in the previous case, one CMOS chip has been realized.

In future developments, the concepts behind the two ICs can be combined to get a final system implementing an ultra low-noise extended potentiostat, capable of doing both DC and AC measurements for bio-nanosensors applications.

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First of all, I would like to thank my research advisor Prof. Marco Tartagni, for his support and encouragement during my Ph.D. course. He always believed in me and in my potential, even more than I did. He is my mentor.

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Introduction

This thesis analyzes in detail the design of advanced CMOS interfaces for high parallel, high precision, bio-nanosensor arrays in lab-on-a-chip applications, whose electronic requirements are various and mainly dependent on the specific application and the kind of nanosensor employed. Therefore, the manuscript reports the study and the design of two CMOS interfaces intended for two different applications:

- Ion-channel-based bio-nanosensor for high throughput screening of chemical compounds. It principally needs very low-noise readout systems able to acquire currents in the picoAmpere range (chapters two, three and four).
- Conductivity-Temperature-Depth (CTD) sensors for monitoring ocean water. It principally needs low-power electronic interfaces working stand-alone for at least a couple of years (chapter 5).

In addition, mixed-signal electronic design is needed in order to meet all the general requirements in terms of peak performance, flexibility and size.

The thesis is organized as follows. Chapter 1 provides an introduction to bio-nanosensors, giving definitions of biosensors and nanosensors. It reviews some of the more interesting electrochemical bio-nanosensor as well as their leading readout techniques and instruments. Finally, it briefly reports a previous project about bio-nanosensing, which is the starting point of this thesis work.

Chapter 2 discusses current-sensing interfaces that are the core electronic element in amperometric measurements for bio-nanosensor applications. It focuses on integrated CMOS interfaces because the integration process grants many benefits in terms of signal-to-noise-ratio, cost, and flexibility. Since very low output currents characterize several interesting bio-nanosensors, the chapter inspects in detail low noise current-sensing interfaces. The chapter reviews and compares the principal current-sensing architectures, analyzing the noise performance and evaluating possible future trends.

Chapter 3 presents a new technique for noise reduction in discrete-time current-sensing interfaces. It is based on decoupling of the noise density from the equivalent noise bandwidth, allowing us to trade power for low noise.

Chapter 4 proposes a novel ultra low-noise CMOS current-sensing interface based on the new noise-reduction technique presented in the previous chapter. It permits DC and transient measurements and achieves input-referred noise power spectrum density as low as state-of-the-art instrumentations. The circuit will be arranged in array fashion so as to implement a high throughput screening system for drug discovery. To improve flexibility, the IC allows multiple input ranges and acquisition bandwidths; moreover it implements an on-chip offset compensation to counteract the voltage drop across the electrode in a two-electrode potentiostat approach.

Chapter 5 presents a 15bit fully-integrated electrochemical impedance spectroscopy (EIS) system for CTD sensors in ocean monitoring applications, but it could also be used in bio-nanosensor applications. The circuit implements a lock-in technique based on a band-pass delta-sigma approach, to lower power consumption and eliminate the need of analog demodulation. The IC generates a stimulating-current signal and reads a voltage to satisfy CTD sensor requirements; however, the proposed approach can be combined with the current-sensing interface presented in chapter 4 so as to get an EIS system for amperometric measurements.

Finally, chapter 6 summarizes the outcomes of the thesis and analyzes an outlook of possible future improvements for the above-presented ICs.

This thesis work started a couple of years ago with the study of a sub-pA current amplifier for parallel recording of ion channels. From that point two research branches began: one aiming to design a new current interface for DC measurements with ultra low-noise capability; and the other targeting a new fully-integrated CMOS interface for AC measurements. These two research activities have been carried out in parallel and in the future will be combined to create an ultra low-noise extended potentiostat for bio-nanosensor applications (Fig. 1).

It should be noted that both ICs are the result of teamwork with the other members of Cesena lab group (M. Bennati, F. Thei and M. Rossi) and my

personal effort has been mainly focused on the aspects highlighted in this thesis and summarized in the abstract.

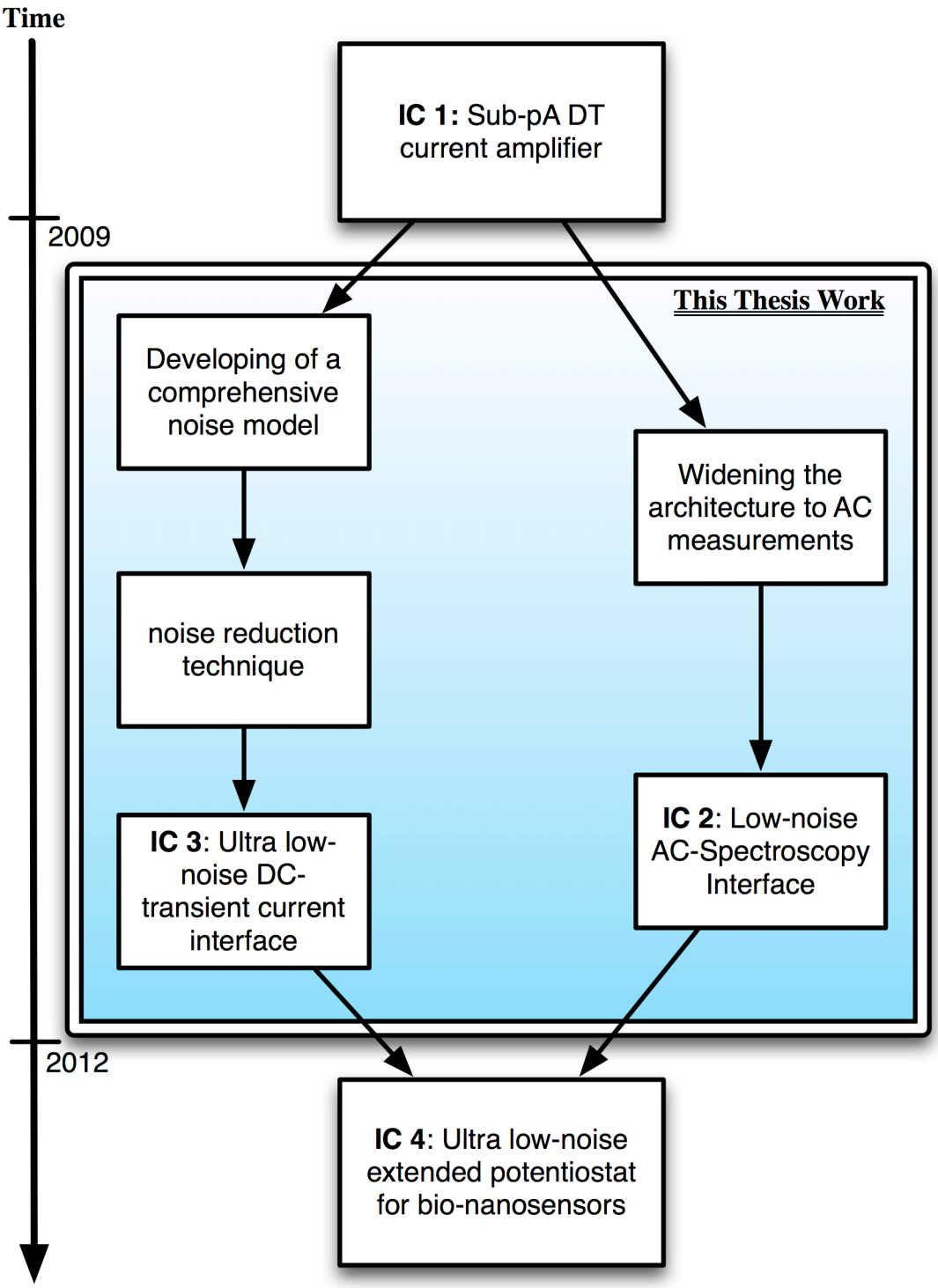

Fig. 1 Flowchart of the research activity discussed in this manuscript.

Chapter 1

Bio-nanosensors, Measurement Approaches and Applications

In the past few years, the convergence of nanotechnology with biotechnology and integrated electronics has shown an emerging and evolving interest. This trend promises great opportunities for the development of new classes of rapid, sensitive, and reliable biosensors systems based on nanotechnologies. These devices could have a great impact on many application fields related to our life: from health-care and environment, to food production and bio-warfare.

This chapter provides an introduction to bio-nanosensors, giving definitions of biosensors and nanosensors and overviewing the main application fields. It reviews some of the more interesting electrochemical bio-nanosensors, such as nanopores and nanowires, as well as their leading readout techniques and instruments. The chapter presents the extended potentiostat as the primary electronic instruments for electrochemical investigation and analyzes the state of the art of integrated bio-nanosensors interfaces. At the end, it briefly reports a previous project about parallel recording of single ion channel, showing the starting point of this thesis work and an example of convergence between biotechnology and integrated electronics.

A nanosensor is any nanometer-sized device able to detect and transduce information about nanoparticles, such as molecules or chemical compounds. Currently there exist different kinds of nanosensors, including

nanostructured materials, nanoparticles, nanoprobes, nanowires, nanometer electro-mechanical systems (NEMS), etc… (Fig. 2). Moreover, there also are several ways to build nanosensors, such as top-down lithography, bottom-up assembly, and molecular self-assembly. The foremost advantages of nanosensors are in terms of cost, performance, and parallelization. Indeed, they require very low quantitative of reagents and improve the signal-to-noise-ratio (SNR) due to increased binding signal variations vs. area [Hassibi,05], as well as reduction of stray capacitances [Bennati,09].

A biosensor is an integrated device providing quantitative or semi-quantitative analytical information using a biological recognition element [Thevenot,01]. One of the earliest classes of biosensors was that of catalytic systems, in which a substrate is converted into a product. Catalysis occurs on the sensing element interface and depletion of the substrate or formation of the product is monitored by a transducer. In more recent years, a new generation of biosensors, called affinity biosensors, have been introduced consisting of analytical devices using antibody, nucleic acid sequence, biomimetic material or receptor protein interfaced with a signal transducer to measure a binding event [Labuda,10].

Modern biosensors are usually implemented at nanometer scale sizes taking the nanosensors benefits. In this thesis we will use the term bio-nanosensor referring to nanometer sensors detecting biological nanoparticles.

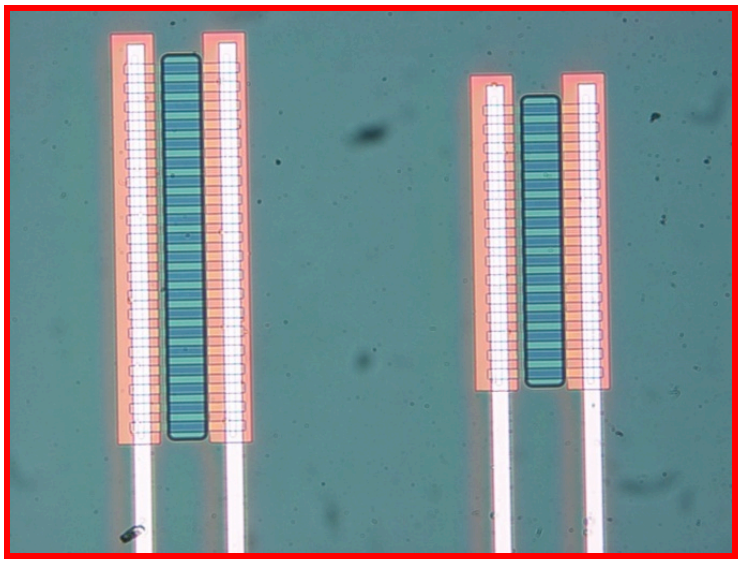

Fig. 2 Microscope photograph of two sets of nanowires featuring 10nm width and 10µm length. Nanowires are gaining great interest from researchers as promising nanosensors.

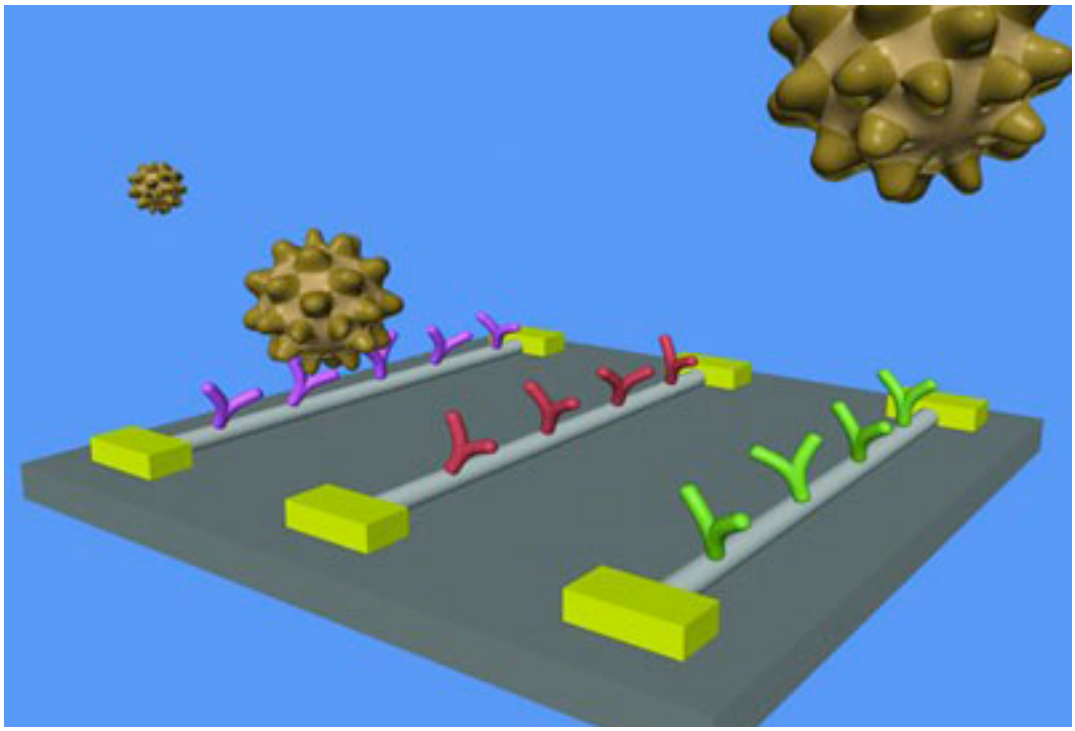

Fig. 3 Example of bio-nanosensors able to detect single viruses. It is an affinity-biosensor based on nanowires functionalized with antibody receptors [Patolsky,06].

The electrochemical bio-nanosensors referred to in this thesis are based on characterization of the current/voltage relationship and will exclude sensors that require light (e.g. surface plasmon resonance or fluorescence), use mechanical motion (e.g. quartz crystal microbalance or resonant cantilever), use magnetic particles, etc. A very interesting class of electrochemical bio-nanosensors, called ion-sensitive field-effect transistors (ISFETs), shows very promising performance. Such sensors rely on the interaction of external charges with carriers in a nearby semiconductor structure, thus exhibiting enhanced sensitivity at a low ionic strength, where counterion shielding is reduced [Schöning,06].

Electrochemical nanosensors can be further divided according to the measurement approach: voltammetry, amperometry or coulometry, and electrochemical impedance spectroscopy (EIS) are the main used readout techniques. Voltammetry and amperometry consist in measuring the current at an electrode as a function of the electrode-solution voltage applied. These approaches involve DC or pseudo-DC changes to the electrode conditions. Conversely, EIS measures the electrical impedance of an interface in AC steady state with constant DC bias conditions. That approach has been used

to study a variety of electrochemical phenomena over a wide frequency range and recently it has extended to biosensor applications.

Electrochemical bio-nanosensors find wide application in the fields of biology, medicine, and environment. Due to their low power, low cost, and miniaturized dimensions, they hold great promise in applications where minimizing size and cost is crucial. To date, some interesting applications are:

1- Genetic examination of diseases through DNA sequencing
2- Viruses detection in diagnostic applications
3- Sensing of blood, hormones, proteins, urine, and others in point-of-care applications
4- Drug testing and discovering in pharmaceutical research
5- Detection of bacteria in food industry applications
6- Detection of toxin and other agents in bio-warfare applications
7- Detection of pollutants nanoparticles in environmental monitoring
8- Water checking in ground water screening and ocean monitoring.

This chapter introduces the reader to bio-nanosensors from a system point of view. The first section reviews some of the foremost electrochemical bio-nanosensors that are: ion channels, solid-state nanopores, nanowires, and carbon nanotube. It briefly presents their physical structure as well as their working principles. Since this thesis work is focused mainly on electronic interface design, section two analyzes the principal readout techniques, while section three presents the potentiostat, which is the primary instrument employed in electrochemistry and bio-nanosensor field. Then, section four reports a former project working through biotechnology and microelectronics integration. The main outcome of this latter project is the developing of a novel hybrid technology for parallel recording of single ion channels. The developed technology offers promising opportunities in high throughput screening (HTS) applications, and it is the starting point of this thesis work.

1.1 Biosensing at Molecular Level

1.1.1 Ion Channels and Their Use as Biosensors

One cell is composed of many organelles surrounded by cytoplasm, a gelatinous fluid, enclosed by an external membrane (Fig. 4) [Hille,01]. This membrane is made of a double layer of lipids and hydrophilic phosphorus molecules called phospholipid bilayer, and protects the cell from the outside environment. To communicate with the external world, a lot of protein molecules are embedded in the cell membrane serving as channels for molecules or ions. There are hundreds of different kinds of ion channels and they are distinguished based upon their ion selectivity, gating mechanism, and sequence similarity. When active, the ion channel allows the ions passage across the membrane down to the channel thanks to an electrochemical gradient between the two solutions separated by the membrane.

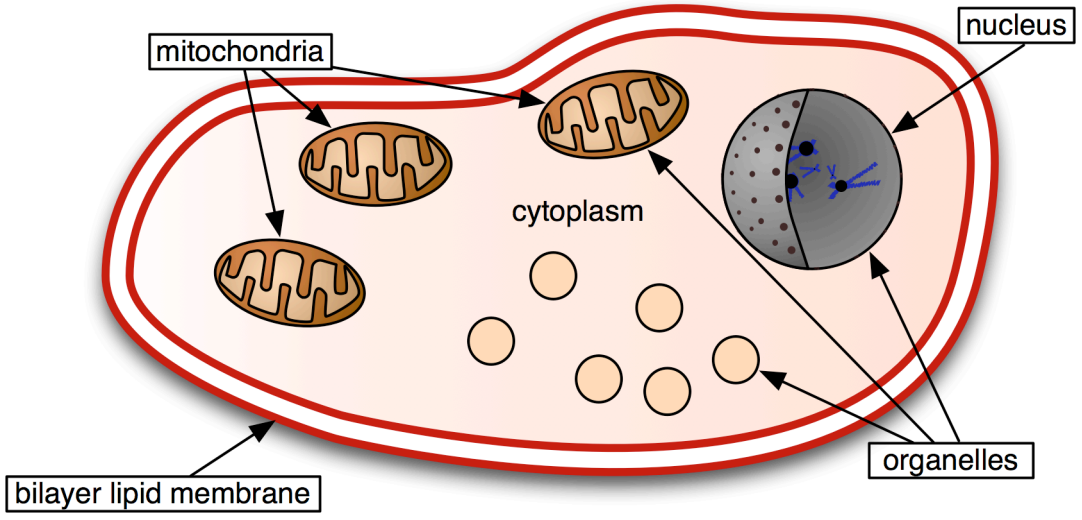

Fig. 4 Diagram of a cell showing internal organelles such as nucleus and mitochondria, the cytoplasm and the external bilayer lipid membrane.

Ion channels have a great importance in various physiological systems because they control the voltage potential across the membrane and regulate the ion current through the channel (they are mainly crucial in nervous and muscle systems) [Camerino,07], [Camerino,08], [Verkman,09]. At the same time, a wide variety of pathologies can affects the ion channels functionality damaging the cell [Ashcroft,06], [Clare,10]. For this reason, ion channels are

principal targets for drugs and they can be employed as natural sensors for molecular drug discovery. Indeed, parallel recording of single ion channels has becoming a primary technique for new drugs research, promising high throughput screening (HTS) capabilities with more than thousands compounds per day [Thei,11]. The basic idea is to create an array of ion channels, each one excited with a different molecule, where the monitoring technique could be manifold: based on fluorescence, on affinity binding, on current monitoring, etc [Sigworth,05], [Thei,10], [Thei,11].

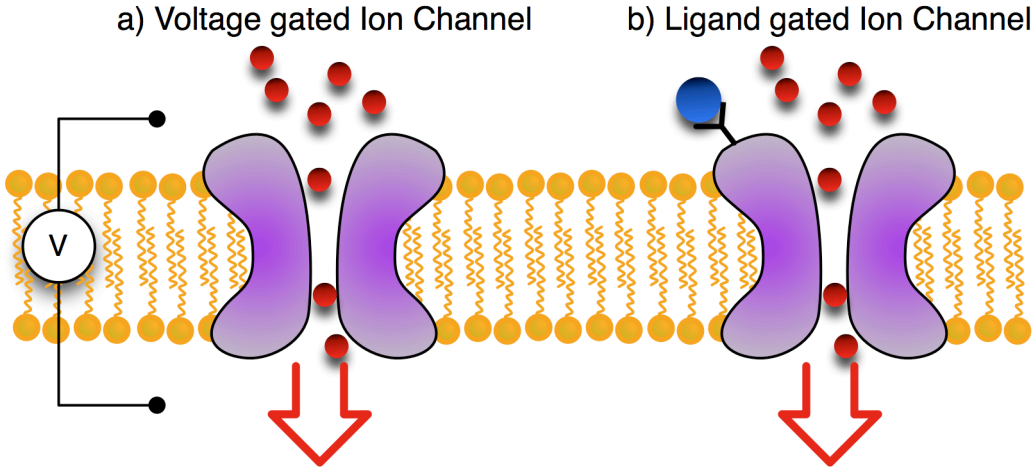

Fig. 5 Ion channels opens and closes in response of different gating mechanisms: a) Voltage gated ion channels opens when a voltage gradient is applied across the membrane; b) Ligand gated ion channels opens when a target molecule binds to a specific receptor.

Moreover, the ion channel sensing behavior inspires new ways for single molecules detection [Bayley,01]. Ion channels can open and close in response to different gating criteria: voltage gated, ligand gated, pH gated, or mechanically gated. Voltage-gated ion channels open or close depending on the voltage gradient across the membrane, while ligand-gated ion channels open or close depending on the binding of ligands to the channel receptor (Fig. 5). Therefore, it is possible to consider ion channels as biological devices capable of detecting single specific molecules in complex fluid mixtures like the blood. The integration of biological nanopores, such as ion channels, with electronics is a promising approach for the development of novel high-sensitive bio-nanosensors able to detect low concentrations of target molecules, or even identify alterations between different DNA bases.

Pioneering work on recording of single-ion channels started decades ago with electrophysiology experiments measuring the flow of ions through single pores in cell membranes [Sakmann,05]. In the 1990s, it was proposed

that it might be possible to use natural nanopores as sensors for DNA [Kasianowicz,96]. Bayley's research group at Oxford University has recently demonstrated single-base identification using an exonuclease enzyme and α-hemolysin (αHL) nanopores [Clarke,09]. Another interesting application of ion channels are single-molecule stochastic sensors, for identification and quantification of analytes, according to the conductance changes of the pores [Bayley,01].

To use the ion channel as bio-nanosensor it is necessary to artificially recreate the bilayer lipid membrane (BLM) embedding the pore. The standard patch-clamp setup is impractical because it uses a glass pipette attached to the membrane of the whole cell, and thus it monitors multiple ion channels [Sakmann,05]. However, the literature offers many different techniques for the creation of stable lipid membranes in artificial environment [Mach,08], [Poulos,09], [Thei,10]. In one possible setup, two reservoirs holding the solution are separated by a thin septum with a small hole. The BLM is then created on this aperture via Montal-Mueller technique [Thei,11]. This solution has proven to be successful mainly for pharmaceutical industry applications. In another technique, the BLM is made on a hole between two planar micro-channels demonstrating high bilayer stability and low electronic noise [Mach,08].

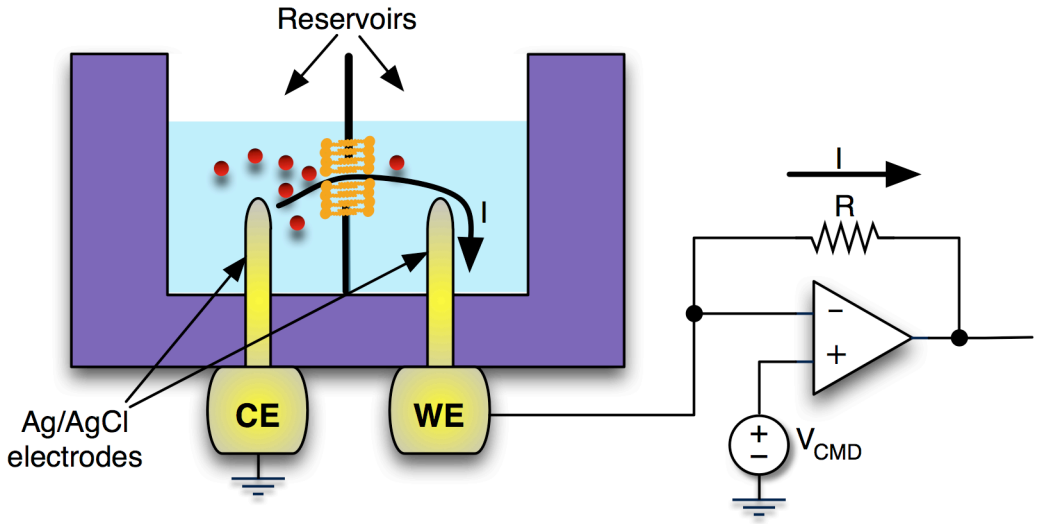

Fig. 6 Voltage-clamp approach applied to BLM artificially created following the method presented in [Thei,11]. The counter electrode (CE) fixes the solution in one reservoir to a reference voltage (i.e. ground) while the working electrode (WE) clamps the other reservoir to a command voltage (V_{CMD}) and monitors the current flowing through the membrane. Ag/AgCl electrodes are employed to convert ionic current into electron current.

Regardless the BLM formation, the electronic setup is rather standard and follows the voltage-clamp scheme of Fig. 6. The counter electrode (CE) fixes the solution in one reservoir to a reference voltage, while the working electrode (WE) clamps the other reservoir to a command voltage (V_{CMD}) and monitors the current flowing through the membrane. The used electrodes must be appropriate so as to convert the ion current into an electronic current; the most common are the silver/silver-chloride (Ag/AgCl) electrodes [Thei,11].

Current recording of single ion channels is challenging because it involves current signals in the pA range, or even below, and in the kilohertz bandwidth; thus the design of the low-noise electronic interface is crucial. For instance, sodium ion channels have typical conductance of 100pS, giving rise to currents in the order of 10pA when driven with 100mV, and involving a root mean square (rms) noise level smaller than 0.1pA at 1KHz [Sigworth,05]

1.1.2 Solid-State Nanopores

One nanopore can be generally defined as a small aperture in an electrically insulating material. It could be a hole in a synthetic material like the silicon or the graphene, or a pore-forming protein in a high electrical resistance lipid bilayer. The ion channels described in section 1.1.1 are indeed biological nanopores.

Even if biological pores have proven to be very useful for a wide range of interesting translocation experiments, they do exhibit a number of disadvantages such as fixed size and limited stability [Clarke,09]. The fabrication of nanopores from solid-state materials presents many advantages over their biological counterpart such as very high stability, control of diameter and channel length, adjustable surface properties and higher potential for easy integration into devices. However, they also exhibit unwanted effects such as extra noise [Smeets,06] and a large variability in pore conductance [Ho,05].

In the past few years, the main application for solid-state nanopores has been the measuring of individual DNA molecules translocation [Dekker,07]. The basic idea is straightforward (Fig. 7): an electrical field drives the DNA, which is a charged molecule, through the nanopore; then the DNA enters the

nanopore and occupy part of the liquid volume, reducing the total ionic current. Solid-state nanopores even demonstrated the translocation of double-strand DNAs and proved more extensive measurements using other monitoring techniques [Dekker,07].

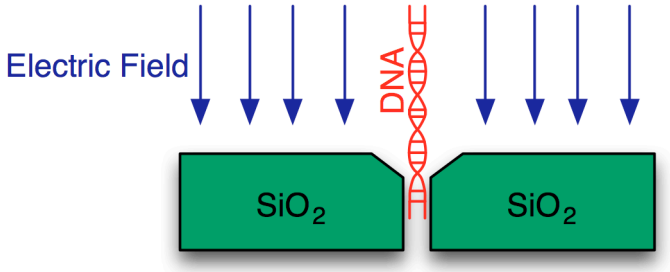

Fig. 7 Cross section of DNA translocation through a solid-state nanopore [Dekker,07]. The electric field drives the charged DNA through the nanopore in a controlled way. This is just the basic idea behind DNA translocation and many research groups proposed their own improvements [Dekker,07].

Recent advances in the fabrication of artificial membranes containing a single nanopore have generated a dramatic increase in the number of applications, thanks to the ability to substitute natural ion channels [Dekker,07].

1.1.3 Nanowires

One nanowire (NW) is a nanodevice characterized by two dimensions in the nanometer scale (i.e. the height and the width), while the other one (i.e. the length) could be in the range of tens to hundreds of micrometers. With such a high aspect ratio (length to width ratio of 1000 or more), the NW can be treated as a one-dimensional device. For ultra thin NWs, with diameters as small as three nm, quantum effects are very important, leading to many properties that are not seen in standard three-dimensional devices. For instance, the electrons become laterally quantum confined, thus they occupy discrete energy levels, leading to discrete values of the electrical conductance [Landauer,89]. However, NWs with such reduced dimensions are hard to physically realize.

Many NWs characteristics depend upon the fabrication process, which can be classified as either bottom-up or top-down. The former uses the self-organization concept and the molecular recognition to realize complex devices from simple nanocomponents, such as single molecules. This

approach provides high-quality materials but lacks of suitable techniques for accurate NWs alignment and electrical contact formation. The latter uses microfabrication techniques to cut, pattern, etch and shape bulk materials so as to reduce their lateral dimensions and realize the NW structure. These techniques are conventionally used in microelectronics facilities, thus they are well established and well controlled. Top-down approach allows realizing low-cost nanowires, but it reduces the lateral dimensions only down to 10 nm [Chen,09].

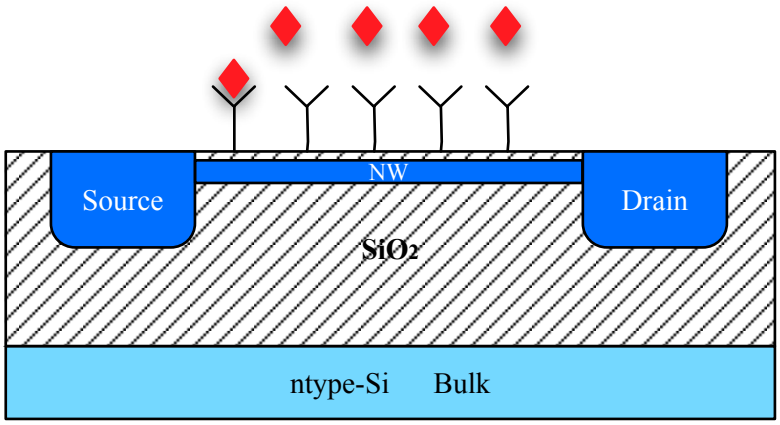

Fig. 8 Cross-section of a typical SiNW emphasizing the contacts and the surface functionalized with bio-detectors for viruses recognition.

There exist many different kinds of nanowires depending on the used material, including metal nanowires (e.g. NiNWs, AuNWs) and semiconducting nanowires (e.g. SiNWs, GaAsNWs). Silicon NWs (SiNWs), as well as carbon nanotubes, are very attractive for the development of future nanoelectronics, since they can be used to realize nanometers transistors and, at the same time, serve as connecting wires [Cui,03]. Moreover, SiNWs are very promising as label-free bio-nanosensors thanks to their extremely high surface-to-volume ratio and the extreme sensitivity of the carrier mobility to variations in the electric field; thus they can successfully work as field-effect transistor (FET) sensors [Wanekaya,06]. The surface of the NW, after a passivation stage, is functionalized using biomolecular receptors like antibodies [Patolsky,06]. Specific binding of biomolecules to the surface of the NW leads to depletion or accumulation of the carriers inside the nanodevice, modulating the source-drain conductance of the NW [Cui,01], [Patolsky,06]. Fig. 8 shows a cross section of a nanowire emphasizing the drain, source and bulk contacts, while the gate is functionalized with biodetectors.

Since the diameter of the NW is very thin, the depletion/accumulation of the carriers occurs in the whole device, while it takes place only in the surface region for a standard planar FET sensor. This feature of SiNWs provides sensitivity as high as necessary to detect single viruses [Patolsky,06]. Therefore, NWs functionalized with specific receptors promise to become the leading sensors for direct, high-sensitivity, label-free, real-time detection of biological end chemical species. Moreover, they offer an easy potential to be integrated in an array fashion so as to increase the number of concurrent testing, using different kinds of receptors [Gao,07], [Zheng,05], as well as the robustness of the detection, counteracting the false positive signals [Patolsky,06].

The first demonstration of the use of NW FET to sense analytes in solution occurred in 2001 with the sensing of pH concentration [Cui,01]. In the past years, the use of NWs has been widespread in many other applications, even demonstrating the possibility to detect single-stranded DNA molecules [Hahm,06].

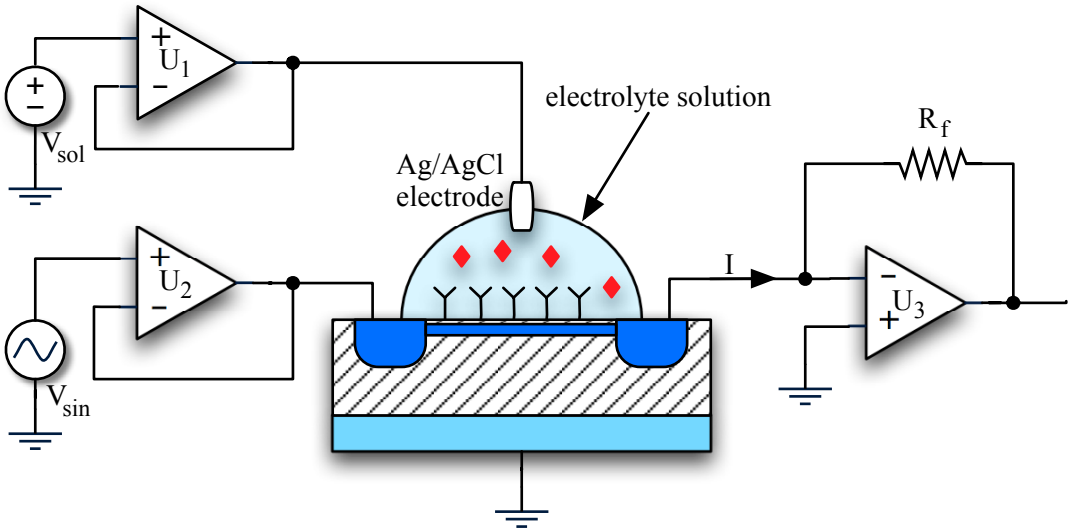

Fig. 9 Standard setup for NW readout. The buffer U1 fixes the potential of the electrolyte solution, while U2 provides the sinusoidal voltage stimulus and U3, in a transimpedance configuration, acquires the current flowing into the NW.

Since the biomolecules modulate the carriers concentration inside the nanowire, the straightforward readout technique is to monitor the conductance change. One standard setup for nanowire-based sensing is depicted in Fig. 9, where a phase-sensitive detection is implemented to achieve high SNR [Chen,09], [Kulkarni,12]. The electrolyte solution is kept at a constant voltage while a voltage sine wave is applied to the NW through

either source or drain contact, and the consequent current is read by a transimpedance amplifier.

Typical nanowire resistances are in the range of 100KΩ to 10MΩ, requiring current readout system less performing than natural ion-channels (the input-referred noise of the readout system is required to be less than 200fA/√Hz). However, the nanowire conductance, as well as its own noise power, strongly depends upon the fabrication process (i.e. doping, dimensions, impurities…).

1.1.4 Carbon Nanotubes

Others very promising nanodevices are the carbon nanotubes (CNTs), which are allotropes of the carbon with a nanometer cylindrical structure. They are usually classified as single-walled nanotubes (SWNTs) and multi-walled nanotubes (MWNTs). CNTs exhibit unique electrical, mechanical and chemical properties: 1) depending on their physical structure the carbon nanotubes can display either metallic or semiconducting behavior, leading to very interesting applications in the electronic industry; 2) they are the strongest and stiffest materials in terms of tensile strength and elastic module; 3) their conductivity is extremely sensitive to the surface, leading to highly sensitive nanosensors.

These properties make CNTs very attractive as bio-nanosensors, suggesting different sensing approaches [Burghard,04], [Wang,05]. CNTs can easily substitute for NWs in FET bio-nanosensor, where the conductivity of the nanosensor is modulated by the concentration of the analyte. Although pure CNTs are very sensitive to the surrounding environment, functionalization of the nanotube surface can be needed to increase the specificity of the bio-nanosensor [Burghard,04].

In another approach, CNTs can be used as electrodes in conventional electrochemical measurements. They substitute for glassy carbon electrodes and metal electrodes for amperometric analyte detection, showing better sensitivity and stability, high reproducibility, and fast response times [Burghard,04]. In this approach, CNTs can serve as either sensing elements, when they are employed without any kind of modification, or transducers, when they are modified with immobilized enzyme to improve sensitivity and selectivity [Wang,05].

Many CNT-based bio-nanosensors have been presented in the literature proving the ability to detect glucose [Deng,09], toxic gasses [Cho,09] and even DNA-hybridization [Sorgenfrei,11]. They are usually employed in amperometric measurements, where the voltage is fixed and the current is read [Burghard,04]. It is not easy to identify standard values for CNTs electrical parameters such as impedance, noise and bandwidth, since all these factors depend upon the specific CNT structure. However, CNTs are generally very noisy, suffering from a strong Flicker noise [Joo,11].

1.2 Electrochemical Measurements

Electrochemical measurements are consolidated investigation tools for fundamental and applied chemistry, and in the last few years they have also become key instruments in biotechnology research. For a detailed description of these methods some of the best resources are classic text books, such as [Bard,01] and [Bockris,98] for general electrochemistry, and [Macdonald,05] for electrochemical impedance spectroscopy. Electrochemical measurements are mainly used as standard characterization tools, redox probes, or a direct impedimetric transduction for biosensors [Lambrechts,92]. For an accurate classification of biosensing techniques the reader is referred to the specific literature [Thevenot,01]. In this section we will focus mainly on amperometric electrochemical measurements, which could be divided into three main classes: cyclic voltammetry, amperometry and electrochemical impedance spectroscopy.

1.2.1 Cyclic Voltammetry

Cyclic voltammetry is a non-linear, large-signal, I-V measurement [Bard,01]. The applied voltage is cyclically and linearly scanned over time (a triangular voltage wave is applied with a fixed slope called scan rate) and the instrument reads the output current. This is a consolidated electrochemical technique and many important electrochemical parameters can be extracted from the voltammogram (Fig. 10), such as the amplitude of current peaks, the voltage distance between peaks (one related to oxidation, and the other to reduction), and the formal potential of reactions. Increasing the scan rate it is also possible to investigate the kinetics of the reaction; indeed, at a scan rate

higher than the reaction rate constant, the I/V plot increases its hysteretic behavior. Standard cyclic voltammetry has typical scan rates ranging from 10mV/s to 10V/s. Such performances are easy to achieve with modern electronic instruments; however, integrated electronics techniques offer ultrafast measurements by means of scan rates in the order of 1MV/s, allowing us to explore electrochemical reactions in the nanosecond timescale [Carminati,09].

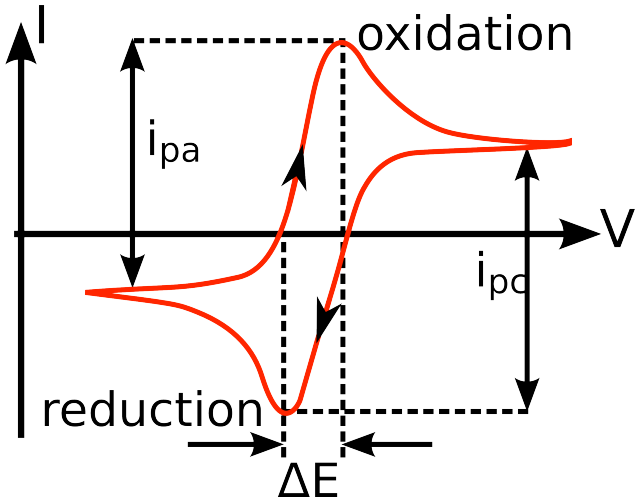

Fig. 10 Voltammogram. Kinetic and thermodynamic parameters could be extracted from this plot. Even if standard cyclic voltammetry can be performed by conventional electronics, ultrafast measurements enabling research in the nanosecond timescale require advanced electronics systems.

1.2.2 Amperometry

Amperometry is a time domain analysis applied to electrochemical interfaces and it is based on measurement of the current resulting from electrochemical reduction-oxidation of electroactive species. This measurement technique is usually done maintaining a constant potential at a counter electrode (CE) or an array of electrodes with respect to a reference electrode (RE), which may also serve as an auxiliary. Then, a step voltage is applied to the sample through working electrode (WE), where the instrument reads the ongoing current (Fig. 11). From the current measure one can acquire information about the electrons passed and thus get the concentration of the analyte.

Amperometry can be seen as a subclass of cyclic voltammetry, where the applied voltage is held constant. Indeed, the difference between the two techniques is mostly historic and related to the inability of reading a current

while the potential is scanned in earliest instruments. In modern electrochemistry, amperometry is mainly replaced by cyclic voltammetry but it has growing interest in bio-nanosensor applications such as DNA translocation or molecule detection using nanopores.

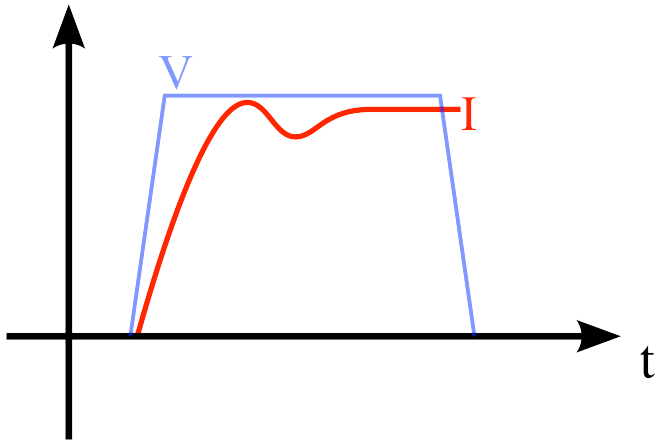

Fig. 11 Amperometric plot. This could be done by a DC or quasi-DC systems. It shows the current time tracking against an applied voltage step

1.2.3 Electrochemical Impedance Spectroscopy

Electrochemical impedance spectroscopy is a technique frequently used in microscopic analysis and solid-state investigation. It has proved less common than cyclic voltammetry in electrochemical experiments, but it is very powerful and is beginning to gain an important role in electrochemical analysis and biosensor applications, as well as in many other fields [Varlan,95]. This technique measures the impedance of the electrochemical cell over a range of frequencies, giving information about dissipative and energy storing phenomenon. EIS is able to give a global characterization of linear system dynamics by simply studying the transfer function and, similarly, it gives insight into non-linear systems providing a small signal equivalent model of the electrochemical cell. In another approach, the impedance or capacitance of the interface may be measured at a single frequency and tracked over time.

Electrical impedance is defined as the ratio of an incremental change in voltage to the resulting change in current (or vice versa) across the electrochemical system. More specifically, when applying a sinusoidal voltage reference

$$V_{REF}(t) = |V_{REF}| \sin(\omega_0 t) \tag{1.1}$$

across the system and assuming linear behavior, we expect the corresponding current to be

$$I(t) = |I|\sin(\omega_0 t + \theta), \tag{1.2}$$

where θ is the phase shift of the signal with respect to excitation (Fig. 12). The relationship between excitation and readout signals is the impedance Z of the cell and can be defined using phasors as

$$Z(j\omega) = \Re e(Z) + j\Im m(Z) = |Z|e^{-j\theta}, \tag{1.3}$$

where

$$\begin{aligned} |Z| &= \frac{|V_{REF}|}{|I|}, \\ \theta &= \theta(\omega). \end{aligned} \tag{1.4}$$

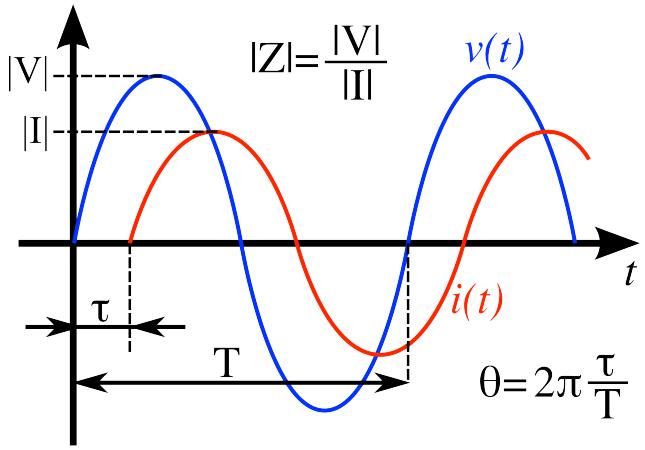

Fig. 12 Typical applied voltage to electrochemical cell (blue line) and related flowing current (red line). The delay between the two waves and the amplitudes ratio give information about the small-signal equivalent impedance of the cell.

Several approaches have been used so as to obtain the impedance measurement, such as AC bridge, transimpedance, and resonant sensing. By some of these techniques one can obtain the impedance plane plot, like the one illustrated in Fig. 13, giving comprehensive information about the impedance and its dependency on frequency. Fig. 13 shows a Nyquist plot referring to an electrode-electrolyte interface. The equivalent model of such a system is composed of an equivalent resistance for the solution (R_{SOL}), a small signal resistance (R_{CT}) modeling the charge transfer in redox reaction, a

double layer capacitance (C_{DL}) and the Warburg impedance (Z_W) accounting for the diffusion phenomenon that regulate mass transfer (Fig. 13)[1].

In bio-nanosensor applications the impedance of the electrode-solution interface changes when the biological probe captures the target analyte, which means that EIS system can be used to sense that impedance change. Impedance biosensors can detect a variety of target analytes by simply varying the biological probe used. As stated before, one modern application of impedance sensors relates to the class of nanosensors that detect very low concentrations of molecules. Impedance measurement does not require any special reagents and is the premier technique for "label-free" operations that are geared to detection without the use of molecular labeling [Daniels,07], [Katz,03], [Nikolelis,10].

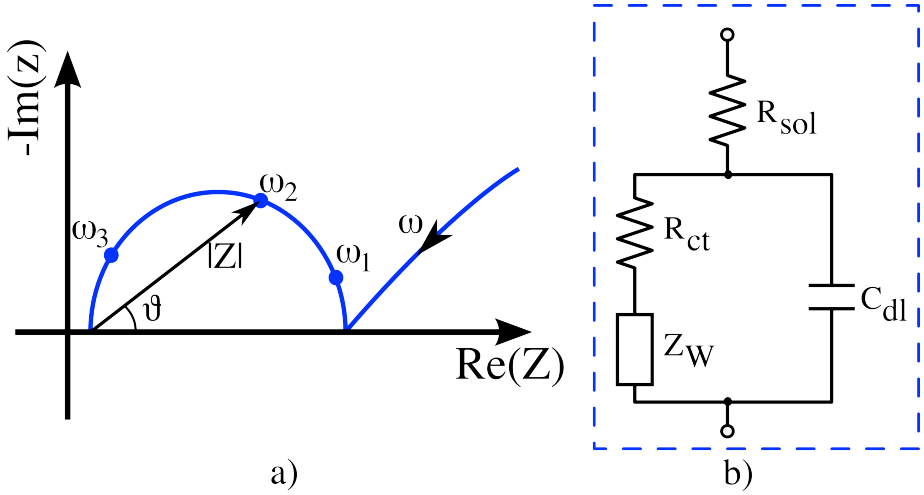

Fig. 13 Small-signal amperometric measurement using EIS: a) Impedance Nyquist plot of a classic faradaic process, showing the relationship between real and imaginary components, the modulus, and the phase of cell impedance Z. b) Electrode-electrolyte interface model corresponding to the Randles model [Bockris,98] illustrated in graph a).

Voltage excitation is usually employed in EIS systems because the most troublesome parasitic elements are in parallel with the measured electrode-solution impedance; however, as will be shown in a later section, excitation using current is also possible due to the reciprocity properties of the system. In impedance bio-nanosensors the voltage applied is usually quite small, typically 10mV of amplitude or less, for various reasons. First, the current-voltage relationship is linear only for small perturbations; second, probe layer perturbations should be avoided since covalent bond energies are in the order of few eV. If correctly performed, electrochemical impedance spectroscopy

[1] This model will be better explained in chapter 5 discussing water checking systems

does not damage the biomolecular probe layer, which is an important advantage over voltammetry or amperometry where larger voltages are usually applied.

1.3 Electronic Instruments

1.3.1 The Extended Potentiostat

The potentiostat is a very common instrument that enables amperometric electrochemical measurements [Bard,01], [Lauwers,01]. It is composed of a circuit that applies a controlled voltage across the electrochemical cell and a current amplifier that senses the corresponding current. The key feature of the extended potentiostat is that all the above mentioned amperometric measurements can be performed using different shapes of the control signal: large voltage control signals, such as a triangular wave, for cyclic voltammetry, DC voltage for amperometry, and finally a small sinusoidal signal for electrochemical impedance spectroscopy.

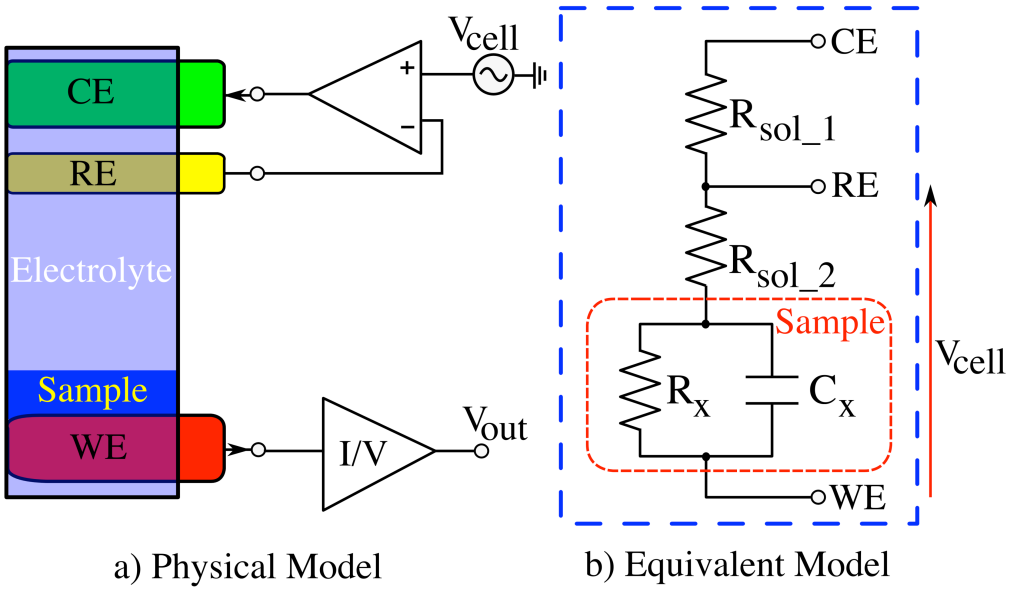

Fig. 14 The potentiostat approach: a) General scheme composed of voltage generator and current amplifier (I/V converter) arranged in a three-electrode configuration. b) AC equivalent model of the electrochemical interface.

A very general scheme of such an instrument is illustrated in Fig. 14, where it is arranged according to a three-electrodes configuration. The basic concept is to apply a known voltage across the electrochemical cell by a CE and

measuring the corresponding current flowing through the WE. The main problem is related to the potential across the electrodes, which could be unknown or dependent on several variables, such as the current itself. For the above reason a RE, with no current flowing, is introduced to sense the liquid potential. To this end, the RE is put in the negative feedback of an operational amplifier (U1), which drives the CE so that the potential of the solution is always kept equal to V_{REF}. A very small RE can be made and placed in proximity of the WE to better ensure the applied potential. In a slightly alternative configuration, the RE is fixed to ground and the WE is used for both voltage stimulation and current readout. If constraints on potential drops across the electrodes are not important, the three-electrode scheme depicted in Fig. 14 could be simplified into a two-electrodes one.

One important point that should be emphasized is that potentiostat characteristics are strictly related to the performance of both blocks of which it is composed: current amplifier and voltage buffer. On the one hand, the current amplifier is the key block for defining the resolution-bandwidth trade-off: research and trends on low-noise wideband current amplifiers can easily be mapped into new performances for potentiostats. On the other hand, the voltage buffer should be considered as an important block for setting the final resolution as well, since noise or interference affecting the RE are directly reflected in the measurement.

The integration of the entire potentiostat into a single solid-state chip has a great prominence in bio-nanosensor field, because it introduces many benefits:

1- Reduce stray capacitance due to interconnections and thus lower the noise [Bennati,09]
2- Enable the development of real-time, label-free, portable electrochemical sensing systems [Manickam,10]
3- Open the possibility of creating integrated array for high parallel acquisition [Levine,08] [Thei,11].

For the above reasons, the next chapters will show design examples of an integrated low-noise current interface (chapter 4) and an integrated EIS interface (chapter 5).

1.3.2 The Lock-in Technique

Integrated electronics allows one to shrink very sophisticated potentiostat structures into a tiny silicon chip using powerful analog and digital architectures. One possible potentiostat scheme implementing a two-electrodes EIS system is illustrated in Fig. 15. It is based on a lock-in technique, or phase sensitive detection technique, in order to obtain comprehensive information about the electrochemical impedance [Blair,75]. Assuming the current flowing into the cell given by (1.2) then the output voltage is given by

$$V_{OUT}(t) = R \cdot |I| \sin(\omega_0 t + \theta), \tag{1.5}$$

where R is the transresistance of the current-to-voltage amplifier.

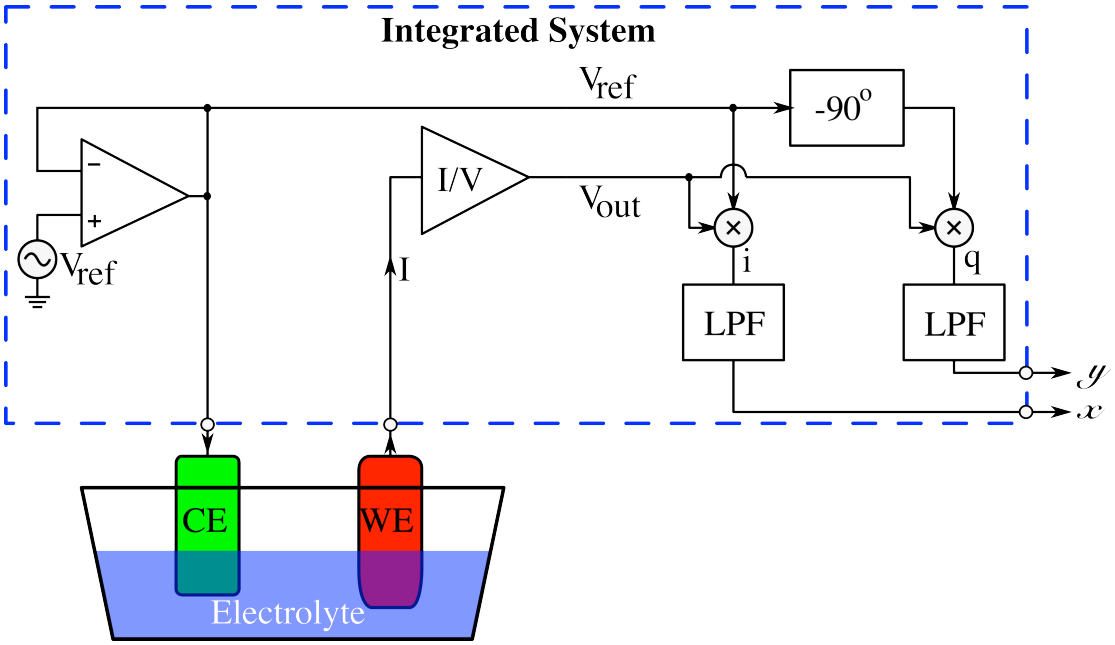

Fig. 15 EIS system following a two-electrodes approach and implementing a lock-in technique so as to recover comprehensive data about electrochemical cell impedance. The acquired current is converted into a voltage and then multiplied by the reference voltage and its 90 degrees shifted version, getting the in-phase and quadrature components of cell impedance. Lock-in algorithm can be implemented in either analog domain or digital domain.

Now, both voltages, V_{OUT} and V_{REF}, are fed into a phase-sensitive processing, where V_{OUT} is multiplied by the reference voltage and its 90 degrees shifted version, providing the in-phase signal (i) and the quadrature signal (q) as follows:

$$\begin{aligned} i &= V_{OUT}(t)\cdot|V_{REF}|\sin(\omega_0 t) = \\ &= R|I||V_{REF}|\cdot\frac{1}{2}\left[\cos(\theta)+2\cos(\omega_0 t+\theta)\right]; \end{aligned} \tag{1.6}$$

$$\begin{aligned} q &= V_{OUT}(t)\cdot|V_{REF}|\cos(\omega_0 t) = \\ &= R|I||V_{REF}|\cdot\frac{1}{2}\left[\sin(\theta)+2\sin(\omega_0 t+\theta)\right]. \end{aligned} \tag{1.7}$$

Both signals *i* and *q* have a DC component, proportional to *cos(θ)* in one case and to *sin(θ)* in the other case, and a high frequency component that will be removed by the low-pass filters (LPF). Thus, after the filtering we obtain:

$$x = \frac{R|I||V_{REF}|}{2}\cos(\theta) \propto \Re e\{Y(\omega)\}; \tag{1.8}$$

$$y = \frac{R|I||V_{REF}|}{2}\sin(\theta) \propto \Im m\{Y(\omega)\}. \tag{1.9}$$

The above two variables can be derived with high accuracy narrowing more and more the pass-band in the LPF [Carminati,09] and we can use them to compute the admittance *Y(ω)* by simple mathematics steps:

$$|Y(\omega)| = \frac{2}{R}\frac{\sqrt{x^2+y^2}}{|V_{REF}|^2}; \tag{1.10}$$

$$\theta(\omega) = \arctan\left(\frac{y}{x}\right). \tag{1.11}$$

It should be noted that this last processing operation could be performed in either analog or digital domain. With those little variations, the potentiostat of Fig. 15 can easily done any electrochemical measurement presented in section 1.2.

1.3.3 State of the Art

Since the voltage applied across bio-nanosensors is typically limited to a few tens of mV, the output current signal falls in the nA and pA range, resulting in the main instrumental challenge. Resolution requirements are more severe in the case of impedance sensing of interfaces with immobilized molecules where, due to the very poor conductivity, teraOhm and attoFarad

domain needs to be reached. At the same time, a wide bandwidth of DC-1MHz is fundamental for exploring extended spectral regions in EIS measurements. Moreover, tracking fast transients can offer deeper insights into essential charge exchange mechanism through the interface, mainly in cyclic voltammetry experiments.

State-of-the-art laboratory potentiostats are sophisticated and very well-engineered instruments, allowing most of the above cited measurements. They are employed in a wide range of electrochemical applications, ranging from corrosion studies and development of novel coatings, to fuel cells and biotechnology. However, they usually are bulky and expensive and cannot be employed for parallel recordings or used in portable and scaled implementations. Since they are mostly based on standard transimpedance amplifiers, they are all subject to the resolution-bandwidth trade-off and thus the signal bandwidth depends on the current range. Although the maximum bandwidth lies in the 1- 10MHz range, it is often reduced to the 10-100kHz range when switching to the more sensitive full-scale (10nA-100pA). The benchmark instrument for current sensing is the Axon amplifier [Axon,08]; it achieves a noise floor as low as 20fArms at 1kHz and it is designed for electrophysiology experiments, such as patch clamp techniques, where single-ion channel recordings from cell membranes are required. However, the instrument is big and needs a cooled head-stage to boost performance.

Most custom-designed, non-integrated potentiostats presented in the literature are designed for a wide range of applications, whose sensitivity is confined to the μA range [Angelini,06], [Huang,07], [Huang,09]. All the basic circuits proposed are specific for cyclic voltammetry or impedance measurements and do not allow execution of both kind of measurement.

Recently results on CMOS-integrated ultra low-noise current amplifiers have gained attention in the literature, fueling research on potentiostats. Although only few CMOS-based potentiostats explicitly allow multiple electrochemical measurements including EIS [Gozzini,09], there are many different implementations for potentiostat or potentiostat-like schemes reported in the literature.

M. Stanacevic et al. proposed a 16-channel potentiostat based on a low power current-mode delta-sigma modulator that reaches 100fA input-referred noise with a conversion time as long as 8s [Stanacevic,07].

A. Gore et al. achieved 50fA sensitivity with a semi-synchronous delta-sigma converter implemented in 42 channels for bio-wire molecular sensing [Gore,06].

Similar sensitivity is achieved in [Ayers,07], integrating the input current on a 50fF capacitor for 400ms that gives a current noise of 110fArms in 1kHz.

M. Ahmadi et al. started from a clear review of potentiostat topologies and then proposed an alternative potentiostat scheme based on current conveyors coupled with current-to-frequency converters for amperometric continuous blood glucose monitoring [Ahmadi,09].

A. Mason et al. realized a switched-capacitor version of a transimpedance amplifier with 100Hz bandwidth and 1pA resolution for a multiplexed array of amperometric biosensors [Mason,09].

M. Bennati et al. recently proposed a discrete-time current mode sigma-delta converter with resulting sub-pA current resolution in the 4kHz bandwidth, demonstrating parallel recordings of single molecule detection of bioengineered ion-channels. Often, discrete-time approaches provide limited bandwidth (from few Hz to few kHz) and cannot be employed for wide-bandwidth impedance measurements [Bennati,09].

By contrast, P. Weerakoon implemented a transimpedance amplifier for whole-cell planar patch-clamp applications providing good features for current time tracking: 10kHz bandwidth and 5pArms current resolution with a 25MOhm feedback resistor [Weerakoon,09].

M. Sampietro et al. have taken a big step forward in current amplifier research by using novel circuit architectures achieving resolutions of 1pArms and 20pArms in 100kHz and 1MHz bandwidth, respectively [Ferrari,09b]. By using such current amplifiers as frontends for potentiostats, they have achieved resolutions of 80zF, which is one of the best-ever performances for measurements using non-cooled headstages. However, the proposed amplifier is shot noise limited and thus the noise increases as well the input current increases [Carminati,09].

P. Levine et al. proposed a four-by-four active sensor array with all the electronic system and the electrodes integrated into one chip [Levine,08]. It included 16 potentiostats composed of dual-slope analog-to-digital converters (ADCs) with 550pArms resolution and 100Hz bandwidth, for cyclic voltammetry employed in real-time DNA detection. The system uses a two-

electrode configuration, with CE and WE realized as gold surface-electrodes by CMOS post-processing steps.

A. Manickam et al. implemented a ten-by-ten biosensor array in a $4mm^2$ integrated chip, in which each biosensor pixel is able to acquire signals in 10Hz÷50MHz frequency range [Manickam,10]. Again, the working electrodes are gold surface-electrodes realized by passivation openings on the top metal layer of the CMOS process, though the CE is external. The system senses the changes in electrode-electrolyte interface impedance due to biomolecular interactions reading the current coming from the biosensors. The i-th current is amplified and converted into voltage by a gain boosted common-gate amplifier, and then it is shifted into DC by two quadrature phase mixers produced by Gilbert-cells turning out an in-phase and quadrature signals, respectively.

It should be noted that results presented in the literature in this field are usually obtained using calibrated external sources to reduce noise effects. For real and autonomous biosensors it is important to implement voltage (or current) sources in the same device.

1.4 Parallel Recording of Single Ion Channels

1.4.1 Introduction

This thesis work started from a previous project about bio-nanosensors and, specifically, about integration between biology and electronics [Receptronics,11][2]. The target of that project was to develop low-cost, label-free biomolecular detectors by integrating concepts and methods from bio-nanotechnology and microelectronics. More specifically, the project aimed to design, fabricate, test and validate an hybrid technology by which biological self-assembling structures are interfaced with advanced electronic circuits for signal detection, amplification and conditioning [Crescentini,09], [Thei,11]. In this way, it exploited the strength of biotechnology to achieve a very high sensitivity and selectivity, as well as the great potential of microelectronics to address system miniaturization, low-power consumption, and low cost.

[2] "Receptronics" is a research project funded by the European Commission within the VI Framework Program under the Nanotechnologies and Nanosciences priority.

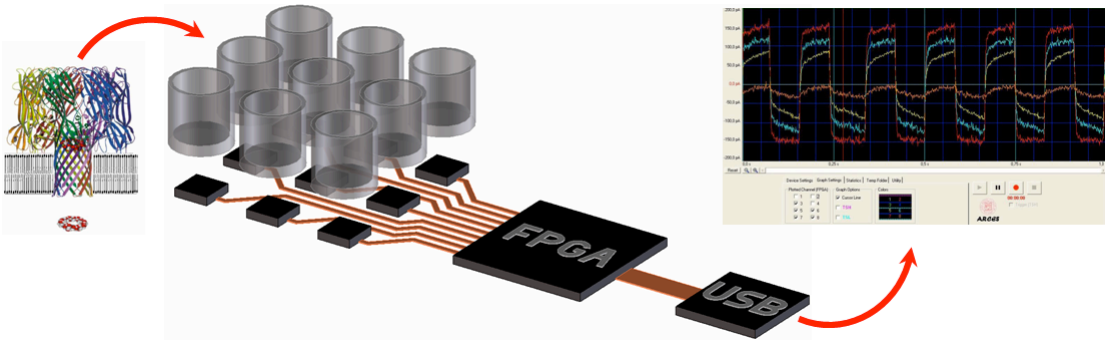

Fig. 16 Hybrid technology concept presented in *"Receptronics"*. Single ion-channes are embedded into artificial lipid membranes that are self-assembled in polymer structures strictly coupled to microelectronic systems for signal amplification and data processing [Thei,11].

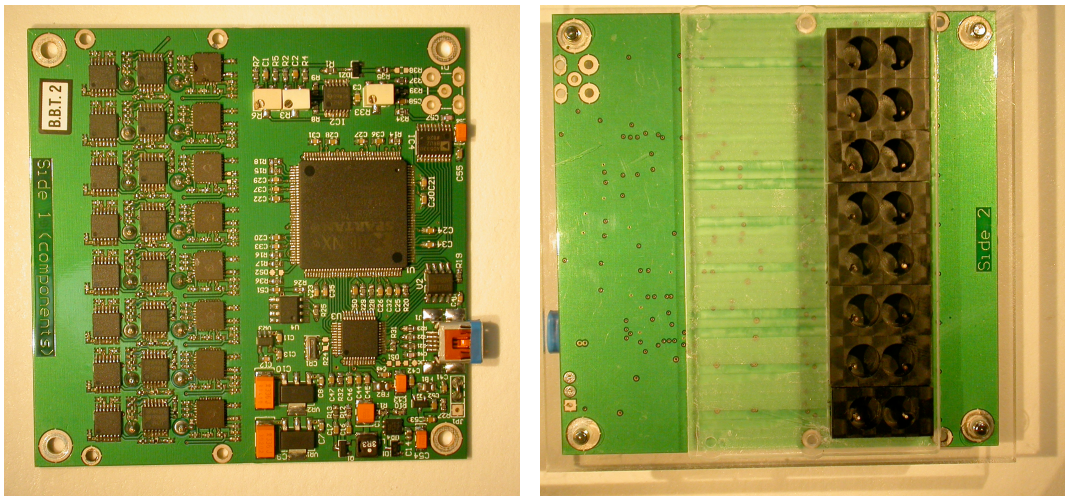

Fig. 17 Top and bottom view of the PCB embedding the overall system: microfluidic devices in the top side; IC current amplifier and FPGA in the bottom side.

Moreover, the resulting platform of this project was the workbench on which the noise model presented in chapter 2 was developed.

A straightforward concept scheme is presented in Fig. 16. The approach is based on arrays of independent and electrically addressable micro-cells where functional lipid bilayers are self-assembled. Membrane functionalization is determined by embedding bioengineered ion channels or receptors in the lipid bilayers to achieve highly specific interactions with target molecules. The array is organized so as to couple each electrochemical cell with a dedicated microelectronic interface detecting the current signal. Each IC amplifies and digitizes the signal following a delta-sigma algorithm so as to provide a one-bit data stream, which allows easy signal routing even in high dimension arrays. Then, a field programmable gate array (FPGA) acquires, filters and decimates all the digital signals and sends the data to a PC via USB

connection. One printed circuit board (PCB) embeds the overall system, both microfluidic and microelectronics; the former is placed on the topside and the latter on the bottom side (Fig. 17) [Crescentini,09], [Thei,11].

The system demonstrated both parallel acquisition from multiple ion channels arranged in array [Thei,10] and detection of single-molecule events with sufficient accuracy in a typical BLM experiment (Fig. 18) [Bennati,09]. The actual experiment yield using a Montal-Mueller protocol is around 50% [Rossi,10] but it is strictly related to the quality of the used microfluidic devices.

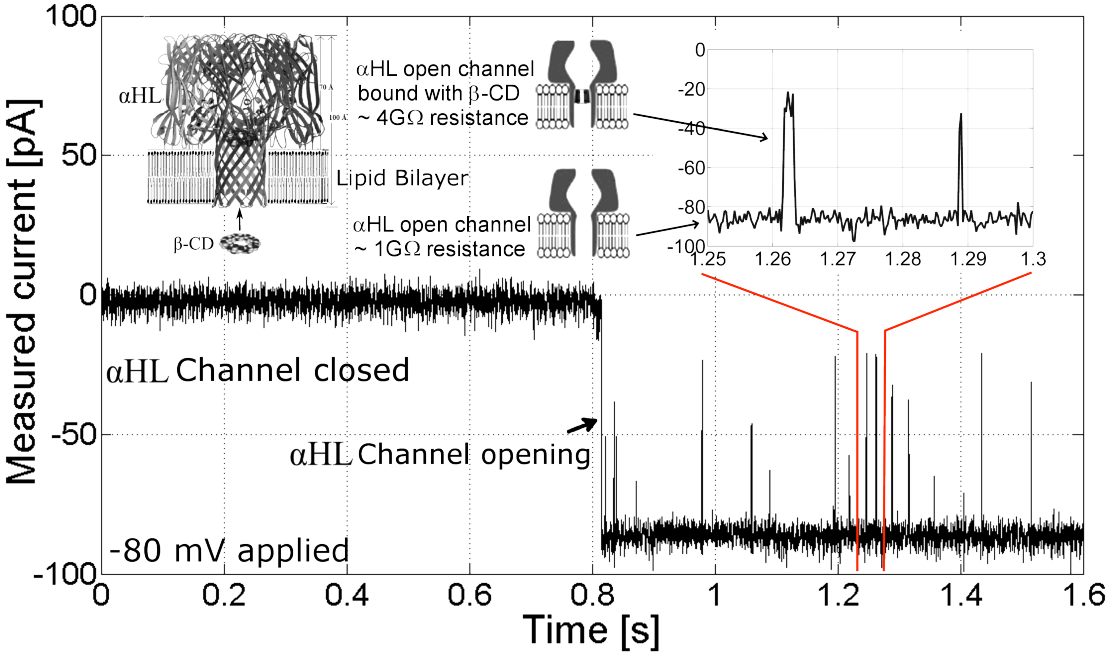

Fig. 18 Single molecule sensing using *"Receptronics"* approach with a sampling frequency of 2kHz and OSR equal to 512. Current spikes are due to Alpha Hemolisyn (αHL) pores, clogged by Beta Ciclodextrin (βCD) molecules.

1.4.2 Sub-pA Discrete-Time Current Amplifier[3]

The block scheme of the integrated electronic interface is shown in Fig. 19 and it is based on a discrete-time charge-sensitive amplifier (CSA) and a delta-sigma converter [Bennati,09]. The current amplifier periodically integrates the input current into a 100fF capacitance placed in shunt feedback to a single-ended operational amplifier (opamp), whose output reset value is previously stored by a correlated double sensing (CDS) scheme. In this way,

[3] This section gives just a short description about the developed IC, because it is made before the starting of my Ph.D. activity. The CMOS prototype is presented with more details in [Bennati,09].

the system is able to reduce low-frequency noise and offsets [Enz,96]. The signal is then transformed from single-ended to fully-differential, and converted into a 1-bit stream by a delta-sigma modulator.

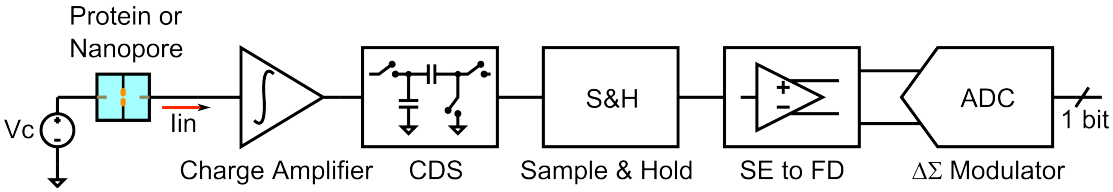

Fig. 19 Block scheme of realized discrete-time current amplifier. It is based on a periodically reset CSA, a CDS to lower the noise and a delta-sigma ADC.

Since typical signals coming from ion channels sensors are in the kHz bandwidth, a digital output stream in the MHz range is satisfactory. The use of oversampling brings key advantages compared with conventional ADC techniques:

1- Higher resolution due to reduced quantization noise. Larger number of equivalent output bits can be obtained with a reduced amount of power and required integration area;
2- Improved flexibility. Any data processing can be performed in the digital domain that is particularly useful to tradeoff SNR with bandwidth by means of oversampling ratio;
3- Simplified array readout. Single-bit output data simplifies the routing architecture for concurrent acquisitions.

A more specific schematic is shown in Fig. 20. A single-ended current integrator is followed by a correlated double sampling circuit, which helps to reduce flicker noise and offset, and also acts as a sample and hold circuit (S&H). The preamplifier integrates the input current for 120μs and then it is reset. The total sampling period of the CDS block is 128μs, limiting the bandwidth to about 4kHz.

During the reset phase, which is 8μs long, the digital signals *Φ1* and *Φ2* are high and the relative switches are closed. The charge amplifier is then reset and because the node *B* is connected to ground during the *Φ2* phase, both 4pF capacitors are charged to the initial opamp offset. Moreover, since *Φ1* opens about 6μs before *Φ2*, that offset also includes the charge injection from the reset transistors. After the reset phase, there is the integration phase lasting

for 120μs. During this phase, the charge amplifier integrates the input current and the second 4pF capacitor of the CDS maintains its initial value.

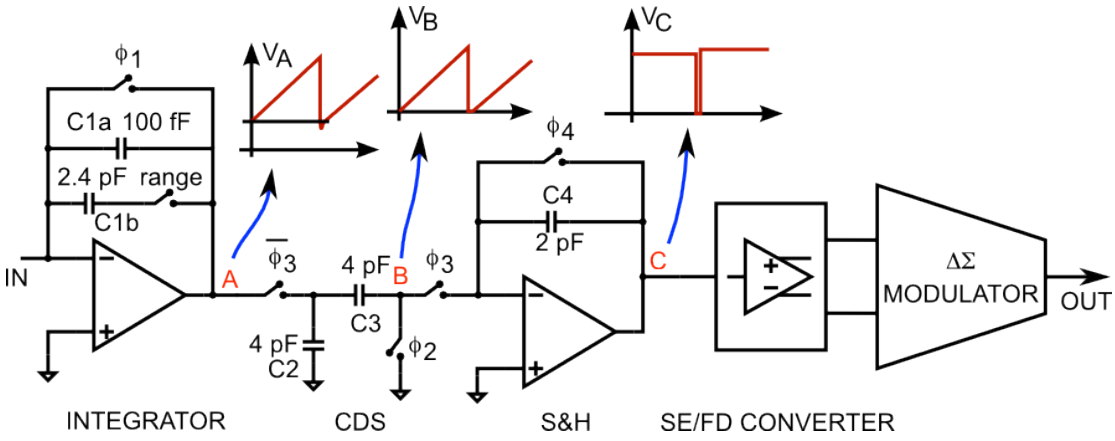

Fig. 20 Schematic of realized sub-pA discrete-time current amplifier.

Finally, there is the sampling phase. Digital signal *Φ4* commands the S&H reset and then *Φ3* orders the transfer of the charge from the two 4pF capacitors to the S&H. Since the two capacitors are now in series, the effective transferred charge Q_4 is given by the difference of the charge stored in each capacitor:

$$Q_4 = Q_2 - Q_3. \tag{1.12}$$

Therefore, the voltage at node *C* is the difference between the result of current integration and the initial offset. That potential, which remains constant for the next 128μs, is converted into a fully differential signal by a switched capacitor network controlled by non-overlapping digital signals (*Φ5* and *Φ6*). Afterwards, a first order delta-sigma modulator digitizes the signal generating a 1bit data stream. Both single-ended-to-fully-differential converter and delta-sigma converter work at clock frequency.

Using 240mV reference voltages and a clock frequency of 1MHz, the full-scale range can be set to 200pA or 5nA, depending on the integrating capacitor which can be selected by a switch. A microphotograph of the chip is shown in Fig. 21; it is implemented in 0.35μm technology occupying a total area of 0.83x0.62mm^2.

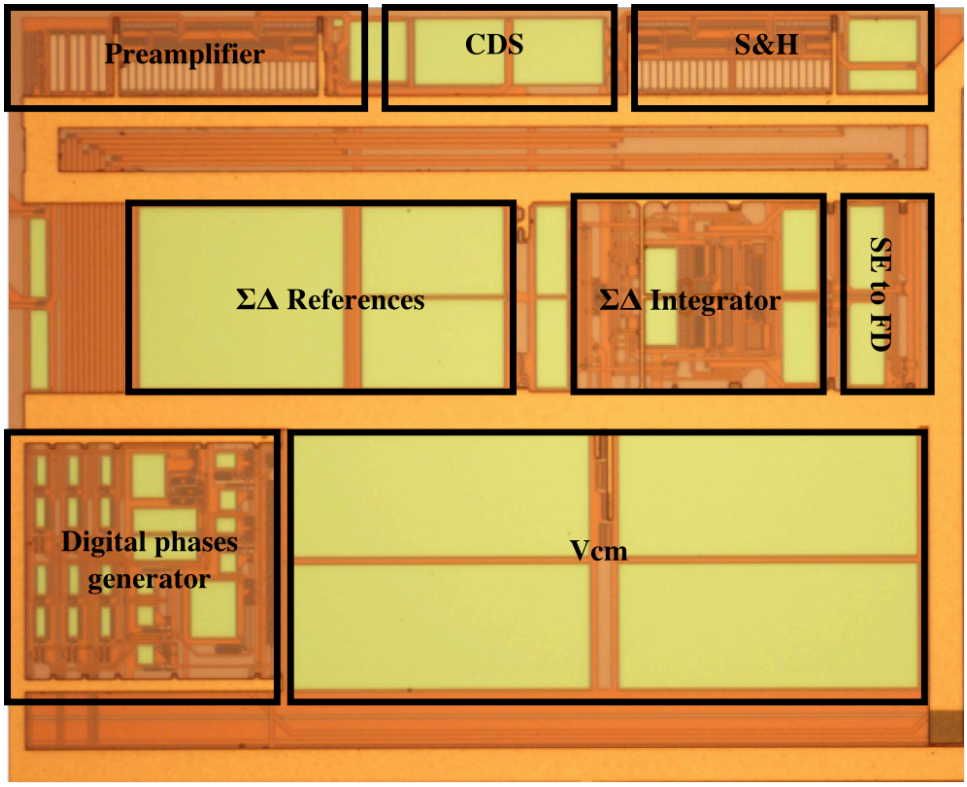

Fig. 21 Die microphotograph.

Chapter 2

Low-Noise Current-Sensing Approaches

Current-sensing readout is one of the foremost techniques used in bio-nanosensing, due to the charge-transfer phenomena occurring at the electrochemical interface. The development of novel nanodevices for biosensing determines new challenges for the interface design, especially when compact and efficient arrays should be organized.

This chapter reviews and analyzes noise limitations and trade-offs in current-sensing interfaces, with particular emphasis on integrated electronic design using CMOS technology. The chapter evaluates the general requirements on current interfaces made by main attractive bio-nanosensor, and then presents some of the most interesting interfaces. Starting from the classic transimpedance amplifier, the chapter presents, investigates and compares charge-sensitive amplifier architectures used in both continuous-time and discrete-time approaches. The most important papers, which recently appeared in the literature, will be discussed study cases and compared each other.

Current readout is a well-known technique widely used in electronic sensors such as radiation detectors, impedance spectroscopy interfaces and mechanical sensors. In the upcoming era of nanosensors, new opportunities are emerging in that field and new challenges are driving attention for the electronic design, especially on miniaturization and array arrangement issues. More specifically, current sensing is becoming one of the most useful readout

techniques for detecting signals from bio-nanosensors. Among them (ref. to chapter 1):

1- Ion channels
2- Solid-state nanopores
3- Nanowires based biosensors
4- Carbon nanotubes.

Another opportunity for current sensing comes from high throughput screening, which is the main application of massive electrophysiology. High throughput screening (HTS), employing either bilayer lipid menmbranes (BLMs) [Dunlop,08], [Zagnoni,09] or patch-clamp on-chip techniques [Fertig,02], is gaining a more crucial rule in screening drugs and medical compounds, thus stimulating the development of new low-noise CMOS current readout interfaces.

Additionally, current sensing is gaining more importance in electrochemical impedance spectroscopy, where voltage excitation is preferred because the most troublesome parasitic impedances are placed in parallel to the measured electrode-solution impedance. Electrochemical impedance spectroscopy (EIS) systems are suitable for studying a large variety of electrochemical phenomena over a wide frequency range and recently they are also used for biosensor applications [Levine,08], [Manickam,10].

Typical current signals in nanosensing applications are in the order of pA and in the KHz bandwidth. That means very low-noise electronic interfaces are required, with an input-referred root means square (rms) noise as low as hundreds of fA in the KHz bandwidth. For instance, sodium ion channels have a typical conductance of approximately 100pS, resulting in current in the order of 10pA when driven with 100mV (that is the typical voltage across the membrane of a cell[4]), and rms noise level smaller than 0.1pA at 1KHz [Sigworth,05]. The benchmark instrument for current sensing, the Axon Axopatch® 200B [Axon,08], is designed for electrophysiology experiments and achieves a noise floor as low as 25fA rms at 1KHz (0.7fA/$\sqrt{}$Hz until 1kHz).

[4] Note that for higher voltages applied on the ion channel, e.g. 1V, the lipid membrane can collapse.

As discussed in the first chapter, IC miniaturization offers a unique opportunity to shrink complex current-sensing architectures into silicon chips, whose main benefits are:

1- Lowering the noise due to reduction of stray and interconnection capacitances so as to achieve performances comparable with laboratory instruments
2- Possibility of arranging readout structures into compact arrays with applications in high throughput biosensing and chemical sensing.

Therefore, CMOS integration is necessary to realize complex, low-noise, high-parallel and cost-effective current-sensing interfaces for bio-nanosensor applications.

This chapter reviews the state of the art of integrated current-sensing interfaces based on CMOS transimpedance amplifiers, derives noise limits and trade-offs of the foremost architectures, and evaluates their ability to scale the dimensions in a design perspective. It analyzes and characterizes low-noise current readout systems highlighting constraints, limitations and design trade-offs. Section one reviews the fundamental concepts about noise in electronic systems and current-sensing interfaces. These concepts will be used in the following sections for a careful understanding of the noise performance in advanced interfaces based on a charge-sensitive amplifier. Furthermore, the section classifies current-sensing interfaces into two different families: continuous time (CT) and discrete time (DT). Sections two and three analyze some interesting schemes presented in the literature pointing out the design trade-off from the noise point of view. The former is focused on the CT approach and the latter is focused on the DT approach. Finally, section four compares the two approaches and analyzes the effects of the scaling process.

2.1 CMOS Current Amplifiers

2.1.1 The Transimpedance Amplifier

As examined in the first chapter, depending on the application and the bio-nanosensors employed, the readout interface has different requirements. On the one hand, ion channels require very low-noise current amplifiers with

bandwidth capability ranging from a couple of Hz to hundreds of KHz. On the other hand, silicon nanowires are noisier and demand slower interfaces, with useful bandwidths of not more than 20KHz. The choice of the proper electronic interface is crucial because it can affect the global performance. Ultra low-noise interfaces used with carbon nanotubes waste a lot of unnecessary power, and fast readout schemes with MHz bandwidths, employed in ion channel applications, have excessive noise. Therefore, the choice of the proper current-sensing interfaces is strongly related to the kind of bio-nanosensors. Table 1 summarizes typical values for noise, bandwidth and output impedance among bio-nanosensors referred to in this thesis, so as to aid proper decisions about readout interface.

Sensor Typology	Sensor Noise	Sensor Bandwidth	Sensor Impedance
Ion Channels	$\leq 6\text{fA}/\sqrt{\text{Hz}}$	10-100KHz	10-100GΩ
Solid-state Nanopores	$6\text{fA}/\sqrt{\text{Hz}}$	10-20MHz	400MΩ
Silicon Nanowires	$\geq 150\text{fA}/\sqrt{\text{Hz}}$	10-20KHz	10K-1MΩ
Carbon Nanotubes	10-20pA/√Hz	10-100KHz	0.1-20MΩ

Table 1 Review of main parameters for the interesting bio-nanosensors. Ion channels are characterized by very low-noise, appreciable bandwidth and extremely high output impedance [Fertig,01], [Mach,08], [Mayer,03]. Solid-state nanopores are more demanding since they achieve bandwidths in the MHz range and have lower impedances [Uram,08]. Silicon nanowires, as well as CNTs, show a great variance over the output impedance because they are strongly dependent on technology and realization process [Dawson,11],[Reza,06], [Stern,07]. Finally, carbon nanotubes are the noisiest sensors, suffering from a strong Flicker noise [Joo,11], [Sorgenfrei,10].

The foremost classic current readout scheme is based on the transimpedance amplifier (TIA) shown in Fig. 22, also known as the feedback ammeter. It is a current-to-voltage converter based on a resistive feedback operational amplifier (opamp); its DC output voltage is given by

$$V_{OUT} = -R_F \cdot I_{IN}, \tag{2.1}$$

where R_F is the feedback resistance and I_{IN} is the input current. That scheme takes full advantage of the operational amplifier working in the linear region [Keithley,98]:

1- It lowers the voltage burden thanks to the "virtual short principle".
2- It reduces the dependency of the output voltage to opamp parameters thanks to the feedback approach.
3- It improves the measure accuracy thanks to the negligible current flowing into the gate of the input pair (if a CMOS opamp is implemented).

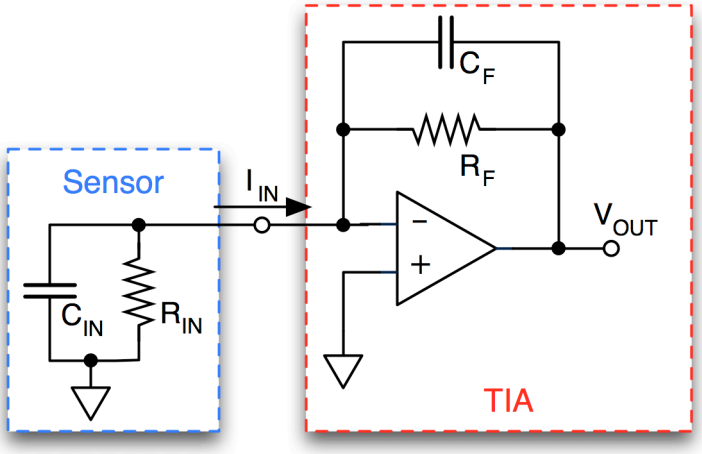

Fig. 22 Schematic of the classic transimpedance amplifier along with the equivalent model of the sensor output. TIA is the simplest current-sensing scheme but it needs high-value feedback resistor to meet low-current and low-noise requirements. Unfortunately, the high resistor is hard to integrate and limits the bandwidth due to the presence of unavoidable parasitic capacitances.

To cope with extremely low currents coming from some kinds of bio-nanosensors, feedback resistance should be very high. For instance, assuming an output full-range of 1V, 1GΩ resistance is needed to read 1nA full-scale input current. Although these resistors are on the market, it is very difficult to integrate them into a CMOS silicon chip. Moreover, discrete resistors have unavoidable stray shunt capacitance C_F that creates a low-pass filter and thus strongly restricts the bandwidth, as clearly shown by the complete transfer function:

$$V_{OUT} = -\frac{R_F}{1 + j2\pi f R_F C_F} I_{IN}. \tag{2.2}$$

2.1.2 Noise in Current-Sensing Interfaces

A generic current-sensing system shows an input-referred noise power $\overline{i_{IN}^2}$ that is given by:

$$\overline{i_{IN}^2} = \overline{i_D^2} + \overline{i_N^2}, \tag{2.3}$$

where $\overline{i_D^2}$ is the noise power spectrum density (PSD) related to the nanodevice, usually composed of both thermal and $1/f^{\alpha}$ components, and $\overline{i_N^2}$ is the PSD related to the electronic interface. Equation (2.3) is appropriate because device-under-test (DUT) and electronic readout are two uncorrelated noise sources, although there is a relation between the sensor output impedance and the input-referred noise of the interface.

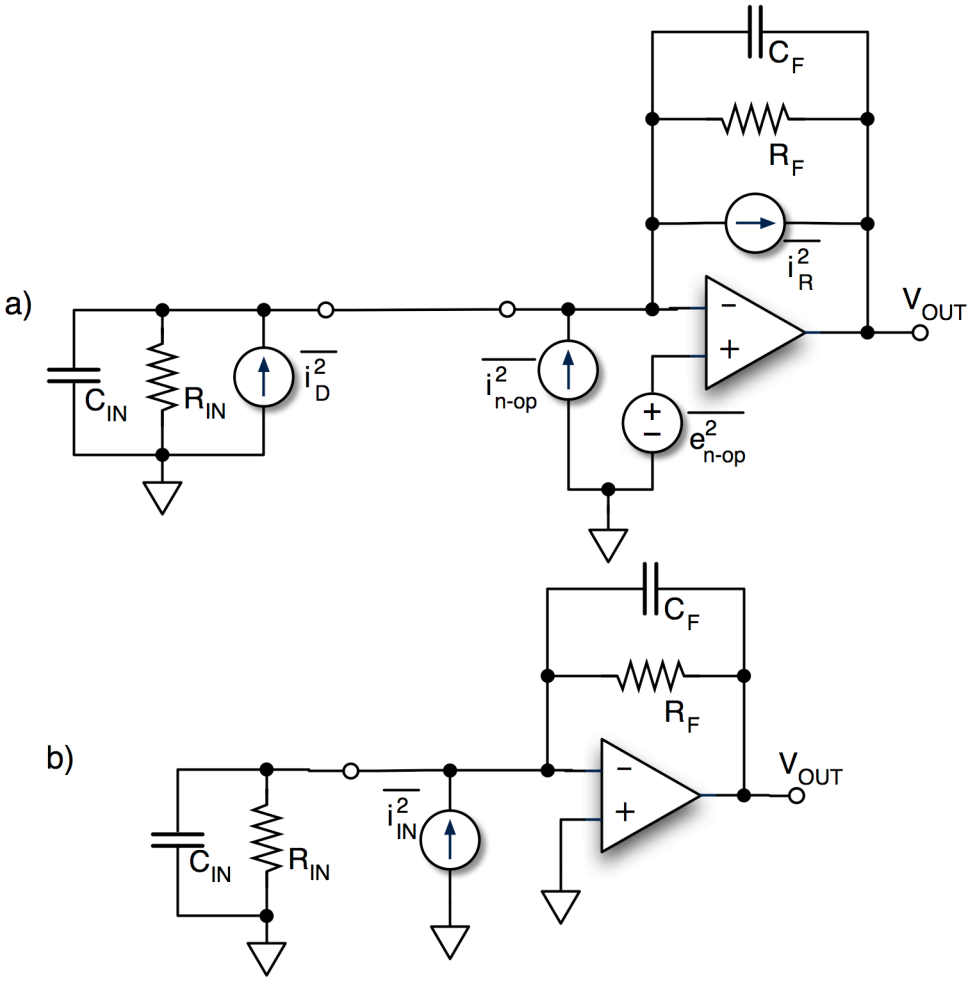

Fig. 23 a) Schematic of bio-nanosensor and TIA highlighting all the noise sources. $\overline{i_D^2}$ is the equivalent noise current generator of the DUT, $\overline{i_{n-op}^2}$ and $\overline{e_{n-op}^2}$ represent the noise generators of the opamp and $\overline{i_R^2}$ is the equivalent noise current generator of the feedback resistor. b) Schematic of bio-nanosensor and TIA with an equivalent input-referred noise current generator $\overline{i_{IN}^2}$ taking into account of all the noise sources referring at the input node.

More precisely, TIA has two uncorrelated noise sources (Fig. 23), the feedback resistors and the operational amplifier; hence the input-referred

noise power is a combination of both, which is easily calculable exploiting the "superposition theorem". The resistor noise $\overline{i_R^2}$ and the current noise generator $\overline{i_{n-op}^2}$ of the opamp can be directly referred to the input as:

$$\overline{i_{N1}^2} = \overline{i_R^2} + \overline{i_{n-op}^2} = \frac{4kT}{R_F} + \overline{i_{n-op}^2}, \tag{2.4}$$

where k is the Boltzmann constant and T is the temperature in Kelvin degrees. More mathematical steps are needed so as to refer the voltage noise generator $\overline{e_{n-op}^2}$ of the opamp to the input. Taking into consideration Fig. 23, the output noise PSD due to $\overline{e_{n-op}^2}$ can be expressed as

$$\overline{v_{on}^2} = \overline{e_{n-op}^2}\left|1 + \frac{Z_F}{Z_{IN}}\right|^2, \tag{2.5}$$

where Z_F is the feedback impedance

$$Z_F = \frac{R_F}{1 + j\omega R_F C_F}, \tag{2.6}$$

and Z_{IN} is the input impedance (i.e. the sensor impedance)

$$Z_{IN} = \frac{R_{IN}}{1 + j\omega R_{IN} C_{IN}}. \tag{2.7}$$

Substituting (2.6) and (2.7) into (2.5) follows

$$\overline{v_{on}^2} = \overline{e_{n-op}^2}\frac{\left(R_{IN} + R_F\right)^2 + \omega^2 R_F^2 R_{IN}^2 \left(C_F + C_{IN}\right)^2}{R_{IN}^2\left(1 + \omega^2 R_F^2 C_F^2\right)}. \tag{2.8}$$

Equation (2.8) shows the dependency of the noise on the input impedance, demonstrating the following points:

1- At low frequency the noise is related to the resistance ratio, minimized for high R_{IN};
2- At high frequency the noise is related to the capacitance ratio, minimized for low C_{IN}.

As illustrated in Table 1, high output resistance characterizes the majority of bio-nanosensors, thus we can approximate (2.8) by:

$$\overline{v_{on}^2} = \overline{e_{n-op}^2}\frac{1+\omega^2 R_F^2\left(C_F+C_{IN}\right)^2}{\left(1+\omega^2 R_F^2 C_F^2\right)}. \tag{2.9}$$

In the following sections we will always neglect R_{IN}, without any effect on our analysis and considerations. In cases where the sensor resistance cannot be neglected, (2.8) is used instead of (2.9) and the results are analogous. Now, dividing (2.9) by the TIA transfer function squared (2.2), we get the input-referred noise related to $\overline{e_{n-op}^2}$:

$$\overline{i_{N2}^2} = \overline{e_{n-op}^2}\left[\frac{1}{R_F^2}+\omega^2\left(C_F+C_{IN}\right)^2\right] = \overline{e_{n-op}^2}\left[\frac{1}{R_F^2}+\left(2\pi f\right)^2\left(C_F+C_{IN}\right)^2\right]. \tag{2.10}$$

The total input-referred noise PSD of TIA is given by the sum of (2.4) and (2.10):

$$\overline{i_N^2} = 2qI_{IN}+\frac{4kT}{R_F}+\overline{e_n^2}\left[\frac{1}{R_F^2}+\left(2\pi f\right)^2\left(C_F+C_{IN}\right)^2\right], \tag{2.11}$$

where $2qI_{IN}$ is the shot noise of the input devices in the case when we are using BJT transistors, and C_{IN} takes care of both sensor output capacitance and stray capacitances placed on the input node of the electronic interface. Thus, the input-referred noise PSD of the interface is given by the sum of three terms. The first one takes into account the shot noise of the input transistors in the case of either a BJT-based or a JFET-based operational amplifier. The second one is the resistor current noise, revealing that a high value resistor is mandatory even for low-noise acquisition. For instance, 1GΩ resistor determines a noise current of 4fA/√Hz, which is acceptable in some applications. Finally, the third term relates to the opamp voltage noise source and expresses the dependency on sensor impedance.

CMOS technology offers the advantage of a negligible shot noise term[5] at the expense of greater contributions of low-frequency noise with respect to BJT and JFET. More specifically, the expression for input-referred noise voltage power in CMOS opamp is given by:

[5] For a CMOS opamp the equivalent input-referred noise current generator $\overline{i_{n-op}^2}$ has no shot noise; moreover it is completely correlated with the noise voltage generator by means of the input admittance ωC_{GS}, which is very poor allowing us to neglect the contribution of the noise current generator.

$$\overline{e_{n-op}^2} = \frac{16kT}{g_m} + \frac{2K_F}{C_{OX}WL} \cdot \frac{1}{f}, \tag{2.12}$$

where g_m is the transconductance of the MOS input pair, W and L are the width and length of a single input device, K_F is the flicker noise coefficient and C_{OX} is the oxide capacitance per unit area [Gray,01], [Razavi,01]. One BJT-based opamp is intrinsically less noisy because it is characterized by higher transconductance and lower flicker coefficient, but it has an unavoidable input current directly affecting the measure and introducing a shot noise term. As a result, the CMOS substrate is a good trade-off, offering a strong and cheap technology integrating complex mixed-signal system. That statement is very important to compare the results shown in this chapter with results from other current-sensing implementations. For extremely low-noise interfaces, other technologies are more appropriate, such as Bipolar-CMOS (BiCMOS), silicon-on-insulator (SOI) or JFET-CMOS processes; however, they all are more expensive, and occupy more space due to longer minimum channel length.

2.1.3 Integrator-Differentiator Scheme

From here on we will assume a CMOS realization for the TIA and thus the input-referred noise PSD becomes:

$$\overline{i_N^2} = \frac{4kT}{R_F} + \overline{e_n^2}\left[\frac{1}{R_F^2} + \left(2\pi f\right)^2\left(C_F + C_{IN}\right)^2\right]. \tag{2.13}$$

That equation shows a low frequency noise floor set by R_F and an asymptotic increase for frequencies greater than a corner point given by the equality of both terms in (2.13) (Fig. 24). It is clear that the total noise power will decrease for higher R_F, achieving an optimum for infinite feedback resistance (Fig. 24). In the last case, the TIA becomes a charge-sensitive amplifier (CSA) where the output voltage is equal to the integral of the input current:

$$v_{OUT}\left(t\right) = -\frac{\int_0^t i_{IN}\left(\xi\right)d\xi}{C_F}; \tag{2.14}$$

$$V_{OUT} = -\frac{1}{j2\pi f C_F} I_{IN}. \tag{2.15}$$

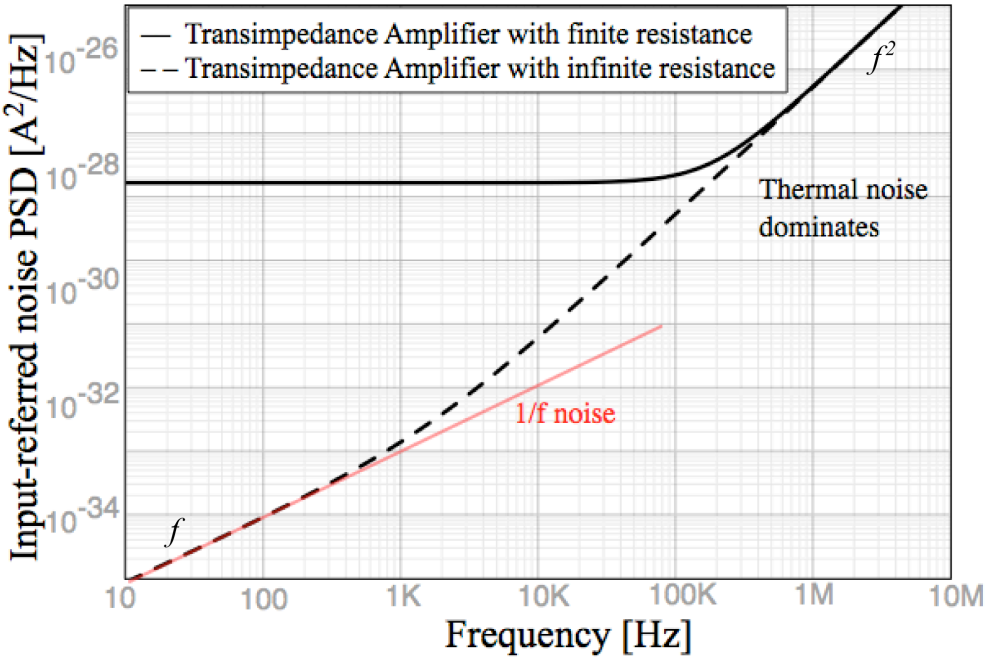

Fig. 24 Input-referred noise power spectrum for standard TIA with finite feedback resistance R_F=1GΩ (solid line) and infinite feedback resistance (dashed line); in both cases the total capacitance facing to the input is set C_T = 1.2pF. The graph refers to a low-noise opamp described by a thermal noise voltage about 3nV/√Hz.

Equation (2.13) shows how to improve signal-to-noise ratio:

1- Avoid feedback resistance in favor of charge-sensing approaches;
2- Reduce input capacitance as much as possible.

In any case, (2.13) demonstrates that the miniaturization of the electronic interface and of the related routing has a dramatic impact on the noise reduction, due to C_{IN} decreasing. Additionally, the miniaturization of the system also has a great effect on the nanosensor noise [Uram,08].

The above directions indicate CSA as the best solution for low-noise current sensing, regardless of the technology employed; however, CSA suffers from saturation because it integrates the current over time. To cope with that issue two techniques are followed:

1- **Continuous-Time approach**: it employs low-noise active feedback to set the bias point and prevent the opamp saturation (Fig. 25-A).

2- **Discrete-Time approach**: it periodically resets the charge stored into the feedback capacitance (Fig. 25-B).

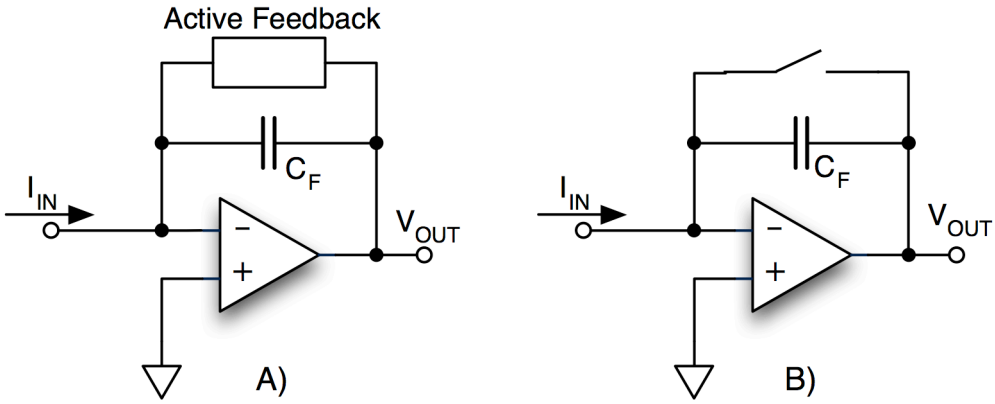

Fig. 25 Implementations of transimpedance amplifier based on charge-sensitive amplifier. A) CT approach using an active feedback to set the bias point and avoid saturation; however the feedback adds extra noise. B) DT approach using a periodically reset to discharge the feedback capacitance and thus prevent saturation; however it is prone to charge injection and kTC noise.

These approaches have a lower input-referred noise PSD with respect to TIA scheme, but they still introduce deviations from ideal CSA behavior, such as incomplete elimination of thermal noise floor in the former case, or charge injection and kTC noise in the latter.

In both cases the output voltage is proportional to the integral of the input current and thus a subsequent derivation step is needed so as to recover the signal. That architecture, usually known as integrator-differentiator scheme, also allows us to neglect the Flicker noise of the first opamp thanks to the derivative step, as shown in Fig. 26.

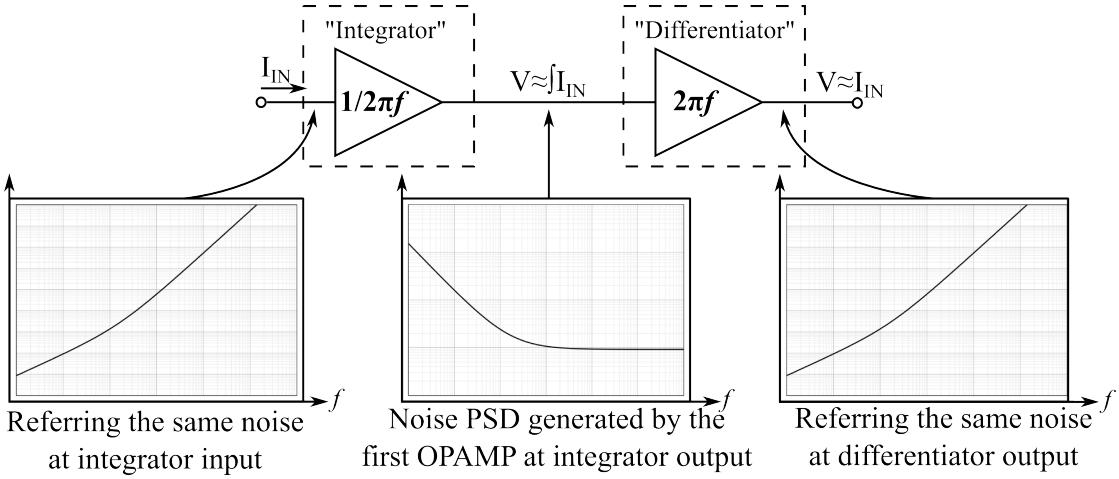

Fig. 26 The noise generated by the first opamp presents different PSD shapes with respect to the node to which is referred. At the integrator output the noise PSD shows a *1/f* behavior at low frequency and a flat behavior at higher frequency. Referring this noise at both integrator input and differentiator output, the shape of the PSD changes, rising with f at low frequency and with f^2 at high frequency.

2.2 Continuous-Time Approach

2.2.1 Resistive Feedback

The most straightforward scheme for continuous-time approach is the TIA itself. Although we have discussed TIA in the previous section, there are some interesting solutions to review in the literature.

A recent paper shows how input-referred noise as low as 1.9fA/$\sqrt{}$Hz, up to a few hundred hertz, could be achieved with bipolar technologies even if one uses discrete components [Ciofi,06]. However, the high resistor value required is not suitable for VLSI implementation and arrays of nanosensors.

A more interesting architecture using the classic TIA approach is presented in [Weerakoon,09], where an integrated patch-clamp system is proposed. The resistor integration problem has been solved using a silicon-on-sapphire (SoS) technology, which offers the capability of implementing high feedback resistances with reduced parasitic capacitances (thanks to the non-conductive substrate, an integrated 25MΩ resistor can be implemented in SoS technology [Weerakoon,09]). Due to the SoS improvements it lowers the input-referred noise floor to 5pArms in 10KHz bandwidth (50fA/$\sqrt{}$Hz). SoS technology has been proven to be a very good solution for low-noise current sensing; however, it is not frequently used in analog design because it is quite expensive.

2.2.2 Active Feedback

A very interesting solution for current interfaces employing CSA in a continuous-time approach is presented in [Ferrari,07] and [Ferrari,09], where a low-noise active feedback spills out the input DC current to prevent opamp saturation. A basic scheme of the idea is presented in Fig. 27. The amplifier *H(s)* in the active feedback is characterized by high gain at very-low frequencies and high attenuation at higher frequencies. In this way, the feedback is strong enough so as to redirect the input DC current into R_{DC}, keeping the band of interest unaffected [Carminati,09].

However, R_{DC} should be very high to keep the input-referred noise low. Therefore, the high value resistor in the feedback network is implemented by

active bidirectional attenuators based on a matched-MOS scheme, where the MOS devices work in sub-threshold region [Gozzini,06] (Fig. 28).

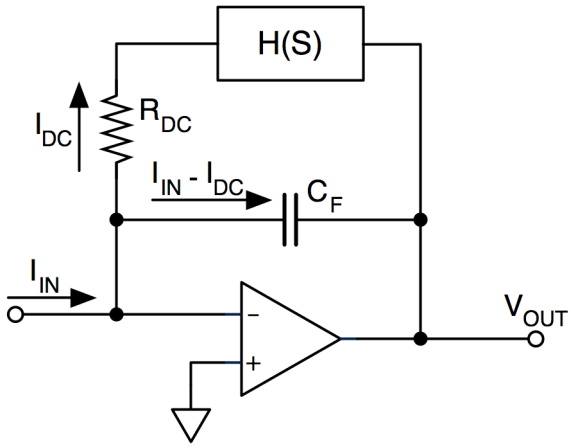

Fig. 27 Schematic of CT current-sensing scheme presented in [Ferrari,09]. The circuit avoids the opamp saturation thanks to the active feedback that spills out DC current from the input node. The amplifier *H(S)* is design so as to have high gain at low frequency (quasi-DC) and strong attenuation at higher frequency; sinking only the DC input current. However, the active feedback is a further source of noise.

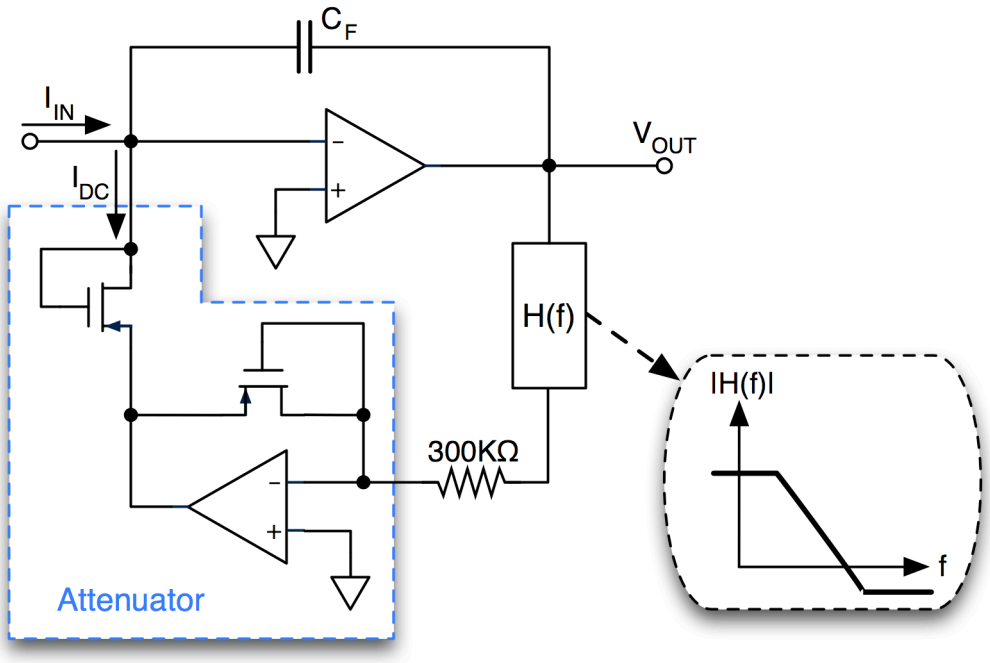

Fig. 28 To minimize the noise, resistance R_{DC} of Fig. 27 should be very high. In [Ferrari,09] the high value resistor is implemented using a 300KΩ resistor and an active bidirectional attenuator [Gozzini,06].

From a noise point of view, the input-referred noise can be estimated as

$$\overline{i_N^2} = \frac{4kT}{R_{DC}} + \overline{i_{MOS}^2} + \left(2\pi f\right)^2 \left(C_F + C_{IN}\right)^2 \cdot \overline{e_{n-op}^2}, \tag{2.16}$$

where R_{DC} is the equivalent resistance seen from the input node through the active feedback, $\overline{i_{MOS}^2}$ is the shot noise generated by diode connected transistors in the attenuator, and the shot noise term of the opamp has been neglected due to CMOS implementation. The first term in (2.16) describes the noise physically generated by the 300KΩ resistor placed in the active feedback that is divided by the attenuator scheme; thus, it is like the noise generated by a resistor of value R_{DC}. The second term is the shot noise of sub-threshold devices, which is negligible for low input currents. For instance, if R_{DC}=1.65GΩ, then the shot noise term is negligible for input current lower than 10pA. The third term is different from the second one in (2.13), although they both describe the noise created by the opamp. In the CT CSA the transfer function is related to the feedback capacitance only, while the active feedback plays only at DC frequency.

Substituting (2.12) into (2.16) and neglecting the shot noise term; it is possible to express the input-referred noise PSD in relations to design parameters:

$$\begin{aligned}\overline{i_N^2} &= 4kT\left(\frac{1}{R_{DC}}+\frac{4}{3}\frac{\left(2\pi f\right)^2\left(C_F+C_{IN}\right)^2}{g_m}\right)+\frac{8\pi^2 K_F}{C_{OX}WL}\left(C_F+C_{IN}\right)^2\cdot f = \\ &\approx \frac{4kT}{R_{DC}}+\frac{16kT}{3}\frac{\left(C_F+C_{IN}\right)^2}{g_m}\left(2\pi f\right)^2,\end{aligned} \tag{2.17}$$

where the last term in the first line is related to the flicker noise, negligible with respect to thermal noise due to R_{DC}.

The input-referred noise PSD given by (2.17) shows a flat behavior at low frequency and a two-fold asymptotical increase at high frequency beyond a corner point. This PSD is very similar to the TIA PSD, both have a noise floor strictly related to the value of the equivalent feedback resistance R_{DC}, resulting in one of the main limitations of the CT approach (Fig. 29).

The last term in the second line of (2.17) is dependent on the transconductance g_m and on the total capacitance C_T=C_F+C_{IN} facing the input node, where C_F is the feedback capacitance and C_{IN} is the sum of the sensor output and input stray capacitances. The above terms set the corner frequency between the flat and the asymptotic f^2 behavior. The increase of C_T decreases the corner frequency, as shown in Fig. 29, resulting in a reduction of the low-

noise bandwidth (i.e. the bandwidth in which the system reaches the noise floor).

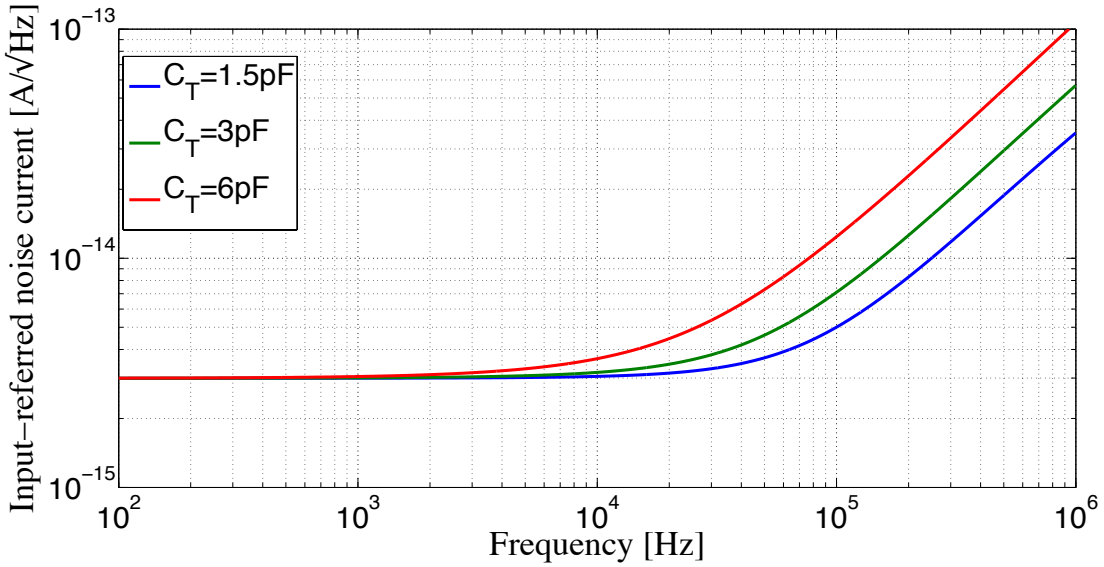

Fig. 29 Simulation of Input-referred noise current of the system presented in [Ferrari,09] for different input capacitances. The simulation follows the square root of (2.17) with a flat behavior at low frequency and an asymptotically increase at high frequency beyond a corner point. That PSD is very similar to TIA PSD.

Note that the input stray capacitance includes the stray capacitances of the wire, the pad and the bond-wire and other capacitances such as pin-to-pin coupling capacitance and opamp input capacitance, which is mainly given by C_{GS}. This last capacitance creates a trade-off in noise optimization since it acts twice in (2.17), both on C_T and on g_m. For instance, a low C_{GS} will reduce C_{IN} and thus the noise; however, it requires smaller input devices for the opamp and thus a smaller transconductance g_m, increasing the noise power. That means there is an optimum value for C_{GS} which minimize the input-referred noise power [Sansen,90]. Substituting the expression of g_m in (2.17) and evaluating the differentiated function, we obtain the optimum value:

$$C_{GS-OPT} = \frac{C_{IN} + C_F}{3}. \tag{2.18}$$

A continuous-time current-sensing interface using the above approach has been proven to reach a noise floor as low as $4\text{fA}/\sqrt{\text{Hz}}$ with a corner frequency of 80KHz, and to acquire current signal in the 100Hz - 2MHz bandwidth [Ferrari,09]. The main challenge of this approach is ensuring the system stability in the face of increased design complexity, resulting from the introduction of the active feedback network [Ferrari,09].

Finally, an interesting alternative approach, based on a current-to-current amplification scheme, is presented in [Ferrari,10]. The circuit is very powerful showing 1pA rms at 100KHz; however, it is shot noise limited, meaning its input-referred noise is directly proportional to the input current (for currents greater than 30/40pA it has a noise floor greater than 4fA/√Hz [Carminati,09]).

2.3 Discrete-Time Approach

2.3.1 Synchronous Reset

The discrete-time approach [Ayers,07], [Bennati,09], [Culurciello,08], [Gore,06], [Stanacevic,07], [Zhang,04] offers several implementation advantages, since it is more robust against device scaling, more suitable for interfacing with digital structures in sensing interfaces[6], and naturally more linear than continuous-time architecture [Johns,97].

DT schemes rely on a common structure and functionality based on a current integration performed over a fixed amount of time. In a standard DT current readout circuit, a switch periodically resets the charge stored in the feedback capacitance C_F, thus avoiding opamp saturation. The presence of a reset period may cause the loss of input data; however, it can be rander negligible by minimizing the reset time.

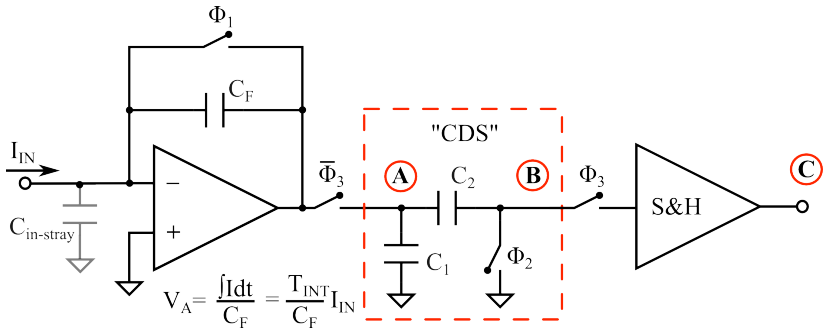

Fig. 30 DT current readout system followed by a CDS block to reduce low frequency noise and offset [Bennati,09]. When Φ_1 is closed the CSA is reset. Then, Φ_1 and Φ_3 are opened and Φ_2 is closed. While Φ_2 opens the CDS takes the noise sample and then starts the integration of the input current. At the end, switch Φ_3 opens and the difference between the last sample and the initial noise sample is stored into the S&H. For more details please refer to section 1.4 or [Bennati,09].

[6] One new trend in analog design is the "digitally-assisted analog", where digital circuits aid rough analog stages so as to get the desired performance with minimum power consumption and keeping the costs low [Murrmann,06].

Moreover, the CSA may suffer from a limited dynamic range due to the limited value of the feedback capacitance, since the final output voltage is given by (2.14). To increase sensitivity without reducing bandwidth, it is mandatory to use a very low capacitance in the feedback loop, implying kTC noise due to reset switch and charge injection phenomena as main issues. To cope with these errors, correlated double sampling (CDS) has proven to be an excellent solution [Ayers,07], [Bennati,09], [Culurciello,08], [Yang,09].

The CDS is a noise and offset reduction technique based on differentiating successive samples [Enz,96], [Oliaei,03], [Pimbley,91], [Wey,86], [White,74]; therefore it can even work as a differentiator stage. The principle is that when noise is acting in a finite bandwidth, low frequency components become correlated and can be used to cancel each other. In summary, the CDS technique is based on sampling the 'signal' twice: the first time when only noise and offset $n(T_1)$ are present, and the second time when both signal and noise are present:

$$\begin{aligned} v_A(T_1) &= n(T_1), \\ v_A(T_2) &= s(T_2) + n(T_2), \end{aligned} \tag{2.19}$$

where $s(t)$ is the informative component of the signal. Finally CDS computes the difference between the two samples:

$$v_B(T_2) = v_A(T_2) - n(T_1) \approx s(T_2). \tag{2.20}$$

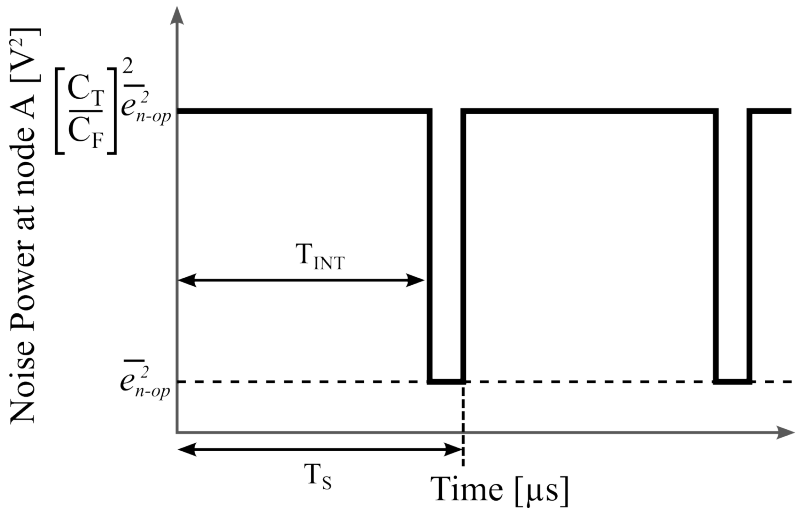

Fig. 31 Time-variant cyclostationary noise power at CSA output. It is modulated by a square wave of period T_S and alternates between $\overline{e^2_{n-op}}$ and $\overline{e^2_{n-op}}$ multiplied by $(C_T/C_F)^2$.

The more the two noise samples are correlated to each other, the better the output difference correspond to the signal itself. For this reason, the CDS technique turns out to be useful to reduce low-frequency noise [Enz,96], [Pimbley,91]. Although CDS reduces *1/f* noise, it results in an increase of white noise due to a folding process, causing a more complex expression for the input-referred noise. For this reason, accurate noise modeling is necessary to understand the trade-off of the DT approach [Crescentini,10].

Fig. 30 shows the DT current-sensing circuit presented in [Bennati,09] composed of a CSA, a CDS and a sample and hold (S&H). This scheme follows the integration-differentiator principle, since CDS acts as differentiation stage. This figure will be used as the reference scheme from here on.

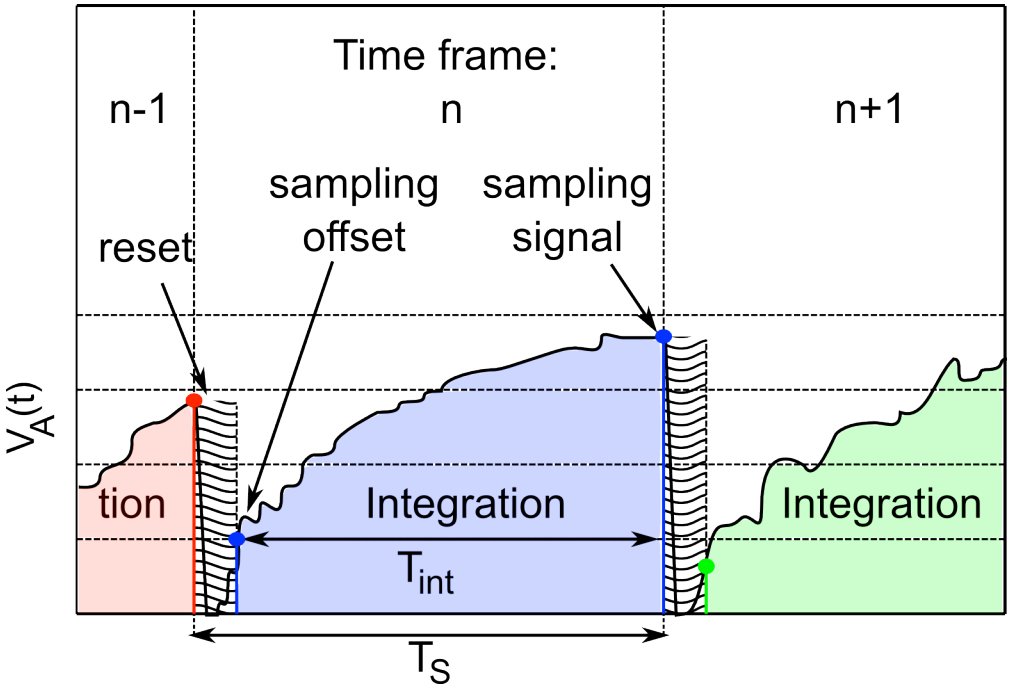

Fig. 32 CDS timing. The first noise sample is taken immediately after the end of the reset period and the second sample is performed just before the reset period. In this way, all samples are out of reset time and the discrete-time signal at the output is again stationary.

Another interesting effect that should be taken into account is the modulation of the noise due to the periodical reset. When the reset switch is open the input noise power is approximately amplified by the ratio C_T^2/C_F^2. On the other hand, when the reset switch is closed the noise power is amplified by one. Thus, the noise voltage is multiplied by a square wave of period T_S and duty cycle

$$d = \frac{T_{INT}}{T_S}, \tag{2.21}$$

where T_{INT} is the integration period and T_S is the sampling period. In other words, the stochastic process becomes cyclostationary with time-varying statistical functions [Phillips,00]. Fig. 31 illustrates the effect of noise modulation, showing the time variant noise power at CSA output.

To mitigate this problem, a "ping-pong" scheme switching between two feedback capacitances of the same value could be used [Zhang,08]. However, in our reference circuit, CDS always takes samples outside the reset frame, as shown in Fig. 32, hence it is possible to neglect the modulation effect. As a result, the noise signal could be treated as stationary.

2.3.2 Noise Modeling in DT Current-Sensing Interfaces

To calculate the minimum detectable input signal of DT schemes, it is necessary to compute the input-referred current noise. However, the input-referred noise can be rigorously define for linear time-invariant circuits only; moreover, since the sampling behavior aliases the high frequency noise components, it is not even possible to define a classic noise transfer function [Pimbley,91]. Thus, we will compute the input-referred noise dividing the output noise PSD by the square of the equivalent analog transfer function, which is the amplifier transimpedance [Crescentini,10]. Taking into account the scheme of Fig. 30, we will assume the circuit is working in time frames of period T_S composed of an integration period lasting T_{INT} and a reset period (Fig. 32).

The kTC noise and the charge injection, generated by the feedback capacitance C_F and the reset switch, are eliminated by the CDS. Additionally, the capacitances used in the CDS are made large enough so as to neglect their own noise sources (that are mainly kTC noise). Thus, the main source of noise in the overall sensing scheme is the opamp, represented by the noise voltage generator $\overline{e_{n-op}^2}$. Neglecting the effect of the reset, $\overline{e_{n-op}^2}$ is amplified and filtered by the CSA, which can be modeled as a first-order amplifier giving a noise PSD at node (A) as:

$$S_A(f) \approx \frac{C_T^2}{\left(C_F + C_T/A_0\right)^2} \cdot \frac{1}{1+\left(f/f_C\right)^2} \cdot \overline{e_{n-op}^2}, \tag{2.22}$$

where A_0 is the open-loop gain, and f_C is the opamp closed-loop cut-off frequency.

Equation (2.20) clearly states that voltage $v_B(t)$ at CDS output (outside the reset) is equal to the input voltage $v_A(t)$ minus the pre-stored input noise sample; thus it can be written as

$$v_B(t) = v_A(t) - \sum\nolimits_n v_A\left(nT_S - T_{INT}\right) \cdot p\left(t - nT_S\right), \tag{2.23}$$

where $p(t)$ is a unity function for $-T_{INT} < t < 0$ and zero elsewhere. To better understand the effects of the CDS on the noise, it is useful to pass from the time domain to the frequency domain, writing the noise PSD at node (B)[7]:

$$\begin{aligned} S_B(f) \approx S_A(f)\left[1 + d^2\mathrm{sinc}^2\left(f \cdot T_{INT}\right) - 2d\mathrm{sinc}\left(2f \cdot T_{INT}\right)\right] + \\ + d^2\mathrm{sinc}^2\left(f \cdot T_{INT}\right)\sum_{k\neq 0} S_A\left(f + \frac{k}{T_S}\right), \end{aligned} \tag{2.24}$$

where the sinc function is defined as

$$\mathrm{sinc}(x) = \sin(\pi x)/\pi x. \tag{2.25}$$

Equation (2.24) is composed of two major components, both shown in Fig. 33. The first one is the differentiation of the input noise PSD. This term describes the CDS as a standard DT differentiator. For frequencies below the sampling frequency, where the correlation between samples is not negligible, the CDS differentiates the input noise, while for higher frequencies it follows the input noise [Oppenheim,99]. As a result, the *1/f* noise and the offset are strongly reduced [Enz,96]. Note that, due to the non-zero reset time, the CDS is not able to completely eliminate the low frequency noise and the offset, but it mitigates them. Indeed, the first term in (2.24) increases at low frequencies, as shown in Fig. 33.

[7] The full mathematical derivation of (2.24) by means of correlation functions and Fourier Transforms is presented in Appendix A.

The last term in (2.24) is related to the high-frequency white noise aliasing due to the undersampling operation of the CDS. Assuming $S_A(f)$ as band-limited white noise with f_C as the -3dB frequency, the undersampling at $f_S << f_C$ implies a folding process of the noise components (Fig. 34). Therefore, the baseband noise is increased by the undersampling ratio (USR) defined as

$$USR = \pi f_C T_S. \tag{2.26}$$

At the end of the integration period, one S&H circuit follows the CDS and stores the final result of (2.23). From a noise point of view, the S&H operation performs an additional noise folding and a further sinc shaping, resulting in a noise PSD at node (C):

$$S_C(f) \approx \mathrm{sinc}^2(fT_S)\cdot\left\{S_A(f)\left[1+d^2\mathrm{sinc}^2(fT_{INT})-2d\mathrm{sinc}(2fT_{INT})\right]+ \right. \\ \left. +2d^2\mathrm{sinc}^2(fT_{INT})\sum_{k\neq 0}S_A\left(f+\frac{k}{T_S}\right)\right\}. \tag{2.27}$$

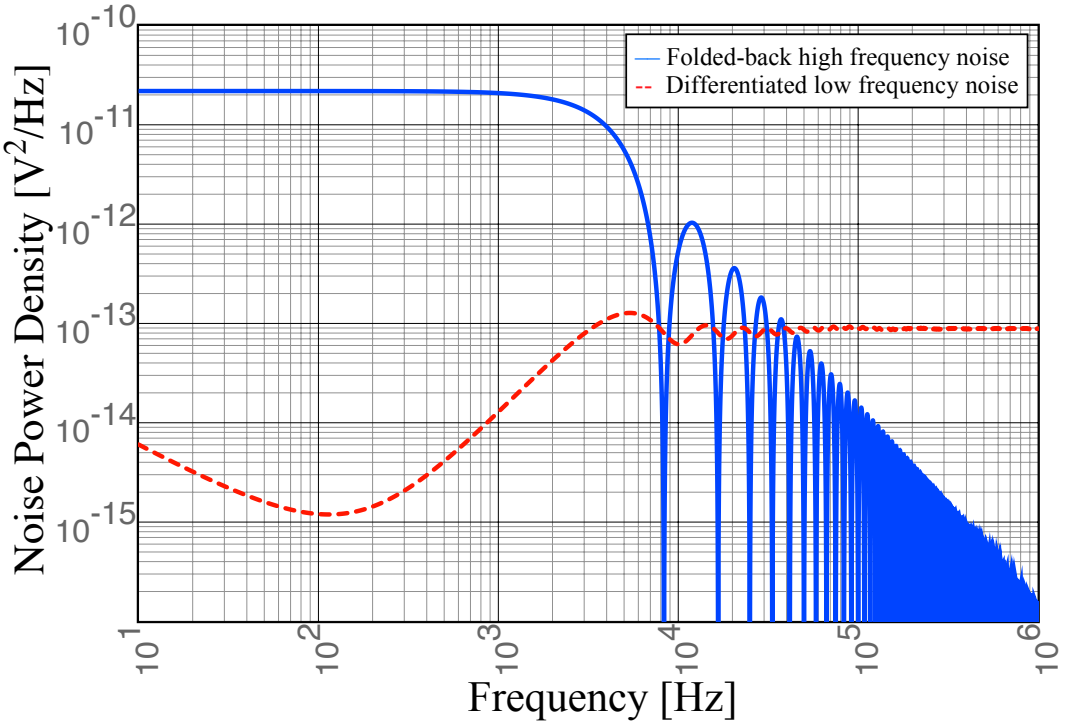

Fig. 33 Noise PSD at node (B) highlighting the components of eq. (2.24). The dashed red line is the differentiated noise given by the first term in (2.24). For frequency below the sampling frequency (in this case approximately equal to 8KHz) the CDS acts as a standard DT differentiator. Due to non-zero reset time (d≈0.937) the low frequency noise is not completely eliminated and a little Flicker noise still remains. The solid blue line is the folded-back white noise due to undersampling operation of the CDS and given by the second term in (2.24). It is clear that, in the band of interest, the latter component dominates over the former.

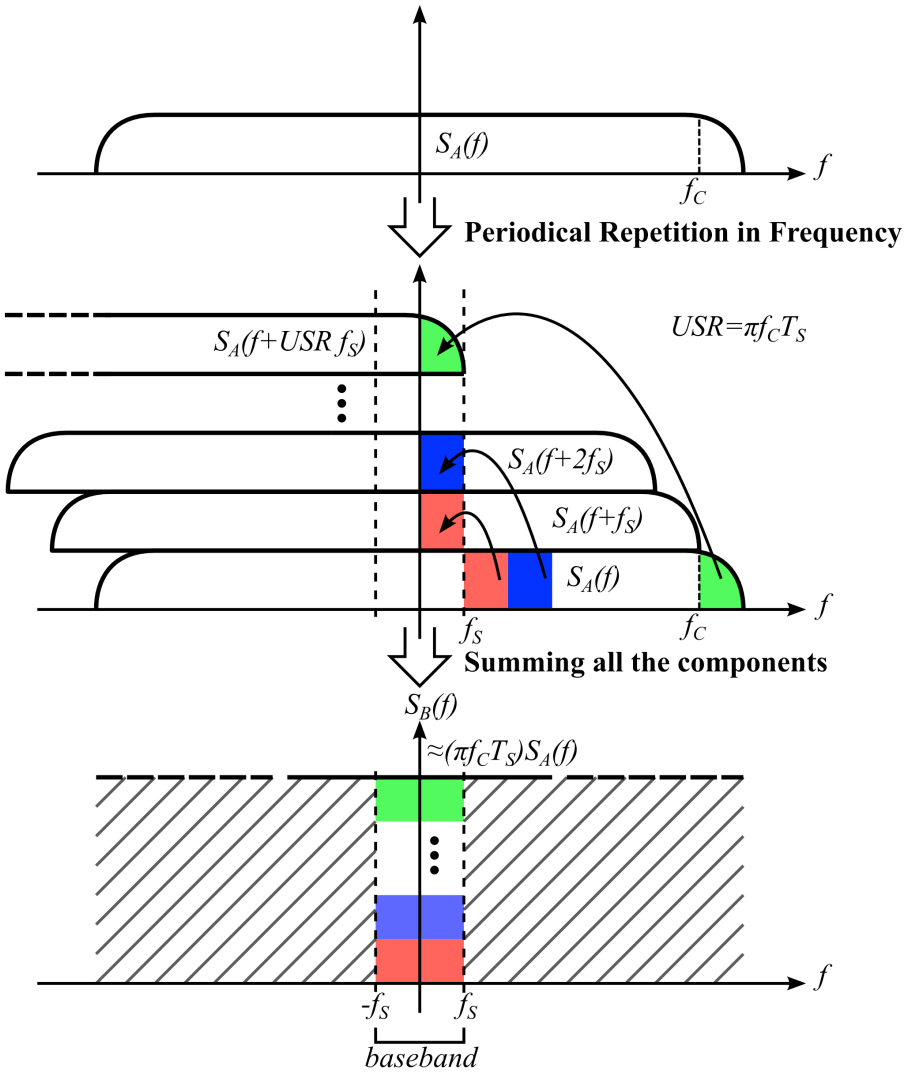

Fig. 34 Noise folding process due to the undersampling. High frequency noise components are folded-back in the baseband by means of the repeated and shifted spectra. Since the sampling frequency is generally lower than the noise bandwidth (i.e. the closed-loop cut frequency), the noise folding process could not be avoided. Summing all the spectra results into a white noise in the useful bandwidth USR times higher than the original noise.

The folding of the Flicker noise can be neglected with respect to white noise, because it is a low frequency noise. Moreover, the undersampling factor of (2.26) can be used to simplify the last term in (2.27) as follows

$$d^2\sum_{k\neq 0} S_A\left(f+\frac{k}{T_S}\right)\approx d^2\left(\pi f_C T_S-1\right)\cdot S_{A,Th}\left(f\right), \tag{2.28}$$

where $S_{A,Th}\left(f\right)$ is the thermal component of $S_A(f)$ [Enz,96]. Note the above approximation is accurate only inside the bandwidth of interest, i.e. for frequencies below $f_S/2$. Combining (2.28) with (2.27) results in

$$S_C(f) \approx \mathrm{sinc}^2(fT_S)\left\{S_A(f)\left[1+d^2\mathrm{sinc}^2(fT_{INT})-2d\cdot\mathrm{sinc}(2fT_{INT})\right]+ \right. \\ \left. +2d^2(\pi f_C T_S-1)S_{A,\,Th}(f)\cdot\mathrm{sinc}^2(fT_{INT})\right\}. \tag{2.29}$$

The folding process greatly increases the noise PSD, but it cannot be eliminated since the sampling frequency f_S must be intrinsically lower than the opamp closed-loop cut-off frequency, in order to sample the signal with the proper accuracy. As shown in Fig. 33, the folding component dominates the output noise in the baseband; thus it is possible to further reduce the (2.29) neglecting the first term:

$$S_C(f) \approx 2d^2(\pi f_C T_S-1)S_{A,\,Th}(f)\cdot\mathrm{sinc}^2(fT_S). \tag{2.30}$$

Considering a short reset time, that implies $d\approx 1$, and applying (2.22) into (2.30) with $A_0 >> 1$ and $f_C >> f_S$, the output noise PSD becomes

$$S_C(f) \approx 2(\pi f_C T_S-1)\cdot\left(\frac{C_T}{C_F}\right)^2\cdot\overline{e^2_{n-op,Th}}\cdot\mathrm{sinc}^2(f\cdot T_S), \tag{2.31}$$

where $\overline{e^2_{n-op,Th}}$ is the thermal component of (2.12). For frequencies below f_S, the CSA and the CDS act on the input signal as an integrator and a differentiator, respectively, and together work as a total equivalent resistance of value

$$R_{EQ} = \frac{T_{INT}}{C_F} \approx \frac{T_S}{C_F}, \tag{2.32}$$

where a negligible reset time has been assumed. Dividing (2.31) by the square of (2.32) and assuming the USR much greater than one, we can write the input-referred noise PSD as

$$\overline{i_N^2} \approx \frac{S_C(f)}{R_{EQ}^2} \approx 2C_T^2\cdot\frac{\pi f_C}{T_S}\cdot\overline{e^2_{n-op,\,Th}}\cdot\mathrm{sinc}^2(f\cdot T_S), \tag{2.33}$$

and for frequencies below $f_S/2$ it can be approximated quite closely as

$$\overline{i_N^2} \approx 2C_T^2\cdot\frac{\pi f_C}{T_S}\cdot\overline{e^2_{n-op,Th}}. \tag{2.34}$$

From (2.33) and (2.34) it is clear that the noise floor of this circuit is set by the bandwidth of the opamp. In principle, input-referred noise benefits from reduction of f_C; however, it cannot be smaller than the settling time of the

opamp. Therefore, the minimum allowed value for f_C depends on the sampling time T_S and the required precision in terms of equivalent number of bits (ENOB) following the equation [Schreier,04]

$$e^{-\frac{\pi f_C}{f_S}} < 2^{-(ENOB+1)}. \tag{2.35}$$

In order to identify design constraints, (2.34) could be revised introducing:

$$f_C \approx GBW \cdot \frac{C_F}{C_T}, \tag{2.36}$$

where GBW is the gain-bandwidth product, which for the CMOS transconductance amplifier is given by

$$GBW = \frac{g_m}{2\pi C_O}. \tag{2.37}$$

The capacitance C_O represents the total capacitance connected to the opamp output (i.e. C_1 + C_2) in a one-stage opamp, and it is the compensation capacitance in a multi-stage realization. Equation (2.34) together with (2.12), (2.36), and (2.37) yields

$$\overline{i_N^2} \approx \frac{16}{3}\frac{C_T C_F}{T_S}\frac{kT}{C_O} = \frac{16}{3}\frac{C_T}{R_{EQ}}\frac{kT}{C_O}. \tag{2.38}$$

where the input-referred noise power of DT current sensing is regarded as the noise generated by an equivalent resistor of value R_{EQ}, or more precisely, as kTC noise related to the output capacitance. Equation (2.38) shows how the input stray capacitance and the sensor capacitance act directly on the noise PSD by means of C_T, and how a large C_O reduces the noise power at the expense of settling time.

It is interesting to note that (2.32) associates the sensitivity of DT systems with the sampling frequency, impacting the dynamic range (DR), which is given by the ratio between the maximum input signal power and the in-bandwidth noise power

$$DR = \frac{V_{OM}^2}{R_{EQ}^2 \cdot \overline{i_n^2} \cdot \frac{f_S}{2}} = \frac{V_{OM}^2}{\frac{8}{3}\frac{C_T}{C_F}\frac{kT}{C_O}}, \tag{2.39}$$

where V_{OM} is the maximum output voltage of the amplifier. Thus, as presented in (2.39) and illustrated in Fig. 35, C_T reduction has a direct benefit on both input-referred noise and DR. Conversely, as illustrated in Fig. 36, reduction of the sampling time impacts both noise level and bandwidth, without affecting the DR.

Finally, note that there are no parameters related to the opamp in (2.38). This is due to the fact that, as in kTC noise, a decrease of the input noise voltage power $\overline{e_{n-op}^2}$ by means of g_m involves an equivalent increase of the bandwidth according to (2.36) and (2.37). Therefore, opamp noise performance does not affect the overall DR, as indicated in (2.39), and the input-referred noise is not subject to the C_{GS} trade-off.

In Fig. 37 the input-referred noise current given by the square root of (2.33) is compared with a measurement on the system developed in [Bennati,09], proving a good match. The graph reports the input-referred noise measured in an ideal environment, using a dedicated low-noise testing board, where the chip was enclosed in a Faraday cage and the input pin was cut. When the IC is placed in the working printed circuit board (PCB) of Fig. 17, the measured input-referred noise is approximately one order of magnitude higher (Fig. 38).

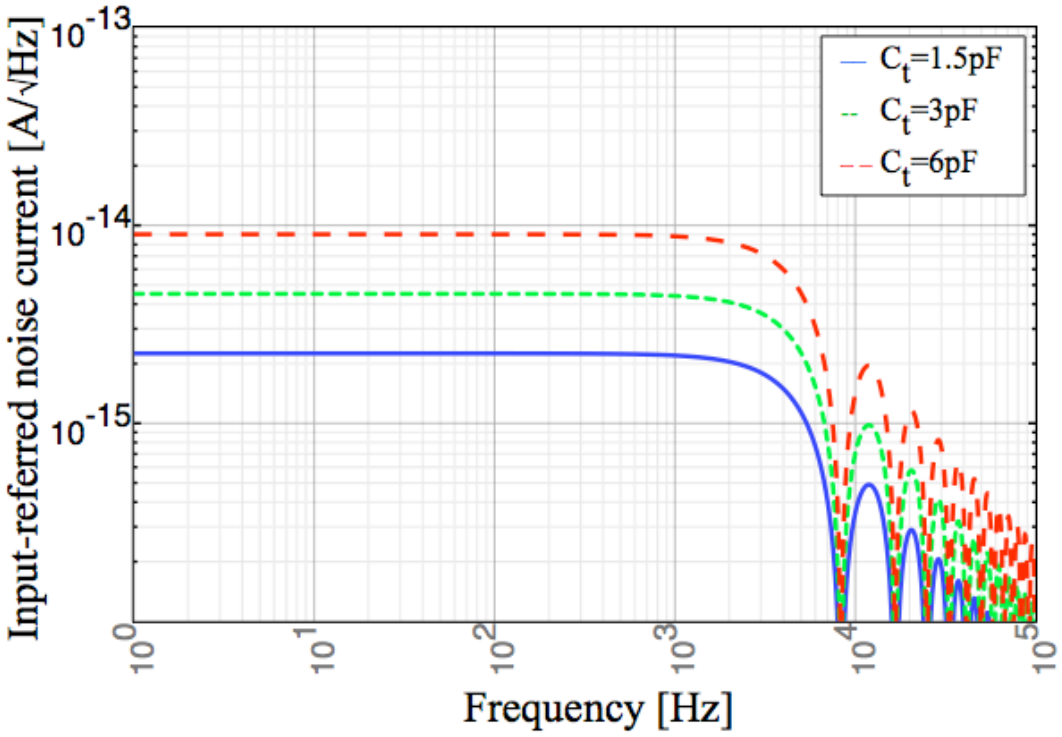

Fig. 35 Plot of the input-referred noise current given by square root of (2.31), where the effect of C_T on f_C has been taken into account. The plot shows the strong effect of C_T on the input referred noise current, assuming C_F fixed to 100fF.

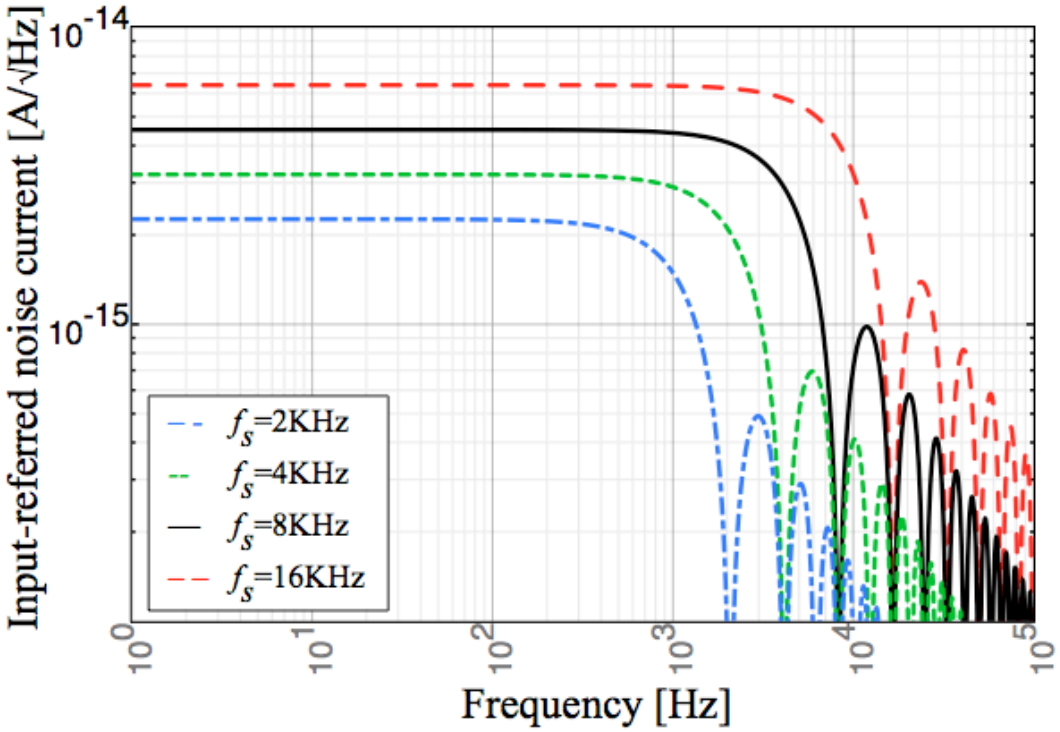

Fig. 36 Plot of the input-referred noise current for different sampling frequency f_S, showing that lower sampling frequency also implies lower bandwidth and noise floor.

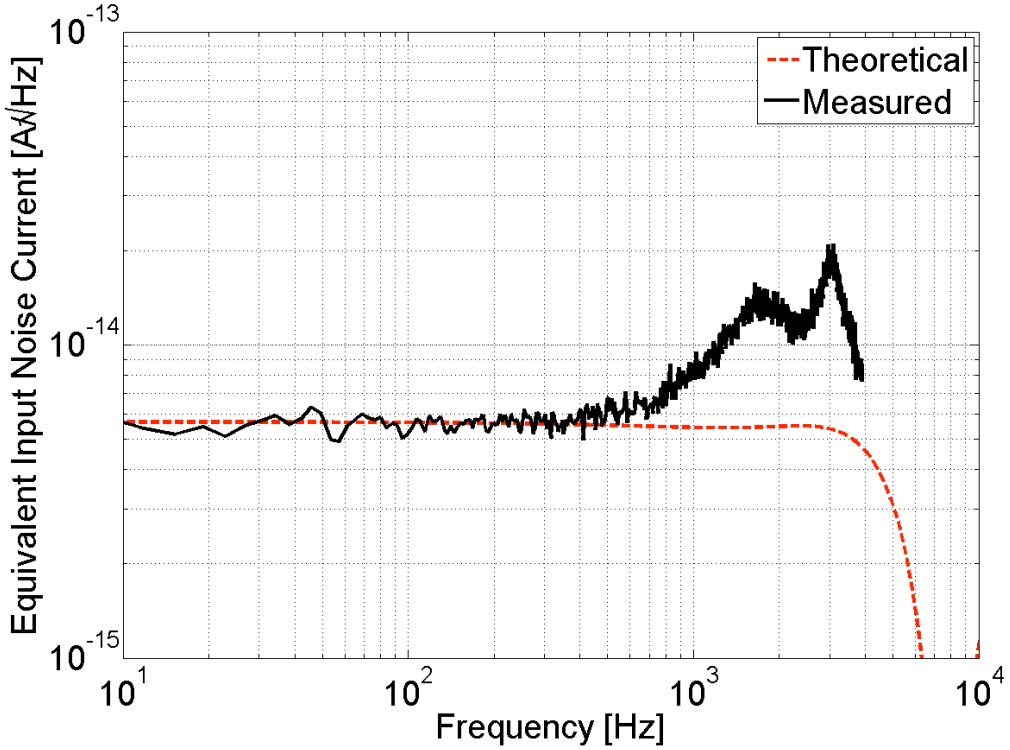

Fig. 37 Equivalent input referred noise current calculated using a 3pF input stray capacitance. The solid black line is the measured current noise on the prototype presented in [Bennati,09]; the dashed red line is given by square root of (2.34) using the same parameters (i.e. T_S=128µs, T_{INT}=120µs, C_F=100fF, C_T=3.1pF). The two peaks around 2KHz and 3KHz in the black line are due to a coupling effect of the 1MHz clock signal.

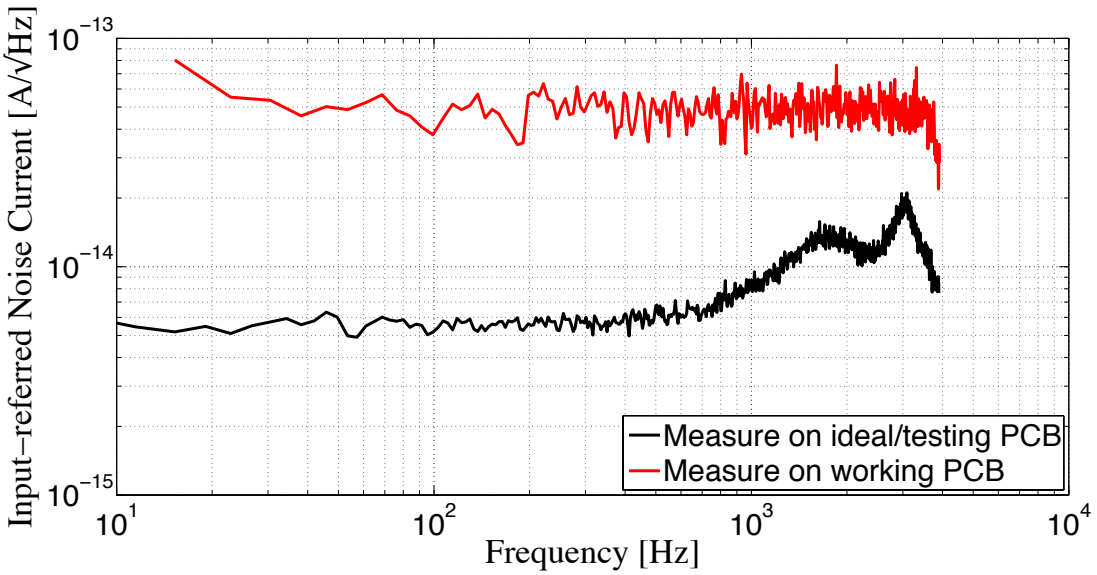

Fig. 38 Measured input-referred noise current of the IC presented in [Bennati,09] tested on an ideal PCB (black line) and tested on the working PCB shown in Fig. 17 (red line). The measures clearly show the effects of parasitic elements on input-referred noise current.

In complex mixed-signal systems like DT current-sensing interfaces, where both analog and digital circuits are integrated, there are many parasitic elements affecting the performance. First of all, the input-referred noise of a DT current amplifier is strongly related to the input capacitance, as stated in (2.38), therefore connecting the interface to the PCB and the sensor will necessarily increase the noise.

Moreover, there are unavoidable coupling effects between noisy digital signals and quiet analog signals, due to many different mechanisms such as substrate paths, power lines or pin-to-pin connections. The easiest way to cope with them is to place the two circuits as far apart as possible, maybe using a buffer space in between, but this takes space and costs a lot.

Digital circuits generate quite large di/dt during the switching activity. This current needed to charge/discharge the load capacitance has to come from the power supply generating glitches on the power supply voltages, thus creating interferences and noise on the analog part. Physically separating the power lines of digital circuits from those of analog circuits is the easiest way to reduce noise coupling from power supplies. Obviously this method requires at least double the number of pins. Sometimes it is not possible to add new pins, or digital and analog circuits are forced to share the same power lines. In these cases it is mandatory to take into account the coupling effects when designing both circuits. From the analog point of view this

means making the circuits more robust by improving the power supply rejection ratio.

Another coupling mechanism is associated with stray capacitances and inductances between closed pins or bond-wires. This issue requires a careful design of pin allocation and chip floor-planning. There also exist package technologies which reduce the coupling effects by means of lower stray elements reducing the coupling effects. Fig. 39 shows simulations of some of these parasitic effects, like power supply noise and pin-to-pin coupling, on the IC reported in section 1.4.

To summarize, DT current-sensing interfaces are described by an input-referred noise PSD different from the one characterizing TIA or CT interfaces and it is unaffected by the C_{GS} trade-off. Moreover, noise reduction in DT current amplifiers could be accomplished by acting on several parameters. For some of them, such as output, stray and feedback capacitances, the reduction of the noise even increases the DR. While for other parameters, such as the sampling time, it does not affect the DR because it reduces the output swing by the same amount.

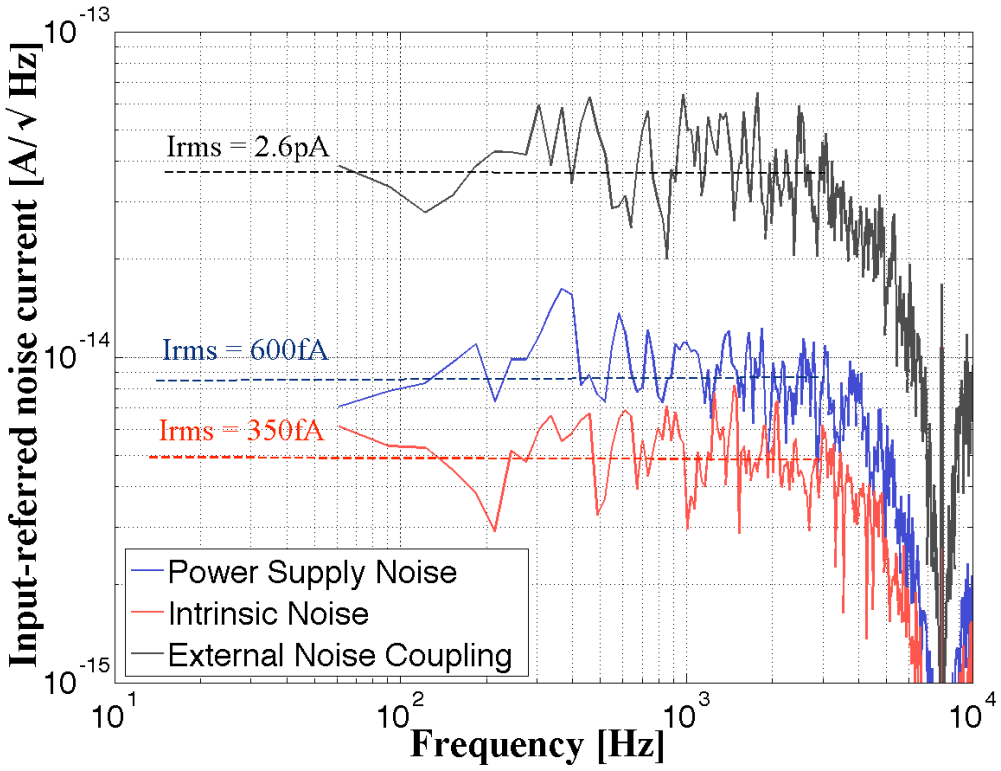

Fig. 39 Simulations of the effects of parasitic elements on the input-referred noise: the red line is the ideal input-referred noise; the blue line estimates the effects of noise coming from power supplies; the black line estimates the noise coming from a near digital pins by means of a pin-to-pin coupling effect due to a 500fF parasitic capacitor.

A DT current-sensing interface using this approach has been proven to reach a noise floor as low as 5fA/√Hz, able to acquire current signals from DC to 4KHz [Bennati,09].

2.4 Comparison between CT and DT Approaches

2.4.1 CT versus DT in the Literature

Paper	Style	Input-referred noise floor current [fA/√Hz]	Noise Floor Band. [KHz]	Input cap. [pF]	Operating Band. [KHz]	Note
[Ferrari,09]	CT	4	80	0.7	0.1÷2,000	
[Gozzini,09]	CT	3	30	0.7	10,000	Data related only to current amplifier
[Weerakoon,09]	CT	50	10	10	10	*1/f* noise not compensated
[Ferrari,10]	CT	0.5	30	0.8	10,000	Shot noise limited
[Hu,10]	CT	158	1÷500	No	1,000	
[Zhang,04]	DT	80	0.1	No	1	CDS noise effect not modeled
[Gore,06]	DT	130	0.5	No	1	Noise inferred on paper data
[Ayers.07]	DT	3	2	No	2	
[Stanacevic,07]	DT	100	1E-4	No	3E-2	Noise inferred on paper data
[Culurciello,08]	DT	33	0.1	50	0.1	
[Bennati,09[	DT	5	0.7	3p	4	
[Heitz,11]	DT	150	0.8	No	0.8	Noise inferred assuming white noise limited
[Wang,10]	DT	7	5	6.5	5	Noise inferred assuming white noise limited

Table 2 Published CMOS integrated implementations of current-sensing interfaces compared by means of many noise and work parameters

Both CT and DT solutions are based on charge-sensitive amplifiers and are limited in bandwidth in different ways. To organize a fair comparison among

them, based on different schemes presented in the literature, it is important to characterize the noise floor by taking into account the total input capacitance C_T affecting the noise PSD either over the entire noise spectrum, as in DT approach, or with respect to the corner frequency, as in CT one. In the latter case, also the bandwidth in which the noise is kept constant should be defined. Indeed, the signal-to-noise ratio (SNR) greatly reduces itself at frequencies higher than the corner frequency given by C_T.

Table 2 compares recent CMOS integrated implementations of current interfaces as presented in the literature. From this comparison, it is possible to observe that many CT approaches reach the MHz bandwidth, while DT approaches are limited to a maximum of 10KHz (Fig. 40). For this reason the CT approach appears to be the best solution for applications where fast current tracking is mandatory, maybe using nanopores as bio-nanosensors.

The stray input capacitance has a negative influence on both approaches; however, DT schemes are more subject to it since the input capacitance acts directly on the noise floor. Thus, the noise performance of a DT interface is often worse due to the sensor capacitance (Fig. 41), but the DT current interfaces show better linearity and are more suitable for integration with digital circuits.

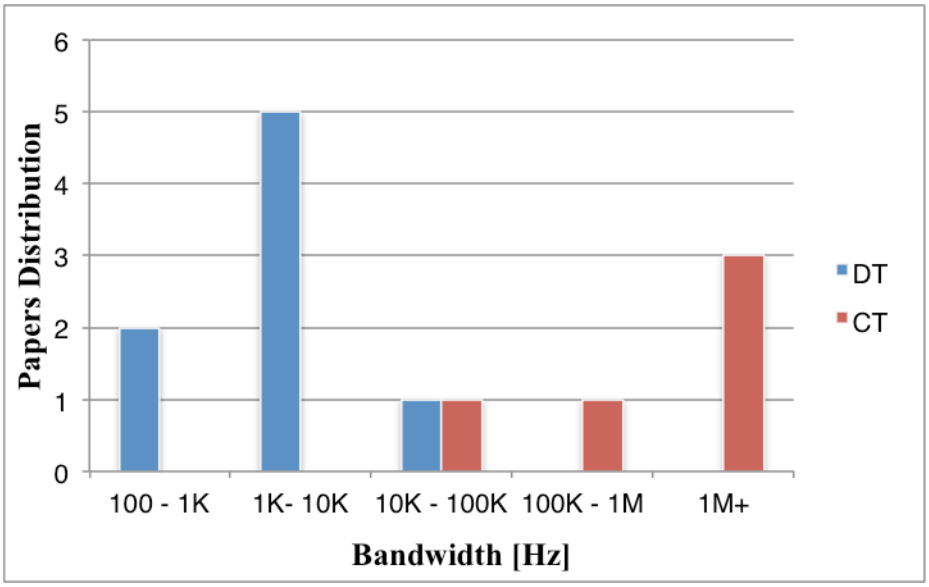

Fig. 40 Distribution of papers in literature regarding their bandwidth. DT approach is not able to overcome the 10K-100KHz wall, but the CT approach easily reaches bandwidths in the MHz range. However, the majority of papers use the DT approach and limit the working bandwidth to 10KHz, since they are intended for ion channel applications.

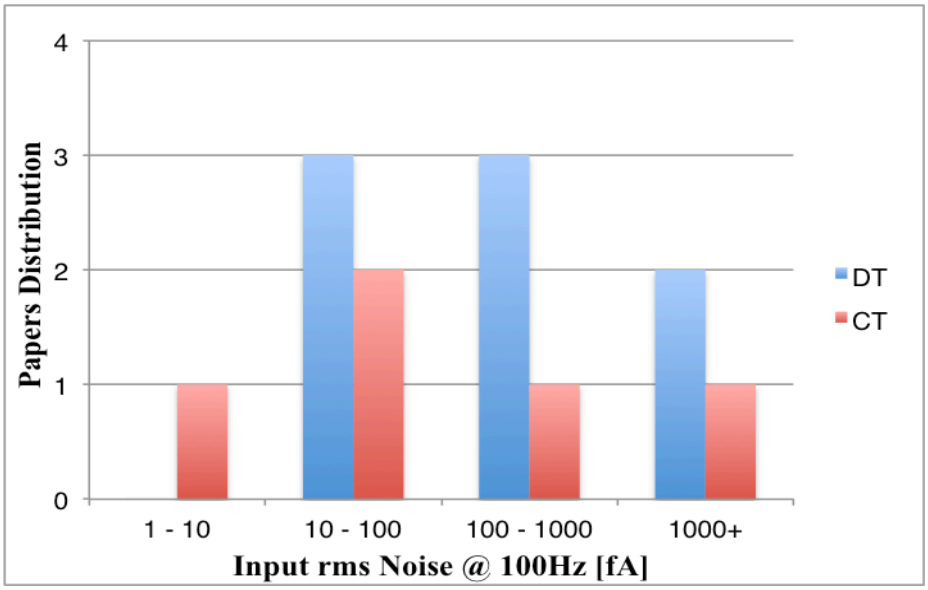

Fig. 41 Distribution of papers in literature regarding their noise performance in terms of input rms noise @ 100Hz. The best circuit is a CT scheme but many DT approaches have a noise just one order of magnitude greater.

In recent years, the interest of the research community in low-noise current-sensing interfaces has grown. Indeed, the excellent potential of bio-nanosensor applications (mainly ion-channels and nanowires) has driven the development of new, high-performance, integrated current readout schemes. Thanks to the development of novel architectures, as shown in Fig. 42, the input-referred rms noise computed at 100Hz decreased by about two orders of magnitude over about 5 years, proving the interest and the relevance of this research field.

2.4.2 Scaling Trends and Future Perspectives

As mentioned and highlighted in many sections so far, the integration step is crucial to many benefits in bio-nanosensor applications; therefore, it is important to evaluate the effects of technology scaling on the noise of both CT and DT approaches. Starting with the CT approach and considering a constant field scaling with factor S, it will be assumed that all the capacitances scale with S, whereas g_m and R_{DC} are kept constant [Wong,83]. Applying that scaling scheme to (2.17) we find:

$$\overline{i_N^2} \approx \frac{4KT}{R_{FEQ}} + \frac{16KT}{3}\frac{C_T^2}{g_m}\cdot(2\pi f)^2\cdot\frac{1}{S^2}. \qquad (2.40)$$

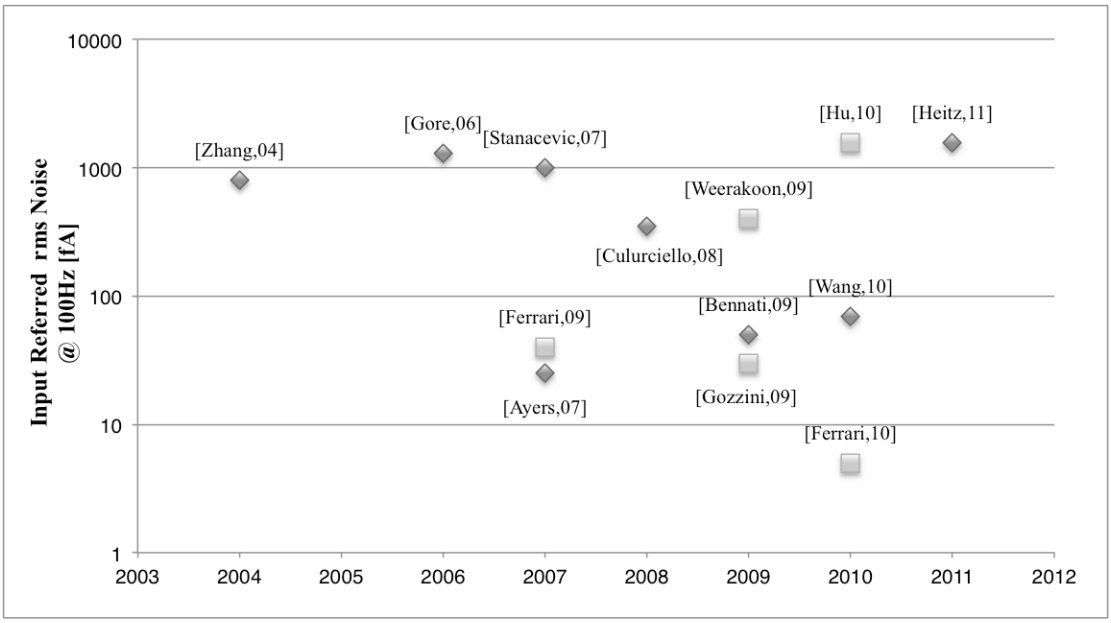

Fig. 42 Evolution trend of current sensing through the last few years. Marks denotes: DT schemes with rhombus; CT schemes with squares.

The scaling process shifts the corner frequency to the right, but has no effect on the noise floor. Thus, the CT approach does not benefit greatly from scaling; moreover, extra care should be taken with flicker noise derived from the active feedback, since it becomes higher with the scaling process.

Applying the same scaling scheme to (2.38) for the DT approach yields

$$\overline{i_N^2} \approx \frac{2}{3}\frac{C_T/S}{C_{OUT}/S}\frac{4kT}{R_{EQ}/S} \approx \frac{\overline{i_N^2}}{S}, \tag{2.41}$$

where a constant field scaling with factor S results in a scaling of the input noise PSD with factor S. It should be noted that even if the scaling process exhibits an increases in flicker noise, kTC noise, and charge injection, the DT current sensing is expected to reduce them by means of the CDS. However, it should be pointed out that kTC noise, deriving from the CDS scheme, could grow if the capacitances of the CDS are shrunk too much. The scaling benefit is directly related to the increase of the sensitivity R_{EQ} by means of C_F scaling. Therefore, to completely fulfill (2.41) the output voltage range should be enlarged; otherwise the DR and the input full-scale will fall.

The most interesting advantage of the DT approach is power consumption. Indeed, since its input-referred noise power is not related to opamp parameters, one can project the operational amplifier focusing on low-power consumption and disregarding noise performance.

As shown in (2.17) and (2.38), in both approaches the input-referred noise power is strongly related to the total input capacitance, hence to the input stray capacitance. Shrinking that capacitance, thanks to the scaling process, improves the resolution of the interface.

Finally, both CT and DT approaches have proven to be subject to architecture and technology improvements. For instances, the development of a novel low-noise active feedback will directly decrease the noise floor in CT current sensing, and many design parameters can be optimized in DT schemes so as to mitigate the folding noise[8]. The development of either CT or DT circuits in SOI technology will bring many advantages in terms of intrinsic noise and coupling noise, since stray capacitances are minimized. As a consequence, we expect further improvements in low-noise current-sensing, in the near future, mainly related to development of novel, more efficient, architectures.

[8] One possible improvements of DT current sensing scheme will be presented in chapter 3.

Chapter 3

Noise-Reduction Technique in Discrete-Time Current-Sensing

This chapter presents a novel technique capable of reducing the kTC noise in systems characterized by high voltage gain. The technique allows the trade of power for better noise performance unleashing the kTC noise constraint. The first section presents the noise-reduction technique in a general way, explaining the basic idea. Section two applies the technique to discrete-time current-sensing interfaces and develops a new mathematical model for the input-referred noise power spectrum density (PSD).

3.1 Unleashing the kTC Noise Constraint

The kTC noise terms refers to the thermal noise in the presence of a filtering capacitor, as shown in the simplified picture of Fig. 43, where the actual source of noise is the transconductor. Supposing a CMOS implementation for the transconductor, the thermal noise power of the MOS device working in saturation region is given by a γ fraction of the resistance of the channel, where γ is usually equal to $2/3$ for long channel MOSFETs [Robinson,74]. Assuming the noise of the transconductor is mainly given by the input differential pair and neglecting the Flicker noise, the noise power density at the output node is given by

$$\overline{v_{n-OUT}^2} \approx \frac{16}{3}\frac{kT}{g_m}A^2, \tag{3.1}$$

where A represents the closed-loop voltage gain of the transconductor. Assuming a one-stage realization for the operational transconductance amplifier (OTA), the equivalent noise bandwidth ($EQNB$) can be written as

$$EQNB = \frac{g_m}{4C} \cdot \frac{1}{A}, \tag{3.2}$$

where C is the output capacitance. The g_m parameter of the transconductor acts in opposite fashion on the noise density and the $EQNB$, thus the total noise power $P_{n\text{-}OUT}$ across the capacitor does not depend upon the transconductor but relies solely on the output capacitance

$$P_{n-OUT} = \int_{EQNB} \overline{v_{n-OUT}} \cdot df = \overline{v_{n-OUT}} \cdot EQNB = \frac{4}{3}\frac{kT}{C} A. \tag{3.3}$$

This strong relation between noise density and bandwidth precludes trading power for low noise. Indeed, increasing the transconductance g_m at the transconductance g_m at the expense of higher power consumption lowers the noise PSD and broadens the $EQNB$ at the same time, without affecting the total noise power.

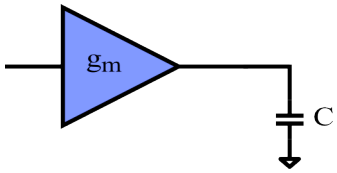

Fig. 43 Simplified scheme for kTC noise study.

To overcome the above limitation it is mandatory to develop a new technique able to decouple noise density from noise bandwidth. One possible solution is the insertion of a resistor between the noisy element and the capacitor, so that a new dominant pole is added to the global transfer function (Fig. 44) [Crescentini,11]. The noise density is the same as before, but now the $EQNB$ is unrelated to the transconductor

$$EQNB = \frac{1}{4RC}. \tag{3.4}$$

and the total noise power across the capacitor is now given by

$$P_{n-OUT} = \int_{EQNB} \overline{v_{n-OUT}} \cdot df = \frac{4}{3}\frac{kT}{g_m RC} A^2. \tag{3.5}$$

In plain words, the resistor filters the noise generated by the transconductor. It is not necessary to put the new pole at frequencies much lower than the original bandwidth, because the strength of the technique is in the decoupling. Indeed, it is now possible to act on g_m so as to lower the noise, keeping the *EQNB* constant in first approximation, as illustrated in Fig. 45.

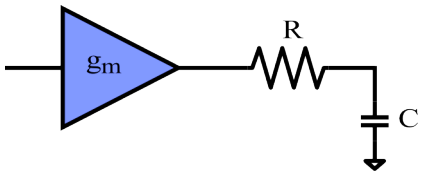

Fig. 44 Scheme modified with the addition of one resistor to decouple noise density from noise bandwidth.

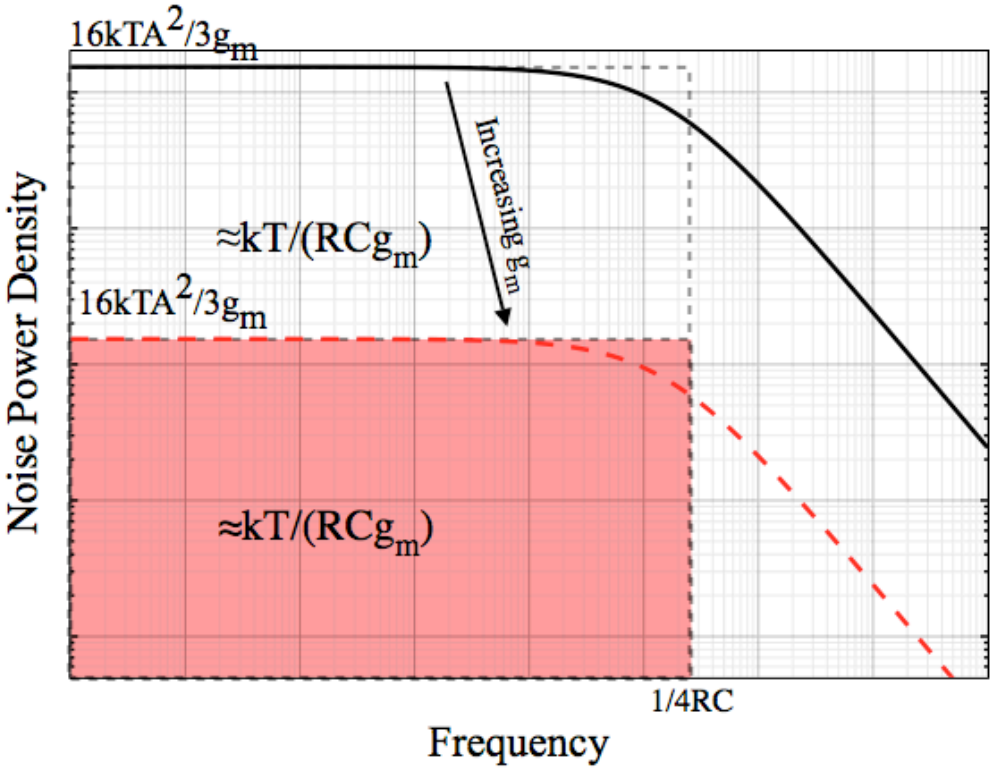

Fig. 45 Example of kTC noise reduction by means of a decoupling resistor. Increasing the transconductance g_m we can lower the noise density without affecting the *EQNB*, achieving a global noise reduction.

The noise-reduction technique presented so far is accurate if the noise of the resistor is negligible compared to the noise generated by the transconductor. In mathematical terms, this becomes an upper bound on the resistance value

$$\begin{aligned} 4kTR &<< \frac{16}{3}\frac{kT}{g_m}A^2 \\ R &<< \frac{4}{3}\frac{A^2}{g_m}. \end{aligned} \tag{3.6}$$

Moreover, the technique can be employed successfully only if the transconductor is characterized by high voltage gain factor A. In fact, if the primary noisy element (in the above case the OTA) is just a simple resistor, the kTC noise reduction technique does not work at all and the total noise power is equal to kT/C. Increasing the transconductance g_m makes the upper bound expressed in (3.6) more and more severe, meaning it is not possible to arbitrarily lower the noise ad infinitum.

The above discussed noise-reduction technique allows the trade of power for low noise, until the noise power generated by the transconductor becomes negligible compared to that one generated by the resistor (again kTC noise but reduced by the voltage gain factor).

The kTC noise reduction technique reported here has been developed independently. However, similar noise reduction techniques are presented in [Fowler06] and [Kapusta,09] in application completely different.

3.2 Application to Discrete-Time Current Sensing

In a general discrete-time (DT) current-sensing interface the noise, whether referring to the input or to the output, is actually kTC noise, as discussed in section 2.3.2 and stated by (2.38) here reported as (3.7).

$$\overline{i_N^2} \approx \frac{16}{3}\frac{C_T}{R_{EQ}}\frac{kT}{C_O}; \tag{3.7}$$

$$\overline{v_{OUT}^2} \approx \frac{16}{3}C_T R_{EQ}\frac{kT}{C_O}. \tag{3.8}$$

The inherent undersampling process folds back the high frequency noise, creating a new white noise PSD with amplitude given by (3.7) referring to the input or given by (3.8) referring to the output, and bandwidth equal to the sampling frequency. The main source of noise is the OTA used in the charge-sensitive amplifier (CSA), which is characterized by high voltage gain. Therefore, discrete-time current sensing meets all the requirements to

successfully apply the kTC noise reduction technique so as to push down the noise and improve the minimum detectable current.

Referring to the equivalent model depicted in Fig. 46, it is possible to compute a formula for the input-referred noise PSD for discrete-time current-sensing interfaces employing "beating" kTC noise technique. In this way we can carefully analyze the effect of the noise-reduction technique.

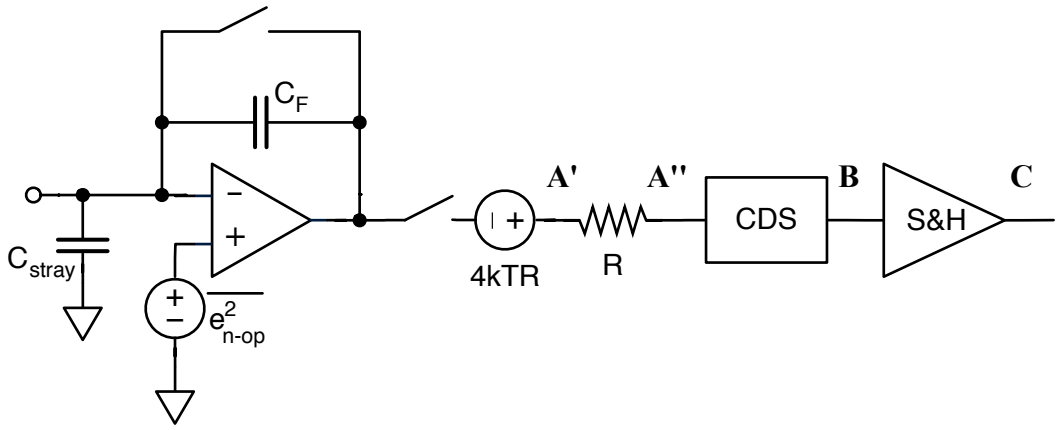

Fig. 46 Simplified scheme of discrete-time current-sensing interface employing CDS and kTC noise reduction technique. The scheme emphasizes the two leading noise sources: the OTA and the resistor.

Fig. 46 shows a simplified scheme of the circuit described in Fig. 30, where the new resistor splits the node *A* into two nodes *A′* and *A″*. At node *A′* the noise PSD is given by the sum

$$S_{A'}(f) = \left(\frac{C_T}{C_F}\right)^2 \overline{e_{n-op}^2} \cdot \frac{1}{1+\left(\frac{f}{f_C}\right)^2} + 4kTR, \tag{3.9}$$

where the first term is the noise generated, amplified and filtered by the OTA and the second term is the noise due to the resistor *R*. At node *A″* the resistor filters the noise and the PSD becomes

$$S_{A''}(f) = \left[\left(\frac{C_T}{C_F}\right)^2 \overline{e_{n-op}^2} \cdot \frac{1}{1+\left(\frac{f}{f_C}\right)^2} + 4kTR\right] \cdot \frac{1}{1+\left(\frac{f}{f_R}\right)^2}, \tag{3.10}$$

where f_R is the cut-off frequency of the filter, given by

$$f_R = \frac{1}{2\pi R C_O}. \tag{3.11}$$

In order to apply the noise-reduction technique correctly, the frequency f_R ought to set the dominant low frequency pole:

$$\begin{aligned} f_R < f_C \Rightarrow \frac{1}{2\pi R C_O} &< \frac{g_m}{2\pi C_O}\frac{C_F}{C_T} \\ \Rightarrow R g_m &> \frac{C_T}{C_F}. \end{aligned} \tag{3.12}$$

Therefore, for frequencies lower than the closed-loop cut-off frequency of the OTA, (3.10) can be simplified to

$$S_{A''}(f) \approx \left[\left(\frac{C_T}{C_F}\right)^2 \overline{e_{n-op}^2} + 4kTR\right] \cdot \frac{1}{1+\left(\frac{f}{f_R}\right)^2}. \tag{3.13}$$

Applying the same logical steps and hypotheses used in section 2.3.2 to the folding of white noise, we can compute the output noise PSD after the correlated double sampling (CDS) and the sample and hold (S&H) as

$$S_C(f) \approx 2\left(\pi f_R T_S - 1\right)\left[\left(\frac{C_T}{C_F}\right)^2 \overline{e_{n-op,Th}^2} + 4kTR\right] \cdot \mathrm{sinc}^2\left(fT_S\right), \tag{3.14}$$

where the undersampling factor (USR) factor is now related to the frequency f_R.

Assuming the USR much greater than one, and dividing (3.14) by the equivalent resistance given by (2.32), we can write the input-referred noise PSD for low frequencies as

$$\overline{i_N^2} \approx 2C_F^2 \frac{\pi f_R}{T_S}\left[\left(\frac{C_T}{C_F}\right)^2 \overline{e_{n-op,Th}^2} + 4kTR\right] \cdot \mathrm{sinc}^2\left(fT_S\right). \tag{3.15}$$

Using (3.11) and the thermal component of (2.12) in (3.15), the amplitude of the input-referred noise PSD at frequencies lower than f_S becomes:

$$\begin{aligned}\overline{i_N^2} &\approx \frac{C_F^2}{RC_O T_S}\left[\left(\frac{C_T}{C_F}\right)^2 \frac{16}{3}\frac{kT}{g_m} + 4kTR\right] \\ &\approx \left(\frac{16}{3}\frac{kT}{C_O}\cdot\frac{C_T^2}{Rg_m T_S} + 4\frac{kT}{C_O}\cdot\frac{C_F^2}{T_S}\right).\end{aligned} \tag{3.16}$$

The first term in (3.16) accounts for the noise generated by the OTA and reduced by the kTC noise reduction technique. The formula is very similar to (3.7) but now there are more degrees of freedom, allowing us to play with the resistance R and the transconductance g_m so as to further reduce the noise density. The dependency of the formula upon OTA parameters (i.e. the transconductance) makes the input-referred noise PSD subject to C_{GS} optimization, as for continuous-time (CT) current sensing.

The second term in (3.16) accounts for the noise generated by the resistor referring back to the input. Again, it is a kTC noise but can be written as

$$4\frac{kT}{C_O}\frac{C_F^2}{T_S} = 4\frac{kT}{R_{EQ}}\frac{C_F}{C_O}, \tag{3.17}$$

and thus regarded as current noise generated by a resistor of value R_{EQ} and multiplied by the ratio C_F/C_O. Note this term is similar to (3.7) but it does not depend on either gate-source capacitances of input devices or stray input capacitance.

Depending on the product $R{\cdot}g_m$, the opamp noise may dominate the resistance noise, or vice versa. Indeed, the first term in (3.16) is dominant over the second one if

$$\begin{aligned}\frac{16}{3}\frac{kT}{C_O}\cdot\frac{C_T^2}{Rg_m T_S} >> 4\frac{kT}{C_O}\cdot\frac{C_F^2}{T_S} \Rightarrow \\ Rg_m << \frac{4}{3}\left(\frac{C_T}{C_F}\right)^2,\end{aligned} \tag{3.18}$$

which is exactly equivalent to (3.6), where A is the ratio C_T/C_F. Using (3.12) in (3.16) we can also infer that the first term in (3.16) is always lower than (3.7) since:

$$Rg_m > \frac{C_T}{C_F} \Rightarrow$$
$$\frac{16}{3}\frac{kT}{C_O}\cdot\frac{C_T^2}{Rg_m T_S} < \frac{16}{3}\frac{C_T}{R_{EQ}}\frac{kT}{C_O} \tag{3.19}$$

Note that (3.16) is valid if and only if the inequality in (3.12) is verified; otherwise the kTC noise-reduction technique does not work and (3.7) is still effective.

Summarizing, the input-referred noise PSD can be given by three different equations, depending upon the exact value of various parameters:

1- If (3.12) is not verified, the input-referred noise PSD is approximately given by (3.7) or (2.38). Actually, (3.7) underestimates the noise power since it does not take the noise generated by the resistor into account.

2- If (3.18) is true, then the noise generated by the OTA is the dominant factor and the input-referred noise can be simplified to:

$$\overline{i_N^2} \approx \frac{16}{3}\frac{kT}{C_O}\cdot\frac{C_T^2}{Rg_m T_S}; \tag{3.20}$$

3- If (3.18) is false, then the resistance noise is the dominant factor and the input-referred noise can be simplified to:

$$\overline{i_N^2} \approx 4\frac{kT}{C_O}\cdot\frac{C_F^2}{T_S}. \tag{3.21}$$

The above bounding conditions are described in Fig. 47, where equations (3.7) and (3.16) are compared to each other in function of either the product Rg_m or the ratio C_T/C_F. These design lines allow us to make some straightforward conclusions. We cannot arbitrarily lower the noise PSD acting on product $R{\cdot}g_m$, because for high values the OTA noise becomes negligible so (3.21) becomes the more accurate formula. Therefore, (3.21) expresses the theoretical lower limit for the input-referred noise PSD. However, it is very hard to work in that region, since it needs either a high value resistor R (lowering the effective bandwidth), or a low capacitance C_T (mainly depending on parasitic elements). Equation (3.20) seems more prone to stray capacitances since it depends upon C_T with square function; however, if we increase the input capacitance too much, (3.20) is no longer valid because the

pole associated with the opamp becomes dominant, and thus we fall again in the region of (3.3).

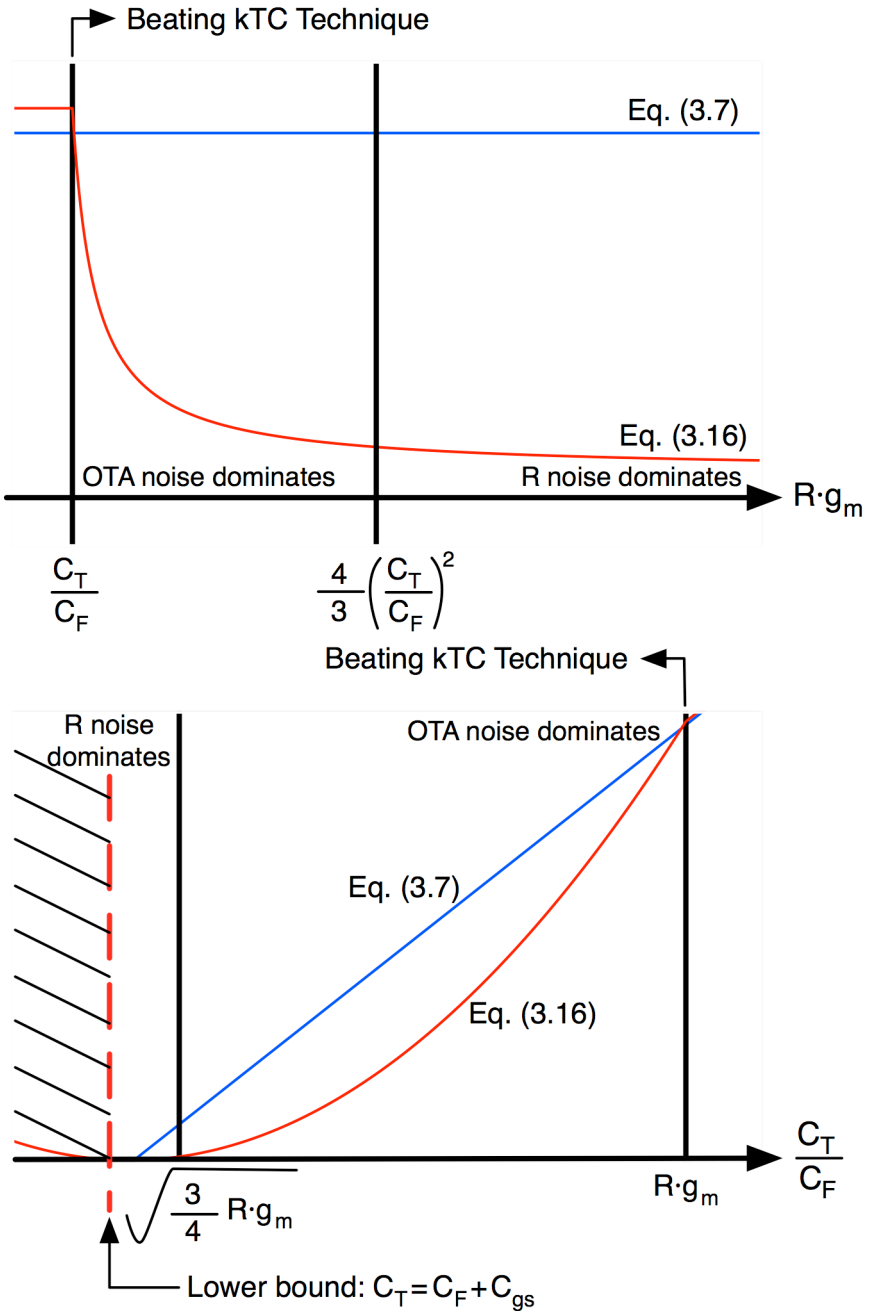

Fig. 47 Design lines showing the amplitude of the input-referred noise as function of parameters R, g_m, C_F, and C_T. Both graphs compare (3.7) with (3.16), directly showing the effect of kTC noise reduction technique. Depending upon both the product Rg_m and the ratio C_T/C_F, equation (3.16) can be simplified to (3.20) where OTA noise dominates, or to (3.21) where resistor noise dominates. At the left of C_T/C_F mark point in the top graph, equation (3.16) is not valid anymore since the dominant pole is set by the OTA; therefore the red line is modeled by (3.7) plus the extra noise due to the resistor. Note that the C_T design line have an unbreakable lower bound corresponding to negligible stray capacitances.

Finally, there also are some practical constraints related to the CDS behavior. Since the CDS is a discrete-time circuit, there is a strong relation between the desired accuracy and the time constant, given by:

$$f_R T > \frac{(ENOB+1)\ln 2}{\pi}, \tag{3.22}$$

where T is the available settling time [Schreier,04]. Substituting (3.11) into (3.22) we can get a new bound on the resistance value:

$$R < \frac{1}{2\ln 2} \cdot \frac{T}{C_O} \cdot \frac{1}{ENOB+1}. \tag{3.23}$$

Since the CDS takes the first noise sample just at the beginning of the integration period, the available settling time is short and thus (3.23) is a strong limitation.

Chapter 4

DC-Transient Current Sensing: A Ultra Low-Noise IC Design

This chapter presents an ultra low-noise CMOS current-sensing interface intended for parallel recording of single ion channels in high throughput screening (HTS) applications. The proposed electronic system is an evolution of the current-sensing interface presented in section 1.4, displying better performance and more features. It implements the kTC noise reduction technique, proving the theory described in chapter 3 and achieving an input-referred noise power spectrum density (PSD) as low as state-of-the-art instrumentations. Moreover, the system incorporates many suggestions and recommendations from final users, including chemists, biologists, and electrophysiologists. With these improvements the electronic interface is highly suitable for real applications.

Ion channel proteins play a pivotal role in a wide variety of physiological processes and chronic diseases and are consequently of considerable interest to the pharmaceutical industry [Ashcroft,06], [Clare,10]. Electrophysiology gives the most detailed information about the function of ion channels and their modulation by pharmaceutical drugs and is the only method that enables the characterization of voltage-gated channels. It involves placing an electrode on either side of a membrane and measuring the current flow through the membrane-embedded channels, which is typically between 1 and 150pA per channel. The challenges are to obtain a "Gigaseal" microfluidic configuration where the two aqueous compartments are electrically insulated

from each other by a stable lipid bilayer, and to design an electronic interface able to read the low currents with a signal-to-noise-ratio (SNR) and a bandwidth suitable for study ion channels relevant for the human being, such as sodium ion channels. Those are difficult to achieve, making conventional electrophysiology a laborious process with a notoriously low throughput.

In collaboration with the University of Southampton, we are developing an array of completely independent suspended bilayers, intending to demonstrate the potential of bilayer lipid membranes (BLMs) for high-throughput drug screening. The project is based on the success and the outcomes of an earlier program and it is divided exploiting our preexisting know-how, since the research is highly interdisciplinary. The research group of the University of Southampton, supervised by Prof. H. Morgan, works through the design of a 96-well microfluidic platform; while our research group, supervised by Prof. M. Tartagni, develops a new IC for low-noise current sensing. The electronic interface is based on our previous work [Bennati,09], employing new techniques (such as the kTC noise reduction technique) to achieve the desired performance and incorporating many advices from electrophysiologists so as to improve the usability.

First section presents the big picture of the system, summarizing the general functionalities and the main specifications. Section two, three and four analyze in detail the core circuit blocks, which are the current amplifier along with the CDS, the analog-to-digital converter, and the offset correction loop. Finally, section five presents some preliminary results from CAD simulations.

4.1 Single Ion Channel Interface

4.1.1 Big Picture

Sodium-ion channels are very interesting membrane proteins with influences on many different cells, such as neurons and cardiac myocytes. They are described by a typical conductance from ten to hundred pS, so by a current in the order of one to ten pA. Moreover, for a high electrophysiology understanding of the channel, the electronic system should be able to acquire signals from DC to tens of KHz. It is evident that our first current-sensing

amplifier, described in section 1.4, is not suitable for such high performance; thus a novel electronic interface is required. We took that opportunity to solve many bugs existing in the old IC and to implement new features so as to simplify the usability and empower new electrophysiology experiments.

The general block scheme of the new CMOS current-sensing interface is depicted in Fig. 48. It implements a charge-sensitive amplifier based on the discrete-time approach (i.e. with periodical reset pulse). A low-pass filter is added after the charge-sensitive amplifier (CSA) so as to realize the noise reduction technique, achieving the sodium channel requirements on the SNR. A new correlated double sampling (CDS) scheme has been developed; it is highly precise and it is able to shift the output signal voltage so as to refer it to a stable common-mode voltage. A 2nd-order low-pass delta-sigma analog-to-digital converter is used to keep the quantization noise beneath the thermal noise and minimize the effects of limit cycles. Finally, the system integrates a digital loop for electrode offset correction.

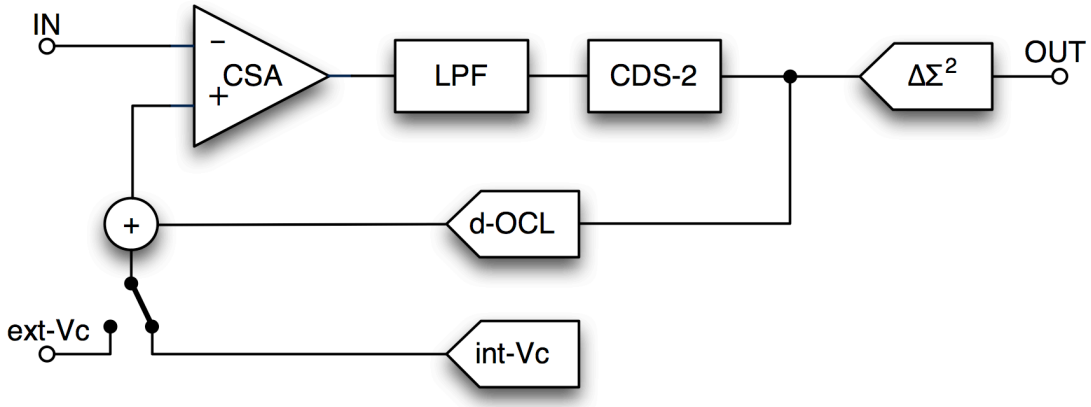

Fig. 48 Block scheme of the new low-noise current-sensing interface intended for single ion channels acquisition. The foremost blocks will be covered in the next sections. Section 4.2 describes the analog acquisition path, composed of a CSA, a LPF and a CDS. Section 4.3 presents the second order delta-sigma modulator. Section 4.3 shows the architecture of the digital offset correction loop (d-OCL) and describes the design of the analog adder.

4.1.2 System Specifications

The system allows the application of the voltage stimulus signal through the working electrode (WE) meanwhile it keeps the counter electrode (CE) at ground voltage (Fig. 49). This can be easily done exploiting the virtual short circuit of the operational transimpedance amplifier (OTA) used in the CSA, although it complicates the CDS as will be described in section 4.2.3. This solution ensures better shielding of the biological sample and is very suitable

for parallel recording of single ion channels, because it keeps the individual channel-spots separate, allows the use of a single CE for the whole system, and simplifies the design of the microfluidic array platform. The stimulus signal can be either generated internally (by a digital-to-analog converter), or externally to the chip (through a dedicated signal generator). In both cases, the command signal must be limited to ±250mV to keep the OTA working in the linear region.

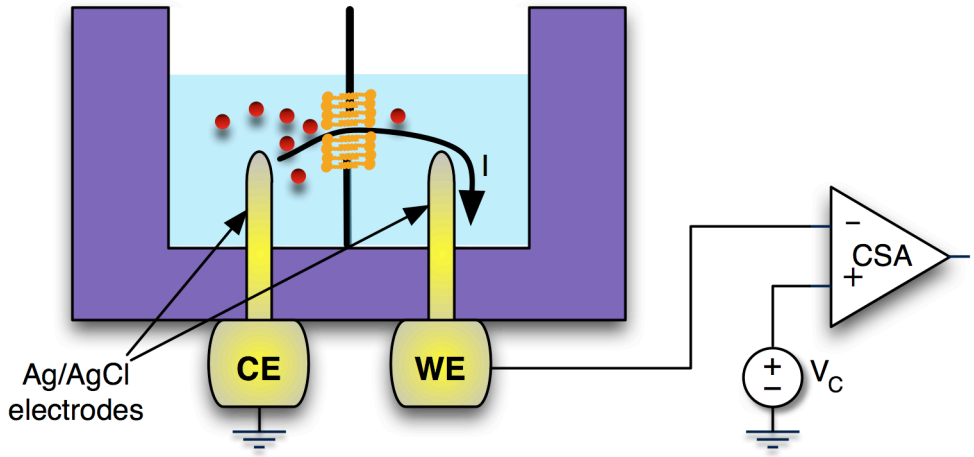

Fig. 49 Experimental set-up with CE connected to ground and WE used for both stimuling and signal acquisition.

Each IC integrates a digital offset correction loop (d-OCL) to improve the acquisition accuracy [Thei,10b]. The approach will be described in section 4.4.

The system requires a dual power supply (-1.65V - +1.65V) in order to acquire bipolar currents while using ground voltage as reference at the CE. Although, the IC admits single power supply (0V – 3.3V) if the CE is connected to the internal generated common-mode voltage *Vcm*.

The new interface acquires current signals over four different selectable bandwidths: 625Hz, 1.25KHz, 5KHz and 10KHz, and two input ranges: ±200pA and ±20nA. For testing and laboratory purposes, the system permits to deactivate its internal discrete-time feedback and activate an external resistive feedback. In this way, the system gains more flexibility over input ranges and bandwidths. Capability of working until 20KHz is permitted by either external feedback or raising the system clock frequency from 10MHz to 20MHz.

Exploiting the kTC noise reduction technique, the system achieves an input-referred noise current of approximately 22fArms at 1KHz, comparable to the state-of-the-art instrument [Axon,08].

Specification	Value
Power Supply	0V - 3.3V / -1.65V - +1.65V
Input Ranges	±200pA / ±20nA / external
Bandwidth	625Hz / 1.25KHz /5KHz / 10KHz / 20KHz / external
System Clock Frequency	10MHz / 20MHz
Maximum Stimulus Signal	±250mV
Offset Compensation	Integrated
Input-referred rms Noise Current	22fA @ 1KHz

Table 3 General specification of the proposed current-sensing interface.

4.2 Discrete-Time Current Amplifier

4.2.1 Architecture

In Fig. 50 is shown a schematic diagram of the analog acquisition chain of the implemented discrete-time current-sensing interface.

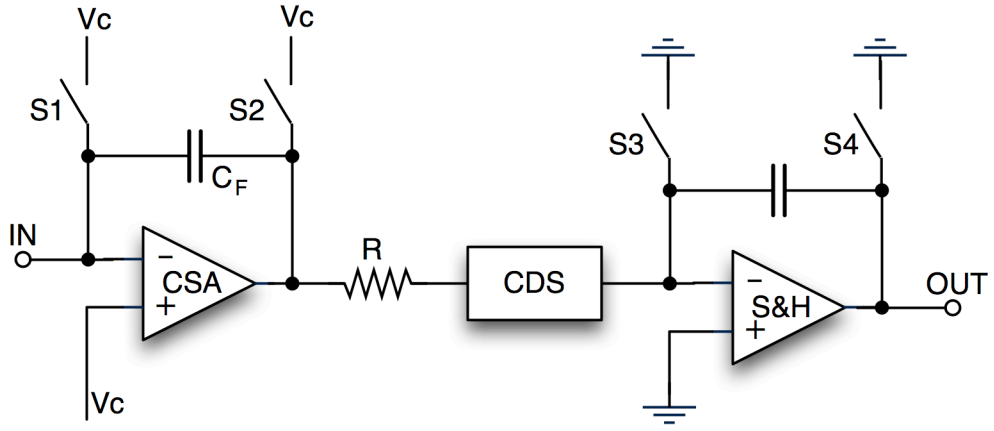

Fig. 50 Schematic of the implemented discrete-time current-sensing interface. It shows only the analog acquisition path consisting of the CSA, the resistor for the noise reduction, the new CDS and the S&H.

The system has a precise and controlled time behavior that is arranged in equal time frames of period *Ts*. Each time frame is divided into three phases: a reset phase, a noise-sampling phase and an integration phase (Fig. 51). During the reset phase, the switches S1, S2, S3 and S4 are closed, resetting the

charge stored in the feedback capacitances of the CSA and the sample and hold (S&H). The use of two switches for the reset of each stage reduces the charge injection, because they are connected to the reference node that is characterized by low impedance. While the reset switches are active, the system does not acquire the input current; therefore the reset phase should be as short as possible to minimize the loss of data. Hence, we have set the reset period to 200ns.

During the noise-sampling phase, the CDS samples the noise, the offset and the charge injection. This phase cannot be too short, because it needs to sample the noise with sufficient accuracy. At the same time, it cannot be too long, otherwise the integration phase will be significantly reduced. To cope with that trade-off, we opted for a constant noise-sampling phase lasting 6.4μs.

During the integration phase the CSA integrates the input current, and the CDS subtracts the pre-stored noise sample. The integration phase is the most important, because it is the only one concerning the input signal. Actually, it sets the equivalent resistance of the system, according to (2.32), affecting the input-referred noise PSD as stated in (2.38) or (3.20). Therefore, the integration phase should last as much as possible.

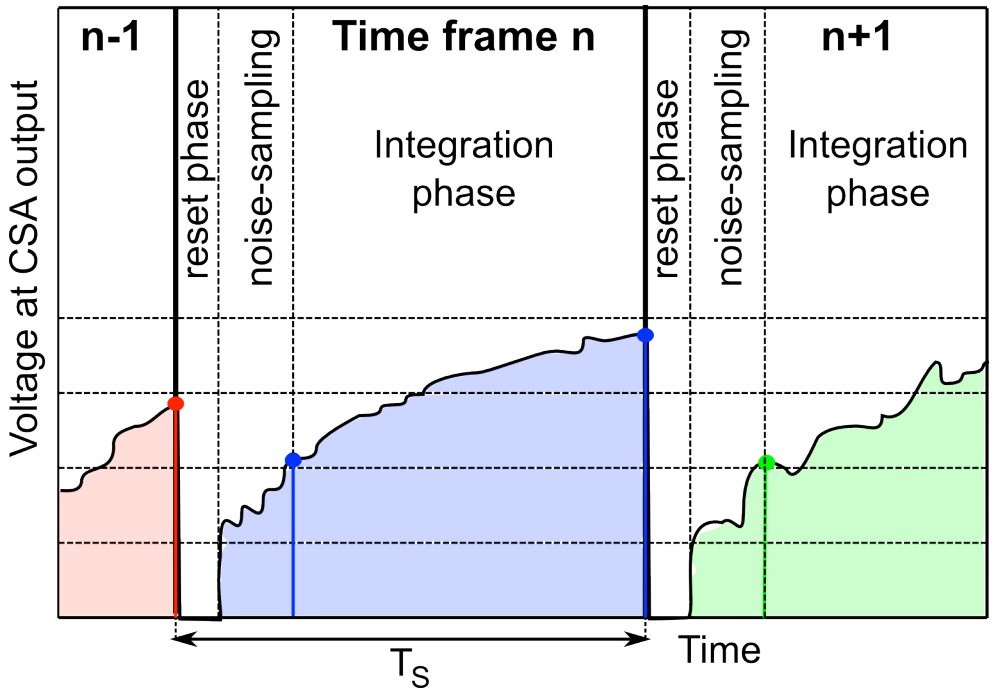

Fig. 51 Timing behavior of the discrete-time current amplifier. It is arranged in time frames of period T_S. Each time frame is divided into three phases: the reset phase, the noise-sampling phase and the integration phase.

The stimulus voltage signal V_C is applied to the positive input of the OTA used in the CSA. As stated above, this is an essential feature with a lot of advantages from the microfluidic and experimental point of view; however, it creates some design issues. First of all, the voltage actually applied to the ion channel is affected by the OTA input offset, although it will be compensated by the offset correction loop. Moreover, the voltage signal at the CSA output is referred to the V_C voltage and cannot be directly provided to the delta-sigma converter. Therefore, the CDS must be able to subtract the stimulus signal, complicating its own circuit scheme. Since V_C is applied directly to the input of the system, it should be a stable and noise-free signal. However, it is also used as reference in many switches (e.g. S1 and S2), creating unavoidable voltage bump and interferences. Therefore, it is mandatory to use a buffer in order to create a V_{C2} signal, separating the positive input of the OTA from the other connections. Finally, the OTA limits the swing of the stimulus signal to ±250mV, which is its own common-mode input range.

The circuit implements the kTC noise reduction technique described in chapter 3. It uses a simple polysilicon resistor to decouple the OTA noise density from the equivalent noise bandwidth (EQNB) (Fig. 50). However, settling and accuracy issues upper limit the resistance value. Following (3.23), we chose a 17KΩ resistor so as to settle with at least 13 bit of accuracy in 6.4μs. According to (3.20), we can lower the noise acting on parameter g_m, which means to design a new operational amplifier with higher transconductance. Employing this technique, the system can achieve an input-referred noise current lower than 1fA/√Hz, as will be demonstrated in this chapter.

4.2.2 Ultra Low-Noise CMOS Single-Ended OTA

The schematic of the designed OTA is illustrated in Fig. 52. It is a high-swing folded-cascode single-ended OTA. It is not the optimum topology but shows a high gain and it is simple to design. The OTA is implemented in 0.35μm CMOS technology. Although Bipolar transistors show higher gain, lower Flicker noise, lower power consumption and lower input-referred offset, the fully-CMOS technology shows the best cost-performance trade-off for the intended application.

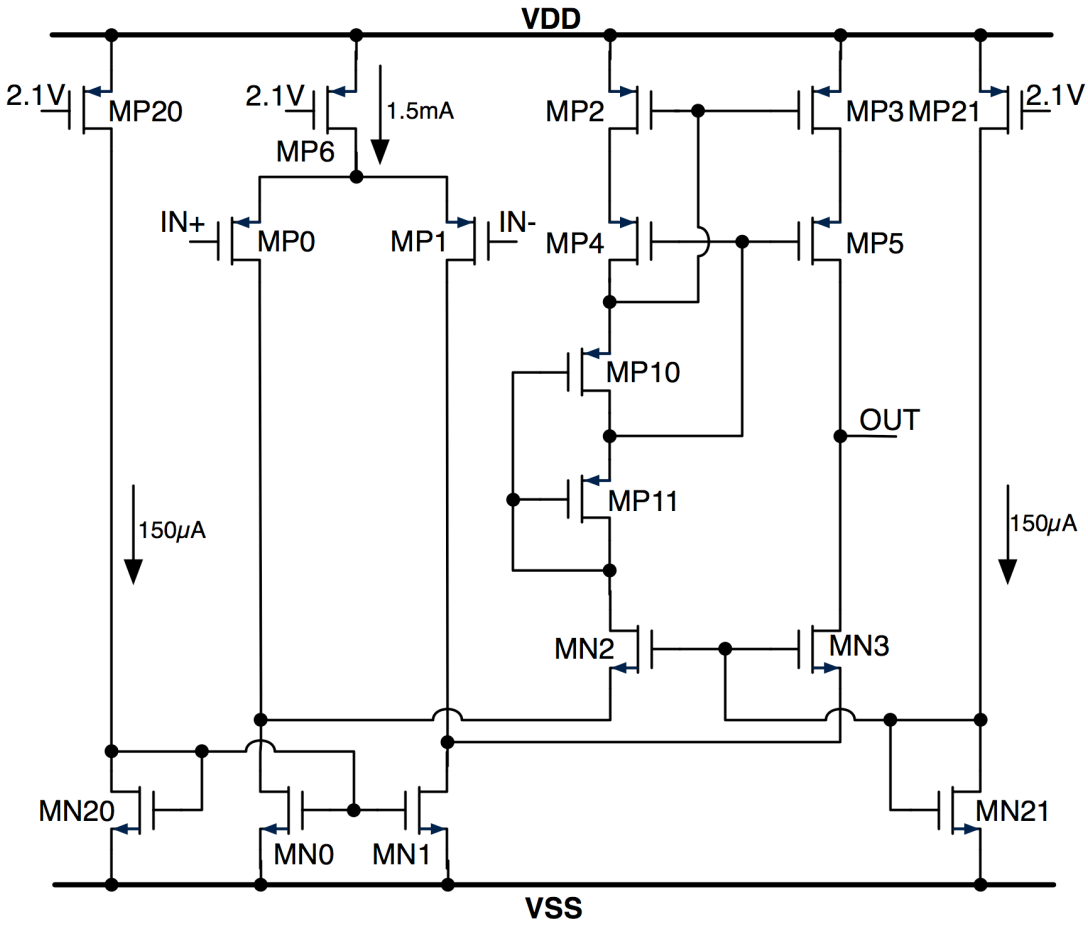

Fig. 52 Schematic of the low-noise single-ended OTA. It is a standard folded-cascode architecture, employing the Sooch current mirror as active load to enlarge the output swing.

Since we cannot use a big resistor, we ought to design a new OTA with a high transconductance to fulfill the noise-reduction technique; therefore, the primary target is to achieve a transconductance g_m in the order of one to ten mA/V, and thus an input-referred thermal noise voltage of approximately 1 or 2nV/√Hz. Due to the undersampling operation of the CDS, the thermal noise sets the noise floor of the system. However, the Flicker noise could not be excessive, otherwise it will fold back significantly. To limit the *1/f* noise and focus only on the white noise, we implemented the OTA with a pMOS input differential pair.

Each transistor in Fig. 52 is potentially a source of noise, but we want to minimize the input-referred noise only to the one generated by the input pair. At low frequencies the noise contribution of cascoded devices is negligible and the input-referred thermal noise voltage can be quantified as

$$\overline{e_{n-op}^2} = \frac{16}{3}kT\left(\frac{1}{g_{mp1}} + \frac{g_{mn1}}{g_{mp1}} + \frac{g_{mp3}}{g_{mp1}}\right), \tag{4.1}$$

where g_{mp1}, g_{mn1}, and g_{mp3} are the transconductances of the input pair, the bias transistors MN0 – MN1, and the load transistors MP2 – MP3, respectively [Razavi,01]. Therefore, the transconductances of the devices MN0, MN1, MP2 and MP3 must be at least one order of magnitude lower than g_{mp1}.

Under this assumption, the transconductance of the input pair should be in the range

$$g_{mp1} = \frac{16}{3}\frac{kT}{\overline{e_{n-op}^2}} \quad \Rightarrow \quad 5.5m{}^{A}\!/_{V} < g_{mp1} < 22m{}^{A}\!/_{V}, \tag{4.2}$$

to achieve an input-referred noise of approximately 1 or 2nV/√Hz. Clearly, such a high transconductance requires high power consumption. Although HTS is not a power-aware application, we decided to limit the total current consumption of the OTA to 2mA: 1.5mA flowing into the input pair, 200μA into the folded branches and the remaining 300μA into the bias circuitry. Setting the overdrive voltage to a reasonable value of 0.2V, the transconductance is

$$g_{mp1} = \frac{2I_D}{V_{OV}} = 7.5m{}^{A}\!/_{V}, \tag{4.3}$$

perfectly fitting the requirements. Using the quadratic model for the drain current flowing in a MOS device, we can get the form factor for the input pair:

Devices	W/L (μm)	I_D (μA)
MP0, MP1	350/0.6	750
MP2, MP3, MP4, MP5, MP11	144/1.3	100
MP10	38.9/1.3	100
MP6	385/1.4	1500
MN0, MN1	60.2/2	850
MN2, MN3	130.25/3.5	750

Table 4 Sizing and drain currents for the transistors used in the OTA of Fig. 52.

$$S_{P0,1} = \frac{2I_D}{\beta'_P V_{OV}^2} = 580. \tag{4.4}$$

This OTA will be employed in a discrete-time (DT) current-sensing interface using the noise-reduction technique described in chapter 3, for which the total input-referred noise PSD is given by (3.20). Thus, the input capacitance of the OTA must be optimized following (2.18). A fair estimation of the input stray capacitance, for a well designed layout, is of approximately 500fF [Ferrari,09]; however, the system uses different feedback capacitances depending on the selected input range and signal bandwidth. Therefore we decided to optimize the OTA for a compromising value of 1.5pF, leading to an input capacitance of the OTA of 550fF. Combining the form factor of (4.4) with the optimized input capacitance, we sized the input pair devices as $W=350\mu m$ and $L=0.6\mu m$.

Another important specification is the output voltage swing V_{OM}, affecting the dynamic range (DR) of the current-sensing interface, as displayed in (2.39). In the old current-sensing interface, which is described in section 1.4, the voltage range was only ±210mV; hence, we decided to increase it to ±450mV that is the allowed voltage range for the delta-sigma converter (section 4.3). The folded-cascode topology is an optimum choice for high gain OTA, but the output swing is limited by the cascoded stage.

Parameter	Schematic Simulation	Post-layout Simulation
GBW @C_L=18pF	41.5MHz	41.3MHz
A_{DM}	88dB	87dB
PM	60°	61°
A_{CM}	-18dB	7dB
CMRR	106dB	81dB
PSRR	80dB	61dB
$e^2_{n\text{-}op}\,|_{thermal}$	2.7nV/√Hz	3nV/√Hz
Corner Frequency	30KHz	30KHz
Output DR	-0.7V - +1.15V	-0.7V - +1.15V
CM Input Range	-250mV - +250mV	-250mV - +250mV
Input Offset	±500μV	±3mV
Non Linearity	-85dB	-85dB

Table 5 Summarize of primary performances of low-noise OTA.

To maximize V_{OM} we used a Sooch current mirror, allowing a voltage swing from -0.7V to 1.15V [Gray,01]. With hindsight, the Sooch mirror was not a good choice because it increases the input offset and the nonlinearities, creates stability issues and reduces the CMRR.

Table 4 summarizes the dimensions and the drain currents for each transistor depicted in Fig. 52. The exact sizing of the transistors was adjusted during both transistor level simulation and layout design, taking into account the more complex model used by the circuit simulator and the extracted parasitic elements. Unfortunately, this adjusting process increased the transconductance of some devices, like MN1, affecting the input-referred noise voltage given by (4.1). Table 5 summarizes the global performance achieved by the designed OTA.

4.2.3 Enhanced Correlated Double Sampling

The CDS implemented in this new current-sensing interface is more complex than the one presented in [Bennati,09] for two main reasons:

1- The CDS subtracts both the pre-stored noise sample and the reference voltage;
2- The CDS is designed to maximize the integration period by a reduction of dead times.

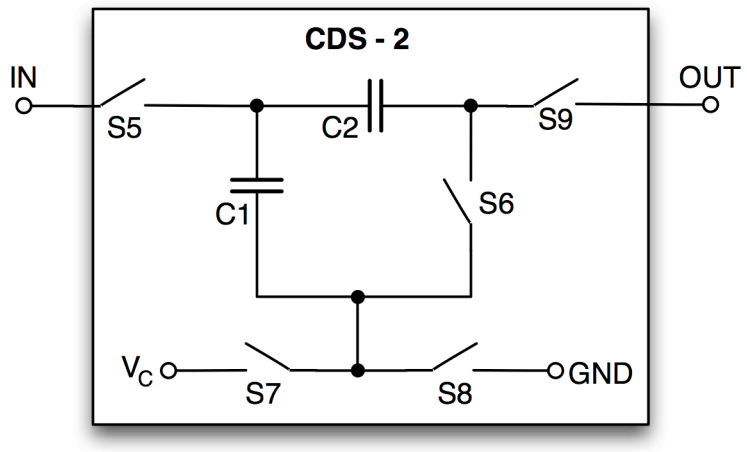

Fig. 53 Schematic of the enhanced correlated double sampling scheme. It reduces the low frequency noise and subtracts the *Vc* signal so as to refer the output signal to ground. During the integration period the switch S7 is closed, referring all the voltages to VC; when the CDS transfers the charge to the S&H the switch S8 is closed, so as to refer the voltages across the capacitors C1 and C2 to GND.

To cope with the first point, two alternating switches have been added as shown in Fig. 53. During the integration period the switch S7 is closed, referring all the internal voltages to V_C; when the CDS transfers the charge to the S&H the switch S8 is closed, so as to refer the voltages across the capacitors C_1 and C_2 to *GND* (i.e. the common-mode voltage for dual supply).

Other than sample the signal and subtract the pre-stored noise, the CDS has to change the reference voltage, transfer the charge to the S&H and reset its own internal nodes. All those features require time to be accomplished, especially if the employed capacitors are relatively large, reducing the integration time of a significant amount. To eliminate those dead times, pipeline architecture, with two equal CDS stages, was implemented.

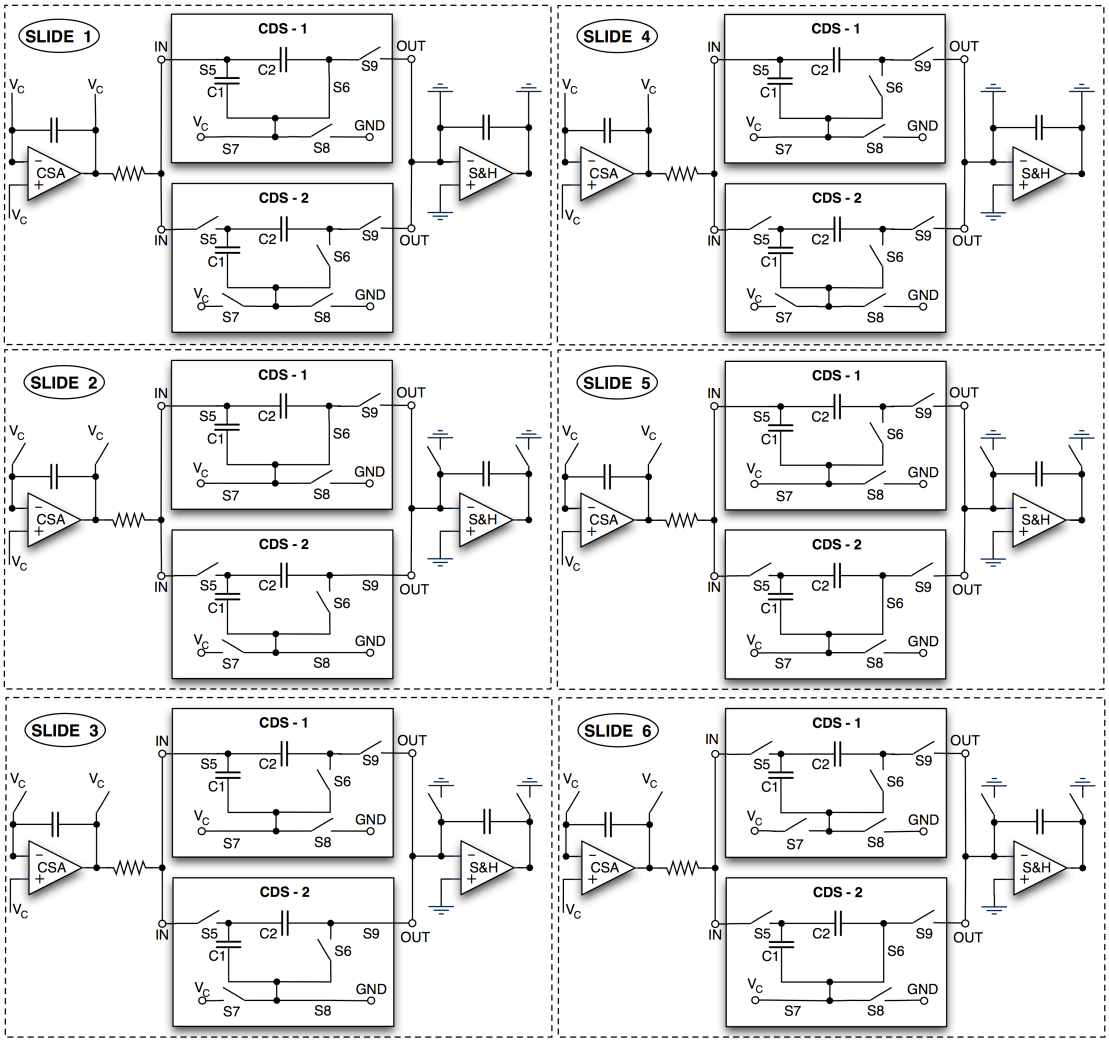

Fig. 54 This picture shows the switching activity of the CDS pipeline through a complete time frame. Slide 1 shows the reset of both CSA and S&H (reset phase). In slide 2 CDS1 starts the noise-sampling phase, while CDS2 transfers the charge to the S&H. In slide 3, CDS1 samples the noise and starts the integration phase. In slide 4, the charge transfer of CDS2 ends, while CDS1 is still in the integration phase. In slide 5 the CDS2 resets its internal nodes, preparing for the next time frame. In slide 6, CDS1 ends the integration phase with the sample of the input signal. The slide succession starts again with CDS1 and CDS2 interchanged.

To better understand the proposed CDS, Fig. 54 shows an example of signal elaboration through a complete time frame. The time frame starts with the reset of both CSA and S&H (slide 1). Later, CDS1 is connected to the CSA and the noise-sampling phase begins, meanwhile, CDS2 changes the reference voltage to *GND* (S7 is open and S8 is closed) and transfers to the S&H the charge stored during the preceding time frame (slide 2). After 6.4μs, the switch S6 in CDS1 opens, sampling the noise, the offset and the charge injection. Immediately after, the integration phase starts (slide 3). CDS2 stays connected to the S&H for 18.7μs, although the charge transfer takes approximately 400ns. Therefore, it is disconnected from the S&H while CDS1 is still in the integration phase (slide 4). Later, switches S6 and S7 in CDS2 are closed, resetting the nodes to V_C voltage (slide 5). Finally, switches S7 and S5 in CDS1 open in succession, sampling the difference between the final CSA output and making the difference with the pre-stored noise sample (slide 6). The slides succession starts again with CDS1 and CDS2 interchanged.

The pipeline solution maximizes the integration time but needs two CDS stages very well matched, otherwise an undesired square-wave will appear at the S&H output. To maximize the matching we used quite big capacitances (8pF each one) arranged in a common-centroid layout.

With an input-referred noise of solely 22fArms, as claimed in section 4.1.2, imperfections and errors in the CDS become noteworthy. The main source of error is the charge injection due to the many switches in the circuit. To cope with this, we designed complementary switches with dummy structures and we optimized them for voltages around *GND* [Razavi,01]. Moreover, we designed the digital signals, which command the switches, so as to realize the back-sampling technique, proving a further reduction of the charge injection [Haigh,83]. The diagram of Fig. 55 shows the timing of the digital signals for 5KHz working frequency. Using all the above-cited techniques, the final error due to CDS behavior is of approximately 22μV, corresponding to an input current error less than 10fA (note this is just an estimation, matching issue during the chip layout will increase this error).

Fig. 55 The signal A commands the reset phase of CSA and S&H. The signal C selects the active CDS stage during the integration phase. All the other signals control the switches inside each CDS stage.

4.2.4 Adaptive Phases

If the feedback capacitance C_F is negligible compared to total input capacitance C_T, then the increase of the sampling time T_S has a positive effect on the input-referred noise PSD, as shown by (3.20) here reported as (4.5)

$$\overline{i_N^2} \approx \frac{16}{3}\frac{kT}{C_O}\cdot\frac{C_T^2}{Rg_mT_S}; \tag{4.5}$$

This is somehow unexpected, because a reduction of the sampling frequency proportionally increases the amount of the folding noise. However, a higher sampling period results also in an higher equivalent resistance R_{EQ} of the system, following the equation

$$R_{EQ} \cong \frac{T_S}{C_F}. \tag{4.6}$$

With an output voltage range V_{OM} set by the rails of the delta-sigma modulator, the equivalent resistance cannot rise, thus the feedback capacitance must follow the growth of the sampling period, reducing the amplification factor of the noise generated by the opamp, which is the first term inside brackets in (3.15). Since the last cited is a quadratic relation, the final result is a reduction of the input-referred noise PSD.

To benefit from that, the digital signals used in the CDS were designed to be scalable with the sampling frequency. In this way, while changing the acquisition bandwidth, the CDS changes the sampling frequency and the periods of all the other control signals, preserving the time behavior described in section 4.2.3. That reasoning is mainly applicable to the ±200pA input range, which has feedback capacitances lower than 300fF.

In case the feedback capacitance C_F is the dominant contribution over C_T, then (3.20) is no longer usable and (3.21) becomes the right formula for the input-referred noise PSD, where the leading noise component is the one due to the resistance. Therefore, the growth of the sampling period has only a negative effect on the input noise PSD, due to the folding of high frequency thermal noise. This latter effect has to be taken into account for the ±20nA range, which has feedback capacitances greater than 2pF.

Finally, it is to point out some little differences between the 10KHz operation and the others bandwidths. If the 10KHz bandwidth is chosen, the time frame lasts 50μs only; thus the noise-sampling period is reduced to 1.6μs, and a 6KΩ resistor replaces the 17KΩ resistor (Fig. 56).

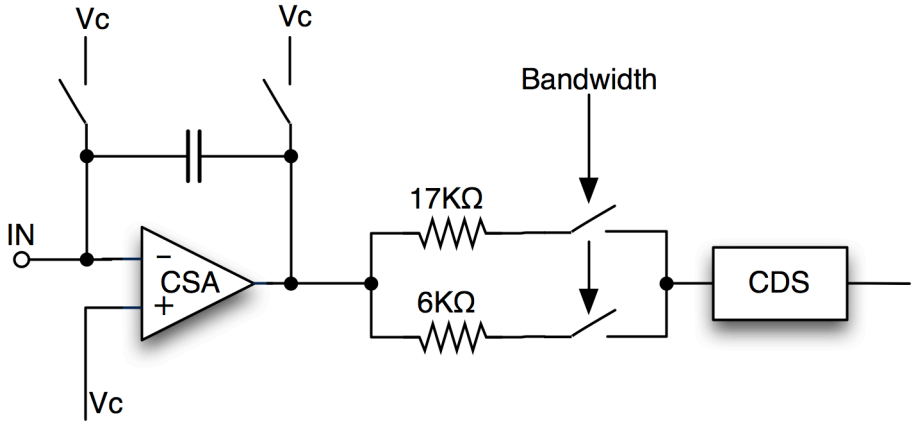

Fig. 56 Scheme of first stages of the current-sensing interface, underlying the presence of two different filtering resistors to cope with different bandwidths. The 6KΩ resistor is enabled only when the 10KHz bandwidth is selected; the 17KΩ resistor is enabled in all the other cases. The CDS stage depicted incorporates the pipeline structure.

4.3 Second-Order Delta-Sigma Modulator

4.3.1 Basic Principles of Delta-Sigma Modulation[9]

The delta-sigma modulator is an oversampling analog-to-digital converter (ADC). It has been originally used in high-resolution audio applications, and now it is widespread in many other applications. The modulator benefits from both oversampling and noise-shaping to obtain high resolutions.

Given a signal with bandwidth B, the delta-sigma modulator samples it at a frequency f_S given by

$$f_S = OSR \cdot 2B, \tag{4.7}$$

where OSR is the oversampling ratio. In this way the quantization noise power is spread over frequencies from DC to $f_S/2$. Then, a digital filter removes the noise from f_B to $f_S/2$, leading to a quantization noise power P_Q given by

[9] The main topics of this section are taken from [Schreier,04] and [Maloberti,07].

$$P_Q = \frac{V_{LSB}^2}{12} \cdot \frac{2f_B}{f_S} = \frac{V_{LSB}^2}{12} \cdot \frac{1}{OSR}. \tag{4.8}$$

In terms of signal-to-quantization-noise-ratio (SQNR) and equivalent number of bits (ENOB), the (4.8) results in

$$SQNR\big|_{dB} = 6.02N + 1.76 + 10\log\left(OSR\right), \tag{4.9}$$

$$ENOB = N + 0.5\log_2\left(OSR\right), \tag{4.10}$$

where N is the number of bits of the quantizer. Equation (4.10) clearly shows that an increase of the OSR by a factor of four improves the resolution by 1bit. However, it requires a very high OSR to achieve a significant improve in terms of number of bits.

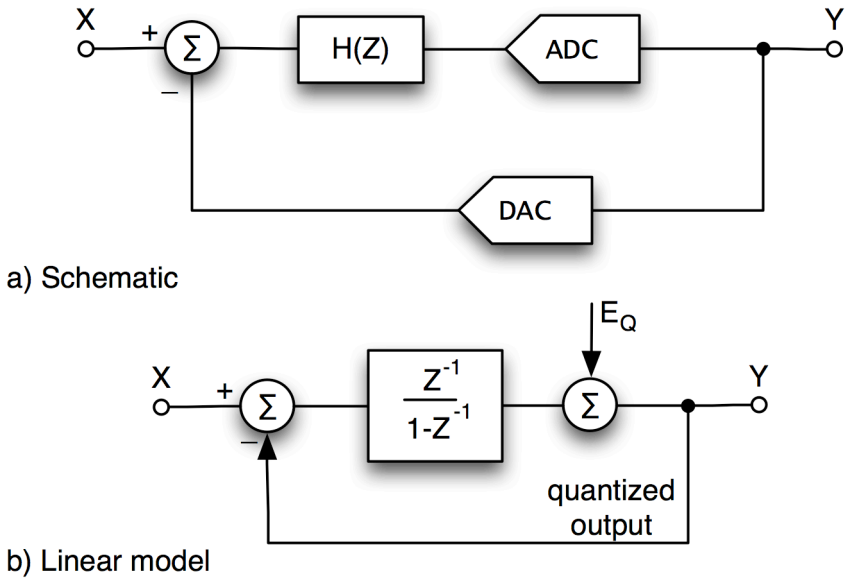

Fig. 57 a) Basic circuit of a 1st-order delta-sigma modulator. It is composed of an integrator described by the discrete transfer function $H(Z)$, an ADC (for the 1-bit modulator it is a simple comparator) and a DAC in the feedback loop. b) Equivalent linear model of the 1st-order delta-sigma modulator.

The noise-shaping technique uses a negative feedback to reshape the noise. Fig. 57 a) shows a scheme of a 1st-order delta-sigma modulator, consisting of an integrator, a quantizer (for the 1-bit modulator it is just a comparator) and a 1-bit digital-to-analog converter (DAC) in the negative feedback loop. Assuming the quantization noise is white shaped and looking at the linear model of Fig. 57 b), it is possible to compute the signal transfer function (STF) and the noise transfer function (NTF) as

$$STF(z) = \frac{Y(z)}{X(z)} = \frac{H(z)}{1+H(z)} = z^{-1}, \tag{4.11}$$

$$NTF(z) = \frac{Y(z)}{E_Q(Z)} = \frac{1}{1+H(z)} = 1 - z^{-1}. \tag{4.12}$$

While the signal goes through a low-pass filter as stated in (4.11), an high-pass transfer function (4.12) shapes the quantization noise: it lowers the noise density in the band of interest in spite of an increase of the out-of-band noise (Fig. 58). Having more noise in high frequency regions is not problematic, because the digital filter used after the ADC will remove it. Integrating the shaped noise from DC to B, we can lead to a new formula for the SQNR of a 1-bit delta-sigma modulator:

$$SQNR\big|_{dB} = 6.02 + 1.76 - 5.17 + 30\log(OSR). \tag{4.13}$$

Now, doubling the OSR will improve the SQNR of approximately 9dB, which means an increase of the ENOB by 1.5bit. The SQNR of a delta-sigma modulator can be further improved using quantizer with more than 1 bit (complicating both quantizer and DAC), or increasing the number of stages around the loop (higher-order modulator).

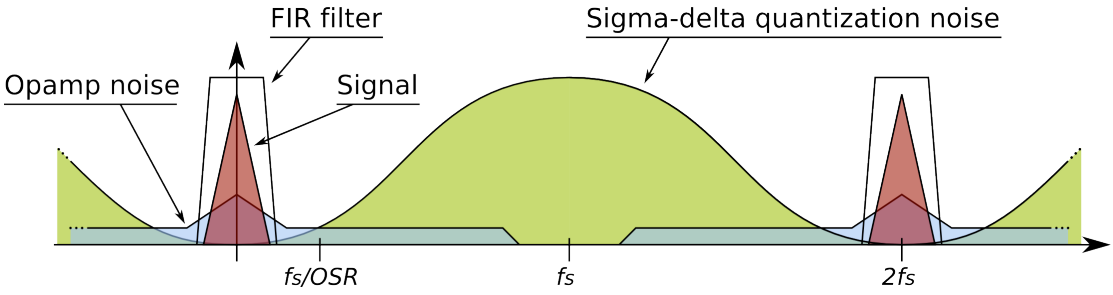

Fig. 58 Representation of the power spectrum densities in a delta-sigma modulation. The signal power is centered at zero frequency and has a bandwidth B much lower than the sampling frequency. The quantization noise is shaped so as to lower its density in the signal bandwidth.

The output of 1-bit delta-sigma modulators is a digital 1-bit data stream at a sampling frequency f_S higher than the Nyquist frequency. Operating at this high frequency causes a waste of power in the digital domain. Therefore, the digital filter after the ADC acts twofold: it removes the high frequency noise and decimates the data to get the proper frequency.

The possibility to trade bandwidth for resolution by changing the OSR is the best feature of delta-sigma modulators. Moreover, they show an intrinsic

good linearity and a high tolerance to imperfections of the analog components.

4.3.2 Architecture

A main drawback of delta-sigma modulators is the presence of limit cycles, also known as idle tones. For a DC input signal equal to zero (i.e. placed in the middle of the delta-sigma full-scale range), the output of the modulator is a periodic sequence of zeros and ones, with an average output equal to zero, exactly as the input. Adding a small voltage ε to the input signal, the output becomes a sequence of zeros and ones like before, but two successive ones, placed at each K samples, interrupt the sequence. Filtering the output stream we get a DC signal equal to ε plus an idle tone at frequency $f_S/2K$, where the lower the ε the higher is the K [Schreier]. (Fig. 59)

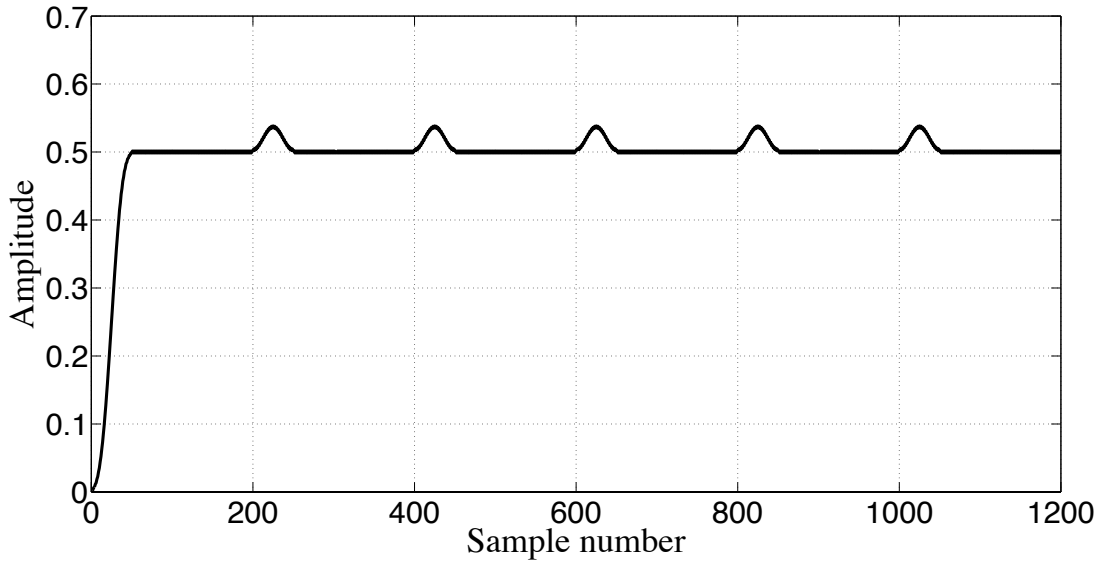

Fig. 59 Simulation of an idle tone in a 1st-order delta-sigma modulator using a sinc filter as LPF.

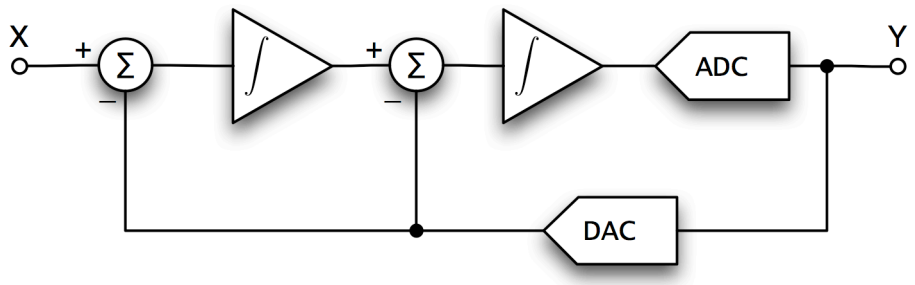

Fig. 60 Block scheme of the designed 2nd-order delta-sigma modulator. The scheme is rather standard and uses switched-capacitor integrators.

To ease that drawback, as well as other limitations like dead zones, we designed a 2nd-order delta-sigma modulator. The scheme of the implemented delta-sigma modulator is rather standard and it is depicted in Fig. 60. It uses two switched-capacitor integrator stages in the feedback loop, leading to the same STF of a 1st-order modulator but to an NTF equal to

$$NTF(z) = \frac{Y(z)}{E_Q(Z)} = \left(1 - z^{-1}\right)^2, \tag{4.14}$$

Equation (4.14) is the square of (4.12), resulting in an increased attenuation of the quantization noise at low frequencies. Indeed, the SQNR for a 2nd-order 1-bit delta-sigma modulator is given by:

$$SQNR\big|_{dB} = 6.02 + 1.78 - 12.9 + 50\log(OSR), \tag{4.15}$$

ensuring an increase of 15dB (or alternatively 2.5bit) for every doubling of the oversampling ratio.

The implemented 2nd-order delta-sigma modulator works at a sampling frequency of 1.25MHz and allows us to choose the *OSR* among four values: 64, 128, 512 and 1024 for signal bandwidths of 10KHz, 5KHz, 1.25KHz and 625Hz, respectively. To ensure better stability, the gain of the first integrator stage was halved. The designed delta-sigma modulator uses the same OTAs of the delta-sigma modulator shown in [Bennati,09].

Sampling Frequency	OSR
10KHz	64
5KHz	128
1.25KHz	512
625Hz	1024

Table 6 OSR values among different acquisition bandwidths.

4.3.3 Saturation Detection

For input currents much greater than the full-scale inpu range, the system of Fig. 48 shows a malfunction, producing a zero output. For instance, a 2nA input current with the ±200pA range selected, causes the saturation of the CSA before the end of the noise-sampling phase. Therefore, the CDS subtracts two equal values and gives to the delta-sigma modulator a signal equal to zero. To cope with that issue, we added a window comparator (Fig. 61). It

compares the CSA output with two reference voltages: if the signal is higher than references, the output of the delta-sigma modulator is forced to a sequence of logic ones, if the signal is lower than references, the output of the delta-sigma modulator is forced to a sequence of logic zeros.

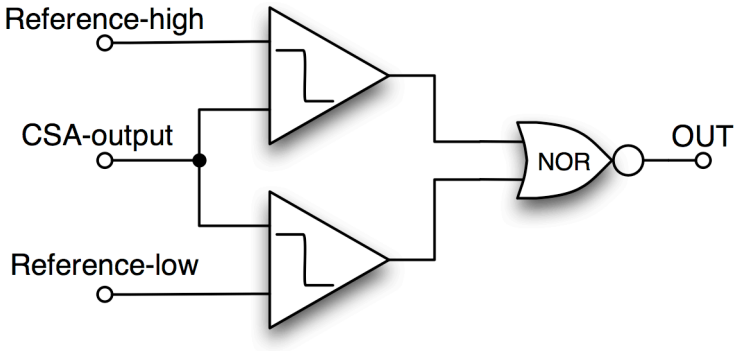

Fig. 61 Scheme of the circuit detecting the saturation of the CSA. In case the CSA saturates, the circuit forces the output of the delta-sigma modulator to either a sequence of zeros or a sequence of ones.

4.3.4 Digital Filtering Using FPGA

To recover the high precision data from the 1-bit high-frequency stream, both low-pass and decimator filters are needed. The required LPF parameters are chosen to be as flat as possible over the signal bandwidth and very selective. It is also desirable to have a flat group delay response in the signal band. A linear-phase finite-impulse response (FIR) filter can easily satisfy all the above conditions.

Since the output signal of the delta-sigma modulator is a single bit data stream, it may be practical to use a single-stage high-order linear-phase FIR filter, eliminating the need of multiplications between the samples of the signal and the FIR coefficients (the taps). However, it is usually more efficient and economical to implement the filtering and the decimation in a multi-stage approach. The first stage is a sinc filter. The sinc is a FIR filter with *N-1* delays and *N* equal valued tap weights, computing a running average of the input bit stream *v(n)* every *N* samples. Thus, the output *w(n)* of the sinc filter is:

$$w(n) = \frac{1}{N}\sum_{i=0}^{N-1} v(n-i). \tag{4.16}$$

When used to suppress the shaped quantization noise, the sinc filter has a residual output noise of approximately OSR times higher than an ideal LPF [Schreier,05].

The second stage is FIR filter employing a Kaiser window function. It shows a good trade-off between transition bandwidth and stop-band attenuation, and reduces the non-idealities in the passband, such as the ripples [Oppenheim,99]. The Kaiser window function is defined as

$$w(n) = \frac{I_0\left[\beta\sqrt{1-\left(1-2n/N\right)^2}\right]}{I_0(\beta)}, \qquad 0 \le n \le N-1, \tag{4.17}$$

where I(β) is the modified zero-order Bessel function of the first kind, N is the length (order) of the filter and β is the shape parameter which determines the rate between the main-lobe width for the transition bandwidth and the side-lobe peak level in the stop-band [Oppenheim,99].

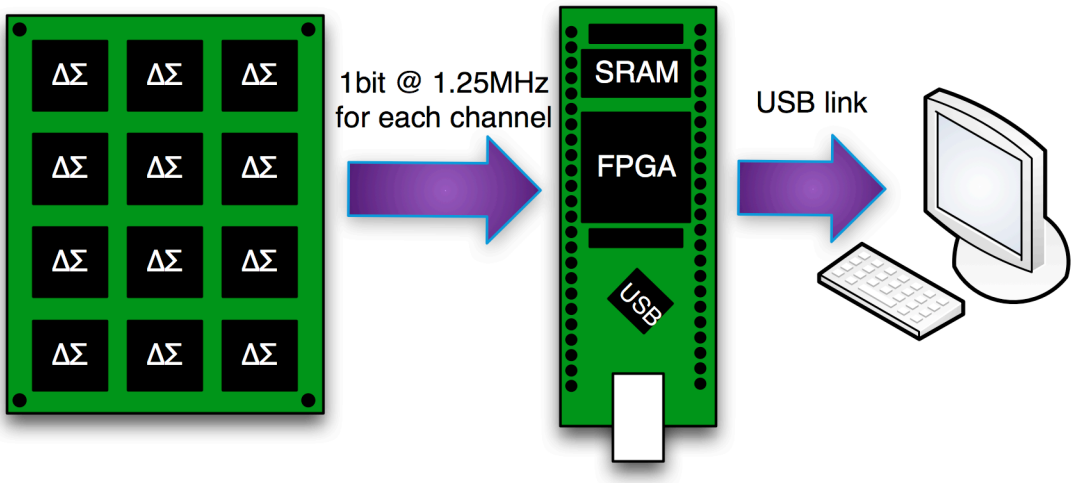

Fig. 62 The proposed current-sensing interface IC can be arranged in a parallel fashion to allow concurrent acquisition of single ion channels. The 1-bit delta-sigma output simplifies the routing architecture even for high array dimensions. One FPGA module can easily handle the data coming from each channel. It implements a two-stage FIR filter removing the quantization noise and decimating the signal. All the data are sent to a PC via a USB link.

The proposed IC can be arranged in an array fashion, as depicted in Fig. 62, allowing parallel acquisition of single ion channels. The delta-sigma approach is very suitable for array architecture, because it simplifies the routing design by means of the minimized number of output lines [Thei,11]. To concurrently filter and decimate all the data channels, a field-programmable-gate-array (FPGA) is used. The FPGA board also includes a USB chip interface to easily

communicate with a PC. The implementation of the two-stage LPF in the FPGA board requires to transform the computational blocks of the FIR filters in an approach suitable for the FPGA architecture, based on distributed memory and a defined number of multiplier [Thei,11].

The architecture of this system is designed to be expanded to a very large amount of simultaneously acquired data channels, depending only on the performance of the FPGA and the maximum capacity of the data transfer link. As proof of concept, supposing an acquiring channel at 4 kHz with 16 bit of resolution for each data sample, through a USB 2.0 full speed (12 Mb/sec) it is possible to send up to 75 channels simultaneously. Moreover, through a USB 2.0 high speed (480 Mb/sec) data link, the number of simultaneously channels elaborated grows up to 3.000 channels. Using Ethernet links, able of GBps as data rate, the number of simultaneously channels grows up of orders of magnitude. Commercial FPGA (i.e. Xilinx Virtex VI® XC6VSX475T) offers up to 2.016 DSP slices operating at 600 MHz, where each slice can elaborate one channel.

4.4 Offset Correction Loop

4.4.1 Architecture

The solid-liquid interface between the electrolyte solution and the metal electrodes has to be carefully analyzed since it affects the current measure and thus the total accuracy. One junction potential occurs whenever dissimilar conductors are placed in contact, resulting in an intrinsic offset voltage [Bard,01]. In the experiment setup of Fig. 63, the junction potential due to the electrode-electrolyte interface is usually in the order of tens to hundred of mV. Such a high offset voltage creates an offset current that limits the acquisition range or even cause the saturation of the CSA. Although the two electrodes should compensate each other with equal offset voltages, the intrinsic variability of the single-junction Ag/AgCl electrodes leads to a final non-zero offset voltage.

The offset variability of the electrode-electrolyte interface is a well known electrochemical problem, especially in voltammetry, patch clamp and ion-channel-based systems [Sakmann,95]. Different approaches have been

proposed in the literature to solve this problem, such as three electrode systems (Ag/AgCl plus Au or Pt electrode [Triroj,06]), liquid junction, and agar-salt bridge [Shao,07]. However, these approaches are commonly employed in single acquisition systems or multiplexed systems, where a single readout instrument is switched between the microfluidic channels.

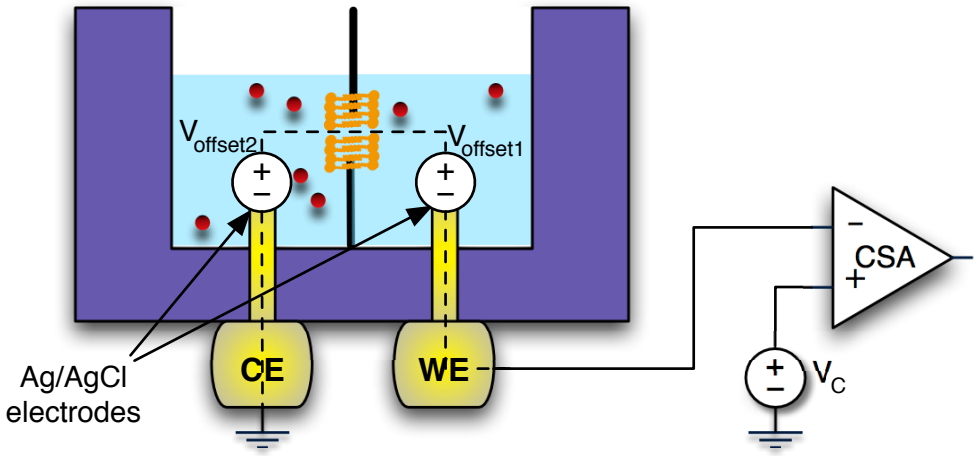

Fig. 63 Standard experiment setup for ion channel acquisition, where the voltage offsets due to junction potential in the electrode-electrolyte interfaces is emphasized. Note that the two offset voltages are not equal due to mismatches between the electrodes, resulting in a total offset voltage in the order of tens to hundreds of mV.

To cope with junction potential offset in an array platform, we developed a digital offset correction loop integrated in each readout interface. It is composed of a comparator, an up/down counter and a digital-to-analog converter (Fig. 64). The d-OCL compares the CDS output with the ground voltage, which is the value corresponding to a zero input current. If the CDS output is higher, then the d-OCL increases its output until the input current is nulled, and vice versa [Thei,10b]. The digital counter is refreshed at low frequency, 150Hz, to meet all the bandwidth limitations throughout the electrochemical system. A 10-bit comparator with a full-range of 200mV has been chosen so as to compensate standard offset values with a tolerable minimum step of 200μV.

The offset correction loop is activated only at the system startup, reducing the effect of the junction potentials; while the feedback loop is cut and the final output value is stored into the DAC, when the system acquires the input current. Finally, an analog adder sums the result of the d-OCL with the stimulus signal V_C (obviously the V_C signal is kept constant during the offset correction phase).

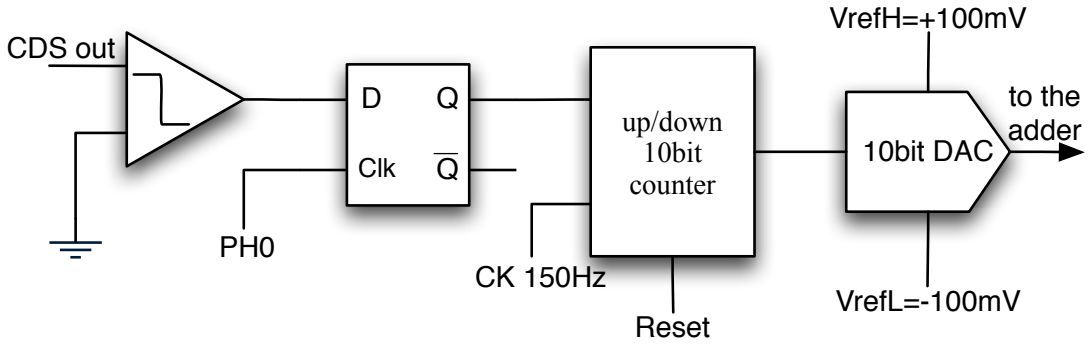

Fig. 64 Block scheme of the implemented digital offset-correction-loop. It is composed of a comparator, a flip-flop, an up/down counter and a 10 bit DAC working between ±100mV. The system is activated at the system startup, reducing the effect of the junction potential.

4.4.2 Analog Adder

The analog adder is a very critical circuit, since its own noise power directly adds with the noise power $\overline{e_{n-op}^2}$ generated by the CSA. To mitigate this effect we implemented an analog adder with the following properties:

1- It uses the same low-noise OTA employed in the CSA

2- It is a switched capacitor circuit, eliminating the need for noisy resistors

3- It employs big filtering capacitors (external to the IC) to lower the bandwidth as much as possible.

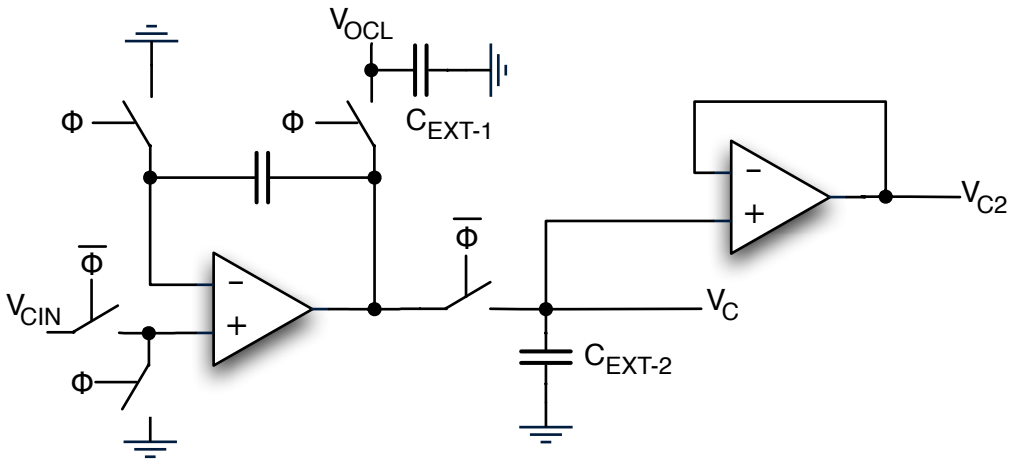

Fig. 65 Schematic of the proposed switched-capacitor analog adder. The OTA depicted on the left stores the d-OCL output in the feedback capacitor, when ϕ is high. It sums this stored value with the input V_{CIN}, when ϕ is low. The OTA depicted to the left works as a buffer creating a V_{C2} signal, which will be fed to the switches in the main system path.

The scheme of the proposed analog adder is depicted in Fig. 65. It stores the output voltage of the d-OCL in the feedback capacitor and works as a

voltage buffer for the V_{CIN} signal. Thanks to the short circuit principle, the output of the adder is

$$V_C = V_{CIN} + V_{OCL}; \tag{4.18}$$

where V_{CIN} is the stimulus signal coming from either an external generator or the integrated DAC, and V_{OCL} is the output voltage of the offset correction loop. The circuit suffers from some non-idealities. The actual output signal is affected by the offset of the OTA ($V_{OTA\text{-}off}$), thus

$$V_C = V_{CIN} + V_{OCL} + V_{OTA-off}; \tag{4.19}$$

however, this offset will be automatically compensated by the d-OCL. The charge stored in the feedback capacitor tends to reduce itself due to unavoidable leakages. To cope with that, a periodical refresh of the feedback capacitor is implemented. Therefore, the analog adder works in two different phases: the refresh phase and the summing phase. This switching behavior should be invisible to the other part of the system; thus, a simple S&H circuit is implemented using a switch and a capacitor. While the adder refresh the feedback capacitor, this switch is open and the capacitor $C_{EXT\text{-}2}$ stores the output voltage. Nevertheless, the refresh phase should be as short as possible; otherwise the output signal will not exactly follow the input stimulus signal.

Note that capacitors $C_{EXT\text{-}1}$ and $C_{EXT\text{-}2}$ are external big capacitors, in the order of some nF. They are mainly used to lower the bandwidth of the adder and thus reduce the noise. However, both capacitors cannot be too large or they will affect the correct functionalities of the system. If $C_{EXT\text{-}1}$ is larger than 100nF, it introduces a pole at very low frequency in the digital offset compensation loop, preventing the offset correction. If $C_{EXT\text{-}2}$ is larger than 10nF, it narrows the bandwidth of the adder too much, which is no more able to track stimulus signals with 10KHz bandwidth. An additional buffer is placed at the output of the analog adder to create a replica of the V_C that should be connected to the switches throughout the system (please refer to section 4.2.1). Although we have carefully addressed the noise issue during the adder design, we even expect an increase in the final input-referred noise PSD of the entire system.

4.5 *Preliminary Results*

The final scheme of the proposed system is depicted in Fig. 66. It is a first prototype designed for a whole lot of tests and experimentations. Using a 24-bit integrated SPI, it is possible to program the IC so as we can test the functionality of each single block. From the application point of view, the IC is very flexible:

1- It can be used for both signal generation and acquisition

2- Both delta-sigma and adaptive phases techniques, allow the user to easily and effectively trade bandwidth for low noise

3- The d-OCL can be either activated or deactivated depending on the experiment requirements

4- The possibility to use an external resistor in the feedback loop allows the IC to be used even in applications with higher currents (like μA).

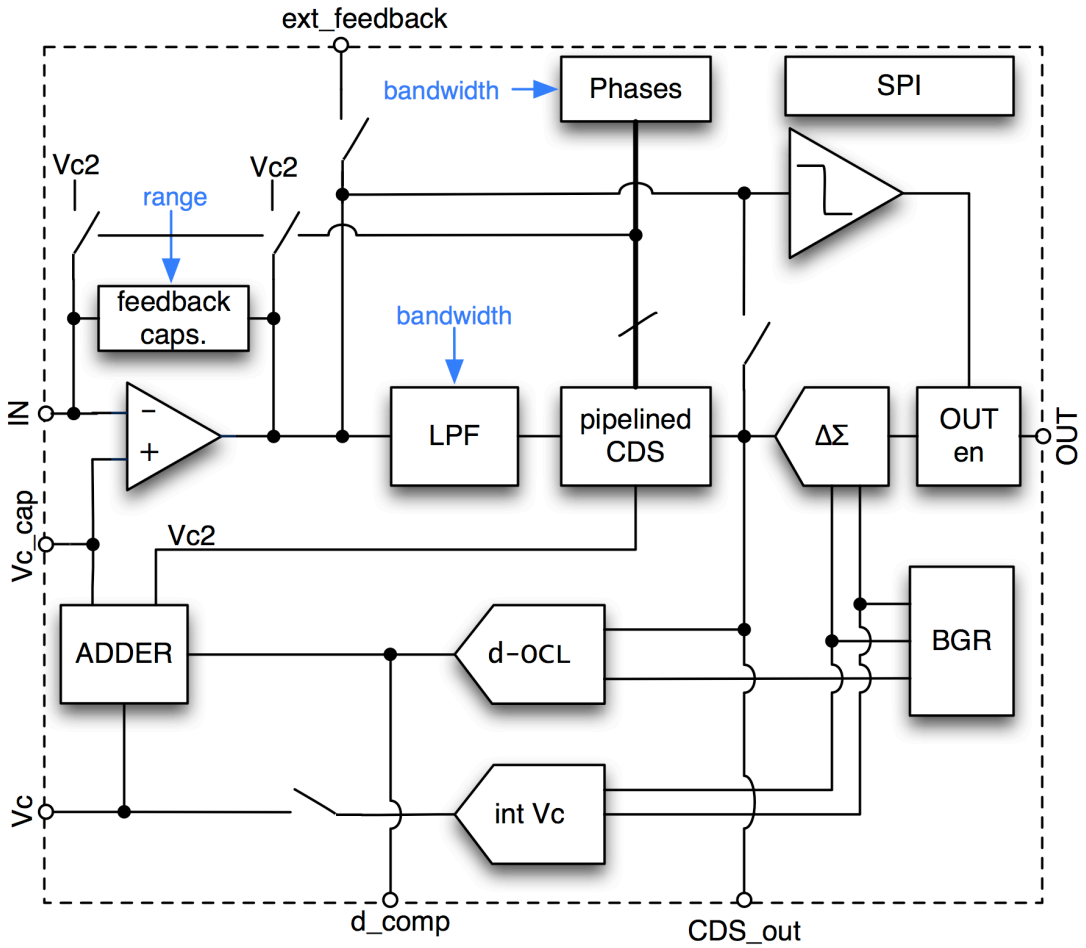

Fig. 66 Final scheme of the proposed low-noise current-sensing interface.

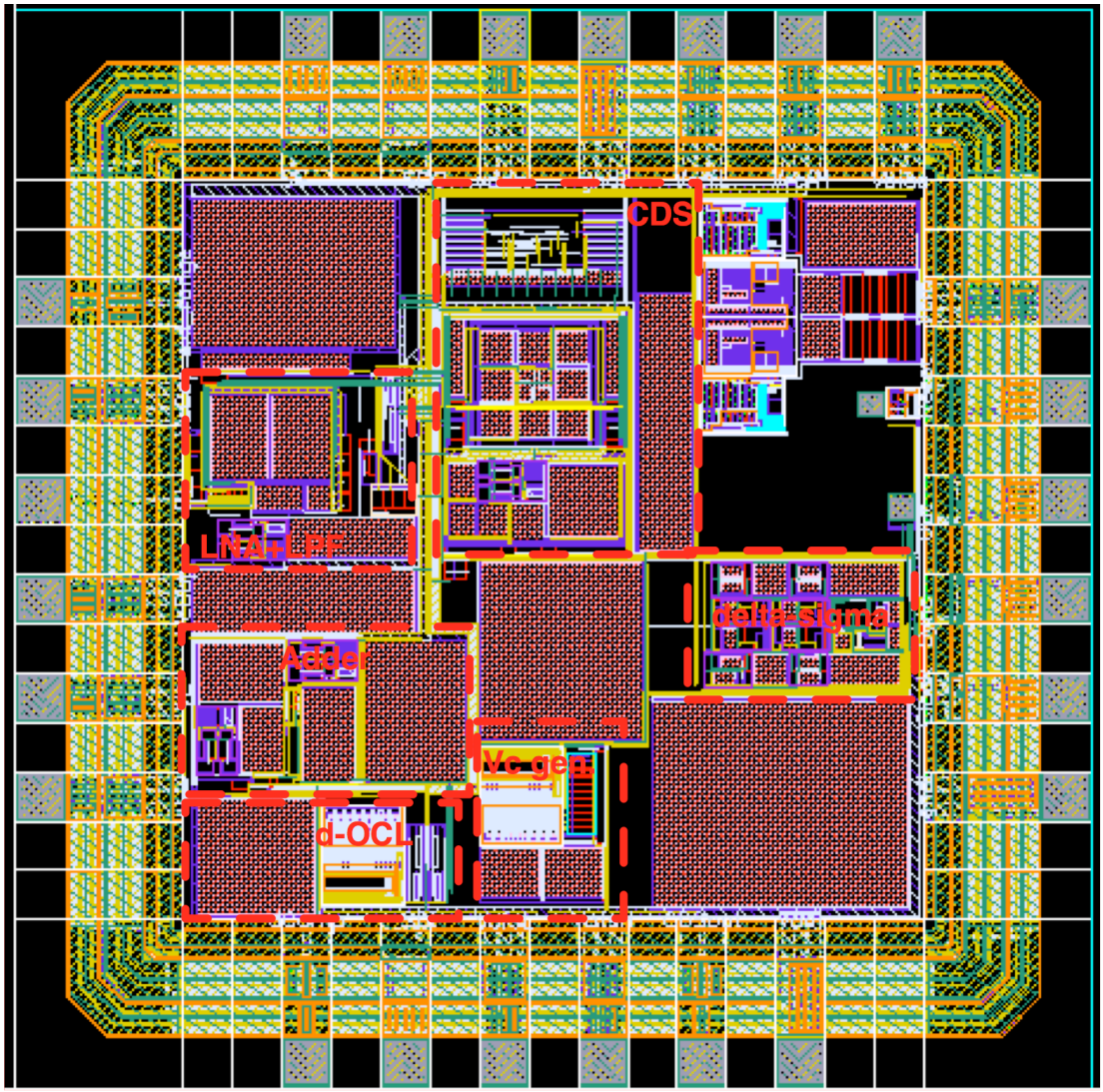

Fig. 67 Layout of the proposed DT current-sensing interface shown in Fig. 66.

Fig. 67 shows the final layout of the 5mm^2 IC, highlighting the placement of the main stages of the system. The CSA has been located as close as possible to the input pin to minimize the stray capacitance on the input node. To mitigate the effects of digital coupling mechanisms, the majority of the silicon area is occupied by filtering capacitors placed on supply and reference signals. Moreover, the IC keeps analog and digital supplies separated each other. They will be connected together at PCB level so as to take benefit of stray inductance from bond-wires. Also the pin layout has been carefully studied; pins connected to V_C surround the input pin, and digital pins are placed at the opposite side of analog ones (See appendix B).

Since the IC is still in fabrication, we only have simulation results. The first test is the acquisition of a steady DC current. We modeled the ion channel with 6GΩ resistor and applied a 200mV stimulus signal by means of the

internal V_C generator. The system works at the lower input range (i.e. ±200pA) and at 5KHz bandwidth. The simulation was done on layout-extracted netlist so as to estimate the effects of parasitic elements. This is just a behavioral simulation, thus it only takes the quantization noise into account. Fig. 68 shows the final result of a 5ms acquisition[10]. The system has a starting transient time of approximately 0.5ms before settling to a stable value. Apart from an expected gain error, the output shows a 5KHz parasitic disturb with amplitude of approximately 20fA, which is related to matching issues between the two CDS stages. The resulting stray sine wave has amplitude proportional to the input signal, leading to a nonlinear resolution. For the simulated 33pA input current, the parasitic wave overwhelms the quantization noise, leading to 14.1bit as ENOB of the system. However, the digital FIR filter can easily eliminate the stray wave, since it is exactly at the edge of the acquisition bandwidth.

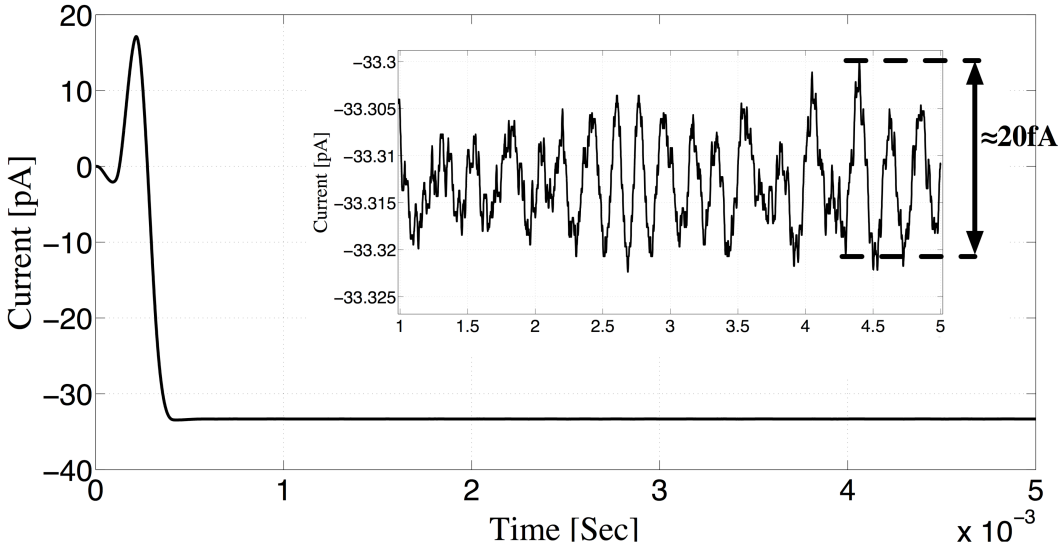

Fig. 68 Simulation of a current acquisition with ±200pA input range and 5KHz bandwidth selected. The ion channel was modeled with 6GΩ resistor stimulated by 200mV internally generated. The system has approximately 0.5ms of starting transient time before settling to a stable value. Apart from an expected gain error, the output shows a 5KHz parasitic disturb with amplitude of approximately 20fA, which is related to matching issues between the two CDS stages. The resulting wave has amplitude proportional to the input signal, leading to a nonlinear resolution.

Fig. 69 shows the result of a 10KHz acquisition with simulated thermal noise. In this simulation the parasitic wave is buried under the thermal noise but acts to increase the peak-to-peak error to 1.2pA, resulting in a total rms

[10] The delta-sigma output stream was filtered and decimated by a FIR filter implemented in Matlab.

noise of approximately 220fArms. This rms noise value takes into account all the noise and error sources (such as thermal noise, quantization noise, matching errors...); therefore, it is slightly bigger than the estimation reported in Table 7.

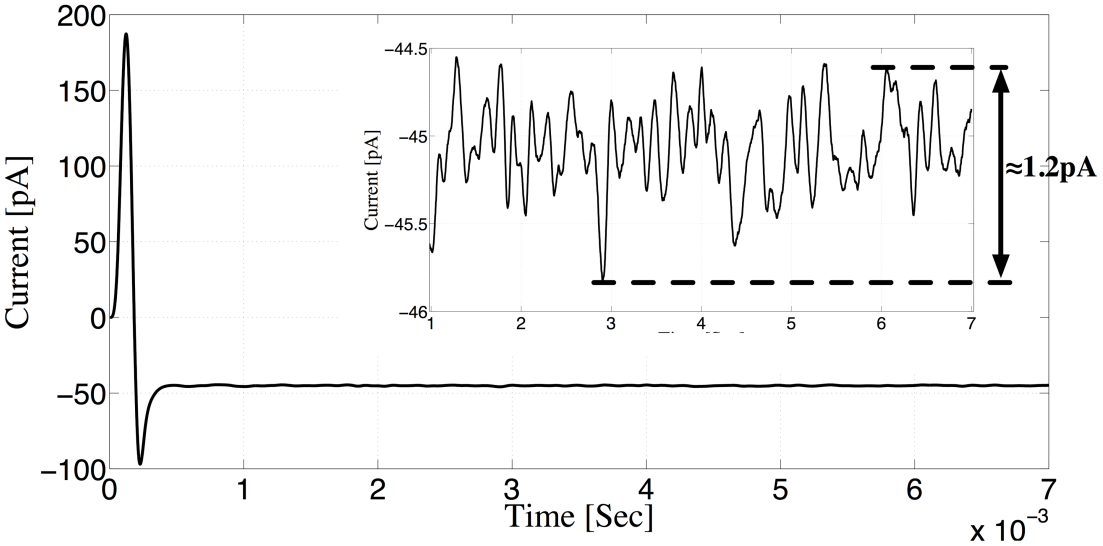

Fig. 69 Simulation of a current acquisition with ±200pA input range and 10KHz bandwidth selected. The simulation takes into accounts all kinds of noise sources and errors, such as thermal noise, kTC noise, quantization noise, and charge injection. The ion channel was modeled with 1GΩ resistor stimulated by 50mV internally generated. In this simulation the parasitic wave is buried under the thermal noise but acts to increase the peak-to-peak error to 1.2pA, leading to a total rms noise of approximately 220fArms.

Fig. 70 shows the input-referred noise PSD of the system for different acquisition bandwidths, proving the ability of the proposed IC to reach an input-referred noise current lower than 1fA/√Hz. If the real prototype will confirm the simulations, the proposed IC will become the state-of-the-art CMOS current-sensing interface. The system shows an input-referred rms noise current at 1KHz that is comparable with leading instrumentation [Axon,08]. The simulation was done as a transient time noise simulation to cope with the DT behavior, and consider an input stray capacitance of 3pF. Moreover, the digital feedback and the adder were neglected to simplify and boost up the simulation time. Table 7 summarizes noise and accuracy parameters among different bandwidths.

Equation (3.20) gives a rather good estimation of the input-referred noise PSD for all the bandwidths, proving the value of the theory exposed in chapter 3. For instance, in the 5KHz bandwidth, the input-referred noise current is given by

$$\overline{i_N} \approx \sqrt{\frac{16}{3}\frac{kT}{C_O}\cdot\frac{C_T^2}{Rg_mT_S}} = 1.2\,fA/\sqrt{Hz}\,, \tag{4.20}$$

where the following parameters were used: C_F=42fF, C_{IN}=3.6pF, T_S=102.4μs, g_m=7mA/V, R=17KΩ, C_O=16pF.

Bandwidth	Noise Current	rms Noise Current	ENOB
10KHz	1.88 fA/√Hz	188 fArms	11.05
5KHz	1.17 fA/√Hz	83 fArms	12.24
1.25KHz	0.7 fA/√Hz	25 fArms	14.2
625Hz	0.55 fA/√Hz	14 fArms	>15

Table 7 Input-referred noise current for different working bandwidth. The system shows an input-referred rms noise current at 1KHz comparable with state-of-the-art laboratory instruments [Axon,08].

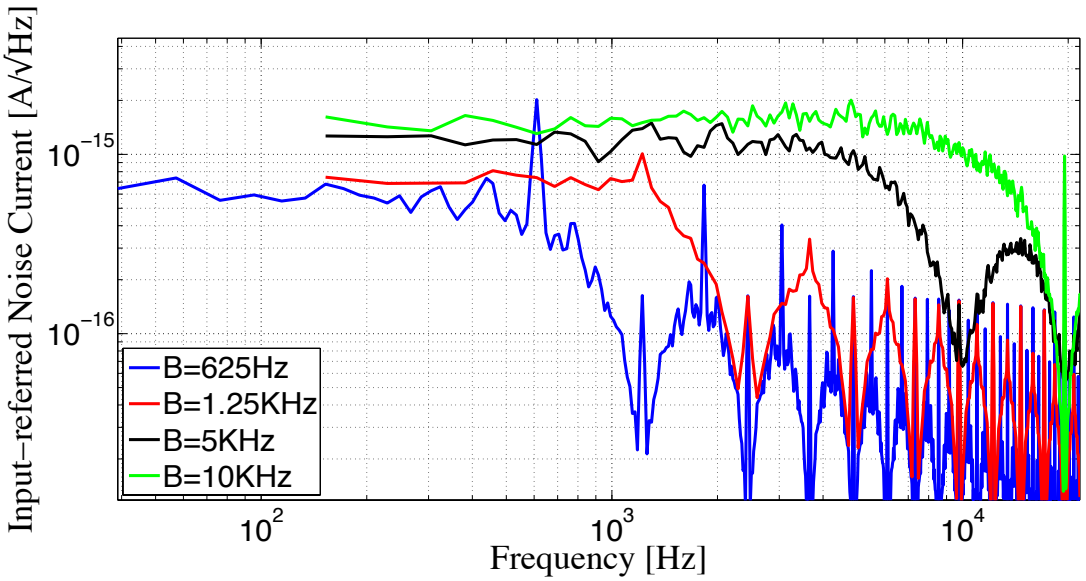

Fig. 70 Simulation of input-referred noise PSD for different acquisition bandwidths. The simulation was done as a transient time noise simulation to cope with the DT behavior, considering an input stray capacitance of 3pF. The system shows an input-referred rms noise current at 1KHz that is comparable with leading instrumentation.

To prove the effectiveness of the kTC noise reduction technique, Fig. 71 compares the input-referred noise PSD of the new IC with the one presented in [Bennati,09]. Although the bandwidth of the new current-sensing interface is slightly greater, the input-referred noise current is five times lower.

We expect a slightly increase of the input-referred noise PSD in measurement tests due to the digital feedback and the analog adder. To lower this effect we filters the output of the adder by means of an external capacitor.

Fig. 72 shows the result of a noise simulation taking into account the whole system and an extra 6nF capacitor placed at adder output.

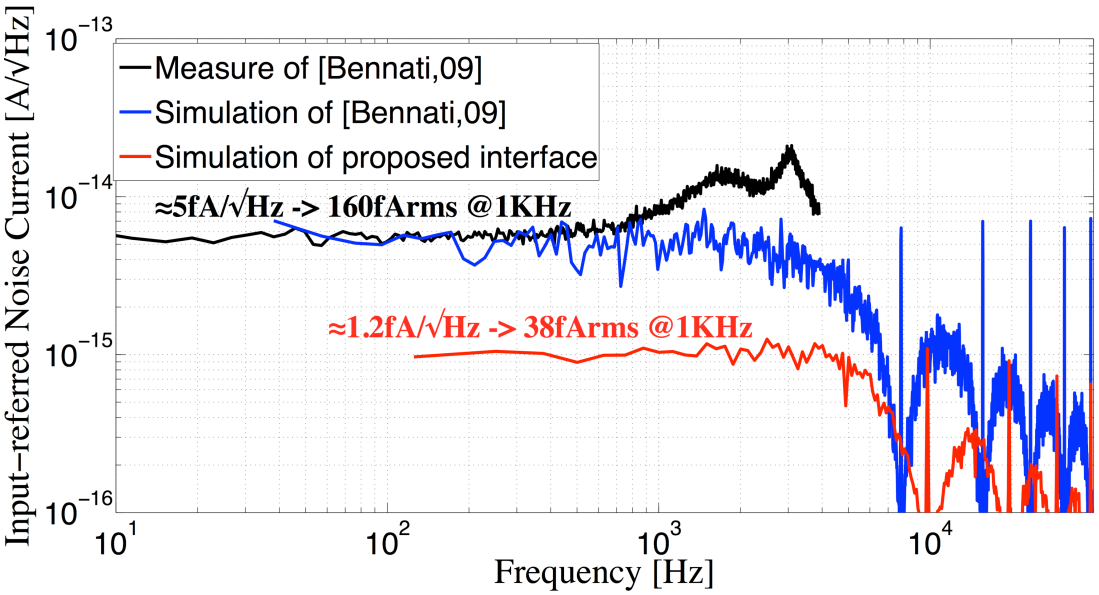

Fig. 71 The current-sensing interface presented in [Bennati,09] shows an input-referred noise floor of approximately 5fA/√Hz up to 4KHz, resulting from both simulations (blue line) and measures (black line); while the new current-sensing interface shows an input-referred noise floor of only 1.2fA/√Hz. This graph proves the ability of the kTC noise reduction technique to lower the noise in DT current-sensing interfaces.

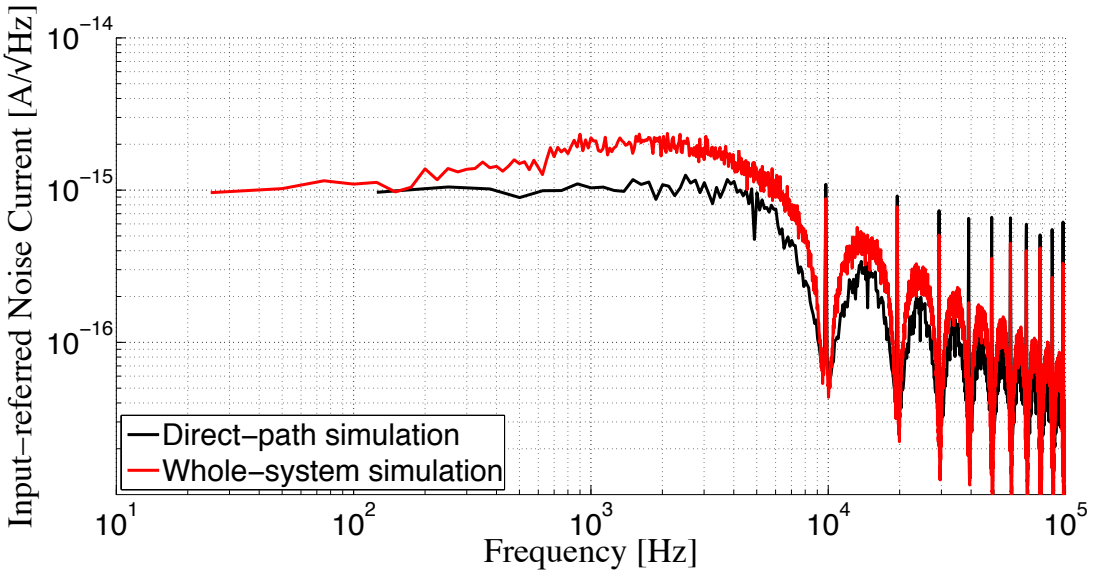

Fig. 72 Simulation showing the effect of the analog adder and digital feedback on the input-referred noise current. The simulation has done placing a 6nF filtering capacitor at adder output; it is the maximum capacitance allowed avoiding bandwidth reduction of the V_C signal.

Chapter 5

AC Impedance Sensing: A High Dynamic Range IC Design

This chapter presents a fully integrated 15-bit EIS system designed to be used with conductivity-temperature-depth (CTD) sensors. It will be employed in environmental applications for ocean monitoring and studying. Moreover, the system could also be used in bio-nanosensor applications, mainly for nanowire-based sensors that require AC measurement. The proposed EIS system integrates both driving signal generation and signal acquisition. It is based on a band-pass delta-sigma approach, eliminating the need for an analog down-conversion stage. The system is designed for 15-bit resolution and low power consumption, ensuring a lifetime of approximately 1 year using button-size batteries.

Oceans cover about three quarters of the planet and their effect on humans, plants and animals is often underestimated. The importance of understanding the oceans has increased dramatically because they play a crucial role in the rapidly changing global climate. The measurement of essential physical properties of seawater such as: salinity, temperature and depth pressure is crucial for marine environmental study. Conductivity, temperature and depth sensors are the primary investigation tools for those parameters, providing information about oceanic circulation, mixing and climate processes. Therefore, CTD sensors act as important ecological tools, helping scientists to study the marine changes as well as aquatic organisms. Small, low-powered CTD sensors are becoming used strategically in autonomous instruments like

moored profilers, gliders, profiling floats and autonomous underwater vehicles (AUVs) [Whoi,11]. Conductivity sensors are required in many other application fields, including biomedical devices, environment monitoring, agriculture, and food production process chemistry. Several high accuracy CTD sensors are commercially available, but they are all very bulky [Seabird,11], [StarOddi,11], [Valeport,11]. Smaller systems have been developed to measure temperature and salinity but they are often inaccurate or power-hungry [Li,05], [Ramos,08], [Broadbent,07], [Hyldgard,08]. A small, high-accuracy system for CTD sensors capable of lasting one year or more could create new opportunities for the study of oceans and climate changes, by means of massive CTD sensors networks. This chapter addresses the design of an IC interfacing with the high-accuracy CTD sensors provided by University of Southampton. The IC implements an electrochemical impedance spectroscopic (EIS) system suitable for CTD sensor applications as well as for bio-nanosensor applications.

The first section introduces the reader to CTD sensor systems, explaining the best sensing techniques, discussing accuracy issues, analyzing the currently state of the art, and presenting our EIS system. Sections two, three and four analyze in detail the architecture of each core component of the EIS system. Finally, section five shows the IC implementation and preliminary results.

5.1 CTD Sensor System

5.1.1 High Accuracy CTD Sensing

The resolution and accuracy of conductance measurements depend on the physical and electrical non-idealities such as contacts and interfaces. Four-terminal (or Kelvin) sensing is widely used to reduce contact and interface interferences. The key advantage of this approach is the separation of current and voltage electrodes, eliminating the contribution of wiring impedance and contact resistances R_S as shown in Fig. 73.

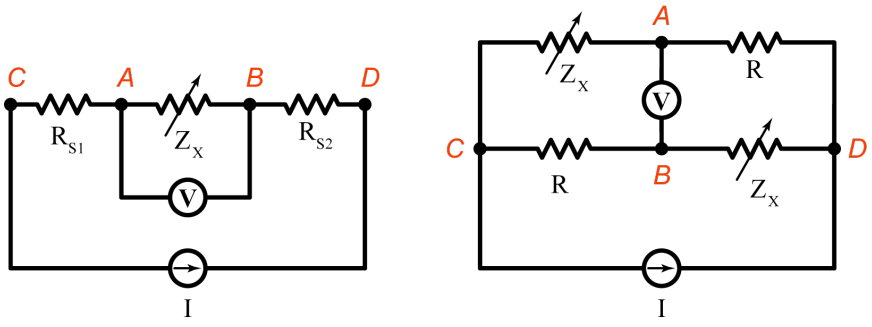

Fig. 73. Impedance sensing by four-terminals sensing technique: set-up implemented for water conductivity sensor (left); and current-based Wheatstone bridge for platinum resistance thermometers (right).

The current is supplied via two connections, C and D, so that a voltage drop across the impedance can be measured in A and B connections. Since the differential amplifier used for the voltmeter has infinite input impedance, the current flowing into the sensor is known; thus the unknown impedance can be determined disregarding wiring resistances by Ohm's law. The above approach, based on current-forcing and voltage-sensing, is particularly suited for CTD sensors and can also be applied to Wheatstone bridge structures using the same interface (Fig. 73).

In the specific case of sensing seawater conductance, metal-solution interface modeling should be taken into account as illustrated in Fig. 74, [Hyldgard,08], [Bard,01].

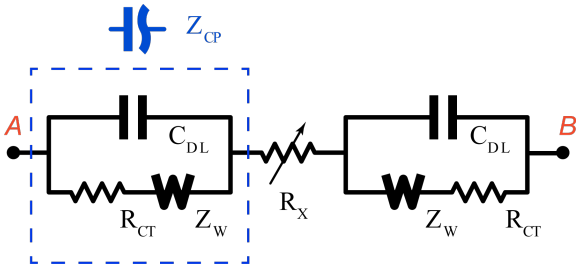

Fig. 74. Electrochemical interface model for measuring conductivity of aqueous solutions.

Assuming a pure resistor modeling the aqueous solution and neglecting the polarization, the charge transfer to and from the interface is the result of either reduction-oxidation (red-ox) processes at the interface, or charging of the electrode-solution double layer capacitance as in a semi-conductor junction. The two processes can be modeled as a resistive (R_{CT} and Z_W) and a capacitive (C_{DL}) component in parallel. The charge transfer resistance R_{CT} represents the mass transfer due to the red-ox process, i.e. the transfer of metal ions in or out the metal-solution interface. That resistance is highly non-

linear and depends on both the concentration of ions in the solution and the applied potential. To reduce red-ox processes, the potential should stay as low as possible (a few tens of mV) so that corrosion of the electrodes is minimized. This is of course of primary importance in micro-systems where the area of the electrodes is limited. For small-applied voltages the charge transfer resistance could easily achieve values above 1MΩ and the corrosive processes could be neglected. Z_W is called *Warburg impedance* and is due to the ion diffusion process in proximity to the interface. The double layer capacitance C_{DL} depends on the material of the electrodes and on the ion concentration, with typical values in the range of 10–40 $\mu F/cm^2$. Usually the combined effect of R_{CT}, Z_W, and C_{DL} is modeled by constant phase angle impedance Z_{CP} of the form

$$Z_{CP} = \frac{A}{(j\omega)^{\beta}}, \tag{5.1}$$

where A and β are constant and β is usually slightly smaller than 1 [Morgan,01].

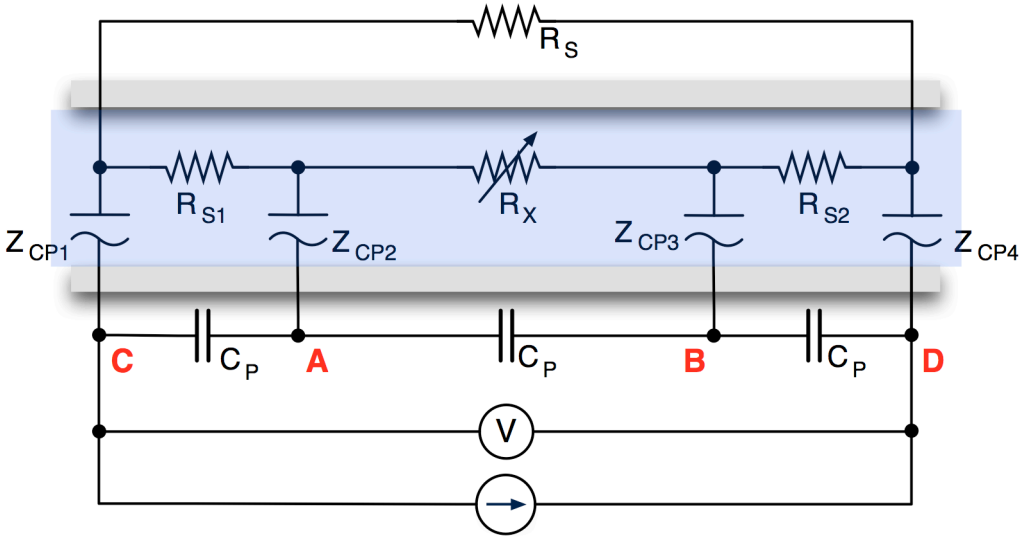

Fig. 75. Cross section of four-electrode conductivity cell showing parasitic capacitances, series stray resistances, and metal-solution interfaces.

Although a compact four-point conductivity sensor is usually implemented by patterning noble metals on an insulating material [Huang,11], parasitic resistances (R_S) and parasitic capacitances (C_P) are unavoidable, as shown in Fig. 75. However, adding more electrodes placed in feedback loops will keep electrodes C and D at the same potential and consequently will reduce the

influence of R_S [Gong,08]. Alternatively, parasitic capacitances could be neglected by using the appropriate frequency range. More specifically, the measured impedance is given by the relationship

$$Z_X \approx \frac{1}{j\omega C_P + \dfrac{1}{R_X + \dfrac{2A}{(j\omega)^\beta}}} \approx \frac{R_X}{1 + j\omega R_X C_P}. \tag{5.2}$$

The last approximation is given for $\omega >> 2A/R_X$, where interface impedance is much lower than the sensed resistance R_X. If we further assume $\omega << 1/R_X C_P$, equation (5.2) becomes

$$Z_X \approx \frac{R_X}{1 + j\omega R_X C_P} \approx R_X - j\omega R_X^2 C_P. \tag{5.3}$$

In other words, impedance sensing could be performed in a frequency range which is lower-bounded by interface effects and upper-bounded by parasitic capacitance impedance. For electrodes of approximately 1mm^2, the optimal frequency is in the 1kHz-1MHz range where R_X varies between 1.5kΩ and 20kΩ for seawater conductivity varying between 5mS/cm and 70mS/cm. The second term of equation (5.3) indicates the estimation error, which is clearly identifiable by phase measurement. For that reason, phase detection is an important part of impedance sensing in CTD sensors.

5.1.2 State of the Art

To better explain the aims and future opportunities of proposed CTD system, it is useful to review the latest published literature and the commercially available CTD systems.

W. Gong proposes a conductivity-temperature sensor based on a two-electrode conductivity cell and a thermistor, both excited with a 334KHz sine wave. The acquisition system and stimulus generation are created using discrete components mounted on a PCB. The system has been tested in 0.2-1 mol/L potassium chloride (KCl) bath cells, showing a conductivity measurement error around 2.7% and a temperature accuracy of 0.003m°C

over 0-30ºC temperature range. It demonstrated the ability to last 48 hours using standard batteries [Gong,08].

X. Huang proposes a conductivity-temperature sensor based on a seven-electrode conductivity cell and a platinum resistance temperature detector (RTD). It is able to measure conductivity in the range of 25-55mS/cm with accuracy of 0.03mS/cm and temperature in the range 4-34ºC with accuracy of 0.01ºC [Huang,11]. Once again, the electronic system is implemented with discrete components. The overall system occupies approximately 10x15cm and lasts 1 month using PP3 batteries.

A Hyldgard proposes a CTD sensor system for fish-tag applications. It embeds a platinum conductivity sensor, a titanium silicide RTD, and a piezo-resistive pressure sensor in a single 4x4mm chip. The system allows conductivity, temperature and pressure measurement with accuracies of 0.6mS/cm, 0.065ºC, and 0.05 bar, respectively. Moreover, the electronic system has been developed using discrete components and the overall system, occupying 8x8x50mm, has been covered with epoxy glue [Hyldgard,11].

Sea-birds Electronics is one of the leading companies in marine instrument development [Seabird,11]. That enterprise has worked in the maritime research field since 1974, developing and bringing to market high quality instruments. The Sea-bird SBE 911plus CTD system is the primary instrument chosen by research institutes all over the world. It shows the best CTD performance in terms of accuracy: 0.003mS/cm over 0-70mS/cm range for the conductivity sensor, 1mK over -5-35ºC range for the temperature sensor, and 0.015% for the pressure sensor. However, it is very bulky and power hungry.

Star-Oddi, an Icelandic company, is the industry leader in fish-tagging applications analyzing fish migration, distribution, and feeding behavior [StarOddi,11]. The Star-Oddi DST CTD is the smallest CTD logger sensor available on the market, just 15x46mm, capable of lasting 4 years in a working environment, with a sampling interval of 10 minutes. However, it is less accurate than the Sea-bird SBE 911plus.

Table 8 reviews the present day state of the art of CTD sensors, comparing the systems described above. The Sea-bird SBE 911plus is the most accurate system but it is very bulky and power hungry, and therefore unsuitable for fish-tag application. On the other hand, the Star-Oddi DST CTD and

Hyldgard's system are sufficiently small, but they show accuracies 100 times worse. Against that background it is clear that the development of small, low-power CTD sensor systems with accuracies similar to those shown by the Sea-bird product will be a tremendous benefit to ocean research.

CTD Sensor	Conductivity accuracy	Temperature accuracy	Pressure accuracy	Power or battery life
[Gong,08]	2.7% @ 0.2-1mol/L in KCl solution	0.003ºC	N.A.	48 hours
[Huang,11]	0.03mS/cm (25-55mS/cm)	0.01ºC (4-34ºC)	N.A.	1 month @ 10sec sampling
[Hyldgard,08]	0.6mS/cm	0.065ºC	0.05bar	N.A.
[Seabird,11]	0.003mS/cm (0-70mS/cm)	0.001ºC (-5-35ºC)	0.015% @ FS 10500m	1A @ 14.3V
[StarOddi,11]	1.5mS/cm (10-50mS/cm)	0.1ºC (-1-50ºC)	0.4% @ FS 200m	4 years @ 10min sampling

Table 8 Review CTD systems state-of-the-art.

A small, low-power CTD sensor able to measure conductivity in the range 10-50mS/cm with accuracy of 0.005mS/cm, and temperature in the range 0-40ºC with accuracy of 1mºK, is now under development by the H. Morgan research group at University of Southampton. However, the sensor also needs a high-accuracy electronic system for stimulus generation and signal acquisition. In order to get both the high accuracy reached by the sensor and the low-power requirements for fish-tag applications, a fully integrated high-resolution electronic system is needed.

5.1.3 Integrated EIS System for CTD Sensor

As explained in section 5.1.1, the Kelvin sensing technique based on current-forcing and voltage-sensing is the best measurement solution for CTD

sensors. That technique requires a current generator and a voltage readout circuit. To cope with reduced dimensions and greater autonomy, both above blocks should be integrated into IC. Resolution requirements for CTD application are quite challenging, in the order of one thousand of degrees in the range 0-30ºC and 0.003 mS/cm in the range 0-70 mS/cm. Therefore, the interface should be characterized by at least 15bit of equivalent number of bits (ENOB). To reach such requirements it is also important to integrate the ADC, so as to reduce any loss of resolution and take the entire system as compact as possible [Bracke,05]. Likewise, all the building blocks of the system must follow a noise-aware design and the global power consumption should be kept as low as possible, so as to allow lifetime of 1 year or more in real working environment.

As stated before, parasites and non-idealities coming from sensor implementation limit the impedance sensing to a defined frequency range. For the delivered CTD sensors the optimal frequency is approximately 1KHz and the signal bandwidth is just 10Hz. Therefore, the current generator should be able to produce a low-noise high-accuracy current sine wave centered at 1KHz. Likewise, the readout circuit should make an AC measurement featuring a demodulation process so as to recover amplitude and phase of sensor impedance. Demodulation can be done in analog way using Gilbert cell [Manickam,10] or switched system [Gozzini,09] as analog multiplier. However, analog multipliers are usually noisy, hard to design, and sources of non-idealities and non-linearities.

To summarize, CTD sensors require a small electro impedance spectroscopy readout system able to achieve very-high resolution (i.e 15 bit or more) and low-power consumption, at the same time. It is clear that designing such a system is quite challenging.

To come up with those requirements we propose a fully-integrated EIS system based on a band-pass delta-sigma (BPDS) approach. Both signal generation and signal acquisition are integrated into chip. The use of BPDS converter allows acquiring and digitalizing the AC signal without the need of analog multiplier. Fig. 76 clarifies the proposed approach showing out the main building blocks. A delta-sigma modulated bit stream is fed to a voltage-to-current converter generating the 1KHz current sine wave stimulating CTD sensors. A fully-differential low-noise amplifier (LNA) acquires and amplifies

the voltage at CTD terminals. BPDS converter samples LNA output and digitize it. Then, demodulation process is fairly done in digital using two XOR gates. The EIS outputs are two digital data streams at 2KHz of sampling frequency containing information about the real and the imaginary part of sensor impedance, respectively. To recover the impedance value, the two data streams must be fed to an FPGA able to decimate at proper frequency. The EIS system has been designed to work at 1KHz but it allows operating frequency scalability so as to interface with different sensor classes and applications. Moreover, it will be capable of operating in an array mode.

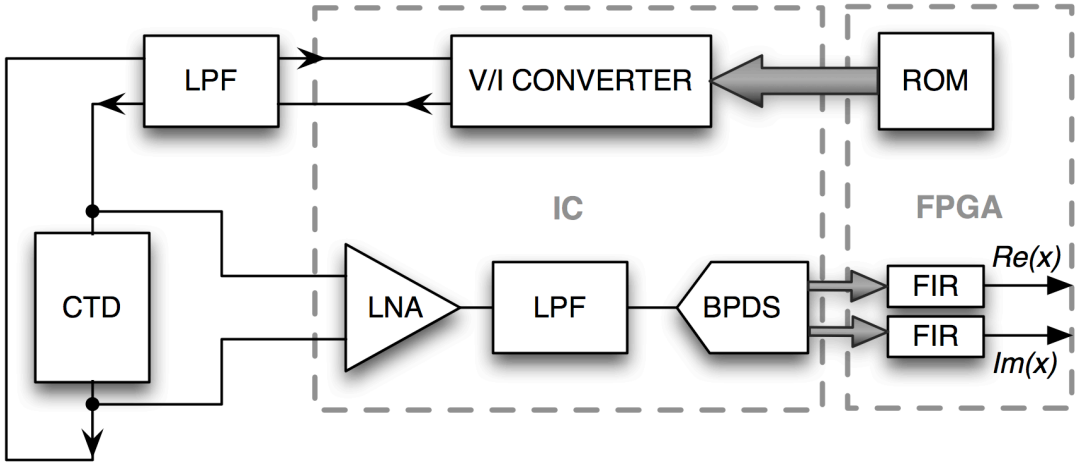

Fig. 76. Block scheme of proposed BPDS based EIS system. A delta-sigma modulated bit stream is fed to a voltage-to-current converter generating the 1KHz current sine wave stimulating the CTD sensor. A fully-differential low-noise amplifier acquires and amplifies the voltage at CTD terminals. BPDS converter samples LNA output and digitize it. BPDS approach allows easy demodulation process by digital circuits.

5.1.4 Noise Budget Design

Since the proposed system architecture is quite complex, it is subject to several sources of error and inaccuracy, such as thermal and quantization noise and jitter, affecting the overall accuracy and resolution. Both signal generation and acquisition have a significant impact upon the system resolution; thus they should be considered together in the noise estimation. The target precision has been calculated from the application requirements so as to set the voltage range at the LNA input to 90mV. More precisely, since the application requires the detection of a thousandth of a temperature degree over a scale of 30^0C, a minimum detectable signal (MDS) of approximately 2uV has been set, corresponding to $4pV^2$ of equivalent input-referred noise power.

The design, with respect to precision, was organized in two steps. First, the quantization noise limit referring to the input of the LNA was calculated from the required precision. Then, the architecture was designed to keep thermal noise lower than quantization noise, targeting 16-bit precision with a confidence error of 0.02% between adjacent levels. We chose a more strict requirement for random noise because there are many sources of noise in a mixed-signal integrated-circuit other than the ones taken into account in this section, such as: substrate noise, power line noise, coupling effects and so on.

Since sensor specifications require a full-scale (FS) voltage range of about 90mV, the total input-referred noise variance should be

$$\sigma^2 = \left(\frac{FS}{6 \cdot 2^{16}}\right)^2 \cong 52 f V^2, \tag{5.4}$$

where six MDS standard deviations were used so as to achieve the required degree of confidence. From the design point of view, the above constraint was equally shared between the current signal generation (i.e. sinusoidal reference and sensor) and the acquisition chain (i.e. LNA, LPF and BPDS), as shown in Fig. 77. This analysis considers noise due to the operational transconductance amplifiers, folding noise due to the sampling process of the filter, and kTC noise.

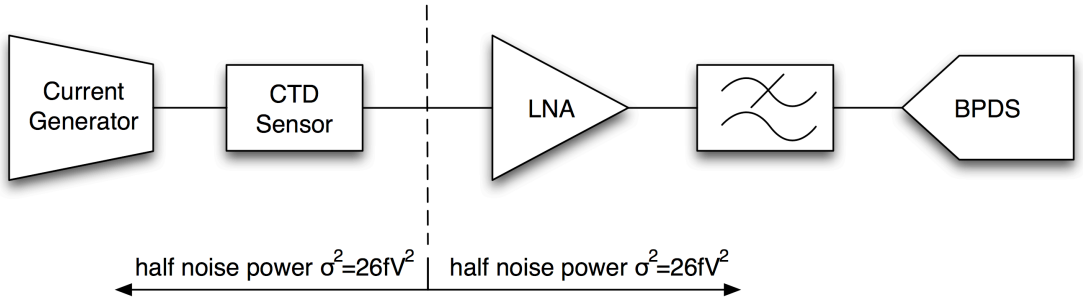

Fig. 77 The random noise budget, determined by (7.4), was equally shared between signal generation and signal acquisition.

The estimated jitter error is mainly related to the type of clock generator and the working frequency. In our case the clock signal is generated off-chip with sufficient accuracy using a commercial quartz oscillator. Moreover, the working frequency is fairly low at 1KHz. For discrete-time delta-sigma modulators the SNR due to jitter error can be computed as

$$SNR \cong 10\log\left[\frac{OSR}{4\pi^2\left(\frac{\Delta}{T}\right)^2\left(\frac{f_0}{f_S}\right)^2}\right] = 99dB, \tag{5.5}$$

where OSR is the oversampling ratio, Δ/T is the jitter error of the clock source, f_0 is the working frequency and f_S is the sampling frequency [Tao,99]. For discrete-time delta-sigma modulators the jitter error does not depend on the modulator order; therefore (5.5) is suitable for modulators of any order, and sets the ultimate achievable SNR performance for this level of jitter, which has been estimated in approximately $800fV^2$ of input-referred noise power, using commercially available clock generators.

5.2 Band-Pass Delta-Sigma Converter

5.2.1 Basic Principles[11]

Standard delta-sigma modulators are used to digitize analog low-pass signals for which the bandwidth is a small fraction of the sampling frequency. They consist of an integrator acting as low-pass filter, a comparator, a single bit DAC[12], and an adder. Now, substituting the integrator with a band-pass filter, it is possible to give rise to a band-pass converter known as band-pass delta-sigma converter (BPDS). This one is able to digitize narrowband signals modulated at frequency even comparable with the sampling frequency.

Usually, the input of BPDS converters is a IF (intermediate-frequency) or RF (radio-frequency) modulated signal characterized by a narrow bandwidth compared to the modulating frequency. At BPDS output there is the desired delta-sigma digital stream representing the input signal and surrounded by quantization noise. Then, a digital multiplier mixes to DC the delta-sigma stream, generating in-phase and quadrature signals. At the end, a digital low-pass decimator filter removes the out-of-band noise from both signals (Fig. 78).

[11] The material in this section is summarized from [Schreier,04] and [Maloberti,07].

[12] Multi-bit DAC can be used in delta-sigma modulators to increase SQNR, but they also increase complexity.

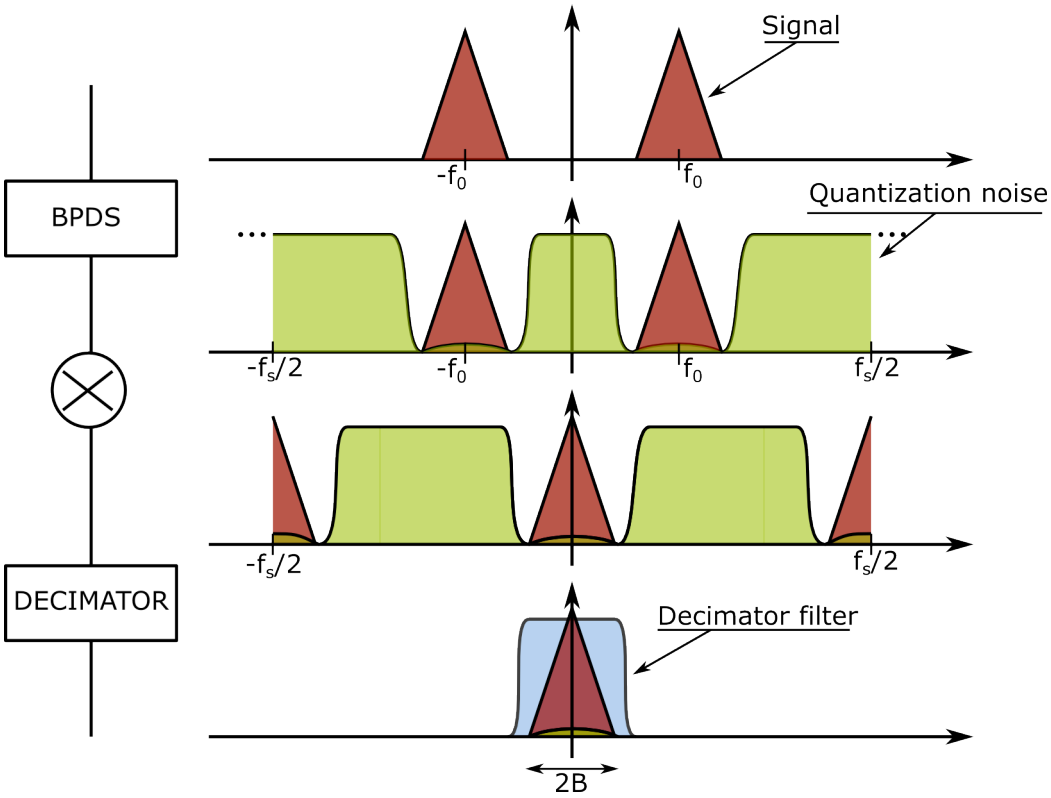

Fig. 78. Frequency domain representation of BPDS behavior. At BPDS output there is the modulated input signal with a shaped quantization noise, mainly concentrated at high frequency. The multiplier mixes the signal into DC and then the decimator filters out quantization noise and signal spectrum replica.

The main difference between low-pass delta-sigma and BPDS is the NTF. Indeed, for BPDS modulators the NTF has a stop frequency placed at a frequency f_0 that is the center frequency of the modulated signal, i.e. away from DC. However, BPDS modulators are usually derived from low-pass delta-sigma prototypes. The transformation z^{-1}->z^{-2} transforms a low-pass NTF with n zeros near $z=1$ into a band-pass NTF with $2n$ zeros: n zeros near $z=j$ and n zeros near $z=-j$. In this way the BPDS has an NTF similar to the original one but shifted to f_0 and replicated to $-f_0$. That transformation implies the sampling frequency must be

$$f_S = 4 f_0. \tag{5.6}$$

It is possible to demonstrate that BPDS modulators derived in such a way are equivalent to two copies of the original low-pass delta-sigma modulator, interleaved each other and working with alternating polarities. That means a $2n^{th}$-order BPDS has the same SQNR profile of a n^{th}-order low-pass delta-sigma modulator. That kind of BPDS is called pseudo two-path and leads to a design with reduced number of active elements, saving power and area. An

equivalent scheme of a pseudo two-path modulator is depicted in Fig. 79. There exist other transformations and other general schemes for BPDS modulators, but the pseudo two-path is the easiest one.

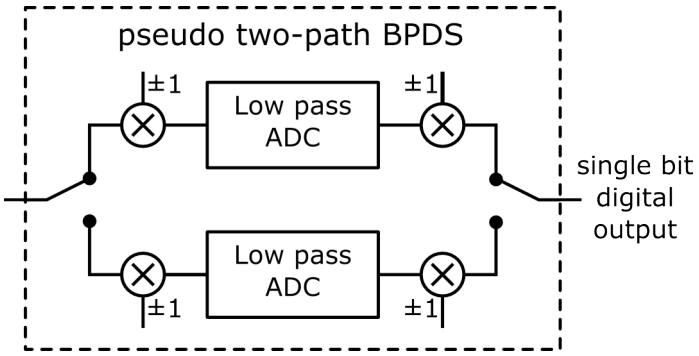

Fig. 79. Equivalent scheme for pseudo two-path BPDS modulator.

The *OSR* for BPDS modulators is defined in the same way as done for low-pass delta-sigma; it is

$$OSR = \frac{f_S}{2B} \tag{5.7}$$

where B is the two-sided bandwidth and f_S is the sampling frequency. Since B is lower than the modulating frequency, BPDS converters allow sufficiently high *OSR* values with a sampling frequency f_S slightly higher than the modulating frequency f_0. Note that BPDS output can be decimated by a factor of *2OSR* without loosing information because it is composed of 2 data streams (complex data).

BPDS modulators preserve many of lowpass delta-sigma advantages such as linearity, simple anti-aliasing filtering, high tolerance to analog component imperfection, and bandwidth-resolution trade-off. Moreover, they show other two great advantages in comparison with other types of ADC:

1- They eliminate the need of analog down-conversion preserving the separation between signal and low frequency noise;
2- They are more power efficient since focus the power consumption on accurate conversion of interesting bandwidth.

5.2.2 Architecture

To address all the accuracy and power requirements of CTD sensor we decided to use a 4th-order pseudo two-path BPDS. The pseudo two-path

solution permits us to minimize area and power consumption, due to a lower number of active elements. According to (5.6) a carrier frequency of 1KHz forces a sampling frequency of 4KHz, corresponding to a 2KHz sampling of both real and imaginary signals. Following (5.7), the 10Hz signal bandwidth and the 2KHz sampling frequency impose an *OSR* of 100. Therefore, a 4th-order modulator is required to reach the desired resolution. Indeed, the *SQNR* of a 4th-order 1-bit BPDS modulator with *OSR*=100 is

$$SQNR = 6.02 + 1.78 - 12.9 + 50\log(OSR) = 94.9dB \tag{5.8}$$

corresponding to 15.76-bit resolution [Maloberti,07]. Note that (5.8) is the *SQNR* formula for a standard 2nd-order low-pass delta-sigma modulator.

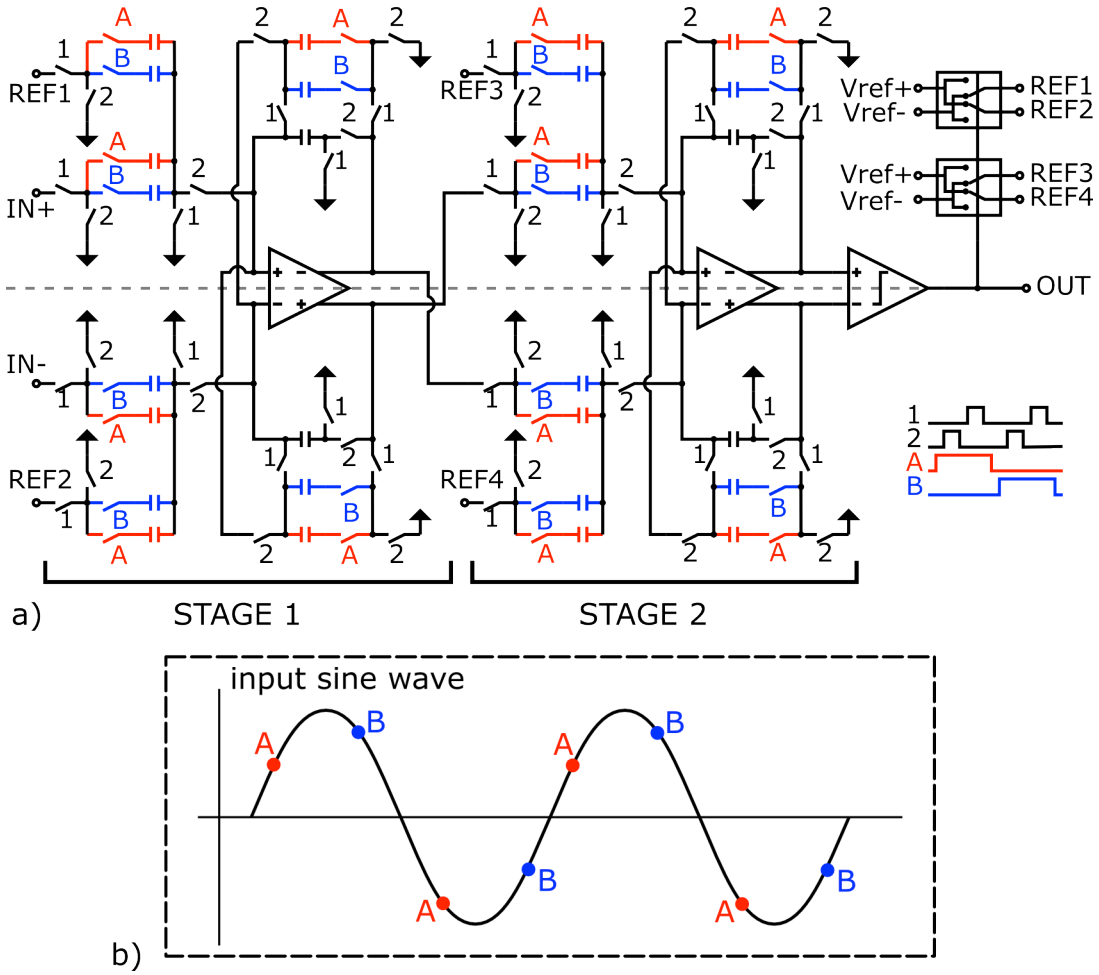

Fig. 80. a) Proposed 4th-order pseudo two-path BPDS architecture based on two symmetric stages. The two paths (A and B) share the same active elements so as to reduce power and area. b) BPDS samples the input sine wave 4 times for each period and sends the samples to path A and B, alternatingly.

The proposed architecture for a pseudo two-path BPDS modulator, depicted in Fig. 80-a, is based on previous works [Palmisano,88], [Francesconi,97]. It consists of two fully symmetric switched-cap stages working between two reference voltages (V_{REF-}=*1.2V* and V_{REF+}=*2.1V*) centered on a common-mode (CM) voltage (*Vcm=1.65V*). The cross-connections at the input of each stage perform the multiplication by ±1 shown in the equivalent two-path scheme of Fig. 79.

For simplicity we will consider only the first stage, since the second stage works in the same manner. The architecture samples the input sinusoid at exactly four times its frequency and alternates sending the samples to one branch or the other, where these samples are digitized (Fig. 80-b). Note that the two branches share the same active elements in a sort of time-interleaving scheme. When branch A is active, all the switches denoted by label A are closed and those denoted by label B are open. When branch B is active the opposite happens.

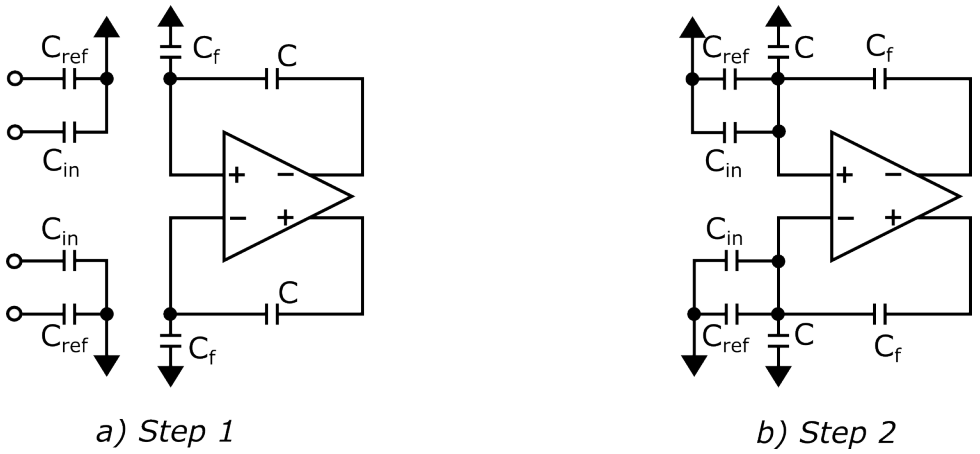

Fig. 81. Representation of BPDS two-step working mode for a single stage. a) In step 1 BPDS stores the result of previous sum and precharge input capacitors for next sum. b) In step 2 BPDS sums together charges stored onto input capacitors.

Both branches work in a two-step mode. The first step is the one identified with phase number 2. In this period the stage sums all the charges stored on capacitors *C*, C_{ref}, C_{in} and saves the result on C_f. Then, when phase 1 is active (second step), the result of the sum is stored on capacitor *C* while C_{in} and C_{ref} are precharged to the input and reference values, respectively. The two steps start again for the other branch. As depicted in Fig. 80, the phases controlling the two-step behavior are two non-overlapping square waves at 4KHz, which is the sampling frequency. Table 9 summarizes the system timing regarding both 2-step behavior and branch interleaving.

Because of the time shift of 1/4 of the sinusoid period (equivalent to 90° phase difference) between the samples going to one branch with respect to the other, the final digital outputs are the in-phase and the quadrature component of the input signal.

Phases signals depicted in Fig. 80-a are generated internally from the external 1MHz clock signal by a digital frequency divider circuit. Hence, it is possible to simply change BPDS working frequency f_0 by varying the clock frequency. 2MHz clock will set BPDS working frequency to 2KHz keeping all perfectly working.

Active Branch	Step	Action
A	2	Both stages sum together charges stored onto input capacitors and save the result on feedback capacitor C_f.
A	1	Both stages store the result of the previous sum onto capacitor C_a and precharge the input capacitors for the next summing step.
B	2	Both stages sum together charges stored onto input capacitors and save the result on feedback capacitor C_f.
B	1	Both stages store the result of the previous sum onto capacitor C_b and precharge the input capacitors for the next summing step.

Table 9 Timing of proposed pseudo 2-path BPDS.

5.2.3 Low-Power Fully-Differential OTA

The core element of the BPDS shown in Fig. 80-a is the fully-differential operational transconductance amplifier (OTA). The main requirement on the OTA is the power consumption. Since the delta-sigma modulator follows a gain stage (i.e. the LNA as in Fig. 76), the noise requirement can be relaxed a little bit. For these reasons, a single stage scheme seems the best choice. We opted for a standard fully-differential folded cascode operational transconductance amplifier because it is a simple and strong architecture

which exhibits high gain, satisfying output range, solid stability issue, and finally it is very compact [Gray,01], [Razavi,01]. Fig. 82 illustrates the schematic of the designed OTA. The system has been designed using AMS-C35B4C3 technology provided by Austriamicrosystem, which features $0.35\mu m$ minimum channel length [AMS,11]. One separate circuit, shared between each low-power OTA, generates the polarization voltages V_{B0}, V_{B1}, and V_{B3}. The *Vcm* is a temperature-stabilized voltage coming from a band-gap reference circuit.

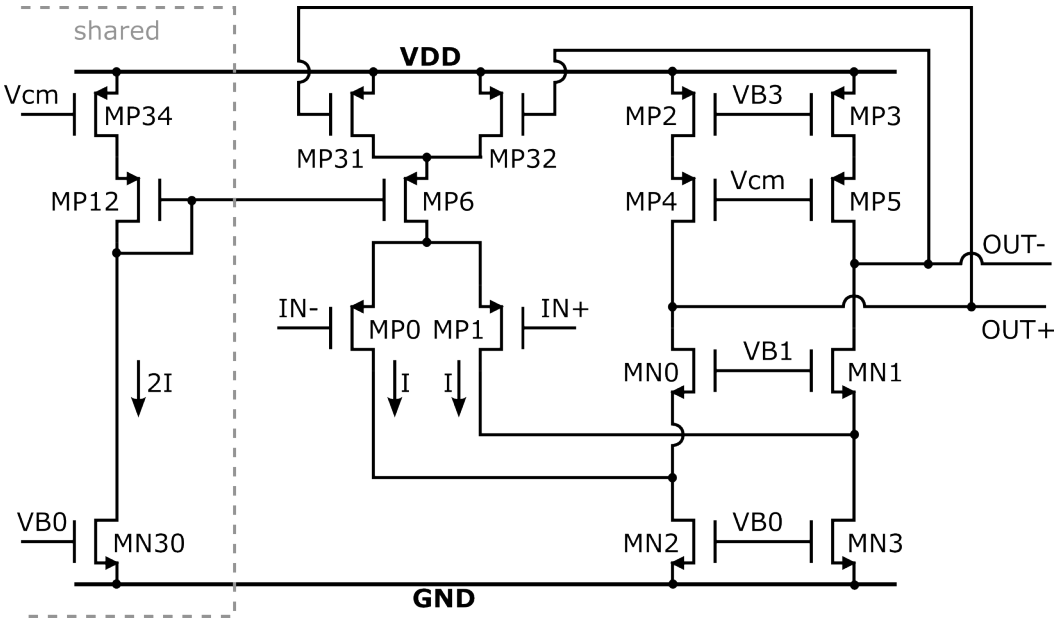

Fig. 82. Schematic of low-power fully-differential OTA employed in the BPDS. It is a standard folded-cascode architecture, employing transistors in the linear region as CMFB. The input differential pair is polarized in W.I. maximizing the g_m/I ratio. The branch in the left of the picture, used by the CMFB as CM reference, is shared between different OTA implementations so as to reduce the total power consumption.

Although the noise topic can be relaxed as stated before, it is always a major concern if we want to reach the 15-bit accuracy. As usually known, p-type input pair displays lower flicker noise, but higher thermal noise, than n-type input pair (Fig. 83). Equating p-type and n-type noise formulae, for equally sized transistors, we obtain a corner frequency f_X. P-type pair is less noisy for systems working at frequency below this corner, while n-type pair is better for systems working at frequency above the corner. For the used CMOS technology the corner frequency f_X is

$$\frac{8}{3}\frac{kT}{g_{m,nM}}+\frac{K_{f,nM}}{C_{OX}WL}\cdot\frac{1}{f}=\frac{8}{3}\frac{kT}{g_{m,pM}}+\frac{K_{f,pM}}{C_{OX}WL}\cdot\frac{1}{f}$$
$$f_x \cong -3\frac{\mu_n\mu_p}{\mu_p-\mu_n}\cdot\frac{K_{f,nM}-K_{f,pM}}{8KT\cdot L^2}\cong 20KHz, \quad (5.9)$$

where μ_n and μ_p are nMOS and pMOS mobility, $K_{f,n}$ and $K_{f,p}$ are the flicker parameters, and L is the channel length, which has been set to $0.7\mu m$. Equation (5.9) states that p-type pair is the right choice concerning our 1KHz application.

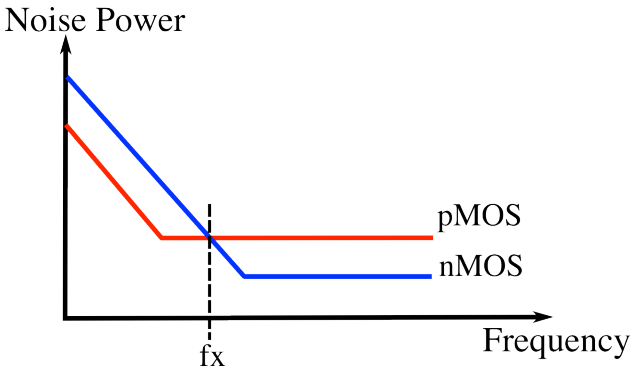

Fig. 83. Comparison between typical pMOS and nMOS noise PSD. For a given technology it is possible to define a corner frequency dividing the frequencies where pMOS are less noisy, from the frequencies where nMOS are less noisy.

Our starting goal was power consumption around 20µW, thus a current consumption lower than 6µA for 3.3V supply. Since leading OTA features are related to the input pair we allocated 2.4µA to it and around 1µA for cascoded branches. The common-mode feedback (CMFB) consumes the residual current, as will be discussed later. The output current is not a primary concern, since the OTA will work in a switched capacitor system characterized by large time frames (i.e. 256µs).

Polarizing the pMOS input differential pair, consisting of MP0 and MP1, in weak inversion, we can maximize g_m/I ratio and minimize systematic input offset [Enz,96]. Usually, a transistor is said in strong inversion (S.I.) if its inversion coefficient (I.C.) is greater than 10, and in weak inversion (W.I) if IC is lower than 0.1; for value in between, the transistor is polarized in moderate inversion. The I.C. parameter is defined as

$$I.C.=\frac{I_D}{I_S}, \quad (5.10)$$

where I_D is the drain current and I_S is the moderate inversion characteristic current given by

$$I_S = 2n\mu C_{OX} V_{th}^2 \cdot \frac{W}{L}, \tag{5.11}$$

where n is the subthreshold slope factor, C_{OX} is the oxide capacitance per unit area, and V_{th} is the thermal voltage. We chose an I.C.=0.05 for the input pair so as to polarize it in deep weak inversion; thus the form factor for MP0 and MP1 can be computed as

$$\begin{aligned} I_S &= \frac{I_D}{I.C.} = 24\mu A \\ \left.\frac{W}{L}\right|_{M0,M1} &= \frac{I_S}{2n\mu C_{OX} V_{th}^2} = 250. \end{aligned} \tag{5.12}$$

Large input transistors will also decrease the flicker noise [Gray,01]]. For transistors polarized in W.I., the transconductance g_m is almost given by [Harrison,03]

$$g_m \approx \frac{I_D}{nV_{th}} \cdot \frac{2}{1+\sqrt{1+4IC}}, \tag{5.13}$$

and for our input pair this means

$$g_m = 33\,\mu A/V. \tag{5.14}$$

Now, we can estimate both gain-bandwidth product (GBW) and input-referred noise only due to the input pair [Gray,01], [Razavi,01]

$$GBW\big|_{C_L=5pF} \approx \frac{g_m}{C_L} \approx 6MHz, \tag{5.15}$$

$$\overline{v_{in}} = \sqrt{\frac{8}{3}\gamma \frac{kT}{g_m}} \approx 13nV/\sqrt{Hz}. \tag{5.16}$$

The GBW given by (5.15), as well as the noise expressed in (5.16), are sufficient for our application. Indeed, for the required input full scale (FS), that is 900mV, the noise should be lower than

$$v_{in-rms}\big|_{B=10} = \sigma = \frac{FS}{6 \cdot N} = \frac{900mV}{6 \cdot 2^{16}} \approx 2.3\mu V_{rms} \Rightarrow \overline{v_{in}} = \sqrt{\frac{\sigma^2}{10}} \approx 700nV/\sqrt{Hz} \tag{5.17}$$

in order to reach the 16-bit accuracy over random noise[13]. This means the other transistors of this OTA can be designed regardless the noise performance. The remaining transistors have been mainly designed to meet high gain, stability, and output swing requirements. Table 10 summarizes dimensions and operating condition of the transistors depicted in Fig. 82. The exact sizes of the transistors employed in this OTA, have been optimized during both transistor level simulation and layout design.

Devices	W/L (µm)	I_D (µA)	g_m (µA/V)
MP0, MP1	175/0.7	1.2	31
MN0, MN1	14/0.7	0.4	10
MP2, MP3	2.8/1.4	0.4	6.3
MP4, MP5	10.5/0.7	0.4	8.6
MN2, MN3	1.4/1.75	1.6	16
MP6, MP12	4.2/1.4	2.4	24
MP31, MP32	0.7/1.75	1.2	/
MP34	1.4/1.75	2.4	/
MN30	2.1/1.75	2.4	/

Table 10 Sizes and operating conditions of transistors used in Fig. 82.

Since it is a fully-differential OTA, the common-mode feedback holds a crucial rule. The employed CMFB is based on transistors MP31, MP32 and MP34 working in the linear region [Gray,01], [Razavi,01]. The same current flows in MP6 and MP12, thus they have the same V_{GS}. Sizing MP34 double than MP31 and MP32, they must have the same V_{DS} and V_{GS}, implying output CM voltage equal to V_{CM}. The negative feedback can be demonstrated analyzing variation on the CM output. If both V_{OUT-} and V_{OUT+} increase, then the V_{GS} of MP31 and MP32 lowers and the current flowing into the input pair decreases. However, the current in MN2 and MN3 is constant and thus cascoded branches must counteract by decreasing the output voltages. Note that the left branch in Fig. 82 is shared between different OTA instances, in order to further reduce the power consumption.

The OTA has been heavily tested during both design and layout. Table 11 briefly summarizes simulation results. To better compare the designed OTA

[13] Please refer to section 5.1.4 for more details on noise budget.

with other architectures presented in the literature, we also show the GBW figures of merit (FOM_{GBW}) [Laker,94]:

$$FOM_{GBW} = \frac{GBW \cdot C_L}{I_{TOT}} = 4.5\frac{MHz \cdot pF}{\mu A}, \tag{5.18}$$

where C_L is the load capacitance and I_{TOT} is the total current consumption. Note that only half of the current flowing into MN30 is taken into account in I_{TOT}, because that branch is shared between two instances of the same OTA.

Parameter	Schematic Simulation	Post-layout Simulation
GBW @C_L=5pF	4MHz	4MHz
A_{DM}	90dB	90dB
PM	68°	69°
A_{CM}	-25dB	-14dB
CMRR	115dB	103dB
PSRR	233dB	227dB
v_{in} | @f=1KHz	120nV/√Hz	112nV/√Hz
Corner Frequency	7KHz	7KHz
Output DR	0.3V÷2.55V	0.3V÷2.5V
CM Input Range	0.7V÷2.8V	0.7V÷2.8V
Differential input offset	≈100μV	3mV

Table 11 Summarize of primary performance of the low-power OTA employed in the BPDS.

5.3 Delta-Sigma Modulated Current References

5.3.1 High-Precision Current Sine Wave Generation

The integration of stimulus generation into the IC is a very important feature, since the precision of the entire system is related to that one of the reference signal. Hence, the measured system accuracy will be the real accuracy, unaffected by "ideal" measurement set-up. It is to point out that impedance interfaces presented in the literature usually employ external stimulus generator to reach the desired precision [Manickam,10], [Ferrari,09], [Levine,08], [Yang,09]. This is somehow misleading, since the real laboratory experiments will be a little bit different from papers outcomes.

To generate the high-precision sinusoidal signal we proposed to use a delta-sigma digital-to-analog converter (DAC). In this way, we can take benefit from the delta-sigma noise shaping so as to create a 16-bit sine wave. More precisely, we make a single bit delta-sigma stream by software using a Matlab™ script. A read only memory (ROM), mounted in a FPGA, stores the delta-sigma modulated bit stream, which is at a frequency rate proportional to the system clock, thus it is always synchronized with the succeeding BPDS ADC. Studying the frequency spectrum, it is possible to discern the single tone component and the shaped noise, as shown in Fig. 84.

The digital output of the ROM is converted into a current with the possibility of choosing among several transconductance values.

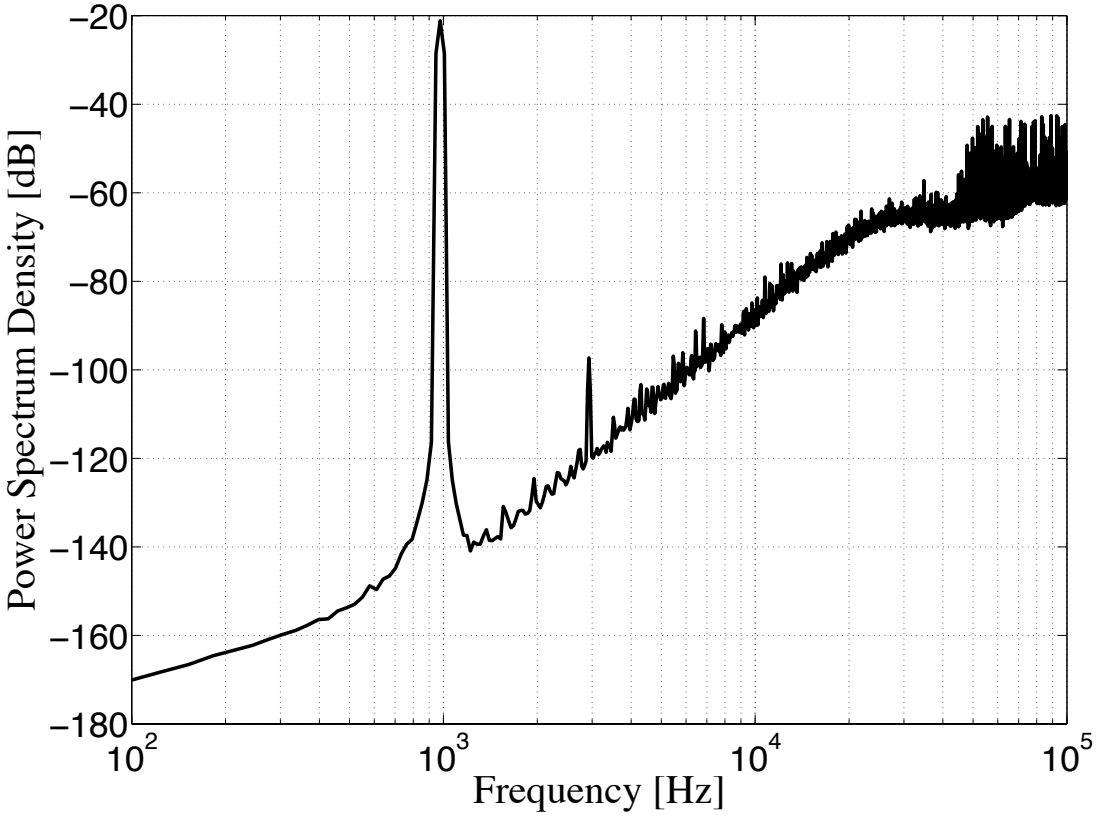

Fig. 84 Frequency spectrum of delta-sigma modulated data stream stored in the ROM. The graph clearly shows the noise shaping of the spectrum.

The proposed solution has many advantages:

1- It saves area and power, since the DAC is implemented via software
2- It is flexible and easily customizable for different applications
3- It allows adjusting the phase errors in the measurement with simple and fast changes on the Matlab script for delta-sigma data generation.

However, the current signal has a lot of high frequency noise lowering power efficiency and requiring many filtering stages throughout the acquisition chain. Indeed, it needs an external LPF before the sensor and another filter before the ADC.

5.3.2 Current Generator

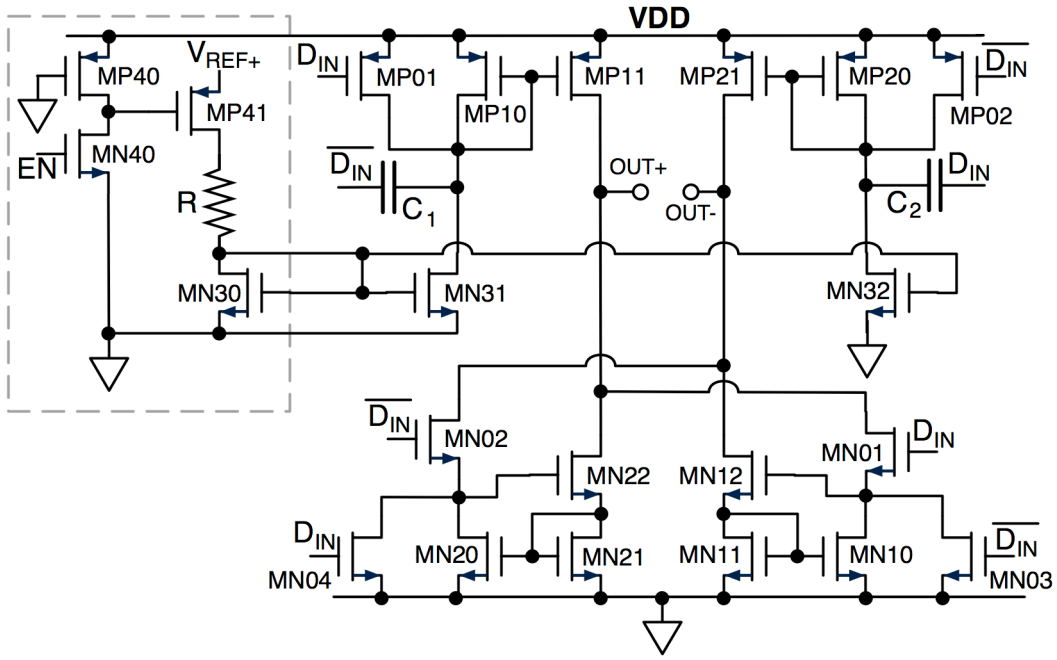

Fig. 85 Schematic of the current generator. It is based on an H scheme with two symmetrical half-circuits working in switched mode. When one half-circuit is on, it pushes the current into OUT+ and drains from OUT-. When the other half-circuit is on, it pushes the same current into OUT- and drains from OUT+.

The data stored in the ROM is fed into a circuit converting the voltage bit stream into a current bit stream switching between $+I_{REF}$ and $-I_{REF}$. An example of current bit stream is shown in Fig. 87 left. The current generator circuit shown in Fig. 85 is based on a so-called "H-scheme". The branches in the dashed box in Fig. 85 create a DC current proportional to V_{REF+}, which is the same voltage used in the BPDS, realizing a ratiometric measurement. This current is mirrored on MN31 and MN32. Depending on the digital input signal D_{IN}, only one of these MOS devices is active. In this way, the circuit pushes a current into the positive output and drains from the negative output, and vice versa.

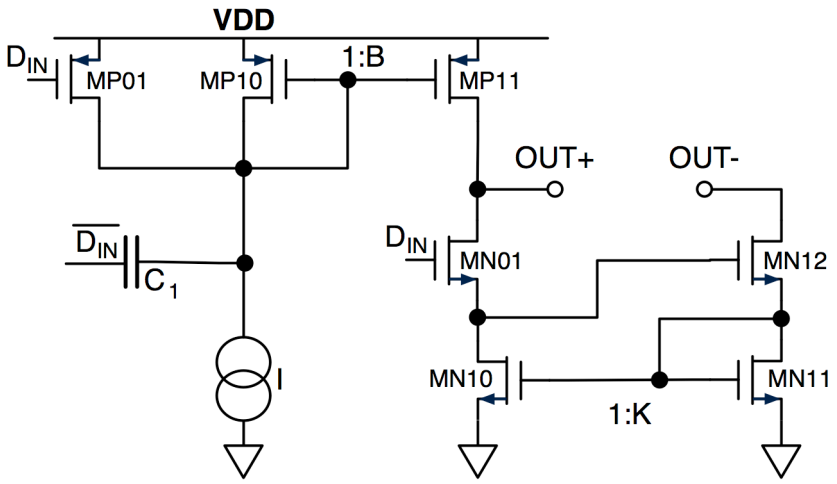

Fig. 86 Current generator half circuit. The pMOS current mirror amplifies the current of a factor B to achieve the desired value. The nMOS current mirror has a mirror factor K in the order of 1000 or more, so as to force the current flows into MN12 and not into MN01.

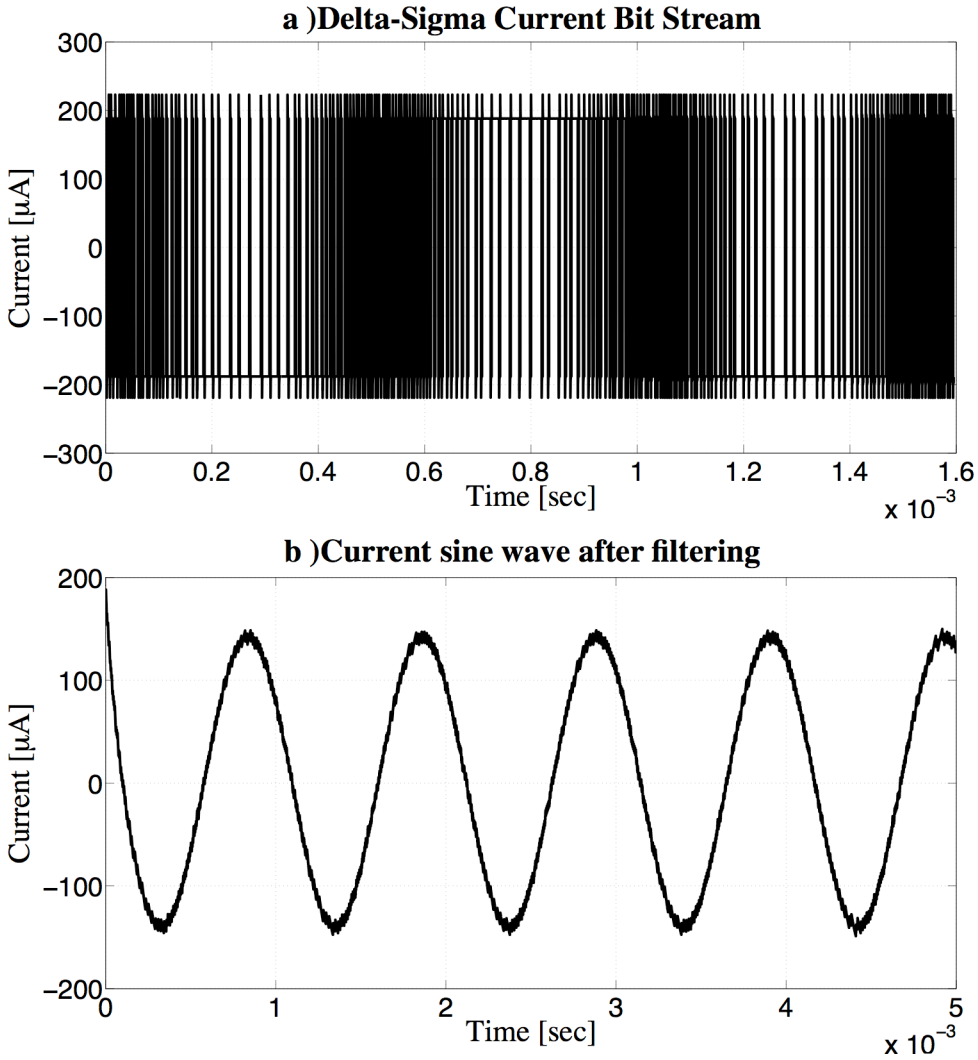

Fig. 87 a) Example of delta-sigma current bit stream modulating 150µA sine wave. b) After the low-pass filtering, the current sine wave is more evident.

For sake of simplicity let $D_{IN}=1$ and focus only on left-half circuit shown in Fig. 86; the other half circuit is switched off. Since D_{IN} is high, MP01 is deactivated and the current is mirrored on the *OUT+* branch with scaling factor B. The 1:K ratio of the current mirror MN10:MN11 forces the current to flow into the output load. Then, the current returns into the circuit flowing through MN12 and MN11. When $D_{IN}=0$, this half-circuit turns-off and the other one starts pushing the current into *OUT-*. Capacitors C_1 and C_2 create a voltage bump during D_{IN} switching so as to speed up the half circuit activation.

At the current generator output, an external LPF filter is needed to achieve maximum linearity and minimum total harmonic distortion (THD). The current sine wave after filtering is shown in Fig. 87, b). The circuit has been replicated four times, allowing the user to choose among the four current sine waves with amplitude 10μA, 150μA, 300μA, and 1mA.

5.4 Low Noise Amplifier

5.4.1 Architecture

Fig. 88 shows the schematic of the proposed low-noise voltage amplifier. It is based on a rather common fully-differential amplifier. The midband gain *G* is set by the ratio C_2/C_1, where C_2 can be chosen among eight different capacitors. The allowed gains are 0.5, 1, 2, 5, 10, 20, 50, and 100. Together with the four current sine waves, it gives a strong flexibility to the entire EIS system. For the targeting CTD application the usual gain is *G=10*. This will be the standard value from here on.

AC coupling on the input pins blocks the DC offset and the low voltage drift. This is an important feature mainly for nanowire applications where voltage drifts strongly affect the functionality.

The major issue of the proposed architecture is the presence of floating nodes X. To set the DC value and lower the high sensibility on leakage currents and stray disturbs, a MOS-bipolar device, acting as pseudoresistor, has been placed at node X [Harrison,03]. For negative V_{GS} the MP transistors act as diode-connected pMOS transistors. For positive V_{GS} the MOS transistors

are deactivated but the parasitic pnp bipolar devices (source-well-drain) are active and work like diode-connected BJTs. In this way, the MP transistors implement nonlinear incremental resistors keeping the right DC value at nodes X.

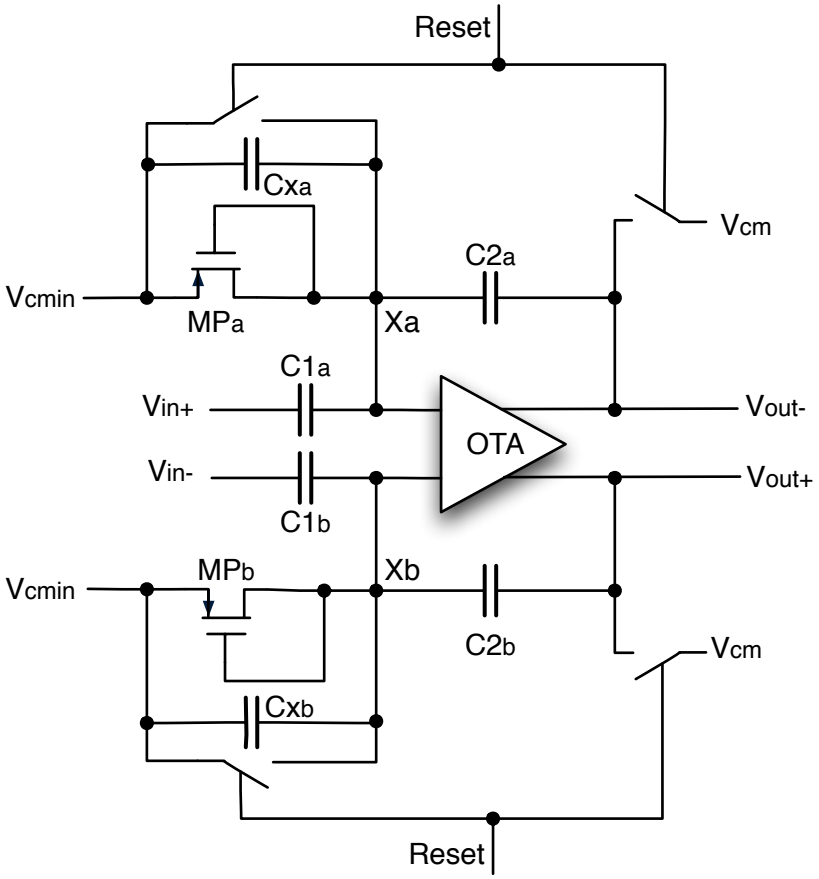

Fig. 88 Architecture of the fully-differential low-noise amplifier. The midband gain is set by the ratio C_2/C_1. The pMOS transistors work as nonlinear incremental resistors so as to set the correct DC value at nodes X. They implement very high resistances, in the order of tera-ohm. To speed it up an asynchronous reset is used, lasting only 250μs.

Fig. 89 shows the differential resistance of the MP pseudoresistor for various voltages applied. For small voltages across the device, the equivalent resistance is very high (i.e. in the order of tera-ohm). The pseudoresistor element is not in shunt feedback as usually done [Harrison,03], because the CM voltage at the OTA input must be different from the one at the output. Indeed, the employed OTA has an input range shifted to low voltages, as will be discussed in section 5.4.2.

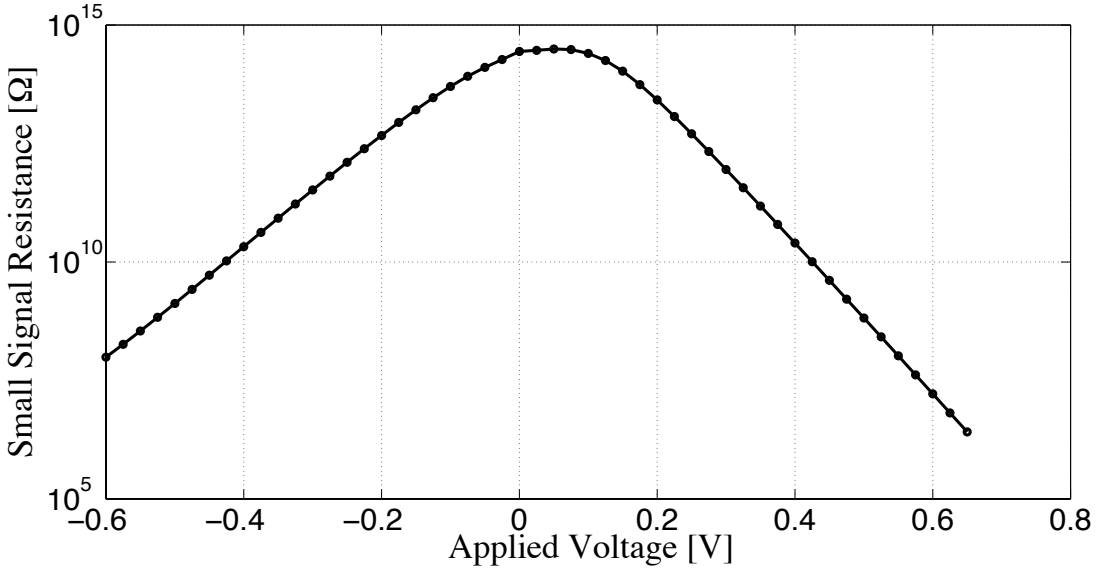

Fig. 89 Incremental small-signal resistance of mos-bipolar pseudoresistor MP for different voltages applied. It is sized as follow: W=4μm and L=2μm.

The high resistances realized by MP pseudoresistors imply very long time constants, especially at the system start-up. To speed it up, an asynchronous reset system has been added (Fig. 90). It monitors each single output of the amplifier. If the signal is higher than the maximum allowed output voltage (V_{REF+}), then a train of pulses, lasting 250µs each one, turns on the switches. By means of "**Force**" pin, reset circuit is also active while SPI interface acquires the programming signals, realizing a start-up-reset. Note that, while the LNA is in the reset phase, the input pins are floating and teh capacitors C_1 are shortened to *Vcm*.

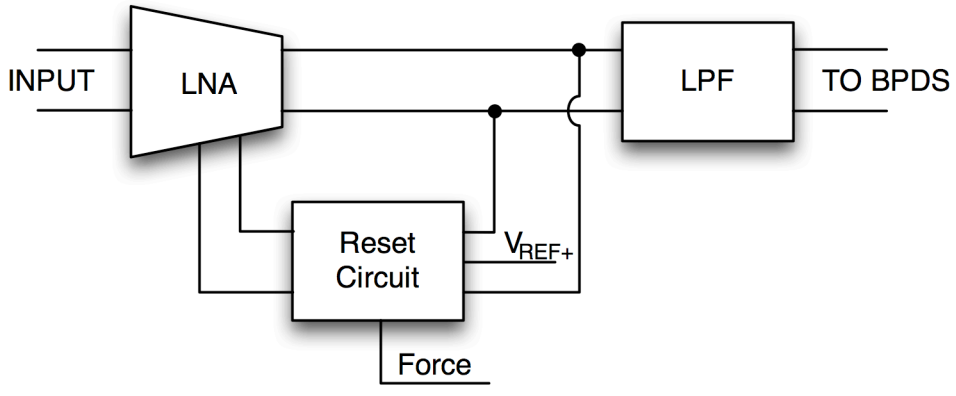

Fig. 90 Asynchronous reset that constant checks the LNA output. If the LNA output signal is in a forbidden region, then the system resets the LNA output as well as the internal floating nodes. The "Force" signal comes from the SPI to forces reset while the system is in programming mode.

The input signal coming from the sensor is not a purely differential signal; it could have a large CM component. Assuming a Wheatstone bridge that employs a standard 1KΩ platinum resistance thermometers (PRTs) supplied by a current sine wave with amplitude 1mA. The output voltage will be a CM sine wave of amplitude 500mV plus a smaller DM sine wave holding the temperature information. To arrange such a large CM input voltage signal, C_X capacitors have been added on nodes X. In this way, the CM voltage signal at nodes X is lowered following

$$v_X = \frac{C_1 v_{IN} + C_2 v_{OUT}}{C_1 + C_2 + C_X}. \tag{5.19}$$

At LNA output, the CM signal is eliminated by the high OTA CMRR.
The C_X capacitors do not affect the midband gain G

$$G = \frac{C_1}{C_2 + \dfrac{C_1 + C_2 + C_X}{A_0}} \approx \frac{C_1}{C_2}, \tag{5.20}$$

providing the OTA has a sufficiently high open-loop gain A_0. However, they will reduce the bandwidth

$$f'_{-3dB} = f_{-3dB}\left(1 + \frac{A_0 C_2}{C_1 + C_2 + C_X}\right), \tag{5.21}$$

where f_{-3dB} is the OTA first pole.

The principal noise source in Fig. 88 is the operational transconductance amplifier. The LNA input-referred noise can be related to the OTA noise as:

$$\overline{v^2_{in-LNA}} = \left(\frac{C_1 + C_2 + C_X}{C_1}\right)^2 \cdot \overline{v^2_{in-opamp}}. \tag{5.22}$$

Equation (5.22) states that capacitor C_X will also increase the input-referred noise by a factor of approximately 1.6. That will be taken into account in the OTA design.

5.4.2 Low-Noise Low-Power Fully-Differential OTA

The design of this OTS is harder than the previous one; mainly because it should meet very low-noise requirement in a low power context. Section 5.1.4

gives a thermal noise budget of approximately $25fV^2$ for the reading chain; that means an input-referred noise voltage of 50nV/√Hz for 10Hz bandwidth. Thanks to first stage gain, the noise of following stages could be neglected, and the above noise budget could be entirely allocated to the LNA. However, the presence of capacitors C_X reduces the allowed OTA input-referred noise voltage to value lower than 30nV/√Hz.

The schematic of the operational transconductance amplifier is shown in Fig. 91. It is a two-stage amplifier with 14.2μA flowing in the first stage and 300nA flowing in the second stage.

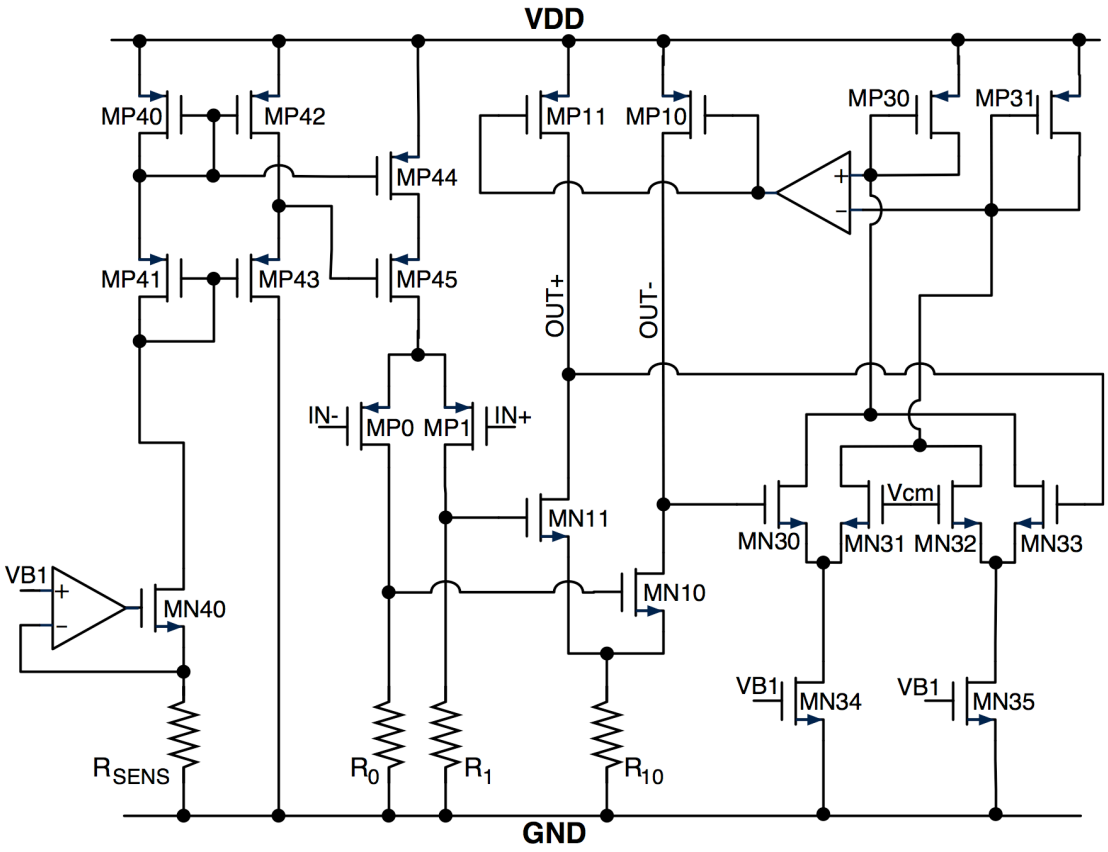

Fig. 91 Schematic of the low-noise low-power fully-differential OTA. It is a two stage OTA employing DDA as CMFB. The input differential pair, as well as the common source stage, is polarized in the weak inversion region. The first stage is resistive loaded so as to reduce flicker and thermal noise. Unusually, the low frequency pole is related to second stage, therefore capacitive loading the output nodes can stabilize the OTA.

The input differential pair is polarized in moderate/weak inversion, maximizing g_m/I ratio, which means minimize the noise power for a given current consumption. To further lower flicker and thermal noise, the input pair is realized using large pMOS devices purely resistive loaded, since passive resistors are less noisy than active elements [Ferrari,09]. The first stage has a voltage gain of approximately 10, slightly relaxing noise requirements

on the second stage. The load resistors also act as CMFB for this first stage. Indeed, the output CM voltage of the first stage is fixed to

$$V_{OUT1-CM} = \frac{R \cdot I_{TAIL}}{2}, \tag{5.23}$$

where R is the load resistance (i.e $R=R_0=R_1$) and I_{TAIL} is the tail bias current.

The tail current generator is an high-swing cascoded current mirror, because it increases the CMRR with a minimum reduction on the input range [Gray,01]. It limits the input range to voltages lower than 2.2V. On the other hand, the resistive load does not introduce any lower bound to the input voltages. As a result, the allowed input range is pushed to ground. The simple OTA connected in feedback with MN40 works to make the tail current more process independent.

The second stage is composed of two symmetric common-source (CS) amplifiers with source degeneration. Since the first stage gain is not so high, all the MOSes in the second stage are again polarized in weak or moderate inversion. In this way, load transistors show a greater output resistance increasing the stage gain. This second stage has a gain equal to 100 for a total open-loop gain A_0 of 60dB.

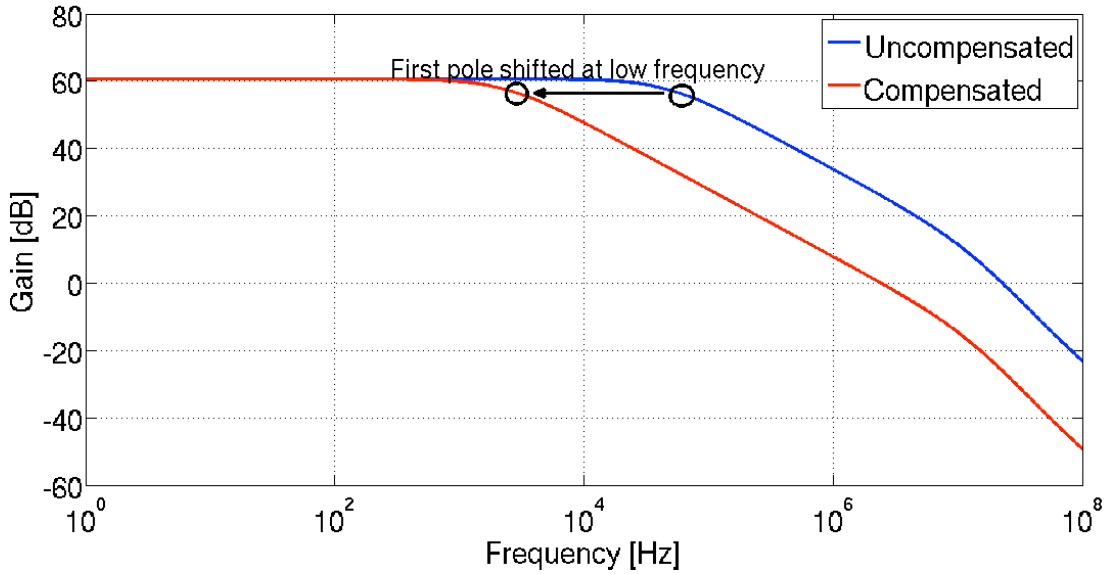

Fig. 92 Open-loop gain vs frequency. The blue line shows the gain for the uncompensated OTA. The low frequency pole is placed around 40KHz and it is related to the second stage. The red line shows the gain for the OTA with 5pF compensation capacitances placed on the output nodes. The compensation process shifts the low frequency pole to 2KHz.

Usually, a 2-stage OTA has higher current consumption in the second stage. Instead, the proposed OTA has higher current flowing into the first stage to better address noise requirements, and lower current in the second stage to minimize the power consumption. This causes a pole flipping. Fig. 92 shows the Bode diagram of the OTA, where the first pole placed around 40KHz is unusually related to the second stage. This kind of system can be stabilized placing a load capacitor on the output node, so as to shift the low frequency pole to the left of the Bode diagram.

Table 12 summarizes dimensions and operating conditions of each transistor shown in Fig. 91. As usually, the final sizes results from an optimization process throughout OTA simulations.

Devices	W/L (µm)	I_D (µA)	g_m (µA/V)
MP0, MP1	336/0.7	7.1	168
MP44, MP45	101/2	14.2	210
MP40, MP42, MP43	17.25/2	2.45	37
MP41	17.25/10	2.45	20
MN40	11/4	2.45	37
MN10, MN11	59.5/0.35	0.3	84
MP10, MP11	2.5/7	0.3	30
MN30 – MN33	1/25	0.41	1.8
MN34, MN35	1.8/18	0.82	4.3
MP30, MP31	0.7/7	0.82	2.4

Table 12 Sizes and operating conditions of the transistors used in Fig. 91.

The CMFB circuit that uses transistors in triode region has a low gain and it is intrinsically slower than differential amplifier [Sansen,06]. In this OTA we need a stronger and faster CMFB. For this reason, we used a differential difference amplifier (DDA) as CMFB. It makes the difference between the CM output voltage and the voltage reference *Vcm*, using two differential pairs. The resulting error is amplified and fed back in the gate of MP30 and MP31. To enlarge DDA input voltage range, the nMOSes used in the differential pairs are polarized with large overdrive voltages. However, this solution lowers the CMFB gain, requiring an additional gain stage in the CMFB loop, thus increasing the power consumption.

Resulting performances from schematic simulations and post-layout simulations are summarized in Table 13. The OTA is fast enough for the target application with total power consumption around 33μA. However, it should need more bandwidth so as to read impedance up to tens of MHz. Additionally, noise performances are well below the requirements with a corner frequency as low as 400Hz. This is crucial, since the following switched capacitor filter will increase the noise due to a folding process.

Parameter	Schematic Simulation	Post-layout Simulation
GBW @C_L=5pF	2.5MHz	2MHz
A_{DM}	60dB	60dB
PM	76°	78°
A_{CM}	-90dB	-89dB
CMRR	150dB	149dB
PSRR	322dB	188dB
$v_{in}|_{@f=1KHz}$	17nV/√Hz	18.5nV/√Hz
Corner Frequency	400Hz	450Hz
Output DR	0.08V÷2.25V	0.08V÷2.25V
CM Input Range	0V÷2.2V	0V÷2.2V
Differential input offset	70nV	600μV

Table 13 Summarize of primary performances of the OTA shown in Fig. 91.

The GBW FOM is

$$FOM_{GBW} = \frac{GBW \cdot C_L}{I_{TOT}} \approx 0.4 \frac{MHz \cdot pF}{\mu A}, \tag{5.24}$$

where all branches have been considered, due to both bias circuitry and CMFB. This FOM is somehow misleading since it does not take the noise into account. Indeed, the proposed OTA consumes a lot of power to lower the noise. A more appropriate figure-of-merit is the noise efficiency factor (NEF) given by [Steyaert,87]

$$NEF = v_{in-rms}\sqrt{\frac{2I_{TOT}}{4\pi kT \cdot V_{th} \cdot B}} = 3.9, \tag{5.25}$$

where $v_{in\text{-}rms}$ is the input-referred rms noise and B is the -3dB bandwidth. It is not the best NEF presented in the literature but it is on the right track.

Moreover, our OTA is the only fully-differential amplifier among the ones summarized in Table 14.

	Gain	I_{TOT}	NEF	B	$v_{in\text{-}rms}$	Fully-Diff.
This work	60dB	33μA	3.9	2.5KHz	0.85μV	YES
[Harrison,03]	40dB	16μA	3.8	7.5KHz	2.1μV	NO
[Wu,06]	40.2dB	0.3 μA	3.8	245Hz	0.94 μV	NO
[Wattanapanich,07]	40.8dB	2.7 μA	2.67	5.32KHz	3 μV	NO
[Holleman,07]	36.1dB	0.8 μA	1.8	4.7KHz	3.6 μV	NO

Table 14 Comparison between proposed low-power low-noise OTA and other amplifiers existing in the literature.

5.4.3 Integrated Switched Capacitor Low-Pass Filter

Although we use a BPDS converter, a simple first-order filter is required to cancel out the high frequency noise before digital conversion. The schematic of the implemented switched capacitor LPF is shown in Fig. 93. It can obtain very low cut-off frequencies without using huge resistors or external capacitances. Moreover, the cut-off frequency is proportional to the clock frequency by means of

$$f_{-3dB} = \frac{1}{2\pi R_{eq} C_1} = \frac{C_0}{2\pi\left(C_0 + C_1\right)} \frac{f_{CK}}{4}. \tag{5.26}$$

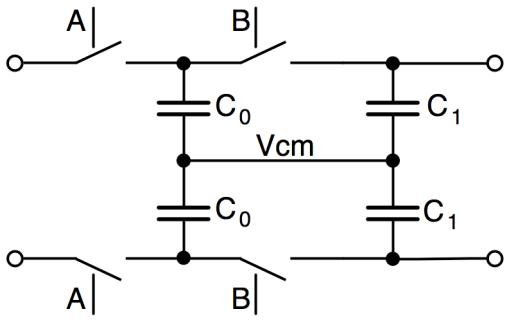

Fig. 93 Schematic of the implemented switched capacitor LPF filter inherently allowing frequency scalability. C_0 and C_1 set the cut-off frequency to $4f_0$. The switches are realized using complementary transistors with dummy elements.

In this way, the filter frequency scales with the clock and the BPDS operating frequency. Capacitors C_0 and C_1 have been chosen so as to set a cut-

off frequency four times the modulating frequency f_0. A and B are non-overlapping digital signals generated from the clock signal. Their frequency is ¼ of the clock frequency.

The switches are realized using complementary transistors with dummy elements so as to arrange a greater voltage swing, and minimize thr charge injection [Razavi,01].

The LPF increases the noise power due to a folding process because it is a switching system [Crescentini,10], [Liou,79]. However, the switching frequency is higher than the LNA bandwidth, if LNA gain greater than 10 are chosen. Thus, the undersampling-ratio of the noise is small, as well as the noise folding. Fig. 94 shows the effect of the LPF on the noise PSD, assuming the LNA gain equal to 10.

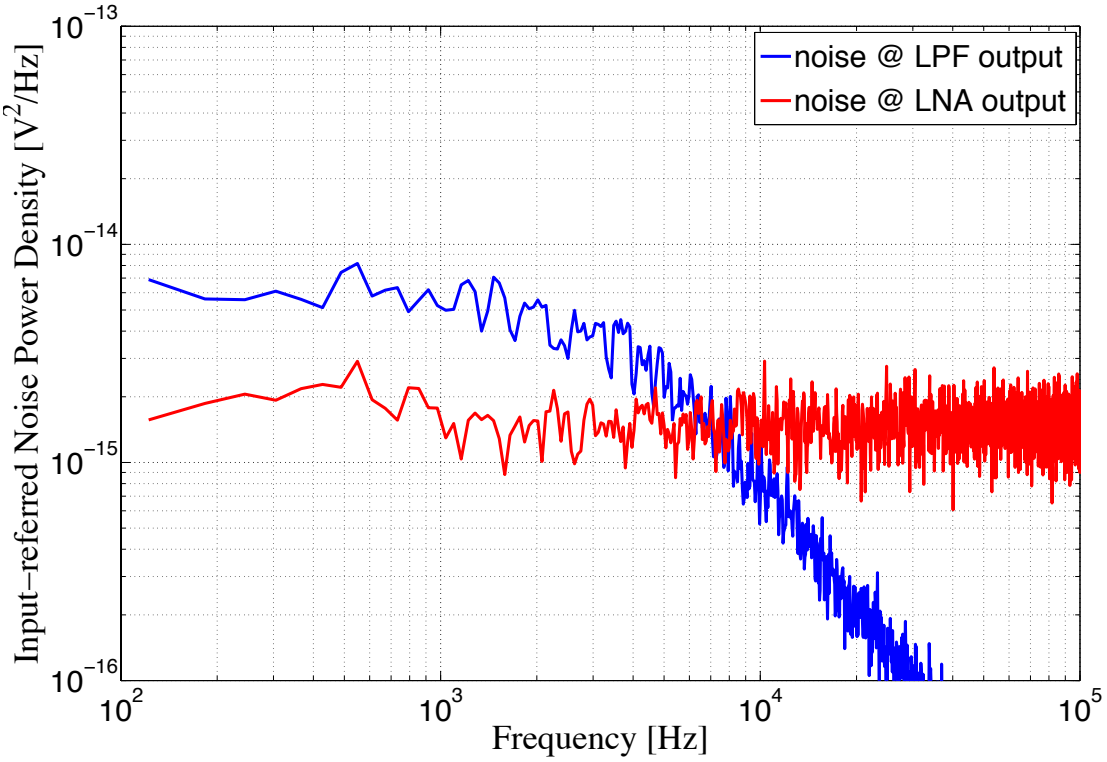

Fig. 94 Effect of the switched capacitor LPF on the noise PSD. The red line is the noise PSD at the LNA output. The blue line is the noise PSD after the switched capacitor filter. The filter cancels the high frequency noise and increases the low frequency noise of a factor of approximately 3.

5.5 IC Implementation

5.5.1 4-Core Approach

Obviously, a CTD system is composed of 3 different sensors; a conductivity sensor, a temperature sensor and a depth sensor. The proposed EIS system was arranged in a 4-core fashion so as to read each sensor concurrently, where the 4th core is connected to an adjustable voltage source for cleaning purposes. Fig. 95 shows the floorplan of the implemented IC. Each single core is placed in a corner physically separated from the other ones.

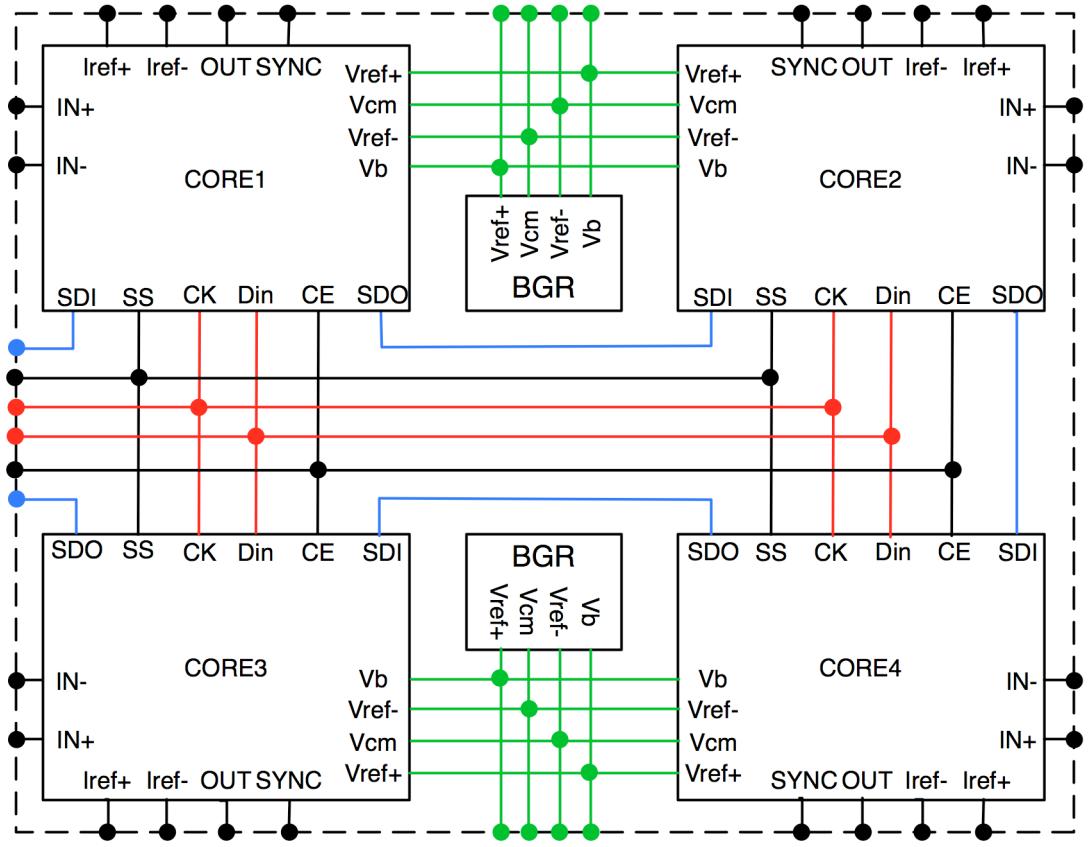

Fig. 95 4-core block scheme.

The system is programmable using an SPI interface. The SPI is composed of 4 shift registers, one for each core. The SPI allows the user to shut down and program the cores, independently. The digital signals, which drive the SPI interface, are placed in a centerline of the IC, dividing the chip in two symmetrical sections. In this way, we separate analog and digital circuits as much as possible. Moreover, to ban dangerous coupling effects between digital lines and analog reference signals, the band-gap reference (BGR) has been replicated two times. However, this causes a strong increase in total

current consumption since the BGR is the most power hungry element, with a current consumption of 300μA.

In Fig. 95, the BPDS outputs are arranged in a different way than explained in section 5.2.2, because there are synchronization issues between each core and the FPGA. The real and imaginary signals, coming out from each BPDS, are serialized into a single bit line. Then, each core provides a synchronization signal (SYNC), working as in Fig. 96. The FPGA samples the real output signal during SYNC rising edges, and the imaginary output signal during SYNC falling edges.

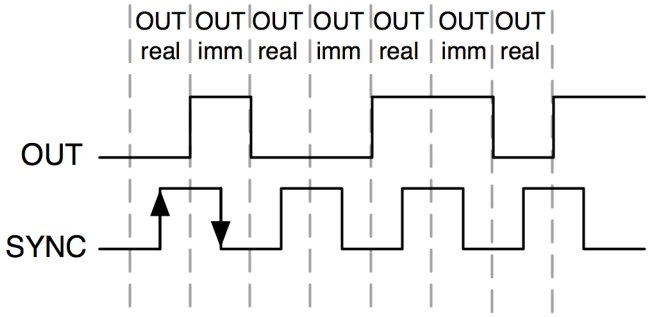

Fig. 96 Synchronization protocol between the EIS system and the FPGA. Both signals are provided by the EIS. FPGA samples output real data while SYNC rising edge and output imaginary data while SYNC falling edge.

The clock signal is provided externally by the FPGA. For the targeting 1KHz CTD application, the clock frequency must be 1MHz. However, varying the clock frequency it is possible to change the system working frequency and thus completely characterize the sensor impedance versus frequency. The system has been tested for working frequency up to 25KHz, which means a maximum clock frequency of 25MHz.

The layout of the final 4-core EIS system is depicted in Fig. 97. It is a 9mm^2 IC with total power consumption between 3mW and 6mW, depending on the used current reference sine wave. To boost-up the system lifetime, a power duty-cycling approach will be implemented at PCB level. Employing standard batteries and assuming a latency period of 6s between each measurement, the expected lifetime is around 1 year with 1mA as current reference.

The 4-core EIS chip will be mounted on a final PCB along with the sensors, the FPGA and a flash memory. The entire system will be employed in fish-tag applications for ocean monitoring; however, the proposed EIS system is

general and could be employed with different sensors and in different application fields.

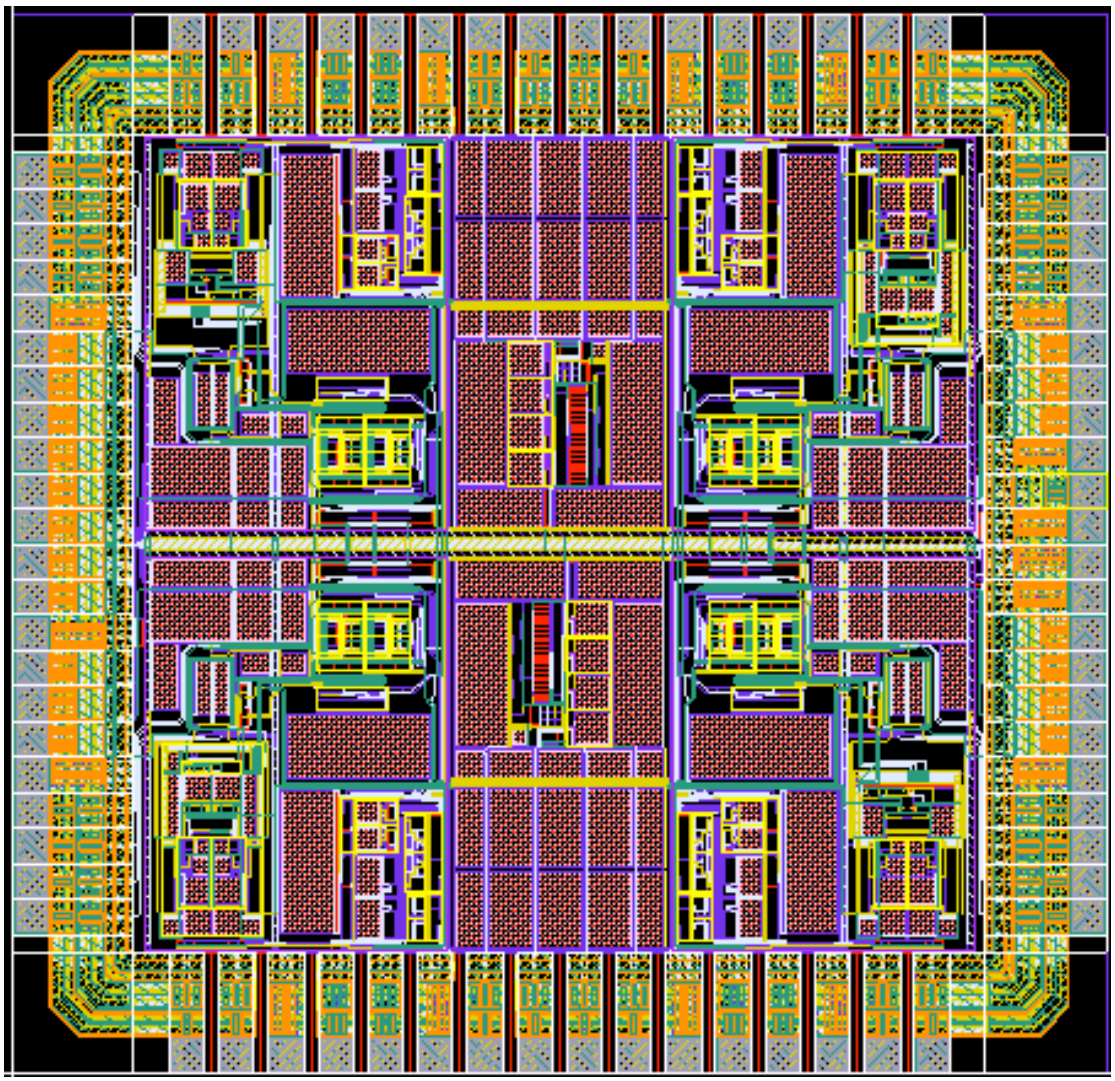

Fig. 97 Final layout of proposed 4-core IC.

5.5.2 Preliminary Results

The first prototype of the EIS system described in this chapter had a layout error. There was a short-circuit between two reference signals preventing any functionality. To fix the error we tried with a post-processing focused ion-beam (FIB) attack. However, the error was very narrow, it was just a via connection as large as few micrometers. The FIB process dug a small hole but with an undesired metal replacement as shown in Fig. 98, avoiding the usability of the system. Thus, we solved the error in the layout and re-submitted the project to the foundry. The IC is currently in fabrication;

therefore we have not measurement results, at this time. The following are simulation results.

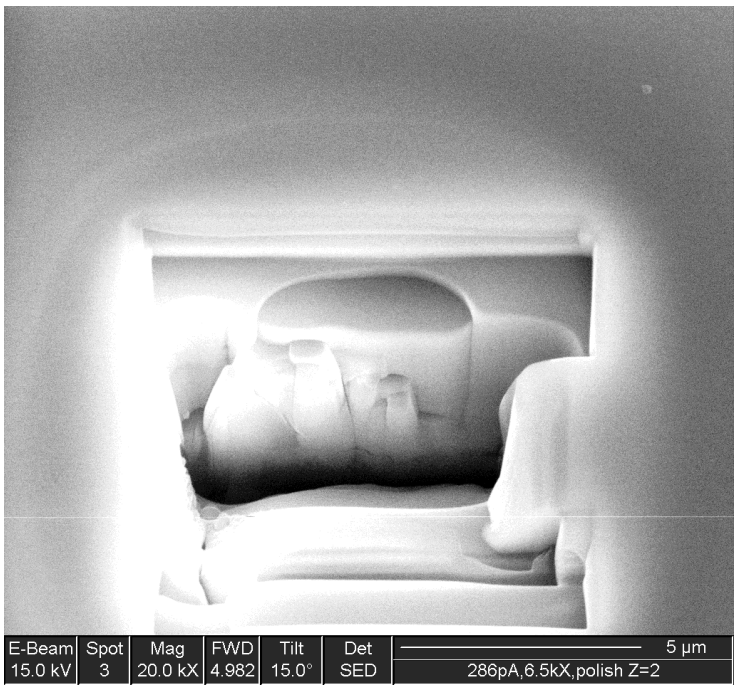

Fig. 98 Microscope picture of short-circuit error after FIB attach. The FIB was able to dug so small hole but an undesired metal replacement made the operation useless.

Fig. 99 shows the result of an impedance acquisition test, verifying the system functionality. The simulation employs 10μA sine wave as current reference, a simple 500Ω resistor modeling the sensor, and LNA gain set to 10. The decimated output has an initial transient time of approximately 400ms, which is OSR dependent and could be easily changed. For instance, with OSR=200 the system takes less than 200ms to settle. The final result converges to amplitude of 470.6Ω and phase of approximately -23.7 degrees. The error on the absolute value is related to non-idealities and parasitic elements, affecting the LNA gain, while phase shift is related to the system delay. Both errors are expected and can be nulled by calibration through system characterization process. The simulation was done on layout-extracted netlist without thermal noise; therefore, the noise shown in the magnifications of Fig. 99 is only quantization noise, attesting a resolution as high as desired. Fig. 100 shows the result of the same simulation in the complex plane. Dividing the quantization noise power by the square of the LNA gain, we obtain the input-referred quantization noise approximately equal to $2pV^2$, well below the design constraints.

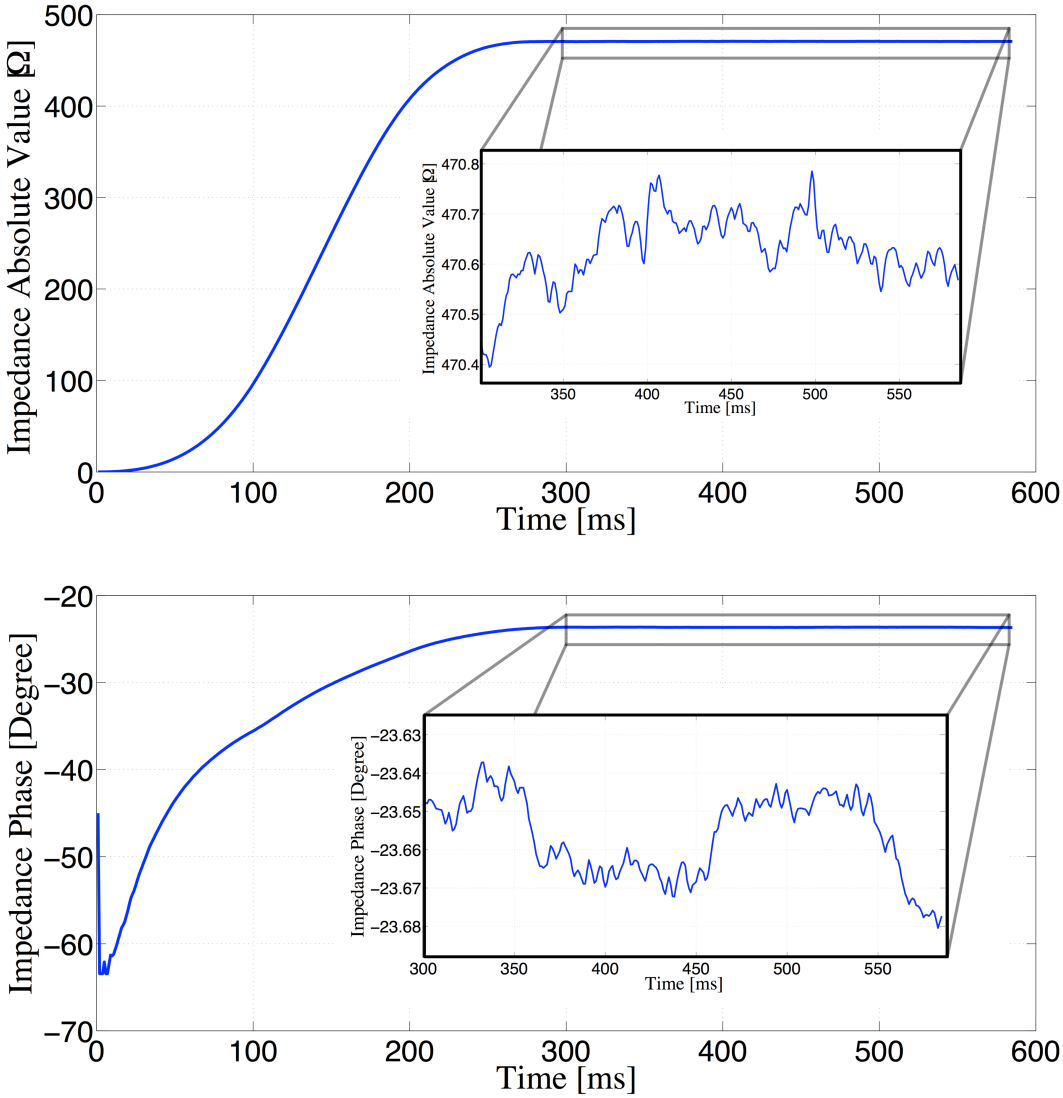

Fig. 99 Decimated output of a 600ms simulation. The top picture shows the absolute value of the input impedance, while the bottom picture shows the phase. We used 10μA sine wave as reference current signal, a simple 500Ω resistor modeled the sensor, and the LNA gain was set to 10. The simulation was done on layout-extracted netlist taking into account of all parasitic effects. However, for simulation time constraints, the thermal noise was neglected. The system takes 400ms to settle to the final value and shows input-referred quantization noise error of 2pV^2. The system converges to an absolute value of 470Ω and a phase of -23 degrees. The gain error is related to parasites and nonidealities, while the phase shift accounts for the system delay. Both were expected and can be adjusted in digital.

Fig. 101 shows the result of another simulation, where the input impedance was changed so as to induce phase shifts of 45 degrees. The simulation demonstrates the ability of the EIS system to track the sensor phase with the required precision.

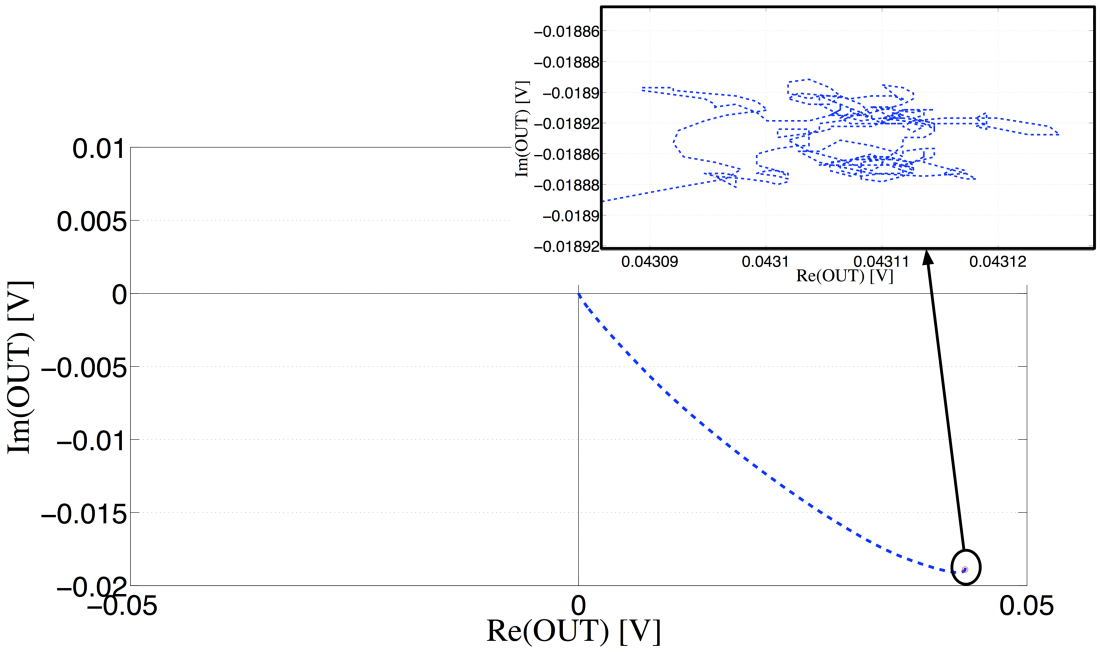

Fig. 100 Representation of the output signal in the complex plane. The magnification picture shows a quantization error of 80μVpp on the imaginary line and 30μVpp on the real line, leading to approximately 15.5bit of resolution.

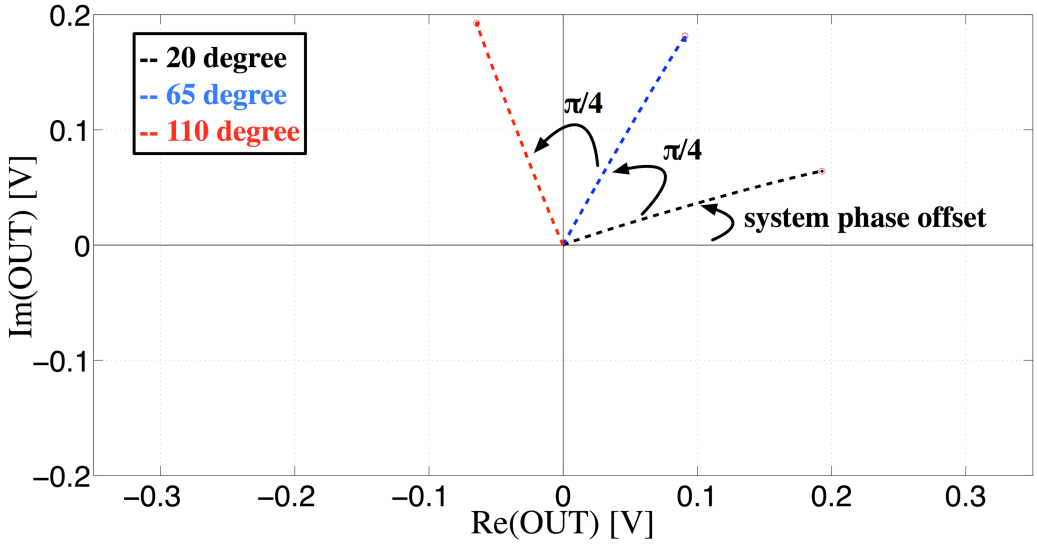

Fig. 101 Impedance plan plot showing the ability of the system to track phase shift of the sensor. The blue line is the output of the EIS system using an input impedance that induce a phase shift of 45 degrees and the red line is the output with a further 45 degrees shift.

The noise budget design has been verified using transient time noise simulations of the whole architecture by means of Spectre® simulator [Crescentini,10]. Fig. 102 shows the noise PSD referring to the sensor input node and considering only the current generator as the noise source. The simulation was done choosing 1mA as output current and setting $D_{IN}=1$, thus only one half-circuit is active. Since the system works in switched mode with

alternating active branches, the total noise PSD can be estimated doubling the one shown in Fig. 102. The total noise power in 10Hz bandwidth around 1KHz is very low, allowing SNR higher than 100dB.

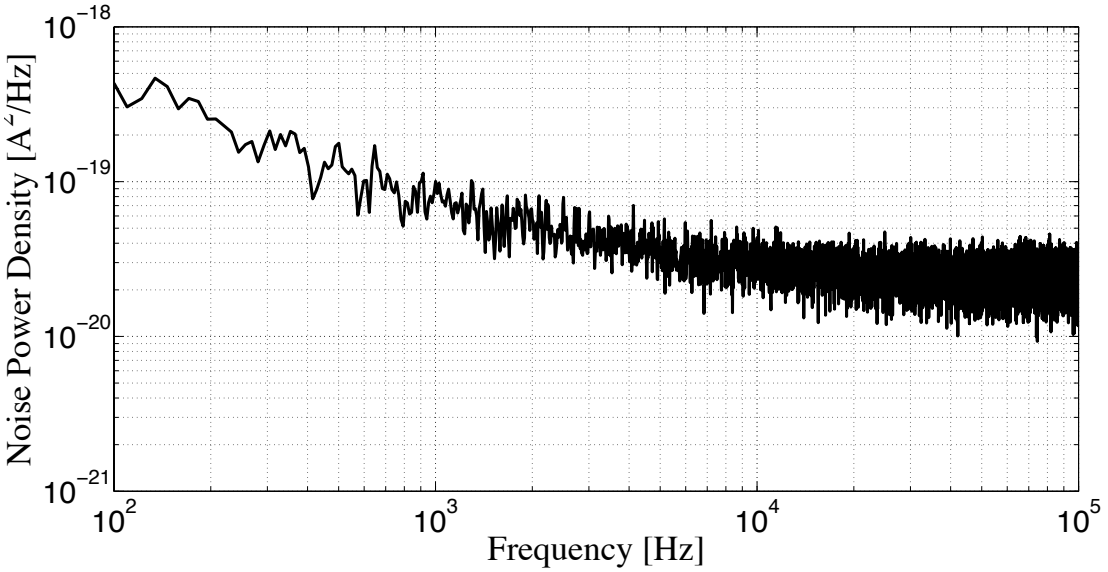

Fig. 102 Noise PSD referring at the input node. This simulation estimates only the noise due to the current generator. The simulation was done choosing 1mA as output current and setting $D_{IN}=1$, thus only one half-circuit is active. Since the system works in switched mode with alternating active branches, the total noise PSD can be estimated doubling the one shown in the picture.

Fig. 103 shows the input-referred PSD of the noise generated by the acquisition chain. The simulation takes into account thermal and flicker noise, kTC noise, charge injection, as well as folding effects due to switched capacitor filter and BPDS converter. The folding effect increases the white noise and thus shifts the flicker corner frequency at lower values. However, we are mainly interested about noise around 1KHz, far away from the corner frequency. The simulation reports an input-referred noise PSD as low as $5fV^2/Hz$, implying a total noise power of $50fV^2$ in 10Hz bandwidth. The result is slightly bigger than estimated and exceeds the requirements described in section 5.1.4. However, the random noise was targeted for a 16-bit resolution with confidence error of 0.02%, thus this marginally performance deterioration is not critical.

Another important system parameter is the achieved linearity. Fig. 104 shows the input-referred non-linearity error for different DM input voltages. The simulation has been realized also taking account of a stray CM sine wave as high as 1V. The maximum non-linearity error of the acquisition system is around 20μV, below the quantization error.

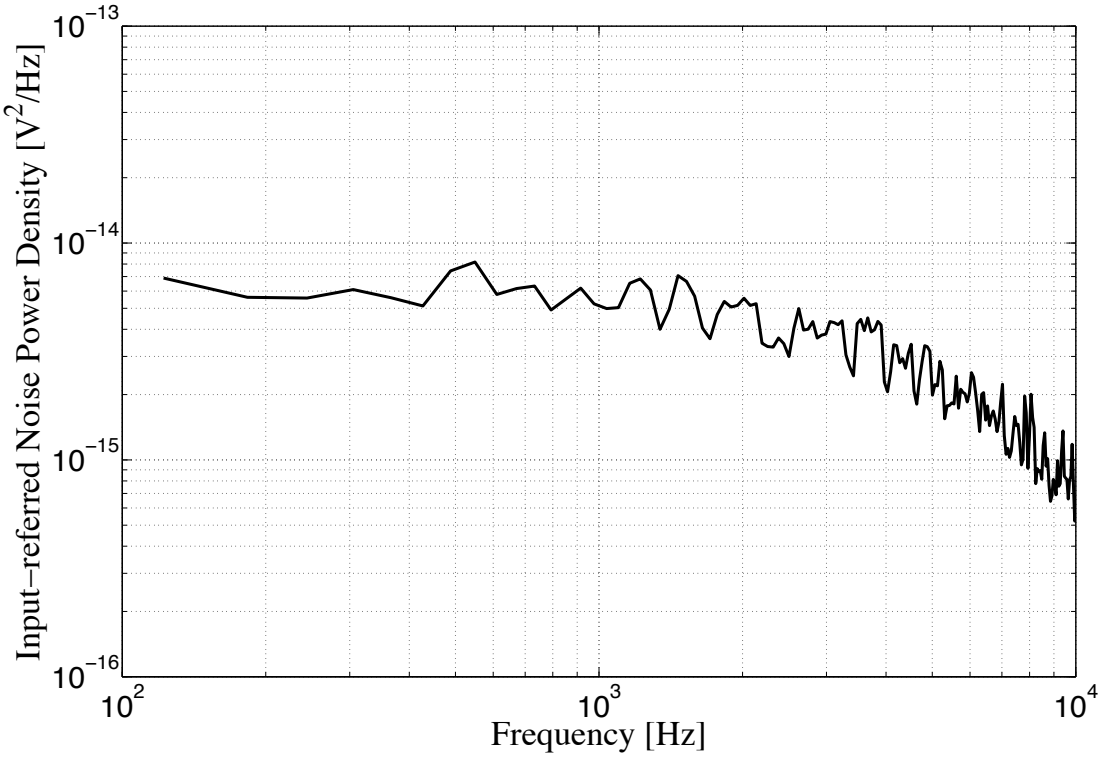

Fig. 103 Input-referred PSD of the noise generated by the acquisition chain.

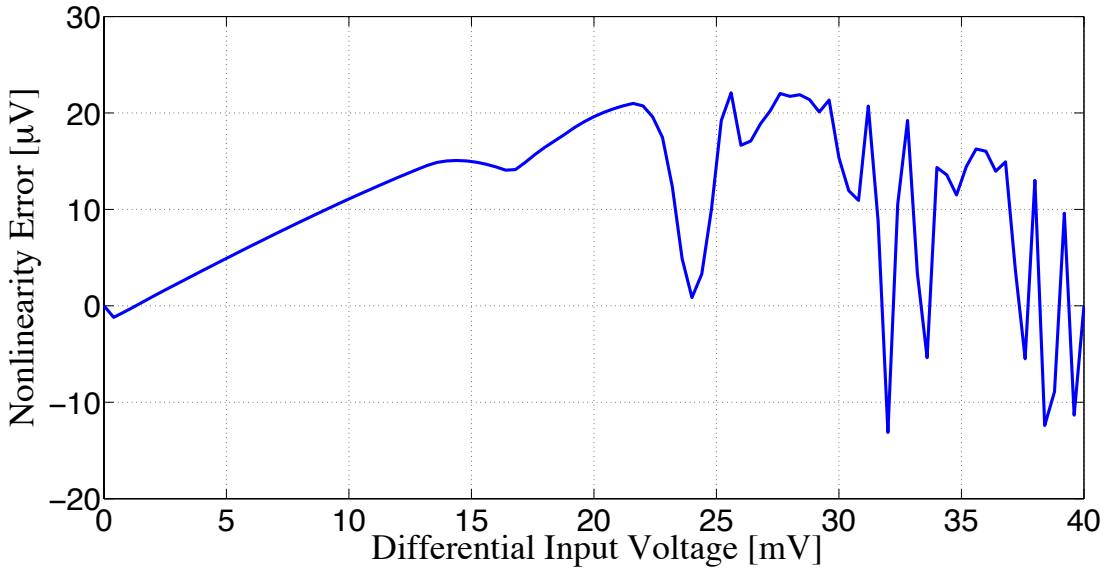

Fig. 104 Simulation of the non-linearity error for the acquisition path. The simulation takes into account the LNA, the switched capacitor LPF, the reset and the BPDS. The simulation shows a maximum nonlinear error of approximately 20μV, below the simulated quantization noise shown in Fig. 100.

Chapter 6

Conclusions and Future Perspectives

6.1 Conclusions

This thesis has exposed the problem of designing advanced electronic interfaces intended for parallel acquisition from bio-nanosensors. The focus was the study and the design of low-noise interfaces, specifically current-sensing interfaces that are very used with promising electrochemical bio-nanosensors, like ion-channels and nanowires. A comprehensive analysis of the noise in current-sensing interfaces has been illustrated, leading to a noise model for both CT current-sensing interfaces and DT current-sensing interfaces. A novel noise-reduction technique for DT current-sensing interfaces has been presented, and ad-hoc IC based on this technique has been designed. This IC is mainly intended for ultra low-noise DC-transient measurements (i.e. amperometry) of single ion channels, and promises an input-referred noise PSD comparable with state-of-the-art instruments (10fArms at 500Hz, 22fArms at 1KHz and 83fArms at 5KHz). The CMOS chip also implements additional features suitable for parallel electrophysiological measurements of ion channels, like correction of electrode offset or internal generation of the stimulus signal.

Meanwhile, another integrated CMOS interface for bio-nanosensors has been developed and presented in this manuscript. This latter IC implements an EIS system intended for CTD applications in the environmental field; however, it can be also used with bio-nanosensors like nanowires. It is a low-noise system enabling AC measurements and integrating both signal generation and signal acquisition.

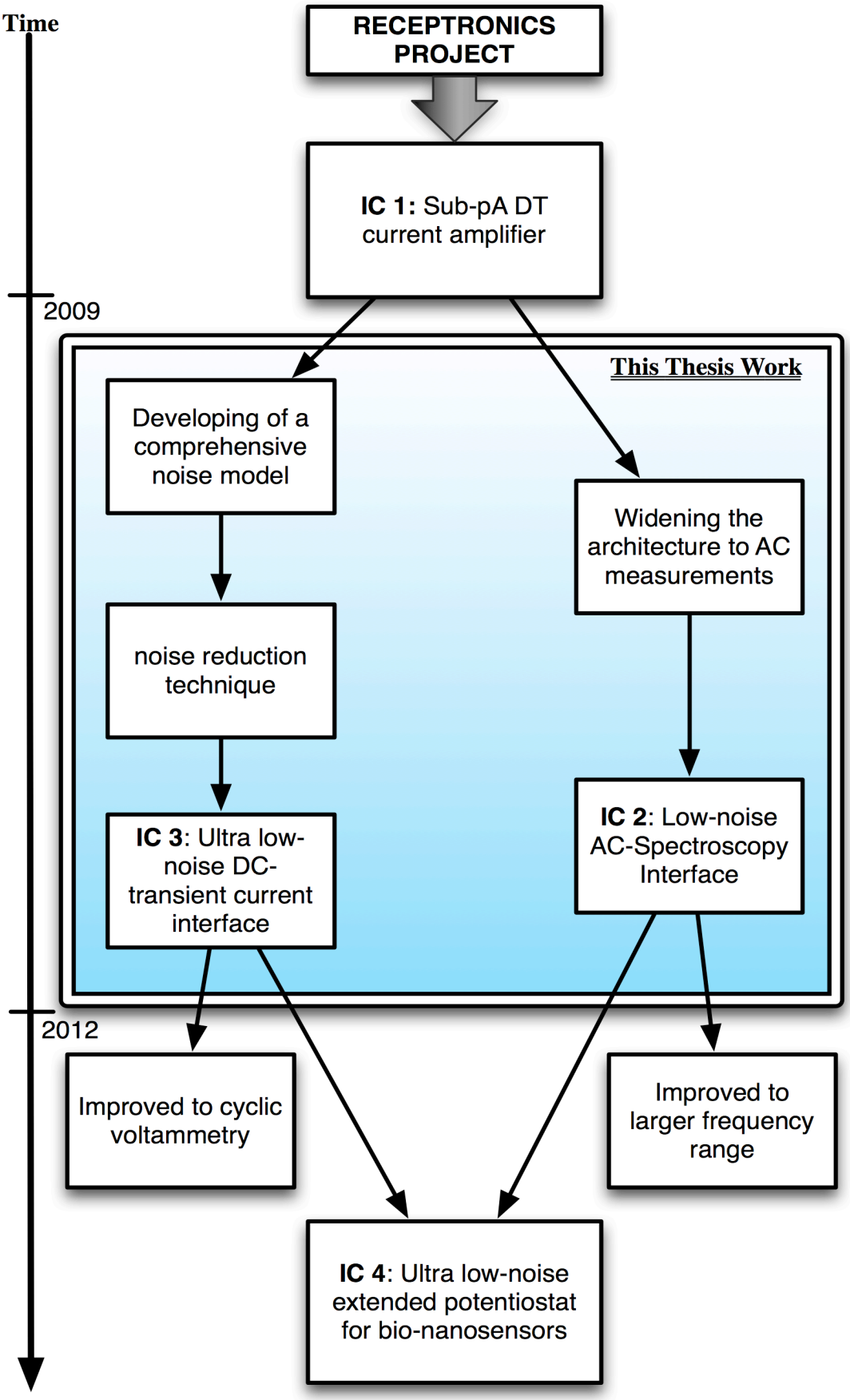

Fig. 105 Flowchart of the research activity discussed in this manuscript, highlighting the future steps.

The IC allows impedance acquisitions from hundreds of Hz to 25KHz with 15bit accuracy. Both ICs are now under fabrication and will be laboratory characterized in next months.

6.2 Future Perspectives

This thesis work is part of a bigger research activity started in 2005 with the "*Receptronics"* project founded by the European commission, and will continue in the future for at least a couple of years. Indeed, every year we discover new perspectives, applications and features to further improve our global system.

In the near future, the ICs have to be tested and characterized; moreover, we already know some interesting improvements for both: the DC-transient current-sensing interface (described in chapter 4) has to be improved so as to enable cyclic voltammetry measurements; the AC interface (described in chapter 5) has to be improved so as to acquire signals in a larger frequency range.

Finally, both ICs will be combined so as to meet the ultimate target of the current research activity: the development of an ultra low-noise fully-integrated CMOS extended-potentiostat. This interface, together with the hybrid-technology presented in [Thei,10], could become the core instruments for bio-nanosensors applications as well as for high-throughput electrochemical applications.

Appendix A

Mathematical Derivation of DT Current-Sensing Noise Model

Introduction

This appendix presents more details about mathematical derivation of the noise model used in DT current-sensing interfaces.

Notation

To be more general, some notations used in this appendix will be different with respect to the one used in chapter two. Figure 1 defines the variables here used.

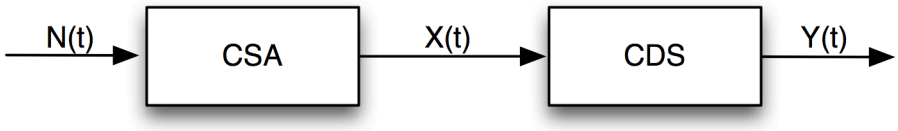

Fig. 106 Figure 1 Block scheme of a general DT current-sensing interface employing CDS.

Hereafter a variable in capitol letters will refer to random process, and the same variable in lower letters will refer to a realization of the same random process. The power spectrum density of a signal X is referred as $G_X(f)$.

Derivation of Equation (2.24)

Let's start assuming a lowpass-filtered thermal noise $N(t)$ at CSA input (Fig. 107). It is a continuous time (CT) wide-sense stationary (wss) ergodic random process (r.p.). Due to the periodical reset, the noise at CSA output is an amplified and filtered version of $N(t)$. This noise is represented by the r.p. $X(t)$ given by:

$$X(t) = N(t)\sum_n p(t - nT), \tag{b.1}$$

and it is a cycle-ergodic r.p. with period T as shown in Fig. 108 a). The window function $p(t)$ is simply a rect function equal to 1 for $-\vartheta \leq t \leq 0$ and zero for all others values of t. It is depicted in Fig. 108 f).

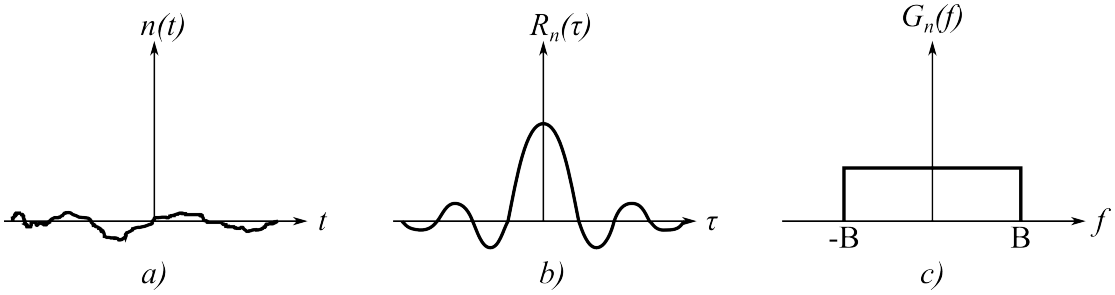

Fig. 107 Representation of low-pass filtered thermal noise $N(t)$ showing a) a single realization, b) its autocorrelation function and c) its power spectrum density.

Correlated double sampling (CDS) takes the first noise sample at the beginning of each integration period (i.e. with period T equal to the sampling period) and thus can be described by the discrete-time ergodic r.p. C_n (Fig. 108 d)):

$$C_n = X\left(nT - \theta\right) = \int_{-\infty}^{\infty} x\left(t - \theta\right) \cdot \delta\left(t - nT\right) dt. \tag{b.2}$$

One capacitor stores and holds this noise sample for all the integration period ϑ, generating a pulse amplitude modulated (PAM) signal $X_n(t)$ described by:

$$\begin{aligned} X_n\left(t\right) &= \sum_n C_n \cdot p\left(t - nT\right) \\ X_n\left(t\right) &= \sum_n X\left(nT - \theta\right) \cdot p\left(t - nT\right). \end{aligned} \tag{b.3}$$

Also $X_n(t)$ is cicle-ergodic r.p. (Fig. 108 b)). Then CDS makes the difference between the input signal and the PAM signal $X_n(t)$, so as the output $Y(t)$ is constructed as (Fig. 108 c)):

$$\begin{aligned} Y\left(t\right) &= X\left(t\right) - X_n\left(t\right) \\ Y\left(t\right) &= X\left(t\right) - \sum_n X\left(nT - \theta\right) \cdot p\left(t - nT\right). \end{aligned} \tag{b.4}$$

Subsequently, the S&H samples the output signal $Y(t)$ at then end of the integration period. However, this appendix focuses on CDS noise effects, thus the last sampling function will be neglected hereafter.

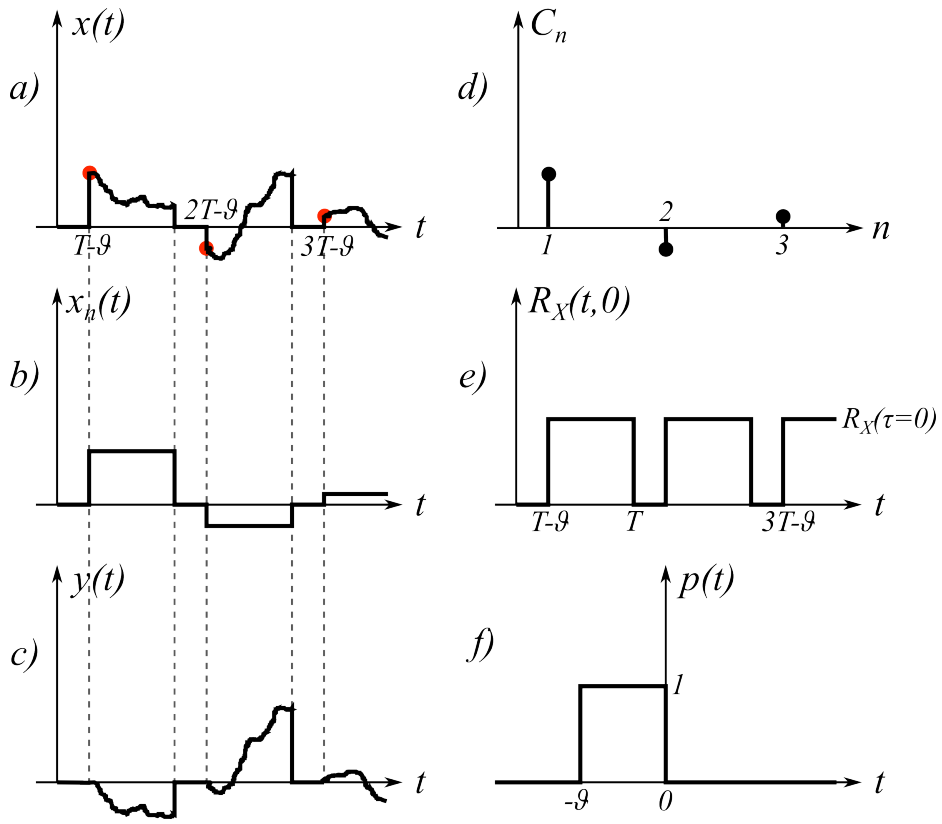

Fig. 108 Examples of realization for each r.p. involved in the mathematical derivation: a) r.p. $X(t)$ at CSA output; b) r.p. $X_n(t)$ representing the first noise sampling done by CDS; c) CDS output $Y(t)$; d) discrete time r.p. C_n. e) Autocorrelation function of the r.p. $X(t)$ with shifting parameter τ set to 0. f) Windowing function $p(t)$.

To understand the CDS effects on the noise it is mandatory to compute the PSD of $Y(t)$ as a function of the PSD of $X(t)$. Since noise signals are power-limited signals, their PSD should be computed by means of correlation functions [Gardner, 90].

$$\begin{aligned} G_Y(f) &= F\left\{\left\langle R_Y(t,\tau)\right\rangle_T\right\} = F\left\{\left\langle \mathrm{E}\left[Y(t)Y(t-\tau)\right]\right\rangle_T\right\} = \\ &= F\left\{\left\langle \mathrm{E}\left[X(t)X(t-\tau)\right] + \mathrm{E}\left[X_n(t)X_n(t-\tau)\right] - 2\mathrm{E}\left[Xn(t)X(t-\tau)\right]\right\rangle_T\right\} = \\ &= F\left\{\left\langle R_X(t,\tau)\right\rangle_T\right\} + F\left\{\left\langle R_{X_n}(t,\tau)\right\rangle_T\right\} - 2\Re e\left\{F\left\{\left\langle R_{X,X_n}(t,\tau)\right\rangle_T\right\}\right\} = \\ &= G_x(f) + G_{x_n}(f) - 2\Re e\left\{F\left\{\left\langle R_{X,X_n}(t,\tau)\right\rangle_T\right\}\right\} \end{aligned} \tag{b.5}$$

Assuming known the PSD of $X(t)$ (i.e. $G_X(f)$), the above equation splits the problem of computing $G_Y(f)$ into two minor quests: compute the autocorrelation of $X_n(t)$ and compute the cross-correlation between $X_n(t)$ and $X(t)$. Let starts with the computation of $G_{Xn}(f)$. Since $X_n(t)$ is a cycle-ergodic r.p. its own PSD can be expressed as:

$$G_{x_n}(f) = F\left\{\left\langle R_{X_n}(t,\tau)\right\rangle_T\right\}; \tag{b.6}$$

where the PSD is given by the Fourier transformation of the time average of the autocorrelation function over a single period.

$$\begin{aligned} R_{X_n}(t,\tau) &= \mathrm{E}\left[X_n(t)X_n(t-\tau)\right] = \\ &= \mathrm{E}\left[\sum_n C_n p(t-nT)\sum_m C_m p(t-mT-\tau)\right] = \\ &= \mathrm{E}\left[\sum_n C_n p(t-nT)\sum_k C_{n-k} p(t-(n-k)T-\tau)\right] = \\ &= \sum_n\sum_k \underbrace{\mathrm{E}\left[C_n C_{n-k}\right]}_{R_C(k)} p(t-nT)p(t-(n-k)T-\tau) = \\ &= \sum_k R_C(k)\underbrace{\sum_n p(t-nT)p(t-(n-k)T-\tau)}_{\text{periodic function of period T}} \end{aligned} \tag{b.7}$$

$$\begin{aligned} \left\langle R_{X_n}(t,\tau)\right\rangle_T &= \mathrm{E}\left[X_n(t)X_n(t-\tau)\right] = \\ &= \left\langle \sum_k R_C(k)\sum_n p(t-nT)p(t-(n-k)T-\tau)\right\rangle_T = \\ &= \frac{1}{T}\sum_k R_C(k)\underbrace{\int_T\sum_n p(t-nT)p(t-(n-k)T-\tau)dt}_{R_p(\tau-kT)} = \\ &= \frac{1}{T}\sum_k R_C(k)\cdot R_p(\tau-kT) = \\ &= \frac{1}{T}R_C(k) * R_p(\tau) \end{aligned} \tag{b.8}$$

Since $R_C(k)$ is the autocorrelation function of the sequence C_n, it is a discrete time function and thus $\langle R_{Xn}(t,\tau)\rangle$ is the convolution between a discrete time function and a continuous time function.

$$\begin{aligned} G_{x_n}(f) &= F\left\{\left\langle R_{X_n}(t,\tau)\right\rangle_T\right\} = \\ &= F\left\{\frac{1}{T}R_C(k) * R_p(\tau)\right\} = \\ &= \frac{1}{T}F\left\{R_C(k)\right\}\cdot\left|P(f)\right|^2. \end{aligned} \tag{b.9}$$

The computation of $|P(f)|^2$ is straightforward:

$$\left|P(f)\right|^2 = \theta^2\mathrm{sinc}^2(f\theta); \tag{b.10}$$

so the problem is shifted to the computation of $R_C(k)$.

In order to evaluate $R_C(k)$ let's define a new r.p. $X_C(t)$ as follow:

$$X_C(t) = \sum_n X(nT-\theta)\delta(t-nT) = X(t-\theta)\sum_n \delta(t-nT). \tag{b.11}$$

This is an ergodic r.p. given by the convolution between the r.p. C_n and the summation of Dirac's delta. The autocorrelation of $X_C(t)$ is:

$$\begin{aligned} R_{X_c}(\tau) &= \mathrm{E}\left[X_C(t)X_C(t-\tau)\right] = \\ &= \mathrm{E}\left[X(t-\theta)\sum_n \delta(t-nT)\cdot X(t-\theta-\tau)\sum_m \delta(t-mT)\right] = \\ &= \underbrace{\mathrm{E}\left[X(t-\theta)X(t-\theta-\tau)\right]}_{R_X(t,\tau)}\cdot \sum_n \delta(t-nT)\sum_m \delta(t-mT). \end{aligned} \tag{b.12}$$

Using the Poisson summation rule:

$$\begin{aligned} R_{X_c}(\tau) &= R_X(t,\tau)\cdot\frac{1}{T}\sum_n e^{j2\pi\frac{n}{T}t}\cdot\frac{1}{T}\sum_m e^{j2\pi\frac{m}{T}t} = \\ &= R_X(t,\tau)\cdot\frac{1}{T^2}\sum_n\sum_m e^{j2\pi\frac{n+m}{T}t} = R_X(t,\tau)\cdot\frac{1}{T^2}\sum_k e^{j2\pi\frac{k}{T}t} = \\ &= R_X(t,\tau)\cdot\frac{1}{T}\sum_k \delta(t-kT). \end{aligned} \tag{b.13}$$

Equation (b.13) means that the discrete-time signal resulting from a sampling process has an autocorrelation function that is the sampling of the autocorrelation funtion of the original continuous-time signal [Gardner,90], [Proakis,00]. Therefore, the autocorrelation of $X_C(t)$ is the sampling of $R_X(t,\tau)$ by steps T. Following the same idea, since C_n is the succession obtained sampling $X(t)$, then $R_C(k)$ is the sampling of $R_X(t,\tau)$. Therefore (b.9) can be written as:

$$\begin{aligned} G_{x_n}(f) &= \frac{1}{T}F\left\{R_C(k)\right\}\cdot\left|P(f)\right|^2 = \\ &\cong \frac{\left|P(f)\right|^2}{T^2}\sum_k G_x\left(f+\frac{k}{T}\right) = \\ &= \frac{\theta^2}{T^2}\mathrm{sinc}^2(f\theta)\cdot\sum_k G_x\left(f+\frac{k}{T}\right) = \\ &= d^2\mathrm{sinc}^2(f\theta)\cdot\sum_k G_x\left(f+\frac{k}{T}\right). \end{aligned} \tag{b.14}$$

The cross-correlation between $X_n(t)$ and $X(t)$ encloses all the information about the difference operation, since it is strictly related with the correlation between two delayed samples. In order to simplify the math procedure the following formalism should be taken:

$$R_{X_n,X}(t,\tau) = R_{X_n,X}(t_1,t_2) \tag{b.15}$$

where the cross-correlation is the ensemble average between $X_n(t)$ evaluated at $t=t_1$ and $X(t)$ evaluated at $t=t_2$.

$$\begin{aligned} R_{X_n,X}(t_1,t_2) &= \mathrm{E}\left[X_n(t_1)X(t_2)\right] = \\ &= \mathrm{E}\left[\sum_n X(nT-\theta)p(t_1-nT)X(t_2)\right] = \\ &= \sum_n p(t_1-nT)\mathrm{E}\left[X(nT-\theta)X(t_2)\right] \end{aligned} \tag{b.16}$$

Assuming t_1 existing only in the interval $[nT\text{-}\theta, nT]$, thus:

$$p(t_1-nT) = \begin{cases} 1 & n=\bar{n} \\ 0 & n\neq\bar{n} \end{cases}, \tag{b.17}$$

where

$$\bar{n} = \left\lfloor \frac{t_1}{T^+} + 1 \right\rfloor \rightarrow \text{per } t_1 \in [0,T] \Rightarrow \bar{n} = 1. \tag{b.18}$$

Using (b.17) and (b.18) into (b.16) we can write:

$$\begin{aligned} R_{X_n,X}(t_1,t_2) &= \mathrm{E}\left[X(\bar{n}T-\theta)X(t_2)\right] = \\ &= \mathrm{E}\left[X(\bar{n}T-\theta)X(t_1-\tau)\right]. \end{aligned} \tag{b.19}$$

Introducing the time ε

$$\varepsilon = \bar{n}T - t_1 \quad \varepsilon \in [0,\theta), \tag{b.20}$$

the cross-correlation becomes:

$$R_{X_n,X}(t_1,t_2) = \mathrm{E}\left[X(\bar{n}T-\theta)X(\bar{n}T-\varepsilon-\tau)\right]. \tag{b.21}$$

Defining other two dummy variables:

$$\begin{aligned} \mathrm{t}_0 &= \bar{n}T - \theta \\ \xi &= \mathrm{t}_0 - \bar{n}T + \varepsilon + \tau = \tau + \varepsilon - \theta, \end{aligned} \tag{b.22}$$

the cross-correlation can be rewritten as

$$\begin{aligned} R_{X_n,X}(t_1,t_2) &= \mathrm{E}\left[X(t_0)X(t_0-\xi)\right] = R_X(t_0,\xi) = \\ &= R_X\left(\bar{n}T - \theta, \tau + \varepsilon - \theta\right). \end{aligned} \tag{b.23}$$

Since the autocorrelation function R_X is periodic of period T the last equation can be rewritten as:

$$R_{X_n,X}(t_1,t_2) = R_X\left(-\theta, \tau + \varepsilon - \theta\right). \tag{b.24}$$

The time-average of (b.24) over a period is:

$$\begin{aligned} \left\langle R_{X_n,X}(t_1,t_2)\right\rangle_T &= \frac{1}{T}\int_T R_X\left(-\theta, \tau + \left\lfloor\frac{t_1}{T}\right\rfloor T - t_1 + T - \theta\right)dt_1 = \\ \text{for } t_1 \in [0,T] &\Rightarrow \left\lfloor\frac{t_1}{T}\right\rfloor = 0 \forall t_1 \\ &= \frac{1}{T}\int_T R_X\left(-\theta, \tau - t + T - \theta\right)dt = \\ &= \frac{1}{T}\int_0^T R_X\left(-\theta, \tau - t + T - \theta\right)dt. \end{aligned} \tag{b.25}$$

Defining the integral function as:

$$\begin{aligned} R'_X\left(-\theta, \tau - t + T - \theta\right) &= \int R_X\left(-\theta, \tau - t + T - \theta\right)d\tau = \\ &= -\int R_X\left(-\theta, \tau - t + T - \theta\right)dt, \end{aligned} \tag{b.26}$$

the time-average could be expressed as:

$$\left\langle R_{X_n,X}(t_1,t_2)\right\rangle_T = \frac{1}{T}\left[R'_X\left(-\theta, \tau + T - \theta\right) - R'_X\left(-\theta, \tau - \theta\right)\right]. \tag{b.27}$$

Now, the PSD of the cross-correlation function is given by the Fourier transformation of (b.27):

$$
\begin{aligned}
F\left\{\left\langle R_{X_n,X}\left(t_1,t_2\right)\right\rangle_T\right\} &= \frac{1}{T}\left[F\left\{R'_X\left(-\theta,\tau+T-\theta\right)\right\}-F\left\{R'_X\left(-\theta,\tau-\theta\right)\right\}\right]= \\
&= \frac{1}{T}\left[F\left\{\int R_X\left(-\theta,\tau+T-\theta\right)d\tau\right\}-F\left\{\int R_X\left(-\theta,\tau-\theta\right)d\tau\right\}\right]= \\
&= \frac{1}{T}\left[F\left\{\int_0^{\xi} R_X\left(-\theta,\tau+T-\theta\right)d\tau\right\}-F\left\{\int_0^{\xi} R_X\left(-\theta,\tau-\theta\right)d\tau\right\}\right]= \\
&= \frac{1}{T}\left[\frac{F\left\{R_X\left(-\theta,\tau+T-\theta\right)\right\}}{j2\pi f}-\frac{F\left\{R_X\left(-\theta,\tau-\theta\right)\right\}}{j2\pi f}+A\delta\left(f\right)\right],
\end{aligned}
\tag{b.28}
$$

where the A factor in the last equation is constant that takes into care the bounding conditions and describes the behavior of the PSD at zero frequency. For the sake of simplicity this last contribution will be neglected and (b.28) can be arranged as follow:

$$
\begin{aligned}
F\left\{\left\langle R_{X_n,X}\left(t_1,t_2\right)\right\rangle_T\right\} &\cong d\left[\frac{G_X\left(f\right)e^{j2\pi f\left(T-\theta\right)}-G_X\left(f\right)e^{-j2\pi f\theta}}{j2\pi fT}\right]= \\
&= dG_X\left(f\right)\left[\frac{\cos\left[2\pi f\left(T-\theta\right)\right]-\cos\left(2\pi f\theta\right)+j\sin\left[2\pi f\left(T-\theta\right)\right]+j\sin\left(2\pi f\theta\right)}{j2\pi fT}\right]
\end{aligned}
\tag{b.29}
$$

As stated in (b.5) we are interested only in the real part of (b.29), which is:

$$
2\Re e\left\{F\left\{\left\langle R_{X_n,X}\left(t_1,t_2\right)\right\rangle_T\right\}\right\} = 2dG_X\left(f\right)\frac{\sin\left(2\pi f\theta\right)+\sin\left[2\pi f\left(T-\theta\right)\right]}{2\pi fT}. \tag{b.30}
$$

Finally, using both (b.14) and (b.30) in (b.5), we get:

$$
\begin{aligned}
&G_Y\left(f\right)=G_x\left(f\right)+G_{x_n}\left(f\right)-2\Re e\left\{F\left\{\left\langle R_{X,X_n}\left(t,\tau\right)\right\rangle_T\right\}\right\}= \\
&\cong G_X\left(f\right)+d^2\mathrm{sinc}^2\left(f\theta\right)\sum_k G_X\left(f+\frac{k}{T}\right)-2dG_X\left(f\right)\frac{\sin\left(2\pi f\theta\right)+\sin\left[2\pi f\left(T-\theta\right)\right]}{2\pi fT}= \\
&= \underbrace{G_X\left(f\right)\left\{1+d^2\mathrm{sinc}^2\left(f\theta\right)-2d\frac{\sin\left(2\pi f\theta\right)+\sin\left[2\pi f\left(T-\theta\right)\right]}{2\pi fT}\right\}}_{\text{Differentiated baseband component}}+\underbrace{d^2\mathrm{sinc}^2\left(f\theta\right)\sum_{k\neq 0} G_X\left(f+\frac{k}{T}\right)}_{\text{Folding component}} \\
&\cong G_X\left(f\right)\left[1+d^2\mathrm{sinc}^2\left(f\theta\right)-2d\mathrm{sinc}\left(2f\theta\right)\right]+d^2\mathrm{sinc}^2\left(f\theta\right)\sum_{k\neq 0} G_X\left(f+\frac{k}{T}\right).
\end{aligned}
\tag{b.31}
$$

The last equation in (b.31) is exactly equation (2.24) used in chapter two. It shows the PSD at CDS output as a combination of two components, a

differentiated component describing the differentiator behavior of CDS together with a folding component of the high frequency noise.

Appendix B

ICs Technical Data

This appendix summarizes some technical data about the realization of the ICs described throughout the thesis.

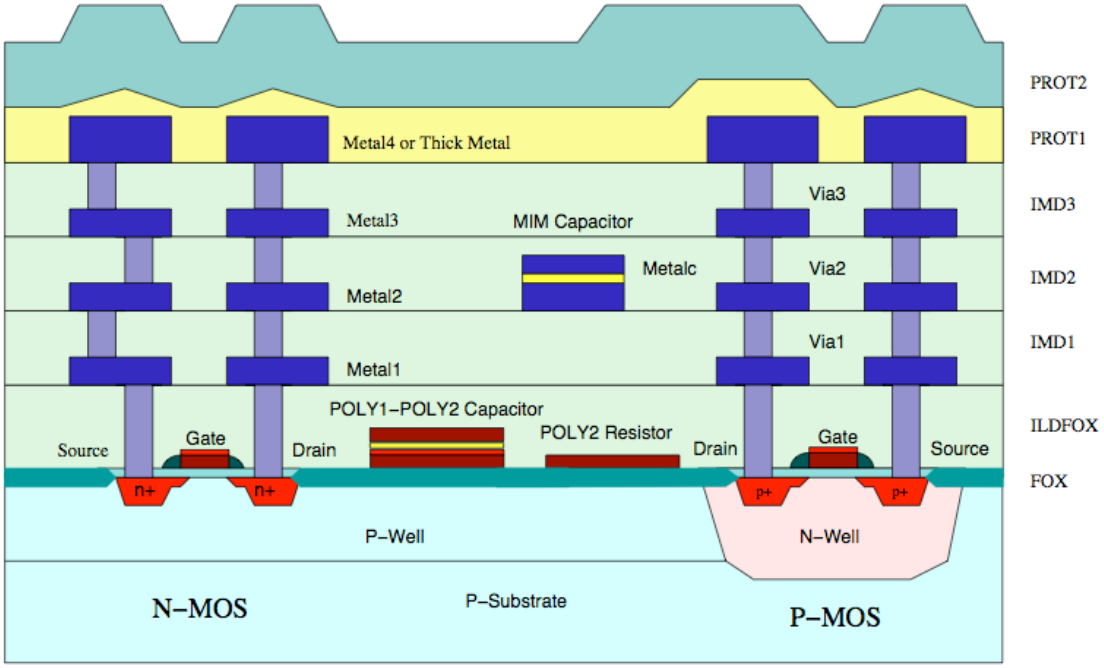

Fig. 109 Wafer cross-section of the AMS-C35B4C3 technology (0.35μm minimum channel length) used for all the ICs described in this manuscript. It is a standard 'analog' technology with 4 metal layers, poly-poly capacitor, high-resistivity poly-layer and single-well. Note that the metal-metal capacitor shown in the picture is only available in the different process AMS-C35B4M3.

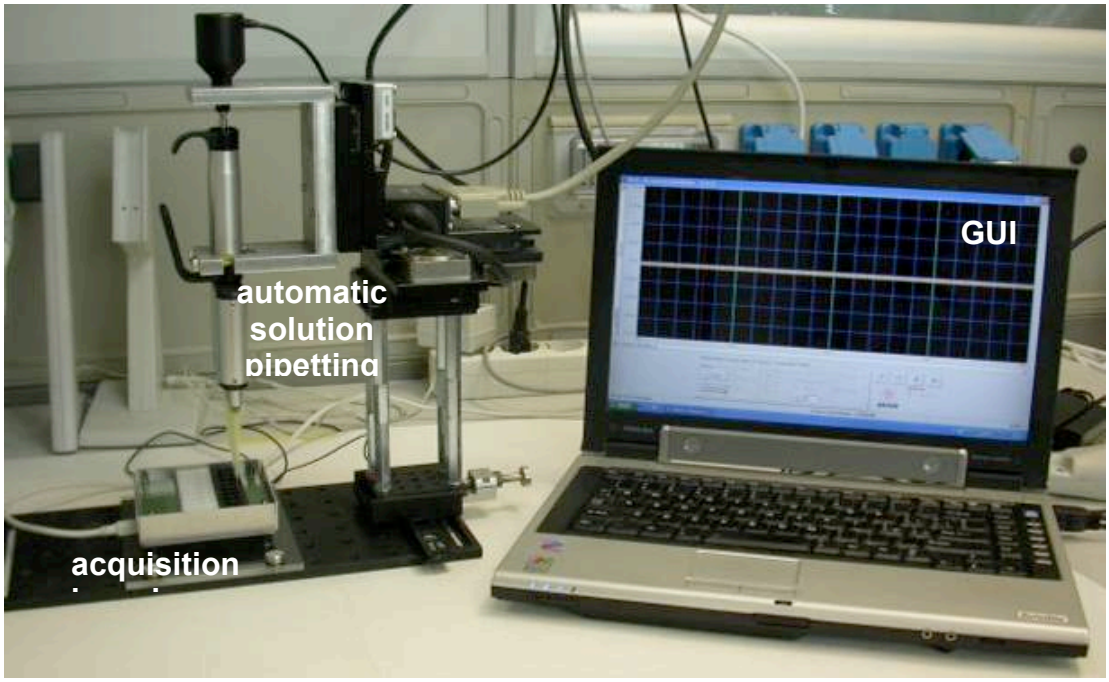

Fig. 110 Hybrid acquisition platform integrated into a fully automatic system for dispensing chemical solutions and compounds, for parallel BLM formation on several independent microfluidic devices [Thei,11]. This kind of architecture has been realized to work with the IC presented in [Bennati,09], but can be easily customized for the DC-Transient current sensing interface described in chapter 4.

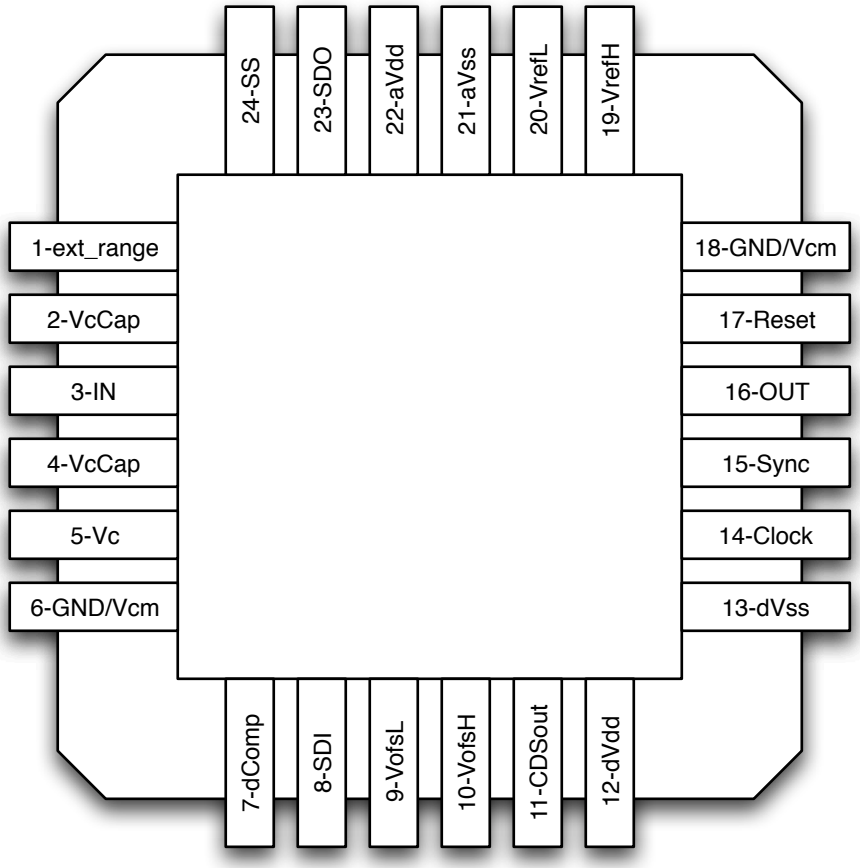

Fig. 111 Pinout of the DC-Transient current-sensing IC described in chapter 4, implemented in a standard QFN-24 package.

Pin	Name	Description	Range
1	ext_range	Pin for shunt feedback resistor in case of external range	
2-4	VcCap	Pin for external capacitor filtering the Vc signal	6nF for 10KHz filter
3	IN	Analog input	
5	Vc	Control voltage input/output test pin for the internal Vc DAC	±250mV
6-18	GND/Vcm	Ref. voltage at middle supply	0 V / 1.65 V
7	dComp	Output digital compensation	
8	SDI	SPI input data pin	from dVss to dVdd
9	VofsL	Test pin: Vcm – 100mV	
10	VofsH	Test pin: Vcm + 100mV	
11	CDSout	Test pin: CDS output signal	
12	dVdd	Digital power supply (positive)	1.65 V / 3.3 V
13	dVss	Digital power supply (negative)	-1.65 V / 0 V
14	Clock	Clock input and SPI clock	from dVss to dVdd
15	Sync	Synchronization for OUT signal	from dVss to dVdd
16	OUT	Digital output	from dVss to dVdd
17	Reset	Reset input, active HIGH	from dVss to dVdd
19	VrefH	Test pin: + 450mV	
20	VrefL	Test pin: – 450mV	
21	aVss	Analog power supply (negative)	-1.65 V / 0 V
22	aVdd	Analog power supply (positive)	1.65 V / 3.3 V
23	SDO	SPI output data pin	from dVss to dVdd
24	SS	SPI enable input	from dVss to dVdd

Table 15 Pinout description for the DC-Transient current-sensing IC described in chapter 4.

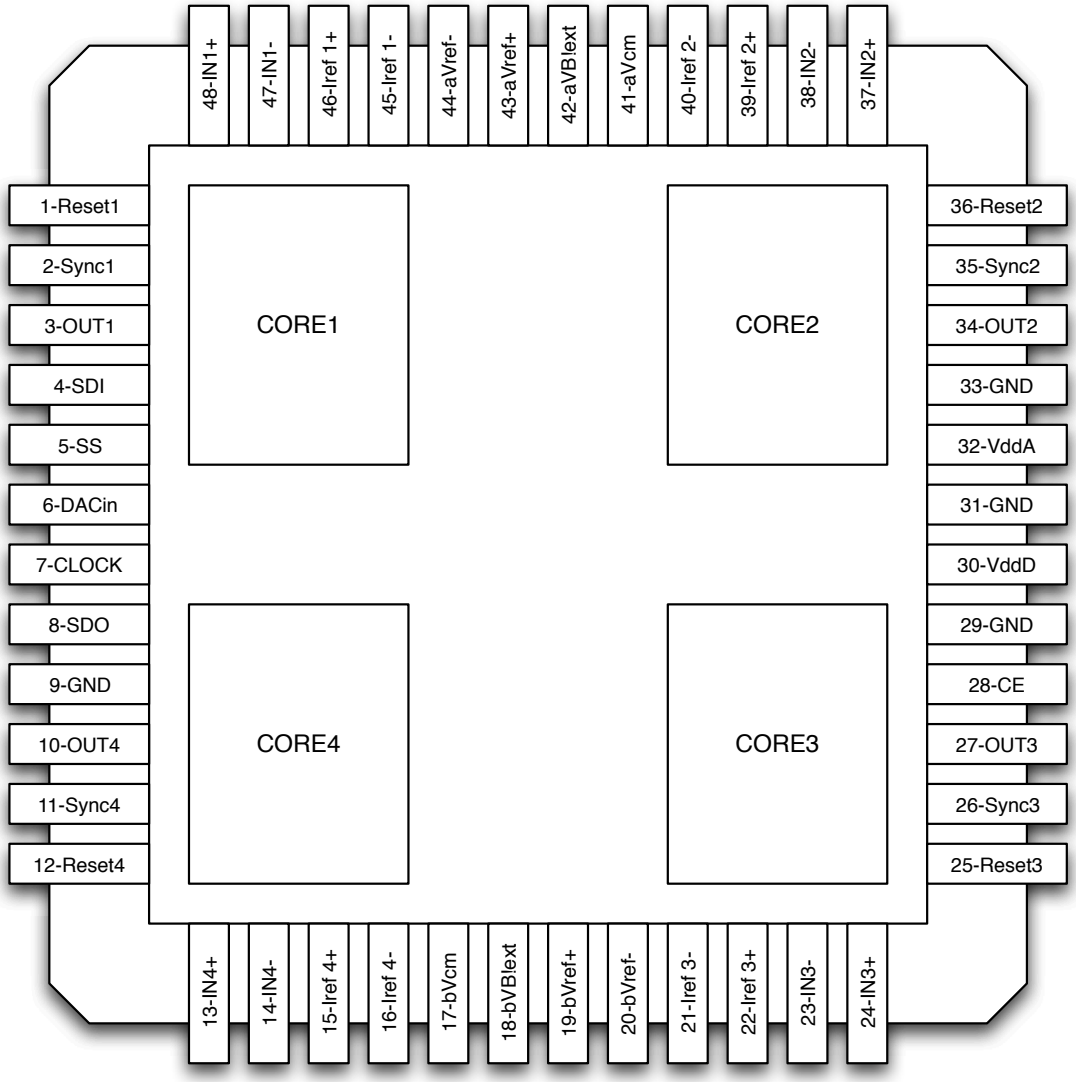

Fig. 112 Pinout of the AC-Impedance Sensing IC described in chapter 5, implemented in a standard QFN-48 package.

PIN	NAME	DIRECTION	DESCRIPTION
1	Reset1	out	Reset signal for CORE1
2	Sync1	out	Synchronization for OUT1 signal
3	OUT1	out	Digital output or CORE1
4	SDI	in	SPI input data pin
5	SS	in	SPI enable input
6	DACin	in	Digital input for the delta-sigma modulated sine wave
7	CLOCK	in	System and SPI Clock
8	SDO	out	SPI output data pin
9	GND		Ground
10	OUT4	out	Digital output or CORE4
11	Sync4	out	Synchronization for OUT4 signal
12	Reset4	out	Reset signal for CORE4
13	IN4+	in	Positive analog input for CORE4
14	IN4-	in	Negative analog input for CORE4
15	Iref4+	out	Positive analog output for current ref. of CORE4
16	Iref4-	out	Negative analog output for current ref. of CORE4
17	bVcm	out	Vcm signal generated by BGR-b = 1.65V
18	bVB1ext	out	VB1 signal generated by BGR-b = 0.85V
19	bVref+	out	Vref+ signal generated by BGR-b = 2.1V
20	bVref-	out	Vref- signal generated by BGR-b = 1.2V
21	Iref3-	out	Negative analog output for current ref. of CORE3
22	Iref3+	out	Positive analog output for current ref. of CORE3
23	IN3-	in	Negative analog input for CORE3
24	IN3+	in	Positive analog input for CORE3
25	Reset3	out	Reset signal for CORE3
26	Sync3	out	Synchronization for OUT3 signal
27	OUT3	out	Digital output or CORE3
28	CE	in	Chip enable, active High
29	GND		Ground
30	VddD		Digital Power supply (3.3V)
31	GND		Ground
32	VddA		Analog Power supply (3.3V)
33	GND		Ground

34	OUT2	out	Digital output or CORE2
35	Sync2	out	Synchronization for OUT2 signal
36	Reset2	out	Reset signal for CORE2
37	IN2+	in	Positive analog input for CORE2
38	IN2-	in	Negative analog input for CORE2
39	Iref2+	out	Positive analog output for current ref. of CORE2
40	Iref2-	out	Negative analog output for current ref. of CORE2
41	aVcm	out	Vcm signal generated by BGR-a = 1.65V
42	aVB1ext	out	VB1 signal generated by BGR-a = 0.85V
43	aVref+	out	Vref+ signal generated by BGR-a = 2.1V
44	aVref-	out	Vref- signal generated by BGR-a = 1.2V
45	Iref1-	out	Negative analog output for current ref. of CORE1
46	Iref1+	out	Positive analog output for current ref. of CORE1
47	IN1-	in	Negative analog input for CORE1
48	IN1+	in	Positive analog input for CORE1

Table 16 Pinout description for the AC-Impedance Sensing IC described in chapter 5.

Index of Abbreviations

AC	Alternating Current
A_{CM}	Common Mode Gain
A_{DM}	Differential Mode Gain
ADC	Analog to Digital Converter
Ag/AgCl	Silver/Silver-Chloride
BiCMOS	Bipolar CMOS
BGR	Band-Gap Reference
BJT	Bipolar Junction Transistor
BLM	Bilayer Lipid Membrane
BPDS	Band-Pass Delta-Sigma
CAD	Computer Aided Design
CDS	Correlated Double Sensing
CE	Counter Electrode
CM	Common Mode
CMFB	Common Mode FeedBack
CMRR	Common Mode Rejection Ratio
CNT	Carbon NanoTube
CMOS	Complementary Metal Oxide Semiconductor
CS	Common Source
CSA	Charge-Sensitive Amplifier
CT	Continuous Time
CTD	Conductivity-Temperature-Depth
DAC	Digital to Analog Converter
DC	Direct Current
DDA	Differential Difference Amplifier
DM	Differential Mode
DNA	DeoxyriboNucleic Acid
DUT	Device Under Test
d-OCL	Digital Offset Correction Loop
DR	Dynamic Range
DSP	Digital Signal Processing
DT	Discrete Time

EIS	Electrochemical Impedance Spectroscopy
ENOB	Equivalent Number Of Bits
EQNB	EQuivalent Noise Bandwidth
FET	Field Effect Transistor
FIB	Focused Ion Beam
FIR	Finite Impulse Response
FOM	Figure Of Merit
FPGA	Field Programmable Gate Array
FS	Full-Scale
GBW	Gain BandWidth product
GND	Ground
HTS	High Throughput Screening
I.C.	Inversion Coefficient
IC	Integrated Circuit
IF	Intermediate Frequency
ISFET	Ion-Sensitive Field Effect Transistor
JFET	Junction Field Effect Transistor
KCl	Potassium Chloride
LNA	Low-Noise Amplifier
LPF	Low-Pass Filter
MDS	Minimum Detectable Signal
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MWNT	Multi Walled NanoTube
NEF	Noise Efficiency Factor
NEMS	Nanometer Electro-Mechanical System
NTF	Noise Transfer Function
NW	NanoWire
opamp	Operational Amplifier
OSR	OverSampling Ratio
OTA	Operational Transconductance Amplifier
PCB	Printed Circuit Board
PM	Phase Margin
PRT	Platinum Resistance Thermometer
PSD	Power Spectrum Density
PSRR	Power Supply Rejection Ratio
RE	Reference Electrode

red-ox	Reduction-Oxidation
RF	Radio Frequency
rms	Root Mean Square
ROM	Read Only Memory
r.p.	Random Process
RTD	Resistance Temperature Detector
S.I.	Strong Inversion
SiNW	Silicon NanoWire
S&H	Sample and Hold
SNR	Signal to Noise Ratio
SOI	Silicon On Insulator
SoS	Silicon on Sapphire
SPI	Serial-Parallel Interface
SQNR	Signal to Quantization Noise Ratio
STF	Signal Transfer Function
SWNT	Single Walled NanoTube
SYNC	Synchronization signal
THD	Total Harmonic Distortion
TIA	TransImpedance Amplifier
USB	Universal Serial Bus
USR	UnderSampling Ratio
VLSI	Very Large Scale Integration
WE	Working Electrode
W.I.	Weak Inversion
wss	Wide Sense Stationary

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List of Publications

Journals

F. Thei, M. Rossi, M. Bennati, M. Crescentini, F. Lodesani, H. Morgan, and M. Tartagni, "Parallel Recording of Single Ion Channels: A Heterogeneous System Approach" *IEEE Trans. Nanotechnol.,* vol. 9, pp. 295-302, Mar 2010.

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Patents

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