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Analog Signal Acquisition and Conditioning for Near-Field Capacitive Communication and Active Combined EEG-EIT Monitoring

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Introduction

A sensor is a device that measures a physical quantity and converts it into a signal that can be read by an instrument or by an observer. In general, the sensed quantities are of analog nature, and can be further elaborated in an analog environment or converted for digital processing.

Focus of the presented work has been on the acquisition and conditioning of analog signals for near-field capacitive communication and biological data acquisition. In the developed applications, signals are transferred between heterogeneous medias, at short distances or in contact.

Miniaturization of VLSI technology has allowed the integration of a growing number of devices in a single die, and this trend still holds today. Nevertheless the increasing technical challenges and developing costs are increasing exponentially, thus pushing for the investigation of different approaches to increase system complexity and performance, in general referred to as the *More-than-Moore* approach. An analog wireless channel, based on near-field capacitive communication can be a feasible way to allow inter-chip vertical proximity communication between different dies which can be fabricated in different technologies and assembled at a later time. This allows each block (analog, digital, memory, optical and so on) to be designed in the best suitable technology, but still be able to communicate with the other ones in a 3D stacked system known as a system-in-package (SiP).

Nevertheless an analog channel can be implemented to allow communication between even *more heterogeneous* devices, such as a probe card and an integrated circuit (IC). This can be applied to semiconductor wafer testing, an early test procedure for ICs performed at the time when the ICs are

still laying on the silicon wafer. Currently such tests are performed by mechanical contact of probes, with many different drawbacks, the first being the damage caused by the contact itself.

In this direction, we can think of analog signal acquisition from even *more heterogeneous* systems, one being an *electronic* device, and one being a *biological* system, such as the human body. In a scenario of gathering information from a biological sample we talk of bio-potential acquisition. This is the case for electroencephalography (EEG), which consists in sensing voltages on a human scalp, as produced by the firing of the neurons in the brain cortex. Electrical impedance sensing currents can also be applied in order to gather further information on the body under study, such as in electrical impedance tomography (EIT), with currents and voltages applied and sensed at the boundaries in order to infer the electrical conductivity of the body under study.

In this thesis such applications have been studied and implemented, and we believe the development of interfaces between electronic devices and biological systems is only at the very beginning of a long and exciting journey.

The significant original contributions of this work include:

- Developed an innovative flow for near-field capacitive communication modeling for 3D stacked structures.
- Introduced capacitive communication for wireless wafer probing and tested with the implementation of a prototype chip with dedicated wireless pads as well as modified libray pads for contact and contactless functioning and a wireless probe card.
- Introduced the first readout circuit for simultaneous acquisition of EEG and EIT signals with low-noise and high-CMRR behavior.
- Introduced a model for dry flat and spiked electrodes as a function of area, number of spikes and penetration depth.

This thesis is organized as follows: Chapter 1 introduces capacitive coupling for near-field chip-to-chip communication and wireless wafer

probing. In Chapter 2 circuits for analog EEG and EIT signal acquisition are presented, while in Chapter 3 the electromagnetic problem of contact impedance between biological and electronic systems is discussed. Finally conclusions are drawn.

Chapter 1

Capacitive coupling for near-field communication

The mainstream approach to the integration of multi-functional systems to handle and process large amount of data is represented by Systems-on-a-Chip (SoC). In a SoC all building blocks are fabricated in a single die and can hence communicate at very high speed with each other. Nevertheless, SoCs today need to face many design challenges since integration on a single die has two inherent drawbacks: limited flexibility and yield loss. The first is caused by the fact that each part of the system is fabricated in the same lithographic step, while the second is due to the intrinsic direct relationship between system complexity and silicon area. An appealing solution to overcome the limitations of SoCs is represented by 3D stacking technology either at package or die level. The latter approach, although it involves more technological challenges, can provide shorter and hence faster interconnections between two substrates and at the same time guarantees heterogeneity, while also reducing the systems footprint and volume. This approach is commonly referred to as 3D System-in-Package (SiP) integration and caters for assembly of dies fabricated in different technologies such as digital, memory, analog, optical as sketched in Fig. 3.3.

By exploiting the third dimension for routing, the average path length of the interconnects is reduced, thus decreasing the resistive and capac-

itive parasitic elements and optimizing performance in terms of power and speed. Vertical interconnects can be placed anywhere along the die area and hence a higher pin count can be implemented, achieving larger bandwidths.

1.1 3D stacking technologies for chip-to-chip communication

Although the benefits of 3D technology are potentially reached with any 3D die assembly, technological differences have a huge impact on system performance. Current state of the art technologies can be grouped into ohmic and AC-wireless interconnects. Several ohmic interconnects can be used such as wire bonding, pillar bumps and Through-Silicon-Vias (TSVs), while wireless solutions are based either on capacitive or inductive coupling.

Wire bonding imposes the fewest assembly challenges, but is also the

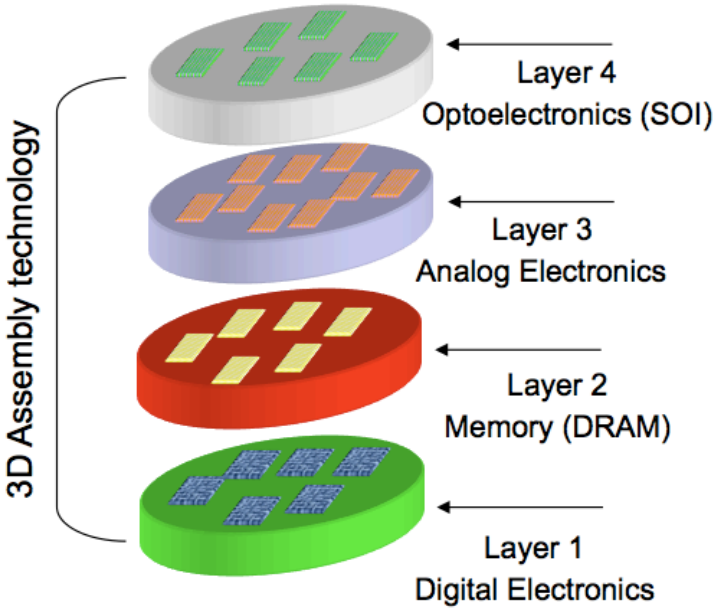


Figure 1.1: 3D assembly technology

least promising in terms of power dissipation and bandwidth capabilities: parasitic resistances and wire capacitances (typically around a few picoFarads) put a constraint on minimum channel delay and power consumption. At the same time parallelism cannot be increased as the I/Os are limited to the dies periphery just as in 2D interconnections, and pitches are limited by the bonding process (typically $100\mu m$).

Pillar bump technology is significantly more advanced than wire bonding, since these interconnects are not limited to the chip periphery and can also achieve smaller pitches, typically around $60\mu m$, with a capacitive load of about 50fF, which leads to much lower power dissipation than wire bonding [5].

Nevertheless high data rates require thousands of pillar bumps: process variations or even bump oxidation can result in electrical open-circuits compromising the system functionality and decreasing the overall yield. The state-of-the-art for 3D vertical ohmic interconnects is represented by TSVs, which allow vias to be built with widths of only a few micrometers, and exhibit an ohmic load smaller than 3Ω [6, 7, 8, 9, 10]. Although TSVs can achieve high frequencies and parallelism capabilities, they have the disadvantage of requiring extra wafer processing to accomplish vertical interconnections, which has a negative impact on costs and yield as is the case for pillar bumps.

Contactless technology forms a good trade-off between performance and complexity. Fig. 1.2 and Fig. 1.3 show schemes for inductive and capacitive links. In inductive coupling transmission is current-controlled while capacitive coupling is voltage-driven. These interconnects have low parasitic loads and can hence give advantages in terms of bandwidth and energy consumption when compared to DC vertical connections. Table 1.1 summarizes the main features of the above mentioned technologies.

Both inductive and capacitive coupling technologies have proved capable of communicating at Gb/s data rate with a power consumption below $100fJ/b$ [11, 14, 15, 16, 17, 18, 13, 19, 20, 21]. Contactless communication could thus provide a valid alternative to state-of-the-art Through-Silicon-Vias. In fact although TSVs have fewer limitations as they allow

more than two stacked dies per package, they require additional process steps and production equipment which have a big impact on manufacturing costs and yield. Moreover wireless communication allows one to assemble dies which can function at different power supplies and without the need for any ESD protection. To the best of our knowledge, the

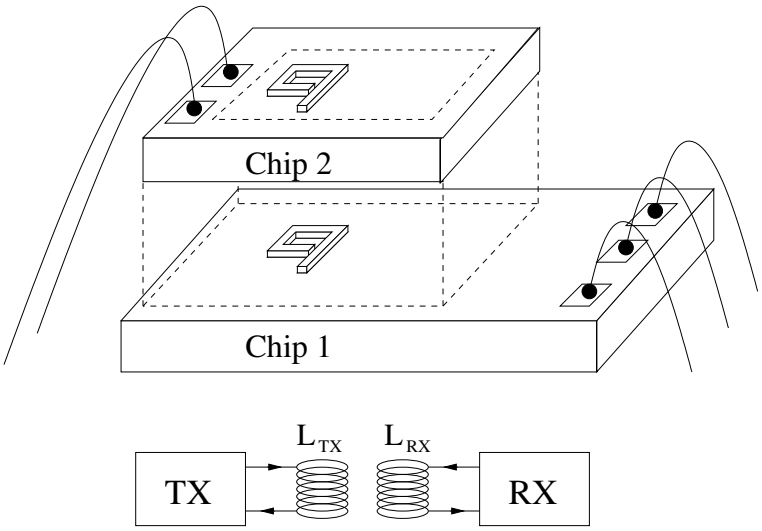


Figure 1.2: Scheme of an inductive coupling link

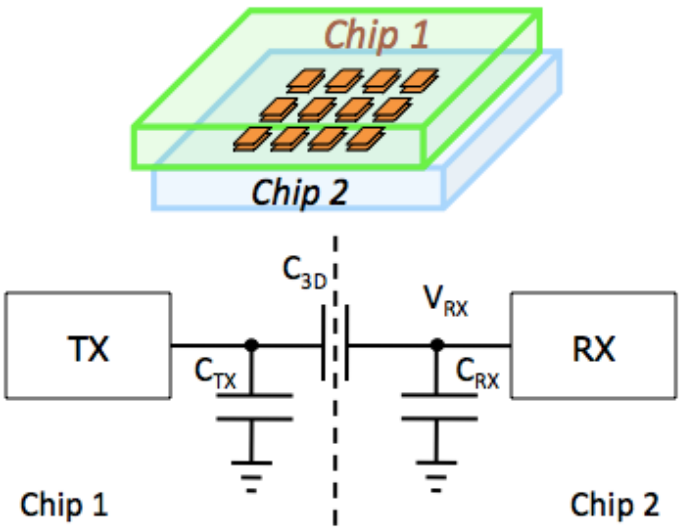


Figure 1.3: Scheme of a capacitive coupling link

	Bonding wires	**Bumps [5]**	**Through -silicon vias [6, 7, 8, 9, 10]**	**Inductive contactless interconnects [11, 12]**	**Capacitive contactless interconnects [13]**
Assembly	Die level	Die and wafer level	Wafer level	Die level	Die and wafer level
Pitch	$100\mu m$	$60\mu m$	$2.5\mu m$	$20\mu m$	$10\mu m$
Load	$1pf$	$50fF, 14m\Omega$	2.5Ω	$10\mu H$	$6fF$

Table 1.1: 3D stacking technologies.

minimum inductor sizes were presented in [12] with a pitch of $20\mu m$ and a vertical distance between $1 - 5\mu m$. Inductive coupling allows transmission at farther distances ([22] in Fig. 1.4) but in this case the size of the inductors must be increased. In [13] capacitive links with a pitch as small as $10\mu m$ are presented for a vertical distance of $1\mu m$, which means that higher parallelism for a given area can be achieved, as shown in Fig. 1.4.

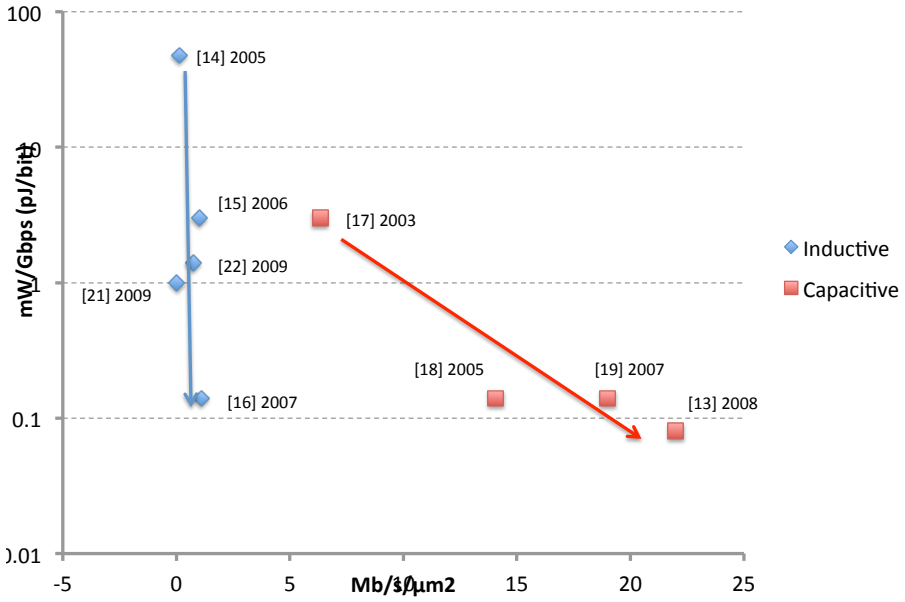


Figure 1.4: Comparison among inductive and capacitive interconnections.

1.1.1 Circuit design for capacitive coupling

In capacitive coupling technology, two electrodes fabricated in the upper metal layer are placed in close proximity, creating a parallel plate capacitor. A signal transmitted from one chip to the other through the capacitive interface is attenuated by a capacitive divider (Fig. 1.3) by a factor L:

$$L = \frac{C_{3D}}{C_{3D} + C_{RX}} \tag{1.1}$$

In the above formula, C_{3D} represents the capacitive coupling between the two aligned electrodes, while C_{RX} is the parasitic capacitance of the receiving electrode. The attenuation factor has a direct impact on the transceiver design constraints and dedicated communication circuitry must be implemented for the signal to be successfully transmitted and restored. In order to limit signal attenuation L the inter-electrode capacitance C_{3D} should be as large as possible. C_{3D} can be thought of as a parallel plate capacitor and is strongly dependent on the physical geometry of the electrodes which serve as plates. C_{3D} has a quadratic dependency on the electrode widths (W) and an inverse linear dependency on vertical distance (d) as explained in paragraph 1.1.3.

Digital communication

Synchronous [19] and asynchronous [13] communication protocols have both been implemented in $0.13\mu m$ CMOS technology for digital communication. Fig. 1.5 outlines a scheme for the synchronous circuitry.

The transmitter performs a level-to-edge conversion while the receiving circuitry is biased at the logic-threshold. An additional asynchronous channel must be implemented for clock transmission but it can be shared among many synchronous channels. In asynchronous communication (Fig. 1.6) the transmitting function is performed by a buffer driving the input electrode while the receiver is designed in a double feedback topology in order to guarantee high sensitivity to input voltage transition while minimizing static power.

The two communication protocols have been exhaustively tested and

compared. Synchronous communication with $15\mu m$ x $15\mu m$ electrodes has proved able to achieve a throughput of 1.2 Gbps/pin, while 2.4 Gbps/pin is achieved by the asynchronous approach with the same electrode size. In Table 1.2 power consumptions and throughput per pin are summarized for both synchronous and asynchronous circuits with different electrode sizes.

The asynchronous protocol shows better performance, in terms of both speed and power and is preferred for SiP applications. Moreover, the asynchronous approach allows bidirectional channels to be implemented, although in this case the maximum measured throughput proves to be 1.5Gbps/pin, lower than mono-directional channels but still faster than

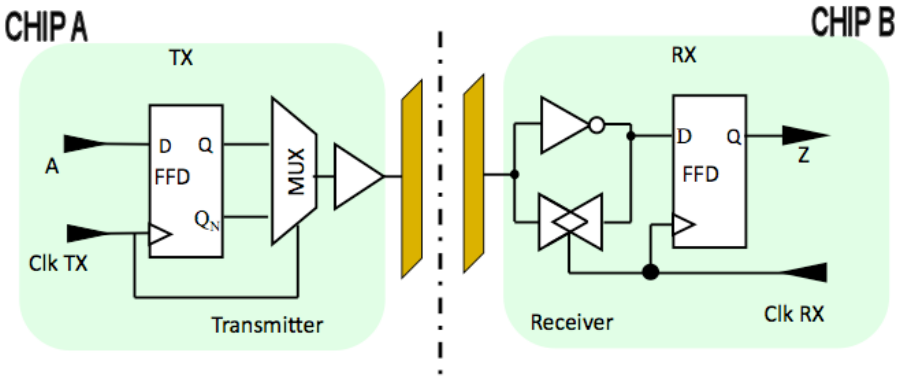


Figure 1.5: Synchronous communication.

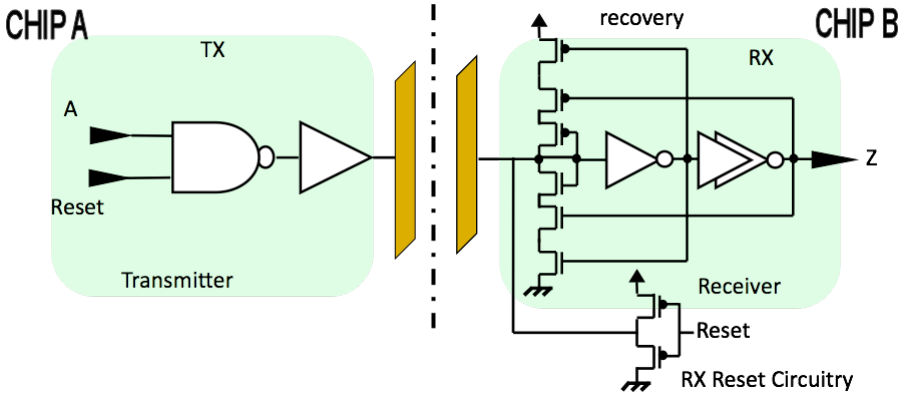


Figure 1.6: Asynchronous communication.

Size	Throughput/pin	
	Synchronous [19]	Asynchronous[13]
$8x8\mu m^2$	1.23	2.3
$15x15\mu m^2$	1.2	2.4
$20x20\mu m^2$	1	2.5
Average power	$0.11\mu W/MHz + 17\mu W$	$0.15\mu W/MHz + 1.6\mu W$

Table 1.2: Measured performance for different electrode sizes.

synchronous communication. BER measurements demonstrate the reliability of these AC interconnections with no error on more than 10^{12} bits transmitted [13].

Analog communication

Although digital communication has been the main focus of 3D capacitive channels, it has been demonstrated that capacitive links can also be used to transmit analog signals [23]. The scheme shown in Fig 1.7 includes a calibration channel which automatically generates the control voltage of a voltage gain amplifier (VGA) in order to compensate for the attenuation factor L. The generated control voltage is then applied to all the identical VGAs of the n signal channels. Assuming ideal behavior by the circuit building blocks, amplitude errors between input and output voltages can only be caused by mismatches in the attenuation factors between the calibration and signal channels. This approach may be useful for sensor network applications where analog to digital conversion can be an inconvenient option.

1.1.2 Assembly

High accuracy assembly is one of the essential requirements for capacitive coupling and for this reason various different technological assembly options have been investigated, at both chip and wafer level [13, 24]. In die-level assembly, a pair of dies is stacked face-to-face with the two chips slightly shifted, as shown in Fig. 1.8. The electrodes are fabricated in the upper aluminum layer and no passivation is applied in order to minimize

the inter-chip distance and hence reduce attenuation. Dies are held together by an acrylate-based adhesive, which also provides inter-chip isolation and serves as a dielectric ($\epsilon_r \approx 2.7$) for the parallel plate capacitor formed by the two electrodes.

The stacked dies are mounted on a standard board implementing a Chip-on-Board (CoB) assembly to provide I/O and power connectivity. Standard wire-bonding connects the bottom die to the top side of the PCB, while the top die is bonded to the bottom side of the board through a milled-out trench [25]. Wire-bonding is covered by a glob top to increase

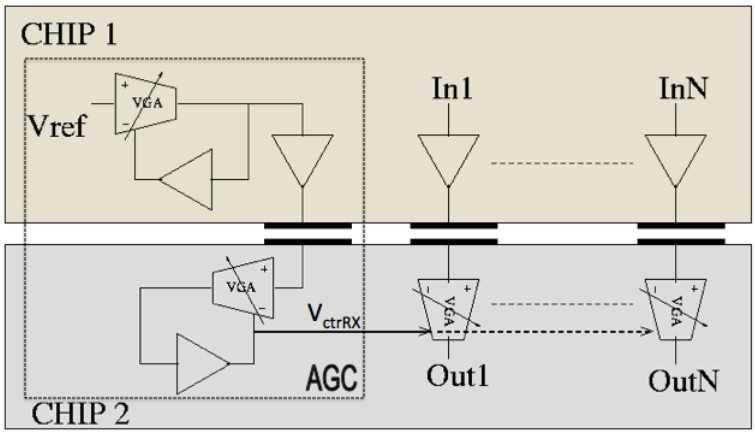


Figure 1.7: Block diagram of the 3D capacitive transmission system for n analog signals. The buffers have unit gain.

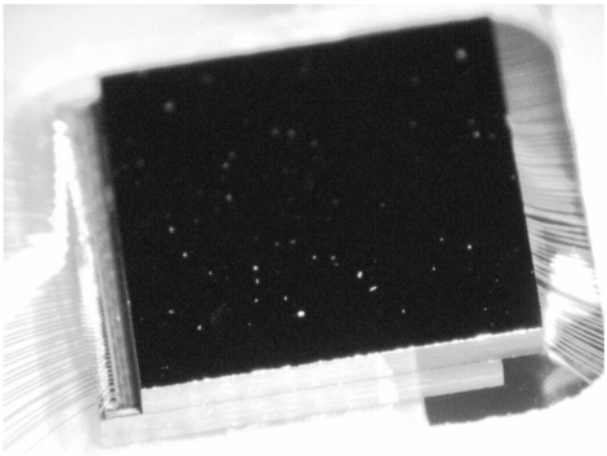


Figure 1.8: Die-level assembly.

its mechanical reliability. An inter-electrode distance below $1\mu m$ has been achieved with die-level assembly. In wafer-level assembly (Fig. 1.9) two wafers with symmetrical layouts are conditioned for molecular direct bonding, precisely aligned and bonded face-to-face [24]. Then the top substrate of the stacked wafers is thinned down and the buried I/O pads of both chips are opened by creating trenches. With this approach, $1\mu m$ alignment accuracy and $400nm$ inter-electrode distance have been achieved. Wafer-level assembly has a big advantage in terms of parallelism, and is hence particularly suitable for highly regular structures such as memories. On the other hand it is strongly affected by Known-Good-Die (KGD) issues as the assembled chips cannot be tested before the assembly. Yield is also decreased by the fact that assembling devices of different areas causes a waste of silicon on the wafer including the smallest die. In die-level assembly KGD issues are less critical because chips can be tested before stacking. This assembly option is also more flexible and suitable for dies

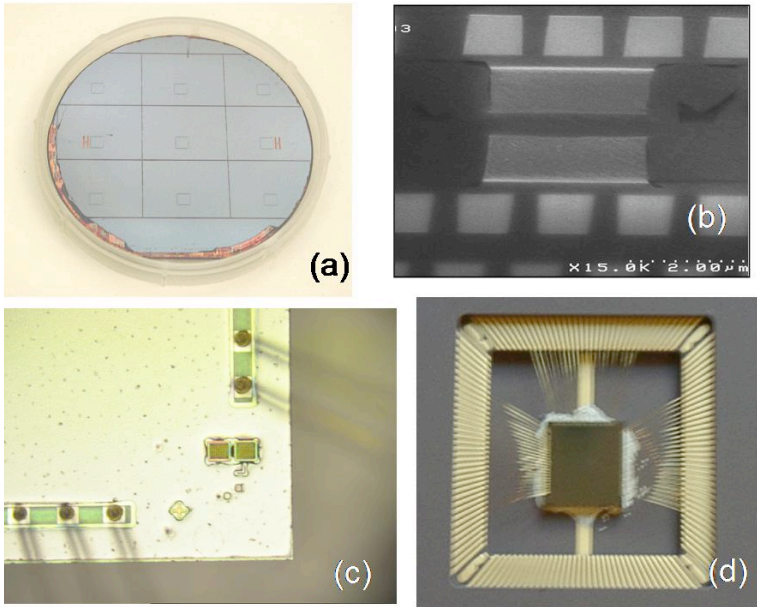


Figure 1.9: Wafer-to-wafer assembly: (a) wafers are aligned, stacked face-to-face and connected via direct molecular bonding; (b) SEM highlights the bonding interface; (c) via opening for I/O connections and (d) wire-bonding to standard ceramic package.

with different form factors. On the other hand chip-to-chip bonding has higher equipment costs and the assembly process has lower parallelism. The assembly option should therefore be carefully chosen according to the application. We believe that die-level assembly is the best choice for SiPs as its versatility more easily guarantees the heterogeneity needed.

1.1.3 Modeling

As pointed out at the beginning of this chapter, AC-wireless interconnects are very promising in terms both of performance and cost, nevertheless they have yet to be used in a commercial product. One of the reasons is the lack of 3D CAD support for the designer. These interconnects can not be modeled as common ohmic interconnects in terms of lumped RC or RLC circuits because of the wireless electro-magnetic nature of the transmission. Dedicated transmitter (TX) and receiver (RX) circuits must be designed to allow for wireless interconnection; the full 3D channel composed of a TX, an AC coupling link, and an RX must therefore be characterized in terms of performance measured as propagation delay and power consumption. In order to overcome such problems, the author has worked on an innovative design method as a technology enabler for capacitive coupling interconnects, introduced in [26] and further discussed in this thesis. Accurate 3D capacitive interface modeling is embedded in a 2D CAD flow which relies on standard post-layout parasitic extraction tools, allowing the designer to place 3D capacitive interconnects like any other 2D macro block [27]. As explained in paragraph 1.1.1, a signal transmitted from one chip to the other through the capacitive interface is attenuated by a factor L, which is given in equation 1.1 .

Fig. 1.10(a) and Fig. 1.10(b) present the proposed 3D communication channel and waveforms from SPICE simulations. The transmitting function is performed by a standard buffer driving the input electrode while the receiver implements a double feedback topology that provides high sensitivity to input voltage transition as well as high-impedance for the AC-input. For the RX to work correctly,

$$\Delta V_{RX} = \frac{C_{3D}}{C_{3D} + C_{RX}} V_{DD} > V_{min} \tag{1.2}$$

where V_{min} is the minimum amplitude of the voltage transition at the RX input node which guarantees an output voltage transition to the correct value.

FEM Simulator Based Characterization Flow

The attenuation factor L puts constraints on transmitting buffer transistor sizes and receiver sensitivity and for this reason modeling the capacitive

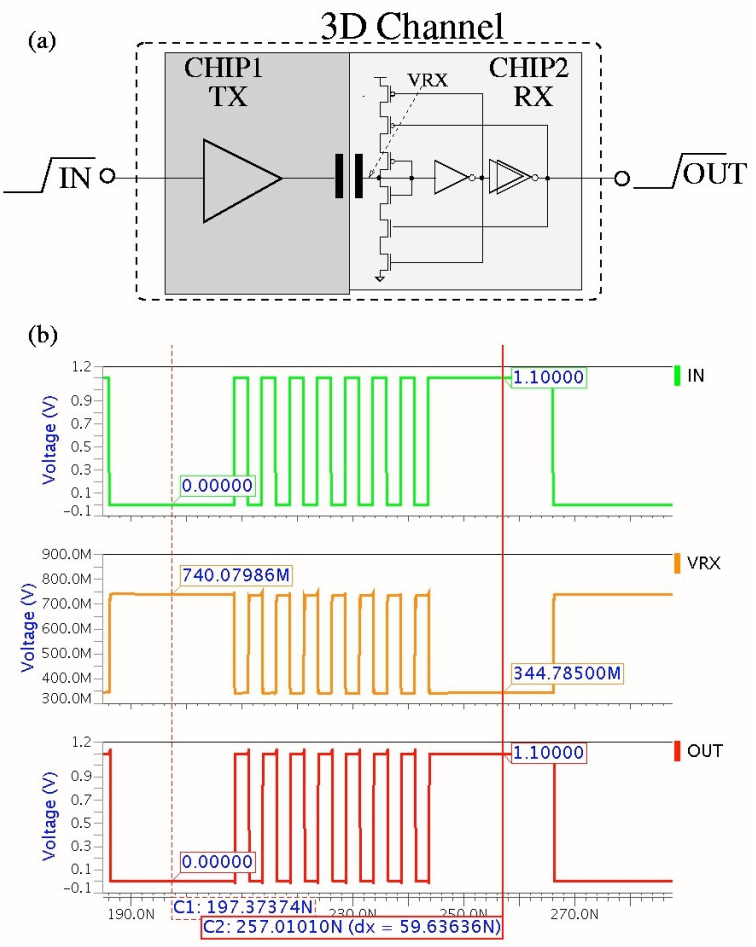


Figure 1.10: (a) 3D capacitive interconnection channel, (b) from top to bottom: V_{in}, V_{RX}, V_{out} waveforms.

interface becomes critical. With reference to Fig.1.3 and equation 1.1, finite element method (FEM) electromagnetic simulators such as Comsol [28] are in general used to compute the C_{3D} as a function of electrode size, pitch, inter-chip distance, die alignment and dielectric properties as shown in [29], whereas C_{RX} is estimated by standard post-layout parasitic extraction tools. A sketch illustrating this approach is shown in Fig. 1.11.

The output of the FEM simulator is used to model the wireless interconnections as a netlist of capacitors. This netlist is merged with the netlist extracted from the layout using 2D extraction tools, such as Raphael NXT. Although this approach is a feasible solution to characterizing the capacitive interconnections, there are some major drawbacks: first of all use of an FEM simulator makes automation of macrocell characterization harder to achieve for a standard CAD flow; moreover, FEM solvers are highly time-consuming. It must also be noted that the capacitive interconnection model drawn in Fig. 1.3 is a simplification, the nature of the problem being more complex: in the real case scenario C_{RX} is replaced by a capacitive matrix of cross-coupling and parasitic capacitances, as is shown in Fig. 1.12 for a 3x1 channel array.

Each C_{ij} represents a crosstalk capacitance between two electrodes,

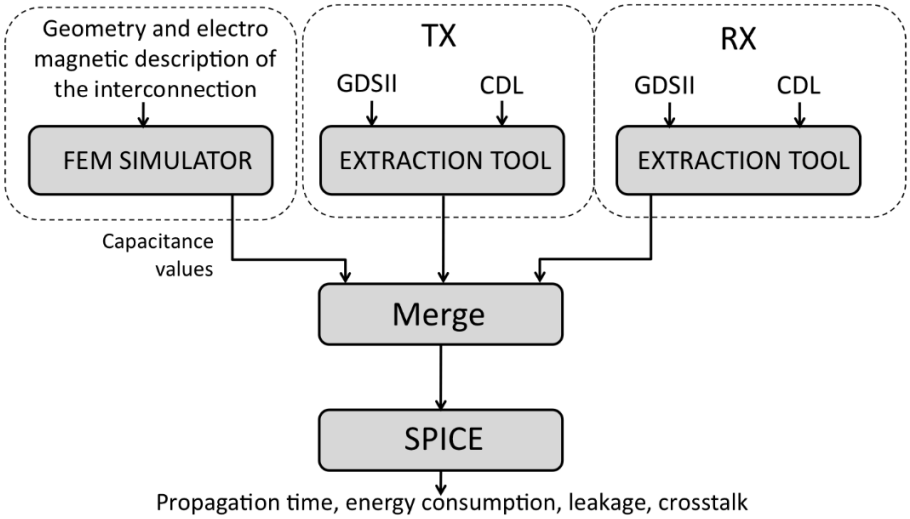


Figure 1.11: FEM simulator based characterization flow.

while C_{subi} are the electrode capacitances to the substrate and C_{3D_i} are the parallel plate capacitances. Only in a situation where all the neighboring electrodes are held at a constant potential or the distance of the neighboring electrodes makes the effects of cross-coupling capacitances negligible does the model of Fig. 1.12 turn back into the one shown in Fig. 1.3. Moreover, the physical structure of the capacitive coupling link is highly complex and difficult to replicate in an FEM simulator. As an example, Fig. 1.13 sketches the interface of two adjacent channels: the complex structure of the different dielectric layers commonly found in a CMOS process with the purpose of limiting inter-metal parasitic capacitances is also drawn in a simplified way. The geometry shown is inconvenient for any FEM solver where the minimum mesh element size in each subdomain is related to its thickness and could result in meshes with an unbearable number of elements.

Another important drawback of the flow shown in Fig. 1.11 is related

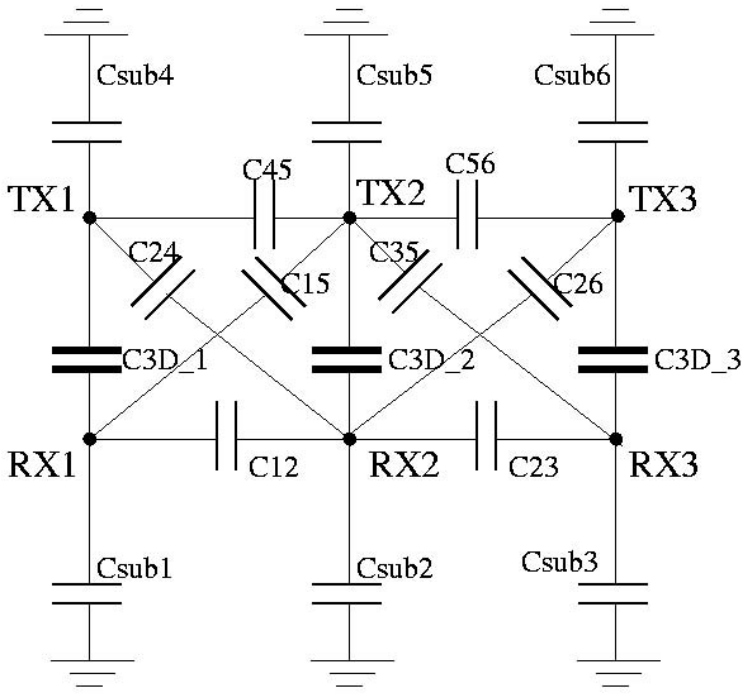


Figure 1.12: Model of a 3x1 channel array.

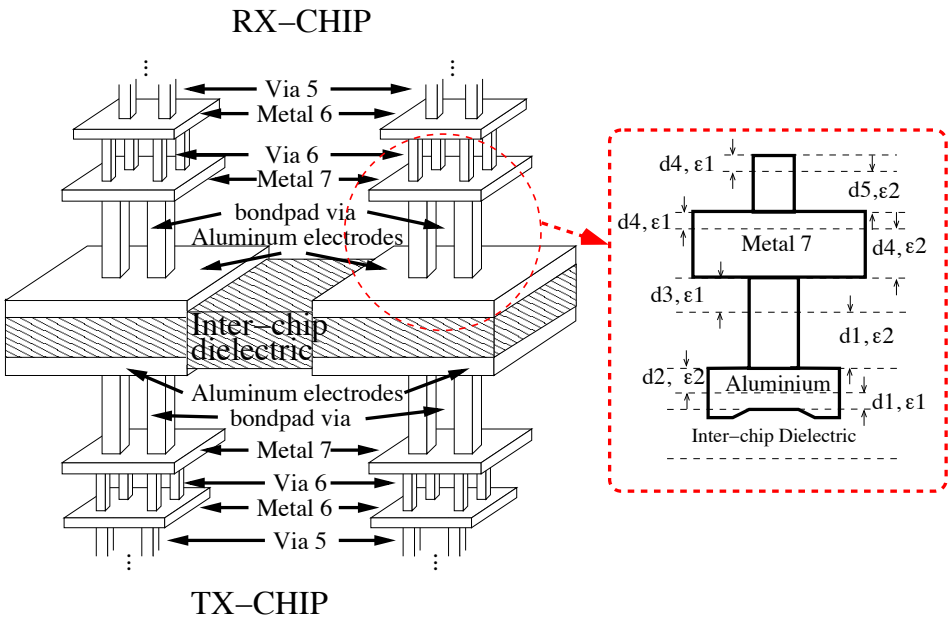


Figure 1.13: Interface of two neighboring channels: ϵ_i and d_i represent dielectric constants and thicknesses.

to accuracy. When the capacitive contributions to the substrate and to the adjacent channels constituting C_{RX} are evaluated separately from the vertical capacitance C_{3D} some approximation is introduced, resulting in an incorrect estimate for the channel attenuation L. A simplified Comsol simulation is shown in Fig. 1.14 to explain the phenomenon. The simulation consists of three adjacent channels held at constant potential. This does not represent the real case scenario but is the necessary setup to evaluate the inter-electrode capacitances in the FEM simulator. Fig. 1.14 shows how the electric field lines behave differently in the case of a single die (1.14 (a)) and of two stacked dies (1.14 (b)). When a vertical channel is created, a part of the field lines that would otherwise close into the neighboring electrodes of the same die or substrate now have a shorter path to the electrode above, thus reducing cross- coupling capacitances.

In [30] a non-FEM electromagnetic simulator (Agilent Momentum) based on the method of moment (MOM) was used to characterize capacitive interconnects but the same limits as for an FEM simulator apply to design

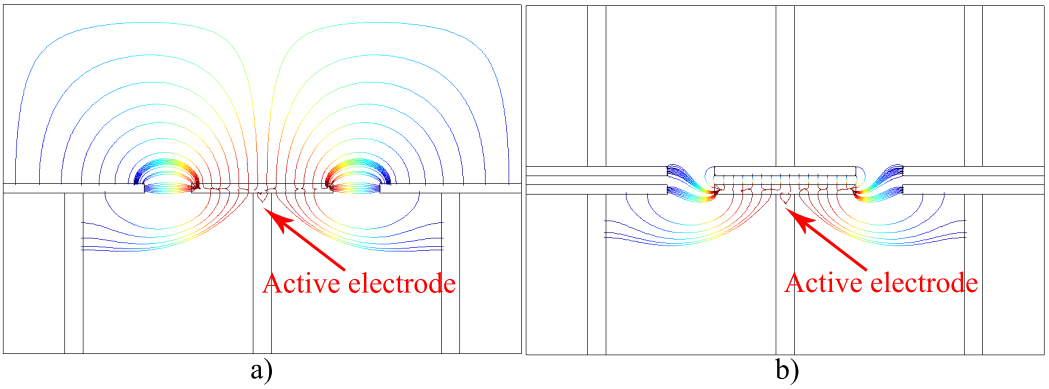


Figure 1.14: Electric field lines in a) single die assembly, b) a stacked die structure.

automation and accuracy in describing the real 3D structure. For the above reasons a new extraction and simulation flow was proposed.

Proposed characterization flow

The key goal of the proposed procedure is to use a single tool to evaluate all the capacitances of the model presented in Fig. 1.12, in order to overcome the issue explained at the end of paragraph 1.1.3. For this purpose two tools for post-layout parasitic extraction are used, Star-RCXT [31] and Raphael NXT [32], as well as a SPICE-like circuit simulator at the transistor level. Star-RCXT performs the extraction using pattern-matching algorithms based on interconnect structures calibrated with field solvers. In cases where higher accuracy is needed, such as critical nets, cells or blocks, Star-RCXT can interface with Raphael NXT, a fast field solver based on a statistical method known as random walks [33]. When compared to FEM, statistical methods have proven better suited to dealing with larger and more complex geometries. Thus, in a statistical method the electric potential can be evaluated at any given point without knowledge of the global solution [33], which means that the problem can be more easily parallelized. In the approach proposed all the capacitances are evaluated by Raphael NXT, as Star-RCXT is only used to translate the input files into Raphael NXT format.

Fig. 1.15 sketches the procedure, which comprises the following steps:

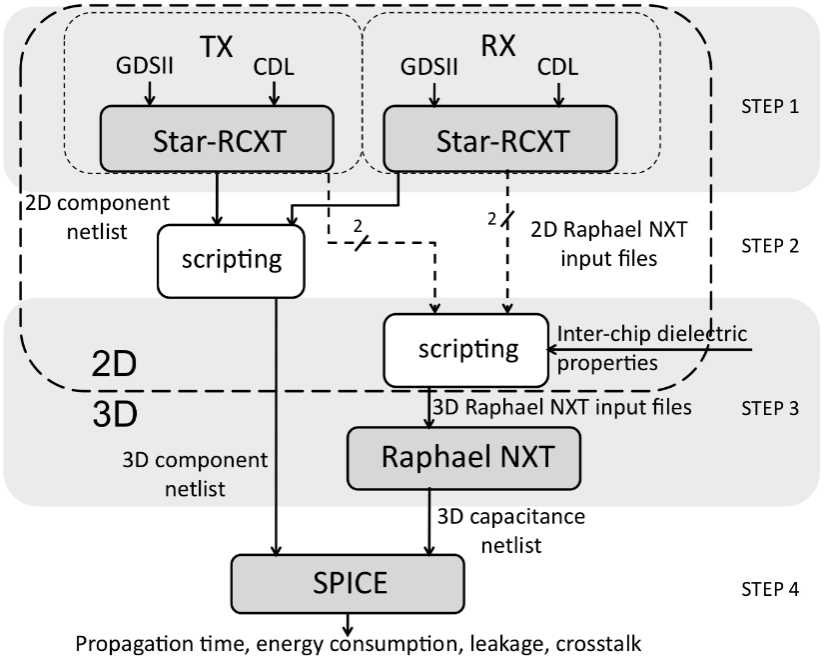


Figure 1.15: Proposed characterization flow.

- Step 1: TX and RX circuits are processed in parallel by Star-RCXT, given the CDL netlists at schematic level and the layout descriptions in GDSII format. For each circuit, Star-RCXT produces three output files. The first one (solid line) is the netlist describing the circuit topology with exact values of MOS transistor geometrical parameters (such as drain and source areas and perimeters) but no parasitic effects due to interconnection layers. The two additional files (dashed lines) are fed as inputs to Raphael NXT.

- Step 2: The TX and RX netlists are simply combined together, creating a single netlist.

- Step 3: The four files containing the layout information to extract the capacitance values are combined into a script via an additional technology file describing the inter-chip dielectric in order to completely describe the 3D structure as shown in Fig. 1.13. The stacked electrode positions can also be shifted to include assembly misalignments. The script output comprises the whole 3D structure and is

	FEM based flow [Fig. 1.11]	**Proposed flow [Fig. 1.15]**	**Relative difference**
Tools	*Comsol + Raphael NXT*	*Star-RCXT + Raphael NXT*	
C_{3D}[fF]	5.69	5.72	-0.5%
C_{PAR} [fF]	10.17	8.91	$+14\%$
L	0.359	0.391	-8.1%

Table 1.3: Extraction and simulation flow comparison in a worst case scenario (W=15μm, S=3μm)

processed by Raphael NXT to generate a capacitance netlist. Validation of the script was performed comparing the 3D capacitances extracted on a simplified structure with the values obtained by using a FEM simulator (Comsol [28]).

- Step 4: The capacitance netlist is then merged with the component netlist to create the input for SPICE circuital simulations.

In order to quantify the benefit of the proposed flow in terms of accuracy a direct comparison with the method of Fig. 1.11 was carried out. A test structure comprising a 3x3 channel matrix with $15\mu m$ electrodes widths (W) and $3\mu m$ electrodes spacing (S) was analyzed by the two different flows described, the central electrode being the one under test. A $1\mu m$ loctite inter-chip dielectric with $\epsilon_r = 2.8$ was chosen but could also be parameterized since various dielectric materials could be used if needed. Table 1.3 summarizes the results of this analysis. C_{3D} is the coupling capacitance between the RX and the TX electrodes as shown in Fig. 1.12 for the 3x1 case, while C_{PAR} represents the sum of all the cross-coupling and substrate capacitances at the receiving node RX. The negligible difference in C_{3D} values simulated with the two flows demonstrates that the proposed flow can be correctly used to estimate the coupling capacitance. On the contrary, there is a substantial difference in calculation of the total parasitic capacitance. This was to be expected and represents an overestimation of the FEM based flow as explained at the end of paragraph 1.1.3. This error translates into an incorrect estimate for the attenuation factor L, which has been estimated as in 1.1, with C_{RX} substituted by C_{PAR},

assuming all the neighboring electrodes are held at a constant potential. L is a critical parameter as it influences the channel's sensitivity according to 1.2 and directly affects the channel's performance, as will be explained in the following paragraph. The proposed approach is inherently more accurate, as the simulation environment represents the whole geometry while in the FEM based flow the electromagnetic problem is separated in different sub-problems. This should be avoided as the problems are not independent.

Design space exploration for 3D capacitive interconnects

The proposed 3D extraction and simulation flow is used to automate validation and characterization of capacitive coupled interconnections in order to ease integration of these in a digital design flow. A 3D channel matrix, with an arbitrary number of rows and columns and selectable channel width (W) and pitch (width W plus spacing S) is treated as a macro block. When varying W or S or both, the channel attenuation and the crosstalk immunity change, and a set of timing constraints have accordingly been computed to allow the macro block to be integrated in a digital flow, as shown in Fig. 1.16. The procedure described is applied to various different 3D capacitive structures, a single 3D channel as well as a 3x1 array and a 3x3 matrix.

Single 3D Channel

With reference to a CMOS 90 nm process with 1V nominal power supply, a single channel with electrode widths (W) of $15\mu m$ was first characterized considering worst (wc) and best case (bc) scenarios. The whole communication chain of 1.10 is characterized as a macro. Misalignment in the x and y direction may be caused by the assembly procedure. A $1\mu m$ misalignment in both directions is therefore included in the worst case scenario. The main electrical parameters for the communication circuitry are propagation time (tp_{rise} and tp_{fall} for rising and falling transitions, measured in ps and representing the delay between the input and output at their 50% values), dynamic energy consumption per transition (E_{dyn}, measured

	Worst case	Best case
MOS	*SLOW*	FAST
Temperature [°C]	125	-40
Misalignment x-direction [μm]	1	0
Misalignment y-direction [μm]	1	0
Vdd [V]	0.9	1.1

Table 1.4: Corner analysis parameters.

in fJ/b), current leakage averaged on the two different operating points ($I_{leakage_{av}}$ measured in μA), and the received voltage step (ΔV_{RX}, measured in mV). Table 1.4 summarizes the corner analysis parameters, while Table 1.5 shows simulation results.

Multiple Channel Macros

A 3x1 and a 3x3 macro were characterized with the proposed flow, in or-

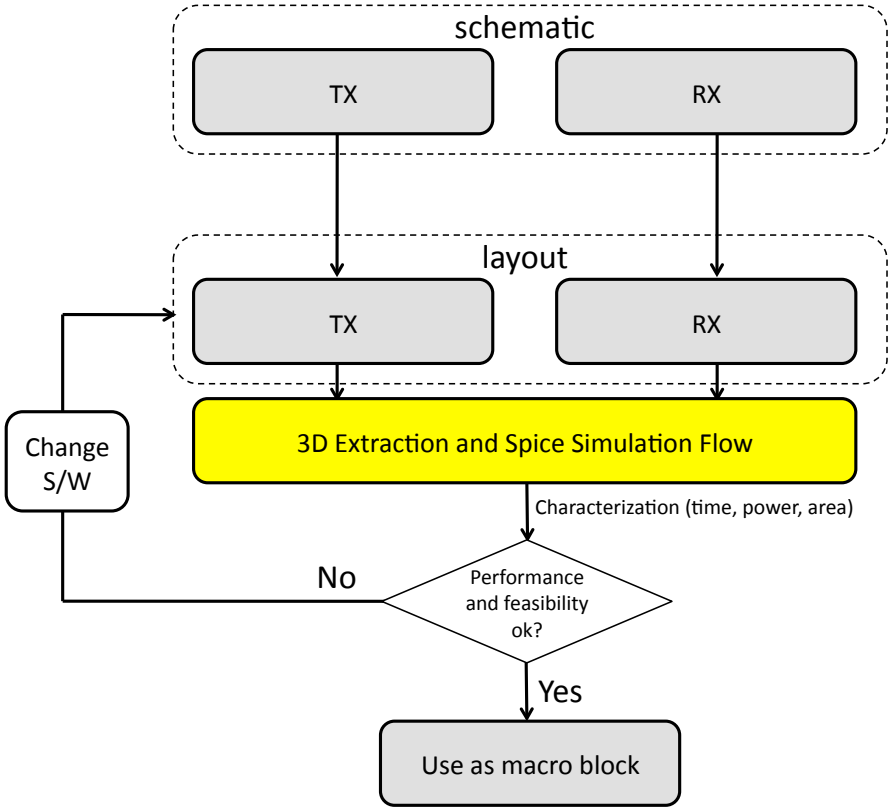


Figure 1.16: 3D macro design flow chart.

	Worst case	Best case
tp_{fall}	581	237
tp_{rise}	494	204
E_{dyn}	38	50.3
$I_{leakage_{av}}$	2.9	5.8
ΔV_{RX}	289	394

Table 1.5: Single channel characterization (W=15μm).

der to quantify the impact of crosstalk from neighboring electrodes upon channel performance as a function of spacing (S). Fig. 1.17(a) shows 3D views of a 3x3 matrix captured using a profilometer. In the simulation setup the central electrode acts as the victim, while all other electrodes act as aggressors and perform opposite transitions, as sketched in Fig. 1.17(b) for the 3x3 case, causing ΔV_{RX} to decrease. An example is shown in Fig. 1.18. The same scenario is used to characterize the 3x1 array.

The impact of crosstalk can be directly measured by ΔA_{RX}, defined as:

$$\Delta A_{RX} = |\Delta V_{RX} - \Delta V_{RX_C}| \tag{1.3}$$

where ΔV_{RX} is the received voltage for the crosstalk configuration while ΔV_{RX_C} is the value simulated when $S \to \infty$. ΔA_{RX} increases as the neighboring electrodes are brought closer together: Fig. 1.19 shows the relation-

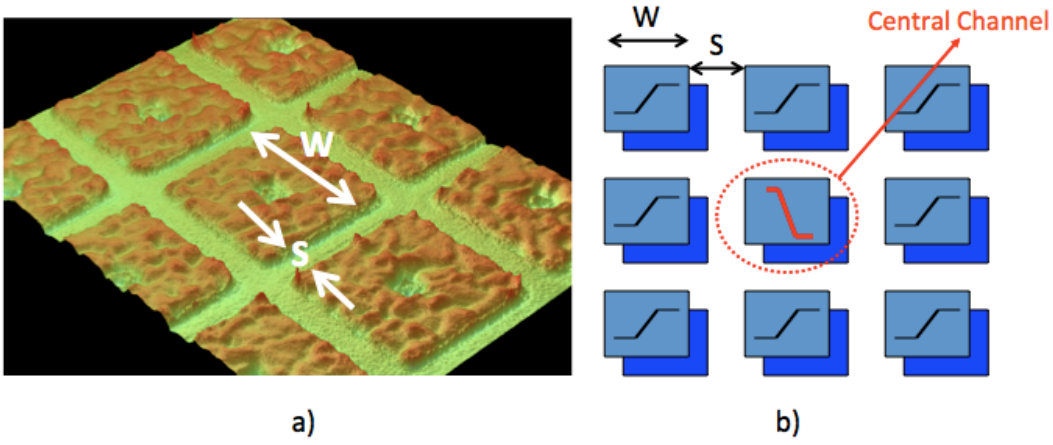


Figure 1.17: a) 3x3 array captured by the profilometer, b) simulation setup for crosstalk analysis in the 3x3 array.

ship between the electrode spacing and ΔA_{RX} for the 3x1 array and the 3x3 matrix in worst and best cases. In Fig. 1.20 the propagation time tp averaged between tp_{rise} and tp_{fall} is shown for the 3x1 and the 3x3 arrays normalized to the single channel values reported in Table 1.5, as a function of electrode spacing. The propagation time increases due to crosstalk for decreasing S. In the worst case scenario, the 3x3 matrix does not operate correctly when inter-electrode spacing is below $3\mu m$. Fig. 1.21 sketches dynamic energy (E_{dyn}) as a function of electrode spacing. Dynamic energy consumption increases as the electrodes are brought closer together because the total parasitic capacitance in the receiving node is increased and therefore a larger capacitance is charged, leading to greater power consumption.

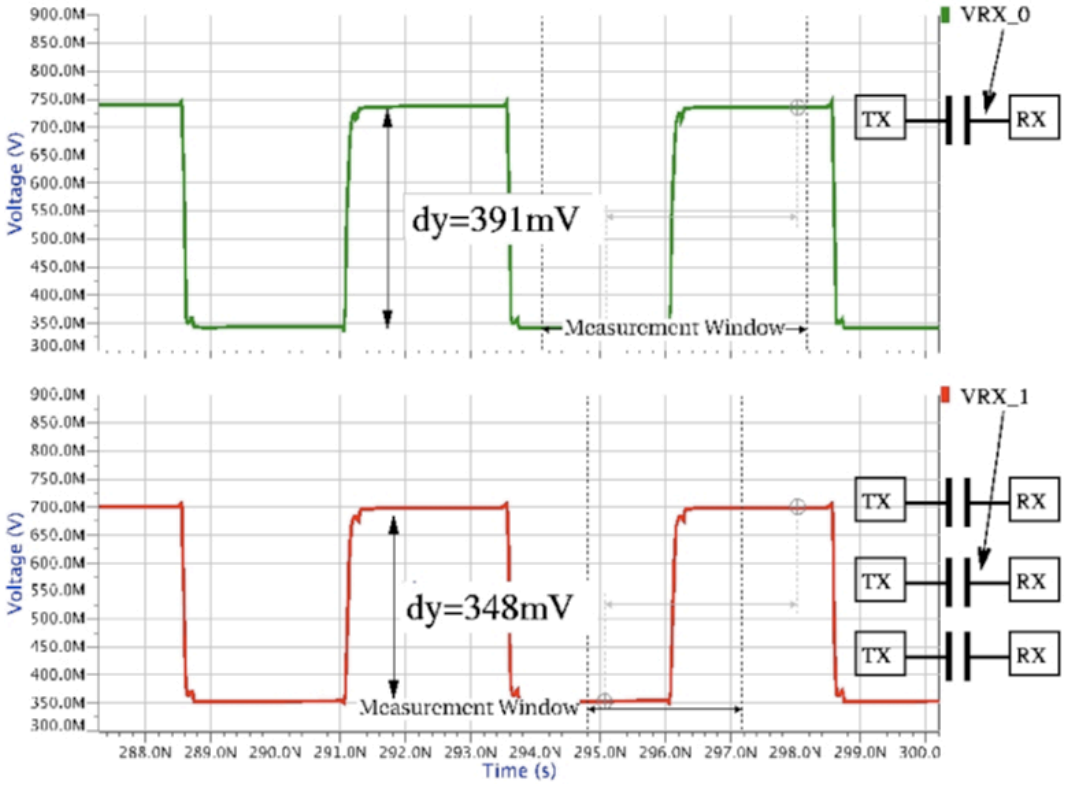


Figure 1.18: Crosstalk effects: (top waveform) ΔV_{RX} is shown for a single channel (ΔV_{RX} =391mV) and (bottom waveform) for the central electrode in the 3x1 array (ΔV_{RX} =348mV).

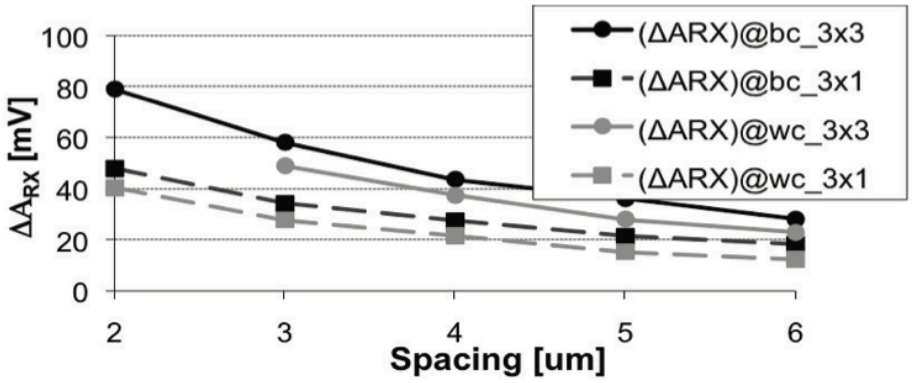


Figure 1.19: ΔA_{RX} as a function of electrodes spacing in the 3x1 and 3x3 arrays in worst and best cases.

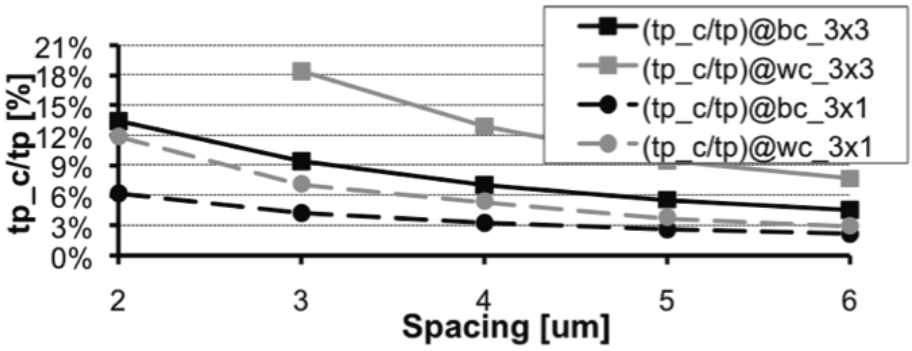


Figure 1.20: Propagation time as a function of electrode spacing in the 3x1 and 3x3 arrays in worst and best cases.

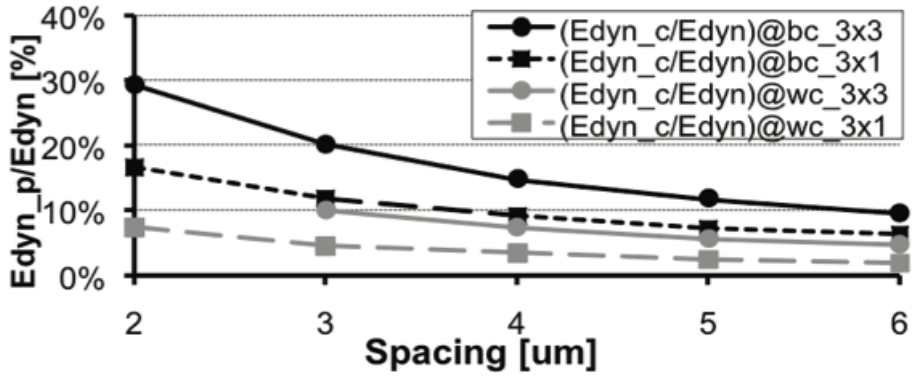


Figure 1.21: Dynamic energy as a function of electrode spacing in the 3x1 and 3x3 arrays in worst and best cases.

	Worst case	Best case
tp_{fall}	665	248
tp_{rise}	510	205
E_{dyn}	40.3	52
ΔV_{RX}	266	373

Table 1.6: Channel characterization for the 3x1 case (W=15μm, S=5μm).

1.1.4 Memory interface application

A high-speed memory-to-processor interface based on capacitive coupling was designed as an example application with the aid of the presented characterization flow, in a standard 90nm CMOS process as a collaboration between STMicroelectronics and the University of Bologna[34]. The author has been responsible for the modeling and characterization of the capacitive links. The 3D system is assembled in a die-to-die fashion and power is delivered through wire bonding [24]. The interface comprises 128 channels running at 250 MHz achieving a bandwidth of 32 Gbit/sec. This 3D memory interface has been integrated in a System-on-a-Chip based on a standard ARM9 platform, as shown in Fig. 1.22. The system is composed of an ARM926-EJS RISC core, with 16+16KByte on-chip instruction and data memory, a 32-bit AMBA Bus sub-system with a parallel port and a JTAG interface for testing purposes. The 3D memory sub-system is interfaced to the AMBA Bus as a standard memory. The wireless interface is arranged in four linear arrays of 32 elements, each of them composed of TX/RX circuits and connected to a 15x15 μm^2 electrode placed linearly one next to the other. Table 1.6 reports the simulation results for the pitch selected.

In the application we are dealing with, the ARM processor limits the maximum operating frequency to 250 MHz. The characterization results for the 3x1 array report a worst case propagation time of 802ps for $2\mu m$ spacing, which translates into an operating frequency of approximately 1.2 GHz. On the other hand, the memory form factor imposes a $5\mu m$ electrode spacing so that the interconnect propagation delay specifications are fulfilled with an ample margin. Moreover, the imposed choice of $5\mu m$

	Power consumption $[mW/Gbps]$	**Bandwidth per area unit** $[Mbit/sec/\mu m^2$
Rambus 90nm [35]	2.2	0.02
DDR1-400-90nm [36]	10.4	0.055
DDR2-800-250nm[37]	7.3	0.085
Capacitive coupling[34]	0.035	0.64
Inductive coupling[38]	1	0.007

Table 1.7: Memory interface comparison.

spacing results in less dynamic power consumption than with $2\mu m$ spacing. The measurement of this AC interconnection when a pseudorandom signal is applied as input in chip 1 and the relative output in chip 2 is shown in Fig. 1.24. Table 1.7 shows a brief comparison with other state-of-the-art memory interfaces. As can be seen, capacitive coupling provides a higher bandwidth per area unit, with smaller power consumption. Fig. 1.23 shows a die photograph.

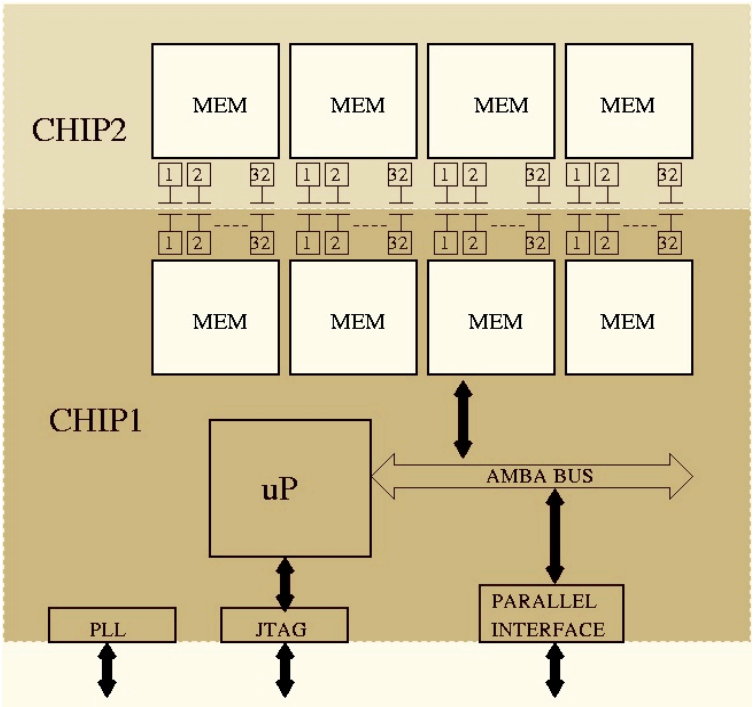


Figure 1.22: Block diagram of 3D memory interface.

1.1.5 Discussion

In the previous chapters the key features of chip-to-chip communication based on capacitive coupling have been highlighted. It was shown how

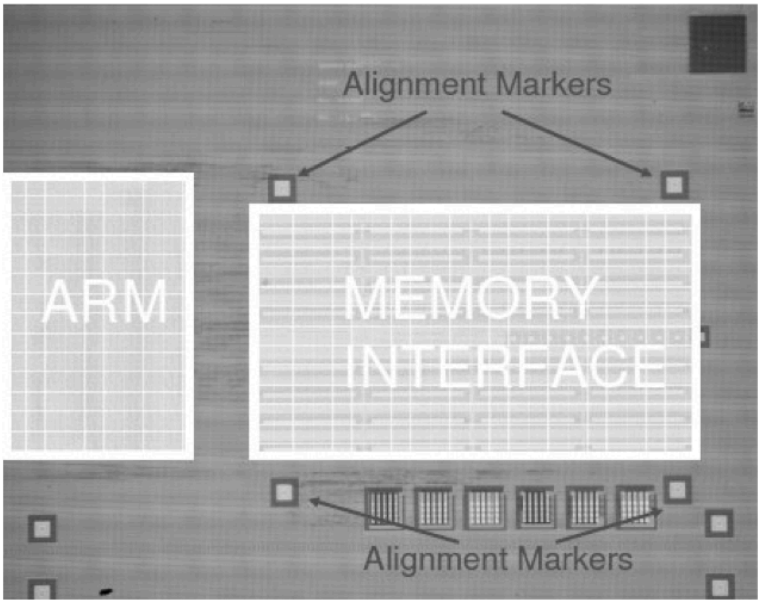


Figure 1.23: Die photograph.

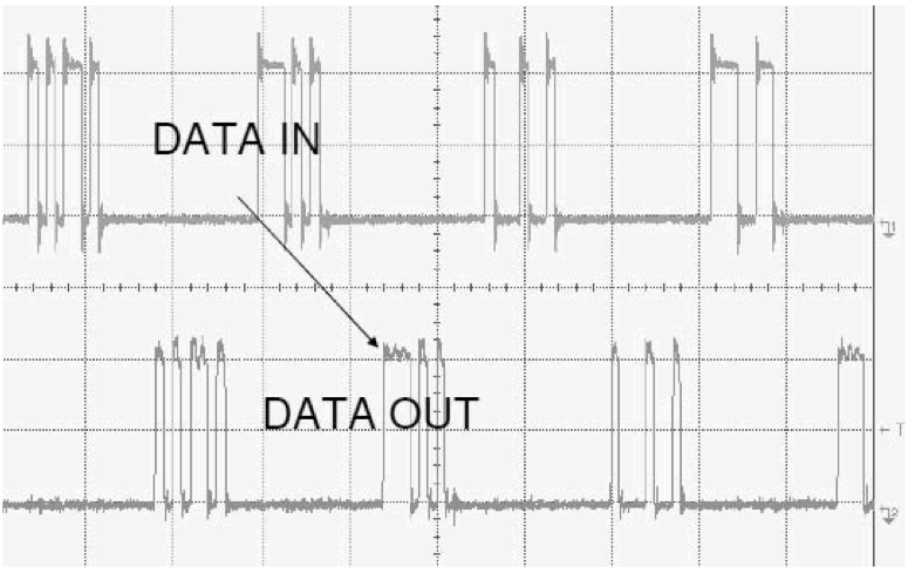


Figure 1.24: Measurement waveforms of test structures with pseudorandom input.

this technology can boost memory-to-processor interface performance in terms of power, speed and also allows transmission of analog data. Nevertheless there are still open issues which need to be investigated in depth to make this a marketable technology. The major issue for 3D contactless technology is power transfer. Circuits can be designed to transfer power between dies capacitively based on charge pumps [39]. Even if this can be done in low-power applications as in [40], this solution is not feasible for standard logic or memory through the AC interface, and DC connections must be implemented to provide power as in the two assembly technologies described in paragraph 1.1.2. The limiting factor for 3D vertical charge pumps is related to the area required for the energy transfer. The energy that can be accumulated in a 3D capacitor is proportional to the capacitor value, for a parallel plate capacitor proportional to the plates areas. As the energy requirements for the stacked chip increase, the area requirements become unbearable. Another open issue is related to the electrical characterization of the communication channel. As shown in paragraph 1.1.3 we have carried out extensive work to develop a characterization flow with higher accuracy and higher compatibility with the standard CAD design flow. This approach allows one to set channel layout parameters such as pitch and electrode widths according to feasibility and performance of communication and then use it as a constrained macro in a digital flow. With the proposed flow crosstalk effects and attenuation are correctly evaluated with respect to the electrode geometric configuration. Finally, thermal effects must be studied to achieve a thermal-aware design [10, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63].

1.2 Wireless wafer probing

The testing of semiconductors is a growing problem in the very large scale integrated circuits manufacture industry, because of its increasing costs and challenges. As the More- than-Moore approach continues to gain momentum, Systems-in-a-Package (SiP) and Systems-on-a-Chip (SoC) are

emerging approaches to multi-die integration as explained in paragraph 1.1. It is hence crucial to discard faulty dies before packaging, especially when assembling SiPs, where known good dies (KGD) must be identified in order to maximize the yield of the whole system. KGD sorting is performed through wafer probing: at this phase the I/O pads are contacted through cantilever or vertical probes and tested via automatic test equipment (ATE).

In the case of a SiP this procedure should be done for every building block (i.e. memory, logic), which could be fabricated by different suppliers. Nowadays SiPs can be vertically assembled through the combined use of Through-Silicon-Vias (TSV) and micro bumps. Testing this kind of vertical interconnections is currently a challenge due to their sizes and pitches [64]. Up to now the cost of wafer testing has been dominated by ATEs, but the cost of the interface is rising and its current trend shows that it will be higher than the ATE cost in the short term [65].

1.2.1 Contact wafer probing issues

Interfacing dies on a wafer is a complicated matter, mainly for geometry reasons. Custom probe cards must be designed for each design. The pitch for wire-bonded I/O pads is already below $30\mu m$ [65] and testing is posing a limit to the minimum pad size, as the probes cannot keep up with the scaling trend. Moreover, direct contact probes can cause severe damage to the pads, as over-travelling is required to establish an acceptable electrical connection. The probes themselves are also subject to damage and they need to be cleaned and replaced regularly, increasing test times and costs. Parallelism of testing is also limited by probe card technology, either in terms of the total number of accessed pads and dies or maximum testing frequency. Parallelism is not only limited by the required pitch, but also by the necessary force required to establish the electrical connection for multiple pads. A force of 4g [66] should be exerted on each pad, meaning that an overall force of 0.8 tons is needed for a wafer of 2000 chips with 100 pads each.

1.2.2 Non-contact approach benefits

Techniques based on contactless wafer probing were recently proposed [67] in order to avoid pad damage and to reduce the total force. As distribution of power supply still requires contact pads, the actual reduction of the force depends on the ratio between the number of I/O signal pads and the number of supply pads. Among contactless technologies, different approaches have emerged based on either capacitive [66, 68] or inductive coupling [69, 70, 71, 72] or on optical interfaces [67]. The latter, though, has the disadvantage of requiring extra technology steps added to a standard CMOS process. Inductive and capacitive coupling on the other hand are fully CMOS process compatible. Moreover, in capacitive coupling the same metal pads used for standard I/O purposes can be used as the on die electrode for wireless communication, while in inductive coupling a dedicated antenna must be designed. Capacitive coupling is characterized by one single connection to the probe pad as opposed to the two necessary for a dipole antenna. There is an advantage for inductive communication in terms of communication range, i.e. the less severe requirement on the distance between the probe needle and the dies pad, with respect to the capacitive one; however the advantage of keeping the pad metallization identical to the standard I/O case justifies the capacitive approach. Circuits for 3D inter-chip communication based on capacitive coupling have been proposed [13, 34, 73, 74], and have been demonstrated to be effective with electrodes sized below $10\mu m$, as detailed in paragraph 1.1. These sizes make this approach interesting for TSVs [64] or micro-bumps testing. The wafer-level testing platform based on capacitive coupling [66, 68] exploits the same communication scheme: an interposed layer, with electrodes designed to communicate face-to-face with the dies, is placed between the probe card and the wafer. A dedicated non-contact test-interface must be added to the DUT circuit to allow the testing procedure; in this block receivers specified to the capacitive communication are designed. Instead, in our work the modification of a standard I/O pad of a digital library to add the capability of a contactless testing, while maintaining the

feature of the original pad of allowing direct (wired bonded) contact is discussed. In addition, we assume that the testing platform is based on a probe card with cantilever needles and it does not require any interposer layer.

1.2.3 Test-chip

Wireless communication based on capacitive coupling is discussed extensively in paragraph 1.1 for chip-to-chip communication. In the case of capacitive communication between a probe card and a chip, we introduce a similar attenuation factor to that presented in equation 1.1. In this case, again due to the voltage capacitance partition principle, as sketched in Fig. 1.25, where C_C is the capacitance between needle and pad, while C_{NEEDLE} is the needle parasitic capacitance and C_{PAD} the pad parasitic capacitance. When a signal is transferred through such a bi-directional capacitive interface it is attenuated of a factor $H_{IN(OUT)}$. As it is shown in 1.4 the attenuation factor $H_{IN(OUT)}$ is related to the coupling capacitance C_C and the parasitic capacitance on the receiving node, which in case of an input (output) transition to (from) the pad, is represented by the pad (needle) parasitic capacitance $C_{PAD}(C_{NEEDLE})$.

$$H_{IN(OUT)} = \frac{C_C}{C_C + C_{PAD(NEEDLE)}} \tag{1.4}$$

The value of C_C (in the femtoFarad range) is orders of magnitude smaller

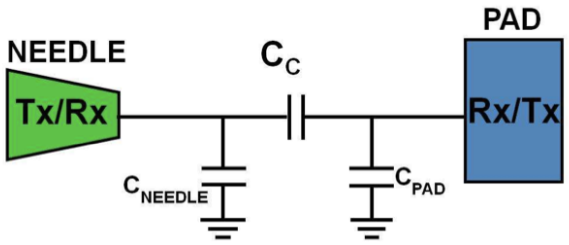


Figure 1.25: Model of a wireless bidirectional capacitive interconnection between needle and pad.

than the values of C_{PAD} (about 1 pF) and C_{NEEDLE} (a few picoFarads). For this reason the receiver should be able to detect very small signal voltage variations. A test chip has been designed in a CMOS 90 nm STM technology with 1.2 V of core supply voltage and 5 V power supply for I/O buffer (Vdde). The fabricated test chip has not been specifically optimized for high frequencies and low power applications, as this study had the main goal of evaluating the feasibility of wireless probing methodology combined with standard direct contact testing. In the following, it is first described the design of a pad suitable only for input capacitive coupling and then the customization of a standard I/O pad available in the digital 90 nm standard-cell library in order to operate both in contact and contactless communication. As it was pointed out, the design is critical due to the small voltage signal received; for this reason the circuit behavior has been characterized at corner analysis (technology, voltage and temperature variation) and post-layout simulations [26].

Input wireless stand alone pad

In this paragraph the design of an input wireless Stand Alone (SA) pad is described. It is composed of a receiver and a top metal layer, granting both direct (wired) contact and contactless testing capabilities since it acts as the electrode for capacitive coupling.

The receiver schematic is sketched in Fig. 1.26. It works in asyn-

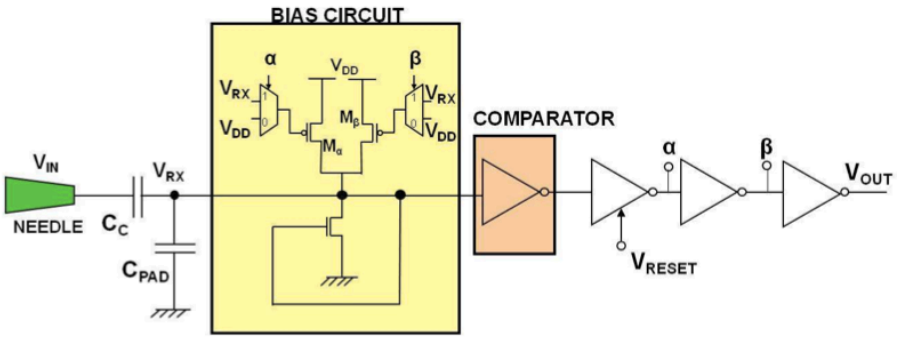


Figure 1.26: Receiver schematic for a contactless input pad.

chronous mode switching when a signal edge transition is detected. The first stage is composed of a bias circuit that biases the receiver node RX above/below the threshold voltage of the comparator depending on the previous signal edge transition. For instance, if the transmitted signal is a rising (falling) edge, after the receiver has detected the signal, the bias circuit fixes the receiver node above (below) the threshold voltage thanks to the output feedback through signals α and β. In this way the receiver is ready to detect the opposite transition. A buffer chain restores the output signal, as shown in Fig. 1.26. This circuit topology allows for the detection of very small voltage variations when the receiver node is biased close enough to the comparator threshold voltage: the receiver sensitivity, i.e. the minimum voltage transition at the RX input node ($V_{RX_{min}}$) which is correctly detected and amplified, is about 80 mV. V_{max}, the internal core power supply, is 1.2 V. The occupation area is 9.67x$11.45\mu m^2$ while the top aluminum layer is 131x$63\mu m^2$. The parasitic capacitance C_{PAD} is 84 fF that is a very low value due to under-sizing of ESD protection circuit, and the maximum operating frequency is 200 MHz with an output capacitive load of 0.5pF. The static power consumption is $13.5\mu W$, while the dynamic energy is $63fJ/bit$.

I/O direct contact and contactless pad (IO/W pad)

For both contact and contactless communication, the scheme in Fig. 1.26 must be modified. First of all, ESD circuit protections must be included in order to prevent accidental breaks. In addition I/O capability is a common requirement. For this reason a standard I/O pad from ST Microelectronics has been modified in order to implement I/O contactless testing features while still being able to operate on direct contact. This allows the pad to be tested either wirelessly or with direct contact at wafer level before the assembly. In Fig. 1.27 the block diagram for direct contact and contactless I/O is drawn. The input contactless receiver scheme sketched in Fig. 1.26 has been appended inside the standard I/O thanks to its small occupation area, hence holding the same pad dimensions as it can be seen in Fig. 1.28.

A selection signal SEL has been added to switch its operation mode from direct contact to contactless. The wireless output functionality works using the standard output buffer already implemented in the I/O circuitry. Due to the ESD protection and the output driver, the parasitic capacitance C_{PAD} 1.4 is higher than the previous stand-alone receiver (paragraph 1.2.3) and it is around 470 fF. The area is determined by the top aluminum layer and is $131\text{x}63\mu m^2$ as in the standard I/O pad. On the contrary of the SA pad, high voltage (5 V) transistors have been used in the contactless receiver, because the receiving node RX is shared with the output driver pad and the top aluminum layer. This cause the receiver sensitivity to increase to around 200 mV while the maximum output signal frequency is constrained by the standard output buffer at 4 MHz with a 25 pF capacitive load. The static power consumption is $46.5\mu W$, while the dynamic

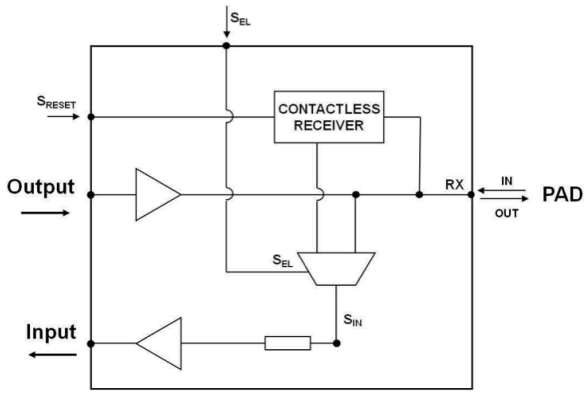


Figure 1.27: IO/W pad schematic for direct contact and contactless testing.

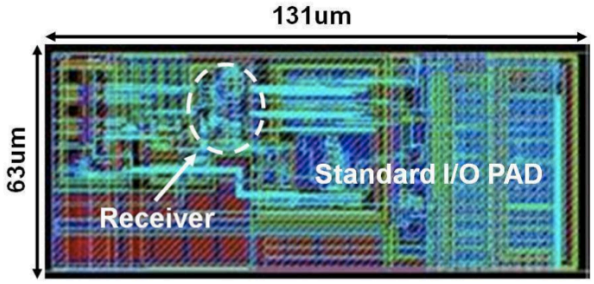


Figure 1.28: IO/W pad layout for direct contact and contactless testing.

energy is $1.1pJ/bit$.

Padframe structure

The test chip photo is shown in Fig. 1.29. The basic structure sketched in Fig. 1.30 including 10 pads is replicated where:

- Pads 6 to 10 are common to all structures and dedicated to supply voltage.
- Pad 5 is common to all structures and is used to reset the wireless receiver.
- Pad1 and pad 3 are of type IO/W (Fig. 1.27) or input SA of Fig. 1.26. Different configurations are designed in order to prove the bidirectional capability of IO/W pads.
- Pad 2 and pad 4 are of type IO/W (Fig. 1.27). They work for direct contact testing either as input or output, configurable at design time.

In Fig. 1.30 the contact (C) and wireless (W) functionality is highlighted according to the probe card design, as it is explained in paragraph 1.2.4. Pad pitch and width are $101\mu m$ and $63\mu m$ respectively, as shown in Fig. 1.29.

1.2.4 Probe card and modeling

A probe card dedicated to the test chip has been designed and is shown in Fig. 1.31. The test structure comprises 10 pads, as illustrated in the previous paragraph. In particular, there are 2 wireless cantilever needles, as shown in Fig. 1.32, while the remaining ones are designed for direct contact. The edges of the wireless needles are flattened and with a diameter of $52\mu m$, in order to maximize the capacitive coupling between pad and probe. Direct contact and contactless needles have a slightly different length of about $60\mu m$, as it can be seen in the figure.

In order to establish an acceptable electrical connection of the contact needles, an over-travel of about $50\mu m$ occurs, therefore the nominal distance between the pad and the wireless needle is around $10\mu m$. Using a standard probe station combined with a micro-positioner and a micrometer it is possible to control the distance between probe and DUT with an accuracy of a few microns. A constraint in the maximum between z vari-

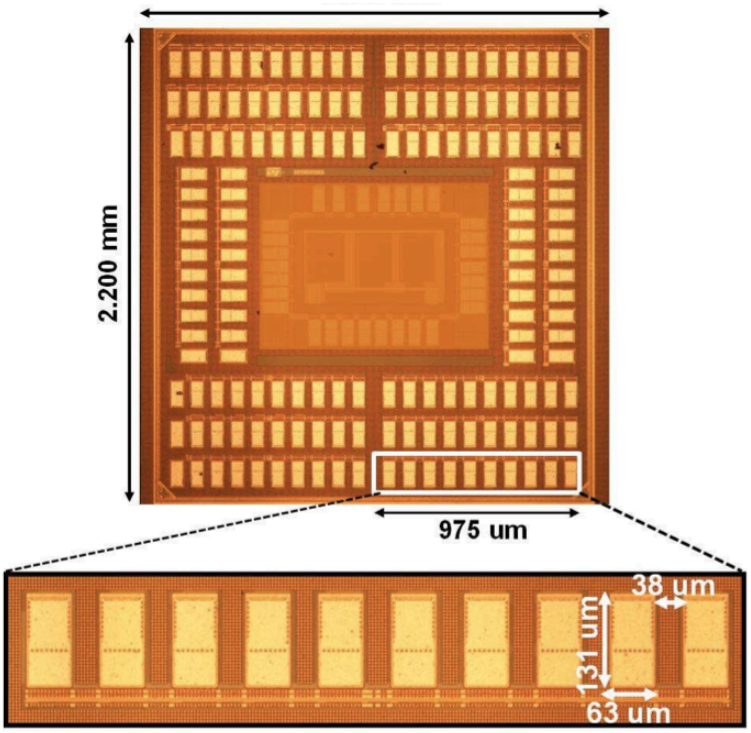


Figure 1.29: Chip microphotograph layout and test block with 10 pads.

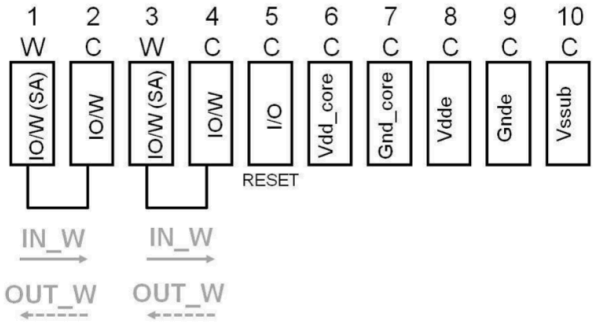


Figure 1.30: Block diagram for a 10 pad test structure.

ation of the wireless needles must be considered in the probe card design. In the actual implementation a maximum difference of $7\mu m$ has been measured by a profilometer. A 3D model of the probe card has been sketched with Ansoft software [75] as shown in Fig. 1.33. The model was used to perform electromagnetic (EM) simulations, in order to realistically evaluate the interaction between the probe card (needles and PCB interconnections) and the chip.

Electromagnetic simulations are used to extract admittance parameters, which are used to create an equivalent lumped element model (see Fig. 1.34). The needles equivalent resistance is negligible and the following analytical equations 1.5 describe the lumped model:

Figure 1.31: Probe card: top and bottom views.

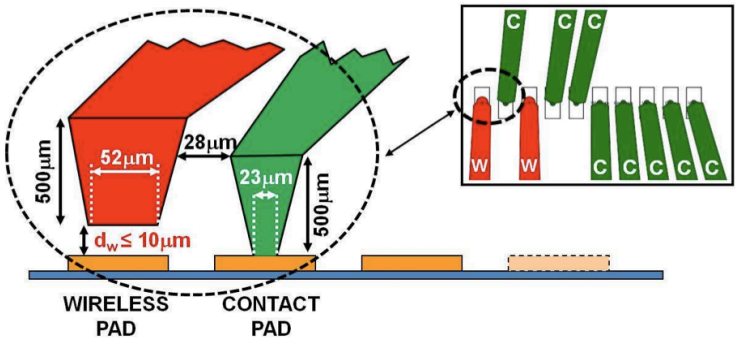


Figure 1.32: Probe Card configuration after a $50\mu m$ overtravel.

$$
\begin{aligned}
Y_{11}(s) &= \frac{(C_C + C_{NEEDLE})\, s}{1 + L_{NEEDLE}\,(C_C + C_{NEEDLE})\, s^2} \\
Y_{12}(s) &= \frac{C_C s}{1 + L_{NEEDLE}\,(C_C + C_{NEEDLE})\, s^2}
\end{aligned} \tag{1.5}
$$

Y_{11} and Y_{12} parameters vary with frequency and are shown in the graph in Fig. 1.34 for a distance of $2\mu m$ from the probe to the DUT. At frequencies lower than 1 GHz the behavior is approximately linear hence in this frequency range it is possible to extract the parameters for the equivalent lumped element model in Fig. 1.34 neglecting the effect of L_{NEEDLE} and using the following approximated equations where it is also assumed $C_{NEEDLE} \gg C_C$:

$$
\begin{aligned}
C_{NEEDLE} &= \frac{Im\,[Y_{11}(j\omega)]}{\omega} = 5.2pF \\
C_C &= \frac{Im\,[Y_{12}(j\omega)]}{\omega} = 13pF
\end{aligned} \tag{1.6}
$$

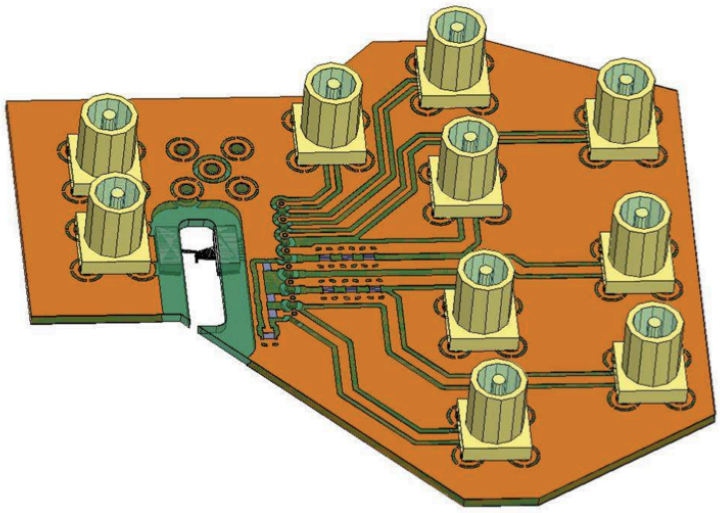


Figure 1.33: 3D model of the probe card.

The equivalent inductance L_{NEEDLE} is extracted from the resonance frequency at 1.7 GHz and is around 1.7 nH. The value of C_C extracted from the simulation is higher than that derived from a preliminary calculation considering a parallel plate capacitor model and resulting in a C_C of about 9 fF. This difference can be explained considering that the simulator takes also into account the added fringing electric field lines between the pad area and the sides of the needle. The result of 3D EM simulation has been compared with simulation of the lumped elements circuit showing good agreement in the frequency range of interest.

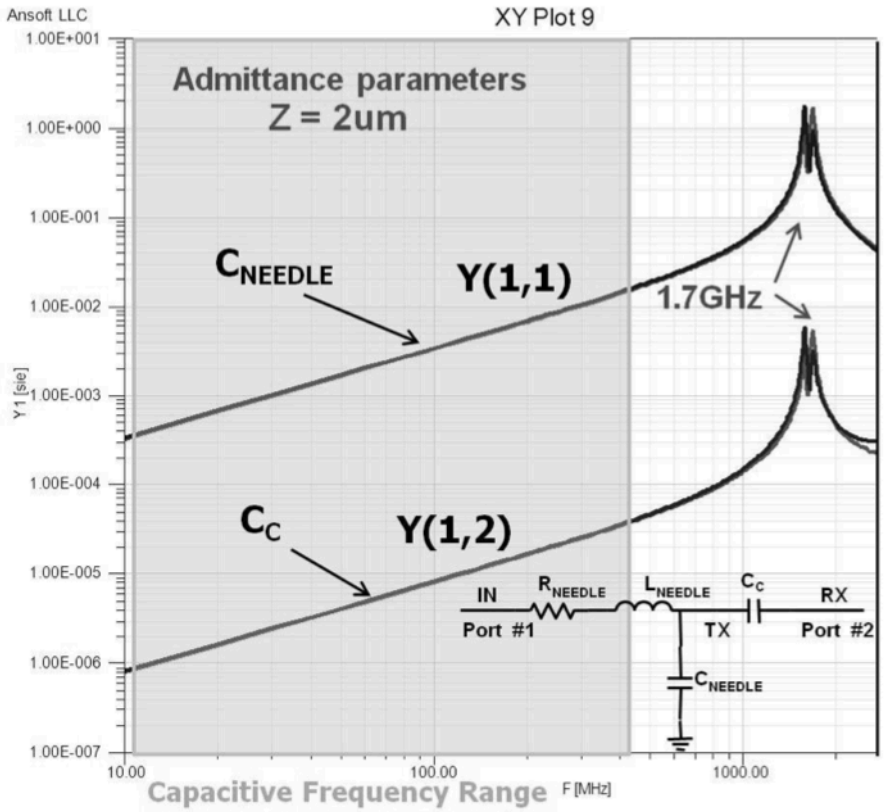


Figure 1.34: Admittance parameters varying with frequency and equivalent lumped element model of probe card.

1.2.5 Experimental results

In this paragraph preliminary experimental results are presented in order to demonstrate the feasibility of wireless probing by capacitive coupling.

Input and output direct contact testing

IO/W pad has been initially tested for direct contact functionality. Referring to Fig. 1.32, this mode of operation requires an over travel larger than $60\mu m$. The input signal at pad 1 and output signal at pad 2 are shown in Fig. 1.35. As it can be seen, the IO/W pad correctly works.

Input wireless testing

In this paragraph the input wireless functionality of the SA and IO/W pads is illustrated. The test setup is shown in Fig. 1.36. The procedure starts with a direct contact test with the wireless needle touching the pad as shown in the previous paragraph. It is possible to lift up the needle from the DUT using the micro-positioner with a resolution step of a few microns. In order to guarantee the wireless communication it is necessary

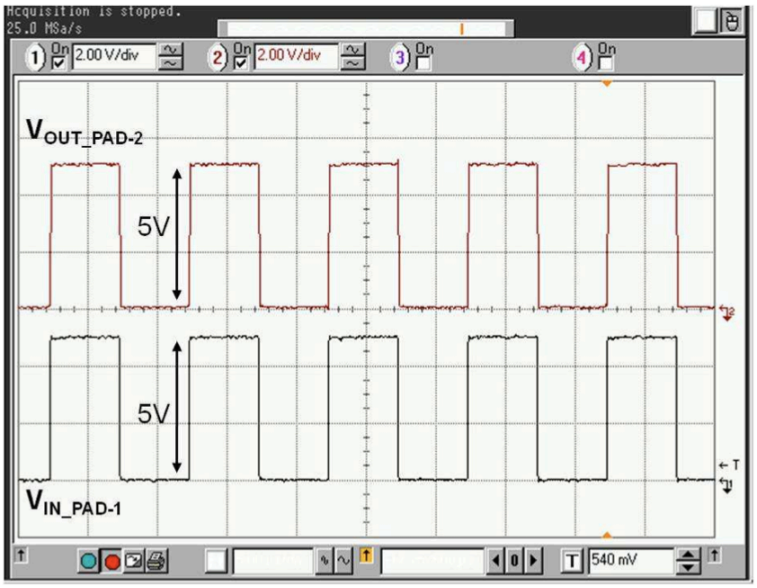


Figure 1.35: Input and output signals of IO/W pads.

to increase the peak-to- peak input signal voltage generated by a function generator. Both the SA and the IO/W pads have been characterized. SA can communicate at longer distances due to the higher sensitivity of the receiver and to the lower parasitic capacitance (C_{PAD}). In Fig. 1.37 the measured data (continuous line) are compared with the theoretical values (dashed line) computed using the following equation 1.7:

$$V_{pp_{IN}} \geq V_{RX_{min}} \frac{C_C + C_{PAD}}{C_C} \tag{1.7}$$

where $V_{pp_{IN}}$ is the minimum peak-to-peak input signal voltage. The experimental data fits very well with the theoretical function 1.7.

Output Wireless Testing

The output signal varies between Vdde (5 V) and Gnd. In order to limit the parasitic capacitance from the probe card to the instrumentation, an

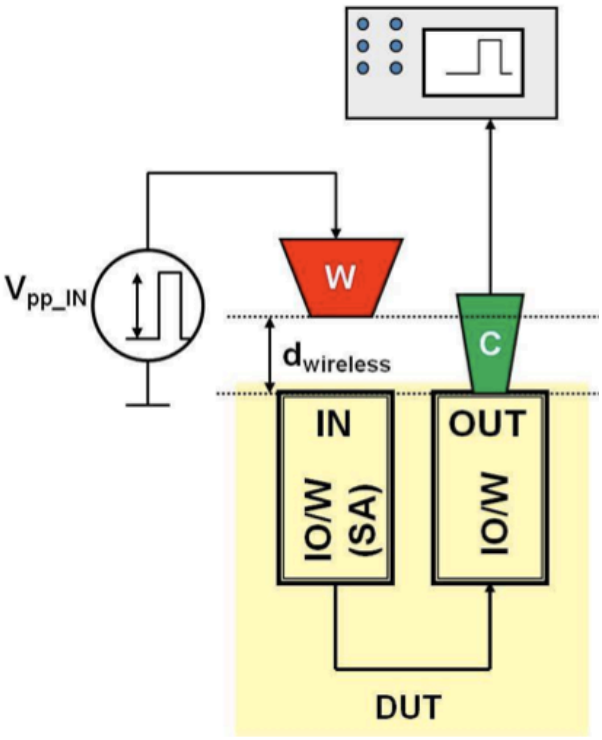


Figure 1.36: Measurement setup for input wireless testing mode.

oscilloscope probe with a parasitic capacitance of 9 pF has been used (see Fig. 1.38). The total parasitic capacitance, given by the sum of C_{NEEDLE} and the oscilloscope input probe is around 14.2 pF. Fig. 1.39 shows the output signal detected at different distances between needle and pad. The signal is about 5.84 mV for a communication distance of $2\mu m$. From equation 1.4, with C_C = 13 fF the estimate output voltage amplitude is 4.5 mV, while 4.57 mV is computed by 3D EM simulation in good agreement with the measured value. In the proposed implementation a 5V power supply has been used. As the CMOS scaling trend imposes smaller voltages, the received signal decreases and hence an active probe card will be needed in order to amplify the signal as close as possible to the needle to reduce the total parasitic capacitance and therefore the voltage attenuation (equation 1.4).

Cross-talk analysis

In order to evaluate the effects of cross-talking between the needles of probe 1 and 2 (which are designed in opposite direction, see Fig. 1.32), the measurement described in Fig. 1.38 has been carried out also increasing

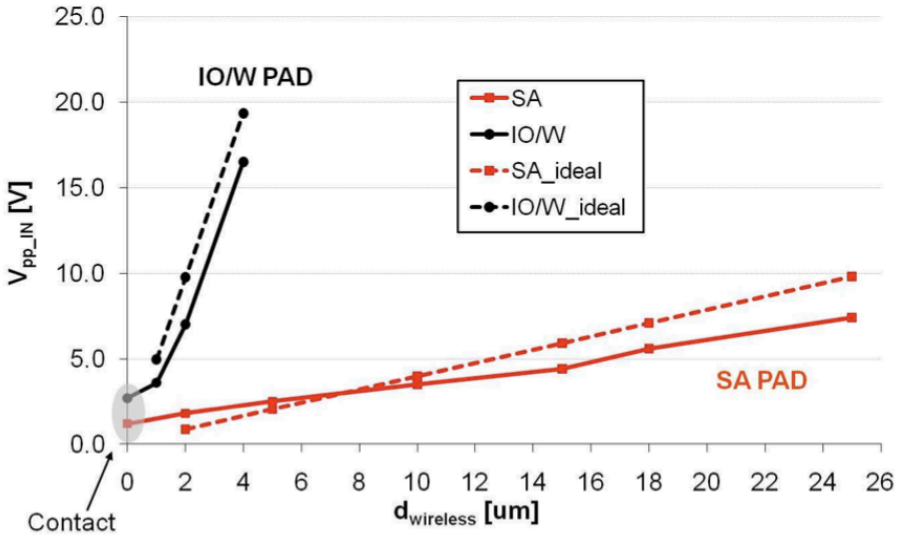


Figure 1.37: Minimum peak-to-peak input voltage as a function of distance for input wireless testing SA and IO/W pads.

the distance between probe and DUT up to values that do not guarantee anymore the input contact connection (i.e. with no communication be-

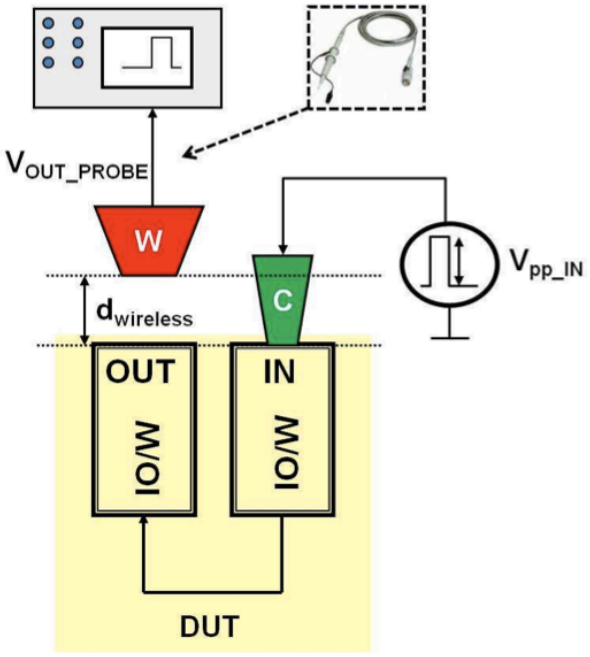


Figure 1.38: Measurement setup for output wireless testing mode.

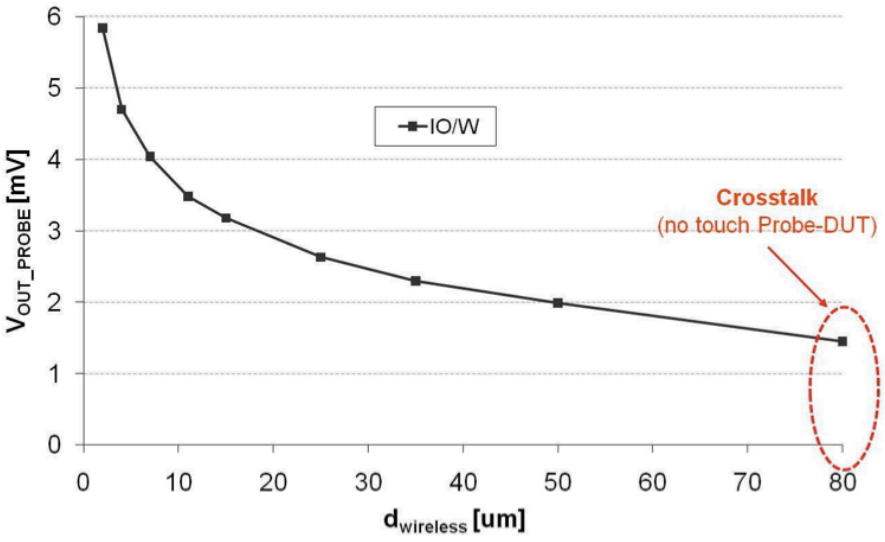


Figure 1.39: Output voltage as a function of distance for the output wireless testing of IO/W pads.

tween the probes through the circuit). For a 5 V input signal, the measured amplitude due to the coupling between the needles is 1.5 mV, which is around 25% of the received test signal (5.84 mV) measured for a $2\mu m$ communication distance (see Fig. 1.39). From this value it can be deduced that the cross-talking capacitance is about 4 fF. Different values are obtained with different needles design and in particular using vertical needles. For a given probe technology, the cross-talk effects need to be considered in order to evaluate layout constraints in terms of minimum pitches and/or distribution of input and output pads on the design chip. In this example, the input pads could be placed one next to the other because the cross-talk effect is negligible in comparison to the signal. The same situation applies to the output pads. A different scenario to be considered would be the placement of an input pad next to an output pad. This configuration is critical because the high voltage input needle can generate a significant cross-talk effect to its neighbour. As a pad-frame design guide, a bias or a supply pad should be placed between two adjacent input and output pads in order to create a ground shield to reduce cross-talk.

1.2.6 Discussion

An I/O pad for both direct contact and contactless testing featuring the same occupation area of a traditional pad from ST library has been presented. Moreover an input only pad has been designed to function over larger communication distances. Measures have been carried out using a dedicated cantilever probe card. Experimental results validating the wireless probing by capacitive coupling have been shown. The main issue with capacitive coupling wireless testing is related to the attenuation of the signal received by the probe from the output pad. This requires amplifying the signal on the probe card as close as possible to the needle, in order to reduce parasitic capacitances. For this reason, a new probe card with active circuitry capable of amplifying the received signal is currently under study. Moreover, different probe card technologies are currently being investigated, as vertical needles could translate into easier industrialization

and higher parallelism.

Chapter 2

Active electrodes for simultaneous EEG and EIT

2.1 Brain Imaging

Brain imaging consists of measuring an aspect of a brain function to understand the relationship between activity in certain brain areas and specific mental functions. The process has applications in heterogeneous fields, such as the study of cognitive processes, brain related pathologies and conditions, and the implementation of brain computer interfaces (BCIs).

Many of the most prominence discoveries in cognitive functioning have come from developments in the brain imaging technology in the last two decades. We are now capable of giving answers to questions such as how the sensory input is mapped onto the brain or how do sensory and motor representations interact to guide our "motor action". Also, we can investigate how memory, language and emotions are organized in the human's brain. Imaging explores how functional systems are formed in the physical structure of the brain [1].

Brain pathologies and conditions can benefit from brain imaging as this can be used for localization, and thus relate pathologies to certain specific brain areas. Localization is of primary importance in pathologies such as epilepsy [76], as discovering the epileptic foci can help with drug administration and surgery in the most critical cases.

One of the most interesting and recent fields that has found an application for brain imaging has been the development of brain computer interfaces (BCIs). These are communication systems that allow the human brain to interface with an external device. BCIs can serve and assist people with sensory or motor disabilities, providing a way to overcome such problems.

Brain imaging technologies can be distinguished in two groups:

- *electro-magnetic* (EM) based solutions, or anatomical imaging techniques, which measure the changes in the field distribution of an applied external strong electromagnetic field or X-ray. These include (functional) magnetic resonance imaging (f)MRI, X-RAY computerized tomography (CT scanning), positron emission tomography (PET).

- *biopotential* based solutions which rely on the measurements of electric potential, such as electroencephalography (EEG) and electrical impedance tomography (EIT).

In general, the first group of solutions are limited to medical and research environments, as they rely on large and expensive machines. They also allow for a high spatial resolution while suffering from limited temporal resolution. Moreover, they do not allow for continuous monitoring due to the strength of the applied fields, hence they are not a feasible solutions for pathologies such as epilepsy, which are characterized by sporadic random events. For this reason, biopotential based solutions, with their relative portable hardware, can serve better in those situations where portable monitor is needed such as for the epileptic foci localization or BCIs.

2.1.1 Electroencephalography (EEG)

Electroencephalography (EEG) consists in the recording of electrical activity along the scalp, as produced by the firing of neurons within the brain. An example is shown in Fig. 2.1.

The invention of the EEG is attributed to Hans Berger, who was an established researcher on cerebral blood circulation at the University Clinic

for Psychiatry in Jena, Germany. Berger, while an officer in the Prussian Army, received a letter from his sister with the description of a dream, in which he would fall off a horse. It turned out that the officer indeed had fallen off a horse at about the time when the letter was sent. Doctor Berger, once returned to Jena after his military duties, was promoted Chair of the Department of Psychiatry and Neurology in 1919 and focused his career on the study of brain's electrical activity. Berger thought that the electromagnetic forces generated by the human brain could be carried by one individual to another, thus establishing a phenomenon of telepathic

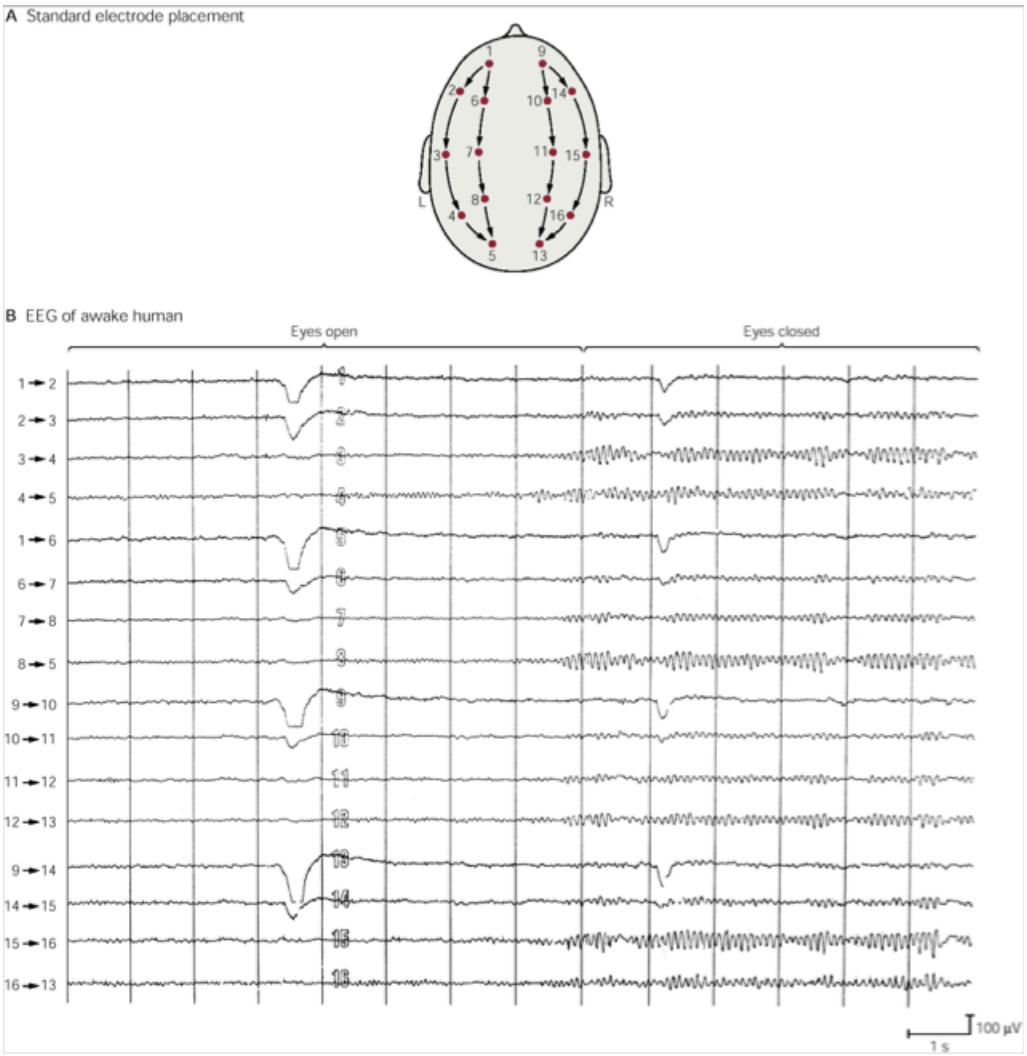


Figure 2.1: Electroencephalography (Source: [1]).

communication.

Berger soon started recording the electrical activity on the human scalp, discovering what he called the alpha and beta rhythms, corresponding to the brain rhythms characterizing an individual with his eyes closed or open. Although he wasn't able to prove his hypothesis of telepathy, he gave birth to EEG, an excellent instrument for the study of the quickly changing brain activity [77].

The potential measurements on the scalp are performed in a differential manner using electrodes, which are most commonly passive, but can include active circuitry as explained in paragraph 2.1.1. These potentials originate from the activity of the neurons in the cerebral cortex, also known as gray matter. The electric field then propagates through the skull to the scalp. Field propagation is limited by the electrical properties of the skull and hence the potential difference are usually in the μV range [78].

In order to find the location and the distribution of the sources the so-called inverse problem must be solved. Unluckily, many different sources configuration can generate the same potentials on the scalp [79], that means that the mathematical problem is ill-posed. This can be solved through different algorithms which rely on different approaches, using different mathematical, biophysical, statistical or anatomical constraints [80, 81].

EEG is a technique that can provide high temporal resolution as the detectable neural activity is concentrated at low frequencies, usually below 30 Hz, although standard clinical EEG should be performed up to 100 Hz [82]. Typical EEG waveforms are localized at specific frequencies, usually referred to as rhythms [77] and are indicative of the patients state (deep/light sleep, awake etc.). These rhythms are usually classified as follows, in increasing frequency order:

- *Delta rhythm*: 0.5-4 Hz.
- *Theta rhythm*: 4-8 Hz
- *Alpha rhythm*: 8-13 Hz
- *Beta rhythm*: 13-30 Hz.

- *Gamma rhythm*: 30-100+ Hz.

An example of brain rhythms is shown in Fig. 2.2.

Active electrodes for EEG

Electrodes are used extensively in health care to record or monitor biopotentials to assess various body functions, as explained in further detail in chapter 3. Several solutions have proposed the integration of low noises high-impedance amplifiers on the electrode [83, 84, 85, 86, 87], and we are presenting here our own as well [88]. Active electrodes have shown the ability of improving signal quality by reducing artifacts related to cable noises and interferences as shown in Fig. 2.3.

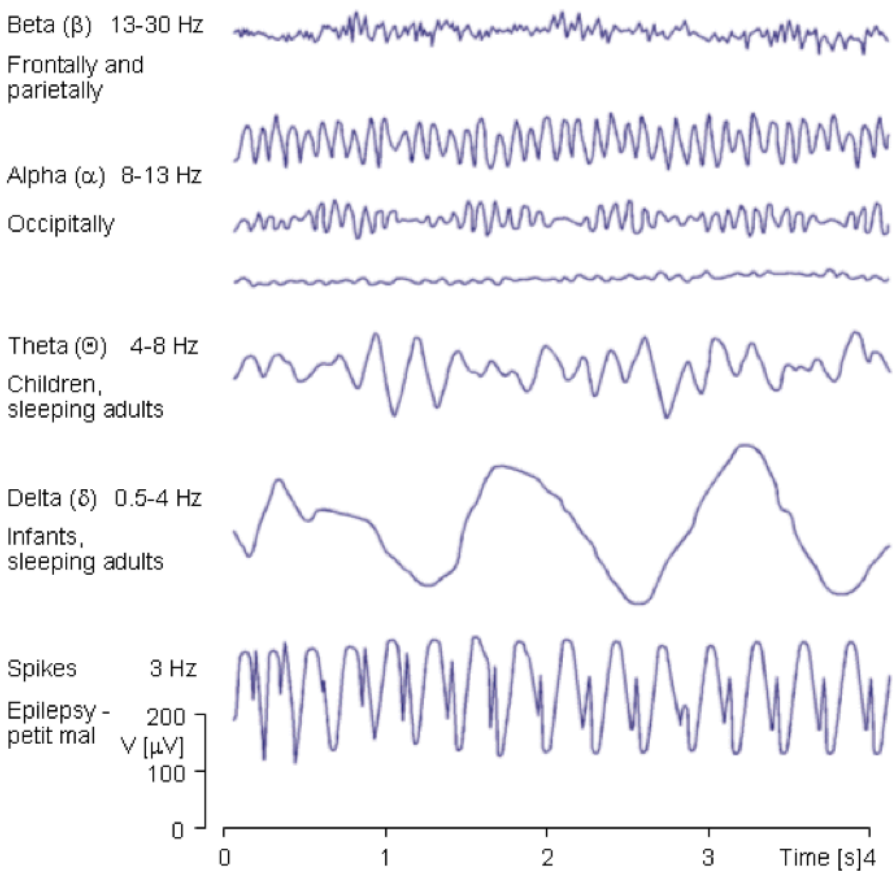


Figure 2.2: EEG rhythms (Source [2]).

2.1.2 Electrical Impedance Tomography (EIT)

Electrical impedance tomography (EIT) is a medical imaging technique which consists in inferring the internal conductivity distribution by measuring surface potentials as a response to injected AC currents. This is again an inverse-problem, similar to the source localization problem in EEG. The basic scheme is shown in Fig. 2.4. A similar technique was initially proposed for geological studies in the 1930s, although known as electrical resistivity tomography (ERT) [89, 90, 91]. In contrast to the medical imaging technique, ERT is performed by injecting direct currents, nevertheless mathematically it is the same inverse problem.

The first published work on impedance images in the medical field, as noted in [92], is the one by Henderson and Webster [93]. In this work, 100 electrodes were placed on one side of the chest, while a single large electrodes serving as ground was placed on the other side. With such setup they were able to produce an image of the tissue, as low conductivity areas in the image were claimed to match with the lungs. Interestingly, the second work in the field of EIT was already related to brain imaging: a system

Figure 2.3: Active electrodes can reduce impact of cable noise and interferences.

for the detection of brain tumors [94]. The authors presented a prototype impedance scanner with two parallel arrays of electrodes immersed in a saline filled tank, which was able to detect impedance changes between the electrode arrays. The very first clinical EIT device, at the time called applied potential tomography (APT), was developed in 1987 and commercialized with the name of Sheffield Mark 1 system [95] by Brian Brown and David Barber at the Department of Medical Physics in Sheffield. The system is still in use in many centers today and is capable of making multiple impedance measurements of an object with 16 electrodes placed around its surface. Since then the system has been used to image lung ventilation [96], cardiac cycles [97], at a rate of 10 images per second. The advantage of an EIT system, when compared to CT and MRI, is related to its lower costs and higher portability. Nevertheless, the EIT never gained widespread clinical acceptance due to its lower spatial resolution when compared to other techniques such as X-rays and ultrasound. For a complete review on EIT please see [92, 98, 81, 99].

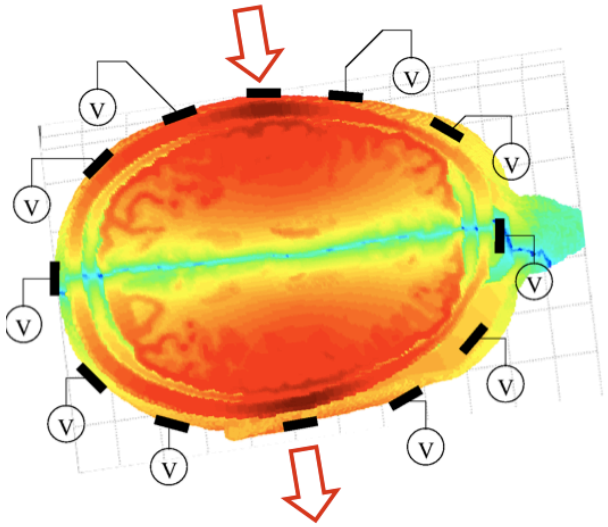


Figure 2.4: Electrical Impedance Tomography.

2.1.3 Simultaneous EEG and EIT

Today, localization of EEG signal sources is an established method for providing low-cost and high-temporal resolution brain activity maps [80]. Nevertheless localization accuracy is greatly influenced by unknown brain, skull and skin conductivities. Conductivities maps can be determined with the use of EIT as explained in paragraph 2.1.2. The two techniques can hence be used in combination, but the use of two separate systems poses some limitations due to bulky hardware and low configurability. Recently we developed an IC directly integrating the EEG and EIT signal acquisition, as well as EIT input current synthesis, along with continuous monitoring of electrode to skin impedance (ESI) [88]. EIT in fact might give a-priori information for the EEG source localization problem and possibly provide complementary information since the physical principle observed is correlated but different from that of EEG [100, 101]. Moreover, continuous monitoring of the electrode to skin impedance (ESI) can provide information on whether the electrode might need to be re-positioned, thus improving artifact removal algorithms. Electrode to skin impedance is treated in greater depth in chapter 3.

The main weakness of active electrodes is related to the increased electrode area, number and weight of cables, which could hence limit the electrode density. We developed two prototypes which will be discussed in details in paragraph 2.3 and 2.4. The active electrode area is small enough to be compatible with high-density integration; moreover, since EEG, EIT and ESI signals share the same output line, the wire number is minimized and only one acquisition channel is required by each electrode which can be continuously configured between two operation modes:

- EIT current injection
- simultaneous EIT potential, EEG and ESI readout.

2.2 System overview

The overall system in which the active electrodes are integrated is shown in Fig. 2.5. The author has been responsible for the development and implementation of the readout circuit design. For this reason the current generators are not presented in depth. Further information can be found in [88].

The acquired EEG and EIT signals are then used for inverse problem solving by state-of-the-art parallelized software [101]. The cable number and electrode area are minimized in the IC design in order to support high density imaging systems ranging from 256 to 512 electrodes. Both IC prototypes require few external components on the PCB and 4 wires (OUT, CLOCK, DATA and ground, see Fig. 2.6) to interface with the back-end.

2.3 First IC Prototype

A schematic for the first prototype is shown in Fig. 2.6. The output line (OUT) is shared between the analog supply AVDD and the three appli-

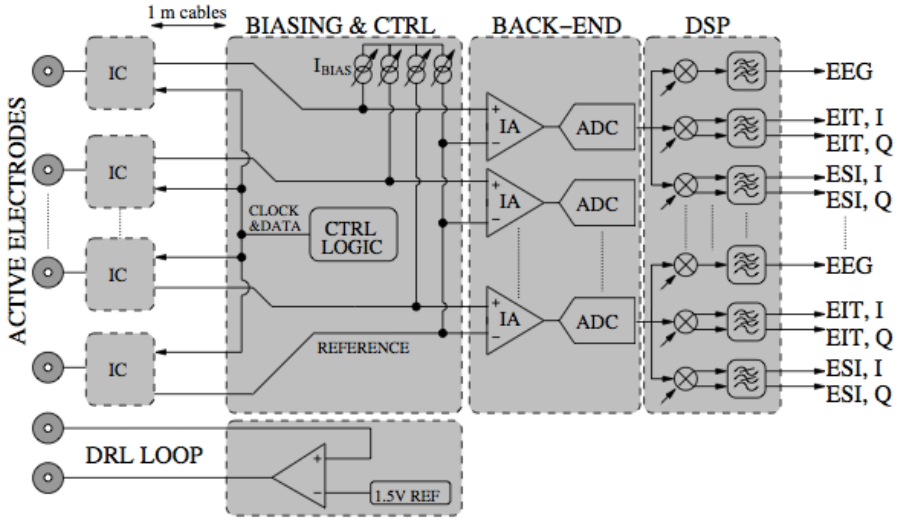


Figure 2.5: Overview of the full system on which active electrode ICs are integrated.

cation readout signals by assigning them different frequency ranges; it is externally biased by a programmable DC current source. The behavior of the IC is programmed via a two-wire digital interface; the power supply for the digital interface (DVDD) is derived from the DATA signal. In order to relax both IC and back-end noise specifications, the low frequency EEG signal is up-converted at a 2 KHz central frequency and the EIT signal is down-converted from high frequency to 4 KHz as explained in paragraph 2.3.1. Final down-conversion to baseband (with quadrature signals for ESI and EIT) and separation of the three signals are not performed until after analog to digital conversion. The active electrode IC is comprised of a readout circuit for the electrode biopotential (composed of two passive mixers and a differential amplifier and detailed in paragraph 2.3.1), a programmable current source injecting EIT square wave currents up to $535\mu A_{pp}$ in steps of $2.1\mu A_{pp}$ at frequency f_{EIT} from 10 KHz to 1 MHz, a current source by which to inject the ESI test current and the digital interface for programming electrode behavior.

The first IC and the required external components are fitted into a 6 mm

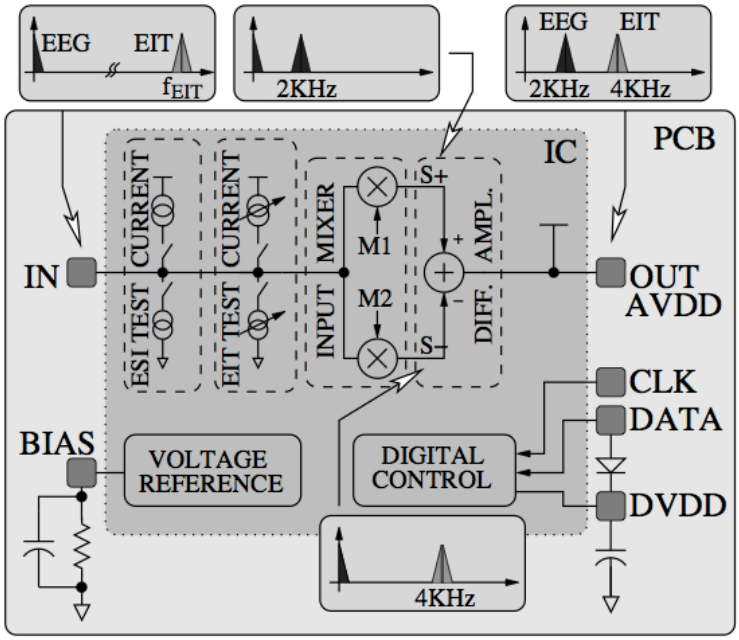


Figure 2.6: Architecture of the active electrode IC and the containing PCB.

by 8 mm PCB, shown in Fig. 2.7, along with a standard 10 mm diameter Ag/AgCl electrode, connected to IN.

2.3.1 Readout circuit design

A simplified schematic of the read out circuitry is shown in Fig. 2.8, while Fig. 2.9 shows the I/O configuration for the designed block. The input signal is directly connected to the electrode on the patient's scalp. The DC node is connected to a PCB capacitor which prevents the internal DC node to oscillate. The current bias generator, which uses a bandgap reference circuit, needs an external resistor with a nominal precision of 0.05% and a capacitor again to prevent oscillation. The high-precision bias generator gives a current of approximately $66\mu A$, given by the ratio of the bandgap voltage, approximately 1.2V, and the external resistor of $18k\Omega$. Such precision is not strictly needed for the readout circuit, but its purpose serves the current generators. A slightly modified scheme has been used in the second prototype where two different bias are used, dependent on the mode of operation of the IC (readout or injection), as explained in paragraph 2.4. The output signal, as explained, carries the analog data related to EEG, EIT and ESI, as well as the analog power supply. When the IC is not per-

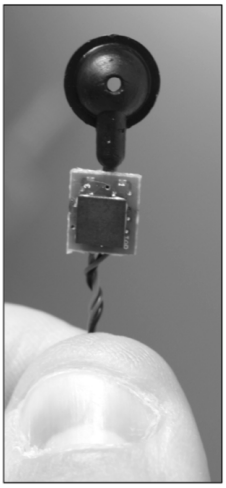


Figure 2.7: First IC prototype, PCB and electrode.

forming a readout, this signal is fed to the current generator for supply, as well as the bias signal. Signals M1P/N and M2P/N are fed to the readout circuit to the frequency mixing, as explained in paragraph 2.3.2.

2.3.2 Common mode rejection ratio

To avoid distribution of a reference signal, the IC performs single-ended amplification, and subtraction with a reference signal is only performed in

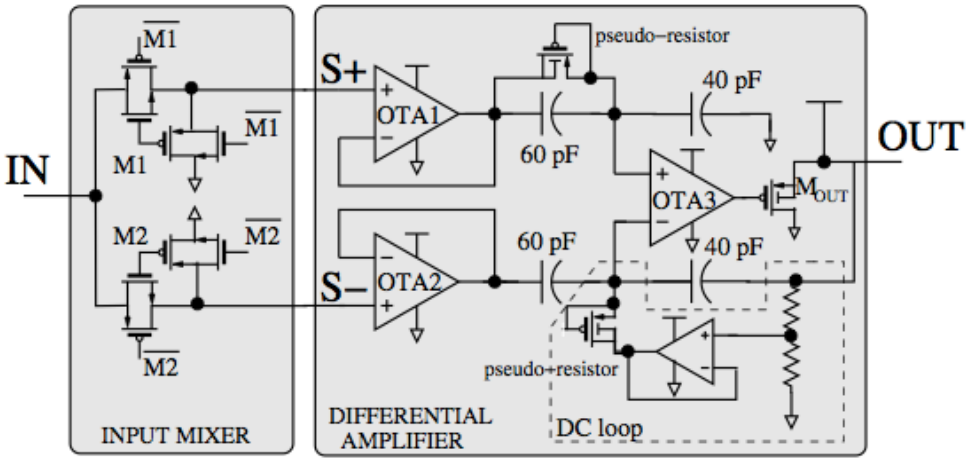


Figure 2.8: Overview of the readout circuit.

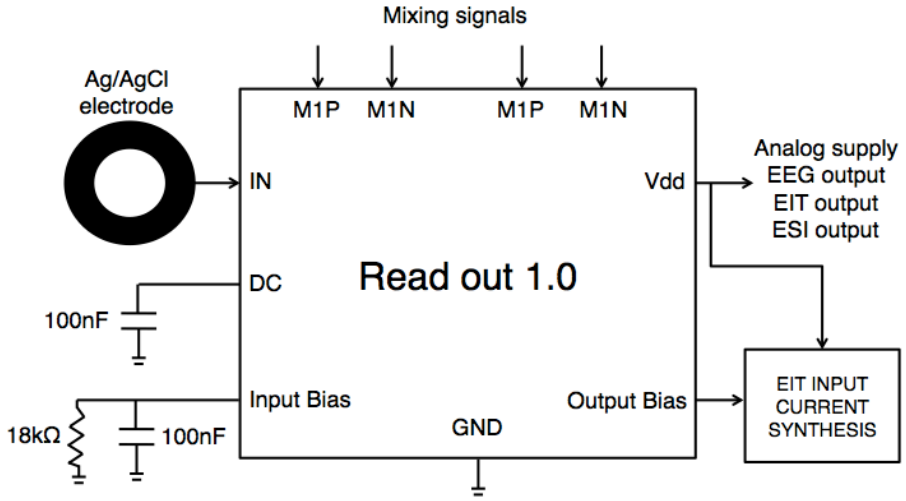


Figure 2.9: Input/Output configuration for the first prototype readout circuit.

the back-end (Fig. 2.5); the common mode rejection ration (CMRR) of the full system is thus a function of readout circuit gain value and accuracy, as shown in [102].

If we assume two active electrodes each have a gain of G_i and G_j, we can calculate the difference in their gain as:

$$\begin{aligned} V_{out} &= G_i V_{in_i} - G_j V_{in_j} \\ &= \left(\frac{G_i + G_r}{2}\right) \cdot (V_{in_i} - V_{in_j}) + (G_i + G_j) \cdot \left(\frac{V_{in_i} + V_{in_j}}{2}\right) \end{aligned} \tag{2.1}$$

Differential and common mode input can be written as:

$$V_{DM} = V_{in_i} - V_{in_j} \tag{2.2}$$

$$V_{CM} = \frac{V_{in_i} + V_{in_j}}{2} \tag{2.3}$$

Common mode rejection ratio, given by the ratio of the differential gain (G_{DM}) to the common mode gain (G_{CM}) and expressed in dB can be formulated as:

$$\begin{aligned} CMRR &= 20 \log \left(\frac{G_{DM}}{G_{CM}}\right) \\ &= 20 \log \left(\frac{G_i + G_j}{2\,|G_i - G_j|}\right) \end{aligned} \tag{2.4}$$

In order to understand how this relationship affects the amplifiers' design, we should relate it to our design constraints. The IFCN standards [82] require the system to have a CMRR of at least 110dB. If we assume that common mode voltages on the patient head are reduced by approximately 45 dB by a driven-right-leg circuit [103], our electrodes need to satisfy:

$$CMRR \geq 65dB \tag{2.5}$$

which has then a direct impact on their gain accuracy. In order to quantify this impact, we can write the closed loop response of an electrode as:

$$A_{CL} = \frac{A_{OL}}{1 + \beta A_{OL}} \tag{2.6}$$

and if we consider a unity gain configuration ($\beta = 1$) equation 2.6 becomes:

$$A_{CL_{unity}} = \frac{A_{OL}}{1 + A_{OL}} \tag{2.7}$$

For the two electrodes i and j their gains G_i and G_j can be written as:

$$\begin{aligned} G_i &= A_{i,CL_{unity}} \\ &= \frac{A_{i,OL}}{1 + A_{i,OL}} \end{aligned} \tag{2.8}$$

$$\begin{aligned} G_j &= A_{j,CLunity} \\ &= \frac{A_{j,OL}}{1 + A_{j,OL}} \end{aligned} \tag{2.9}$$

If we consider ΔA_{OL} to be the maximum possible difference between the ideal open loop gain A_{OL} we can consider the worst case scenario and equations 2.8 and 2.9 become:

$$A_{i,CL_{unity}} = \frac{A_{OL} + \Delta A_{OL}}{1 + A_{OL} + \Delta A_{OL}} \tag{2.10}$$

$$A_{j,CL_{unity}} = \frac{A_{OL} - \Delta A_{OL}}{1 + A_{OL} - \Delta A_{OL}} \tag{2.11}$$

Therefore, the CMRR in equation 2.4 becomes:

$$
\begin{aligned}
CMRR &= 20\log\left(\frac{G_i+G_j}{2\left|G_i-G_j\right|}\right) \\
&= 20\log\left(\frac{\frac{A_{OL}+\Delta A_{OL}}{1+A_{OL}+\Delta A_{OL}}+\frac{A_{OL}-\Delta A_{OL}}{1+A_{OL}-\Delta A_{OL}}}{2\left|\frac{A_{OL}+\Delta A_{OL}}{1+A_{OL}+\Delta A_{OL}}-\frac{A_{OL}-\Delta A_{OL}}{1+A_{OL}-\Delta A_{OL}}\right|}\right) \\
&= 20\log\left(\frac{\frac{(A_{OL}+\Delta A_{OL})(1+A_{OL}-\Delta A_{OL})+(A_{OL}-\Delta A_{OL})(1+A_{OL}+\Delta A_{OL})}{(1+A_{OL}+\Delta A_{OL})(1+A_{OL}-\Delta A_{OL})}}{2\left|\frac{(A_{OL}+\Delta A_{OL})(1+A_{OL}-\Delta A_{OL})-(A_{OL}-\Delta A_{OL})(1+A_{OL}+\Delta A_{OL})}{(1+A_{OL}+\Delta A_{OL})(1+A_{OL}-\Delta A_{OL})}\right|}\right) \\
&= 20\log\left(\frac{A_{OL}+A_{OL}^2-\Delta A_{OL}}{|2\Delta A_{OL}|}\right) \qquad (2.12)
\end{aligned}
$$

Being $\Delta A \ll A_{OL}$ equation 2.12 can be approximated as:

$$
\begin{aligned}
CMRR &\simeq 20\log\left(\frac{A_{OL}+A_{OL}^2}{|2\Delta A_{OL}|}\right) \\
&= 20\log\left(\frac{1+A_{OL}}{2\left|\frac{\Delta A_{OL}}{A_{OL}}\right|}\right) \\
&\simeq \log\left(\frac{A_{OL}}{2\left|\frac{\Delta A_{OL}}{A_{OL}}\right|}\right) \\
&= 20\log\left(A_{OL}\right)-20\log\left(\frac{2\Delta A_{OL}}{A_{OL}}\right) \qquad (2.13)
\end{aligned}
$$

If we now consider the further hypothesis of defining the maximum open loop gain variability as half of the ideal open loop gain:

$$
\Delta A_{OL} = \frac{A_{OL}}{2} \qquad (2.14)
$$

We obtain:

$$
CMRR = 20\log\left(A_{OL}\right)-20\log\left(\frac{2\Delta A_{OL}}{A_{OL}}\right)
$$

$$
\begin{aligned}
&= 20\log\left(A_{OL}\right) - 20\log\left(\frac{2A_{OL}}{2A_{OL}}\right) \\
&= 20\log\left(A_{OL}\right) - 20\log\left(1\right) \\
&= 20\log\left(A_{OL}\right) \qquad (2.15)
\end{aligned}
$$

which shows that that the CMRR of an electrode, in equation 2.13, is approximately equal to its open loop gain. Equation 2.15 shows that in order to satisfy equation 2.5, the open loop gain in the EEG band must satisfy:

$$A_{OL} \geq 65dB \qquad (2.16)$$

Frequency Mixing

The baseband EEG signal is double sideband mixed at a central frequency of 2 KHz and the high frequency EIT signal is down-converted to 4 KHz by two single-ended passive mixers controlled by digital signals M1 and M2 respectively, with $f_{M1} = 2KHz$ and $f_{M2} = f_{EIT} - 4KHz$. Outputs **S+** and **S-** are fed to a differential amplifier, where unity gain buffers are introduced to improve input impedance. The readout circuit is therefore designed so as to guarantee the gain accuracy required for a CMRR of at least 65 dB for a differential voltage readout in the 1-to-5 KHz band, in order to be in line with IFCN recommendations for EEG measurements [82]. As shown in paragraph 2.3.2 this approximately translates into an open loop gain of approximately 65 dB in the aforementioned band. Up-conversion of the baseband EEG signal is needed to achieve the accuracy required and a better trade-off between flicker noise and power consumption. This technique is often known as ”chopping” [104, 105]. The high-frequency EIT signal is down-converted in order to reduce the differential amplifiers bandwidth requirements. The frequency mixing is exemplified in Fig. 2.10.

Frequency mixing introduces signal attenuation. With reference to Fig. 2.8, a sinusoidal signal $V_{in} = A\sin(2\pi f_0 t)$ is fed into the two branches and

gets multiplied by two square waves with frequencies f_{M1} and f_{M2}. The square waves can be written as a sum of sinusoidal signals as:

$$V_{M1}(t) = \frac{4}{\pi}\sum_{k=1}^{\infty}\frac{sin\left((2k-1)\,2\pi f_{M1}t\right)}{2k-1} \tag{2.17}$$

$$= \frac{4}{\pi}\sin(2\pi f_{M1}t) + \frac{4}{3\pi}\sin(6\pi f_{M1}t) + \frac{4}{5\pi}\sin(10\pi f_{M1}t) + \ldots \tag{2.18}$$

If we only consider the first harmonic for signal $V_{M1}(t)$, the signal on node $\mathbf{S}+$ is given by:

$$V_{S+}(t) = V_{in}(t)\cdot V_{M1}(t)$$

$$V_{S+}(t) = \frac{A}{2}\sin(2\pi f_0 t)\cdot\frac{4}{\pi}\sin(2\pi f_{M1}t)$$

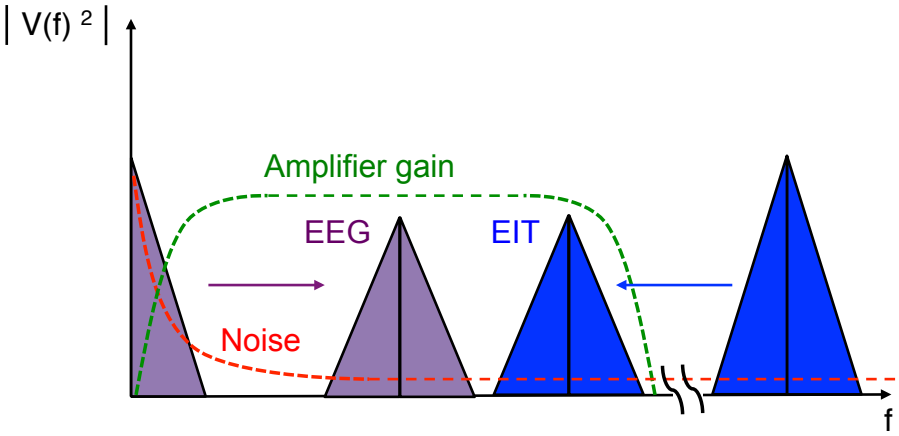


Figure 2.10: Frequency mixing exemplification. The low-frequency EEG signal is up-converted in order to reduce the amplifier's input noise, while the EIT signal is down-converted in order to be inside of the amplifier's flat gain band.

$$
\begin{aligned}
&= \frac{2A}{\pi}\sin(2\pi f_0 t)\sin(2\pi f_{M1} t) \\
&= \frac{A}{\pi}\left(\sin\left(2\pi(f_{M1}+f_0)\right)t + \sin\left(2\pi(f_{M1}-f_0)\right)t\right) \qquad (2.19)
\end{aligned}
$$

which means that the input signal $V_{in}(t)$ is thus found at the two frequencies given by the sum and difference of the modulating signal and the input frequency. The same applies for signal **S-** with the use of a modulating signal V_{M2}. As explained earlier, in our implementation we chose these as to have the EEG signal around 2 kHz and the EIT signal around 4 kHz. For the low frequency EEG signal, this translates into a square modulating wave of $f_{M1} = 2kHz$, in order to have the signal shifted at about 1.9 kHz and 2.1 kHz. The high frequency EIT signal is modulated with a square wave with a frequency $f_{M2} = f_{EIT} - 4kHz$. The attenuation factor, shown in equation 2.19 is approximately $1/\pi$. The differential amplifier's loop gain is set by the ratios of the capacitors with values 60fF and 40fF, which gives a gain in absolute value of approximately 1.5. When an EEG signal is applied, its power spectrum gets spread between two frequencies $2\pi(f_{M1}+f_0)$ and $2\pi(f_{M1}-f_0)$. The back end can then recover the whole power spectrum and hence a factor of two needs to be accounted in the overall gain. This is equivalent to a double side band (DSB) modulation. The voltage gain A_v is then given approximately by:

$$
\begin{aligned}
A_v &= 2 \cdot \frac{60pF}{40pF} \cdot \frac{1}{\pi} \\
&= \frac{3}{\pi} \\
&\simeq 1 \qquad (2.20)
\end{aligned}
$$

Equation 2.20 gives the voltage gain obtained when only one channel is used, assuming both EEG and EIT signals are sampled. If we decide to perform only the EEG, the input signal can be fed to both positive and negative branches (i.e. $f_{M2} = f_{M1}$, operating in counter phase, and thus

introducing an additional factor of two in the voltage gain).

Differential amplifier design

The differential amplifier, as can be seen from Fig 2.8, comprises 3 operational transconductance amplifiers (OTAs). Fig. 2.11 shows the circuit details for each OTA. They are two-stage OTAs with PMOS input stages optimized for noise and PSRR performances, the aim being to avoid significant feedback of the output signal through the power supply connection which could corrupt gain accuracy and stability. The output DC voltage is fixed to 3V by a feedback loop using high differential resistance pseudo-resistors [106], M_{OUT} (in Fig. 2.8) directly drives the output and positive power supply voltage of all analog circuits.

Layout implementation

Capacitors are used to set the feedback loop gain, thus they have been designed to minimize mismatch, optimizing symmetry and centre of gravity. They are implemented in a poly-to-poly fashion and connections between capacitors have been optimized as not to run above the capacitors' areas,

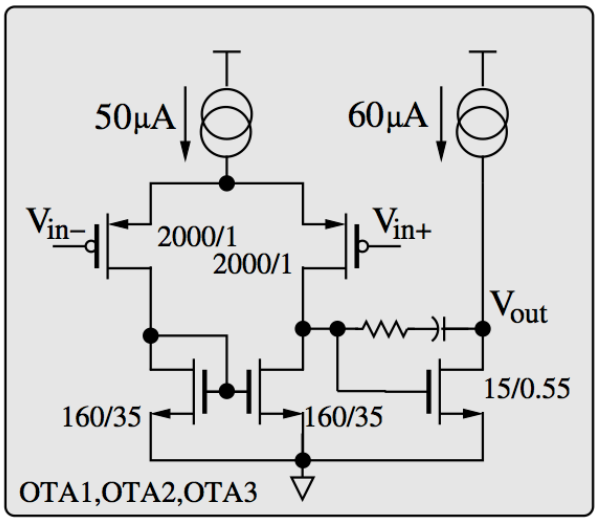


Figure 2.11: Operational transconductance amplifier.

as this can cause undesired coupling effects with a direct effect in the capacitance values and hence again on the CMRR. Further details to mismatch minimizations are given in paragraph 2.4.1. Moreover differential input pairs, current mirrors and active load have also been designed as to minimize possible mismatches. The IC was fabricated in AMS $0.35\mu m$ CMOS technology; the die measures $4mm^2$ and is encapsulated in a 5 mm by 5 mm QFN package. A photograph of the IC is presented in Fig. 2.12.

2.3.3 Measurements

The measurement setup is shown in Fig. 2.13. Performances in terms of input referred noise are reported in Fig. 2.15. Since each electrode performs single-ended amplification, in order to evaluate noise at the input of the back-end ADC (see Fig. 2.5), the test setup is composed of an input DC signal connected to two ICs whose outputs are subtracted by an instrumentation amplifier (IA) for medical applications. With mixer control signals M1=1 and M2=0 (upper graph of Fig. 2.15), the cascade of ICs differential amplifiers and external IA is characterized as shown in Fig.

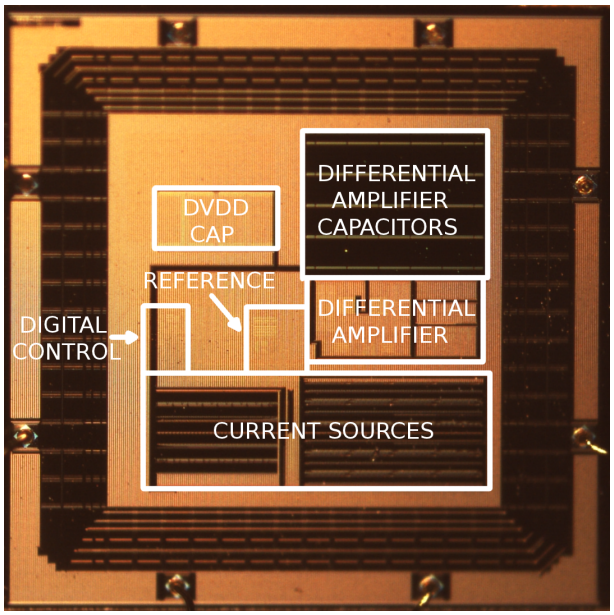


Figure 2.12: Photograph of the first IC prototype.

2.14.

The overall flicker noise corner frequency is at 500 Hz while the input referred thermal noise level is below $40nV/Hz$. The lower graph of Fig. 2.15 shows noise spectral density during normal operation for simultaneous EEG and EIT acquisition, with M1 and M2 running at 2 KHz and 4 KHz respectively. The input referred noise is $0.9\mu V_{RMS}$ for the EEG signal integrated between 0.5 and 100 Hz and for the EIT signal in a 100 Hz band centered on the EIT injection frequency. If only the EEG or EIT signal is required, M1 and M2 are driven in counterphase, doubling the output signal and therefore halving the input referred noise level to $0.45\mu V_{RMS}$

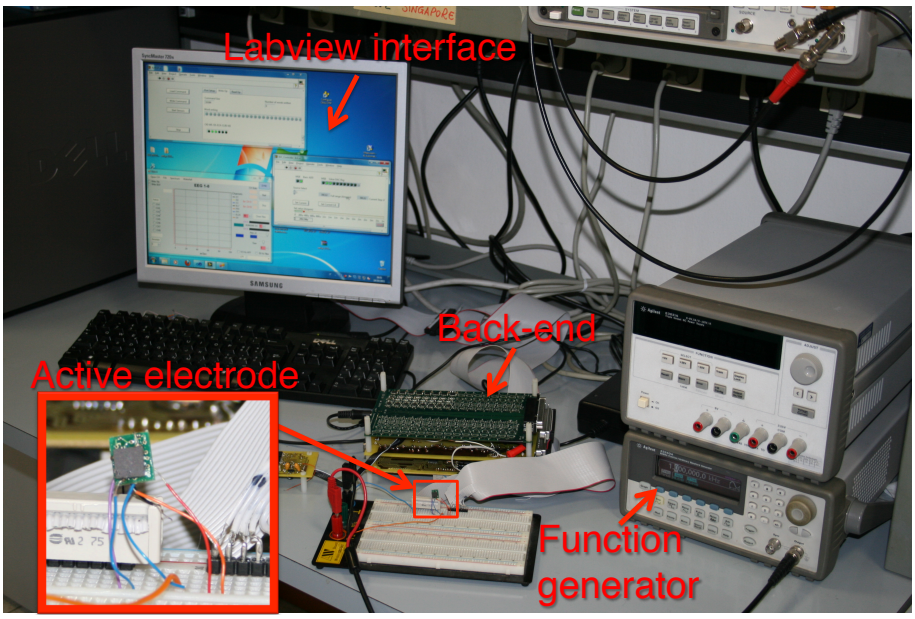


Figure 2.13: Measurement setup.

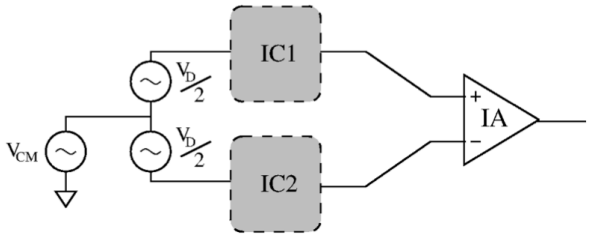


Figure 2.14: Two ICs and an IA are used to characterize the IC noise performance.

in the above mentioned bands. The test setup for the CMRR is shown in Fig. 2.16, where Zc1 and Zc2 are used to represent the electrode contact impedances.

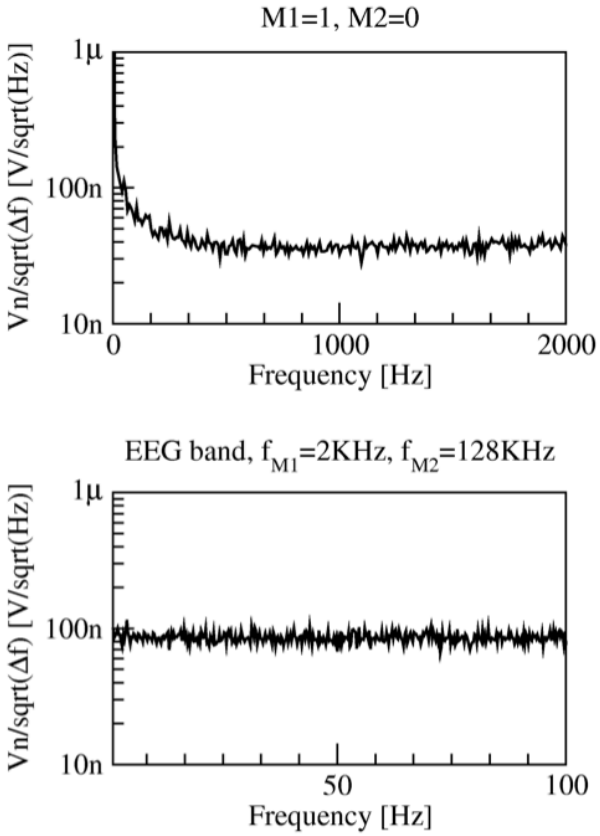


Figure 2.15: Measured performances of the cascade of differential amplifiers and IA with M1=1, M2=0 (no frequency conversions) and in simultaneous EEG/EIT acquisition.

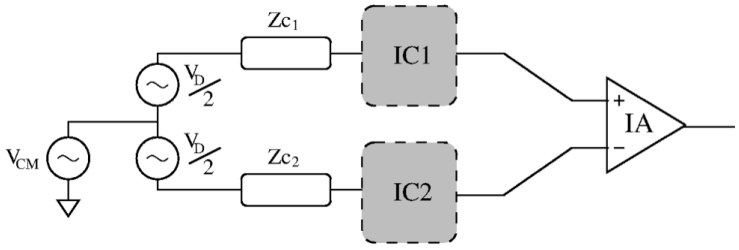


Figure 2.16: Two ICs and an IA are used to characterize the CMRR noise performance.

The CMRR in the EEG band is shown in Fig. 2.17. The CMRR is higher than 65 dB in the EEG frequency range which, thanks to the external DRL loop, results in an overall CMRR for the full system of 110 dB, in line with the IFCN requirements. Fig. 2.18 shows CMRR as a function of frequency for EIT in the case of no contact impedance mismatch and for a 100% impedance mismatch (nominal contact impedance $Z_c = 1k\Omega$).

Fig. 2.19 shows the functionality in the acquisition of an EEG signal.The EEG signal is acquired in the right occipital position O2, with reference on Fpz as shown in Fig. 2.20. Alpha waves in the 8-13 Hz range are visible when the subject has his eyes closed in the second half of recording (lighter tones correspond to higher power spectral density in the short

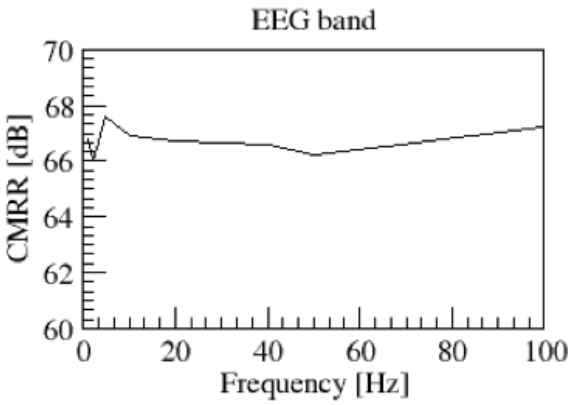


Figure 2.17: CMRR in the EEG band.

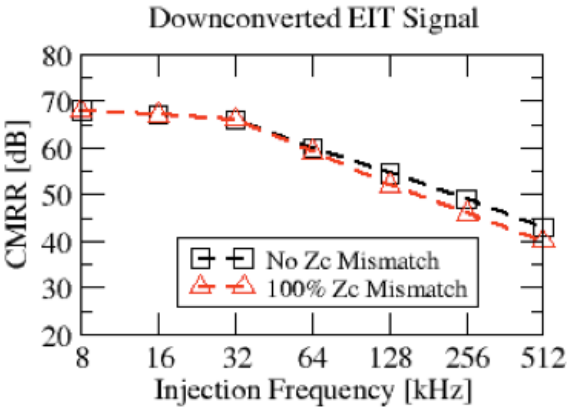


Figure 2.18: CMRR as a function of frequency for EIT injection.

	Measures
Noise	$0.45\mu V_{RMS}$
CMRR (EEG)	66 dB + 40 dB (DRL)
CMRR (EIT)	60 dB (0-64 kHz)
Power consumption	1mW

Table 2.1: Readout measured performance.

time Fourier transform graph). Power consumption in the readout mode is 1 mW, a rather high value compared to low power differential EEG instrumentation amplifiers [106, 104] due to the decision not to take the reference signal to every electrode, as well as the contemporary acquisition of both EEG and high frequency EIT. Power consumption is low enough however not to be of major concern in non-portable high density imaging systems and for the thermal dissipation introduced not to affect patient comfort. Table 2.1 summarizes the IC readout performance.

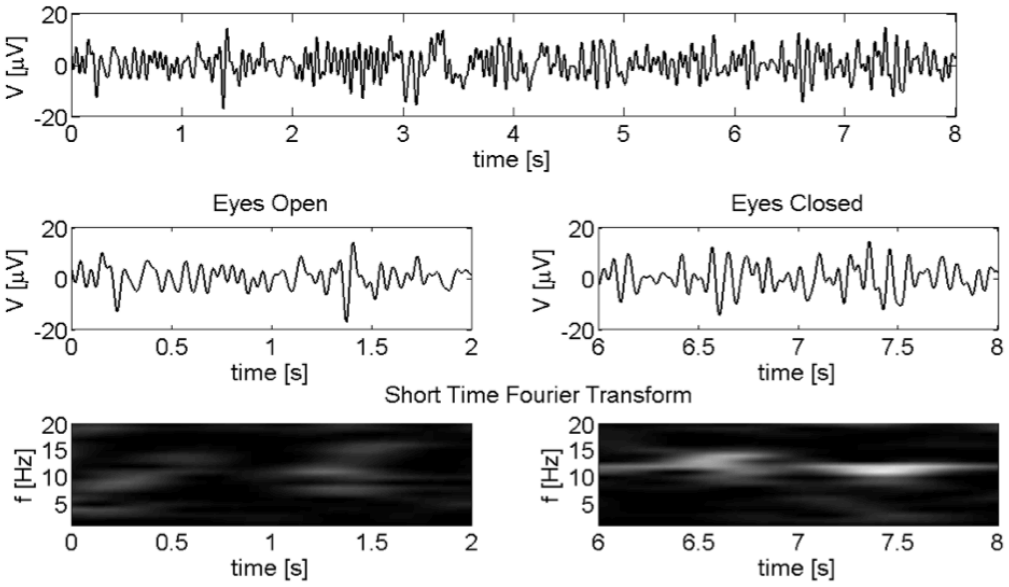


Figure 2.19: EEG functional test. Alpha rhythms are visible with the patient's eyes closed in the second half of the recording.

2.4 Second IC Prototype

A second, more robust prototype has been developed. The new IC has a more complex digital logic and a sequential access memory which allows it to be programmed beforehand and run autonomously. The author has worked on an improved readout circuit modified from the one presented in 2.3.1 as described in the following paragraph. As in the work presented in paragraph 2.3, the IC requires only 4 wires, thus allowing for the implementation of high-density electrodes systems.

2.4.1 Readout Circuit Design

The new readout circuit is shown in Fig. 2.21. As can be seen, the input is mixed in the same way as presented in paragraph 2.3.2, while the differential amplifier, in the first prototype comprising 3 OPAMPs, is now implemented with one single differential difference amplifier (DDA). This results in reduced power consumption while still attaining a lower input referred noise. Moreover, the new circuit includes two separate current bias generators. A high precision $18k\Omega$ resistor is again employed for a high precision current bias for the EIT current generators, while a low-current $1\mu A$ bias is used for the analog front end. The high-precision bias

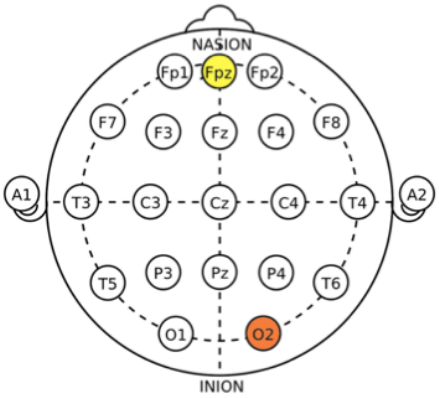


Figure 2.20: The EEG signal is acquired in the right occipital position O2 with reference on Fpz.

can be switched off when the IC is in readout operation mode, further minimizing total power consumption, which is reduced to $350\mu W$ for the whole readout circuit. The I/O configuration for the readout is shown in Fig. 2.22.

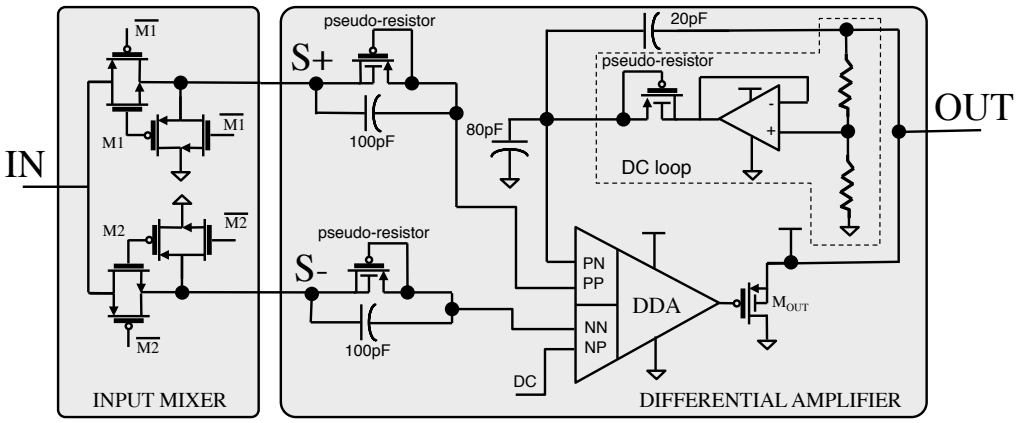


Figure 2.21: Overview of the second prototype readout circuit.

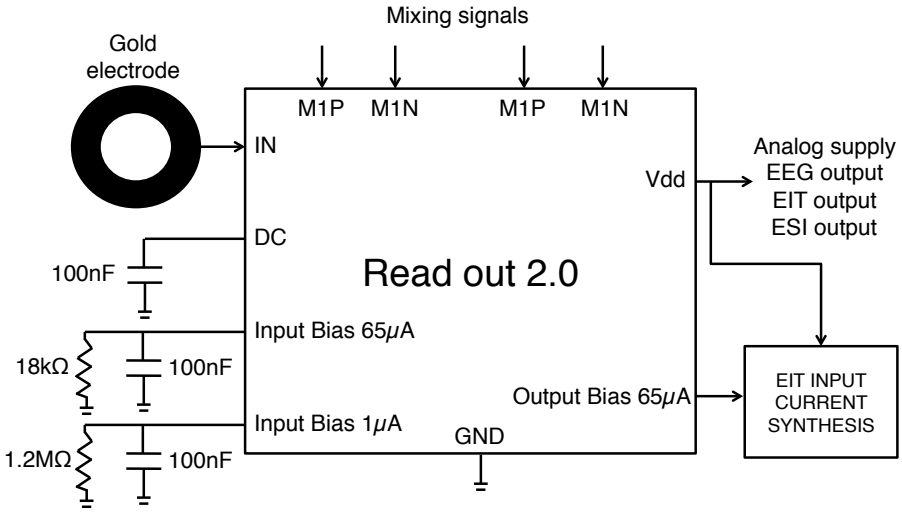


Figure 2.22: Input/Output configuration for the second prototype readout circuit.

Differential difference amplifier design

The differential difference amplifier, as presented in [107] and [108, 109] is an extension of the opamp concept, and its symbol is shown in Fig. 2.23. A DDA comprises two differential inputs, V_{pp} and V_{pn} for the positive terminal and V_{np} and V_{nn} for the negative input. The operating principle of an *ideal* two-terminal opamp, V_p and V_n with with negative feedback can be summarized as:

$$V_p = V_n \tag{2.21}$$

Similarly, an ideal DDA with negative feedback can be summarized as:

$$V_{pp} - V_{pn} = V_{np} - V_{nn} \tag{2.22}$$

A schematic of the implemented DDA is shown in Fig. 2.24. As can be seen, the DDA comprises two differential P-type pairs, with a large W/L ratio as to minimize input noise. The current generators for the two pairs are realized as standard P-type current mirrors, with $W = 600\mu m$ and $L = 100\mu m$ in order to reduce their mismatch. Post-layout simulations have shown that a mismatch between the two current mirrors can directly affect the voltage at the PMOS sources, thus introducing a degeneration in the CMRR.

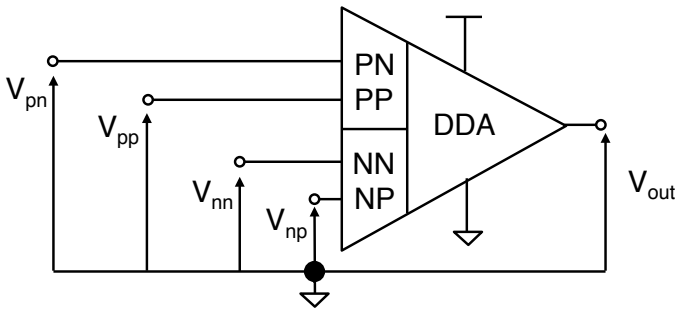


Figure 2.23: Differential difference amplifier symbol.

Loop gain

The chosen DDA configuration is of a non-inverting fashion. The scheme is shown in Fig. 2.25. In such a configuration the loop gain can be approximated as:

$$V_{out} = (V_{pp} - V_{nn}) \cdot \left(1 + \frac{C_1}{C_2}\right) \tag{2.23}$$

Equation 2.23 does not take into account input parasitic capacitances.

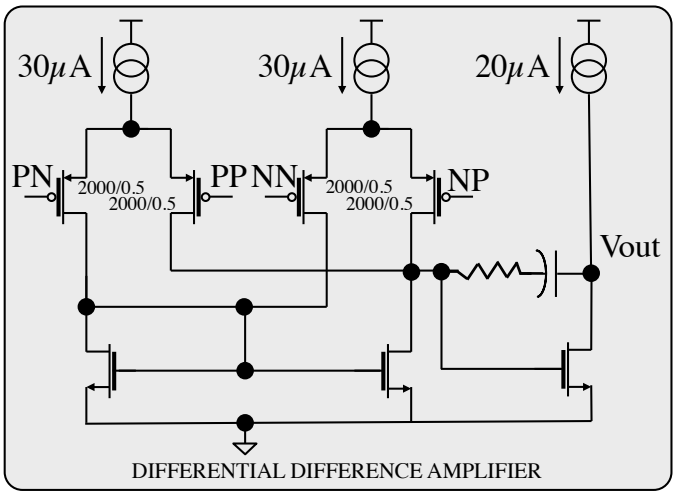


Figure 2.24: Differential difference amplifier.

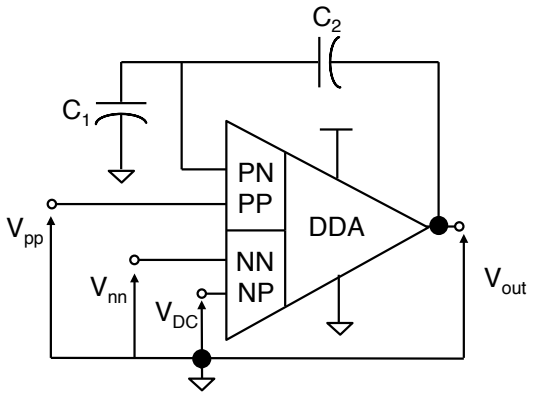


Figure 2.25: Non-inverting configuration.

Taking these into accounts modifies our output voltage as:

$$V_{out} = (V_{pp} - V_{nn}) \cdot \left(1 + \frac{C_1 + C_p}{C_2}\right) \tag{2.24}$$

where C_p represents the parasitic capacitances at the negative input node PN. In order to overcome such effect, the schematic has been modified with the addition of two series capacitors C_0, as shown in Fig. 2.26. A pseudo-resistor is added in parallel to capacitors C_0 for DC purposes. The output voltage is now given by:

$$V_{out} = (V_{pp} - V_{nn}) \cdot \frac{C_0\,(C_1 + C_p + C_2)}{C_2\,(C_3 + C_p)} \tag{2.25}$$

By choosing:

$$C_0 = C_1 + C_2 \tag{2.26}$$

The output voltage reverts back to equation 2.23. Gain variability due

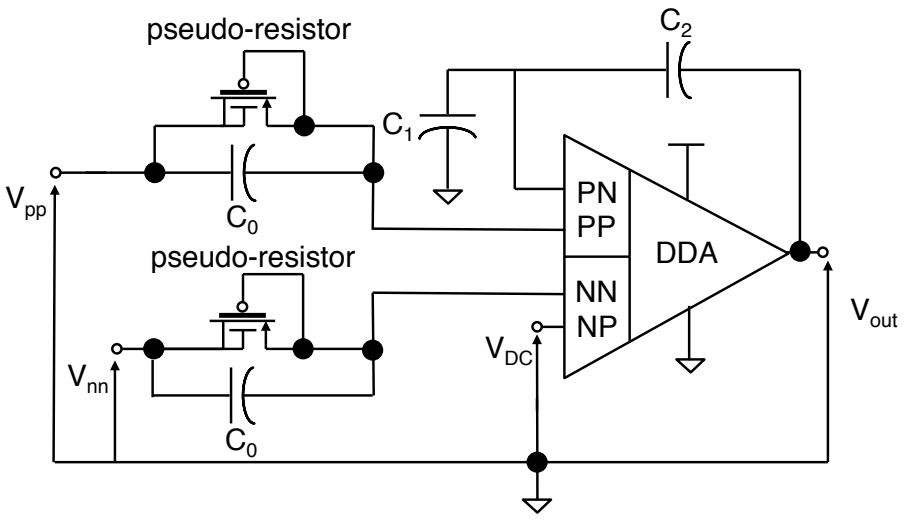


Figure 2.26: Non-inverting configuration with the addition of compensating capacitors.

	$Capacitance\,[pF]$	$Area\,[\mu m^2]$
C_1	80	40000
C_2	20	10000
C_0	100	50000

Table 2.2: Capacitor values and areas.

to this particular effect is now related to process variations, which can be controlled by choosing capacitors with the appropriate size. In the AMS $0.35\mu m$ technology used, a poly-to-poly capacitor of $20pF$ guarantees a variability compatible with our CMRR specifications. In order to minimize process variability, each capacitor has been implemented as a parallel combination of $20\,fF$ capacitors, thus maintaining a common centre of gravity, as illustrated in Fig. 2.27. The gain has been maximized in compatibility with the available area, and the capacitance values and areas are shown in Table 2.2.

The loop gain is given by:

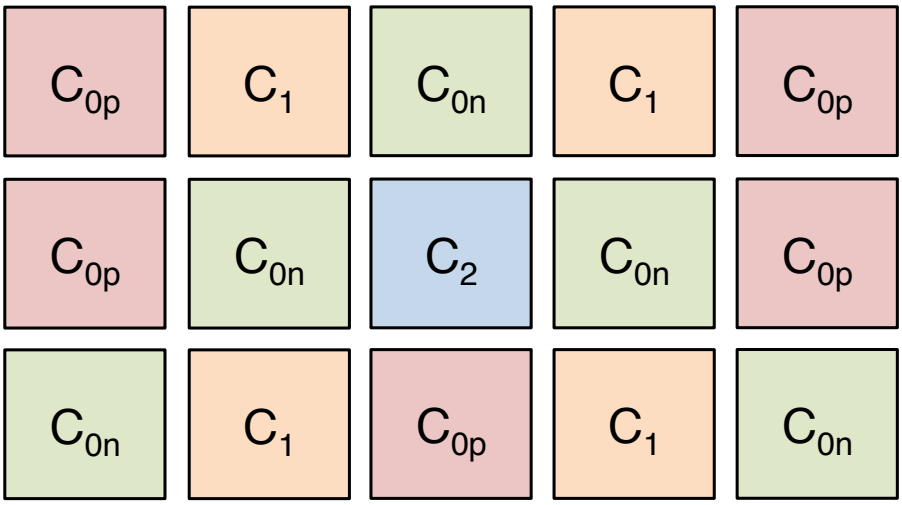


Figure 2.27: Capacitors layout implementation. C_{0p} and C_{0n} are the compensating capacitors for the positive and negative input respectively. The centre of gravity is approximately located around the centre of capacitor C_2.

	Measures
Total Input Referred Noise (EEG)	$0.35\mu V_{RMS}$ (EIT OFF)
Total Input Referred Noise (EEG)	$0.7\mu V_{RMS}$ (EIT ON)
Input Referred Noise (EIT)	$30nV/\sqrt{Hz}$ (EEG OFF)
Input Referred Noise (EIT)	$60nV/\sqrt{Hz}$ (EEG ON)
CMRR (EEG)	$60dB + 40dB(DRL)$
CMRR (EIT)	$66dB$
Input Dynamic Range	$+/-250mV$
Power consumption	$350\mu W$

Table 2.3: Second version readout measured performance.

$$\begin{aligned} A_v &= 1 + \frac{C_1}{C_2} \\ &= 5 \end{aligned} \tag{2.27}$$

The expression in 2.27 refers to the amplification without taking into account mixing attenuation. As shown in 2.3.2, this is approximately equal to π, when both EEG and EIT signals are considered.

2.4.2 Measurements

The setup measurement is the same presented in 2.3.3. The two channels exhibit a slight different CMRR. It has been chosen to use the higher CMRR channel for the EIT acquisition, as the EEG has a DRL for CMRR enhancement. Fig. 2.28 shows the CMRR for the EIT channel as a function of injection frequency with and without contact impedance mismatch (nominal $Z_c = 1k\Omega$). Fig. 2.29 shows the level of input referred noise in the EEG band. Finally table 2.3 summarizes the readout performance. As can be seen in Fig. 2.28, CMRR is negatively affected by the electrode contact impedance mismatch. This is a crucial aspect in bio-potential acquisition and for this reason different electrode types have been evaluated as described in the following chapter.

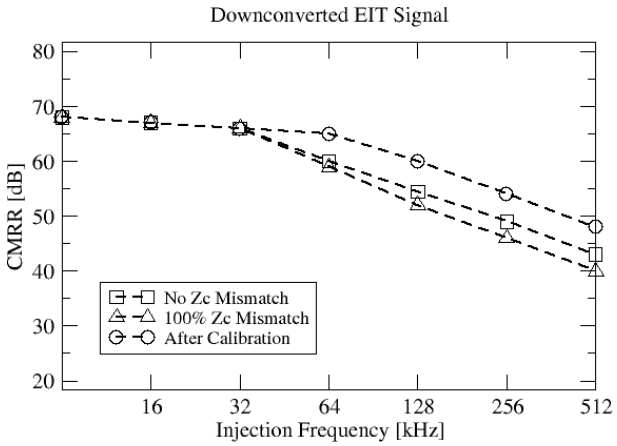


Figure 2.28: CMRR as a function of frequency for EIT injection.

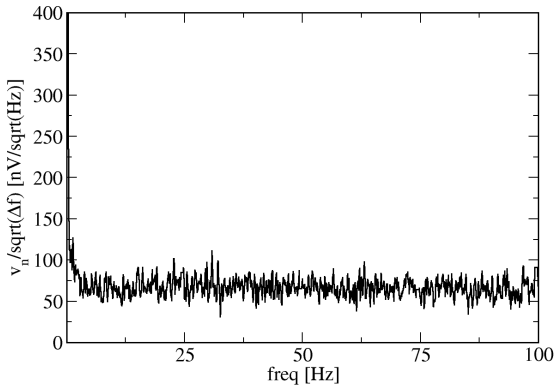


Figure 2.29: Input referred noise in the EEG band.

Chapter 3

Electrodes contact impedance

As shown in Chapter 2, contact impedance can have a strong negative impact on bio-potential acquisition as it degrades common mode rejection ratio and can introduce undesired artifacts. For this reason this aspect is examined in depth in this chapter.

3.1 Bio-potential acquisition

The first experiments involving bio-potential signals are as old as the 17th century, when Francesco Redi discovered that a highly specialized muscle of the electric ray fish generated electricity. It was later found that electricity could also interact with human muscles, generating muscle contractions, and that vice versa, it was possible to record electrical activity caused by voluntary muscle contractions. Since then, many technologies have emerged for the recording of bio-potential data, such as electroencephalography (EEG, discussed in paragraph 2.1.1), used for the diagnosis of brain diseases such as epilepsy, multiple scleroris, tumors and strokes, or electrocardiogram (ECG), used to study and monitor abnormal heart behavior, or electrical impedance tomography (EIT, discussed in paragraph 2.1.2), used to determine conductivity maps of tissues.

Besides bio-potential acquisitions for monitoring purposes, electrical activity can also be induced inside the human body for healing purposes.

Electrical stimulation is commonly used for physical therapy to recover injuries related to muscles, tendons and ligaments [110], and it has been shown that electrical stimulation can speed up the regenerative process of skin wounds [111, 112, 113].

3.2 The electrode

The electrode represents the physical interface between the electrical system and the tissue being sensed and/or stimulated. As stated in [114], *the electrode is the site of the shift from electronic to ionic conduction*. The electronic part being the metal, the ionic part being an electrolyte gel or the tissue. The electron-ion interface is an extremely complicated matter, highly dependent on geometry factors. There are several types of electrodes that can be used for bio-potential acquisition:

- *Wet Ag/AgCl electrodes*: are the most common and commercialized [115] as they are use for standard clinical EEG and ECG. The electrode functions as a redox electrode and the reaction is between the silver metal (Ag) and its salt, silver chloride (AgCl). These electrodes can achieve very good contact with the skin but require skin abrasion before application.

- *Dry electrodes*: can be fabricated using different materials, either conductive [116, 117, 118, 119, 120], or insulated [121, 122, 123], or even non-contact [124, 125]. These sensors do not require adhesives or gels, they are more comfortable on the skin, and suitable for long-term monitoring.

Standard Ag/AgCl electrodes have been extensively characterized and studied [120, 126, 127] and most of its properties are well understood [128]. Even though dry electrodes have also been studied extensively [129, 130], these have yet to be adopted for standard clinical use and are mostly limited to non-medical applications. This is related to their generally poor performance in terms of noise and motion artifacts, which is strictly related to their highly unpredictable contact impedance.

3.3 Contact impedance

A common issue when recording bio-potentials is related to the impact of the electrode contact impedance. An impedance mismatch between electrodes can diminish the common mode rejection ratio (CMRR) of the system, thus increasing power-line interference sensitivity [131], as widely discussed in paragraph 2.3.2.

In clinical practice Ag/AgCl electrodes along with a conductive paste or gel are commonly used for bio-potential acquisition. This setup has proven to be effective for many applications, but its use is mostly limited to clinical settings or research labs, due to the difficulties in establishing robust and long-lived electrical contacts.

Dry electrodes applied without glue are more convenient for the wearer and are significantly faster to apply in emergencies, but suffer from movement artifacts that are often large enough to cause the amplifier to saturate during acquisition [120]. Application of electrical currents in EIT and functional stimulation can also be affected by contact impedance as it introduces variability in the injected currents. Contact impedance mismatches as small as 20% [132] can make an EIT image meaningless [133, 134]. Thus, investigating the electrode properties is critical for EIT applications.

3.3.1 Electromagnetic theory

Electromagnetic (EM) simulations have been carried out with the FEM tool Comsol Multiphysics [28]. Comsol can be used to numerically solve partial differential equations. For a nonmagnetic material such as a biological tissue, Maxwells equations, with the inclusion of the equation of continuity can be written, with reference to table 3.1, as:

$$\nabla \times \mathbf{H} = \mathbf{J} + \frac{\partial \mathbf{D}}{\partial t} \tag{3.1}$$

$$\nabla \cdot \mathbf{B} = 0 \tag{3.2}$$

Symbol	EM meaning
E	Electric field
B	Magnetic field
D	Electric displacement
H	Magnetic intensity
ϵ	electric permittivity
μ	Magnetic permittivity

Table 3.1: Electromagnetic quantities.

$$\nabla \times \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t} \tag{3.3}$$

$$\nabla \cdot \mathbf{D} = \rho(\mathbf{r}, t) \tag{3.4}$$

$$\nabla \cdot \mathbf{J} = -\frac{\partial \rho(\mathbf{r}, t)}{\partial t} \tag{3.5}$$

$$\tag{3.6}$$

When studying contact impedance for bio-potential acquisition such as EEG or EIT we make the following assumptions that greatly simplify the problem:

1. Negligible external **B** field.
2. Quasi-static limit $\left(\frac{\partial \mathbf{D}}{\partial t} = 0\right)$

Negligible external B field

The first of the two assumptions is justified as long as there is no electromagnetic interference (EMI). This means that the EIT and EEG should be performed in a proper clinical environment and no other electromagnetic disturbance such as might be caused by an imaging technique, e.g. MRI, trans-cranial magnetic stimulation (TMS) or ablation, is performed concurrently. EMI could still be present at the power-line frequency (50 Hz or 60 Hz), which is one of the key issues when recording EEG and EIT. As explained in the beginning of this chapter, an electrode contact impedance mismatch could easily cause a decrease in the systems CMRR.

Measurement of the contact impedance can be carried at frequencies below or above the power-line frequency, therefore allowing us to neglect the **B** field. Techniques to mitigate such interference, such as wire twisting [131] and increasing the CMRR through a DRL loop [103] exist, but are out of the scope of the presented work. Additional EMI could occur from mobile phones when measuring the contact impedance, but this is nullified if the devices are held at a proper distance from the patient and EEG/EIT instrumentation [135].

Quasi-static limit approximation

The quasi-static approximation is valid as long as the EIT injected frequency is low enough for the electromagnetic propagation delay to be neglected [136]. For a 100 kHz EIT signal in a human head with a radius $\rho_h = 0.2m$, the propagation delay is approximately given by ρ_h/c , where c is the speed of the electromagnetic waves in the body, which approaches the speed of light. This results in a delay which is less than a nanosecond, much smaller than the signal period of $10^{-4}s$. Secondly, the ratio of the displacement current to the conduction current is of the order of $\omega\epsilon/\sigma$ [137]. For biological tissues the permittivity ϵ varies with frequency, ranging between 10^{-7} at 10 kHz and 10^{-5} at 10 Hz [136], with $\omega\epsilon/\sigma$ resulting between 10^{-2} and 10^{-3} . This means that we can ignore the contribution of the displacement current. With such assumptions, the electric field can be expressed solely in terms of the electric potential. The time-harmonic equation of continuity, assuming no charge variation in the volume and an applied external current can be written as:

$$\begin{aligned} \nabla \times \mathbf{J} &= \nabla(\sigma\mathbf{E} + \mathbf{J}^{\mathrm{e}}) \\ &= -j\omega\rho\left(\mathbf{r}, t\right) \\ &= 0 \end{aligned} \tag{3.7}$$

Combining 3.7 with Poisson's equation (3.4) yields:

$$\nabla \times ((\sigma + j\omega\epsilon)\,\nabla V - \mathbf{J}^{\mathrm{e}}) = 0 \tag{3.8}$$

The boundary conditions are set as:

$$\mathbf{n} \cdot \mathbf{J} = 0 \tag{3.9}$$

at all points other than at the current injecting and absorbing electrodes, which are set respectively as:

$$\int \frac{V}{area} = \mathbf{Z} \cdot \mathbf{I} \tag{3.10}$$

and

$$V = 0 \tag{3.11}$$

The impedance, which is frequency dependent is usually represented as a complex number with real and imaginary part:

$$\mathbf{Z} = Re\,[\mathbf{Z}] + jIm\,[\mathbf{Z}] \tag{3.12}$$

accounting for its resistive and reactive components. On the internal boundaries between two adjacent domains D_1 and D_2 continuity is given by:

$$\mathbf{n} \cdot (J_1 - J_2) = 0 \tag{3.13}$$

Equation 3.8, along with 3.9, 3.10, 3.11, 3.13 constitutes a problem that can be numerically solved with Comsol.

3.3.2 Methods

Contact impedance is evaluated in a real-life scenario with either two or four electrodes as shown in Fig. 3.1. Four electrode measurements achieve higher accuracy as they allow one to separate the contribution of the con-

tact impedance from the underlying volume. The assumption is that high input-impedance amplifiers drain negligible current and if two separate electrodes are used for voltage sensing no significant voltage drop should occur on these electrodes. Subtraction between the two measurements yield the contact impedances of the current injecting and absorbing electrodes. This is subject to the approximation that the two current injecting and sensing electrodes cannot be placed in the same location, unless concentric electrodes are used. Nevertheless, four electrodes measurements are not always a feasible option due to the extra-cost of the additional electrodes. In the work we presented [88], an active electrode for simultaneous EIT and EEG measurements has been introduced, along with continuous contact electrode impedance monitoring between two electrodes. For this reason, a two electrodes simulation environment has been chosen.

Comparison between different simulation setups

In order to validate the simulation, several steps have been taken. First of all a 2D simulation for flat, square electrodes has been performed. The simulation environment is depicted in Fig. 3.2, where the volume depth is set to 1cm and ideal electrodes (1cm x 1cm) are placed 5cm apart. The arrows represent the current flow as current is introduced on the left electrode and returned into the right electrode.

As can be seen in Fig. 3.2 the skin is characterized as a two-layer volume: a thicker conductive layer of $0.6cm$ (deep tissues containing a granular layer) and a thin, resistive layer of $32\mu m$ of stratum corneum (SC),

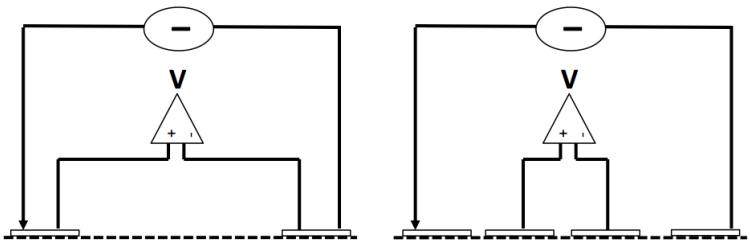


Figure 3.1: Two-electrodes (left) and four-electrodes (right) impedance measurements.

as presented in [138] and [139]. Dead cells mainly form the latter, and because of its low conductivity is usually removed by abrasion when performing EEG or EIT. This model is in accordance with literature [129, 130] for dry electrodes. In such models, a resistor and a capacitor are used in parallel to represent the SC, with an additional series resistor for the underlying skin as its properties are mainly resistive. Additionally, a half-cell potential generator can be considered, but due to its DC nature it can be neglected for our purposes, as EEG and EIT are not performed with direct currents. This and other model limitations are discussed in paragraph 3.3.4.

The resulting impedance for this configuration is compared with a full 3D simulation, shown in Fig. 3.3, a 3D equivalent model to the one presented in Fig. 3.2. In both Figs. 3.2 and 3.3, the color scale represents the electric potential, while the arrows represent the total current density. The injecting electrode is hence the one with the higher potential (in red), while the absorbing electrode is kept at ground (in blue). The setup of the two previous examples (in 2D or 3D) is the most common scenario for contact impedance measurements, with the assumption that the volume between the two electrodes is rather small compared to the contact impedance at lower frequencies. When performing an EM simulation, the setup can be simplified, including only one standard electrode and a ground electrode

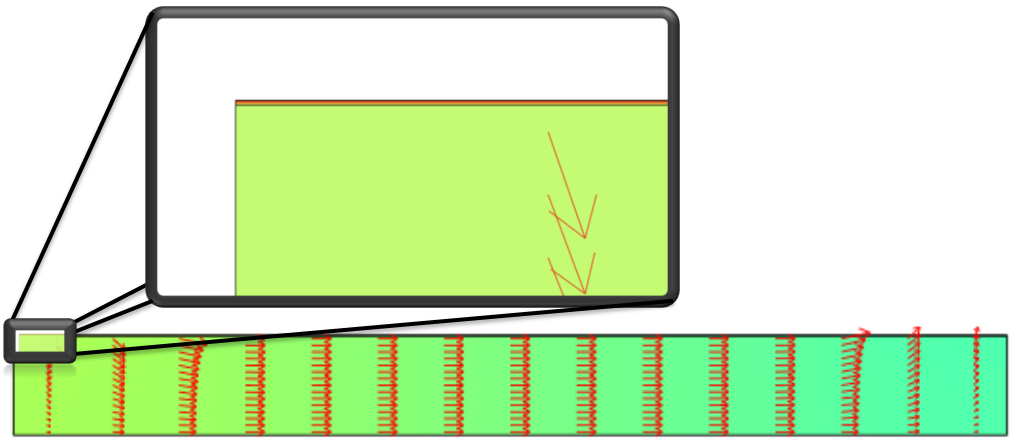


Figure 3.2: 2D Two-electrodes simulation.

underneath the skin, as depicted in Fig. 3.4. In this setup, current is injected from the top face and absorbed at the bottom face and the current density is hence oriented along the z-axis. This allows focusing the study on the impact of the SC rather than the underlying volume.

3D FEM simulations require a high number of elements and geometric simplification is the key factor in order to be able to obtain significant simulation data. This is critical for memory usage as the ratio of the overall geometry ($10^{-2}m$) to the SC thickness ($30^{-6}m$) is very large, requiring a problematically large number of mesh elements. Although it has been shown that 2D simulations are accurate, electrode geometries such as needles or micromachined multipoint spiked electrodes cannot be simulated in a 2D environment. The simulation setup in Fig. 3.4 represents a reasonable trade-off for a 3D environment. In order to include possible fringing effects, which cannot be simulated in 2D, the volume has been expanded

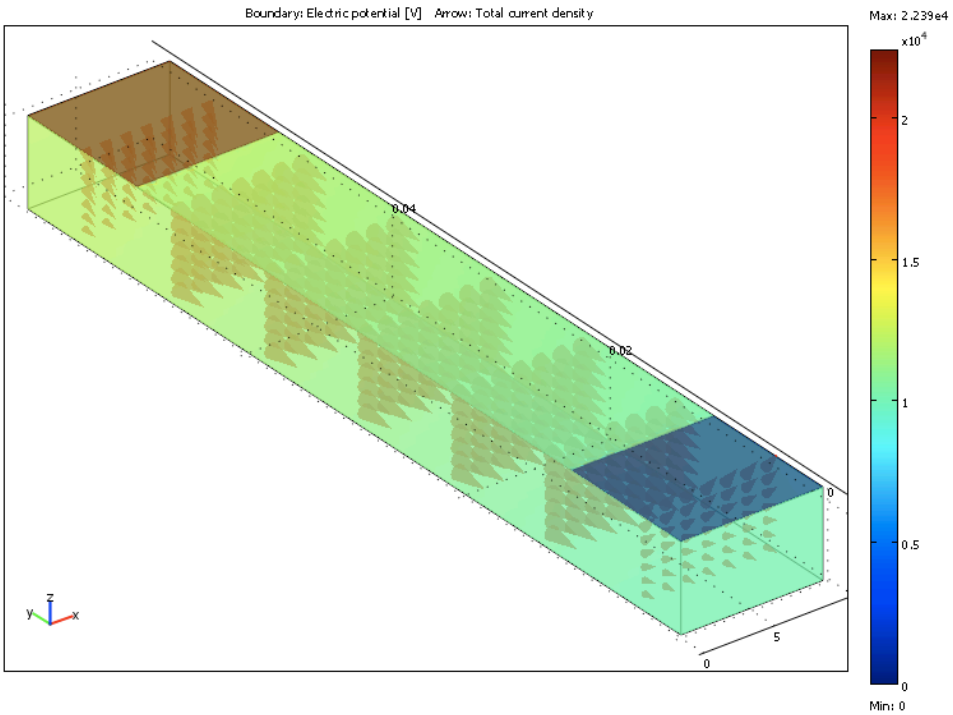


Figure 3.3: 3D Two-electrodes simulation.

by a factor of two in the x and y directions, as shown in Fig. 3.5, with the injecting surface on the top face kept constant. This choice enables the current to flow unrestricted by tight boundaries, and hence gives a more accurate representation of the physical problem under study. This can be seen as the current density in Fig. 3.5 has a component in the x and y direction, as opposed to the strictly vertical current density shown in Fig. 3.4.

Impact of contact area on flat electrodes

One of the key factors when considering the electrode contact impedance is given by the contact area. In practice when a metal plate is used, its entire surface is not always in contact with the skin. This is caused by multiple factors, such as skin pores and hair obstructing the electrode to skin interface. In order to simulate such scenarios, parametric simulations

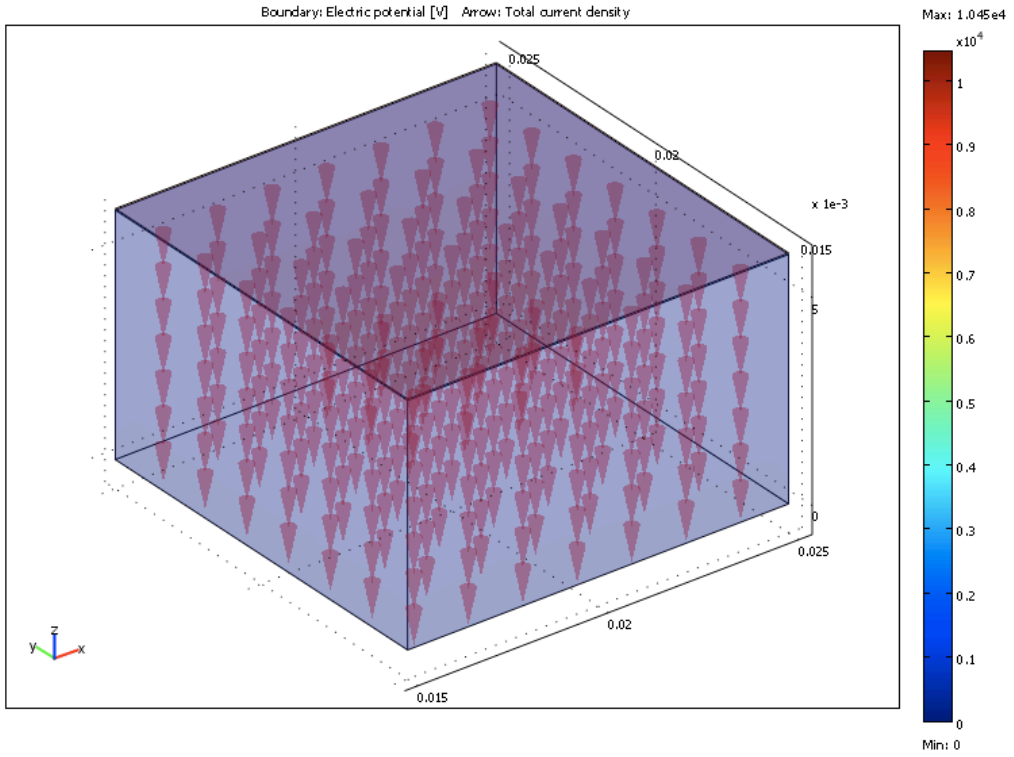


Figure 3.4: 3D Single electrode setup.

as a function of the effective electrode area have been performed.

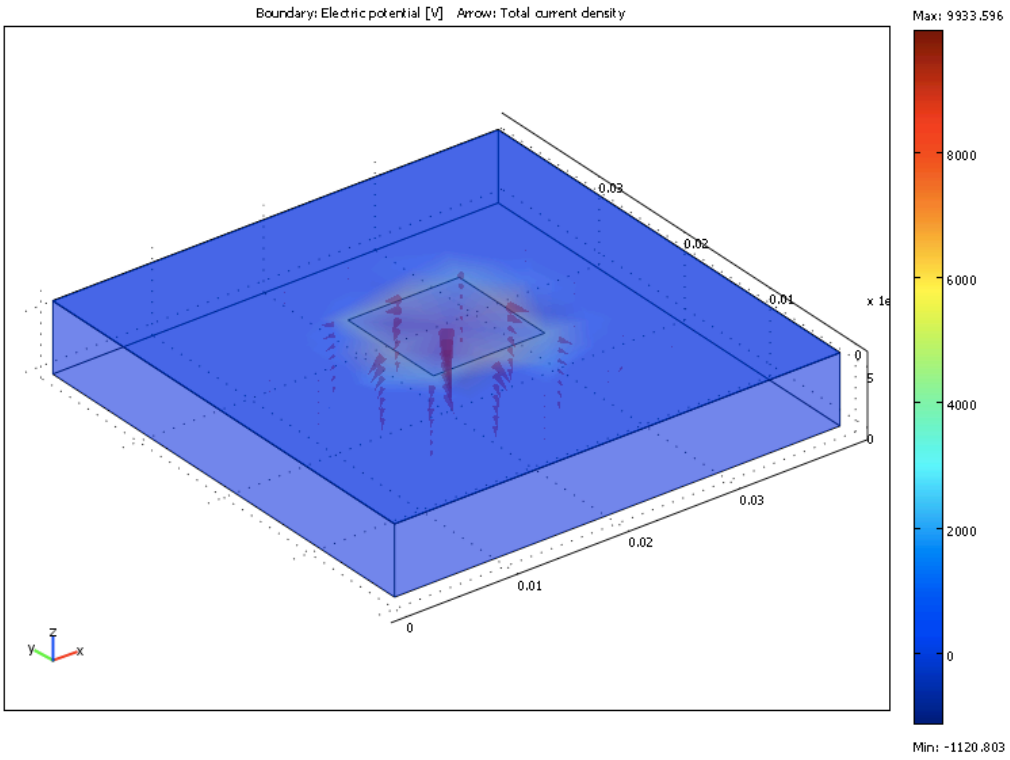
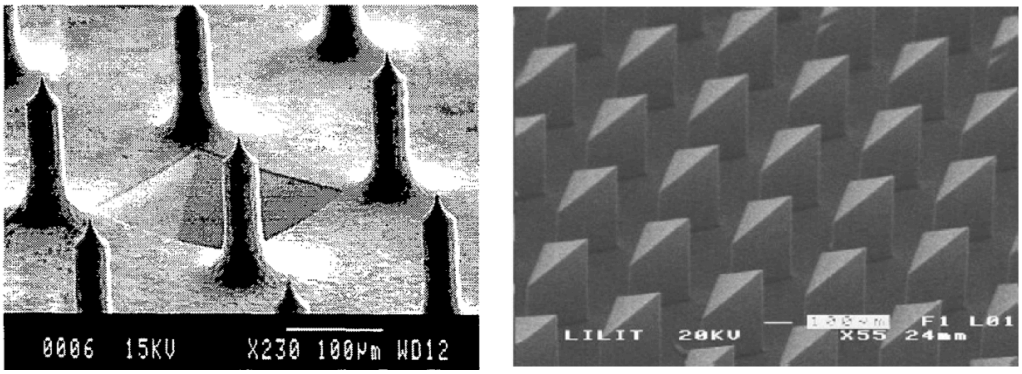


Figure 3.5: 3D Single electrode expanded geometry to include fringing fields.



a) b)

Figure 3.6: Micromachined spiked electrodes. Sources a) [3], b) [4]

Micromachined multipoint spiked electrodes

With the development of MEMS technology, new dry micromachined multipoint spiked electrodes have been presented [3, 4], as shown in Fig. 3.6 a) and b) respectively. Such electrodes offer some benefits when compared to other dry electrodes, and wet Ag/AgCl electrodes. Standard clinical use of wet electrodes for EEG or EIT measurements requires the abrasion of the SC layer. This is a time-consuming practice and can make the patient uncomfortable. Another drawback is presented by the impedance temporal dependency, caused by gel dehydration [140]. Spiked electrodes, on the other hand, can be used without any sort of skin preparation as the micromachined needles can go through the superficial layer of the SC significantly reducing the contact impedance. In Fig. 3.7 a 16 needles electrode simulation is shown. All needles are $40\mu m$ in diameter, to match the electrodes presented in [3].

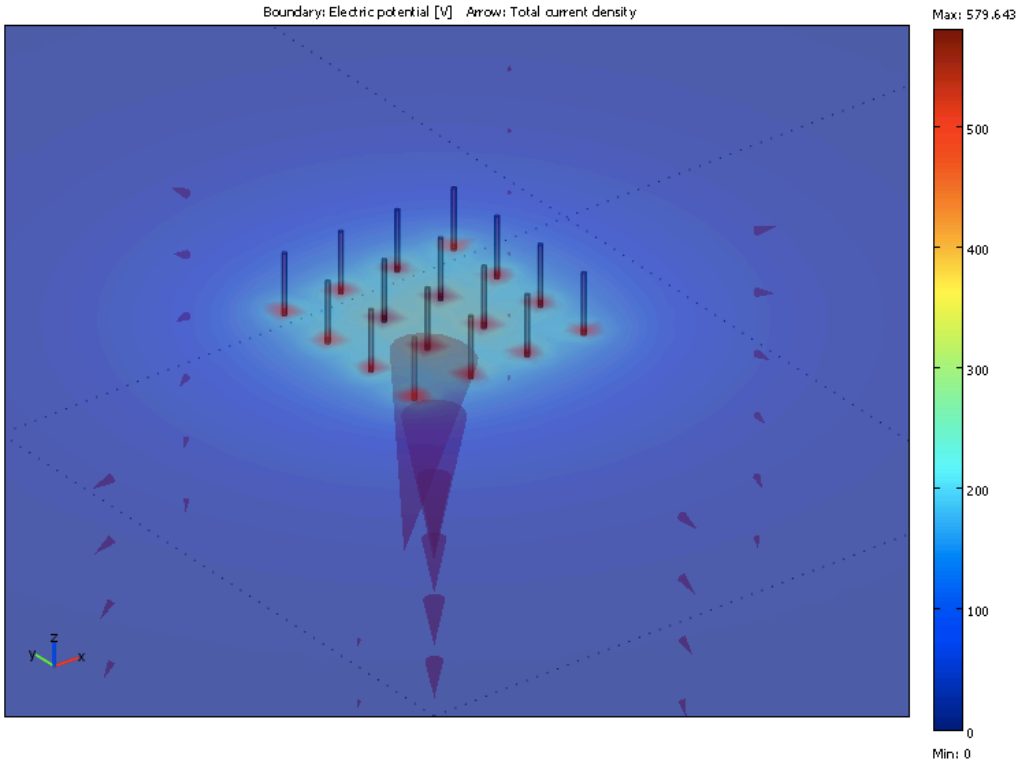


Figure 3.7: 16 Spikes-electrode

One of the key aspects that can be evaluated with the FEM simulator is contact impedance sensitivity to variations in the SC layer. The SC water content can be subject to variations causing a change in SC permittivity (ϵ) and conductivity (σ), as well as thickness [141]. A 10% decrease in both conductivity and permittivity and a $10\mu m$ increase in its thickness have been simulated as case studies. These are reasonable changes and it must be noted that even larger variations could be expected, as the SC thickness can vary from tens to hundreds of μm in different body areas [142]. We hypothesize that flat electrodes are influenced by such changes, while penetration of spiked electrodes offer a degree of immunity enabling it to be in direct contact with the underlying skin layer.

3.3.3 Results

Comparison between different simulation setups

The preliminary study with the 2D geometry (Fig. 3.2) shows that, whenever possible, a 2D simplification is highly advisable, as similar simulation results to the 3D setup (Fig. 3.3), with a much smaller computational cost can be obtained. The difference in the evaluated impedance between the 2D ($|\mathbf{Z}| = 42092\Omega$) and 3D simulations ($|\mathbf{Z}| = 41932\Omega$) is within 0.4%. It is also interesting to note that almost the entire potential drop is confined in the SC, as it can be seen in Fig. 3.3. This was to be expected as the underlying skin volume is highly conductive and is in agreement with the simulations performed in [143], which show that this is the case for frequencies up to 1kHz.

The simplified one-electrode setup in Fig. 3.4 shows that the evaluated impedance is, as expected, slightly smaller than half of the previous one. In this case only one electrode is considered, and the high-conductive volume is also reduced. When the volume under study is enlarged in the x-y direction (to avoid fringing effects), the contact impedance is slightly reduced because of additional current flowing in this plane. Table 3.2 summarizes the results for these simulations.

In Table 3.2 the simulated data has also been compared with the mea-

		$Re\,[Z]\,[\Omega]$	$Im\,[Z]\,[\Omega]$	$\lvert Z\rvert\,[\Omega]$
Measured data	Two round electrodes (measured values) [138]	30000	5000	30400
Simulated data	2D two square electrodes Fig. 3.2	38644	16685	42092
	3D two square electrodes Fig. 3.3	38498	16619	41932
	3D single square electrode Fig. 3.4	17609	8347	19487
	3D single square electrode expanded geometry Fig. 3.5	15880	7585	17598

Table 3.2: Comparison between different simulation setups and measurements at 20 Hz.

surements presented in [138], where circular electrodes of a comparable size (diameter of $0.9cm$ at a $5cm$ distance) have been used along with a conductive gel. The gel impedance and additional effects due to electrode polarization and wire strays have been subtracted by the authors. This was done by measuring the direct electrode to electrode impedance, so the measured impedance is related to the SC and the underlying skin, as in the presented work. The simulated data can be seen to be comparable with the measured data in [138]. It must be noted that an extensive comparison with literature could not be undertaken, as all the presented works systematically disagree on the reported impedance values [144, 138, 142, 120, 129, 130].

Impact of contact area on flat electrodes

The graph in Fig. 3.8 shows $|\mathbf{Z}|$ as a function of the electrode effective area for a $1cm$ x $1cm$ square electrode. As expected, the effective area of contact is a key factor in the contact impedance. Measurements have shown that rough-surface electrodes can be used in order to optimize this parameter [142]. A simple regression has been applied to the simulated data in order

to obtain an analytical expression for $|\mathbf{Z}|$ as a function of frequency and area. The model fits well at low frequencies but does not provide accurate data when used at 2 kHz. This is not unexpected, as shown in[143], at 1 kHz the underlying skin starts dominating the impedance. This is why the analytical model, which is predicting impedance for the stratum corneum, would give a negative value for the impedance at frequencies greater than 1kHz, as shown in Fig. 3.8. The analytical expression is discussed in paragraph 3.3.5.

Micromachined multipoint spiked electrodes

Table 3.3 summarizes the results of the simulated variations in the SC conductivity and thickness. As hypothesized in paragraph 3.3.2, the flat electrodes exhibit a high sensitivity to such changes, while the spiked electrodes, thanks to their penetration depth set in this example to $72\mu m$, are immune. It is shown that if this value is constant, even a change in the SC

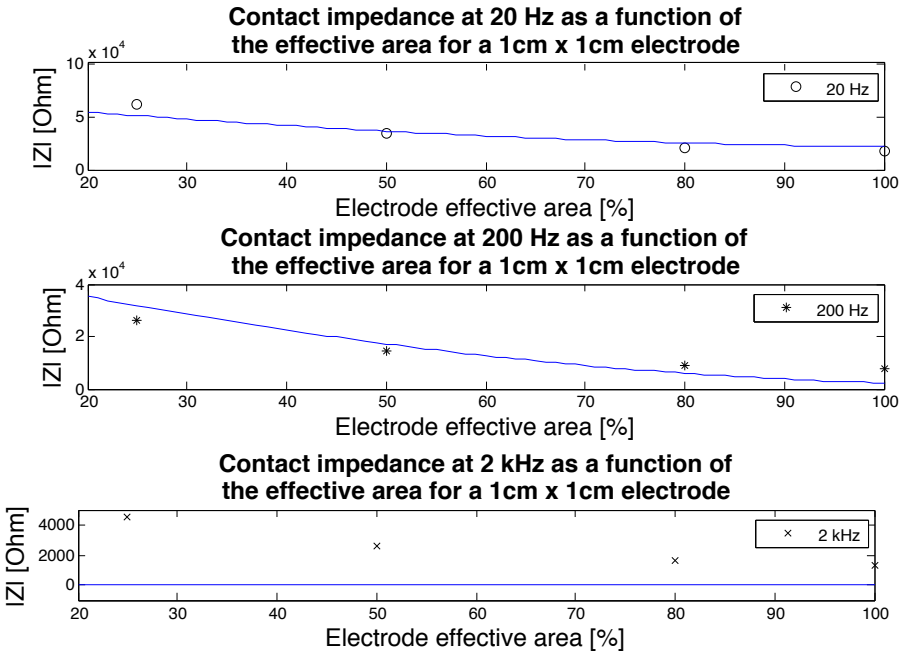


Figure 3.8: Contact impedance as a function of electrode effective area. The plotted data points are from the FEM simulation and the solid line the fitted regression model.

	$\lvert Z\rvert$ [Ω] σ, ϵ nominal	$\lvert Z\rvert$ [Ω] $\sigma, \epsilon - 10\%$ Thickness $+10\mu m$	Δ [%]
Flat 20 Hz	17598	25594	45
16 needles 20 Hz	1155	1146	-0.8
Flat 200 Hz	7544	10964	45
16 needles 200 Hz	1005	997	-0.8
Flat 2 kHz	1323	1910	44
16 needles 2 kHz	922	915	-0.8

Table 3.3: Comparison between different simulation setups and measurements at 20 Hz.

conductivity, permittivity or thickness is negligible. Nevertheless in a real-life scenario the applied force is variable and will result in varying depth. Moreover, the number of needles in contact with the skin can decrease due to surface roundness or electrode damage.

Fig. 3.9 shows impedance variations for a 16 spikes electrode due to penetration depth changes, while Fig. 3.10 shows contact impedance as a function of the number of spikes. Again, a regression has been applied to the simulated data in order to obtain an analytical model to predict the contact impedance and fits well with the data. As shown in Fig. 3.9 and Fig. 3.10, penetration depth and the number of spikes are crucial parameters and can result in significant impedance variability.

3.3.4 Limitations

Although it has been shown how a FEM EM simulator can provide enough flexibility to study different geometries and directly allow for the evaluation of impedance values, it must be noted that there are several limitations to this method. The presented results outline how, even when the same electrodes are used, great variability in the contact impedance can occur due to setup mismatches such as area of contact for flat electrodes or penetration depth for spiked electrodes.

Nevertheless there are other effects that cannot be simulated in such environment. The major limitation is due to the electrochemical nature of

the electrodes. An electrode constitutes the site of a charge carrier shift, a charge exchange between electrons and ions [114]. At this interface, electrochemical processes occur, with effects such as half-cell potentials and electrical double-layer, causing additional DC voltages and series capacitors and resistors.

Moreover, the underlying skin becomes moistened with time due to sweat-gland activity, thereby decreasing the electrode-skin impedance [140].

3.3.5 Analytical model for the electrode to skin interface

As shown in Figs. 3.8, 3.9, 3.10, an analytical formula provides a reasonable approximation of the contact impedance. This allows one to quickly

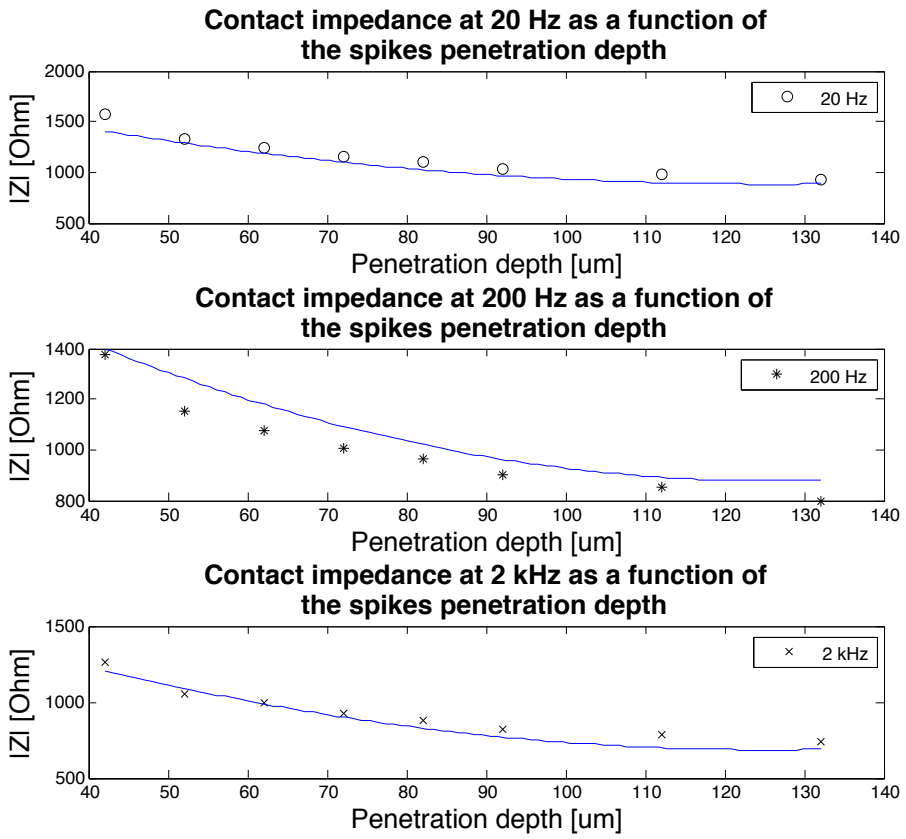


Figure 3.9: Contact impedance as a function of the penetration depth. The plotted data points are from the FEM simulation and the solid line the fitted regression model.

estimate the impedance for flat or spiked electrodes as a function of the area, the number of spikes and their penetration depth. Table 3.4 shows the analytical formula for the different scenarios where f, A, s and d represent frequency, area, number of spikes and penetration depth respectively. The coefficient of determination $\mathbf{R}^2$ is evaluated in order to provide a measure of quality for the statistical regression. This is defined as:

$$\mathbf{R}^2 = 1 - \frac{SS_{err}}{SS_{tot}} \tag{3.14}$$

Where SS_{err} and SS_{tot} are defined respectively as:

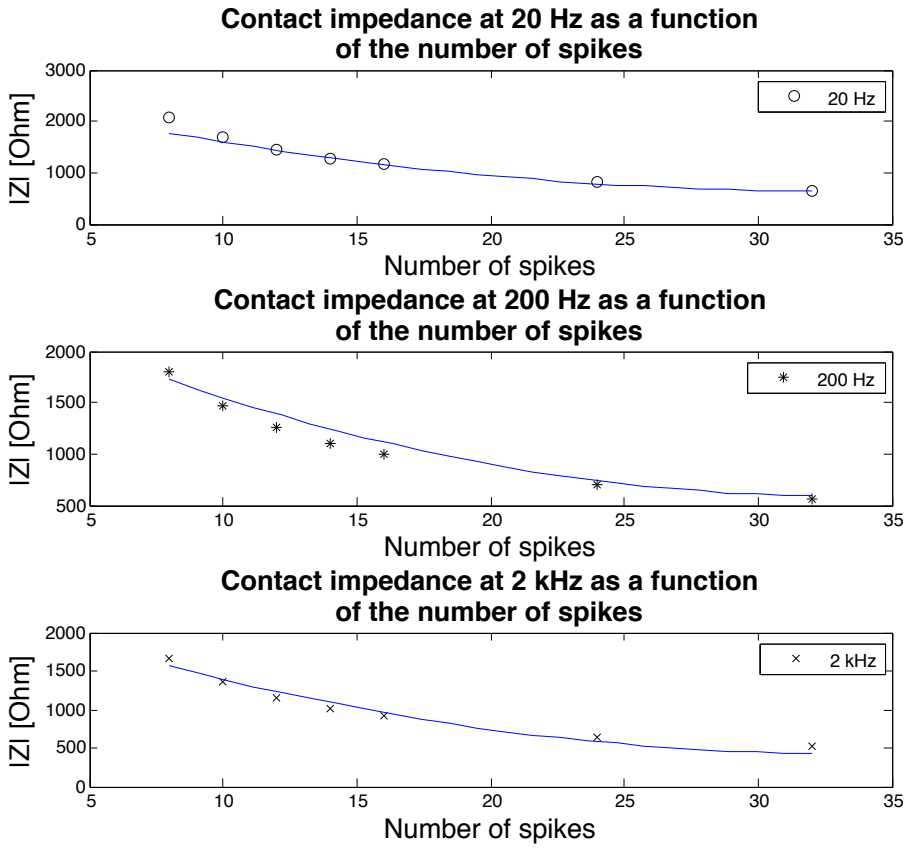


Figure 3.10: Contact impedance as a function of the number of spikes. The plotted data points are from the FEM simulation and the solid line the fitted regression model.

	$\|\mathbf{Z}\|$	$\mathbf{R^2}$
Flat electrode $\|\mathbf{Z}\| = max\,(0, \|\mathbf{Z}\|\,(f, A))$	$\|\mathbf{Z}\| = 7.1 \cdot 10^4 - 8.7 \cdot 10^8 A - 5.3 \cdot 10 f + 3.8 \cdot 10^{12} A^2$	0.93
Spiked electrode $\|\mathbf{Z}\| = \|Z\|\,(f, s)$	$\|\mathbf{Z}\| = 2.6 \cdot 10^3 - 1.2 \cdot 10^2 s - 2.8 \cdot 10^{-1} f + 1.8 s^2$	0.95
Spiked electrode $\|\mathbf{Z}\| = \|\mathbf{Z}\|\,(f, d)$	$\|\mathbf{Z}\| = 1.5 \cdot 10^3 - 1.4 \cdot 10 d - 2.0 \cdot 10^{-2} f + 7.4 \cdot 10^{-2} d^2$	0.87

Table 3.4: Comparison between different simulation setups and measurements at 20 Hz.

$$SS_{err} = \sum_i (y_i - f_i)^2 \tag{3.15}$$

$$SS_{tot} = \sum_i (y_i - \mu)^2 \tag{3.16}$$

with y_i and f_i being simulated and predicted values, and μ the mean of the simulated data.

Although the analytical expression, as seen in paragraph 3.3.3, gives zero impedance values for flat electrodes at high frequencies, the evaluated $\mathbf{R}^2$ value is still high in this case. This is explained by the fact that the impedance at these frequencies is much smaller than at lower frequencies and therefore has a smaller impact on the coefficient of determination.

3.3.6 Discussion

Flat and micromachined multipoint spiked electrodes have been simulated in order to investigate their sensitivity to geometrical parameters and skin properties variability. It has been shown how flat electrodes are more susceptible to variations when the most superficial layer of skin is not constant, while spiked electrodes, due to their ability to go through this layer, are immune to such changes. Flat electrodes are also influenced by the mechanical setup that can reduce the contact area, but the same is true for micromachined multipoint spiked electrodes as different pressures can result in different penetration depths and hence different contact

impedances. Although FEM EM simulations explain the relationship between electrode geometries and contact impedance, biological effects cannot be modeled and thus it is crucial to explore new ways to measure contact impedance while performing clinical EEG and EIT. Finally, analytical expressions are given as a way to quickly estimate the contact impedance. These were more successful at fitting the spiked electrodes than the flat electrodes, which are influenced by the capacitive nature of the stratum corneum.

Conclusions

The work of the present thesis was focused on the implementation of microelectronic voltage sensing devices, with the purpose of transmitting and extracting analog information between devices of different nature at short distances or upon contact.

Initally, chip-to-chip communication has been studied, and circuitry for 3D capacitive coupling has been implemented. Such circuits allow the communication between dies fabricated in different technologies. Due to their novelty, they are not standardized and currently not supported by standard CAD tools. In order to overcome such burden, a novel approach for the characterization of such communicating links has been proposed. This results in shorter design times and increased accuracy. A chip-to-chip memory interface prototype has been developed with the aid of the proposed flow, with an operating frequency of 250 MHz achieving a bandwidth of 32Gbit/sec, although it has been shown that this is limited by the ARM processor, while the chosen geometry would allow for a higher operating frequency of 1.2 GHz.

Communication between an integrated circuit (IC) and a probe card has been extensively studied as well. Today wafer probing is a costly test procedure with many drawbacks, which could be overcome by a different communication approach such as capacitive coupling. For this reason wireless wafer probing has been investigated as an alternative approach to standard on-contact wafer probing. The new approach eliminates the damage caused by the probes to the devices under tests, and allows higher testing parallelism. A CMOS 90nm test chip and a wireless probe card have been implemented as a proof-of-concept.

At last, interfaces between integrated circuits and biological systems have been investigated. Active electrodes for combined electroencephalography (EEG) and electrical impedance tomography (EIT) have been implemented in a $0.35\mu m$ process. Such electrodes represent the first attempt to integrate EEG and EIT in the same system and could offer greater insights to the field of brain imaging. The active electrode performs single-ended amplification thus allowing for maximum flexibility in terms of system configuration, as an arbitrary number of electrodes can be used, with the addition of an electrode at any given time. In such setup subtraction with the reference signal is only performed in the back-end, thus not requiring the additional reference wire to be fed to each electrode. Moreover the number of wires has been minimized by sharing the analog outputs and supply on a single wire, thus implementing electrodes that require only 4 wires for their operation (analog supply and signals, ground, digital data, digital clock), as the digital supply is generated on the electrode PCB with the aid of a zener diode and the data signal. Minimization of wires reduces the cable weight and thus limits the patient's discomfort. In single-ended amplification the common mode rejection ratio is directly related to the loop gain accuracy, and it decreases as the loop gain is increased. It has been shown how this is directly related to the open loop response of the readout amplification circuit, and in the presented implementation a CMRR larger than 60 dB has been achieved for both EEG and EIT, along with a total input referred noise of $0.35\mu V[RMS]$ for EEG only acquisition or $0.7\mu V[RMS]$ when EIT is performed simultaneously.

The physical channel for communication between an IC and a biological medium is represented by the electrode itself. As this is a very crucial point for biopotential acquisitions, large efforts have been carried in order to investigate the different electrode technologies and geometries. An electromagnetic model is finally presented in order to characterize the properties of the electrode to skin interface. It has been shown how a dry spiked electrode is mostly immune to variations in the more superficial layer of the skin, the stratum corneum, while a same size flat electrode exhibits a very high variability and is hence more prone to the introduction

of undesired artifacts during acquisition.

The presented work has investigated analog signal acquisition and conditioning between heterogeneous medias. As the heterogeneity of the two medias increases, the acquisition is made more complex as new effects need to be considered. The presented near-field capacitive communication schemes could be implemented for other applications, such as sensing internal nodes in ICs for testing or debugging purposes, while the presented techniques for biopotential acquisition could be extended to different biological systems, such as electrical impedance myography or electrocardiography. Furthermore, as the problem of contact impedance in dry electrodes is addressed with new micromachined electrodes, wireless application for long-term monitoring of EEG could be developed, thus allowing for the study of human brain activity during every day duties, such as physical activity, work or sleep without the confinement of a medical lab.

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