ALMA MATER STUDIORUM - UNIVERSITÀ DI BOLOGNA

ARCES - ADVANCED RESEARCH CENTER ON ELECTRONIC SYSTEMS
FOR INFORMATION AND COMMUNICATION TECHNOLOGIES "E. DE CASTRO"

DOTTORATO DI RICERCA IN TECNOLOGIE DELL'INFORMAZIONE

CICLO XXIII - ING-INF/01

Physical Models for Numerical Simulation of Si-Based Nanoscale FETs and Sensors

Tesi di Dottorato

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Esame Finale: anno 2011

Alma Mater Studiorum - Università di Bologna
FACOLTÀ DI INGEGNERIA

Dottorato di ricerca in Tecnologie dell'Informazione

Ciclo XXIII (Anni accademici 2008-2010)

Settore scientifico disciplinare ING-INF/01

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To my family

Contents

List of symbols and abbreviations

Symbols

$D_{i,v}$	Carrier diffusivity
$D_{it}(E)$	Trap states energy distribution
ϵ_{Si}	Silicon dielectric constant
$\hat{\boldsymbol{\varepsilon}}$	Strain tensor
E	Energy
$E(\mathbf{k})$	Energy dispersion relation
E_{C}	Conduction band-edge
E_{eff}	Effective electric field
$E_{\mathrm{Fn},i,v}$	Subband quasi-Fermi energy
E_g	Band gap
$E_{i,v}$	Subband energy
$E_{\parallel}$	Longitudinal electric field
$E_{\perp}$	Normal electric field
E_{V}	Valence band-edge
$F^v_{1,j}$	Form factor
g_v	Valley degeneracy
$\hbar$	Reduced Plank's constant
H	Device height
I	Current
$\mathbf{J}$	Current density vector
$\mathbf{J}_{i,v}$	Subband current density vector
$\mathbf{k}$	Lattice wave vector

$k_{\parallel}$, $k_{\perp 1}$, $k_{\perp 2}$	Lattice wave vector components in the ellipsoid coordinate system
k_1, k_2, k_3	Lattice wave vector components in the device coordinate system
k'_1, k'_2, k'_3	Lattice wave vector components in the crystal coordinate system
k_B	Boltzmann constant
L	Gate length
n	Electron density
N_{depl}	Depletion charge concentration
$N_{i,v}$	Subband electron concentration
N_{inv}	Inversion-layer carrier concentration
$\hat{m}$	Effective mass tensor
m_0	Free electron mass
m_{d_v}	Valley density-of-state mass
m_l	Longitudinal effective mass
m_t	Transverse effective mass
m_x	Transport effective mass
m_y	Width effective mass
m_z	Quantization effective mass
$\hat{\mu}_{\text{eff}}$	Effective mobility tensor
$\hat{\mu}_v$	Valley effective mobility tensor
μ_{top}	FinFET top-side mobility
μ_{lateral}	FinFET lateral-side mobility
N_A	Acceptor doping concentration
N_D	Donor doping concentration
p_v	Valley population
ϕ	Electrostatic potential
ϕ_s	Surface electrostatic potential
ψ	Wave function
q	Electron elementary charge
$\mathbf{r}$	Position vector
$\Re_{B \leftarrow A}$	Rotation matrix from the coordinate system A to the coordinate system B
ρ	Charge density
$\hat{\boldsymbol{\sigma}}$	Mechanical stress tensor
t_{IL}	Interfacial layer thickness
t_{ox}	Gate oxide thickness
t_{Si}	Silicon film thickness
τ_{AC}	Acoustic phonon average momentum relaxation time

τ_{CS}	Coulomb average momentum relaxation time
$\tau_{\delta t_{\mathrm{Si}}}$	Thickness fluctuations average momentum relaxation time
τ_{it}	Interface states average momentum relaxation time
τ_{OP}	Optical phonon average momentum relaxation time
τ_{PS}	Phonon average momentum relaxation time
τ_{RCS}	Remote Coulomb average momentum relaxation time
τ_{RPS}	Remote phonon average momentum relaxation time
τ_{RSR}	Remote surface-roughness average momentum relaxation time
τ_{SP}	Surface phonon average momentum relaxation time
τ_{SR}	Surface-roughness average momentum relaxation time
$\hat{T}$	Kinetic energy operator
T	Lattice temperature
U	Potential energy
V	Voltage
W	Device width
W_v	Valley carrier distribution effective width
$\zeta_{i,v}$	Subband electron eigenfunction

Abbreviations

1D	One-dimensional
2D	Two-dimensional
2DEG	Two-dimensional electron gas
2DHG	Two-dimensional hole gas
3D	Three-dimensional
BOX	Buried oxide
CCS	Crystal coordinate system
CMOS	Complementary metal-oxide-semiconductor
DCS	Device coordinate system
DG	Double-gate
DIBL	Drain induced barrier lowering
DPCP	Diphenylchlorophosphate
ECS	Ellipsoid coordinate system
EOT	Equivalent oxide thicknesses
FET	Field Effect Transistor
GAA	Gate-All-Around

HH	Heavy hole
I_{ON}	On-current
I_{OFF}	Off-current
LH	Light hole
MOSFET	Metal-oxide-semiconductor field-effect transistor
MRT	Momentum relaxation time
MuG	Multi-gate
NR	Nanoribbon
NW	Nanowire
RCS	Remote Coulomb scattering
RPS	Remote phonon scattering
RSS	Remote surface-roughness scattering
OP	Organo-phosphorus compounds
SCE	Short-channel effect
SG	Single-gate
SiNR	Silicon nanoribbon
SiNW	Silicon nanowire
SOI	Silicon-on-insulator
SS	Inverse sub-threshold slope
TABINOL	3-(4-ethynylbenzyl)-1, 5, 7-Trimethyl-3-AzaBIcyclo [3.3.1] Nonane- 7-methanOL
TCAD	Technology Computer-Aided-Design
UTB	Ultra-thin body

Abstract

To continuously improve the performance of metal-oxide-semiconductor field-effect transistors (MOSFETs), innovative device architectures, gate stack engineering and mobility enhancement techniques are under investigation. Performance will also derive from heterogeneity, coming from the increasing diversity of functions integrated on complementary metal-oxide-semiconductor (CMOS) platforms. For example, new architectural concepts and technological approaches are being studied in the field of nanosensing.

In this framework, new physics-based models for Technology Computer-Aided-Design (TCAD) simulation tools are needed to accurately predict the performance of upcoming nanoscale devices and to provide guidelines for their optimization. In this thesis, advanced physically-based mobility models for ultrathin body (UTB) devices with either planar or vertical architectures such as single-gate silicon-on-insulator (SG-SOI) field-effect transistors (FETs), double-gate FETs, FinFETs and silicon nanowire FETs, integrating strain technology and high-κ gate stacks are presented. The effective mobility of the two-dimensional electron/hole gas in a UTB FETs channel is calculated taking into account its tensorial nature and the quantization effects due to both the application of a transverse electric field and the structural confinement. All the scattering events relevant for thin silicon films and for high-κ dielectrics and metal gates have been addressed and modeled for UTB FETs on differently oriented substrates. The effects of mechanical stress on (100) and (110) silicon band structures have been modeled for a generic stress configuration. The resulting analytical models, based on physical insights and theoretical analyses, have been thoroughly calibrated on available experimental data. Finally, they have been combined to provide a unified compact mobility model for electrons and holes, which has shown to give a correct interpretation of the mobility features originating both in planar and non-planar post-CMOS devices. In addition, the effective mobility models have been incorporated into a quantum drift-diffusion (QDD) simulation tool, addressing the 2D coupled Schrödinger-Poisson equations on the device cross-sections normal to the transport direction and the 1D drift diffusion equation for the current flow. The

QDD simulator has been extended to accommodate different surface orientations by means of a generalized effective-mass approach. Extensive simulation studies have been carried out to investigate different architectural and geometrical solutions for the future technology nodes. Finally, starting from the effective mobility models, local mobility models have been developed, in order to allow the easy inclusion in commercial TCAD tools.

Beyond-CMOS nanostructures are of interest not only to extend the FET scaling process, but also to develop innovative sensor applications. Benefiting from properties like large surface-to-volume ratio and extreme sensitivity to surface modifications, silicon-nanowire-based sensors are gaining special attention in research. In this thesis, emphasys is given to the silicon nanowire technology for biological and chemical detection. A comprehensive analysis of the physical effects playing a role in the detection of gas molecules is carried out by TCAD simulations combined with interface characterization techniques. The complex interaction of charge transport in silicon nanowires of different dimensions with interface trap states and remote charges is addressed to correctly reproduce experimental results of recently fabricated gas nanosensors.

Sommario

Al fine di migliorare costantemente le prestazioni elettriche dei transistori ad effetto di campo (*field effect transitor*, FET) di tipo metallo-ossido-semiconduttore (MOSFET), si stanno attualmente indagando nuove architetture, strutture di gate innovative e tecniche per migliorare la mobilità dei portatori di carica. L'aumento delle prestazioni proviene inoltre dalla eterogeneità, derivante dalla crescente diversità di funzioni integrate nelle piattaforme di tipo metallo-ossido-semiconduttore complementare (CMOS). Ad esempio, si stanno studiando nuove scelte architetturali e approcci tecnologici nel campo del nano-rilevamento.

In tale contesto, si necessita di nuovi modelli fisici per simulazioni TCAD (*Technology Computer-Aided- Design*), al fine di predire con accuratezza le prestazioni dei futuri dispositivi su scala nanometrica e di fornire linee guida per la loro ottimizzazione. In questa tesi si presentano modelli di mobilità su base fisica avanzati per dispositivi a film ultra-sottile (*ultrathin body*, UTB) con architettura sia planare che verticale, come il transistore a singolo gate realizzato in tecnologia SOI (*silicon-on-insulator*), il transistore a doppio gate, il transistore FinFET e il transistore basato su nanofilo di silicio (*silicon nanowire*), che integrano stress meccanico e strutture di gate ad alta costante dielettrica. La mobilità efficace del gas di elettroni/lacune bidimensionale nel canale di un transistore a film sottile è calcolata tenendo conto della sua natura tensoriale e degli effetti di quantizzazione dovuti sia all'applicazione di un campo elettrico nella direzione trasversale al dispositivo sia dal confinamento strutturale. I meccanismi di collisione rilevanti nei film sottili di silicio e in presenza di dielettrici ad alta permittività e gate metallici sono modellati per dispositivi UTB con differenti orientazioni del substrato. Gli effetti dello stress meccanico sulle strutture a bande del silicio (100) e (110) sono modellati per una generica configurazione di stress. I risultanti modelli analitici, che si basano su una visione fisica e su analisi teoriche, sono stati accuratamente calibrati sui dati sperimentali disponibili. Infine, sono stati combinati in un modello di mobilità compatto per elettroni e lacune, il quale ha dimostrato di interpretare correttamente le caratteristiche della mobilità in dispositivi post-CMOS sia di tipo planare che non-planare. In aggiunta, i modelli

di mobilità efficaci sono stati incorporati in un simulatore del trasporto ohmico-diffusivo quantistico (QDD), che risolve le equazioni di Schrödinger e Poisson 2D accoppiate in una sezione del dispositivo trasversale alla direzione del trasporto e l'equazione ohmico-diffusiva per il flusso di corrente elettrica. Il simulatore QDD è stato adattato a differenti orientazioni cristallografiche attraverso un approccio generalizzato per il calcolo delle masse efficaci. Si sono eseguiti studi approfonditi attraverso simulazioni per investigare diverse soluzioni architetturali e geometriche per i futuri nodi tecnologici. Infine, a partire dai modelli di mobilità efficace, si sono sviluppati modelli di mobilità locale, allo scopo di consentirne una facile integrazione in simulatori TCAD commerciali.

Le nanostrutture post-CMOS sono di interesse non solo per estendere il processo di *scaling* dei dispositivi, ma anche per sviluppare nuove applicazioni per sensori. Beneficiando di proprietà come un elevato rapporto superficie-volume e un'estrema sensibilità alle variazioni superficiali, i sensori basati su nanofili di silicio stanno acquisendo notevole interesse in ricerca. In questa tesi, si da' enfasi alla tecnologia a nanofili di silicio per il rilevamento biologico e chimico. Un'analisi dettagliata degli effetti fisici che giocano un ruolo nel rilevamento di molecole di gas è effettuata mediante simulazioni TCAD combinate con tecniche di caratterizzazione dell'interfaccia. Viene affrontata la complessa interazione del trasporto di carica nei nanofili di silicio di diverse dimensioni con gli stati trappola all'interfaccia per riprodurre correttamente i risultati sperimentali di nanosensori fabbricati di recente.

Introduction

In the last fifty years, integrated circuits (ICs) have driven the information technology revolution. Complementary metal-oxide-semiconductor (CMOS) is the technology that makes it possible to integrate digital and analog circuitry in ever-smaller silicon chips that lie at the heart of all the electronic products, from personal computer to mobile phones and from electronic stability systems in cars to miniature medical devices. The main actor of this improvement has been the metal-oxide-semiconductor field-effect transistor (MOSFET), due to its ultra-high scalability. However, the request for increasing performance and reduced area occupancy pushes the scaling process every day closer to its physical limits. Innovative device structures, gate stack materials, strain engineering and unconventional surface orientations have been therefore proposed and investigated. The purpose is to overcome the limitations that nowadays nanoscale MOSFETs experience, i.e., short channel effects and gate leakage.

In Fig. 1 the Overall Roadmap Technology Characteristics (ORTC) of the International Technology Roadmap for Semiconductors (ITRS) 2010, is reported, showing present and future trends in nanoelectronics. Ultrathin body (UTB) devices with either planar or vertical architectures such as single-gate fully depleted silicon-on-insulator (FDSOI) field-effect transistors (FETs) and multi-gate (MuG) FETs are the most promising candidates for the future technology nodes. In fact, UTB FETs enable better electrostatic control of the channel, hence a more aggressive scalability, reduced leakage currents, and enriched functionality. Nevertheless, in order to scale UTB FETs down to the ultimate technology nodes, the silicon body needs to be thinned down to a few nanometers to suppress short channel effects, thus raising a concern on device variability due to statistical process fluctuations and charge transport limitations. Carrier mobility is indeed a sensitive function of the silicon-body thickness.

In the last few years, gate oxide thicknesses have been reduced to about 1 nm as demanded by device scaling, leading to an exponential increase of the gate leakage. In addition, undesired detrimental effects on carrier mobility due to remote scattering effects have been observed. Therefore, the study of high-κ di-

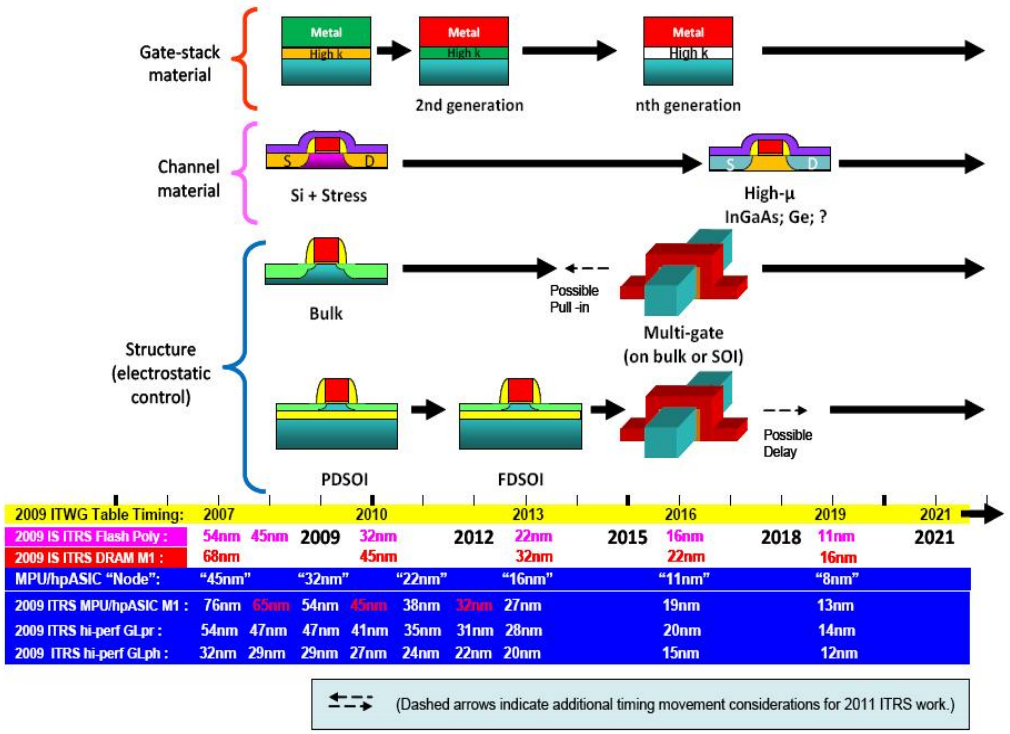

Figure 1: *Overall Roadmap Technology Characteristics (ORTC) of the International Technology Roadmap for Semiconductors (ITRS) 2010. Graphical trends, including overlay of 2009 industry logic "nodes" and ITRS trends for comparison, are shown [1].)*

electrics to replace SiO_2 is motivated on one side by the necessity of reducing the gate leakage, and, on the other side by the additional carrier mobility degradation that has regularly been reported for high-κ-based gate stacks due to remote scattering events. Metal-gate electrodes are also investigated to overcome the polysilicon depletion effect and for compatibility with high-κ dielectrics. Again, effects on the channel effective mobility have been observed.

Most of the recently proposed architectural solutions and materials for continuing device scaling have been demonstrated to negatively affect the carrier mobility in the channel. On the other hand, carrier mobility has been proven to play an important role on device performance even for ultrashort gate lengths. Therefore, several techniques to optimize carrier mobility, such as strain engineering and suitable surface orientations of the channel material are being studied. Furthermore, structures such as rectangular SiNW-FETs or FinFETs usually exhibit vertical transport on unconventional crystallographic planes. Thus, a deep comprehension of the physical details related with the different crystallographic orientations is required.

In this variegated framework, new physical models for Technology Computer-

Aided-Design (TCAD) simulation tools are needed, to provide guidelines for the optimization of upcoming nanoscale devices. In the process of development of novel technologies and designs, the use of TCAD is of fundamental importance for reducing time and investments costs. Many are the possible levels of abstraction going down from compact models for circuit simulations to more physics based models for the analysis of transport in single devices.

In the first and main part of this thesis, the aim has been developing physically-based models for TCAD simulation tools, necessary for the design and study of advanced nanoelectronic devices. In particular, since all the innovative technology solutions described above positively or negatively impact the low-field carrier mobility, and since its importance on device performances, accurate mobility models are needed. Although the mobility concept in short-channel FETs becomes questionable because of the strong influence of quasi-ballistic transport, and the fundamental relationship between low-field mobility and drive current in such devices is still not well understood, the device transport properties are traditionally related to the low-field carrier mobility measured in long-channel devices. Thus, physically-based mobility models are essential for interpreting experimental mobility data.

When developing a simulation tool, importance has to be given to the trade-off between the accuracy in the physical description and the required computational burden. Modeling complex physical effects, which are inherently affected by a wide variety of physical mechanisms by means of full physical calculations would be very expensive in terms of computational time and resources. As an alternative physics-based analytical models translate complex numerical calculations into simple analytical expressions, where a number of parameters are allowed to vary to best fit the experiments and/or theoretical predictions.

Moreover, the preference is always on analytical physics-based models rather than empirical one. The hope is that a good physics-based model can be made scalable to different gate lengths and widths without requiring table-model based interpolation. Likewise, the emerging of mobility anisotropy effects in UTB FETs due to the breaking of the 3D symmetry enforces the requirement of good electron and hole mobility models for TCAD simulations. The consideration of every single physical effect, such as subband splitting, valley repopulation, scattering mechanisms and the like, is important to keep track of the underlying physics and also helps in the extraction of empirical parameters, when these are needed to express complex effects in simplified form, as well as unknown physical parameters. So doing, it is not needed to extract parameters by a global fitting, which most likely would generate unphysical results.

Therefore, the efforts have been focused on the realization of physically-based analytical mobility models for electrons and holes in planar and vertical UTB FETs. The physical mechanisms affecting electron and hole mobility in ultrathin-

silicon films with different crystallographic orientations, and in presence of bi-axial/uniaxial strain and high-κ dielectrics have been addressed, modeled and calibrated on available experimental data. The resulting unified model has been shown to correctly predict the low-field mobility in planar and vertical multi-gate architectures, even with complex stress configurations. A numerical simulation tool based on the self-consistent solution of the Schrödinger and Poisson equation in UTB FETs with different crystallographic orientations has been developed and used to calibrate the analytical models. In addition, the mobility models are implemented in a quantum drift-diffusion simulator addressing the 2D coupled Schrödinger-Poisson equations on the device cross-sections normal to the transport direction and the 1D drift diffusion equation for the current flow, in order to investigate the extent of the current improvements related with mobility enhancement. In commercial TCAD simulators the effective-mobility dependence on integral (non-local) carrier concentration and electric field may lead to numerical problems. Therefore, local mobility models, which depends on the local normal electric field and carrier concentration are preferred. Thus, in order to make the new mobility models suitable for commercial TCAD tools, local models are also provided.

In Chapter 1, the development of an analytical low-field electron mobility model for UTB FETs with different crystallographic orientations is presented in detail and its validation against experiments is illustrated. The Coulomb, surface-roughness and phonon scattering models for unconventional surface orientations and ultra-thin body are treated. An accurate analytical description of the energy subbands which includes non-parabolicity effects is shown to give a correct interpretation of experimental mobilities on different crystallographic orientations and channel directions, as well as of the repopulation effects in ultra-thin-silicon films. Additional effects for ultra-thin SOI, like silicon-thickness fluctuations, suppression of intervalley-phonon scattering and surface phonons are also treated. In Chapter 2, the corresponding model for low-field hole mobility is presented. It provides accurate predictions of hole mobility in SOI FETs with (100) and (110) crystallographic orientations and silicon thickness down to about 2 nm. Chapter 3 is focused on the remote scattering effects related to ultra-thin gate dielectrics and gate stacks composed of high-κ oxide and metal gates. In Chapter 4, the effects of strain are included in the mobility models for electrons and holes. Valley splitting, valley repopulation, band deformation, and scattering contributions under biaxial and uniaxial strain conditions are studied and modeled. The effects of mechanical stress on (110) planes are also addressed, which are essential for the study of mobility in vertical architectures with (110)-oriented sidewalls. The developed models are suitably combined to predict the mobility behavior in n- and p-FinFETs with complex stress configurations, showing a nice agreement with experimental data. In Chapter 5, the attention is on the mobility impact

on the on-current. A quantum drift-diffusion simulation tool, which includes the new mobility models, is used to carry out extensive simulation study of single- and double-gate UTB FETs.

The research on new architectural solutions to fulfill the request for continuing the scaling process of nanoelectronics is also meeting the need of integrating new functionalities in ICs. In particular, special attention is devoted to nanostructures which could be integrated within CMOS platforms, enabling functions that allow the world of digital computing to interact with the real world, providing conversion of non-digital as well as non-electronic information, such as chemical, mechanical, thermal, acoustic, optical and biomedical functions to digital data and vice versa. Nowadays nanodevices for the development of innovative applications with increased performance in the field of nanosensing, energy harvesting, nanocooling and RF are being thoroughly investigated. Nanotechnology can offer powerful ways to bring added value, in terms of costs, reproducibility, sensitivity, automation and new functionalities in healthcare applications such-as in-vitro diagnosis, as well as in environment control (water, air, soil), agriculture and food, defence or homeland security. A wide range of sensors is studied, such as chemical sensors, sensors for liquid and gas spectroscopy. Miniaturization enables price reduction, functionality multiplication and integration with electronics which will reduce parasitic effects, as well as ultra-high-sensitivity detection for chemical and biological applications.

The second part of this thesis (Chapter 6) is focused on the study of silicon nanowires for gas sensor applications. In these devices the surface charges exert a significant effect on the electrical conductivity. Therefore, attention is given to the modeling of interface traps and remote charges, and how they affect the device electrostatics. A TCAD simulation study, combined with experimental characterization, allowed for a correct interpretation of the experimentally observed current modulation upon exposure to gas. Furthermore, the impact of nanowire surface-to-volume ratio on sensor sensitivity is investigated, demonstrating a significant performance enhancement when the device width is shrunk below 50 nm.

Part I

MOBILITY MODELS FOR NANOSCALE MOSFETs

Chapter 1

Mobility Model for Differently-Oriented UTB SOI n-FETs.

The scaling of CMOS devices is reaching intrinsic limitations and needs new technological solutions. Ultra-thin body (UTB) devices with either planar or vertical architectures such as single-gate silicon-on-insulator (SG-SOI) FETs, double gate (DG) FETs, FinFETs and silicon nanowires (SiNWs) are the most promising candidates for fabricating sub-50-nm devices [1]. The study of the device performance requires the development of predictive physical models for carrier transport. To this purpose both mobility models [2] and enhanced drift-diffusion models which account for quasi-ballistic transport have been proposed [3]. To further improve the device performance for the future technology nodes, attention is being paid to the carrier mobility, which has been proved to play an important role on device performance even for ultra-short gate lengths [4], [5].

Several techniques to optimize carrier mobility in UTB FETs, such as strain [6] and suitable surface orientations [7], are still under investigation. Furthermore, structures such as rectangular SiNWs, FinFETs or Tri-gate FETs usually exhibit sidewall transport on the (110) crystallographic planes [8] [9] [10] [11]. Thus, a deep comprehension of the physical details related with the different crystallographic orientations is required.

In order to scale UTB FETs down to the ultimate technology nodes, the silicon body needs to be thinned below 5 nm to suppress short-channel effects, thus raising a concern on transport limitations. It has been experimentally demonstrated that electron mobility is a sensitive function of the silicon-body thickness, especially when t_{Si} is below 5 nm [12] [13] [14] [15] [16] [17].

The carrier mobility of single-gate (SG) and double-gate (DG) UTB MOSFETs has been extensively investigated, and a TCAD model has been proposed [2]. However, a TCAD model for UTB MOSFETs with unconventional surface and current-flow orientations is missing, and only experimental investigations can be found in the literature. The aim of this work is to derive a physically-based mobility model for device simulation tools which accurately predicts the low-field electron mobility in SG and DG FETs with different surface and channel orientations and silicon thicknesses as small as 2.5 nm. The mobility model presented in [2] has been modified to account for different crystallographic orientations.

In the following, a complete description of the model is provided and its validation against experiments is illustrated. Starting from a mobility formulation for bulk MOSFETs as a function of the effective transverse field, doping density, surface and channel orientations [18], a number of improvements have been added to reproduce the experiments taken on (100), (110)/⟨100⟩ and (110)/⟨110⟩ SG and DG FETs with ultra-thin silicon body.

In sections 1.1, 1.2, 1.3 and 1.4 some concepts essential for the comprehension of this thesis are introduced. In particular, in section 1.3 a Schrödinger-Poisson solver for different crystal orientations is presented. In section 1.5 the generalized mobility model is discussed. The effective inversion-layer thickness model for unconventional surface orientations and ultra-thin body is described in section 1.6; Coulomb and surface-roughness scattering models for unconventional surface orientations are treated in section 1.7; an accurate analytical description of the energy subbands which includes non-parabolicity effects is reported in section 1.8. The scattering induced by interface states is modeled in section 1.9 to improve the fitting of the (110) mobility data. Additional effects for ultra-thin SOI are shown in section 1.10, more specifically, silicon-thickness fluctuations, the suppression of inter-valley phonon scattering due to the shift of the energy minima, and surface phonons. Finally, the introduction of a simple analytical formulation allows us to include the effect of volume inversion on DG UTB MOSFETs (section 1.11). A review of the complete model is reported in section 1.12.

1.1 The Miller index notation

The Miller indices are commonly used to specify directions and planes in a crystal [19]. The Miller indices of a plane are defined as follows. First of all, three lattice vectors have to be defined. For cubic crystal systems, the lattice vectors are chosen along the edges of the crystallographic unit cell. Any crystal plane intercepts the axes in certain points. The Miller indices are determined by taking the reciprocals of these numbers and reducing them to the smallest three integers having the same ratio. The result is a triplet of integer values in parentheses $(hk\ell)$. A Miller index 0 means that the plane is parallel to the respective axis.

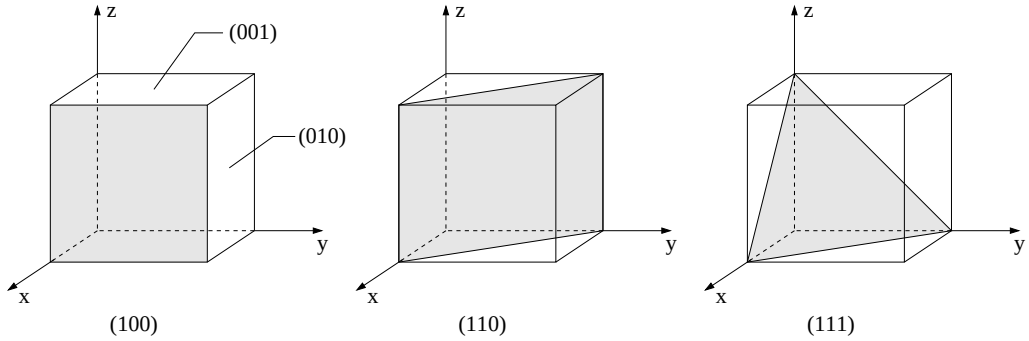

Figure 1.1: *Miller indices of some important planes.*

Negative indices are indicated with a bar written over the number or with the minus before the number.

In the conventional notation, $[hk\ell]$ with square brackets instead of round brackets, denotes a direction in the basis of the lattice vectors. The notation $\{hk\ell\}$ denotes all planes that are equivalent to $(hk\ell)$ by the symmetry of the crystal. Similarly, the notation $\langle hk\ell\rangle$ denotes all directions that are equivalent to $[hk\ell]$ by symmetry. In cubic crystal systems the Miller indices of a plane are the same as those of the direction perpendicular to the plane. Fig. 1.1 shows the Miller indices of important planes in a cubic crystal.

1.2 Bulk silicon band structure

The band structure describes the variation of the energy E with the momentum $\mathbf{k}$. Silicon is an indirect band gap material with a band gap (E_g) of approximately 1.12 eV [20]. In the effective mass approximation, the band structure close to the conduction band edge can be approximated by ellipsoidal energy surfaces and a parabolic energy dispersion $E(\mathbf{k})$. In bulk silicon the conduction band minima are located at six equivalent points near the zone boundary X along the Δ symmetry lines. Choosing the momentum coordinate system aligned with the principal axes of a generic valley, the energy dispersion reads

$$E(\mathbf{k}) = \frac{\hbar^2 k_\parallel^2}{2m_l} + \frac{\hbar^2(k_{\perp 1}^2 + k_{\perp 2}^2)}{2m_t} \ , \tag{1.1}$$

where $\mathbf{k} = (k_\parallel, k_{\perp 1}, k_{\perp 2})$. $m_l = 0.916\ m_0$ and $m_t = 0.19\ m_0$ are the longitudinal and the transverse mass, respectively, m_0 is the free electron mass and $\hbar$ the reduced Planck constant. The constant energy surfaces of all six valleys are ellipsoids of revolution grouped into three pairs placed along the principal axes $\langle 100\rangle$, as shown in Fig. 1.2. In the following, the term "valley" is often adopted referring to a valley pair.

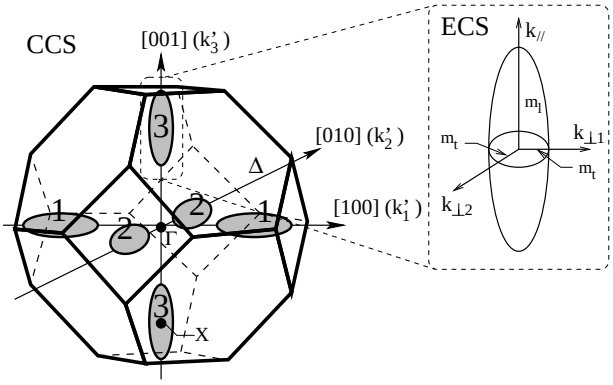

Figure 1.2: *Constant energy surfaces for the conduction band minima of silicon. Equivalent valley pairs are labeled with the same number. The silicon crystal coordinate system (CCS) and the single-ellipsoid coordinate system (ECS) are indicated.*

The valence band edges are located at the Γ point. The transport properties for the valence band are mainly affected by the properties of the heavy hole (HH) and light hole (LH) valleys. The constant-energy surfaces of HH and LH bands have complex warped shape [20].

1.3 Quantum confinement in UTB FETs

In Fig. 1.3-(A) a 3D sketch of the silicon-on-insulator (SOI) single-gate (SG) FET is shown. In the SG FET the silicon channel is sandwiched between the gate oxide (GOX) and a buried oxide (BOX), which provides vertical isolation limiting the detrimental effect of parasitic capacitances and leakage currents of the pn junctions. The short-channel effects (SCEs) consist in the loss of control of the gate on the potential profile along the channel, due to the aggressive reduction of the gate length L. The SOI technology allows the integration of multiple gates to ensure a better electrostatic control reducing SCEs. The 2D scheme of a planar DG FETs is illustrated in Fig. 1.3-(B), where two gate/oxide stacks are processed independently. Multi-gate (MuG) devices with a non-planar structure have been also proposed, such as FinFETs, where the conducting channel is formed in a thin silicon body covered by the gate stack on three sides, or gate-all-around silicon nanowire (SiNW) FETs. Although several experimental realizations have been reported during the last years for MuG-FETs, there are still many challenges associated with integration of these new structures [1]. In this chapter, the focus is on planar architectures while vertical structures will be treated later in this thesis.

Charge carriers confined in a narrow potential well does not behave classically. Increasing V_{GS} beyond the threshold voltage increases the inversion charge density

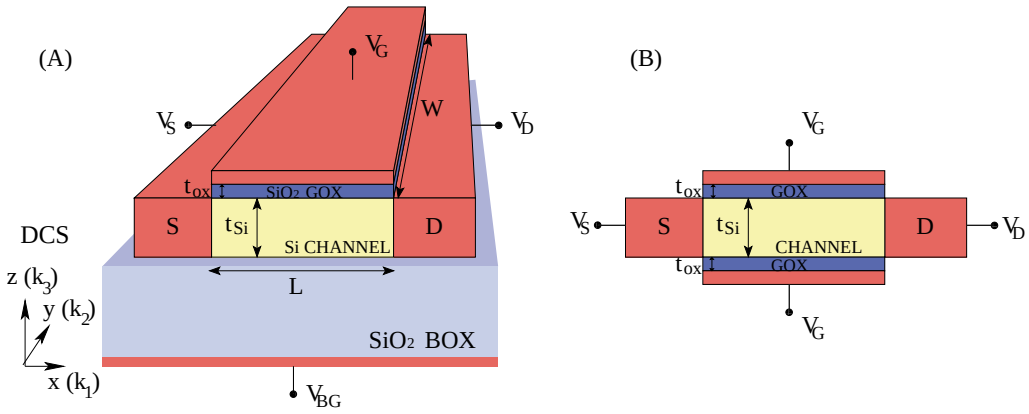

Figure 1.3: *(A) 3D schematic of the SG-SOI device structure. The different device regions are depicted with different colors. The silicon layer between the buried oxide (BOX) and the back-gate contact is not shown. The device coordinate system (DCS) is also indicated. (B) 2D cross-section of a DG-SOI FET along the transport direction.*

in the channel, which also increases the electric field perpendicular to the channel. The electric field in the inversion layer of a FET is strong enough to produce a potential well whose width in the direction perpendicular to the surface is small compared to the carrier wavelength [21]. Thus, quantization of the motion in discrete levels is expected along this direction. The energy levels of the carriers are called subbands, each of which corresponds to a quantized level of motion in the direction vertical to the interface. In addition, when considering ultra-thin body (UTB) FETs with silicon-film thickness below 10 nm, as requested by device scaling rules [1], the electron gas is structurally confined in the vertical direction, with a continuum for motion in the plane parallel to the surface. Therefore, in the thin silicon layer a quasi two-dimensional electron gas (2DEG) or hole gas (2DHG) is formed.

The calculations of the energy levels of carriers confined in a quantum well are commonly based on the following approximations [21]: i) the Hartree approximation, stating that each electron moves in the average potential produced by all other electrons, thus neglecting many-body effects; ii) in the semiconductor, the effective mass approximation is applied; iii) for the calculation of the energy levels it can also be assumed that the barrier between the insulator and the semiconductor is large enough that the envelope wave functions vanish at the semiconductor-insulator interface, which is reasonable for the Si/SiO_2 interface.

The physical model for the description of the device behavior comprises the Schrödinger and Poisson equations, namely

$$\nabla_{\mathbf{r}} \cdot (\epsilon_{\mathrm{Si}} \nabla_{\mathbf{r}} \phi) = \rho \tag{1.2}$$

$$\left(\hat{T} + U(\mathbf{r})\right)\psi = E\psi \ , \tag{1.3}$$

which are needed to realistically compute the device electrostatics. In (1.2), $\phi(\mathbf{r})$ is the electric potential, ϵ_{Si} is the silicon permittivity and ρ is the charge density, given by the sum of the contributions due to free carriers, doping concentration and other fixed charge centers, as for example charges trapped at the Si/SiO_2 interface. In (1.3), E is the total electron energy, $\hat{T}$ is the operator for the electron kinetic energy, and $U(\mathbf{r})$ is the electron potential energy.

In the following, a reference frame with the z axis normal to the Si/SiO_2 interface and current transport along the x-direction is assumed, as shown in Fig. 1.3; the y-axis is along the device width. For the sake of simplicity, it is further assumed that the FET has a translational symmetry along the width, so that 1.2 and 1.3 can be solved in the (x, z) plane only. Thus, the position vector $\mathbf{r}$ and the (x, z) coordinates are used interchangeably. The general expression for $E(\mathbf{k})$ in the device coordinate system (DCS) (k_1, k_2, k_3) reads out

$$E(k_1, k_2, k_3) = \sum_{i,j=1}^{3} \frac{\hbar^2 k_i k_j}{2m_{ij}} \ , \tag{1.4}$$

where m_{ij} are the components of the effective mass tensor.

If the potential is assumed to be a function of z only, i.e. $U(x, z) = U(z)$, it is possible to the separate the trial solution of (1.3) into a z-dependent factor $\xi(z)$, and a plane wave factor representing free motion in the xy plane [22]

$$\psi(x, y, z) = \xi(z)\exp(jk_1x + jk_2y) \ . \tag{1.5}$$

The kinetic energy operator $\hat{T}$ is obtained by replacing k_z with the quantum-mechanical operator $-j(\partial/\partial z)$. Therefore, by substituting (1.5) in (1.3), it is found that the functions ξ must satisfy the equation

$$\frac{\hbar^2}{2m_{33}}\frac{\mathrm{d}^2\xi}{\mathrm{d}z^2} + j\hbar^2\left(\frac{k_1}{m_{13}} + \frac{k_2}{m_{23}}\right)\frac{\mathrm{d}\xi}{\mathrm{d}z} + (q\phi(z) + E')\xi(z) = 0 \ , \tag{1.6}$$

where

$$E' = E - \frac{\hbar^2}{2}\left(\frac{k_1^2}{m_{11}} + \frac{2k_1k_2}{m_{12}} + \frac{k_2^2}{m_{22}}\right) \ . \tag{1.7}$$

Following Stern and Howard [22], the first derivative in the above equation can be eliminated taking

$$\xi(z) = \zeta(z)\exp\left(-j\,z\,m_{33}\left(\frac{k_1}{m_{13}} + \frac{k_2}{m_{23}}\right)\right) \ . \tag{1.8}$$

The differential equation for $\zeta(z)$ takes the form

$$\left(-\frac{\hbar^2}{2m_z}\frac{\mathrm{d}^2}{\mathrm{d}z^2} + U(z)\right)\zeta_i(z) = E_i\zeta_i(z) \ , \quad \text{with} \quad m_z = m_{33} \ , \tag{1.9}$$

where the eigenfunctions and the eigenvalues are labeled by a subscript i. The energy spectrum is given by

$$E(k_1,k_2) = E_i + \frac{\hbar^2}{2}\left(\left(\frac{1}{m_{11}} - \frac{m_{33}}{m_{13}^2}\right)k_1^2 + 2\left(\frac{1}{m_{12}} - \frac{m_{33}}{m_{13}m_{23}}\right)k_1k_2 + \left(\frac{1}{m_{22}} - \frac{m_{33}}{m_{23}^2}\right)k_2^2\right) \quad (1.10)$$

and represents constant-energy ellipses above the minimum energy E_i. The energy levels E_i for a given value of m_z generate a set of subband minima called ladder. Since the value of the quantization mass depends on the substrate orientation, so do the number and the degeneracy of the subband ladders. Obviously, if conduction band valleys have the same orientation with respect to the surface, these valleys belong to the same ladder. It is worth noting that the valleys with the largest quantization mass m_z have the lowest energy. Following a widely used convention, the subbands belonging to the ladder lowest in energy are labeled $0, 1, 2, \ldots$, those of the second ladder $0', 1', 2', \ldots$, the third ladder $0'', 1'', 2'', \ldots$, and so on [21].

In order to determine the device electrostatics, the Schrödinger equation and the Poisson equation have to be solved self-consistently by numerical methods. The electrostatic potential determined by solving (1.2), enters in (1.3) through the determination of the potential energy ($U(\mathbf{r}) = E_g/2 - q\phi(\mathbf{r})$, with q the elementary charge). On the other hand, the electron density depends on the solution of the Schrödinger equation through the square modulus of the electron wave function. Thus, a coupling between (1.2) and (1.3) is determined and an iterative self-consistent scheme has to be applied for the determination of the solution.

Eq. (1.2) is solved in the 2D domain (x, z). The boundary conditions for the Poisson equation are calculated by assuming charge neutrality and equilibrium at the contacts. Neumann boundary conditions for the potential are applied to the bottom edge of the buried oxide in SG-SOI FETs. In order to compute the quantum-mechanical charge density ρ, the 1D Schrödinger-like equation (1.9) is solved at each mesh point $\overline{x}$ along the channel, where $0 < \overline{x} < L$, and for each valley. The eigenfunctions are zero at the Si/SiO_2 interfaces. Due to the constant density of states for a 2DEG, the electron concentration for each subband belonging to the v^{th} valley is proportional to the Fermi integral of order zero, which is expressed below

$$N_{i,v} = \frac{g_v m_{d_v} k_B T}{\pi\hbar^2}\ \ln(1+\exp(-(E_{i,v} - E_{\mathrm{Fn},i,v}/k_BT)))\,|\zeta_{i,v}|^2\ . \quad (1.11)$$

where $m_{d_v} = \sqrt{m_{x_v} m_{y_v}}$ is the density-of-states effective mass of the 2DEG in the v^{th} valley, with m_{x_v} and m_{y_v} the effective masses along the transport and the width direction, respectively. g_v is the valley degeneracy ($g_v = 2$ for the silicon

conduction band), k_B is the Boltzmann constant, T the lattice temperature. $E_{i,v}$, $E_{\mathrm{Fn},i,v}$ and $\zeta_{i,v}$ are the energy, the quasi-Fermi level and the eigenfunction of the i^{th} subband belonging to the v^{th} valley, respectively.

The Schrödinger-Poisson solver in [23] has been generalized to SG- and DG-SOI MOSFETs with different crystal orientations. To this purpose, the effective masses along the quantization (m_z), the transport (m_x) and the width (m_y) directions have been computed for each valley in an arbitrary-oriented device. Three orthogonal coordinate systems are considered: the device coordinate system (DCS) (k_1, k_2, k_3), with k_1, k_2 and k_3 along the source-to-drain (i.e., transport), the device width and the channel thickness (i.e., quantum confinement) direction, respectively (see Fig. 1.3); the crystal coordinate system (CCS) (k'_1, k'_2, k'_3) , with k'_1 along the [100] direction, k'_2 along [010] and k'_3 along [001] (see Fig. 1.2); the single-ellipsoid coordinate system (ECS) $(k_\parallel, k_{\perp 1}, k_{\perp 2})$, along the principal axes of each constant energy ellipsoid (see Fig. 1.2).

Eq. (1.1) can be written as

$$E = \frac{\hbar^2}{2} \vec{k}_E^T (M_E^{-1}) \vec{k}_E \,, \tag{1.12}$$

where $\vec{k}_E = (k_\parallel k_{\perp 1} k_{\perp 2})^T$, and (M_E^{-1}) is the 3×3 diagonal matrix with m_l^{-1}, m_t^{-1} and m_t^{-1} along the diagonal.

Defining $\Re_{E \leftarrow C}$ the rotation matrix which transforms the components of a vector in the CCS $\vec{k}_C = (k'_1 k'_2 k'_3)^T$, to its components in the ECS,

$$\vec{k}_E = \Re_{E \leftarrow C} \vec{k}_C \,. \tag{1.13}$$

A second rotation matrix transforms the wave vector $\vec{k}_D = (k_1 k_2 k_3)^T$ in the DCS in the corresponding one in the CCS

$$\vec{k}_C = \Re_{C \leftarrow D} \vec{k}_D \,. \tag{1.14}$$

By combining (1.13) with (1.14) it is found

$$\vec{k}_E = \Re_{E \leftarrow D} \vec{k}_D \,, \tag{1.15}$$

where

$$\Re_{E \leftarrow D} = \Re_{E \leftarrow C} \Re_{C \leftarrow D} \,. \tag{1.16}$$

Substituting (1.15) in (1.12) it is obtained

$$E = \frac{\hbar^2}{2} \vec{k}_D^T (M_D^{-1}) \vec{k}_D \,, \tag{1.17}$$

where the inverse mass tensor in the DCS (M_D^{-1}) is

$$(M_D^{-1}) = \Re_{E \leftarrow D}^T (M_E^{-1}) \Re_{E \leftarrow D} \,. \tag{1.18}$$

The quantization mass $m_z = m_{33}$ is directly obtained from (M_D^{-1}). Following the generalized effective mass approach by Rahman [11], each conduction band ellipsoid can be mapped into an equivalent regular ellipsoid whose principal axes are oriented along the device coordinate axes x, y and z with corresponding effective masses $m_x = m_1'$, $m_y = m_2''$ and m_z, respectively, where

$$\frac{1}{m_1'} = \left(\frac{1}{m_{11}} - \frac{m_{33}}{m_{31}^2}\right) \tag{1.19}$$

and

$$\frac{1}{m_2''} = \left(\frac{1}{m_2'} - \frac{m_1'}{m_{12}'^2}\right) , \tag{1.20}$$

$$\frac{1}{m_2'} = \left(\frac{1}{m_{22}} - \frac{m_{33}}{m_{23}^2}\right) , \quad \frac{1}{m_{12}'} = \left(\frac{1}{m_{12}} - \frac{m_{33}}{m_{31}m_{23}}\right) . \tag{1.21}$$

The resulting m_x and m_y enter in Eq. (1.11), m_z in Eq. (1.9).

The Schrödinger-Poisson solver for differently-oriented devices will be extensively utilized in the development of the carrier mobility models.

1.4 Carrier mobility

The carrier mobility characterizes the ability of charge carriers to move in a semiconductor or a metal in presence of an electric field, and is defined as the ratio between the carrier drift velocity and the electric field itself. In a three-dimensional silicon lattice the drift velocity is a linear function of the electric field for low values of the field itself, then saturates for fields approaching 10^4 V/cm. Thus, the low-field mobility is a constant equal to about 1400 cm^2/Vs for electrons and 500 cm^2/Vs for holes in undoped silicon at room temperature.

Inside the inversion layer of a MOSFET the effective low-field mobility μ_{eff} is much lower than in a three-dimensional lattice, and it has been found to be universal function of the effective vertical field, as experimentally demonstrated by Takagi [24]. E_{eff} is defined as

$$E_{\text{eff}} = (q/\epsilon_{\text{Si}})(\eta N_{\text{inv}} + N_{\text{depl}}) \ , \tag{1.22}$$

with N_{inv} the carrier concentration in the inversion layer, N_{depl} the depletion charge per unit area and η is a constant equal to 1/2 for electrons and 1/3 for holes. For unconventional (110) and (111) substrate orientations it was found that a similar universal behavior is achieved when the value of η is properly adapted [24].

From a microscopic point of view it is possible to demonstrate that the mobility is proportional to the average time between two perturbations of the carrier motion. These perturbations, called scattering events, can be caused by several factors. In conventional bulk MOSFETs the most relevant are the interactions

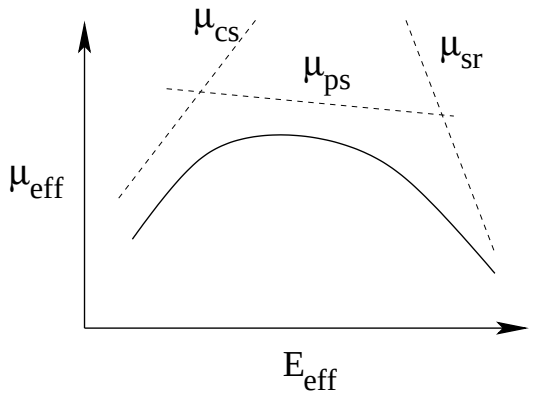

Figure 1.4: *Schematic of the universal mobility curves for bulk MOSFETs. μ_{CS}, μ_{PS} and μ_{SR} are the Coulomb-, phonon- and surface roughness-limited mobility, respectively.*

with i) lattice vibrations (phonon scattering), ii) ionized atoms of the dopant or fixed charges (Coulomb scattering), and iii) the microscopic roughness of the Si/SiO_2 interface (surface roughness scattering). The impact of the different scattering mechanisms is described in Fig. 1.4, which shows the typical dependence of the channel mobility on the effective field.

However, with the advent of the UTB SOI technology and the introduction of high-κ gate oxides and metal gates the universal mobility behavior is no longer respected, due to the detrimental effect of additional scattering mechanisms. In order to compensate the mobility loss, strained channels and suitable surface orientations are being investigated. These aspects will be widely addressed in this thesis.

Approaching the ultimate technology nodes, the device channel length is pushed down in the deca-nanometric regime. The mobility concept in ultra-short channel FETs becomes questionable because of the strong influence of quasi-ballistic transport, and the fundamental relationship between low-field mobility and conduction current in such devices is still not clear. Apart from the importance of the these aspects, the analysis of the role played by the effective mobility in short-channel FETs is beyond the scope of this thesis. The mobility concept implies a uniform device subject to a vanishing electric field in the current-flow direction. In fact, an additional scattering mechanism, optical phonon scattering, which is unimportant at low-field conditions, becomes dominant at higher fields leading to the carrier velocity saturation [25]. The conditions of device uniformity and low-field in the current-flow direction are best met with long-channel FETs, and this is why experimental data are usually obtained from such devices. Thus, the low-field mobility models presented in this thesis turn out to be essential for the interpretation of the experimental results providing guidelines for the device optimization.

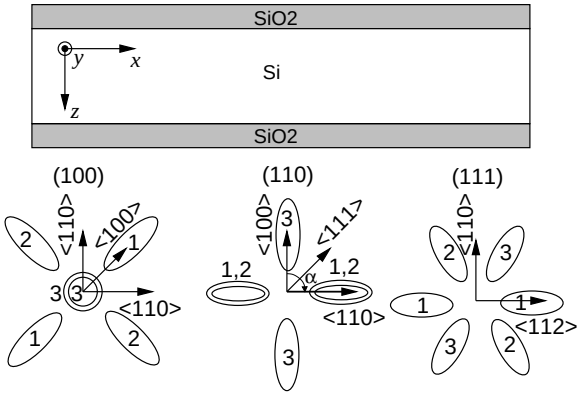

Figure 1.5: *Top: orientation of the reference axes. Bottom: in-plane minima projections for (100), (110) and (111) surface orientations. The equivalent minima are labeled with the same number. The most relevant in-plane current flow directions are also indicated.*

The effective low-field mobility μ_{eff} can be experimentally determined at low drain biases as

$$\mu_{\text{eff}} = \frac{L^2 I_{\text{D}}}{V_{\text{DS}} \int_{-\infty}^{V_{\text{GS}}} C_{\text{GC}}\, dV_{\text{GS}}} \,, \tag{1.23}$$

where L is the MOSFET length, V_{GS} and V_{DS} are the gate and drain voltages, respectively. I_{D} and C_{GC} are the measured drain current and gate-to-channel capacitance.

1.5 Generalized mobility model

Consider a silicon film on a substrate with one of the three crystallographic orientations indicated in Fig. 1.5, bottom. The z axis is set parallel to the structural confinement direction, while carrier transport occurs along the x axis. The inversion-layer quantization, due to the combined effect of structural confinement and application of a transverse electric field, causes the formation of energy ladders. More specifically, (100)-oriented FETs exhibit two energy ladders: the lower one, referred to as "unprimed", is two-fold degenerate and originates from the valleys labeled "3", while the upper one, referred to as "primed", is four-fold degenerate and is related with the valleys "1" and "2". In (110) substrates, the "unprimed" ladder is related to the valleys "1" and "2", while the primed one is related to the "3" valleys. Finally, a single six-fold degenerate ladder is formed along the (111) orientation.

In order to calculate the effective masses along the quantization (m_z), the transport (m_x) and the width (m_y) directions for each valley in an arbitrary-oriented device, the generalized effective mass approach by [11] described in section 1.3 has been implemented. Two different channel directions are analyzed for

(110)-oriented samples, namely the ⟨100⟩ and ⟨110⟩ (see Fig. 1.5). The effective masses corresponding to the analyzed cases are reported in table 1.1.

The quantization leads to unequal relative populations of the different valley pairs. Therefore, in-plane transport is generally described by a 2D tensorial effective mobility which retains the anisotropy of the single-valley effective mobilities:

$$\hat{\mu}_{\text{eff}} = \sum_{v=1}^{3} p_v \hat{\mu}_v \,. \tag{1.24}$$

where $\hat{\mu}_v$ and p_v are the mobility tensor and relative population of the v^{th} valley, respectively. A similar formulation is already available in 3D drift-diffusion transport simulation tools which handle bulk piezoresistivity and, in general, material anysotropy (see, e.g., [26] and [27]). Such tools can be directly used also in this case given that the out-of-plane (normal to the interface) mobility component plays no role and provided that the in-plane effective mobility model (1.24) is implemented. Unfortunately, this approach is unpopular in commercial TCAD tools because the effective-mobility dependence on integral (non-local) electron concentration and electric field may lead to numerical problems. As an alternative, a local mobility tensor $\hat{\mu}$ which depends on the local normal electric field $E_\perp(z)$ and carrier concentration $n(z)$ can be defined, satisfying the following equation:

$$\hat{\mu}_{\text{eff}} = \frac{\int_o^{t_{\text{Si}}} (n(z) - n_0(z)) \hat{\mu}(n, E_\perp) \mathrm{d}z}{\int_o^{t_{\text{Si}}} (n(z) - n_0(z)) \mathrm{d}z} \,, \tag{1.25}$$

where $n(z) - n_0(z)$ is the excess electron concentration in the inversion layer. It should be noted that experiments measure only the xx component of the mobility tensor.

A two-step procedure is followed in the model development. In the first step, an analytical model for the effective mobility (1.24) is defined as a function of the effective electric field E_{eff} and the inversion-charge concentration per unit area, calibrating the parameters on experiments. E_{eff} is calculated as:

$$E_{\text{eff}} = \frac{\int_o^{t_{\text{Si}}} (n(z) - n_0(z)) E_\perp(z) \mathrm{d}z}{\int_o^{t_{\text{Si}}} (n(z) - n_0(z)) \mathrm{d}z} \,. \tag{1.26}$$

In the second step, a local mobility model, which depends on $E_\perp(z)$ and $n(z)$, is provided as described in section 1.12.

The relative populations are calculated by using the Boltzmann statistics as

$$p_v = \frac{m_{d_v} \exp\left(-E_{\text{C}_v}/k_B T\right)}{\sum_{v=1}^{3} m_{d_v} \exp\left(-E_{\text{C}_v}/k_B T\right)} \,, \tag{1.27}$$

where $m_{d_v} = \sqrt{m_{x_v} m_{y_v}}$ is the density-of-states effective mass of the 2DEG in the v^{th} valley, E_{C_v} is the valley bottom energy, k_B is the Boltzmann constant

Table 1.1: *Principal effective masses for a 2DEG in (100), (110) and (111) oriented samples ($m_l = 0.916\ m_0$ and $m_t = 0.19\ m_0$)*

(Wafer)/<channel>	m_x	m_y	m_z	valleys (see Fig. 1.5)
(100)/⟨100⟩	m_l	m_t	m_t	1
	m_t	m_l	m_t	2
	m_t	m_t	m_l	3
(110)/⟨100⟩	m_t	$\frac{m_l+m_t}{2}$	$\frac{2m_l m_t}{m_l+m_t}$	1,2
	m_l	m_t	m_t	3
(110)/⟨110⟩	$\frac{m_l+m_t}{2}$	m_t	$\frac{2m_l m_t}{m_l+m_t}$	1,2
	m_t	m_l	m_t	3
(111)/⟨112⟩	$\frac{2m_t(2m_l+m_t)}{3(m_l+m_t)}$	$\frac{m_l+m_t}{2}$	$\frac{3m_l m_t}{2m_l+m_t}$	1,2
	$\frac{2m_l+m_t}{3}$	m_t	$\frac{3m_l m_t}{2m_l+m_t}$	3

and T the lattice temperature. As will be shown in section 1.8, the subband bottom energies are calculated analytically, accurately reproducing the solution of the Schrödinger-Poisson problem in the cross section normal to the transport direction. Following [28], the single-valley mobility tensor is modeled as

$$\hat{\mu}_v = \mu_v \hat{m}_v^{-1}, \quad \hat{m}_v^{-1} = \begin{pmatrix} m_0/m_{x_v} & 0 \\ 0 & m_0/m_{y_v} \end{pmatrix}, \tag{1.28}$$

where $\hat{m}_v^{-1}$ is the inverse scaled mass tensor of a 2DEG, defined for each valley v to account for the anisotropy effects induced by different in-plane crystal directions. This is expecially needed when considering the unprimed 4-fold valleys in (110) samples. Finally, μ_v is calculated accounting for the different scattering mechanisms combined via Matthiessen's rule, which assumes uncorrelated scattering mechanisms:

$$\mu_v = \frac{q}{m_0 \sum_j \tau_{v_j}^{-1}}\,. \tag{1.29}$$

In (1.29), τ_{v_j} represents the average momentum relaxation time (MRT) due to the j-th scattering mechanism for the v^{th} valley, as discussed in the next sections.

1.6 Phonon scattering

The average MRT $\tau_{\mathrm{PS},v}$ is obtained by averaging the mean relaxation times $\langle\tau_{\mathrm{PS},i,v}\rangle$ of the i^{th} subbands in the v^{th} ladder, each weighted with the population $p_{i,v}$ of the same subband

$$\tau_{\mathrm{PS},v} = \frac{\sum_i p_{i,v}\langle\tau_{\mathrm{PS},i,v}\rangle}{\sum_i p_{i,v}}\,. \tag{1.30}$$

The mean $\langle\tau_{\mathrm{PS},i,v}\rangle$ can in turn be calculated according to the study in [29] considering the effect of intravalley acoustic phonon scattering dominant at low fields.

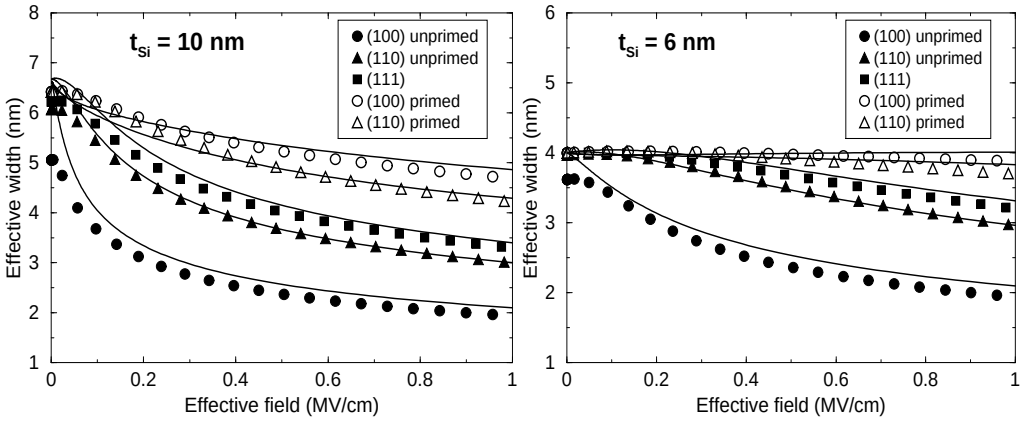

Figure 1.6: *Effective widths for the unprimed and primed subband ladders as a function of the effective field at* $t_{\rm Si} = 10$ *nm (left) and* $t_{\rm Si} = 6$ *nm (right). Symbols: numerical computations. Solid lines: Eq. (1.35).*

Intervalley scattering is not considered in view of the low-field regime, which is close to equilibrium. First, the microscopic scattering rate in the i^{th} subband of the v^{th} ladder can be written as

$$\frac{1}{\tau_{{\rm PS},i,v}(E)} = C_v m_{d_v} \sum_j F^v_{i,j} U(E - E_{j,v}) \ , \tag{1.31}$$

where C_v is a constant related to the physical parameters of the acoustic-phonon scattering mechanism. The summation extends over all subbands of the same ladder, U being the unit-step function, $E_{j,v}$ the bottom energy of the j^{th} subband, and $F^v_{i,j}$ the form factor relative to the (i,j) subbands couple

$$F^v_{i,j} = \int_0^{t_{\rm Si}} |\zeta_{i,v}(z)|^2 |\zeta_{j,v}(z)|^2 {\rm d}z \, , \tag{1.32}$$

where $\zeta_{i,v}(z)$ are the electron eigenfunctions. Then, by considering that most of the electron population of each subband occupies the subband's bottom, it is assumed $\langle \tau_{{\rm PS},i,v} \rangle = \tau_{{\rm PS},i,v}(E_{i,v})$. With this approximation, (1.30) becomes

$$\frac{1}{\tau_{{\rm PS},v}} = \frac{C_v m_{d_v}}{W_v} \ , \tag{1.33}$$

where the effective width W_v of the electron distribution relative to the v^{th} ladder has been introduced

$$W_v = \frac{\sum_i p_{i,v} \left(\sum_{j \le i} F^v_{i,j} \right)^{-1}}{\sum_i p_{i,v}} \tag{1.34}$$

and C_v are parameters reported in Appendix A.

The numerical computation of the effective widths for (100),(110) and (111) surface orientations has been carried out in equilibrium conditions ($V_{DS} \approx 0$) by

means of the Schrödinger-Poisson solver generalized to single-gate and double-gate SOI MOSFETs with different crystal orientations described in section 1.3. The calculated W_v are reported in Fig. 1.6 vs. the effective field $E_{\rm eff}$ for different surface orientations in SG-SOI FETs with $t_{\rm Si} = 10$ and 6 nm, respectively. The average effective width is modeled as:

$$W_v = \frac{W_{{\rm T}v}}{\left[1 + \left(W_{{\rm T}v}/W_{{\rm E}v}\right)^4\right]^{1/4}} \quad , \tag{1.35}$$

where

$$W_{{\rm T}v} = \frac{2}{3}\, t_{\rm Si} + W_{{\rm T}0v} \left(\frac{t_{\rm Si}}{t_{\rm Si0}}\right)^4 \left(\frac{E_{\rm eff}}{E_{\rm eff0}}\right) \tag{1.36}$$

and

$$W_{{\rm E}v} = W_{{\rm E}0v} \left(\frac{E_{\rm eff}}{E_{\rm eff0}}\right)^{-\gamma} \quad . \tag{1.37}$$

$W_{{\rm T}v}$ represents the effective width of the confined electron gas at low effective fields and small silicon thicknesses; $W_{{\rm E}v}$ is the effective width at large normal fields and thick SOI films. In (1.36) and (1.37) $t_{\rm Si0} = 10^{-7}$ cm, $E_{\rm eff0} = 10^6$ V/cm; $W_{{\rm T}0v}$ and $W_{{\rm E}0v}$ are fitting parameters calibrated on numerical results (see Fig. 1.6, solid lines) and are reported in Appendix A. By comparing the average widths of the primed and unprimed subband ladders, a slighter dependence on the electric field is observed, due to the higher energy levels which are less sensitive to it. Eq. (1.37) is the generalization to the v^{th} valley of the theoretical formulation by Ando et al. [21], relative to the effective width for a single subband (single valley) case:

$$W = \frac{8}{3}\sqrt[3]{\frac{2}{3}}\sqrt[3]{\frac{\hbar^2}{q m_z}} E_{\rm eff}^{-1/3} \, . \tag{1.38}$$

γ in (1.37), whose theoretically predicted value is 1/3, as shown in Eq. (1.38), is found to be equal to 0.29 for the (111) orientation and for the unprimed ladders of (100) and (110), while the values of 0.17 and 0.2 have been found for the primed ladders of (100) and (110), respectively (see Appendix A). As illustrated in Fig. 1.6, the difference between the unprimed and primed effective widths is more pronounced in (100) than in (110) samples. This effect can be due to the smaller difference between the quantization masses of the unprimed and primed valleys in the (110) case, leading to closer primed and unprimed energy levels.

1.7 Coulomb and surface roughness scattering

The Coulomb scattering term is modeled as

$$\frac{1}{\tau_{{\rm CS},v}} = C_{{\rm CS}_0} \left(\frac{N_{\rm inv0}}{N_{\rm inv}}\right) \left(\frac{N_A}{N_{A0}}\right)^{\sigma} \quad , \tag{1.39}$$

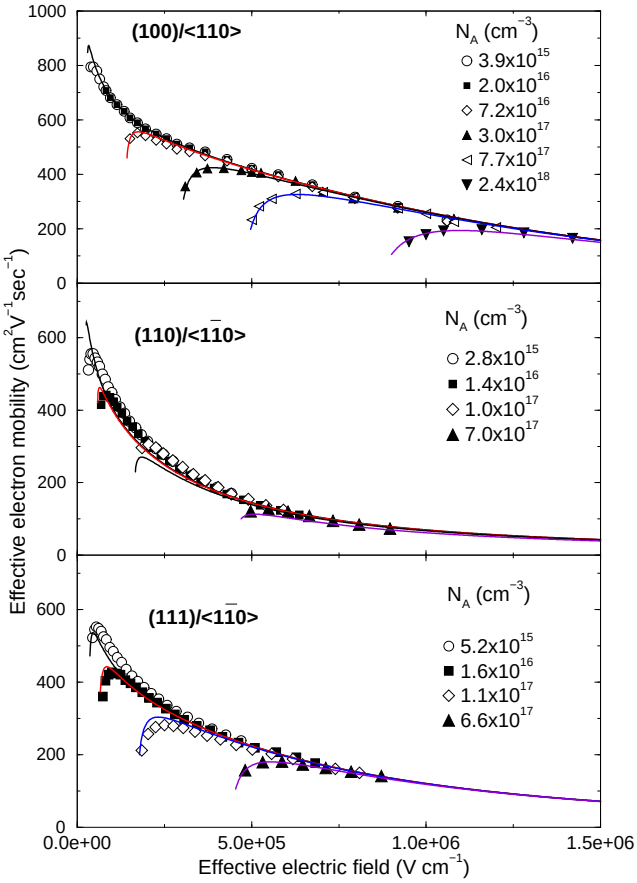

Figure 1.7: *Electron mobility in (100), (110) and (111) bulk MOSFETs vs. effective field for various substrate doping concentrations. Symbols: experiments from [24]. Solid lines: this model.*

where N_A is the substrate doping density, $N_{A0} = 10^{17}$ cm^{-3}, $N_{\rm inv0} = 10^{13}$ cm^{-2}, $C_{\rm CS_0}$ and σ are fitting parameters (see Appendix A), which are extracted by comparing the analytical model with experiments for bulk MOSFETs [24] with different N_A, as shown in Fig. 1.7. The inverse-linear dependence with the inversion-layer electron density $N_{\rm inv}$ is mainly due to the enhanced screening effect exerted by the electron charge [30]. $N_{\rm inv}$ for the bulk MOSFETs with uniform N_A measured in [24] can be calculated by inverting the usual expression

$$E_{\rm eff} = (q/\epsilon_{\rm Si})(\eta N_{\rm inv} + N_{\rm depl}) \ , \tag{1.40}$$

with η is a constant equal to 1/2 for (100) and 1/3 for (110) and (111) substrates, as suggested in [24]. In (1.40), $N_{\rm depl}$ is calculated as

$$N_{\rm depl} = \sqrt{4\epsilon_{\rm Si}\Phi_B N_A/q} \ , \tag{1.41}$$

with $\Phi_B = k_B T \log(N_A/N_i)$ the Fermi potential and $N_i = 8.765 \times 10^9$ cm^{-3} the intrinsic carrier concentration at 300 K. It is worth noting that, when implement-

ing the mobility model in a TCAD tool like, e.g., the 1D quantum drift-diffusion solver for SOI MOSFETs described in Chapter 5, $E_{\rm eff}$ and $N_{\rm inv}$ are directly obatined from the numerical results.

The theoretical formulation of surface roughness scattering under the assumption of single subband occupation reads

$$\frac{1}{\tau_{{\rm SR},v}} = C_{\rm SR0} m_{d_v} \left(\frac{E_{\rm eff}}{E_{\rm eff0}} \right)^{\delta} \tag{1.42}$$

where $C_{\rm SR0}$ is a constant and $\delta = 2$ [24]. Here the same expression is used, with $C_{\rm SR0}$ a fitting parameter (see Appendix A) and $\delta = 2.7$ for (100), 1.5 for (110) and 1 for (111) orientations, as found from experiments in Fig. 1.7. The different impact on mobility of Coulomb and surface-roughness scattering for different orientations was predicted by Monte Carlo simulations [31], and was ascribed to the different energy quantization and interface properties. This result is not surprising since the density of surface atoms and available bonds strongly depend on the crystal orientation [32], [20].

1.8 Band structures and repopulation effects

In order to compute the relative populations of the unprimed and primed ladders in (100) and (110) oriented samples and their dependence on the silicon-film thickness and the effective field, an analytical formulation based on physical considerations is developed. In (111) samples a single six-fold degenerate ladder is present; hence no repopulation occurs. For zero normal electric field (quantum well) the analytical solution of the Schrödinger equation provides the expression for the energy levels. The relative distance between the primed and unprimed subband edges reads:

$$\Delta E_{\rm CT} = E'_{\rm CT} - E_{\rm CT} = \frac{(\hbar\pi)^2}{2t_{\rm Si}^2} \left(\frac{1}{m_z^{pr}} - \frac{1}{m_z^{unpr}} \right) \quad . \tag{1.43}$$

From (1.43), the separation between the energy minima of the two ladders increases with the reduction of $t_{\rm Si}$, and electrons mostly populate the unprimed ladder. On the other hand, at large electric fields the energy minima can be theoretically calculated assuming a triangular potential well [22] as:

$$\begin{aligned} E_{{\rm CE}_v} &= \left(\sqrt[3]{\frac{9}{32}} + \sqrt[3]{\frac{9}{4}} \right) \sqrt[3]{\frac{\hbar^2 q^2}{m_{z_v}}} E_{\rm eff}^{2/3} \\ &= E_{{\rm CE0}_v} \sqrt[3]{\frac{m_0}{m_{z_v}}} \left(\frac{E_{\rm eff}}{E_{\rm eff0}} \right)^{\chi_v} \quad . \end{aligned} \tag{1.44}$$

The last expression is adopted and $E_{{\rm CE0}_v}$ and χ_v are used as fitting parameters (see Appendix A) to accurately reproduce the energy minima of bulk MOSFETs

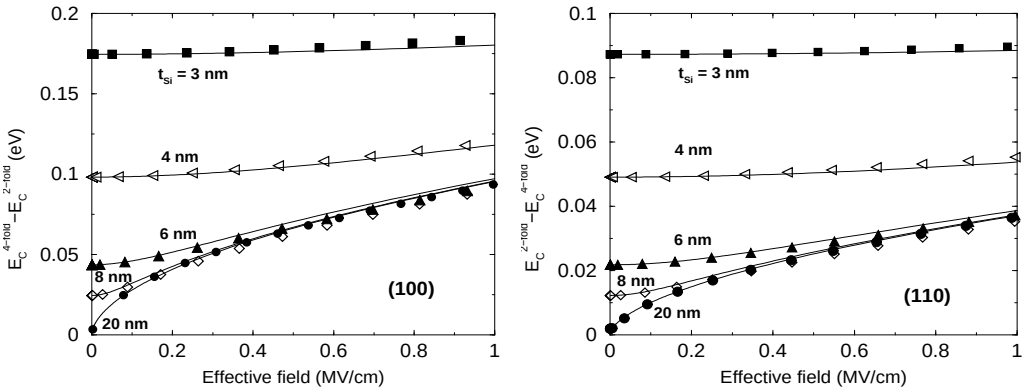

Figure 1.8: *Difference between the conduction subband edges of the 2-fold and 4-fold valleys in (100) samples (left) and (110) samples (right) vs. the effective normal field for SG-SOI FETs with different silicon thicknesses. Symbols: numerical values; solid lines: Eq. (1.45).*

on (100) and (110) substrates, as computed by the Schrödinger-Poisson solver. Indicating with ΔE_{CE} the difference between the ladder minima at high electric fields, the behavior of ΔE_{C} can be expressed as

$$\Delta E_{\mathrm{C}} = \Delta E_{\mathrm{CT}} \left[1 + (\Delta E_{\mathrm{CE}} / \Delta E_{\mathrm{CT}})^{\beta} \right]^{1/\beta} , \tag{1.45}$$

where $\beta = 3.5$. Fig. 1.8 compare Eq. (1.45) with numerical simulation results provided by the Schrödinger-Poisson solver for different silicon thicknesses, effective fields and substrate orientations. The above model for the energy difference between the subband edges of the primed and unprimed ladders allows us to compute the relative valley populations from Eq. (1.27), which are reported in Fig. 1.9 vs. t_{Si} for (100)-oriented samples. According to previous works [33], [17], a clear repopulation effect occurs at about $t_{\mathrm{Si}} = 7$ nm. The unprimed ladder, which exhibits the lower transport effective mass (see table 1.1), turns out to be fully populated for $t_{\mathrm{Si}} \leq 4\,\mathrm{nm}$, with a beneficial effect on mobility.

1.8.1 Anisotropy and non-parabolicity in the (110) orientation

Further band-structure analyses are required for (110) substrates. As already pointed out, the effective mobility in (110) samples exhibits a strong in-plane anisotropy. Consider for example a ⟨100⟩-oriented FET channel on a (110) substrate. As shown in Fig. 1.5, bottom, the unprimed ladder is the most populated one and exhibits a higher mobility due to the low transport effective mass (see table 1.1). On the contrary, if the FET channel is ⟨110⟩ oriented, the transport effective mass of the four-fold ladder is higher. This clarifies the experimental mobility reduction with respect to that of the ⟨100⟩ oriented FET channel [34].

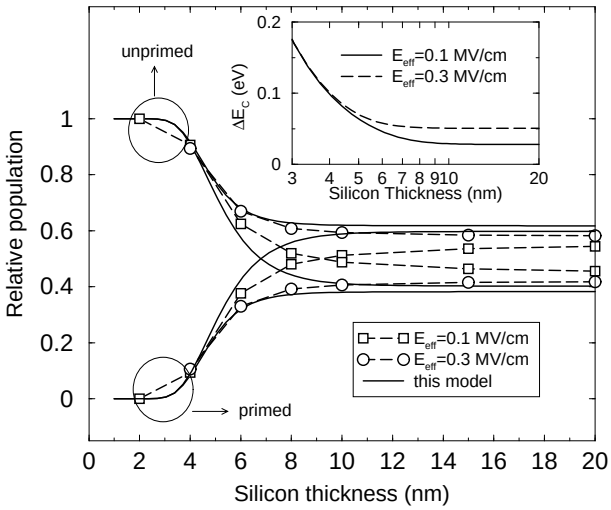

Figure 1.9: *Relative occupancy of the unprimed and primed subband ladders in (100) oriented SG-SOI samples vs. the silicon thickness for two different effective fields from (1.27). Symbols: numerically calculated relative populations; lines: this model. Inset: energy shift between primed and unprimed ladders from (1.45).*

An additional effect has been outlined in the experimental analysis carried out by Uchida in Ref. [34]. The strong nonparabolicity of the conduction band in the [110] crystalline direction, i.e. the quantization direction for the (110) orientation, leads to a smaller subband-edge difference than predicted by Eq. (1.45) between the unprimed and primed ladders for energies exceeding 100 meV. In order to account for this effect, Eqs. (1.43) and (1.45) have been modified. The nonparabolicity effects are assumed to play a relevant role in the 2-fold primed ladder, mainly because of the high energy minimum. At zero field, the lowest energy of the primed ladder in the parabolic-band approximation is

$$E'_{\mathrm{CT}} = \frac{(\hbar\pi)^2}{2t_{\mathrm{Si}}^2 m_{\mathrm{z}}^{pr}} \quad . \tag{1.46}$$

According to [35], a non-parabolic energy dispersion relationship for the conduction band minimum can be expressed as

$$E'^{\mathrm{NP}}_{\mathrm{CT}}(1 + \alpha E'^{\mathrm{NP}}_{\mathrm{CT}}) = \frac{(\hbar k_z)^2}{2m_{\mathrm{z}}^{pr}} \quad , \tag{1.47}$$

where α is the non-parabolicity factor and k_z is the wave vector component in the quantization direction. When $k_z = \pi/t_{\mathrm{Si}}$ and using (1.46), Eq. (1.47) yealds

$$E'^{\mathrm{NP}}_{\mathrm{CT}} = \frac{-1 + \sqrt{1 + 4\alpha E'_{\mathrm{CT}}}}{2\alpha} \quad . \tag{1.48}$$

The α value has been fitted on Uchida's nonparabolic energy dispersion relationship [34] shown in the inset of Fig. 1.10, and has been fixed at 3.4 eV^{-1}.

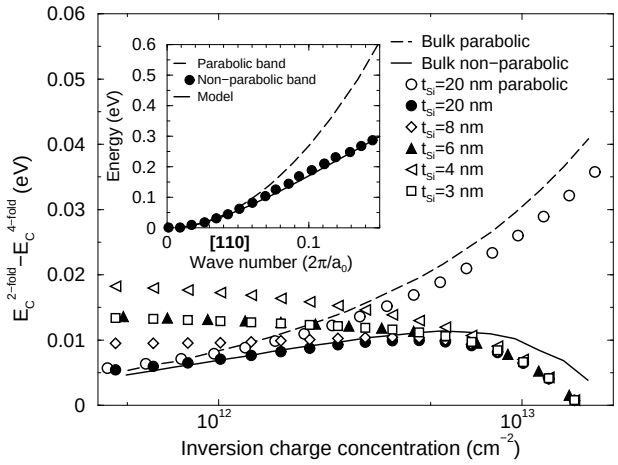

Figure 1.10: *Difference of conduction-subband edges between the 2-fold and 4-fold valleys of (110) oriented substrates vs. the inversion charge concentration for SG-SOI FETs with different silicon thicknesses after nonparabolic corrections (1.48) and (1.49). The parabolic and nonparabolic bands of a bulk MOSFET calculated in [34] are also shown. Inset: $E(k)$ relationship of energy ellipsoids "3" in Fig. 1.5 along [110] crystal orientation calculated in [34] (symbols) and from (1.48) (solid line).*

A second correction is made in order to account for nonparabolicity effects at high electric fields. From Eq. (1.44) the energy minima have an increasing trend with $E_{\rm eff}$ due to the parabolic-band approximation. In order to avoid an overestimation of $\Delta E_{\rm C}$, Eq. (1.45) is modified as follows

$$\Delta E_{\rm C}^{\rm NP} = \Delta E_{\rm C} \left[1 - \log\left(1 + \frac{N_{\rm inv}}{9 \times 10^{12}}\right)\right] \quad , \tag{1.49}$$

and reproduce the difference of the subband edges of the primed and unprimed ladders calculated in [34], as shown in Fig. 1.10. At low $N_{\rm inv}$ $\Delta E_{\rm C}^{\rm NP}$ increases by decreasing $t_{\rm Si}$ up to about 4 nm, decreases for $t_{\rm Si}$ between 4 and 2.5 nm where it becomes zero and unprimed and primed ladders cross each other (see Fig. 1.10). The effects of anisotropy and nonparabolicity on experimental mobilities for (110)/⟨100⟩ and (110)/⟨110⟩ devices are shown in Fig. 1.11. The enhancement of the 4-fold ladder population, which is favourable for the ⟨100⟩ and unfavourable for the ⟨110⟩ channel directions, has a strong impact on mobility if a parabolic band model is used (dashed lines). The nonparabolic corrections to $\Delta E_{\rm C}$ (solid lines) make the subband repopulation less effective.

As illustrated in Fig. 1.11, the application of the nonparabolic corrections to $\Delta E_{\rm C}$ is required to reproduce the experimental results. It is worth noting that the effective width in (1.34) is still based on a parabolic-band approximation, but in the low-medium $E_{\rm eff}$ range and for $t_{\rm Si} > 5$ nm, the non-parabolicity effects on carrier mobility are negligible.

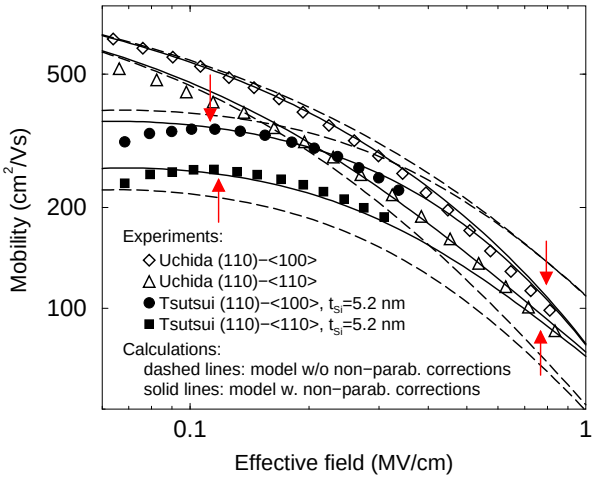

Figure 1.11: *Electron mobility in bulk and SG-SOI MOSFETs on (110) substrates vs. the effective field for* ⟨100⟩ *and* ⟨110⟩ *channel directions. Symbols: experiments from [34] and [16]. Solid lines: this model with non-parabolic corrections. Dashed lines: this model with parabolic bands. Arrows highlight the different impact on mobility of the two non-parabolic corrections in (1.48) and (1.49) for small* t_{Si} *and high electric field, respectively.*

The physical effects considered so far allow us to reproduce the experimental mobilities in [13] and [16] with t_{Si} as small as about 5 nm, as illustrated in Fig. 1.12. However, to further improve the fitting of the (110) experiments, the scattering induced by interface states in SG-SOI FETs has to be included, as explained in the next section. Unfortunately, no experimental investigations are available in the literature to validate the mobility model in the (111) SOI case.

1.9 Scattering induced by interface states

As experimentally observed in Fig. 1.12, a mobility degradation appears at very low effective fields for (110)-oriented FETs with $t_{\mathrm{Si}} = 9$ and 5.2 nm, even if the devices are practically undoped. In [17], the interface-state limited mobility μ_{it} was calculated for (100) samples in the frame of a momentum-relaxation time (MRT) approximation accounting for intersubband transitions and for the silicon-film thickness (Fig. 6 in [17]). A negligible degradation of μ_{it} has been demonstrated when the silicon film is reduced from 30 down to about 10 nm, but becomes important below 10 nm. As detailed below, when t_{Si} is shrunk below 10 nm in SOI FETs it is appropriate to model an additional scattering contribution which accounts for the mobility reduction induced by interface states

$$\frac{1}{\tau_{it,v}} = C_{\mathrm{CS}_0} \left(\frac{N_{it}}{N_{it0}}\right) \left(\frac{N_{\mathrm{inv0}}}{N_{\mathrm{inv}}}\right)^{0.7} \left(\omega \frac{t_{\mathrm{Si0}}}{t_{\mathrm{Si}}}\right)^{\varphi} \quad , \tag{1.50}$$

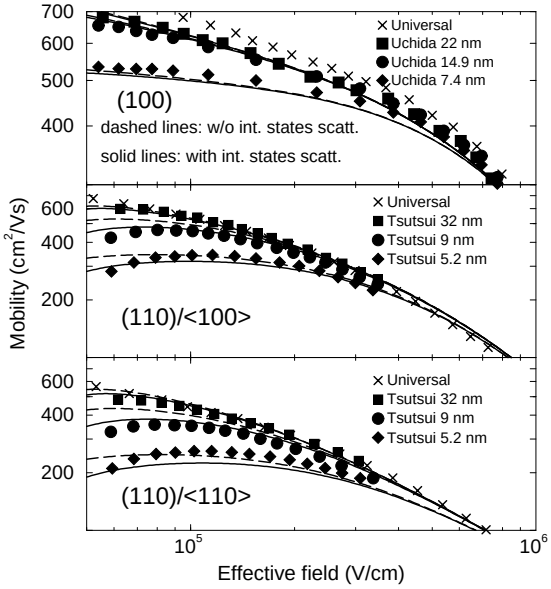

Figure 1.12: *Electron mobility in (100),* (110)/⟨100⟩ *and* (110)/⟨110⟩ *SG-SOI FETs vs. effective field for various silicon thicknesses. Symbols: experiments in [16] and [13]. μ vs. $N_{\rm inv}$ curves in [16] have been converted in μ vs. $E_{\rm eff}$ curves assuming $N_A = 5 \times 10^{15}$ cm^{-3}. Dashed lines: mobility model without the scattering induced by interface states. Solid lines: mobility model with the scattering induced by interface states as given by Eq. (1.50).*

where $N_{it0} = 5 \times 10^{10}$ cm^{-2}, φ and ω have been extracted from the $\mu_{it}(t_{\rm Si})$ curve in Fig. 6 of Ref. [17] and were found to be 1.27 (see inset in Fig. 1.14) and 112, respectively. Also, the $N_{\rm inv}^{-0.7}$ dependence in (1.50) has been extracted by the fitting in the inset of Fig. 1.14 [13], [36].

According to a recent experimental analysis on biaxially strained n-MOSFETs [37] and on highly-doped MOSFETs, [38], the $N_{\rm inv}$ dependence of μ_{it} increases when the mean distance between electrons and the Si/SiO_2 interface $\langle Z_{\rm inv} \rangle$ decreases, even in the weak inversion region. This is exactly what happens when the silicon-body thickness is strongly reduced. The result extracted from [17] of $N_{\rm inv}^{-0.7}$ is confirmed by the experimental investigation in [13] at low $t_{\rm Si}$, thus validating our approach.

In addition, it is shown in [37] that μ_{it} is degraded in strained channels since the unprimed ladder, whose electron wave functions are nearer to the interface than those in the primed ladder in view of their larger quantization mass, becomes more populated (see Fig. 1.13). When a (110) substrate is considered, the quantization masses of the unprimed and primed ladders are very close and the first eigenfunctions of the two ladders are approximately at the same distance from the interface, as illustrated in Fig. 1.13. Thus, the impact of repopulation on μ_{it} in (110) structures may be neglected and the interface state scattering can

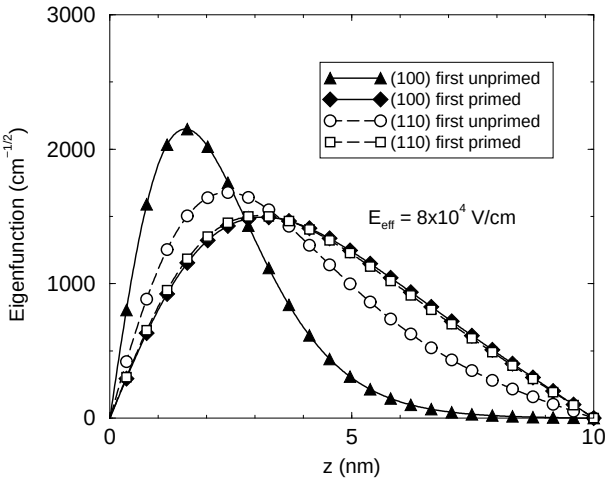

Figure 1.13: *First unprimed and primed eigenfunctions for (100) and (110) SG-SOI structures as a function of position along the z axis at* $E_{\rm eff} \simeq 8 \times 10^4$ *V/cm calculated by our Schrödinger-Poisson solver.*

be modulated only by $\langle Z_{\rm inv} \rangle$. However, the $\mu_{it}(t_{\rm Si})$ curve in Fig. 6 of [17] continues to decrease exactly as $t_{\rm Si}^{1.27}$ also when the unprimed valleys are completely populated (between 2 and 3 nm), i.e. when $\langle Z_{\rm inv} \rangle$ is simply reduced by structural confinement. Thus, the same $t_{\rm Si}^{1.27}$ dependence of μ_{it} can be used for (110) structures. The value of φ for (110) devices has been verified by a comparison with experimental mobilities from [15] at low temperature, as illustrated in Fig. 1.14. Considering that the phonon-limited mobility depends on temperature as $T^{-1.75}$ as suggested by [24], the scattering rate in Eq. (1.33) has been multiplied by 0.15 for all valleys to reproduce the experiments at 100 K. In (1.50) only ω has been adjusted with respect to the 100 K fitting ($\omega(100\,K) = 480$).

In (1.50), N_{it} represents the density of states per unit area at the interface. Recently, a number of publications reported the amount of interface states in devices with different orientations (e.g. [7], [39]) and indicated that (110)-oriented devices have an interface state density about three times larger than (100)-oriented devices. As already mentioned in section 1.7, a higher interface state density is indeed expected due to a larger atomic surface density, which increases the probability of dangling bonds or coordination defects at the interfaces. Therefore, considering that in a (100) oriented device the interface-state density is typically of the order of $5 \times 10^{10}\,{\rm cm}^{-2}$, $N_{it} = 1.5 \times 10^{11}\,{\rm cm}^{-2}$ has been used for (110) structures. Thus, this scattering contribution is found to be effective only in the (110) case as shown in Fig. 1.12 and does not remarkably influence conventionally-oriented mobilities. This is confirmed by the investigation in [17], showing that an unrealistically large amount of interface states should be needed to observe a mobility degradation at low effective field in conventionally-oriented

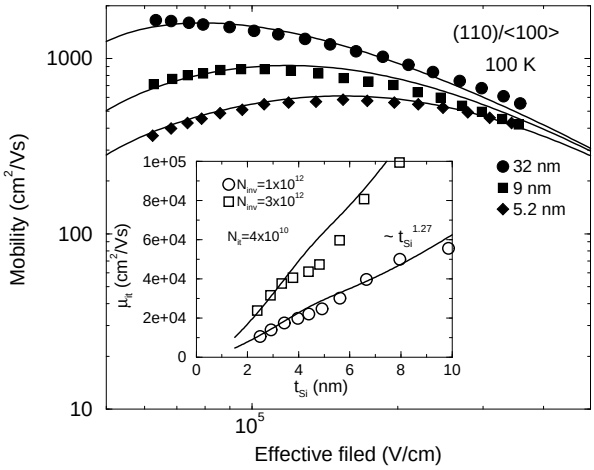

Figure 1.14: *Electron mobility vs. effective field at 100 K for (110) SG-SOI FETs. Measurements from [15] (symbols), our model with 15% of phonon scattering (solid line). Inset: μ_{it} vs. $t_{\rm Si}$ from simulations in [17] (symbols) and from our model in (1.50).*

devices.

For $t_{\rm Si} < 5\,$nm, further physical effects need to be addressed and modeled, as explained in section 1.10. Due to the lack of experimental data on (111) substrates, the mobility analysis $t_{\rm Si} < 5\,$nm is limited to the (100) and (110) orientations.

1.10 Model enhancements for $t_{\rm Si} < 5\,$nm

1.10.1 (100) substrates

1) Scattering induced by silicon-thickness fluctuations

The measured (100) mobility for $t_{\rm Si} < 5\,$nm exhibits a strong degradation which was ascribed to SOI-thickness fluctuation scattering [2], [17], [40]. In [2], it was assumed that this effect influences mobility only at low effective gate fields. Here the previous model [2] is improved by recognizing that the structural confinement induced by $t_{\rm Si}$ is important at high electric fields as well. Thus, the scattering contribution

$$\frac{1}{\tau_{\delta t_{\rm Si} h,v}} = \frac{1}{\tau_{\delta t_{\rm Si} h} \left(\frac{t_{\rm Si}}{t_{\rm Si0}}\right)^{\eta_1} \left(\frac{E_{\rm eff0}}{E_{\rm eff}}\right)} \quad , \tag{1.51}$$

is added to the formulation in [2], which reads

$$\frac{1}{\tau_{\delta t_{\rm Si} l,v}} = \frac{1}{\tau_{\delta t_{\rm Si} l} \left(\frac{t_{\rm Si}}{t_{\rm Si0}}\right)^{\eta_1} \left(C_{\delta t_{\rm Si}} \left(\frac{E_{\rm eff}}{E_{\rm eff0}}\right)^{\eta_2} + 1\right)} \quad , \tag{1.52}$$

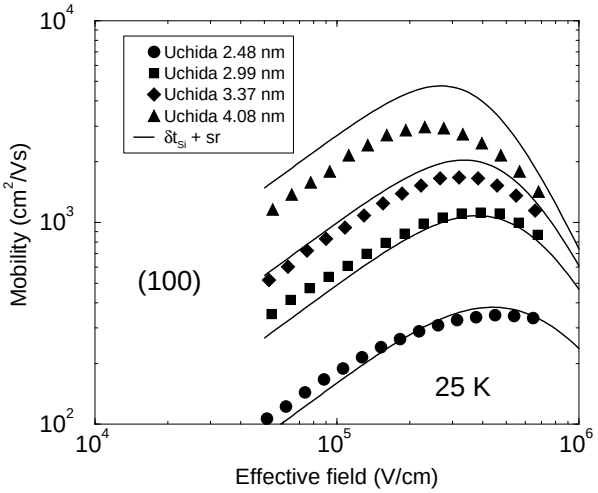

Figure 1.15: *Electron mobility vs. effective field at 25 K for SG-SOI FETs. Symbols: measurements from [12]. Solid lines: surface-roughness + silicon-thickness-fluctuation limited mobility.*

to reproduce the measurements at 25 K [12] shown in Fig. 1.15. In (1.51) and (1.52) $\tau_{\delta t_{\mathrm{Si}} l}$, $\tau_{\delta t_{\mathrm{Si}} h}$ and $C_{\delta t_{\mathrm{Si}}}$ are fitting parameters; η_1 is found to be equal to 6 as theoretically predicted [40], and η_2 is equal to 1. At 300 K only $\tau_{\delta t_{\mathrm{Si}} l}$ and $\tau_{\delta t_{\mathrm{Si}} h}$ are adjusted with respect to the 25 K fitting (see Appendix A).

2) Suppression of inter-valley phonon scattering

As highlighted in [33], another important physical effect must be considered when the silicon-film thickness is smaller than 5 nm, i.e. the suppression of inter-valley phonon scattering. In the absorption process of inter-valley f-type phonons, electrons in the unprimed ladder with an energy E reach states in the primed ladder with energy $E + E_{fp}$, where E_{fp} is the energy of the inter-valley f-type phonon. Thus, if the energy difference between the minima of the primed and unprimed ladders is higher than E_{fp}, the scattering process is suppressed. The simplest way to introduce the suppression of inter-valley phonon scattering is to model a reduction of the inverse momentum relaxation time in the expression (1.33) relative to the unprimed valleys:

$$\frac{1}{\tau_{\mathrm{PS}}^{\prime\, unpr}} = \frac{1}{\tau_{\mathrm{PS}}^{unpr}} \big(1 - f(\Delta E_{\mathrm{C}})\big) \quad . \tag{1.53}$$

Exploiting the subband structure model presented in the previous section, $f(\Delta E_{\mathrm{C}})$ in (1.53) is modeled with a combination of analytical functions:

$$f(\Delta E_{\mathrm{C}}) = \frac{f_l}{\left[1 + (f_l/f_h)^{\alpha_f}\right]^{1/\alpha_f}} \quad , \tag{1.54}$$

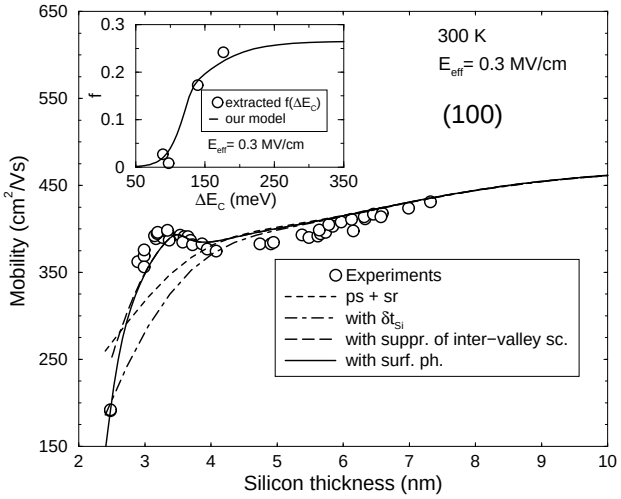

Figure 1.16: *Electron mobility vs. silicon thickness at* 300 *K for (100) SG-SOI devices. Symbols: measurements from [12]. Lines: phonon + surface-roughness limited mobility (dashed), phonon + surface-roughness + thickness fluctuation limited mobility (dashed-dotted), phonon + surface-roughness + thickness-fluctuation + surface optical-phonon limited mobility (long-dashed), total mobility (solid). Inset: function f as extracted from experiments compared with the analytical expression (1.54) vs. the difference of the energy band edges of the primed and unprimed valleys.*

with

$$f_{l,h} = \frac{f_0}{1 + \exp\left[-\left(\Delta E_{\mathrm{C}} - \Delta E_{\mathrm{C0_{l,h}}}\right)/C_{l,h}\right]} \quad , \tag{1.55}$$

where f_0, $\Delta E_{\mathrm{C0_l}}$, $\Delta E_{\mathrm{C0_h}}$, C_l and C_h are fitting parameters (see Appendix A) calibrated on experiments from [12] at $E_{\mathrm{eff}} = 0.3$ MV/cm, as depicted in Fig. 1.16, and $\alpha_f = 15$. Thus, the mobility enhancement observed in the experimental data from [12] cannot be entirely attributed to repopulation effects, as supposed in our previous work [2]. $f(\Delta E_{\mathrm{C}})$ is reported in the inset of Fig. 1.16. It may be noticed that it becomes different from zero for $\Delta E_{\mathrm{C}} > 60$ meV, which coincides with the value of E_{fp} reported in [33], and starts saturating when ΔE_{C} is between 250 and 300 meV. This energy range is the same over which the experimentally-observed mobility enhancement in biaxially-strained (100) FETs tends to saturate. Also in this case, the same physical effects come into play, namely: the enhancement of the unprimed-valley population and the suppression of inter-valley phonon scattering. In several works ([41], [42] and [43]) the saturation of mobility enhancement occurs when the percentage of Ge in the SiGe layer is about 30%. Calculating the corresponding energy shift with the commonly-used deformation potential model [44] and assuming again 30% Ge, $\Delta E_{\mathrm{C}} = 209$ meV is found, which has to be added to the quantization-induced shift (see Fig. 1.8), thus

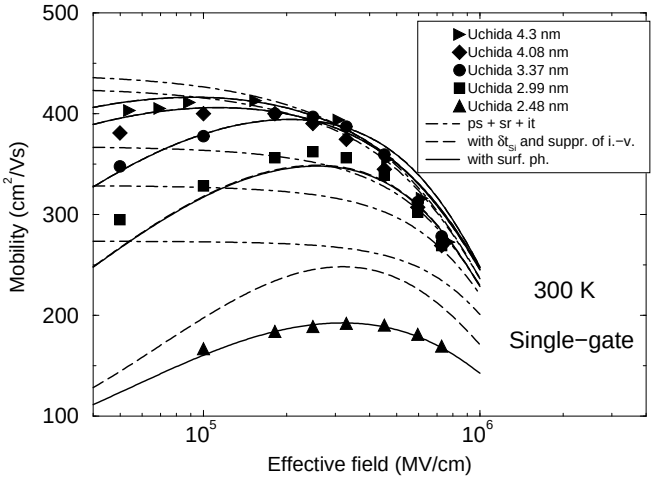

Figure 1.17: *Electron mobility in (100) SG-SOI FETs versus effective field for small silicon thicknesses. Measurements in [16] (symbols), phonon + surface roughness + interface states limited mobility (dotted-dashed), phonon + surface-roughness + interface-states + thickness-fluctuation + suppression of inter-valley phonon scattering term (dashed), total mobility (solid).*

obtaining a value between 250 and 300 meV.

Another important observation is that, according to (1.53)-(1.55), the mobility enhancement in (100) samples is expected to increase as E_{eff} increases, because of the ΔE_{C} growth with E_{eff} (see Fig. 1.8). However, when E_{eff} exceeds 0.3 MV/cm in very thin-film FETs (below 5 nm), additional scattering mechanisms limit the carrier mobility, i.e. the scattering induced by silicon-thickness fluctuations presented in the previous section and the scattering with surface optical phonons, that will be described in the next section.

3) Surface optical phonons

In order to reproduce the mobilities of devices thinner than 2.7 nm at 300 K, the surface-mode optical-phonon scattering contribution is introduced [2], namely

$$\frac{1}{\tau_{\text{SP},v}} = C_{\text{SP0}} \exp\left(-\gamma \frac{t_{\text{Si}}}{t_{\text{Si0}}}\right) \quad , \tag{1.56}$$

where C_{SP0} and γ are fitting parameters calibrated on experiments, and are reported in Appendix A. The exponential form is somewhat arbitrary, even if it reflects the fundamental physical dependencies [17]. A confirmation of the nature of this contribution, i.e. the electron-phonon interaction, is given by the good agreement of the model with experiments for $t_{\text{Si}} = 2.48$ nm at 25 K, shown in Fig. 1.15. The inclusion effects of the above scattering terms are highlighted in Fig. 1.17.

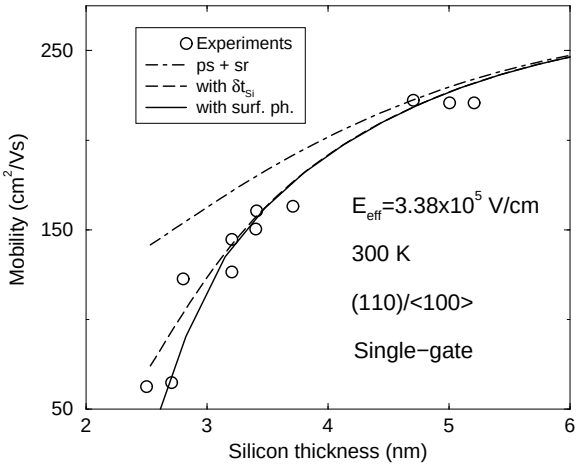

Figure 1.18: *Electron mobility vs. silicon thickness at* $300\,K$ *and* $E_{eff} = 3.38 \times 10^5$ *V/cm for* $(110)/\langle 100\rangle$ *SG-SOI devices. Symbols: measurements from [15]. Lines: phonon + surface-roughness limited mobility (dash-dotted); phonon + surface-roughness + thickness-fluctuation limited mobility (dashed); total mobility (solid).*

1.10.2 (110) substrates

1) Scattering induced by silicon-thickness fluctuations

Unfortunately, no experimental investigations are available in the literature for (110) SOI at low temperature and for $t_{\mathrm{Si}} < 5\,\mathrm{nm}$ to calibrate the scattering induced by silicon-thickness fluctuations. Thus, the same expressions (1.51) and (1.52) adopted for the conventionally-oriented SOI are used. The model parameters are calibrated directly on experiments at 300 K (see Appendix A). Specifically, η_1 is found to be equal to 7.5 and η_2 to 1.5. The different behaviors of $\tau_{\delta t_{\mathrm{Si}}}$ observed for (100) and (110) samples can be attributed to two factors: first, (100) and (110) FETs show different quantization effective masses and subband structures; next, the fabrication processes for (100) and (110) orientations generate different interface characteristics, as already mentioned in section 1.7. These considerations are supported by the fact that a single set of parameters allows us to reproduce the effective mobilities of (110) devices with different current flow directions, i.e. $\langle 100\rangle$ and $\langle 110\rangle$.

2) Suppression of inter-valley phonon scattering

The suppression of inter-valley phonon scattering should not take place in (110) FETs, because, as described above, the non-parabolicity effect limits the energy difference between the two ladders below E_{fp}, thus forbidding the suppression of inter-valley scattering and reducing carrier repopulation. This is confirmed

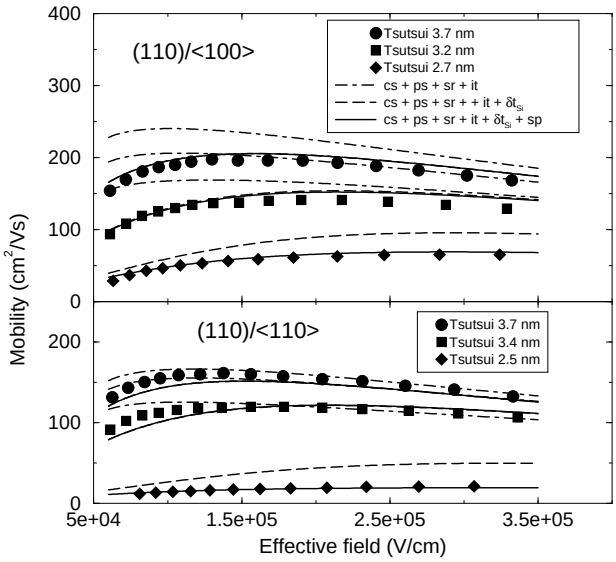

Figure 1.19: *Electron mobility in* (110)/⟨100⟩ *and* (110)/⟨110⟩ *SG-SOI FETs versus effective field for small silicon thicknesses. Measurements in [16] (symbols), coulomb + phonon + surface roughness + interface states limited mobility (dotted-dashed), coulomb + phonon + surface roughness + interface states + thickness fluctuation limited mobility (dashed), total mobility (solid).*

by the experimental mobility in (110) substrates shown in Fig. 1.18, where the curves monotonically decrease by shrinking the silicon-body thickness.

3) Surface optical phonons

The same expression (1.56) adopted for the conventional orientation is also used in this case. The model parameters are calibrated directly on experiments at 300 K and are reported in Appendix A. The inclusion effects of the above scattering terms are highlighted in Fig. 1.19.

1.11 Mobility in double-gate FETs

As already pointed out in [2], no substantial differences are experimentally observed when (100) double gate instead of single gate devices are considered to justify a modification of the mobility model. The comparison between the model and experiments is illustrated in Fig. 1.20, which shows a satisfactory agreement with experiments. In (110) substrates, a slight mobility enhancement at medium-high electric field is experimentally demonstrated for (110)/⟨100⟩ and (110)/⟨110⟩ double gate devices [15]. The reasons of this (110) mobility behavior can be attributed to the volume inversion which suppresses surface-roughness

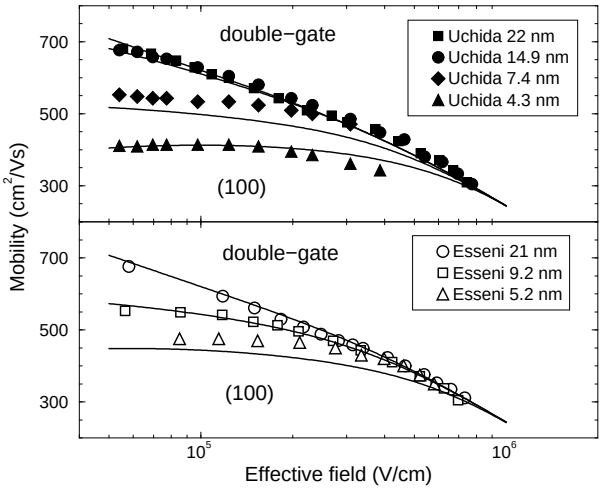

Figure 1.20: *Electron mobility in DG MOSFETs vs. effective field for various silicon thicknesses. Solid lines: this model; symbols: measurements from [13] (top) and [14] (bottom).*

scattering, because the carriers flow occurs at the center of the SOI layer, far from the Si/SiO_2 interface [15] [14] [45]. Thus, C_{SR_0} in Eq. (1.42) is corrected for a double-gate FET as

$$C_{\mathrm{SR}_0}^{\mathrm{DG}} = C_{\mathrm{SR}_0} - \left(\frac{C'_{vi}}{\exp((t_{\mathrm{Si}}/t_{\mathrm{Si0}} - C''_{vi})/C'''_{vi}) + 1} \right) \quad , \tag{1.57}$$

where C'_{vi}, C''_{vi} and C'''_{vi} are fitting parameters calibrated directly on experiments from [15] and reported in Appendix A. This fitting is shown in Fig. 1.21 for $(110)/\langle 100 \rangle$ devices at $E_{\mathrm{eff}} = 0.338 \times 10^5\,\mathrm{V/cm}$, which corresponds to $N_{\mathrm{inv}} = 6 \times 10^{12}\,\mathrm{cm}^{-2}$ for $N_A = 5 \times 10^{15}\,\mathrm{cm}^{-3}$. The same result has been obtained also for $(110)/\langle 110 \rangle$ devices (not shown).

Fig. 1.21 exhibits a mobility enhancement at $t_{\mathrm{Si}} = 5\,\mathrm{nm}$ for the double-gate device architecture, because the volume inversion is more effective in thinner silicon films [15]. However, when t_{Si} is shrunk below about 3.7 nm, silicon-thickness fluctuations and surface optical-phonons prevail on volume inversion, thus masking its effect. The resulting model is shown in Fig. 1.22, together with the experimental mobilities in $(110)/\langle 100 \rangle$ and $(110)/\langle 110 \rangle$ samples, showing a nice agreement.

As discussed above, no volume inversion is visible in (100) experimental data. An extensive investigation based on Monte Carlo simulations has been carried out in [45] on the different mobility behaviors in (100) and (110) DG structures. Due to the different subband structures of (100) and (110) substrates, the second subband of the unprimed valley in (100) samples is close to the energy of the first (lowest) primed subband while, in (110) samples, the second unprimed subband

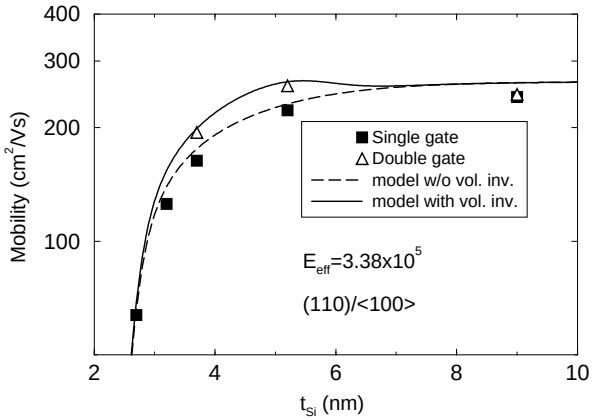

Figure 1.21: *Electron mobility vs. silicon thickness at* $300\,K$ *for* $(110)/\langle 100\rangle$ *SG and DG devices. Symbols: measurements from [15] and [16]. Dashed line: model without the correction for DG devices in (1.57). Solid line: model with the correction in (1.57).*

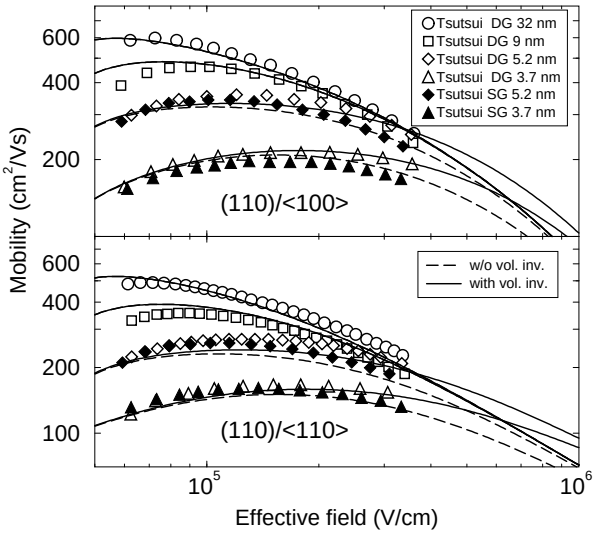

Figure 1.22: *Electron mobility vs. silicon thickness at* $300\,K$ *for* $(110)/\langle 100\rangle$ *and* $(110)/\langle 110\rangle$ *DG devices. Symbols: measurements from [15]. Dashed line: model without the correction for DG devices in (1.57). Solid line: model with the correction in (1.57).*

lies significantly higher than the lowest primed subband. When the electric field increases, the population of the second unprimed subband in (100) FETs grows in DG structures, while remaining quite the same in SG ones. This is verified by Schrödinger-Poisson simulations shown in Fig. 1.23-(B). On the contrary, the higher unprimed subbands in (110) samples remain practically empty. Thus, intersubband scattering in (100) DG-FETs between the first primed and second

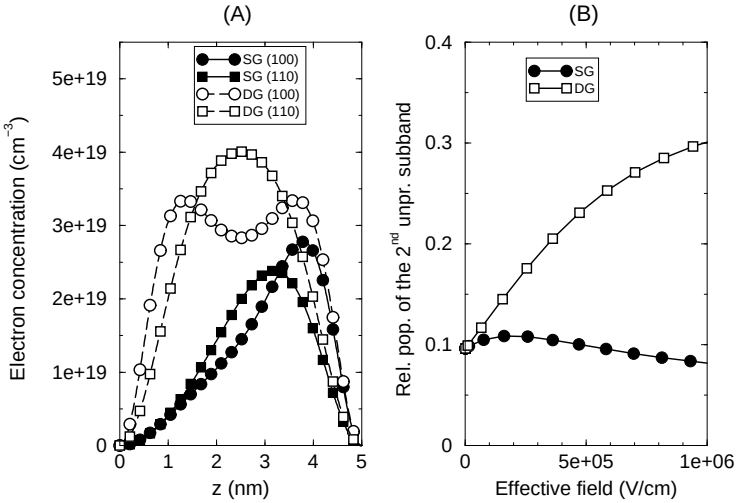

Figure 1.23: *(A) Electron concentration as a function of position along the z axis in SG and DG FETs on (100) and (110)-oriented substrates. (B) Relative population of the second unprimed subband in (100) structures with* $t_{\mathrm{Si}} = 5\,nm$ *as a function of the effective field in SG and DG devices.*

unprimed subbands completely masks the beneficial effect of volume inversion due to the high carrier density in the second unprimed subband.

Moreover, by exploiting our Schrödinger-Poisson solver, the electron concentration profiles have been investigated in the transverse direction in (100) and (110) single- and double-gate FETs. As shown in Fig. 1.23-(A), due to the different band structures, the electron distribution in (100) samples is quite close to the interface both in single- and double-gate FETs at medium-high transverse electric fields ($E_{\mathrm{eff}} = 3.5 \times 10^5\,\mathrm{V/cm}$ in the figure). Instead, it is more spread around the symmetry plane for both device types in (110) samples. These effects can qualitatively justify the stronger impact of volume inversion on (110) structures.

1.12 Review of the complete mobility model

All the scattering terms described so far need to be accounted for to calculate the effective mobility, i.e.

$$\sum_j \frac{1}{\tau_{v_j}} = \frac{1}{\tau_{\mathrm{PS},v}} + \frac{1}{\tau_{\mathrm{CS},v}} + \frac{1}{\tau_{\mathrm{SR},v}} + \frac{1}{\tau_{\delta t_{\mathrm{Si}} l,v}} + \frac{1}{\tau_{\delta t_{\mathrm{Si}} h,v}} + \frac{1}{\tau_{\mathrm{SP},v}} + \frac{1}{\tau_{it,v}} \quad . \tag{1.58}$$

The modification in (1.53) has to be applied to the phonon scattering term relative the the unprimed valleys. When considering (110) double gate devices the

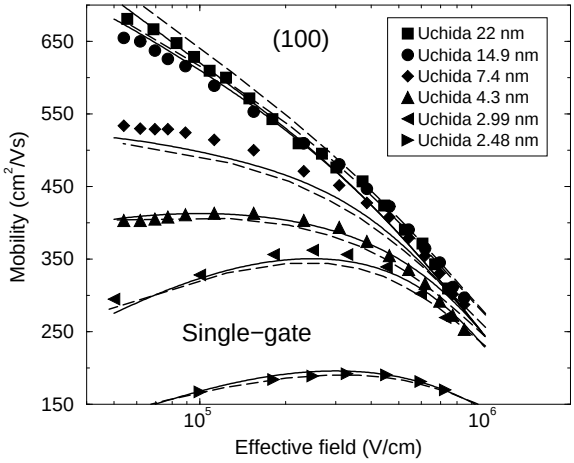

Figure 1.24: *Electron mobility in (100) SG-SOI FETs versus effective field for a wide range of silicon thicknesses at* 300 *K. Solid lines: effective mobility model; dashed lines: simulation results obtained by using the local mobility model; symbols: measurements from [12].*

parameter of the surface roughness scattering C_{SR_0} changes as in (1.57).

For implementation reasons, drift-diffusion commercial device simulators require a mobility model dependent on the local electron concentration n and transverse electric field $E_\perp$, rather than the nonlocal inversion-layer electron density and effective field. To this purpose, N_{inv} and E_{eff} are simply replaced by n and $E_\perp$ in our model, and the fitting parameters are re-extracted by comparison with experiments and are reported in Appendix A-table A.2. Figs. 1.24, 1.25 and 1.26 show the comparison between measurements and local model (dashed lines) for the complete set of measurements data in [12] and [16] for SG-SOI FETs as a function of the effective field and silicon thickness. The effective mobility is also shown with solid lines. The performance of the local mobility model is good, the maximum relative error being 15%. This partly confirms the qualitative results obtained in [46].

1.13 Summary

In this chapter a low-field electron mobility model suitable for device-simulation tools in (100) and (110) UTB-SOI MOSFETs has been presented. The model accounts for the main physical effects related to the quantum-mechanical structural confinement, such as valley repopulation, in-plane anisotropy and nonparabolicity, and transposes them into simple analytical formulations. The correct description of the band structure (energy levels and effective masses) is shown to be fundamental to predict mobility in UTB devices for any arbitrary in-plane current-flow direction. The inclusion of silicon-thickness fluctuations and surface-

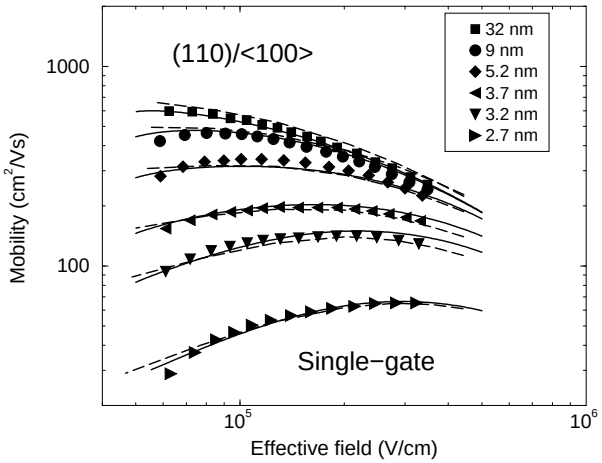

Figure 1.25: *Electron mobility in* (110)/⟨100⟩ *SG-SOI FETs versus effective field for a wide range of silicon thicknesses at* 300 *K. Solid lines: effective mobility model; dashed lines: simulation results obtained by using the local mobility model; symbols: measurements from [16].*

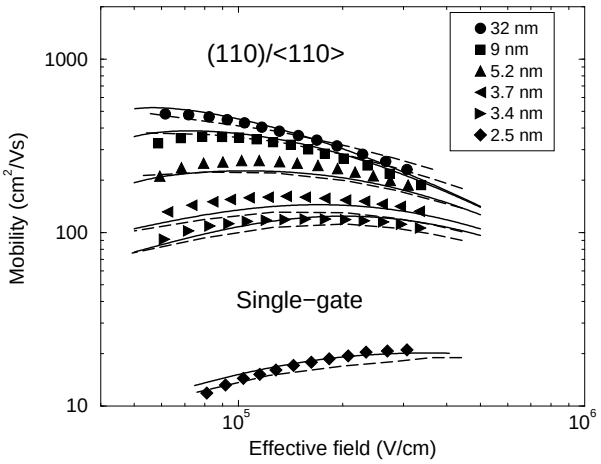

Figure 1.26: *Electron mobility in* (110)/⟨110⟩ *SG-SOI FETs versus effective field for a wide range of silicon thicknesses at* 300 *K. Solid lines: effective mobility model; dashed lines: simulation results obtained by using the local mobility model; symbols: measurements from [16].*

phonon scattering extends the validity of the model to very small silicon thicknesses. Moreover, accounting for the scattering induced by interface states and the impact of volume inversion on surface-roughness scattering, the model is able to reproduce (110) mobilities in SG and DG structures.

Experimental data on (100), (110)/⟨100⟩ and (110)/⟨110⟩ SG and DG MOSFETs are reproduced with a maximum error of about 15%.

Chapter 2

Mobility Model for Differently-Oriented UTB SOI p-FETs

Recently, it has been experimentally demonstrated that the hole mobility, similarly to the electron mobility, is a sensitive function of the silicon-body thickness, especially when t_{Si} is below 5 nm [47]. A number of experimental investigations can be found on UTB single-gate silicon-on-insulator (SG-SOI) pMOSFETs along with theoretical microscopic analyses accounting for full-band structure and the most relevant scattering mechanisms [48] [49] [50], but a physically-based analytical model for the hole low-field mobility is still missing.

The aim is to derive a TCAD mobility model, suitable for device simulation tools, which accurately predicts the low-field hole mobility in bulk and UTB FETs with different surface and channel orientations and silicon thicknesses from bulk-like to values as small as 2.3 nm.

In the following, a complete description of the model is provided and its validation against experiments is illustrated. The mobility formulation is given in 2.1. The modeling of the scattering contributions, namely, acoustic and optical phonon, Coulomb, surface-roughness and interface-state scattering, is described in section 2.2. An accurate analytical description of the energy subbands is reported in section 2.3. The additional effects needed for ultra-thin SOI are shown in section 2.4. A review of the complete model is reported in section 2.5.

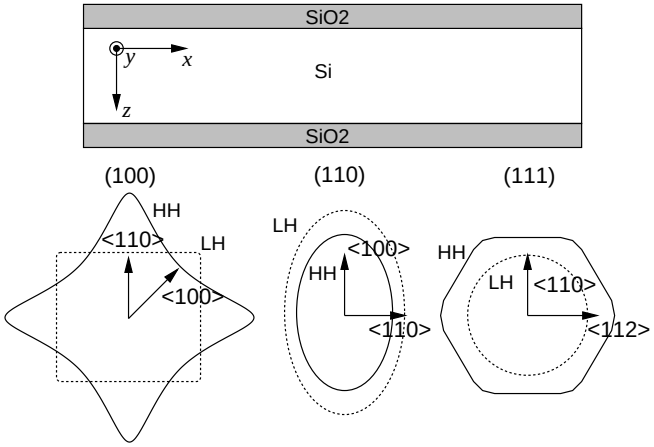

Figure 2.1: *Top: orientation of the reference axes. Bottom: in-plane minima projections for (100), (110) and (111) surface orientations. The most relevant in-plane current flow directions are also indicated.*

2.1 Generalized mobility model

Consider a silicon film on a substrate with one of the three crystallographic orientations indicated in Fig. 2.1, bottom. The z axis is set parallel to the structural confinement direction, while carrier transport occurs along the x axis. The inversion-layer quantization, due to the combined effects of the structural confinement and the application of a transverse electric field, causes the formation of energy subbands splitted in three different groups: heavy hole (HH), light hole (LH) and split-off subbands. The latter ones have not been considered in this work because of their lower energy, which makes them practically unpopulated [48]. The complex shape of the valence-band valleys makes the analytical calculation of the principal effective masses quite problematic. Therefore a simplified approach has been followed. The masses along the quantization direction (m_z) for the (100), (110) and (111) oriented wafers have been extracted by comparing the valley edges calculated by means of a six-band $\mathbf{k} \cdot \mathbf{p}$ approach reported in [48] with the well-known analytical expression determined for a triangular well by Stern and Howard [22], which reads:

$$E_{V_v} = \left(\sqrt[3]{\frac{9}{32}} + \sqrt[3]{\frac{9}{4}} \right) \sqrt[3]{\frac{\hbar^2 q^2}{m_{z_v}}} E_{\text{eff}}^{2/3} , \tag{2.1}$$

where $\hbar$ is the reduced Planck constant, q is the elementary charge, E_{eff} is the transverse effective field and m_{z_v} is the quantization mass relative to the v^{th} valley. In the following $v = 1$ and $v = 2$ indicate the LH and HH valleys, respectively. The comparison of Eq. (2.1) with the $\mathbf{k} \cdot \mathbf{p}$ results is illustrated in Fig. 2.2, while the extracted quantization masses are reported in table 2.1. In order to

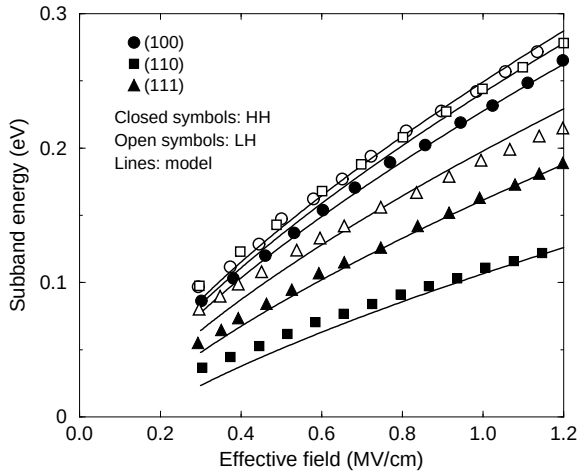

Figure 2.2: *Energy of the valley edges as a function of the effective field for (100), (110) and (111) wafers. Symbols: numerical computations from [48]. Solid lines: Eq. (2.1) with a shift of -44 meV.*

calculate the 2D density-of-state effective masses, different approaches have been used for the three considered crystallographic orientations. More specifically, in the (100) and (111) orientations circular parabolic in-plane bands for the HH and LH valleys have been assumed. Within such approximation the HH and LH density-of-state effective masses have been extracted by comparing the analytical calculations of the relative valley populations as functions of the effective field with the numerical data reported in [48]. For the analytical calculations, the Boltzmann statistics has been assumed:

$$p_v = \frac{m_{d_v} \exp\left(-E_{\mathrm{V}_v}/k_B T\right)}{\sum_{v'=1}^{2} m_{d_{v'}} \exp\left(-E_{\mathrm{V}_{v'}}/k_B T\right)} \,. \tag{2.2}$$

The comparison of the analytical p_v with numerical results is reported in Fig. 2.3.

Differently from the cases described above, in the (110) case a clear in-plane anysotropic energy distribution can be observed (Fig. 2.1, bottom). In this case, elliptical parabolic in-plane bands for the HH and LH valleys have been used, and the effective masses along the transport (m_x) and the device width (m_y) directions have been extracted by comparison with the band calculations reported in [51] as shown in Fig. 2.4. The extracted effective masses are reported in table 2.1. Finally, the density-of-state effective masses in the (110) case have been calculated as $m_{d_v} = \sqrt{m_{x_v} m_{y_v}}$, and their values have been validated by comparing the analytical p_v with the corresponding numerical results shown in [48] (see Fig. 2.3).

Similarly to the electron mobility model in Chapter 1, the in-plane transport is generally described by a 2D tensorial effective mobility which retains the

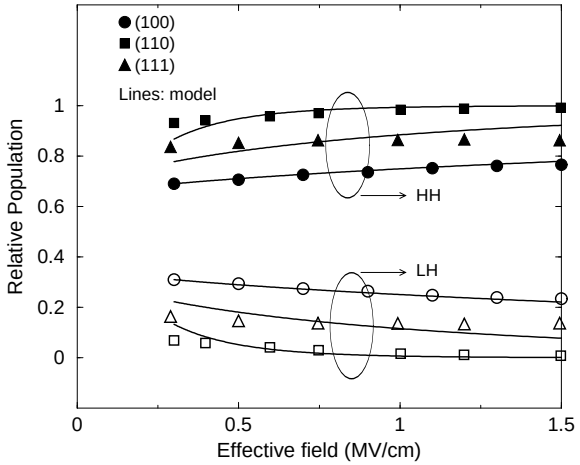

Figure 2.3: *Relative valley populations as a function of the effective field for (100), (110) and (111) wafers. Symbols: numerical calculations by [48]. Solid lines: Eq. (2.2).*

anisotropy of the single-valley effective mobilities:

$$\hat{\mu}_{\text{eff}} = \sum_{v=1}^{2} p_v \hat{\mu}_v \,. \tag{2.3}$$

A similar formulation is already available in 3D drift-diffusion transport simulation tools which handle bulk piezoresistivity and, in general, material anisotropy (see, e.g., [27]). Such tools can be directly used also in this case given that the out-of-plane (normal to the interface) mobility component plays no role and provided that the in-plane effective mobility model (2.3) is implemented. Unfortunately, this approach is unpopular in commercial tools because the effective mobility dependence on integral (non-local) carrier concentration and electric field may lead to numerical problems. As an alternative, a local mobility tensor $\hat{\mu}$ which depends on the local normal electric field $E_\perp(z)$ and the hole concentration $n(z)$ can be defined, satisfying the following equation:

$$\hat{\mu}_{\text{eff}} = \frac{\int_0^{t_{\text{Si}}} (n(z) - n_0(z)) \hat{\mu}(n, E_\perp(z)) dz}{\int_0^{t_{\text{Si}}} (n(z) - n_0(z)) dz} \,, \tag{2.4}$$

where $(n(z) - n_0(z))$ is the excess carrier concentration in the inversion layer. It should be noted that the experiments measure only the xx component of the mobility tensor.

As for the electron mobility described in Chapter 1, a two-step procedure has been followed in the model development. In the first step, an analytical model has been defined for the effective mobility (2.3) as a function of E_{eff} and the inversion-charge concentration per unit area, calibrating the parameters on

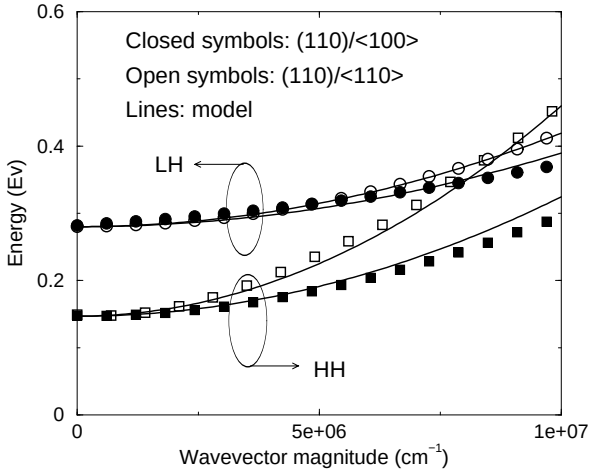

Figure 2.4: *Energy dispersion relations in (110) wafers obtained by using the* $\mathbf{k} \cdot \mathbf{p}$ *approach [51] (symbols) and the parabolic band approximation (lines). The* $\langle 110 \rangle$ *and* $\langle 100 \rangle$ *in-plane crystal directions have been used to separately extract* m_x *and* m_y*.*

experiments. E_{eff} is calculated as:

$$E_{\text{eff}} = \frac{\int_0^{t_{\text{Si}}} (n(z) - n_0(z)) E_\perp(z) dz}{\int_0^{t_{\text{Si}}} (n(z) - n_0(z)) dz} \,. \tag{2.5}$$

In the second step, a local mobility model, which depends on $E_\perp(z)$ and $n(z)$, is provided as described in section 2.5.

As far as the relative valley populations are concerned, Eq. (2.2) is used. In Eq. (2.2), the subband edges E_{V_v} can be calculated as given by Eq. (2.1) when a bulk MOSFET structure is considered. A different approach needs to be followed when a thin silicon film is addressed, as will be shown in section 2.3. The single-valley mobility tensor is modeled as

$$\hat{\mu}_v = \mu_v \hat{m}_v^{-1}, \quad \hat{m}_v^{-1} = \begin{pmatrix} m_0/m_{x_v} & 0 \\ 0 & m_0/m_{y_v} \end{pmatrix}, \tag{2.6}$$

where $\hat{m}_v^{-1}$ is the inverse normalized mass tensor of a 2DHG, defined for each valley v to account for the anisotropy effects induced by different in-plane crystal directions. Note that when (100) or (111) samples are considered $m_{x_v} = m_{y_v} = m_{d_v}$. Finally, μ_v is calculated as usual by accounting for the different scattering mechanisms combined via Matthiessen's rule:

$$\mu_v = \frac{q}{m_0 \sum_j \tau_{v_j}^{-1}} \,. \tag{2.7}$$

In (2.7), τ_{v_j} represents the average momentum relaxation time (MRT) due to the j-th scattering mechanism for the v^{th} valley. The average MRTs are illustrated in the next sections.

Table 2.1: *Effective masses for a 2DHG in (100), (110) and (111) oriented samples in units of m_0.*

(Wafer)/<channel>	m_z	m_x	m_y	m_d	valleys
(100)	0.25	0.245	0.245	0.245	1 (LH)
	0.29	0.43	0.43	0.43	2 (HH)
(110)/⟨110⟩	0.23	0.274	0.348	$\sqrt{m_x m_y} = 0.309$	1 (LH)
	1.8	0.122	0.215	$\sqrt{m_x m_y} = 0.162$	2 (HH)
(110)/⟨100⟩	0.23	0.348	0.274	$\sqrt{m_x m_y} = 0.309$	1 (LH)
	1.8	0.215	0.122	$\sqrt{m_x m_y} = 0.162$	2 (HH)
(111)	0.41	0.244	0.244	0.244	1 (LH)
	0.67	0.454	0.454	0.454	2 (HH)

2.2 Scattering contributions

Following the approach adopted for the electron mobility in Chapter 1, the acoustic phonon-limited inverse MRT relative to the v^{th} valley is calculated as

$$\frac{1}{\tau_{\mathrm{AC},v}} = \frac{C_v m_{d_v}}{W_v} \quad , \tag{2.8}$$

where W_v is the effective width of the hole distribution in the v^{th} valley and C_v is a constant related to the intravalley acoustic-phonon scattering parameters (see Appendix A). Intervalley scattering is not considered in view of the low-field regime (vanishing longitudinal electric field), which is close to equilibrium. The average effective widths W_v are modeled as for the electron mobility (see Eqs. (1.35), (1.36) and (1.37)) and their calibration has been carried out against the numerical predictions of the Schrödinger-Poisson solver, generalized to SG-SOI p-FETs with different crystal orientations, as shown in Fig. 2.5. The extracted parameters are reported in Appendix A. The eigenfunctions are zero at the Si/SiO_2 interfaces. Neumann boundary conditions for the potential are applied to the bottom edge of the buried oxide in SG-SOI FETs.γ, whose theoretically predicted value is 1/3 [21], is found to be equal to 0.29, 0.33 and 0.29 for the HH valleys, while the values of 0.29, 0.17 and 0.24 have been found for the LH valleys of (100), (110) and (111), respectively.

The overall (110) phonon-limited mobility, both from numerical calculations [48] and experiments [47], showed a trend in E_{eff} which differs significantly from the usual $E_{\mathrm{eff}}^{-1/3}$ (see Fig. 2.6). At low temperatures such a trend is indeed no longer observed. This may suggest that optical phonons can limit mobility at low E_{eff} and high temperatures, when the two lowest HH bands and the first LH band are close enough to allow intersubband transitions assisted by absorption of optical phonons to play a role. On the contrary, when the confinement induced by E_{eff} becomes stronger, this process is weakened by the distance of the energy

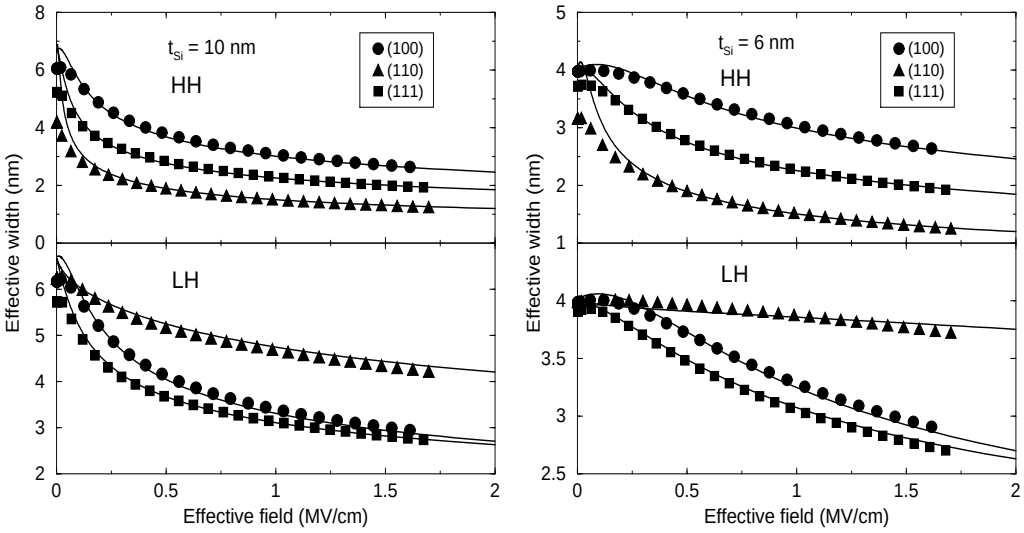

Figure 2.5: *Effective widths for the unprimed and primed subband ladders as a function of the effective field at* $t_{\rm Si} = 10$ *nm (left) and* $t_{\rm Si} = 6$ *nm (right). Symbols: numerical computations. Solid lines: Eq. (1.35).*

levels, and the phonon-limited mobility increases until a usual decreasing trend with $E_{\rm eff}$ is recovered again [48]. In order to model this effect the optical phonon-limited inverse MRT relative to the HH band in (110) wafers has been accounted for as

$$\frac{1}{\tau_{\rm OP,2}} = C_{\rm OP}\, m_{d_2} \left(\frac{E_{\rm eff0}}{E_{\rm eff}} \right)^{\zeta} \quad , \tag{2.9}$$

where $\zeta = 0.31$ has been extracted from calculations in [48] (see inset in Fig. 2.6) and $C_{\rm OP}$ is a fitting parameter, whose value is reported in Appendix A. The phonon-limited mobility relative to the HH valley has been calculated by combining the scattering term in (2.9) with (2.8) via Eq. (2.7). In Fig. 2.6 the calculated total phonon-limited mobility curves are compared with those extracted from experiments in [47] with different $t_{\rm Si}$. The details on the modeling of the optical phonon scattering as a function of $t_{\rm Si}$ are discussed in section 2.4.

The Coulomb and surface roughness scattering terms are modeled as in Eqs. (1.39) and (1.42), and the fitting parameters, reported in Appendix A, have been extracted by comparing the analytical model with a large set of experiments for bulk MOSFETs in the three considered crystallographic orientations (see Fig. 2.7). Finally, a mobility degradation with respect to the universal bulk-mobility curve is experimentally observed at low-medium $E_{\rm eff}$ for (110)-oriented SG-SOI FETs with $t_{\rm Si} = 32$ nm, even if the device is essentially undoped (see Fig. 2.13). Recently, a number of publications reported the amount of interface states in devices with different orientations (e.g. [7], [39]) and indicated that (110)-oriented devices have an interface state density about three times larger than

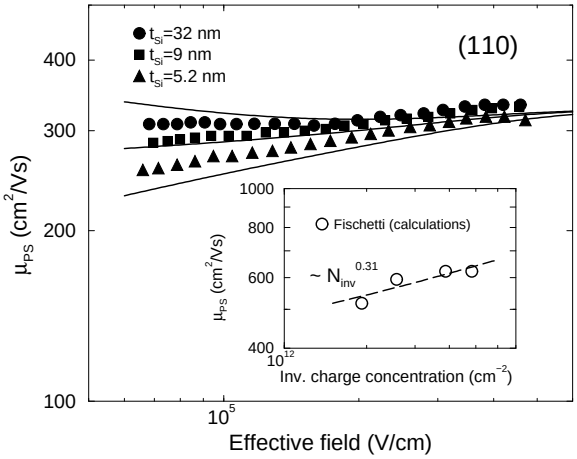

Figure 2.6: *Phonon-limited hole mobility vs. effective field for (110)/⟨110⟩ surface extracted from experiments in [47] (symbols) and from our model. Inset: μ_{PS} vs N_{inv} from simulations in [48].*

(100)-oriented devices. Moreover, it is known that the buried-oxide interface can influence mobility in UTB SOI-FETs [55]. Thus, when considering SOI-FETs it is appropriate to model an additional contribution which accounts for the mobility reduction induced by interface states

$$\frac{1}{\tau_{it,v}} = C_{\mathrm{it}_0} \left(\frac{N_{it}}{N_{it0}}\right) \left(\frac{N_{inv0}}{N_{inv}}\right)^{\zeta} \quad . \tag{2.10}$$

where $N_{it0} = 5 \times 10^{10}$ cm^{-2}, $\zeta = 0.5$ as reported in the literature and C_{it_0} is a constant extracted from comparison with experiments (see Appendix A). A value of $1.5 \times 10^{11}\,\mathrm{cm}^{-2}$ for N_{it} (similar to what experimentally shown in [32]) has been used to reproduce the experiments by Tsutsui et al. [47]. Considering that in a (100)-oriented device N_{it} is typically of the order of $5 \times 10^{10}\,\mathrm{cm}^{-2}$ [32], the above scattering contribution is found to be effective only in the (110) case. N_{it} should be considered an effective interface state density accounting also for the back interface defects.

Differently from electrons (see Chapter 1), the hole mobility curves at low temperature reported in [47] are independent of t_{Si} down to 9 nm. Thus, no dependence on t_{Si} has been modeled in (2.10). For $t_{\mathrm{Si}} < 9\,\mathrm{nm}$, additional physical effects become relevant and contribute to degrade mobility, as explained in the following.

2.3 Band structures and repopulation effects

In order to calculate the relative populations of the LH and HH valleys in samples with different t_{Si} and orientations, an analytical function has been developed

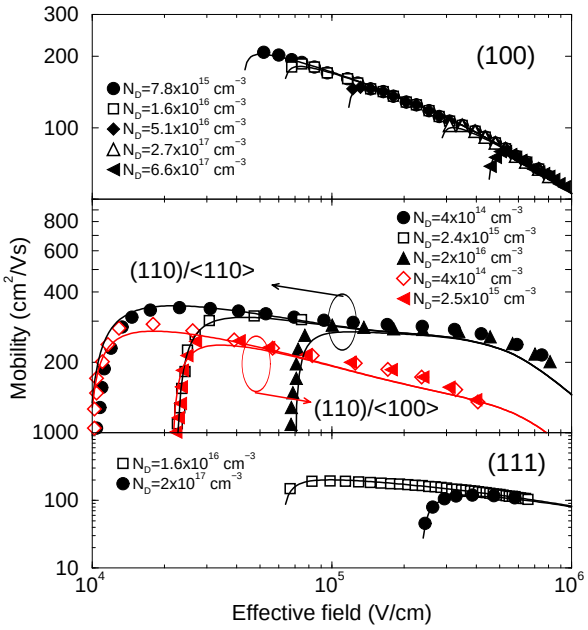

Figure 2.7: *Hole mobility in (100), (110) and (111) bulk MOSFETs vs. effective field for various substrate doping concentrations. Symbols: (100) experiments from [24], (110) from [52] and (111) from [53] and [54]. Solid lines: our model.*

based on physical considerations. Due to the lack of experimental data on (111) substrates, the mobility analysis is limited to the (100) and (110) ones.

For zero normal electric field (quantum well) the analytical solution of the Schrödinger equation provides the expression for the energy levels. The relative distance between the LH and HH valley edges reads:

$$\Delta E_{\mathrm{VT}} = E'_{\mathrm{VT}} - E_{VT} = \frac{(\hbar\pi)^2}{2t_{\mathrm{Si}}^2}\left(\frac{1}{m_{z,1}} - \frac{1}{m_{z,2}}\right) . \tag{2.11}$$

The separation between the energy minima of the two valleys increases with the reduction of t_{Si}, and holes mostly populate the HH valley.

At large normal electric fields the energy edges can be theoretically calculated assuming a triangular potential well as in Eq. (2.1) and their difference is indicated with ΔE_{VE} in the following. Finally, adopting the same formulation used for the conduction band edges in Eq. (1.45), the difference between the valley edges at high normal fields ΔE_{V} can be expressed as

$$\Delta E_{\mathrm{V}} = \Delta E_{\mathrm{VT}}\left[1 + (\Delta E_{\mathrm{VE}}/\Delta E_{\mathrm{VT}})^{\beta}\right]^{1/\beta} , \tag{2.12}$$

where $\beta = 3.5$. In order to validate Eq. (2.12), the relative valley populations for (100) FETs have been calculated by using Eq. (2.2) as a function of t_{Si} and compared with those reported in [48] (see Fig. 2.8). A clear repopulation

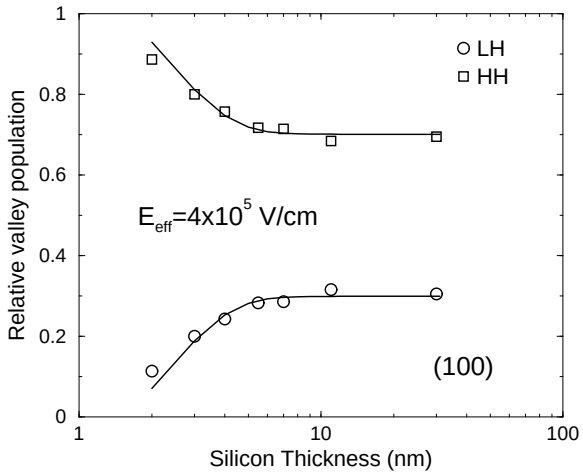

Figure 2.8: *Relative occupancy of the HH and LH valleys in (100) oriented samples vs. the silicon thickness at* $E_{\rm eff} = 4 \times 10^5$ *V/cm from (2.2). Symbols: numerically calculated relative populations in [48]; lines: this model.*

effect is evident at about $t_{\rm Si} = 7$ nm. The HH valley, i.e. the unprimed one, which exhibits the higher transport effective mass (see table 2.1), turns out to be repopulated for $t_{\rm Si} < 7\,$nm, with a negative effect on mobility. This effect contributes to the monotonic mobility degradation with decreasing $t_{\rm Si}$ shown in section 2.4. As far as the (110) orientation is concerned, the same formulation in Eq. (2.12) has been used. However, in this case the repopulation effect does not remarkably influence the hole mobility, since the HH valley is almost entirely populated even at very thick silicon films and bulk MOSFETs (Fig. 2.3).

2.4 Model enhancements for $t_{Si} < 5\,$nm

2.4.1 (100) substrates

1) Scattering induced by silicon-thickness fluctuations

The measured (100) mobility for $t_{\rm Si} < 5\,$nm exhibits a strong degradation which was ascribed to the scattering induced by $t_{\rm Si}$ fluctuations [17]. Eqs. (1.51) and (1.52) are used here to reproduce the experiments available at 25 K [12], as shown in Fig. 2.9 (top). The extracted parameters are reported in Appendix A.

2) Suppression of inter-subband phonon scattering

This effect should not take place in (100) FETs, because the energy difference between the HH and LH valleys is lower than the energy of the f-type phonons even at high $E_{\rm eff}$ (see Fig. 2.2), thus forbidding the suppression of the inter-subband phonon scattering. This is confirmed by the experimental mobility in

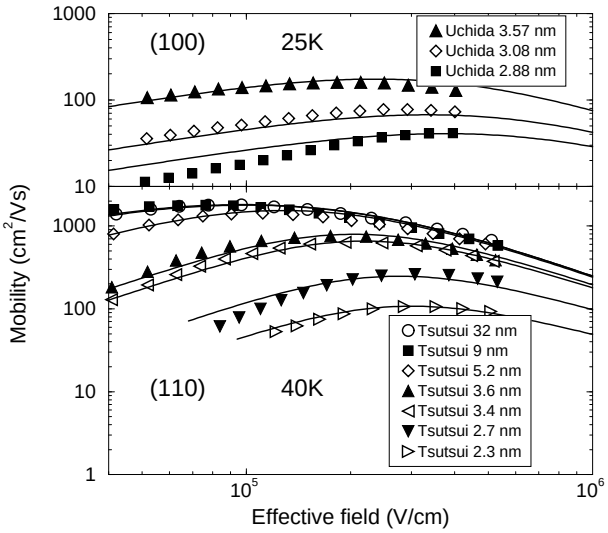

Figure 2.9: *Hole mobility vs. effective field at low temperature for (100) (top) and (110)/⟨110⟩ oriented FETs (bottom). Symbols: measurements from [12] and [47]. Solid lines: Coulomb + surface roughness + silicon thickness-fluctuation limited mobility. The phonon scattering contribution depends on temperature as $T^{1.75}$ [48] thus its influence on mobility at low temperature is quite negligible (1% and 3% of phonon scattering at room temperature at 25 K and 40 K respectively).*

(100) substrates reported in Fig. 2.10, bottom, where the curve monotonically decreases by shrinking t_{Si}.

3) Surface optical phonons

In order to reproduce the mobilities of devices thinner than 3 nm at 300 K, the surface-mode optical-phonon scattering contribution has been introduced [2]. The effects of the above scattering terms are highlighted in Fig. 2.10, top. The values of the fitting parameters are reported in Appendix A.

2.4.2 (110) substrates

1) Scattering induced by silicon-thickness fluctuations

The same model has been used for the (110) case as well, with parameters extracted by comparison with experiments carried out at 40 K by Tsutsui et al. [47] (see Fig. 2.9, bottom).

As explained in section 2.2, when (110) p-FET is considered, the impact of optical-phonon scattering becomes nontrivial and its dependence on t_{Si} should be correctly modeled. In [47], the phonon scattering limited mobility has been extracted by means of the Matthiessen rule and by assuming that only the phonon

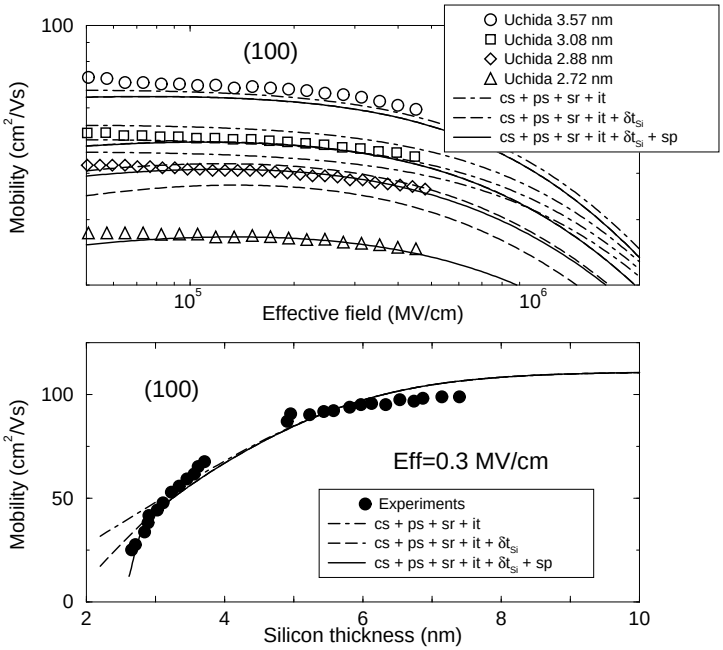

Figure 2.10: *Hole mobility vs. effective field (top) and silicon thickness (bottom) at* $300\,K$ *for (100) devices. Symbols: measurements from [12]. Lines: Coulomb + phonon + surface-roughness limited mobility (dashed), Coulomb + phonon + surface-roughness + thickness fluctuation limited mobility (long-dashed), Coulomb + phonon + surface-roughness + thickness-fluctuation + surface optical-phonon limited mobility (solid).*

contribution would change remarkably with temperature. However, this is incorrect because the scattering induced by thickness fluctuations varies with temperature as well. Indeed, the phonon limited mobility extracted in [47] for $t_{\rm Si} < 5$ nm results to be negative for $N_{inv} < 10^{12}$ cm^{-2}. Here, the temperature dependence of the MRTs relative to $t_{\rm Si}$ fluctuations has been assumed to be equal in (100) and (110) FETs. Thus, in order to correctly model the phonon-limited mobility in ultra-thin (110) SOI, the latter has been re-extracted from the experiments and used as a reference for the model validation (see open symbols in Fig. 2.11, top).

2) Suppression of inter-valley phonon scattering

As anticipated in section 2.2, the absorbtion of optical phonons between the lowest HH and the lowest LH subbands plays a role at low fields, while it is suppressed at high $E_{\rm eff}$. The simplest way to introduce the suppression of inter-valley phonon scattering is to model a reduction of the inverse momentum relaxation time (2.9) as a function of $\Delta E_{\rm V}$:

$$\frac{1}{\tau'_{\rm OP,2}} = \frac{1}{\tau_{\rm OP,2}}\big(1 - f(\Delta E_{\rm V})\big) \quad , \tag{2.13}$$

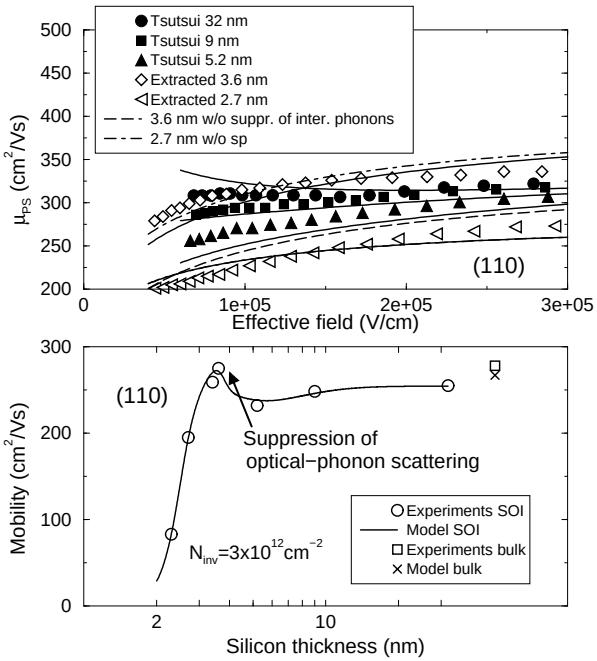

Figure 2.11: *Phonon-limited mobility in (110)/⟨110⟩ FETs versus effective field (top) and versus silicon thickness (bottom) for small silicon thicknesses. The measurements are from [47] (symbols). The impact of the suppression on inter-valley optical phonons and of the surface-optical phonons are highlighted.*

By exploiting the subband structure model presented in the previous section, $f(\Delta E_{\mathrm{V}})$ in (2.13) is modeled as:

$$f(\Delta E_{\mathrm{V}}) = \frac{f_0}{1 + \exp\left[-\left(\Delta E_{\mathrm{V}} - \Delta E_{\mathrm{V0}}\right)/C_{\mathrm{iv}}\right]} \quad , \tag{2.14}$$

where f_0, ΔE_{V0} and C_{iv} are fitting parameters (see Appendix A) calibrated on experiments by [47] at $N_{\mathrm{inv}} = 3 \times 10^{12}$ cm^{-2}, as depicted in Fig. 2.11 (bottom). Thus, the mobility enhancement observed in [47] can be nicely reproduced by the above approach. $f(\Delta E_{\mathrm{V}})$ becomes significantly different from zero for $\Delta E_{\mathrm{V}} > 60\,\mathrm{meV}$.

Another important observation is that, according to (2.13)-(2.14), the mobility enhancement in (110) samples is expected to increase as E_{eff} increases, because of the ΔE_{V} growth with E_{eff} (see Fig. 2.2). However, in very thin-film FETs (below 5 nm), additional scattering mechanisms limit the carrier mobility, i.e., the scattering induced by t_{Si} fluctuations (presented in the previous section) and the scattering with surface optical phonons (described below).

3) Surface optical phonons

The same expression for the conventional orientation is also used in this case. The model parameters are calibrated directly on experiments at 300 K. The effects of this scattering term is shown in Figs. 2.11 (top) and 2.13.

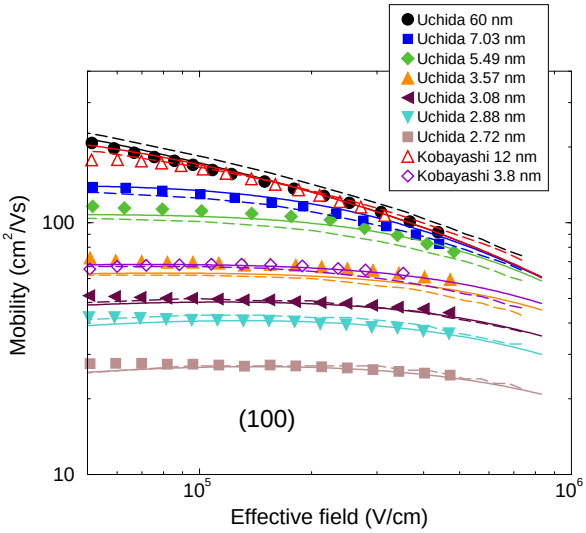

Figure 2.12: *Hole mobility in (100) FETs versus effective field for a wide range of silicon thicknesses at* 300 *K. Solid lines: effective mobility model; dashed lines: simulation results obtained by using the local mobility model; symbols: measurements from [12] and [56].*

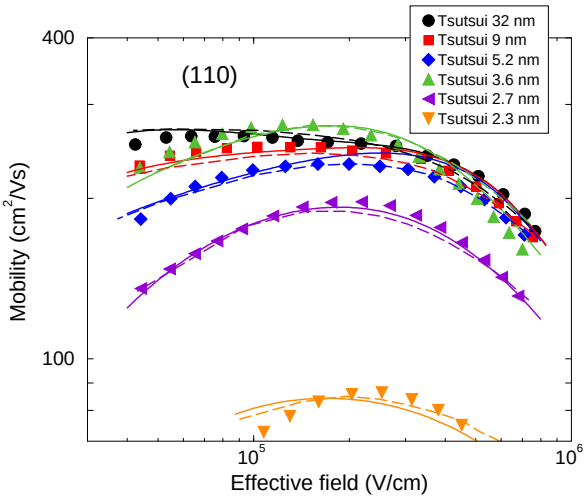

Figure 2.13: *Hole mobility in (110)/⟨110⟩ FETs versus effective field for a wide range of silicon thicknesses at* 300 *K. Solid lines: effective mobility model; dashed lines: simulation results obtained by using the local mobility model; symbols: measurements from [47].*

2.5 Review of the complete mobility model

All the scattering terms described above need to be accounted for in Eq. (2.7) to calculate the effective mobility. When bulk MOSFETs are considered $1/\tau_{it,v}$

should be neglected. Figs. 2.12 and 2.13 compare the predictions of the complete mobility model with the complete set of measurements data. For implementation reasons, commercial drift-diffusion device simulators require a mobility model dependent on the local carrier concentration n and transverse electric field $E_{\perp}$, rather than the non-local inversion layer carrier density and effective field. To this purpose, N_{inv} and E_{eff} are simply replaced by n and $E_{\perp}$ in our model, and the fitting parameters are re-extracted by comparison with experiments and are reported in Appendix A-table A.4. Figs. 2.12 and 2.13 show the comparison between measurements and local model (dashed lines) for the complete set of measurements data in [12], [56] and [47] for SG-SOI FETs as a function of E_{eff} and t_{Si}. The effective mobility is also shown with solid lines. The performance of the local mobility model is good, the maximum relative error being 13%.

2.6 Summary

In this chapter a low-field hole mobility model suitable for device-simulation tools in (100) and (110) UTB-SOI MOSFETs has been presented. The model accounts for the main physical effects related to the quantum-mechanical structural confinement and transposes them into simple analytical formulations. The inclusion of silicon-thickness fluctuations and surface-phonon scattering extends the validity of the model to very small silicon thicknesses. Moreover, accounting for the scattering induced by interface states and the impact of the suppression of intervalley optical phonon scattering, the model is able to reproduce (100) and (110) mobilities. Experimental data on (100), and (110) are reproduced in the model with a maximum error of about 10-15%.

Chapter 3

Effects of High-κ Gate Stacks and Metal Gates

The further miniaturization of CMOS technology requires the use of high-κ gate dielectric, as an alternative of conventional SiO_2, to reduce gate leakage current while keeping unvaried the gate capacitance [57]. Metal-gate electrodes have also attracted attention to overcome the poly-depletion effect that takes place under gate inversion for poly-Si gates resulting in a capacitance loss, and for compatibility with high-κ materials [58]. One of the most suited and very promising candidate is hafnium oxide (HfO_2) combined with titanium nitride (TiN) metal gate. However, apart from the specific materials and the related issues coming from their integration, a degradation of the inversion channel mobility has been regularly reported for devices with high-κ gate stacks. Extensive investigation has been carried out to discover the possible causes of the mobility loss. It has been suggested that the main physical mechanisms playing a role are the coulombic interactions of carriers in the inversion layer with remote charges or dipoles far from the Si/oxide interface (remote Coulomb scattering) [59], scattering events related to the potential modification of channel electrons due to the roughness of the oxide/gate interface (remote surface roughness) [60], and remote soft-phonon scattering [61]. Mobility lowering due to remote scattering mechanisms is observed in general for equivalent oxide thicknesses (EOT) less than about 2 nm, and results more effective for high-κ-based devices. The scattering with low energy optical phonons in high-κ dielectrics is due to the large polarizzability of their bonds and is therefore an intrinsic property [61].

However, even if there is no consensus yet on the relative importance of the different remote scattering mechanisms and on their physical origin, the experimentally observed mobility loss remains a crucial issue. A comprehensive mobility model for numerical simulation of high-κ and metal gate stacks has been lacking

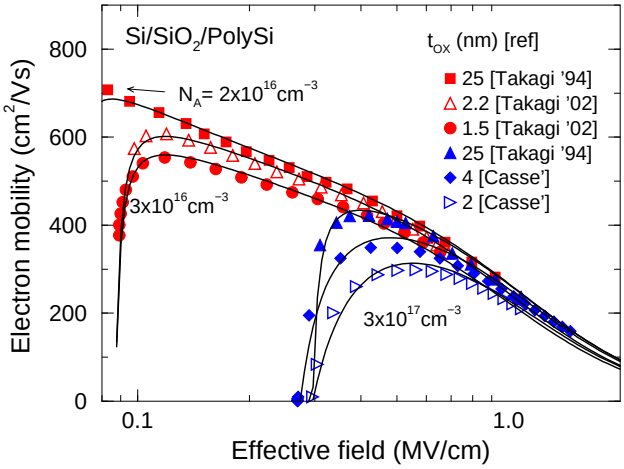

Figure 3.1: *Electron mobility as a function of the effective field for devices with SiO_2/poly-Si gate stack on (100)-oriented Si, and with different oxide thicknesses and substrate doping concentration. Symbols: experiments from [24], [62] and [64]. Lines: this model.*

so far, which makes device simulation unreliable, if quantitatively accurate predictions are sought. As shown in Chapters 1 and 2, the use of different silicon crystal orientations can be a way to compensate for the mobility degradation in high-κ MOSFETs, since carrier mobility can be improved by a suitable selection of surface and channel orientations. On the other hand, novel structures, e.g. FinFETs and Tri-gate FETs, widely utilize unconventional surface and channel orientations.

In the following, simple analytical formulations for remote scattering terms have been added to the electron and hole mobility models for differently-oriented FETs presented in Chapters 1 and 2, respectively. Recent experimental results for devices with gate stacks composed of different materials, and with varying oxide thickness, channel doping, crystalline surface orientation and channel direction [54] [62] [63], have been exploited to separately model the scattering contributions in the total mobility.

Aim of this investigation is that of providing an analytical low-field mobility model for MOSFETs with either poly-Si or TiN gate, ultrathin SiO_2/HfO_2 gate stacks and different substrate and channel orientations. Physical insights, theoretical analyses and experimental investigations are used to develop and accurately calibrate the model. In section 3.1, remote scattering terms are modeled and calibrated for devices with ultrathin SiO_2/poly-Si and SiO_2/TiN gate stacks. Remote scattering terms for high-κ dielectrics are then addresses in section 3.2 for (100), (110) and (111) silicon crystal orientations.

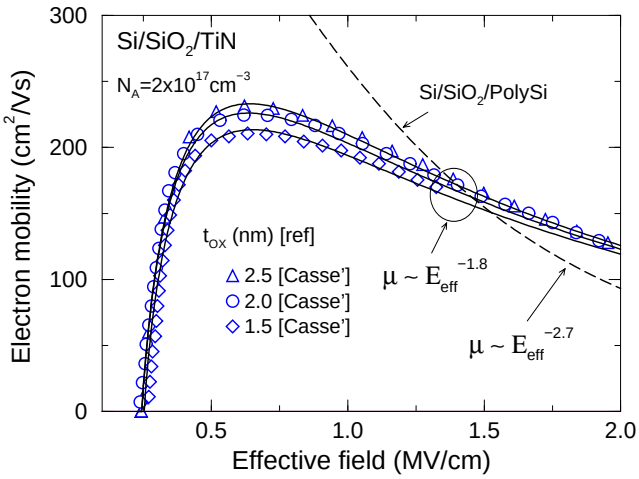

Figure 3.2: *Electron mobility as a function of the effective field for devices with SiO_2/TiN gate stack on (100)-oriented Si, and with different oxide thicknesses. Symbols: experiments from [62]. Lines: this model.*

3.1 Remote scattering effects with thin oxides and metal gates

From recent experimental analyses [62] [64] a mobility lowering with reduced oxide thickness t_{ox} has been observed mainly for electrons for both polysilicon and metal gates (Figs. 3.1, 3.2 and 3.4). Such effect can be attributed to remote Coulomb scattering (RCS), remote soft-phonon scattering (RPS) and remote surface-roughness scattering (RSS) mechanisms: they have been modeled as additional terms in the Matthiessen formulations (1.58) and (2.7) for electrons and holes, respectively, each with an exponential dependence on the oxide thickness (t_{ox}), calibrated on experiments. The semi-empirical formulation of the remote-phonon inverse relaxation time relative to the v^{th} valley reads

$$\frac{1}{\tau_{\mathrm{RPS},v}} = \exp\left(-k_{\mathrm{RPS}}\, t_{\mathrm{ox}}\right) \frac{C_{\mathrm{RPS}}\, m_{d_v}}{W_v} \quad , \tag{3.1}$$

with C_{RPS} and k_{RPS} fitting parameters, whose values are reported in Appendix A-table A.5. W_v is given in Eq. (1.35) and $m_{d_v} = \sqrt{m_{x_v} m_{y_v}}$ as explained in Chapter 1.

The remote-surface-roughness-limited inverse relaxation time reads

$$\frac{1}{\tau_{\mathrm{RSR},v}} = C_{\mathrm{RSR}} \exp\left(-k_{\mathrm{RSR}}\, t_{\mathrm{ox}}\right) m_{d_v} \left(\frac{E_{\mathrm{eff}}}{E_{\mathrm{eff0}}}\right)^{\delta} \tag{3.2}$$

with C_{RSR} and k_{RSR} fitting parameters (see Appendix A-table A.5). $E_{\mathrm{eff0}} = 10^6$ V/cm and δ is given in Eq. (1.42).

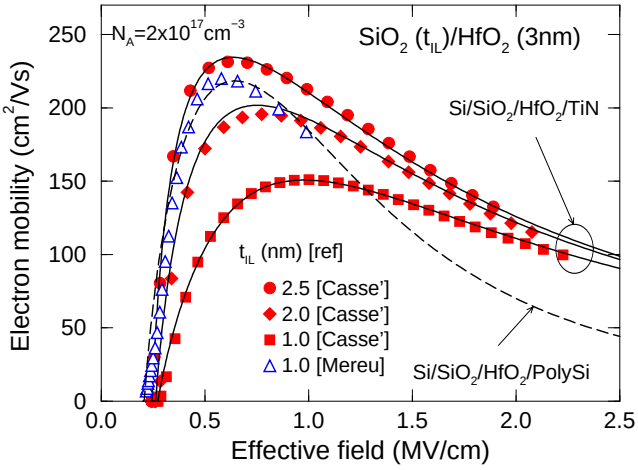

Figure 3.3: *Electron mobility as a function of the effective field for devices with $SiO_2/HfO_2/TiN$ gate stack on (100)-oriented Si, and with different oxide thicknesses. Symbols: experiments from [62] and [54]. Lines: this model.*

Finally, the inverse relaxation time limited by the remote Coulomb scattering is modeled as

$$\frac{1}{\tau_{\mathrm{RCS},v}} = C_{\mathrm{RCS}} \exp\left(-k_{\mathrm{RC}}\, t_{\mathrm{ox}}\right) \left(\frac{N_{\mathrm{inv0}}}{N_{\mathrm{inv}}}\right) \left(\frac{N_{A/D}}{N_{A0}}\right)^{\beta_{\mathrm{RCS}}} , \tag{3.3}$$

where C_{RCS} and k_{RCS} are fitting parameters (see Appendix A-table A.5). $\beta_{\mathrm{RCS}} = 1.96$, $N_{\mathrm{inv0}} = 10^{13}$ cm^{-2} and $N_{A0} = 10^{17}$ cm^{-3}, while $N_{A/D}$ is the acceptor/donor doping concentration when considering n- or p-FETs, respectively.

The calibrated model is shown in Fig. 3.1 for electrons. The hole mobility shows negligible effects related to the oxide thinning as shown in Fig. 3.4. Thus no additional contribution is added to the model.

In [62], an experimental investigation has been carried out on SiO_2/TiN devices in order to address the impact of TiN itself on mobility and to quantitatively determine how it influences the overall degradation, often fully attributed to the high-κ dielectrics. Devices with metal gates (SiO_2/TiN) show a clear mobility reduction at low electric fields, attributed to a higher Coulomb scattering contribution (Fig. 3.2). At higher fields, experiments show a weaker E_{eff} dependence, giving rise to a slight mobility enhancement. As such effects originate from chemical reactions related to the adopted deposition process [62], different values of C_{CS_0} ($C_{\mathrm{CS}_0} = 9.13 \times 10^{-4}$ s^{-1} for electrons and 8.4×10^{-5} s^{-1} for holes) and C_{SR0} ($C_{\mathrm{SR0}} = 4.98 \times 10^{13}$ cm^{2}eV^{-1}s^{-3} for electrons and 6.9×10^{13} cm^{2}eV^{-1}s^{-3} for holes) in (1.39) and (1.42), respectively, are used in the presence of TiN gates. δ, that is equal to 2.7 for (100) oriented n-type devices with poly-Si gate, is found to be 1.8 for TiN metal gates (see Fig. 3.2), in agreement with [65].

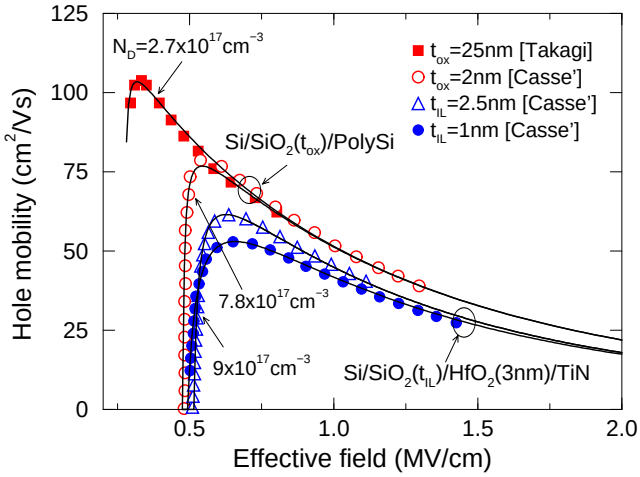

Figure 3.4: *Hole mobility as a function of the effective field for devices with both SiO_2/poly-Si and SiO_2/HfO_2/TiN gate stacks on (100)-oriented Si, and with different oxide thicknesses. Symbols: experiments from [24] and [62]. Lines: this model.*

3.2 Remote scattering effects in high-κ stacks

Here the main goal is to develop a mobility model for gate stacks realized with an SiO_2 interfacial layer (with given thickness t_{IL}), which either spontaneously interposes or is intentionally grown, and a high-κ dielectric on top (with given thickness t_{HfO_2}). To this purpose, the experiments carried out by [62] on devices with metal gates (TiN) and for different t_{IL} and different t_{HfO_2} have been used to calibrate the remote scattering terms. On the other hand, the remote scattering terms related to the presence of the high-κ dielectric are assumed independent of the gate material (polySi or TiN). As no significant dependence on the high-κ layer thickness is experimentally observed, the assumption in [62] that the remote scattering terms are mainly related to the surface at the SiO_2/HfO_2 interface has been followed. Thus, t_{ox} in the scattering terms (3.1), (3.2) and (3.3) has been replaced by the interfacial-layer thickness t_{IL}. In Figs. 3.3 and 3.4 the model parameters are calibrated on experiments with t_{IL} down to about 1 nm for electrons and holes, respectively. The extracted fitting coefficients are reported in Appendix A-table A.5.

Finally, the model has been applied to different surface and channel orientations without any change in the previously fitted data. A nice agreement is shown in Fig. 3.5 between the model for electron mobility in SiO_2/HfO_2/poly-Si gate stack and the corresponding experimental results.

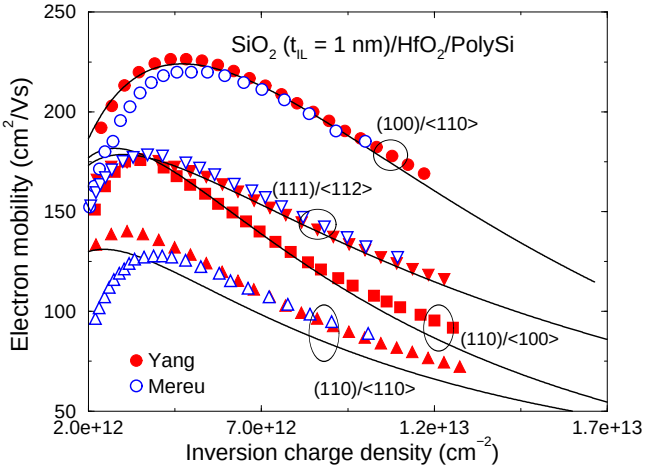

Figure 3.5: *Electron mobility as a function of inversion electron concentration for devices with SiO_2/HfO_2 gate stacks with poly-Si gate and different surface and channel orientations. Symbols are experiments in [54] and [63]. The thickness of the interfacial layer is 1 nm. Lines: this model.*

3.3 Summary

In this chapter, the effects of high-κ and metal gate stacks and surface and channel orientations have been included in the mobility models for electron and holes presented in the previous chapters. Simple analytical formulations are adopted to account for the main physical effects affecting carrier mobility in high-κ based devices and to perform fast and accurate numerical simulations.

Chapter 4

Effects of Mechanical Stress for Planar and Vertical FETs

Among all the new technologies proposed and investigated to continuously improve device performance, strain engineering during the past decade has been the dominant one. It allows to enhance device performance while providing a low-cost and low-risk technique by maintaining the traditional MOSFET fabrication process. In particular, strain has a large effect on the conduction current, because carrier mobility can be enhanced by appropriate stress configurations. The origin of strained-silicon technology can be traced back to silicon layers grown on relaxed silicon-germanium (SiGe) substrates in the 1980s [66]. The thin silicon layer tends to keep the larger lattice constant of the SiGe thus inducing a biaxial tensile stress. In the 1990s, two other strained-silicon techniques have been studied based on process-induced strain to introduce uniaxial tensile and compressive strain into the channel: high-stress capping layers deposited on MOSFETs [67] and SiGe in the source and drain area [68]. Even though the primary focus of the industry in the 1980s and 1990s was on biaxial stress, recently, growing attention is being paid to uniaxial process-induced stress for several reasons. First, uniaxial versus biaxial stress has been demonstrated to provide larger mobility enhancement and drive current improvement for nanoscale short-channel devices due to band warping and reduced conduction effective mass. Second, uniaxial process-induced stress has the advantage of a smaller shift in the threshold voltage [69]. However, because many process flow parameters need to be changed when fabricating strained MOSFETs, there is some uncertainty on whether strain alone is responsible for the performance enhancement (for example, reduced external resistance can itself play some role). Therefore, in order to check the role of strain itself and to investigate the best mechanical stress configuration, the wafer-bending apparatus has been widely utilized by researchers to apply well

defined external mechanical stress by simply bending the silicon wafer and characterizing the on-chip devices under stress conditions. The amount of applied stress can be easily extracted from the wafer curvature as explained in [6].

In addition to strained conventional MOSFETs ultra-thin body (UTB) devices with either planar or vertical architectures such as silicon-on-insulator (SOI) FETs, double gate (DG) FETs, FinFETs, Trigate FETs and silicon nanowires (SiNWs) are the most promising candidates for the future technology nodes. A recent research issue is that of investigating the role played by strain in such architectures and eventually combining these new architectures with uniaxial strain engineering to enable additional performance enhancement.

In the previous chapters mobility models for planar UTB SOI structures with unconventional orientations and high-κ oxides and metal gates have been proposed. Further attention needs to be paid to the carrier mobility behavior in non-planar FETs, due not only to the different crystallographic orientations of the top and lateral channels, but also to the complex stress configurations originating from the process steps (see, e.g., [70]). In addition, the experimental studies in narrow FinFETs [71] showed mobility behaviors which still are not clearly explained.

Even if several theoretical works have been performed to analyze strain-induced carrier mobility enhancement in both n- and p-MOSFETs [72], [73], a lack of universally accepted mobility models for planar and non-planar structures with both externally-applied or process-induced mechanical stress makes it difficult to perform quantitatively accurate simulations of such devices.

In this chapter, the aim is to provide a unified compact mobility model for electrons and holes comprehensive of all the relevant effects in FinFETs, based on the combination of the top and lateral channels. The model is physically based and extensively calibrated on experiments. It is shown to give a correct interpretation of the mobility features originating in non-planar devices.

In section 4.1 the model for biaxial stress is presented, while in section 4.2 the effects of uniaxial strain for (100) and (110) crystallographic planes are addressed and modeled. Afterwards, the resulting mobility models for electrons and holes are combined to compute the effective mobility of non-planar n- and p-FinFETs by averaging the top- and sidewall-channel mobilities (see section 4.3).

4.1 Strain effects in biaxial conditions

The models described in Chapter 1 and 2 for electron and hole mobilities, respectively, have been extended to include the effects of strain on valley splitting, valley repopulation, band deformation and scattering contributions. The stress tensor $\hat{\boldsymbol{\sigma}}$ or, alternatively, the strain tensor $\hat{\boldsymbol{\varepsilon}}$ in the crystal coordinate system (CCS) is the input of the model. As a first step, the 3×3 stress matrix $\hat{\boldsymbol{\sigma}}_{\boldsymbol{D}}$, con-

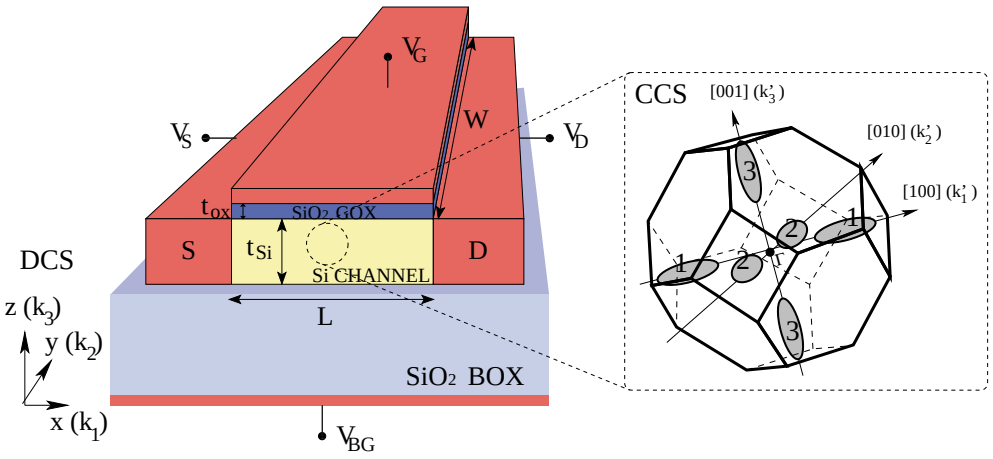

Figure 4.1: *Orientation of the device coordinate system (DCS) and the crystal coordinate system (CCS).*

ventionally given in the device coordinate system (DCS), have to be opportunely rotated in the CCS (see Fig. 4.1):

$$\hat{\boldsymbol{\sigma}}_{\boldsymbol{C}} = \Re^{T}_{D\leftarrow C}\, \hat{\boldsymbol{\sigma}}_{\boldsymbol{D}}\, \Re_{D\leftarrow C} \ , \tag{4.1}$$

where $\Re_{D\leftarrow C}$ is the rotation matrix from the CCS to the DCS. The six-component vector notation for $\hat{\boldsymbol{\varepsilon}}$ and $\hat{\boldsymbol{\sigma}}_{\boldsymbol{C}}$ allows to write the strain in the CCS as

$$\hat{\boldsymbol{\varepsilon}} = \mathbf{S}\, \hat{\boldsymbol{\sigma}}_{\boldsymbol{C}} \ , \tag{4.2}$$

where $\mathbf{S}$ is the six-by-six stiffness compliance matrix. The cubic symmetry of the silicon crystal reduces the independent components of $\mathbf{S}$ to only three, $S_{11} = 7.681\times10^{-6}$ MPa^{-1}, $S_{12} = -2.138\times10^{-6}$ MPa^{-1} and $S_{44} = 12.56\times10^{-6}$ MPa^{-1} [27].

The energy shifts of the conduction and of the HH and LH valleys are calculated for biaxial strain following [48]. For the conduction band, the edges of the valleys whose minima are located along the v^{th} $\langle 100\rangle$ axis is shifted by

$$\Delta E^{s}_{\mathrm{C}_v} = \Xi_d(\varepsilon_{xx}+\varepsilon_{yy}+\varepsilon_{zz}) + \Xi_u\varepsilon_{vv} \ , \tag{4.3}$$

where the index $v = x$ corresponds to valleys "1", $v = y$ to valleys "2", and $v = z$ to valleys "3", respectively (see Fig. 4.1). $\Xi_d = 1.1$ eV and $\Xi_u = 9.29$ eV denote the dilatation and the shear deformation potentials of silicon, respectively. The valley repopulation is calculated by adding the strain-induced shifts to the quantization eigenvalues in Eq. (1.27).

For the valence band, the energy shifts for stress along ⟨100⟩ can be written as [74]

$$\Delta E^{s}_{\mathrm{V},1} = -\frac{\Delta_0}{6} + \frac{\delta E_{001}}{4} + \frac{1}{2}\left[\Delta_0^2 + \Delta_0\ \delta E_{001} + \frac{9}{4}(\delta E_{001})^2\right]^{1/2} , \tag{4.4}$$

$$\Delta E^{s}_{\mathrm{V},2} = \frac{\Delta_0}{3} - \frac{\delta E_{001}}{3} , \tag{4.5}$$

where index 1 indicates the LH band and 2 the HH band, respectively. $\Delta_0 = 44$ meV and $\delta E_{001} = 2b(\varepsilon_{zz} - \varepsilon_{xx})$, where $b = -2.33$ eV is the shear deformation potential for a strain of tetragonal symmetry, and z is the quantization direction (perpendicular to the conduction plane). The energy shifts induced by the strain are added to the corresponding energy eigenvalues in Eq. (2.2) to the purpose of calculating the relative populations with the Boltzmann statistics approximation.

For holes, a complication arises because the valence band is strongly deformed by strain. The quantization masses m_{z_v} for holes extracted from the subband energy calculations in the unstressed case nicely reproduce the subband energy calculations also in the stressed case as reported in [48], therefore no m_{z_v} change is needed when stress is applied. On the contrary, the in-plane effective masses are strongly modified by strain, as shown by [48] and [75]. The in-plane inverse effective masses are defined as polynomial functions of ε_{xx}

$$\frac{1}{m^{\mathrm{str}}_{d_v}} = \frac{1}{m^{\mathrm{unstr}}_{d_v}} \left(1 + \sum_{j=1,3} b_{v,j}\, \varepsilon^{j}_{xx}\right) , \tag{4.6}$$

where $m^{\mathrm{unstr}}_{d_v}$ are given in table 2.1, and the fitting parameters $b_{v,j}$ are reported in Appendix A-table A.6. The density-of-state masses $m^{\mathrm{str}}_{d_v}(\varepsilon_{xx})$ for strained silicon grown on $\mathrm{Si}_{(1-x)}\mathrm{Ge}_x$ substrates with different Ge content x are reported in Fig. 4.2, along with the mobility enhancement due to band changes only, compared with theoretical calculations by Wang et al. [73]. The empirical relationship between Ge content x and strain in Si reads:

$$\varepsilon_{xx} = \frac{(a_{\mathrm{SiGe}} - a_{\mathrm{Si}})}{a_{\mathrm{Si}}} , \qquad a_{\mathrm{SiGe}} = a_{\mathrm{Si}} + a_0 x(1-x) + (a_{\mathrm{Ge}} - a_{\mathrm{Si}})x^2 , \tag{4.7}$$

where $a_{\mathrm{Si}} = 5.4331 \times 10^{-8}$ cm, $a_{\mathrm{Ge}} = 5.646 \times 10^{-8}$ cm and a_{SiGe} are the lattice constants of pure Si, pure Ge and SiGe, respectively, and $a_0 = 0.200326 \times 10^{-10}$ cm.

For both electrons and holes the valley repopulation and mass deformation alone do not explain the mobility enhancement shown by experiments. In fact, when strain is applied, the interband optical phonon scattering is reduced due to the band splitting, and the mobility is enhanced (see section 1.10.1). Moreover,

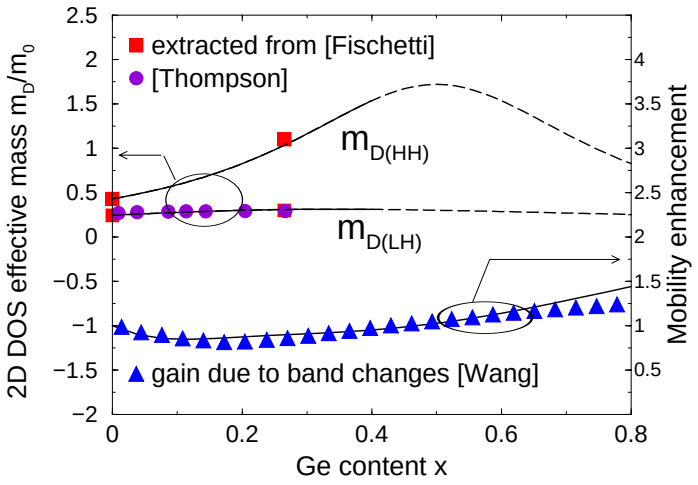

Figure 4.2: *Modeled density-of-states effective masses $m_{d_1} = m_{d_{LH}}$ and $m_{d_2} = m_{d_{HH}}$ (lines) compared with data extracted from subband repopulation [48] and* $\mathbf{k} \cdot \mathbf{p}$ *band calculations [75] (symbols). The mobility gain contribution due to band changes (lines) nicely follows the data based on the* $\mathbf{k} \cdot \mathbf{p}$ *band structure [73] up to x =0.8 (triangles).*

the assumption of a beneficial effect of strain on the interface as indicated by the experiments is followed. Thus, the inverse momentum relaxation times (MRTs) are modeled as a function of strain. For electrons, the same polynomial function has been applied to all the relaxation time contributions:

$$\sum_j \frac{1}{\tau_{v_j}^{\mathrm{str}}} = \sum_j \frac{1}{\tau_{v_j}^{\mathrm{unstr}}(1 + \eta_1 \varepsilon_{xx} + \eta_2 \varepsilon_{xx}^2 + \eta_3(\varepsilon_{xx} - \varepsilon_{yy}))} \ , \tag{4.8}$$

where $\sum_j \frac{1}{\tau_{v_j}^{\mathrm{str}}}$ is given by Eq. (1.58) and $\eta_1 = 109.95$, $\eta_2 = -616.76$ and $\eta_3 = -30.00$ are fitting parameters independent of the valley index. Calibration of η_1 and η_2 is shown in Fig. 4.3 with experiments by Driussi et al. [76], Nayfeh et al. [77] and Rim et al. [78].

For holes, the valence band is strongly warped and non-parabolic effects arise when considering the band deformed by strain. As far as the relaxation times are concerned, only the phonon-limited contribution explicitly shows a dependence on strain. The strain effect was already shown in the literature by Fischetti et al. [48] and Lee et al. [25]. Here, the expression of the effective width given by Eq. (1.37) has been extended to account for the effects of strain and to reproduce theory and experiments as shown in Figs. 4.4 and 4.5. The strain-dependent effective width reads:

$$W_{\mathrm{E}_v}^{\mathrm{str}} = W_{\mathrm{E0}_v}^{\mathrm{unstr}} \sqrt[3]{\frac{\hbar^2}{q m_{z_v}}} E_{\mathrm{eff0}}^{-\gamma^{\mathrm{unstr}}} \left(\frac{E_{\mathrm{eff}}}{E_{\mathrm{eff0}}} \right)^{-\gamma^{\mathrm{str}}} \ , \tag{4.9}$$

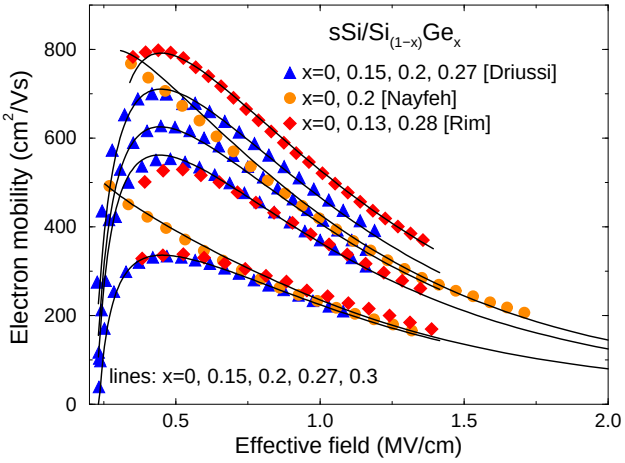

Figure 4.3: *Effective mobility for electrons as a function of the effective field in strained-Si grown on $Si_{(1-x)}Ge_x$ subtrates with different Ge content. Symbols: experiments from [76], [77] and [78]. Lines: this model.*

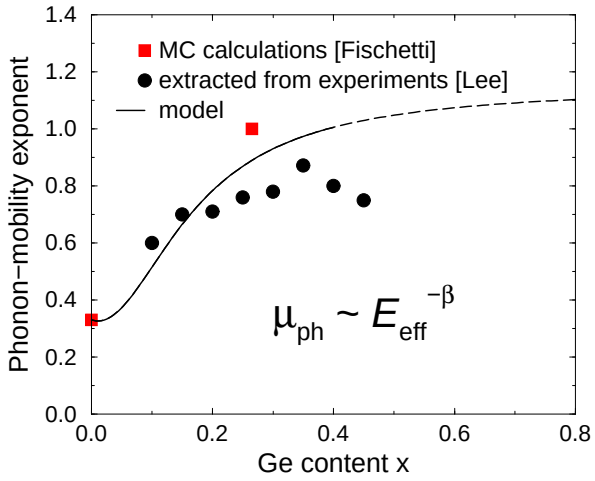

Figure 4.4: *The exponent of the phonon-limited mobility given by Eq. (4.10) and calibrated on experiments as a function of strain, compared with both theoretical predictions [48] and experimental extractions [25].*

with $W_{\mathrm{E0}_v}^{\mathrm{unstr}}$, γ^{unstr} and E_{eff0} the same introduced in section 2.2,

$$\gamma^{\mathrm{str}} = \gamma^{\mathrm{unstr}} + \frac{p_0 \varepsilon_{xx} + p_1\, \varepsilon_{xx}^2}{1 + p_2\, \varepsilon_{xx}^2} \ , \tag{4.10}$$

with $p_0 = -18.32$, $p_1 = 2.10 \times 10^4$ and $p_2 = 2.74 \times 10^4$. Finally, the phonon-limited relaxation time extended to account for the strain effects reads:

$$\frac{1}{\tau_{\mathrm{AC},v}^{\mathrm{str}}} = \frac{1}{\tau_{\mathrm{AC},v}^{\mathrm{unstr}}} \left(f_0 + \frac{f_1}{1 + \exp\left[(\varepsilon_{xx} - \varepsilon_0)/\varepsilon_1\right]} \right) \tag{4.11}$$

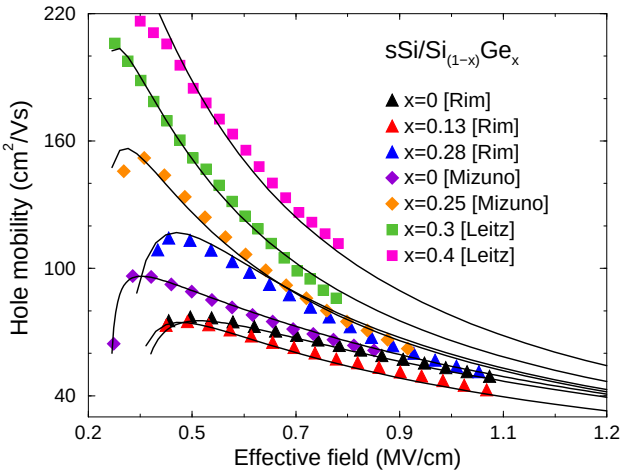

Figure 4.5: *Effective mobility model for holes as a function of the effective field in strained-Si grown on $Si_{(1-x)}$ Ge_x substrates with different Ge content. Symbols: experiments from [78], [79] and [80]. Lines: this model.*

with $\tau_{\mathrm{AC},v}^{\mathrm{unstr}}$ given by Eq. (2.8), $f_0 = 0.33$, $f_1 = 0.7$, $\varepsilon_0 = 0.008$ and $\varepsilon_1 = 0.00248$. The calibration of the overall hole mobility model is shown in Fig. 4.5 with experiments by Rim et al. [78], Mizuno et al. [79] and Leitz et al. [80].

4.2 Uniaxial stress effects for (100) and (110) crystallographic orientations

The equienergy surfaces of the six conduction band minima and of the HH and LH valleys projected on the (100) and (110) planes are reported in Fig. 4.6, as well as the relative effective masses along with the relevant directions.

4.2.1 Electron mobility

The experimental and theoretical analyses carried out by [81] and [72] have been considered in order to accurately model uniaxial-strain effects for (100)- and (110)-oriented nFETs. In particular, whenever the strain tensor in the principal crystal system contains nonvanishing shear elements (e.g., $\varepsilon_{xy} \neq 0$ as a result of uniaxial stress along $\langle 110 \rangle$ crystal direction), the band-edge energy of the valley pair "3" moves down with respect to the valleys "1" and "2" of a quantity $\Delta E^{\mathrm{shear}}$ defined as:

$$\Delta E^{\mathrm{shear}} = -\frac{\Theta}{4k^2}\varepsilon_{xy}^2, \quad |\varepsilon_{xy}| < k \tag{4.12}$$

where $\Theta = 0.53$ eV is the band separation between the two lowest conduction bands at the conduction-band edge of the unstrained lattice and $k = 0.0189$ [72]. The valley repopulation is calculated by adding the shear-strain-induced

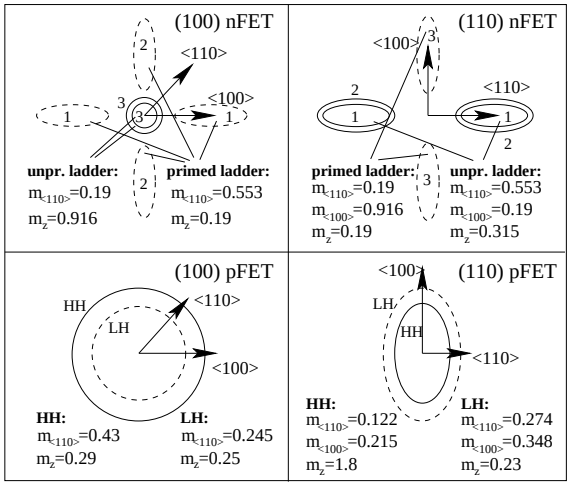

Figure 4.6: *Isoenergetic surfaces projected on the (100) and (110) planes for electrons and holes, along withe the relative principal effective masses.*

shift to the quantization eigenvalues in Eq. (1.27). Moreover, valley pair "3" results deformed (see inset of Fig. 4.7) under ⟨110⟩ tensile stress. The in-plane effective mass m_t of valleys "3" is changed differently in the parallel ⟨110⟩ and perpendicular ⟨-110⟩ direction with respect to the stress as:

$$m^{\mathrm{str}}_{t\langle 110\rangle} = m^{\mathrm{unstr}}_t(1+\gamma^{\mathrm{str}}\,\varepsilon_{xy}) \tag{4.13}$$

$$m^{\mathrm{str}}_{t\langle -110\rangle} = m^{\mathrm{unstr}}_t(1-\delta^{\mathrm{str}}\,\varepsilon_{xy}) \tag{4.14}$$

where $m^{\mathrm{unstr}}_t = m_t$, $\gamma = 3.089$ and $\delta = 5.296$. The effective masses modulated by strain are reported in Fig. 4.7 compared with numerical calculations reported in [81]. On the other hand no band warping is observed when uniaxial ⟨100⟩ stress is applied [81]. From the above expressions the corresponding 2DEG mass tensor and the density-of-state effective mass can be easily obtained for the mobility computation (see section 1.5).

(100)/⟨110⟩ nFETs

In (4.13) and (4.14), $m_{t\langle 110\rangle}$ and $m_{t\langle -110\rangle}$ correspond to m_{x_3} and m_{y_3} in the model, respectively, for conventional (100)/⟨110⟩ FETs (see section 1.5). The inverse MRTs change with strain is accounted for as in (4.8). The model for uniaxially-stressed (100)-nFETs is shown in Fig. 4.8 for both compressive and tensile stress and for stress directed both parallel and perpendicular to the transport direction.

Uniaxial tensile ⟨110⟩ stress on (100) silicon advantageously contributes to repopulate the unprimed two-fold valley "3", shifting downwards the corresponding valley edge with respect to the one relative to the primed ladder "1"-"2" (Eq. (4.3)). However, since the (100) primed and unprimed valley edges are

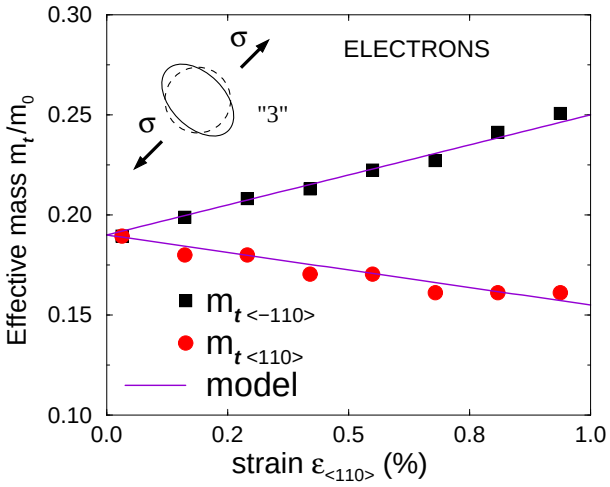

Figure 4.7: *The two-fold valleys "3" are warped by the ⟨110⟩ strain: the in-plane effective mass m_t is differently changed in the parallel and perpendicular direction. The m_t models (lines) are compared with numerical data by [81] (symbols).*

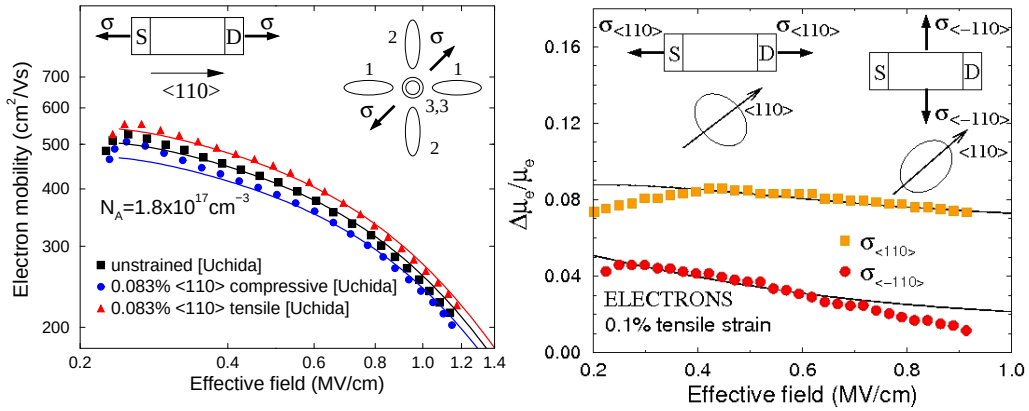

Figure 4.8: *(Left) Effective electron mobility under uniaxial ⟨110⟩ tensile and compressive strain for (100)/⟨110⟩ nFETs. (Right) Electron mobility enhancement under tensile uniaxial ⟨110⟩ strain parallel and perpendicular to the transport direction. Experiments: [82]. Lines: this model.*

quite separated due to large difference between the quantization masses (see Fig. 4.6), the repopulation effect is weak and saturates at small stress levels, while the interband scattering is remarkably reduced by strain-induced valley splitting. In addition, the decrease of the transport effective mass m_{x_3} shown in Fig. 4.7 when tensile stress is applied in the transport direction is also beneficial (Eq. 1.28), especially under high mechanical stress.

A final validation of the mobility model under uniaxial ⟨110⟩ stress is reported for electrons in Fig. 4.9, where the mobility enhancement as a function of strain

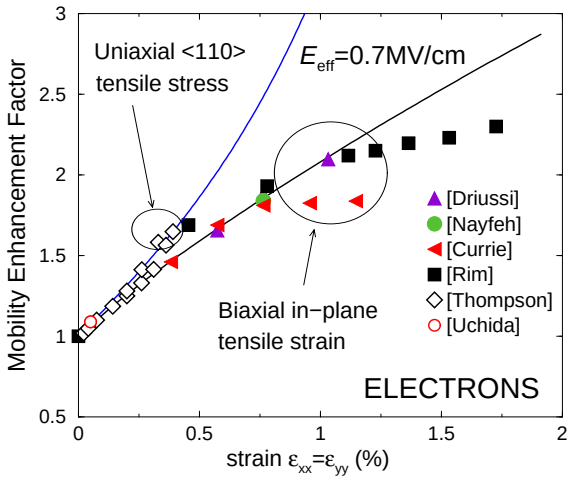

Figure 4.9: *Effective electron mobility enhancement as a function of strain. Experiments: [76], [77], [41], [42], [6] [81].*

is compared with experimental results obtained using high strain wafer bending. The biaxial case is also reported for comparison, showing that the enhancement for uniaxial $\langle 110 \rangle$ stress is higher than for the biaxial case due to the effective mass deformation with shear strain. A negligible dependence on effective field is observed on a range from 0.4 to 1 MV/cm (not shown).

(100)/⟨100⟩ nFETs

For completeness, the model has been generalized to account for uniaxial stress along $\langle 100 \rangle$ in-plane crystal directions. It is worth noting that the last term in the denominator of (4.8) is different from zero only when uniaxial stress along $\langle 100 \rangle$ crystal directions is applied ($\varepsilon_{xx} \neq \varepsilon_{yy}$). The parameter η_3 in (4.8) has been therefore calibrated on experiments for (100)/$\langle 100 \rangle$ nFETs, as shown in Fig. 4.10 for both compressive and tensile stress and for stress directed both parallel and perpendicular to the transport direction.

(110)/⟨110⟩ nFETs

For (110)/$\langle 110 \rangle$ nFETs, $m_{t\langle 110 \rangle}$ and $m_{t\langle -110 \rangle}$ in (4.13) correspond to m_{x_3} and m_{z_3}, respectively (see section 1.5). The variation of m_{z_3} is neglected in our model for (110) crystal orientation, since it would make the energy splitting between the unprimed four-fold ladder "1"-"2" and the primed two-fold ladder "3" to be overestimated. The energy splitting calculated with full-band approach in [34] when uniaxial stress is applied along $\langle 110 \rangle$ is thus nicely reproduced by the analytical model in (4.3) with the additional shear term in (4.12) (see Fig. 4.11).

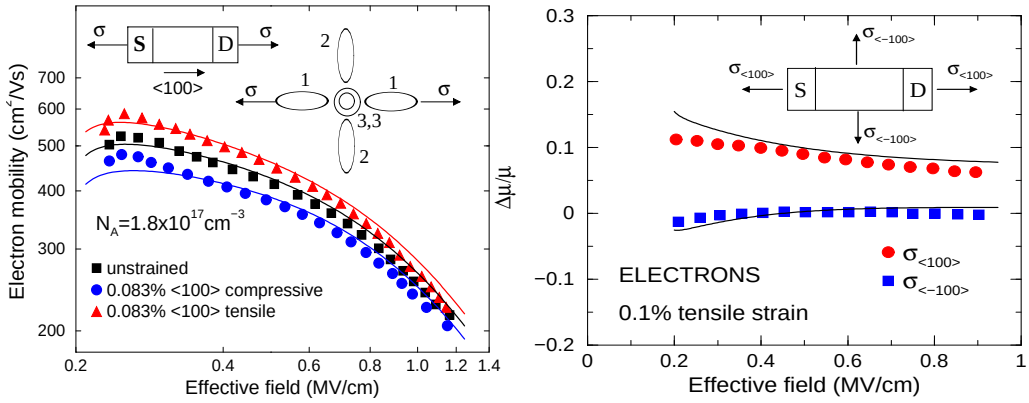

Figure 4.10: *(Left) Effective electron mobility under uniaxial ⟨100⟩ tensile and compressive strain for (100)/⟨100⟩ nFETs. (Right) Electron mobility change under tensile uniaxial ⟨100⟩ strain parallel and perpendicular to the transport direction. Experiments: [82]. Lines: this model.*

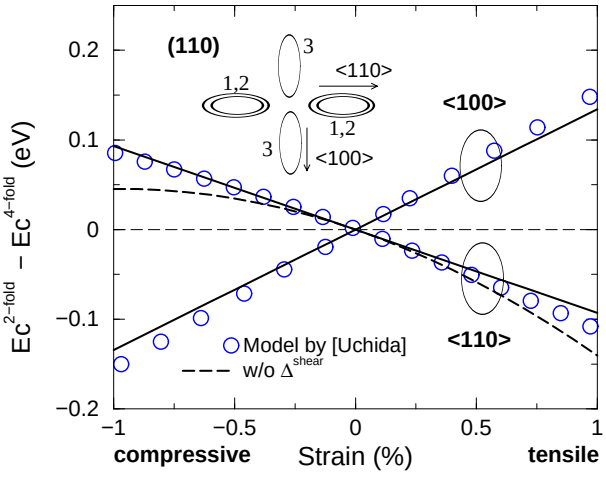

Figure 4.11: *Energy difference between 2-fold valley and 4-fold valley minima of (110) crystallographic plane as a function of strain. The model (solid lines), accounting for additional shift due to shear strain (4.12), is compared with calculations in [34]. The model in (4.3) is also reported for comparison (dashed lines).*

Differently from the (100) orientation, where the most relevant effect influencing electron mobility is the variation of scattering contributions with strain, in (110)-oriented planes valley repopulation and effective mass change are dominant in the mobility enhancement. For (110)/⟨110⟩ nFETs the applied stress is advantageous when the primed two-fold valley "3" is repopulated, because of its lower effective mass along the transport direction (see Fig. 4.6). This holds when the primed and unprimed valley edges are moved closer to each other by

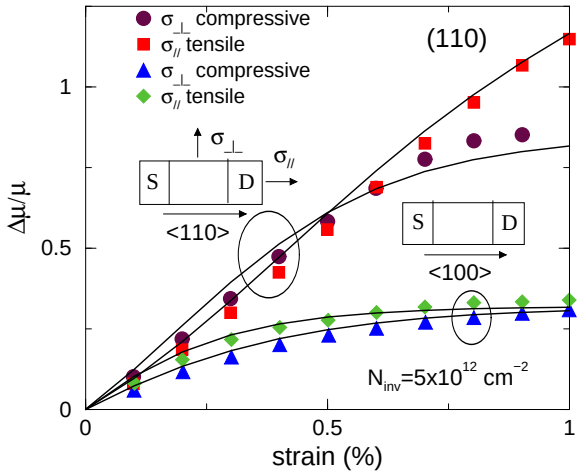

Figure 4.12: *Electron mobility enhancement for (110)-nFETs as a function of strain for different configurations. Symbols: numerical calculations from [34]. Lines: this model.*

applying uniaxial tensile stress along the transport direction or compressive along the width direction.

(110)/⟨100⟩ nFETs

On the other hand, in (110)/⟨100⟩ nFETs the stress produces a mobility enhancement when the unprimed four-fold ladder "1"-"2" is repopulated, because of its lower effective mass along the transport direction (see Fig. 4.6). This condition is accomplished again if tensile stress along the transport direction or compressive along the width direction is applied.

In Fig. 4.12, all the favorable conditions above are examined for high strain levels, where the analytical model is compared with numerical calculations from [34]. No change in the scattering contributions with stress is considered. It is worth noting that (110)/⟨110⟩ nFETs shows higher mobility enhancement than (110)/⟨100⟩ nFETs. Moreover, (110)/⟨110⟩ nFETs under uniaxial ⟨110⟩ stress shows up to be the best configuration, since the mobility enhancement does not saturate even at high strain levels, thanks to the reduction of the conduction effective mass. On the other hand, the mobility enhancement by uniaxial ⟨100⟩ compressive stress saturates at high stress, since the change of the electron population saturates at large energy splittings. The model for uniaxially-stressed (110)-nFETs is validated on experiments for different stress configurations in Fig. 4.13 for low strain level and in Fig. 4.14 with numerical calculations from [34] for high strain.

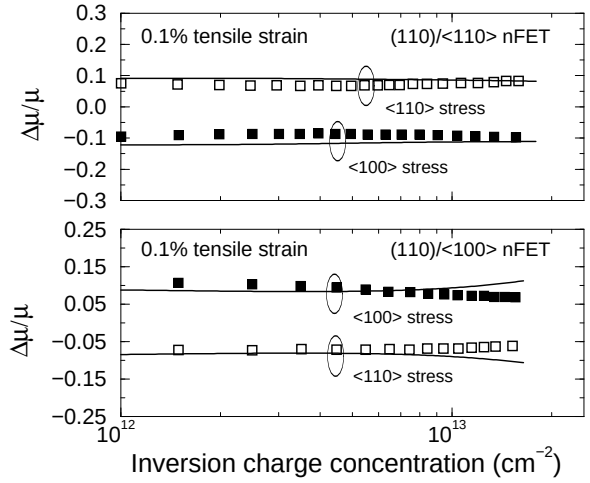

Figure 4.13: *Electron mobility variation versus inversion charge concentration in (110)/⟨110⟩ and (110)/⟨100⟩ nFETs. Symbols: experiments from [34]. Lines: this model.*

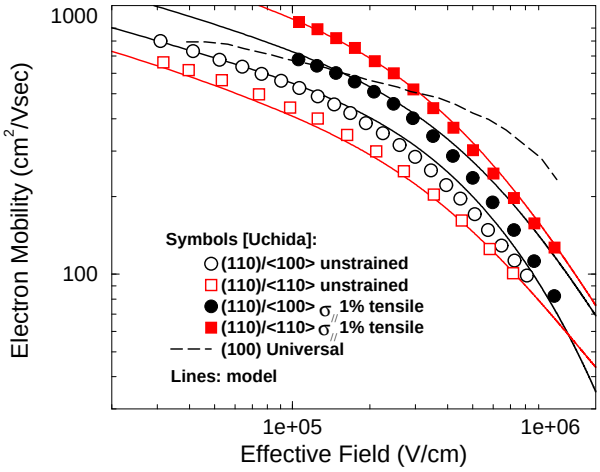

Figure 4.14: *Electron mobility versus inversion charge concentration in (110)/⟨110⟩ and (110)/⟨100⟩ nFETs. Symbols: calculations from [34]. Lines: this model. The (100) universal curve is also shown for comparison.*

4.2.2 Hole mobility

(100)/⟨110⟩ pFET

As far as the valence band deformation under uniaxial stress conditions is concerned, starting from the circular parabolic band model, the change in the parallel ⟨110⟩ and perpendicular ⟨-110⟩ directions with respect to the stress has been considered as depicted in Fig. 4.15.

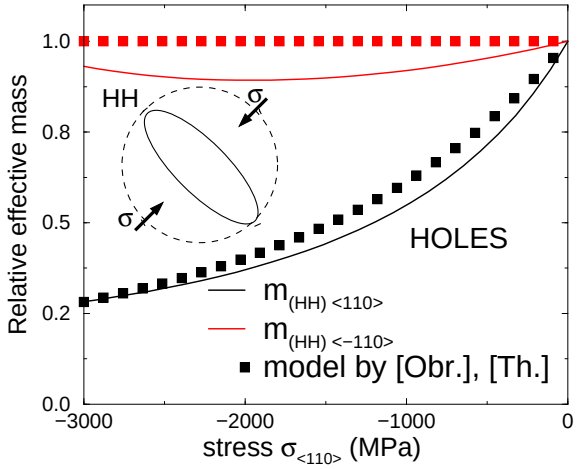

Figure 4.15: *The HH band is modeled as a single ellipsoid with stress dependent transverse ($m_{(HH)<-110>} = m_{y_2}$) and longitudinal ($m_{(HH)<110>} = m_{x_2}$) masses (lines). Symbols: data by [83] and [75].*

The model reads:

$$\frac{1}{m_{x_2}^{\text{str}}} = \frac{1}{m_{x_2}^{\text{unstr}}} \left(1 + \sum_{j=1,2} c_{2,j}\, \varepsilon_{xy}^{j} \right) \tag{4.15}$$

$$\frac{1}{m_{y_2}^{\text{str}}} = \frac{1}{m_{y_2}^{\text{unstr}}} \left(1 + \sum_{j=1,2} d_{2,j}\, \varepsilon_{xy}^{j} \right) \tag{4.16}$$

where $m_{x_2}^{\text{unstr}} = m_{y_2}^{\text{unstr}} = 0.43 m_0$ (see Fig. 4.6) and the fitting parameters $c_{2,j}$ and $d_{2,j}$ are reported in Appendix A-table A.6. The phonon inverse MRT variation with strain is accounted for as in (4.11). From the above expressions the corresponding 2DHG mass tensor and the density-of-states effective mass can be easily obtained for the hole mobility computation (see section 2.1). The model for uniaxially-stressed (100)-pFETs is shown in Fig. 4.16 for both compressive and tensile stress.

A final validation of the mobility model under uniaxial ⟨110⟩ stress is reported for holes in Fig. 4.17, where the mobility enhancement as a function of strain is compared with experiments on uniaxial ⟨110⟩ compressive strain (using wafer bending [6] or extracted from devices with SiGe source/drain regions or compressive contact etch-stop layers [84]). The biaxial results are also reported for comparison. The hole mobility presents the highest enhancement with uniaxial compressive stress (validated with experiments up to a factor 3), mainly due to the HH transport effective mass (m_{x_2}) reduction in Eq. (4.15). A relevant dependence on electric field is observed for both biaxial and uniaxial stress cases,

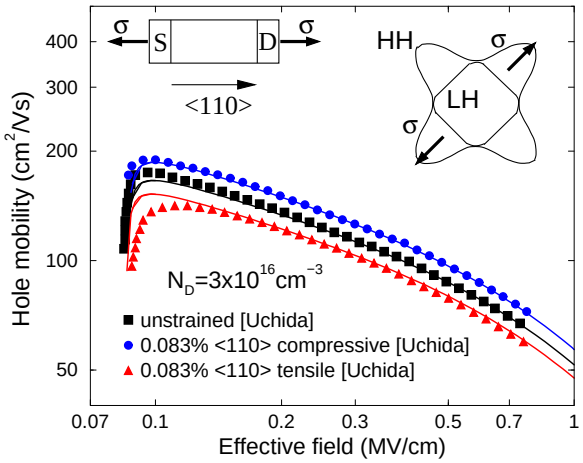

Figure 4.16: *Effective hole mobility under uniaxial ⟨110⟩ tensile and compressive strain for (100)-oriented substrates. Experiments: [82]. Lines: this model.*

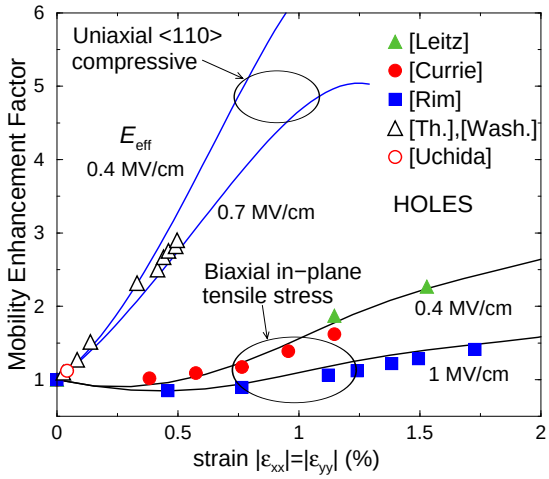

Figure 4.17: *Effective hole mobility enhancement as a function of strain. Experiments: [80], [41], [42], [6] [84] [82]. Lines: this model.*

showing that the hole mobility enhancement with strain is partly lost at higher transverse effective electric fields.

(110)/⟨110⟩ pFETs

As fas as the (110) valence band is considered, HH valley presents ellipsoidal shape in the (110) plane (see Fig. 4.6). In order to take into account the HH band deformation under ⟨110⟩ uniaxial stress, the density-of-states effective mass $m_{d_2} = \sqrt{m_{x_2} m_{y_2}}$ has been modeled as a function of shear strain following [75] as

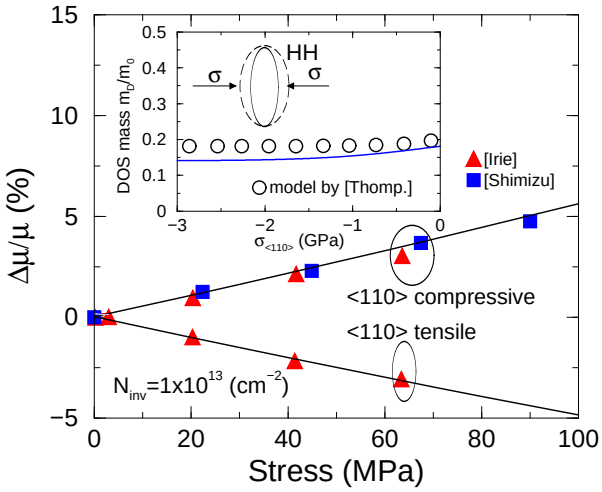

Figure 4.18: *Hole mobility variation in (110)/⟨110⟩ pFETs under uniaxial stress along the transport direction versus stress. Symbols: experiments [53], [85]; lines: this model. Inset: density-of-state effective mass variation as a function of stress. Symbols: model from [75]*

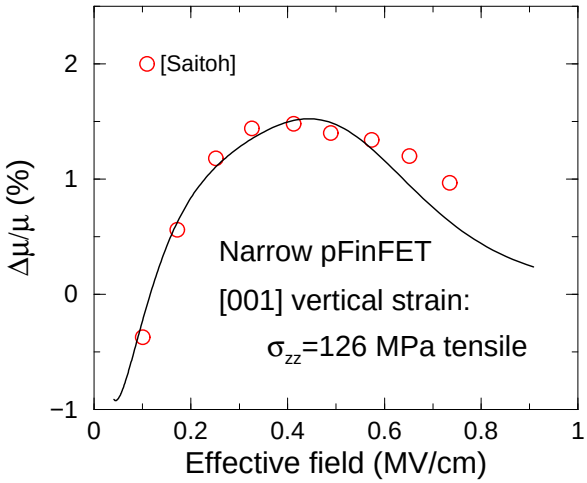

Figure 4.19: *Hole mobility variation in pFinFET under uniaxial stress along the fin-height direction versus effective electric field. Symbols: experiments [86]; lines: model.*

shown in the inset of Fig. 4.18. The model reads:

$$m_{x_2}^{\mathrm{str}} = m_{x_2}^{\mathrm{unstr}} \left(f_0 + \frac{f_1}{1 + \exp\left(\varepsilon_{xy}/\varepsilon_0\right)} \right) , \tag{4.17}$$

with $m_{x_2}^{\mathrm{unstr}} = 0.122\, m_0$ (see Fig. 4.6), $f_0 = 0.6$, $f_1 = 0.8$ and $\varepsilon_0 = 1.884 \times 10^{-3}$. m_{y_2} is left unchanged. The increase (decrease) of m_{d_2} in the presence of

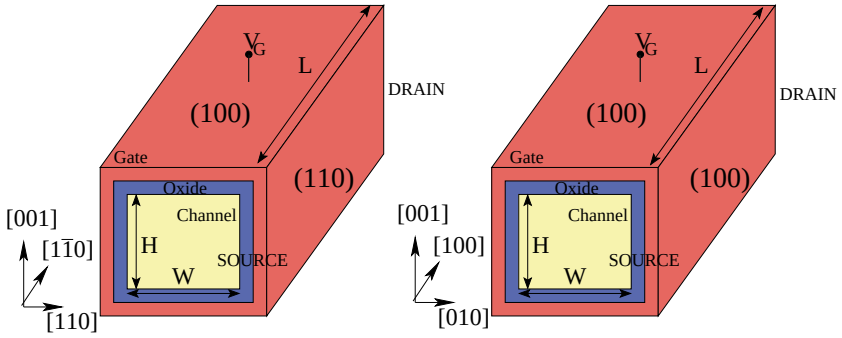

Figure 4.20: *3D schematic view of the SiNW FET. Also shown the crystallographic orientations of the top, bottom and lateral planes along with the crystallographic directions of the transport, the device width and the device height directions.*

uniaxial ⟨110⟩ tensile (compressive) strain makes the effective mobility to decrease (increase), as shown in Fig. 4.18.

(110)/⟨100⟩ pFETs

On the other hand, the uniaxial ⟨100⟩ strain does not affect m_d and only a repopulation effect occurs, thus being less effective on mobility as shown in Fig. 4.19, where the model is compared with the slight experimental mobility enhancement observed when tensile uniaxial stress is applied along the fin height direction of a narrow FinFET (i.e., where the transport occurs manly on (110) sidewalls, as will be explained in detail in the next section).

4.3 Mobility model for non-planar FETs

As already mentioned before in this thesis, multi-gate (MuG) devices with a non-planar structure are being studied for the next technology nodes. Several experimental demonstrations have been reported in the last years, moving from partially gate-covered channels, as vertical double-gate FETs or FinFETs (where the gate stack is on three sides), to gate-all-around devices, such as silicon nanowires (SiNW) FETs.

In Fig. 4.20 a 3D sketch of the rectangular SiNW FETs is shown, where the semiconductor is completely surrounded by the gate stack, which ensures the best electrostatic control on the conducting channel. The two most common orientations are shown, where the sidewalls are (100)- or (110)-oriented, depending on the crystallographic direction of the transport.

Experimental measurements have been recently carried out on long-channel rectangular SiNW-FETs and FinFETs with different widths and orientations,

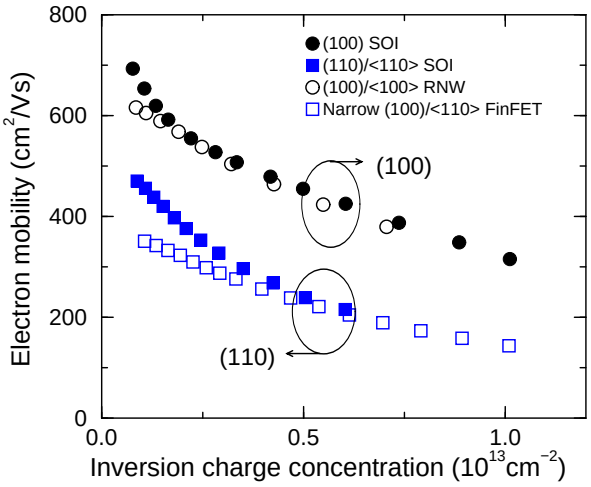

Figure 4.21: *Recently extracted experimental mobilities from [87] and [88] for vertical FETs (i. e., rectangular SiNW FETs with all the interfaces oriented along (100) crystallographic orientation and narrow FinFETs with sidewalls along (110) crystallographic planes) are compared with mobilities for planar FETs on (100) and (110) crystallographic orientations.*

showing that the effective mobilities in non-planar devices with a dominant transport contribution along the (100)/[1$\bar{1}$0] or (110)/[1$\bar{1}$0] directions tend to the corresponding universal curves, with the exclusion of the values at low N_{inv}, which are affected by a stronger impact of the interface states, as shown in Fig. 4.21. The above results suggest that a unified mobility model for (100)- and (110)-oriented UTB planar devices could be applied to non-planar device mobilities by correctly combining the top- and sidewall-channel contributions.

A 3D schematic of the FinFET is reported in Fig 4.22. The typical orientation with sidewall channels on a (110) crystallographic plane and the transport along the [1$\bar{1}$0] direction is illustrated. The equienergy surfaces of the six conduction band minima and of the HH and LH valleys projected on the (110) plane are also reported, as well as the relative effective masses along with the relevant directions. The top channel lies on a conventional (100) plane with [1$\bar{1}$0] transport direction. In the following, a FinFET structure is considered, but the model can be easily extended to SiNW FETs. As proposed in [71], the effective mobility of a FinFET of $W > 75$ nm can be written as the average of the effective mobilities in the top and sidewall channels:

$$\mu_{\text{eff}} = \frac{\mu_{\text{top}} W + \mu_{\text{lateral}} 2H}{2H + W} \,. \tag{4.18}$$

Eq. (4.18) holds under the assumption that the charge is equally distributed in the top and sidewall channels. Otherwise, the inverse charge contributions have to be taken into account. By using Eq. (4.18) and the models described so far, the

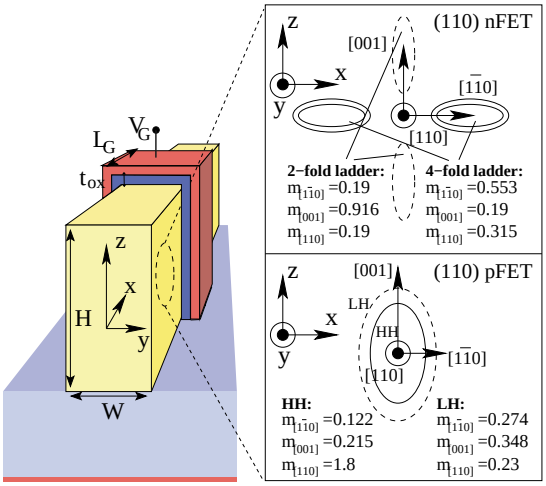

Figure 4.22: *3D schematic view of a FinFET. Also shown the isoenergetic surfaces projected on the (110) plane for electrons and holes, along with the relative conduction and quantization effective masses.*

effective mobility for both electrons and holes is nicely reproduced for FinFETs with $SiO_2/HfO_2/TiN$ gate stack and with W down to 75 nm (see Fig. 4.23 for hole mobility with no stress). For $W < 75$ nm, the rounding of the fin corners must be taken into account. Following [89], a (111) crystallographic orientation can be assumed in the corners. Hence, the FinFET mobility can be written as:

$$\mu_{\text{eff}} = \frac{\mu_{\text{top}} W' + \mu_{\text{lateral}} 2H' + \mu_{\text{c}} L_{\text{c}}}{2H' + W' + L_{\text{c}}}, \tag{4.19}$$

where μ_{c} is the corner mobility, and W', H' and L_{c} are the effective width, height and corner extensions, respectively, which need to be extracted from TEM images as shown in the inset in Fig. 4.23. By using Eq. (4.19), the carrier mobility is nicely predicted for FinFETs with W down to 25 nm (Fig. 4.23).

For width narrower than 25 nm, the presence of intrinsic stress related to the fabrication process can not be neglected, especially when metal gates are used [70]. In such narrow structures, the fin height is usually about 50-60 nm and the transport occurs mainly on (110)-oriented sidewalls, thus the above modeled strain effects for (110) FETs are essential to correctly evaluate the carrier mobility. In Figs. 4.24 and 4.25, the model is nicely compared with experiments on narrow FinFETs with different stress configurations. The corresponding (110) mobilities for planar devices are also reported for comparison. The slight differences between the unstrained mobilities (filled symbols) are due to stronger impact of interface charges in complex 3D structures ($N_{it} = 9 \times 10^{11}$ cm^{-2} has been used in Eq. (1.50) to fit the unstressed FinFET mobility from [88]). Moreover, remote scatterings are considered for thin oxides (FinFETs measured in [88] have $t_{\text{ox}} = 2.2$ nm) and for $SiO_2/HfO_2/TiN$ gate stack (FinFETs measured in

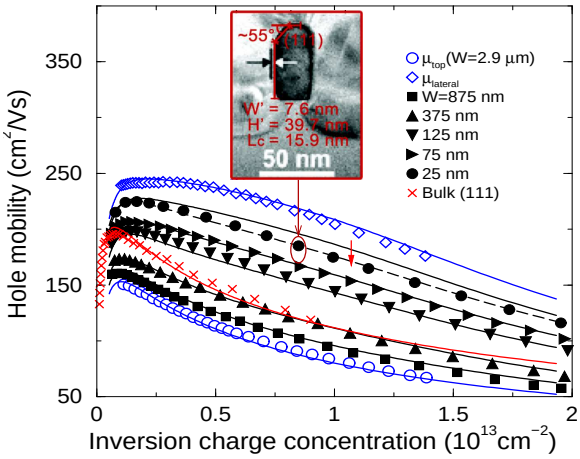

Figure 4.23: *Hole mobility of FinFETs with W ranging from 2875 to 25 nm. Symbols: experiments [71]. Solid lines: this model using Eq. (4.18). Dashed line: this model using Eq. (4.19). Inset: TEM image of the narrow FinFET (W = 25 nm) [71], with the extracted geometrical extensions.*

[70] have $t_{\mathrm{IL}} \approx 1$ nm). For electrons, strained FinFETs can reach a relevant mobility enhancement when a longitudinal tensile stress is applied, with a resulting mobility comparable to the bulk (110) case under similar stress. Vertical compressive strain in FinFET channel, due to both intrinsic stress in TiN metal gate and to differences in thermal expansion coefficients following plastic relaxation at high temperature [70], also contributes to enhance electron mobility. Finally, into such narrow fins almost fully elastic strain relaxation is known to take place along the fin width direction [88], [90], thus the effects of the corresponding strain component are not studied in this thesis.

On the contrary, the hole mobility shows a slight enhancement at low inversion charge concentrations and degradation at higher inversion charge concentrations with respect to the (110) planar case, respectively, when a high compressive vertical strain is present in the channel. A strong tensile stress along the transport direction seriously degrades hole mobility. This suggests that, assuming a symmetric variation of the HH conduction mass with strain, longitudinal compressive stress would strongly enhance hole mobility. Unfortunately, to the author knowledge, no experimental measurements with high compressive longitudinal stress are available in literature to date to validate the model. The vertical compressive stress induced by 3 GPa tensile TiSiN metal gate (MG), with thickness 7 nm in [91], is estimated by the formula:

$$\sigma_{\mathrm{Si}} \approx \frac{\sigma_{\mathrm{MG}}}{(W_{\mathrm{fin}}/t_{\mathrm{MG}} + Y_{\mathrm{MG}}/Y_{\mathrm{Si}})}\,, \tag{4.20}$$

with σ_{MG} and t_{MG} the intrinsic stress in the metal electrode and its thickness, respectively, and Y_{MG} (for TiSiN [92]) and Y_{Si} the elastic moduli of the metal

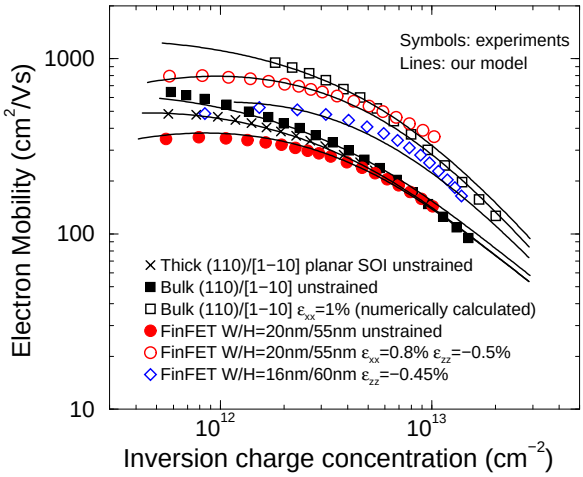

Figure 4.24: *Electron mobility of (110)/[1$\bar{1}$0] planar and vertical devices under different stress conditions. Symbols: experiments [88], [70] and numerical calculations [34]. Lines: this model. A compressive vertical strain of 0.45% in assumed for the data in [70], as measured for a 20 nm-wide FinFET.*

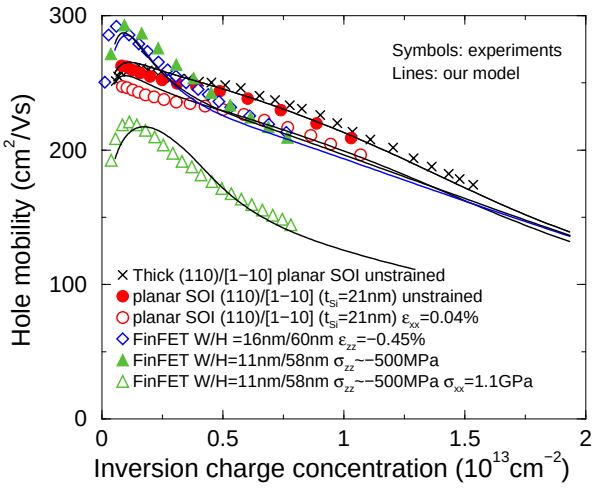

Figure 4.25: *Hole mobility of (110)/[1$\bar{1}$0] planar and vertical devices under different stress conditions. Symbols: experiments [93], [70], [91]. Lines: this model. A compressive vertical stress of about 500 MPa is estimated to be induced by 3 GPa tensile metal electrode in [91].*

gate and silicon underneath, respectively. With $Y_{\mathrm{MG}} \approx 500$ GPa (for TiSiN [92]), $Y_{\mathrm{Si}} \approx 130$ GPa and $W_{fin} = 11$ nm, a value of about 500 MPa is estimated and used in the simulations.

4.4 Summary

In this chapter, a new analytical model for the electron and hole low-field mobility in ultra-thin body structures with differently-oriented channels and accounting for the effects of mechanical stress has been developed and calibrated on planar FETs. The new model is used to compute the effective mobility of non-planar FinFETs averaging the top- and sidewall-channel mobilities. Experimental data for a wide range of planar and non-planar devices are nicely reproduced demonstrating a good predicting capability in FinFETs. The model can be useful to extend the standard TCAD commercial tools to the performance prediction of post-CMOS technology nodes.

Chapter 5

QDD simulations

In the first part of this thesis, unified models for the low-field effective electron and hole mobilities in MOSFETs, which feature ultrathin SiO_2/HfO_2 gate stacks, different substrate and channel orientations, quantum-confinement effects for single-gate (SG) and double-gate (DG) SOI FETs, and general stress conditions, are presented. In the previous chapter the models for planar FETs have been combined and applied to the study of the effective mobility in vertical architectures. In this chapter the mobility models are included in a 1D quantum drift-diffusion (QDD) solver in order to investigate the *I-V* characteristics improvements related with mobility enhancement.

The QDD tool features are illustrated in section 5.1. Then the simulation studies of nMOSFETs aimed at investigating the impact of different surface orientations, silicon-film thicknesses (for SOI and DG devices) and uniaxial stresses are decribed in sections 5.2, 5.3 and 5.4, respectively.

5.1 1D quantum drift-diffusion model

For relatively-long devices, i.e. for channel lengths greater than the average distance that the charge carrier travels in the semiconductor before being scattered (carrier mean-free path), estimated to be in the 10-20 nm range (depending on the channel length and the transverse electric field [94]), an accurate simulation of carrier transport is possible using a technique which combines the solution of the coupled SchrödingerPoisson equations within the device cross sections normal to the transport direction with the classical drift-diffusion model. This approach is referred to as quantum drift-diffusion (QDD). The theoretical foundations of such approach, given in [95], are reported in the following.

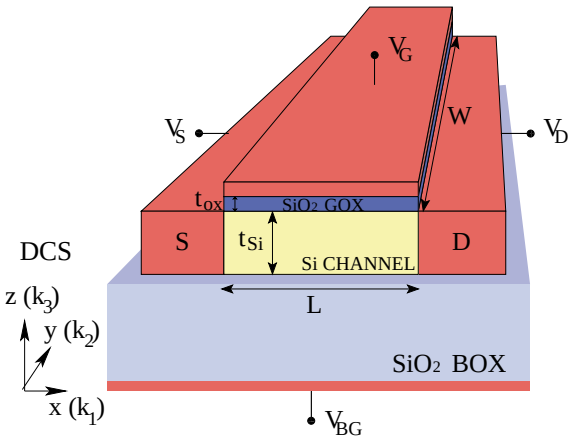

Figure 5.1: *Schematic of the ultrathin-body device structure. The device coordinate system consists of orthogonal axes x, y, and z along the transport, width, and thickness directions, respectively.*

Semiconductor devices where the electron gas is structurally confined in one-dimension, such as UTB SG- or DG-FETs are considered here. However, the treatment holds for non-planar devices, such as FinFETs and SiNW FETs, as well with minor changes. As already pointed out in section 1.3, the physical description of the device electrostatics can be derived by solving the Poisson and Schrödinger equations, namely

$$\nabla_{\mathbf{r}} \cdot (\epsilon_{\mathrm{Si}} \nabla_{\mathbf{r}} \phi) = \rho \tag{5.1}$$

$$\left(-\frac{\hbar^2}{2} \left(\nabla_{\mathbf{r}} \cdot \frac{\nabla_{\mathbf{r}}}{\hat{m}} \right) + U(\mathbf{r}) \right) \psi = E\psi \ , \tag{5.2}$$

where the kinetic energy operator has been written in compact form, with $1/\hat{m}$ the inverse effective-mass tensor. The device coordinate system is oriented as shown in Fig. 5.1, where the z axis is normal to the Si/SiO_2 interface, the current transport is assumed along the x-direction and the y-axis is along the device width. The UTB FET has a translational symmetry along the width, so that we can solve 5.1 and 5.2 in the (x, z) plane. Thus, the position vector $\mathbf{r}$ refers to (x, z) coordinates. Finally, it is assumed that the wave function can be decomposed into the product of two separate functions of x and z, i.e. $\psi(x, z) = \varsigma(x)\zeta(z)$, with $\zeta(z)$ a real function. If the channel length is larger than the carrier mean-free path, electrons in the channel are expected to suffer several collisions. In this case, electron transport in the longitudinal direction can be recounted by a modified drift-diffusion model which, however, must be harmonized with the Schrödinger equation. The key to ensure this compatibility is Bohm's theory, according to which the time-dependent Schrödinger equation can be decomposed into two coupled equations with unknowns $R = |\psi|$ and $S = \hbar \arg[\psi]$ [96]. The

first one is a norm conservation equation; the second one can be interpreted as the Hamilton–Jacobi equation, provided a quantum potential $Q(\mathbf{r})$ is added to the classical potential $U(\mathbf{r})$. This means that a classical description of electron transport is possible even for decananometer-size devices without resorting to the Ehrenfest theorem. Bohm's quantum potential for a conduction electron in a semiconductor crystal is

$$Q(\mathbf{r}) = -\frac{\hbar^2}{2R}\left(\nabla_{\mathbf{r}} \cdot \frac{\nabla_{\mathbf{r}} R}{\hat{m}}\right) . \tag{5.3}$$

If the potential is independent of x, i.e. $U(x,z) = U(z)$, we may assume that $\varsigma(x) = \exp(jk_1 x)$. Under this simplifying assumption $R(x,z) = |\psi(x,z)| = \zeta(z)$. Eq. (5.3) turns out to be quite similar to the usual Schrödinger-like equation for $\zeta(z)$

$$\left(-\frac{\hbar^2}{2m_{z_v}}\nabla_z^2 + U(z)\right)\zeta_{i,v}(z) = E_{i,v}\zeta_{i,v}(z) , \tag{5.4}$$

and becomes identical to it if it is assumed

$$Q(z)_{i,v}(z) = E_{i,v} - U(z) . \tag{5.5}$$

Thus, according to the previous identification, Bohm's potential as well will assume the discrete set of determinations $Q_{i,v}$ for the electrons pertaining to the i^{th} subband of the v^{th} valley. Eq. (5.5) shows that, in a stationary state, Bohm's potential represents the electron kinetic energy associated with its vibrational motion normal to the Si/SiO_2 interface. When a voltage is applied to the drain of the FET, the energy eigenvalues $E_{i,v}$, which also represent the subband edges, are not uniform anymore, i.e. $E_{i,v} = E_{i,v}(x)$. Thus, the electrons pertaining to the i^{th} subband will be subject to a driving force given by $\nabla_x E_{i,v} = \nabla_{\mathbf{r}}[U(\mathbf{r}) + Q_{i,v}(\mathbf{r})]$.

The transport equation in the i^{th} subband, suitably corrected to account for Bohm's potential in the drift-diffusion model reads

$$\mathbf{J}_{i,v} = \mu_{i,v} N_{i,v} \nabla_x E_{i,v} + q D_{i,v} \nabla_x N_{i,v} = \mu_{i,v} N_{i,v} \nabla_x E_{\mathrm{Fn},i,v} \ , \tag{5.6}$$

where $\mathbf{J}_{i,v}$ is the current density per unit width in the i^{th} subband of the v^{th} valley; $N_{i,v} = N_{i,v}(x)$ is the electron concentration of the 2DEG per unit area in the i^{th} subband given in Eq. (1.11) and $E_{\mathrm{Fn},i,v}$ is the electron quasi-Fermi level. Also, $\mu_{i,v}$ and $D_{i,v}$ are the electron mobility and diffusivity, respectively, in the same subband. It should be noticed that, under degenerate conditions, the Einstein relationship is modified in order to ensure that the current vanishes in equilibrium. The generalized Einstein relationship for a 2DEG becomes

$$\frac{D_{i,v}}{\mu_{i,v}} = \frac{k_B T}{q} \ln(1 + \exp(-(E_{i,v} - E_{\mathrm{Fn},i,v})/k_B T))(1 + \exp((E_{i,v} - E_{\mathrm{Fn},i,v})/k_B T)) . \tag{5.7}$$

Finally, the continuity equations to be solved are

$$\nabla_x \cdot \mathbf{J}_{i,v} - C_{i,v} = 0 \ , \tag{5.8}$$

where $C_{i,v} = C_{\mathrm{in},i,v} - C_{\mathrm{out},i,v}$ represents the difference between the number of electrons scattered in and out of the i^{th} subband per unit area and unit time. The total current density $\mathbf{J}$ is simply obtained by summing up the contributions $\mathbf{J}_{i,v}$ of the individual subbands, i.e.

$$\mathbf{J} = \sum_v \sum_i \mu_{i,v} N_{i,v} \nabla_x E_{i,v} + q D_{i,v} \nabla_x N_{i,v} \ . \tag{5.9}$$

Here, a QDD solver for UTB FETs on different crystal orientations is presented. The Schrödinger-Poisson tool introduced in section 1.3 is coupled with the 1D drift-diffusion solver in the longitudinal direction of the device. The solution of the Schrödinger-Poisson problem, indeed, depends on the quasi-Fermi potential profile along the x-direction, which is used for the calculation of the charge density. It is provided by the solution of the drift-diffusion equations. The procedure is iterated until an overall convergence is reached.

The effective mobility models described in the previous chapters as a function of the effective field E_{eff} and the inversion charge concentration N_{inv} have been directly incorporated in the 1D transport model, provided E_{eff} and N_{inv} are calculated in each cross-section, without transforming them into local mobility models, as required in classical simulation codes. It is assumed that the mobility is the same for each subband belonging to the same valley ($\mu_{i,v} \rightarrow \mu_v$).

The QDD solver allows to easily include the effects of mechanical stress on device performance. To this purpose, besides the mobility change, accounted for by means of the strain mobility model (see Chapter 4), the strain induced valley edge splittings in Eqs. (4.3) and (4.12), have been addressed in the Schrödinger problem, thus allowing to consider in the simulations the threshold voltage variation with strain.

In order to account for the velocity saturation effect at high longitudinal electric fields, the QDD model assumes the high-field saturation of mobility as given by the Caughey-Thomas formula [97]:

$$\mu(E_\parallel) = \frac{\mu_{\mathrm{low}}}{\left[1 + \left(\frac{\mu_{\mathrm{low}} E_\parallel}{v_{\mathrm{sat}}}\right)^{\beta}\right]^{1/\beta}} \tag{5.10}$$

where μ_{low} denotes the low-field mobility, $E_\parallel$ the electric field component along the transport direction, $v_{\mathrm{sat}} = 10^7$ cm/s the saturation velocity and β a parameter ($\beta = 1.109$ and 1.213 for electrons and holes, respectively). Such approach is expected to underestimate the on-currents of short-channel devices, when the transport becomes quasi-ballistic [98]. No attempt has been made to change the mobility parameters in the high-field conditions in order to empirically correct

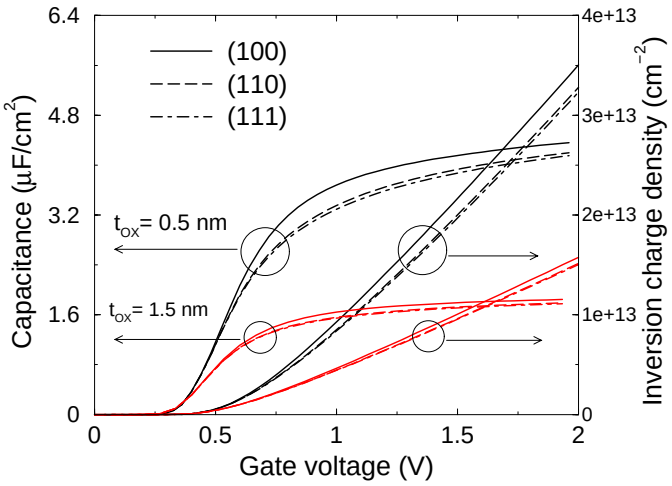

Figure 5.2: *Inversion charge density and capacitance vs. gate voltage for two different EOTs given by the Schrödinger-Poisson solver.*

the saturation velocity. Anyway, the calculated current characteristics have been analyzed so to find out the relative importance of the low-field mobility.

5.2 Analysis of SOI FETs with different surface orientations

The inversion charge and gate capacitance of MOS capacitors with different orientations are reported in Fig. 5.2 as a function of the gate voltage, showing the orientation influence for device with equivalent oxide thicknesses (EOTs) less than 2 nm. A relative difference of the capacitance for the (110) and (111)orientations with respect to the (100) one at $V_{\rm GS} = 1$ V of about 5% and 10% is found for the EOT = 1.5 and 0.5 nm, respectively.

Fig. 5.3 show the turn-on characteristics at low and high drain voltage for two different SG-SOI MOSFETs, with two gate lengths (L) and silicon thicknesses $t_{\rm Si}$, on different wafer orientations. Also indicated are the relative current variations with respect to the (100) case at $\rm V_{GS} = 1$ V. Such values should be compared with the corresponding relative variations of the low-field mobility indicated in Fig. 5.4 for an effective field corresponding to the average along the channel.

At low $\rm V_{DS}$, current and mobility variations almost match, in particular for the FETs with the larger thickness. At high $\rm V_{DS}$, the channel velocity partly saturates, making the current variation smaller. This is more evident in the shorter MOSFETs.

Furthermore, the effect of different surface/channel orientations on the maximum transconductance $g_{m_{\rm MAX}} = (\partial I_{\rm DS}/\partial V_{\rm GS})_{MAX}$ calculated at $V_{\rm DS} = 0.05$ V

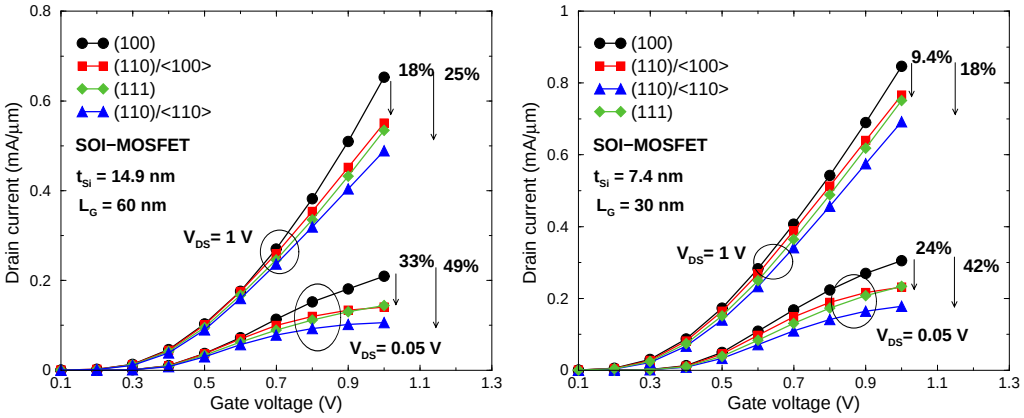

Figure 5.3: *Calculated turn-on characteristics of SG-SOI FETs on different substrates and channel directions with: (left) 14.9 nm silicon thickness, 60 nm channel length and 1 nm SiO_2 oxide thickness; (right) 7.4 nm silicon thickness, 30 nm channel length and 1 nm SiO_2 thickness.*

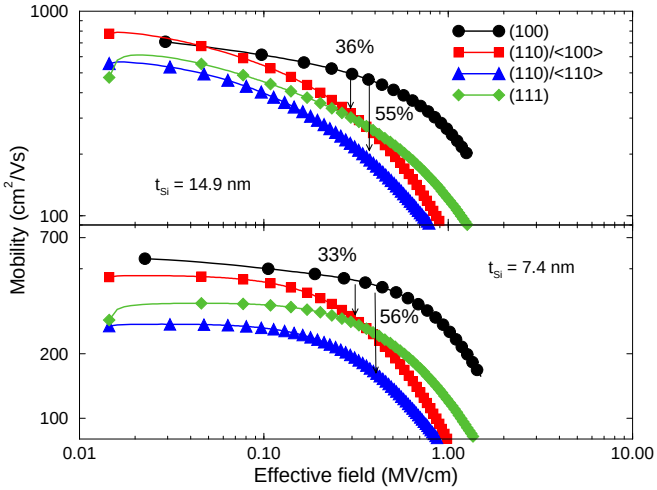

Figure 5.4: *Calculated electron mobility in SOI-MOSFETs on different substrate and channel directions versus the effective field for two silicon thicknesses.*

and on the on current I_{ON} for two SG-SOI FETs and one DG-SOI FET with different channel lengths and EOT = 1.4 nm has been investigated. Geometrical data and biases are given in the caption of Fig. 5.5, which reports the relative variations with respect to the best performing (100) wafer. Three considerations are useful to describe the results in Fig. 5.5: i) in general, shorter gate lengths induce a smaller orientation effect, due to the velocity saturation at high longitudinal fields; ii) the series source/drain resistances tend to mask the orientation effects for the shorter gate lengths; iii) the mobility degradation with orientation is stronger for thinner t_{Si}, as shown in Fig. 5.6, where the mobility curves as a

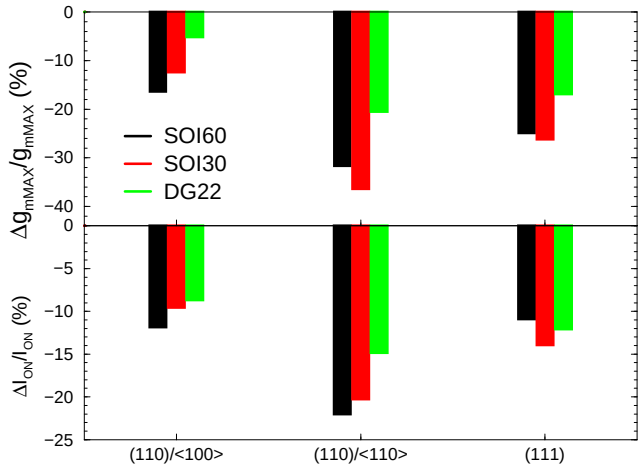

Figure 5.5: *Relative variation of* g_{mMAX} *and* I_{ON} *with respect to the (100) case calculated for two SG-SOI FETs and one DG-SOI FET with different channel orientations. SOI60:* $L = 60\,nm$, $t_{\mathrm{Si}} = 15\,nm$. *SOI30:* $L = 30\,nm$, $t_{\mathrm{Si}} = 7\,nm$. *DG22:* $L = 22\,nm$, $t_{\mathrm{Si}} = 10\,nm$. *All devices have 10 nm source/drain regions doped with* $5.2 \times 10^{19}\ cm^{-3}$. g_{mMAX} *is calculated with* $V_{\mathrm{DS}} = 0.05\ V$, I_{ON} *with* $V_{\mathrm{GS}} = 0.5\ V$ *and* $V_{\mathrm{DS}} = V_{\mathrm{DD}} = 0.85\ V$.

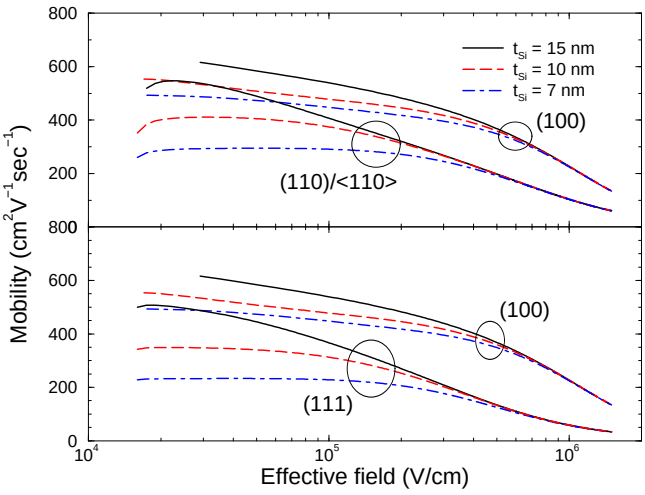

Figure 5.6: *Mobility vs. effective field for different channel orientations and* t_{Si} *= 15, 10 and 7 nm. Top: (100) and (110)/*$\langle 110 \rangle$ *cases. Bottom: (100) and (111) cases.*

function of the effective field for $t_{\mathrm{Si}} = 15, 10$ and 7 nm and different orientations are reported. This consideration applies mainly to the "SOI30" device.

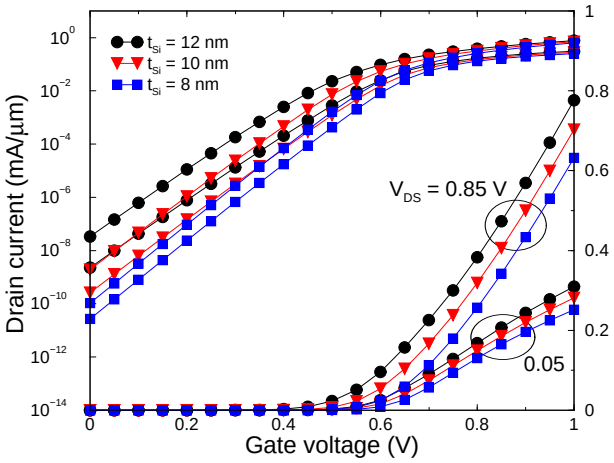

Figure 5.7: *Turn-on characteristics of a DG-FET with $L_G = 22\,nm$, $t_{\mathrm{IL}} = 0.7\,nm$ and $t_{\mathrm{HfO2}} = 2.9\,nm$ stack with TiN gate for different silicon thicknesses.*

Table 5.1: *DIBL, SS, I_{ON} and I_{OFF} of the DG-FET with different t_{Si}*

t_{Si} (nm)	12	10	8
DIBL (mV/V)	91	63	41
SS (mV/dec)	78	72	67
I_{ON} (μA/μm)	473	406	342
I_{OFF} (nA/μm)	0.033	0.0019	1.04×10^{-4}

5.3 Analysis of DG-FETs with different silicon thicknesses

The effect of different t_{Si} on the 22nm DG-FET by using a SiO_2/HfO_2 stack with $t_{\mathrm{IL}} = 0.7$ nm, $t_{HfO_2} = 2.9$ nm ($\kappa = 16$) and TiN gate (workfunction is 4.8 eV) has been analyzed. The use of TiN instead of Polysilicon allows a low channel doping of $1.2{\times}10^{15}$ cm^{-3} (the threshold voltage is set by the TiN workfunction and high channel doping is not needed), with an implicit advantage in the low-field mobility. The turn-on characteristics with different t_{Si} are shown in Fig. 5.7. The corresponding significant figures of merit to evaluate the device performance are also collected in table 5.1, i.e. the drain-induced barrier lowering (DIBL), the inverse subthreshold slope (SS), the on-current (I_{ON}) and the off-current I_{OFF}. As V_{DS} increases, a decrease of the source(or drain)-to-channel energy barrier is observed in short-channel MOSFETs, which is responsible of the large I_{OFF} at large V_{DS}. This short-channel effect (SCE) can be evaluated with the DIBL, which is the difference of the threshold voltage at low V_{DS} and the one at large

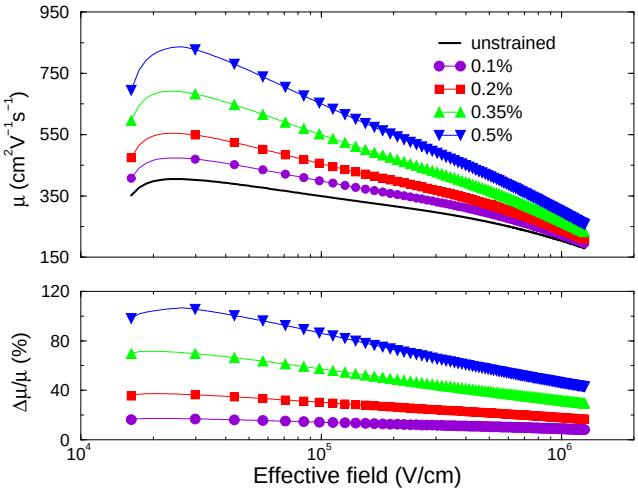

Figure 5.8: *Mobility (top) and mobility enhancement (bottom) as a function of the effective field as predicted by the model for uniaxial tensile* ⟨110⟩ *strain of 0.1, 0.2, 0.35 and 0.5%. The predicted mobility enhancement nicely reproduces the experimental findings in [6] by using the high-strain wafer bending technique.*

V_{DS}. The inverse subthreshold slope is extracted as $\mathrm{SS} = \partial V_{\mathrm{GS}}/\partial \log(I_{\mathrm{DS}})$.

When reducing t_{Si}, on one side a better electrostatic control of the channel allows to reduce SCEs, i.e. DIBL, SS and I_{OFF}, on the other side electron mobility is degraded and therefore the $\mathrm{I_{ON}}$ decreases as well. The device with $t_{\mathrm{Si}} = 10\,\mathrm{nm}$ represents a reasonable compromise between I_{ON} and I_{OFF}.

5.4 Analysis of DG-FETs under ⟨110⟩ uniaxial stress

Mobility curves and mobility enhancement factors are shown in Fig. 5.8 for different strain conditions, where the parameters of the "DG22" device with HfO_2 and TiN are considered. Fig. 5.9 shows the g_{mMAX} and I_{ON} enhancements of "DG22" versus the mobility enhancement extracted from Fig. 5.8 at an effective field of 10^5 V/cm. The transconductance is calculated for $V_{\mathrm{DS}} = 0.05$ V, while I_{ON} is calculated for $V_{\mathrm{GS}} = V_{\mathrm{DS}} = V_{\mathrm{DD}} = 0.85$ V. A linear fit gives a correlation factor of 0.5 and 0.2 for the g_{mMAX} and I_{ON} enhancements, respectively. It is worth noting, however, that the QDD model intrinsically tends to underestimate the strain-induced enhancement, especially at high V_{DS} and (I_{ON}), because of the velocity saturation in short devices (see, e.g., [103]). Some data deduced from published experimental results are also reported in Fig. 5.9 for comparison: the qualitative agreement is satisfactory also taking into account that the experimental data correspond to devices with geometrical parameters different from the "DG22" (i.e., partially- and fully-depleted strained-SOI (PD- FD-sSOI) and strained-Si on SiGe (sSi/SiGe)).

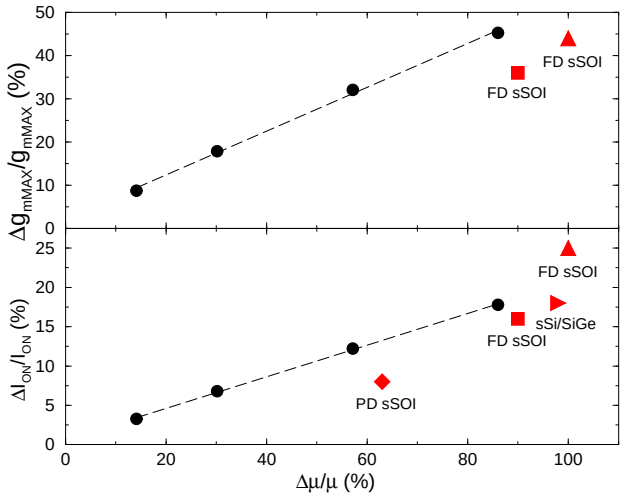

Figure 5.9: *Relative variation of g_{mMAX} and I_{ON} with respect to the mobility enhancement for the "DG22" ($t_{\mathrm{IL}} = 0.7\,nm$, $t_{\mathrm{HfO2}} = 2.9\,nm$, TiN gate) (circles). Dashed lines: linear regression curves with slopes 0.5 (top) and 0.2 (bottom). Other symbols: data extracted from experiments on devices with gate lengths ranging from 25 to 75 nm available in literature ([99], [100], [101] and [102]).*

5.5 Summary

The carrier mobility models presented in the previous chapters have been incorporated into a 1D quantum drift-diffusion (QDD) simulation tool featuring quantum-confinement effects in SG- and DG-SOI FETs in order to investigate the device performance of future technology nodes. Short ($L = 22$ nm) DG-FETs, where mobility is modified by quantum-confinement effects, ultrathin SiO_2/HfO_2 gate stacks and metal gate, have been investigated. Finally, the correlations between the mobility enhancement induced by uniaxial stress in a 22nm DG-FET and the transconductance and on-current have been calculated.

Part II

SILICON NANOWIRES FOR GAS DETECTION

Chapter 6

TCAD analysis of gas sensors based on SiNWs

Nanowire (NW) structure has been demonstrated to be an excellent candidate for chemical sensors because of the enhanced sensitivity that derives mainly from small size and very high surface-to-volume ratio [104]. The presence of a few chemically-active charged molecules on the NW surface can modulate the carrier distribution over their entire cross-sectional conductive pathway through the surface charging induced by chemical reaction, thus operating an electrical transduction of the chemical reaction itself. This can result in an increased sensitivity as compared to traditional CMOS-based sensors. Although such structures can be made with a broad array of materials (metal oxides, such as ZnO [105], In_2O_3 [106], conducting polymers [107] and carbon nanotubes [108]) and a significant progress has been recently made in the use of non-traditional fabrication approaches and new materials [104], silicon-based nanowires (SiNWs) have still received special attention given the sophisticated state of silicon fabrication technology for large scale integration. Silicon-based sensors can be readily integrated with CMOS circuits that can be used for signal processing and analysis, thus providing fast and low-cost detection. Moreover, SiNWs can be manufactured using top-down approach [109] [110] [111], which makes the prospect of sensor arrays realistic and the exposed surface can be also modified to act as both electron transfer mediator and immobilizing matrix for biological or chemical molecules [112]. A challenging issue is the processing of the chemical functionalization which is commonly used to enhance the sensitivity, but is always critical for the sensor performance [113] [114].

In addition, despite the important technological advances in silicon-based nanosensors, their design principles are not still well elaborated, and the path

to further optimization has to be defined. Although SiNWs have been already experimentally demonstrated for high-sensitive detection of gases [115] [116] [117], DNA [118] [119], pH levels and proteins [120], a detailed analysis of the physical mechanisms playing a role in the detection phase is still missing.

In this thesis, the optimization of a SiNW gas sensor for the detection of chemical warfare agents has been investigated. The organo-phosphorus compounds (OPs) represent one of the most important and lethal classes of chemical warfare agents. The ease of manufacturing OPs based on inexpensive starting materials makes these agents a potential weapon for terrorist attacks [121]. Thus, the rapid sensing of these nerve agents has become an increasingly important research goal. The use of chemically-fuctionalized silicon nanoribbons (SiNRs) as OPs detectors has been already demonstrated [114]. In particular, the silicon surface has been grafted with 3-(4-ethynylbenzyl)-1, 5, 7-Trimethyl-3-AzaBIcyclo [3.3.1] Nonane-7-methanOL (TABINOL) and exposed to diphenylchlorophosphate (DPCP), used as a simulant of nerve agents due to its similar structure and chemical reactivity, but much lower toxicity. Highly sensitive and selective detection of OPs has been experimentally obtained. The SiNR sensors operated at sub-ppm level of gas pressure and showed a very fast and marked response.

In a research activity carried out in strict collaboration with the Institute of Information and Communication Technologies, Electronics and Applied Mathematics (ICTEAM), Université Chatolique de Louvain (UCL), Louvain-la-Neuve, Belgium, the Institute of Electronics Microelectronics and Nanotechnology (IEMN), Villeneuve d'Ascq, France, and the CEA-Grenoble, LITEN/DTNM/LCRE, Grenoble, France, arrays of p-doped parallel NWs fabricated on -insulator (SOI) substrate and chemically-functionalized with TABINOL are shown to improve NR-based sensors performance, providing a higher sensitivity to vapors of DPCP. Although it is generally accepted from experimental results that SiNWs with reduced width provide better sensitivity, a detailed physical analysis of the transduction mechanism, and the study of the semiconductor surface and interface properties is still lacking. In this thesis, an extensive TCAD simulation study of the nanosensors has been performed, aimed at a thorough analysis of the physical behavior and at a systematic optimization of the device. An insight on the physical mechanisms involved in the gas detection has been gained and the impact of surface-to-volume ratio on sensor sensitivity has been quantitatively determined showing a strong increase in sensitivity for widths below 50 nm.

In section 6 the details of the fabrication process of the NR/NW sensors are reported, together with the description of the measurement procedures adopted for their electrical characterization. Moreover, the experimental results for NR- and NW-based sensors are described in detail. The analysis of the interface trap formation at the Si/SiO_2 and Si/molecular-layer interfaces of the nanosensors before gas exposure is addressed in sections 6.2 and 6.3, respectively. The chemical

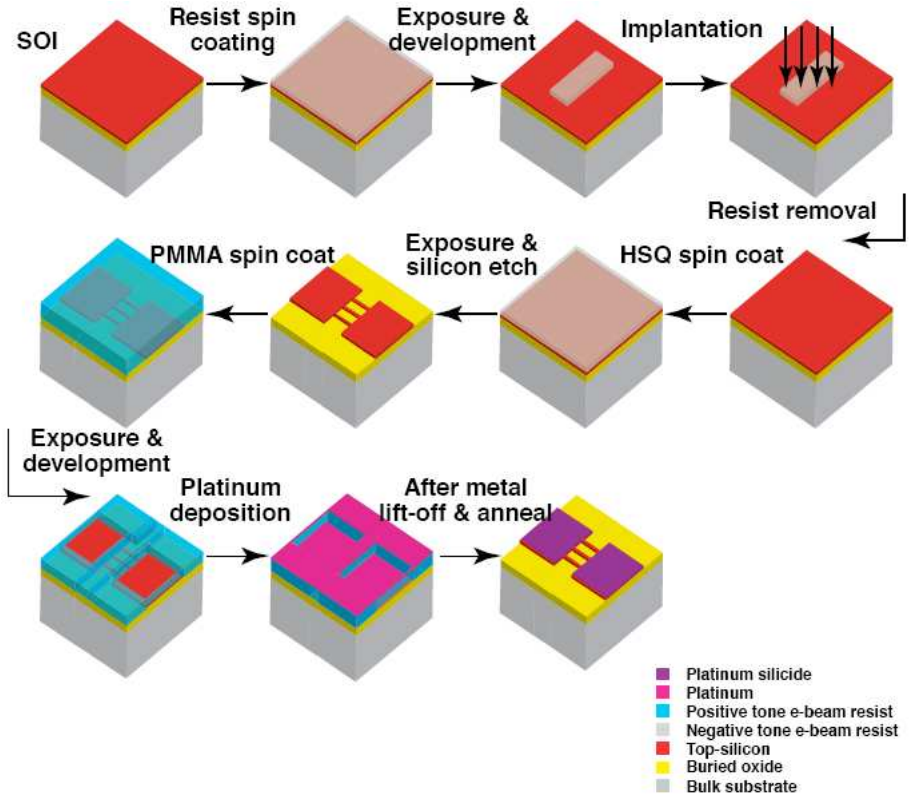

Figure 6.1: *Process steps for top-down fabrication of the SiNWs and SiNRs.*

and physical mechanisms involved in the gas detection phase are pointed out in section 6.4, together with the TCAD analysis of the nanosensors after gas exposure. Finally, the TCAD analysis of the sensor sensitivity and the role played by the NW dimensions are reported in section 6.5. Device fabrication process and sensor characterization The complete process steps are illustrated in Fig. 6.1. The starting material is a p-type silicon-on-insulator (SOI) substrate with top silicon thickness (t_{Si}) of 50 nm, buried oxide thickness (t_{BOX}) of 145 nm and bulk Si substrate thickness of approximately 700 μm. The processing is started by a cleaning step in piranha mixture (sulphuric acid and hydrogen peroxide 1:3) for 10 mins followed by a deionized (DI) water rinse for 10 mins. Then, the substrate is dipped in hydrofluoric acid (HF) of 1% concentration for 20 s to remove the chemical oxide followed by DI water rinse. First, alignment marks are exposed with EL-13% positive tone electron beam resist. After exposure with VISTEC EBPG 5000+ beam writer at 50 keV, the wafer is developed in mixture of propanol (IPA 60 ml) and methylisobutylketone (MIBK 30 ml) for 1 min and then rinsed in IPA for 30 s. After development, the marks are etched with SF6/N2 chemistry to etch the top silicon, CF4/Ar chemistry to etch the buried oxide, followed by SF6/N2 chemistry to etch in the bulk Si substrate. Resist is

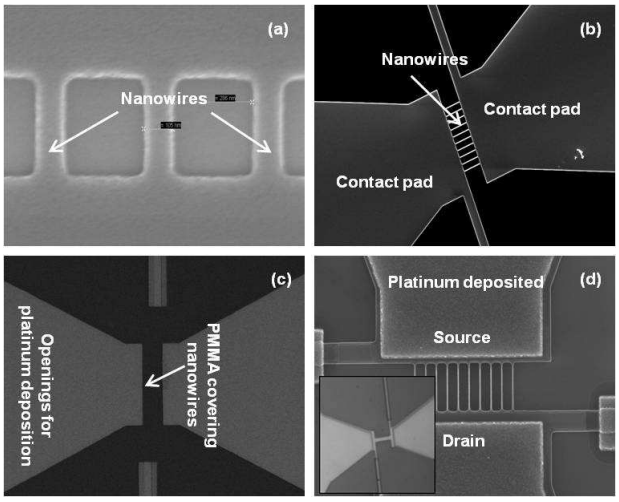

Figure 6.2: *Top-view SEM image of SiNWs (a) after resist development (b) after silicon etching and resist removal (c) after exposure of PMMA to make openings for metal deposition (d) after lift-off of platinum on the source and drain pads.*

removed by exposure under UV light followed by acetone, propanol cleaning and drying by nitrogen. Negative tone electron beam resist hydrogen silsesquioxane (FOx-16/HSQ) is spin coated and exposed. Implantation of source/drain region is done with boron at 20 keV, with a dose of $5{\times}10^{15}$ cm^{-2}. The regions where HSQ is exposed are protected from implantation thanks to the physical barrier provided by the resist. After implantation, resist is removed using HF-1% dip for 2 mins followed by DI water rinse and nitrogen blow drying. Activation of impurities is done by subjecting the wafer to 950° C for 2 mins in nitrogen atmosphere. After standard cleaning using piranha mixture for 10 mins followed by DI rinse, FOx-12 is spin coated on the substrate to give a thickness of 50 nm. The resist is exposed (with proximity corrections included) with the pattern consisting of NWs and contact pads. After development in tetramethylammonium hydroxide (TMAH) 25% for 1 min the wafer is rinsed in DI water (Fig. 6.2a). Then the top-silicon is defined with chlorine based chemistry (Fig. 6.2b). An over etch time of 5 s is considered to assure the complete removal of the top-silicon layer. Ellipsometer measurement is done to measure the buried oxide. The resist is removed by immersing the wafer in HF 1% for 1 min followed by DI water rinse. Then, PMMA 2% 950k is spin coated on the wafer to give a thickness of 200 nm. Exposure of patterns to make openings for the contacts is done (Fig. 6.2c), followed by the development and HF1% to remove native oxide. Platinum is deposited to a thickness of 20 nm. Lift-off is performed by immersing the wafer in acetone together with the use of ultrasonic agitation to avoid sidewall flakes of metal. Back side metal deposition is performed by protecting the front side using a resist. After inspecting the wafer with scanning electron microscope (SEM)

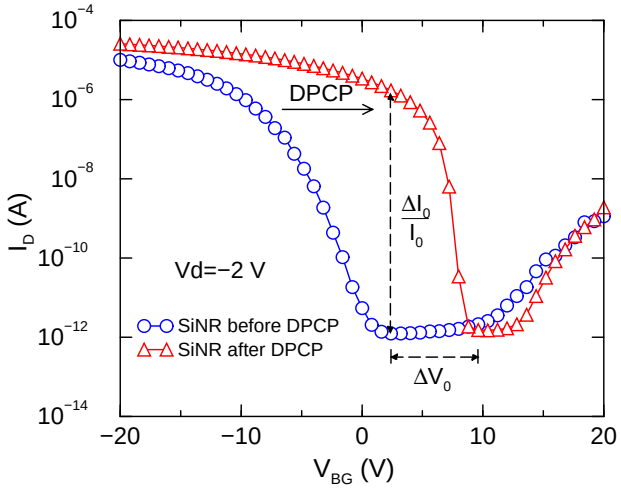

Figure 6.3: *Measured $I_D - V_{BG}$ characteristics of SiNR before and after DPCP exposure for 1 hour.*

(Fig. 6.2d), the front-side resist is removed and the wafer is annealed at 400° C for 2 mins in nitrogen atmosphere. The contacts are of platinum silicide.

One NR resistor (shown as the inset of Fig. 6.2d) has been fabricated with a width W = 1 μm and a length L = 5 μm, while a set of array of 10 parallel NW resistors has been realized with a NW spacing of 0.3 μm, different W (25, 50, 75, and 100 nm) and L (0.3, 0.6, 1.2 and 2.4 μm). Among the available architectures, the NR and the array of NWs with W = 25 nm and L = 0.3 μm have been processed to realize the sensor. The devices have been functionalized via covalent grafting through thermal hydrosilylation of TABINOL onto HF-penetrated substrate in refluxing mesitylene for 2 hours.

The electrical characterization has been carried out with an Agilent 4155C semiconductor parameter analyzer. DC drain current versus back-gate voltage ($I_D - V_{BG}$) characteristics have been measured to check the sensor functionality. The functionalized nanosensors were fully characterized before and after 1 h exposure to DPCP vapors. In a typical experiment, two drops of DPCP were deposited in a 50 mL closed Petri dish to generate a stabilized vapor pressure of DPCP, the chip was then introduced carefully so that it was not in direct contact with the DPCP but only exposed to the vapor for one hour. DPCP vapor pressure was estimated to be in the 500-800 ppb range.

I_D versus time measurement has been also performed. In order to avoid the issues of charge-trapping effects or Joule effect, I_D is acquired in pulsed mode, with $V_{DS} = -2$ V and $V_{BG} = 2$ V pulses maintained for 50 ms to allow the acquisition of I_D, and then followed by a recovery time of 10 s with $V_{DS} = V_{BG} = 0$ V.

Fig. 6.3 shows the measured $I_D - V_{BG}$ characteristics of the NR resistor

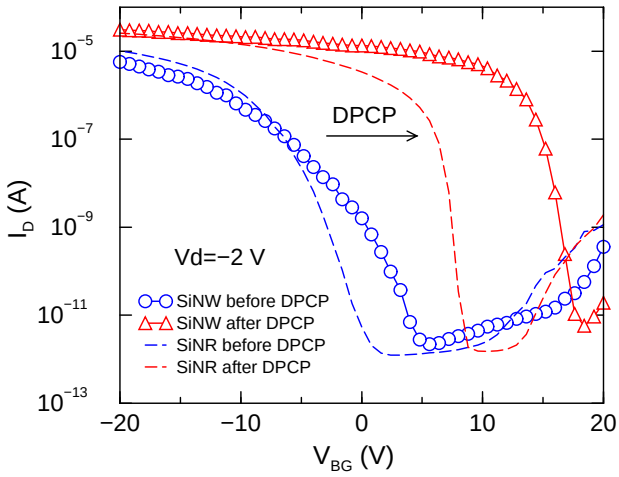

Figure 6.4: *Measured $I_D - V_{BG}$ characteristics of an array of 10 parallel NWs with $W = 25$ nm before and after DPCP exposure for 1 hour.*

before and after DPCP exposure. The device response to vapors of DPCP is very marked. Both an enhancement of the current level and a shift of the trans-characteristics towards more positive V_{BG} values are observed. They can be quantitatively analyzed by extracting I_0/I_0 and ΔV_0, where I_0 and V_0 are the drain current and the back-gate voltage at the minimum current level before exposure (see Fig. 6.3). The NR sensor showed $\Delta I_0/I_0 \approx 1.6 \times 10^6$ and $\Delta V_0 \approx 7$ V, which are in agreement with [114]. The experimental transfer curves before and after DPCP exposure of the NW-based sensors are presented in Fig. 6.4. The turn-on characteristics of the NR-based sensor described above are also shown in dashed lines for comparison. The NW-based device clearly shows both an higher $\Delta I_0/I_0$ and a wider ΔV_0 with respect to the NR after DPCP exposure. In particular, it is $\Delta I_0/I_0 \approx 4 \times 10^6$ and $\Delta V_0 \approx 13$ V.

In Fig. 6.5 the time response of I_D for NWs when vapors of DPCP in the 500-800 ppb concentration range are injected in the measurement chamber. The detection of the gas rapidly changes the current level with a very high amplification factor of more than five orders of magnitude. In about 100 s, a plateau is reached corresponding to the saturation of the chemical reactions.

6.1 Definition of the simulation decks

Numerical simulations of the NW/NR-based devices have been carried out within the framework of the Synopsys simulation tools [26]. Poisson's equation coupled with the drift-diffusion transport model has been solved to obtain the $I_D - V_{BG}$ characteristics. The longitudinal dimensions of the devices are indeed large enough to consider the classical drift-diffusion model sufficiently accurate in de-

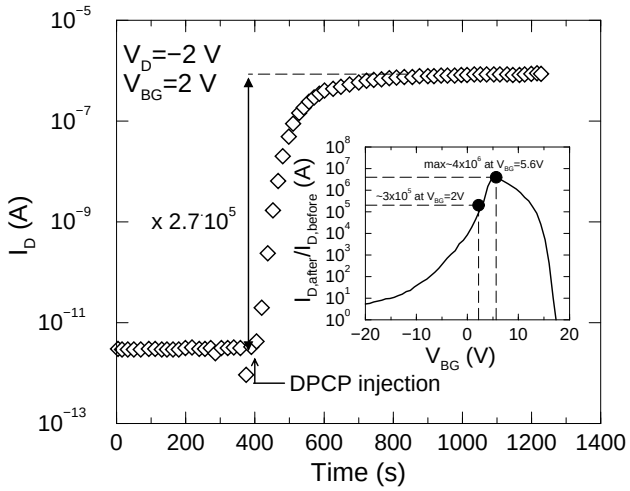

Figure 6.5: *I_D measured in pulsed mode as a function of time. DPCP vapors were introduced at t= 400 s.*

scribing the carrier transport. In addition, the transversal dimensions considered here (greater than 25 nm), are large enough to neglect quantum confinement effects.

The resistors under investigation are intentionally p-doped and with ohmic contacts (source and drain regions are p-doped with a concentration of 6×10^{19} cm^{-3}). The channel doping concentration is a critical parameter in these simulations, since the impact of interface properties (fixed and trapped charges at the interface) on carrier transport is strongly influenced by the doping concentration (especially in depletion and low accumulation regions). Unfortunately, slight variations with respect to the nominal value are expected. In order to provide a doping concentration as realistic as possible to the simulation deck, it has been extracted from the measured resistance of the wire at $V_{DS} \approx 0$ (where the $I_D - V_{DS}$ characteristic is quite linear), and a value of about 4×10^{16} cm^{-3} has been extracted and adopted in the simulation. In Fig. 6.6, the simulation decks for the NR and NW sensors are shown. For the sake of simplicity, it has been assumed that the NR has a translational symmetry along the width, due to its large lateral dimensions. So that a 2D structure can be considered (see Fig. 6.6, left). On the other hand a 3D deck is necessary for the NW sensor, due to its reduced lateral dimensions (the minimum width considered here is 25 nm), to take into account the effects of sidewalls in the simulations. Since the NWs are organized in arrays of 10 parallel wires with spacing of 0.3 μm, a basic cell composed of half wire and half spacing region has been defined and adopted in the simulations (see Fig. 6.6, right). The resulting I_D is then multiplied by 20. In the simulation analysis carried out, the Si/SiO_2 and the Si/molecular layer interfaces are treated separately.

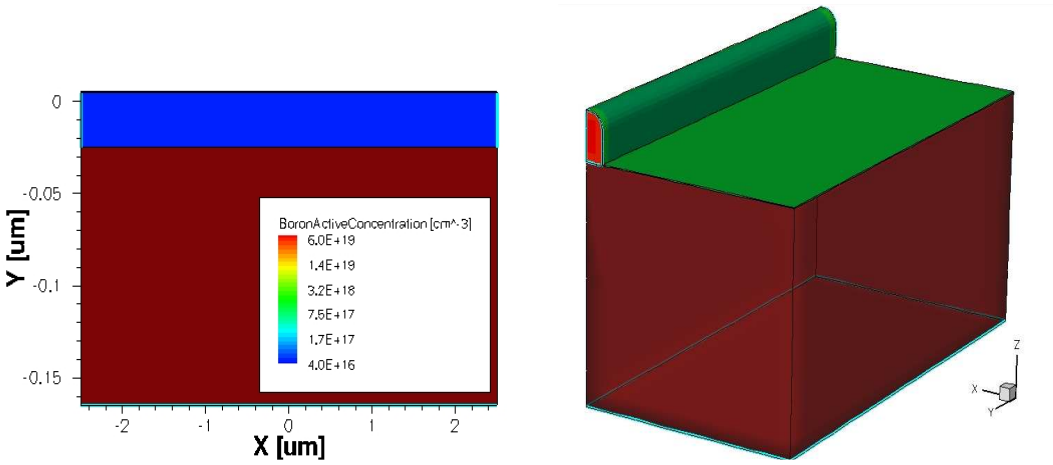

Figure 6.6: *(Left) Two-dimensional and three-dimensional simulation decks for the NR (left) and NW (right) sensors, respectively. The brown region represents the buried oxides and the green one the functionalized molecular layer; Cyan lines delimit the electrodes; the p-type doping concentration is plotted in the silicon regions.*

6.2 Analysis of the Si/SiO_2 trap states in top-down SiNWs

Since the gas detection occurs via modifications of the physical properties of the interface between Si and the molecular layer, it is very important to accurately model the device interfaces in order to perform numerical simulations of the sensor behavior. Consequently, a combined characterization and simulation study is presented to investigate the impact of interface trap states on I_D and to separate the drain current modulation due to the presence of trap states at the Si/BOX interface from the one due to trap states at the Si/molecular layer interface.

Two types of defects dominate the electronic properties of the Si/SiO_2 interface, namely i) the stretched bonds and ii) the silicon dangling bonds with different residual (back) bond configurations. Differently from the sharp energetic levels of defects in bulk silicon, the interface defects show broad energetic distributions. The broadening can be interpreted as due to the statistical disorder in the bond angle and in the distance to the neighbour atoms of the defects themselves [122]. These two kinds of interfacial defects are called intrinsic because they can be treated as eigen-defects of the silicon lattice. Stretched silicon-silicon bonds represent small distortions of the silicon lattice. The related states split from the bands into the gap and show Boltzmann-like distributions (U_T) in the neighbourhood of the band edges (Fig. 6.7). If the distortion becomes larger a bond breaking may be favorable, creating a dangling bond center. The silicon dangling bond center with three silicon back bonds shows a broad double peaked

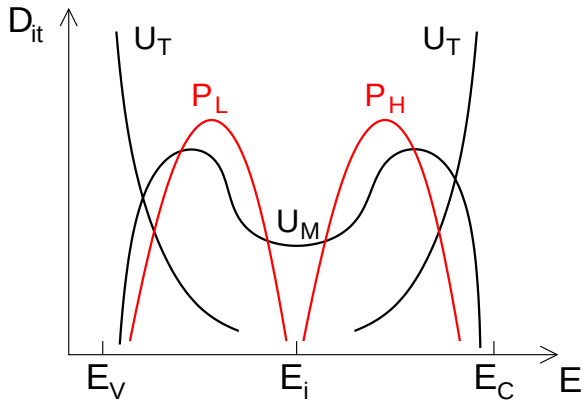

Figure 6.7: *Schematic representation of trap states in the Si bandgap due to defects at the Si/SiO$_2$ interface. Black lines denote intrinsic defects (U_T and U_M), red lines indicate extrinsic defects (P_L and P_H). $E_i = E_g/2$.*

distribution (U_M) modulated over the whole gap with some distance from the band edges, as shown in Fig. 6.7. Two relative peaks can be seen, the first peak lies at E_V + 0.25-0.35 eV and the second at E_V + 0.7-0.85 eV [123], which can be related to the nature of the intrinsic defect itself as explained below. Such defects correspond, to a large extent, to the so-called P_b centers. More specifically, they are denoted as P_{b0} and P_b at the Si(100)/SiO$_2$ and Si(111)/SiO$_2$ interface, respectively. A typical feature of the intrinsic defects is the symmetry of the related distributions in the silicon bandgap caused by their amphoteric character. Each defect gives rise to two corresponding levels: one bonding (donor-like) state in the lower half and one antibonding (acceptor-like) state in the upper half of the bandgap [122]. Acceptor traps are filled with one electron, thus negatively charged, if fully occupied, i.e. if the Fermi level is above the trap level, while they are neutral if unoccupied. On the contrary, donor traps are neutral if occupied, i.e. if the Fermi level is above the trap level, while positively charged (one electron is released) when unoccupied. Unlike doping impurities indeed, donor energy levels are typically located in the lower part of the bandgap and acceptor energy levels are in the upper part of the bandgap [124] [125]. The U-shaped trap distribution, typical for the Si/SiO$_2$ system, is given by the superposition of both intrinsic defect types U_T and U_M.

The extrinsic traps are dangling bond defects with oxygen back bonds and show only donor-like states inside the silicon bandgap. The distributions are broad peaks in the lower (P_L) and upper (P_H) half of the gap, respectively, as shown in Fig. 6.7. The corresponding acceptor-like states are assumed to be inside the silicon conduction band [122].

Due to the complexity of possible defect configurations in a Si/SiO$_2$ interface, a thorough methodology based on theoretical assumptions and experimental re-

sults, which allows for the extraction of the trap configuration and energetic distribution, is needed. To this purpose, the trap distribution at the Si/BOX interface has been extracted by using the Terman apprach [126]. It allows for the extraction of the energy density of the interface trap concentration at the Si/SiO_2 interfaces as illustrated in [127] [128]. The Terman method relies on a high-frequency capacitance-voltage $(C-V)$ measurement at a frequency sufficiently high so that the interface traps are assumed not to respond. By this way, they should not contribute to the $C-V$ characteristics. Although interface traps do not respond to the ac probe frequency, they respond to the slowly varying DC gate voltage and, in this case, cause the high-frequency $C-V$ curve to stretch out along the gate voltage axis as the interface trap occupancy changes with gate bias. In other words, for a MOS capacitance in depletion or inversion additional charge placed on the gate induces additional semiconductor charge Q_{it}, so that the total semiconductor charge results $Q_G = -(Q_b + Q_n + Q_{it})$, where Q_b is the space-charge region bulk charge density and Q_n the electron charge density. The gate voltage results

$$V_G = V_{FB} + \phi_s + V_{\text{ox}} = V_{FB} + \phi_s + Q_G/C_{\text{ox}}\,, \tag{6.1}$$

where V_{FB} is the flat-band voltage and V_{ox} and C_{ox} are the oxide voltage and capacitance, respectively. Therefore it is obvious that for a given surface potential ϕ_s , V_G varies when interface traps are present, leading to the $C-V$ stretch-out. The stretch-out produces a non parallel shift of the $C-V$ curve. Interface traps distributed uniformly through the semiconductor band gap produce a fairly smoothly varying but distorted $C-V$ curve. Interface traps with distinct structure, for example peaked distributions, produce more abrupt distortions in the $C-V$ curve. The energy distribution of trap states can be calculated as

$$D_{it}(E) = \frac{C_{\text{ox}}}{q}\left(\frac{dV_G^{\text{exp}}}{d\phi_s} - \frac{dV_G^{\text{ideal}}}{d\phi_s}\right)\,, \tag{6.2}$$

where V_G^{exp} and V_G^{ideal} refer to the gate voltage obtained by experiments and the ideal one in the absence of traps, respectively. Similarly, $D_{it}(E)$, can be extracted from the difference in derivative in the $I-V$ turn-on characteristics of the device by using the so-called "current-Terman" method [127] as

$$D_{it}(E) = \frac{C_{\text{ox}}}{q}\left(\frac{dV_G^{\text{exp}}}{d\phi_s} - \frac{dV_G^{\text{sim}}}{d\phi_s}\right) = \frac{C_{\text{ox}}}{q}\frac{dI_D}{d\phi_s}\left(\frac{dV_G^{\text{exp}}}{dI_D} - \frac{dV_G^{\text{sim}}}{dI_D}\right) \tag{6.3}$$

where the first term is obtained from the experimental $I-V$ characteristics and the second one is obtained by TCAD device simulations without any trap state. The derivative of I_D with respect to ϕ_s is obtained by the numerical results as well. Moreover, ϕ_s can be directly related to the quasi-Fermi energy in the band gap to obtain $D_{it}(E)$.

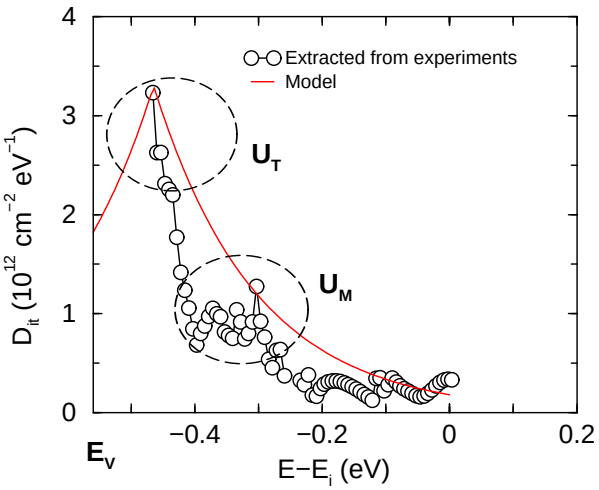

Figure 6.8: *Energy distribution in the bandgap of trap state density at the Si/BOX interface extracted with the current-Terman method (symbols) and used as input of the simulations (red solid line). The signature of intrinsic defects is highlighted.* $E_{\mathrm{i}} = E_g/2$.

The Terman method was one of the first methods for determining the interface trap density and it has been widely criticized in the literature, especially when applied to thin oxides [125]. Moreover, in order to compare experimental with TCAD curves, one needs to accurately describe the doping density local distribution and the device geometry. Despite its questionable accuracy, the method could be useful in our case to extract the trap density at Si/BOX interface of the NR architecture. In fact, the BOX oxide is thick enough and the device structure is simple enough to allow the application of the method with reasonable precision. In addition, the current-Terman method allows to separate the contribution of interface traps at the Si/BOX with that at the Si/molecular layer. Since the surface potential at the Si/molecular layer only slightly varies with V_{BG}, the trapped charge at that interface is almost fixed as well. Therefore, unlike the traps at the Si/BOX interface, the ones at the Si/molecules interface mostly contribute in shifting instead of stretching out the $I_D - V_{BG}$ characteristics and, thus, they do not contribute appreciably to the extracted $D_{it}(E)$.

In Fig. 6.8, $D_{it}(E)$ at the Si/BOX interface is shown, together with the approximated curve adopted in the TCAD simulations (red line). The extracted $D_{it}(E)$ clearly shows the signature of the intrinsic defects: i) a Boltzmann-like distributions ($\mathrm{U_T}$) in the neighbourhood of E_{V} and ii) a broad peak at $\mathrm{E_V}$ + 0.25-0.35 eV ($\mathrm{U_M}$). By applying $V_{BG} < 0$ to p-type devices, the associated band bending makes the Fermi level to scan the lower part of the bandgap. Accordingly, trap density can be extracted from this bandgap region only. Moreover, this implies that acceptor states, which always lie above the mid gap, are not filled

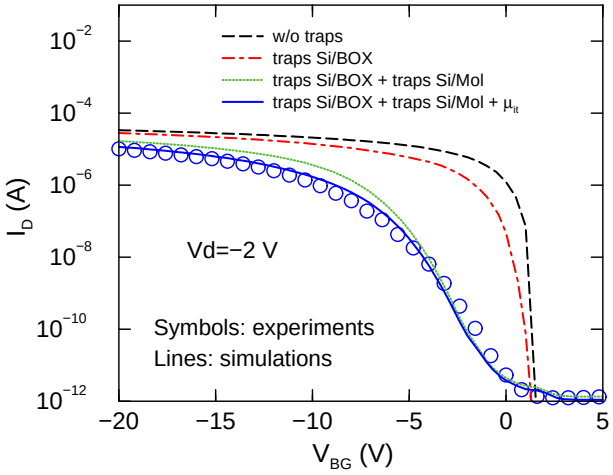

Figure 6.9: *Drain current versus back-gate voltage. Symbols: measurements; lines: simulation results of the ideal case without any trap states (dashed line), considering only traps at the Si/BOX interface (dot-dashed line), with traps both at the Si/BOX and Si/molecular layer interfaces (dotted line) and including the Coulomb scattering contribution due to the interaction with trapped charges (solid line).*

and do not contribute to the current modulation.

The donor-like trap state distribution extracted with the current-Terman method has been modeled with the exponential function

$$D_{it}(E) = 3.3 \times 10^{12} \exp\left(-\left|\frac{(E - E_g/2) + E_1}{E_2}\right|\right) \tag{6.4}$$

with $E_g/2$ the mid gap energy, $E_1 = 0.465$ eV and $E_2 = 0.16$ eV. The model has been used at the Si/BOX interface to simulate the NR device. The TCAD results are reported in Fig. 6.9, showing that the role played by the Si/BOX interface traps is limited to a small modulation of the $I - V$ curve which shows an overall degradation of the current. It is worth pointing out that the mobility degradation due to the coulombic interactions of the interface trapped charges with the carriers in the channel is accounted for consistently. The formulation of the mobility limited by interface charges available in the D-2010.03 release of *Sentaurus Device* [26] has been used in the simulations. In p-type silicon indeed, the Fermi level lies below the mid gap, thus at $V_{BG} = 0$ some positive trapped charges are present at the interface, given by unoccupied donor states. When V_{BG} moves towards negative values the Fermi level shifts down in the band gap near E_V and more donor states are unfilled, resulting in more net positive charge (Fig. 6.10). Therefore, both threshold shift and change in slope of the trans-characteristic are observed. However, the impact of the traps at the Si/BOX interface is not sufficient to reproduce the experimental data. Hence,

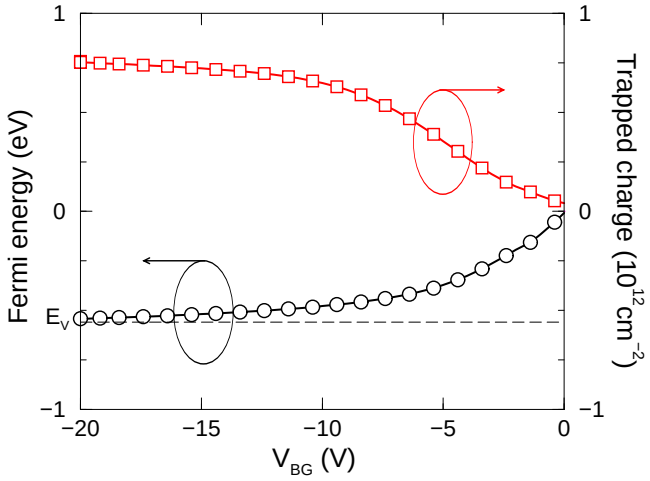

Figure 6.10: *Fermi level at the Si/BOX interface and interface trapped holes as a function of back-gate voltage.*

the remaining gap between the simulated and the experimental curves can be ascribed to the trap states at the Si/molecular layer interface.

6.3 Analysis of the molecular layer interface before exposure

The chemically functionalized organic monolayer can be non uniform and leave some uncovered patches that can react with the air. Also the steric volume of the considered molecule can lead to a partial coverage of the silicon surface. Therefore, it makes sense to consider that the Si/monolayer interface is affected by traps originating from the Si/native SiO_x system. Angermann et al. [129], monitored the evolution of $D_{it}(E)$ curves during the oxidation in air at room temperature on a previously H-terminated surface, by means of a pulsed field-modulated surface photovoltage (SPV) measurements. In order to determine the interface state density $D_{it}(E)$, a varying electric field perpendicular to the surface was applied, which changes the surface potential continuously as a function of the field voltage. Initially, the prepared H-terminated surface is dominated by intrinsic defects, with the characteristic U-shaped distribution, as shown in Fig. 6.11, curve A. An increasing density of these states and additional appearance of extrinsic states P_L was observed after 48 h when the hydrogen coverage decreases (curve B). The occurrence of oxygen backbonded dangling bond defects indicates that the surface is no longer hydrogen-terminated. During further native oxide growth, the P_H group additionally appears (curve C). The superposition of intrinsic and extrinsic states can be approximated with a uniform donor-type D_{it}

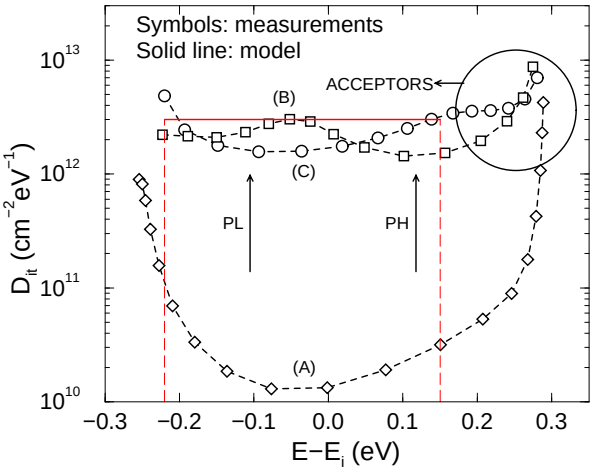

Figure 6.11: *Interface state distribution $D_{it}(E)$. Symbols: measurements from [129] for a H-terminated surface (curve A), after 48 h (curve B) and 21 days (curve C) storage time in air. Red solid line: model adopted for the Si/molecular layer interface.*

level in the bandgap (red solid line) ranging from E_i-0.22 eV to E_i+0.15 eV. On the contrary trap states close to the conduction band edge are acceptors. Fig. 6.9 shows that considering the uniform trap distribution above with $D_{it} = 3 \times 10^{12}$ $cm^{-2}eV^{-1}$, a very good fitting between simulations and experiments is obtained.

6.4 Cooperative effect of molecules on surfaces upon gas exposure

In order to carry out an accurate numerical investigation on gas sensors, the surface transduction mechanism has to be studied in detail and accurately modeled. When TABINOL molecules, grafted on the silicon surface, are exposed to DPCP, aza-adamantane quanternary ammonium salt is formed [114], as shown in Fig. 6.12. It is worth noting that, upon reaction with DPCP, a positive charge is present on the hydrogen atom at a certain distance from the silicon surface, estimated to be of about 0.7-0.8 nm (see blue dots in Fig. 6.13). The modification of the drain current in a molecularly functionalized device can thus be mainly ascribed to many effects, namely: i) a change in the density of silicon surface states [130] [131]; ii) a charge transfer between silicon and molecules, leading to interface dipoles [132]. Since the reaction of DPCP with TABINOL does not change the nature and density of grafting links between TABINOL and silicon, surface states should not be modified during the gas exposure. Therefore, a charge transfer is considered the main effect playing a role [114]. In fact, if

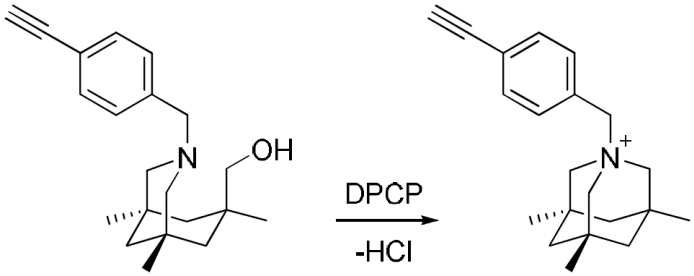

Figure 6.12: *Chemical detection scheme. TABINOL (left) evolves to aza-adamantane quanternary ammonium salt (right) upon exposure to OPs simulant (DPCP). Courtesy of CEA-Grenoble, LITEN/DTNM/LCRE, Grenoble, France.*

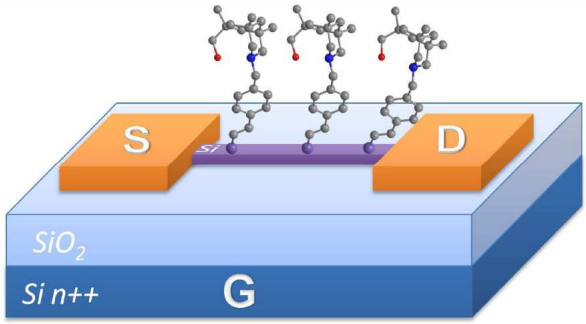

Figure 6.13: *Schematic view of the gas nanosensor with source (S), drain (D) and back-gate (G) contacts. Courtesy of CEA-Grenoble, LITEN/DTNM/LCRE, Grenoble, France.*

the surface molecules are well-oriented and close-packed, cooperative effects can induce a charge redistribution [132]. By assuming the molecular layer as a dipole, with molecules organized parallel to each other and oriented perpendicular to the substrate, the electrostatic potential difference across the dipole layer reads

$$\Delta\Phi = (\mu_\perp \rho)/\epsilon\,, \tag{6.5}$$

where $\mu_\perp$ is the component of the molecular dipole perpendicular to the surface, ρ the surface density of the absorbed molecules and ϵ the dielectric constant. For molecular monolayers $\Delta\Phi$ is typically high enough to induce a very high electric field. In our case, the average molecular density $\rho \approx 2.8{\times}10^{14}$ cm^{-2}, the dielectric constant $\epsilon \approx 2-2.5$ and the thickness of the dipole layer $d \approx 0.7-0.8$ nm [114]. By considering a typical dipole moment $\mu_\perp \approx 1$ Debye (1 Debye $= 3.34{\times}10^{-30}$ C m) [132], the electric field within the molecular layer is $E \approx 7\times10^6$ V/cm. Hence, even with small values of $\mu_\perp$, the potential across a close-packed molecular dipole layer leads to electric fields well exceeding the breakdown value. In such conditions, the molecular layer/substrate system will be induced by the

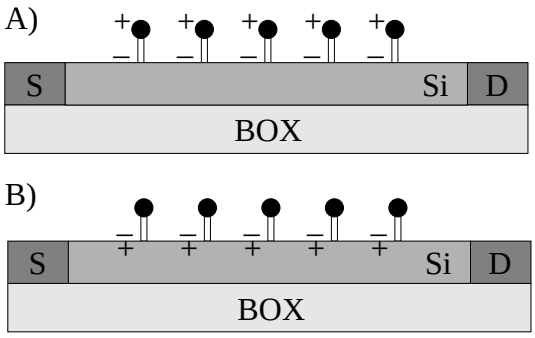

Figure 6.14: *Schematic of the molecularly functionalized silicon device. The molecules are represented as dipoles A) before charge rearrangement and B) after charge rearrangement, which reduces the electric field within the molecular layer.*

high field to a charge redistribution so as to decrease the field, leading to a reduction of $\Delta\Phi$ in equation (6.5). The dipolar property of the molecules can lead to intramolecular charge reorganization, which induces a dipole moment reduction. This mechanism is, however, negligible in organized organic layers made up of molecules with low polarizzability, i.e., low ϵ, as in our case. If such molecules are close-packed in a well-ordered layer, then the energetically most favorable way for reducing the field across the layer is a charge transfer to or from the silicon substrate. This amount of charge usually results in more than 10^{12} electrons or holes per cm^2 [132] [114]. A schematic view of the charge redistribution phenomenon which takes place after gas exposure is shown in Fig. 6.14. The positive charges resulting from the reaction of TABINOL with DPCP cause the formation of negative charges at the interface between the silicon and the molecular layer, which attract holes and modify the silicon surface potential.

In Fig. 6.15, the simulation result is compared with the experimental curve after gas exposure, showing a good agreement. A concentration of 1.93×10^{12} cm^{-2} of transferred electrons has been considered in order to reproduce experiments, in line with values in literature [132] [114]. The coulombic interaction of charge carriers with the fixed negative charge at the interface has been accounted for in the mobility model as well.

6.5 Effect of surface-to-volume ratio on sensitivity

A further investigation has been carried out in order to study the effect of surface-to-volume ratio on sensitivity. To this purpose 3D simulations of NWs with different widths have been performed. The distribution of trap states at the Si/BOX and Si/molecular-layer interfaces and the negative fixed-charge concentration after gas exposure have been fixed to the values extracted against experiments as explained in the previous section. In Fig. 6.16, the sensitivity in terms of

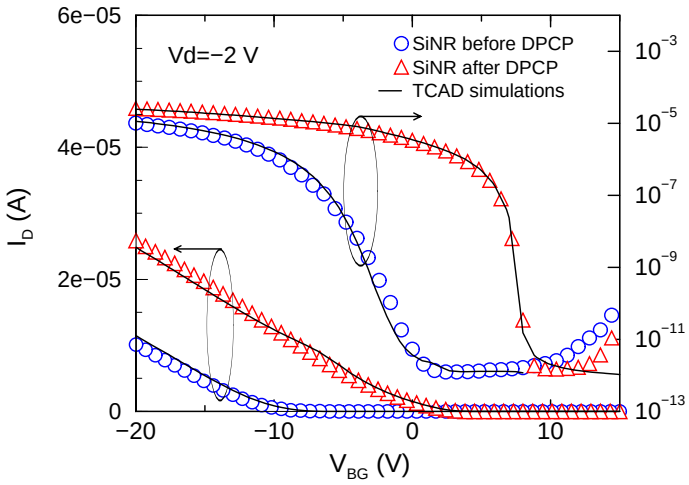

Figure 6.15: *Drain current versus back-gate voltage of the SiNR sensor before and after exposure to DPCP. Simulation results (solid lines) are compared with experimental curves (symbols).*

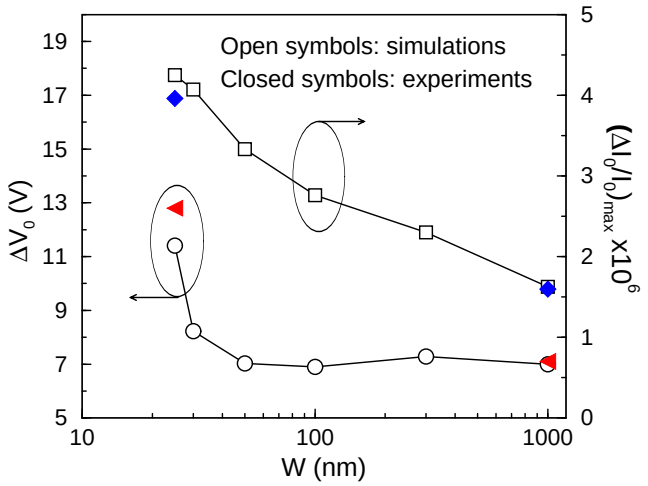

Figure 6.16: *Maximum drain current variation and back-gate voltage shift after DPCP exposure as a function of NW width.*

both the shift of the current curves towards positive V_{BG} (ΔV_0) and the maximum drain current enhancement ($(\Delta I_0/I_0)_{max}$) is shown as a function of the NW width. While in [114] V_0 is defined as the value of V_{BG} corresponding to the minimum current in curves with a marked ambipolarity, here the minumum value of I_D is not always well defined, apart from the experimental curves relative to the array of NWs reported in Fig. 6.4. Therefore V_0 is extracted by imposing $I_{ON}/I_{OFF} = 6 \times 10^6$, where I_{ON} is taken at V_{BG} = -20 V. Although the slight

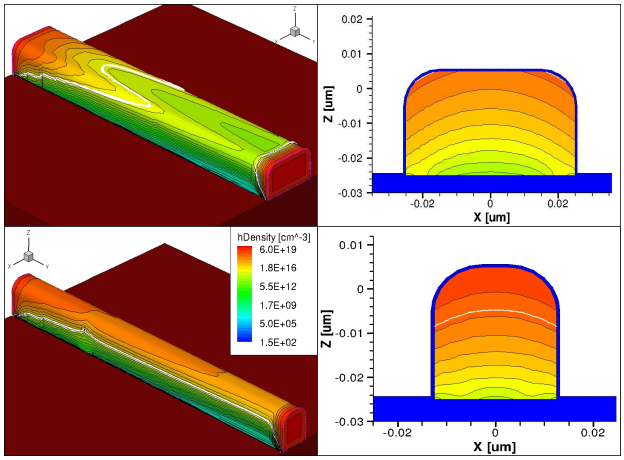

Figure 6.17: *Hole density distribution along with the 3D simulated structure and the device cross-section of the NWs with W = 50 nm (top) and W = 25 nm (bottom) at V_D = -2 V and V_{BG} = 9 V. The while line delimits the depletion region. In the 3D pictures the molecular layer which covers the SiNW is not shown.*

mismatch between simulation and experimental results, likely due to variations of the silicon surface and interface characteristics, Fig. 6.16 clearly shows that the sensor performance can be improved by reducing the NW width, especially when W is shrunk below 50 nm. While $(\Delta I_0/I_0)_{max}$ increases almost linearly when W decreases from 1 μm to 25 nm, ΔV_0 is constant at about 7 V from 1 μm to about 50 nm and exponentially increases when W is below that value. This effect can be ascribed to the impact of negative fixed charges at the NW sidewalls on device electrostatics. In Fig. 6.17 left, the hole density distribution within two NWs of W = 25 and 50 nm is plotted at V_{BG} = 9 V. While wider NW is completely depleted, thus giving no contribution to the transport, the narrower one is still conductive, thanks to the negative charges at the interfaces, which induce a conductive path in the upper half of the wire. The different transport regime is clearly visible in the 2D views of the device cross-sections in Fig. 6.17, right.

6.6 Summary

Extensive TCAD simulation analysis combined with device interface study and characterization have been performed to better understand the physical mechanisms playing a role in the gas detection of SiNW/SiNR sensors. The interaction of carriers with interface trap states and fixed charges is addressed to correctly reproduce experimental responses of recently fabricated gas nanosensors. The impact of surface-to-volume ratio on sensor sensitivity is investigated showing

enhanced performance for narrower wires.

Chapter 7

Conclusions

In this thesis, the development of physically-based mobility models for electrons and holes in ultrathin body SOI FETs have been presented. The resulting models are analytical function of the effective (or local) electric field, substrate doping concentration, silicon thickness, surface orientation and channel direction. The model has been extended to include the effects induced by gate stacks composed of high-κ oxide and metal gate, as well as the impact of mechanical stress on valley splitting, valley repopulation, band warping and scattering rates on (100) and (110) crystallographic orientations. The developed analytical formulations for every single modeled effect have been combined in unified mobility models. They have been demonstrated to correctly account for the simultaneous and complex combination of several effects by correctly predicting experimental mobility in vertical multi-gate FETs with either SiO_2/polysilicon and high-κ/metal gate stacks and different stress configurations, thus proving to be a useful TCAD tool for device optimization of future technology nodes.

Even if based on strong approximations and very far from a rigorous description of the physical phenomena, the developed models are attractive for their capability of keeping tracks of a large number of different physical effects, allowing quantitatively accurate predictions and very low computational costs. However, the development process of such models is non trivial, despite of the resulting simple analytical formulations. Numerical solvers and a wide set of experiments are compulsory to support the analytical model calibration, and not always available. Moreover, it is worth noting that the success in the development of physically-based analytical models is based on a deep study and comprehension of the physical effects and on an accurate choice of the parameters. Despite the importance of these aspects, analytical models are always preferred to add new physical aspects in commercial tools.

Finally, with the growing interest in alternative channel materials, such meth-

ods, mainly applied to the analysis of carrier mobility, could find new important applications.

In the second part of this thesis a TCAD simulation study has been presented, aimed at gaining an insight of the physical mechanisms playing a role in the gas detection of silicon-nanowire sensors. The accurate study and modeling of the effects of trap states and fixed charges generated upon gas exposure at the device interface has allowed to reproduce the experimental trans-characteristics of chemical nanowire sensors fabricated with a tow-down approach. A TCAD analysis has been also carried out to provide guidelines for the optimization of the sensor sensitivity. The sensor performance are shown to monotonically increases with the reduction of device width, especially below 50 nm.

Despite the above important results, further experimental and simulation analysis are needed for the optimization of different aspects. The development of ad-hoc simulation tools is essential to the purpose of investigating nanoscale dimensions of the nanowire cross-section (below 25 nm) with strong geometrical quantum confinement. In addition, an important issue would be the study of the minimum distance between parallel wires in the array of nanowire sensors from a process point of view (limitations given by the functionalization, limitations given by the exposition to gas, and the electrostatic interactions between neighbors). Advanced characterization techniques could be adopted to study the interface properties in bared, functionalized, and nanowires with oxide on top. Finally, in a multidisciplinary framework, the analysis of further chemical grafted molecules could contribute to optimize the chemical-electrical transduction mechanism, providing faster sensing.

Appendices

Appendix *A*

Mobility model coefficients

In the following pages all the parameters of the analytical mobility models presented in this thesis are reported.

Table A.1: Parameters of the electron effective mobility model (Chapter 1)

Parameter	(100)	(110)	(111)	Units
Relative occupancy [Eqs. (1.27) and (1.45)]				
$E_{\mathrm{CE0\,1,2}}$	0.2 0.243	0.237 0.221	0.236 0.236	eV eV
$\chi_{1,2}$	0.622	0.66	0.667	-
χ_3	0.661	0.65	0.667	-
Phonon scattering [Eqs. (1.33) and (1.35)]				
$C_{1,2}$	1.645×10^7	2.04×10^7	1.53×10^7	$\mathrm{cm^3eV^{-1}s^{-3}}$
C_3	2.942×10^7	1.177×10^7	1.53×10^7	$\mathrm{cm^3eV^{-1}s^{-3}}$
$W_{\mathrm{T01,2}}$	5×10^{-11}	1.8×10^{-10}	1.5×10^{-10}	cm
W_{T03}	2×10^{-10}	7×10^{-11}	1.5×10^{-10}	cm
$W_{\mathrm{E01,2}}$	4.9×10^{-7}	3×10^{-7}	3.4×10^{-7}	cm
W_{E03}	2.1×10^{-7}	4.3×10^{-7}	3.4×10^{-7}	cm
$\gamma_{1,2}$	0.17	0.29	0.29	-
γ_3	0.29	0.2	0.29	-
Coulomb scattering [Eqs. (1.39) and (1.40)]				
C_{CS0}	3.2×10^{-5}	9.6×10^{-5}	1.92×10^{-4}	$\mathrm{s^{-1}}$
σ	1.18	0.4	0.45	-
η	0.5	0.33	0.33	-
Surface-roughness [Eq. (1.42)]				
C_{SR0}	5.542×10^{13}	1.724×10^{14}	8.005×10^{13}	$\mathrm{cm^2eV^{-1}s^{-3}}$
δ	2.7	1.5	1	-
Thickness-fluctuation [Eqs. (1.51) and (1.52)]				
$\tau_{\delta t_{Si}l}$(25 K)	8×10^{-3}	-	-	s
$\tau_{\delta t_{Si}h}$(25 K)	0.33	-	-	s
$\tau_{\delta t_{Si}l}$(300 K)	2.6×10^{-2}	2.2×10^{-3}	-	s
$\tau_{\delta t_{Si}h}$(300 K)	0.5	0.025	-	s
$C_{\delta t_{\mathrm{Si}}}$	160	160	-	-
Suppression of inter-valley phonon scattering [Eq. (1.53)]				
f_0	0.278	-	-	-
$\Delta E_{\mathrm{C0_l}}$	125	-	-	meV
$\Delta E_{\mathrm{C0_h}}$	105	-	-	meV
C_l	14	-	-	meV
C_h	50	-	-	meV
Surface-phonons [Eq. (1.56)]				
C_{SP0}	3.617×10^8	4.167×10^7	-	$\mathrm{s^{-1}}$
γ	10	8	-	-
Volume inversion correction [Eq. (1.57)]				
C'_{vi}	-	1.18	-	$\mathrm{cm^2eV^{-1}s^{-3}}$
C''_{vi}	-	5.8	-	-
C'''_{vi}	-	0.4	-	-

Table A.2: Parameters of the electron local mobility model (Chapter 1)

Parameter	(100)	(110)	(111)	Units
Relative occupancy [Eqs. (1.27) and (1.45)]				
$E_{\mathrm{CE0\,1,2}}$	0.2 0.243	0.237 0.221	0.236 0.236	eV eV
$\chi_{1,2}$	0.622	0.66	0.667	-
χ_3	0.661	0.65	0.667	-
Phonon scattering [Eqs. (1.33) and (1.35)]				
$C_{1,2}$	1.556×10^7	2.176×10^7	1.53×10^7	$\mathrm{cm^3eV^{-1}s^{-3}}$
C_3	2.942×10^7	1.177×10^7	1.53×10^7	$\mathrm{cm^3eV^{-1}s^{-3}}$
$W_{\mathrm{T01,2}}$	5×10^{-11}	1.8×10^{-10}	1.5×10^{-10}	cm
W_{T03}	2×10^{-10}	7×10^{-11}	1.5×10^{-10}	cm
$W_{\mathrm{E01,2}}$	4.9×10^{-7}	3×10^{-7}	3.4×10^{-7}	cm
W_{E03}	2.1×10^{-7}	4.3×10^{-7}	3.4×10^{-7}	cm
$\gamma_{1,2}$	0.17	0.29	0.29	-
γ_3	0.29	0.2	0.29	-
Coulomb scattering [Eqs. (1.39) and (1.40)]				
C_{CS0}	3.2×10^{-5}	1.34×10^{-4}	1.92×10^{-4}	$\mathrm{s^{-1}}$
σ	1.18	0.4	0.45	-
η	0.5	0.33	0.33	-
Surface-roughness [Eq. (1.42)]				
C_{SR0}	6.773×10^{13}	3.386×10^{14}	8.005×10^{13}	$\mathrm{cm^2eV^{-1}s^{-3}}$
δ	2.7	2	1	-
Thickness-fluctuation [Eqs. (1.51) and (1.52)]				
$\tau_{\delta t_{Si}l}(25\ \mathrm{K})$	8×10^{-3}	-	-	s
$\tau_{\delta t_{Si}h}(25\ \mathrm{K})$	0.33	-	-	s
$\tau_{\delta t_{Si}l}(300\ \mathrm{K})$	3.4×10^{-2}	2.37×10^{-3}	-	s
$\tau_{\delta t_{Si}h}(300\ \mathrm{K})$	1.053	0.054	-	s
$C_{\delta t_{\mathrm{Si}}}$	160	160	-	-
Suppression of inter-valley phonon scattering [Eq. (1.53)]				
f_0	0.278	-	-	-
$\Delta E_{\mathrm{C0_l}}$	125	-	-	meV
$\Delta E_{\mathrm{C0_h}}$	105	-	-	meV
C_l	14	-	-	meV
C_h	50	-	-	meV
Surface-phonons [Eq. (1.56)]				
C_{SP0}	5.16×10^8	4.167×10^7	-	$\mathrm{s^{-1}}$
γ	10	8	-	-
Volume inversion correction [Eq. (1.57)]				
C'_{vi}	-	1.18	-	$\mathrm{cm^2eV^{-1}s^{-3}}$
C''_{vi}	-	5.8	-	-
C'''_{vi}	-	0.4	-	-

Table A.3: Parameters of the hole effective mobility model (Chapter 2)

Parameter	(100)	(110)	(111)	Units
Acoustic phonon scattering [Eq. (2.8)]				
C_1	2.962×10^7	3.416×10^7	3.03×10^7	$cm^3eV^{-1}s^{-3}$
C_2	1.584×10^7	2.321×10^7	3.03×10^7	$cm^3eV^{-1}s^{-3}$
W_{T01}	1.7×10^{-10}	1×10^{-11}	2×10^{-10}	cm
W_{T02}	2.8×10^{-10}	1.8×10^{-10}	5×10^{-10}	cm
W_{E01}	3.3×10^{-7}	4.8×10^{-7}	3.1×10^{-7}	cm
W_{E02}	3×10^{-7}	1.55×10^{-7}	2.25×10^{-7}	cm
γ_1	0.29	0.17	0.24	-
γ_2	0.29	0.33	0.29	-
Optical phonon scattering [Eq. (2.9)]				
C_{OP}	-	1.242×10^{14}	-	$cm^2eV^{-1}s^{-3}$
Coulomb scattering				
C_{CS0}	2.73×10^{-5}	1.64×10^{-4}	4.64×10^{-4}	s^{-1}
σ	0.844	0.4	0.844	-
η	0.33	0.33	0.33	-
Scattering induced by interface states [Eq. 2.10]				
C_{it_0}	1.1×10^{-4}	6.6×10^{-4}	-	s^{-1}
Surface-roughness				
C_{SR0}	4.43×10^{13}	3.92×10^{14}	6.823×10^{12}	$cm^2eV^{-1}s^{-3}$
δ	1.3	1.5	2	-
Thickness-fluctuation				
$\tau_{\delta t_{Si}l}$(25 K)	1×10^{-5}	-	-	s
$\tau_{\delta t_{Si}h}$(25 K)	0.02	-	-	s
$\tau_{\delta t_{Si}l}$(40 K)	-	3.3×10^{-4}	-	s
$\tau_{\delta t_{Si}h}$(40 K)	-	0.526	-	s
$\tau_{\delta t_{Si}l}$(300 K)	1.3×10^{-4}	4.3×10^{-3}	-	s
$\tau_{\delta t_{Si}h}$(300 K)	0.05	0.132	-	s
η_1	7.6	6	-	s
η_2	0.65	1.5	-	s
$C_{\delta t_{Si}}$	4×10^3	4×10^3	-	-
Suppression of inter-valley phonon scattering [Eq. (2.13)]				
f_0	-	0.38	-	-
ΔE_{V0}	-	97	-	meV
C_{iv}	-	15	-	meV
Surface-phonons				
C_{SP0}	2.94×10^{16}	1.631×10^3	-	s^{-1}
γ	15.6	4.5	-	-

Table A.4: Parameters of the hole local mobility model (Chapter 2)

Parameter	(100)	(110)	(111)	Units
Acoustic phonon scattering [Eq. (2.8)]				
C_1	3.789×10^7	3.416×10^7	3.03×10^7	$cm^3eV^{-1}s^{-3}$
C_2	1.235×10^7	1.934×10^7	3.03×10^7	$cm^3eV^{-1}s^{-3}$
W_{T01}	1.7×10^{-10}	1×10^{-11}	2×10^{-10}	cm
W_{T02}	2.8×10^{-10}	1.8×10^{-10}	5×10^{-10}	cm
W_{E01}	3.3×10^{-7}	4.8×10^{-7}	3.1×10^{-7}	cm
W_{E02}	3×10^{-7}	1.55×10^{-7}	2.25×10^{-7}	cm
γ_1	0.29	0.17	0.24	-
γ_2	0.29	0.33	0.29	-
Optical phonon scattering [Eq. (2.9)]				
C_{OP}	-	1.242×10^{14}	-	$cm^2eV^{-1}s^{-3}$
Coulomb scattering				
C_{CS0}	2.73×10^{-5}	1.64×10^{-4}	4.64×10^{-4}	s^{-1}
σ	0.844	0.4	0.844	-
η	0.33	0.33	0.33	-
Scattering induced by interface states [Eq. 2.10]				
C_{it_0}	1.1×10^{-4}	6.6×10^{-4}	-	s^{-1}
Surface-roughness				
C_{SR0}	6.81×10^{13}	4.26×10^{14}	6.823×10^{12}	$cm^2eV^{-1}s^{-3}$
δ	1.5	1.5	2	-
Thickness-fluctuation				
$\tau_{\delta t_{Si}l}$(25 K)	1×10^{-5}	-	-	s
$\tau_{\delta t_{Si}h}$(25 K)	0.02	-	-	s
$\tau_{\delta t_{Si}l}$(40 K)	-	3.3×10^{-4}	-	s
$\tau_{\delta t_{Si}h}$(40 K)	-	0.526	-	s
$\tau_{\delta t_{Si}l}$(300 K)	1.9×10^{-4}	3.73×10^{-3}	-	s
$\tau_{\delta t_{Si}h}$(300 K)	0.15	0.111	-	s
η_1	7.6	6	-	s
η_2	0.65	1.5	-	s
$C_{\delta t_{Si}}$	4×10^3	4×10^3	-	-
Suppression of inter-valley phonon scattering [Eq. (2.13)]				
f_0	-	0.494	-	-
ΔE_{V0}	-	97	-	meV
C_{iv}	-	15	-	meV
Surface-phonons				
C_{SP0}	2.94×10^{16}	1.435×10^3	-	s^{-1}
γ	15.6	4.5	-	-

Table A.5: Parameters of the remote scattering terms (Chapter 3)

ELECTRONS

Remote phonon scattering [Eq. (3.1)]

Parameter	SiO_2/PolySi	metal gate (TiN)	high-κ (HfO_2)	Units
C_{RPS}	2.686×10^7	4.626×10^6	4.865×10^6	$\mathrm{cm^3eV^{-1}s^{-3}}$
k_{RPS}	1.94×10^7	0.68×10^7	0.69×10^7	$\mathrm{cm^{-1}}$

Remote surface-roughness scattering [Eq. (3.2)]

C_{RSS}	6.658×10^{13}	-	-	$\mathrm{cm^2eV^{-1}s^{-3}}$
k_{RSS}	1.2×10^7	-	-	$\mathrm{cm^{-1}}$

Remote Coulomb scattering [Eq. (3.3)]

C_{RCS}	5.654×10^{-4}	5.56×10^{-3}	1.645×10^{-2}	$\mathrm{s^{-1}}$
k_{RCS}	2.7×10^6	1.88×10^7	1.9×10^7	$\mathrm{cm^{-1}}$

HOLES

Remote phonon scattering [Eq. (3.1)]

Parameter	SiO_2/PolySi	metal gate (TiN)	high-κ (HfO_2)	Units
C_{RPS}	-	-	5.661×10^7	$\mathrm{cm^3eV^{-1}s^{-3}}$
k_{RPS}	-	-	2.37×10^7	$\mathrm{cm^{-1}}$

Remote surface-roughness scattering [Eq. (3.2)]

C_{RSS}	-	-	-	$\mathrm{cm^2eV^{-1}s^{-3}}$
k_{RSS}	-	-	-	$\mathrm{cm^{-1}}$

Remote Coulomb scattering [Eq. (3.3)]

C_{RCS}	-	-	3.159×10^{-4}	$\mathrm{s^{-1}}$
k_{RCS}	-	-	2.2×10^7	$\mathrm{cm^{-1}}$

Table A.6: Parameters of the strain model (Chapter 4)

Parameters of the hole density-of-states effective masses Eq. [4.6]

Parameter	LH ($i = 1$)	HH ($i = 2$)
$b_{v,1}$	-36.65	-78.53
$b_{v,2}$	1.816×10^3	2.056×10^3
$b_{v,3}$	-2.153×10^4	0

Parameters of the hole principal effective masses Eq. [(4.15)]

Parameter	$\varepsilon_{xy} > 0$	$\varepsilon_{xy} < 0$
$c_{2,1}$	88.26	48.54
$c_{2,2}$	1948	1363.6
$d_{2,1}$	-17.652	52.956
$d_{2,2}$	194.8	1363.6

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Curriculum Vitae

Luca Silvestri was born in Pescara, Italy, on December 15, 1981. He received his Bachelor and Master Degree (with honors) in Electronic Engineering in 2004 and 2007, respectively. Since May 2007, he has been with the ARCES research center, University of Bologna, Bologna, starting the European Ph.D. program in Information Technology in January 2008. From October 2009 to July 2010, he has been a Visiting Researcher with the Institute of Information and Communication Technologies, Electronics and Applied Mathematics (ICTEAM), Université Catholique de Louvain (UCL), Louvain-la-Neuve, Belgium. He is currently working with the ARCES device modeling and simulation group.

List of Publications

Journal Publications

1) V. Passi, F. Ravaux, E. Dubois, S. Clavaguera, A. Carella, C. Celle, J.-P. Simonato, L. Silvestri, S. Reggiani, J.-P. Raskin, D. Vuillaume, "High Gain and Fast Detection of Warfare Agent using Back-Gated Silicon Nanowires MOSFETs", submitted to IEEE Electron Device Letters.

2) L. Silvestri, S. Reggiani, E. Gnani, A. Gnudi, G. Baccarani, "A Low-Field Mobility Model for Bulk and Ultrathin Body SOI p-MOSFETs with Different Surface and Channel Orientations", IEEE Trans. Electron Devices, Vol. 57, No. 12, pp. 3287-3294, 2010.

3) L. Silvestri, S. Reggiani, E. Gnani, A. Gnudi, G. Baccarani, "A Low-Field Mobility Model for Bulk, Ultrathin Body SOI and Double-Gate n-MOSFETs with Different Surface and Channel Orientations. Part I: Fundamental Principles", IEEE Trans. Electron Devices, Vol. 57, No. 7, pp. 1567-1574, 2010.

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5) P. Palestri, C. Alexander, A. Asenov, V. Aubry-Fortuna, G. Baccarani, A. Bournel, M. Braccioli, B. Cheng, P. Dollfus, A. Esposito, D. Esseni, C. Fenouillet, C. Fiegna, G. Fiori, A. Ghetti, G. Iannaccone, A. Martinez, B. Majkusiak, S. Monfray, V. Peikert, S. Reggiani, C. Riddet, J. Saint-Martin, E. Sangiorgi, A. Schenk, L. Selmi, L. Silvestri, P. Toniutti, J. Walczak, "A Comparison of Advanced Transport Models for the Computation of the Drain Current in Nanoscale nMOSFETs", Solid-State Electronics, Vol. 53, pp. 1293-1302, 2009.

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1) L. Silvestri, S. Reggiani, A. Gnudi, E. Gnani, G. Baccarani, "Mobility Model for Electrons and Holes in FinFETs with High-κ Stacks, Metal Gate and Stress", in Proc. of the 11th International Conference on Ultimate Integration of Silicon (ULIS), pp. 73-76, March 2010, Glasgow, UK.

2) P. Palestri, C. Alexander, A. Asenov, V. Aubry-Fortuna, G. Baccarani, A. Bournel, M. Braccioli, B. Cheng, P. Dollfus, A. Esposito, D. Esseni, C. Fenouillet, C. Fiegna, G. Fiori, A. Ghetti, G. Iannaccone, A. Martinez, B. Majkusiak, S. Monfray, V. Peikert, S. Reggiani, C. Riddet, J. Saint-Martin, E. Sangiorgi, A. Schenk, L. Selmi, L. Silvestri, P. Toniutti, J. Walczak, "Comparison of Advanced Transport Models for Nanoscale nMOSFETs", in Proc. of the 10th International Conference on Ultimate Integration of Silicon (ULIS), pp. 125-128, March 2009, Aachen, DE.

3) L. Silvestri, S. Reggiani, E. Gnani, A. Gnudi, M. Rudan, G. Baccarani, "Effects of Channel Orientations, High-κ Gate Stacks and Stress on UTB-FETs: A QDD Simulation Study", in Proc. of the IEEE International Workshop on Design and Test of Nano Devices, Circuit and Systems (NDCS), pp. 7-10, October 2008, Boston MA.

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