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**A HYBRID TECHNOLOGY FOR PARALLEL  
RECORDING OF SINGLE ION CHANNELS**

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## **A hybrid technology for parallel recording of single ion channels**

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# Preface

This PhD thesis will describe the work spent from January 2008 to December 2010 at the Advanced Research Center on Electronic Systems (ARCES) into the research team lead by Prof. Marco Tartagni in the Second School of Engineering of the University of Bologna, Cesena Campus. The research activity is aimed at investigating the role of hybrid technologies into high performance nanosensor acquisition platforms and at evaluating their performance.

The work started from the background of the Receptronics project founded by the Sixth European Framework Program. The aim was the develop of compact and low-cost molecular sensors for quantifying target molecule concentrations using a biomorphic approach where sensing elements made of chimeric ligand-gated ion channels are strictly interfaced to advanced microelectronic systems. This thesis focuses some of the results gained within this project to develop a fully parallel single ion-channel acquisition platform for high throughput screening (HTS).

The results of this thesis highly benefitted by several months spent in public and private institutions for evaluating the platform, more specifically: University of Southampton (UK), Ionovation GmbH (DE), Nanlon GmbH (DE) and HEKA Technologies GmbH (DE).



# Abstract

Hybrid technologies, thanks to the convergence of integrated microelectronic devices and new class of microfluidic structures could open new perspectives to the way how nanoscale events are discovered, monitored and controlled. The key point of this thesis is to evaluate the impact of such an approach into applications of ion-channel High Throughput Screening (HTS) platforms. This approach offers promising opportunities for the development of new classes of sensitive, reliable and cheap sensors. There are numerous advantages of embedding microelectronic readout structures strictly coupled to sensing elements. On the one hand the signal-to-noise-ratio is increased as a result of scaling. On the other, the readout miniaturization allows organization of sensors into arrays, increasing the capability of the platform in terms of number of acquired data, as required in the HTS approach, to improve sensing accuracy and reliability. However, accurate interface design is required to establish efficient communication between ionic-based and electronic-based signals.

The work made in this thesis will show a first example of a complete parallel readout system with single ion channel resolution, using a compact and scalable hybrid architecture suitable to be interfaced to large array of sensors, ensuring simultaneous signal recording and smart control of the signal-to-noise ratio and bandwidth trade off. More specifically, an array of microfluidic polymer structures, hosting artificial lipid bilayers blocks where single ion channel pores are embedded, is coupled with an array of ultra-low noise current amplifiers for signal amplification and data processing. As demonstrating working example, the platform was used to acquire ultra small currents derived by single non-covalent molecular binding between  $\alpha$ -hemolysin pores and  $\beta$ -cyclodextrin molecules in artificial lipid membranes.

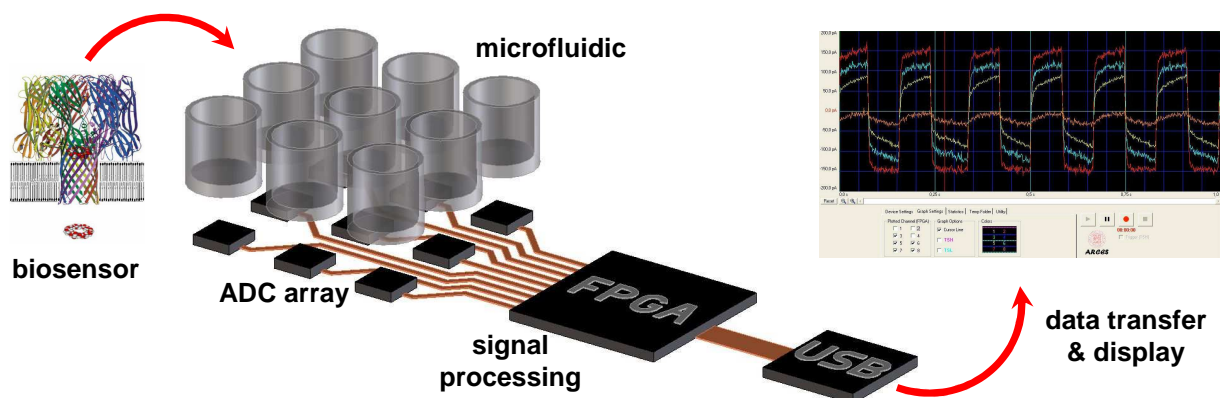


Fig. 1 – Hybrid technology concept. Single ion-channels are embedded into artificial lipid membranes (BLMs) that are self assembled in microfluidic structures strictly coupled to microelectronic systems for signal amplification and data processing.





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# Introduction

This work will present the system design of a multichannel acquisition platform for acquiring signals generated by an array of single ion channels. A key contribute of this work over the state of the art in this field is to demonstrate how a structured design based on an array approach will be fully functional with very high performance. The proposed architecture is fully scalable and flexible, offering high data throughput as demanded by HTS requirements.

The thesis is organized in five chapters. The Chapter 1 is an overview on the biochemistry concepts about ion channels, their behaviour in the natural biology environment and the possibility that they offer to be used as stochastic sensors. A brief review about the state of the art in electrophysiology apparatus en experimental methodologies, as well as the patch clamp techniques used in biochemistry labs is also presented in this chapter. Chapter 2 briefly explains the theory behind Delta Sigma converters and their role in sensing processes, to reduce noise in acquisition processes. Furthermore, design process for Application Specific Integrated Circuit (ASIC) is illustrated, from the electronic and layout design to the foundry fabrication process, as well as the characterization and the evaluation of the final prototypes.

Chapter 3 presents the evolution of the digital data elaboration and visualization architecture, through the development of digital architecture for a multiple and concurrent channels acquisition systems. More specifically, Digital Signal Processing (DSP) issues are treated to elaborate simultaneously different data channels using a Field Programmable Gate Array (FPGA). The development of a Graphical User Interface (GUI) is presented together with a software interface designed to be platform independent to reach the best performances among the datapath to a host PC.

Chapter 4 presents the overall platform for multiple ion channel acquisition system by introducing the hybrid technology approach where microfluidic devices are electronically interfaced to an acquisition system in a stand-alone platform, including all the controls for experimental diagnostics, data display and storage.

Finally, Chapter 5 illustrates the capabilities of the acquiring platform, presenting examples for industry application and futures prospective on the market.

This work is an example of highly interdisciplinary project, where different skills are used to evaluate and solve problems related to different fields, from the microelectronic design to the electrochemistry interfaces, as well as the evaluation of the computational performances offered by digital elaboration architectures and microfluidic and packaging design issues.

An important issue should be pointed out. The platform is the result of a team where different people worked together to reach a common target, offering their expertise into different aspects. The following flowchart is an effort representation of my work within this project.

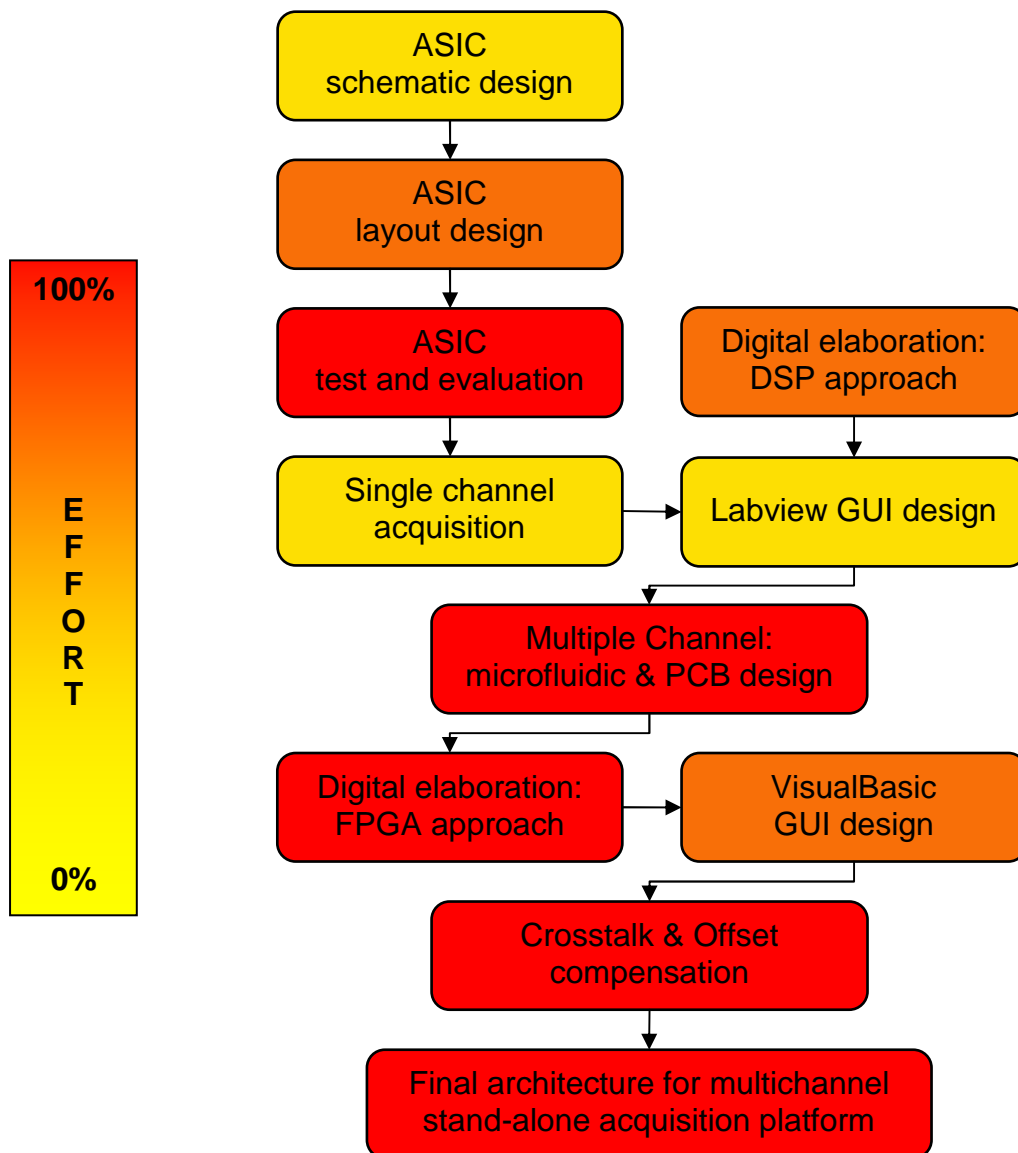


Fig. 2 – Effort flowchart for hybrid technology acquiring platform development.

# Chapter 1

## Ion channel for High Throughput Screening

### Introduction

Ion channels are proteins present in the membrane that surround all the biological cells and intracellular organelles (nucleus, mitochondria, endoplasmic reticulum and so on) of living systems [Hille01] (Fig. 3). They are involved in a wide variety of fundamental physiological processes that include rapid changes in cells such as cardiac, skeletal, and smooth muscle contraction, epithelial transport of nutrients and ions, T-cell activation and pancreatic beta-cell insulin release [Camerino07] [Verkman09] [Tricarico08] by regulation and selective transport of ions across the membrane cells.

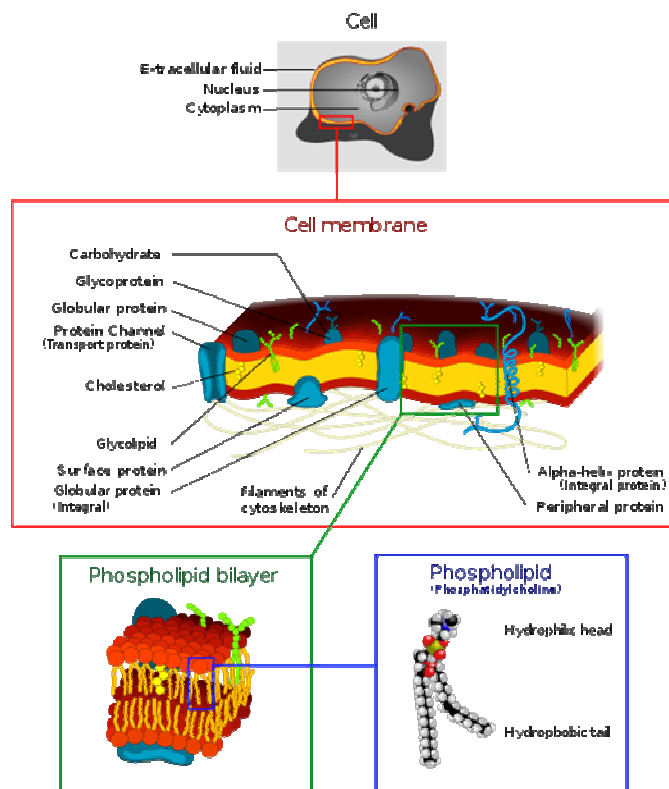
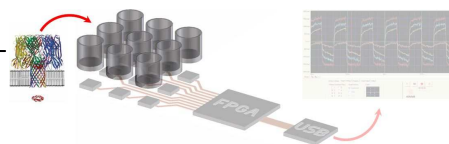


Fig. 3 – Ion channel environment: nanopores formed by proteins that span the cell membrane are involved in a wide variety of physiological cell process, allowing the ions flow across the cell membrane constituted by a phospholipid bilayer [web1].



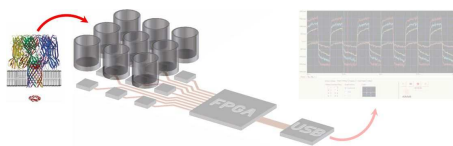
The importance of ion channels is underlined by their involvement in a wide range of pathologies, spanning all major therapeutic areas [Ashcroft06] [Clare10]: their critical biological roles means that they become a major class of drug targets [Tab. 1]. The pharmacological modulation of ion channel function enables the subtle correction of their dysfunction, being involved in many diseases and disorders particularly in the nervous, gastrointestinal and cardiovascular system. Another aspect of ion channel drug development is the safety liability issues of the developed drug candidates (e.g. acquired QT interval prolongation), which is why the FDA and other regulatory entities require safety testing, for example on hERG for all new chemical entities [Fertig08] [Redfern03].

Drug	Commercial Name	Target Channel	Disease Indication
Verapamil	Verelan	L-type CaV	Angina, hypertension, arrhythmia
Diltiazem	Cardizem	L-type CaV	Angina, hypertension, arrhythmia
Amlodipine	Norvasc	L-type CaV	Angina, hypertension, arrhythmia
Nimodipine	Nimotop	L-type CaV	Angina, hypertension, arrhythmia
Nifedipine	Procardia	L-type CaV	Angina, hypertension, arrhythmia
Sotalol	Beta pace	hERG	Arrhythmia
Amiodarone	Cordarone	hERG	Arrhythmia
Flecainide	Tambocor	NaV1.5	Arrhythmia
Gabapentin	Neurontin	CaV $\alpha_2\delta$	Pain
Ziconitide	Prialt	CaV2.2	Severe chronic pain
Lidocaine	Lidocaine	NaV	Local anesthesia
Phenytoin	Dilantin	Brain NaV	Epilepsy
Carbamazepine	Tegretol	Brain NaV	Epilepsy
Lamotrigine	Lamictal	Brain NaV	Epilepsy, bipolar disorder
Topiramate	Topamax	Brain NaV	Epilepsy
Flupirtine	Flupirtine	KCNQ2/3	Epilepsy
Benzodiazepine	Diazepam	GABA	Depression
Glibenclamide	Glimepiride	$K^{ATP}$	Diabetes
Lubiprostone	Amitiza	CLC2	Constipation

Tab. 1 – Actual Ion Channel drugs [Hopkins06].

About 13.4% of known drugs have their primary therapeutic effect on ion channels. Worldwide sales of ion channel drugs are estimated to be in excess of \$12 billion [Clare10] [Hopkins06]. Nonetheless, despite being such a rich source of targets and notwithstanding much attention from the pharmaceutical industry, ion channels have proved to be particularly

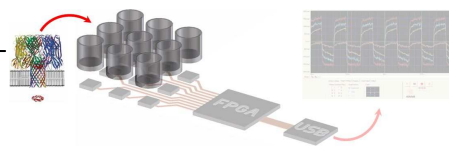




resistant to high-throughput, molecular-targeted approaches for drug discovery [Clare10]. Almost all of the current ion channel drugs were discovered using traditional tissue or animal-based pharmacological methods, in many cases without any knowledge of their molecular target [Clare10]. Ion channels present challenges for molecular drug discovery and recent technical developments that have increased their tractability should improve the prospects for developing better therapeutic ion channel modulators [Clare10]. The huge functional and structural diversity of ion channels presents major logistical and technical challenges for molecular drug discovery [Clare06]. High Throughput Screening (HTS) of large chemical libraries generally requires cloning of the target protein which must be abundantly expressed in a heterologous system (normally a stable cell line) in a form that closely resembles its native correlates [Clare10]. For ion channels this is problematic since authentic reproduction of native functional and pharmacological properties is dependent on efficient expression, localization, and orientation of an appropriate combination of subunits, each of which may have multiple transmembrane domains that fold in and out of the membrane [Clare10]. As a consequence there is enormous potential for misfolding and mis-assembly when ion channels are over-expressed [Clare10]. Even if cloning and expression is successful, the development of robust, biologically relevant assays with sufficient capacity for high throughput screening can be very challenging [Clare10].

The patch clamp technique [NehSak92] is the state-of-the-art technique for the ion channels study, it offers the temporal resolution needed for measuring the ultra-rapid kinetics of ion channels (which can open and close within just a few milliseconds) and is also exquisitely sensitive, being capable of measuring currents as low as 10 pA, but it is very low throughput and a laborious process that require a skilled and highly trained scientist [Fertig08].

Within the last ten years, various assay formats have been developed for high throughput screening (HTS) of ion channels. High throughput screening is a method of drug discovery that involves a brute force approach where tens of thousands of compounds are tested against a particular target daily. Compound libraries can have millions of compounds, selected for drug-like characteristics such as solubility, partition coefficient (logP), molecular weight, and number of hydrogen bond donors/acceptors [web2]. Generally, high throughput screening involves modern robotics, sophisticated control software, advanced liquid handling, and sensitive detection methods. Although lacking the precision, temporal resolution, and voltage control of electrophysiology, the associated costs, throughput, and speed of these approaches make them suitable for screening sizeable compound libraries that are now typical throughout the pharmaceutical industry. These approaches are summarized in Tab. 2.



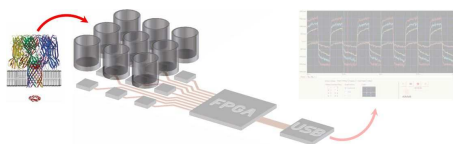
Assay format	Throughput	Functional relevance	Advantages	Disadvantages
Ligand binding	H	L-M	Simple well-established format, low cost, measures direct interactions	May not correlate to functional effects, limited to single binding site interactions and by availability, relevance of ligand,
Voltage sensitive dyes	H	M	Well established, low cost, functional format	Non-physiological activation of voltage-gated channels, indirect read-out (e.g., endogenous channels/mechanisms contribute) non-linear response, compound interference, false +ves.
Fluorophore binding dyes	H	M	Well established, low cost, functional format	Non-physiological activation of voltage-gated channels, indirect read-out (e.g., endogenous channels/mechanisms can contribute), compound interference, false +ves.
Ion flux	M	M	Functional format, direct read-out	Non-physiological activation of voltage-gated channels, non-kinetic read-out, and surrogate ions can alter channel properties and shift potencies.
Automated electrophysiology	M	H	Information-rich (e.g., measures state-dependence), good precision and fidelity	High cost, hydrophobic compounds can be problematic.
Manual electrophysiology	L	H	Gold standard, high precision and fidelity	Labor intensive, technically demanding, high cost

**Note:** H, high; M, medium; L, low.

Tab. 2 – Comparison of ion channel screening formats [Clare 10].

High throughput assays can be classified as either functional or nonfunctional. Functional assays measure the activity of a compound in modifying the actual function of a target protein (eg, ion currents through hERG channels). Nonfunctional assays often simply measure binding of a compound to the target protein or use some indirect measure of target activity [web2]. Examples of nonfunctional assays include tritiated binding assays, the measure of fluorescence activity associated with calcium signaling, or techniques such as fluorescence resonance energy transfer (FRET). Functional assays are preferred since they are less prone to false positive hits. High throughput assays refer to assays that allow the screening of between 10,000 and 100,000 compounds per day. Ultra-high throughput assays refer to assays that allow the screening of over 100,000 compounds per day.

Ion channel activity can also be monitored using indirect methods, which offer a throughput compatible with HTS. Current systems for primary drug screening using cellular assays are mostly based on fluorescence, affinity binding or radioactive flux assays. Most of these methods have low temporal resolution (in the range of seconds to minutes, as compared to submilliseconds for patch clamp), often require extensive assay development and are known for their high false-negative and false-positive rates. Some of them are not applicable to all ion channel types because the readout is coupled to a specific ion species, for example, calcium-sensitive dyes, or rubidium efflux assays, which also require the use of radioactive compounds. Ion channels activated by a change in transmembrane voltage sometimes offer a challenge to



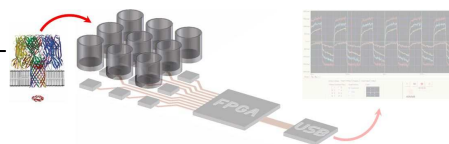
investigate, owing to the lack of voltage control of the cellular membranes. On the positive side, these methods allow for the screening of 100,000s of compounds in limited time frames. Tab. 3 summarizes the strengths and drawbacks of the most commonly used HTS techniques. Detailed analysis and discussion of high-throughput ion channel screening methods can be found in several recent reviews [Fertig08] [Molokanova08] [Treherne06] [Terstappen04].

Method	Information content	Throughput	Costs	Sensitivity	Temporal resolution	Comments
Automated patch clamp	High	Low to medium	High	High	Submillisecond	High data density with increased throughput
Manual patch clamp	Very high	Ultra-low	Very high	High	Submillisecond	Gold standard
Automated oocyte TEVC <sup>1</sup>	High	Low	High	High	Milliseconds	Nonmammalian system, requires RNA preparation
Radioactive flux assays	Medium	Medium to high	Low to medium	Medium	Seconds to minutes	Requires synthesis of radiolabeled probe
Redistribution of voltage-sensitive dyes	Medium	Medium	Medium	Medium	Minutes	Requires high expression, prone to artefacts, long assay development
Ca <sup>2+</sup> -dyes	Medium	Medium to high	Low	Medium to high	Several seconds to minutes	Limited to Ca <sup>2+</sup> (or Ca <sup>1+</sup> -coupled) channels
FRET-based voltage sensors	Medium	Medium	Low	Medium	Several seconds to minutes	Voltage changes need many open channels

Tab. 3 – Comparison of ion channel assay methods using cell based sensor [Fertig08] [Gonzalez99].

Using the indirect screening techniques, listed in Tab. 3, a ‘Yes/No’ type of answer generates to the question of compound activity, and they are limited in sensitivity and information content, with the risk of false negatives. Therefore, a follow-up, secondary screening with more information dense methods like patch clamp are required for further characterization of the ‘hits’ from the primary screening. Ideally, electrophysiological measurements should be performed as early as possible in the screening cascade, to obtain better information about the drug candidates, and also possible safety liability issues.

Many pharmaceutical companies are screening between 100,000 and 300,000 compounds per screen to produce approximately 100 to 300 hits. Usually only 1 or 2 of these hits become lead compounds for further development. Occasionally, screens of over 1 million compounds are required to generate a sufficient number of lead compounds. Lead generation can be improved by increasing the diversity of compound libraries (ie, number of unique scaffolds). HTS assays are also being used in safety studies, to screen for compounds with undesirable activity. A common example of safety HTS is screening for blockade of the hERG ion channel. hERG blockade has been associated with sudden death in a number of marketed drugs and many companies are screening their libraries beforehand to eliminate these compounds before a hit is even identified. large-scale ion channel screening of wanted and unwanted drug effects



is required, but has been limited by the lack of adequate screening technology, because available methods put a trade-off between high-throughput and high-information content. The advent of automated patch clamp platforms has revolutionized ion channel screening, enabling investigations from a more functional perspective at a much higher throughput [web2].

To summarize, several screening techniques with high-throughput capabilities are available for drug screening efforts, but those are limited in sensitivity and thereby at risk for false negatives and missing out on a potential blockbuster drug [Fertig08]. The development of automated patch clamp technology has the potential to provide detailed information on structure–activity relationship of the compound at much higher throughput earlier in the drug discovery process [Sinclair02] [Estes08]. New developments within this area hold a promise for increasing the throughput capabilities even more, and lowering the price per data point, which are the two main requirements heard from the pharmaceutical industry.

## Ion channel acquisition techniques

Ion channels are natural pores formed by proteins that spontaneously insert into cell membranes. When it forms, the ion channel allows the ions passage across the membrane down to the channel thanks to an electrochemical gradient between the two solutions separated by the membrane. There are hundreds of different ion channels and they are distinguished based upon their ion selectivity, gating mechanism, and sequence similarity. Ion channels can open and close their pore in response to different gating criteria: voltage gated, ligand gated, pH gated, or mechanically gated. I.e., voltage-gated ion channels open or close their pore depending on the voltage gradient across the membrane while ligand-gated ion channels open or close their pore depending on binding of ligands to the channel receptor Fig. 4.

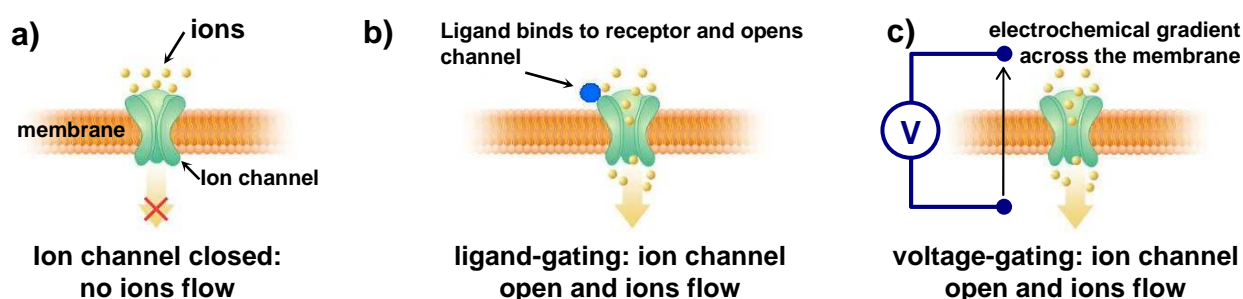
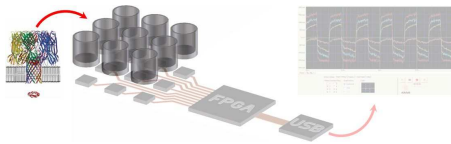


Fig. 4 – Ion channel gating mechanism: a) ion channel closed and no ion current flow through it; b) ligand binds to ion channel receptor and pore opening; c) voltage-gating by means of an electrochemical gradient across the membrane.



In a typical setup system, a membrane embedding ion channels separates two solutions, that can be the intra and extra cellular solution, when whole cells are used (the patch clamp technique) (Fig. 5 a), otherwise a septum with a small hole, where an artificial lipid membrane is formed, is separating two reservoirs each of one is filled with solution (Fig. 5 b). The ions flowing under an electrochemical gradient across the membrane can be detected and converted into an electrical current by means of appropriate electrodes, shown in Fig. 5. For instance, typically,  $10^4$   $\text{Na}^+$  ions that cross the membrane each millisecond by a single opened  $\text{Na}^+$  channel are equals to a current of 1.6 pA ( $1.6 \times 10^{-19}$  C/ion  $\times 10^4$  ions/ms  $\times 10^3$  ms/s).

Several types of electrodes are used in electrophysiological measurements; the most common is a silver/silver chloride (Ag/AgCl) interface, which is a silver wire coated with

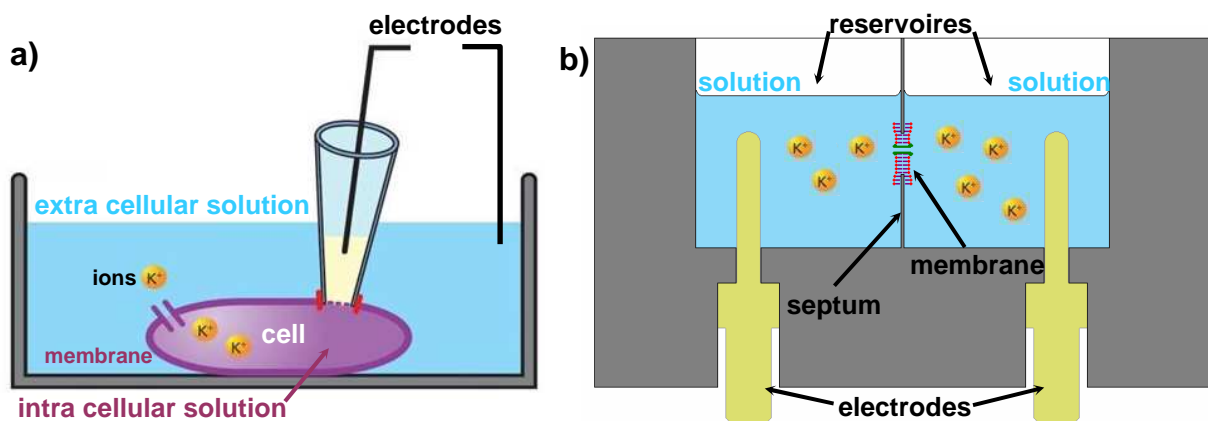


Fig. 5 – Different Ion channel setup: a) show a typical patch clamp system, where the cell membrane separate the extra cellular from the intra cellular solution. Ions flow is regulated by ion channels through across the membrane; b) illustrate a setup for artificial lipid bilayer with bedded ion channel, instead the cell membrane, to allow the ion flow between the two reservoirs separated by a septum.

silver chloride. If electrons flow from the silver wire to the electrode AgCl pellet, they convert the AgCl to Ag atoms and the  $\text{Cl}^-$  ions become hydrated and enter the solution (Fig. 6). If electrons flow in the reverse direction, Ag atoms in the silver wire that is coated with AgCl give up their electrons (one electron per atom) and combine with  $\text{Cl}^-$  ions that are in the solution to make insoluble AgCl.

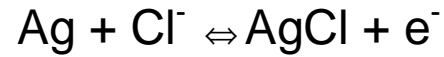
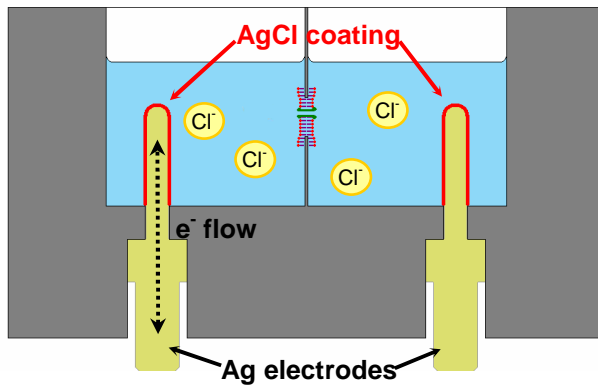
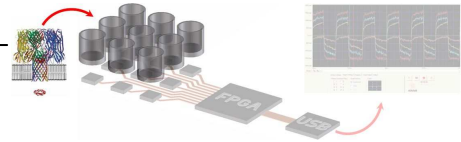
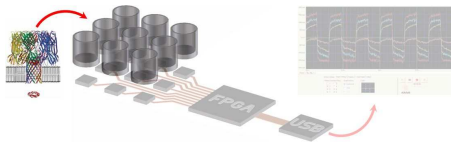


Fig. 6 – Ions flowing to electronic current exchange, from Ag/AgCl electrodes to Cl<sup>-</sup> ions at the electrode coating interface to the solution containing ions; red-ox equation.

This is, therefore, a reversible electrode, i.e., current can flow in both directions. There are several points to remember about Ag/AgCl electrodes:

- the Ag/AgCl electrode performs well only in solutions containing chloride ions;
- because current must flow in a complete circuit, two electrodes are needed. If the two electrodes face different Cl<sup>-</sup> concentrations (for instance, 3 M KCl inside a micropipette and 120 mM NaCl in a bathing solution surrounding the cell), there will be a difference in the half-cell potentials (the potential difference between the solution and the electrode) at the two electrodes, resulting in a large steady potential difference in the two wires attached to the electrodes. This steady potential difference, termed liquid junction potential, can be subtracted electronically and poses few problems as long as the electrode is used within its reversible limits;
- if the AgCl is exhausted by the current flow, bare silver could come in contact with the solution. Silver ions leaking from the wire can poison many proteins. Also, the half-cell potentials now become dominated by unpredictable, poorly reversible surface reactions due to other ions in the solution and trace impurities in the silver, causing electrode polarization. However, used properly, Ag/AgCl electrodes possess the advantages of little polarization and predictable junction potential [Axon08].

The ions flowing across the cell membrane, converted into an electronic current by means of appropriate electrodes, is acquired by a headstage, constituted by a glass micropipette containing the reading Ag/AgCl electrode and an operational amplifier circuit in the trans impedance configuration. The reading electrode is clamped at the command voltage  $V_{cmd}$ , as indicated in Fig. 7, thanks to the virtual short circuit of the operational amplifier. The command voltage is the stimulus provided to the cell membrane, to activate the ion flow across the ion channel. By means of a resistive feedback  $R_f$ , the input current to voltage trans-impedance



operational amplifier convert the acquired current  $i$  to a proportional voltage signal,  $V_{out}$ , that can be converted into a digital one to be measured and displayed. The electrical measurement with the previously indicate circuit is affected by some problems, related to the performances required to the system. Typically, electro physiologists are interested in recording ion channel activity with a resolution of about  $150 \mu\text{s}$  or less. In whole cell acquisitions, the entire cell membrane contributes to the charging time constant. The equivalent series resistance of the Ag/AgCl electrode immersed in solution is typically  $5\text{-}20 \text{ M}\Omega$  and the cell membrane capacitance is typically about  $12 \text{ pF}$  or more. The resulting time constants, ( $\tau = R \cdot C = 20 \text{ M}\Omega \cdot 12 \text{ pF} = 4 \text{ ms}$ ), is in the order of millisecond, so more higher then the required performances. This access time constant is also the time constant for the membrane current  $i$  of Fig. 7 to reach the current measuring circuitry [NehSak95]. Therefore, compensation circuitry to increase bandwidth is an indispensable component of a whole-cell patch clamp system.

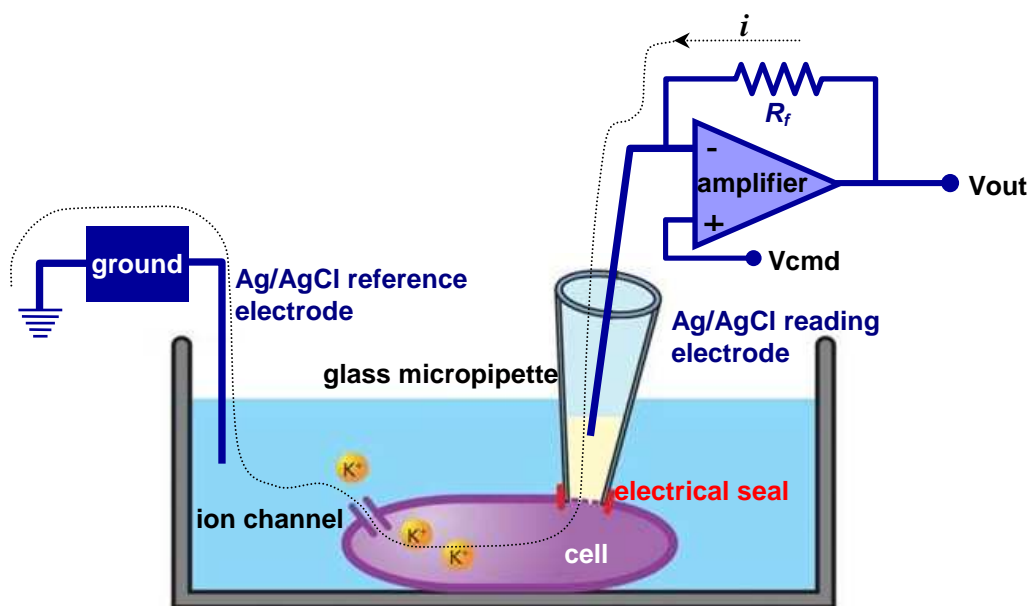
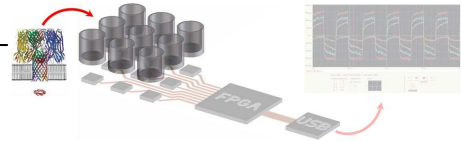


Fig. 7 – Current readout circuit. The headstage, constituted by a glass micropipette containing an Ag/AgCl electrode, monitors the cell membrane current while the reading electrode is clamped at the command voltage,  $V_{cmd}$ , using an input current to voltage trans-impedance operational amplifier by means a resistive feedback  $R_f$ . The output signal  $V_{out}$  is proportional to the measured current  $i$ .

### Series resistance compensation

The time constant associated with charging the cell membrane when a command voltage step  $V_{cmd}$  is applied to the reading electrode is several hundred microseconds. There is also a voltage error (Fig. 8) of tens of millivolts between the electrode potential  $V_p$  and membrane



potential  $V_m$  due to the voltage drop across the series resistance since the membrane currents  $i$ , that is in the order of nano amperes. A series resistance compensation is required to minimize this error. In the ideal experiment, the resistance of the patch micropipette in whole-cell experiments would be zero. In this case, the time resolution for measuring membrane currents and changing the membrane voltage would be limited only by the speed of the electronics (typically just a few microseconds). Series resistance compensation using positive feedback is an attempt to achieve this ideal electronically [Axon08].

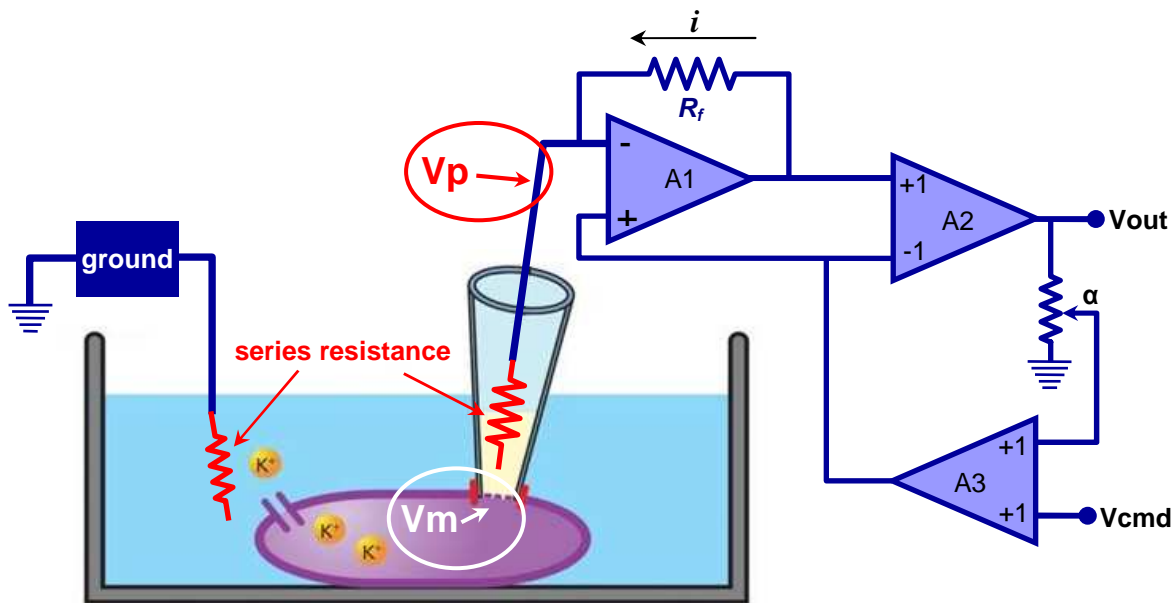
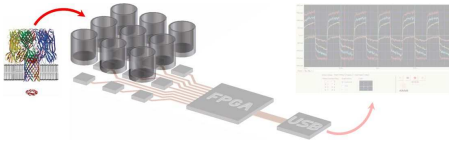


Fig. 8 – Series resistance evidential in patch clamp setup, due to the Ag/AgCl electrode interface to the bath solution, typical in the 10-20 M $\Omega$  range. Operational amplifier A1 is configured as a current-to-voltage converter. Differential amplifier A2 subtracts the pipette potential ( $V_p$ ) to generate the current output ( $V_{out}$ ). A fraction ( $\alpha$ ) of  $V_{out}$  is summed with the command voltage ( $V_{cmd}$ ) used to control  $V_p$ . This causes both a transient and a steady-state increase in  $V_p$  compared with  $V_{cmd}$ . As a result, the membrane charges faster, the voltage drop across the electrode resistance is compensated and the bandwidth is increased.

Basically, a signal proportional to the measured current  $i$  is used to increase the command potential  $V_{cmd}$  (Fig. 8). This increased command potential compensates in part for the potential drop across the micropipette. The amount of compensation achievable is limited by two considerations. First, as the compensation level  $\alpha$  (part of  $V_{out}$ ) approaches 100%, the increase in the command potential hyperbolically approaches infinity. For example, at 90% compensation, the command potential is transiently increased by a factor of ten ( $V_{cmd}/(1 - \alpha)$ ). Thus at large compensation levels the electronic circuits approach saturation. Second, the current feedback is positive; therefore, the stability of the circuit is degraded by the feedback and at 100% compensation the circuit becomes an oscillator. In practice, the oscillation point is





much lower than 100% because of non-ideal phase shifts in the micropipette and the cell membrane [Axon08].

In Fig. 8, a single pipette is used to voltage-clamp the cell. Operational amplifier A1 is configured as a current-to-voltage converter. Differential amplifier A2 subtracts the pipette potential ( $V_p$ ) to generate the current output ( $I$ ). A fraction ( $\alpha$ ) of  $I$  is summed with the command voltage ( $V_{cmd}$ ) used to control  $V_p$ . This causes both a transient and a steady-state increase in  $V_p$  compared with  $V_{cmd}$ . As a result, the membrane charges faster, the voltage drop across the electrode resistance is compensated and the bandwidth is increased.

## Capacitance compensation

Compensating the pipette capacitance in a patch clamp has different purposes. First, during the transient the potential at the top of the pipette is changing slowly while the pipette capacitance charges. By rapidly charging the pipette capacitance through the compensation circuitry, the potential at the top of the pipette is stepped more rapidly, reducing the likelihood that rapid-onset ionic currents will be distorted. Second, uncompensated pipette capacitance has a detrimental effect on the stability of the series-resistance correction circuitry. The component of the current that flows into the pipette capacitance is not in series with any resistance. Thus the series-resistance correction circuit exceeds 100% compensation for this component of the current as soon as the circuit is switched in [Axon08].

The bulk of the transient is reduced by using the fast magnitude and time constant ( $\tau$ ) controls. The magnitude control compensates the net charge. The  $\tau$  control adjusts the time constant of the charge compensation to match the time constant of the command pathway and to compensate for small non-idealities in the frequency response of the pipette and electronics. The residual slow component seen in many pipettes is reduced by using the slow magnitude and  $\tau$  controls. A simplified circuit of the fast and slow compensation circuitry is shown in Fig. 9. When the command potential ( $V_p$ ) changes, current  $i_m$  flows into  $C_m$  to charge it to the new potential. If no compensation is used,  $i_m$  is supplied by the feedback element ( $R_f$ ), resulting in a large transient signal on the output ( $i$ ). By properly setting the fast and slow magnitude and  $\tau$  controls, a current ( $i_{ci}$ ) can be induced in capacitor  $C_i$  (connected to the headstage input) to exactly equal  $i_m$ . In this case no current needs to be supplied by  $R_f$ , and there is no transient on the output.

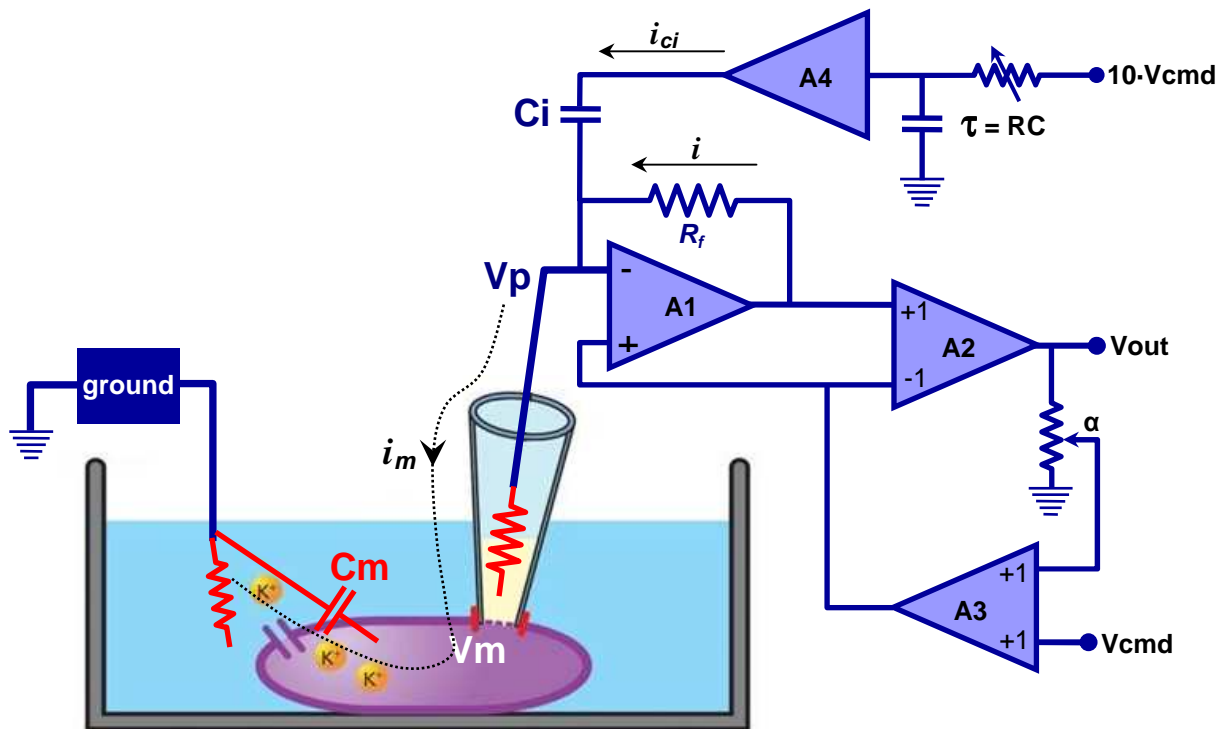
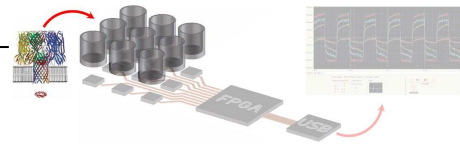
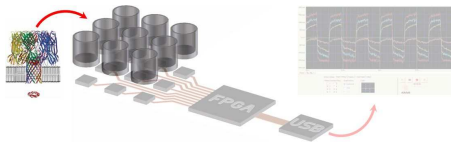


Fig. 9 – Capacitance compensation circuit, to reduce the parasitic of the cell membrane.

When the command potential ( $V_p$ ) changes, current  $i_m$  flows into  $C_m$  to charge it to the new potential. If no compensation is used,  $i_m$  is supplied by the feedback element ( $R_f$ ), resulting in a large transient signal on the output ( $i$ ). By properly setting the fast and slow magnitude and  $\alpha$  controls, a current ( $i_{ci}$ ) can be induced in capacitor  $C_i$  (connected to the headstage input) to exactly equal  $i_m$ . In this case no current needs to be supplied by  $R_f$ , and there is no transient on the output.

## Conventional experimental techniques

Several techniques were developed to study the ion channel activity, ranging from the patch clamp technique, used in electrophysiology experiments, to the planar lipid membrane (BLM) used as artificial substrate for protein insertion to host ion channels. These and other techniques can be grouped into two main categories: those that use natural whole cells with embedded ion channel or giant BLM vesicles, and those that use artificial lipid membranes, shaped into planar membrane suspended over a small apertures formed by means of different techniques.



## Patch clamp

The standard technique for measure small electrical currents that flow through ion channels is known as patch clamp electrophysiology method, developed by Erwin Neher and Bert Sakmann in the late 1970s and early 1980s, winners of the Nobel Prize in 1991 [NehSak92]. In the commonly setup configuration, the tip of a glass micropipette, containing a silver/silver chloride electrode and filled with a solution matching the ionic composition of the bath solution, is positioned onto the membrane surface of a cell (Fig. 10).

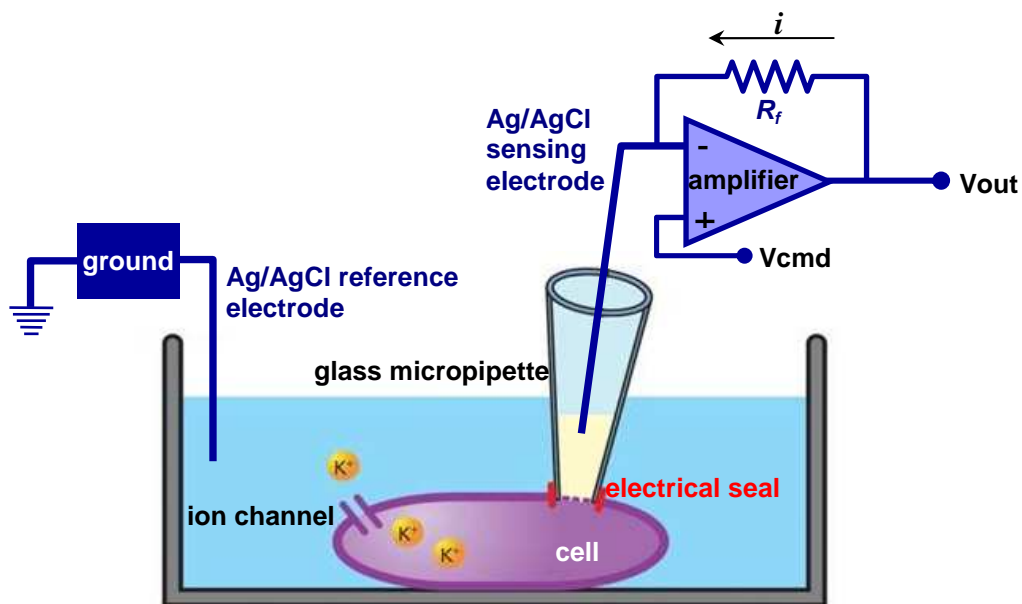
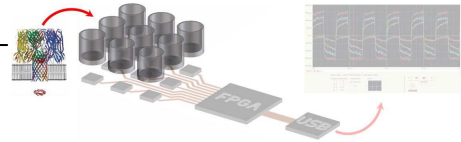


Fig. 10 – Patch clamp technique.

A mild suction is then applied at the micropipette to form a high resistance seal between the micropipette glass and the cell membrane, (a "gigohm seal" or "gigaseal," since the electrical resistance of that seal is in excess of a gigaohm), and to pull away the piece of cell membrane enclosed by the pipette tip (the *patch*). The high resistance of this seal makes it possible to electronically isolate the currents measured across the membrane patch with little competing noise, as well as providing some mechanical stability to the recording. In this way, an electrical continuity between the pipette electrode is established, and the inside cell solution plus all the membrane potential can be precisely voltage controlled (*clamped*). The investigator can change the composition of the bath solution or add drugs to study the ion channels under different conditions. Currents passing across the entire cell membrane, representing the overall activity of all the ion channels embedded into the cell membrane, can then be recorded with a voltage reference fixed to a second electrode positioned in the external medium. Unlike traditional two electrode voltage clamp recordings, patch clamp recording uses a single electrode to record

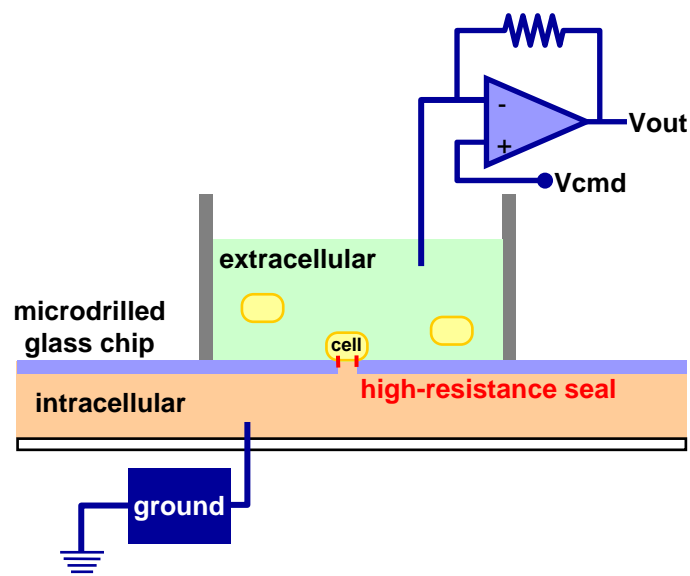


currents. Many patch clamp amplifiers do not use true voltage clamp circuitry but instead are different amplifiers that use the bath electrode to set the zero current level. This allows a researcher to keep the voltage constant while observing changes in current. Alternatively, the cell can be current clamped in whole cell mode, keeping current constant while observing changes in membrane voltage.

Patch clamping is a very powerful technique since it is very sensitive and present the needed temporal resolution for detecting the ultra rapid kinetics of ion channels (which can open and close within just a few milliseconds) and it is capable of measuring currents as low as 10 pA (corresponding to flow rates of only  $10^{-7}$  ions per second). The data obtained by this method present very high fidelity and quality since the technique provides a direct readout of ion channel function and a precise control over the channel gating is obtained thanks to the clamping of the membrane potential.

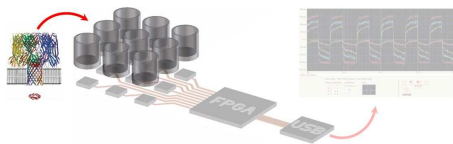
### ***Planar patch clamp***

The planar patch clamp is a novel ion channel investigation technique, developed for high throughput electrophysiology approach, and offer the capability to be automated. Instead of positioning the patch pipette on an adherent cell, if a suspension of cells is added over a glass chip containing a microscopic aperture and suction is applied through it, a cell becomes trapped and an electrical seal is formed.



*Fig. 11 – Planar patch clamp technique.*

As with manual patch clamp, the patch of membrane over the aperture is then sucked away so that whole cell recordings can be made between a ground electrode located below the glass



chip, and the recording electrode that are lowered into the well (Fig. 11) [Fertig02]. The planar geometry of the glass chip offers a variety of advantages compared to the classical experiment patch clamp setup: it allows for integration of microfluidics, which enables automatic compound application for ion channel investigation; the system is accessible for optical or scanning probe techniques; perfusion of the intracellular side can be performed.

## **Artificial lipid bilayer formation techniques**

Instead of cell membranes, artificial lipid bilayers can be used to host ion channels, and different techniques to form BLM have been known since the 1950s [Tien74]. The first methodology developed was the *painted* bilayer, also known as a *black lipid membrane*, where the bilayer are made by a painting process. First, a small aperture is created in a hydrophobic material foil such as Teflon or Delrin, and typically the hole diameter is in the range from tens to hundreds of micrometers. A solution of lipids dissolved in an organic solvent is then applied with a borosilicate rod over the aperture. The solvent used, usually the decane, must have a very low partition coefficient in water and must be relatively viscous to prevent immediate rupture. A monolayer of lipid spontaneously forms at the interface between the organic solvent and aqueous phases on either side of the lipid solution droplet. Because the walls of the aperture are hydrophobic the lipid-solvent solution wets this interface, thinning the droplet in the center. Once the two sides of the droplet come close enough together, the two lipid monolayers fuse, rapidly excluding the small remaining volume of solution. At this point a bilayer is formed in the center of the aperture, but a significant annulus of solvent remains at the perimeter. This annulus is required to maintain stability by acting as a bridge between the 5 nm thickness bilayer and the thick sheet in which the aperture is made [White72].

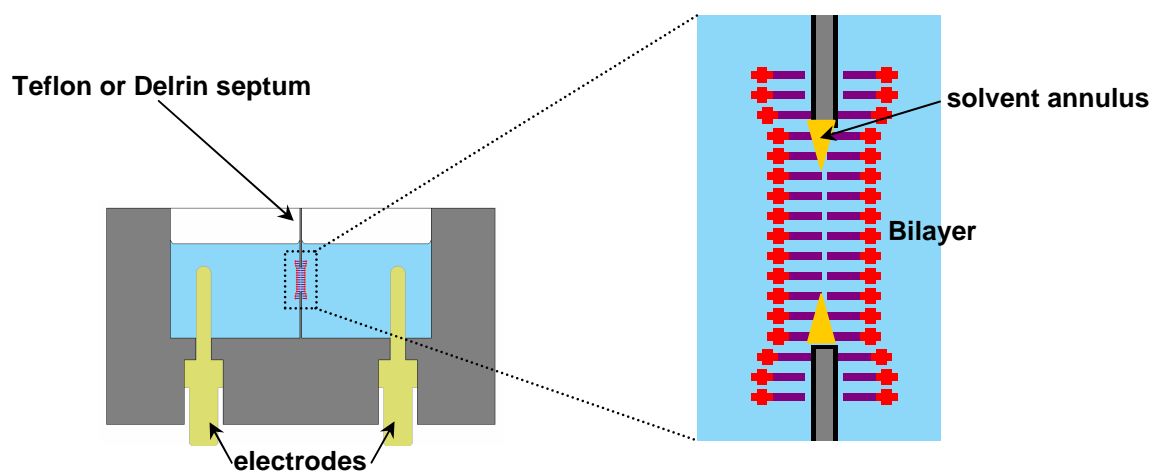
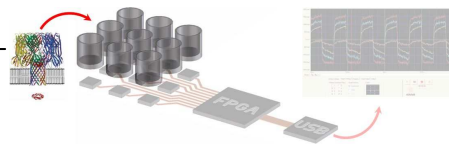


Fig. 12 – Painting technique for BLM formation on a small hole on a Teflon or Delrin septum that split two chambers. Detail of BLM assembly over the hole, and residual solvent annulus around the hole border.



The term *black* bilayer means that the membrane is dark to reflected light because its thickness is only a few nanometers, so light reflecting off the back face destructively interferes with light reflecting off the front face. Indeed, this was one of the first clues that this technique produced a membrane of molecular-scale thickness [Tien66]. The two chambers setup, separated by the bilayer, allows a good characterization of the electrical properties of black lipid membranes by means of simple placement of electrodes inside both solution chambers. Simple measurements indicate when a bilayer forms and when it breaks, as an intact bilayer has a large resistance ( $>G\Omega$ ) and a large capacitance ( $\sim 2\mu\text{F}/\text{cm}^2$ ). Membrane proteins such as ion channels typically cannot be incorporated directly into the painted bilayer during the formation process because the lipid immersion in an organic solvent would denature the protein. Instead, the protein is solubilized with a detergent and added to the aqueous solution after the bilayer is formed. The detergent coating allows these proteins to spontaneously insert into the bilayer over a period of minutes. Some experiments have been performed to combine electrophysiological and structural investigations of black lipid membranes [Beerlink09].

The painting technique present some problems, as the residual solvent and limited lifetime of the bilayer. Some researchers believe that pockets of solvent trapped between the two bilayer leaflets can disrupt normal protein function. To overcome this limitation, Montal and Mueller developed a modified deposition technique that eliminates the use of a heavy non-volatile solvent [MM72]. The technique (Fig. 13) consist of the formation of two lipid monolayers above the aqueous surface by applying a lipid solution in a volatile solvent, such as pentane or chloroform, and waiting for the solvent evaporation.

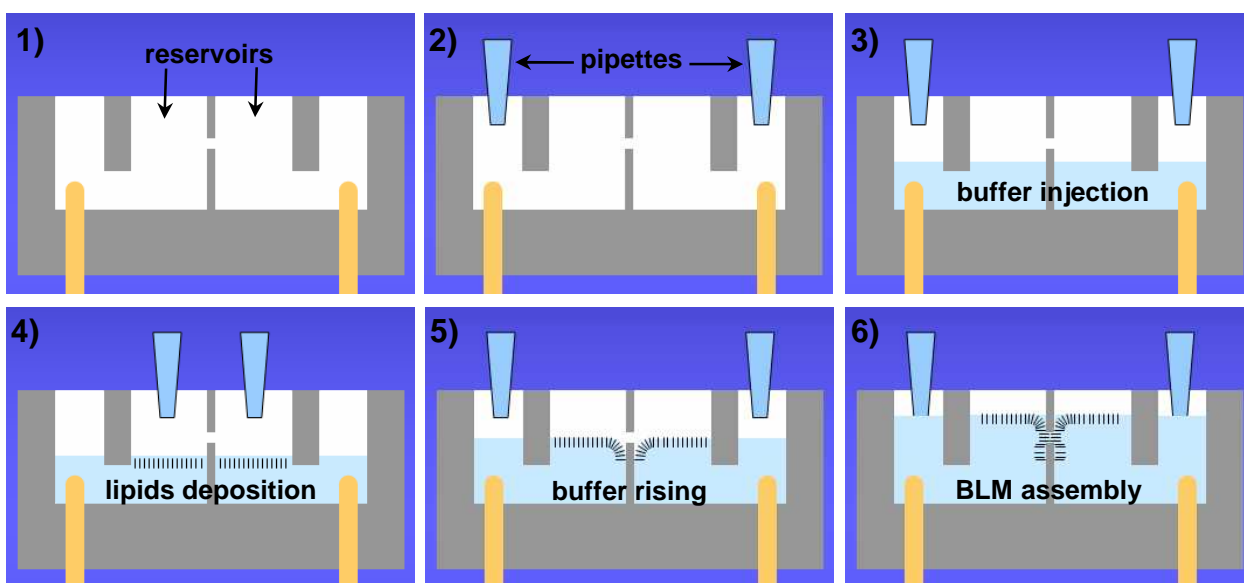
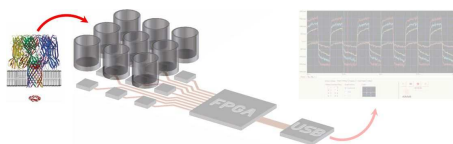


Fig. 13 – Montal Muller technique for BLM formation on a small hole on a Teflon or Delrin septum that split two chambers. 1) device empty; 2) pipette positioning on the inlet channels; 3) injection of buffer solution; 4) deposition of lipids for monolayer assembly on the two solution surfaces; 5) rising solution level to 6) the final bilayer assembly.



The two chambers are always separated by a thin septum, but the micro aperture during the monolayer formation is out the aqueous surface. After the evaporation time, the micro aperture of the septum is lowered into the air-aqueous surface, and the two monolayers from the separate chambers are folded down against each other, forming a bilayer across the aperture [MM72].

BLM lifetime strictly depends on several issues, from the setup stability, temperature, differential pressure on the two chambers, voltage applied. This lifetime can be extended by precisely structuring the supporting aperture [Ziegler08], chemically crosslinking the lipids or gelling the surrounding solution to mechanically support the bilayer [Jeon07] [Pioufle08], [Sandison07], [Poulos09], [Baaken08], [Schmidt08].

Others techniques are currently under develop, as the falling droplets through a small bottle need, or the deposition of small droplets of lipid solution over a previously formed lipid monolayer, using the aqueous-lipid monolayer interface. Nevertheless, these techniques are not suitable to be automated, because they requires a very accurate electrode positioning to one of the droplets, to ensure the electrical connection.

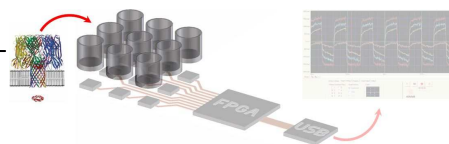
## Commercial instrumentation

There are several instruments available on the market for low noise current measurements in patch clamp electrophysiology setup, depending from the target application: experimental investigation over single ion channel or automatic approach to HTS systems. One important feature is the number of parallel acquisition channels available, even the microfluidic integrated systems.

The benchmark laboratory instrument for electrophysiology experiments and patch clamp techniques is the Axon Axopatch 200B amplifier from Molecular Devices [Axon08] that achieves an input-referred noise floor as low as 25 fArms at 1kHz ( $0.7\text{fA}/\sqrt{\text{Hz}}$  up to 1kHz), but offers only one acquisition channel. Another laboratory instrument is the family of HEKA EPC 10, available in the configuration from one to four acquisition channels. The noise performance, using the “Red Star Headstage” are 31 fArms at 1kHz ( $0.98\text{fA}/\sqrt{\text{Hz}}$  up to 1kHz) [heka].



Fig. 14 – On market available patch clamp amplifier: HEKA EPC 10, Axon Axopatch 200b.



They have also several parasitic capacitance and resistance compensation circuits especially for whole cell patch clamp acquisitions. However, these instrument are bulky and often they uses a cooled headstage to boost performance, so they are primarily used in laboratory since they are bulky and require expert users. Several automated platforms are commercially available, the first one on the market being the Ionworks HT and later Ionworks Quattro (Molecular Devices Corporation, now MDS Analytical Technologies, <http://www.mdsinc.com/>) followed by the PatchXpress (MDS, formerly Axon Instruments Inc.), and Nanion's Port-a-Patch (Nanion Technologies GmbH, <http://www.nanion.de/>). Other automated patch clamp devices are Sophion's QPatch-16 and -48 (Sophion Biosciences A/S, <http://www.sophion.dk>), Flyion's Flyscreen (Flyion GmbH, <http://www.flyion.com>) and Nanion's Patchliner platform. The true giga-seal patch clamp recording platforms are the PatchXpress, Port-a-Patch, Patchliner, Flyscreen and the QPatch. In Tab. 4 the different instruments are compared and their features and capabilities are listed [Fertig08].

Instrument	Patchliner	Port-a-Patch	QPatch	PacchXpress	Ionworks HT	Flyscreen B500
<b>Company</b>	Nanion	Nanion	Sophion	MDS	MDS	Flyion
<b>Substrate supplier</b>	Nanion	Nanion	Sophion	Aviva	MDS	Flyion
<b>Recording configuration</b>	Whole cell, perforated patch	Whole cell, perforated patch, bilayer	Whole cell	Whole cell	Perforated patch (loose patch clamp)	Whole cell, perforated patch
<b>Electrode type</b>	Planar, glass	Planar, glass	Planar, silicon	Planar, glass	Planar, plastic	Pipette, glass
<b>Recording chambers</b>	16	1	16,48	16	384	3-6
<b>Amplifier channels</b>	4-8	1	16,48	16	48	3-6
<b>Data points per day</b>	250-500	50	250-3500	300	3000	100-500
<b>Recording during application</b>	Yes	Yes	Yes	Yes	No	Yes
<b>Compound wash out</b>	Yes	Yes	Yes	Yes	No	Yes
<b>Unlimited cpd/wash additions</b>	Yes	Yes	No	Yes	No	No
<b>Seal resistance</b>	>1 GΩ	>1 GΩ	>1 GΩ	>1 GΩ	50-1000 MΩ	>1 GΩ
<b>Rs and Cslow compensation</b>	Yes	Yes	Yes	Yes	No	Yes
<b>Internal perfusion</b>	Yes	Yes	No	No	No	No
<b>Temperature control</b>	Yes	Yes	No	No	No	Yes
<b>Current clamp</b>	Yes	Yes	No	No	No	Yes
<b>User intervention during experiment</b>	Yes	Yes	No	No	No	No
<b>Consumable pricing</b>	Moderate	Moderate	High	High	Moderate	Moderate

Success rates for stable whole-cell recordings are in the range of 50–90% for all instruments according to provider websites but experiences by individual users do vary. Perfusion time constants are claimed to be around 50 ms for all systems.

Tab. 4 – Features and performance of the available automated patch clamp instrumentation [Fertig08].



# Chapter 2

## Low Noise front-end ASIC design: Delta Sigma ADC and single bit data output

### Introduction

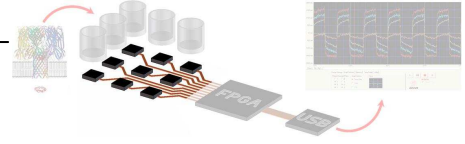
Membranes that contain nanopores are attracting rapidly increasing interest from a broad community of scientists in nanotechnology, chemistry, physics, engineering, and the life sciences [Choi06] [Ito04] [Martin00] [Branton02] [Seidel07] [Bayley06] [Blake06] [Capone07] [Gitlin08]. This interest partially stems from the ability of these pores to act as a sensitive transducer that can detect nanoparticles, individual macromolecules, and even individual small molecules in solution. In a typical experiments, a voltage is applied across the membrane and the ionic current flowing through the pore is monitored. Two parameters are of critical importance for pore-based sensing [NehSak95] [Axon08] [Kriebel03] [Rae98]:

- the signal bandwidth, that determines the accuracy with which a temporal change in the current flowing through the pore is detected;
- the current noise, that directly influences the sensitivity of a given pore.

A detailed theoretical and experimental study on the signal bandwidth and the noise of current recordings from membranes that contain nanopores is required to reach the guidelines for achieving reliable and sensitive low-noise recordings from these pores, enabling the optimization and an accurate prediction of these two parameters in the low noise acquisition front-end design process.

Interfacing current based nanopores becomes challenging since the output signals consist of currents in the pA range or less and in the kHz bandwidth. Resistive sensing interfaces could be used for nanotube and nanowire sensing [Lieber01], however they are not applicable to nanopores with rapid time varying current outputs.

Future applications of nanobiosensors require a readout circuit tightly close to the sensor substrate for the following reasons: i) the noise is correlated to the input stray capacitance and the closer the readout the lower the noise; ii) nanosensors are usually arranged in array structures: due to the low currents and the timing required, multiplexing should be avoided since this reduces the performance [Cresc09]. For the above reasons, a compact and integrated sensing structure is required to increase the overall performance. This chapter will present in



the next sections an architecture for a low-noise, ultra-low current amplifier based on a integrated discrete time approach.

## Noise vs. bandwidth

In all current acquisition front-end for nanopores, the input stage of the recording electronics convert the measured current into a voltage signal by using a current-to-voltage converter, also know as trans-impedance amplifier, illustrated in Fig. 15. This I-V converter generates the majority of the noise that is added to the current signal in the acquisition front-end [NehSak95].

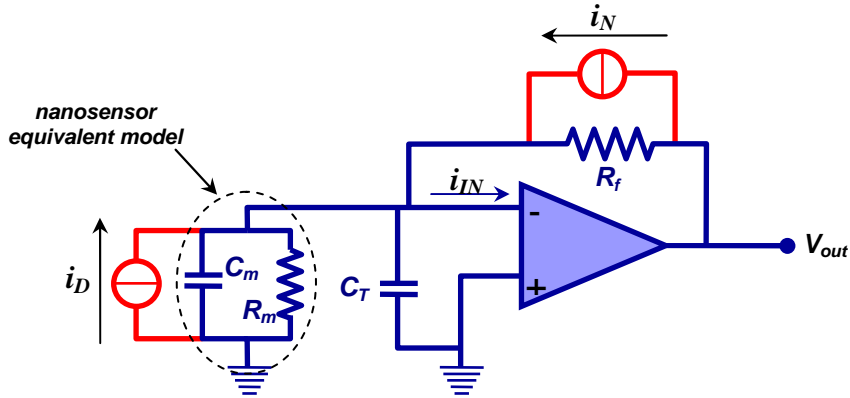


Fig. 15 – Current acquisition front-end. A trans-impedance amplifier convert the input current  $i_{IN}$  to a voltage ( $V_{out}$ ). Evidential of noise contribute, from the feedback resistor  $i_N$  and from the equivalent simplified model of the sensor  $i_D$ .

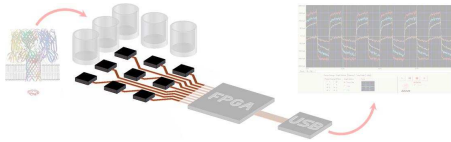
A generic current sensed nanodevice shows an input-referred noise floor current  $\overline{i_{IN}^2}$  that is given by:

$$\overline{i_{IN}^2} = \overline{i_D^2} + \overline{i_N^2} \quad (1)$$

where  $\overline{i_D^2}$  is the noise power related to the nanodevice, usually composed of both thermal and  $1/f^\alpha$  components and by the electronic interface noise  $\overline{i_N^2}$ . In the case where input is sensed by a continuous time trans-resistance,  $\overline{i_N^2}$  is approximately given by [Uram08]:

$$\overline{i_N^2} \cong 2qi_{IN} + \frac{4kT}{R_f} + e_n^2 \left( \frac{1}{R_f^2} + 4\pi^2 f^2 C_T^2 \right) \quad (2)$$

where the first term is due to the shot-noise of input devices ( $q$  is the elementary charge of an electron),  $R_f$  is the feedback resistance of the amplifier,  $C_T$  is the total capacitance facing to



the input of the interface (composed of both stray and feedback capacitances) and  $\overline{e_n^2}$  is the input-referred voltage noise of the amplifier, depending also to the signal bandwidth.

For quantitative resistive pulse sensing experiments (i.e., experiments that make use of the peak amplitudes or widths of resistive-pulses), the signal bandwidth must be sufficient to resolve fully the resistive pulses [Kriebel03] [Ke06] [NehSak95] otherwise the data may be inaccurate. Ensuring a high signal bandwidth increases the information content and accuracy of the recordings, however also strongly increases the noise of the current recordings (Fig. 16); this noise limits the signal-to-noise ratio and hence the sensitivity of the pore because the amplitude of a resistive pulse must be above the noise to be detectable [Sun00] [Mitsui04].

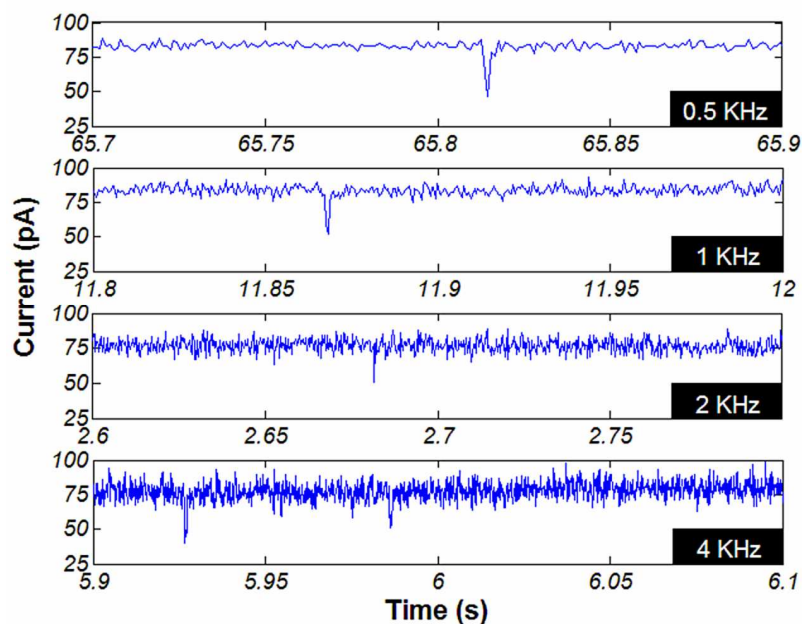
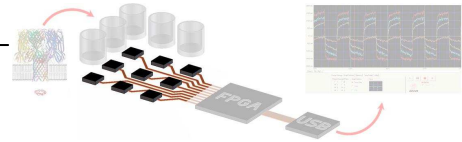


Fig. 16 – Resistive pulses acquired at different bandwidths, from 0.5 to 4 kHz. As shown, increased signal-to-noise ratio can be obtained at the expenses of reduced temporal resolution. Pulses can be detected with respect to the noise floor using narrower bandwidths (from bottom to top). However, some of them are lost when the sampling rate is reduced.

By determining the individual sources of noise, it may be possible to design the acquisition front-end for the experimental setup in a fashion that minimizes the noise, and to predict accurately the current noise of a given experiment. Noise spectra given by (2) shows a typical shape where the noise is asymptotically increasing for frequencies greater than a corner point given by the prevalence of the third term over the others, [Ferrari09] [Gozzini09]. Eq. (2) clearly shows the directions to improve signal-to-noise-ratio (SNR): i) avoid feedback resistances in favor of charge-integrating approaches; ii) reduce input capacitance as much as possible; iii) trade-off input shot noise with low  $\overline{e_n^2}$  values (i.e. MOS vs. JFET transistors). In any case, eq.



(2) shows that the miniaturization of the electronic interface and of the related routing would have a dramatic impact on noise reduction, due to the reducing of  $C_T$ .

## Continuous vs. discrete time approach

The design approach for improving the Signal-to-Noise Ratio (SNR) has led to two general approaches: the continuous time and the discrete time.

The Continuous Time (CT) approach uses a continuous-time feedback loops (a resistor  $R_f$ ) to set the optimal operation point [Ferrari09] [Gozzini09] [Sampietro07] [Culurciello] [Carminati09]. This provides very good results in terms of noise and bandwidth, however, the feedback loop should be carefully designed for both stability and performance within several constraints, and the total input capacitance  $C_T$  plays an important role. Additionally, the noise floor for frequencies under the corner frequency given by  $C_T$  is set by the noise sources in the feedback loop ( $R_f$ ) that need to be carefully analyzed and sized [Sampietro07].

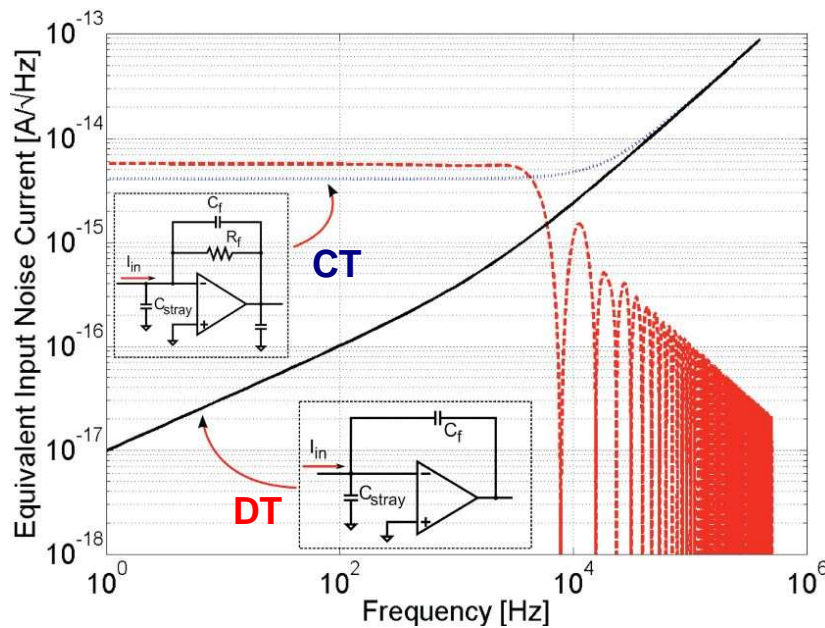
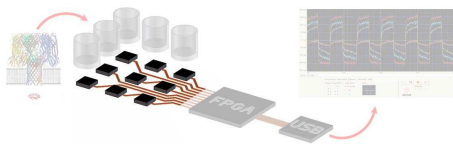


Fig. 17 – Input-referred noise current; comparison between CT sensing using  $R_f=1G\Omega$  (blue), DT approach presented in [Benn09] with 8KHz of sampling frequency (red) and ideal charge sensing amplifier without periodic reset (continuous black line). The values of  $C_f$  and  $C_{stray}$  are identical and equal to 100fF and 3pF, respectively [Cresc10].

The Discrete Time (DT) approach uses a charge integrator as input stage, constituted by a capacitor in the feedback loop of the operational amplifier front-end. The charge integrator is reset at certain time intervals in a discrete-time mode to avoid the signal saturation at the amplifier output [Zhang04] [Stancevic07] [Ayers07] [Gore06] [Benn09]. The discrete-time



solution offers easier and more structured design approach than continuous time ones. In principle, the charge amplifier with no feedback loops offers the best input-referred noise performance at low frequencies, but may suffer of limited dynamic range due to limited values of the feedback capacitance and needs some offset-cancelling technique, making necessary the introduction of auto-zeroing procedures. These procedures introduces noise folding of the output of the charge amplifier resulting in a more complex expression that eq. (2). In order to increase sensitivity, without a strong reduction of operating time, it is mandatory to use a very low value capacitance in the feedback loop. This makes error sources like  $KT/C$  or charge injection phenomena due to reset switches main issues.

## Delta Sigma ADC converter and Low noise front-end

Future applications of nanobiosensors require a readout circuit tightly close to the sensor substrate for the following reasons: i) the noise is correlated to the input stray capacitance and the closer the readout the lower the noise; ii) nanosensors are usually arranged in nanoarray structures: due to the low currents and the timing required, multiplexing should be avoided since this reduces the performance [Cresc09]. For the above reasons, a compact and integrated sensing structure is required to increase the overall performance.

### *Delta Sigma modulator converters*

Delta Sigma modulation is a method for encoding high resolution signals into lower resolution signals using pulse density modulation. This technique has found increasing use in modern electronic components such as analog-to-digital (ADC) and digital-to-analog (DAC) converters, frequency synthesizers, switched-mode power supplies and motor controls. One of the earliest and most widespread uses of delta-sigma modulation is in data conversion. An ADC or DAC circuit which implements this technique can relatively easily achieve very high resolutions using low-cost CMOS processes, such as the processes used to produce digital integrated circuits. A sigma-delta ADC can give more bits of resolution than any other ADC structure [Schreier05].

For the analog to digital converter, the Delta Sigma modulator works as a voltage-controlled oscillator, where the controlling voltage is the voltage to be measured and where linearity and proportionality are determined by a negative feedback loop. The Delta Sigma modulator's output is a pulse stream, each pulse of which has a known, constant amplitude  $V$  and time duration  $dt$ , and thus has a known integral  $V \cdot dt$  but variable separating interval. The interval between pulses

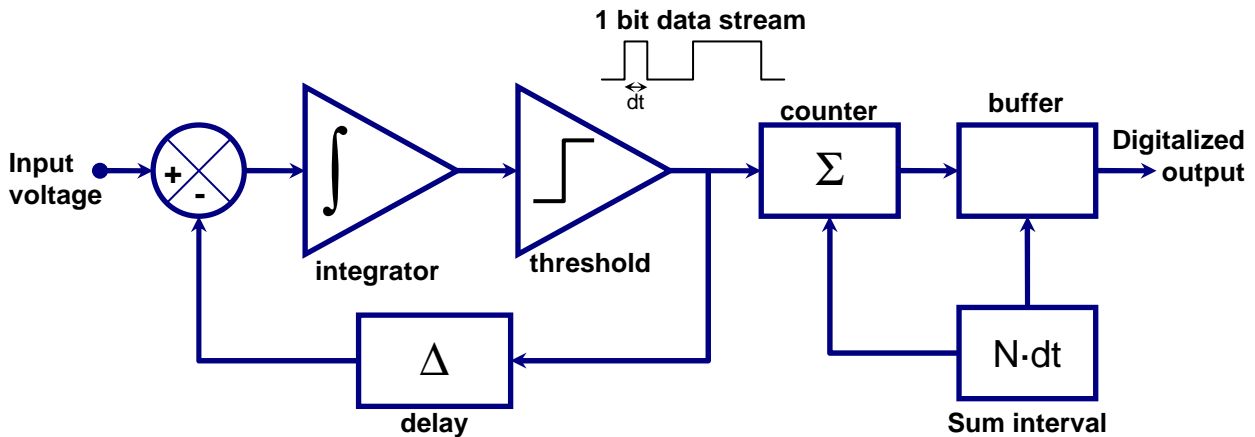
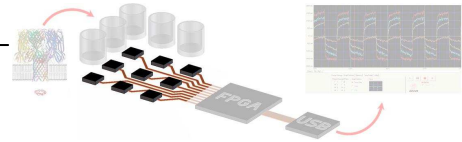


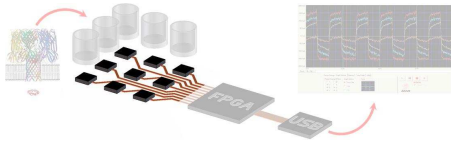
Fig. 18 – Delta Sigma Analog to Digital converter block diagram.

is determined by the feedback loop delay,  $\Delta$ . A low input voltage produces a long interval between pulses and a high input voltage produces a short interval between pulses [Schreier05]. In fact, neglecting switching errors, the interval between pulses is proportional to the inverse of the mean of the input voltage during that interval and thus over that interval,  $t_s$ , is a sample of the mean of the input voltage proportional to  $V/t_s$ . The feedback loop is arranged so that the integral of the input voltage is matched within one count by the integral of the pulse stream [Schreier05]. The finally output count produced is the digitization of the input voltage determined by counting the pulses produced in the way described above in a fixed summing interval  $N \cdot dt$  producing a sum,  $\Sigma$ . The integral of the pulse stream is  $\Sigma \cdot V \cdot dt$  which is produced over an interval  $N \cdot dt$  and thus the average of the input voltage over the summing period is  $V \cdot \Sigma / N$  and is the mean of means and so subject to little variance. The accuracy achieved depends on the accuracy with which  $V$  is known and the precision or resolution is within one count in  $N$  [Schreier05]. Variations in scaling can be produced by either varying the fixed summing interval,  $N \cdot dt$  or by counting down the pulses by a fixed ratio or both methods can be used.

The pulses described above may be treated as the Dirac  $\delta$  (delta) function in a formal analysis and the count as  $\Sigma$  (sigma). It is these pulses which are transmitted for delta-sigma modulation but are counted to form sigma in the case of analogue to digital conversion.

A Delta Sigma ADC is also known as an oversampling converter, because it samples the input signal at a frequency much greater than required by Shannon's theorem and converts the information into a 1-bit data stream [Schreier05] (the one bit data stream of Fig. 18). The ratio between the input oversampling frequency (the fixed delay  $\Delta$  in Fig. 18) and the output Nyquist data rate ( $N \cdot dt$  in Fig. 18) is called oversampling ratio (OSR).

Since the nanosensor signals are in the kHz bandwidth, an input oversampled frequency in the MHz range, corresponding to a one bit digital stream, is sufficient for the required



application. The use of an oversampling ADC converter brings key advantages compared with conventional ADC techniques:

- Higher resolution due to reduced quantization noise. Larger number of equivalent output bits can be obtained with a reduced amount of power and required integration area.
- Improved flexibility. Any data processing can be performed in the digital domain that is particularly useful to tradeoff signal-to-noise-ratio with bandwidth by means of oversampling ratios.
- Simplified array readout. The Delta Sigma approach simplifies the routing architecture since it minimizes the number of output lines because the 1 bit data output signal and allows acquisition of multiple signals concurrently.

### **Low Noise front-end: ASIC architecture**

The developed readout architecture is shown in Fig. 19 [Benn09]. The sensed current is periodically integrated into a single-ended (SE) charge sense amplifier whose output reset values are previously stored into a correlated double sensing, to reduce low-frequency noise and offsets [Temes96], and into a sample-hold block. The S&H output is then transformed from single-ended (SE) into a fully-differential (FD) signals and finally converted into a 1-bit stream by a Delta Sigma modulator.

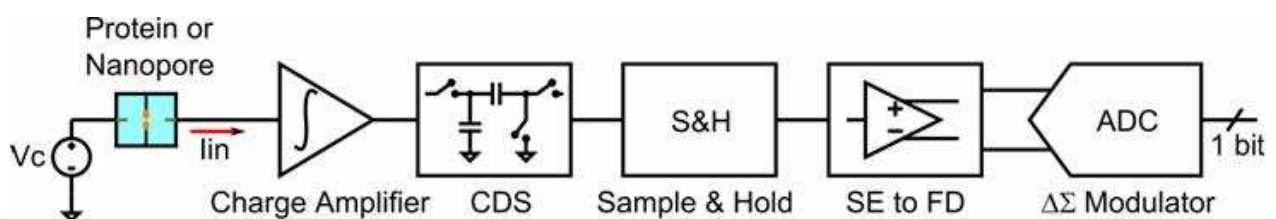
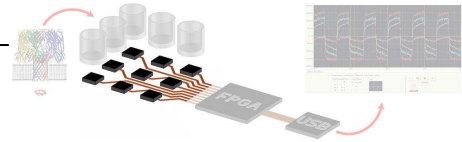


Fig. 19 – Integrated readout front-end. The input current is integrated into a charge sense amplifier whose output reset values are previously stored in a correlated double sensing first and into a sample-hold block then. The S&H output is transformed from single-ended (SE) into a fully-differential (FD) signals and converted into a 1-bit data stream by a Delta Sigma modulator.

A more specific block diagram is shown in Fig. 20. A single-ended charge integrator is followed by a correlated double sampling circuit, which helps to reduce flicker noise and offset, and also acts as a S/H circuit. The preamplifier integrates the input current for 120 $\mu$ s and then it is reset. The total sampling period of the CDS block is 128 $\mu$ s, limiting the bandwidth to about 4kHz. During the reset phase, which is 8  $\mu$ s long, the digital signals  $\Phi$ 1 and  $\Phi$ 2 are high and the relative switches are closed. The charge amplifier is then reset and because the node B is connected to ground during the  $\Phi$ 2 phase, both the two 4pF capacitors are charged to the initial



opamp offset. Moreover,  $\Phi_1$  opens about 6  $\mu\text{s}$  before  $\Phi_2$  therefore this offset includes also the charge injection from the F1 reset transistors. After the reset phase, there is a 120 $\mu\text{s}$  integration phase. During this phase, the charge amplifier integrates the input current and the second 4pF capacitor of the CDS maintains its initial value. Finally, there is the sample phase. First, the S/H is reset by the  $\Phi_4$  digital signal. Then  $\Phi_3$  goes high and the charge of the two 4pF capacitors, which are connected in series this time, is transferred to the second integrator of the front-end.

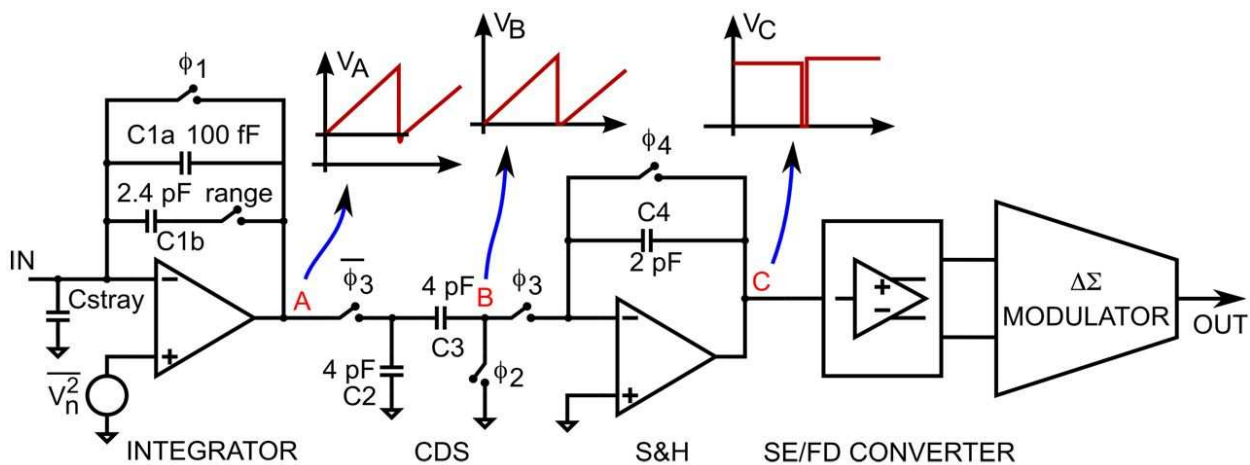


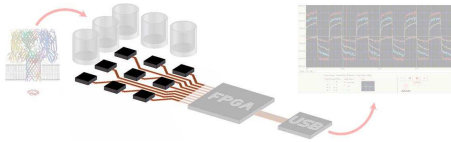
Fig. 20 – Integrated circuit data flow, with phases indication for the signal conversion operation.

Since the two CDS capacitors are in series, the effective charge transferred is the difference of the two CDS capacitor charges and the value at the node C sampled by the S/H is the difference between the final integrated input current and the initial offset. The potential at the node C, which remains constant for the next 128  $\mu\text{s}$ , is converted into a fully differential signal by SC network controlled by the  $\Phi_5$  and  $\Phi_6$  not overlapping digital clock signals and then digitized by a first order  $\Delta\Sigma$  modulator. Both the single-ended-to-fully-differential converter and the delta-sigma converter have a 1MHz sampling frequency. Using 240mV reference voltages and a clock period of 1MHz, the full scale range can be set to 200pA and 5nA respectively, depending on the input charge integrator feedback capacitor which can be selected with a switch.

## Design simulations

Since the Correlated Double Sensing is a time-variant discrete-time circuit, it is not possible to use the classical AC noise analysis to correctly describe its noise behaviour, so a transient time analysis is performed [Rochelle05] as follows. The time-variant input noise sample is generated using Matlab®, with the proper power spectrum described by  $\overline{e_n^2}$ . The flicker noise is





generated using the algorithm provided by [Little07]. Samples are in SPECTRE® simulator using the PWLF generator placed at non-inverting input. The results of SPECTRE® transient analysis are loaded in Matlab® to compute the input referred noise and compare it with theory study.

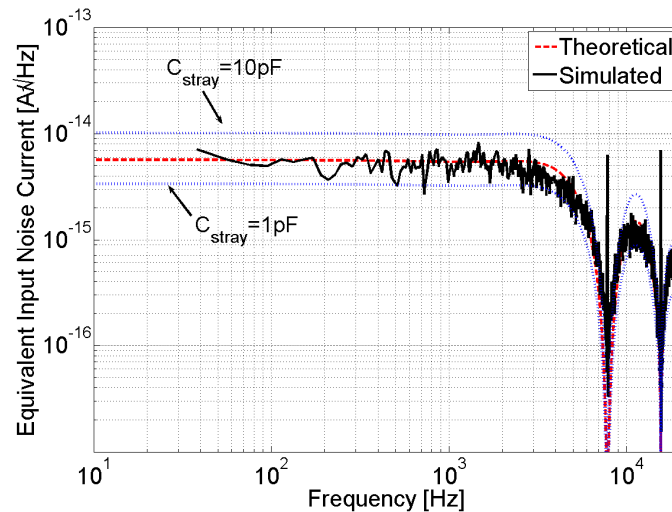


Fig. 21 – Input-referred equivalent noise: SPECTRE® simulated (solid black line) versus model using different input capacitances (dashed lines). The best fit is given with  $C_{stray} = 3\text{pF}$  [Cresc10].

Main curves shown in Fig. 21 are made using a 3pF stray capacitance. The figure shows a good fitting of the theoretical values with the simulated ones and highlights the strong dependency of the noise floor on the input stray capacitance.

## Layout design and ASIC fabrication

The silicon layout design of the ASIC is realized by the Cadence™ tool software, using the AustriaMicroSystems 0.35 $\mu\text{m}$  CMOS process toolkit. Starting from the electric scheme, the layout design follows two main steps, that are the DRC (Design Rules Check) and the LVS (Layout Versus Schematics) procedures. The LVS procedure is a methodology (Fig. 22) of design that starts from a circuit schematic, exports all the components (N-Mos, P-Mos and capacitors) and the netlist from the schematics view to the layout silicon view, then assists the layout designer during the routing of the netlist, respecting the design rules of the CMOS process technology selected. Finally it extracts the parameters from the layout process, and with them it reconstructs the scheme, to compare with the starting one, also considering the parasitic effects.

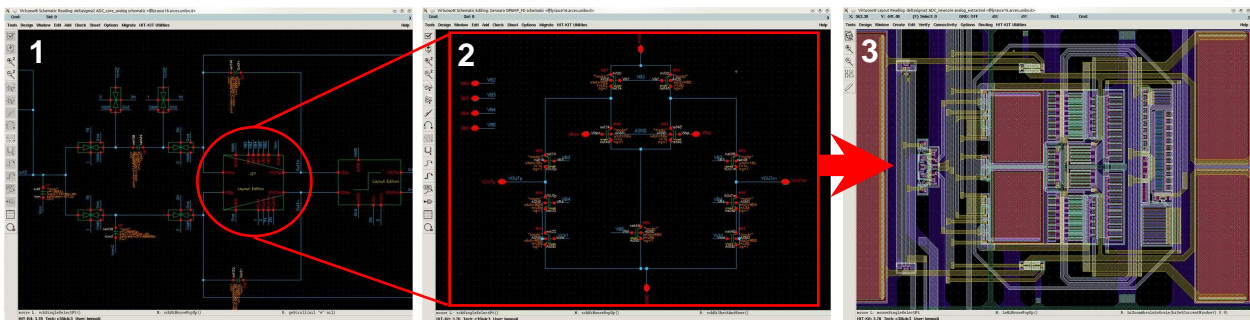
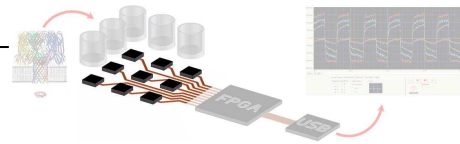


Fig. 22 – Cadence layout design process: from the general schematic (1) to a component detail (2) to the equivalent layout (3).

The sketch of the layout chip follows the top-down approach, based on the topcell hierarchy, where a single topcell could contain various cells, every of them corresponds to a piece of layout. Mixing analog and digital circuits on the same layout require special attentions with respect to the digital noise that can pair off between the analog components, and require more guard rings and the large gaps between them.

The AMS CMOS C35B4 process technology is a foundry process with 0.35  $\mu\text{m}$  minimum gate width, 4 metal layers, PolySi – Insulation - PolySi capacitors and PolySi Resistors. A wafer cross section, indicating all the layers, is shown in Fig. 23.

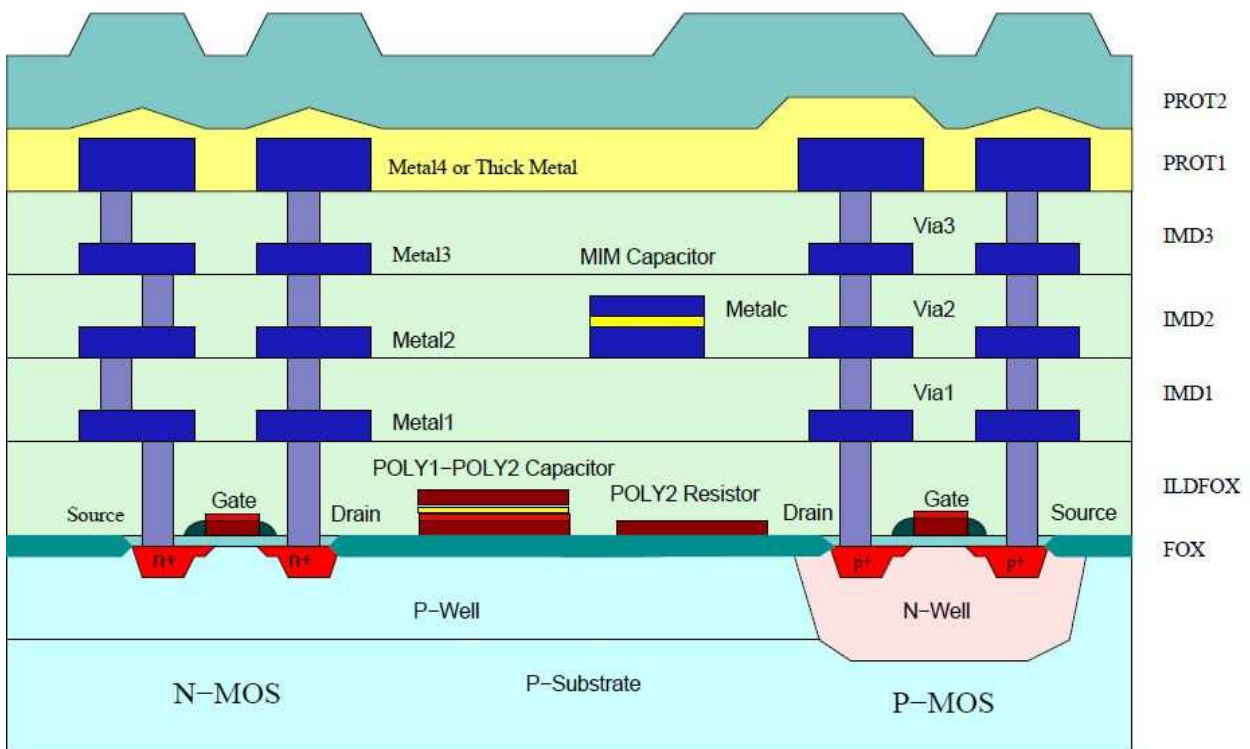
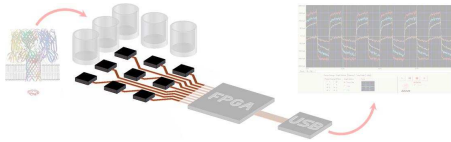


Fig. 23 – Wafer cross section of AustriaMicroSystem C35B4C3 technology process.



The final ASIC layout, illustrated in Fig. 24, was submitted to a Multi Project Wafer (MPW) run through the Europractice IC consortium on March 2008, to realize a first prototype of the chip.

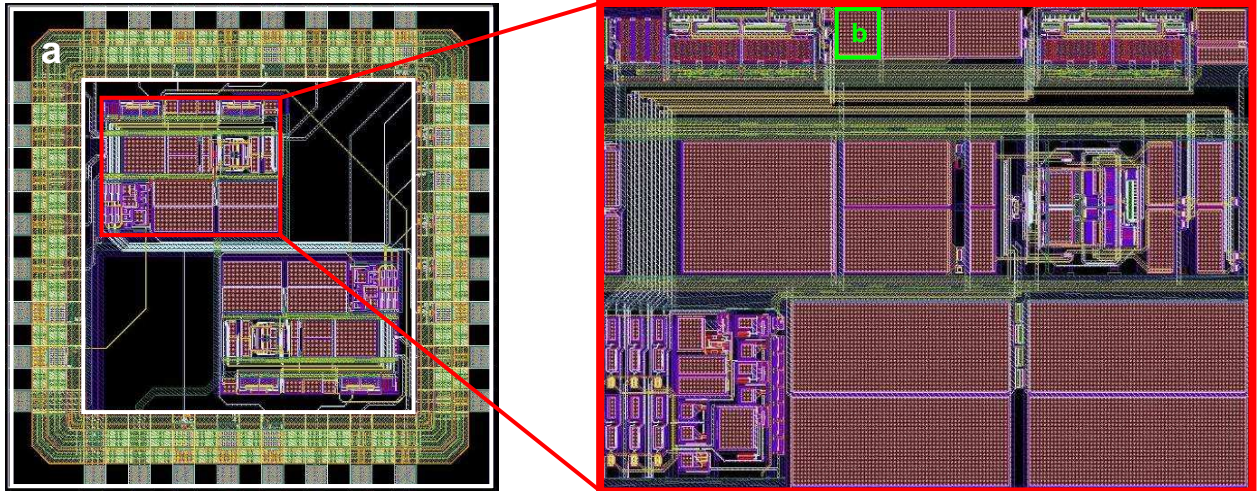


Fig. 24 – ASIC Cadence Layout: inside a 32 pins ringpad (a), two  $\Delta\Sigma$  ADC cores are placed, with the only difference in the feedback input stage capacitance (b), 100fF and 50 fF respectively.

### Chip measurement and characterization

A prototype is fabricated using a 2P4M 0.35 $\mu\text{m}$  CMOS process and a chip photograph showing the main blocks is shown in Fig. 25. The amplifier occupies 0.5mm<sup>2</sup> and the power consumption is below 23mW at 3.3V as supply. The chip have been packaged in a QFN32 case

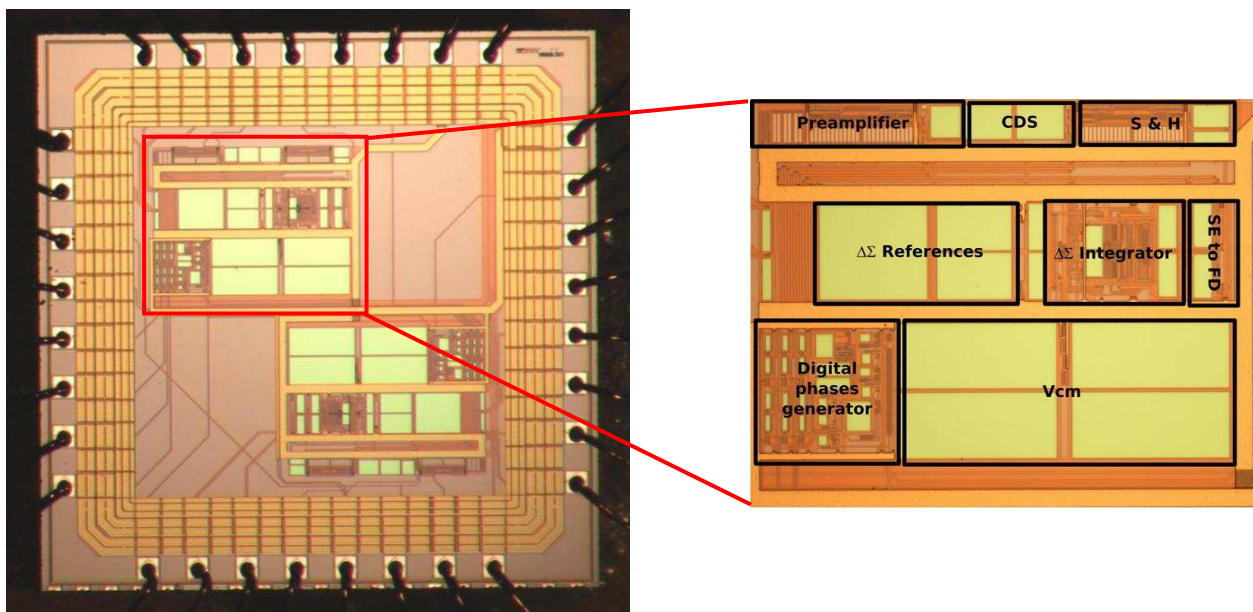
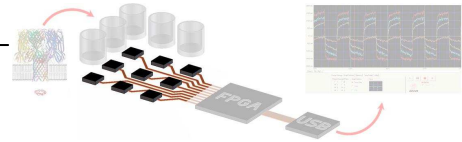


Fig. 25 – Chip microphotograph. The core area measures 0.83x0.62mm<sup>2</sup>. To note that most of the area is occupied by capacitors (large rectangles) for reducing substrate noise and reference interferences.



and placed in a testing printed circuit board, to make all the chip measurements and characterization, and afterwards directly interfaced with a microfluidic structure [Thei10] to sense single molecule events by means of ion channel current acquisition (see Chapter 4). A pin out description and the package characteristics are reported in Appendix (see Fig. 97, Fig. 98 and Tab. 6). The 1-bit delta sigma output stream is digitally elaborated to be stored and displayed by means of a numerical filtering system and a graphical user interface specifically designed, explained in the next Chapter 3.

The program is designed to change the readout bandwidth, from 0.5 kHz to 4 kHz by means of OSR. This is particularly useful since it can be performed in real-time during the acquisition process so as to balance the best signal-to-noise-ratio with respect to signal bandwidth. Stored data can be further analyzed for event counting and statistics using Matlab<sup>®</sup> algorithms.

### **Noise and distortion measurements**

Input-referred current noise on zero-signal input is shown in Fig. 26, where the theoretical expected curve is compared directly with the measured data of the chip prototype. The best fit is obtained using a 3pF stray capacitance, which is in a good agreement with typical input pad and pin capacitance. The two bumps at the right end of the graph are probably due to digital signals alias. The plot shows a reduction of the flicker noise due to the CDS scheme. The low-frequency noise is about  $5\text{fA}/\sqrt{\text{Hz}}$  at room temperature. Even if noise performance of our system is still worse than that of dedicated instrumentation, noise model has indicated the way to make substantial improvements in our architecture in a future release of the chip to compete with state-of-the-art instrumentation.

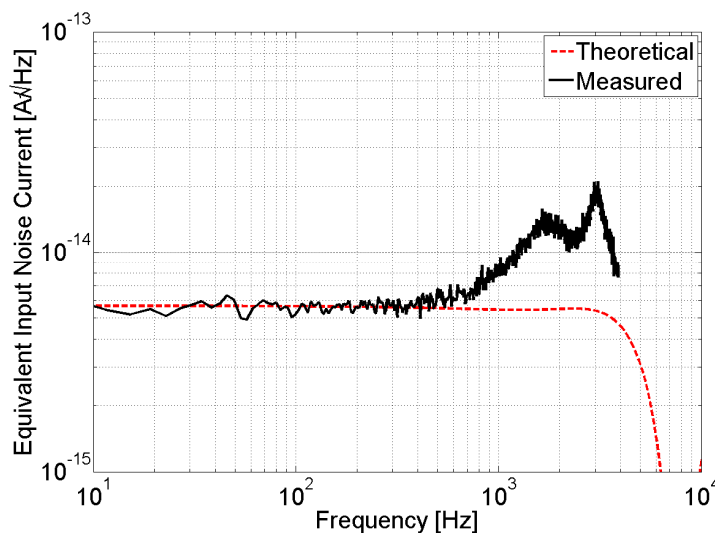
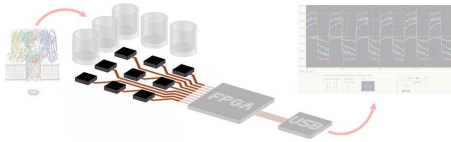


Fig. 26 – Measured input referred current noise (solid black line) compared with model (dashed red line) using 3pF of input stray capacitance.



Even if distortion is not crucial for the application, Fig. 27 plots the nonlinearity error of the amplifier in the 200pA and 5nA ranges.

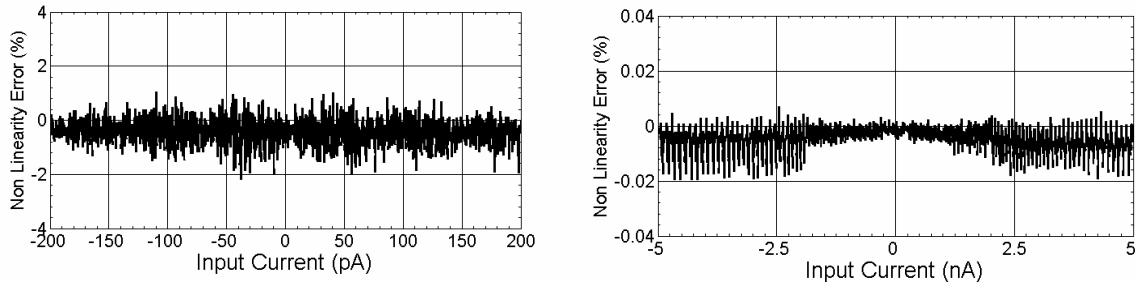


Fig. 27 – Non linearity error for 200pA scale range and 5nA scale range.

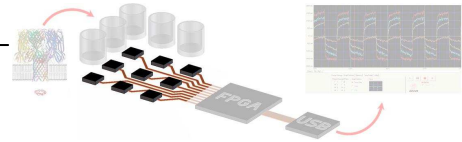
## Testing setup

To run the chip measurements and characterization, a PCB board is design to do a completely set of tests on the ASIC, to verify all it's parts and to analyze the maximum performance about noise and bandwidth during signals acquisition. To verify all the function separately of the chip and bypassing possible errors in the layout design, the board implements the support circuitry to substitute the internal chip biasing, voltage references and timing/phasing circuits. It's possible to use the board in different ways, in particularly:

- standalone chip mode: the chip is only supplied with the mains power, and operate with self biasing and timing circuits, at the fixed clock frequency of 1MHz;
- core chip mode: to check separately all the internals part of the chip, especially the bias and timing circuits, with the possibility to provide all this signals by externals generators (implemented on the PCB).

The first case correspond to the typical usage of the chip in an acquisition configuration, instead the second gives the possibility to obtain an improvement in the performance and sample rate. The mains features of the board are:

- a socket with 32 contacts for a small pcb boards (21x21mm) on which ones soldering the QFN32 chip package;
- two 3,3 V voltage regulator, to split the digital from the analogic power supply of the chip;
- two resistor voltage divider, to provide the  $V_{cm}$  (1,65 Volt) to the chip;
- two current bias network to provide the 100 $\mu$ A to the chip;
- a controlled-current test output circuitry, achieved by 1G  $\Omega$  resistor supplied by a remote PC controlled voltage;



- a fully scalable clock and phase digitally generator, to overclock the chip from the actual programmed sample rate to rise the bandwidth;
- a 15 pins D connector to interface the readout system box with the numerical elaboration unit.

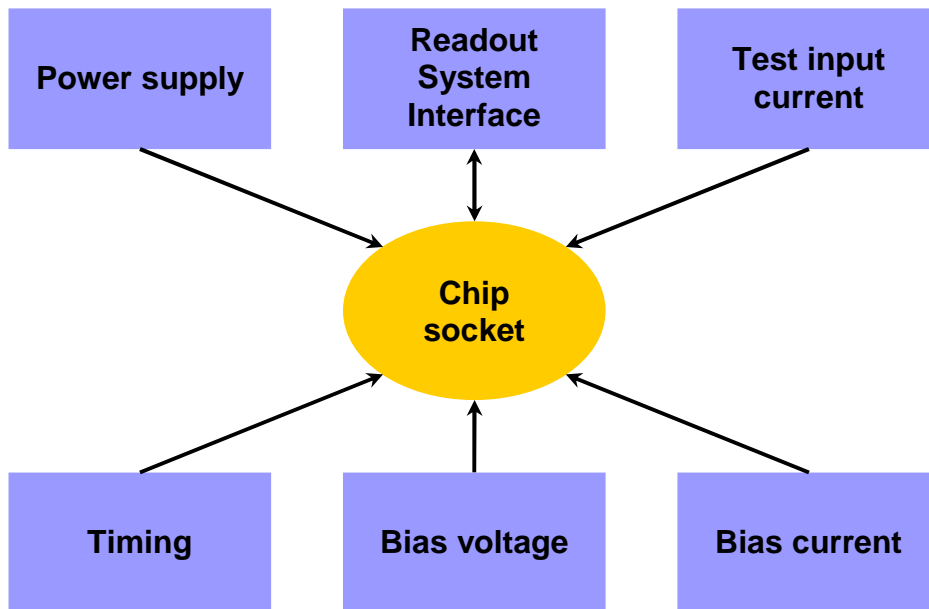
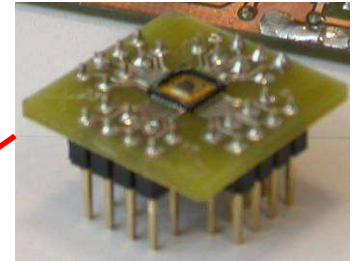
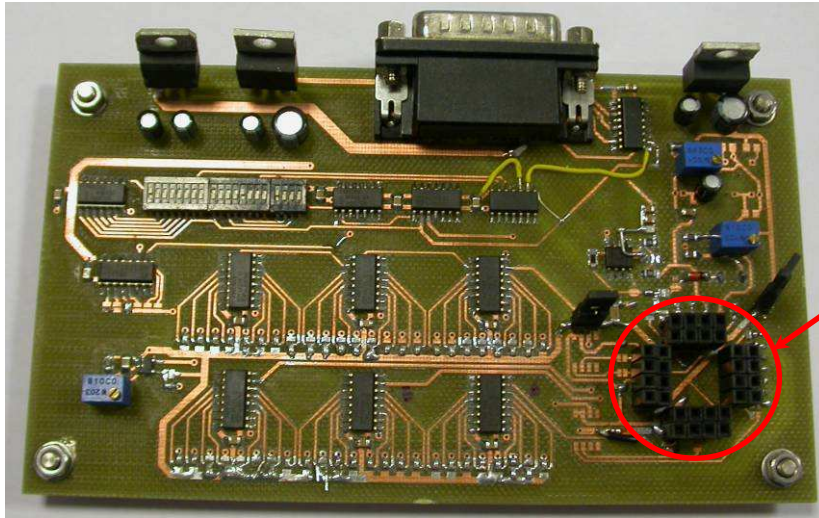
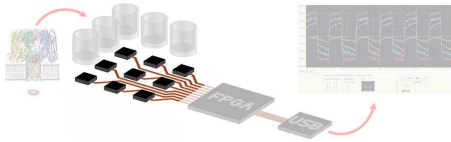


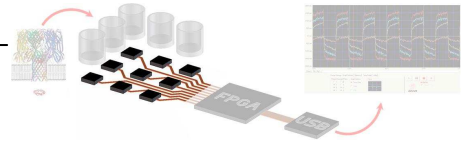
Fig. 28 – ChipTest PCB board block diagram.

The first simplest way to use the board is the standalone Chip mode. In this mode of functioning, the chip is directly interfaced with the readout system, and it work on a sample rate of 1MHz. It is very important to pay attention with the range of the input test applied current signal. The chip have two delta sigma converters, called A and B. The only difference between these two cores is in the feedback capacitor ( $C_f$ ) of the input charge sense amplifier, described in the section “Delta Sigma ADC converter and Low noise front-end” of this chapter. The core A present an input range of  $\pm 5$  nA, thanks to a feedback capacitor of 100fF, instead the B core input range, that is 2,5 nA by means of an half input feedback capacitor. The inputs pads are respectly the A and B points on the PCB, whose scheme is presented in appendix (Fig. 99). No others signals or generators are required from board to work in this conditions, it bring all the necessary information from the connection with the readout system.



**Chip socket**

*Fig. 29 – Photographe of ChipTest board and the chip socket where to plug different ASICS.*





# Chapter 3

## Digital Architectures

### Introduction

One of the main advantages offered by the Delta Sigma analog to digital converters is the one bit data output, a single digital line that transfer, at the oversampling rate, the data streaming of the converted input analog signals. In a multi path architecture, where each acquisition channel is interfaced with a dedicated analog to digital converter, the one bit data output allows a simple routing of the system, and the possibility to reduce the final dimensions of the platform.

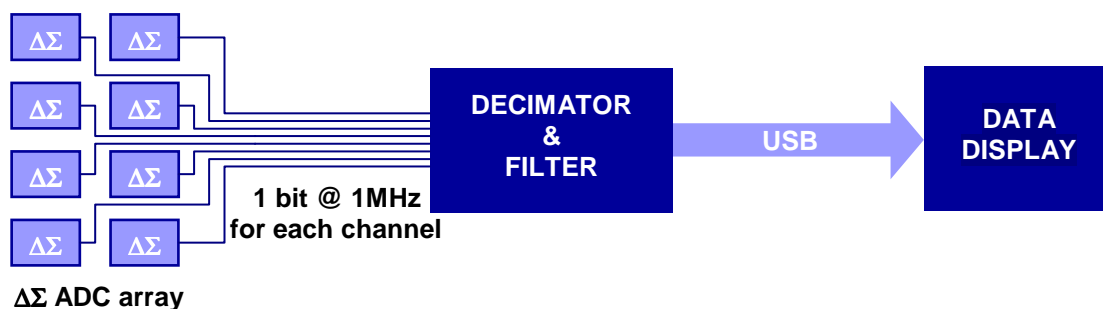
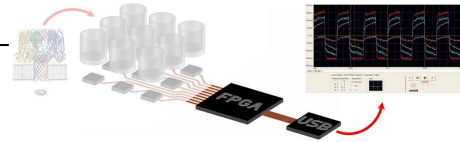


Fig. 30 – Digital elaboration chain. A single bit data output of each Delta Sigma converter is routed to a filtering and decimation unit for data processing, to recover data at the required bandwidth and resolution in terms of bit. Afterwards, data are send through a USB data channel to a host PC, for data display and storage.

To recover data at the Nyquist rate and at the required resolution, in terms of bits, the one bit data output of each Delta Sigma converter is down converted by a digital elaboration system, using a decimation and a filtering process. In a first instance, the numerical elaboration system was implemented using a Digital Signal Processing (DPS) because a limited number of data channels were concurrently acquired, so a firmware approach was used to run the digital process. Afterwards, to increase the capability in terms of simultaneously data channels acquired, a Field Programmable Gate Array (FPGA) was chosen, thanks to the powerful of the hardware computational resources offered from these chip family. On this new platform, a flexible and fully scalable architecture for the decimation and filtering process was implemented, thinking to a real parallel approach.

The digital architecture also include the interface for the data transfer from the acquiring platform to a Personal Computer, as well as the remote signal controls for the selection of the



acquiring parameters, like the current range or the bandwidth. In a first approach, an high speed serial RS232 was chosen, that was enough to transfer up to a small number of concurrently acquired data channels to a Labview software interface. To reach the array request, in terms of simultaneously data channels acquired, the serial link was substituted by a USB 2.0 full speed interface, and a custom Graphical User Interface was written in Visual Basic.

## Digital data elaboration

As already mentioned in Chapter 2, for quantitative resistive pulse sensing experiments, the signal bandwidth and the signal resolution, in terms of bit, must be sufficient to resolve fully the resistive pulses [Kriebel03] [Ke06] [NehSak95] otherwise the data may be inaccurate. Ensuring a high signal bandwidth increases the information content and accuracy of the recordings in terms of minimum time resolution, however also strongly increases the noise of the current recordings (Fig. 16 a) and lower the amplitude signal resolution. Vice versa, at low bandwidth, the noise is limited by the filtering and the amplitude signal resolution rise. A trade-off between signal-to-noise ratio and the signal resolution, in terms of bits, determine the final signal bandwidth required from the nanopores sensitivity because the amplitude of a resistive pulse must be above the noise and above the minimum acquisition time interval to be detectable [Sun00] [Mitsui04].

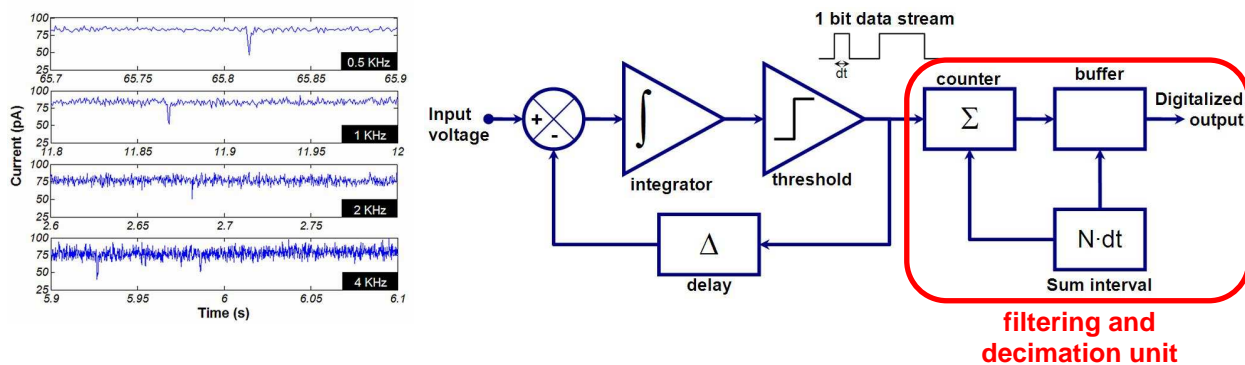
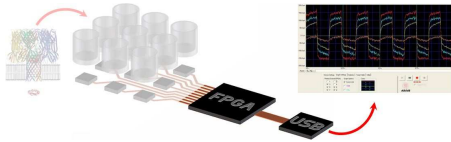


Fig. 31 – Resistive pulses can be detected with respect to the noise floor using narrower bandwidths. The Delta Sigma converter, thanks to the selectable ratio between the input sampling frequency and the output data rate ( $OSR = F_{in}/F_{out}$ ), offer the trade-off for the signal to noise ratio required for the specific signal.

A key aspect offered by the Delta Sigma oversampling converters is the speed/resolution trade-off. In fact, the filtering process inserted after the modulator not only filters the whole sampled signal in the band of interest (cutting the noise at higher frequencies), but also reduces



the frequency of the oversampled signal increasing its resolution in terms of bit. This is obtained by a sort of averaging of the higher data rate bit stream.

## Quantization and Delta Sigma Noise shaping

To convert a continuous time analog signal into a digital one, two operations need to be performed: sampling the analog signal (usually with a constant sampling period  $T$ ) and quantizing its amplitude so that it assumes one of a finite number of allowable values [Schreier05]. Quantization is usually uniform, so that any two adjacent quantized values differ by a fixed level spacing  $\Delta V$ . The device carrying out the quantization is called a quantizer, or ideal A/D converter. It is assumed to be a memoryless nonlinear device completely defined by static input/output characteristics reported in Fig. 32 [Schreier05].

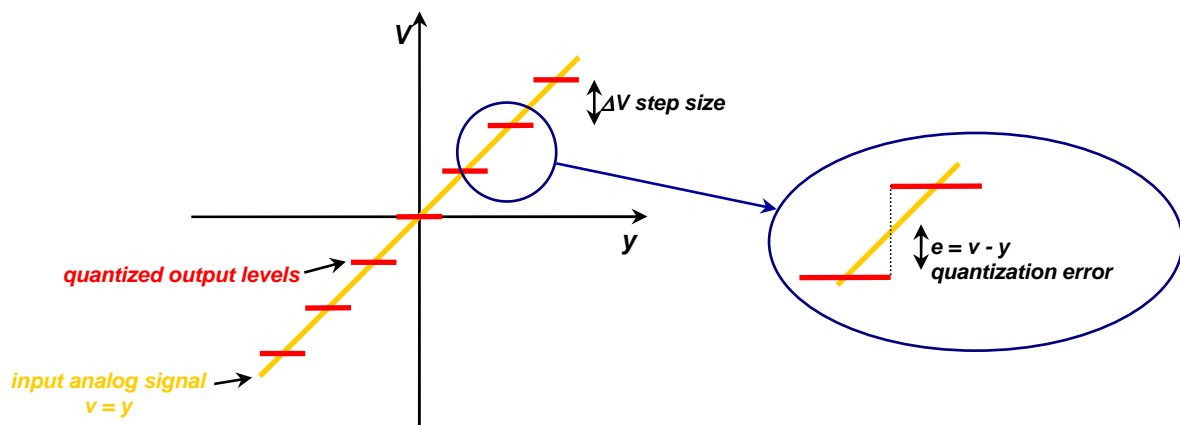
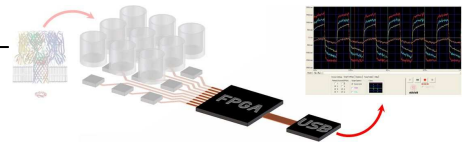


Fig. 32 – Quantization transfer curve (red levels) of an analog signal  $v$  (yellow). Evidential of the quantization error.

The difference between the quantized value and the input analog signal ( $v$ ) is called quantization error  $e$ , or quantization noise. The ideal quantizer is a deterministic device;  $v$ , and hence also the error  $e$ , are fully determined by the input  $y$ . However, if  $y$  stays within the input range of the quantizer, and changes by sufficiently large amounts from sample to sample so that its position within a quantization interval is essentially random, then it is permissible to assume that  $e$  is a with noise process with samples uniformly distributed between  $-\Delta/2$  and  $+\Delta/2$  [Schreier05]. In this case, the root mean square value of this quantization noise is

$$e_{rms} = \sqrt{\frac{1}{\Delta} \int_{-\Delta/2}^{+\Delta/2} e^2 de} = \frac{\Delta}{2\sqrt{3}} \quad (3)$$



This “noise” is simply added to the scaled input to give the output  $v = y + e$ . The Delta Sigma converter introduces a noise shaping on the input sampled signal, that consist in the increasing of the signal to noise ratio into the signal bandwidth by altering the spectral shape of the error that is introduced by dithering and quantization such that the noise power is at a lower level in frequency bands at which noise is perceived to be more undesirable and at a correspondingly higher level in bands where it is perceived to be less undesirable.

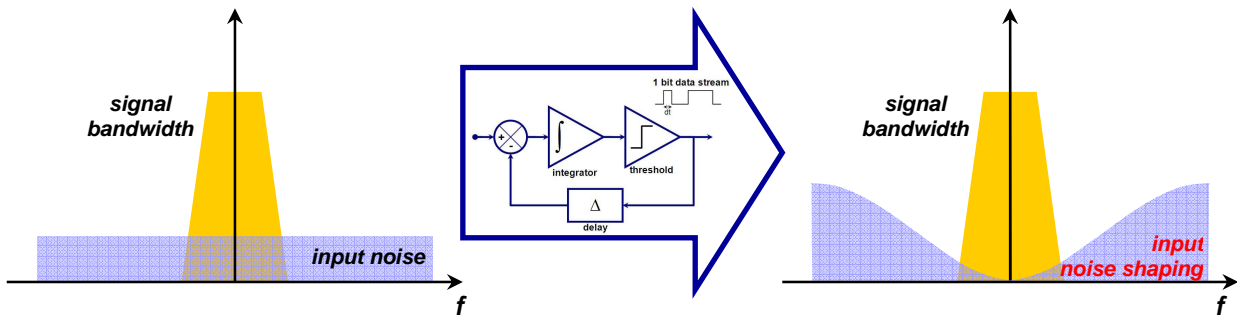
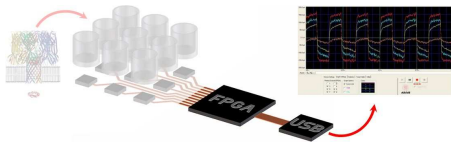


Fig. 33 – Noise shaping effect due to the Delta Sigma modulator: the input noise, including the quantization noise, is modelled at the delta sigma output. To note that the data information displayed in the graph on right is the one bit data stream.

Noise shaping works by inserting the quantization error in the feedback loop. Any feedback loop functions as a filter, so by creating a feedback loop for the error itself, the error can be filtered as desired. The simplest example would be

$$y[n] = x[n] - e[n - 1] \tag{4}$$

where  $y$  is the outbound sample value that has to be quantized,  $x$  is the inbound sample value,  $n$  is the sample number, and  $e$  is the quantization error made at sample  $n$  (error when quantizing  $y[n]$ ). This formula can also be read: the outbound sample is equal to the inbound sample plus the quantization error on previous sample. Essentially, when any sample's bit depth is reduced, the quantization error between the rounded (truncated) value and the original value is measured and stored. That "error value" is then added to the next sample prior to its quantization. The effect here is that the quantization error itself (and not the valid signal) is put into a feedback loop. This simple example gives a single-pole filter (a first-order Butterworth filter), or a filter that rolls off 6 dB per octave. The cutoff frequency of the filter can be controlled by the amount of the error from the previous sample that is fed back. Noise shaping must also always involve an appropriate amount of dither within the process itself so as to prevent determinable and correlated errors to the signal itself. If dither is not used then noise shaping effectively functions merely as distortion shaping - pushing the distortion energy around to



different frequency bands, but it is still distortion. If dither is added to the process as then the quantization error truly becomes noise, and the process indeed yields noise shaping.

## Decimation and Filtering

As shown in Fig. 33, the output signal contains very little quantization noise at low frequencies, but the power spectral density of the delta sigma modulator output noise grows rapidly with increasing frequencies, surpassing also the input white input quantization noise. Hence, the out of signal band noise must be removed by a digital low-pass filter (LPF). Afterwards, the LPF's output signal may be also decimated, to reduce the input oversampling one bit data rate to the final Nyquist bandwidth [Schreier05].

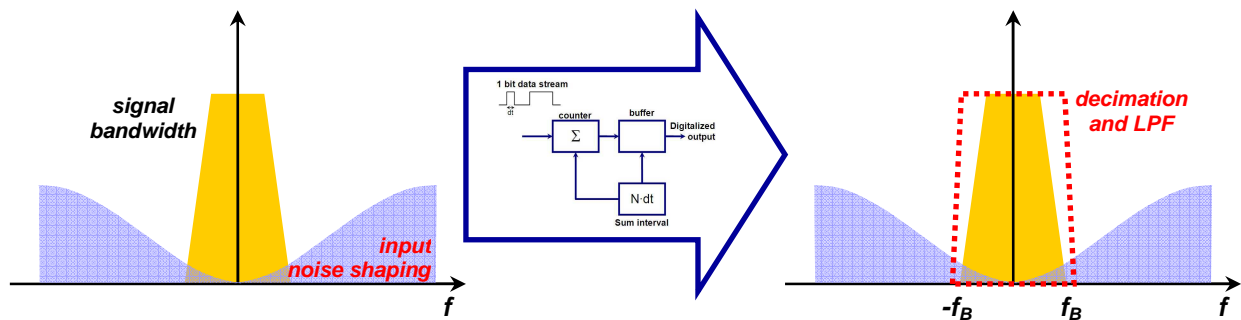


Fig. 34 – Noise shaping effect due to the Delta Sigma modulator: the input noise, including the quantization noise, is modelled at the delta sigma output.

The requirements on the LPF parameters are that its gain response be flat and large over the signal band  $[0, f_B]$ , and very small outside the bandwidth. It is also desirable to have a flat group delay response in the signal band. These conditions can be satisfied by using a linear-phase finite-impulse response (FIR) LPF [Oppenheim89]. A FIR filter (Fig. 35) is a type of digital

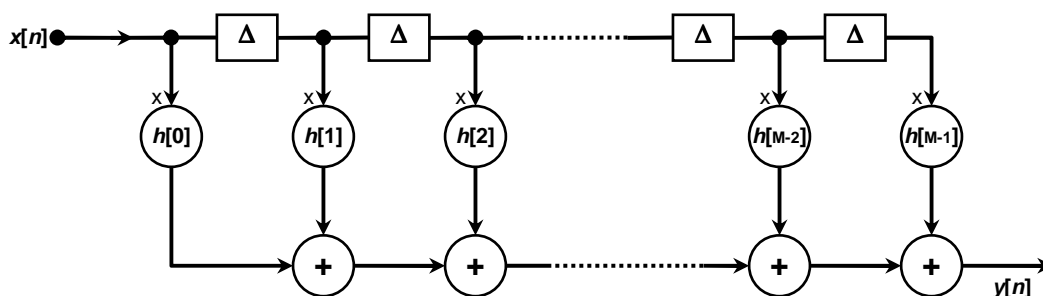
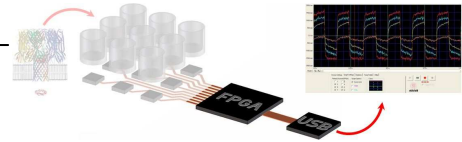


Fig. 35 – Flow graph representation of a convolution sum through a Finite Impulse Response (FIR) filter. The input samples  $x[n]$  are delayed by fixed time steps and multiplied by the filter taps,  $h[n]$ . The progress of the delay/multiplied results are added in sequence, to obtain the final result,  $y[n]$ .



filter, presenting a finite impulse response because it settles to zero in a finite number of sample intervals [Oppenheim89]. In FIR filtering process, the input samples  $x[n]$  are delayed by fixed time steps and multiplied by the filter coefficients,  $h[n]$ . The progress of the delay/multiplied results are added in sequence, to obtain the final result,  $y[n]$ .

The FIR filter is also an implementation of the *convolution sum*: if  $x[n]$  is an N point signal running from 0 to N-1, and  $h[n]$  is a M coefficient set (from  $h[0]$  to  $h[M-1]$ ), the convolution  $y[n] = x[n] * h[n]$  of the two signals is an N+M-1 point signal running from 0 to N+M-2, given by:

$$y(n) = h(n) * x(n) = \sum_{i=0}^{M-1} h(i) \cdot x(n - i) \tag{5}$$

This equation is called the *convolution sum*. It allows each point in the output signal to be calculated independently of all other points in the output signal. The index  $n$ , determines which sample in the output signal is being calculated

Since the output signal of the Delta Sigma converter is a single bit data stream, it may be practical to use a single-stage high-order linear-phase FIR filter, since there are no actual multiplications required between the samples of the signal and the FIR coefficients [Schreier05]. However, it is usually more efficient and economical to implement the filtering and decimation process in stages, to avoid too long high order FIR filters. The implemented architecture is based on two stages, which transforms the digital Delta Sigma output from a 1-bit stream, occurring at the oversampling rate  $F_{in}$ , to the output data at the Nyquist rate depending on the OSR by the relation  $F_N = F_{in} / OSR$ .

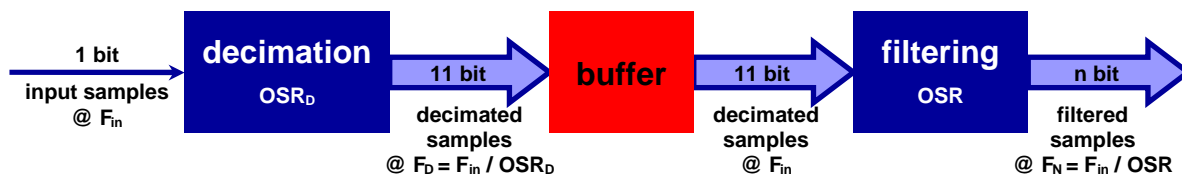
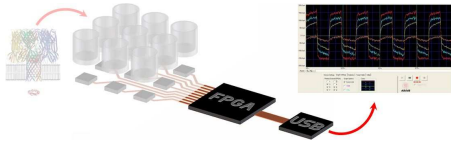


Fig. 36 – Filtering and decimation stages related to the OSR, or else the final required bandwidth, and the output resolution in terms of bit. It is more efficient to implement the filtering architecture into two stage instead then a single LPF, since it would require a too long elaboration process (i.e. too many filter coefficients) to obtain the same output characteristics of the two stages architecture.

The first stage decimate the one bit data input to the output data at 11 bit at the rate of is  $F_D = F_{in} / OSR_D$ . The decimation process consists into a running data average, performed each  $OSR_D$  input samples. The data produced by the decimator are stored into a buffer, from which they are taken at the  $F_{in}$  rate to be filtered by the next block, the filtering, by a convolution sum actuated each  $n=OSR$  data samples, resulting in an output bandwidth  $F_N = F_{in} / OSR$ .



The system presents up to five possible  $OSR$ , which determine the input signal bandwidth, the output data rate, and the output data resolution, in terms of equivalent bit. The relations between  $OSR$  and performances are reported in

Tab. 5, calculated from the real input oversample frequency, that is 1MHz. The equivalence between the signal to noise ratio and the data output resolution, in terms of bit, for a generic delta sigma ADC is:

$$SNR_{dB} = 6.02 B + 1.76 + 10 \log_{10} \frac{2L+1}{\pi^{2L}} + 3.01(2L+1) \log_2 OSR \quad (6)$$

where  $L$  is the delta sigma order and  $B$  is the number of bit of the quantizer. For a first order delta sigma, eq. 6 became

$$SNR_{dB} = 2.61 + 9.03 \log_2 OSR \quad (7)$$

Hence, the resolution, in terms of equivalents bit is

$$n \text{ bit} \cong 0.4 + 1.5 \log_2 OSR \quad (8)$$

$OSR$	64	128	256	512	1024
$OSR_D$	32	32	32	32	32
Resolution n. bit	9	10	12	13	14
Signal rate [Hz]	15625	7812	3906	1953	976
Bandwidth [Hz]	7800	3900	1950	970	485

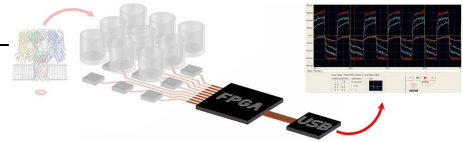
Tab. 5 –  $OSR$  relation vs. bandwidth, output data rate and resolution in terms of bit, calculated from an input oversampling frequency of 1MHz and through eq. 8.

## Decimation

The decimation process is a running average of the one bit data input, calculated each  $N$  samples. It is possible to represent the average computation by

$$w(n) = \frac{1}{N} \sum_{i=0}^{N-1} x(n-i) \quad (9)$$

where  $N$  is the number of input samples,  $x(n-i)$  is the  $i^{\text{th}}$  input sample and  $w(n)$  is the mean value. In the time domain, it is possible to represent this function as a rectangular transfer function, where the amplitude is one and the length is equal to  $N \cdot dt$ . In the frequency domain, the equivalent function is represented by the *sinc* function [Proakis], and the same mean data could be obtained by the convolution between the signal spectrum and the *sinc* function, as indicated in Fig. 37. It is important to find out how much residual noise remains at the output of



the *sinc* filter when it is used to suppress the shaped quantization noise, as well as the mean value calculation as decimator filter [Schreier05].

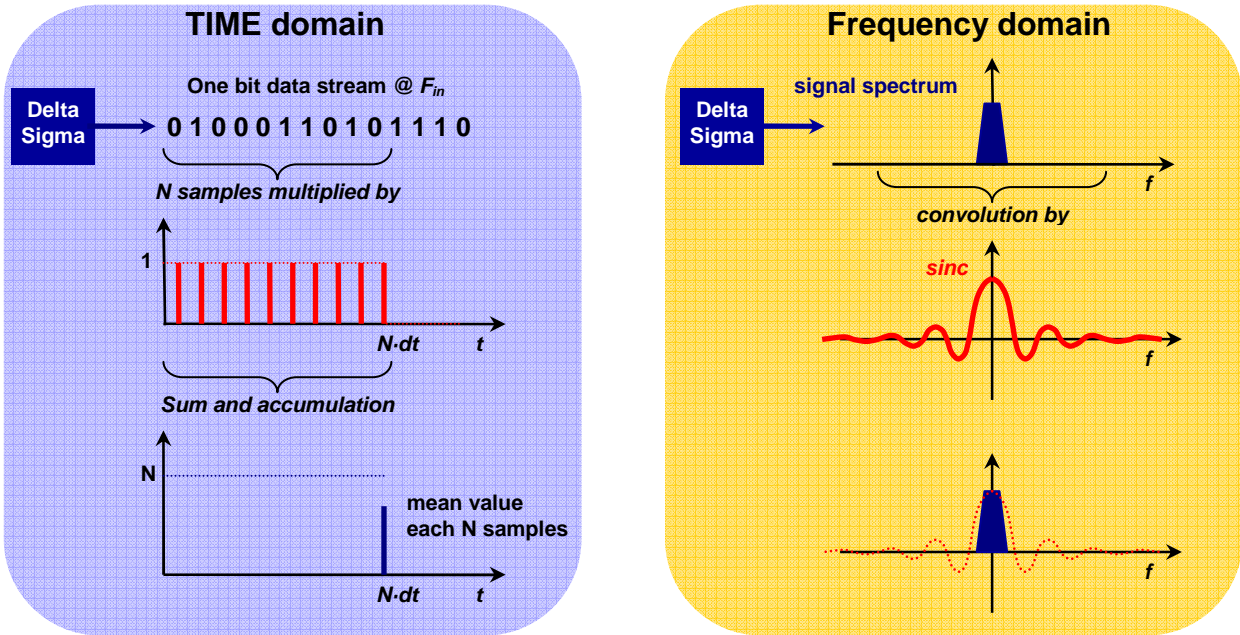


Fig. 37 – Decimation process in the time and frequency domain.

In the time domain, the noise at the output of the *sinc* filter is

$$q(n) = \frac{1}{N} [e(n) - e(n-N)] \tag{10}$$

Assuming  $e(n)$  and  $e(n-N)$  are uncorrelated, and that each has an rms value  $e_{rms}^2$ , the quantization noise power at the output of the *sinc* filter is [Schreier05]

$$q_{rms}^2 = \frac{2 e_{rms}^2}{N^2} \tag{11}$$

The output noise power for an ideal LPF with unit gain at  $f=0$  is

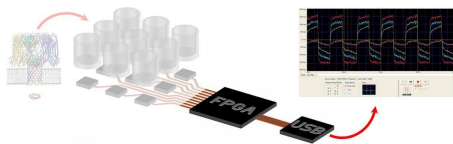
$$q_{rms}^2 = \frac{\pi^2 e_{rms}^2}{3 N^3} \tag{12}$$

Thus, it is clear that the *sinc* filter is nearly  $N$  times less effective than the ideal LPF. Hence, the *sinc* filter is seldom used as a complete decimation filter. To reduce the residual quantization noise, a known technique is the cascading two *sinc* filters, resulting in the so-called *sinc*<sup>2</sup> filter. In the time domain, eq. 10 became, for a *sinc*<sup>2</sup> filter [Schreier05]

$$q(n) = \frac{1}{N^2} \sum_{i=0}^{N-1} [e(n-i) - e(n-N-i)] \tag{13}$$

If  $e$  is white noise of power  $e_{rms}^2$ , the power of the quantization noise at the output of the *sinc*<sup>2</sup> filter is





$$q_{rms}^2 = \frac{2 e_{rms}^2}{N^3} \quad (14)$$

Comparing  $q_{rms}^2$  for the  $\text{sinc}^2$  to the  $\text{sinc}$ , there is a gain factor of  $N$  times in the signal to noise ration, due to the  $N^3$  vs.  $N^2$  denominator in the eq. 11 and 14.

The impulse response (or frequency transfer function) of the  $\text{sinc}^2$  filter is obtained by convolving the rectangular impulse response of the  $\text{sinc}$  filter with itself, resulting in a triangular shape made by  $2N$  steps [Schreier05].

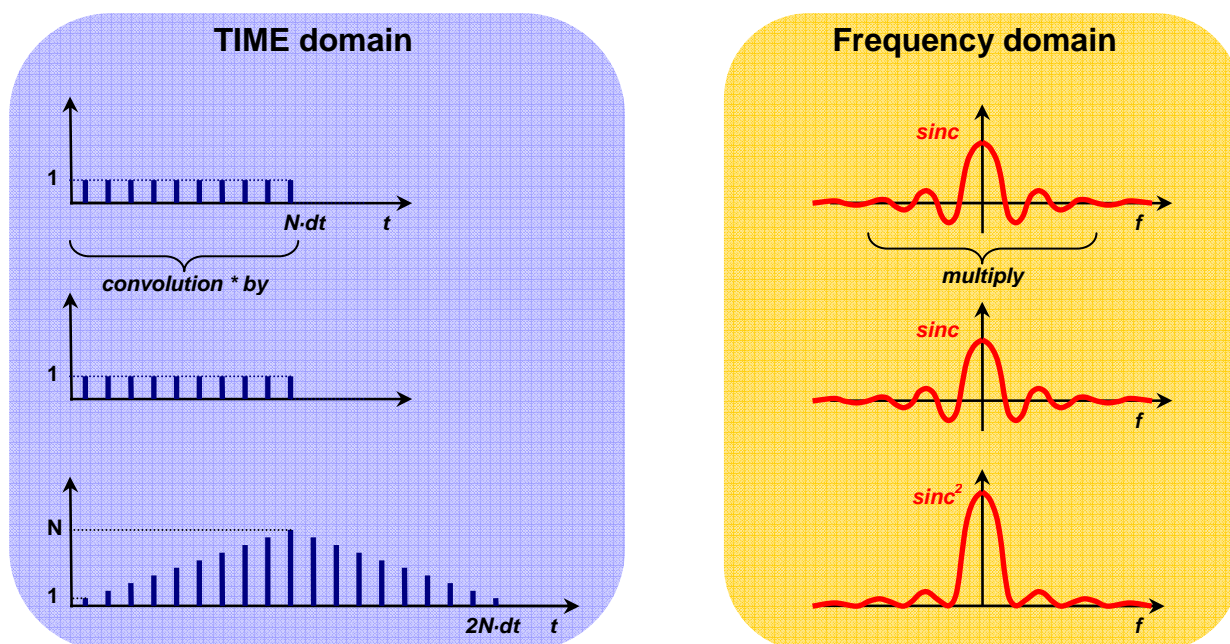


Fig. 38 – Impulse response (or frequency transfer function) of the  $\text{sinc}^2$  filter, obtained by convolving the rectangular impulse response of the  $\text{sinc}$  filter with itself, resulting in a triangular shape [Schreier05].

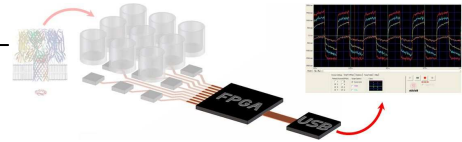
## Filtering

The second block of the two-stages architecture is a LPF FIR, designed with a *Kaiser* function window that allow to obtain a good trade off between the transition bandwidth and the stop-band attenuation, and reduces the non-ideality as the ripple in the bandpass, the non zero bandwidth in the transition band, limiting the stop-band attenuation [Oppenheim89].

The Kaiser window is defined as

$$w(n) = \frac{I_0 \left[ \beta \sqrt{1 - (1 - 2n/N)^2} \right]}{I_0(\beta)}, \quad 0 \leq n \leq N-1 \quad (15)$$

where  $I_0(\beta)$  is the modified zero-order Bessel function of the first kind,  $N$  the length (order) of the filter and  $\beta$  is the shape parameter which determines the rate between the main-lobe width



for the transition bandwidth and the side-lobe peak level in the stop-band. Empirical design formulas have also been derived by Kaiser for determining parameters  $\beta$  and  $N$ .

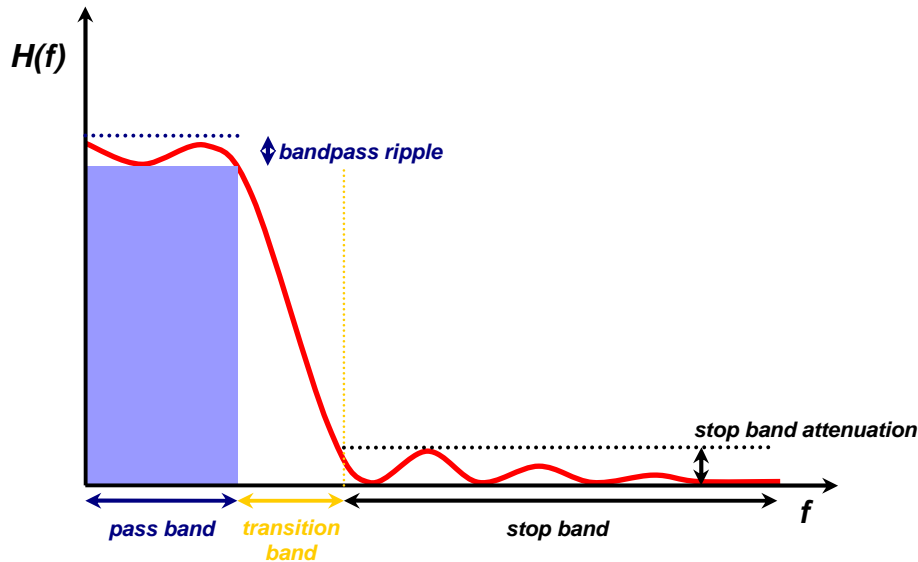


Fig. 39 – Frequency transfer function of a LPF filter with Kaiser window, with evidence of band pass, transition band and stop band, ripple in bandpass and attenuation in stop band.

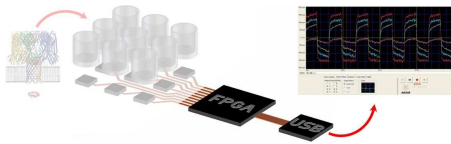
To achieve narrow transition bandwidth, high filter orders have to be used. Increasing the filter order, however, increases the computation time of the filtering process, since the filtering involves a convolution of the signal array with the filter array.

The LPF FIR filter can be realized by the convolution of the output signal of the first stage (the  $\text{sinc}^2$  output) with the impulse response of the LPF FIR filter with Kaiser window. The decimation of the signal can be achieved computing the output samples by the *convolution sum* once in every  $N = \text{OSR}$  clock cycles.

The LPF FIR filter coefficients  $h[n]$  (the tap weights) of the impulse response can be easily calculated by a simple Matlab implementation, through filter designer tool (like SPTool, FDATool), selecting the filter characteristics in order to maximize the stop-band attenuation (about 50dB) and minimize the transition bandwidth ( $< 10\%$  pass-band). The filter order was chosen equal to the total  $\text{OSR}-1$ . The LPF filter reduces also the data rate to the final Nyquist-rate, giving the final data resolution in terms of bit.

### **The final digital architecture**

Summarizing, the digital data elaboration of the one bit data stream produced as output from the delta sigma analog to digital converter is processed by a decimator and filtered, to reduce



the quantization noise, limiting the bandwidth and to reach the final data resolution, in terms of bit. The filtering chain, previously illustrated in Fig. 36, is here reported to explain a processing

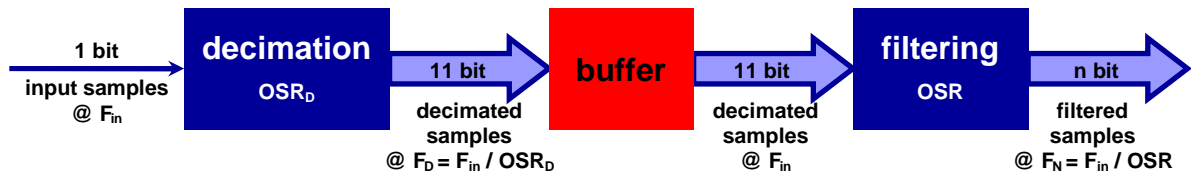


Fig. 40 – Filtering and decimation stages related to the OSR, or else the final required bandwidth, and the output resolution in terms of bit.

example of a one bit data stream. The design parameters are:

- $F_{in} = 1$  MHz (the input oversampling frequency, equal to the delta sigma output one bit data stream);
- OSR variable from 128 to 1024 (see
- Tab. 5);
- maximum data output resolution: 14 bit.

Because the digital elaboration chain is splitted into two parts, to avoid to long FIR filters, it is assumed to fix  $OSR_D$  equal to 32, so the  $sinc^2$  filter, that operates over  $2N$  samples, results long 64 steps. With this parameters, the data generated by the  $sinc^2$  filter is an average value, where the maximum possible value at the end of the average computation is given by

$$\sum_{N=1}^{32} N + (32 - N) = \sum_{N=1}^{32} 32 = 1024 \quad (16)$$

Since the one bit data output of the delta sigma can be 0 or 1, the average must be a value included between 0 and 1: for this reason, it is necessary to divide the final data output (at the filtering output) by a factor of 1024, like to right shift the data by 10 bits. The next picture shows an example of data flux of how the  $sinc^2$ , corresponding to the block *decimator* in Fig. 40, operates on one bit data input.

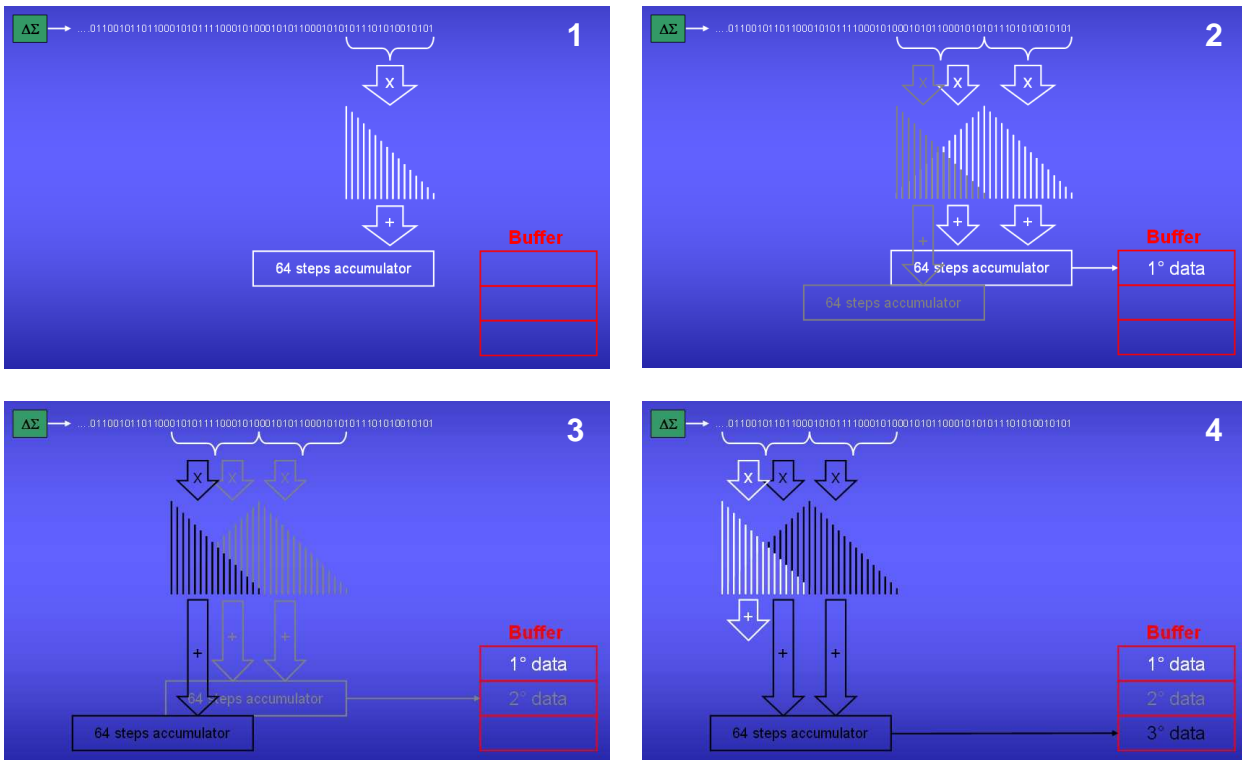
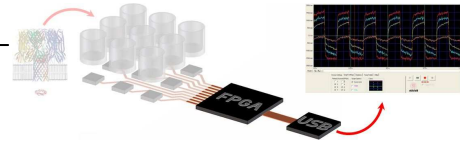


Fig. 41 –  $Sinc^2$  running average. Each bit of the one bit data stream output given by the delta sigma, is multiplied by two corresponding values of the  $sinc^2$  filter, one for the “rising” triangular ramp and one for the “lower” triangular ramp. Each multiplication is stored into an accumulator (1). The process restart every 32 input bits, so every 32 steps a filtered data, stored in the accumulator, is ready to be stored into a buffer (2). The process is a work as a loop (3-4), filling the buffer in a circular way, where the final length of the buffer is equal to OSR.

To maximize the 18 bit about the LPF coefficients and, simultaneously, adapt the output at the project request of 14 bit resolution, it is necessary to adapt the tap values at the maximum size of  $2^{18}$ , by multiplying the taps for a factor  $2^N$ , depending on the OSR selected. Also in this case, the final output must be divided by this factor, always by a right shifting of the final data.

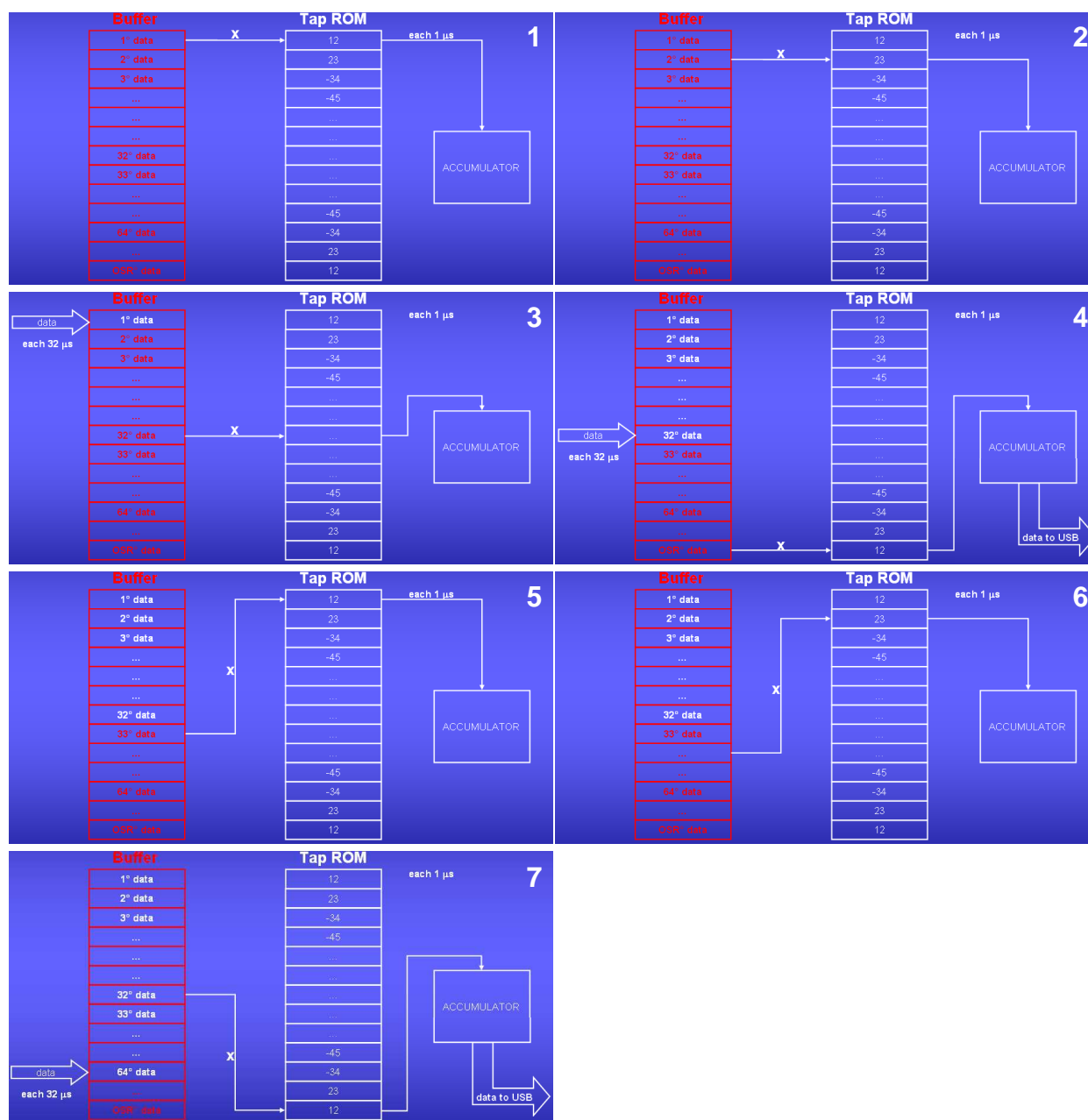
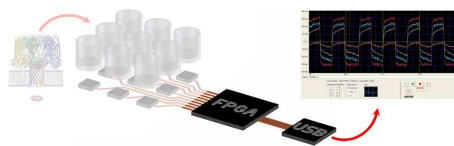
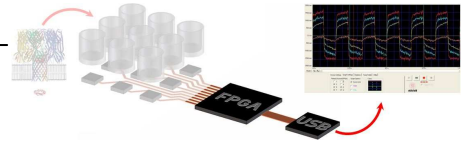


Fig. 42 – Filtering process. Data are taken from the (red) buffer at the rate of 1 MHz (every 1  $\mu$ s), and multiplied for the corresponding value of the Kaiser LPF filter (the tapROM) (slides 1-2), to be stored into a temporary accumulator. After 32 steps, a new data is written at the top of the buffer (slide 3). The process continues for all the length of the filter (equal to the OSR selected) filling the top positions of the buffer each 32 steps with new data; only at the last filter value, a data from the accumulator ended the filtering process, so it is ready to be sent via USB to be displayed (slide 4). The filtering process restart taking data from the 33<sup>rd</sup> position of the buffer (slide 5-6), and continues with the multiplying/accumulation process while the buffer is refilled starting from the 33<sup>rd</sup> position with new data, always every 32 steps.



## Digital Signal Processing approach

In a first instance, the digital elaboration process was implemented in a DSP board, that was an Orsys MicroLine® C6713CPU, with a 32 bit floating point DSP with a clock speed of 300 MHz by Texas Instruments TMS320C6713.

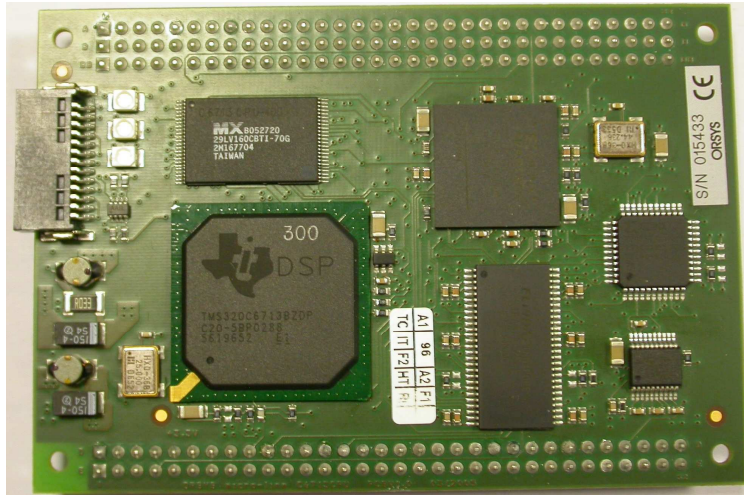


Fig. 43 – Orsis DSP board C6713CPU.

The main features of this board is the programming simplicity, because it has a RS232 interface to download directly and store permanently the applications into the 2 Mbyte on-board flash memory. Moreover, it has a fully digital addressable data bus, like a microcontroller, by specifics C++ code instructions.

The DSP clock speed is 300 MHz, so the maximum performance achievable is 6 concurrently channels filtered at 4 KHz of bandwidth for each channel.

The core of the application program was developed by other people during the Receptronics project, and basically it consist of a C++ implementation of a  $\text{Sinc}^2$  Fir filter that realize a running average and pre-decimation of the incoming data stream bit, followed by a low bandpass Fir filter, with selectable numbers of taps, according to the selected bandwidth. This core was first developed and debugged by the DSK TSM320C6713 starter kit of Texas Instruments, and later re-adapted to the specific Orsys hardware, plus all the implementation of the protocol to interface the USB FIFO FT245R chip for communication through the readout system and the PC.

An interface PCB (see BoardInt, Fig. 100) was also designed to plug the DSP board, and to allow the connection between the host PC and other acquisition boards hosting a single or an array of delta sigma asics.

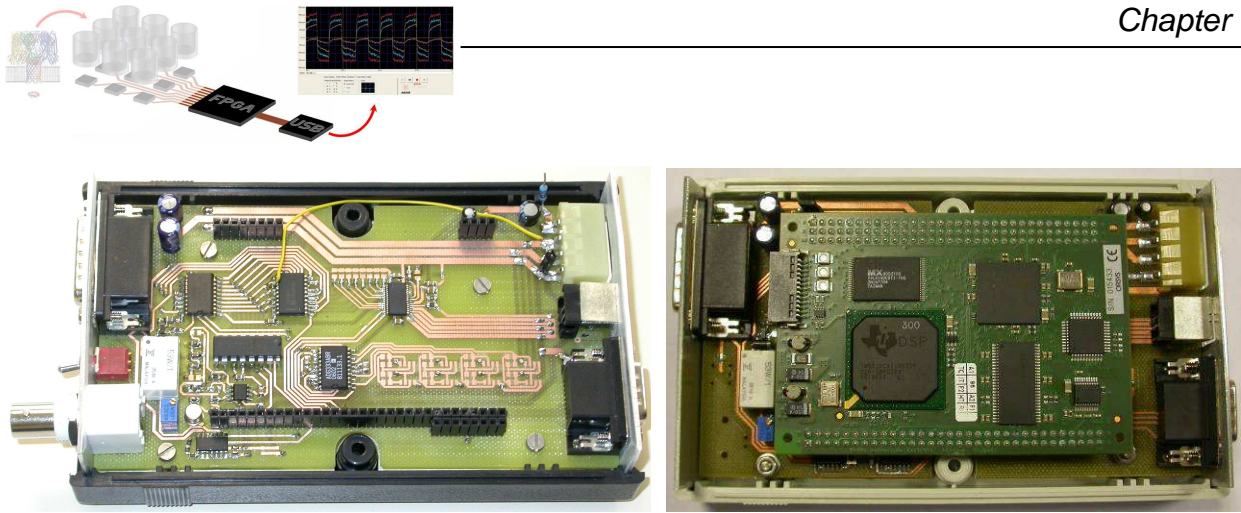


Fig. 44 – Orsis DSP board C6713CPU and BoardInt box.

## Labview Software interface

To display and store the data, a Labview software interface was designed in a first instance. Up to three data channel are concurrently displayed, and the interface allows to set remotely on the DSP board the OSR (so the acquisition bandwidth), variable from 0,5 to 4 kHz), two different ranges of the maximum input current, 200 pA or 5 nA.

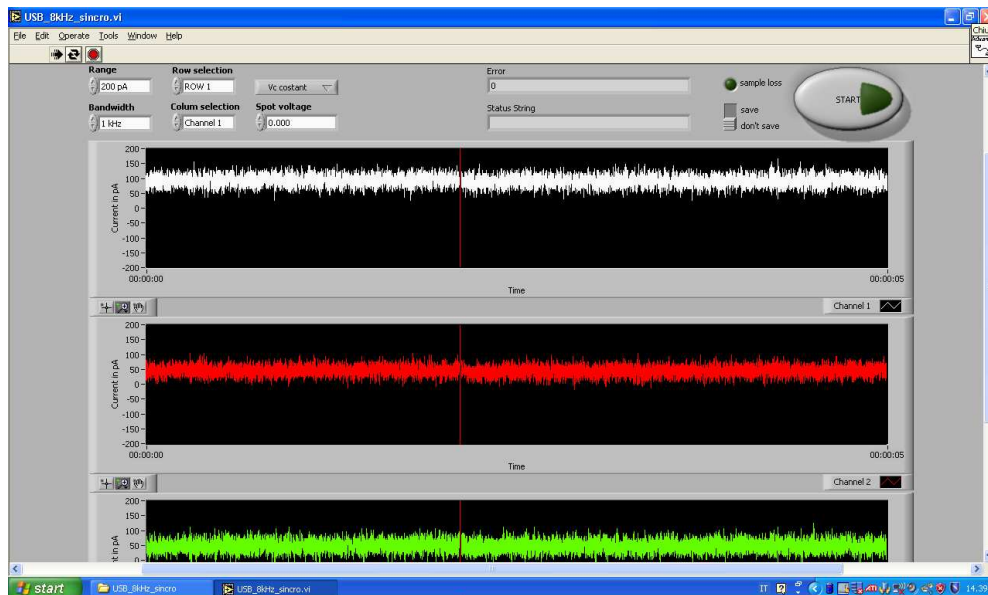
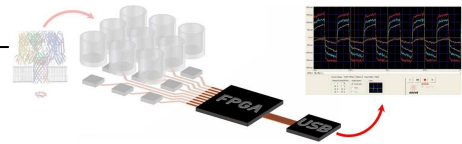


Fig. 45 – GUI Labview software interface.

## Field Programmable Gate Array approach

As shown in the previously section, the DSP approach is more suitable in the case of few data channels acquired concurrently. In the case of application were no hard algorithms have to be implemented, to increase the performance in terms of maximum bandwidth and number of simultaneously acquired channels, a FPGA approach is preferred.



The FPGA implementation requires to transform the computational blocks of the FIR filters previously exposed in an approach suitable for the FPGA architecture, based on hardware computational blocks, as distributed memory and multiplier.

The selected device is the DLP-FPGA module, from DLP Design manufactory [dlp]. It is a compact module ready to use, with a USB interface and a pin connection for signal in/output. Here the block diagram and the main features:

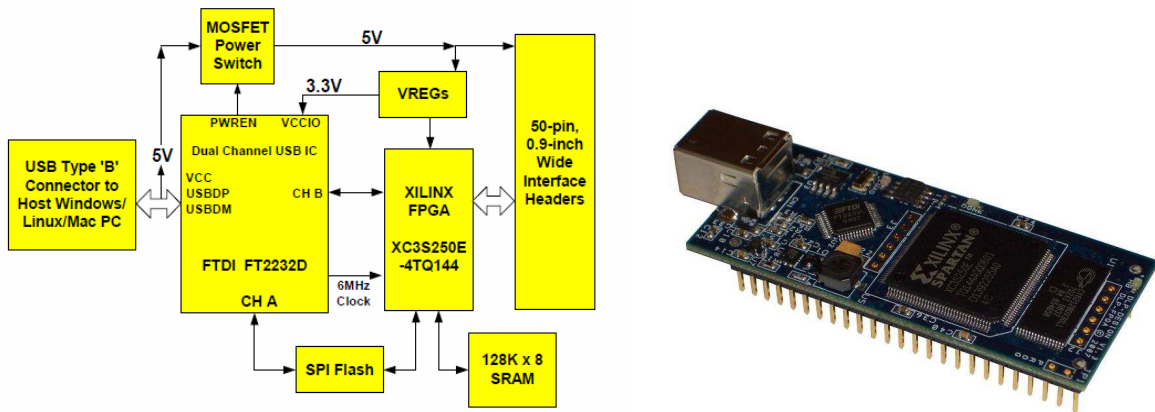


Fig. 46 – DLP-FPGA module [dlp].

- a FTDI FT2232D USB 2.0 full speed (12Mb/s) interface with 2 data ports and royalty free drivers;
- 250 kgate FPGA, 216 Kbit RAM (12x18 Kbit), 12 multipliers (18x18 bits), 4 DCMs clock resource;
- 40 I/O channels;
- SPI Flash for code download to self-programming;
- 128 KB SRAM;
- fully USB powered.

The development software tool is the ISE 10.1, provided by Xilinx, including all the simulation, mapping and routing tool to develop FPGA projects and create the .bit file ready for the FPGA initialization. DLP design offer the code downloader, through the USB, to the onboard SPI flash to initialize the FPGA.



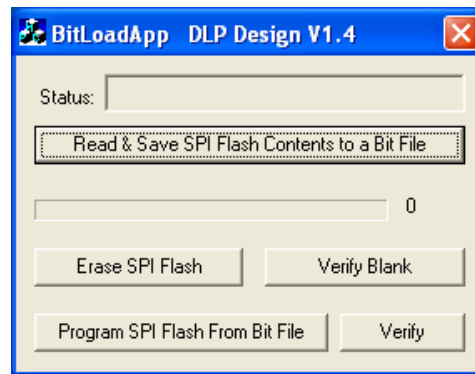
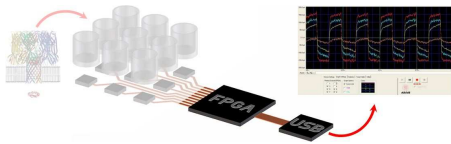


Fig. 47 – Bitload download application for DLP-FPGA module.

## USB interface Protocol

There are two protocols about the communications between the FPGA and the PC through the USB interface:

- 1 - the sample channels data streaming, incoming from the FPGA decimator filter of the one bit output data stream for each ADC converter to the PC;
- 2 - the control bytes, from the PC to the FPGA, to control the OSR sample rate, range, offset feedback correction, Vc source and amplitude.

1) The data flow incoming from the FPGA-USB interface is a streaming of byte. Each data sample from one single channel is represented by 14 bits, equivalent to 16.384 different values. The 14 bits are splitted in two bytes, each one have 7 bits, as shown below:

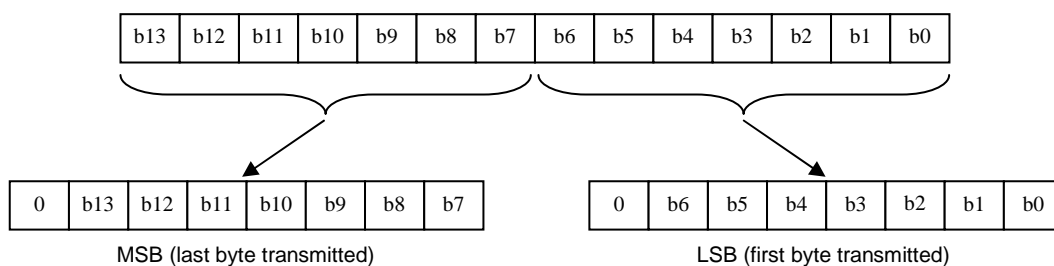
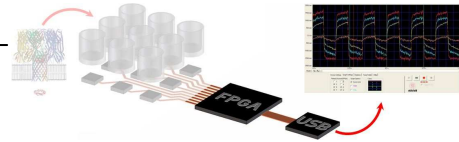


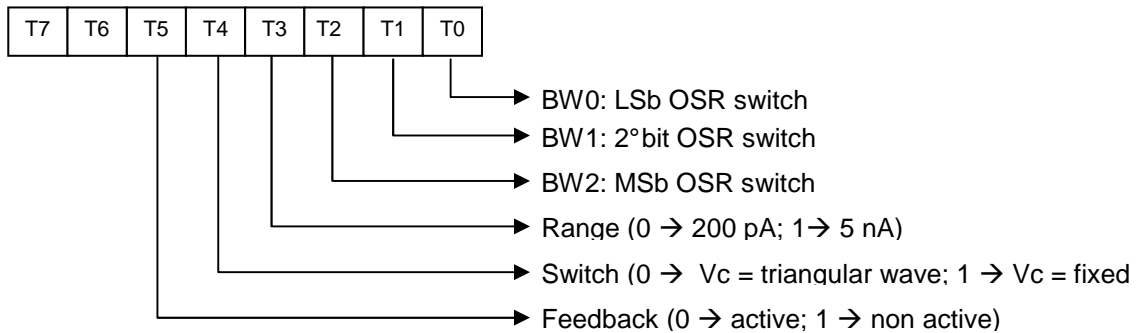
Fig. 48 – Data output format. The 14 bit data samples are splitted into two parts each of one of 7 bit.

The data flow from the channels is grouped into packets of 9 bytes, where the first byte is a synchronization byte (80h), followed by the data channels, from 1 to 8, where the first byte for each channel is the LSB byte followed by the MSB.

2) Control Bytes. There are three controls byte, sent from the PC to the FPGA, organized as follow:



- first byte (t\_data)



- second byte (s\_data): this byte select the Vc fixed voltage level, with the following scale. Each bit increment correspond to 1 mV voltage step.  
 00h → -128 mV  
 80h → 0 mV  
 FFh → +127 mV
- third byte (f\_data): future use

## FPGA implementation

The decimator and filtering application presents others specifics requirements, in addition to the main features described in the previously chapters. In particular, the need to handle the USB communication between the FPGA and the PC. As indicated in the protocol characteristics, it is possible to split the project into two branches, depending on the data flow direction from the PC and the FPGA. Moreover, the bidirectional USB interface allow to develop separately the two data flux, through a notice system integrated into the USB chip for incoming and out coming data. The first branch is the SETTING block, that stores all the data control bytes incoming from the PC, regarding the OSR and the RANGE selector. The second branch is the FILTERING block, that implement all the filtering and decimator processing for each Delta Sigma channel, and outputs a data streaming to the PC for the remote viewing.

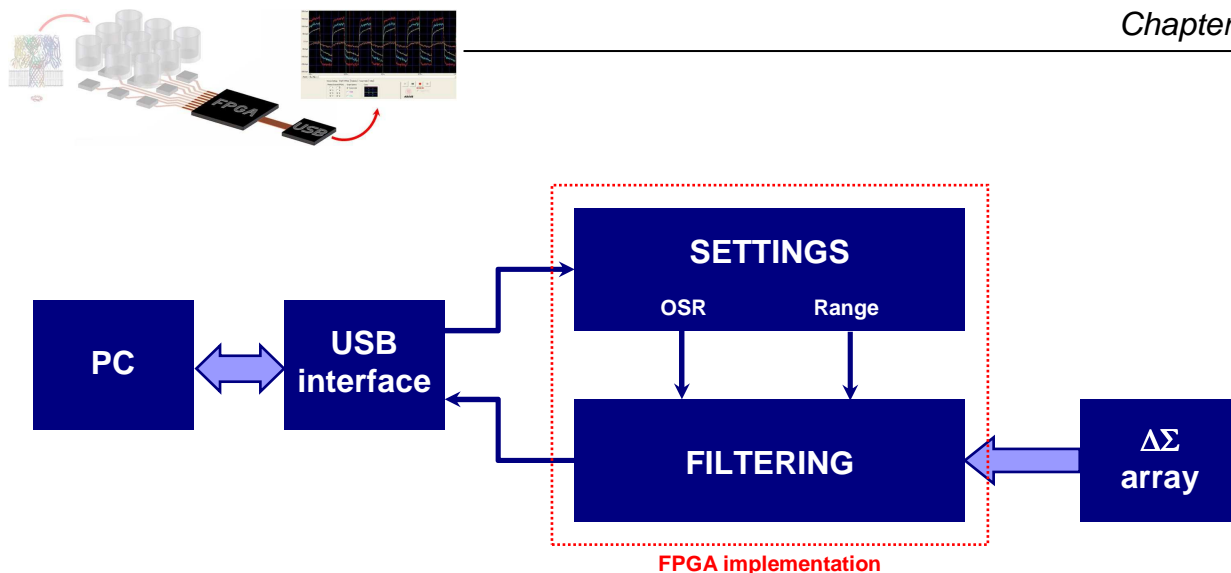


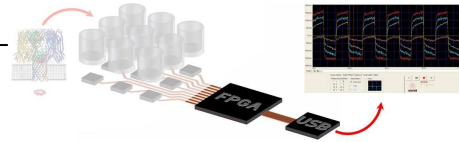
Fig. 49 – FPGA implementation approach – data exchange.

The USB Interface block of Fig. 49 consist in a USB transceiver chip, the FT2232D from FTDI. It interface directly the USB link integrating the handshake protocol, also contains two data ports (as FIFO buffers), used as input and output. The data are exchanged through a 8 bit data bus, with 4 control signals for reading and writing operation. The maximum data rate is 1MB for second, as indicated in the USB 2.0 full speed device (12Mb/s). All the software driver to develop GUI interfaces (Visual Basic, LabView, C++) are available from the manufactory company for free.

The implementation of the project in the chosen FPGA was realized by two design methods: the schematic approach and the VHDL approach. In particular, the schematic approach allow to optimize the performance minimizing the number of logic resources creating modules available in the VHDL environment, just by the block instantiation.

### **The *SETTING* block**

The SETTINGS block of Fig. 49 is the interface for the USB chip to read and store the control bytes specified in the paragraph *USB interface protocol*. It takes as input the 8 bit data bus of the USB chip and the relative control signal (RD# and RXF#), and outputs 4 control data group: the OSR switch (5 signals), the t\_byte, s\_byte and f\_byte, each of one must be stored until the next PC control request. Its design comes from the reading time diagram of the chip datasheet, reported in Fig. 50.



Document No.: FT\_000173  
 FT2232D DUAL USB TO SERIAL UART/FIFO IC Datasheet  
 Version 2.00  
 Clearance No.: FTDI# 127

**8.3 245 FIFO Mode Timing Diagram**

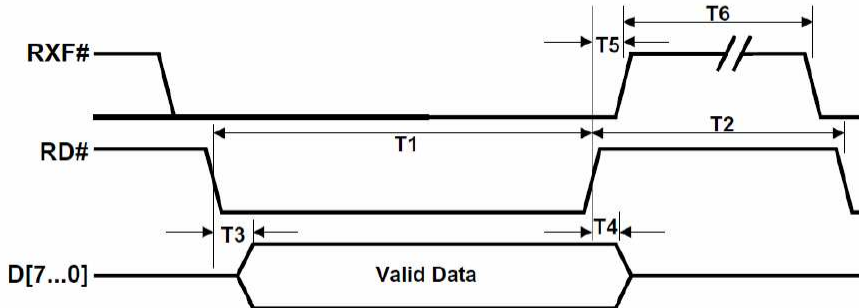


Fig. 50 – Reading time diagram for FTDI 2232D USB interface.

The data read process (Fig. 50) start when a valid data (one or more bytes) are sent from the PC to the USB interface, that acquire and store the data in the internal FIFO buffer. The notice of a data valid into the buffer is generated by the RXF# signal, which goes low and remains low until the buffer is completely emptied. To read the data, the logic has to put low the RD# signal, and then sampling the byte on the low-to-up RD# transition after a specific time delay. The read process continues until the RXF# signal back to up, indicating the total emptying of the buffer.

Since the protocol requires 3 control bytes, the SETTINGS block is realized by 3 cascade 8-bit latches, and the latch signal is generated by a combination of the master clock (@ 1MHz) and the RXF# signal.

**The FILTERING block**

The FILTERING block of Fig. 49 is the core of the application, because it includes 8 independent digital elaboration ways and the logic to interface on output the data stream towards the PC through the USB chip. It is design starting from the principles illustrated in Fig. 36, and the related description in paragraph *Decimation and Filtering*.

The block diagram of Fig. 51 is characterized by two mains kinds of blocks: some of this (the withe) are common for all the design because they provide to distribute signals shared between all the 8 elaboration channels, while the others (the gray) are replicated many times as the total number of the acquired channels. In particular, the common blocks are the filters (Sinc<sup>2</sup> and LPF) coefficients generator, the address generator for the circular buffer (the RAM) and the USB interface for data output.

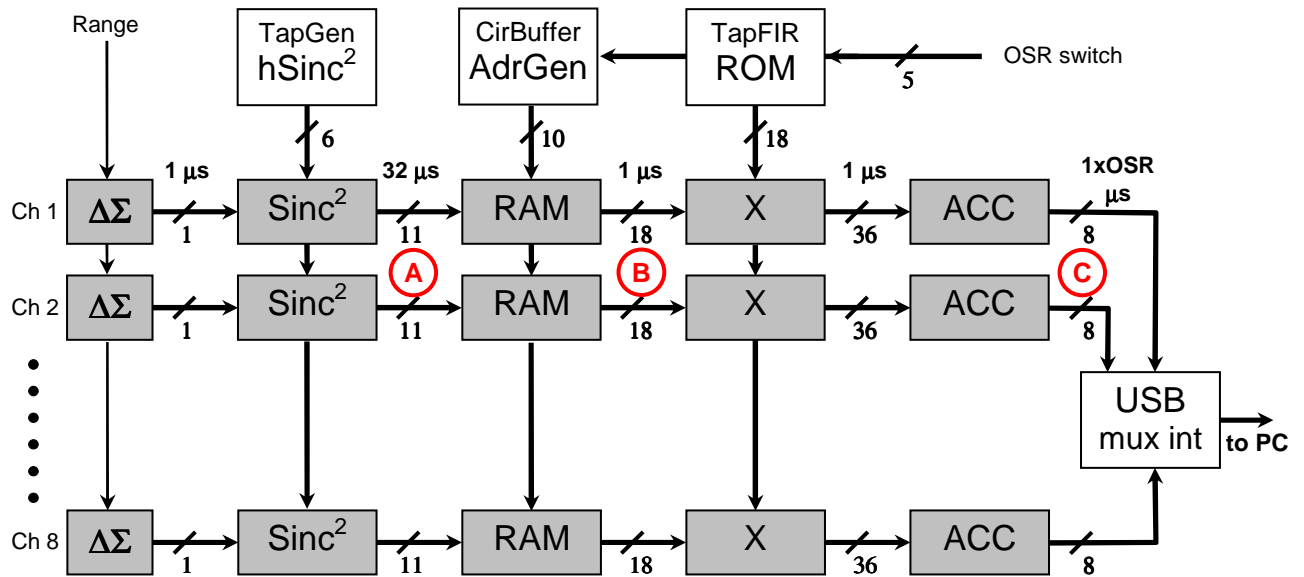
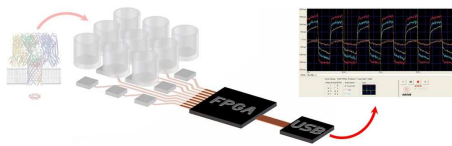


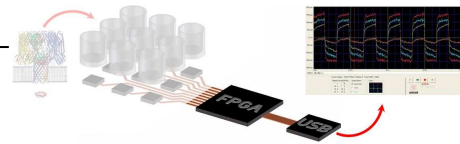
Fig. 51 – FPGA architecture for parallel data decimation.

Briefly, each Delta Sigma data input channel is sampled and multiplied by two different  $\text{Sinc}^2$  coefficients and stored into two separated accumulators. This first step happens at the rate of 1 MHz, and the total period of each accumulation process takes 64 clock periods, after which the new data is ready to be stored in a buffer and the accumulator is cleared. The two process are shifted by 32 clock periods (the one bit sample is multiplied by coefficient  $H_N$  and by coefficient  $H_{N+32}$ ), so the final output rate of the  $\text{Sinc}^2$  block (point A in Fig. 51) is  $1 / 32 \mu\text{s} = 31250 \text{ Hz}$ . This data are stored in a circular buffer of variable size, depending by the selected OSR. From this buffer (point B in Fig. 51), at the rate of 1 MHz, a data is taken and multiplied with a correspondent LPF coefficient, and the result is added in an accumulator. The LPF filtering process is long as the selected OSR, from 64 to 1024 clock periods, corresponding to a final data rate from 15625 Hz to 976 Hz of the accumulator data output (point C in Fig. 51). Finally, this data are multiplexed in the input data bus of the USB chip interface.

### ***hSinc<sup>2</sup> TapGen***

The  $h\text{Sinc}^2$  TapGen block of Fig. 51 is the  $\text{Sinc}^2$  coefficients generator. The purpose of this stage is to provide the correct coefficients for the input data multiplier, to obtain the average data each 32 input data samples. The  $\text{Sinc}^2$  filter born from the correlation, in the time domain, between two cascade Sinc filters, and it is possible to represent its coefficients as a triangular distribution along the time axis, as already illustrated in Fig. 38, Fig. 39 and Fig. 41.

The block generates two separately data flux output, each of one is a repetition of 64 coefficients, increasing from 1 to 32 and then decreasing to 0. The two data flux are shifted by



32 clock periods, and coming from a common binary counter (Q[0..14]), using the multiplexing each 32 clock periods between two different elaboration blocks, that are an adder (Q[1..4] + 1) and the inverted counter output signals (#Q[1..4]). The following time diagram show respectively the Q[0..14] outputs from the binary counter (T), the adder and inverters outputs and, finally, the two coefficient outputs, hSinc2u and hSinc2d.

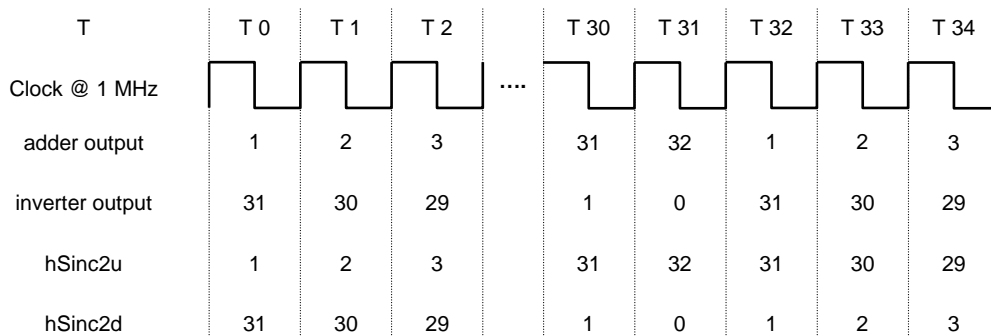


Fig. 52 – hSinc<sup>2</sup> tap time sequence generation.

There are also three signals generated inside the hSinc<sup>2</sup> TapGen block. They are the reset signals (rst\_Sinc2u and rst\_Sinc2d), to notice the last of the 64 coefficients cycle, one for each data flux (hSinc2u and hSinc2d), and the write signal (WR\_Sinc2) to store the average result in a buffer. The rst\_Sinc2u is active when Q[0..5] = 3Fh, that means that is active each T = 63 + n64, and rst\_Sinc2d is active when Q[0..5] = 1Fh, that means that is active each T = 31 + n64. The WR\_Sinc2 signal is active when Q[0..4] = 1Eh, that means that is active each T = 30 + n32.

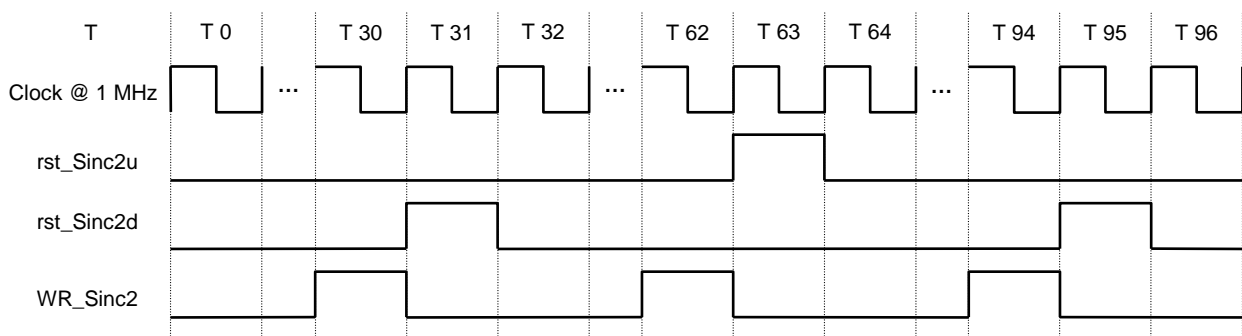
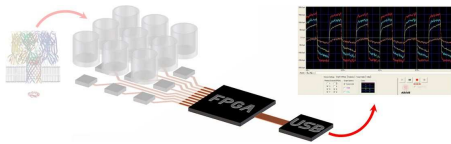


Fig. 53 – Reset signals for hSinc<sup>2</sup> tap block.

### TapFIR ROM

The *TapFIR ROM* block, underlined in Fig. 55, is the Low Pass Filter coefficients generator. It provide 5 different set of coefficients, depending on the OSR selection, from 64 to 1024. Each set of coefficients is symmetric with respect to the middle: for example, for the set



corresponding to ORS 64,  $H(0)$  is equal to  $H(63)$ ,  $H(1) = H(62)$ , ...  $H(31) = H(32)$ . This property allow to halve the final capacity of the ROM, that became of 32 positions, in the case of  $OSR = 64$ , just using a correct addressing system.

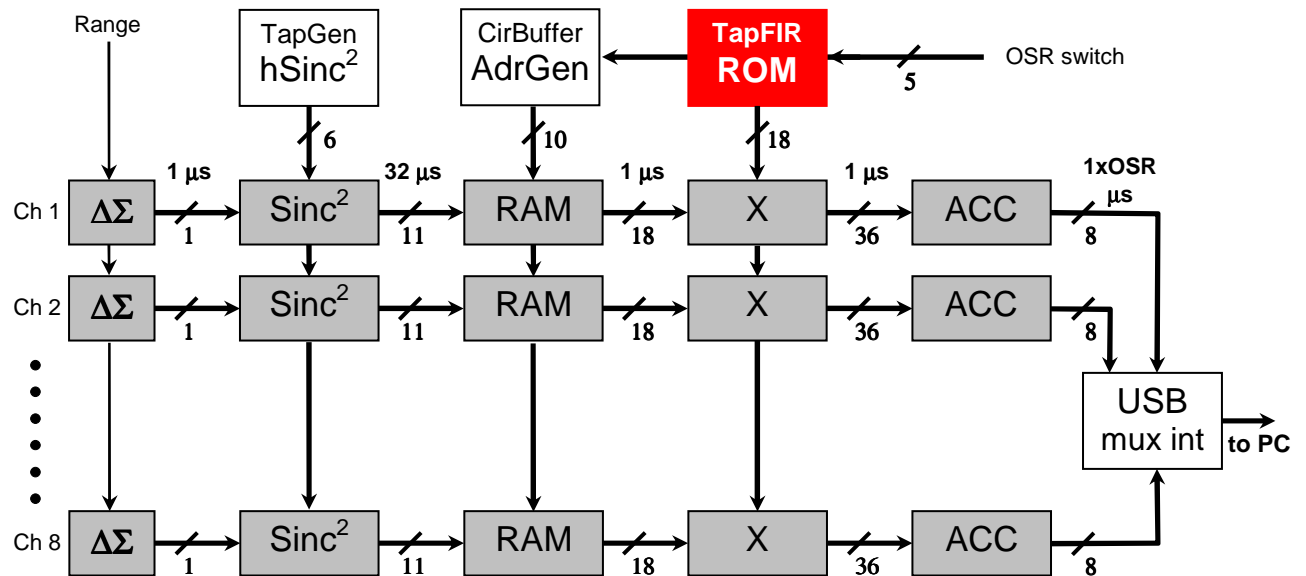


Fig. 54 – FPGA architecture for parallel data decimation: evidential of the ROM block containing the 5 different filter coefficients, related to the 5 selectable OSR.

The LPF filtering process is aligned to the main counter ( $Q[0..14]$ ), so to obtain the correct addressing for the ROMs it is enough to use the relative number of counter outputs following the property

$$N. \text{ address line} = (\log_2 OSR) - 1 \quad (17)$$

where each address line is combined in a *xor* with the counter output number  $\log_2(OSR)$ . The ISE Xilinx software allows the automatic creation of a ROM, using the Distribute Memory Generator tool, simply defining the memory size in term of locations and the data with for the locations (Depth and Data Width), plus the chip enable and the coefficients files (COE) to use to pre-load the ROM with the final filter coefficients. The VHDL instantiation code of the memory component is generated by the automatic tool, and present the bus address “a”, the clock input “clk”, the chip enable “qspo\_ce”, and the registered bus data output “qspo”. On the low-to-high transition of the clock at  $T = n$ , the data stored at the address selected during the last clock period ( $T = n-1$ ) is load into the registers data output bus, and it is available during all the  $T = n$  clock period, if the chip enable is active, otherwise, if it is inactive, the data output bus present the last value stored in the data registers output, as shown in Fig. 55.

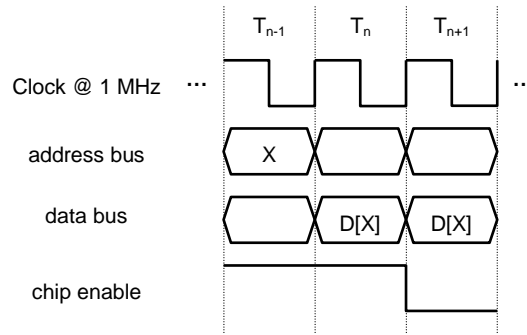
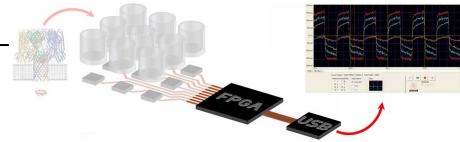


Fig. 55 – Chip enable timing for memory block.

The block is completed with a data output bus multiplexing, according to the OSR selected. Inside the project three of the ISE software, this block is called “hFir”, and in the following figure is shown the relative entity inside the project hierarchy.

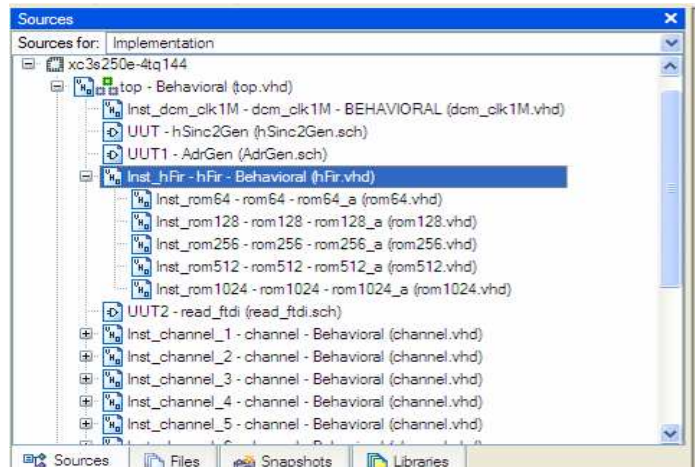


Fig. 56 – ROM Memory instantiation.

### CirBuffer AdrGen

The *CirBuffer AdrGen* block of Fig. 57 Fig. 51 is the address generator for the writing and reading operations on the circular buffer situated between the Sinc<sup>2</sup> and the LPF stages, one buffer for each channel. The length of the buffer (hence the addressing space) depends on the OSR selected, and it is variable from the minimum size, corresponding to 64 memory locations to the maximum size, that is 1024.



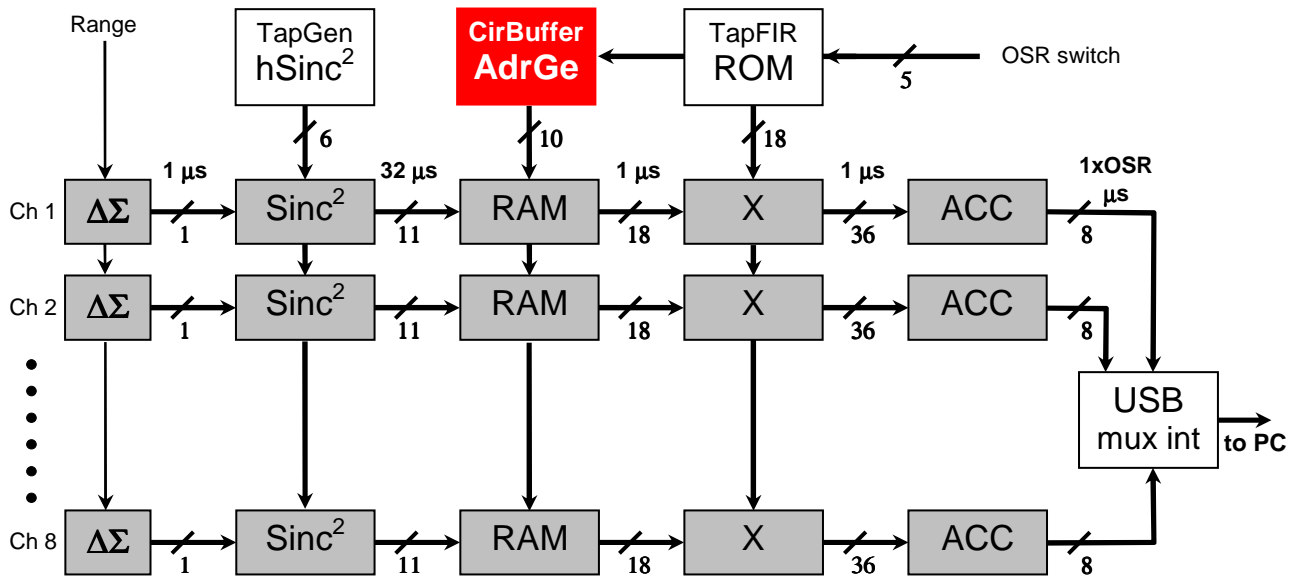
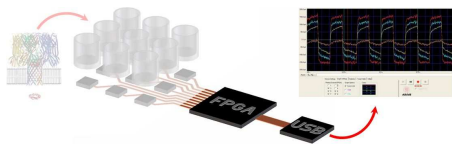


Fig. 57 – FPGA architecture for parallel data decimation: evidential of the circular buffer address generator, that generate the address for the circular buffer (the RAM blocks) with 5 different length, depending to the selected OSR.

As shown in Fig. 57, the circular buffer is written every 32 clock periods, while it is read each clock period. This operation method is possible because while the  $Sinc^2$  is processing a new data to store in the position X, using 32 clock periods, the LPF use the data inside X during the first clock period of the entire convolution process (see Fig. 42). Follows a graphical representation of the evolution of the buffer in the case of OSR = 64.

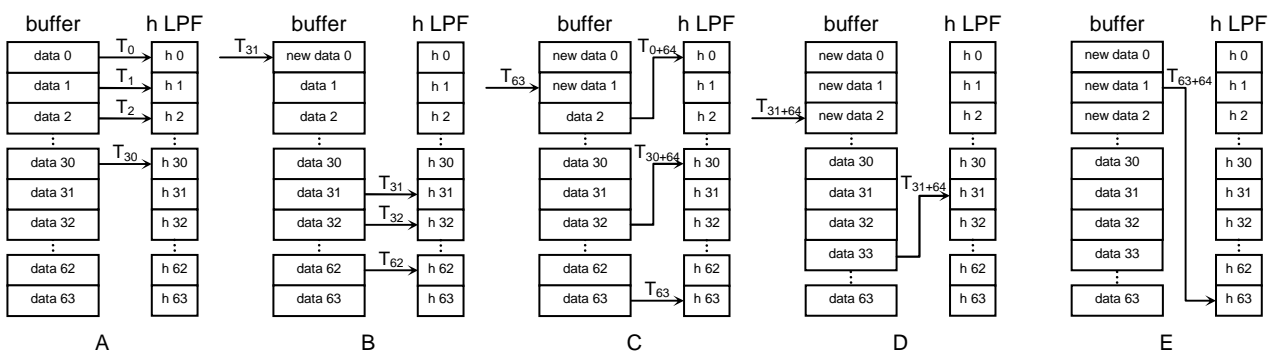
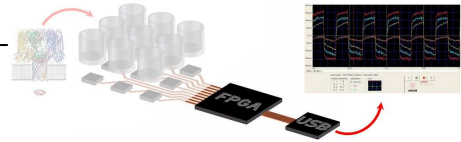


Fig. 58 – Buffer evolution.

During the step A of Fig. 58, the convolution between the data in the circular buffer and the LPF coefficients starts, running a multiplication and sum each clock period, until period  $T_{30}$ . During the following clock period,  $T_{31}$  of step B, a new data incoming from the  $Sinc^2$  is written in the first position of the circular buffer, while the convolution continues. After others 32 steps, as shown in step C of Fig. 58, at the end of the first convolution computation, corresponding to  $T_{63}$ ,



another new data from  $Sinc^2$  is written in the buffer. At the following step,  $T_{0+64}$ , starts a new convolution computation, where the first data taken from the buffer is in the 3<sup>rd</sup> position, that means each new convolution starts with an offset from the previous equal to  $OSR / 32$ . The second convolution cycle continues during step D of Fig. 58 until  $T_{31+64}$ , where a new data from  $Sinc^2$  is written in the buffer in the 3<sup>rd</sup> position. Finally, as shown in step E of Fig. 58, the last clock period of the second convolution process, equal to  $T_{63+64}$ , taken the “new data 1” from the circular buffer, explaining the meaning of circular buffer.

About the implementation of this block, it is important to take into account that the circular buffer presents two data access port, one for reading operations and the other for writing operations, each of one is separately addressable so requires two dedicated address bus.

The write address bus ( $WRadrBuf[0..10]$ ) is originated directly from a combinations between the outputs of the main counter ( $Q[5..14]$ ) and the OSR switch. Due to the specifics to write data into the buffer each 32 clock periods, beside the alignment property of the write process to the main counter output, the address buffer start from the output  $Q[5]$  of the main counter.

The read address bus is obtained by the sum of the main counter outputs  $Q[0..9]$  with a variable offset, depending from the OSR chosen, to realize the circularity of the buffer explained in Fig. 58. In particular, for each convolutional process of the LPF filter, that takes OSR clock periods, the value to sum to the  $Q[0..9]$  outputs is a multiple of  $OSR/32$ , variable from 0 to  $OSR-OSR/32$ , obtainable from a combination between the OSR switch and the main counter outputs  $Q[6..14]$ . The adder output must also be clipped to  $n$ .  $address\ line = \log_2(OSR)$ , so the generated address bus always insists on the same address space.

## ***Sinc<sup>2</sup>***

The  $Sinc^2$  block of Fig. 59 is the arithmetic unit which calculate a runtime average, contributing as first step in the filtering and decimating chain of the one bit data input from the Delta Sigma converters. This block uses the two shifted coefficients data flux  $hSinc2u$  and  $hSinc2d$ , generated by the common  $hSinc^2$  TapGen block, and multiplies them for the same input data sample from the Delta Sigma converter. Both the results of the two flux are stored in two different accumulators, where every 32 clock periods, alternately, a data is ready to be stored in the subsequent buffer.

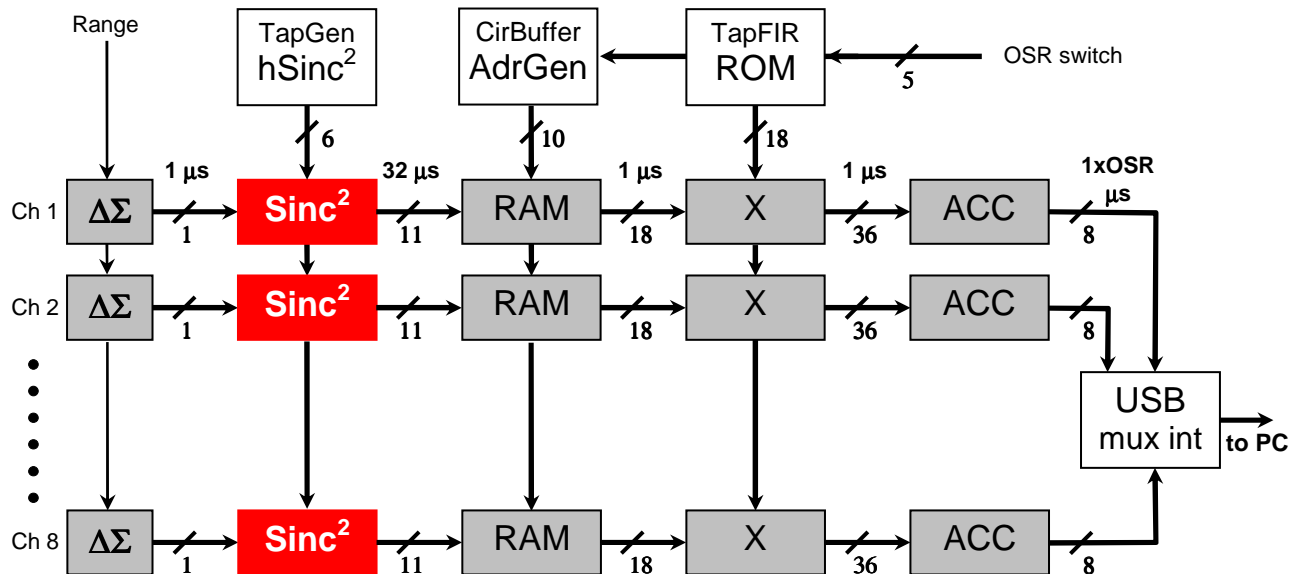
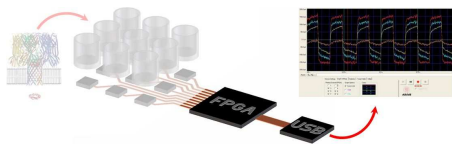


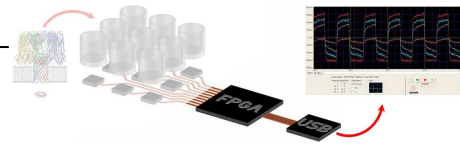
Fig. 59 – FPGA architecture for parallel data decimation: evidential of  $Sinc^2$  blocks, the arithmetic unit replied  $n$ . channel times, that calculate the decimation of each one bit data input stream provided by the delta sigma convertes and outputs the mean value each 32 input samples.

The multiplication and the accumulation process is realized for a single data flux, and than replied two time to calculate separately the hSinc2u and hSinc2d data flux. It takes as input the hSinc2u (or hSinc2d) data bus, and multiply the data for a single bit, that is the output of the Delta Sigma converter, just through a vector of AND gates. The multiplying result is added to the value of the accumulator, that is stored in a registry vector. The registry is synchronized to the master clock at 1MHz, while the Reset signal is connected to the rst\_Sinc2u (or rst\_Sinc2d), so every 64 clock periods the accumulator is reset. The data bus output, that is the adder output, is multiplexed with the same data bus output from the parallel Sinc2Adder elaboration branch for the hSinc2d data flux, alternately every 32 clock periods, hence following the Q[5] of the main counter status. In the VHDL code implementation, that's means

```
Sum <= SumU when (Q(5) = '1') else SumD; -- SumU is referred to hSinc2u; SumD is referred to hSinc2d
```

## RAM

The RAM block of Fig. 60 is the circular buffer of the elaboration chain of the filtering and decimation process for each data channel. It is generated by the Block Memory Generator, the automatic toll provided by ISE Xilinx interface, and preset the following features: 1024x11 bit memory organization (the maximum size required to the circular buffer is equal at the maximum OSR); dual port memory access (one port for reading operations and one port for writing



operation); registered (each read and write operations are triggered on the clock signal); write enable signal.

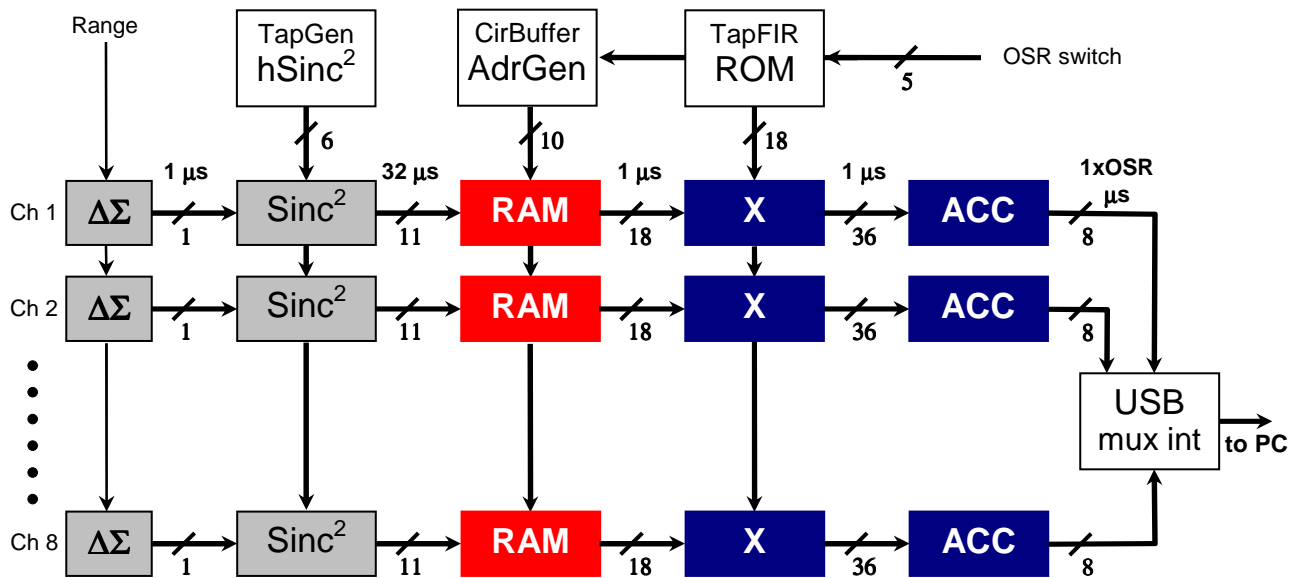


Fig. 60 – FPGA architecture for parallel data decimation: evidential of RAM block (the circular buffer), and the arithmetic blocks X (the 18 bit multiplier) and the accumulator (at 36 bit).

### X and ACC

The X and ACC block of Fig. 60 are the core arithmetic unit of the LPF filter. In particular, the X block is one of the twelve 18x18 bit multipliers available on the FPGA. The 36 bit output is added to the accumulator value stored during the previous elaboration step. The output of this block is a vector of flip-flop, used to store on the WR\_Data enable signal the final data, resulting from the complete convolution process. This data is maintained on the outputs for all the throughout convolution process.

### USB mux int

The USB mux int of Fig. 60 is the write data bus interface for the USB chip. As exposed for the reading process, the design of this block is based on the write time diagram of the chip datasheet. The block implementation is divided into two blocks, each of one contains a Switch operator, to align the USB writing operation to the main counter outputs.

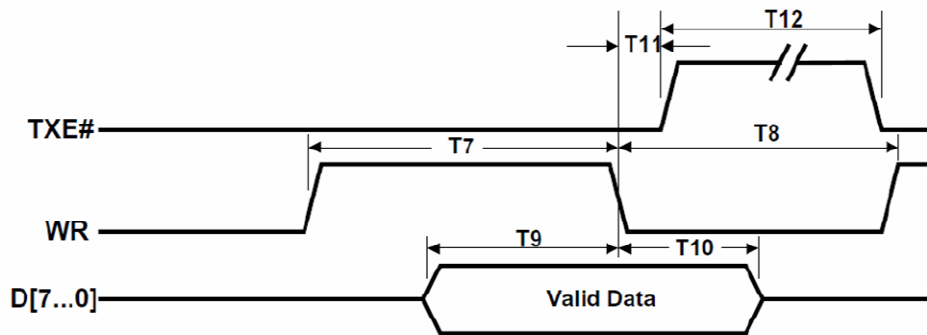
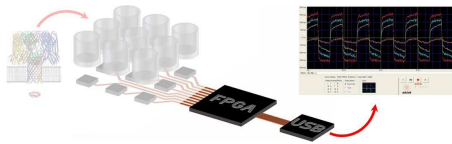


Fig. 61 – FTDI 2232D USB interface FIFO write cycle timing diagram.

The first Switch uses the Q[1..5] condition input to multiplex on the USB chip write data bus the 8 channels data outputs, each of one with the Low Significant Byte first and the Most Significant Byte second, as described in the chapter *USB Interface Protocol*. As condition for all the others unassigned cases, the bus output is forced equal to the synchronization byte.

The second Switch checks the status of the FTDI\_TXE signal as first, to be sure that the chip is ready to accept data on its FIFO buffer. Then, on the low-to-high transition of the master clock, it uses the Q[0..5] condition input to generate a pre write signal (FTDI\_WR\_pre) for the USB chip. The write signal for the synchronization byte (FTDI\_WR\_syc) is obtained by a combination depending on the OSR selection. The resulting writing signal connected to the USB chip is a combination between the two previously explained write signals and the OSR selected.

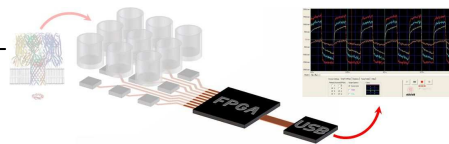
### **Master Clock generator**

Finally, a brief description of the master clock generator, running at the frequency of 1 MHz. This clock is obtained by the Xilinx Clocking Wizard tool, included inside ISE. It takes as input the 6 MHz clock on the board, used by the USB chip, and simply divide it for a factor 6.

## **GUI – Graphical User Interface software for display and data storage**

The PC software interface has the task to set some FPGA parameters and to acquire and save the read data, following the protocol described in the chapter *USB Interface Protocol*. Specifically, the parameters required from the FPGA are:

- the over sampling ratio;
- the full scale range;



- the type of  $V_c$  (if a triangular signal or a constant value);
- the  $V_c$  value in the case of constant  $V_c$ ;
- the feedback correction activation.

Every time one of these parameters is changed on the software interface, a 3-byte long data packet is sent to the FPGA via the same USB connection containing these settings.

Meanwhile, the filtered and decimated data are sent from the FPGA to the PC as a continuous stream of 13 bytes long packets (2 bytes per channel for 8 channels at a time plus a synchronization byte). This data are stored on the hard drive of the PC and visualized by the software. The software interface follows the algorithm indicated in Fig. 62, where, after the open procedure of the input device (the USB chip interface FT2232D), a synchronization byte (code 80h) is expected to start the data visualization on the graphical interface. If the storing function is activated, the software ask for the data path and name for the archive. Fig. 63 shows a screenshot of the designed GUI interface. Apart the FPGA settings, the software presents several options to select the plotted channels and to personalize some aspects like colours or zoom (see Fig. 64 a).

An interesting feature is the chance to evaluate statistical properties of the acquired data in real time, while the measurements are running (Fig. 64 b). For instance, the software calculates the mean value and the standard deviation of the selected channel and it also permits to set two thresholds which can be used to detect peaks in the acquired currents and it measures the mean time ( $\tau$ ) between them. This value can be directly related to molecule concentrations in some kind of experiments [NehSak95] [Bayley01].

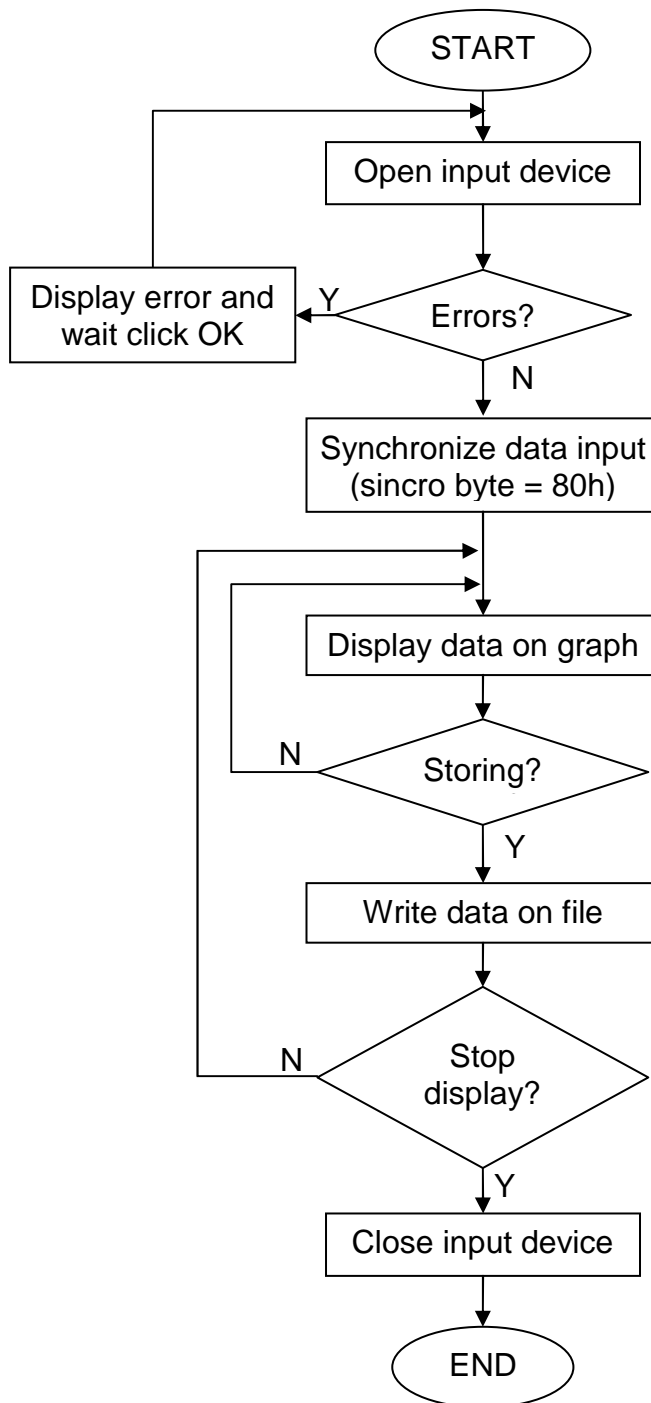
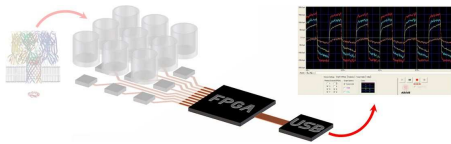


Fig. 62 – GUI flow chart. After the open procedure of the input device (the USB chip interface FT2232D), a synchronization byte (code 80h) is expected to start the data visualization on the graphical interface. If the storing function is activated, the software ask for the data path and name for the archive. The display process ends after the stop request.

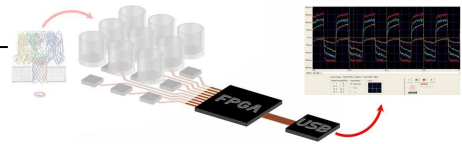


Fig. 63. A Graphical User Interface screenshot showing concurrent display of three traces where single molecule events are recorded

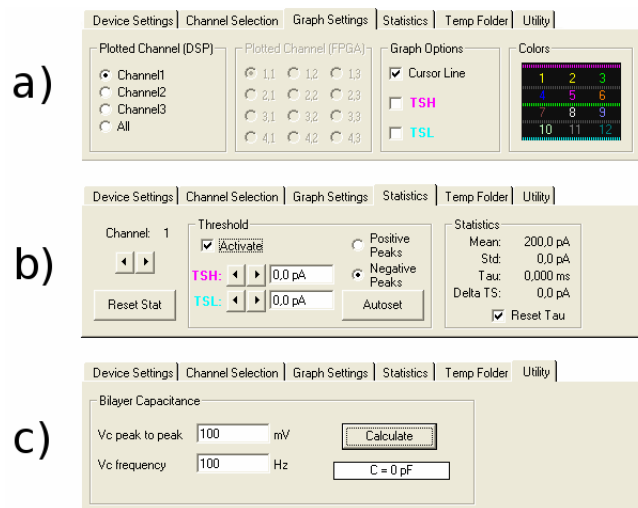
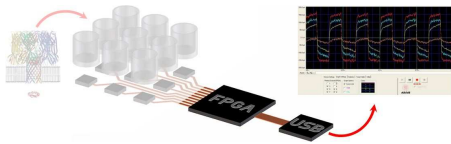


Fig. 64 Some of the settings tabs: (a) Plot settings options; (b) Real time statistics; (c) Utility for bilayer capacitance calculation.

Moreover, there is also a simple utility (Fig. 64 c) used to calculate the BLM physical properties by means of impedance measurements.

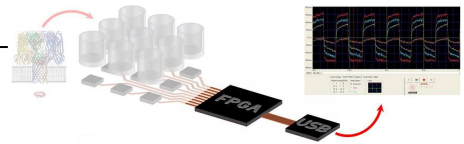




Data are saved in text files (one file every 5 minutes of recording) in form of values separated by a TAB character. This format can be easily read by Matlab®, by GNU Octave or by a specific Visual Basic routines to be performed in the background.

## Maximum FPGA performances related to standard serial data links

The architecture of this system is designed to be expanded to a very large amount of simultaneously data channel elaboration, depending only on the performance of the FPGA and the maximum capacity of the data transfer link. As proof of this concept, supposing an acquiring channel at 4 kHz with 16 bit of resolution for each data sample, through a USB 2.0 full speed (12 Mb/sec) data link it is possible to send up to 75 channels simultaneously. Moreover, through a USB 2.0 high speed (480 Mb/sec) data link, the number of simultaneously channels elaborated grows up to 3.000 channels. Using Ethernet links, able of Gbps as data rate, the number of simultaneously channels grows up of orders of magnitude. Commercial FPGA (i.e. Xilinx Virtex VI® XC6V SX475T) offers up to 2.016 DSP slices operating at 600 MHz, where each slice can elaborate one channel.



# Chapter 4

## Microfluidics and acquisition platforms

### Introduction

Microfluidics are devices designed to host small quantities of chemical agents to run different kinds of tests and experiments, in the fields of physics, biotechnology or electrophysiology. Usually, they are made in several materials, from polymers to glass, depending on the features required for the specific application, using different fabrication processes like lithography and etching or mechanical machining. Particular shapes and conformations of reservoirs, channels and pipes, allow the dispensing of certain amounts of liquid and offer mechanical support for biological entities, like Black Lipid Membranes for example.

Depending on the sensing system employed to interface microfluidic devices with measurement instruments, optical and/or electronic interfaces are utilized. In the electronic case, microfluidics embed electrodes to allow ion exchange to sustain current signals. Microfluidic device miniaturization is the key point for lab-on-chip systems, where it is possible to recreate real experimental setups in areas of few mm<sup>2</sup>. That means the possibility to parallelize experiments, improving the accuracy of results, or even reducing the time required to carry out long tests.

As already indicated in Chapter 1, the most part of ion channel acquiring setups are bulky and expensive, because from one side, if very small microfluidic devices are able to perform high successful and accurate tests, they lose their appeal because not optimized in the electronic interface, typically constituted from bulky instrumentation and inappropriate plug systems (see Fig. 65).

Embedding microfluidic and electronic readout into a single system is a new point of view, because the design process optimizes all the requirements of electrophysiology setups. In this chapter, the hybrid technology concept is explained, showing the development from a single channel acquiring system, used to validate the system approach, to an array for multiple channels acquiring platform. All the design steps are illustrated, about the microfluidic development, the electrodes fabrication, the strategies for the PCB design. Specific requirements, even originated by the multi channel platform, are resolved and implemented in the final setup.

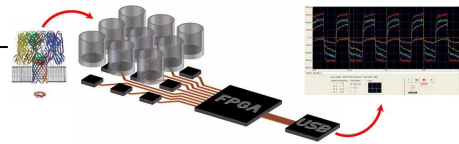


Fig. 65 – Tecella Apollo 384ch Patch Clamp Amplifier (from Tecella product catalogue).

## Hybrid technology for electronic/microfluidic embedding

The hybrid technology consist into a multilevel system approach, where a single platform incorporates all the necessary to run specific tests, from the microfluidic devices, that host the biosensors, to the electronic read out front-end, constituted by the analog to digital converters, the digital elaboration and signal control, the data transfer interface to a host PC, and the data visualization and storage. Each level involved into this approach is shown in Fig. 66.

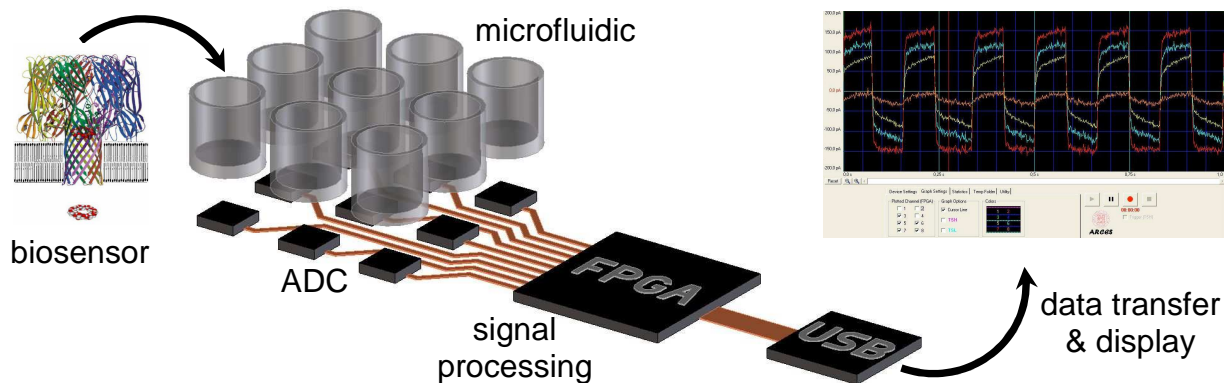
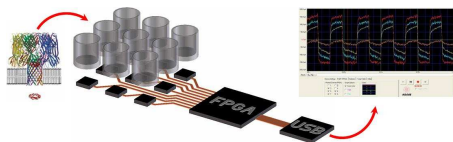


Fig. 66 – Hybrid technology concept for heterogeneous system approach.

Therefore, it is clear the interdisciplinary request by the project. A relevant focus needs the multilevel approach, where each level performs specific functions:



- a first level is constituted by the microfluidic devices, capable to host the bio sensor by providing all the mechanical support, the reservoirs for chemical agents, and also including the Ag/AgCl electrodes;
- a second level is dedicated to the microelectronic, where a low noise acquiring front-end is specifically designed;
- a third level where a digital elaboration architecture run the numerical computation of data, control the system functions and organize the data transfer to a host PC;
- a last level, to display and storage the acquired data.

A common point for all the platforms designed during the project development is the embedding of the firsts two levels into a unique PCB. This new approach, where a readout circuit is tightly close to the sensor substrate (Fig. 67), is particularly suitable for nanosensor readout for the following reasons: first, since the noise is correlated to the input stray capacitance, the closer the readout the lower the noise. Secondly, whenever nanosensors are arranged into array structures, due to the low current regime and timing requirements, single-BLM signal multiplexing should be avoided since this reduces performances. Thus, it is crucial to place the electronic conversion as close as possible to each BLM of the array. Third, the PCB is not exposed to the chemical agents, and allows a simple and fast replacement of microfluidic devices.

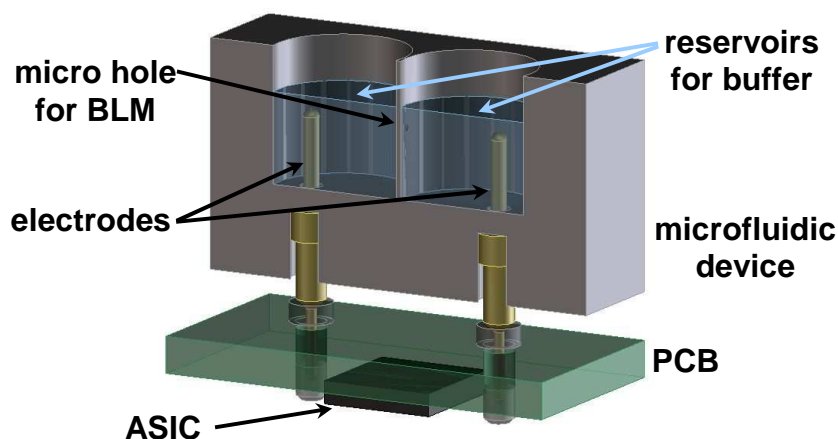


Fig. 67 – Example of multilayer approach for microfluidic and electronic embedding.

For the presented application, the main purpose of the microfluidic device is to provide a mechanical support, typically a micro hole into a thin substrate (Fig. 68) that connect two separated reservoirs, for the BLM formation. Each reservoir contains the buffer solution and must be contacted by electrodes to the electronic read out front-end. When it forms, the BLM have to seal the two reservoirs, to ensure the instauration of an electrochemical gradient between them.

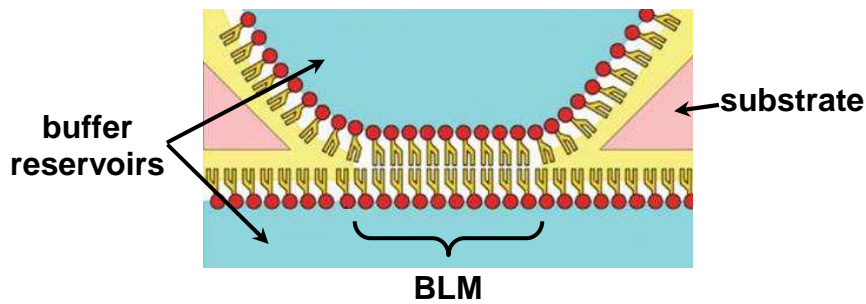
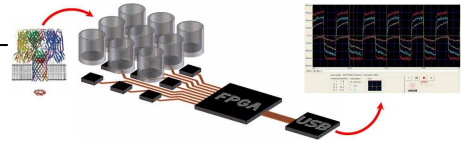


Fig. 68 – Model of bilayer formation on artificial substrate.

To allow the BLM formation, several characteristics must be satisfied, such as the hydrophobicity of the substrate material, required for the lipid hydrophilic tail attachment at the substrate surface; the micro hole diameter, in the range of few hundred microns; the substrate thickness, and the electrical insulation. Several techniques were developed to produce small apertures suitable for BLM substrates, and literature is full of examples, from silanized glass microdrilled or etched after lithography process, Teflon sheets drilled by electric discharge, Delrin (POM) and Polysulphone (PSU) devices milled.

To establish an electrical connection between the buffer solution (typically KCl at different Molar concentrations) and the electronic read out front-end, Ag/AgCl electrodes are used, positioned into the reservoirs filled by buffer as illustrated in previously Fig. 67.

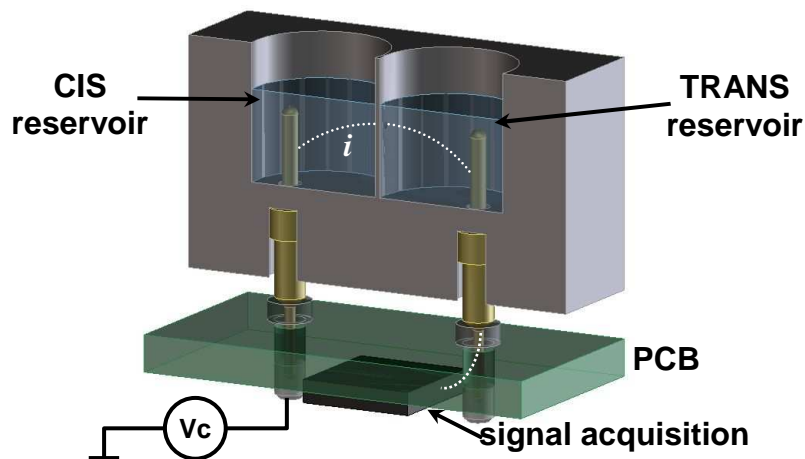
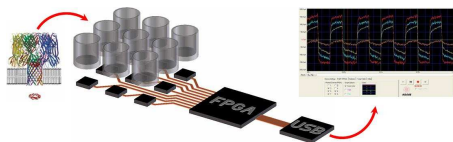


Fig. 69 – Control signal ( $V_c$ ) and acquisition of Ion current on sectioned microfluidic device.

The chlorization of the Silver surface electrodes (usually called Ag/AgCl) is required for the ion  $Cl^-$  exchange at the interface electrode/buffer to allow a current flux.

One electrode connects the stimulus ( $V_c$ ) to the CIS reservoir, as shown in Fig. 69. This is the control voltage applied to one side of the biosensor. Because the input stage of the ADC is referred to  $V_{cc}/2$ , as explained in Chapter 2, also the stimulus have to be referred to the same



potential, by an analogic adding circuitry. The second electrode is the acquiring pin, that connect the TRANS reservoir at the input stage of the ADC ASIC for the signal acquisition.

A requirement of the system is the monitoring of the BLM formation process. Since a BLM is electrically equivalent to a capacitance (in a simplified model), and observing that a micro hole, filled by a conductive solution (the KCl buffer, as example), is electrically equivalent to a resistance, it is possible to monitor the BLM formation by an impedance check, observing the evolution of a signal response to a prefixed stimulus. The stimulus chosen for this purpose is a voltage triangular wave: as illustrated in Fig. 70, if no BLM are formed on the micro hole, a triangular current is monitored (Fig. 70 a), otherwise, if a BLM is forming, the acquired current became approximately a square wave (Fig. 70 b).

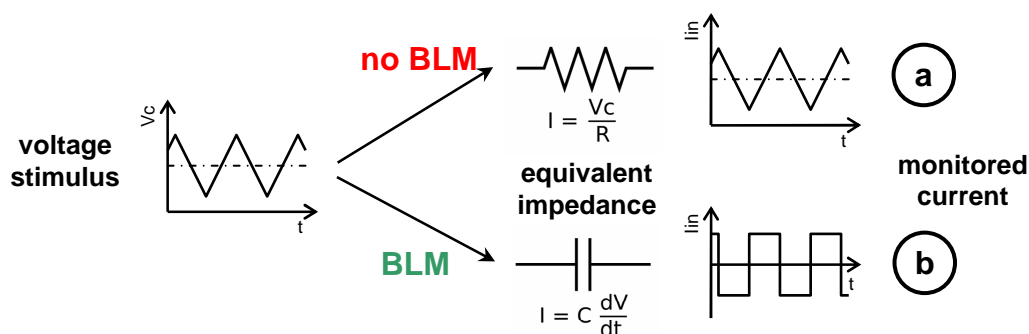


Fig. 70 – Signal response to BLM stimulus signal ( $V_c$ ).

Other requirements of the platform are the possibility to provide a variety of voltage stimulus, in the range of some hundred mV, plus all the digital controls to select the different acquisition modality of the ADC.

The digital elaboration of data is devolved to an external unit, in particular a DSP board, for the first prototypes, while in the final platform is completely embedded on the same PCB.

## Single channel acquisition platform

The development of an acquiring platform embedding electronic readout and microfluidic devices started from a single channel system test, more specifically from the emulation of the state-of-art electrophysiology workstation (Fig. 71), the typical experimental setup for BLM and ion channel investigation. The usage of the same microfluidic device (the Warner BLM chamber) allows a direct comparison of data, to verify the performances of the Delta Sigma low noise acquiring front-end.

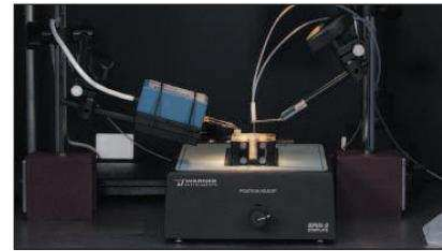
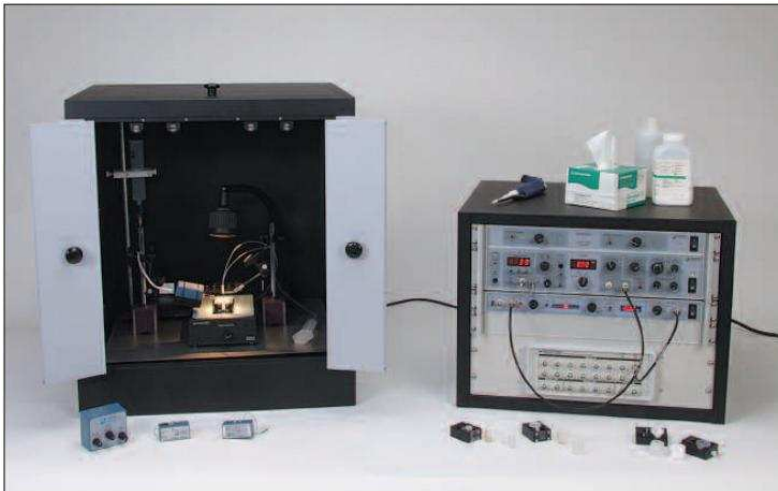
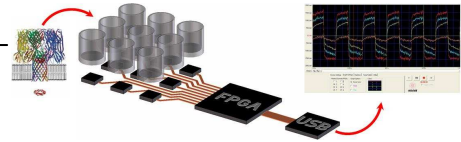


Fig. 71 – Warner Instruments Planar Lipid Bilayer (BLM) Workstation setup.

The platform can be represented by the following block scheme Fig. 72. Characteristics of the PCB are a single acquisition channel through a delta sigma ASIC, an adjustable voltage offset adding circuitry for the control voltage (the experiment stimulus), a series of selectable inverters

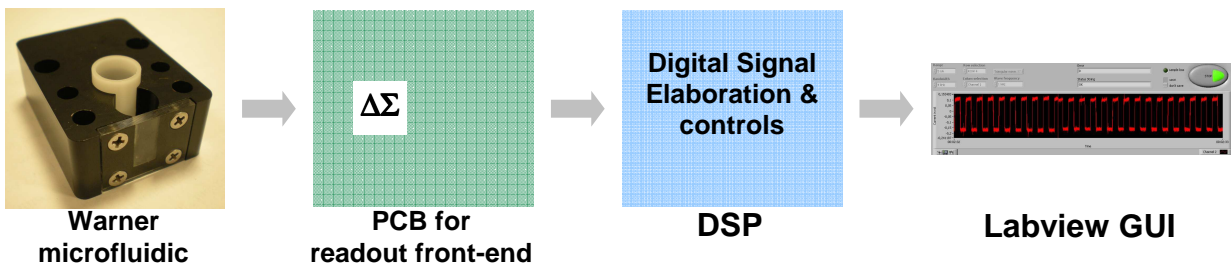


Fig. 72 – Single channel acquiring platform based on Warner microfluidic device.

CMOS on the digital I/O lines of the delta sigma, to reduce the noise due to the digital switching activity on the Vdd (the digital power supply), a BNC connector to plug an external signal generator and a 15 pins connector for the control and power supply board, for the numerical data process (the DSP interface BoardInt). The electrical scheme of this first acquiring board, called TestChipSensor 1, is shown in Fig. 101. A peculiarity of this PCB is the socket for the Delta Sigma ASIC, to allow the reuse of the chip tested with the ChipTest board, discussed in Chapter 2. The PCB was realized with the double side technology by an internal university facility, the LPKF Protomat micromilling machine, and the final board is illustrated in the next picture Fig. 73.



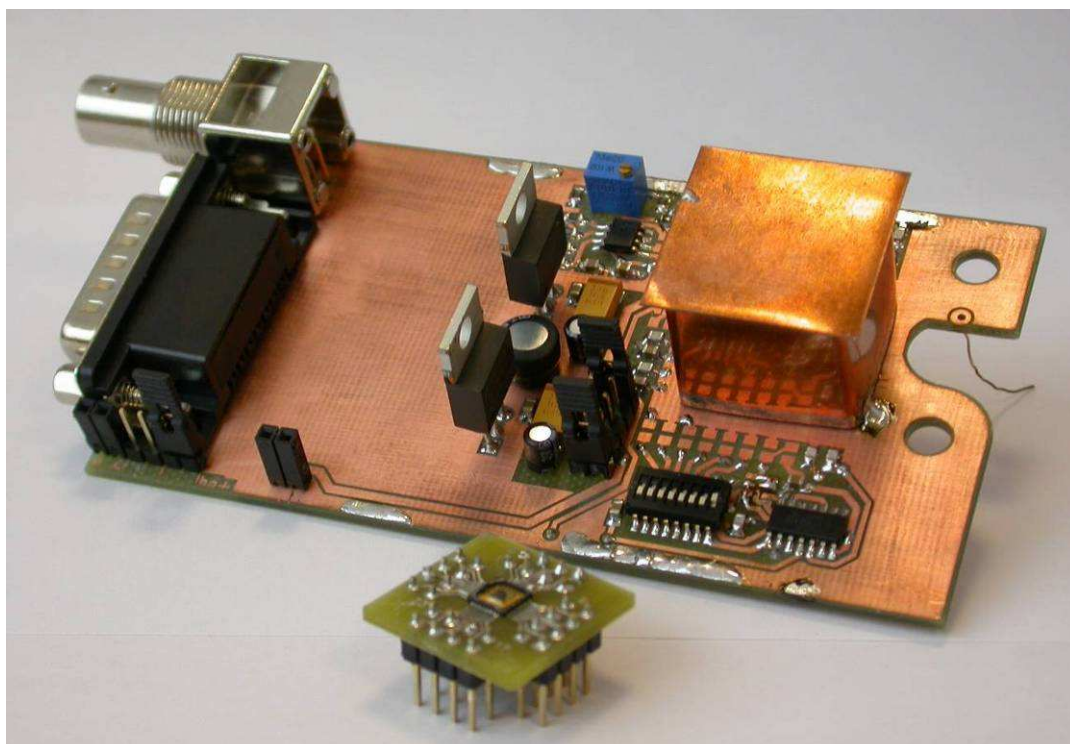
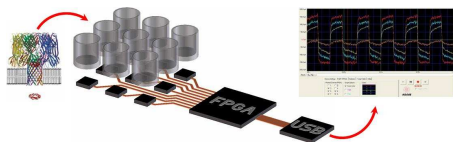


Fig. 73 – PCB board TestChipSensor 1.

The PCB was coupled over the Warner microfluidic device, as shown in Fig. 74, with two Ag/AgCl electrodes immersed into the two reservoirs. Some tests were done and several single channel acquisition were recorded through the Labview GUI software interface.

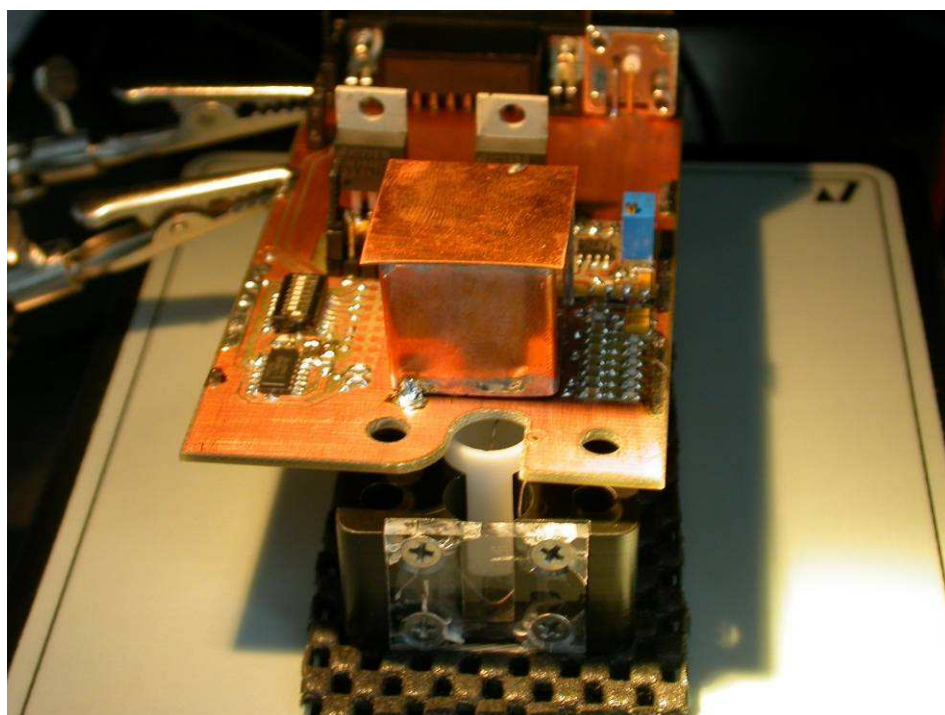
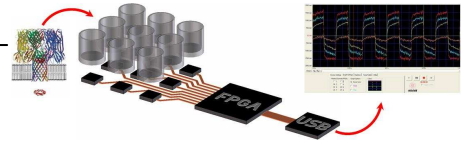


Fig. 74 – Experiment setup for platform TestChipSensor 1.



To reduce the total noise on the acquired signal, due to the socket dimension used the host the ASIC plus some soldering residual on the substrate ASIC socket (the FR4 material without solder resist surface treatment), an evolution of the PCB TestChipSensor 1 was designed: the PCB TestChipSensor 2 (Fig. 102). From the electrical point of view, the two board are almost the same, but the main difference with the first version is the PCB manufactory: an industrial process was selected to produce this new PCB, using a four metal layer PCB, especially to introduce some grounded layer to shield the analog signals on the board from the digital clock lines.

Also in this case, the PCB was coupled over the Warner microfluidic device, as shown in Fig. 75, with two Ag/AgCl electrodes immersed into the two reservoirs. Some tests were done and several single channel acquisition were recorded through the Labview GUI software interface.

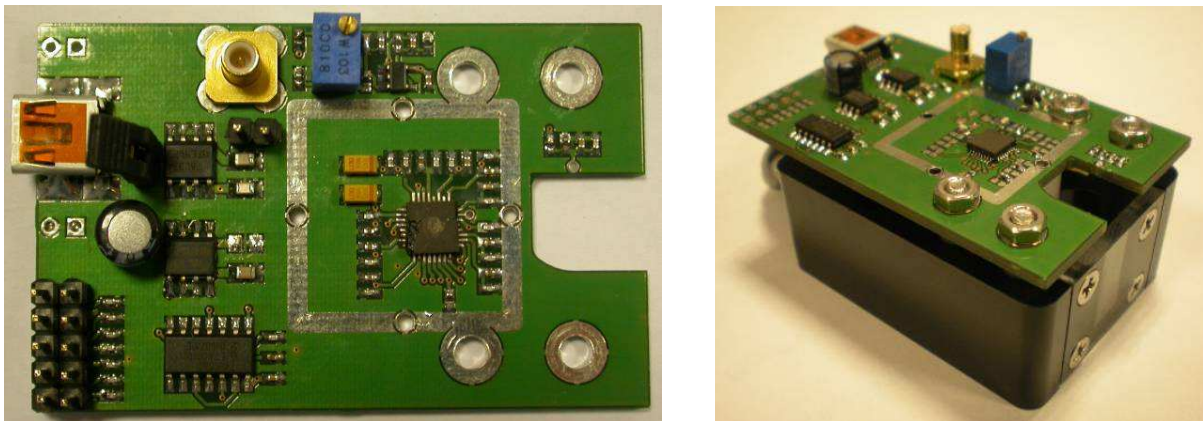
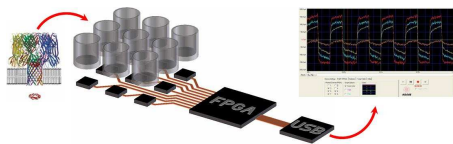


Fig. 75 – PCB board TestChipSensor 2.

The first phase of tests on the Delta Sigma ASIC plus all the numerical elaboration chain, constituted by a DSP and a Labview software interface to acquire and store data, was used to acquire single channel activity with successful results, by a direct comparison with the same kind of data acquired by the Warner workstation.

### ***Roadmap to the final array solution***

From the single channel acquisition platform, the system development evolves to the array target, where a relevant part of the project development was required by an appropriate microfluidic design, ready to be reduced in size but maintaining all the properties for the BLM formation, with respect to the previously used Warner microfluidic device. Various test devices was realized by means of different fabrication techniques, improving at each step the performances in terms of reproducibility and simplicity in manufactory process. Part of this work



was done at the University of Southampton, where a glass-based microfluidic prototype (Fig. 76 a) was interfaced with the single channel acquisition board (Fig. 76 b). This type of approach

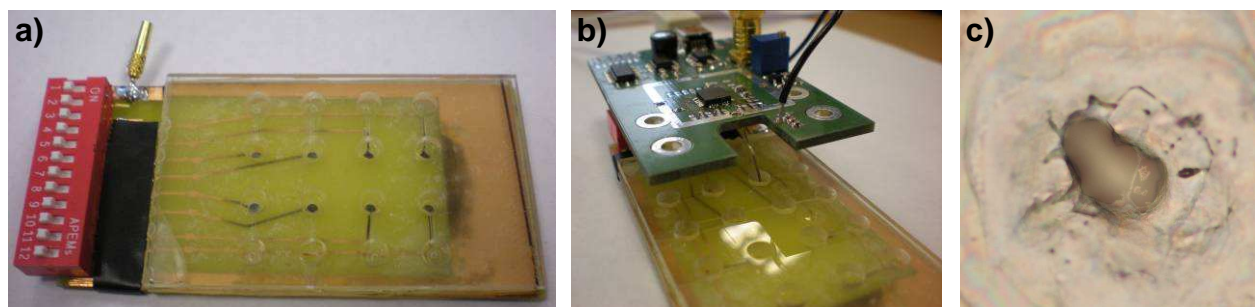


Fig. 76 – Glass-based microfluidic device.

presents several problems, from the difficult in the BLM formation over the too much irregular micro hole (Fig. 76 c), obtained by electrochemical erosion, the silanization process required from the glass surface pre-treatment, and finally the leakages in the glass-PCB bonded interface. A radical change in the process fabrication was required, and consequently, in the material used as substrate. A new design was realized by milling a Delrin substrate, explained in Fig. 77 where the microfluidic is coupled with a PCB. In the section view of Fig. 77 b are

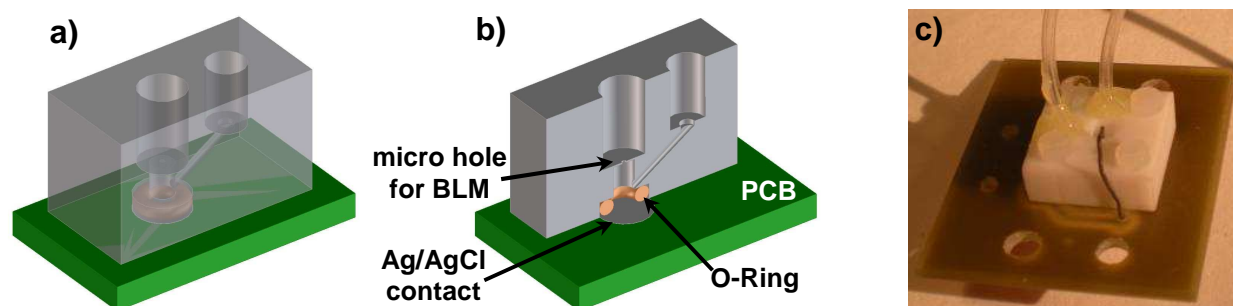


Fig. 77 – First microfluidic device milled into Delrin substrate.

represented all the characteristics of the machined microfluidic, from the micro hole to host the BLM, the top and bottom reservoirs, the fluidic access to the bottom reservoir, the Ag/AgCl pad on the PCB that acts as the acquiring electrode, and the o-ring used to seal the microfluidic block to the PCB. To test the microfluidic, a single channel device was realized and coupled to a small PCB to plug directly on the TestChipSensor 2 board. Some BLM was successfully obtained, so the next step was the exportation of the microfluidic structure to an array configuration, milling into a single Delrin block up to 12 channels (Fig. 78 a). At the same time, a PCB to host the ASIC array plus the Ag/AgCl pads was design, following the indication reported into Fig. 78 b/c. The related scheme of this board, TestChipArray, is shown in Fig. 103.

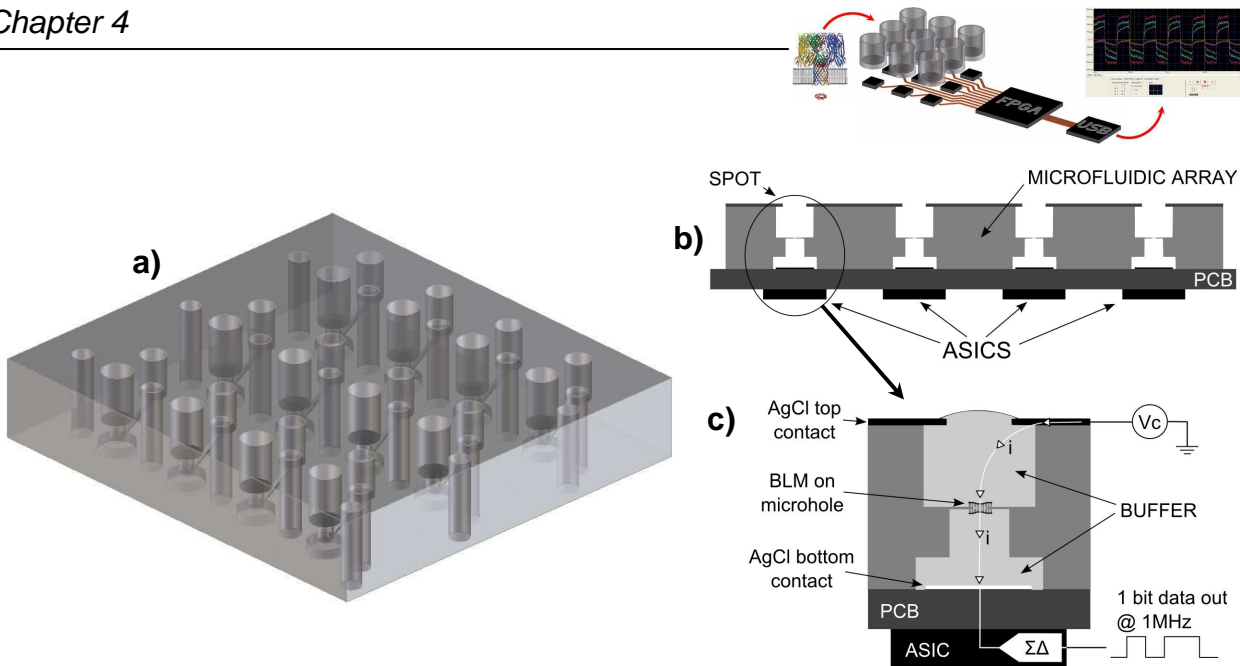


Fig. 78 – Microfluidic test array design and coupling detail with dedicated acquiring board.

Others features of the TestChipArray board are an addressable switching system to select 3 channels at once, an adjustable voltage offset adding circuitry for the control voltage (the experiment stimulus), and an array of 12 Delta Sigma ASIC, one to each acquiring channel. Also this PCB was realized by an industrial process using four metal layers.

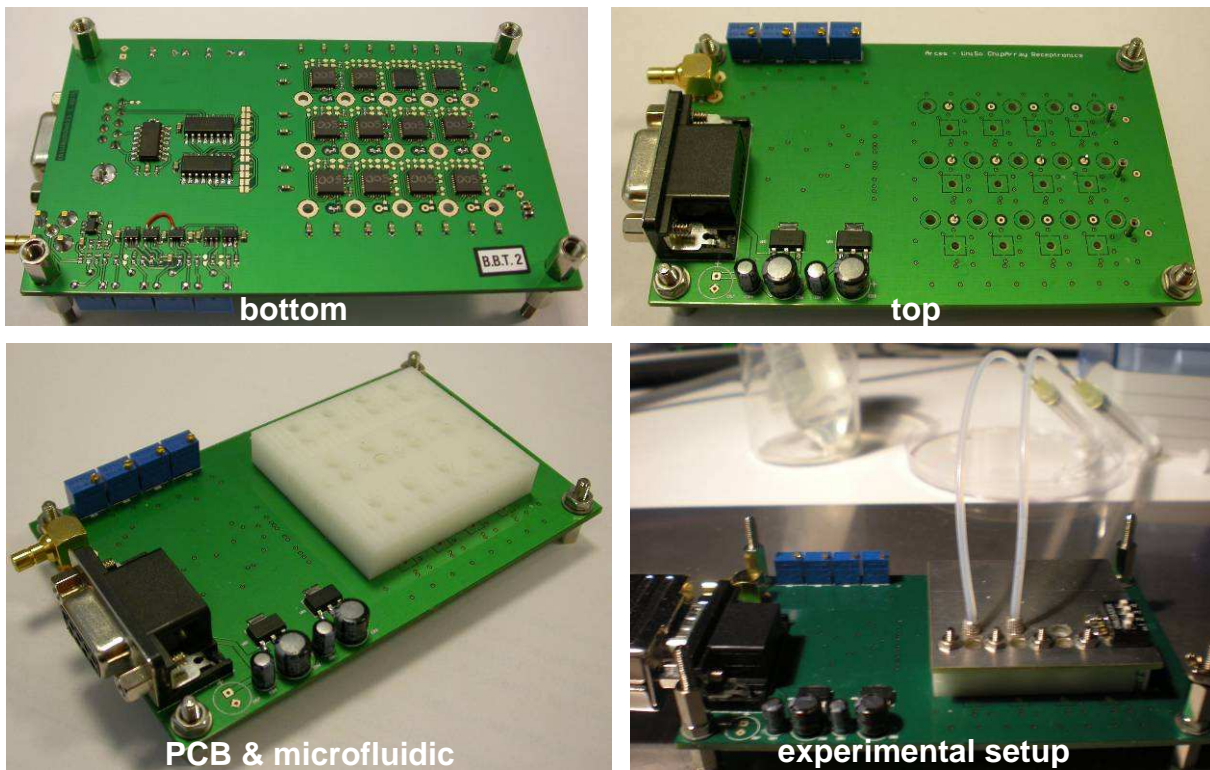
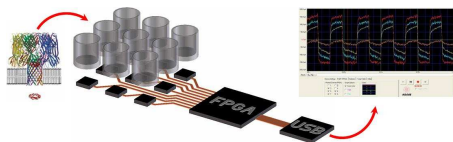


Fig. 79 – Board TestChipArray, top and bottom, with microfluidic and experimental setup view.



The TestChipArray board was connected to the DSP BoardInt, to process up to three of the twelve data channels concurrently by a column selection of the array, and data was displayed through the Labview GUI software interface. After several tests on the array platform, different problems was observed, and they are listed below:

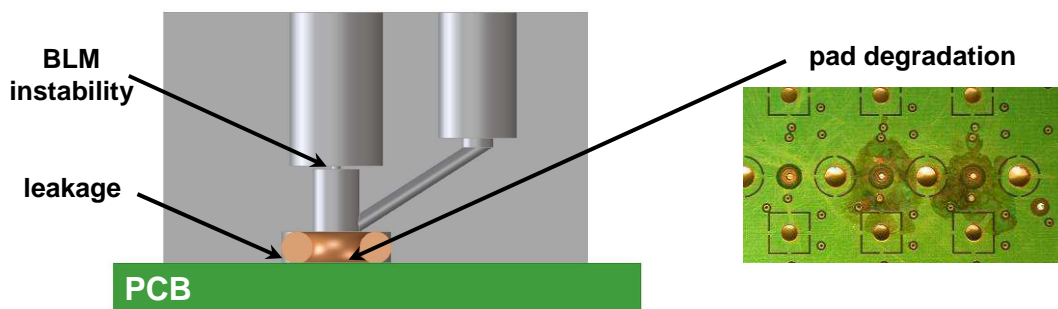
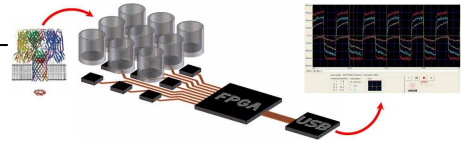


Fig. 80 – Board problems.

- the electrode wear, due to the re-chlorization of the electrodes after each test, because a cleaning action is required for the electrode before the re-chlorization so the PCB substrate under the pad will be damage after few times (Fig. 80);
- the electrode instability, due to the very thin layer of silver plated on the copper pad on the PCB;
- a BLM instability, due to the buffer pressure variation of the bottom reservoir because the pipe system to filling, susceptible to the movements;
- a leakage of solutions at the PCB-microfluidic interface, due to the not perfect sealing of the o-ring caused by a degradation of the PCB substrate, after several re-chlorization of the pad;
- the pipe systems is too much complicate because it requires one pipe and the relative flow control system for each channel to fill the relative bottom reservoir;
- the output of a milling process that involve all the microfluidic array is susceptible to defects of single septum or micro holes, critical parts for the BLM formation;
- the PCB exposure to chemical solutions, as the KCl buffer as example, increase the humidity around the acquiring pads, and contributes to leakages in the current;
- from the electronic point of view, the common control voltage ( $V_c$ ) supply to each channel introduces a crosstalk at the input stage of the Delta Sigma ASICS (see next paragraph “Automatic offset compensation”).

The report of all these problems was take into account during the final design, resolving point by point all the difficulty of the first samples.



## Multiple channel acquisition platform: the final solution

The collection of all the experiences previously acquired, in the fields of microfluidic design and fabrication, low noise PCB design, long life electrodes fabrication, is used to realize the final multiple channel acquisition platform. The key points to take into account, during the platform design, are:

- the simplicity in the microfluidic devices fabrication, made by fully automated CNC milling machines, splitting the array into single blocks that host a single BLM, and reassembling the blocks into a modular structure;
- a separation between electrodes immersed into chemical solution by the PCB substrate, to prevent boards damage;
- electronic readout front-end as close as possible to the acquiring electrodes, plus grounded metal layers to shield the analog signals;
- a simple system to perfuse solutions to the reservoirs, to avoid complicated pipe systems and pumps.

The following paragraph explain the platform design, from the point of view of all the indicated points, starting from the microfluidic, the electrodes fabrication, the automatic voltage offset compensation, and finally the PCB design. As proof of this concept, Fig. 81 shows the

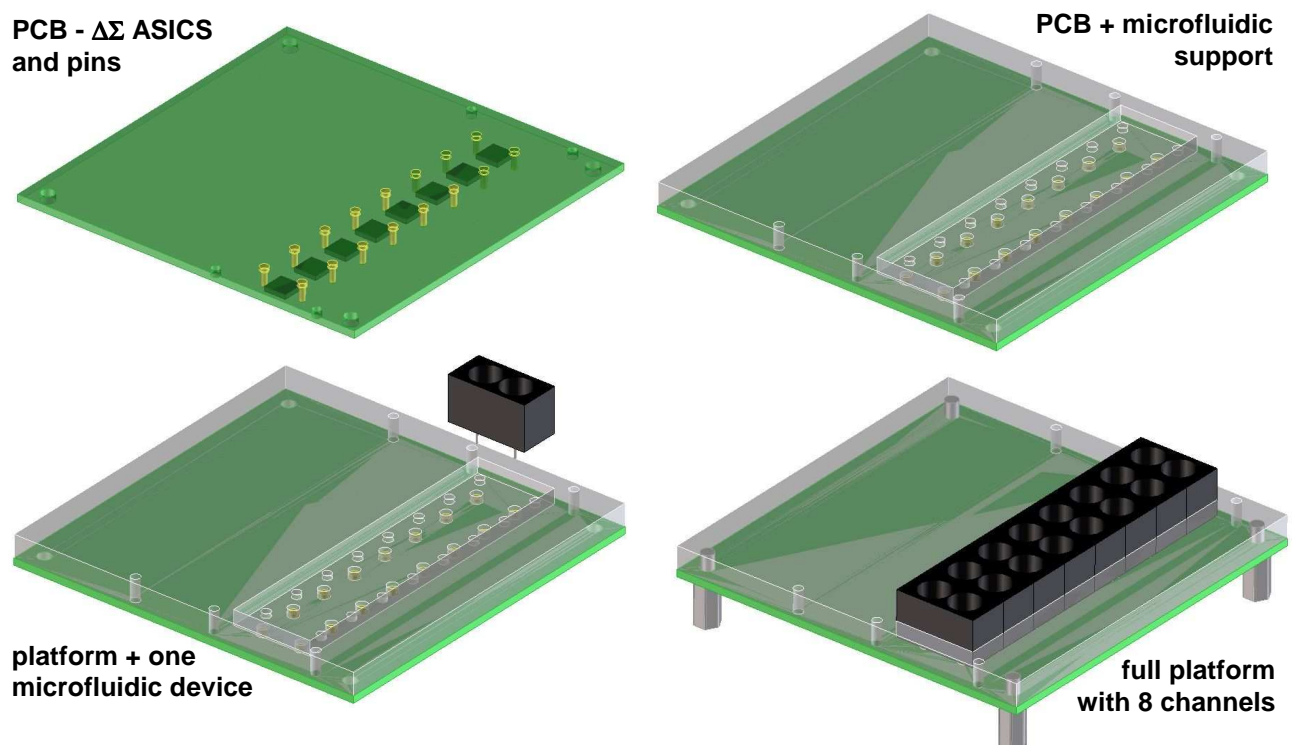
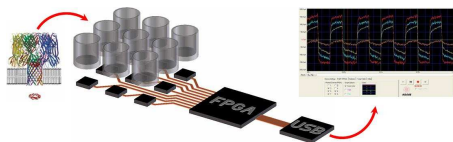


Fig. 81 – 8 channels microfluidic acquiring platform.



combined electronic and microfluidic design, the PCB layout for the acquiring front-end and the microfluidic devices disposition into array configuration.

### **Modular and disposable microfluidic blocks**

Very few examples of parallel ion channel recording platform are present in literature [Pioufle08] [Sandison09], and the main problems related to the mentioned platforms are: i) the above approaches are based on monolithic microfluidic structures where the yield of the array is linked to that of single microfluidic device; ii) the above operations frequently rely on microfluidic routing channels that do not scale efficiently with respect to the dimension of the array. Aim of this paper is to present a versatile and low-cost microfluidic platform realized using a micromilling process fabrication of polyoxymethylene homopolymer (Delrin™) substrates. The devices are suitable to embed lipid bilayer membrane arrays for ion channel recording activity using a fully automated approach and are ready to be embedded in a parallel readout hybrid electronic platform [Thei10]. The main advantages of the proposed approach over state-of-the-art are:

- the microfluidic structure is selectively disposable at single spot level where faulty elements can be automatically revealed by electronic sensing;
- the platform can be interfaced to any generic micro-pipetting machine and is fully scalable to any array size;
- each microfluidic spot is directly interfaced with an electronic interface for a truly parallel readout signal acquisition.

The fabrication process is based on a computer numerical control (CNC) milling machine (Fig. 82), starting from a Delrin block milled on top and bottom surfaces, for engraving the fluidic

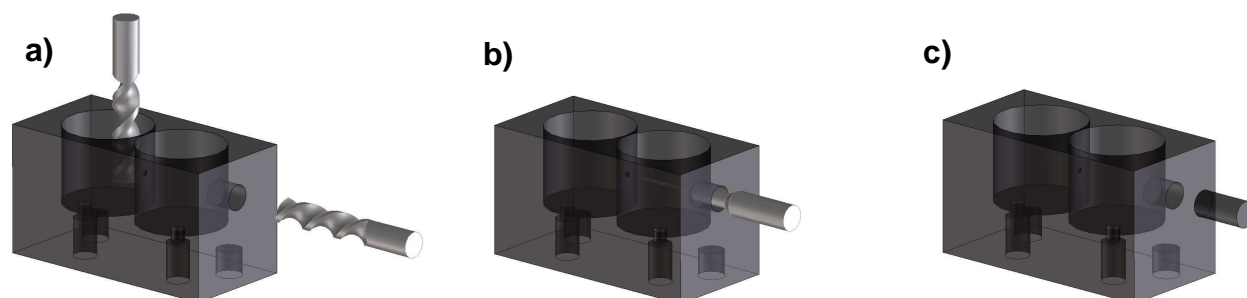
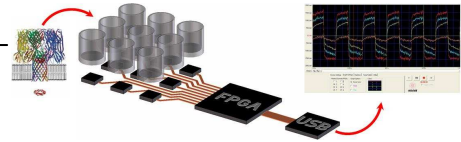


Fig. 82 – Microfluidic milling phases. a) top and bottom milling surface and side drilling for microdrilling bit access; b) microdrilling process by a 200  $\mu\text{m}$  drill bit; c) sealing of construction holes with Delrin cylinders. The thickness of the septum is 50 $\mu\text{m}$ .

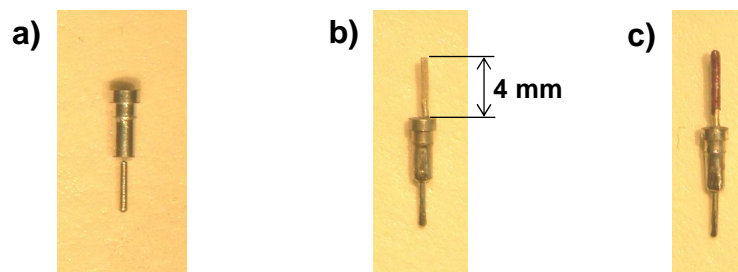


access channel and the reservoirs cavities on the top side, and the electrode slots on the bottom one. Next, side holes are made (Fig. 82 a-b) to realize the interconnecting channels, and an access hole to allow the last drilling phase is made using a 200  $\mu\text{m}$  diameter drill bit (Fig. 82 b). The fabrication process ends by sealing the constructions holes (Fig. 82 c) by a Delrin cylinder. Two Ag/AgCl electrodes are stuck into the bottom slots.

Single Delrin blocks can be assembled on a PCB board to realize arrays of any size, with the final purpose to improve the acquisition capability of ion channels organized in parallel fashion.

### ***Ag/AgCl electrodes fabrication***

The electrodes fabrication consist of two phases. Starting from a commercial socket contact, like the Harwin D01-997XX01 (Fig. 83 a), a 0.5 mm diameter silver wire is first inserted into the socket and than soldered (Fig. 83 b), with a final external length of 4 mm. Than the silver wire is cleaned by any tin residual over the external part, that is heated and immersed into a fused AgCl solution. The final electrode is illustrated in Fig. 83 c. Because the thick AgCl layer deposited on the silver electrode, the average life time is greater than 200 hours, without any special re-treatment required.



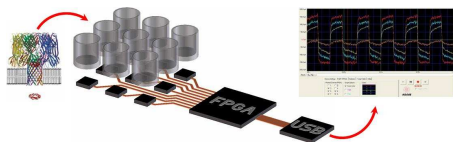
*Fig. 83 – Ag/AgCl electrode fabrication phases.*

When the electrode is unused, it is important to store it into a dark holder, to prevent any light oxidation of the AgCl surface.

### ***Automatic offset compensation***

Very few examples of parallel ion channel recording platforms are currently present in literature, due to the complexity of the setup. However, single-junction Ag/AgCl electrodes suffer of intrinsic voltage offsets, due to the electrode-buffer interface variability. This is very critical, since ion channel recording requires high accuracy (pA resolution) within the full scale (nA range), limiting the operability of the measurement, especially on a multichannel approach. In





this paragraph, an automatic voltage offset correction system is presented, showing the design and the implementation on the multichannel platform, that allows offset-free recording of ion channel signals.

The voltage offset variability of the interface between the Ag/AgCl electrodes and the KCl buffer solution in the biosensor devices, schematically represented in Fig. 84, is a well known electrochemical problem, especially in voltammetry, patch clamp and ion channels acquiring systems [NehSak95], previously explained in Chapter 1, Fig. 8.

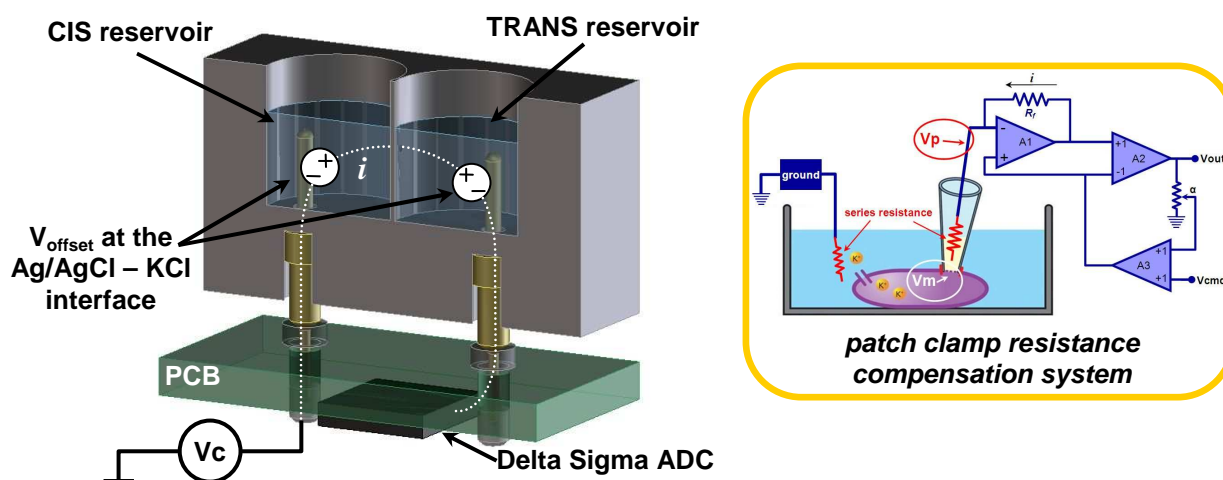
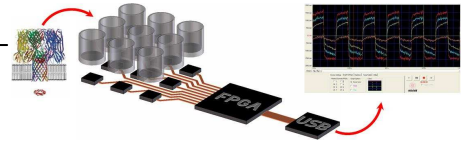


Fig. 84 – Voltage offset at the electrodes Ag/AgCl –KCl buffer interface on sectioned microfluidic device, compared with the patch clamp resistance compensation system.

Different approaches have been proposed to solve this problem, such as three electrode systems (Ag/AgCl plus Au or Pt electrode [Triroj06]), liquid junction, and agar-salt bridge [Shao07]. However, these approaches are usually used into single or multiplexed acquisition systems, where a single measurement instrument is switched between the channels without taking into account crosstalk and routing issues arising on concurrent signal acquisition on multichannel arrays.

The crosstalk at the amplifier input stage of the Delta Sigma ADC is the effect of the array approach, where a unique stimulus (the control voltage signal) feeds all the sensors of the array. Particularly, small differences between sensors, detectable through variations of the equivalent impedance of the micro hole, are mapped into relevant voltage offset variations at the input of the ADCs. Moreover, the input of the Delta Sigma ADC presents different impedances, due to the intrinsic tolerances in the technology process parameters of the chip fabrication. These differences affect the measured current, especially during the initial steps of the acquiring process, where a zero input current is required to correctly initialize the system. On the other hands, unknown offsets over the supply signal of the biosensor affect the accuracy of the measure, especially during voltage-gated ion channels experiments.



The solution is based on an electronic feedback system, employing single-junction Ag/AgCl electrodes, capable to be implemented into platforms for parallel ion-channel recording [Thei10] (Fig. 85). The platform is implemented and tested on a printed circuit board hosting the array where one side is dedicated to the electronic components and the other to the microfluidic array (bottom and top view of Fig. 85 b).

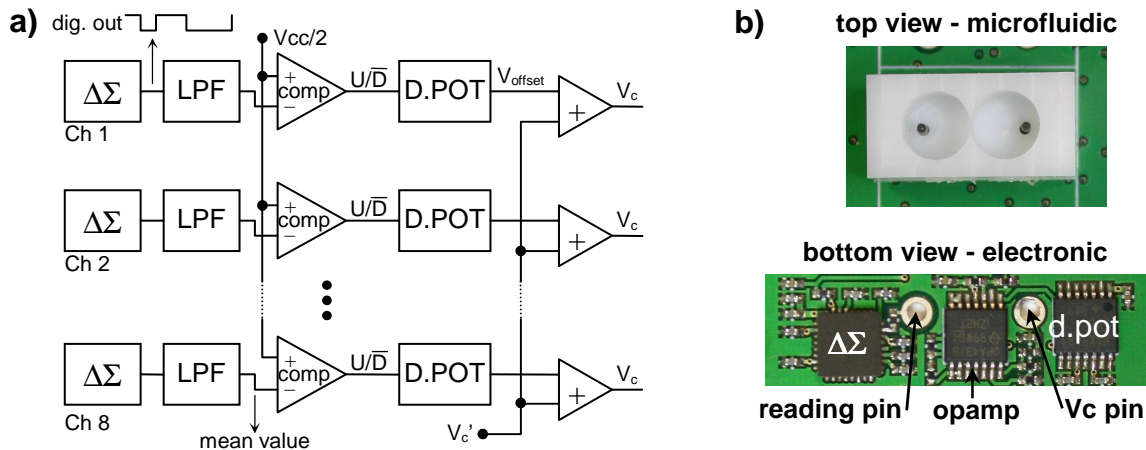
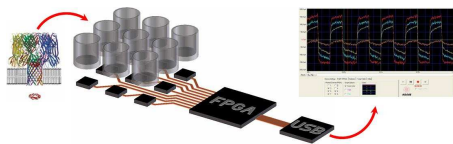


Fig. 85 – (a) The feedback block diagram for Ag/AgCl – buffer interface voltage offset correction within the array approach; (b) detail of one channel section of the PCB implementation with feedback correction and embedded microfluidics.

The first offset correction step consists in the searching for the voltage signal value that sets to zero the corresponding current signal. The obtained value becomes the virtual ground reference for the selected channel of the system. The proposed approach is based on an automatic voltage offset correction, operating independently and simultaneously on each channel of the array. The offset correction is implemented using the digital output of the Delta Sigma ADC employed for the acquisition [Benn09]. Since the Delta Sigma ADC output is a digital signal proportional to the oversampled analog input, it is possible to extract the original offset value by integrating the single bit digital output stream during the setup phase by a LPF stage. To store permanently the offset voltage value provided by the LPF, a digital potentiometer is used, connected between two voltage references in the range of typical Ag/AgCl - buffer electrochemical interface values (hundred of mV). The digital potentiometer resistance variation is driven by the comparison between the low pass filtering of the Delta Sigma output (the *mean value* of Fig. 85 a) and the virtual input ground, corresponding to  $V_{cc}/2$ , that is the voltage value equivalent to a zero measured input current (Fig. 85 a). If the LPF output is greater than the virtual ground, corresponding to the case of a positive input current acquired by the Delta Sigma ADC, the comparator output (signal  $V_c$  of Fig. 85 a) provides a negative saturation, corresponding to a zero logic value (signal  $V_c'$  of Fig. 85 a), allowing to reduce the offset voltage, and the effect is a decrease of the measured current. By this



indication, the digital potentiometer implements the reduction of the output voltage ( $V_{offset}$  of Fig. 85 a), reaching the offset compensation through the negative feedback. The  $V_{offset}$  is linearly added to the common control voltage ( $V_c$ ) to obtain the final  $V_c$ , one to each acquired channel.  $V_c$  is the control signal, corresponding to all the channels feeding for the sensor array that can be set to 80 mVpp triangular wave @ 10 Hz, used to monitor the BLM formation, or a fixed voltage in the range of  $\pm 128$  mV, to supply the ion channel.

The overall procedure for the automatic feedback correction follows the steps illustrated in Fig. 86. Each of them could be automated: i) the microfluidic reservoirs are filled with KCl solution and the micro hole equivalent impedance is electronically verified; ii) the voltage offset is corrected and stored into the digital potentiometer; iii) artificial BLM is formed and electronically verified by detection of the impedance modification, evaluating the equivalent capacitance; iv) ion-channels are inserted into BLMs by means of  $\alpha$ -hemolysin proteins; v) signals are recorded and displayed in real time using a PC-based graphical user interface.

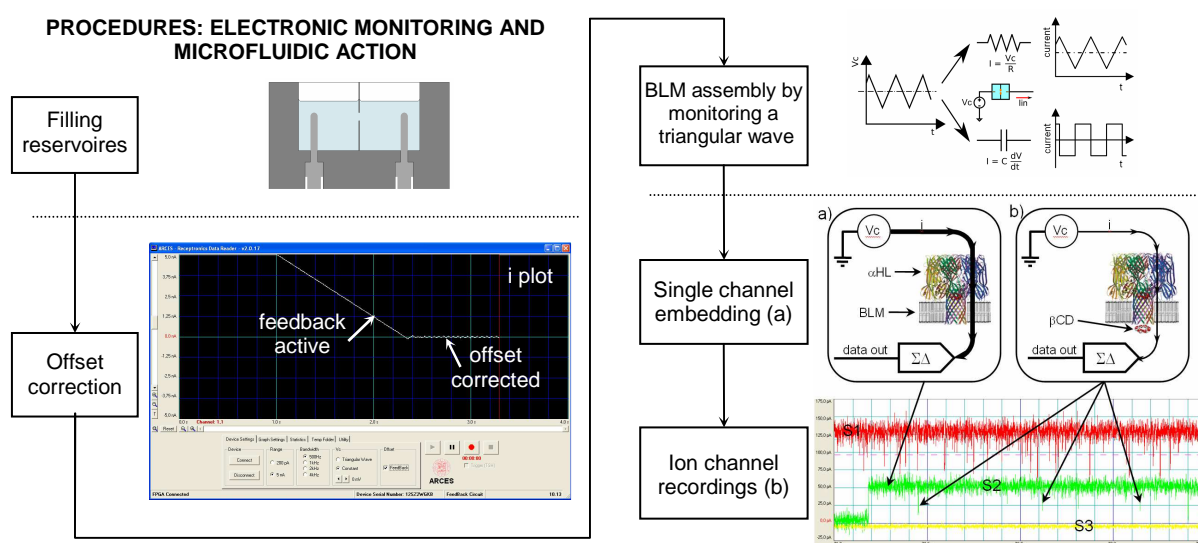
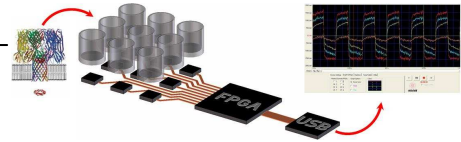


Fig. 86 – Flow chart of the overall operational procedures for the automatic offset correction and multiple ion-channel recordings using a lipid bilayer membrane array.

The offset setup procedure could be applied on successive phases. The accuracy of the offset correction depends on the resolution, that is number of steps, of the digital potentiometer and from the voltage band gap, centred on the virtual ground potential ( $V_{cc}/2$ ), where the digital potentiometer resistance is connected. These two parameters are strictly related to the selected range and resolution of the measured current. For instance, in the range of 5 nA, with a resolution of the Delta Sigma ADC of 12 bits, the maximum resolution of the measured current is 1,22 pA. The digital potentiometer used is a MAX 5481, with 1024 steps available. Assuming



a voltage band gap of 100 mV, the minimum voltage step to compensate the offset is around 100  $\mu$ V. Considering that a microfluidic setup present a resistance in the order of 10 M $\Omega$ , given by the pore plus the Ag/AgCl electrode resistances, the minimum step in the acquired current is about 10 pA, very close to the zero, considering the 5nA scale.

### ***The final multichannel acquiring platform***

Summarizing, the hybrid platform introduced in *Fig. 81* includes the following design features, to be embedded into the final PCB design:

- 8 Delta Sigma ADC asics to acquire up to 8 simultaneously data channels;
- socket connectors for microfluidic devices plug;
- DAC for Vc generator (selectable for the triangular wave or a command voltage Vc constant);
- input for external analog Vc generator;
- filtering and decimation of the data performed by an FPGA;
- automatic electrode offset correction;
- noise shielding by grounded metal layers on the PCB;
- USB 2.0 data link;
- auto powered from the USB.

By means of the techniques explained in the previously paragraph, the final board is realized, and the electrical schemes are indicated in *Fig. 105*, *Fig. 106*, *Fig. 107*, *Fig. 108*. From the electronic point of view, the block scheme is illustrated in *Fig. 87*.

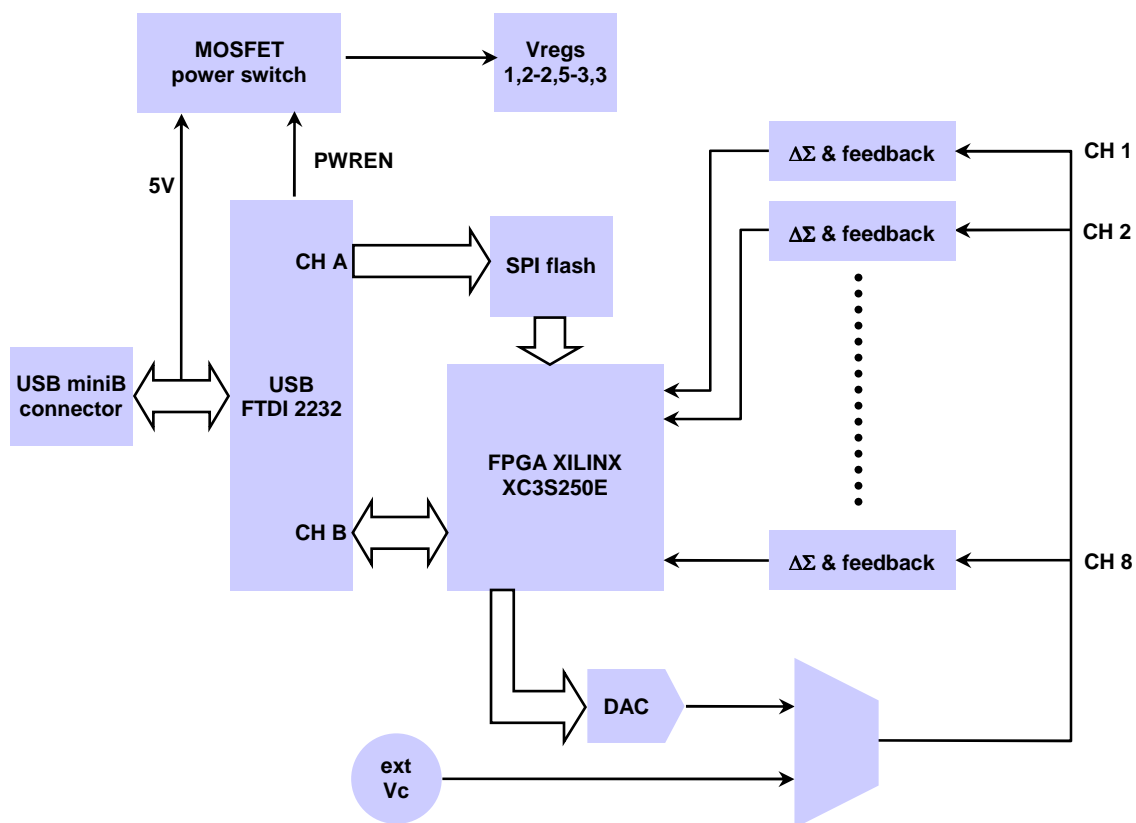
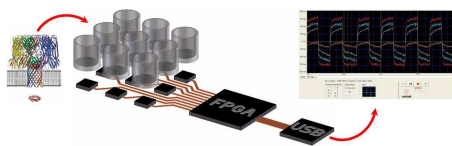


Fig. 87 – 8 channel read out platform block diagram.

The final fabrication of the PCB is shown in Fig. 88, and the PCB-microfluidic assembly is shown in Fig. 89, where singles microfluidic devices are plugged on the related sockets.

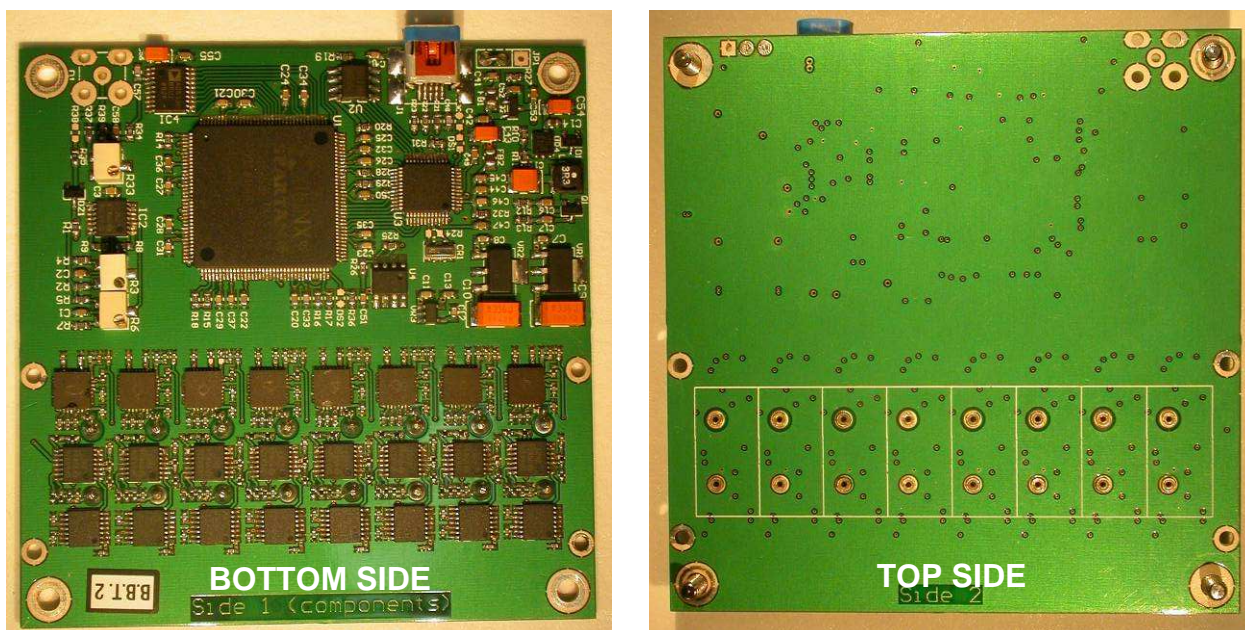


Fig. 88 – Top and bottom view of the ChipArrayRobot PCB, with embedded electronics, digital data elaboration and microfluidic array.

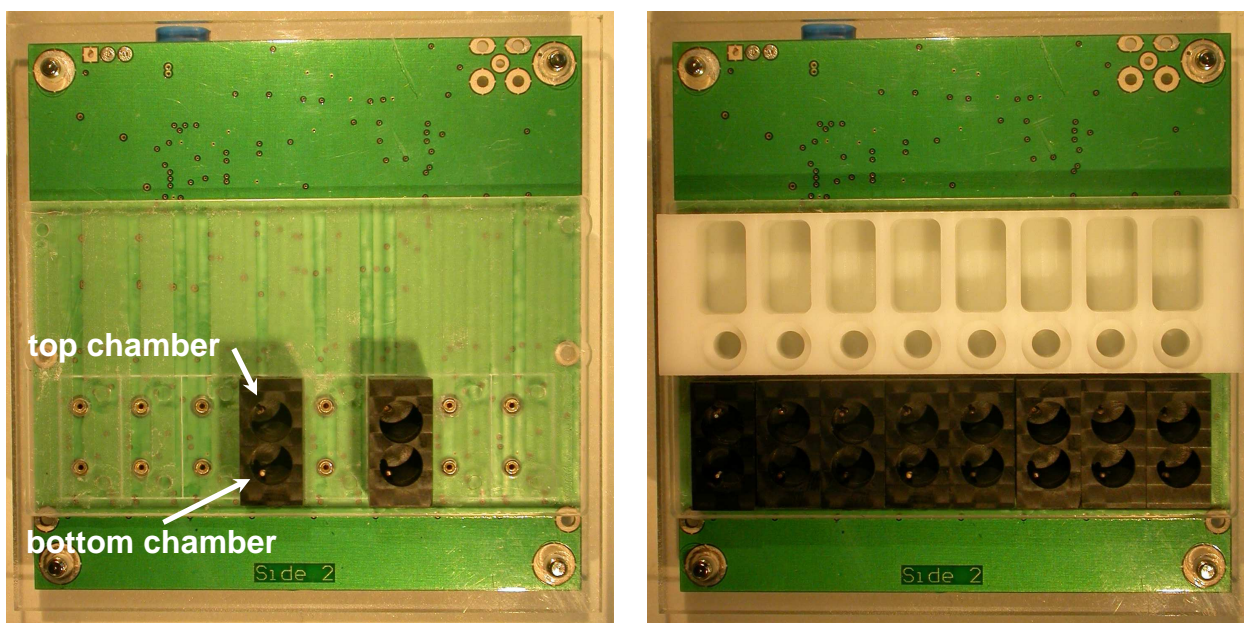
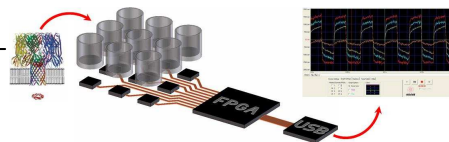


Fig. 89 – Top view of the ChipArrayRobot PCB, with embedded microfluidic devices and reservoirs for compounds storing.

To test the PCB, as proof of concept, a single molecule detection experiment is performed over several channels in parallel way. In these kind of test, ion channels are used to detect single target molecules in solutions, to estimate their final concentration. The test start from the BLM formation on different microfluidic devices of the hybrid platform. As show in Fig. 90, if no lipid bilayer is formed, the microhole of the microfluidic devices acts as an electrical resistor. Hence, the current follows the same shape as the voltage stimulus. When a BLM forms, the circuit element is a capacitor, the current is given by the derivative of voltage stimulus, resulting in a square current waveform. This method is used to monitor formation of the bilayer which is typically 0.5 $\mu$ F/cm<sup>2</sup>.

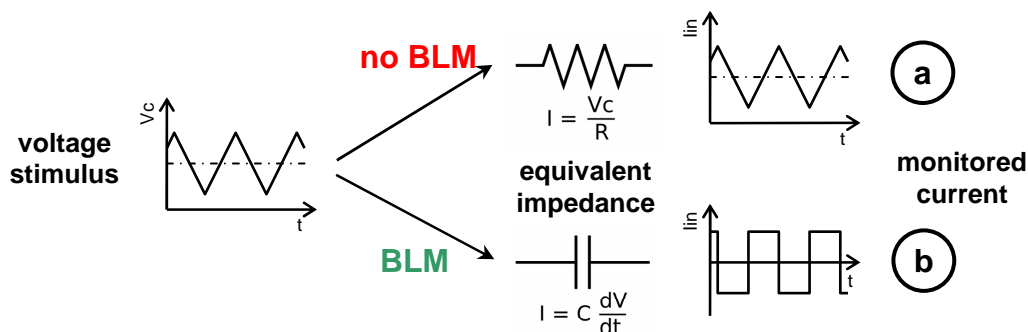
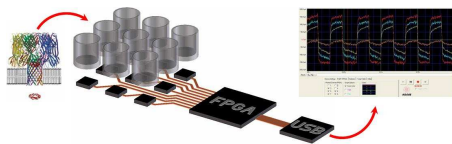


Fig. 90 – Signal response to BLM stimulus signal ( $V_c$ ).

As shown in Fig. 91, BLM formation is automatically monitored by the GUI interface. A triangular 40 mVpp @ 6 Hz signal is generated on the PCB and the corresponding current



monitored by the readout circuits. The typical measured current is about  $200 \text{ pA}_{pp}$ , equivalent to a membrane capacitance of about  $120 \text{ pF}$ , much higher of the septum strain capacitance ( $8\text{-}10 \text{ pF}$  range), which can be neglected.

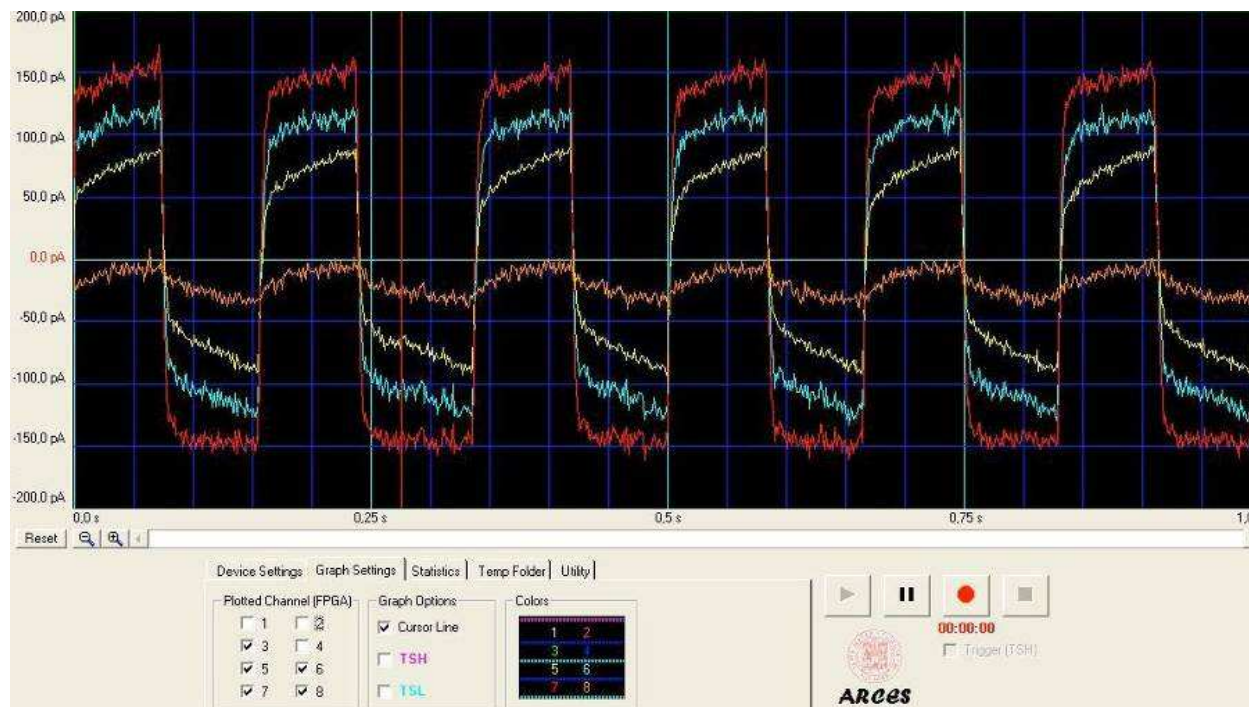
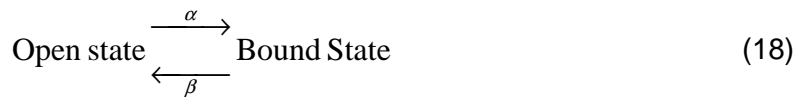
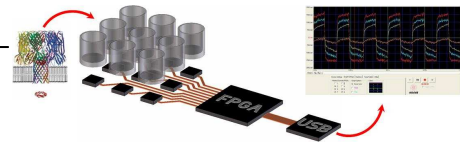


Fig. 91 – Three BLMs formed on the hybrid platform on different channels, monitored by the GUI interface. A triangular  $40 \text{ mV}_{pp}$  @  $6 \text{ Hz}$  signal is generated on the PCB and the corresponding current is monitored by the readout circuits.

For bilayer formation, L- $\alpha$ -phosphatidylcholine from bovine brain (Sigma-Aldrich) was used. BLMs were formed across a  $200\mu\text{m}$  diameter hole separating the two reservoirs. The buffer was  $1 \text{ M KCl}$ ,  $10 \text{ mM TRIS-HCl}$ ,  $1 \text{ mM EDTA}$  (Sigma-Aldrich) in ultrapure water,  $\text{pH } 7.5$ .

As shown in Fig. 92, the readout system was tested by monitoring the current from single  $\alpha$ -hemolysin ( $\alpha\text{HL}$ ) channels in the BLMs. Current pulses were recorded using the  $\beta$ -cyclodextrin ( $\beta\text{CD}$ ) molecule which temporarily modulates the ion-current [Gu00].  $\alpha$ -Hemolysin was added to the top chamber of Fig. 89 to a final concentration of  $10 \text{ ng/ml}$ .  $\beta\text{CD}$  was added to the bottom chamber at varying concentrations in the  $\mu\text{M}$  range. As is well known, the larger the bandwidth the higher the temporal resolution and the lower the signal-to-noise ratio. This trade-off is particularly useful for spike detection and can be set in real time using the GUI interface.

Once current spikes are detected by the readout system, the data can be used for stochastic sensing [Bayley01], and it is possible to measure the  $\beta\text{CD}$  molecular concentrations by correlating current spike information. Interactions between  $\alpha\text{HL}$  pores with  $\beta\text{CD}$  molecules can be modeled by a two state continuous time Markov chain:



where  $\alpha$  and  $\beta$  are the binding and unbinding rate constants, respectively [NehSak05] [DeFelice81].

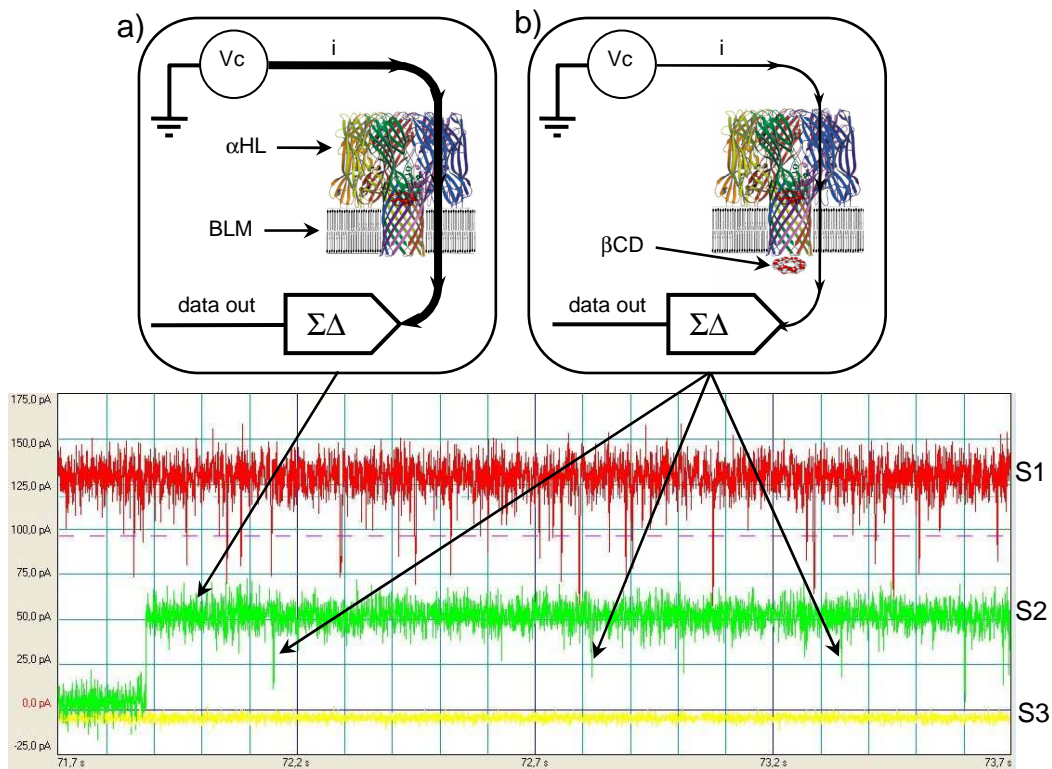


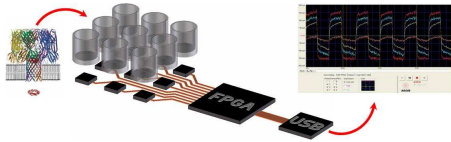
Fig. 92 – Current modulation due to  $\alpha$ HL pores, with  $\beta$ CD molecules. When no ion channel is embedded into BLM, no current flows (S3, yellow). (a) After insertion of a  $\alpha$ HL protein into a BLM, a constant current (S2, green trace) is detected through the membrane. (b) Stochastic binding of  $\beta$ CD molecules with  $\alpha$ HL pores gives current spikes due to the blockage of ions through the pore (S2, green trace). The red S1 trace shows two simultaneously  $\alpha$ HL pores opened.

Whilst  $\alpha$  depends on  $\beta$ CD concentration in solution,  $\beta$  is independent on this value, depending only on the strength of binding with the  $\alpha$ HL channel and the thermal energy of the system. An estimation of the rate  $\alpha$  allow the estimation of  $\beta$ CD concentration in solution through:

$$\alpha = \alpha' \cdot [\beta\text{CD}] \quad (19)$$

where  $\alpha'$  has units  $\text{s}^{-1}\text{M}^{-1}$  and  $[\beta\text{CD}]$  is the molar concentration of  $\beta$ -cyclodextrin. At a constant concentration  $[\beta\text{CD}]$ , the probability that a  $\beta$ CD molecule binds to the pore during  $\Delta t$  is  $\alpha\Delta t + o(\Delta t)$ , where  $o(\Delta t)$  is negligible for small  $\Delta t$ . Considering the lifetime of the  $\alpha$ HL channel, the interval in which the pore is fully open between two consecutive blockades is a continuous





random variable with behaviour described by a probability density function (PDF) where the open lifetime distribution is exponential with an average equal to  $\tau=1/\alpha$  [NehSak05] [Bayley01].

Fitting the vacant time histogram allows us to calculate the time constant, which depends on  $\beta$ -cyclodextrin concentration through:

$$\tau = \frac{1}{\alpha} = \frac{1}{\alpha' \cdot [\beta CD]} \quad (20)$$

Because of the stochastic nature of this kind of sensing, the longer the acquisition time (and the more events) the more reliable is the measure of concentration. Unfortunately, one of the main problems of BLM-based sensor is the fragility and stability over time of the membrane. It is now clear the reason of a need for a parallel setup, because it allows to acquire data from ion channels on different bilayers over several hours (typical lifetime of BLMs), thanks to the intrinsic stochastic property of the sensing system, that allow to combine, on equal terms, data from multiple sensors. Other researchers are trying to develop protocols to extend the lifetime of the lipid membranes [Schmidt08], however, concentration values are sensitive to slow diffusion and thermal gradients, therefore the acquisition time becomes a critical parameter, especially for very low target concentration. For these reasons, the array approach is advantageous since it allows a reduction in acquisition time that is proportional to the number of independent working BLM with embedded ion channels, because the possibility of simultaneously acquiring independent data, also gains an improvement in sensitive.

Fig. 93 shows a parallel recording of  $\alpha$ HL pores on three microholes and the approach adopted for stochastic sensing. Current spikes caused by single  $\beta$ CD molecules are acquired by filtering at 500 Hz.

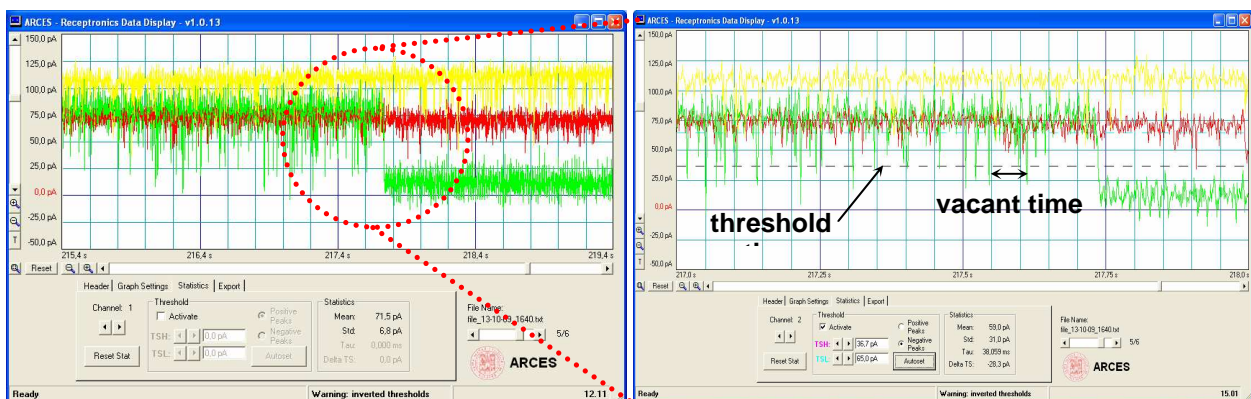
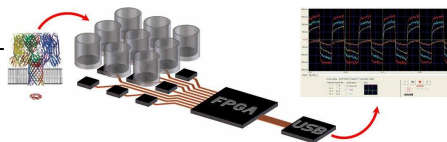


Fig. 93 – Parallel recording from three different BLMs on three independent microholes (blue, red and yellow traces), each with a different number of simultaneously open nanopores. Spikes events, caused by partial blocking of  $\alpha$ HL channels by  $\beta$ CD, are determined using a threshold. Vacant times are averaged over the acquisition time and correlated to concentration using equation (3). The GUI interface allows real-time calculation of  $\beta$ CD concentration using stochastic sensing approach.



At this low bandwidth they are clearly identifiable above the noise floor. Using a threshold as a trigger, vacant times are registered, stored and averaged in registers. This operation is performed for different known concentrations of target molecules in solution, allowing an estimate of  $\alpha'$  by interpolation. Using concentrations of  $40\mu\text{M}$ ,  $60\mu\text{M}$  and  $80\mu\text{M}$ , we determined  $\tau = 103\text{ms}$ ,  $75\text{ms}$  and  $43\text{ms}$ , respectively. The experimental data yields a value of  $\alpha' = 2.6 \times 10^5 \text{ s}^{-1} \text{ M}^{-1}$  which is in agreement with literature [Gu00]. Once the value of  $\alpha'$  is calculated, it is possible to estimate any unknown concentrations of  $\beta\text{CD}$  from equation (20). Once a threshold is fixed, the GUI interface automatically calculates the value of  $\tau$  and enables  $\beta\text{CD}$  concentration to be determined in real-time. It is important to point out that this approach constitutes a highly quantitative analytical detection system. Additionally, as already demonstrated [Ervin09], stochastic sensing could even be performed by employing multiple ion channels in the same membrane, improving the overall sensitivity of the system.

# Chapter 5

## Platform perspectives

### Fully automatic system

As conclusion of the presented work, the proposed hybrid platform for ion channel low noise signal acquisition in parallel format, reported in Fig. 94, is completely designed, realized, and implemented in a fully performing system. The electronic performances are evaluated by the

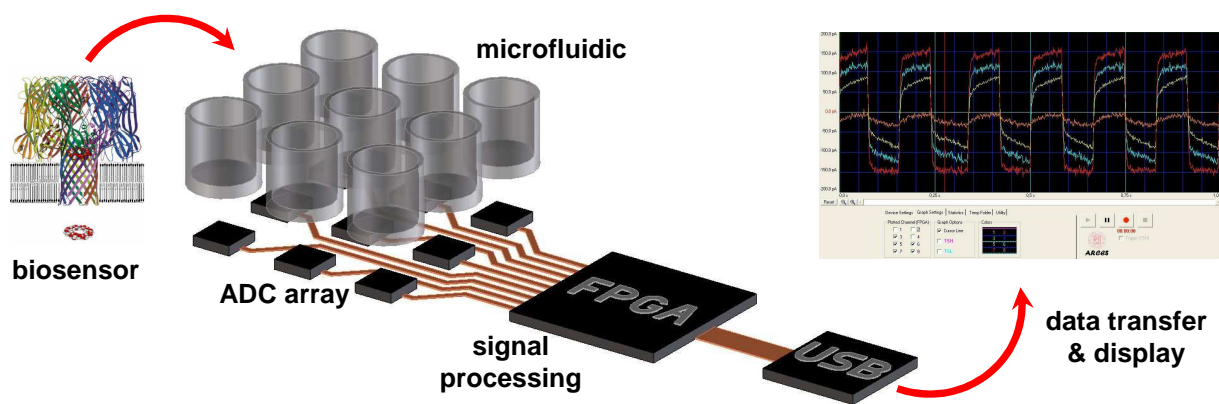


Fig. 94 – Hybrid technology concept for heterogeneous system approach.

single molecule detection technique, explained in Chapter 4, on different channels running simultaneously. The low noise vs. bandwidth and resolution tradeoff (see Chapter 2) is successfully validated from the measured performances of the integrated acquisition front end, and satisfies the characteristics required for the designed purpose.

Starting from single channel acquisition systems, several microfluidic platform has been tested, to reach the final multichannel array system. Typically, a manual procedure to run the experiments is applied, regarding the BLM formation by means of painting technique (see Chapter 1), manual perfusion of  $\alpha$ HL proteins and  $\beta$ CD molecules to acquire single molecule gating activity on  $\alpha$ HL ion channels.

As final step, the platform has been integrated into a fully automatic system for dispensing chemical solutions and compounds, in particular the KCl buffer and the lipid solution, for the final target to get BLMs in parallel format on several independent microfluidic device. The overall system is presented in Fig. 95, with some details enlarged in Fig. 96.

The actual yield of BLM formation, using a Montal Muller protocol [Rossi10], is around 50% (see Fig. 91), and it is strictly related to the quality of the microfluidic devices used. In fact, since

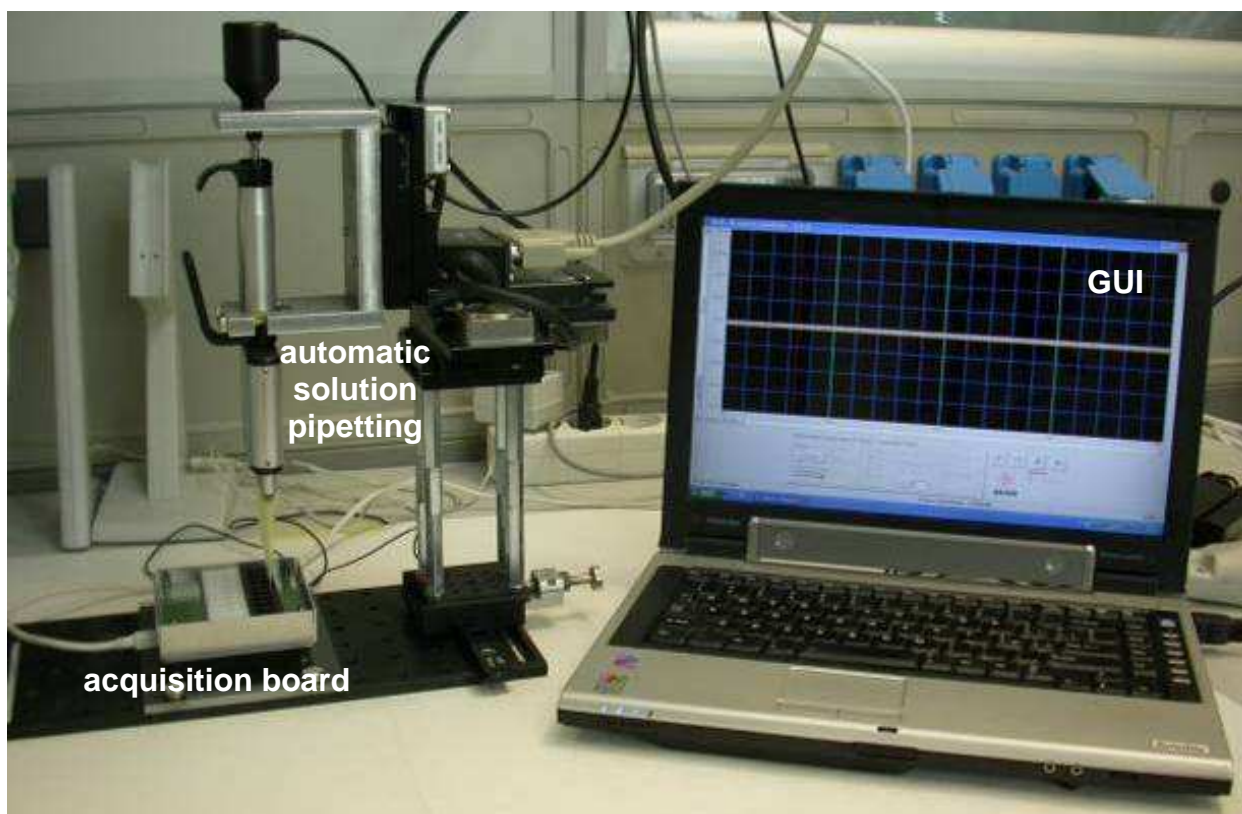
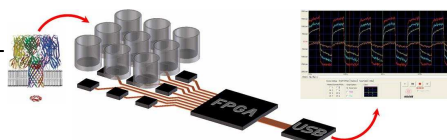


Fig. 95 – Hybrid acquisition platform integrated into a fully automatic system for dispensing chemical solutions and compounds, for parallel BLM formation on several independent microfluidic devices.

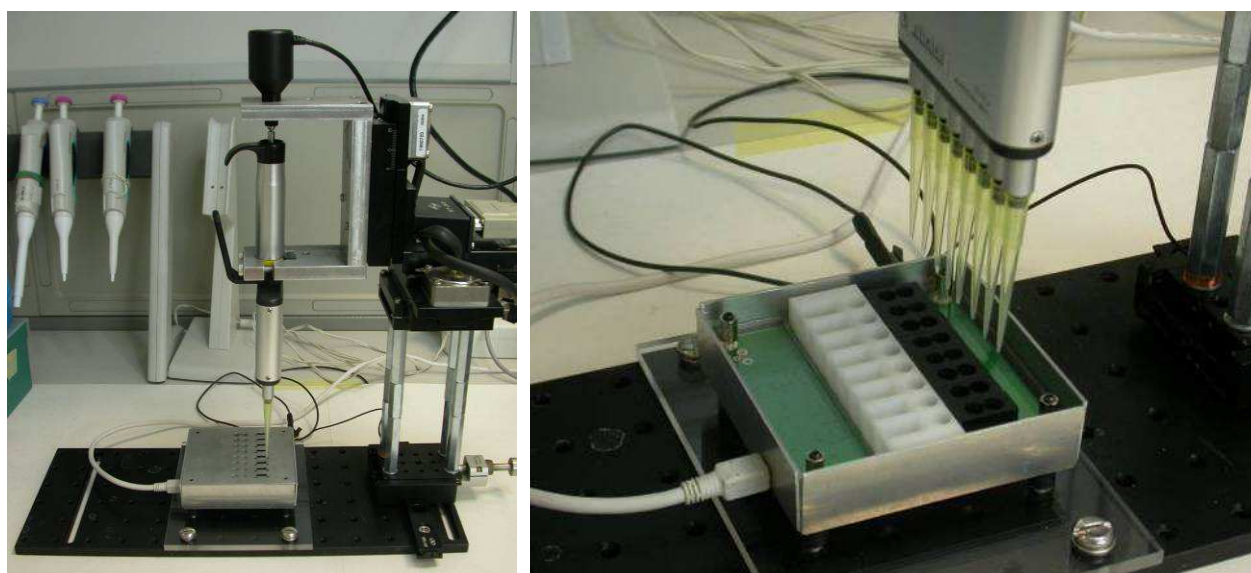
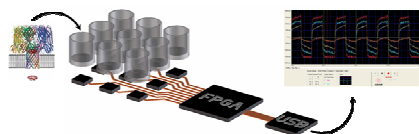


Fig. 96 – Details of the automatic solution dispenser. A micromanipulator (Sutter Instruments) moves an 8 tips pipette dispenser over the acquisition platform, to dispense buffer and lipids for automatic BLM formation.

some defects in the milling process for the microfluidic fabrication, due to a not standard industrial approach, that usually means the usage of Control Numerical Computer machining

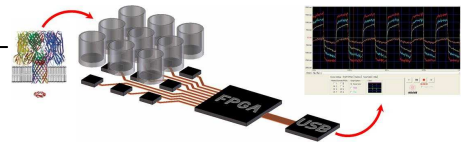


tools for the large scale manufactory producing, the microfluidic devices are not perfectly equals, determining the yield rate reported. However, that means that the approach is promising, by refining the microfluidic devices fabrication.

## Future perspetcives

The platform has been tested also over different microfluidic system developed from Germany companies like Nanion (the Port-A-Patch system [Nanion1]) and Ionovation (the Ionovation Compact system [Ionovation1]). A short test was done also at the University of Twentee, (NL), over a microfluidic glass chip for BLM formation by capillarity process [Stimberg10]. These experiences demonster an extra advantage of the developed acquisition platform, in terms of adaptability and flexibility of the interface, plus a real interest from industrial companies into the development of HTS systems.

This work describes a design methodology of nanosensor array based on a hybrid system approach where integrated electronic sensing and a fluidic devices are embedded on a single platform. A concurrent readout procedure, based on arrays of delta sigma converters is described. Using this technique it is possible to acquire simultaneously data from multiple BLMs, and by adequate signal processing, storing and display on a host PC. Experimental results demonstrate the formation of the lipid bilayer, single molecule detection and stochastic sensing. Although the noise performance of the integrated interface is below that of state of the art laboratory instrumentation, experiments show that the full functionality of the system enable acquisition of single molecule events within an integrated, stand-alone system. Improvements to the electronic interface and the fluidic structure of the platform are currently being pursued and it is anticipated that this will lead to a new generation of high performance fully automatic bilayer recording and processing system.



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# Index of abbreviations

ADC	Analog to Digital Converter
Ag/AgCl	Silver/Silver Chloride
ASIC	Application Specific Integrated Circuit
BLM	Bilayer Lipid Membranes
CNC	Computer Numerical Control
$\Delta\Sigma$	Delta Sigma
DSP	Digital Signal Processing
FIR	Finite Impulse Response digital filter
FPGA	Field Programmable Gate Array
GUI	Graphical User Interface
HTS	High Throughput Screening
KCl	Potassium Chloride buffer solution
LPF	Low Pass Filter
OSR	Over Sampling Ratio
PCB	Printed Circuit Board
USB	Universal Serial Bus
$\alpha$ HL	Alpha Hemolysin protein
$\beta$ CD	Beta Ciclodextrin



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- [1] F. Thei, M. Rossi, M. Bennati, M. Crescentini, M. Tartagni, "An Automatic Offset Correction Platform for High-Throughput Ion-Channel Electrophysiology", EUROSENSORS XXIV, Linz, 2010
  
- [2] M. Rossi, F. Thei, H. Morgan, M. Tartagni, "A Disposable Microfluidic Array Platform for Automatic Ion Channel Recording", MicroTAS, Groningen, 2010
  
- [3] F. Thei, M. Bennati, M. Rossi, M. Crescentini, M. Tartagni, "Concurrent Acquisition Approach for High Resolution Sensor Arrays", SENSORDEVICES 2010, Venice, 2010
  
- [4] F. Thei, M. Rossi, M. Bennati, M. Crescentini, F. Lodesani, H. Morgan, M. Tartagni, "Parallel Recording of Single Ion Channels: A Heterogeneous System Approach", IEEE Transaction on Nanotechnology, 1536-125X, May, 2010, 0, 9, 3, 295-302
  
- [5] M. Crescentini, M. Rossi, M. Bennati, F. Thei, A. Baschiroto, M. Tartagni, "A Nanosensor Interface based on Delta-Sigma arrays", 3rd IEEE International Workshop on Advances in Sensors and Interfaces, IWASI, Trani, Jun, 2009
  
- [6] M. Bennati, F. Thei, M. Rossi, M. Crescentini, G. D'Avino, A. Baschiroto, M. Tartagni, "A Sub-pA Delta-Sigma Current Amplifier for Single Molecule Nanosensors", International Solid State Circuit Conference, ISSCC 2009, San Francisco, Feb, 2009, 0, 52, 0, 348--350

# Appendix

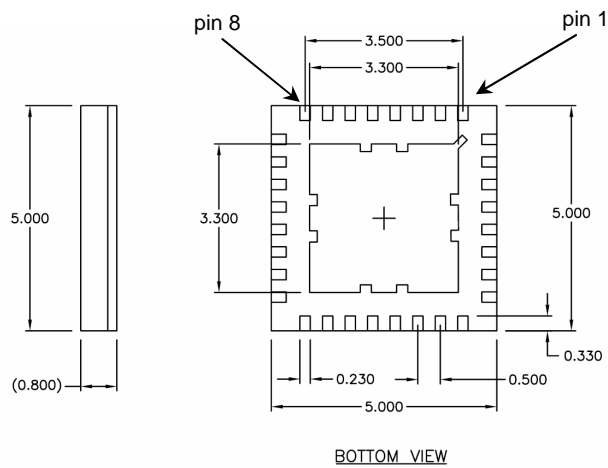


Fig. 97 – QFN 32 pin package.

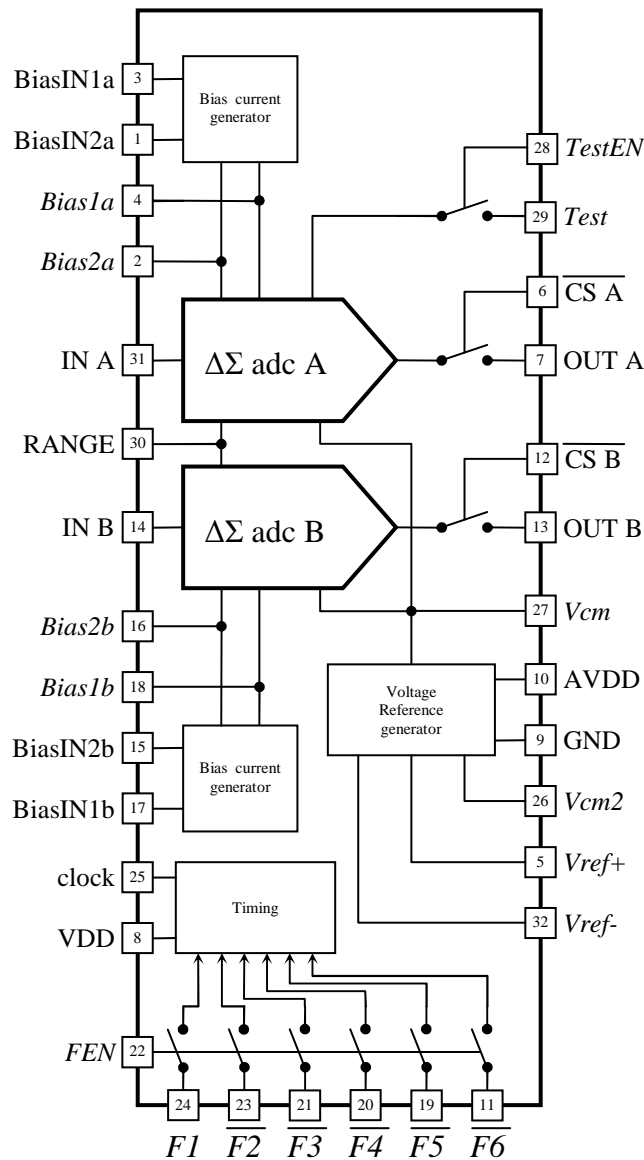


Fig. 98 – ASIC pinout description.

Pin	Name	Dir	Function	Range
1	BiasIN2a	in	Generate internal current reference, connect to AVDD (3,3 Volt)	3,3 V
2	<i>Bias2a</i>	in	Test pin	
3	BiasIN1a	in	Generate internal current reference, connect to AVDD (3,3 Volt)	3,3 V
4	<i>Bias1a</i>	in	Test pin	
5	Vref+	in/out	Test pin, typically 1,89 Volt - connect to bypass capacitor of 100nF	
6	/CSA	in	Enable output data channel A, active low	0 – 3.3 V
7	OUT A	out	Output data channel A, tree state	0 – 3.3 V
8	VDD	in	Digital power supply, connect to +3,3 Volt	3.3 V
9	GND	in	Ground (common for analog and digital)	
10	AVDD	in	Analogic power supply, connect +3,3 Volt	3.3 V
11	/F6	in	Test pin	
12	/CSB	in	Enable output data channel B, active low	0 – 3.3 V
13	OUT B	out	Output data channel B, tree state	0 – 3.3 V
14	IN B	in	Current input signal channel B	5 nA max
15	BiasIN2b	in	Generate internal current reference, connect to AVDD (3,3 Volt)	3.3 V
16	<i>Bias2b</i>	in	Test pin	
17	BiasIN1b	in	Generate internal current reference, connect to AVDD (3,3 Volt)	3.3 V
18	<i>Bias1b</i>	in	Test pin	
19	/F5	in	Test pin	
20	/F4	in	Test pin	
21	/F3	in	Test pin	
22	FEN	in	Test pin, connect to GND	
23	/F2	in	Test pin	
24	F1	in	Test pin	
25	clock	in	Clock input, 1 MHz	0 – 3.3 V
26	Vcm2	in/out	Test pin, typically 1,65 Volt - connect to bypass capacitor of 100nF	
27	Vcm	in/out	Test pin, typically 1,65 Volt - connect to bypass capacitor of 100nF	
28	TestEN	in	Test pin, connect to GND	
29	Test	out	Test pin	
30	RANGE	in	Range pin: 1 → max 5 nA; 0 → max 200 pA	0 – 3.3 V
31	IN A	in	Current input signal channel A	5 nA max
32	Vref-	in/out	Test pin, typically 1,41 Volt - connect to bypass capacitor of 100nF	

Tab. 6 – ASIC pinout description.

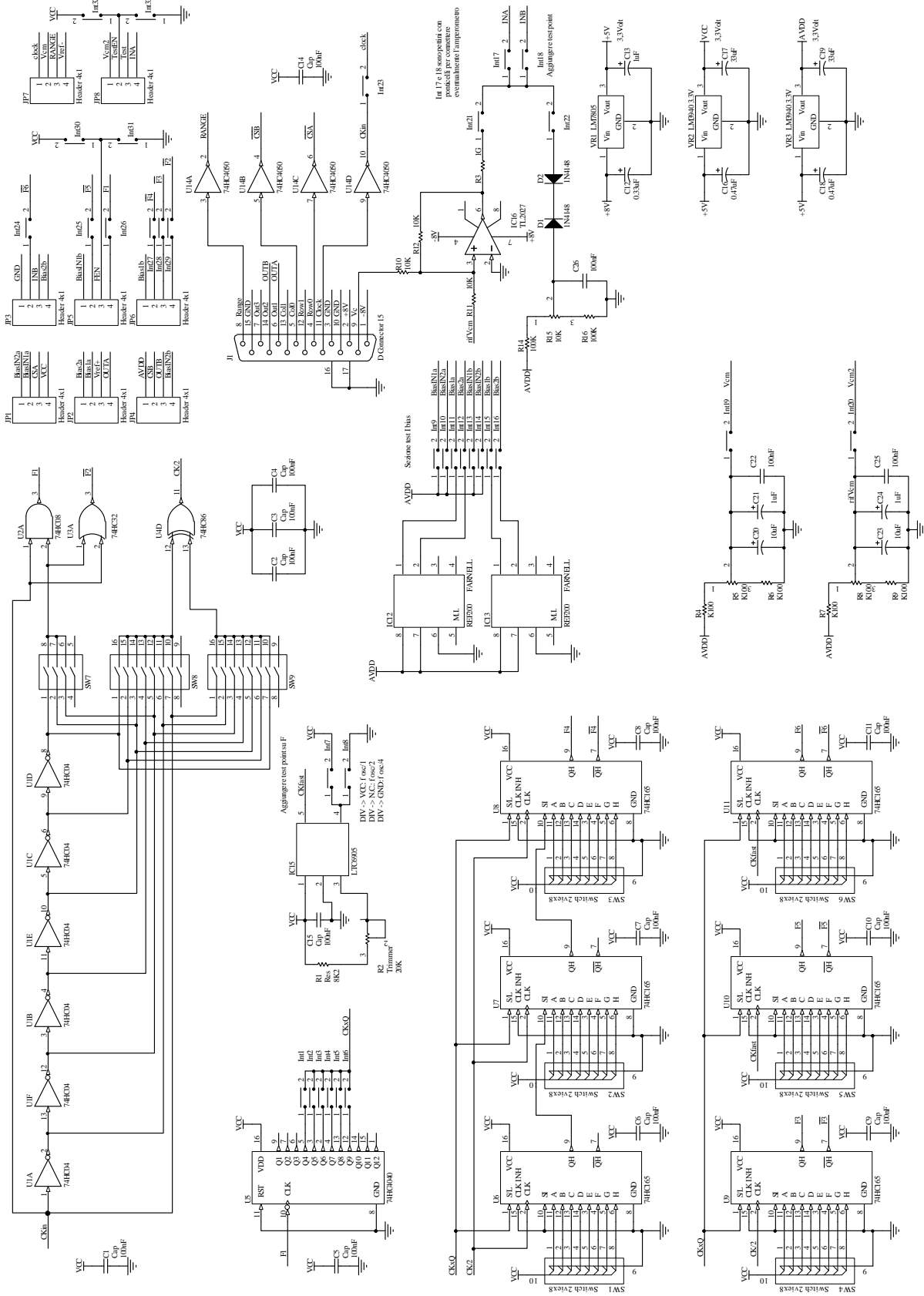


Fig. 99 – Scheme PCB ChipTest.

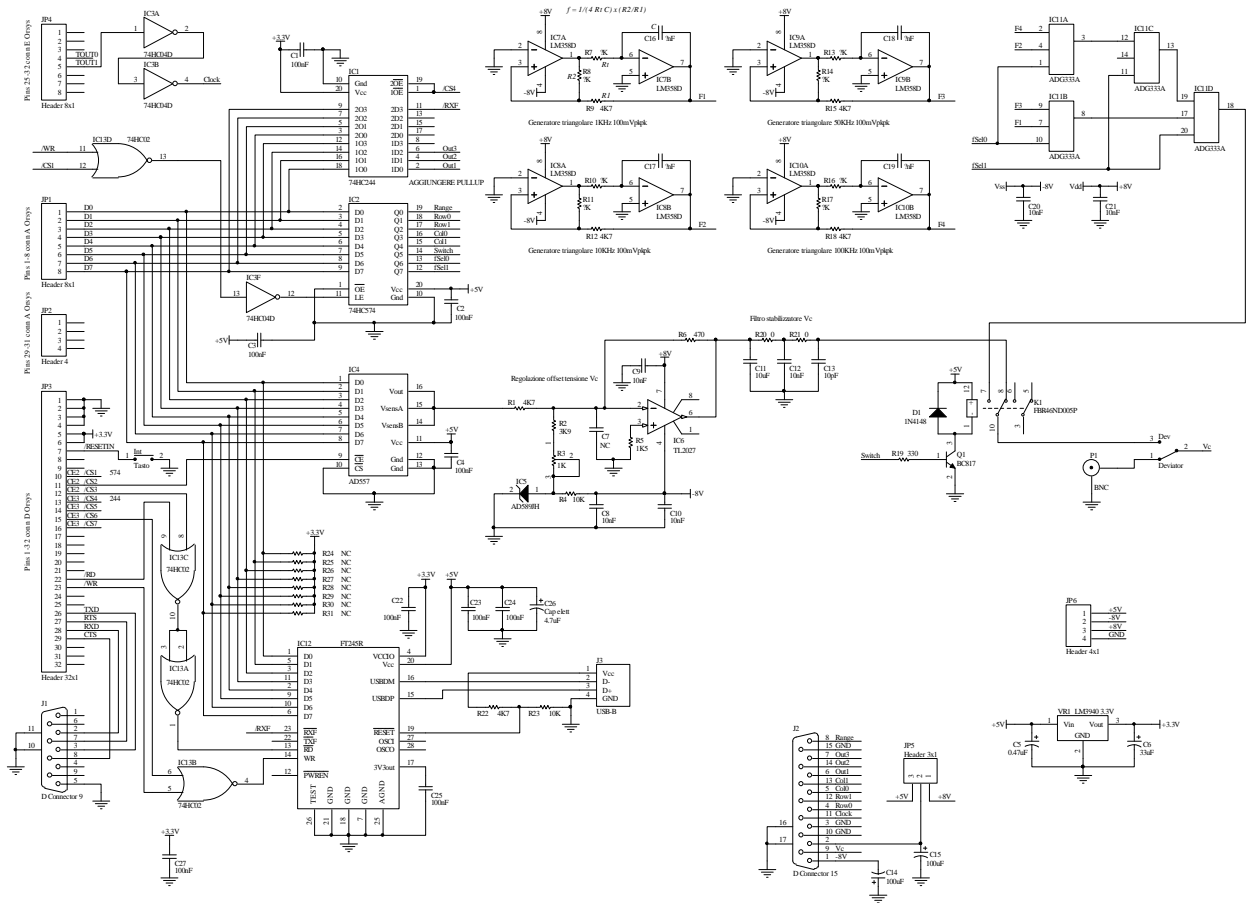


Fig. 100 – Scheme PCB BoardInt

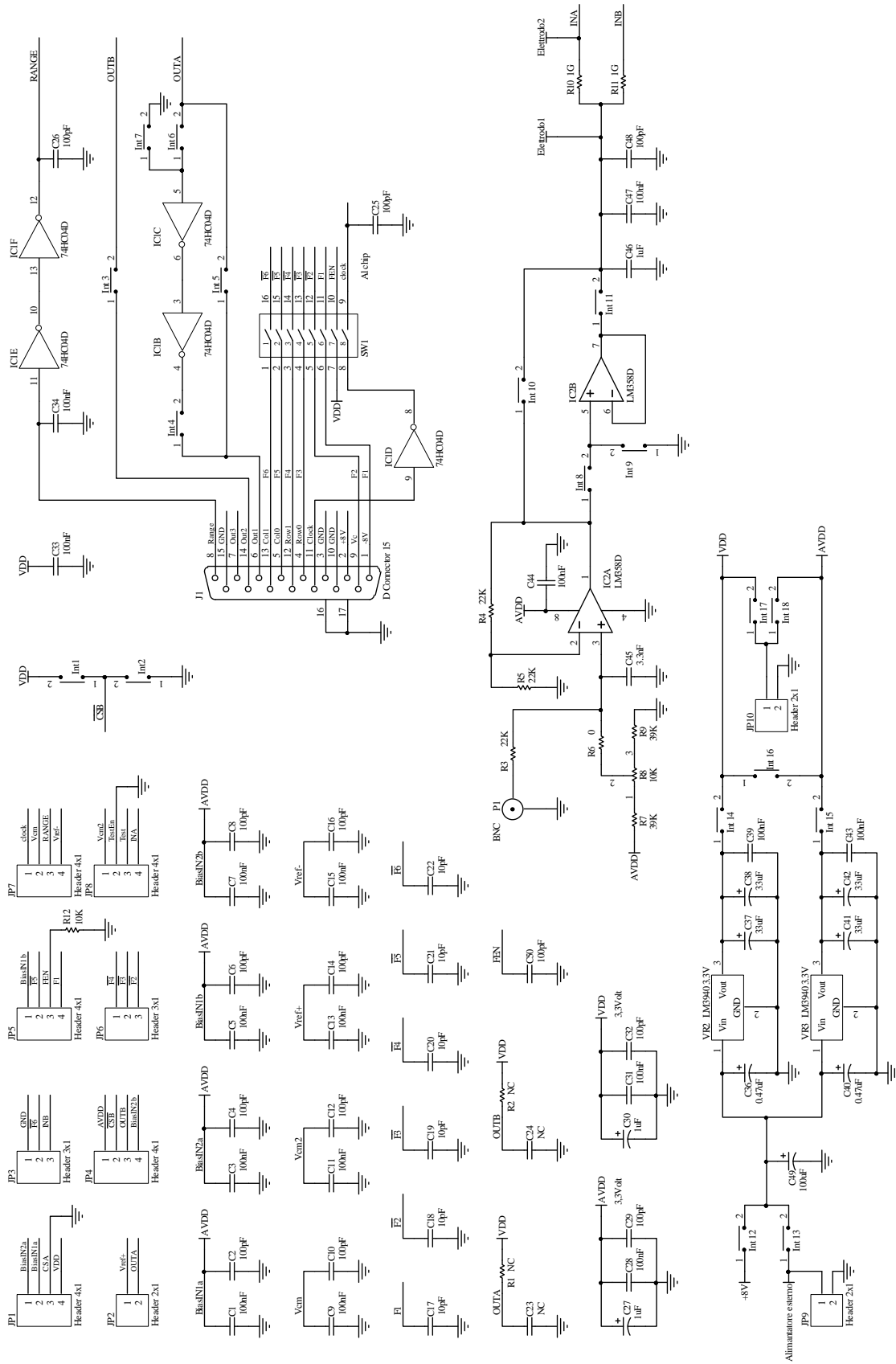


Fig. 101 – Scheme PCB TestChipSensor 1.



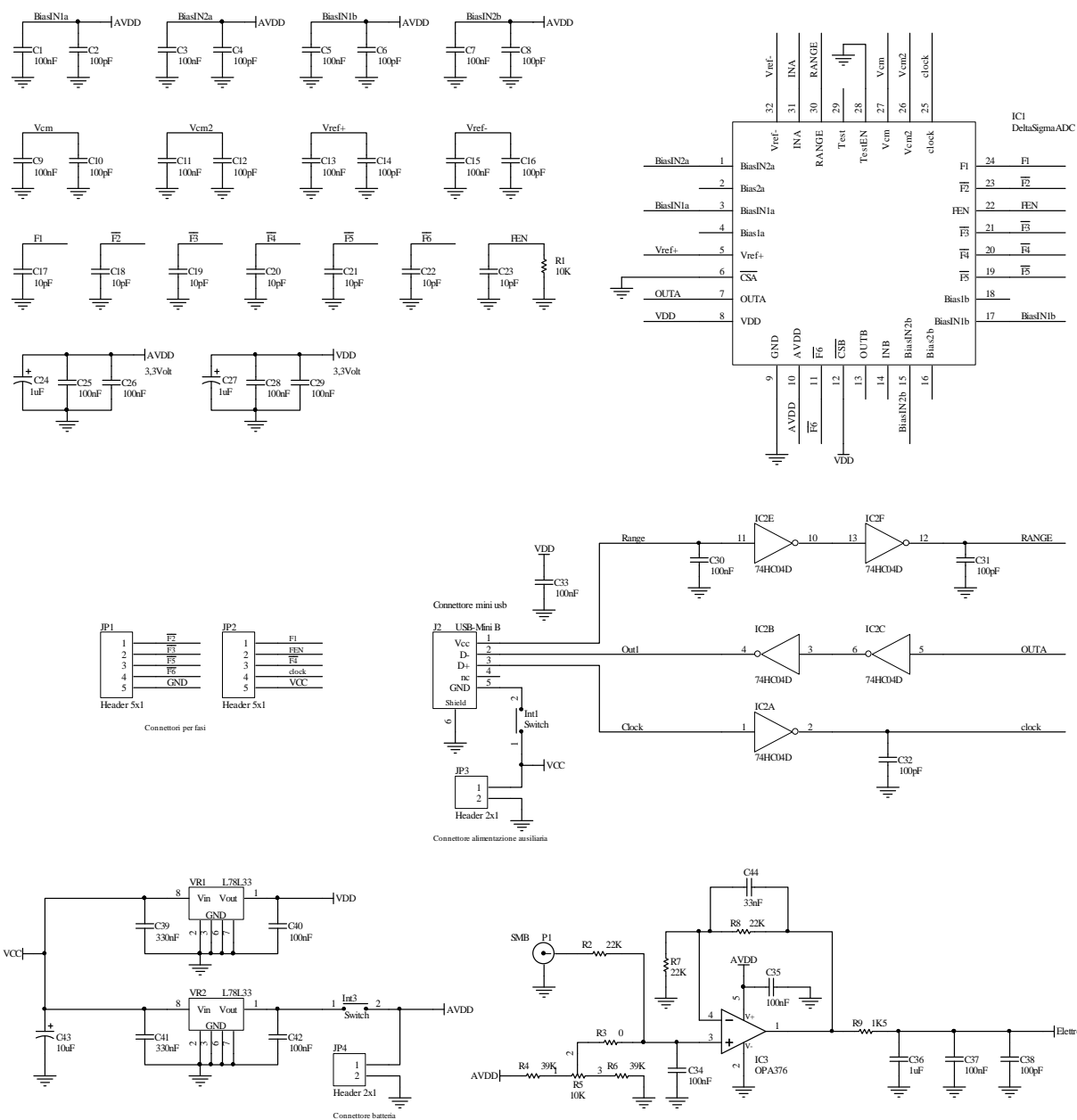


Fig. 102 – Scheme PCB TestChipSensor 2.

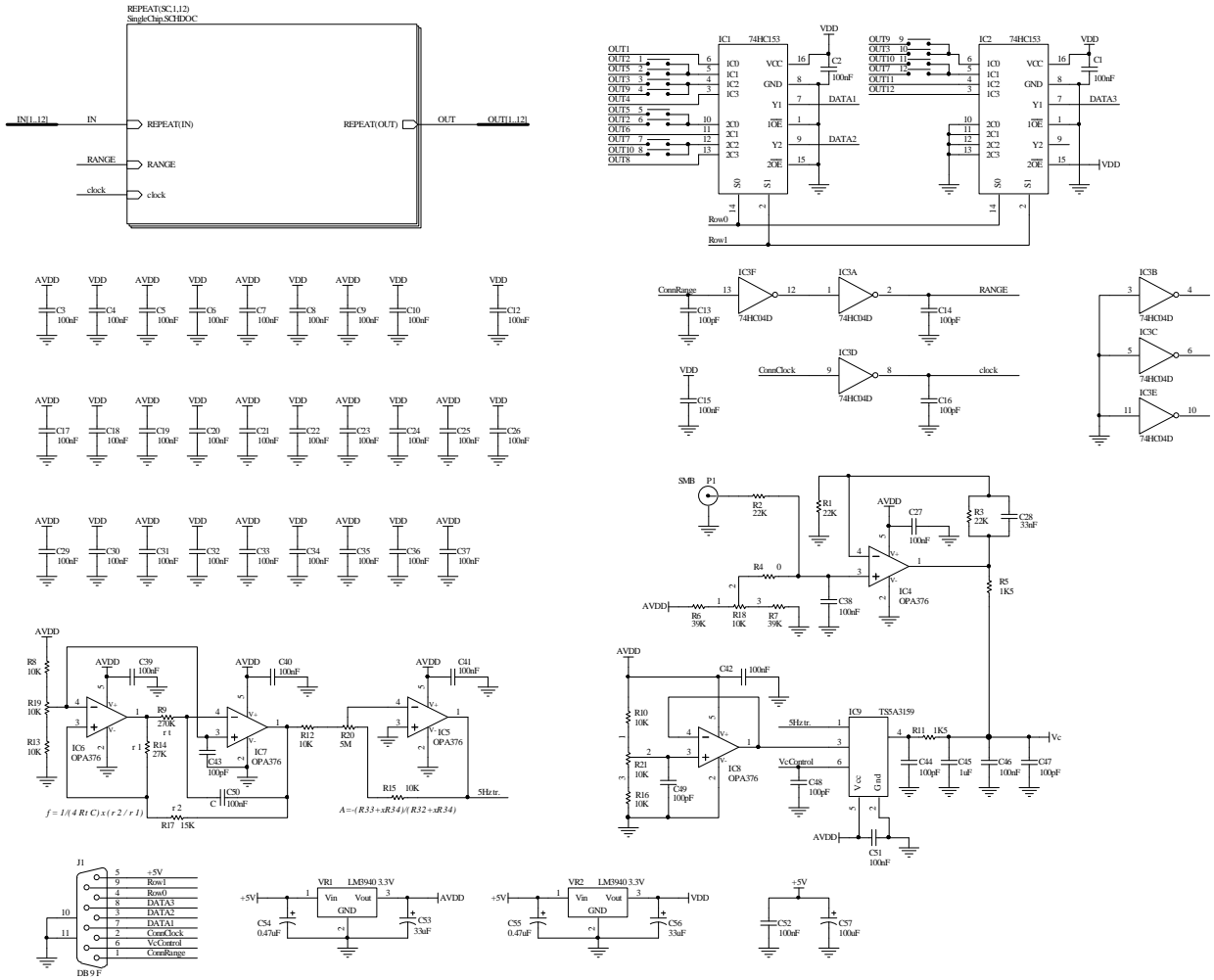


Fig. 103 – Scheme PCB TestChipArray.

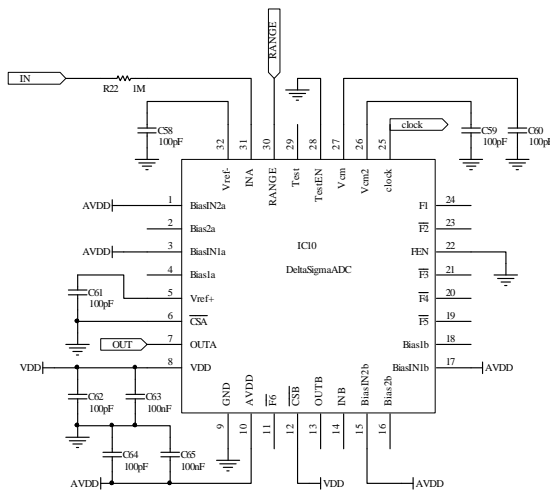


Fig. 104 – Scheme PCB SingleChip (subpart of TestChipArray).



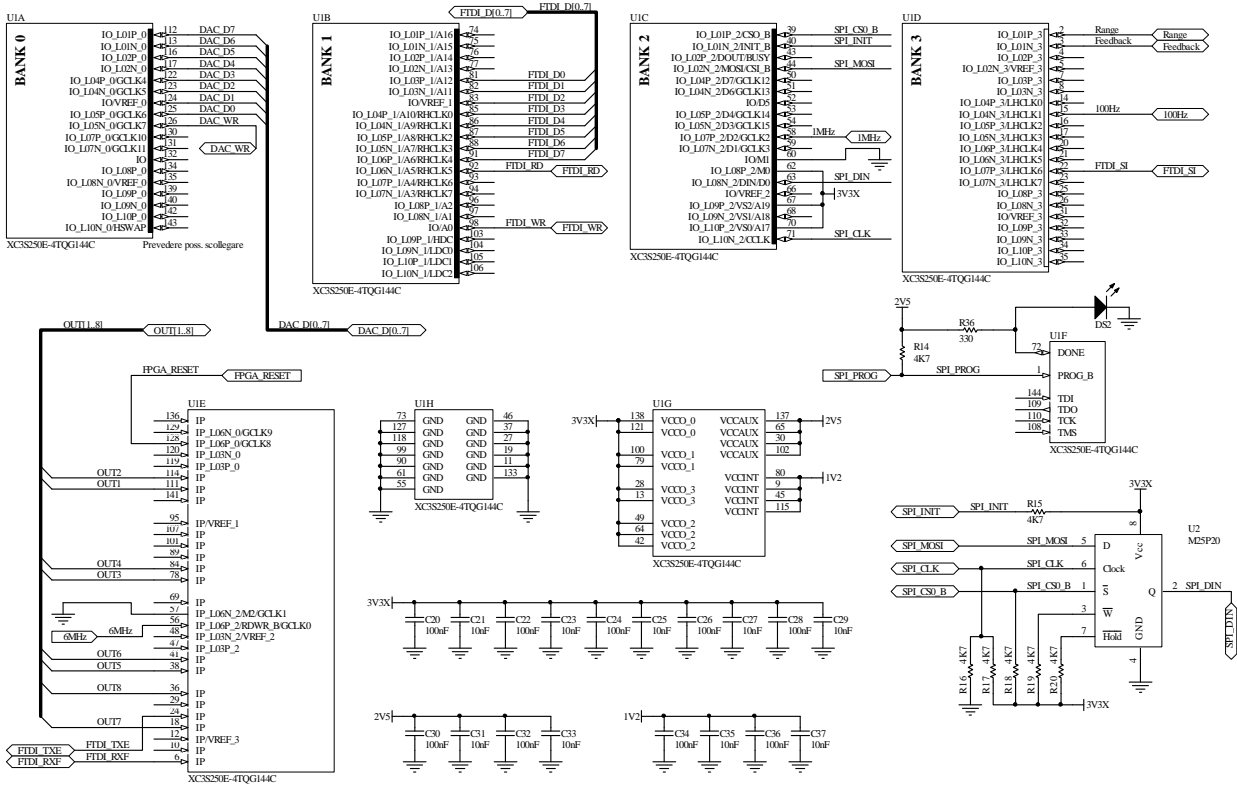


Fig. 107 – Scheme PCB FPGA module (subpart of ChipArrayRobot).

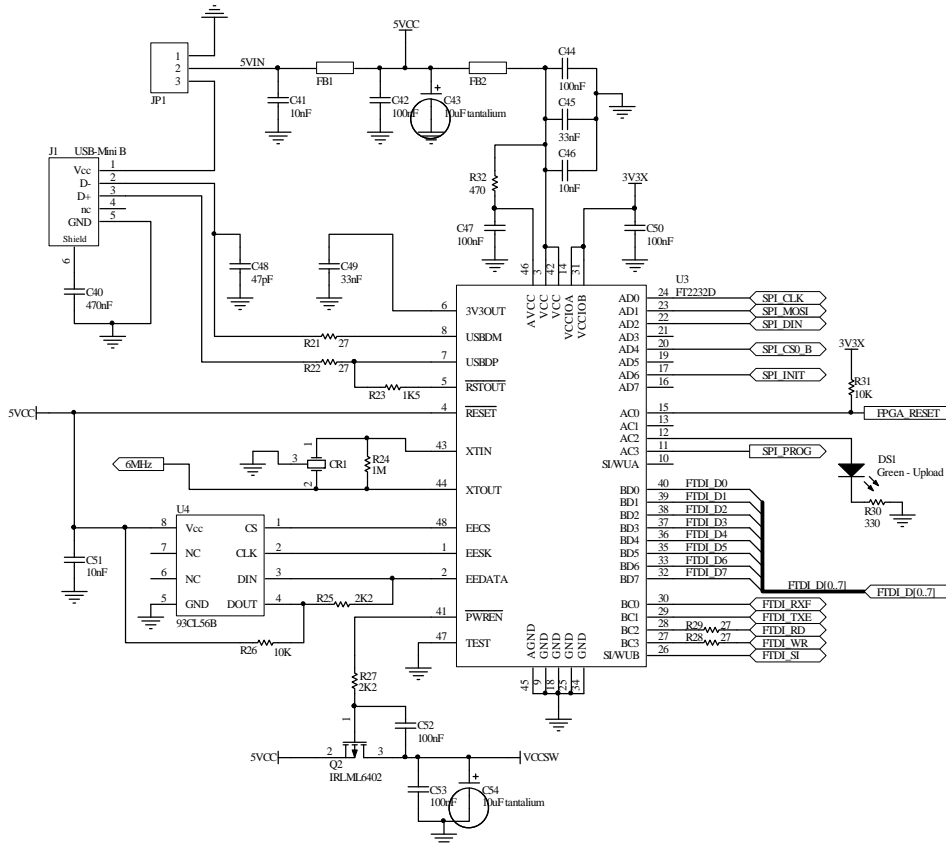


Fig. 108 – Scheme PCB FTDI (subpart of ChipArrayRobot).