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Characterization and Modeling of Low-Frequency Noise in Mosfets

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Contents

List of Figures

List of Tables

List of Symbols and Acronyms

Symbol

b	Variation parameter in electron wavefunction (m^{-1})
C_D	Depletion layer capacitance (Fm^{-2})
C_{GB}	Gate-to-channel capacitance (Fm^{-2})
C_{GC}	Gate-to-channel capacitance (Fm^{-2})
C_{ox}	Gate oxide capacitance (Fm^{-2})
D_{it}	Interface trap density (m^{-2})
ΔE	Coulomb blockade energy (eV)
E_{CS}	Conduction band energy at Si-SiO_2 interface (eV)
E_F	Fermi energy level (eV)
E_{T0}	Trap energy level at flatband (eV)
E_T	Trap energy level (eV)
F_S	Electric field normal to the surface (Vm^{-1})
f	Frequency (Hz)
f_{sw}	Switching frequency (Hz)
g_d	Drain conductance (S)
g_m	Transconductance (S)
$\hbar$	Reduced Plank's constant (Js)
ΔI	RTS amplitude (A)
I_{CP}	Charge-pumping current (A)
I_{DS}	Drain current (A)
k	Boltzmann's constant (JK^{-1})

L	MOSFET channel length (m)
m_0	Electron mass (Kg)
m^*	Effective electron mass (Kg)
m_l	Longitudinal effective mass (Kg)
m_t	Transverse effective mass (Kg)
n	Electron concentration (m^{-3})
n_{2D}	Electron concentration in 2D (m^{-2})
N_A	Substrate doping concentration (m^{-3})
N_C	Conduction band effective density of states (m^{-3})
$N_C(2D)$	Conduction band effective density of states in 2D (m^{-2})
N_P	Polysilicon doping concentration (m^{-3})
P	Noise power (A^2)
$p(z)$	Probability function (m^{-1})
q	Electronic charge (C)
Q_B	MOSFET bulk charge (Cm^{-2})
Q_{inv}	MOSFET inversion charge (Cm^{-2})
S_{id}/I_d	Normalized noise power spectral density of drain current (AHz^{-1})
SS	Subthreshold slope (V/decade)
T	Temperature (K)
t_{ox}	Gate oxide thickness (m)
T_{sw}	Switching period (s)
V_{BS}	Substrate-to-source voltage (V)
V_{DS}	Drain-to-source voltage (V)
V_{FB}	Flatband voltage (V)
V_{GS}	Gate-to-source voltage (V)
V_{TH}	Threshold voltage (V)
v_{th}	Electron thermal velocity (ms^{-1})
W	MOSFET channel width (m)

x_t	Trap position in the oxide with respect to the Si-SiO_2 interface (m)
$\bar{z}$	Charge centroid location of the inversion layer (m)
α_H	Hooge's empirical factor
ε_0	Permittivity of free space (F/m)
ε_{ox}	Oxide relative dielectric constant
ε_{si}	Silicon relative dielectric constant
λ_t	Attenuation wave function coefficient (m)
μ_0	Low field mobility ($m^2V^{-1}s^{-1}$)
μ_c	Mobility limited by Coulomb scattering ($m^2V^{-1}s^{-1}$)
μ_{eff}	Effective mobility ($m^2V^{-1}s^{-1}$)
μ_{fe}	Field effect mobility ($m^2V^{-1}s^{-1}$)
μ_{ph}	Mobility limited by surface acoustic phonon ($m^2V^{-1}s^{-1}$)
μ_{sr}	Mobility limited by surface roughness ($m^2V^{-1}s^{-1}$)
ϕ_F	Fermi potential (V)
ϕ_p	Voltage drop across poly-depletion region (V)
ϕ_s	Surface potential (V)
σ	Capture cross-section (m^2)
σ_0	Capture cross-section prefactor (m^2)
τ_0	Mean time spent in the "low" state of the RTS (s)
τ_1	Mean time spent in the "high" state of the RTS (s)
τ_c	Mean capture time of the RTS (s)
τ_e	Mean emission time of the RTS (s)

Acronym

AC	Alternating current
C-V	Capacitance-voltage
CB	Constant bias
CMOS	Complementary metal oxide semiconductor
DC	Direct current

DUT	Device under test
FSB	Forward substrate bias
FT	Fourier transform
I-V	Current-voltage
IC	Integrated circuit
IFT	Inverse Fourier transform
IP	In-phase with respect to the gate voltage
LNA	Low noise amplifier
MC	Monte Carlo
nMOSFET	n-channel Metal oxide semiconductor field effect transistor
pMOSFET	p-channel Metal oxide semiconductor field effect transistor
OP	Out-of-phase with respect to the gate voltage
PSD	Power spectral density
RF	Radio frequency
RSB	Reverse substrate bias
RTS	Random telegraph signal
SB	Switched bias
Si	Silicon
SiO_2	Silicon dioxide
SMU	Source-measure unit
SRH	Shockley-Read-Hall
WKB	Wentzel-Kramers-Brillouin
ZSB	Zero substrate bias

Chapter 1

Introduction

Semiconductor technology started to be developed more than five decades ago. The first step was made when the bipolar junction transistor was invented in the late 1940s. After deep research in the field, it was possible to create good quality gate oxides in the 1960s-opening the way to the development of metal-semiconductor-oxide field effect transistor (MOSFET). The era of integrated circuits (ICs) was born. The progress of device integration has proceeded for more than forty years following the well-known Moore's law. Gordon Moore, in 1965, made his famous prediction that the number of transistors in an integrated circuit would double every year [1]. Moore's law has been updated in 1975 with a prospected density doubling rate of two years.

The ICs are divided into two main groups: digital and analog/RF. The driving force of digital logic and memory ICs has been the scaling of device size. In this frame, CMOS has been the technology of choice for the digital ICs. Analog and RF circuits for wireless and mobile communication application must meet many other performance specifications. The relationships between device feature size and performance figures of merit are more complex for RF and analog IC applications. RF and analog IC technologies depend on many different materials and device structures to provide optimal solutions. For many years, RF and analog ICs have been mainly developed using bipolar and compound semiconductor technologies due to their better performance.

In the last years, the advance made in CMOS technology allowed analog and RF circuits to be built with such a technology. Performance improvement, cost advantage and ease of integration have been the driving force to use CMOS technology for analog and RF applications. In Fig. 1.1 the transition frequency (f_T) of nMOSFETs for different technology nodes in a CMOS process is reported.

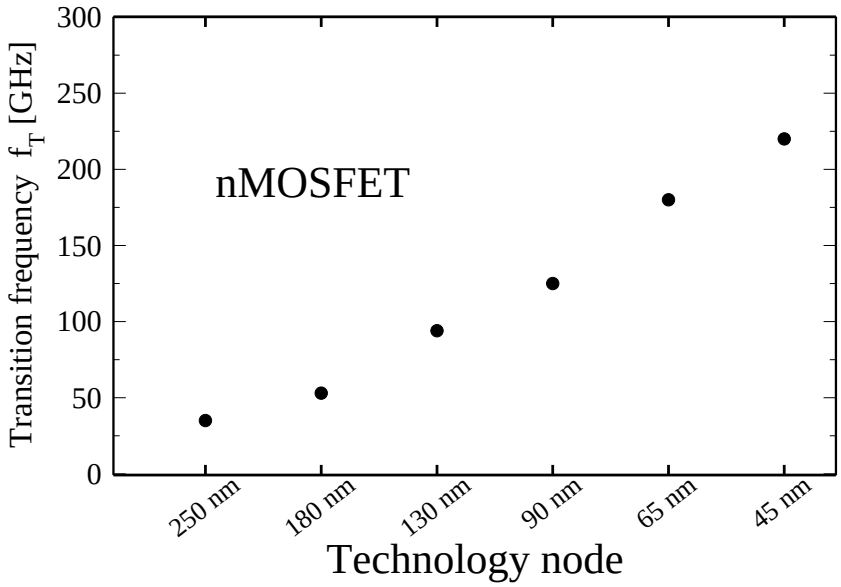


Figure 1.1: Typical f_T for nMOSFETs vs. technology node in CMOS process (source: www.fujitsu.com).

This is one of the figures of merit that qualifies the transistor for application in analog/RF circuits. The f_T is strongly improved by technology scaling.

The integration of digital, RF and analog circuits in the same chip has given birth to the so called system-on-chip (SoC). The new scenario further increases the interest for analog and RF applications of MOSFET technology.

A field in which the integration of digital and analog/RF circuits has been successful is that of wireless communications. Wireless communications started to grow rapidly ten years ago. The driving force has been the development of digital coding and digital signal processing. As for all digital applications, CMOS technology has been the technology of choice due to its high performance, low cost, and integration capability. The next step was to develop the front-end part of a wireless system in the same technology. CMOS devices for RF and analog applications are developed in order to fulfill the needs of wireless communication system.

1.1 Motivation of this work

Advances in MOSFET technology have definitely paved the way to the integration of different circuits in the same chip, but its use in RF application instead of

bipolar technology has also brought more issues in terms of noise.

The noise cannot be completely eliminated and will therefore ultimately limit the accuracy of measurements and set a lower limit on how small signals can be detected and processed in an electronic circuit. One kind of noise which affects MOS transistors much more than bipolar ones is the low-frequency noise. In MOSFETs, low-frequency noise is mainly of two kinds: flicker or $1/f$ noise and random telegraph signal noise (RTS).

Flicker noise is the excess noise at low frequencies whose power spectral density (PSD) approximately depends inversely on the frequency. The $1/f$ noise of MOS transistors is a severe obstacle in analog and RF circuits [2]. The $1/f$ noise is, for example, up-converted to undesired phase noise in voltage controlled oscillator (VCO) circuits, which can limit the information capacity of communication systems [2].

The downscaling of the device dimensions not only entails a downscaling of the voltage levels, but made RTS noise more and more prominent. RTS noise is caused by traps or defects at the silicon-oxide interface or in the oxide and in small-area MOSFETs a single RTS signal can be isolated. RTS noise is also assumed to be the origin of flicker noise in large-area devices [3]. In particular, the superposition of the RTS noise from many traps could lead to a $1/f$ spectrum. In the last years, the direct influence of random telegraph signal noise in circuits has been shown. In [4] the erratic behavior in SRAM due to RTS noise is demonstrated. RTS noise can also be a limiting factor in CMOS image sensors where it affects the pixel read noise floor [5].

In 1991, it was noted for the first time [6] that low-frequency noise could be reduced by cycling a MOSFET between strong inversion and accumulation. That means that, turning ”OFF” the device for a certain time before turning it ”ON” again, reduces the noise measured when it is always ”ON”. This effect is related to the fact that the noise not only depends on the present bias but also on the bias history of the device. Soon afterwards this effect was associated with the emptying of traps that cause RTS noise [7]. The reduction of flicker noise in switched bias CMOS circuits has been studied in [8].

1.2 Scope of this thesis

As we have seen from the above section, low-frequency noise in MOSFETs has a strong influence in modern CMOS circuits. Low-frequency noise can be found

in many applications and it can be influenced under switched bias conditions. This kind of noise appears both as flicker and RTS noise.

The objective of this thesis is to characterize and to model the low-frequency noise by studying RTS and flicker noise under both constant bias and switched bias conditions. Different biasing schemes have been investigated both for RTS and flicker noise in time and in frequency domain.

In *chapter 2* the basic working principles of the MOS capacitor are discussed, and the importance of quantum mechanical effects is analyzed. The fundamental basis of the MOS transistor is also presented. *Chapter 3* describes the basic electrical characterization by means of current-voltage (I-V), capacitance-voltage (C-V), and charge-pumping measurements. Two methods to extract both the interface trap density and the mobility have been adopted in order to analyze MOSFETs having a different process option. In *chapter 4*, after the review of stochastic signals, a Monte Carlo simulator able to simulate both RTS and flicker noise under constant and switched bias conditions is presented. *Chapter 5*, after a brief introduction on different kind of traps present in the silicon oxide, describes the Shockley-Read-Hall (SRH) theory for trapping and detrapping of electrons in traps located at the silicon oxide interface or inside the oxide. Measurements and simulation of the gate bias dependence of RTS emission and capture time constants in n and pMOS transistors are presented. In *chapter 6* measurements of flicker and RTS noise under constant and switched bias conditions are proposed. The effect of a forward substrate bias is deeply analyzed. The final conclusions of this thesis are presented in *chapter 7*.

Chapter 2

MOSFETs: device physics

The metal-oxide-semiconductor field effect transistor (MOSFET) is the fundamental component for digital circuits such as microprocessor and memories. In the last years CMOS technology replaced the bipolar one in analog, RF and power applications in which the bipolar technology has been for many years the preferred choice. The CMOS technology has the great advantage of combining low-cost, high performance, high yield, low standby power, and larger integration of functions. The ability to reduce the dimensions of MOS transistors and the consequent higher integration lead to faster and smaller chips. This chapter is organized as follows: in the first part the basic working principles of the MOS capacitor are discussed and the importance of quantum mechanical effects is analyzed. In the second part of the chapter the fundamental basis of the MOS transistor are presented.

2.1 MOS capacitor

In order to understand the working principle of a MOS transistor it is useful first to analyze its basic part: the MOS capacitor. The MOS capacitor consists of a metal-oxide-semiconductor structure as illustrated by Fig. 2.1. A thin oxide layer usually SiO_2 separates the metal and the semiconductor (silicon) regions. The metal is referred as gate and the semiconductor as bulk or substrate. The bulk can be p- or n-type depending on the adopted doping. In this section we always refer to a p-type substrate.

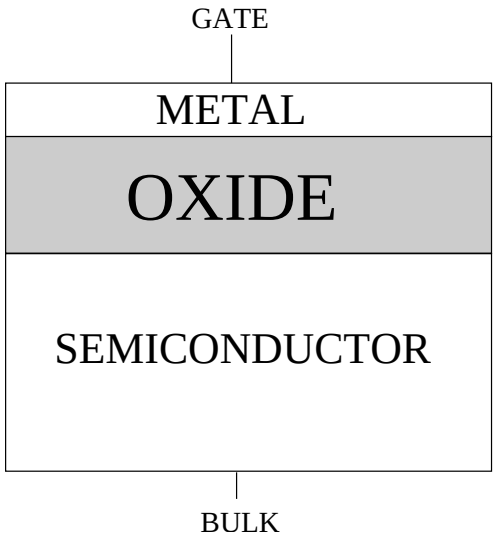


Figure 2.1: Schematic cross section of a MOS capacitor

2.1.1 Energy band diagram

To understand the basic operation of a MOS capacitor it is useful to refer to its energy band diagram. The energy band diagram represents the different energy levels of the three materials metal-oxide-semiconductor. Depending on the applied voltage at the gate terminal the energy levels in the structure can bend giving rise to four different operation modes (Fig. 2.2). For simplicity, we assume that the metal work function is the same as the silicon work function.

Flatband When no voltage is applied to the gate terminal, the Fermi level of the semiconductor and the metal line up and the bands both in the silicon and in the oxide are flat. This condition is called *flatband* condition and is shown in Fig. 2.2(a)

Accumulation When a negative voltage is applied to the gate terminal, it results in a rise of the Fermi level of the metal with reference to the Fermi level of the semiconductor as shown in Fig. 2.2(b). This creates an electric field in the oxide. This field accelerates negative charges towards the silicon substrate. A field is also induced at the silicon surface in the same direction as the oxide field. The bands bend upward toward the oxide interface. The Fermi level of the semiconductor is flat since there is no net flow of conduction current. This results in a hole concentration much higher at the surface than the equilibrium hole

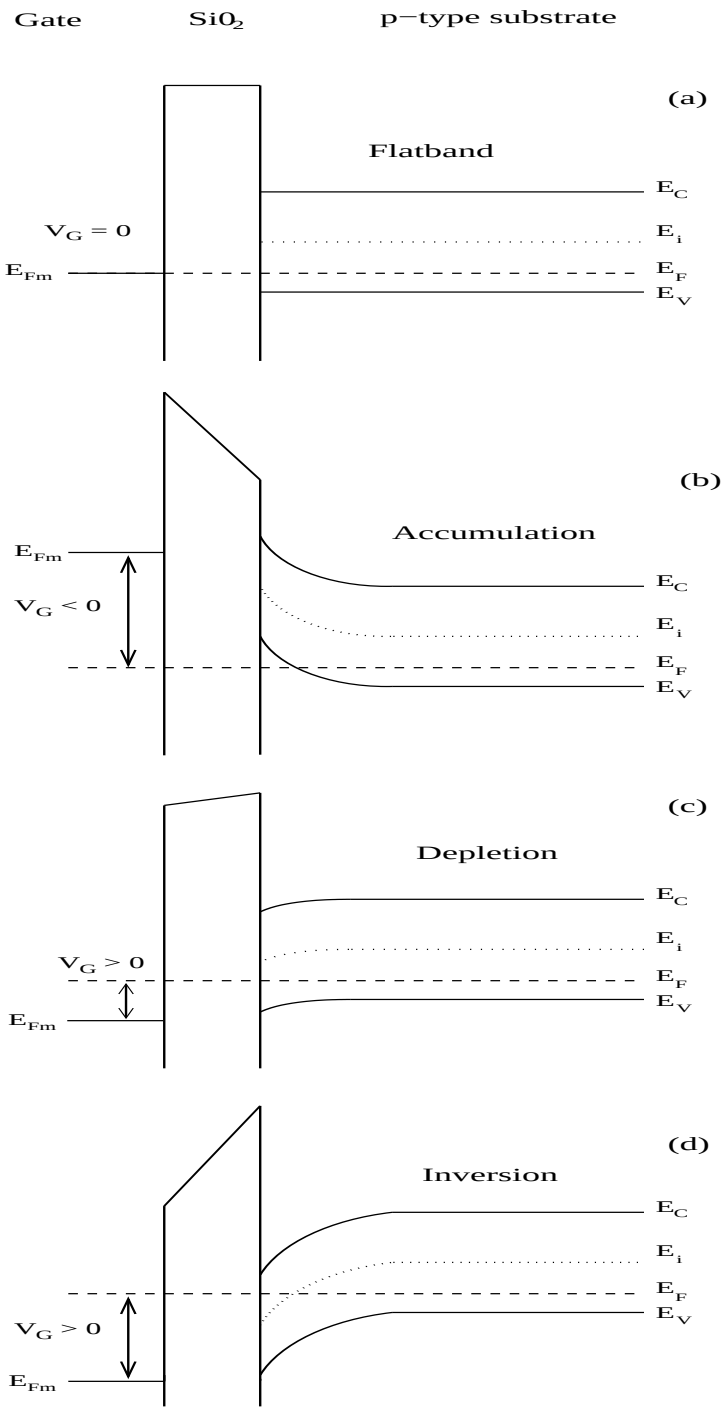


Figure 2.2: Energy band diagram of a MOS capacitor biased (a) Flatband, (b) Accumulation, (c) Depletion, (d) Inversion.

concentration in the bulk. Since excess holes are accumulated at the surface, this is referred to as the *accumulation* condition.

Depletion When a positive voltage is applied to the gate of the capacitor, the Fermi level of the metal move downward and creates an oxide field in the oxide and in the silicon surface which causes the bands to bend downward toward the surface, as shown in Fig. 2.2(c). In this case, the holes are repelled from the interface side of the semiconductor, resulting in the formation of immobile negative ions layer near the interface and a depletion charge Q_B is associated to this layer. This condition is called *depletion*.

Inversion When the applied voltage to the gate is increased, the band bending increases and the depletion region becomes wider. This process will continue and reach the state where the intrinsic level of the semiconductor E_i is equal to the Fermi level E_F making it intrinsic. A further increase in the gate voltage creates no further depletion and, at the interface side of the semiconductor, a layer of electrons is formed. An inversion charge Q_{inv} is associated to this layer. This is referred to as the *inversion* condition.

The inversion condition is the most important because is the one that allows the flowing of a current in a MOS transistor.

2.1.2 Classical model

In this section we introduce the basic notion necessary to characterize the inversion layer of a MOS device using the classical approach.

For the classical semiconductor theory the electrons in the conduction band are free to move in any direction forming a three-dimensional gas. The electron concentration it is assumed maximum at the interface and, under some simplifications, the electron concentration at the interface between the substrate and the oxide is [9]:

$$n = N_C \exp\left(\frac{E_F - E_{CS}}{kT}\right) \tag{2.1}$$

where E_{CS} is the conduction band energy level at the Si-SiO_2 interface, and E_F the Fermi level (Fig. 2.3).

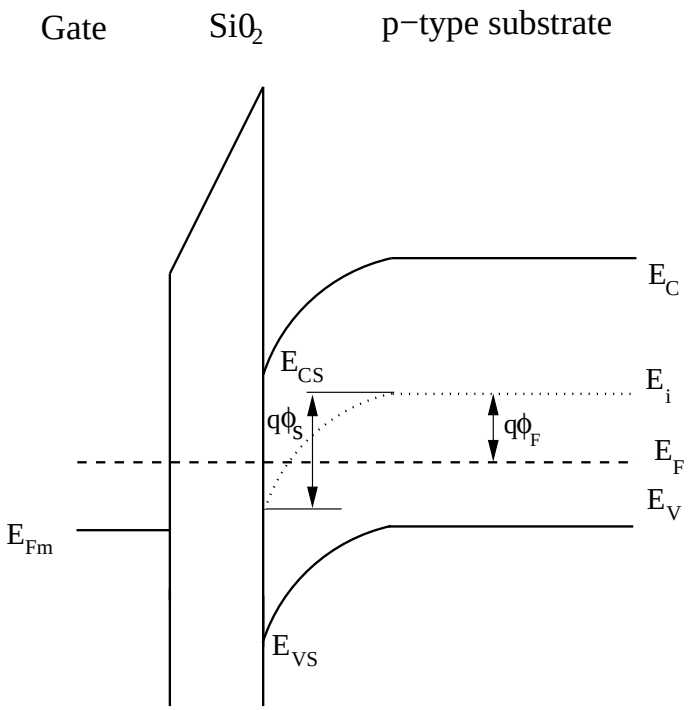


Figure 2.3: Band structure of a p-type MOS capacitor in inversion.

N_C is the effective density of states in the conduction band and can be expressed as:

$$N_C = 2\left(\frac{m^* kT}{2\pi\hbar^2}\right)^{\frac{3}{2}} \tag{2.2}$$

where m^* is the effective electron mass, k is the Boltzmann's constant, T is the temperature and $\hbar$ is the reduced Planck's constant.

A 3D approach is acceptable only for lightly doped semiconductor in which the electric field at the surface is relative small. When the semiconductor is highly doped, like in modern devices, quantization effects are present and a 2D approach is more appropriate. A brief introduction on quantization effects is given in the next section.

2.1.3 Quantum mechanical effects

Electrons in the inversion layer of a MOS are confined in a potential well close to the Si-SiO_2 interface. This potential well is formed by the silicon conduction

band, that is bent under the effect of the electric field, and the silicon-oxide barrier. To ensure a good control of the gate on the channel in small size devices, it is necessary to reduce the gate oxide thickness and to increase the substrate doping concentration. This results in a very high surface electric field. The higher the electric field the higher is the confinement of electrons in the potential well. The width of the potential well in the z direction, the direction perpendicular to the interface, is small compared to the wavelengths of the carriers. The quantum mechanics demonstrated that the energy of confined carriers is discretized. Each discrete level corresponds to a *subband* of the electron gas. To each subband is then associated a discrete value of energy for the motion of the carriers perpendicular to the interface (z direction), and a continuum of energies for the motion in the plane parallel to the interface. The total number of electrons in the conduction band is therefore the sum of the electrons present in each subband.

Inversion layer electrons on a $<100>$ surface are known to be composed of two kinds of subbands (Fig. 2.4). One is the 2-fold valleys along the z direction. These valleys respond to the external electric field with their longitudinal effective mass m_l=$0.916m_0$. The other 4-fold valleys respond with the transverse effective mass m_t=$0.19m_0$. Each set of subbands can be visualized as a ladder. Thus, two different ladders will be obtained for the 2-fold (*unprimed ladder*) and the 4-fold (*primed ladder*) valleys. In Fig. 2.5 the first four sets of subbands are illustrated. The levels E_0, E_1 and E_2 are due to the doubly degenerate energy ellipsoids, while the $E_0^{'}$ level is the ground state for the 4-fold degenerate ellipsoids [10]. It is interesting to notice that the unprimed ladder has a larger effective mass, so the energies of the subband associated to the unprimed ladder are relatively smaller than the energies of the subbands associated to the primed ladder.

Another difference with respect to the classical approach is that only a small amount of the electron density is located at the Si-SiO_2 interface but has a peak at a certain distance $\overline{z}$ called charge centroid and a total distribution defined by the probability function $p(z)$, see Fig. 2.5.

Comparing the quantum mechanics approach with the classical one two main key effects can be underlined.

The first effect is an increase of the threshold voltage. The threshold voltage is approximately the gate voltage for which the conduction band goes below the Fermi level. However, due to the energy quantization, the lowest level that electrons occupy is not the bottom of conduction band, rather it is the first energy level E_0, which is little higher than the conduction band at the interface

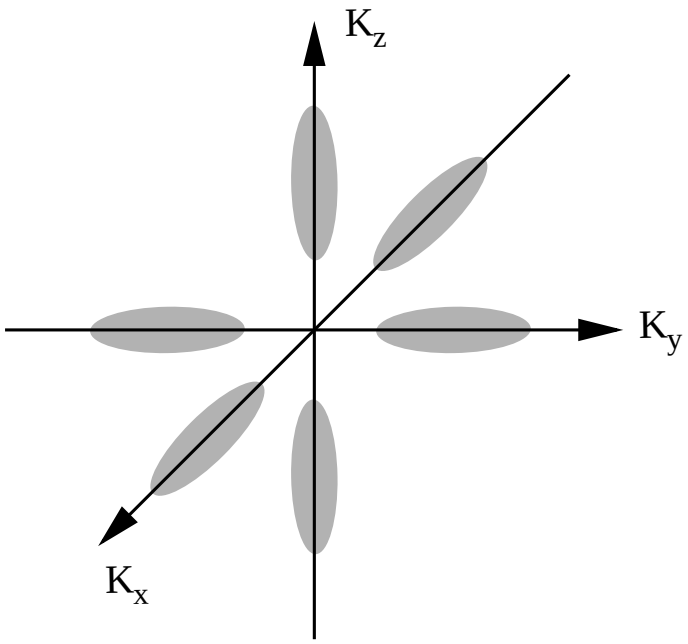


Figure 2.4: Constant energy ellipsoids for silicon along (100) surface.

E_{CS}. Hence, to bend this band below the Fermi level, a little more gate voltage is needed. This is reflected to a higher threshold voltage compared to the one calculated by the classical theory.

The second effect comes from the spatial distribution of inversion charge that follows the probability function $p(z)$. While the classical distribution shows a peak at the oxide semiconductor interface, the quantum mechanical distribution shows a peak inside the substrate with an average distance $\overline{z}$. The average carriers distance produces an increase of the effective oxide thickness. Therefore, the quantum mechanical calculation predicts a larger effective oxide thickness, which means a lower gate capacitance. Thus, for a certain gate voltage, the amount of inversion charge will be somewhat smaller than that predicted by the classical analysis. This is more important as the oxide thickness becomes smaller with each technology generation.

In our work, in order to analyze experimental results, we use a first order approximation of quantization effects taking into account only the lowest subband E_0 in which the most of electrons resides. An exhaustive discussion of this approach is presented in [11]. Here we report only the basic notion needed in our work.

The effective density of states for electron in the 2D case is:

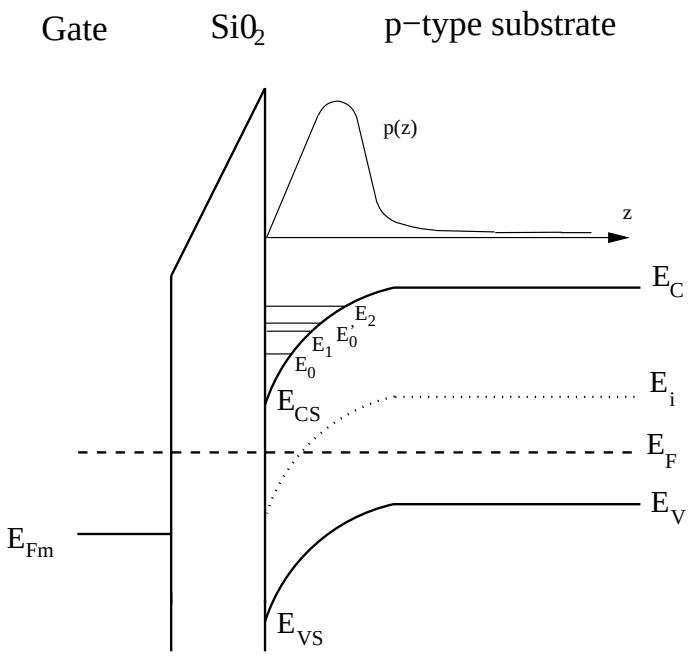


Figure 2.5: Band structure of a p-type MOS capacitor in inversion showing the energy subbands due to quantization effects.

$$N_C(2D) = \frac{2kTm_t}{\hbar^2\pi} \tag{2.3}$$

where m_t is the electron transverse effective mass.

The electron concentration is expressed by:

$$n_{2D} = N_C(2D)\exp\left(\frac{E_F - (E_{CS} + \Delta E_0)}{kT}\right) \tag{2.4}$$

where $\Delta E_0 = E_0 - E_{CS}$ and it is given by:

$$\Delta E_0 \approx \left(\frac{\hbar^2}{2m_l}\right)^{\frac{1}{3}} \left(\frac{9\pi q}{8}F_S\right)^{\frac{2}{3}} \tag{2.5}$$

where m_l is the electron longitudinal effective mass, and F_S is the electric field normal to the interface.

The probability function of finding electrons along the z direction can be expressed as:

$$p(z) = \left(b^3/2\right)z^2\exp(-bz)\big) \tag{2.6}$$

with:

$$b = \left[\frac{12qm_l}{\hbar^2\varepsilon_0\varepsilon_{si}}\left(Q_B + \frac{11}{32}Q_{inv}\right)\right]^{\frac{1}{3}} \tag{2.7}$$

where ε_0 is the permittivity of free space, and ε_{si} is the silicon relative dielectric constant.

The charge centroid of the inversion layer is calculated as:

$$\overline{z} = \frac{3}{b} \tag{2.8}$$

Eq. 2.8 gives an estimation of the average distance of carriers from the interface.

2.2 Fundamental of MOSFETs

The MOS transistor is basically a MOS capacitor to which two more regions called source and drain are added. A cross section of a MOS transistor is shown in Fig. 2.6.

The gate terminal controls the formation of the channel and the flowing of the current between the source and the drain terminals. The substrate terminal is usually connected to ground, even if in some applications a positive o negative voltage could be applied. The well forming the substrate is n- or p-doped for a p- or n-channel MOSFET, respectively. The source and the drain regions present a large concentration of dopants of opposite type of the substrate. In Fig. 2.6 the schematic cross section of a n-type MOS is shown. The gate electrode is usually made of poly-silicon or metal and it is separated from the Si substrate by an insulator with a thickness t_{ox}. The typical material of the insulator is SiO_2 or nitrided SiO_2.

2.2.1 MOSFET I-V characteristic

The operation of a MOSFET can be separated into three different modes, depending on the voltages applied to the terminals. For a n-channel MOSFET the modes are:

- *Cutoff or subthreshold mode*: when $V_{GS} < V_{TH}$, where V_{GS} is the gate-to-source voltage and V_{TH} is the threshold voltage of the device. The transistor is turned OFF, and there is no conduction between drain and

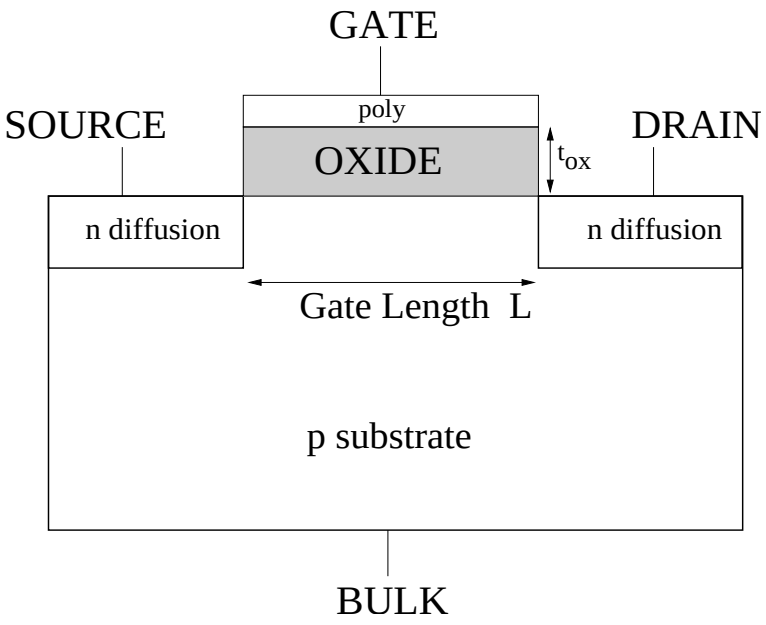


Figure 2.6: Schematic cross section of a standard 4-terminal MOSFET

source. While the current between drain and source should ideally be zero, there is a weak-inversion current or *subthreshold leakage*.

- *Triode or linear region*: when $V_{GS} > V_{TH}$ and $V_{DS} < V_{GS} - V_{TH}$, where V_{DS} is the drain-to-source voltage. The transistor is turned ON, and a channel has been created which allows current to flow between the drain and the source. The MOSFET operates like a resistor controlled by the gate voltage. The current from drain to source can be expressed as:

$$I_{DS} = \frac{W}{L} C_{ox} \mu_{eff} \left((V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right) \tag{2.9}$$

  where L is the channel length, W is the channel width, $C_{ox} = \varepsilon_0 \varepsilon_{ox} / t_{ox}$ is the oxide capacitance, μ_{eff} is the effective mobility, N_A is the substrate doping concentration.

- *Saturation*: when $V_{GS} > V_{TH}$ and $V_{DS} > V_{GS} - V_{TH}$. The transistor is turned on, and a channel has been created which allows current to flow between the drain and source. Since the drain voltage is higher than the gate voltage, a portion of the channel is turned off. The oneset of this region is also know as pinch-off. The drain current is now relatively independent

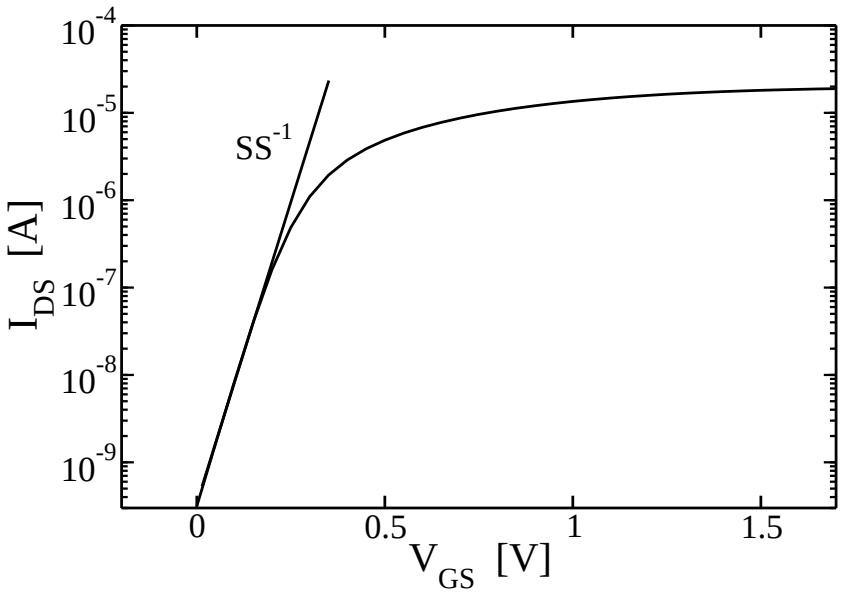


Figure 2.7: I_{DS} vs. V_{GS} characteristic in logarithmic scale.

of the drain voltage (in a first-order approximation) and the current is only controlled by the gate voltage:

$$I_{DS} = \frac{W}{2L} C_{ox} \mu_{eff} (V_{GS} - V_{TH})^2 \tag{2.10}$$

The threshold voltage can be expressed as:

$$V_{TH} = V_{FB} + 2\phi_F + \frac{\sqrt{4\varepsilon_0 \varepsilon_{si} q N_A \phi_F}}{C_{ox}} + \frac{\sqrt{2\varepsilon_0 \varepsilon_{si} q N_A}}{C_{ox}} (\sqrt{V_{SB} + 2\phi_F} - \sqrt{2\phi_F}) \tag{2.11}$$

where V_{FB} is the flatband voltage, V_{SB} is the source-to-substrate voltage, and ϕ_F is the Fermi potential.

The simple expressions for the drain current (Eqs. 2.9 and 2.10) can be obtained from hand-calculation under many approximations. The most important one is the *Gradual Channel Approximation* [12] which assumes that the electric field in the direction normal to the Si-SiO_2 interface is much larger than the one parallel to the transport direction.

The ability to turn OFF a transistor is described by the subthreshold slope (Fig. 2.7):

$$SS = \frac{\partial V_{GS}}{\partial log_{10} I_{DS}} = \frac{kT}{q} ln(10) \left(1 + \frac{C_D}{C_{ox}}\right) \tag{2.12}$$

where C_D is the depletion layer capacitance.

A steep subthreshold slope is desired since the current drops faster with decreasing the gate voltage, therefore, the device is easier to turn OFF. This allows a lower threshold voltage and as a consequence a higher ON-current. In MOSFETs the value of the substhreshold slope is usually between 60-100 mV/dec. SS is sensitive to the presence of traps at the Si-SiO_2 interface. This fact depends on the capacitance associated with the interface states which will be parallel with the depletion layer capacitance C_D (Eq. 2.12) and will therefore increase the subthreshold slope.

The characteristic which has made MOSFETs so interesting is the scalability. Already from Eqs. 2.9 and 2.10, it is possible to evaluate the dependence of the current on the different geometry parameters and applied voltages. For example, a decrease of the gate length L leads to an increase of the drain current I_{DS}. Shrinking the device dimensions is not a straightforward task, and especially in the short-channel regime, many second-order effects become more and more relevant such as quantization effects previously reported.

2.2.2 Carrier mobility

In a semiconductor under thermal equilibrium and no applied electric field the carriers move rapidly with the thermal velocity $\sim 10^7$ cm/s in random directions and no net current flows. The motion of the carriers is perturbated by the semiconductor lattice (phonon) and impurities (dopants and defects). These perturbations are called scattering events. The application of an electric field accelerates the carriers between two collisions and the carrier mobility is defined as the ratio of the carrier velocity and the electric field. The carrier mobility in an inversion layer of a MOSFET is much lower than in the bulk since the carriers are confined in a narrow layer below the Si-SiO_2 interface suffering therefore from scattering at the surface (roughness and surface phonons). If the different scattering mechanisms are assumed to be mutually independent and to have the same energy dependence, the effective mobility μ_{eff} in the inversion layer can be calculated using the Matthiessen's rule according to [10, 13]:

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_{ph}} + \frac{1}{\mu_{sr}} + \frac{1}{\mu_c} \tag{2.13}$$

where μ_{ph} is the mobility limited by surface acoustic phonon scattering, μ_{sr} is the mobility due to surface roughness scattering and μ_c is the mobility limited by

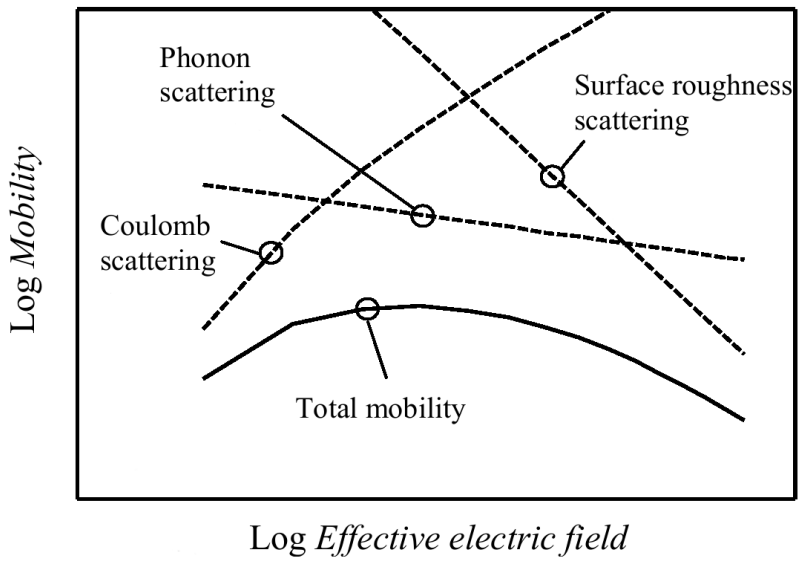


Figure 2.8: Carriers mobility in an inversion layer of a MOSFET as a function of the effective electric field. The dependence on the main scattering sources and on temperature is shown. Picture is taken from [13].

Coulomb scattering mainly due to ionized atoms of dopants and fixed/trapped charge in the gate oxide. The conditions for using the Matthiessen's rule are only seldom fulfilled in practice, however Eq. 2.13 is useful to analyze the dependence of the effective mobility on the scattering events. Both the surface roughness scattering due to the micro roughness at the Si-SiO_2 interface and the Coulomb scattering are sensitive to technology factors such as doping concentration, surface cleaning and the gate oxidation process. On the other hand, the phonon scattering has only a weak dependence on technology for a semiconductor material of good crystalline quality.

The impact of different scattering mechanisms is described in Fig. 2.8. It is interesting to notice the strong impact of surface roughness at large effective field that is required by MOSFETs with large substrate doping concentration in order to operate in strong inversion. Indeed, phonon scattering and Coulomb scattering are both strongly temperature dependent, whereas surface roughness scattering has a weaker dependence on temperature.

Chapter 3

Basic electrical characterization of MOS devices

Device-level electrical characterization is a fundamental tool used to study and to verify the basic characteristics of a device. Electrical characterization is also important in the modeling in order to calibrate the models. In the first part of this chapter we introduce the basic electrical characterization of MOS transistors by means of current-voltage (I-V), capacitance-voltage (C-V), and charge-pumping measurements. In the second part the proposed methods are then performed in order to evaluate the interface state density and the mobility of MOSFETs having a different process option.

3.1 I-V characterization

I-V characterization is usually the first step to evaluate a device measuring the currents at the terminals versus the applied voltages. The instrument that allows this kind of measurements is the parameter analyzer. In our measurement we used the HP 4156C. It provides several Source-Measure Units (SMUs) in order to apply and to measure currents and voltages. SMUs perform Kelvin measurements to avoid the effects of parasitic series resistance. This measurement procedure, also know as the four-wire method, consists of a stimulating line (force) with a second one in parallel (sense) (Fig. 3.1). Ohmic losses on the force line are eliminated by the operational amplifier (op-amp) in voltage follower mode. This means that the op-amp output will exhibit a somewhat higher voltage than the desired test voltage at the device under test (DUT) to compensate the ohmic

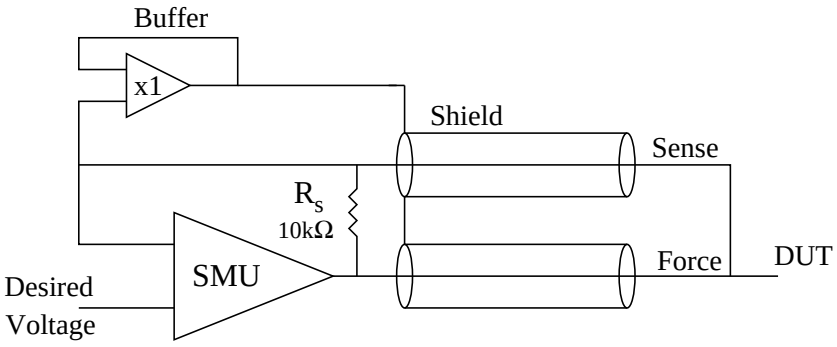


Figure 3.1: Schematic of a Kelvin measurement.

losses along the force line due to the flowing of the test current. The sense line, connected to the inverting input of the op-amp, guarantees that the DUT is exactly biased with the desired test voltage.

While this method eliminates DC errors, it does not avoid dynamic measurement problems such as electromagnetic influences. To solve these problems, an extra inner shielding (guard) is applied between the internal signal wire and the external cable shielding (triax cables). The guard is connected to a separate second op-amp which follows exactly the value of the desired test voltage. This auxiliary op-amp supplies the charging current for the test cables while the main op-amp can measure the current from the DUT independently of this charging problem.

Many properties and parameters of a device can be extrapolated from the I-V characterization such as the effective channel length L_{eff}, the parasitic source and drain series resistance R_{SD} [14, 15], the effective mobility μ_{eff}, the field effect mobility μ_{fe}, and the threshold voltage V_{TH}. For the purpose of our work we are interested in measuring the threshold voltage and the field effect mobility.

3.1.1 Threshold voltage extraction

Many different methods have been proposed in order to extract the threshold voltage of MOS transistors [16]. A powerful and easy method used in this work has been proposed by Ghibaudo [17]. This method uses the intercept of the $I_{DS}/g_m^{1/2}$ function with the x-axis (Fig. 3.2), where g_m is the transconductance and is defined as:

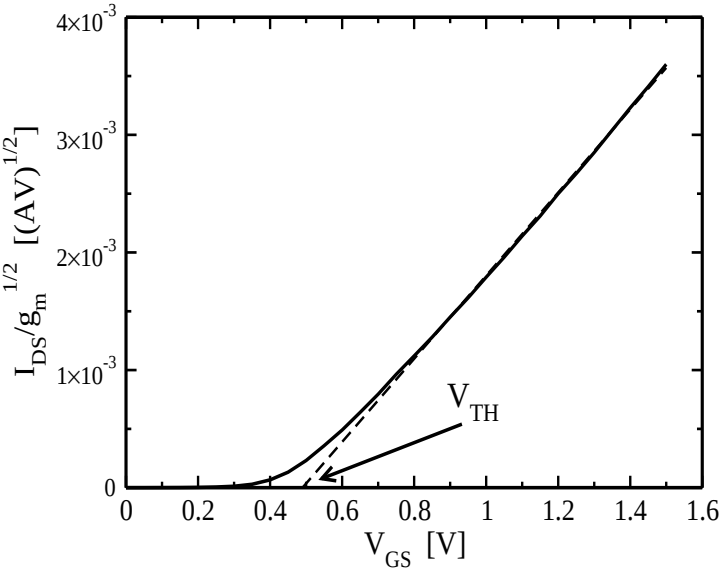


Figure 3.2: Typical $I_{DS}/g_m^{1/2}$ characteristic for an nMOS used to extract the threshold voltage.

$$g_m = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS}} \tag{3.1}$$

The transconductance g_m is a very important parameter for analog circuit designers and can be extracted from $I_{DS}-V_{GS}$ curves. Indeed, see section 3.1.2, the low field transconductance, measured therefore at low V_{DS}, is also useful in order to estimate the carrier mobility.

3.1.2 Mobility extraction

The mobility can be extracted in different ways. In particular, depending on the method two different mobilities for electrons in the inversion layer can be extracted: the effective and the field effect mobility.

The effective mobility can be obtained from I-V measurements in the linear regime at small V_{DS} rearranging Eq. 2.9:

$$\mu_{eff} = g_d \frac{L}{WC_{ox}(V_{GS} - V_{TH})} \tag{3.2}$$

where g_d is the drain conductance and is defined as:

$$g_d = \left.\frac{\partial I_{DS}}{\partial V_{DS}}\right|_{V_{GS}} \tag{3.3}$$

This method is not accurate for bias conditions close to threshold voltage. This is mainly due for two reasons: first because the threshold voltage is not well defined, second because Eq. 3.2, based on the approximation $Q_{inv} = C_{ox}(V_{GS} - V_{TH})$, is not correct close to the threshold and well above threshold where polysilicon depletion and the inversion layer capacitance reduce the gate capacitance. However, this method is quite easy to apply.

A more accurate method is the split-CV technique [18, 19] that uses both a capacitance and a current measurement in order to extract the effective mobility. In the split-CV method the inversion charge is calculated by a C-V measurement:

$$Q_{inv}(V_{GS}) = \int_{V_{GS_{acc}}}^{V_{GS}} C_{GC}(V)dV \tag{3.4}$$

where $V_{GS_{acc}}$ is a voltage chosen in strong accumulation, and C_{GC} is the gate-to-channel capacitance. The effective mobility is then extracted by:

$$\mu_{eff} = \frac{L}{W}\frac{I_{DS}}{Q_{inv}V_{DS}} \tag{3.5}$$

Even if the split-CV method is the most accurate, it is also the most difficult to perform and some advanced test structures should be used [20].

Another possibility is to extract the field effect mobility μ_{fe} [18, 21]. In this case Eq. 2.9 is rearranged taking its partial derivative with respect to the V_{GS}:

$$\mu_{fe} = g_m \frac{L}{WC_{ox}V_{DS}} \tag{3.6}$$

where the transconductance g_m is defined by Eq. 3.1.

Both the effective mobility μ_{eff} from Eq. 3.2 and the field effect mobility from Eq. 3.6 are deduced by I-V characterization and simple analytical models. Specifically, the effective mobility is extracted from the drain conductance g_d while the field effect mobility from the transconductance g_m. The field effective mobility is generally lower than the effective mobility due to a different V_{GS} dependence. This fact can be easily explained explicating the V_{GS} dependence of the effective mobility in Eq. 2.9 [17]:

$$\mu_{eff} = \frac{\mu_0}{1 + \theta(1 + V_{GS} - V_{TH})} \tag{3.7}$$

where μ_0 is the low field mobility and θ is the mobility attenuation factor.

In Eq. 3.6 the field effect mobility is:

$$\mu_{fe} = \frac{\mu_0}{[1 + \theta(1 + V_{GS} - V_{TH})]^2} \tag{3.8}$$

The quadratic dependence of the field effect mobility on the V_{GS} explains the lower values of μ_{fe} compared to μ_{eff}.

In our work, in order to evaluate the mobility, we use Eq. 3.6 therefore we evaluate the field effect mobility.

3.2 C-V characterization

C-V testing is widely used to determine semiconductor parameters, particularly in MOS capacitor and MOSFET structures. C-V measurements can reveal oxide thickness, oxide charges, contamination from mobile ions, and interface trap density [22, 23]. These measurements can be used also during the wafer processes after each process step such as lithography, etching, cleaning dielectric, polysilicon deposition, and metalization. In this frame C-V measurements are quite useful to analyze the quality of each process step. Also reliability issues can be investigated by the C-V characterization.

The C-V measurement consists in applying a small AC signal on top of the DC bias across the structure and sensing the AC current at the same frequency. Commonly, AC signals with frequencies from about 1 kHz to 10 MHz and peak-to-peak voltages between 10 and 50 mV are used. This is typically performed using an LCR meter which measures the phase and modulus of the impedance. In our work we used an HP 4284A.

The aim of C-V measurement in our work has been the extraction of the gate oxide capacitance by measuring both the gate-to-channel capacitance and the gate-to-substrate capacitance versus the bias applied to the gate terminal. The measurement configurations are reported in Fig. 3.3 and examples of measurement results in Fig. 3.4. In the gate-to-channel configuration (Fig. 3.3(a)) the gate, drain and source are connected to the LCR meter while the bulk is tied to ground. This configuration measures the change in inversion charge with the applied voltage:

$$C_{GC} = \frac{dQ_{inv}}{dV_{GS}} \tag{3.9}$$

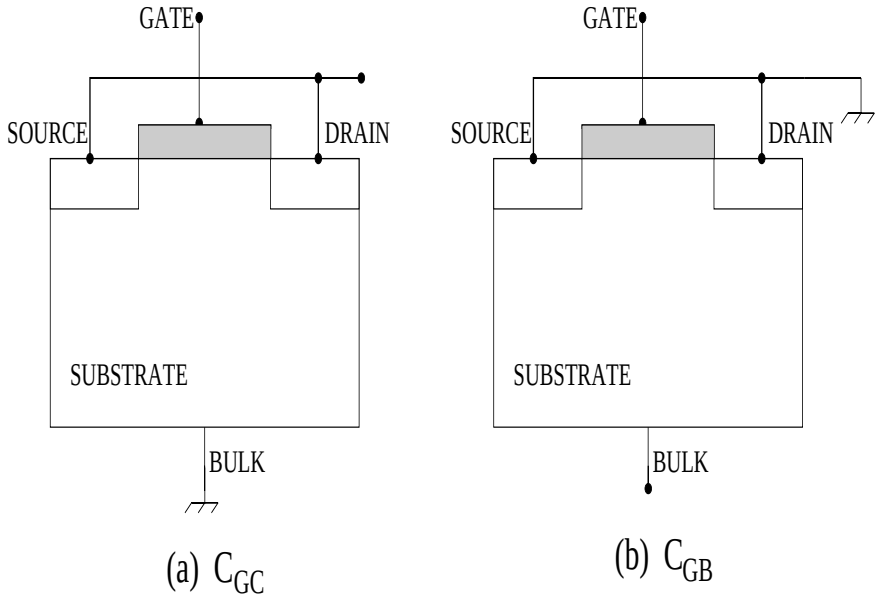


Figure 3.3: Measurement configurations for the gate-to-channel capacitance (a) C_{GC} and the gate-to-substrate capacitance (b) C_{GB}.

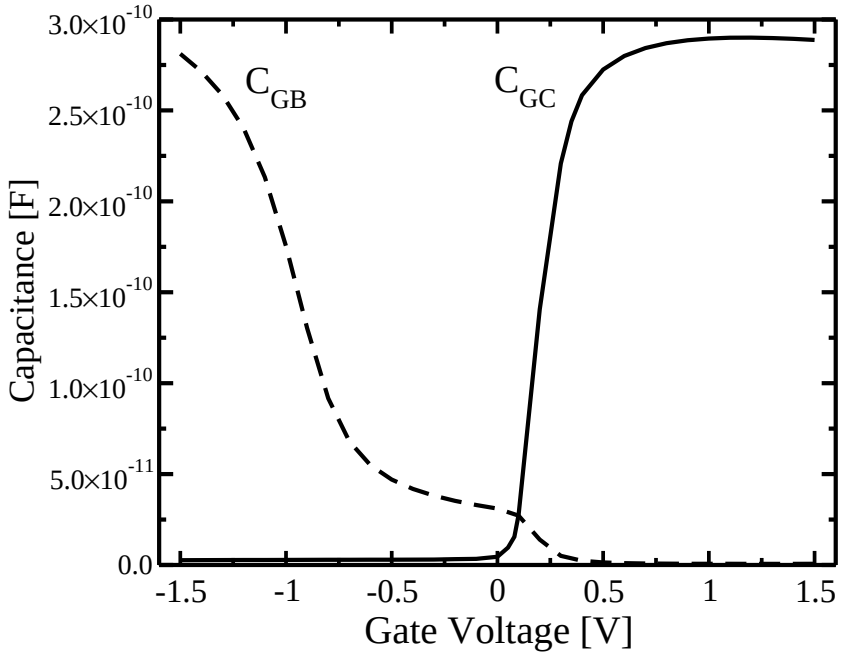
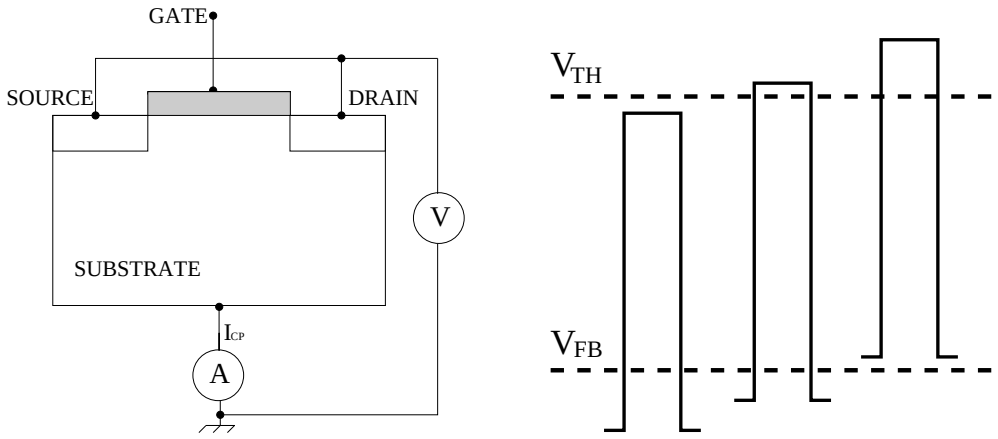


Figure 3.4: C_{GC}, C_{GB} characteristics for an nMOSFET.



(a) Setup (b) Waveform of gate voltage

Figure 3.5: Charge-pumping measurements

In strong inversion C_{GC}=WLC_{ox_eff}, whereas C_{GC} approaches zero below threshold as Q_{inv} decreases exponentially. Poly-depletion and inversion layer quantization effects concur to reduce the effective oxide capacitance:

$$\frac{1}{C_{ox\_eff}} = \frac{1}{C_{ox}} + \frac{\bar{z}}{\varepsilon_0 \varepsilon_{si}} + \frac{W_{poly}}{\varepsilon_0 \varepsilon_{si}} \tag{3.10}$$

therefore $C_{ox\_eff} < C_{ox} = \varepsilon_0 \varepsilon_{ox}/t_{ox}$.

The second term of Eq. 3.10 is due to the quantization effects that move the inversion layer away from the interface on an average distance $\bar{z}$ (see Chapter 2), while the last term is the capacitance of a depletion layer with a width W_{poly} in the polysilicon gate. Scaling more and more the oxide thickness is becoming an important problem due to the limitations caused by the quantization and the poly-depletion effects.

The gate-to-substrate capacitance C_{GB} is measured with the source and the drain terminals grounded (Fig. 3.3(b)) and approaches C_{ox} in accumulation and the series combination of C_{ox} and $C_D = \varepsilon_0 \varepsilon_{si}/W_D$ in depletion.

3.3 Charge-pumping measurement

The Si-SiO_2 interface contains electronic states with energies within the forbidden bandgap. These interface states act as carrier traps and degrade the subthreshold slope and the mobility through Coulomb scattering.

Charge-pumping measurements are widely used to characterize interface state densities in MOSFET devices [24].

The basic charge-pumping technique involves measuring the substrate current while applying voltage pulses of fixed rise time, fall time, and frequency to the gate of the transistor, with the source and drain tied to ground (Fig. 3.5(a),(b)). When the transistor is pulsed into inversion, the surface becomes deeply depleted and electrons will flow from the source and drain regions into the channel where some of them will be captured by the surface states. When the gate pulse is driving the surface back into accumulation, the mobile charge drifts back to the source and drain, but the charges trapped in the surface states will recombine with the majority carriers from the substrate and give rise to a net flow of negative charge into the substrate. This is the so-called charge-pumping effect (Fig. 3.6).

The gate pulse can be applied with a fixed amplitude, sweeping the base level or with a fixed base level, sweeping the amplitude. In a voltage base sweep, the amplitude and the period of the pulse are fixed while sweeping the pulse base voltage (Fig. 3.5(b)). At each base voltage, the substrate current can be measured and plotted against the base voltage. In an amplitude sweep, the base level is fixed while sweeping the amplitude of the pulse. In both these approaches, the basic idea is to reach the condition in which the maximum charge-pumping current can be measured. This condition is reached when the transistor is pulsed between accumulation and inversion, therefore from values below the flatband voltage to values above threshold voltage.

The interface trap density (D_{it}) can be extracted with the following equation:

$$D_{it} = \frac{I_{CP}}{qAf} \tag{3.11}$$

where I_{CP} $[A]$ is the measured charge-pumping current, A [cm^2] is the area of the device, and f $[Hz]$ is the frequency of the applied voltage pulses.

Eq. 3.11 give us the interface trap density in [cm^{-2}]. A more appropriate way is to calculate the effective energy levels reached by the gate pulse and to express the interface state density in [cm^{-2}eV^{-1}] [25].

For the purpose of our work we use Eq. 3.11.

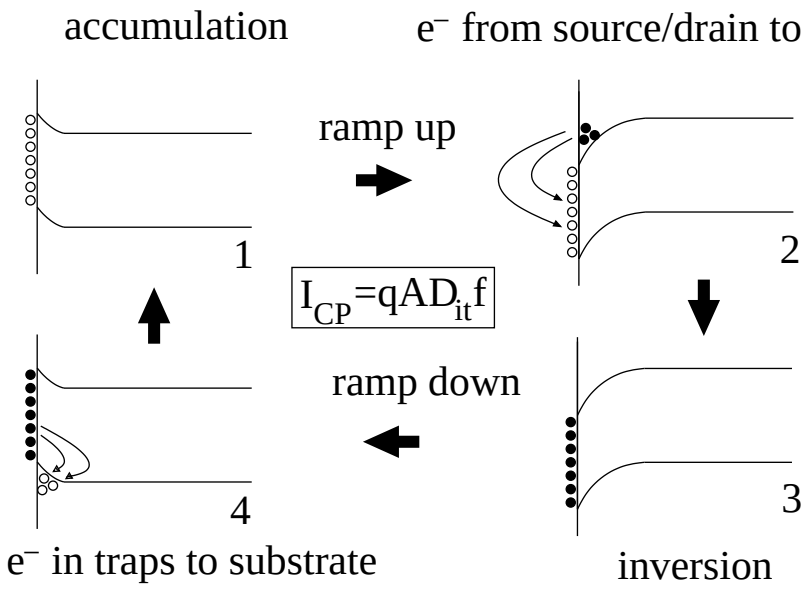


Figure 3.6: Energy band diagram of a nMOSFET commutating between inversion and accumulation and the relative CP current.

3.4 Results of charge-pumping and mobility measurements

In this section we present the results of both charge-pumping and mobility measurements to compare devices with a process split that introduces an additional fluorine doping step to the standard process. Measured MOSFET devices were manufactured in a 0.13 μm technology [26] with a nitrided gate oxide with two thickness: t_{ox}=2.2 nm (SG$_{ox}$) and t_{ox}=5.4 nm (DG$_{ox}$). The effect of the fluorine doping step is reported only for n-type MOSFETs. When we compare devices with and without the fluorine doping step we will use the symbol WF and WOF, respectively. C-V measurements on large area MOSFETs have shown that WF devices have a lower gate oxide capacitance, therefore the fluorine doping step could influence the oxide dielectric constant and/or the oxide thickness. This fact implies also that the threshold voltage of the WF devices is higher than the one of WOF devices.

Charge-pumping results

Charge-pumping measurements are done with the base voltage sweep method.

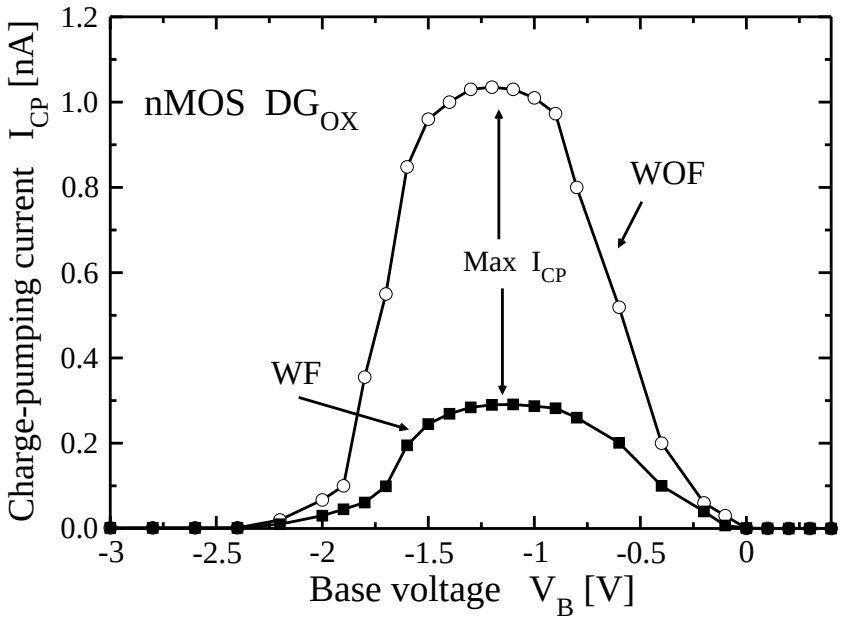


Figure 3.7: Charge-pumping currents for nMOSFETs with DG$_{ox}$ WF and WOF.

The switching frequency of the gate pulse is set to f_{sw}=1 MHz with rising and falling times t_r=t_f=10 ns. Charge-pumping current measured when the gate voltage is pulsed from values below V_{FB} and above V_{TH} is used in Eq. 3.11 to extract the interface state density. The gate voltage amplitude is set to 1.6 V and 1.7 V for SG$_{ox}$ and DG$_{ox}$, respectively. For each analyzed device type, D_{it} is the average of interface state densities measured in six different transistors in different dies inside the wafer. The following devices have been analyzed:

- nMOS SG$_{ox}$ WOF, Area=18.72 um^2
- nMOS SG$_{ox}$ WF, Area=18.72 um^2
- nMOS DG$_{ox}$ WOF, Area=62.4 um^2
- nMOS DG$_{ox}$ WF, $Area = 62.4$ um^2
- pMOS SG$_{ox}$ WOF, $Area = 54.72$ um^2
- pMOS DG$_{ox}$ WF, $Area = 182.4$ um^2

Typical charge-pumping currents are shown in Fig. 3.7 where I_{CP} as a function of the voltage base for nMOSFETs with DG$_{ox}$ with (WF) and without (WOF) the fluorine doping step is reported.

	SG_{ox} WOF	SG_{ox} WF	DG_{ox} WOF	DG_{ox} WF
D_{it} [cm^{-2}]	1.02x10^{10}	4.23x10^{9}	1.07x10^{10}	2.97x10^{9}

Table 3.1: Interface state density D_{it} for nMOS devices with different oxide thicknesses and process steps.

	SG_{ox}	DG_{ox}
D_{it} [cm^{-2}]	4.93x10^{10}	1.63x10^{10}

Table 3.2: Interface state density D_{it} for pMOS devices with different oxide thicknesses.

Results of charge-pumping measurements for nMOS transistors are shown in Table 3.1.

Comparing the interface state density of devices WF and WOF it is interesting to notice that for both the oxide thicknesses SG_{ox}, and DG_{ox} the fluorinated devices (WF) show a lower value, so lower interface states density. This can be explained supposing that the fluorine doping step contributes to decrease the defect density of Si-SiO_2 interface.

Table 3.2 reports the interface state density for pMOS devices with two different oxide thicknesses showing that the DG_{ox} devices have a better Si-SiO_2 interface.

Mobility results

To analyze the effect of the fluorine doping step on the carriers mobility we performed mobility measurement with the g_m method described in section 3.1.2, thus measuring the field effect mobility. The g_m has been measured in nMOSFETs with SG_{ox} and DG_{ox} WF and WOF having long channel (L=10 μm) and large width (W=10 μm). The drain-to-source voltage V_{DS} is set to 50 mV to ensure the linear regime.

In order to compare transistors with and without the fluorine doping step having different threshold voltages and gate oxide capacitance, we report the transconductance g_m over C_{ox} versus the gate voltage overdrive $V_{GS} - V_{TH}$.

In Figs. 3.8 and 3.9 the transconductance g_m has been reported for transistors with different oxide thicknesses with and without the fluorine doping step. For both the oxide thicknesses the mobility is higher in the case of devices with the fluorine doping step. From the considerations made in section 2.2.2 and the

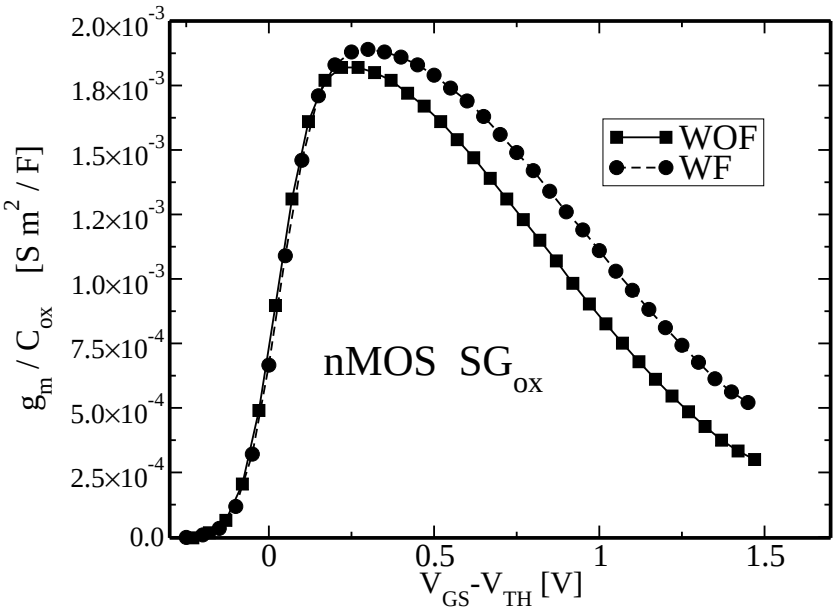


Figure 3.8: Mobility measurements: nMOS with SG_{ox} with and without the fluorine doping step.

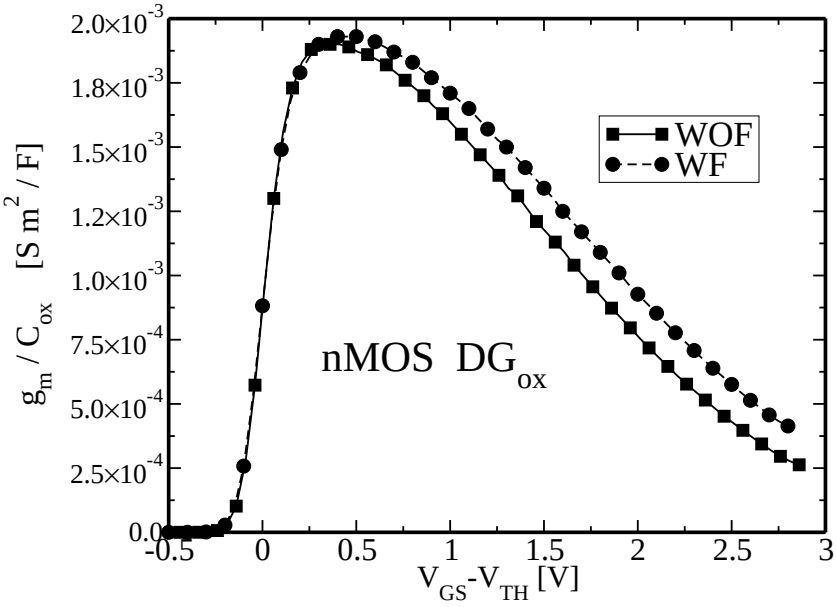


Figure 3.9: Mobility measurements: nMOS with DG_{ox} with and without fluorine doping step.

results of charge-pumping measurements, the higher mobility in fluorinated devices could be related to less Coulomb scattering events due to a lower density of interface states. Coulomb scattering increases when a larger number of trapped charge is present at the interface or inside the oxide. The fluorine doping step, lowering the number of interface states, reduces also the Coulomb scattering and increases carriers mobility. Indeed, the fluorine doping step may also have an influence on the surface scattering reducing the micro roughness at the Si-SiO_2 interface.

Chapter 4

Low-frequency noise in MOSFETs

Noise in electronic circuits is generally associated to the random fluctuations affecting currents and voltages. Noise cannot be completely eliminated and it sets the lower limit of the signal being processed by a circuit without significant deterioration in the signal quality. In electronics and telecommunications an important quantity is the signal to noise ratio (SNR). SNR represents a measure of the signal strength relative to the background noise. In a circuit the goal is to maximize the SNR paying attention on the power consumption. In modern circuits, due to the decreasing dimensions of the devices, the signals levels are becoming very low therefore decreasing the SNR. The study of noise becomes more and more important as it aims, at the same time, to understand its basic principle and to find methods to reduce it. The chapter begins with the review of stochastic signals and their statistical analysis. This background information is necessary to analyze the noise in the following chapters. The second part of the chapter discusses the fundamental noise mechanisms in semiconductors: thermal noise, shot noise, generation and recombination noise, random telegraph signal noise (RTS), and flicker noise ($1/f$). In the third part of the chapter $1/f$ noise in MOSFETs is presented; the existing models are reviewed and the effect on flicker noise of switching the transistor between an ON- and an OFF-state is discussed. Finally, a detailed analysis of RTS noise is reported and a Monte Carlo simulator of RTS and $1/f$ noise under both constant and switched bias conditions is presented.

4.1 Background

The value of a stochastic signal at a particular time cannot be predicted due to its random origin. A stochastic signal can be described by its statistical properties. In this section a brief introduction to stochastic signals and to the techniques for their time and frequency domain analysis is reported.

Stochastic signals

A stochastic signal is the counterpart to a deterministic signal. Each value of a deterministic signal is fixed and can be determined by a mathematical expression, rule, or table. Because of this, future values of any deterministic signal can be calculated from past values. For this reason, these signals are relatively easy to analyze as they are predictable, and we can make accurate assumptions about their past and future behavior.

Unlike deterministic signals, stochastic signals, or random signals, cannot be characterized by a simple, well-defined mathematical equation and their future values cannot be predicted. Rather, we must use probability and statistics to analyze their behavior.

A collection of stochastic signals rather than just one instance of that signal is called a stochastic process (Fig. 4.1). At each time the value assumed by the process is unknown. The value of the process at a certain time t_1 is completely random, therefore, i(t_1) is a random variable.

Describing stochastic signals

The *expected value* of a stochastic signal $x(t)$ is its time average and it is also called *mean value* $m_x(t)$. It is given by:

$$E[x(t)] \equiv m_x(t) = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{+T/2} x(t)dt \tag{4.1}$$

The expected value of $x(t)$ represents also the *first moment* of the stochastic signal. The n^{th} moment of a stochastic signal is the expected value of $x(t)^n$ and it is given by:

$$E[x(t)^n] = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{+T/2} x(t)^n dt \tag{4.2}$$

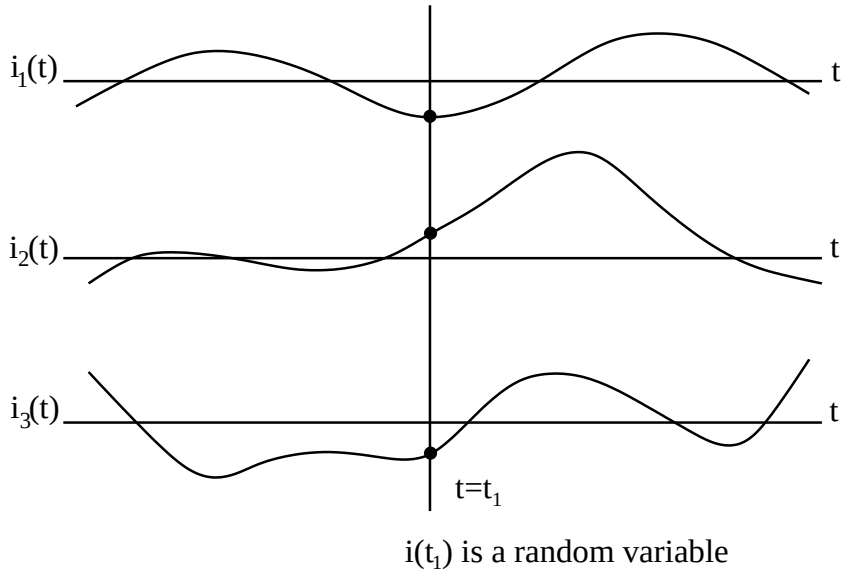


Figure 4.1: Representation of a stochastic process (e.g.. noise) as a function of time.

The 2^{nd} moment of $[x(t)-m_x(t)]$ is the variance (σ^2) of the stochastic signal:

$$\sigma^2 \equiv E[(x(t)-m_x(t))^2] = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{+T/2} (x(t)-m_x(t))(x(t)-m_x(t))dt \quad (4.3)$$

The autocorrelation function of a stochastic signal $x(t)$ is:

$$\begin{aligned} R_{xx}(t,t+\tau) &= E[x(t)x(t+\tau)] \\ &= \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{+T/2} x(t)x(t+\tau)dt \end{aligned} \quad (4.4)$$

while the autocovariance is defined as:

$$\begin{aligned} C_{xx}(t,t+\tau) &= E[(x(t)-m_x(t))(x(t+\tau)-m_x(t+\tau))] \\ &= \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{+T/2} (x(t)-m_x(t))x((t+\tau)-m_x(t+\tau))dt \end{aligned} \quad (4.5)$$

The only difference between the autocorrelation and the autocovariance is that in the autocovariance the mean is subtracted from the input data. If the

mean of a stochastic signal is zero the two functions are identical. Therefore, the autocorrelation is more complete and, in general, the autocovariance function should be only used in the specific case where the intent is to disregard the mean of a non-zero mean stochastic signal.

When one considers electric circuits, it is possible to relate the moments of a stochastic signal $x(t)$ to characteristic quantities:

- The 1^{st} moment of $x(t)$, $m_x(t)$, is the *DC component*.
- The 2^{nd} moment of $x(t)$ is the *total power*.
- The 2^{nd} moment of $[x(t) - m_x(t)]$, σ^2, is the *AC power*.

Stationary, ergodic and cyclostationary stochastic signals

A stochastic signal is *stationary* if the moments of the signal are not a function of time. In particular, if this is true for the moments of any order the signal is *strictly stationary*. In case this is satisfied for all moments up to and including the second one, the signal is *wide-sense stationary*. If the signal is wide-sense stationary, the autocorrelation function defined in Eq. 4.4 will be a function of the time difference τ only and no longer of the absolute time t:

$$R_{xx}(t, t+\tau) = R_{xx}(\tau) \tag{4.6}$$

A stochastic signal is *ergodic* if the ensemble average (average of instantaneous values over a number of realizations) is equal to the time average of one realization of the signal. A signal is ergodic in the strict sense if all its moment are ergodic; it is wide-sense ergodic if the first and second moments are ergodic. Stationarity is a necessary condition for a signal to be ergodic, on the other hand, stationary signals are not necessarily ergodic.

A signal whose moments of any order are periodic in T is said to be *strictly cyclostationary* in T. A cyclostationary signal is defined wide-sense cyclostationary if its mean and its autocorrelation function are periodic in T [27, 28]:

$$\begin{aligned} m_x(t) &= m_x(t+T) \\ R_{xx}(t, t+\tau) &= R_{xx}(t+T, t+T+\tau) \end{aligned} \tag{4.7}$$

Power and energy of a stochastic signal

The power of a stationary stochastic signal $x(t)$ is expressed as:

$$P = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{+T/2} x^2(t)dt \tag{4.8}$$

while the total energy is:

$$\lim_{T\to\infty} TP = \int_{-\infty}^{+\infty} x^2(t)dt \tag{4.9}$$

PSD and the Wiener-Khinchin theorem

In the frequency domain analysis the basic mathematical tool is the Fourier transform. The Fourier transform allows the analysis of signals both in the frequency and in the time domain. The Fourier transform (FT) and its inverse (IFT) of a stochastic signal $x(t)$ are defined by:

$$X(f) = \int_{-\infty}^{+\infty} x(t)e^{-2j\pi ft}dt \tag{4.10}$$

$$x(t) = \int_{-\infty}^{+\infty} X(f)e^{2j\pi ft}df \tag{4.11}$$

The power spectral density (PSD) of a signal is a plot of the power per unit of bandwith as a function of the frequency. The Wiener-Khinchin theorem relates the autocorrelation function to the PSD of the stochastic signal [29]:

$$S(f) = FT(R_{xx}(t, t+\tau)) \tag{4.12}$$

The power (P) of the signal can be expressed in the time domain and in the frequency domain as:

$$\int_{-\infty}^{+\infty} S(f)df = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{+T/2} x^2(t)dt \tag{4.13}$$

Another way to calculate the PSD, without first calculating the autocorrelation function, is:

$$S(f) = \lim_{T\to\infty} \frac{|X(f)|^2}{T} \tag{4.14}$$

The PSD contains less information than the signal in the time domain. While computing the PSD with Eq. 4.12, we should consider that different time domain signals may have the same autocorrelation function, hence, the same PSD. By computing the PSD with Eq. 4.14, we discards phase information by taking the magnitude of $X(f)$. However, the PSD of a stochastic signal is very useful, keeping in mind that for some particular needs, a time domain description is mandatory.

4.2 Noise sources

The current flowing in a device under DC conditions can be written as $I(t) = I_{DC} + i_n(t)$, where I_{DC} is the wanted current due to the chosen bias point, while $i_n(t)$ is a random fluctuating current related to the noise. This latter current can be caused by external noise sources and by fundamental physical processes. External sources are for example cross-talk between adjacent circuits, electrostatic and electromagnetic coupling from AC power lines, vibration etc. These disturbances can often be eliminated by shielding, filtering, and change of layout. Fundamental physical sources cannot be eliminated, but it is however possible to reduce them by proper design of the devices and circuits. In this work we are interested only in these latter sources. A brief introduction on fundamental noise sources is reported below.

4.2.1 Thermal noise

Thermal noise, also called Nyquist or Johnson noise, is the noise associated with the thermal random motion of charge carriers. The direct current has no influence on the thermal noise since the electron drift velocity is much less than the electron thermal velocity. Considering a piece of material with a resistance R at a temperature T, thermal noise can be represented by a current generator ($\bar{i}^2$) parallel to R or a voltage generator ($\bar{v}^2$) in series to R:

$$\bar{i}^2 = 4kT\frac{1}{R}\Delta f; \quad \bar{v}^2 = 4kTR\Delta f \tag{4.15}$$

where k is the Boltzmann's constant and Δf is the bandwidth in Hertz. Eq. 4.15 shows that thermal noise is proportional to the absolute temperature and it ap-

proaches zero if the temperature approaches zero. The PSD of thermal noise is also independent of frequency. All noise sources which are independent of frequency are called *white noise* sources. This is because all different frequencies are present with the same strength.

4.2.2 Shot noise

Shot noise is associated to the direct current flowing across a potential barrier like a pn-junction. Shot noise is caused by the random fluctuation of the electric current due to the discrete nature of the electronic charge (electrons). The noise increases proportionally to the flowing current crossing the potential barrier. The mean square value of the current associated to the shot noise is:

$$\bar{i}^2 = 2qI\Delta f \tag{4.16}$$

where q is the electronic charge. Shot noise is independent of frequency and it should be distinguished from the current fluctuations at equilibrium, which are present without any applied voltage or without any average current flowing through the device.

4.2.3 Generation-recombination noise

Generation-recombination (g-r) noise in semiconductors stems from traps that randomly capture and emit carriers acting as generation-recombination centers. These events cause fluctuation in the number of carriers available for current transport. The trapped charge can also induce fluctuations in the mobility, electric field, barrier height etc. Traps involved in g-r noise are located in the forbidden bandgap and they exist due to the presence of various defects or impurities in the semiconductor or at its surfaces. The power spectral density of g-r noise is a Lorentzian [30]. A single trapping/detrapping process leads to random telegraph signal (RTS) noise.

4.2.4 Flicker or $1/f$ noise

Flicker noise is present in active as well passive devices and may be due to several mechanisms as it will be discussed in the next section. Flicker noise is associated with the flow of a direct current and the mean square value of the current affected by this kind of noise is:

$$\bar{i}^2 = K\frac{I^\beta}{f^\gamma}\Delta f \tag{4.17}$$

where K is a constant associated with the device, I is the direct current, β is the current exponent with a value between 0.5 and 2, and γ is a parameter with a value close to 1. Considering $\gamma = 1$ in Eq. 4.17, the noise spectral density is proportional to $1/f$ and for this reason flicker noise is also called '$1/f$' noise. In the case the parameter γ has values outside the range 0.9-1.1, the noise is referred as $1/f$-like noise. Flicker noise is most significant at low frequencies while it disappears under thermal noise at higher frequencies. However, in devices showing a high level of $1/f$ it can dominate also in the MHz range. Flicker noise is also called *pink noise* because of the frequency dependence of the spectral density. $1/f$ noise occurs in many different systems and sometimes the suggestive adjective 'ubiquitous' is associated to this noise. It is possible to find $1/f$ noise, in biology, astronomy, fluid dynamics, optical systems and economics.

4.3 MOSFETs 1/f noise model

MOSFETs are particularly affected by low-frequency noise having a spectral density inversely proportional to the frequency ($1/f$ or $1/f$-like noise). $1/f$ noise in MOSFETs has been under investigation since more than forty years [31]. Despite the efforts to identify the origins of this noise, there is still not a unique accepted theory and therefore a model to simulate flicker noise. Two different theories have been proposed to explain the physical origins of $1/f$ noise: number fluctuation and mobility fluctuation. These two theories are based on the fluctuation of the conductivity of MOS transistors that is:

$$\sigma = \mu n q \tag{4.18}$$

where μ and n are the mobility and the concentration of the carriers, respectively. Hence, from Eq. 4.18 it is clear that a fluctuation of the conductivity is induced either by a fluctuation of the number of carriers (ΔN) or a fluctuation in the channel mobility ($\Delta\mu$).

4.3.1 ΔN model

The carrier number fluctuation theory [32, 33, 34, 35], originally proposed by McWhorter [36], attributes the origin of flicker noise to the random trapping and

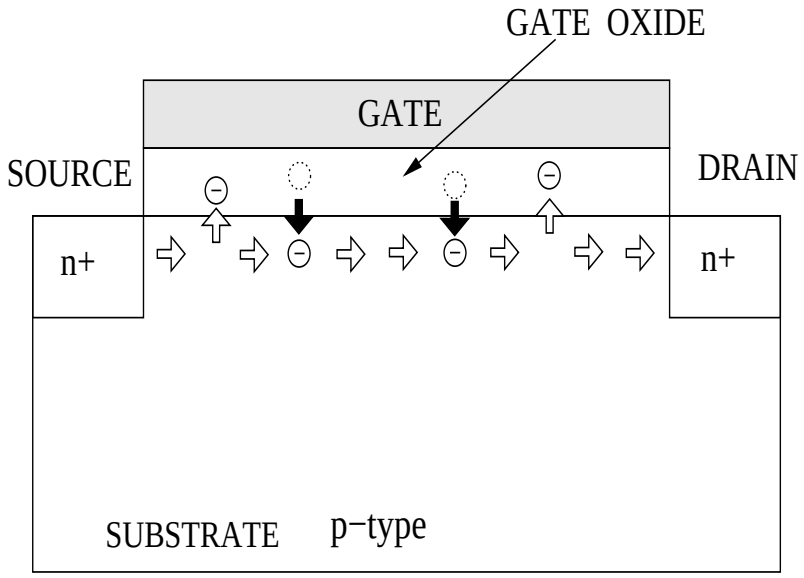


Figure 4.2: Schematic illustration of trapping/detrapping of electron in/from traps for a nMOSFET.

detrapping of charge carriers into or from traps located inside the oxide. Trapping/detrapping process from a single trap leads to an RTS. Each trap is characterized by a relaxation time τ that depends on the mean time needed for the trapping process and the mean one needed for detrapping. The trapping/detrapping process occurs through the tunneling of charge carriers from the channel into traps located inside the oxide and vice versa. A schematic illustration is represented in Fig. 4.2.

For a given trap characterized by the relaxation time τ, the occupation function $N(t)$ is defined as: $N{=}1$ when the trap is occupied, $N{=}0$ when the trap is empty. The power spectral density of $N(t)$ is given by:

$$S_N(\tau) = (\Delta N)^2 \frac{4\tau}{1 + (2\pi f)^2 \tau^2} \tag{4.19}$$

When several traps are present with time constants τ distributed as:

$$g(\tau) = \begin{cases} K/\tau & \text{if } \tau_1 < \tau < \tau_2 \\ 0 & \text{otherwise} \end{cases} \tag{4.20}$$

The superposition of RTS signals due to each traps gives a $1/f$ noise with PSD given by:

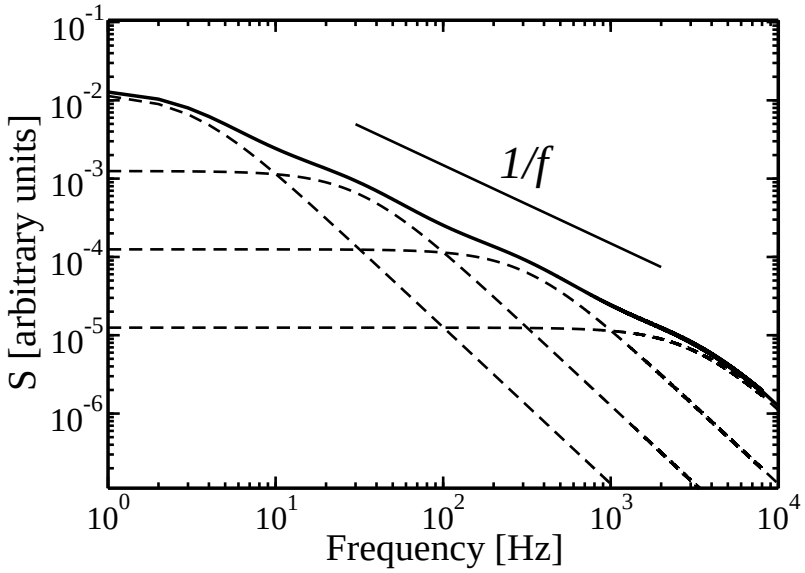


Figure 4.3: The superposition of 4 Lorentzians gives a total power spectral density roughly proportional to $1/f$ over several decades of frequency.

$$\begin{aligned} S(f) &= \int_0^\infty g(\tau) S_N(\tau)\, d\tau \\ &= \int_0^\infty \frac{K}{\tau}(\Delta N)^2 \frac{4\tau}{1+(2\pi f)^2\tau^2}\, d\tau \\ &= \frac{4K(\Delta N)^2}{2\pi f}\left[arctan(2\pi f\tau)\right]_{\tau_1}^{\tau_2} \\ S(f) &\approx \frac{K}{f}(\Delta N)^2 \ \text{ for } \ 1/2\pi\tau_2 << f << 1/2\pi\tau_1 \end{aligned} \tag{4.21}$$

An example is given in Fig. 4.3 where the superposition of the effects of four individual traps with different relaxation times roughly gives a $1/f$ spectrum. In order to extend the $1/f$ spectrum over ten decades, the spread in time constants must cover many order of magnitude. In MOSFETs the tunneling in the oxide may account for relaxation times between 10^{-5} s and 10^{+8} s. McWhorter showed as a uniform spatial distribution of oxide traps can give rise to a distribution of time constants giving the $1/f$ spectrum typical of MOS transistors [36]. Even if the number fluctuation model is supported by many experiments [34, 37, 38, 39, 40], some remarks are necessary. First, it is assumed that the RTS noise of each single trap can be simply added. This is true only if traps are isolated and do

not interact with each other. Secondly, each trap should be coupled to the output current in the same way (same values for K in Eq. 4.20 for all traps).

4.3.2 $\Delta\mu$ model

A second mechanism that can give a $1/f$ noise is the mobility fluctuation. The noise of homogeneous layers can be described by Hooge's empirical formula [41, 42, 43]:

$$\frac{S_I}{I^2} = \frac{\alpha_H}{fN} \tag{4.22}$$

where I is the current flowing through the sample, S_I is the spectral density of the noise affecting the current, N is the number of free carriers, and α_H is the Hooge's parameter that usually can assume values between 10^{-6} and 10^{-4} [44].

The step now is to determine whether the conductivity fluctuates because of fluctuations in the number of carriers or in their mobility. While number fluctuation can be a reason to explain the conductivity fluctuation in MOSFETs, obviously this cannot be the case in metals.

The only way to separate the ΔN and $\Delta\mu$ is to measure an effect that does not involve an $n\mu$ product. Such effects are the Hall effect, hot electron effects, etc. [44, 45]. An experimental example of the Hall effect in GaAs is presented in [46], where the noise measured across the Hall contacts follows the mobility fluctuations ($\Delta\mu$).

The mobility is determined by the scattering of free carriers. A scattering mechanism that is always present is caused by the acoustic lattice vibrations. However, other scattering mechanisms might be present in a MOSFET: impurity scattering by charged or neutral centers, surface scattering against the crystal boundaries, and carrier scattering by other carriers. The study of $1/f$ noise is of special interest when at least two different scattering mechanisms are present. Considering therefore the case of a varying amount of impurity scattering, together with the always present lattice scattering, the contribution of the two mechanisms to the resulting mobility can be expressed with the Matthiessen's rule:

$$\frac{1}{\mu} = \frac{1}{\mu_{latt}} + \frac{1}{\mu_{imp}} \tag{4.23}$$

The observed noise is plotted as $log\alpha_H$ versus $log\mu$ [47]. The $\alpha_H - \mu$ dependence experimentally found can only be explained by assuming $1/f$ noise in the

lattice scattering while the other mechanisms are noise free. From Eqs. 4.22 and 4.23 following [44, 45, 46] we get:

$$\frac{1}{\mu}\left(\frac{\Delta\mu}{\mu}\right) = \frac{1}{\mu_{latt}}\left(\frac{\Delta\mu_{latt}}{\mu_{latt}}\right) + 0 \tag{4.24}$$

$$\alpha_H = \left(\frac{\mu}{\mu_{latt}}\right)^2 \alpha_{latt} \tag{4.25}$$

Measuring the noise in the intensity of scattered light provides an independent way of proving that the intensity of acoustic lattice modes fluctuates with a $1/f$ spectrum [44].

4.3.3 Unified ΔN and $\Delta\mu$ model

Both ΔN and $\Delta\mu$ theories try to explain and to find correlation between experiments and arguments to support one or the other theory. In MOSFETs, where the charge transport is at the interface, the number fluctuation model apparently provides a better explanation of the origin of $1/f$ noise. Some measurements on devices fabricated with different CMOS processes featuring different oxide thicknesses suggest that flicker noise in nMOS transistors behaves as predicted by the number fluctuation model [48]. In the same study, however, pMOS transistors show a lower $1/f$ noise which is well explained by the mobility fluctuation model.

An extensive analysis of flicker noise in MOSFETs gives a more complicated bias dependence on the gate bias and on the oxide thickness that cannot be predictable by only the number fluctuation or only mobility fluctuation models alone. Hung [49, 50] proposed a unified model that assumes correlated mobility and number fluctuations. The surface mobility fluctuations are attributed to the remote Coulomb scattering due to oxide charges. As mobility and number fluctuations have the same source of origin they are correlated. It is important to remark that the correlated mobility fluctuations in the Hung's unified model are different from the mobility fluctuation previously discussed in the $\Delta\mu$ model whose origin is due to phonon scattering. The unified model is the most used one among those adopted to simulate flicker noise in circuit design tools. It is able to explain most of the experimental data; when this is not true [51], it uses non-physical fitting parameters. The model unifies the number fluctuation model which dominates at low bias and the mobility model which is mostly effective at high bias.

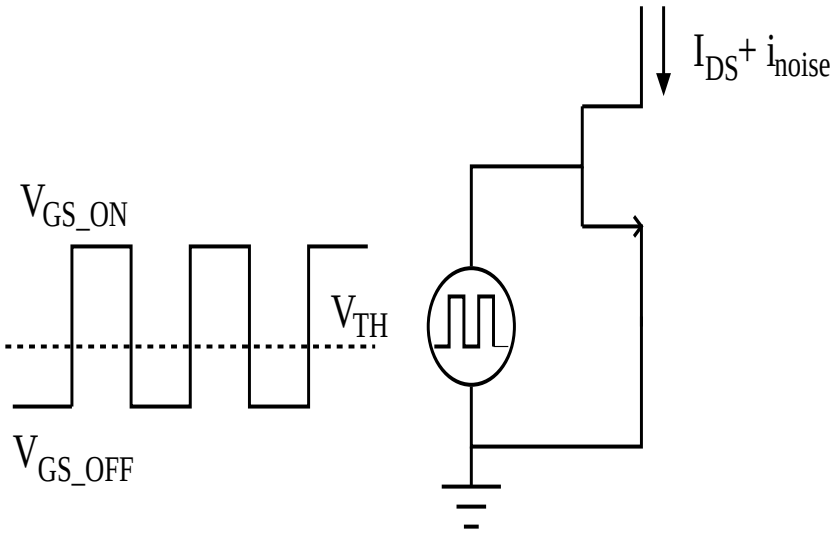


Figure 4.4: nMOSFET cycled between an ON-state (V_{GS_ON}) and an OFF-state (V_{GS_OFF}).

4.4 Flicker noise under switched bias conditions

Flicker noise has a large influence in circuits using MOSFET transistors. Therefore, in the last years a lot of circuit techniques have been proposed in order to reduce its impact [52, 53, 54, 55, 56]. These techniques are anyway unable to reduce the intrinsic $1/f$ noise in MOSFETs.

Bloom and Nemirovsky [6], for the first time, showed that by cycling a MOSFET between strong inversion and accumulation a reduction of the low-frequency noise occurs. Indeed, [7] reported that also RTS noise generated by a single trap is strongly reduced when the MOSFET is cycled between inversion and accumulation. The effect was again observed in ring oscillator phase noise [8] fabricated with a CMOS process.

In Fig. 4.4 the basic principle of cycling a nMOSFET between an ON-state and an OFF-state is illustrated. The input voltage applied to the gate terminal is switched between an ON- and an OFF-state with a pulse signal with 50% duty cycle. Such a bias it is usually called switched bias (SB), the counterpart to a fixed constant bias (CB). The high level (V_{GS_ON}) is higher than the threshold voltage in order to bias the transistor in inversion, while the low level (V_{GS_OFF}) is set below the threshold voltage. V_{GS_OFF} can be set to have the transistor in moderate inversion, weak inversion or in accumulation. In this configuration an intrinsic reduction of the low-frequency noise, compared to constant bias condi-

tions, is due to the fact that the device is OFF for half a period. This translates in an intrinsic reduction by a factor of 4 in the resulting PSD of the noise [57] due to the mixing effect of low frequencies to higher frequencies. Hence, in the analysis presented in this work, the PSD in the case of constant bias is usually divided by a factor of 4 in order to be compared to the PSD under switched bias conditions.

In the last years new progresses in this field have been made. A new measurement approach that allows the observation of $1/f$ noise spectra in MOSFETs under switched bias conditions in a wide frequency band (10 Hz - 100 kHz) has been reported in [57]. They investigated in particular the dependence of flicker noise on the switching frequency and on the voltage applied in the OFF-state.

4.5 Background of Random Telegraph Signal

In this section we provide the necessary background of RTS noise in order to explain and to analyze experimental results.

4.5.1 Statistical properties of RTS

RTS is a random sequence of pulses that switch between two levels: a high and a low state (Fig. 4.5). In our work, we are interested in the RTS noise superimposed to the drain current of small-area MOSFETs. We can associate the state 1 to the high level, and the state 0 to the low level. We assume that the probability of a transition from the state 1 to the state 0 (i.e. from up to down) is given by $1/\tau_1$, the probability of a transition from 0 to 1 is $1/\tau_0$. We also assume that the transitions are instantaneous. Under these assumptions, we show that the random variables representing the times spent in states ”high” and ”low” are exponentially distributed and therefore RTS is a Poisson process.

Let us assume $p_1(t)dt$ the probability that no transition occurs from the state 1 during the time interval t and then a transition happens between t and $t + dt$. If $P(t)$ is the probability of remaining in the ”high” state without making any transition during the time interval t, we get:

$$p_1(t) = P(t)/\tau_1 \tag{4.26}$$

remembering the assumption that $1/\tau_1$ is the probability of making a transition from state 1 to state 0.

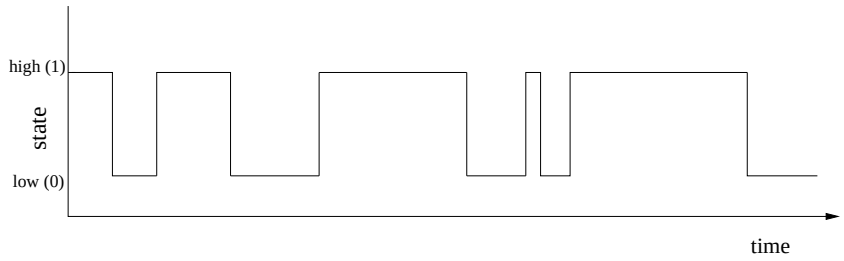


Figure 4.5: A Random Telegraph Signal (RTS).

We have also that:

$$P(t+dt) = P(t)(1 - dt/\tau_1) \tag{4.27}$$

that means that the probability of not making a transition at time $t + dt$ is equal to the product of the probability of not having made a transition at time t and the probability of not making a transition during the interval from t to $t + dt$. Rearranging Eq. 4.27 we obtain:

$$\frac{dP(t)}{dt} = -\frac{P(t)}{\tau_1} \tag{4.28}$$

Now we need to integrate Eq. 4.28 and we get:

$$P(t) = exp(-t/\tau_1) \tag{4.29}$$

With $P(0) = 1$ we get:

$$p_1(t) = \frac{1}{\tau_1} exp(-t/\tau_1) \tag{4.30}$$

and

$$\int_0^\infty p_1(t)dt = 1 \tag{4.31}$$

Following the same procedure for the state ”low” we obtain:

$$p_0(t) = \frac{1}{\tau_0} exp(-t/\tau_0) \tag{4.32}$$

From this analysis, starting with the assumption that the transitions between the high/low and the low/high states are described by single rates, we can show that the times spent in the high/low states are exponentially distributed. The mean time spent in the state ”high” is:

$$\int_0^\infty t p_1(t) dt = \tau_1 \tag{4.33}$$

and the standard deviation is:

$$\sigma \equiv \left[\int_0^\infty t^2 p_1(t) dt - \tau_1^2 \right] = \tau_1 \tag{4.34}$$

To conclude we can say that an RTS signal is characterized by switching between two states, high and low, and that the time spent in both states is exponentially distributed. This shows that RTS is a Poisson process. To each state it is possible to associate a mean time τ_1 and τ_0. We have also seen that the standard deviation is equal to the mean time spent in either state of the RTS and this is normal for a Poisson process.

4.5.2 PSD of RTS: Lorentzian spectrum

Here we derive the power spectral density of an RTS signal as proposed by Machlup [30]. We need first to evaluate the autocorrelation function of the RTS. In order to do that we suppose that the RTS can be in two states, 0 (low) and 1 (high), and that the amplitude of the signal is ΔI. We assume also that all the statistical properties are independent of the time origin. We know that the mean time spent in the state 1 is τ_1 while the mean time spent in the state 0 is τ_0. The probability that the RTS is in the state 1 is therefore $\tau_1/(\tau_0 + \tau_1)$, for the state 0 is $\tau_0/(\tau_0 + \tau_1)$.

The autocorrelation function of such an RTS process is:

$$\begin{aligned} R_{xx}(t) &= < x(s)x(s+t) > \\ &= \sum_i \sum_j x_i x_j \times \{\text{Prob. that } x(s) = x_i\} \\ &\times \{\text{Prob. that } x(s+t) = x_j, \text{given } x(s) = x_i\} \end{aligned} \tag{4.35}$$

Since the low state of the RTS is chosen to be 0 and the RTS amplitude is ΔI, the autocorrelation function is:

$$R_{xx}(t) = (\Delta I)^2 \frac{\tau_1}{\tau_0 + \tau_1} P_{11}(t) \tag{4.36}$$

where $P_{11}(t)$ is the probability of an even number of transitions during the time interval t, starting from state 1. Defining in a similar way $P_{10}(t)$ the probability of an odd number of transitions in time interval t, starting from state 1 we have:

$$P_{11}(t) + P_{10}(t) = 1 \tag{4.37}$$

The probability of an even number of transitions in time $t + dt$ is given by the sum of two mutually exclusive events. The first is the probability of an odd number of transitions during the time interval t and one transition during dt; the second is the probability of an even number of transitions in time interval t and no transition during dt:

$$P_{11}(t + dt) = P_{10}(t)\frac{dt}{\tau_0} + P_{11}(t)\left(1 - \frac{dt}{\tau_1}\right) \tag{4.38}$$

By letting $dt \rightarrow 0$ and substituting Eq. 4.37 into Eq. 4.38, we obtain the following differential equation for $P_{11}(t)$:

$$\frac{dP_{11}(t)}{dt} + P_{11}(t)\left(\frac{1}{\tau_0} + \frac{1}{\tau_1}\right) = \frac{1}{\tau_0} \tag{4.39}$$

Eq. 4.39 can be solved by using $exp[\int(1/\tau_0 + 1/\tau_1)dt]$ as an integrating factor:

$$P_{11}(t) = \frac{\tau_1}{\tau_0 + \tau_1} + \frac{\tau_0}{\tau_0 + \tau_1} exp\left[-\left(\frac{1}{\tau_0} + \frac{1}{\tau_1}\right)t\right] \tag{4.40}$$

The power spectral density can be calculated from Eqs. 4.36 and 4.40 applying the Wiener-Khinchin theorem:

$$\begin{aligned} S(f) &= 4\int_0^\infty R_{xx}(t)cos(2\pi f\tau)d\tau \\ &= \frac{4(\Delta I)^2}{(\tau_0 + \tau_1)[(1/\tau_0 + 1/\tau_1)^2 + (2\pi f)^2]} \end{aligned} \tag{4.41}$$

where the DC term, a delta function at f=0, has been ignored.

In the case of RTS with equal mean times in the high and in the low state, τ_0=τ_1=τ, Eq. 4.41 becomes:

$$S(f) = \frac{2(\Delta I)^2\tau}{4 + (2\pi f\tau)^2} \tag{4.42}$$

The total average power is obtained by integrating $S(f)$ over all frequencies:

$$P = \int_0^\infty S(f)df = \frac{(\Delta I)^2}{(\tau_0 + \tau_1)(1/\tau_0 + 1/\tau_1)} \tag{4.43}$$

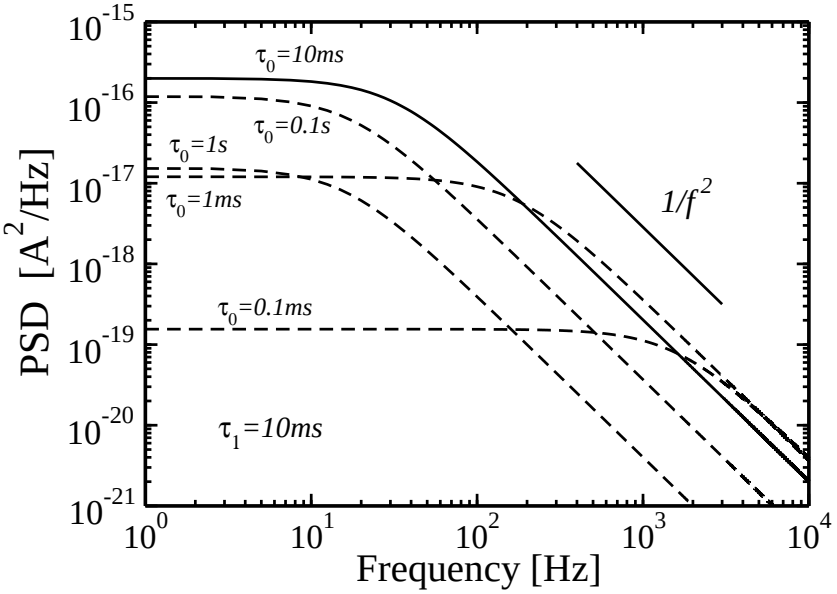


Figure 4.6: Power spectral density of RTS noise with τ_1=10 ms and different values of τ_0. The PSD is a typical Lorentzian, flat at low frequencies and a roll-off of $1/f^2$ at high frequencies.

In Fig. 4.6 the PSD from Eq. 4.41 is reported for ΔI=200 nA, τ_1=10 ms while τ_0 is varied. RTS features a typical Lorentzian PSD characterized by a constant plateau at low frequencies and a $1/f^2$ roll-off above a characteristic cut-off frequency f_t=$1/2\pi(1/\tau_0 + 1/\tau_1)$.

Fig. 4.7 reports the power associated to the RTS from Eq. 4.43. The amplitude of the RTS is ΔI=200 nA and τ_1=10 ms. τ_0 is varied between 0.1 ms and 1 s. The power shows a maximum when τ_0 is equal to τ_1. In this work, the relation between RTS time constants and the noise power is quite important, especially when we analyze RTS noise under switched bias conditions.

4.6 RTS noise in MOSFETs

As already stated, in this thesis we are interested in the RTS noise that affects the drain current of small-area MOS transistors. In MOSFETs, RTS noise is caused by the trapping/detrapping of charge carriers into/from traps that can be located at the Si-SiO_2 interface or in the bulk of the gate oxide. In this scenario it is possible to associate the mean time spent by the current in the high or in the

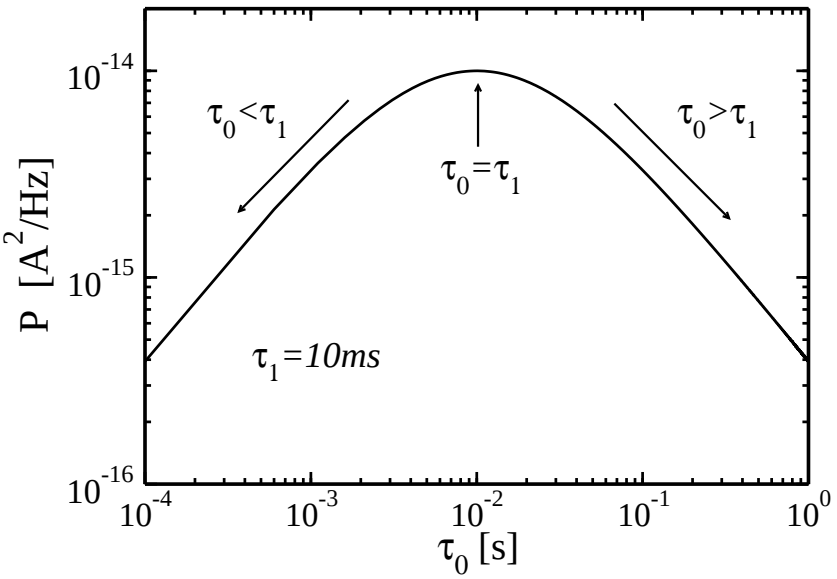


Figure 4.7: Power of RTS noise with τ_1 =10 ms and different values of τ_0. The PSD shows a maximum for $\tau_0 = \tau_1$.

low state with the mean emission or capture times τ_e and τ_c. To associate τ_e and τ_c to the state of the current some considerations must be done and this will be discussed in the next chapter. For the purpose of the next part of this chapter it is enough to know that the emission and capture time constants are associated to capture and emission of charge carriers by a trap.

As for flicker noise, also RTS noise can be measured and modeled under both constant bias (CB) and switched bias (SB) conditions. In particular, in the last years, some important steps have been done in the modeling and in the characterization of RTS noise under SB conditions. In [58] measurements and simulation of RTS noise in nMOSFETs under switched gate bias conditions have been proposed. They have shown that the simple model of a stationary noise generating process whose output is modulated by the bias voltage is not sufficient to explain the switched bias measurement results. This is due to the fact that a simple modulation should give a noise reduction of a factor of 4, while experimental results showed devices where the noise reduction could be both higher or lower than this factor. Therefore, they proposed a model based on cyclostationary RTS noise generation. A new physical model, reproducing the transient behavior and predicting the RTS noise under switched bias conditions has been proposed in [59].

4.6.1 RTS under constant bias conditions

The expressions for the autocorrelation function and the power spectral density reported in the previous section following the Machlup's [30] approach can be used to model the RTS noise of MOSFETs operating under constant bias conditions.

The autocorrelation function can be rewritten as:

$$R_{xx} \propto \gamma(1-\gamma)e^{(-|t|/\tau)} \tag{4.44}$$

while the PSD as:

$$PSD \propto \gamma(1-\gamma)\frac{\tau}{1+(2\pi f\tau)^2} \tag{4.45}$$

where:

$$\tau = \frac{\tau_e\tau_c}{\tau_e+\tau_c} \tag{4.46}$$

$$\gamma = \frac{\tau_e}{\tau_e+\tau_c} \tag{4.47}$$

$$1-\gamma = \frac{\tau_c}{\tau_e+\tau_c} \tag{4.48}$$

It is important to notice that γ represents the occupation probability of a trap under constant bias conditions.

4.6.2 RTS under switched bias conditions

As we have seen in section 4.4, a transistor may be switched between an ON- and an OFF-state. To do that it is necessary to apply to the gate terminal a pulsing waveform that biases the transistor between strong inversion and subthreshold/accumulation. Under this operating condition, the emission and the capture time constants of the RTS noise are modulated. Even if obvious, it is important to remark that, when the transistor is in the OFF-state, no current flows and so the emission and the capture times are not directly measurable.

Kolhatkar in [60] proposes an experimental method to measure the emission and capture time constants under SB conditions. This method, represented in Fig. 4.8, consists in sampling the RTS during the ON-states and then, joining the sampled values together, the RTS under SB conditions is obtained. This

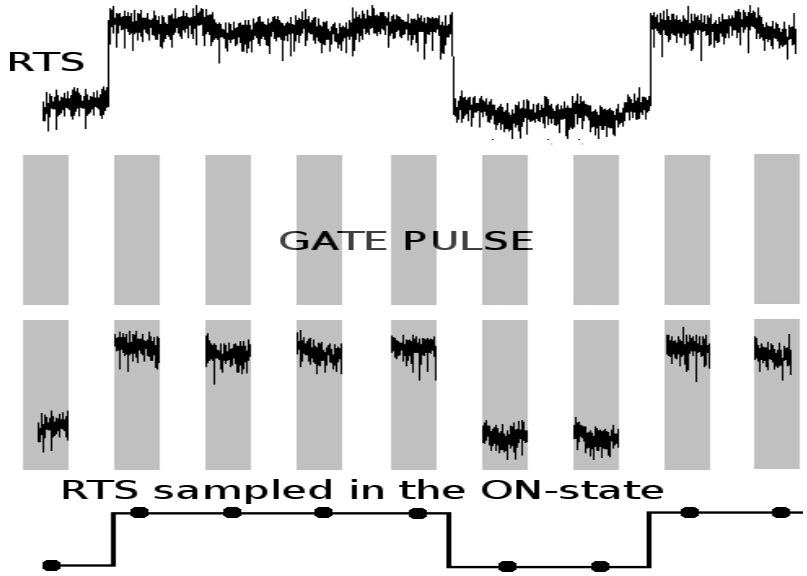


Figure 4.8: RTS noise under constant bias and switched bias conditions. RTS is sampled during the ON-states and joining the sampled values together the RTS under SB conditions is obtained. The ON-state is indicated by the shaded part and the OFF-state by the white part (source [60]).

method will be used in this work in Chapter 6. The expressions of the emission and capture time constants under SB are now derived following the approach proposed by Kolhatkar in [60].

Let's consider a pulse waveform applied to the gate switching between an ON- and an OFF-state with a switching period T_{sw}, being T_{on} and T_{off} the time spent in the ON- and in the OFF-state, respectively. Kolhatkar associates to the ON- and to the OFF-state different time constants: τ_{e_on} and τ_{c_on} to the ON-state, and τ_{e_off} and τ_{c_off} to the OFF-state.

The effective time constants in the ON- and in the OFF-state are expressed in a similar way as in Eq. 4.46 as:

$$\tau_{eff\_on} = \frac{\tau_{c\_on}\tau_{e\_on}}{\tau_{c\_on} + \tau_{e\_on}} \tag{4.49}$$

$$\tau_{eff\_off} = \frac{\tau_{c\_off}\tau_{e\_off}}{\tau_{c\_off} + \tau_{e\_off}} \tag{4.50}$$

The effective emission and capture time constants are given by:

$$\frac{1}{\tau_{e\_eff}} = \frac{T_{on}}{T_{sw}}\frac{1}{\tau_{e\_on}} + \frac{T_{off}}{T_{sw}}\frac{1}{\tau_{e\_off}} \tag{4.51}$$

$$\frac{1}{\tau_{c\_eff}} = \frac{T_{on}}{T_{sw}}\frac{1}{\tau_{c\_on}} + \frac{T_{off}}{T_{sw}}\frac{1}{\tau_{c\_off}} \tag{4.52}$$

Therefore, from expressions above we can express the effective τ as:

$$\tau_{eff} = \frac{\tau_{e\_eff}\tau_{c\_eff}}{\tau_{e\_eff} + \tau_{c\_eff}} \tag{4.53}$$

The autocorrelation function and the PSD under switched bias conditions become:

$$R_{xx} \propto \gamma(1-\gamma)e^{(-|t|/\tau_{eff})} \tag{4.54}$$

$$PSD \propto \gamma(1-\gamma)\frac{\tau_{eff}}{1+(2\pi f\tau_{eff})^2} \tag{4.55}$$

where:

$$\gamma = \frac{\tau_{e\_eff}}{\tau_{e\_eff} + \tau_{c\_eff}} \tag{4.56}$$

$$1-\gamma = \frac{\tau_{c\_eff}}{\tau_{e\_eff} + \tau_{c\_eff}} \tag{4.57}$$

γ represents also the effective occupation probability of a trap (P_{eff}) under switched bias conditions.

We can still write the occupation probability in the ON-state as:

$$P_{on} = \frac{\tau_{e\_on}}{\tau_{e\_on} + \tau_{c\_on}} \tag{4.58}$$

and in the OFF-state as:

$$P_{off} = \frac{\tau_{e\_off}}{\tau_{e\_off} + \tau_{c\_off}} \tag{4.59}$$

4.7 Monte Carlo simulation of RTS and 1/f noise

As we have seen in section 4.5.1, the emission and capture times of an RTS are exponentially distributed and RTS is therefore a Poisson process. The Monte Carlo (MC) simulation technique is ideally suited to simulate Poisson processes.

Supposing that the mean time associated with a Poisson process is τ_0, we can generate a Poisson stochastic time between two distinct events of the process as [61]:

$$t_r = -\tau_0 ln(1 - r) \tag{4.60}$$

where r is a random number uniformly distributed between 0 and 1. However, since r is uniformly distributed between 0 and 1, so also is $(1-r)$, and in practice, in place of Eq. 4.60 we can use:

$$t_r = -\tau_0 ln(r) \tag{4.61}$$

An RTS process is characterized by two possible states: empty trap and occupied trap. Two characteristic times,τ_c and τ_e, are associated to such states: τ_c is the mean time for an empty trap to capture a charge carrier, τ_e is the mean time for the trap to emit a charge carrier. Therefore each occurrence, trapping and detrapping, is conditioned by the other one. For example, a trapping event is possible only if before a detrapping event occurred. Dealing with a process with two characteristic time constants, we need to substitute in Eq. 4.61 the appropriate one according to the current state of the trap. Simulating an RTS process we use τ_e if the trap is occupied and, hence, the next occurrence is a detrapping, τ_c otherwise.

4.7.1 MC under constant bias conditions

Under constant bias conditions a fixed bias is applied to the gate of the transistor. In small-area MOSFETs, a single trap affects the drain current leading to the switching of the current between a high and a low value. This is due to the trapping and detrapping of charge carriers into or from the trap. The core of the simulation of RTS noise is therefore the evaluation of the occupation state of a trap as a function of the time. The simulation of the occupation state of the trap is performed as follows: initially a check on the state of the trap is done: *free* or *occupied*; then the state of the trap is changed after a certain time interval t_r according to Eq. 4.61 in which the appropriate time constant is used. When the occupation state of a trap changes, it contributes to the noise superimposed to the drain current. The amount of this contribution depends on several factors, among them the position of the trap inside the gate oxide. A way to take into account this fact in the simulation, is to ”weight” the contribution of the occurrence (trapping/detrapping) to the current. In other words it means to reflect the trapping/detrapping process to a certain variation of the drain current (ΔI). What we then obtain is a time domain RTS signal reproducing the effect of

trapping/detrapping process on the drain current. This signal switches therefore between two different states with mean times given by τ_e and τ_c and amplitude ΔI. In a second part of the simulation the autocorrelation function of the RTS signal and the Fourier transform of the autocorrelation are calculated in order to get the power spectral density of the simulated RTS.

4.7.2 MC under switched bias conditions

Under switched bias conditions a pulse waveform is applied to the gate of the transistor biasing the transistor between inversion and subthreshold/accumulation conditions, therefore between an ON- and an OFF-state. As described in section 4.6.2, we can model the effect of a switching bias by assuming different time constants during the ON- and the OFF-state. Adopting this approach we can therefore associate an emission time constant to the ON- and to the OFF-state, τ_{e_on} and τ_{e_off}, respectively, and a capture time constant to the ON- and to the OFF-state, τ_{c_on} and τ_{c_off}, respectively. We have therefore to deal with four different time constants. A quasi stationary assumption is done for modeling the emission and capture time constants: τ_{e_on} and τ_{c_on} are assumed to be the emission and capture time constants corresponding to the CB case with V_{GS}=V_{GS_ON}. While τ_{e_on} and τ_{c_on} are measurable because the transistor is ON and a net drain current is flowing, this is not possible when the transistor is in the OFF-state and no current flows. In order to model the time constants in the OFF-state we use the approach proposed in [58] where the relationships between the time constants in the ON- and in the OFF-state are assumed as:

$$\begin{aligned} \tau_{e\_off} &= \tau_{e\_on}/m \\ \tau_{c\_off} &= \tau_{c\_on} \times m \end{aligned} \tag{4.62}$$

where the parameter m is a positive number. The characteristic of this approach by taking the capture time constant in the OFF-state as the one in the ON-state multiplied by the constant m is physically supported by considering that the capture of a carrier is unlikely in the OFF-state of the device since no carriers are present in the channel.

Under these assumptions, the simulation differs only slightly compared to the one under constant bias conditions. In particular, under switched bias conditions it is necessary to know at each simulation time, not only the state of the trap, but also the state of the bias, ON or OFF. According to this two variables, state of

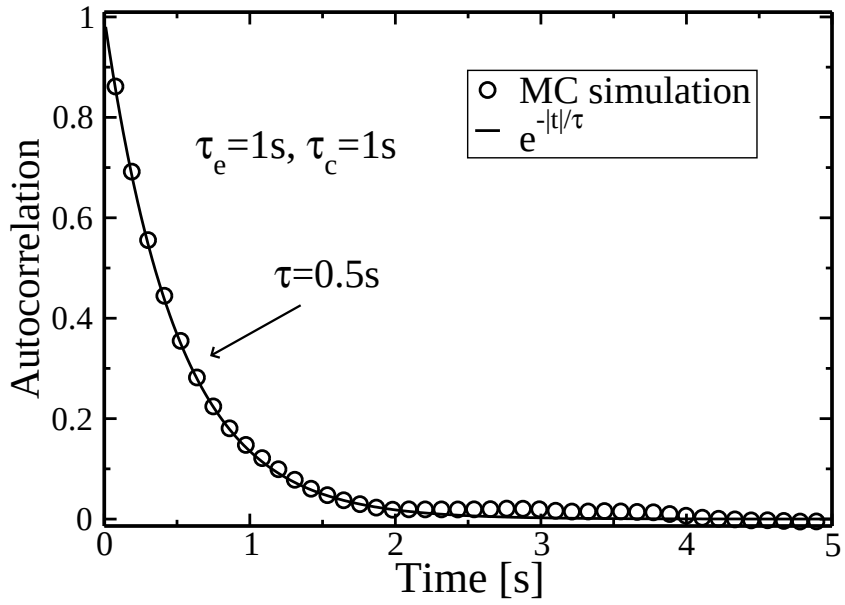


Figure 4.9: Monte Carlo simulation and analytical model of the autocorrelation of an RTS under CB with τ_e=τ_c=1 s.

the trap and state of the bias, the appropriate time constant must be chosen in Eq. 4.61. Indeed, under SB the drain current of the device is switched and, when the gate bias is OFF, no current flows in the transistor. That means that the RTS noise under SB is modulated by a square wave. Therefore, the drain current of the device can be considered as the product of two signals: the contribution of the trap giving the RTS and the square wave applied to the gate. It is important to reamark, see Fig. 4.8, that RTS continues to exist even when it cannot be directly observed because no current is flowing in the device. The square wave applied to the gate with a certain switching frequency f_{sw} contributes in the frequency domain with a series of δ functions at 0 Hz, $\pm f_{sw}$, $\pm 3f_{sw}$, $\pm 5f_{sw}$, ...

From Eqs. 4.51, 4.52, 4.62 we obtain:

$$\begin{aligned} \tau_{e\_eff} &= \frac{2}{m+1}\tau_{e\_on} \\ \tau_{c\_eff} &= \frac{2m}{m+1}\tau_{c\_on} \end{aligned} \tag{4.63}$$

Analyzing Eqs. 4.62 and 4.63 we can see as a change in τ_{c_off} is not as important as a change in τ_{e_off}. In the limit case of taking $m \rightarrow \infty$, τ_{c_eff} becomes twice τ_{c_on}. On the other hand, τ_{e_eff} can change by several orders of magnitude

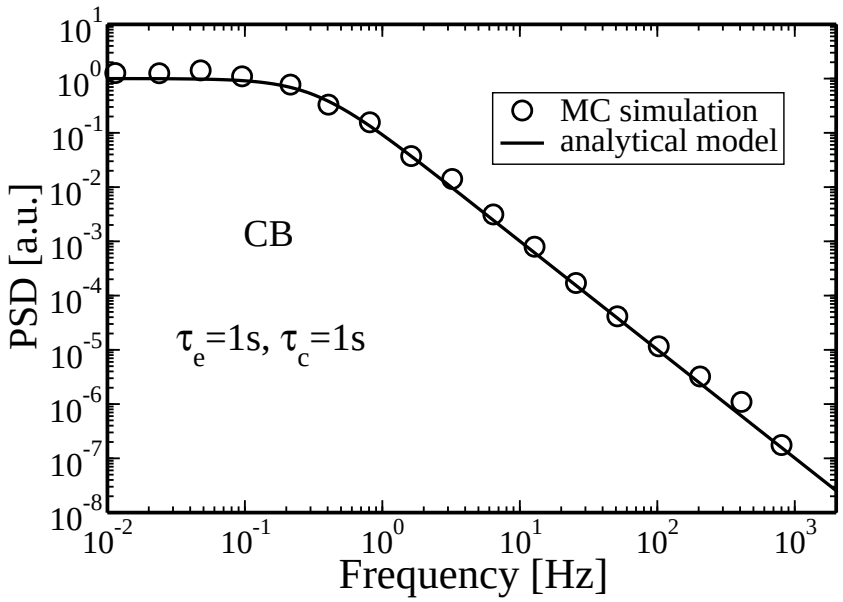


Figure 4.10: Monte Carlo simulation and analytical model of the PSD of an RTS under CB with τ_e=τ_c=1 s.

compared to τ_{e_on}. Further details on this approach are discussed in [58].

4.7.3 Validation

In order to validate the MC simulator, simulations under CB and SB conditions are performed and compared to the analytical models. Under CB we simulate both the autocorrelation function and the power spectral density of an RTS with emission and capture time constants τ_e=τ_c=1 s. Results for the autocorrelation function obtained by both the MC simulator and the analytical model of Eq. 4.44 are reported in Fig. 4.9. Results for the power spectral density are plotted in Fig. 4.10 where the analytical model of Eq. 4.45 is used. From these results we can see as MC simulations under CB are in good agreement with the analytical models.

Fig. 4.11 reports the comparison between the MC simulation of RTS under SB conditions and the analytical model provided by Eq. 4.55. The RTS is modulated by a square wave featuring a duty cycle of 50% and a switching period T_{sw}=1 ms, therefore f_{sw}=1 kHz. The emission and capture time constants in the ON- and in the OFF-state are: τ_{e_on}=τ_{c_on}=1 s, τ_{e_off}=τ_{e_on}/m, τ_{c_off}=$\tau_{c\_on} \times m$ with m=10. Results from Fig. 4.11 confirm the validity of the simulation ap-

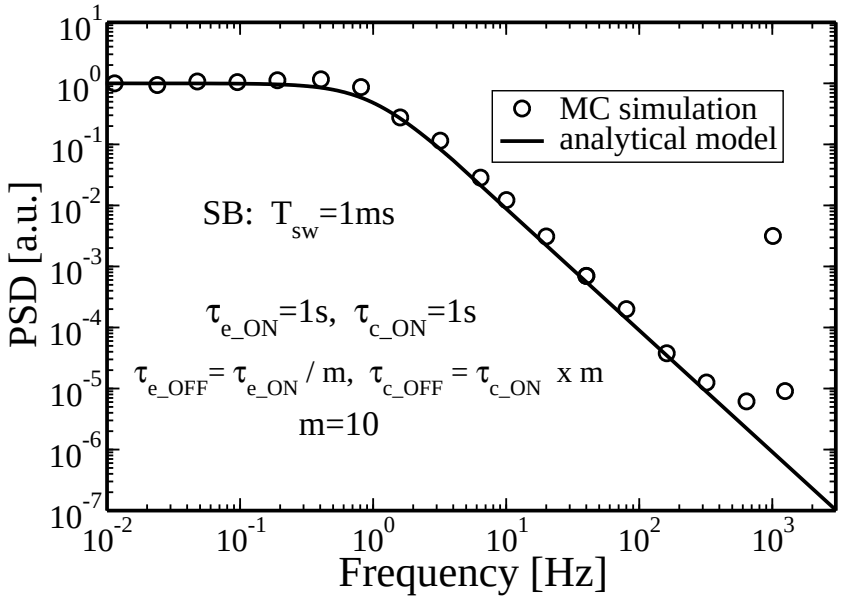


Figure 4.11: Monte Carlo simulation and analytical model of the PSD of an RTS under SB with T_{sw}=1 ms, 50% duty cycle, τ_{e_on}=τ_{c_on}=1 s, τ_{e_off}=τ_{e_on}/m, τ_{c_off}=$\tau_{c\_on} \times m$.

proach using the Monte Carlo technique also under SB conditions. We could notice that the PSD simulated by the MC shows the effect of the modulating square wave applied to the gate with a peak at f_{sw}. This is not the case for the PSD obtained by the analytical model.

4.7.4 Simulation of RTS noise under CB and SB conditions

In this section a comparison of the power spectral density of RTS noise under constant bias and switched bias conditions is performed by means of the MC simulator presented earlier. A simulation of the occupation probability of traps under SB is also reported. In particular, the variation of the occupation probability as a function of the time for different switching frequencies is discussed.

PSD under CB and SB

In Fig. 4.12 the power spectral densities simulated by the MC simulator under CB and SB conditions are reported. Under CB we simulate an RTS with emission and capture time constants τ_e=τ_c=5 ms. As we have seen in section 4.5.2, the

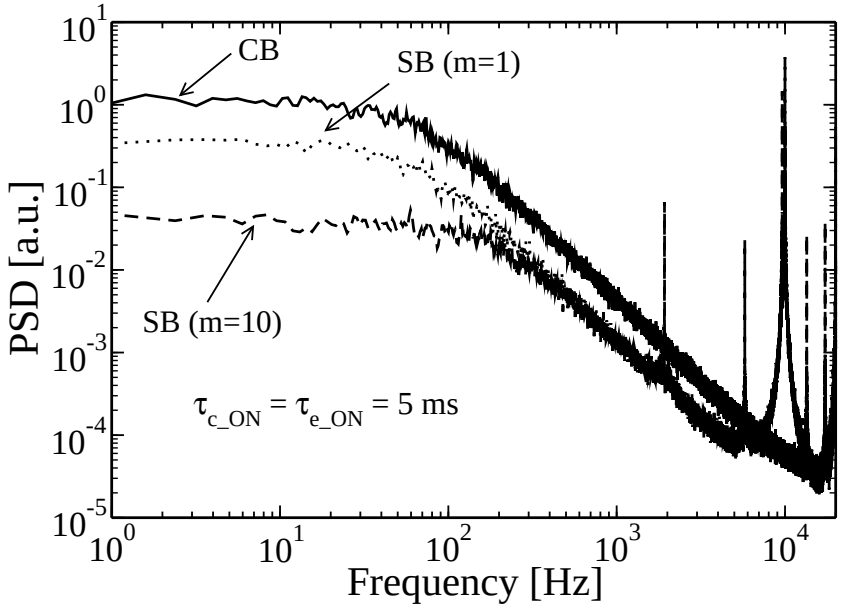


Figure 4.12: Monte Carlo simulated PSD of an RTS under: CB with τ_e=τ_{e_on}=5 ms and τ_c=τ_{c_on}=5 ms; SB (f_{sw}=10 kHz) with fixed τ_{e_off}=τ_{e_on}/m, τ_{c_off}=τ_{c_on} $\times$ m (m=1); SB (f_{sw}=10 kHz) with modulated τ_{e_off}=$\tau_{e\_on}/10$, τ_{c_off}=τ_{c_on} $\times$ 10 (m=10).

condition in which the emission and capture times are equal gives the maximum power associated to the RTS. In this case we can also observe the maximum value of the low-frequency plateau of the PSD. Under SB we apply to the gate of the device a square wave with a switching frequency f_{sw}=10 kHz and a 50% duty cycle. The emission and the capture time constants in the ON-state are set as in the CB case while the time constants in the OFF-state are obtained by Eq. 4.62 with two different values of the parameter m: m=1 and m=10. In the first case there is no modulation of the time constants between the ON- and the OFF-state, on the other hand, assuming m=10 the emission time constant in the OFF-state is ten times faster than in the ON-state, while the capture time constant is ten times slower. As a result of this modulation, the effective emission and capture time constants become (from Eq. 4.63):

$$\begin{aligned} \tau_{e\_eff} &\simeq 0.9 \text{ ms} \\ \tau_{c\_eff} &\simeq 9 \text{ ms} \end{aligned} \tag{4.64}$$

As clear from Fig. 4.12, the PSD under SB without modulation of the time

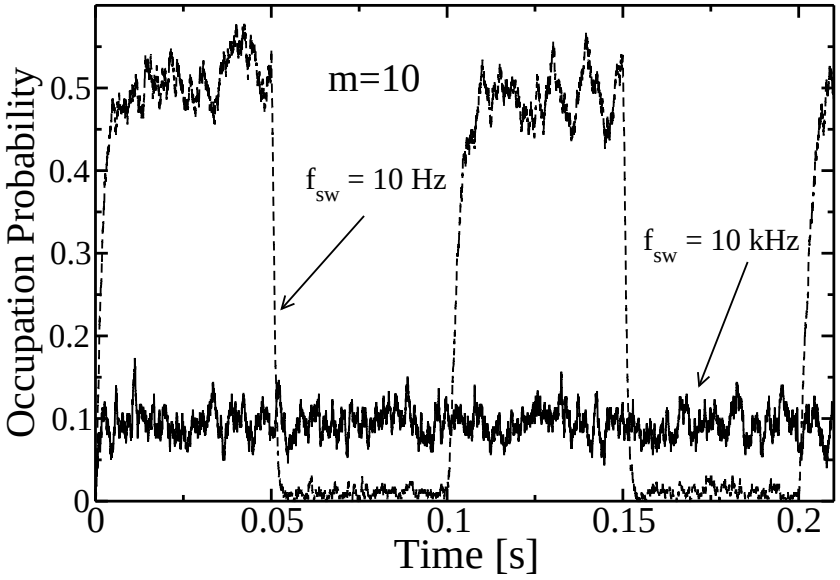


Figure 4.13: Occupation probability simulated with MC under SB conditions with two different switching frequencies: quasi-static f_{sw}=10 Hz and very large f_{sw}=10 kHz. Emission and capture time constants in the ON-state are taken equal τ_{e_on}=τ_{c_on}=5 ms. In the OFF-state are modulated with a m=10.

constants (m=1) shows a 6 dB reduction due the fact that for half a period the transistor is in the OFF-state [57] and no current is flowing. On the other hand, a modulation of the time constants (m=10), further reduces the noise. Noise reduction can be explained with the help of Fig. 4.7. A trap gives the maximum noise contribution when the emission and capture time constants associated to that trap are the same, i.e. τ_e=τ_c. Under SB conditions with m=10 the unbalance between the emission and the capture time constants (Eq. 4.64) gives the noise reduction as shown in Fig. 4.12.

Occupation probability under SB

The MC simulator is also able to simulate the occupation probability of a trap as a function of the time. To do that the simulation must be carried out for a large number of traps featuring the same time constants. At each simulation time the trap-occupancy is calculated by averaging the state (free or occupied) of each trap over the total number of simulated traps.

In Fig. 4.13 MC simulation of the occupation probability of a trap under

SB condition is reported. The trap features emission and capture time constants in the ON-state τ_{e_on}=τ_{c_on}=5 ms and modulated τ_{e_off} and τ_{c_off} with m=10 in the OFF-state. The simulation is performed for two different switching frequencies: a quasi-static f_{sw}=10 Hz and a very large f_{sw}=10 kHz. In the case of f_{sw}=10 Hz, the occupation probability varies between two different values. The values assumed in the ON- and in the OFF-state, P_{on} and P_{off}, are well described by Eq. 4.58 and Eq. 4.59, respectively. In particular, the trap-occupancy increases exponentially from P_{off} to P_{on}, and decrease exponentially from P_{on} to P_{off}, in a cyclic manner. For the analyzed trap we have $P_{off} \rightarrow 0$ and P_{on}=0.5. On the other hand, for a very large f_{sw}=10 kHz, the occupation probability of the trap cannot follow the switching frequency and assumes a constant value (P_{eff}) well described by Eq. 4.56, hence, in this case $P_{eff} \simeq 0.09$. Intuitively, it happens because slow traps cannot adapt quick enough to fast changes in the biasing.

The study of the occupation probability of a trap under SB conditions is another way to explain the effect of the noise reduction shown in Fig. 4.12. In particular, we have seen as the trap-occupancy under SB conditions with large switching frequency is much lower than expected under quasi-static (i.e. CB conditions) due to the effect of the switching bias on the time constants associated to the trap. As a result, the trap is almost always empty producing therefore a lower RTS noise superimposed to the drain current of MOS transistors.

4.7.5 Simulation of flicker noise

As we have seen in section 4.3, flicker noise can be caused by the superposition of the RTS noise generated by traps featuring different time constants. In the previous sections we have presented a MC simulator able to evaluate the effect of RTS noise on the drain current of a transistor due the presence of a trap in the oxide. Simulations can be performed under both constant bias and switched bias conditions. RTS noise simulation is performed in the time domain generating a process characterized by two time constants distributed with a Poisson statistic. The time constants are the mean time needed by a trap to capture a charge carrier and the mean time to emit it. In this frame, by simulating a certain number of RTS processes with different time constants and then summing the contribution to the drain current of each of these processes leads to a time domain signal featuring a $1/f$ spectrum. The frequency range in which the spectrum shows a $1/f$ slope depends on the distribution of the time constants of the elemental RTS

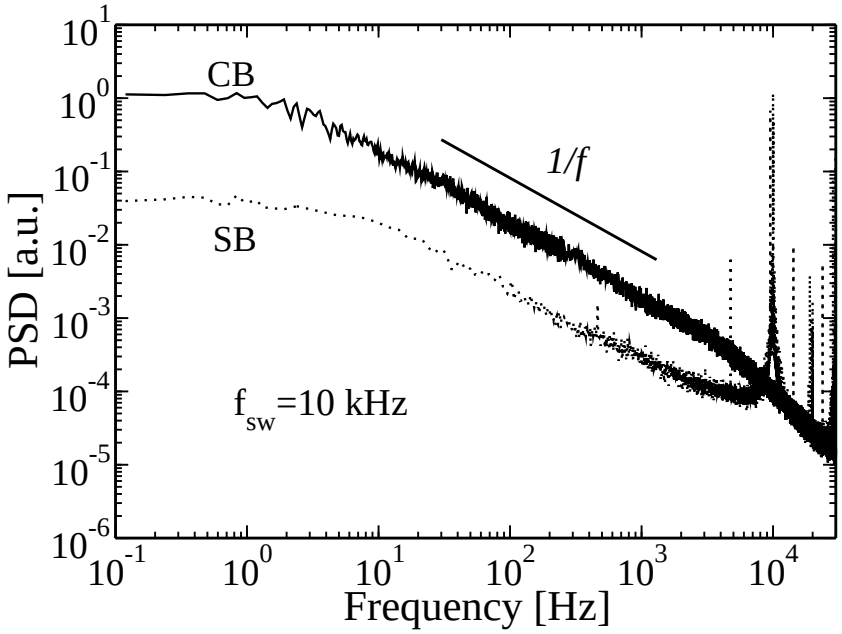


Figure 4.14: Monte Carlo simulation of flicker noise under CB and SB conditions with f_{sw}=10 kHz.

processes as discussed in section 4.3.1.

Simulations of flicker noise can be performed under both CB and SB conditions.

In Fig. 4.14 the MC simulation of the PSD of flicker noise under CB and SB conditions obtained by the superposition of different RTS are reported. Under CB, simulation of four different traps having time constants reported in Table 4.1 have been performed.

Under SB conditions the time constants are modulated during the ON- and the OFF-state. In the simulation, the values of emission and capture time constants in the ON-state for each trap are assumed the same as under CB conditions (Ta-

Trap	τ_e	τ_c
1	100 ms	100 ms
2	10 ms	10 ms
3	1 ms	1 ms
4	0.1 ms	0.1 ms

Table 4.1: τ_e and τ_c for the four different traps simulated to generate flicker noise

ble 4.1); while in the OFF-state the time constants are modulated according to Eq. 4.62 with m=10.

From Fig. 4.14 we can notice that, under CB, the effect of four traps featuring different time constants roughly gives a $1/f$ spectrum over several decades of frequency. Under SB conditions a noise reduction is observed for frequencies below f_{sw} due to the modulation of the time constants during the ON- and the OFF-state.

Results of MC simulation reported in Fig. 4.14 show that, as for RTS noise, also flicker noise can be reduced under SB conditions. This reduction can be explained as the effect of the modulation of the time constants on the occupation probability of the traps whose superposition causes the $1/f$ noise.

Chapter 5

Modeling of RTS under constant bias conditions

RTS is becoming more and more a limiting factor in CMOS circuits adopting small-area devices [4, 5]. A good modeling of RTS is then a major issue. An important aspect is the gate bias dependence of RTS noise. In particular, we have seen that the noise power associated to the RTS assumes its maximum when the emission and capture time constants assume the same value. Every event that produces a departure from this condition will reduce the noise associated to the trap producing RTS noise. Therefore, the gate bias dependence of the RTS time constants is of crucial importance to estimate the noise affecting the drain current of small-area MOSFETs. By means of a frequency domain analysis we can extrapolate the characteristic time constant τ of the RTS process by inspection of the cut-off frequency of the PSD associated to the RTS. τ is the composition of both the emission and the capture time constants, τ_e and τ_c. In order to be able to extract separately the values of τ_e and τ_c a time domain analysis is mandatory. This chapter is organized as follows: after a brief introduction on different kind of traps present in the silicon dioxide, the basis of the Shockley-Read-Hall (SRH) theory for trapping and detrapping of electrons in traps located at the silicon oxide interface or inside the oxide is given. Finally, measurement and simulation of the gate voltage dependence of RTS emission and capture time constants under constant bias conditions for n and pMOS transistors are presented.

5.1 Traps and RTS noise

The most important step toward the success of CMOS technology has been the development of the high quality silicon dioxide (SiO_2). SiO_2 is a good insulator and forms an almost perfect electrical interface with the silicon substrate of a MOS transistor. Even if the silicon dioxide has been part of the success of CMOS technology, it presents some defects that influence the working of MOSFETs [62] (Fig. 5.1):

- The interface traps (Q_{it}), which are located at the Si-SiO_2 interface with energy states in the silicon band gap. They can be produced by excess silicon, excess oxygen, metal impurities, and from different kinds of bond breaking processes such as hot carrier stress and radiation.

- Fixed oxide charges (Q_f), which are located at or near the interface. Different factors influence the density of these charges: oxidation temperature, silicon orientation, and cooling conditions. They are not influenced by an applied electric field and they are fixed.

- Oxide trapped charges (Q_{ot}), these traps can be created, for example, by hot electron injections, by Fowler-Nordheim tunneling, by ionizing radiation, and may be positive or negative due to trapping of holes or electrons. They are distributed inside the oxide and can influence the characteristic of the transistors changing the threshold voltage.

- Mobile ionic charges (Q_m), such as sodium or potassium ions, that can be introduced by an external contamination during the process. These mobile charges, under the effect of an electric field applied across the oxide, can move from one end of the oxide to the other one.

Interface and oxide trapped charges can exchange charge with the bulk region of the transistor while that does not happen for fixed oxide charges and mobile ionic charges. Depending on the surface potential, interface and oxide trapped charges can be filled or emptied by electrons or holes. Two different kinds of traps have been recognized, acceptor-type and donor-type. Assuming electrons as charge carriers, the acceptor-type traps are neutral when empty and negatively charged when filled. The donor-type traps are neutral when filled and positively charged when empty. RTS noise can be originated by both kinds of traps.

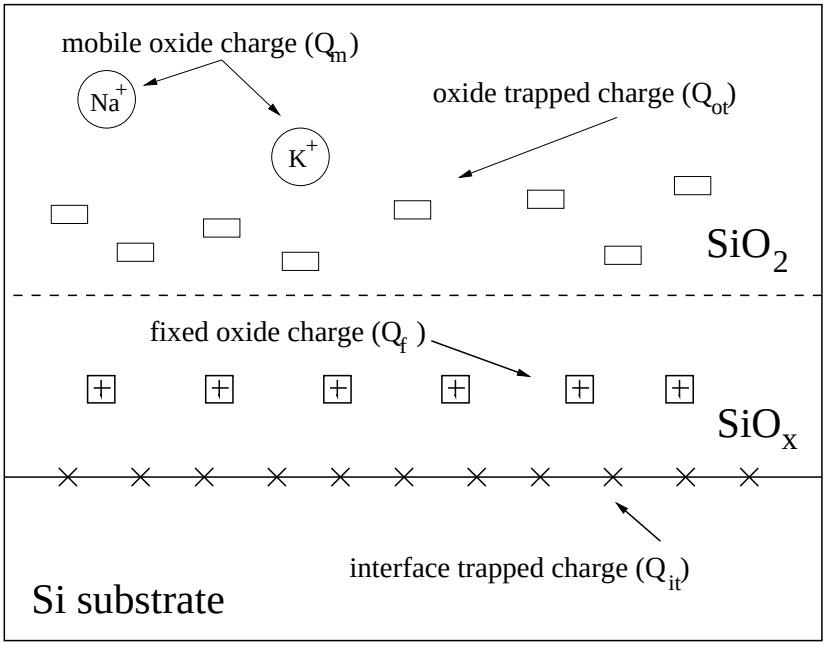


Figure 5.1: Different types of charges present at the Si-SiO_2 interface and in the bulk of the oxide.

In the previous chapter RTS noise was defined as the switching of the current between a high and a low level. Its origin is due to such defects or traps located near the Si-SiO_2 interface or in the bulk of the oxide. In particular, a single RTS is caused by an individual trap. The trapping/detrapping process affects the conductivity of the channel leading to the characteristic switching between a high and a low level in the drain current. More details on the experiments needed to distinguish between acceptor and donor traps are given is section 5.2.2.

5.2 Modeling of RTS

The influence of a trap on the noise is mainly determined by its occupation probability and by the influence of the occupation state of the trap on the drain current. Trapping and detrapping processes are usually modeled by the Shockley-Read-Hall (SRH) theory [63, 64]. SRH theory was originally developed for traps located in the bulk of silicon or at the Si-SiO_2 interface. Therefore, it has to be modified in order to account for tunneling into/from traps located in the oxide.

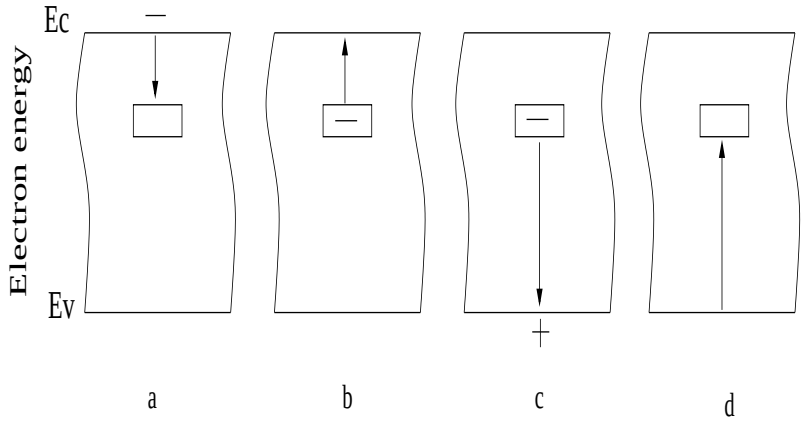


Figure 5.2: The basic processes involved in recombination by trapping: a) electron capture, b) electron emission, c) hole capture, d) hole emission.

5.2.1 SRH theory

In this section the standard SRH theory is presented. We describe the behavior for a nMOS device, operating in inversion condition, in which the charge exchange happens mainly between the conduction band and the trap. Some assumptions must be made:

- A trap can capture only one charge carrier and therefore can change its charge by the unit charge q. An acceptor trap can assume charge states 0 and $-q$ while a donor trap 0 and $+q$.
- No exchange of charges between different traps occurs.
- Trapping and detrapping processes are instantaneous.
- The energy of a trap E_T is independent of its occupancy.

Trapping and detrapping processes between interface traps and the conduction and valence band are shown in Fig. 5.2. A trap in the neutral state can capture an electron from the conduction band (a) or capture an electron from the valence band (d) leaving therefore an hole in the valence band. Process (b) represents the emission of an electron and (c) the capture of an hole.

The capture rate of an electron from the conduction band is given by:

$$c_n = n v_{th} \sigma (1 - f_t) \tag{5.1}$$

where n is the electron concentration, v_{th} is the electron thermal velocity, σ is the capture cross-section and $1 - f_t$ is the probability that the trap is empty and so in the condition to capture an electron.

The emission rate of an electron to the conduction band is given by:

$$e_n = n_1 v_{th} \sigma f_t \tag{5.2}$$

where f_t is the probability that the trap is occupied and n_1 is the electron concentration in the conduction band when the Fermi level falls at E_T (trap energy) and is expressed as:

$$n_1 = N_C \text{exp}\left(\frac{E_T - E_{CS}}{kT}\right) \tag{5.3}$$

The electron concentration is given by Eq. 2.1 and it is here reported:

$$n = N_C \text{exp}\left(\frac{E_F - E_{CS}}{kT}\right) \tag{5.4}$$

At equilibrium the trapping/detrapping process follows the Fermi-Dirac statistic [63], hence the probability occupation of a trap is:

$$f_t = 1/[1 + \text{exp}(E_T - E_F)/kT] \tag{5.5}$$

In this analysis the trap and the electrons in the conduction band are supposed to be in thermal equilibrium so, they have the same Fermi level.

The capture and emission time constants are given by:

$$\tau_c = \frac{1}{n \sigma v_{th}} \tag{5.6}$$

and

$$\tau_e = \frac{1}{n_1 \sigma v_{th}} = \frac{\text{exp}[(E_F - E_T)/kT]}{n \sigma v_{th}} \tag{5.7}$$

The capture and emission rates can be written as:

$$c_n = \frac{1 - f_t}{\tau_c}; \qquad e_n = \frac{f_t}{\tau_e} \tag{5.8}$$

Under constant bias conditions the detail balance principle requires the capture rate to be equal to the emission rate. From Eqs. 5.6 and 5.7 we get:

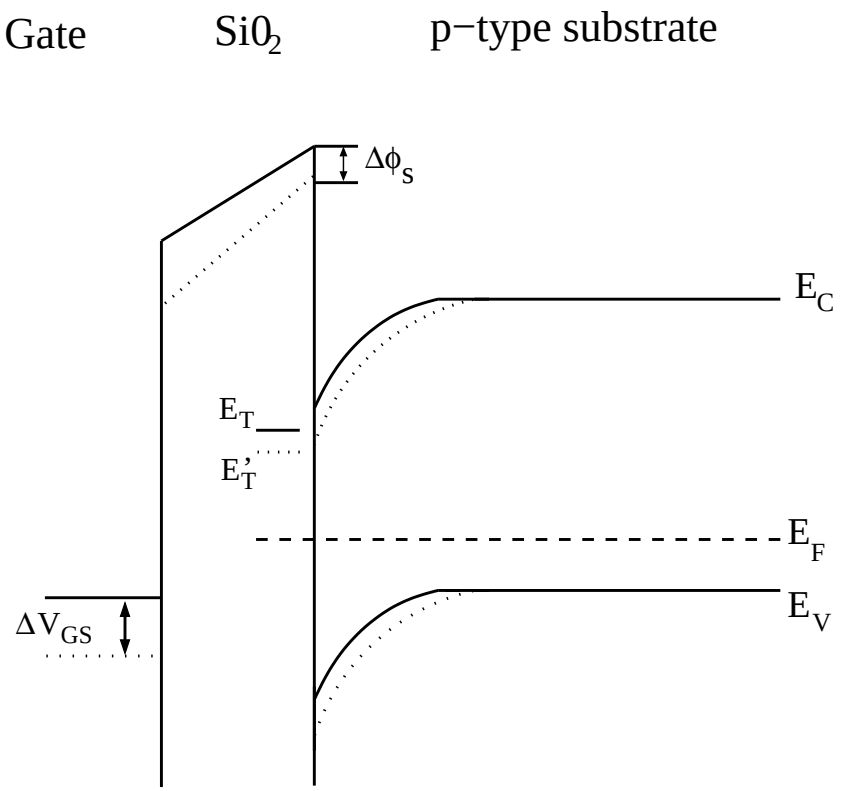


Figure 5.3: Band bending of a nMOSFET. An increase of the gate voltage ΔV_{GS} correspond to a change in the band bending (dotted lines). $\Delta\phi_s$ is the change in the surface potential. E_T and $E_T^{'}$ denote the trap energy before and after changing the gate voltage.

$$\frac{\tau_c}{\tau_e} = \exp\left(\frac{E_T - E_F}{kT}\right) \tag{5.9}$$

Eq. 5.9 gives us an important result: emission and capture time constants assume the same value when the trap energy E_T is equal to the Fermi level E_F.

5.2.2 V_{GS} dependence of τ_c

If we consider an increase of the V_{GS}, the band bending (Fig. 5.3) and the electron concentration n (Eq. 5.4) will increase. Analyzing now the expression for the capture time constant (Eq. 5.6), we can notice that τ_c will decrease. This dependence allows to distinguish from experimental data if the trap producing an RTS signal is an acceptor or a donor one [65]. An acceptor trap is negatively

charged when occupied by an electron and neutral when empty. A donor trap, on the other hand, is neutral when filled by an electron and positively charged when empty [66, 67]. As we have seen in Chapter 4 an RTS signal switches between a high and a low state corresponding in MOSFETs to a high and a low drain current level. For both acceptor and donor traps the high level corresponds to a neutral trap due to a lower threshold voltage. Therefore, for an acceptor trap, the time spent by the current in the high level corresponds to the time needed by the trap to capture an electron. If the mean time spent by the current in the high state decreases with increasing V_{GS} it corresponds to τ_c, on the other hand, the mean time spent in the low state corresponds to τ_e. In our experiments, only acceptor traps have been found. Normally donors traps are observed only at low-temperatures below 70K [66].

5.2.3 V_{GS} dependence of τ_e

The emission time constant τ_e depends on the trap energy E_T. According to Eq. 5.7, τ_e seems to be independent of the applied gate voltage because E_T is independent of V_{GS}. That holds only for traps located exactly at the Si-SiO_2 interface. The energy of a trap inside the oxide depends on the oxide electric field and is given by [68, 69]:

$$E_T = E_{T0} - q\phi_s - q\frac{x_t}{t_{ox}}(V_{GS} - V_{FB} - \phi_s - \phi_p) \tag{5.10}$$

where x_t is the trap position inside the oxide, E_{T0} is the trap energy at flatband condition, q is the electronic charge, ϕ_s is the surface potential, and ϕ_p is the voltage drop across the gate electrode accounting for poly-depletion. The reference energy level is the intrinsic Fermi level in the bulk silicon.

From Eq. 5.10 it is clear that for a trap located at the interface (x_t=0 nm), E_T does not depend on the applied gate voltage. On the other hand, a trap located inside the oxide shows a decrease of the energy with V_{GS}, hence, from Eq. 5.7, an increase of τ_e.

5.2.4 Trap position inside the oxide

Eq. 5.9 can be rewritten following the notation in Fig. 5.4 as:

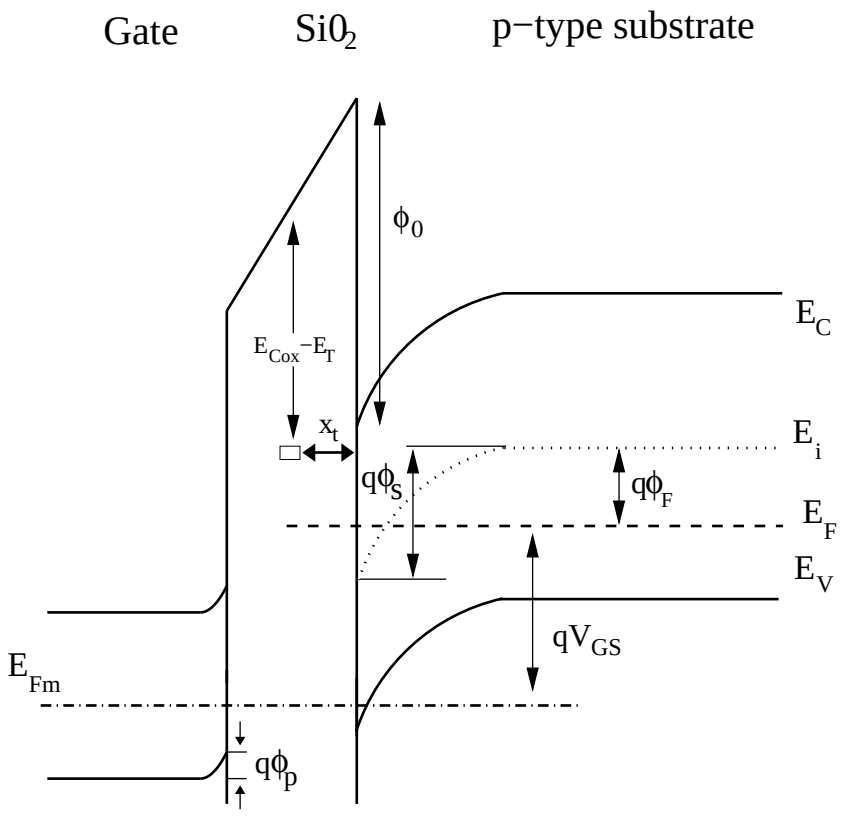


Figure 5.4: The energy band diagram in the channel at the trap position.

$$ln\frac{\tau_c}{\tau_e} = -\frac{1}{kT}\Big[(E_{Cox}-E_T)-(E_C-E_F)-\phi_0 + q\phi_s + q\frac{x_t}{t_{ox}}(V_{GS}-V_{FB}-\phi_s-\phi_p)\Big] \tag{5.11}$$

where E_{Cox} is the bottom of the conduction band of the oxide, E_C is the bottom of the conduction band in the bulk of the silicon, ϕ_0 is the difference between the electron affinity of the Si and the SiO_2, ϕ_s is the surface potential, ϕ_p is the voltage drop across the gate electrode, x_t is the trap position inside the oxide, and t_{ox} is the oxide thickness.

According to [70], the trap position inside the oxide x_t is then calculated based on the gate voltage dependence of the τ_c/τ_e ratio by using Eq. 5.11:

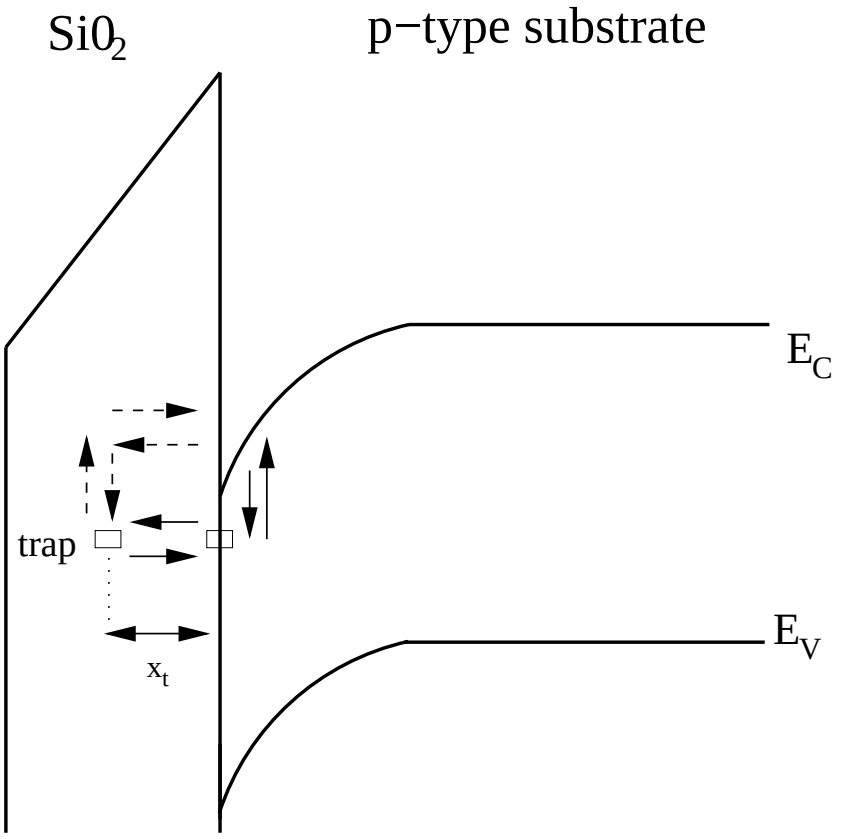


Figure 5.5: ”Tunneling and Capture” (dotted arrows) and ”Capture and Tunneling” (solid arrows) mechanisms for the capture and emission processes for a trap locate at a distance x_t inside the oxide. The arrows indicate electron transitions.

$$\frac{dln\left(\frac{\tau_c}{\tau_e}\right)}{dV_{GS}} = -\frac{q}{kT}\left[\frac{d\phi_s}{dV_{GS}} + \frac{x_t}{t_{ox}}\left(1 - \frac{d\phi_p}{dV_{GS}} - \frac{d\phi_s}{dV_{GS}}\right)\right] \tag{5.12}$$

The extraction procedure requires the evaluation of the slope of the line that provides a linear fitting of the gate bias dependence of $ln(\tau_c/\tau_e)$. The slope corresponds to the left-hand side of Eq. 5.12. It is indeed necessary to know the oxide thickness t_{ox} and the dependence on V_{GS} of the surface potential ϕ_s and of the voltage drop across the gate electrode ϕ_p.

5.2.5 Tunneling mechanisms

To explain the capture and emission processes of electrons in traps located inside the oxide, two different models have been proposed. According to the ”Tunneling and Capture” model [71], electrons from the conduction band first tunnel into the oxide at the distance of the traps, and then are captured by traps (dotted arrows in Fig. 5.5). The validity of this model has been later questioned, since measurement data did not support energy dissipation in the oxide [72]. The ”Capture and Tunneling” model [34] states that electrons first get trapped by fast defects centers at the interface, and then tunnel into the traps inside the oxide (solid arrows in Fig. 5.5). In this latter model electrons do not dissipate energy in the oxide. A continuous trap energy distribution over the bandgap at the interface is required for this process; the presence of such a distribution is generally accepted for the Si-SiO_2 interface. It is important to notice that for a trap featuring an energy level higher than the conduction band energy at the interface, the ”Capture and Tunneling” model has no anymore meaning and direct tunneling of electrons in traps should be effective.

5.2.6 Capture cross-section

The capture cross-section (σ) of an electron trap is an effective area within which an electron is captured by the trap. The larger the cross-section is, the higher is the probability for an electron to be captured and thus the smaller is τ_c (Eq. 5.6).

As we have seen in the previous section, in order to be captured by a trap located in the oxide an electron needs to tunnel to it. Tunneling is a quantum mechanical process and to analyze such a process for the electron/trap system, the knowledge of the structure of the trap would be necessary at the atom level. Unluckily this information is unavailable.

What normally can be done is to model the capture cross-section including in its equation simply the tunneling probability of an electron through the potential barrier given by the difference between the oxide barrier height and the energy of the electrons that tunnel into the trap. The tunneling depends also on the distance that an electron must tunnel to be captured in a trap. The tunneling probability reduces exponentially with the distance. The capture cross-section is then given by [73]:

$$\sigma(x_t) = \sigma_0 \text{exp}(-x_t/\lambda_t) \tag{5.13}$$

where σ_0 is the capture cross-section prefactor, x_t is the trap distance into the oxide, and λ_t is the attenuation wave function coefficient.

5.3 Comparison of RTS models with experimental data

In the first part of this section we report the results of measurements and simulation of emission (τ_e) and capture (τ_c) time constants as a function of gate voltage for eight individual traps [74] in nMOS transistors. In the second part, results are reported for pMOS devices.

5.3.1 Experimental details

RTS noise has been measured in nMOSFETs manufactured in a 0.13 μm technology [26] with nitrided gate oxide and physical oxide thickness t_{ox}=2.2 nm. Small-area devices with physical poly gate width W and gate length L product WxL= 0.16x0.1 μm^2, 0.4x0.1 μm^2, 0.75x0.1 μm^2 have been investigated in order to detect the effect of single traps. Drain current fluctuations have been measured and recorded using a low noise amplifier and a digital oscilloscope. The experiments have been carried out in the linear mode of operation (V_{DS}=50 mV). For each device, the gate bias is varied in order to detect the signature of a single trap, i.e. a clear RTS switch superimposed to the DC drain current. Once the trap was found, the gate voltage was swept over a 200 mV range with 50 mV steps. For each gate voltage a long time frame of the drain current (up to 2 minutes) is recorded by the digital oscilloscope. For accurately extracting the emission and capture time constants, the time domain waveform contains at least 200 transitions between the high and the low state. Indeed, in order to not miss any transition, the sampling frequency of the oscilloscope is set at least 100 times higher than the RTS corner frequency.

Each recorded waveform of drain current has been post-processed in order to estimate τ_e and τ_c. This is done by means of a simple software routine that filters the high-frequency noise and discriminates between the high and the low state by a level-crossing algorithm.

All the measured traps are acceptor traps so the high current level corresponds to the capture time and the low current level to the emission time.

5.3.2 Modeling approaches

To model the gate bias dependence of τ_c and τ_e we used the SRH model (Eqs. 5.6, 5.7) and a modified version proposed by Schulz in [75] by introducing an additional Coulomb energy accounting for the Coulomb blockade effect. For an acceptor-type trap the expression of τ_c is modified including the Coulomb energy ΔE, while τ_e remains the same:

$$\tau_c = \frac{\exp(\Delta E/kT)}{n\sigma(x_t)v_{th}}; \quad \tau_e = \frac{\exp[(E_F - E_T)/kT]}{n\sigma(x_t)v_{th}} \tag{5.14}$$

When a trap captures an electron, electrostatic charges in the substrate, channel and gate are modified. This charge variation expends the energy called Coulomb energy ΔE, which must be provided and which reduces the capture probability according to Eq. 5.14.

Quantization effects

The equations 5.6, 5.7, 5.14 for τ_c and τ_e are valid for a 3D electron gas. As we have seen in Chapter 2, in a MOSFET biased in inversion condition, the profile of the conduction band in the vicinity of the $Si-SiO_2$ interface forms a triangular potential well that induces substantial quantization effects. Due to the confinement introduced by this potential well, the energy component associated to the motion in the direction normal to the silicon-dielectric interface is quantized, leading to the formation of subbands. Therefore, a description in terms of a 2D electron gas is more appropriate.

Following [76, 77], quantization effects in the equation of τ_c and τ_e are taken into account by means of a first order approximation (see Chapter 2) where only the first subband is modeled. The equivalent volume concentration is obtained by Eqs. 2.4 and 2.6 as:

$$n = n_{2D} \int_0^{\overline{z}} \frac{p(z)}{\overline{z}} dz \tag{5.15}$$

where n_{2D} is the electron concentration of the 2D electron gas forming the inversion layer, $p(z)$ is the probability function of finding electrons at depth z and $\overline{z}$ is the distance of the inversion charge centroid from the $Si-SiO_2$ interface.

The capture and emission time constants (Eqs. 5.6 and 5.7) are now given by:

$$\tau_c = \frac{1}{n_{2D} \int_0^{\overline{z}} \frac{p(z)}{\overline{z}} dz\sigma(x_t)v_{th}}; \quad \tau_e = \frac{\exp[(E_F - E_T)/kT]}{n_{2D} \int_0^{\overline{z}} \frac{p(z)}{\overline{z}} dz\sigma(x_t)v_{th}} \tag{5.16}$$

Tunneling mechanism and trap position

In order to model the tunneling we used the "Tunneling and Capture" model earlier discussed supposing that electrons tunnel from the energy of the first subband E_0. For all the traps analyzed in this work, the energy level of the first subband E_0 is always close to the energy level of the trap E_T, therefore this approach seems reasonable. The capture cross-section is modeled as function of the distance of the trap inside the oxide given by Eq. 5.13 and the parameter λ_t is evaluated by the WKB method taking into account the bias dependence of the energy barrier [78]. The capture cross-section prefactor σ_0 is a model parameter and for some traps has been used as a fitting parameter in order to fit experimental data.

The trap position inside the oxide has been calculated using Eq. 5.12.

MOSFET electrostatic

In order to calculate the volume concentration of channel electrons n, the surface potential ϕ_s and the voltage drop across the gate electrode ϕ_p , we used two different approaches.

The first approach (SCHR) consists in the numerical solution of the Poisson and Schrödinger equations in a 1-D MOS structure using the SCHRED 2.0 solver [79]. The simulation are performed directly on the website *www.nanohub.org*.

In the second one (SRG) we used a modified version of the model proposed by Siergiej in [76]. In the frame of the SRG approach, the effect of polysilicon depletion is taken into account by an analytical approximation, leading to the following non-linear system of coupled equations:

$$\phi_s = V_{GS} - V_{FB} - \frac{t_{ox}}{\varepsilon_{ox}}(Q_B + Q_{inv}) - \phi_p \tag{5.17}$$

$$Q_{inv} = \frac{2kTm_tq}{\pi\hbar^2}\exp\left[-\left(\frac{E_g}{2} + q\phi_F - q\phi_s + \Delta E_0\right)/kT\right] \tag{5.18}$$

$$Q_B = \sqrt{(2\varepsilon_s qN_A\phi_s)} \tag{5.19}$$

$$\phi_p = \frac{(Q_B + Q_{inv})^2}{2q\varepsilon_s N_P} \tag{5.20}$$

where ΔE_0 (Eq. 2.5) is the energy distance between E_0 (energy level of the first subband) and the conduction band energy at the $Si-SiO_2$ interface (E_{CS}), m_t

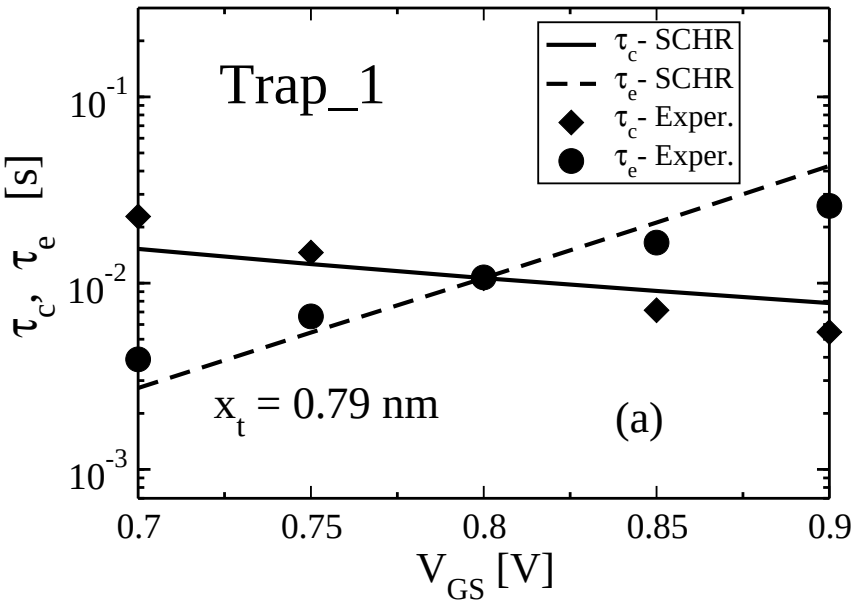


Figure 5.6: Experimental and simulated τ_c and τ_e as a function of V_{GS} (SCHR approach). Estimated x_t=0.79 nm.

and m_l are the transverse and longitudinal effective mass of electrons, respectively, Q_B is the MOSFET bulk charge, Q_{inv} is the inversion charge, E_g is the forbidden band gap, ϕ_F=$(kT/q)ln(N_A/n_i)$, n_i is the intrinsic electron concentration. The flatband volgate V_{FB}, the substrate doping concentration N_A and the polysilicon doping concentration N_P are treated as known technological parameters. The system of Eqs. 5.17-5.20 is solved through Newton-Raphson iterations.

5.3.3 Results

Modeling of τ_e and τ_c requires the preliminary extraction of values for the trap energy at flatband E_{T0} and cross-section prefactor σ_0. For all the considered traps, these parameters are set in order to fit experiments for V_{GS} corresponding to 50% trap occupation probability, thus (see Eq. 4.47) for the case in which τ_c=τ_e.

Figs. 5.6 and 5.7 report experimental and simulated τ_c and τ_e by the standard SRH model (5.16) using both the SCHR and SRG approaches for Trap_1. Experimental τ_c and τ_e are represented by symbols while simulated data by lines. The gate voltage is swept between 0.7 and 0.9 V with 50 mV steps, thus the device is in inversion condition. As reported before, the V_{DS} is always set to 50 mV assur-

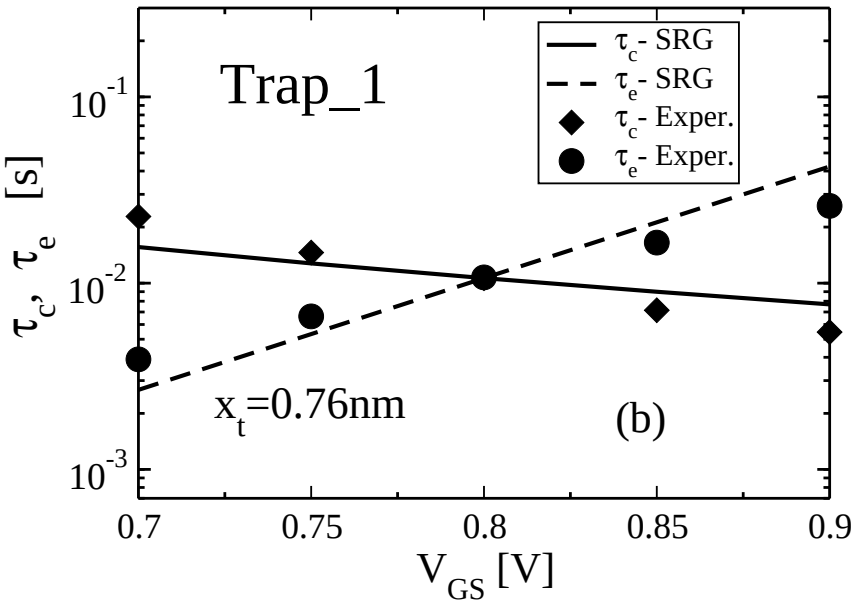


Figure 5.7: Experimental and simulated τ_c and τ_e as a function of V_{GS} (SRG approach). Estimated x_t=0.76 nm.

ing the linear operation mode. The capture time constant shows a decrease with the gate voltage due to an increase of the electron concentration n (Eq. 5.6). The two approaches (SCHR and SRG) provide almost the same results; the estimated trap position is x_t=0.79 nm and x_t=0.76 nm with the SCHR and SRG approach, respectively, and the simulated gate bias dependence of τ_c and τ_e are pretty similar. This is valid for all the traps we have analyzed in this work and therefore we will report results obtained by the simpler and more efficient SRG approach. In fact, while the electrostatic of the MOSFET in the SRG approach is calculating solving the system of Eqs. 5.17-5.20 that takes into account only the first subband, the SCHR approach require to solve numerically, by means of simulation by the SCHRED 2.0 simulator, the Poisson and Schrödinger equations.

Fig. 5.8 reports the gate voltage dependence of experimental and simulated emission and capture time constants for a trap (Trap_2) with x_t=1.12 nm. The gate voltage is swept between 0.65 and 0.85 V. Also in this case the standard SRH model is able to provide a reasonable description of experimental data. We obtained similar results also for two more traps (Trap_3 and Trap_4), not reported in figures, featuring different positions inside the oxide and energies. The relevant parameters of these traps are reported in Table 5.1. Also for Trap_3 and Trap_4 the emission and capture time constants are measured and simulated

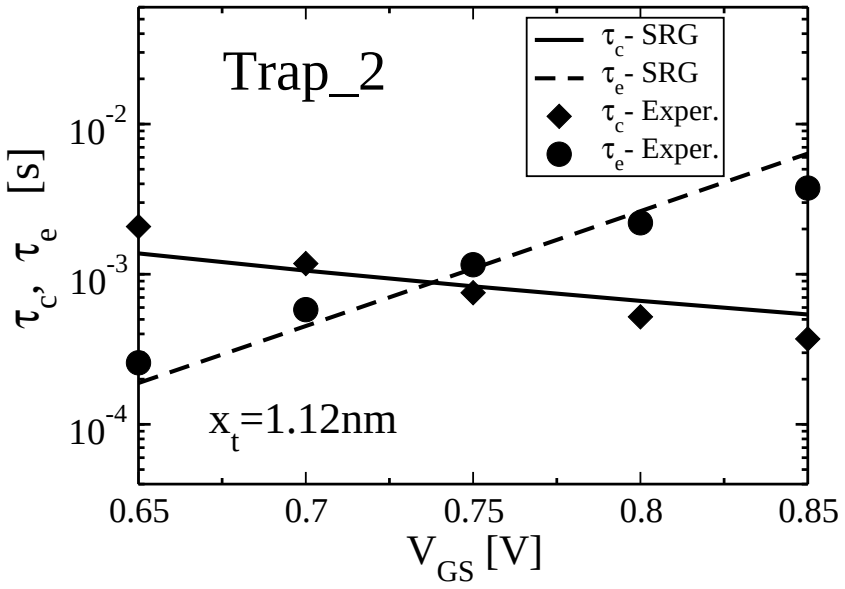


Figure 5.8: Experimental and simulated τ_c and τ_e as a function of V_{GS} (SRG approach). Estimated x_t=1.12 nm.

		x_t [nm]	$E_{T0} - E_{CS}$ [eV]	σ_0 [cm^2]
Trap_1	SCHR	0.79	0.30	5.9x10^{-21}
	SRG	0.76	0.31	5.5x10^{-21}
Trap_2	SRG	1.12	0.39	4.0x10^{-18}
Trap_3	SRG	0.61	0.25	1.4x10^{-20}
Trap_4	SRG	0.71	0.24	1.3x10^{-20}

Table 5.1: Extracted physical model parameters for 4 different traps in 4 different nMOS devices. For these traps the SRH model well reproduces the V_{GS} dependence of τ_e and τ_c. E_{T0} is the trap energy at flatband voltage and E_{CS} is the conduction band energy at the Si-SiO_2 interface.

for a gate voltage swept over a 200 mV range in inversion condition. Similar results were shown in [60] where the standard SRH model is reported to fit well the V_{GS} dependence of three traps.

Fig. 5.9 reports results for an additional trap (Trap_5) located at an estimated distance x_t=0.82 nm. The gate voltage is swept between 0.8 and 1 V. It can be noticed that for this specific trap the dependence of τ_c on V_{GS} is much larger compared to the cases shown in Figs. 5.7 and 5.8. As a consequence, the stan-

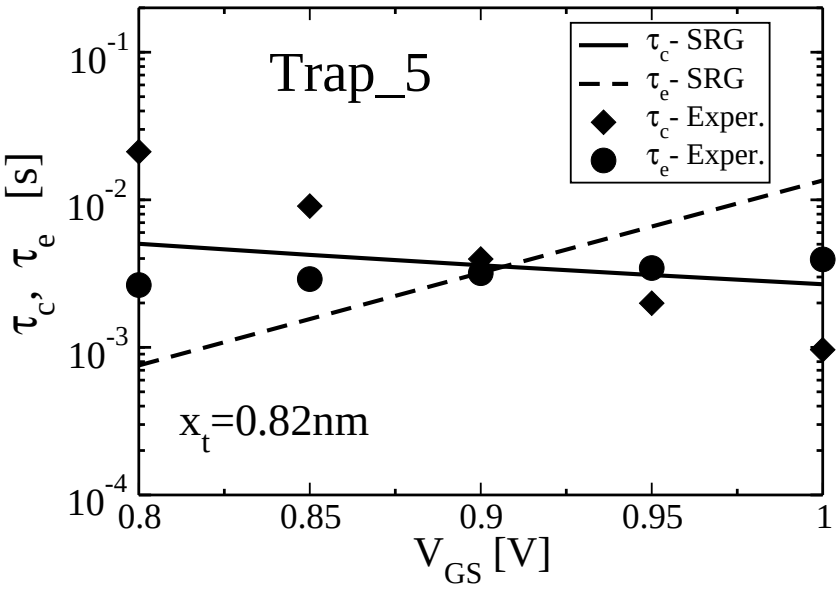


Figure 5.9: Experimental and simulated τ_c and τ_e as a function of V_{GS} (SRG approach). Estimated x_t=0.82 nm.

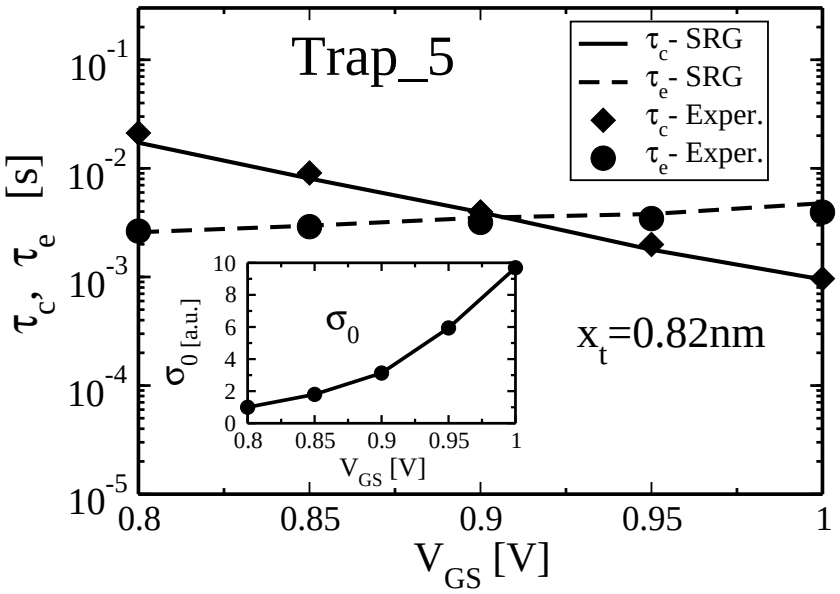


Figure 5.10: Experimental and simulated τ_c and τ_e as a function of V_{GS} (SRG approach). The model assumes an empirical adjustment of σ_0. Estimated x_t=0.82 nm. In the inset the normalized values of σ_0 are reported as a function of V_{GS}.

		x_t [nm]	$E_{T0} - E_{CS}$ [eV]	σ_0 (τ_c=τ_e) [cm^2]
Trap_5	SRG	0.82	0.36	2.2x10^{-20}
Trap_6	SRG	1.13	0.43	7.4x10^{-18}
Trap_7	SRG	0.92	0.34	5.2x10^{-20}
Trap_8	SRG	0.98	0.31	1.1x10^{-18}

Table 5.2: Extracted physical model parameters for 4 different traps in 4 different nMOS devices. Due to the large V_{GS} dependence of τ_c, an empirical adjustment of σ_0 is necessary. E_{T0} is the trap energy at flatband voltage and E_{CS} is the conduction band energy at the Si-SiO$_2$ interface.

dard SRH model provides a much lower gate bias dependence of τ_c compared to experiments. Also the simulated emission time constant does not provide a good fitting of the experimental τ_e. Similar results were obtained in [77, 80] where, in order to fit the experiments, an empirical V_{GS} dependence of the capture cross-section [77] or a modification of the trap energy due to the Coulomb blockade effect [80] were introduced.

In order to recover a better agreement between the experimental and the simulated data of Trap_5, we tried the approach discussed in [77, 81] empirically varying the capture cross-section prefactor σ_0. Results for Trap_5 are shown in Fig. 5.10 where both experimental emission and capture time constants are well reproduced by the model. σ_0 must be increased with V_{GS} and this behavior is also reported in [81]. The normalized values of the capture cross-section prefactor are reported in the inset of Fig. 5.10. In this particular case the capture cross-section prefactor must be increased about of a factor of 10 for the explored gate voltage.

Similar results are shown in Fig. 5.11 for another trap (Trap_6) featuring a distance inside the oxide x_t=1.13 nm. Also for this trap an empirical variation of σ_0 with the gate voltage is necessary in order to reproduce the strong dependence of the capture time constant on V_{GS}.

We have measured four different traps for which an empirical adjustment of the capture cross-section prefactor has been necessary to reproduce the gate bias dependence of emission and capture time constants. The relevant parameters of these traps are reported in Table 5.2. The value reported for the capture cross-section prefactor is the extracted one at the V_{GS} that gives τ_c=τ_e.

Trying to recover a good fitting with experiments for Trap_6, we tried also

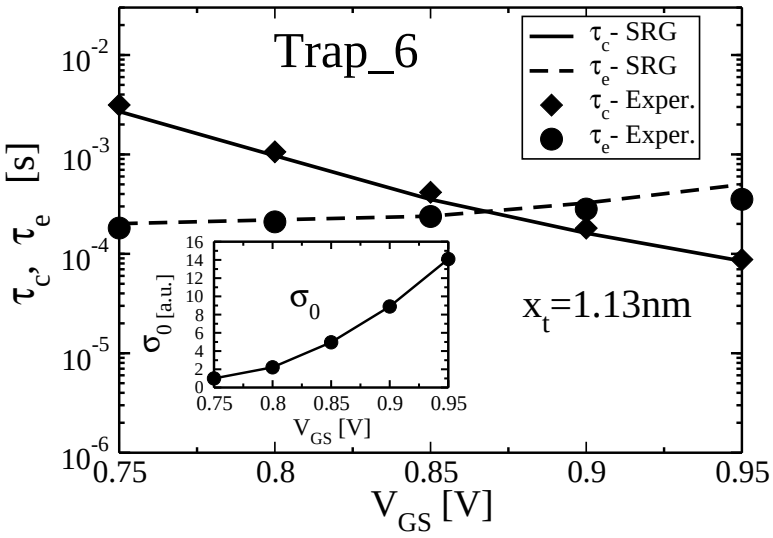


Figure 5.11: Experimental and simulated τ_c and τ_e as a function of V_{GS} (SRG approach). The model assumes an empirical adjustment of σ_0. Estimated x_t=1.13 nm. In the inset the normalized values of σ_0 are reported as a function of V_{GS}.

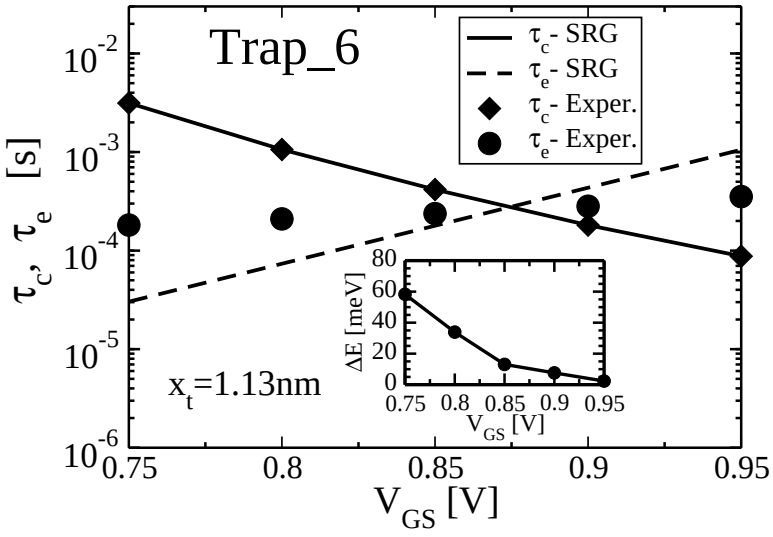


Figure 5.12: Experimental and simulated τ_c and τ_e as a function of V_{GS} (SRG approach). The model accounts for the Coulomb blockade effect. Estimated x_t=1.13 nm. In the inset the values of the Coulomb blockade ΔE are reported as a function of V_{GS}.

the approach proposed in [80] by accounting for the Coulomb blockade effect. Capture and emission time constants are modeled as reported in Eq. 5.14 taking into account quantization effects. The trap energy at flatband voltage E_{T0} and the cross-section prefactor σ_0 are set to fit experiments for the V_{GS} corresponding to τ_c=τ_e. σ_0 is kept constant for each gate voltage. The Coulomb energy ΔE is treated as a fitting parameter in order to reproduce the gate voltage dependence of τ_c. Results of this approach are reported in Fig. 5.12. While the experimental τ_c is perfectly reproduced, the model predicts an excessive dependence of τ_e on V_{GS}. The values of the Coulomb energy are reported in the inset of Fig. 5.12 showing a variation between 60 and 0 mV; these values are comparable to the ones reported in [80].

5.3.4 Discussion

From results previously reported it is interesting to notice that it is not possible to reproduce with a single model the gate bias dependence of emission and capture time constants. In particular, some traps show a quite strong dependence of the capture time constant as a function of the bias applied to the gate. For such traps, the standard SRH model is not able to reproduce experiments, but an empirical variation of the capture cross-section it is necessary to recover a good fitting of experimental τ_c and τ_e. The intersting fact is that we could not find any correlation between the standard characteristics of the traps like the energy and the position and the adequacy of the standard SRH model. In fact, analyzing for example Trap_2 and Trap_6, while they feature quite close values for estimated x_t, E_{T0} and σ_0, only Trap_6 requires a modification to the SRH model in order to cope with the large bias dependence of τ_c.

On the other hand, the modification of the SRH model by means of the Coulomb blockade effect can lead to a perfect agreement between experimental and simulated τ_c but gives an excessive dependence of τ_e on the applied gate voltage.

5.3.5 Extension for pMOSFETs

We have analyzed the gate voltage dependence of emission and capture time constants also for pMOS transistors. Small-area pMOSFETs fabricated with the same technology used for nMOSFETs [26] have been measured. Analyzed devices feature WxL= 0.4x0.1 μm^2 and 0.75x0.1 μm^2 and gate oxide thickness

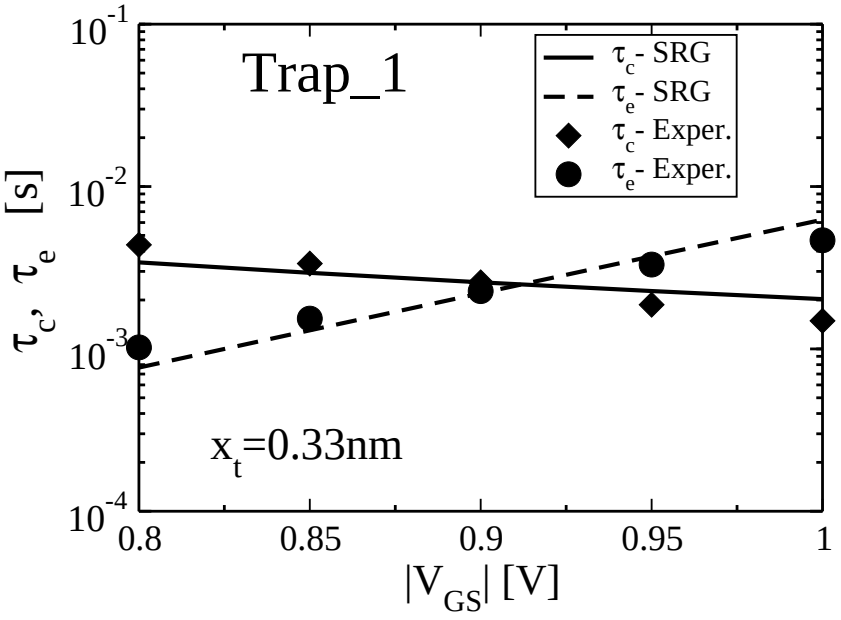


Figure 5.13: Experimental and simulated τ_c and τ_e for a pMOSFET as a function of $|V_{GS}|$ (SRG approach). Estimated x_t=0.32 nm..

t_{ox}=2.2 nm. The same extraction procedure for τ_c and τ_e described for nMOSFETs have been adopted. The drain-to-source voltage has been set to -50 mV in order to operate in linear regime. Once the RTS signal in the drain current due to a trap has been clearly identified, the gate voltage has been swept over a range of 200 mV with -50 mV steps. Modeling of the voltage dependence of emission and capture time constants have been performed with the standard SRH model eventually adopting an empirical variation of the capture cross-section prefactor. For pMOSFETs we used only the single subband approach (SRG) therefore solving the system of Eqs. 5.17-5.20 considering now the appropriate effective masses for both the transport and the tunneling for holes instead than for electrons [82].

Fig. 5.13 reports experimental (symbols) and simulated (lines) emission and capture time constants for a trap (Trap_1) in a pMOSFET as a function of the absolute value of V_{GS}. The estimated trap position is x_t=0.33 nm. It can be noticed that both τ_c and τ_e are well reproduced by the standard SRH model using the single subband approach (SRG). We obtained similar results for other two traps (Trap_2 and Trap_3) for which a good fitting of simulated emission and capture time constants with experiments is achieved. The relevant parameters of these traps are reported in Table 5.3.

		x_t [nm]	$E_{VS} - E_{T0}$ [eV]	σ_0 [cm^2]
Trap_1	SRG	0.33	0.20	1.0x10^{-22}
Trap_2	SRG	0.41	0.26	2.1x10^{-23}
Trap_3	SRG	0.85	0.31	1.2x10^{-19}

Table 5.3: Extracted physical model parameters for 3 different traps in 3 different pMOS devices. For these traps the SRH model well reproduces the V_{GS} dependence of τ_e and τ_c. E_{T0} is the trap energy at flatband voltage and E_{VS} is the valence band energy at the Si-SiO$_2$ interface.

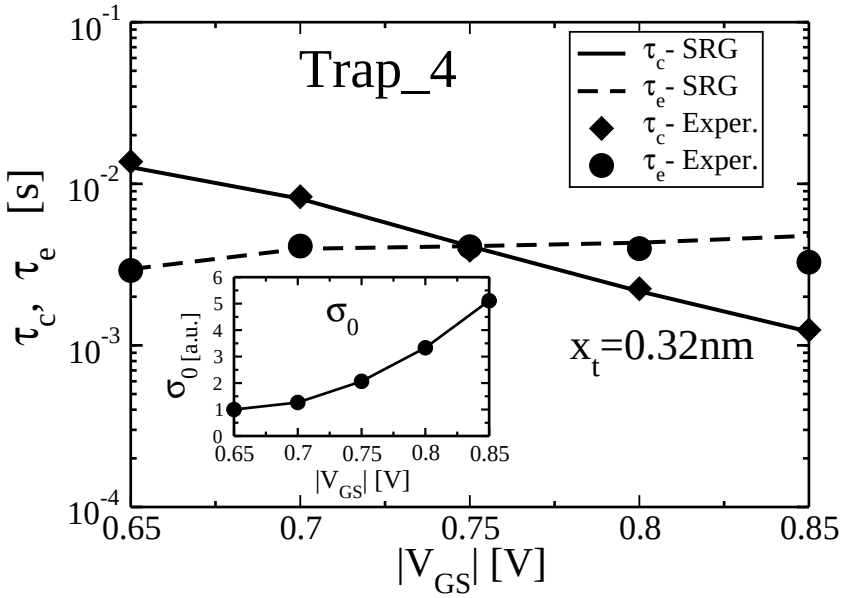


Figure 5.14: Experimental and simulated τ_c and τ_e for a pMOSFET as a function of $|V_{GS}|$ (SRG approach). The model assumes an empirical adjustment of σ_0. Estimated x_t=0.33 nm. In the inset the normalized values of σ_0 are reported as a function of $|V_{GS}|$.

As for nMOS devices, also for some traps in pMOSFETs it has not been possible to obtain an adequate V_{GS} dependence of emission and capture time constants adopting the standard SRH model. For such traps an empirical variation of the capture cross-section has been necessary to recover a good fitting of experimental τ_c and τ_e. An example is shown in Fig. 5.14 where experiments and simulations are reported for a trap (Trap_4) featuring a distance inside the oxide x_t=0.32 nm. The necessary variation of the σ_0 is reported in the inset of the fig-

		x_t [nm]	$E_{VS} - E_{T0}$ [eV]	σ_0 (τ_c=τ_e) [cm^2]
Trap_4	SRG	0.32	0.18	9.8x10^{-23}
Trap_5	SRG	0.54	0.23	1.4x10^{-21}
Trap_6	SRG	0.76	0.31	1.3x10^{-20}
Trap_7	SRG	0.49	0.24	8.1x10^{-21}
Trap_8	SRG	1.21	0.38	1.9x10^{-18}

Table 5.4: Extracted physical model parameters for 5 different traps in 5 different pMOS devices. Due to the large V_{GS} dependence of τ_c, an empirical adjustment of σ_0 is necessary. E_{T0} is the trap energy at flatband voltage and E_{VS} is the valence band energy at the Si-SiO_2 interface.

ure as a function of $|V_{GS}|$. For other four measured traps we needed to empirical vary the capture cross-section prefactor to reproduce the gate bias dependence of τ_c and τ_e (see Table 5.4).

Also for traps in pMOSFETs it has not been possible to correlate the adequacy of the standard SRH model with the trap position inside the oxide, the trap energy, and the capture cross-section. In particular, Trap_1 and Trap_4 show quite similar values for x_t, E_T, and σ_0, but while for Trap_1 the standard SRH model well reproduces the gate voltage dependence of emission and capture time constants, that's not true for Trap_4, for which an empirical variation of σ_0 is needed in order to obtain a good agreement with experiments.

Chapter 6

Measurement of flicker and RTS noise under switched bias conditions

Flicker noise, as reported in previous chapters, may be reduced in MOSFETs cycled between strong inversion and accumulation. The origin of flicker noise is attributed to the random trapping and detrapping of charge carriers into or from traps located inside the oxide responsible for the RTS noise. In this chapter a study of the flicker and RTS noise under constant bias and switched bias conditions is proposed. Measurements of flicker noise have been performed in the frequency domain for nMOS and pMOS transistors adopting different bias schemes, while RTS noise has been measured for small-area nMOSFETs both in the time and in the frequency domain. The chapter is organized as follows: in the first part we introduce the measurement setup used both to measure flicker and RTS noise. In the second part the flicker noise is analyzed comparing the noise under constant and switched bias conditions for different bias schemes. A comparison of the noise in transistors with two different oxide thicknesses is also reported. Finally, RTS noise is investigated both under constant and switched bias conditions in order to find a correlation with results obtained for flicker noise.

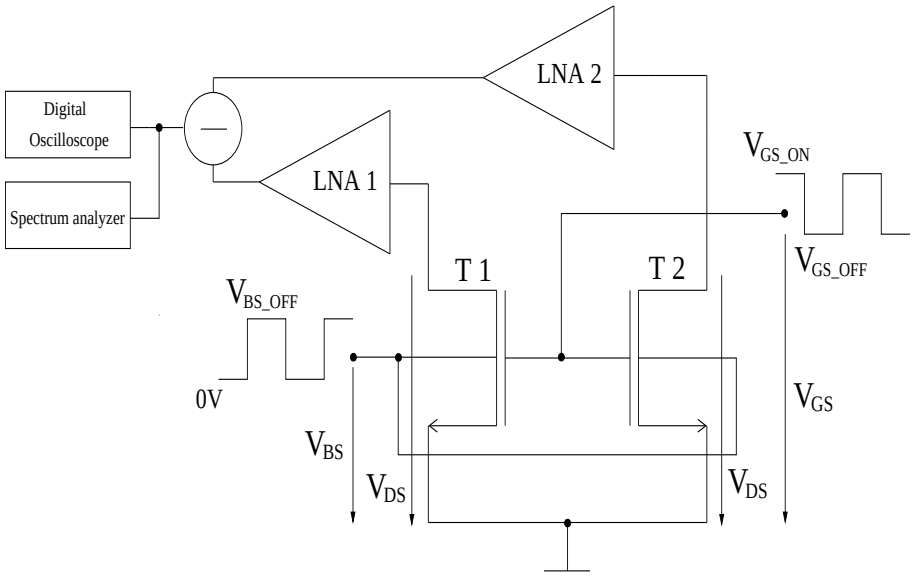


Figure 6.1: Schematic setup for measurement of flicker and RTS noise under constant and switched gate and substrate bias conditions.

6.1 Measurement setup

The measurement setup used to analyze flicker and RTS noise is reported in Fig. 6.1 [83]. The setup measures in a differential scheme the uncorrelated noise in a matched pairs of MOSFETs (T1 & T2). The two transistors have common gate, source and substrate connections. The uncorrelated drain current noise of T1 and T2 is amplified by two low noise amplifiers (LNA) and the out coming signals are subtracted. This arrangement cancels out the large signal perturbation due to the switching gate and substrate signals and adds the noise powers of the two transistors. Gate and bulk terminals of the test structure are terminated by 50 Ω resistors (not shown in Fig. 6.1). The gate and the substrate voltages of the MOSFETs are controlled by a pulse generator which provides for a constant bias (CB) or a periodic switched bias (SB). The biasing of the drain terminals is provided by the two low noise amplifiers. The spectum analyzer measures the drain current noise PSD of the two transistors. Time domain RTS measurements are performed with a digital oscilloscope. Calibration of the setup as well as a measurement of the noise floor by measuring the noise-power when the MOSFETs are 'OFF' and the probes and the amplifiers are connected to the spectrum analyzer have been done.

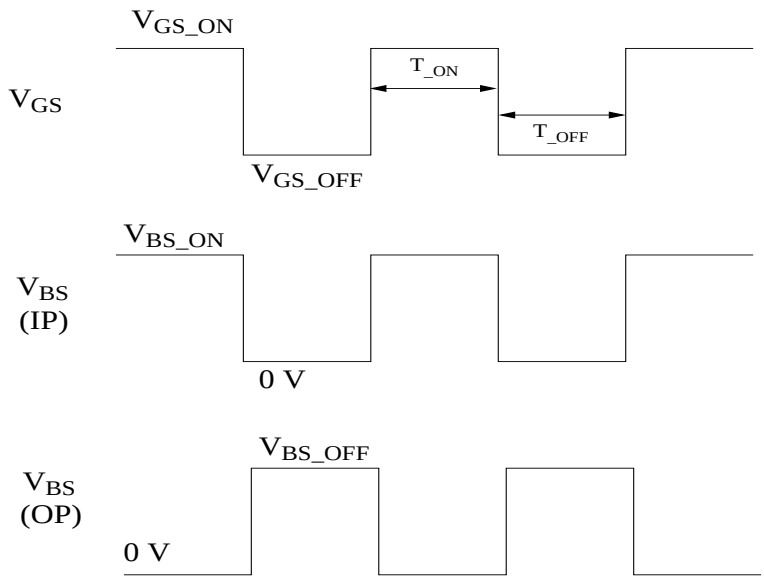


Figure 6.2: Timing scheme for 1/f noise measurement with in-phase (IP) and $180°$ out-of-phase (OP) switched substrate bias (V_{BS}) with respect to the gate voltage (V_{GS}) timing.

6.2 Flicker noise measurements

In this part we report results of measurements of flicker noise under constant and switched bias conditions.

6.2.1 Measurement condition

In this analysis we measured both nMOS and pMOS devices fabricated in a 0.13 μm technology [26] with nitrided gate oxide with thickness t_{ox}=2.2 nm. nMOSFETs have a gate length L=0.3 μm and a gate width W=6 μm. pMOSFETs have L=0.3 μm and W=12 μm. The threshold voltage is V_{TH}=0.26 V and V_{TH}=-0.3 V for n and pMOS devices, respectively. Measurements under CB conditions are performed biasing the devices with V_{GS}=V_{DS}=1 V and V_{GS}=V_{DS}=-1 V for n and pMOSFETs, respectively. The application of a forward and reverse substrate bias has been investigated. Characterization under SB conditions is performed by applying to the gate terminal a square wave with 50% duty cycle switching between an ON- and an OFF-state (V_{GS_ON} and V_{GS_OFF}) and a switching frequency f_{sw}=2.5 MHz with rising and falling times t_r=t_f=8 ns. Under SB conditions different substrate biasing schemes have been

analyzed (Fig. 6.2): a) substrate bias with zero voltage (ZSB), b) constant substrate bias with forward or reverse bias (FSB, RSB), c) forward substrate bias pulsing in-phase with respect to the gate pulsing (IP), and d) forward substrate bias pulsing 180° out-of-phase with respect to the gate switching bias (OP). In the case b), while to the gate is applied a pulse switching between V_{GS_ON} and V_{GS_OFF} with f_{sw}=2.5 MHz, the applied forward or reverse substrate bias is kept constant. In the case c) and d) the substrate bias is not anymore kept constant while the gate bias switches between the ON- and the OFF-state, but V_{BS} is also switched. In c) the V_{BS} is switched to 0 V when the gate pulse is set to V_{GS_OFF} (transistor in the OFF-state) and to a forward V_{BS_ON} when the gate pulse is set to V_{GS_ON} (transistor in the ON-state). Hence, the switching frequency of the pulse applied to the substrate is also f_{sw}=2.5 MHz and has the same rising and falling times as for the pulse applied to the gate. In d), on the other hand, the V_{BS} is switched to a forward substrate bias V_{BS_OFF} when the gate pulse is set to V_{GS_OFF} and to 0 V when the gate pulse is set to V_{GS_ON}.

The effect of V_{GS_OFF} on the noise keeping the substrate bias to zero volt is also analyzed.

The reported results, unless differently stated, are obtained by averaging measurements performed on at least 20 nominally identical devices.

6.2.2 Measurement results

Effect of substrate bias

Figs. 6.3 and 6.4 report the normalized noise power spectral density of drain current (S_{id}/I_d) as a function of frequency for constant (CB) and switched (SB) gate bias conditions with ZSB and FSB for nMOSFETs and pMOSFETs, respectively. I_d represents the drain current in the ON-state. Under SB conditions the gate-to-source voltage in the ON-state has been set to the same value used under CB conditions (nMOS: V_{GS_ON}=1 V, pMOS: V_{GS_ON}=-1 V), while in the OFF-state is always set to zero (V_{GS_OFF}=0 V).

The FSB is set to V_{BS}=0.6 V and V_{BS}=-0.6 V for nMOS and pMOS, respectively. S_{id}/I_d under CB conditions is divided by a factor of 4 in order to be compared to the SB measurements accounting for the intrinsic 6 dB attenuation due to the ON-OFF modulation of the drain current with 50% duty cycle [57]. From Figs. 6.3 and 6.4 it can be noticed that, with zero substrate bias, SB slightly reduces the $1/f$ noise compared to CB. Application of a forward substrate bias

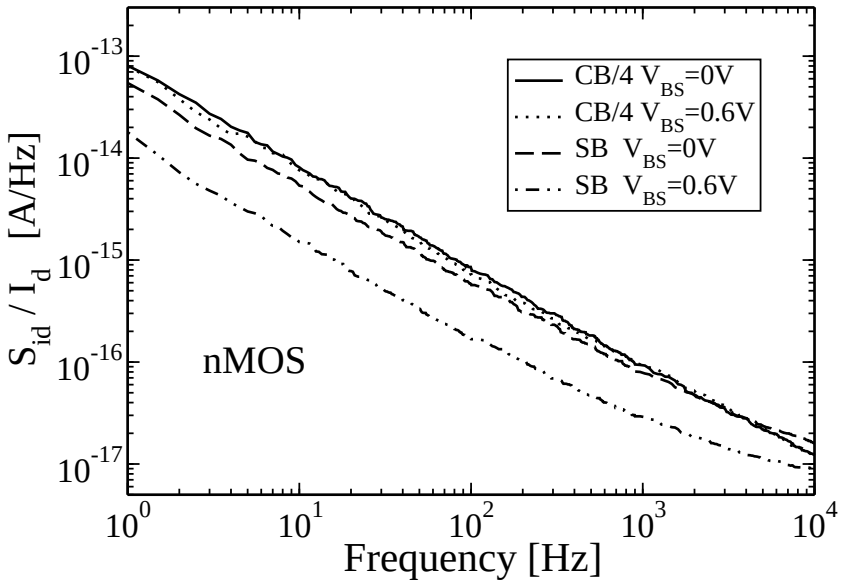


Figure 6.3: Normalized noise power density S_{id}/I_d for nMOSFET under CB and SB conditions (V_{GS_ON}=1 V, V_{GS_OFF}=0 V, V_{DS}=1 V) with ZSB (V_{BS}=0 V) and FSB (V_{BS}=0.6 V) vs. frequency.

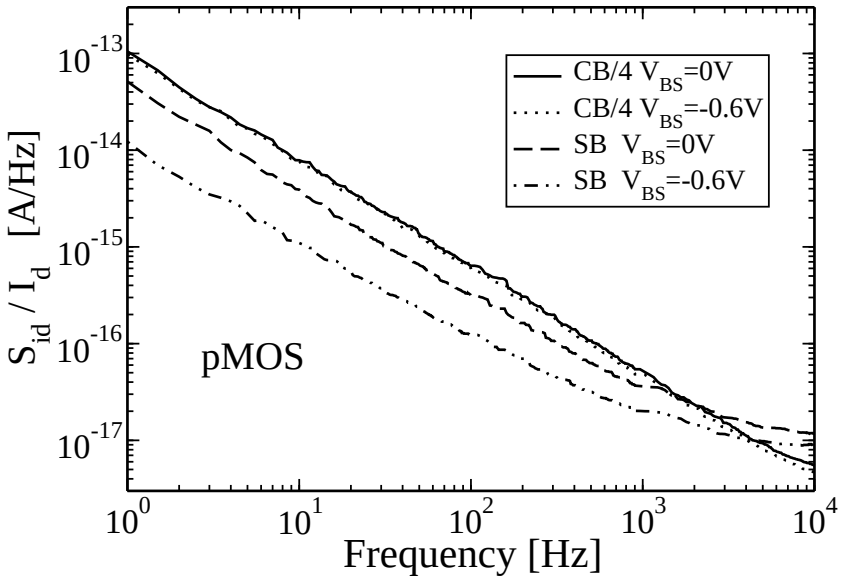


Figure 6.4: Normalized noise power density S_{id}/I_d for pMOSFET under CB and SB conditions (V_{GS_ON}=-1 V, V_{GS_OFF}=0 V, V_{DS}=-1 V) with ZSB (V_{BS}=0 V) and FSB (V_{BS}=-0.6 V) vs. frequency.

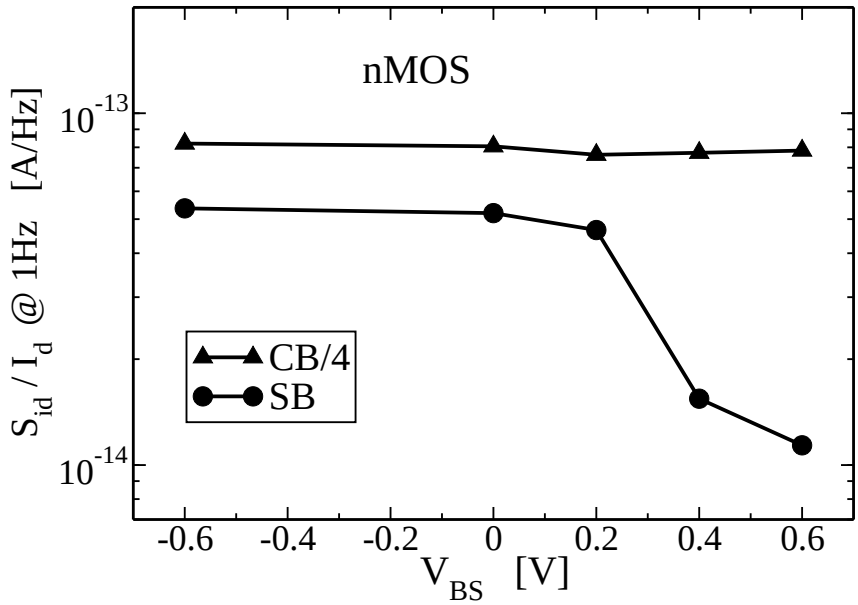


Figure 6.5: S_{id}/I_d @ 1 Hz under CB and SB conditions vs. substrate bias V_{BS} for nMOSFETs with V_{GS_ON}=1 V, V_{GS_OFF}=0 V, V_{DS}=1 V.

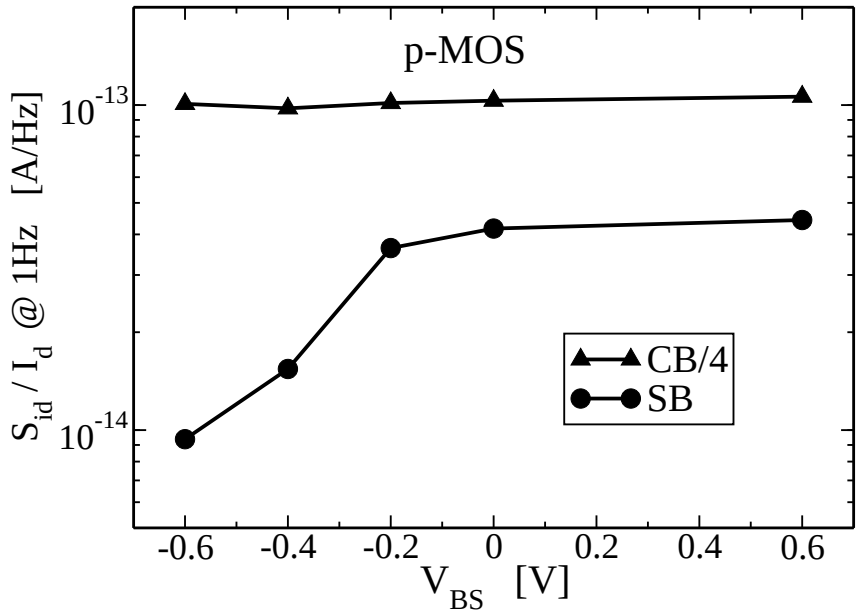


Figure 6.6: S_{id}/I_d @ 1 Hz under CB and SB conditions vs. substrate bias V_{BS} for pMOSFETs with V_{GS_ON}=-1 V, V_{GS_OFF}=0 V, V_{DS}=-1 V.

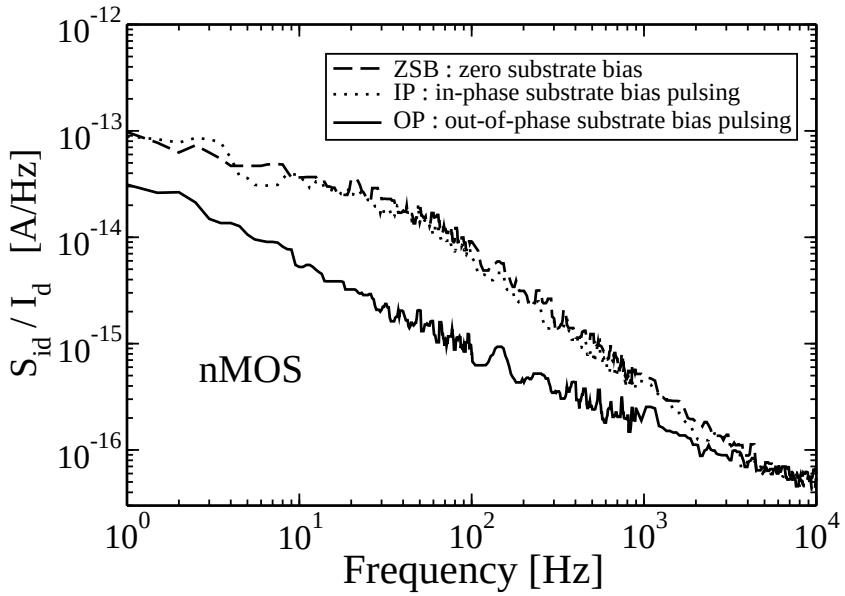


Figure 6.7: S_{id}/I_d vs. frequency for a single nMOS device under SB conditions (V_{GS_ON}=1 V, V_{GS_OFF}=0 V, V_{DS}=1 V) with: zero substrate bias, in-phase and $180°$ out-of-phase substrate bias switching with respect to the gate switching bias.

under SB provides a strong reduction of the noise, while a FSB applied under CB condition hardly modifies the flicker noise. These considerations hold for both nMOS and pMOS transistors.

Another way to visualize the flicker noise is to plot the value of the normalized power spectral density at 1 Hz. This is obtained by fitting the S_{id}/I_d as a function of the frequency with a line and by extracting the intercept of this line with the x-axis where the frequency is equal to 1 Hz. Such a method allows an easy visualization of the noise power spectral density. Figs. 6.5 and 6.6 report the dependence of S_{id}/I_d at 1 Hz on the substrate bias V_{BS} under both CB and SB conditions. Substrate bias is varied from reverse to forward biases for both n and pMOSFETs: from V_{BS}=-0.6 V to V_{BS}=0.6 V for nMOSFETs and from V_{BS}=0.6 V to V_{BS}=-0.6 V for pMOSFETs. For both n and pMOSFETs, a small effect of V_{BS} when applied under CB can be noticed. Under SB conditions, the application of a forward substrate bias reduces significantly the flicker noise when compared to zero substrate bias, while a reverse substrate bias has only a marginal effect.

In order to investigate the effect of a FSB under SB conditions, different bi-

asing schemes have been adopted. Results of these measurements are shown in Fig. 6.7 where the S_{id}/I_d for a single nMOS transistor is plotted as a function of frequency under SB for different substrate bias schemes: ZSB, forward substrate bias pulsing in-phase with respect to the gate pulsing (IP), and forward substrate bias pulsing 180° out-of-phase with respect to the gate switching bias (OP). Therefore, in the IP case a FSB is applied when the transistor is in the ON-state and switched to zero volt when the transistor is in the OFF-state; the OP case is the opposite: the FSB is applied when the transistor is in the OFF-state and switched to zero volt when the transistor is in the ON-state. The significant reduction of flicker noise occurs when the FSB is applied during the OFF-state (OP) of the transistor; on the contrary, FSB is hardly effective when applied during the ON-state (IP). Similar results have been obtained also for pMOS transistors [83].

The results of Fig. 6.7 indicate that the impact on noise of the gate bias switching between the ON- and OFF-state is enhanced when a forward substrate bias is applied during the OFF-state. Since the forward substrate bias tends to drive the MOS system towards accumulation, we may speculate that the substrate bias induced suppression of noise could be related to a transient accumulation of the silicon at the oxide interface.

Effect of gate OFF-voltage

In order to confirm the hypothesis made above, we measured the dependence of flicker noise on the gate OFF-voltage under zero substrate bias. Results are reported in Figs. 6.8 and 6.9, for n and pMOSFETs, respectively. Both the transistors show similar qualitative results. The normalized noise power spectral density S_{id}/I_d shows a small reduction when the gate OFF-voltage is decreased in magnitude towards the threshold voltage. A saturation plateau is observed for values of the gate OFF-voltage corresponding to sub-threshold depletion condition. When the V_{GS_OFF} is further decreased (increased in the pMOS case), driving the substrate at the gate oxide interface into accumulation, a further significant drop of the flicker noise occurs, a behavior not observed in previous works [6, 84].

In addition to the observed saturation plateau, Figs. 6.8 and 6.9 show only a small reduction in noise for a gate OFF-voltage around zero volts. Our finding is in good agreement with a previously reported noise reduction value in [85] for devices with similar gate oxide thickness. Additionally in [85] a diminishing noise reduction towards thinner oxides is found. According to the results shown

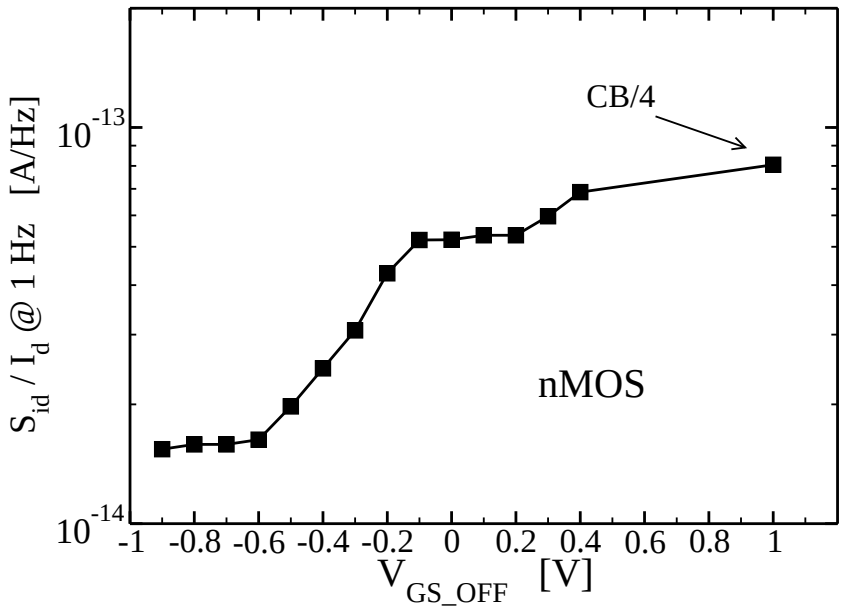


Figure 6.8: S_{id}/I_d @ 1 Hz vs. pulsed gate OFF-voltage V_{GS_OFF} for a zero volt substrate bias for nMOSFETs with V_{GS_ON}=1 V, V_{DS}=1 V.

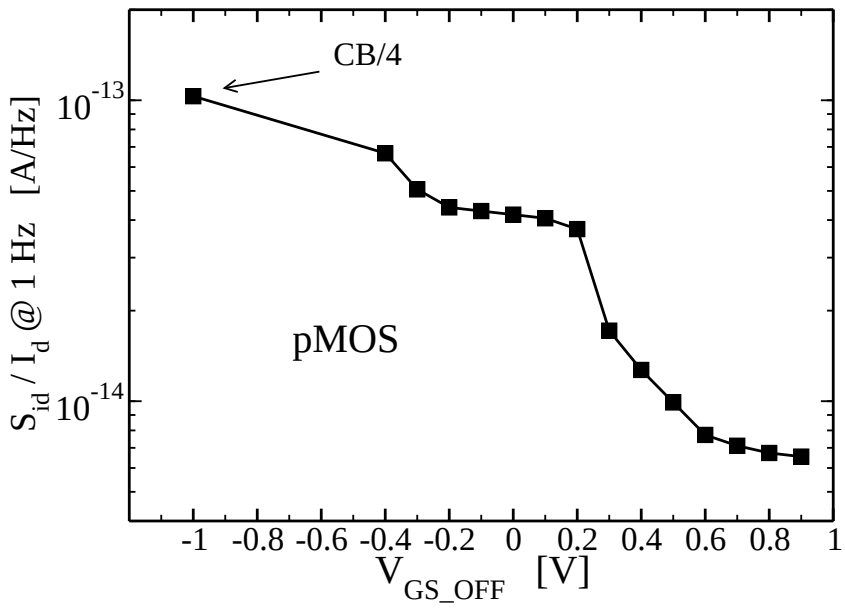


Figure 6.9: S_{id}/I_d @ 1 Hz vs. pulsed gate OFF-voltage V_{GS_OFF} for a zero volt substrate bias for pMOSFETs with V_{GS_ON}=-1 V, V_{DS}=-1 V.

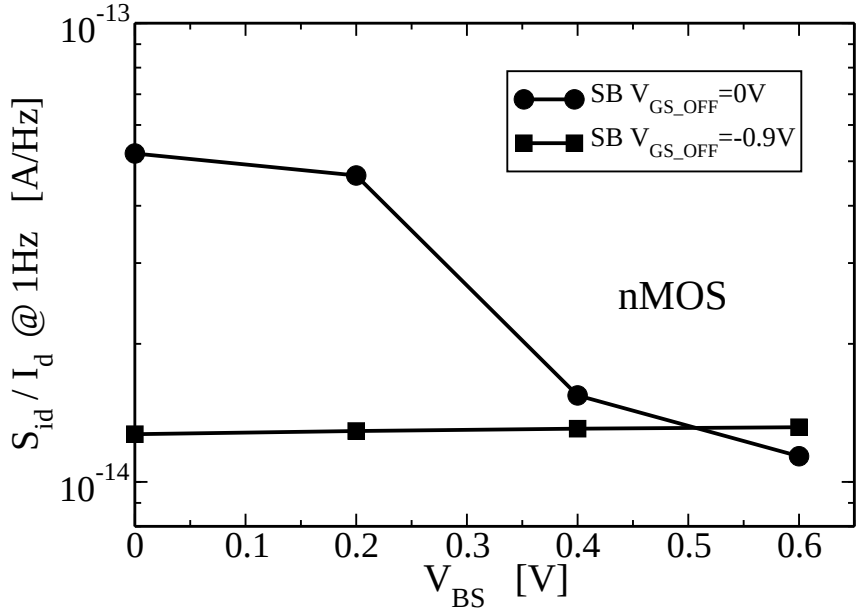


Figure 6.10: S_{id}/I_d @ 1 Hz vs. substrate bias V_{BS} for nMOSFETs with V_{GS_ON}=1 V, V_{GS_OFF}=0, -0.9 V , V_{DS}=1 V.

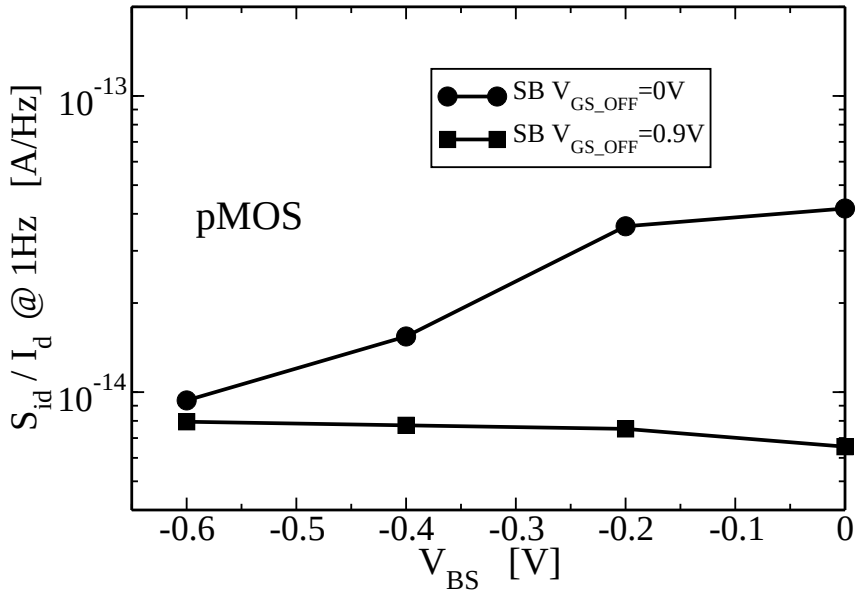


Figure 6.11: S_{id}/I_d @ 1 Hz vs. substrate bias V_{BS} for pMOSFETs with V_{GS_ON}=-1 V, V_{GS_OFF}=0, 0.9 V, V_{DS}=-1 V.

in this chapter a significant noise reduction is possible also for thin oxide devices if a gate voltage beyond zero volts or a respective substrate voltage driving the device into accumulation is provided.

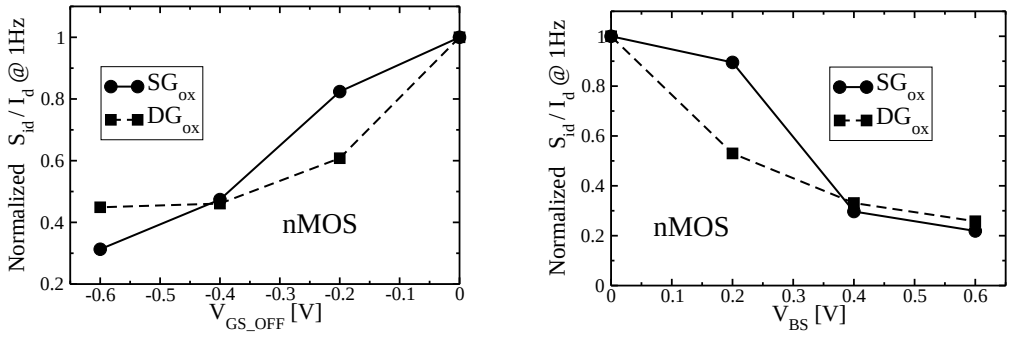
In Figs. 6.10 and 6.11 the substrate bias dependence of S_{id}/I_d is compared for two different gate OFF-voltages for n and pMOSFETs, respectively. As already reported, for a gate OFF-voltage of 0 V a strong dependence of noise on forward substrate bias is observed with a significative noise reduction. On the other hand, for a gate OFF-voltage driving the device towards accumulation (V_{GS_OFF}=-0.9 V for nMOS and V_{GS_OFF}=0.9 V for pMOS devices), only a very small noise variation with forward substrate bias can be found. This behavior additionally supports the assumption that accumulation of majority carriers is necessary for the noise reduction and the effect of forward substrate bias on noise reduction depends on the amount of accumulation reached already by the applied gate OFF-voltage.

Dependence on oxide thickness

In this section, the flicker noise measurements earlier performed are compared for devices having two different oxide thicknesses. Results for n and pMOSFETs, with a t_{ox}=2.2 nm (SG$_{ox}$) and t_{ox}=5.4 nm (DG$_{ox}$) are reported.

In Fig. 6.12(a) the S_{id}/I_d normalized to the value at V_{GS_OFF}=0 V as a function of the gate OFF-voltage for nMOS devices with SG$_{ox}$ and DG$_{ox}$ is reported. The ON-voltage is set in order to bias the transistors in strong inversion. Comparing the S_{id}/I_d for the two different t_{ox} it is evident that the higher sensitivity of the S_{id}/I_d on the V_{GS_OFF} occurs for devices with a thicker oxide thickness (DG$_{ox}$). Fig. 6.12(b) reports the S_{id}/I_d normalized to the value at V_{BS}=0 V as function of the substrate bias for nMOS devices having SG$_{ox}$ and DG$_{ox}$. The ON-voltage is set to operate the devices in strong inversion and the V_{GS_OFF}=0 V. Also in this case, devices with DG$_{ox}$ show a stronger sensitivity of the noise on the substrate voltage. pMOSFETs show similar results (Figs. 6.13(a) and 6.13(b).

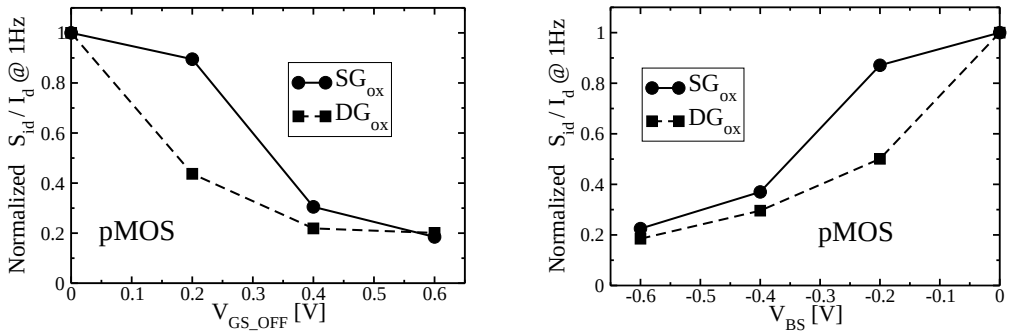
The different sensitivity amongst devices with different oxide thicknesses may be related to the following fact: transistors with a thicker oxide thickness require smaller negative voltages to reach accumulation (positive for pMOSFETs) or smaller values of forward substrate bias. Hence, for MOSFETs with DG$_{ox}$ a stronger reduction of the noise compared to SG$_{ox}$ for smaller variation of the V_{GS_OFF} or of the V_{BS} around zero volt can be found.



(a) Dependence on the gate OFF-voltage V_{GS_OFF}

(b) Dependence on the substrate bias V_{BS}

Figure 6.12: Normalized S_{id}/I_d @ 1 Hz under SB conditions for nMOS devices with different oxide thicknesses.



(a) Dependence on the gate OFF-voltage V_{GS_OFF}

(b) Dependence on the substrate bias V_{BS}

Figure 6.13: Normalized S_{id}/I_d @ 1 Hz under SB conditions for pMOS devices with different oxide thicknesses.

6.2.3 Discussion

From results reported in the previous sections, we can say that forward substrate bias concurs to suppress the flicker noise under switched gate bias by transiently inducing accumulation at the silicon-oxide interface during the OFF-state. Since the $1/f$ noise affecting MOSFET drain current is usually related to the trapping/detrapping processes of minority carriers into/from traps located at the silicon-oxide interface or inside the oxide, we conclude that forward substrate bias, by promoting the accumulation of majority carriers at the interface, reduces the trap emission time constant for emptying traps in the gate oxide during the MOSFET OFF-state. The reduction in emission time is dependent on the gate

to substrate voltage driving the transistor towards accumulation and most probably originates from an increased recombination rate of trapped minority carriers with accumulated majority carriers. Besides the accumulated majority carriers one possibly needs also to regard empty interface states that could support the recombination of trapped charges with majority carriers. Interface states residing in energy between conduction and valence band of the silicon and located at the silicon-oxide interface are empty when they are above the Fermi level during accumulation (nMOS case). Such empty interface states could provide an effective fast path for carrier recombination. For nMOSFETs trapped charges released to the conduction band could recombine via fast interface traps or tunnel directly to interface traps and recombine with the accumulated majority carriers in the valence band. Analog considerations hold for pMOSFETs.

Based on the results reported in Figs. 6.8 and 6.9, we may conclude that the strong reduction of flicker noise can also be obtained by switching the gate bias, provided that V_{GS_OFF} is well below ground or above supply voltage, for the n-channel and p-channel cases, respectively. In circuits, gate voltages below ground and above supply voltage are more difficult to establish. Hence, forward substrate bias seems appropriate for noise reduction in circuits using scaled technologies and switched bias conditions. Especially the fact that forward substrate bias is needed only during the transistor OFF-state suggests new topologies and biasing schemes in circuits [86, 87].

6.2.4 Measurement on a 45 nm technology

All the measurements proposed in the previous part of this chapter have been made on a 0.13 μm technology. During this work, has been possible also to measure flicker noise in devices fabricated in a 45 nm technology. n and pMOSFETs with nitrided gate oxide with a t_{ox} of 1.8 nm have been analyzed. The gate length of the measured devices is L=0.12 μm and the gate width is W=4 μm and W=8 μm for n and pMOSFETs, respectively. The switching frequency of the gate pulse is f_{sw}=2.5 MHz with 50% duty cycle. Rising and falling times are t_r=t_f=8 ns.

Fig. 6.14 shows the dependence of the S_{id}/I_d on the gate OFF-voltage under SB conditions with a V_{GS_ON}=1 V and V_{DS}=1 V. Results are similar to the ones obtained for the 0.13 μm technology. The curve presents a saturation plateau around zero volt and the noise is reduced for gate OFF-voltages below zero volt bringing the devices into accumulation.

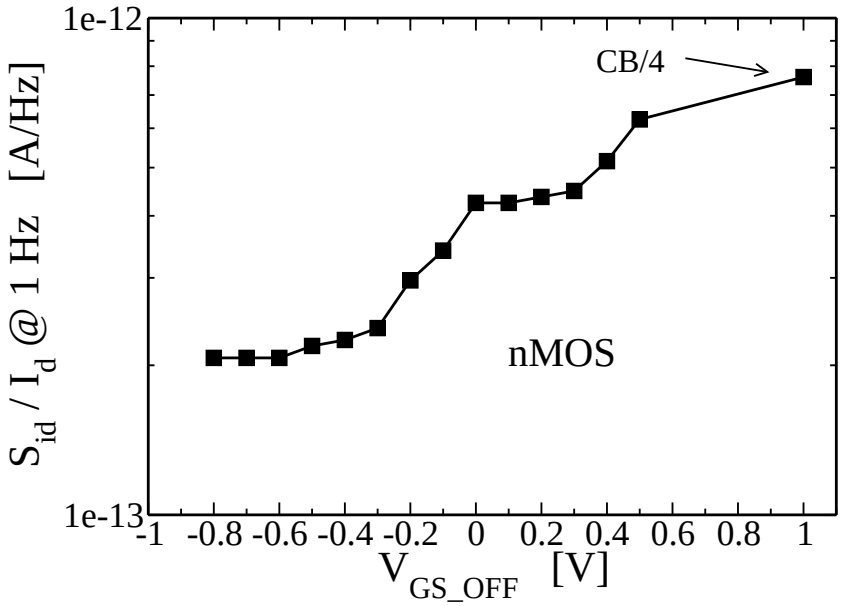


Figure 6.14: S_{id}/I_d @ 1 Hz vs. pulsed gate OFF-voltage V_{GS_OFF} for a zero volt substrate bias for nMOSFETs with V_{GS_ON}=1 V, V_{DS}=1 V.

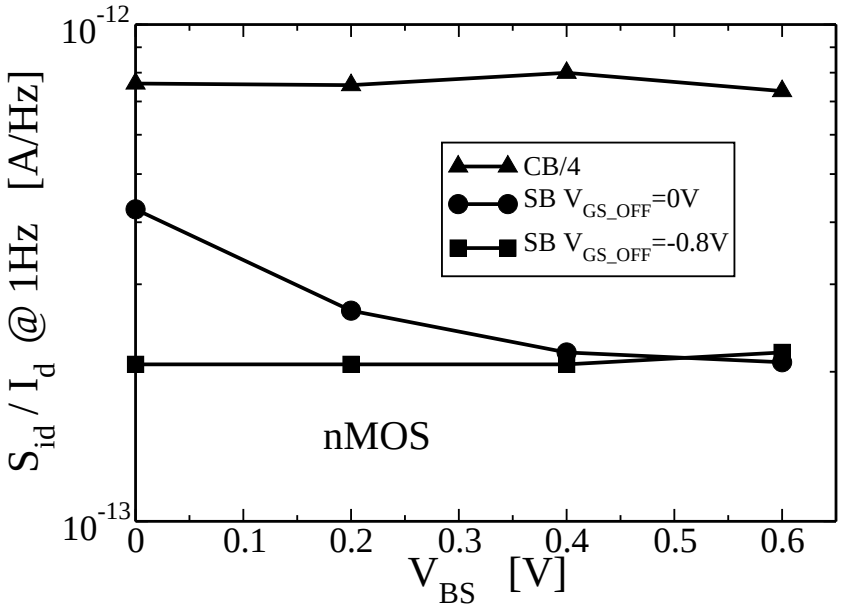


Figure 6.15: S_{id}/I_d @ 1 Hz vs. substrate bias V_{BS} for nMOSFETs under CB (V_{GS}=1 V) and SB (V_{GS_ON}=1 V, V_{GS_OFF}=0 and -0.8 V) with V_{DS}=1 V.

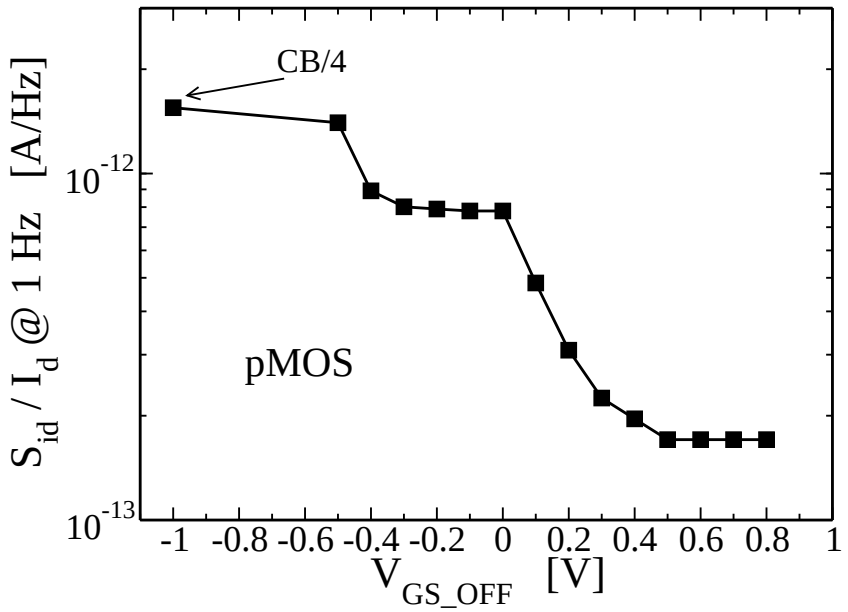


Figure 6.16: S_{id}/I_d @ 1 Hz vs. pulsed gate OFF-voltage V_{GS_OFF} for a zero volt substrate bias for pMOSFETs with V_{GS_ON}=-1 V, V_{DS}=-1 V.

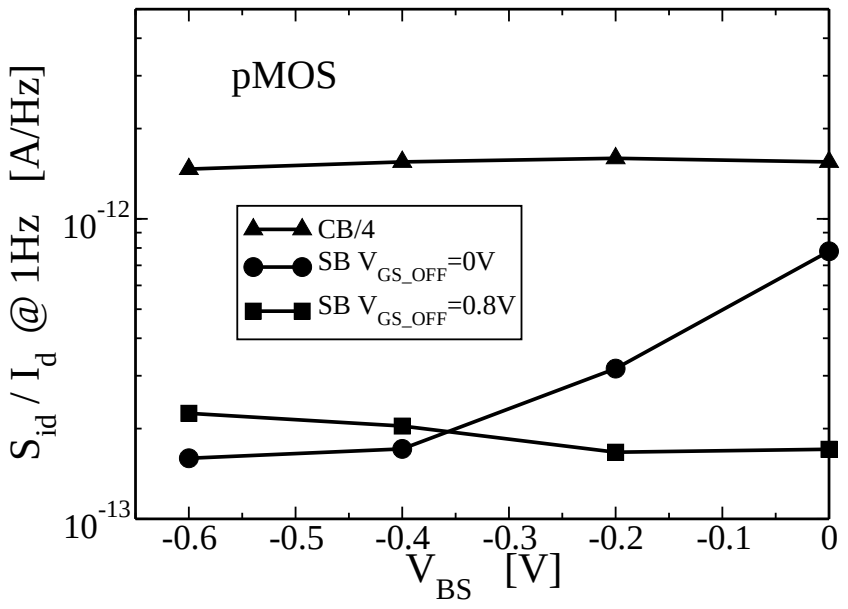


Figure 6.17: S_{id}/I_d @ 1 Hz vs. substrate bias V_{BS} for pMOSFETs under CB (V_{GS}=-1 V) and SB (V_{GS_ON}=-1 V, V_{GS_OFF}= 0 and 0.8 V) with V_{DS}=-1 V.

Fig. 6.15 shows the dependence of flicker noise on substrate bias under CB and SB conditions. In particular, under SB conditions two different gate OFF-voltages have been analyzed: V_{GS_OFF}=0 and -0.8 V with a V_{GS_ON}=1 V and V_{DS}=1 V. A forward substrate bias is hardly effective under CB conditions. A reduction of the flicker noise is achieved when a forward substrate bias is applied with a V_{GS_OFF}=0 V compared to the case V_{BS}=0 V. Once the device is brought into accumulation (V_{GS_OFF}=-0.8 V), the noise reduction is already reached for V_{BS}=0 V and not further reduction occurs applying a forward substrate bias. Similar results hold also for pMOSFETs (Figs. 6.16 and 6.17).

Experimental results on a 45 nm technology confirms the noise reduction under SB conditions induced by applying a forward substrate bias observed in an older 0.13 μm technology.

6.3 RTS noise measurement

In this part we report results of measurements of RTS noise under constant and switched bias conditions in small-area nMOSFETs [88, 89].

6.3.1 Measurement condition

RTS noise measurements have been performed in small-area nMOSFETs with 2.2 nm thick nitrided gate oxide, gate poly length L=0.1 μm and widths W=0.4, 0.75 μm manufactured in a 0.13 μm technology [26]. RTS noise has been measured in both time and frequency domain using the differential set-up reported in Fig. 6.1.

Measurements under CB conditions are performed as describe in Chapter 5 and the gate bias dependence of τ_c and τ_e allows us to extract the trap distance inside the oxide (x_t) and to recognize between acceptor and donor traps. All the analyzed traps are acceptor ones.

Time domain analysis of RTS noise under SB conditions with 50% duty-cycle is performed using the technique described in section 4.6.2 and proposed in [60]. The switching frequency is set to f_{sw}=10 kHz. For each bias condition a long time frame of the drain current in the ON-state (up to 2 minutes) is recorded by the digital oscilloscope. For each semi-period in the ON-state an average algorithm gives the level of the current, high or low, and a simple software extract the capture (τ_c) and the emission (τ_e) time constants. Therefore, a possible transition during a single semi-period is lost and the time resolution of the method is

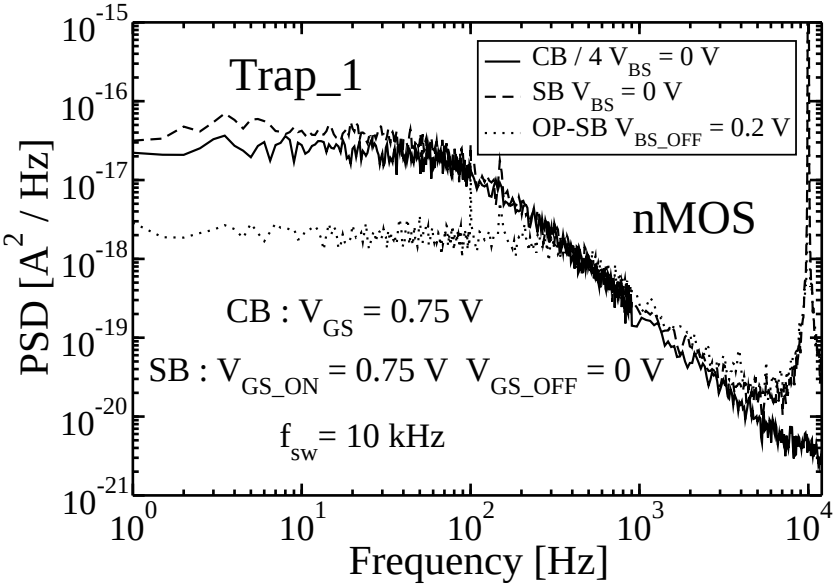


Figure 6.18: RTS PSD for: CB; SB; gate- and substrate-SB (OP). Forward substrate bias applied OP with respect to the gate bias reduces the low-frequency plateau of the PSD.

0.1 ms. To prove the validity of this approach, for each trap and each bias point, the measured power spectral density has been compared to Eq. 4.45 in which the emission and capture time constants have been substituted with the respective extracted values.

The drain-to-source voltage has been kept to V_{DS}=1.0 V and the same bias schemes used for flicker noise measurement have been analyzed (Fig. 6.2). The effect on the PSD and on the time constants of the RTS noise of a substrate bias applied in-phase and out-of-phase with respect to the gate switching bias has been studied. Results on the impact of the V_{GS_OFF} on the RTS noise have been also reported.

6.3.2 Measurement results

Effect of substrate bias

Fig. 6.18 reports the power spectral density of a trap (Trap_1) featuring estimated trap position into the oxide x_t=0.65 nm under: CB (V_{GS}=0.75 V), and SB (V_{GS_ON}=0.75 V and V_{GS_OFF}=0 V) with zero substrate bias and with a for-

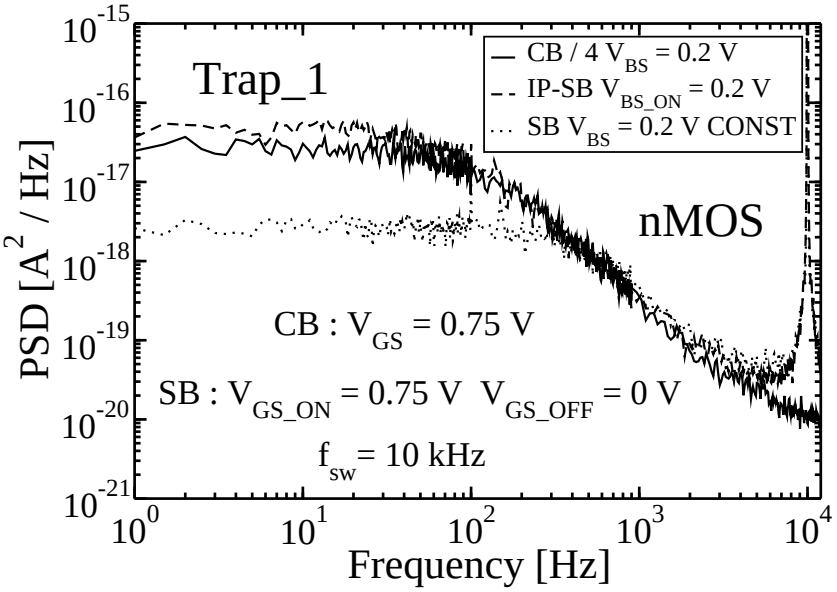


Figure 6.19: RTS PSD for: CB; gate and substrate SB (IP); gate SB and constant FSB.

ward substrate bias switched OP with respect to the gate pulsing. In this latter case the substrate bias in the ON-state is set to V_{BS_ON}=0 V and in the OFF-state to V_{BS_OFF}=0.2 V. It is interesting to notice that switching the gate between an ON- and an OFF-state only marginally affects the noise compared to the CB case. In particular, SB slightly increases the low-frequency plateau of the PSD. The application of a FSB during the OFF-state of the transistor decreases the noise of about one order of magnitude in the low-frequency range.

In order to prove that the FSB is effective only in the OFF-state we performed measurements applying the FSB both in-phase with respect to the gate pulsing and with a constant value over all the switching period, i.e. the FSB is applied both during the ON- and the OFF-state. Results of these measurements for Trap_1 are reported in Fig. 6.19. In order to have the same bias conditions, in the CB case a constant FSB (V_{BS}=0.2 V) has been applied. Fig. 6.19 shows that the strong reduction of the low-frequency noise under SB compared to CB occurs only for a constant FSB (V_{BS}=0.2 V), while applying FSB only in the ON-state (V_{BS_ON}=0.2 V) only marginally affects the PSD. These measurements prove that, as for flicker noise, the application of a FSB concurs to suppress the RTS noise only when applied during the OFF-state of the device.

Fig. 6.20 reports the dependence of the RTS PSD on the V_{BS_OFF} under

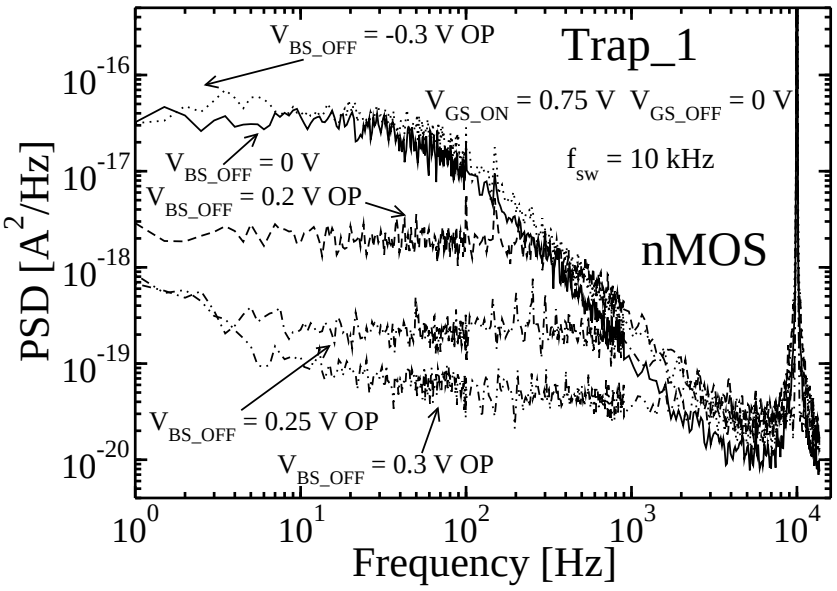


Figure 6.20: RTS PSD under gate- and substrate-SB (OP case) for different values of the substrate bias V_{BS_OFF} applied during the OFF-state. Increasing V_{BS_OFF} the PSD plateau at low frequencies decreases.

gate SB for Trap_1. The gate voltage is switched between V_{GS_ON}=0.75 V and V_{GS_OFF}=0 V while different values of the substrate bias are applied OP with respect to the gate bias. In particular, starting from a reverse substrate bias V_{BS_OFF}=−0.3 V, a forward substrate bias V_{BS_OFF}=0.3 V is reached. Results of Fig. 6.20 show as the application of the reverse substrate bias hardly affects the RTS PSD compared to the case with zero substrate bias. On the contrary, the low-frequency plateau of the PSD is significantly decreased increasing the FSB up to 0.3 V.

As reported earlier in section 4.5.2, the low-frequency plateau of the PSD (Eq. 4.41) and the total power P (Eq. 4.43) associated to the RTS are influenced by three factors: emission and capture time constants and current fluctuation amplitude ΔI. We know that the maximum value of the low-frequency plateau of the PSD and of the total power P occurs for τ_c=τ_e. In order to obtain information on the time constants and on ΔI, a time domain analysis of the RTS noise is mandatory. In our experiments we measure ΔI observing that its value stays constant for each bias point. Thus, a decreasing of the PSD low-frequency plateau and of the total power P is caused by the values assumed by the capture and the emission time constants.

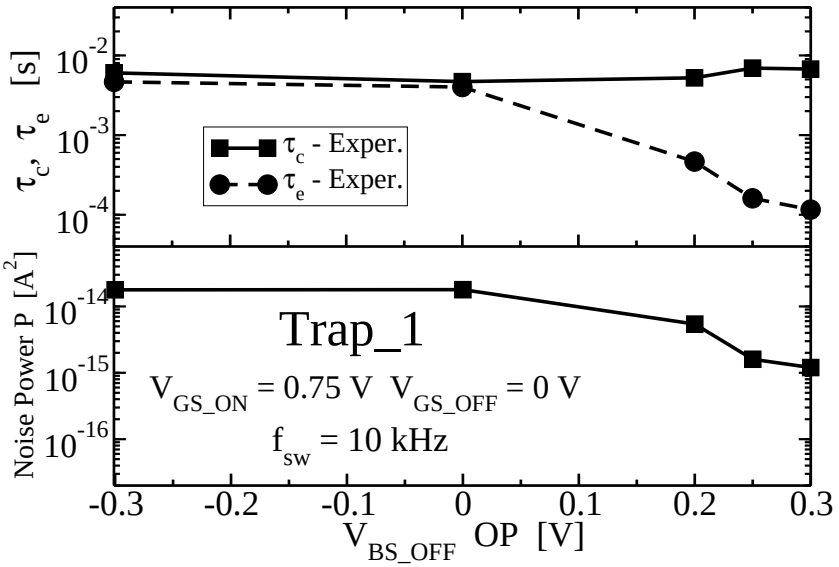


Figure 6.21: τ_c, τ_e and RTS-noise power P under gate and substrate SB (OP case) as a function of substrate bias V_{BS_OFF} applied during the OFF-state. Increasing V_{BS_OFF} τ_e decreases affecting also the noise power that shows a strong reduction.

In order to prove that we extracted τ_e and τ_c under SB conditions with substrate bias applied OP with respect to the gate switching bias. Results are reported in Fig. 6.21. In the upper part of Fig. 6.21 the substrate bias dependence of emission and capture time constants under SB is shown. The substrate bias is applied OP with respect to the gate bias. Focusing on the τ_c and τ_e values at zero substrate bias V_{BS_OFF}=0 V, we can notice that they assume similar values giving therefore the maximum value of the power P, lower part of Fig. 6.21. The application of the reverse substrate bias V_{BS_OFF}=-0.3 V hardly modifies both τ_c and τ_e and therefore also the power P. The strong reduction of the power associated to the RTS noise occurs for FSB and the reason is the decrease of the emission time constant while the capture time constant shows a slight increase enhancing therefore the difference between the two time constants. In fact, increasing the FSB from 0 to 0.3 V a more than one order of magnitude reduction of the τ_e occurs. Practically, the trap is almost always empty and, once an electron is captured, it is emitted with a very fast emission time constant.

We performed the same analysis also for another trap (Trap_2) having an estimated trap position inside the oxide x_t=0.2 nm. Results are shown in Figs. 6.22, 6.23, and 6.24. Under switched bias condition the gate has been commutated

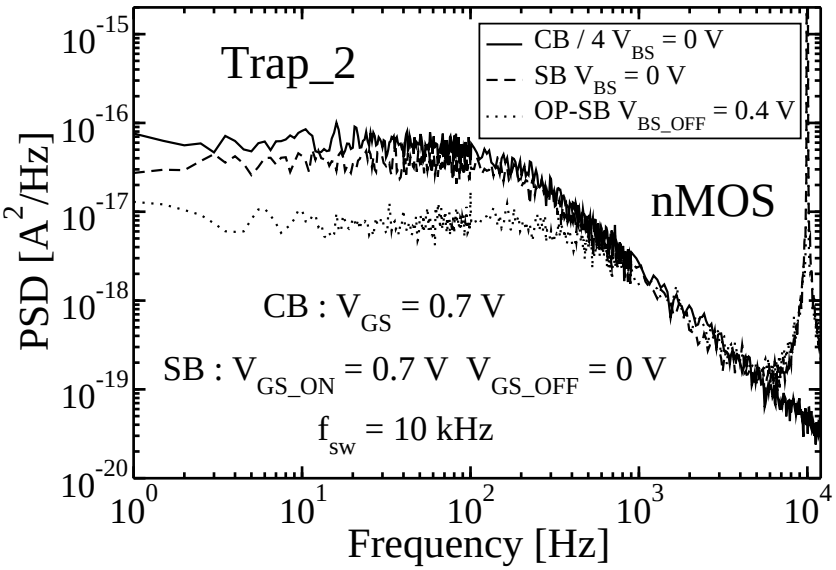


Figure 6.22: RTS PSD for: CB; SB; gate- and substrate-SB (OP). Forward substrate bias applied OP with respect to the gate bias reduces the low-frequency plateau of the PSD.

between V_{GS_ON}=0.7 V and V_{GS_OFF}=0 V with a f_{sw}=10 kHz.

Fig 6.22 shows that while under gate SB with zero applied substrate bias the RTS PSD is only slightly influenced compared to the CB case, the application of a FSB OP with respect to the gate bias strongly reduces the low-frequency plateau of the PSD. The applied value of the FSB during the OFF-state is set to V_{BS_OFF}=0.4 V.

The dependence of the PSD on different substrate bias values applied always during the OFF-state of the transistor are reported in Fig. 6.23. As for Trap_1, also for Trap_2 a reverse substrate bias V_{BS_OFF}=-0.4 V hardly influences the PSD of the RTS noise compared to the case with zero substrate bias. On the contrary, increasing the substrate bias reaching V_{BS_OFF}=0.6 V strongly reduces the noise. Comparing Trap_1 to Trap_2 (Fig. 6.20 and Fig. 6.23), a different sensitivity on V_{BS_OFF} can be noticed. In particular, while for Trap_1 the application of V_{BS_OFF}=0.2 V already concurs to the suppression of the noise, for Trap_2 it is necessary to increase V_{BS_OFF} to 0.4 V to appreciate a reduction of the PSD. This fact is related to a different dependence of emission and capture time constants on the applied substrate bias. Fig. 6.24 shows τ_c and τ_e (upper part) and the total noise power P (lower part) as a function of V_{BS_OFF}. τ_c and τ_e stay almost constant, and hence also the power P, over the range -0.4 V$< V_{BS_OFF} <$ 0.2 V.

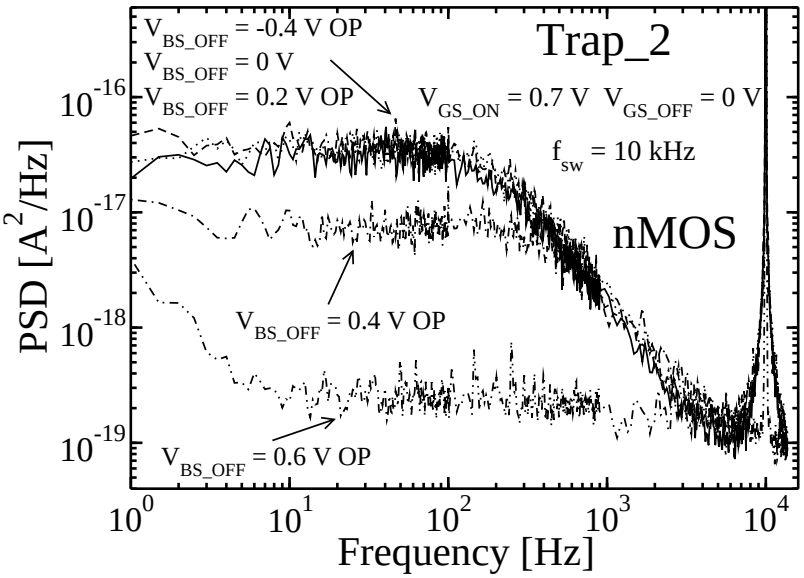


Figure 6.23: RTS PSD under gate- and substrate-SB (OP case) for different values of the substrate bias V_{BS_OFF} applied during the OFF-state. Increasing V_{BS_OFF} the PSD plateau at low frequencies decreases.

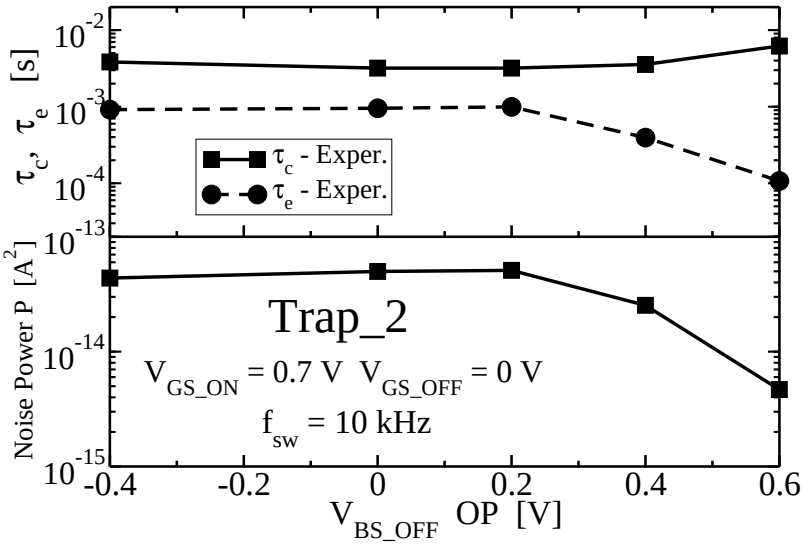


Figure 6.24: τ_c, τ_e and RTS-noise power P under gate and substrate SB (OP case) as a function of substrate bias V_{BS_OFF} applied during the OFF-state. Increasing V_{BS_OFF} τ_e decreases affecting the noise power that shows a strong reduction.

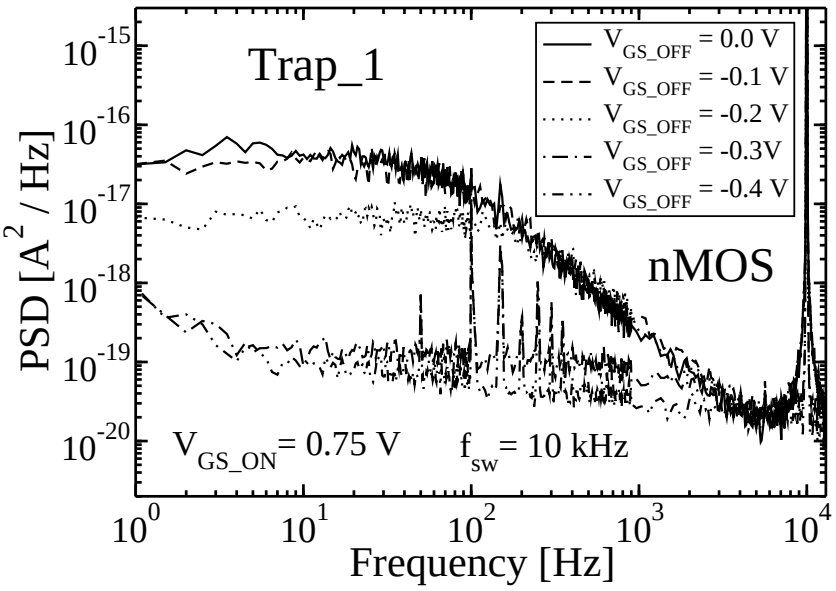


Figure 6.25: RTS PSD under gate SB for different values of the gate OFF-voltage V_{GS_OFF}. Decreasing V_{GS_OFF} the PSD plateau at low frequencies decreases.

As the V_{BS_OFF} is increased above 0.2 V, a strong reduction of the emission time constant concurs to the suppression of the noise power.

Effect of gate OFF-voltage

From previous measurements, we have seen that a strong reduction of the RTS noise can occurs under SB conditions applying a forward substrate bias during the OFF-state of the device. The reduction is due to the decrease of the emission time constant that, enhancing the difference with the capture time constant, concurs to the noise suppression. As for flicker noise measurements, we tried, following investigations proposed in [7, 60], to study the dependence of the RTS noise for different gate OFF-voltages.

The PSD of RTS noise under SB condition for Trap_1 for different V_{GS_OFF} is shown in Fig. 6.25. As already reported in previous works [7, 60], driving the device into accumulation, strongly reduces the RTS noise. In particular, the decrease is higher for lower gate OFF-voltages.

Fig. 6.26 reports the emission and the capture time constants (upper part) and the noise power P (lower part) as a function of the V_{GS_OFF}. The strong reduction

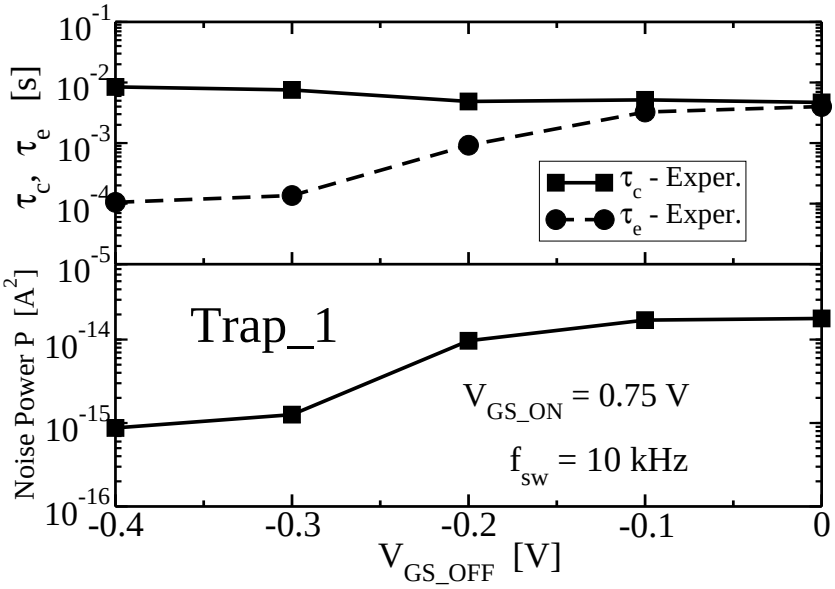


Figure 6.26: τ_c, τ_e and RTS-noise power P under gate SB as a function of gate OFF-voltage V_{GS_OFF}. Decreasing V_{GS_OFF} τ_e decreases affecting the noise power that shows a strong reduction.

of the PSD low-frequency plateau and the power P is associated to a decreasing of the emission time constant with V_{GS_OFF}.

6.3.3 Discussion

Results obtained for RTS noise show that a FSB applied during the OFF-state of the device strongly reduces the noise. From time domain measurements emission and capture time constants have been extracted showing that the suppression of the RTS noise is related to a strong reduction of the emission time constant that enhances the difference with the capture time constant. A departure from the condition τ_c=τ_e implies a reduction of the power associated to the RTS noise. The reduction of the emission time constant can be explained as follows: the forward substrate bias tends to drive the MOS system towards accumulation; hence, we conclude that the FSB-induced suppression of noise could be related to a transient accumulation of the silicon at the oxide interface leading to very large recombination rate of trapped carriers with accumulated holes during the OFF-state.

Another way to bring the device into accumulation is to decrease the gate

OFF-voltage well below the threshold voltage. Experiments proved that for the same traps analyzed applying a forward substrate bias, switching the device to more negative voltages as zero volt, the RTS noise decreases due to a reduction of the emission time constant.

It is important to remark that in some cases the RTS noise can also be increased by switching the gate bias and eventually by the application of a forward substrate bias compared to the constant bias case. This could happen in traps for which the difference between emission and capture time constants under constant bias is high, i.e. $\tau_e > \tau_c$, and the application of a switched bias tends to equilibrate the time constants increasing the RTS noise power associated to such traps.

However, the significant reduction of the RTS noise power of traps with large noise contribution, hence featuring $\tau_c \simeq \tau_e$ under constant bias conditions, could justify the average suppression of flicker noise in large-area devices affected by several traps.

The application of a forward substrate bias could benefit circuits using small-area MOSFETs, especially those showing a large noise tail distribution such as CMOS image sensors [5, 90].

Chapter 7

Conclusions

In this thesis we have investigated low-frequency noise in MOSFETs operating under constant bias and switched bias conditions. Our work has aimed to provide useful results about the modeling and the characterization of flicker and RTS noise in MOSFETs.

After a brief introduction on electrical characterization we performed charge pumping and mobility measurements in order to study the interface state density and the mobility of MOS transistors. We analyzed devices with a different process option that introduces a fluorine doping. Devices having this fluorine doping step show a lower interface state density and a higher mobility. The reason for that may be explained based on the hypothesis that the fluorine doping step improves the interface quality between the silicon and the gate oxide and a less interface states are present compared to conventional devices. As a consequence, the mobility is improved due to the less Coulomb scattering.

Simulation of RTS noise under constant and switched bias conditions has been performed by means of a Monte Carlo simulator. Trapping and detrapping processes have been simulated reproducing the occupation probability of a trap both in time and in frequency domain. Under switched bias condition emission and capture time constants are modulated by the square wave applied to the gate. This modulation could both increase and decrease the RTS noise compared to the costant bias case. This fact depends on the modulation of the emission and capture time constants under switched bias conditions compared to their values under constant bias conditions. The superposition of different traps with different time constants has been simulated to generate flicker noise under both constant and switched bias conditions.

RTS noise has been analyzed in n and pMOSFETs under constant bias con-

ditions, in particular, measuring and simulating the dependence of the emission and capture time constants on the applied gate bias. Time domain measurements have been performed in small-area devices in order to be able to isolate the contribution of a single trap on the drain current. The gate bias dependence of the RTS noise allowed us to distinguish between acceptor and donor traps. In our experiments we found only acceptor type traps. The modeling based on the standard Shockley-Read-Hall theory has shown that emission and capture time constants can be reproduced only for a subset of the analyzed traps. For the others, a much stronger dependence of the capture time constant on the gate bias can be modeled only by empirically varying the capture cross-section of the traps. Similar results hold both for nMOS and for pMOS devices.

Both flicker and RTS noise have been measured in n and pMOSFETs under constant and switched bias conditions analyzing different bias schemes. We have shown that the application of a forward substrate bias strongly reduces the flicker noise of transistors operating under switched bias conditions when the gate is switched between an ON-state in inversion and an OFF-state set to 0 V. We proved that a forward substrate bias is effective when applied during the OFF-state of the device. We speculated that a forward substrate bias, by promoting the accumulation of majority carriers at the interface, reduces the trap emission time constant for emptying traps in the gate oxide during the MOSFET OFF-state. Similar results can be obtained for zero substrate bias if the gate voltage in the OFF-state is set well below 0 V for nMOS and above 0 V for pMOS devices. These results show that reaching accumulation is mandatory to have a reduction of flicker noise. The method presented in this work for the reduction of flicker noise is of particular interest in circuits where it is difficult to reach gate voltages below ground and above supply voltage.

RTS noise measurements in time domain showed a strong reduction of RTS noise due to the reduction of the emission time constant when a forward substrate is applied during the OFF-state of a switched transistor. This is the case when the application of a forward substrate bias enhances the difference between emission and capture time constants with respect to their values under constant bias conditions. We know that an increase of RTS noise can appear under switched bias conditions. However, the significant reduction of the RTS noise power of traps with large noise contribution under constant bias conditions could justify the average suppression of flicker noise in large-area devices affected by several traps. The application of a forward substrate bias could be useful to reduce the RTS noise in circuits using small-area MOSFETs, hence affected by such a noise.

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