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Experimental Characterization and Modeling of GaN-based Power Devices Reliability

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Maurizio

Abstract

Nowadays, power electronics plays a fundamental role in enhancing energy efficiency, reducing CO_2 emissions, and promoting sustainable development, which is crucial for a more environmentally conscious and energy-efficient future. Its applications are spreading everywhere, including energy saving, renewable energy systems, electric/hybrid vehicles, industrial automation, aerospace, etc.. In particular, power electronics deals with the conversion and the control of electric power, using high-efficiency, reliable and even more compact electronic converters based on switching mode semiconductor power devices. In this scenario, gallium nitride (GaN) devices grown on silicon substrates are of great interest due to their capability to operate at relatively high voltage and frequency with higher efficiency and comparable cost of the silicon counterparts. Although GaN transistors demonstrate impressive characteristics, as emerging technology, there are still many degradation mechanisms affecting the device performance and reliability that need further investigation and understanding. More specific, charge trapping and de-trapping mechanisms, triggered by high electric fields and temperatures, are the main causes leading to the transistor degradation/failure.

This PhD research project is focused on the comprehensive identification, characterization, and modeling of the root causes that limit the gate reliability of AlGaN/GaN high electron mobility transistors (HEMTs) featuring pGaN gate technology, by accelerated life tests and electro-thermal simulations. Regarding this topic, this dissertation provides the following contributions:

- gate biases, temperatures, and device geometry dependencies of the long-term gate reliability in GaN-based power HEMTs with p-type gate under DC stress conditions are analyzed. Two failure mechanisms have been identified, hence, accurate field-acceleration fitting models are adopted to estimate the gate lifetime.

- a combined experimental/simulation analysis has been performed to study the time-dependent gate breakdown (TDGB) under pulse stress

conditions. Thanks to this investigation, reliability issues introduced by the switching operation, which could not be identified by DC stress analysis, have been highlighted.

- an extensive analysis on the role of both switching frequency (ranging from 100 kHz to 1 MHz) and duty cycle (from 10% to 90%) on the time-dependent gate breakdown of high electron mobility transistors (HEMTs) with Schottky metal to p-GaN gate. Findings of this analysis are useful both for further technology improvement and for GaN-based power circuit designers.

In addition, storage/release mechanisms within the buffer layers responsible for ON-resistance degradation (ΔR_{ON}) have been investigated by means of back-gating current deep-level transient spectroscopy (I-DLTS) and Technology Computer Aided Design (TCAD) simulations. A genetic algorithm has been employed to accurately fit the experiments allowing to understand the temperature, stress-bias, and stress-time dependence of ΔR_{ON}. Moreover, devices featuring different buffer layers composition are compared, providing useful information for the epi-stack optimization, i.e., vertical down scaling.

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Chapter 1

Introduction

Power electronics is a branch of electrical engineering that focuses on the conversion, control, and manipulation of electrical power. It deals with the design, analysis, and implementation of electronic systems and devices that efficiently convert and manage electrical energy from one form to another one.

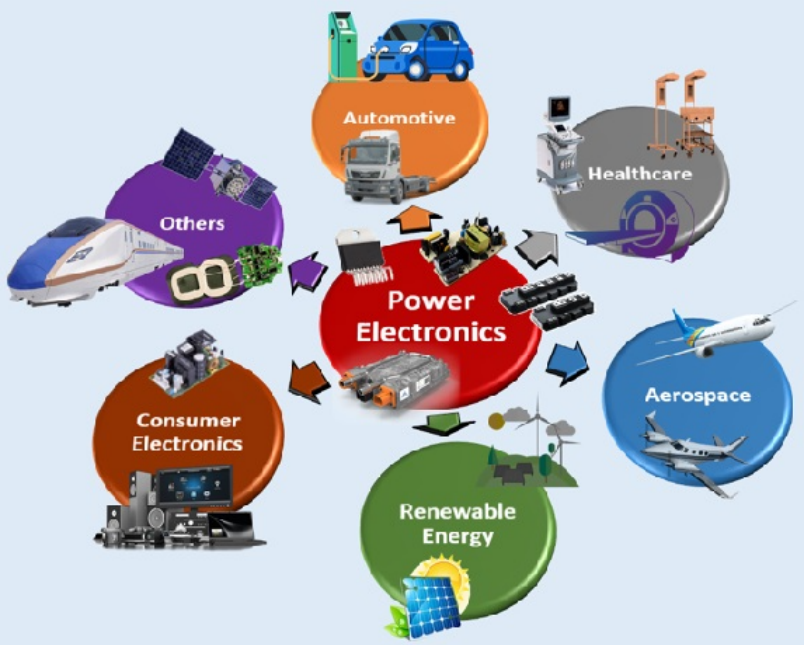

Figure 1.1: *Application fields of Power electronics [1].*

By enabling energy-efficient technologies, electrification of various sectors and promoting the integration of renewable energy sources, power electronics significantly contributes to mitigating climate change and meeting energy

demands associated with higher living standards [2].

Its application underpins various industries (see Fig. 1.1), ranging from energy production, distribution and storage (systems for renewable energy, HVDC/HVAC Transmission, UPS, smart grids, etc.) to transportation (hybrid and electric vehicles, high speed trains, etc.), consumer electronics (laptops, smartphones, and chargers), and many others [3–6].

This expansive field encompasses various research areas, including power converters, switching techniques, control and feedback systems, gate drivers, and thermal management and cooling strategies. Nevertheless, power converters and inverters hold a central position within this complex system, and, consequently, there is a growing demand for power transistors that can deliver high performance, reliability, and cost-efficiency. It comes as no surprise that power transistors have sparked considerable interest within research groups worldwide, given their crucial role in the world of Power Electronics.

In order to cover the wide range of application fields, Power Electronics must face with a multitude of challenges, seeking the balance between performance, cost-effectiveness, and reliability.

1.1 Power Devices Properties

Evaluating the performance and capabilities of power electronics devices or technologies requires considering several figures of merit that provide insight into their efficiency, reliability, and suitability for specific applications. All these factors depend on both the material properties and device dimensions/geometries. Here are some key features commonly used in the evaluation of power electronics devices [7–12]:

1. Efficiency: it is a crucial figure of merit that indicates how effectively a device converts input power to output power. Higher efficiency values mean reduced energy losses and better overall performance.

2. Switching Speed: refers to how quickly a device can switch from high voltage/current levels to low ones, and vice versa. Faster switching speeds are advantageous for reducing switching losses and enabling high-frequency operation which is preferred for reducing the size of passive components like inductors and capacitors in a design.

3. Voltage Rating: represents the maximum voltage that a device can handle safely without breaking down. It's crucial for devices in high-voltage applications to prevent device failure.

4. Current Rating: specifies the maximum current the device can handle without being damaged. A higher current rating is generally preferred for high-power applications.

5. Temperature Rating: it indicates the maximum temperature a device can withstand while maintaining its performance and reliability. This figure is crucial for assessing a device's ability to operate in high-temperature environments without degradation.

6. ON-Resistance: represents the resistance when the device is fully conducting. Lower ON-resistance values lead to reduced conduction losses and higher efficiency.

7. Reliability Metrics: these include figures such as Mean Time Between Failures (MTBF), which provide insights into the device's expected operational lifespan and reliability.

8. Size and Weight: In some applications, the size and weight of the device can be crucial. Smaller and lighter devices may be preferred for space-constrained applications.

9. Cost: the cost of a power electronics device is an essential figure of merit, especially in mass production applications. Balancing performance with cost-effectiveness is crucial.

It's worth precising that the significance of each property depends on the specific application and the requirements of the system in which the power electronics device will be used. A thorough evaluation should consider multiple figures of merit to ensure that the chosen device or technology meets the desired performance, efficiency, and reliability goals.

1.2 Power Device Technologies

To meet the growing need for increasingly efficient, reliable and compact technologies capable of satisfying the requirements of the system in which the power electronics device will be used, the intrinsic limits of Si (i.e. limited switching frequency, blocking voltage and temperature capability) arise the need to move towards wide bandgap (WBG) semiconductors, like gallium nitride (GaN) and silicon carbide (SiC). This wider energy gap allows WBG materials to operate at higher temperatures, voltages, and frequencies, making them suitable for various high-power and high-frequency applications.

1.2.1 Si, SiC and GaN Properties

The application field of Si, SiC and GaN strongly depend on their intrinsic material properties which are useful for switching power applications. In particular, the most important characteristics are [7, 8, 13, 14]:

- Bandgap (E_G): The bandgap energy is the minimum energy required to move an electron from the valence band to the conduction band. Wider bandgap implies lower intrinsic carrier concentration, which is strongly dependent on the temperature and play an important role on the leakage currents. As a consequence, wider bandgap allows devices to operate at higher temperatures;

- Critical Electric Field (E_C): it is the maximum electric field strength that a semiconductor material can withstand. Above such value the rate of impact ionization increases rapidly, leading to device breakdown. Higher critical field means that the impact ionization, hence, the avalanche-induced breakdown, occurs at higher voltages.

- Thermal Conductivity (k): it is a fundamental property of semiconductors materials, and it measures a material's ability to conduct heat. Larger thermal conductivity implies that the device can operate at a higher power density levels, hence, it can be made smaller;

- Carrier Mobility (μ): it measures how easily and quickly charge carriers (electron and holes) can move through the crystal lattice of a semiconductor when an electric voltage is applied. Higher mobility values indicate that the charge carriers can move more efficiently leading to lower resistivity and conduction losses.

- Carrier Saturation Velocity (v_{SAT}): it refers to the maximum velocity the maximum velocity that charge carriers can attain in a semiconductor material under the influence of an electric field before they stop accelerating due to scattering.Higher carrier saturation velocity implies a higher switching frequency at higher voltages.

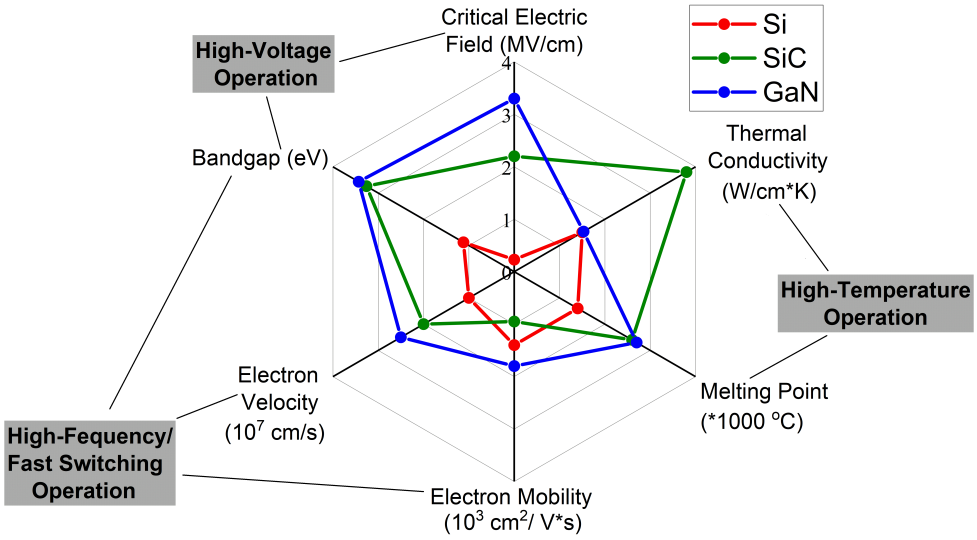

Figure 1.2: *Radar chart of the different physical material properties of Si, SiC and GaN [13, 14].*

Fig. 1.2 provides a comprehensive overview of the key material properties relevant for power electronics. GaN and SiC feature a bandgap approximately 3 times higher than Si which lead to have higher electric breakdown fields and maintain lower intrinsic carrier concentrations, ensuring minimal leakage currents even at elevated operating temperatures. Among all the materials, SiC has the highest thermal conductivity making it suitable for applications demanding high voltage and power handling capabilities. Conversely, GaN emerges as the best choice for high frequency and high current operations since it features the highest electron mobility and carrier saturation velocity. Lastly, for low voltage and frequency applications, silicon remains the preferred choice due to its cost-effectiveness and reliability, despite it has less attractive features for power electronics compared to GaN and SiC. In this thesis, the attention will be focused on GaN devices since research activity have been performed on such technology.

1.2.2 Theoretical Limit: R_{ON} vs V_{BD}

To better compare the performance of different power transistor technologies and evaluating their suitability for a specific application the most appropriate parameters are the breakdown voltage (V_{BD}) and the ON-resistance (R_{ON}) related to the requirements in terms of high blocking voltage capability and low conduction losses, respectively [15]. Such parameters are related each other and their relationships can be analyzed by considering a simple P^+-N

junction [Fig. 1.3(a)]. By applying a positive voltage to the N side, the junction becomes reverse biased and the depletion region expands within the N side (since P^+ region is highly doped) causing the generation of a relatively high electric field. According to the Poisson's equation the electric field is expressed as follows:

$$E_{max} = \frac{qN_D W_D}{\epsilon_0 \epsilon_r} \tag{1.1}$$

where N_D and W_D are the doping concentration and the maximum extension of the depletion region, while,ϵ_0 andϵ_r are the dielectric vacuum constant and the relative dielectric constant of the material, respectively.

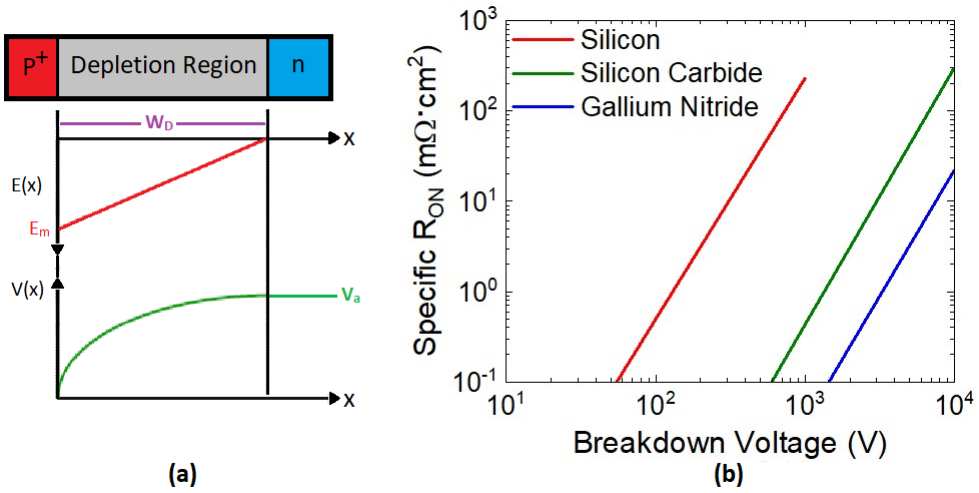

Figure 1.3: *Electric field distribution in a reverse biased P+ /N junction [15] (a) and specific ON-resistance versus breakdown voltage (theoretical limits) of different semiconductor (b) [16].*

At moderate electric filed levels mobile charge carriers entering in the depletion region are accelerated and pushed out with relatively high velocity. If the electric field is relatively high electrons and holes gain enough kinetic energy and colliding with other atoms in the semiconductor lattice can ionize (lose or gain an electron), hence, leading to the formation of additional electron-hole pairs. Such phenomenon is called *impact ionization* which contribute to the increase leakage current through the depletion region but does not necessarily result in catastrophic failure. When the E_{max} approaches to the critical electric field (E_C), the rapid multiplication of electron-hole pairs for impact ionization leads to *avalanche breakdown*, often causing device failure. The occurrence of the latter condition defines the breakdown voltage,

defined as:

$$V_{BD} = \frac{1}{2} E_C W_D = \frac{1}{2} \frac{q N_D W_D^2}{\epsilon_0 \epsilon_r} \tag{1.2}$$

The specific ON-resistance, which is mainly dominated by the resistive component of the N-drift region in on-state operation is equal to:

$$R_{ON,sp} = \rho W_D = \frac{W_D}{q \mu_n N_D} \tag{1.3}$$

Replacing W_D and N_D from Eq. 1.1 and Eq. 1.2 into Eq. 1.3 it is possible notice the mutual dependence between ON-resistance and breakdown voltage::

$$R_{ON,sp} = \frac{4 V_{BD}^2}{\epsilon_0 \epsilon_r \mu_n E_C^3} \tag{1.4}$$

From 1.4 , it can be understood that a trade trade-off exists between achieving low R_{ON} for efficiency and high V_{BD} for robustness, and the choice depends on the specific application and performance criteria. Moreover, since both parameters depends on the intrinsic properties of the materials, the theoretical limits for each semiconductor-based technology can be obtained analytically, as shown in Fig. 1.3 (b). Anyway, the theoretical limit is difficult to reach for any technology since process and design usually leads to higher ON-resistance with respect to the one of the only drift region.

1.3 GaN-Based Technology

Gallium Nitride and its related alloys (e.g. Al_xGa_xN) are promising candites for the next generation of power electronics devices thanks to their attractive material properties which allow them on working under high power and high frequency conditions [12]. As already mentioned, compared with the Silicon counterpart, the wider band gap of these materials make them suitable for high temperature operation thanks to the low leakage current due to the lower intrinsic carrier concentration. Another important feature of GaN is the high critical electric field, hence high breakdown voltage, which make it possible to manufacture smaller devices, lower parasitics (mainly capacitances) which in combination with the high saturation velocity enable higher frequency operation leading to switching losses reduction. Moreover, a smaller device will feature a lower ON-resistance, crucial to achieve low conduction losses, which actually results to be already low thanks to the high mobility of the two dimension electron gas (2DEG) that appears in the AlGaN/GaN heterostructure [17, 18] and works as conductive channel for GaN transistors, namely high electron mobility transistors (HEMTs). The

latter combines the unique properties of gallium nitride and the 2DEG phenomenon to create high-performance transistors that will be discussed along this section.

1.3.1 GaN-on-Si Epi-Stack

In the case of silicon the availability of large size (up to 300mm) and the maturity of process make him a stable, low cost and reliable technology which already reached the theoretical limit. On the contrary, the cost of producing large, high-quality GaN wafers is currently prohibitively expensive and technically challenging, hence their use remains limited to specific niche applications where the benefits of larger wafers outweigh the challenges and costs associated with their production [19, 20]. For these reasons, GaN crystalline layers are typically deposited, by means of compatible semiconductor fabrication processes, on foreign substrates like sapphire, silicon carbide, or silicon which have different lattice constants and thermal expansion coefficients [21]. This situation is usually called heteroepitaxy which makes it easier to lower the costs and to integrate GaN-based devices into existing technology platforms. For AlGaN/GaN materials, techniques like metal-organic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE) are employed to ensure uniformity, crystal quality, and controlled doping [22].

For power applications, silicon is the most used material for the substrates because of its cost-effectiveness and its compatibility with CMOS technology [23]. GaN heteroepitaxy on silicon substrates, however, presents greater difficulties compared to heteroepitaxy on materials like sapphire or silicon carbide. This is primarily due to the substantial disparities in lattice structure and thermal properties, which lead to the accumulation of significant strain in the upper epitaxial layers. Inevitably, if not properly monitored, this situation leads to consequences like the formation of threading dislocation, buildup of strain, performance degradation and reliability concerns [24]. That's why the epitaxial growth process is crucial for creating high-quality GaN layers for exploiting the full potential of this emerging technology.

In Fig.1.4, the layer-by-layer epi-structure of a typical GaN based lateral HEMTs on Si substrate is sketched. The initial step to initiate the epitaxial growth on silicon substrate involves the deposition of an AlN nucleation layer [25, 26]. This particular layer plays an essential role in facilitating the successful integration of the material. Its primary function is to accommodate and alleviate the strain resulting from lattice mismatch, which, if left unaddressed, could cause cracks during the cooling process after the deposition. Notably, GaN epitaxial growth on the AlN nucleation layer exhibits superior quality, yielding a smoother surface morphology that minimizes the

occurrence of defects like stacking faults and threading dislocations, factors that can detrimentally impact the performance of the devices [27].

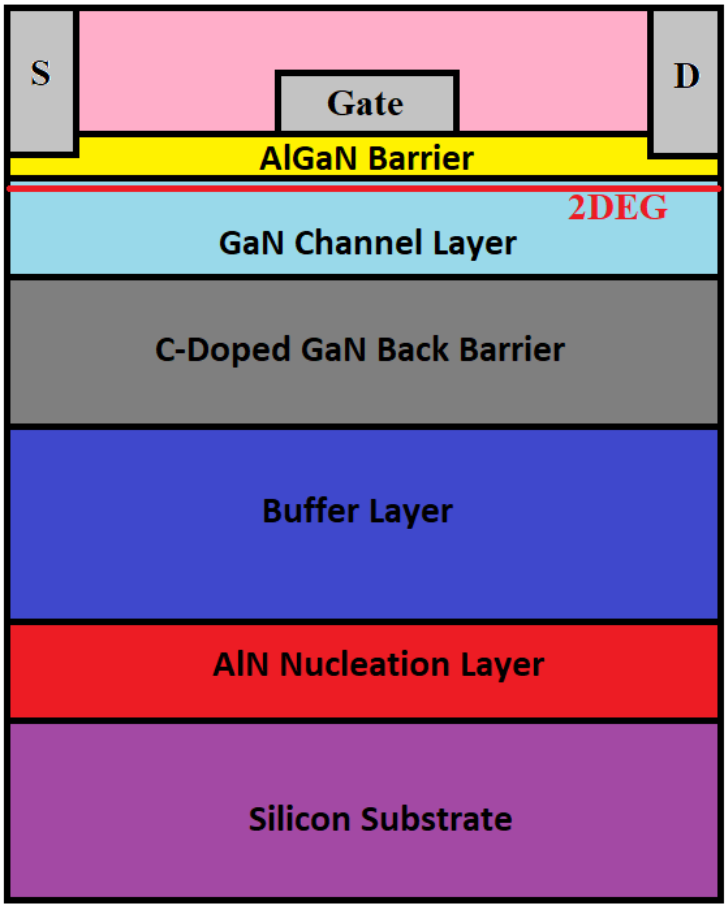

Figure 1.4: *Sketch (not to scale) of a typical GaN-on-Si HEMT epi-stack composition.*

However, when attempting to grow GaN directly on AlN, the process exhibited circular defects, which are likely attributed to silicon outdiffusion from the substrate [28]. These defects could potentially act as stress concentration points, leading to the initiation of cracks. To address this issue, a buffer layer is introduced, playing a vital role in managing and alleviating the strain induced by lattice mismatch. This is crucial for reducing the density of threading dislocations, thus preserving the structural integrity of the GaN layer. Among all the techniques for designing the buffer layer, the most commonly employed method is the utilization of a superlattice buffer. This approach involves the alternating deposition of numerous relatively thin GaN and AlN layers [29]. As the number of these interlayers increases, the final

crystal quality of GaN also improves, enhancing the probability that vertically propagating threading dislocations will eventually annihilate at the interfaces between the multiple layers. This gradual transition allows for the progressive relaxation of strain and minimizes sudden shifts in lattice constants.

On top of the buffer for strain management a layer of GaN doped with carbon is typically used as the back barrier layer, which helps in effectively confining the charge carriers (electrons) within the channel region [30]. This confinement enhances the control of electron movement within the device, resulting in improved transistor characteristics. Moreover, the carbon-doped GaN layer serves to increase the vertical breakdown voltage, to suppress punch-through in the off-state operation and to improve the normally-off operation without changes in the ON-resistance. More details can be found in [31–33].

1.3.2 AlGaN/GaN Heterojunction: 2DEG Formation

The pivotal point of AlGaN/GaN HEMTs is the presence of the high electron mobility 2DEG which naturally appears at the AlGaN/GaN heterointerface [17, 18]. Such phenomenon happens and can be modulated by means of both spontaneous and piezoelectric polarization effects which are related to the polarization of charge within the crystal structure since they can affect band structure, charge distribution and carrier transport properties of the heterojunction, hence device performance.

Spontaneous polarization (P_{SP}) is a physical phenomenon happening along the crystal structure of GaN (or AlGaN) driven by the different electronegativity of Gallium and Nitrogen atoms [17, 18]. As a results, an electric dipole and consequently a built-in electric field is created along the growth direction that leads to the distribution of charges within the crystal structure of GaN (or AlGaN). The orientation of the spontaneous polarization is referred to as "positive polarity" (from Ga to N atoms) and "negative polarity" (from N to Ga atoms) if the bulk is grown as Ga- or N-face, respectively [18].

When two materials with differences in lattice constant are grown one on top of the other one, the lattice adjustment introduces an extra component into the overall polarization known as piezoelectric polarization (P_{PZ}). In particular, the applied mechanical strain or stress at the hetero-structure affect the balance of charges within the crystal. The P_{PZ} point from the region under tensile strain towards the region under compressive strain [17, 18].

In Fig. 1.5 (a), it shown how both polarization are oriented in a Ga-face structure AlGaN/GaN. It is worth noticing that, in this example the P_{SP} and

P_{PZ} (considered only for the AlGaN layer since it is under tensile strain while GaN is relaxed) result to be parallel, so they must be summed up [35]. This means that both of them give contribution to charge distribution within the crystal structure, hence to the formation of the so called Two-Dimensional Electron Gas (2DEG) at the GaN/AlGaN interface and, precisely, in the GaN part.

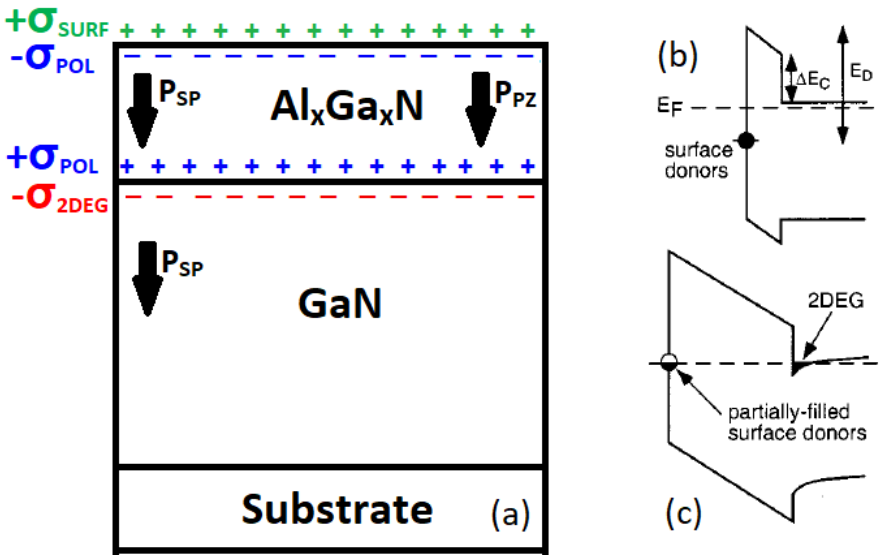

Figure 1.5: *Schematic of charge distribution and polarization orientation within the Ga-face AlGaN/GaN heterstructure (a). Band diagram illustrating the surface donor model with the undoped AlGaN barrier thickness (b) less than, and (c) greater than the critical thickness for the formation of the 2DEG [34].*

Gaining insight into the underlying factors leading to the formation of the 2DEG is crucial for enhancing the electrical characteristics of devices. The confinement of electron in a quantum well in this context arises from a charge compensation mechanism, however, the source of this negative charge has been object of discussion in literature.

Due to the absence of truly n-doping in the AlGaN layer, one of the most plausible physical explanation consists in the presence of donor states located at the surface of AlGaN, which can provide the electrons necessary for forming the 2DEG channel [34]. Consequently, the critical factors influencing the formation and density of sheet charges and, hence, the performance of the GaN-based devices are the thickness of the AlGaN layer and its aluminum content [34–37]. Until reaching a specific thickness known as the critical

barrier thickness [34], the donor energy isn't sufficient to enable the electron transition from an occupied state to an unoccupied conduction band state at the surface, as shown in Fig. 1.5 (b). Once the barrier thickness reaches the critical value, the donor-like states become capable of releasing electrons for the formation of the 2DEG [Fig. 1.5 (c)], leaving behind positive surface charge [σ_{SURF} in Fig. 1.5 (a)]. The AlGaN barrier layer has a strong impact in the 2DEG density and, hence, plays a key role for the performance of the GaN-based devices and in particular on the threshold voltage and ON-resistance.

1.3.3 Commercial GaN Devices for Power Applications

A significant challenge associated with the GaN/AlGaN devices with the previously outlined structure is the persistence of a 2DEG even in the absence of bias. This results in normally-on devices, often referred to as depletion-mode (D-mode) devices [38]. However, in the case of power electronics applications, it is always preferable to have normally-off, also referred as to enhancement-mode (E-mode) devices for the following reasons:

- safety: the normally-on device is always turned on, hence, there is always connection between input and output;
- power consumption: to turn off the normally-on device negative gate voltages must be applied;
- costs: mature technology for normally-off silicon-based MOSFET drivers is already available, and investing in research for new ones can be costly.

Nowadays, different architectures to realize the enhancement-mode (E-mode) GaN products are commercially available. Two of them, namely cascode and direct drive configurations (see Fig. 1.6), are composite devices where a high-voltage D-mode GaN HEMT is combined/integrated with a low-voltage Si-based MOSFET [39–41].

In the case of cascode configuration, the GaN HEMT is indirectly driven by controlling the E-mode MOSFET. The advantage of this technique is to use a low cost and reliable driver for MOSFET already available on the market without any need to redesign another one. On the other hand, the GaN technology potential of working at high frequencies is not fully exploited. A different result can be attained by directly controlling the normally-on GaN device with a driver that switches the gate terminal between zero and negative values with consequent relatively high design cost.

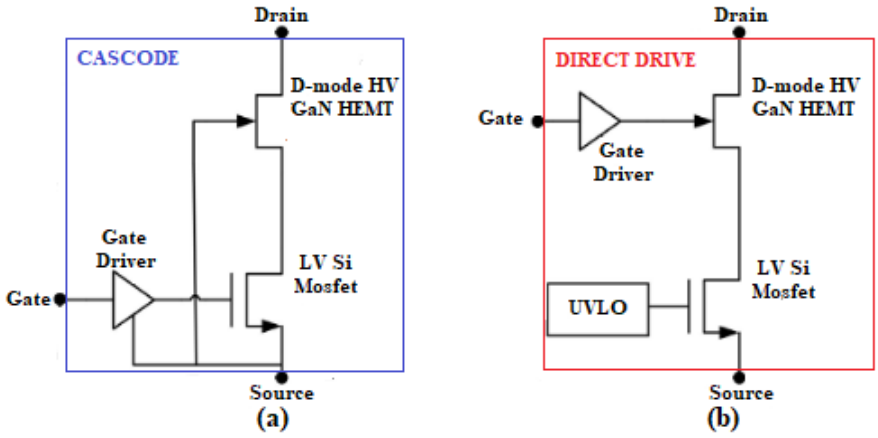

Figure 1.6: *Schematic of (a) Cascode and (b) Direct-drive GaN HEMTs for normally-off operation.*

Anyway, opting for discrete devices is preferred as using two devices would lead to an increase in packaging size and complexity but also to the introduction of parasitics related to interconnection between devices. To do this, many solutions have been proposed in terms of gate design to achieve positive threshold voltage (V_{TH})values [42–45]. Among all of them, Schottky metal to pGaN HEMTs [46, 47] is the only commercialized architecture since results to be the best compromise in terms of stability, reliability and performance [48].

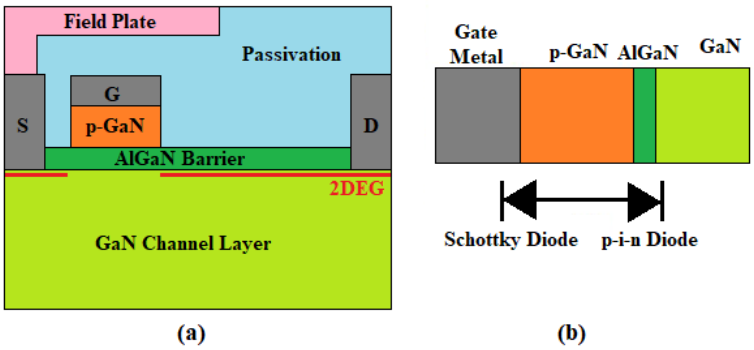

Figure 1.7: *Schematic of a normally-off HEMT with a p-GaN gate (a) and back-to back diode for gate leakage reduction (b).*

Such technology consists in interposing a layer of Magnesium doped (p-type) GaN between the gate Schottky metal and the AlGaN barrier [Fig. 1.7

(a)]. As result of the introduction of the pGaN layer, there is a metal/p-GaN Schottky diode in series with a p-GaN/AlGaN/n-GaN junction [Fig. 1.7 (b)]. Under positive gate voltages the metal/p-GaN diode is reverse-biased effectively reducing the leakage current and, similarly acts the bottom diode under negative gate bias [49]. The presence of such layer pulls up the conduction band of the GaN-channel layer above the eFermi level, leading the depletion of electrons in the 2DEG under the gate at zero bias conditions. By applying a positive gate bias the energy of the electrons at the AlGaN/GaN interface increases so that the conduction band moves closer to the eFermi level forming the 2DEG. Anyway, both the thickness and Al percentage of the AlGaN barrier, as well as the doping level of the pGaN, must be optimized for an efficient threshold voltage positive shift.

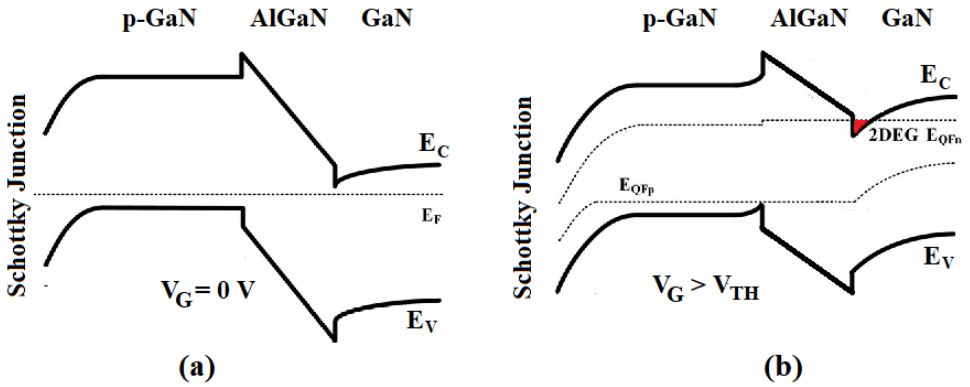

Figure 1.8: *Simulated band-diagram of p-GaN HEMTs along the gate epi-stack for (a) $V_G = 0$ V and (b) $V_G > V_{TH}$.*

1.4 GaN HEMTs Reliability Issues

Apart from delivering excellent performance while minimizing costs, semiconductor power devices must also ensure a high level of reliability in the ever-evolving electronic market. While GaN-based power transistors have demonstrated remarkable performance at competitive costs with respect to Si-counterparts, as emerging technology, reliability remains an important concern that should not to be underestimated.

The primary contributors to the reliability concerns of GaN HEMTs are the effects of charge trapping occurring at different interfaces and within various device layers [48, 50]. Significant trapping phenomena can significantly influence the local electric field and current density, consequently affecting the device's ON-resistance, breakdown voltage, and threshold voltage. Apart

from trapping, other physical processes like impact ionization, electrothermal failure, and the formation of percolation paths can also be responsible for device failures under distinct stress conditions. GaN-based HEMTs are commonly employed in switching mode power converters, where they are subjected to continuous high-frequency state transitions between high-voltage off-state and high-current on-state operations as represented in Fig. 1.9. These demanding conditions expose these devices to various degradation mechanisms that can limit their performance and long-term reliability.

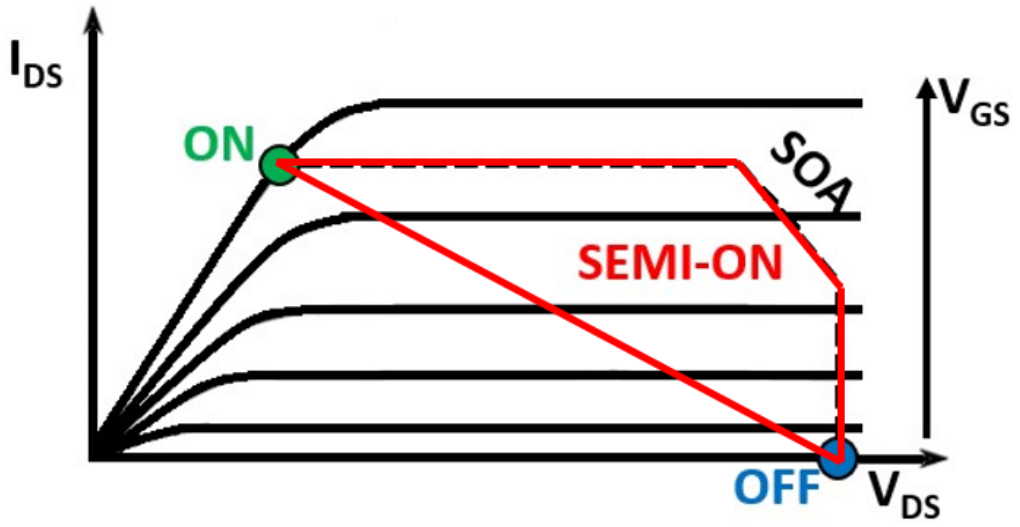

Figure 1.9: *I_D–V_D curve of a hard-switching transition from on- to off-state (and viceversa) with an inductive load.*

When the device operates in OFF-state regime, a relatively high voltage is applied at the drain contact, leading to a high electric field in the gate-to-drain access region as well as vertically across the buffer/transition layers. Such condition may induce to performance instability and/or time-dependent breakdown [51, 52]. More specific, for AlGaN/GaN HEMTS, after the device is exposed to high drain bias, when switched to ON-state, the ON-resistance may result higher than the case of the fresh device which is an undesirable effect for power applications. Such phenomenon is due to charge trapping mechanisms in surface states [53] or in buffer deep levels [54]. Moreover, such operation mode can lead to an unrecoverable breakdown, which is time-dependent and may occur at drain voltages lower than the breakdown voltage evaluated by a DC sweep. The OFF-state breakdown mechanism can occurs vertically (drain to substrate breakdown of the buffer) [55], in the gate-drain region (breakdown of the Schottky junction and the passivation layer) [56, 57]

but also through the GaN channel layer (Drain to Source lateral breakdown) [58, 59].

Furthermore, ON-state bias condition can be induce additional reliability concerns. In order to boost the channel carrier density and, hence, maximize current levels, a large gate overdrive is required for E-mode devices. Consequently, the gate stack is subjected to high electric field across it inducing threshold voltage instabilities and premature failure [60, 61] . In p-GaN gate HEMTs, unrecoverable degradation could be induced by creation of new defects by avalanche multiplication in the depleted region of the Schottky metal/p-GaN junction . Furthermore, while it is ideal for the device to have no voltage drop in the on-state to achieve maximum power transfer and minimize power loss, real devices may exhibit voltage drops in the range of hundreds of millivolts. This can result in substantial power dissipation and self-heating at high operating current levels, potentially affecting long-term operational reliability [62].

Due to parasitics effects (mainly capacitance), in the case of hard switching [as shown in Fig. 1.9], commutations from ON- to OFF-state and vice versa are not instantaneous, i.e., there is time window (few ns) in which the transistors experience both high voltage and high current at the same time which leads to high peaks of dissipated power twice in a switching period. This operational mode is referred to as semi-on-state. The simultaneous presence of high current and high voltage on the drain may favour hot electrons degradation effects, limiting the performance and the lifetime of the device due to charge trapping processes [63–65], .

Given that reliability analysis deals with phenomena which necessitate many years to be identified, accelerated experimental techniques have to be employed for assessing device lifetime and understanding degradation mechanisms within a reasonable timeframe. By utilizing temperature, voltage, current, and humidity as accelerator factors [66], failures can be induced earlier than under normal conditions, and analysis methods/models can then be applied to estimate device lifetime in typical operating modes. This highlights the importance of research in the frame of device reliability issues, as without a thorough investigation into the physical mechanisms responsible for device degradation and failure, reliability predictions can lose their significance.

1.5 Outline of the Thesis

The dissertation is organized as follows:

- Chapter 2 shows the results of an extensive investigation into the long-

term gate reliability of GaN-based power high-electron-mobility transistors with a p-type gate. Three different isolation process options, aimed at improving the time-dependent gate breakdown (TDGB), are proposed and compared by means of constant voltage stress tests performed at different forward gate biases, temperatures, and geometries. In particular, depending on the gate bias and temperature, different lifetime trend have been observed and accurately modeled with two field-acceleration fitting models.

- Chapter 3 is focused on the results obtained thanks to a combined experimental/simulation analysis to study the gate reliability of GaN-HEMTs with p-type gate when subjected to pulse stress conditions. Results show that, in contrast to the DC scenario, additional factors significantly influence TDGB. In addition, after elucidating the fundamental reasons behind gate failures during switching conditions, the chapter investigates how the gate lifetime is impacted by both the switching frequency (ranging from 100 kHz to 1 MHz) and the duty cycle (spanning from 10% to 90%).

- Chapter 4 reports the results of an in-depth analysis of the ON-resistance drift (ΔR_{ON}) induced by storage/release mechanisms occurring in the buffer of GaN-on-Si power devices. The role of both stress condition (bias, temperature, and stress time) and buffer's epi-stack composition on (ΔR_{ON}) has been analyzed by means of back-gating current deep-level transient spectroscopy (I-DLTS). The temperature, stress bias, and stress time dependence of such mechanisms, often overlapping, have been investigated by adopting a genetic algorithm.

- Chapter 5 summarizes the main achievements of this PhD research project.

The research activities presented in this dissertation have resulted in the scientific articles [68], [69], [70], [71] and [72].

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Chapter 2

Time-Dependent Gate Breakdown of p-GaN HEMTs Under DC Stress Conditions

2.1 Introduction and State of the Art

GaN-based Power HEMT's with pGaN Gate technology have aroused a great interest since they promise to dominate the market of semiconductor power devices [1–6]. For this reason, the time-dependent breakdown analysis, in both ON-state and OFF-state conditions, are often used to evaluate the long-term reliability of such devices [7–17]. In particular, many studies report time-dependent gate breakdown (TDGB) analysis under forward gate bias stress [7–12] to investigate the role of the gate stack design and fabrication processes.

In [8, 9], it has been demonstrated that the lower the Mg-doping concentration in the p-GaN layer, the longer the time-to-failure (TTF) indicating an higher robustness to TDGB. In [10] how the TDGB is affected by the AlGaN barrier properties has been reported. In particular, lowering the aluminum content (Al%) and optimizing the thickness of the barrier layer at a given Al% a longer gate lifetime is attained. Furthermore, in [18] it has been demonstrated that a gate leakage component along the gate perimeter causes a premature breakdown. In [11], a lateral etching of the gate metal, namely gate metal retraction (GMR) has been proposed to improve the long-term reliability because of the suppression of perimeter driven transport. In addition, on such devices with the GMR, two temperature-dependent breakdown mechanisms have been found out: i) at relatively low temperatures ($< 80^oC$) failure along the active gate area occurs since both L_G and W_G dependencies

of the TTF have been observed; ii) at higher temperatures ($> 80^oC$), isolation region breakdown is observed showing TTF constant with both gate length (L_G) and width (W_G).

Concerning the TDGB, the choice of an appropriate field acceleration model (TTF vs V_G) is of paramount importance for an accurate lifetime estimation. In [12], Moens et al. compared three different models:

i) $TTF \propto exp(V_G)$ [19];

ii) $TTF \propto 1/I_G$ [7];

iii) $TTF \propto exp(1/I_G)$ [8].

i), also called "E-model", is widely adopted for Time-Dependent Dielectric breakdown (TDDB) studies on S_iO_2 thin films. On the other hand, ii) and iii) are more physical/statical approaches, used for GaN devices, which require a preliminary analysis on the gate leakage and its dependency from V_G [19].

In this chapter, an in-depth high-temperature (T = 150^oC) TDGB analysis of p-GaN HEMTs with the GMR process is presented. Three different isolation process options, designed with the scope of improving the the gate long-term reliability are proposed and compared by means of constant voltage stress tests performed at different forward gate biases, temperatures, and geometries. Experimental evidences show how gate bias and temperature condition influences the localization of breakdown event (along the active gate area or through the isolation region). Furthermore, depending on the kind of breakdown mechanism, two different voltage dependency of the TTF, modeled with different fitting laws, has been observed.

2.2 Device Under Tests

In this study, the device under tests (DUTs) are lateral GaN-based HEMTs with p-type gate, grown on 200 mm Silicon substrate by IMEC. In Fig. 2.1 (a), the schematic of device epi-structure is shown. On top of Si substrate, a 200 nm AlN nucleation layer is deposited. Then, it follows a 1.65 μm (Al)GaN super-lattice layer and a 1 μm C-doped GaN back barrier. The active part of the device is composed of a 200 nm undoped GaN channel layer, a 16 nm thick AlGaN barrier with 23.5% Aluminum (Al) content, a 80-nm-thick p-GaN layer doped with magnesium (with concentration of $\sim 3 \cdot 10^{19}\ cm^{-3}$), and a thin TiN interlayer as gate metal. The latter feature a GMR design, i.e., it is laterally etched with depth of $\sim 130nm$ (Fig. 2.1 (b)). Finally, a passivation composed of a thin layer of Al_2O_3 and a thicker

layer of S_iO_2, is deposited. The isolation between devices is made by means of implantation of Nitrogen atoms (Fig. 2.1(b)). More details on the process steps can be found in [20].

The geometries of the device-under-tests (DUTs) are realized ad-hoc for gate reliability studies. In fact, they feature a symmetric structure with equal gate–to-source and gate-to-drain length ($L_{GS} = L_{GD}$) of 1.5 μm. Different gate lengths (L_G) and widths (W_G) have been characterized to investigate the area and the edges dependence of the time-to-failure.

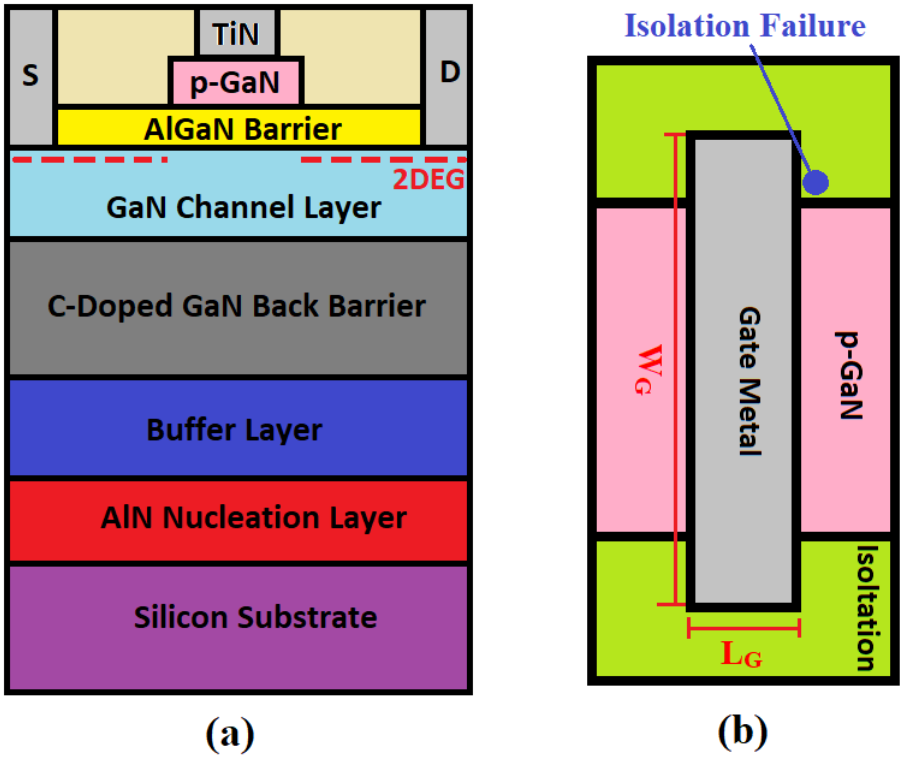


Figure 2.1: *(a) Sketch (not to scale) of the device under tests. (b) Representation of the top-view of the gate region.*

Three different process integration schemes are employed with the objective of enhancing the gate lifetime at high temperatures. Fig. 2.2 illustrates the process integration flows for device isolation. The process splits are:

- Reference: N-implantation after p-GaN patterning and dielectric deposition;
- Split 1: N-implantation prior to p-GaN patterning and dielectric deposition;

- Split 2: N-implantation as Reference, but, before the TiN deposition.

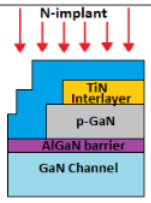
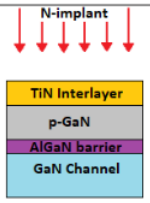
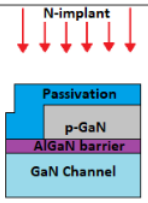
Process step order	 Reference	 Split 1	 Split 2
1	TiN interlayer deposition	TiN interlayer deposition	SiN hard mask deposition
2	P-GaN patterning + gate metal retraction (TiN lateral etch)	AA patterning and N-implant	p-GaN and SiN hard mask patterning
3	Passivation (Al_2O_3 and SiO_2) deposition	P-GaN patterning + gate metal retraction (TiN lateral etch)	Passivation (Al_2O_3 and SiO_2) deposition
4	Active Area (AA) patterning and N-implant	Passivation (Al_2O_3 and SiO_2) deposition	AA patterning and N-implant
5	Passivation etching on top of TiN interlayer (gate region)	Passivation etching on top of TiN interlayer (gate region)	Passivation etching in the gate region (SiN + Al_2O_3 + SiO_2) up to pGaN layer
6	Gate metal stack deposition and patterning	Gate metal stack deposition and patterning	Gate metal stack deposition and patterning

Figure 2.2: *Process flow for three different isolation process options (from the left): Reference process, Split1 and Split2. Note that the process steps 1 is equivalent at the first step after the p-GaN layer deposition.*

2.3 Time-Dependent Gate Breakdown

Time-Dependent gate breakdown analysis has been carried out by means of constant voltage stress (CVS) tests at different gate biases and temperatures, on devices featuring different isolation processes and gate width and length. The activity was performed on devices at the wafer level, employing a probe station and the Keysight B1500A device parameter analyzer. In particular, the test consists on applying a positive bias (a few volts below the breakdown voltage) at the gate contact while monitoring the current over the time until the breakdown occurs [see Fig. 2.3 (a)]. Drain, Source and Substrate contacts are forced to 0V at same time. The time at which the gate current abruptly increases above a threshold value (1mA/mm in this work) is defined as TTF.

For each bias condition, the TTF values are collected and used to build a Weibull plot, as shown in Fig. 2.3 (b). From the Weibull plot, it is possible to extract the value of the shape parameter β which represents the slope of the distribution functions [fitting lines in Fig. 2.3 (b)], and it can give information about the reliability and quality of the process. In particular, the higher the β the smaller the spread on the data which means that the time-to-breakdown is induced by a single degradation mechanism (intrinsic breakdown). On the contrary, a low β value indicates the occurrence of different degradation mechanisms or the poor quality of the device process

is the root cause for premature failure (extrinsic breakdown). Moreover, the Weibull distribution allows to predict the time at which the device has a certain probability of failure (failure rate, F) under a defined stressing condition (bias and temperature).

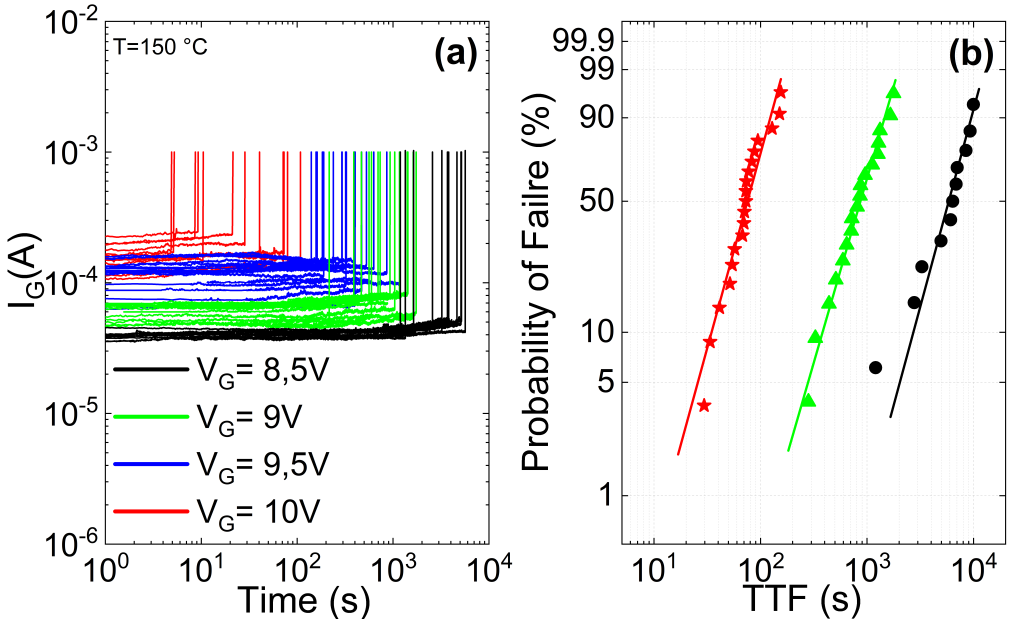


Figure 2.3: *(b) Gate leakage monitored during the CVS tests at VG 8.5V (black line), 9V (green line), 9.5V (blue line) and 10V (red line). (b) Weibull plot of TTF extrapolated from (a).*

By conducting statistical analysis on time-to-failure data under various gate stress biases, it is possible to estimate the lifetime. Fig. 2.4 reports a comparison of the lifetime of devices fabricated with the three different process options (Fig. 2.2) while maintaining identical gate geometries ($W_G = 100\mu m$ and $L_G = 0.8\mu m$). The test temperature is 150 °C and the TTF are extrapolated with F= 1%.

A double V_G dependency is observed in the lifetime plot, suggesting different breakdown mechanisms. In particular, two different field acceleration (TTF vs V_G) fitting laws have been employed: as will be discussed in the subsections 2.3.1 and 2.3.2, a simple "E-model" provides a good fitting when the damage occurs along the active gate area, whereas, a "$TTF \propto exp((1/I_G)$" is more suitable in the case of breakdown through the isolation region, i.e. the region where the gate finger intersects the N-implanted area [see Fig. 2.1 (b)].

Overall, as depicted in Fig. 2.4, it is evident that devices manufactured

using the Split 2 process exhibit poor gate robustness, with a maximum allowable gate voltage for a 10-year lifetime of approximately 4V. On the contrary, devices featuring the Reference and Split 1 processes exhibit an extended lifespans, since they can withstand at least 7V on the gate guaranteeing a lifetime of 10 years when subjected to temperatures of 150^oC.

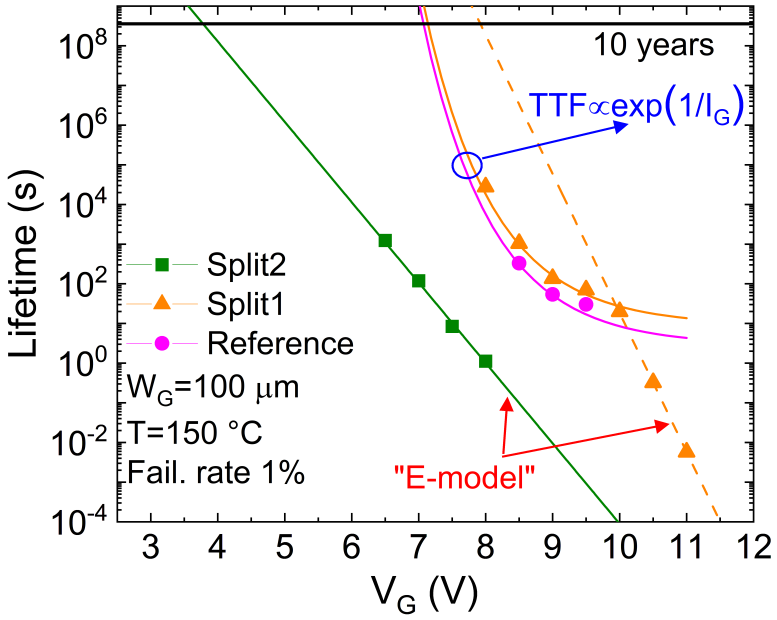


Figure 2.4: *Lifetime comparison between Reference, Split 1, and Split 2 isolation process options. Depending on the kind of breakdown mechanism, if area- or isolation-related, the TTF is fit with the "E-model" or with the "$TTF \propto exp(1/I_G)$" model, respectively. Failure criterion: 1% of failure at 150^oC extrapolated from the Weibull plots.*

2.3.1 Gate Area and Edges Dependency

In order to investigate the underlying factors responsible for the various trends in time-to-failure with V_G observed in Fig. 2.4, as well as the associated breakdown mechanisms, an analysis on the gate area and perimeter dependencies has been conducted. These analyses were carried out on devices that incorporated different isolation process alternatives.

In Fig. 2.5, it is possible to notice that the time-to-failure of the devices under test that have been isolated using Process Split 2 exhibits dependencies on both (a) the gate width and (b) the gate length. If increasing the gate width or the gate length, a larger gate area is attained and, the larger is the surface exposed to relatively high electric field the higher is the prob-

ability of failure of that region, hence, its robustness is lower. This is likely attributed to the deposition of the SiN hard mask layer directly on top of the the p-GaN layer, followed by its subsequent removal before the deposition of the gate metal stack. This process can lead to the formation of highly defective Schottky junction, eventually resulting in premature failures (shortened device lifetime) that are dependent on the gate area.

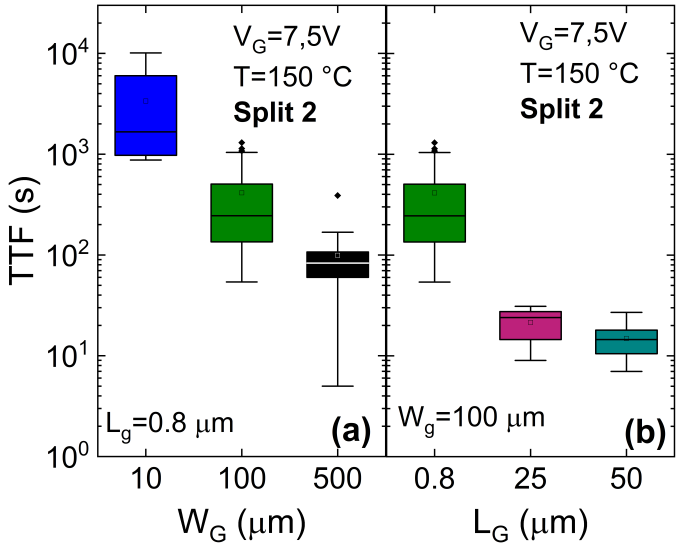


Figure 2.5: *a) Gate width and (b) gate length dependency of the TTF at V_G = 7.5 V and $T = 150^oC$ for devices fabricated with the process Split 2. About 16 devices per group have been stressed. TTF scales with both W_G and L_G..*

In contrast, by observing Fig. 2.6, it can be noticed that the TTF does not exhibit any dependence on either gate area or perimeter, as can be seen in both the Reference (a) and Split 1 (b) processes, as it remains constant with respect to W_G. This absence of area and perimeter dependency implies that the breakdown is occurring in a more localized position, specifically in the region where the gate finger intersects with the isolation region [as illustrated in Fig. 2.1 (b)]. Such statement is confirmed by observing the image of a device after the gate breakdown [11] in Fig. 2.7. It is worth noticing that a black spot is present in the isolation region, which indicates a material damage due to relatively high currents.

Although both process isolation options exhibit a similar mean-time-to-failure (MTTF) (as depicted in Fig. 2.6), their TTF distributions differ, as evident in the insets of Fig. 2.6 (a) and (b). Specifically, the Reference process shows a worse distribution, leading to a lower Weibull slope (equal to 1.5 instead of 2.5 as observed for Split 1). Consequently, this results in a shorter

TTF extrapolated at F=1% (such behavior has been consistent across all gate voltages used for the CVS tests). As a result, the maximum extrapolated applicable gate voltage for ten years of lifetime is slightly lower, as shown in Fig. 2.4. Such difference might be ascribed to shallower and less uniform implant at the gate edge, and/or to possible damages of the passivation caused by the N-implant in the case of the Reference process. Differently, a uniform N-implant is expected for the Split1 and the possible dielectric damage is completely avoided since it is deposited after the implantation.

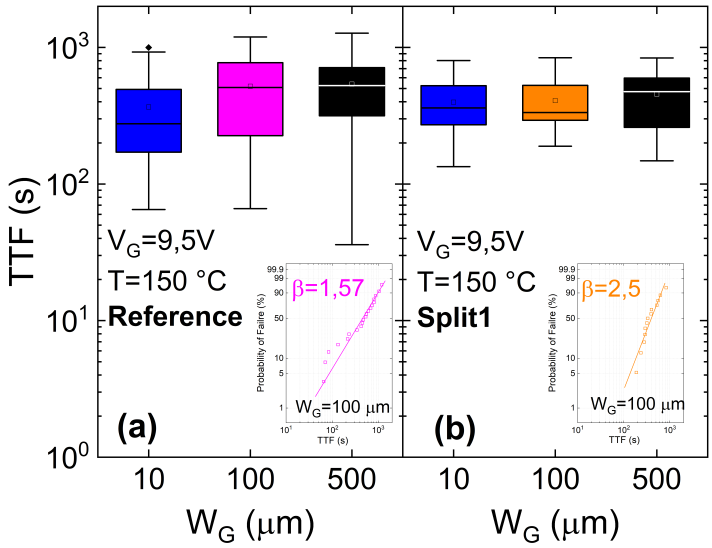


Figure 2.6: *Gate width dependency of the TTF at V_G = 9.5 V and T = 150°C for devices fabricated with (a) Reference and (b) Split 1 process option.In both cases, TTF does not scale with W_G. The insets show the Weibull plot of devices featuring W_G = 100 µm. Different TTF distributions (Weibull slope β) are observed.*

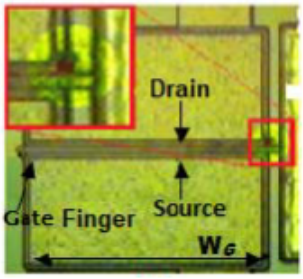


Figure 2.7: *Optical microscopy image after the isolation region failure shown for the first time in [11].*

Given the higher reliability observed with the Split1 isolation process, a more in depth analysis was conducted. Fig. 2.8 shows the lifetime plot for devices featuring different W_G ($10\mu m$, $100\mu m$ and $500\mu m$).

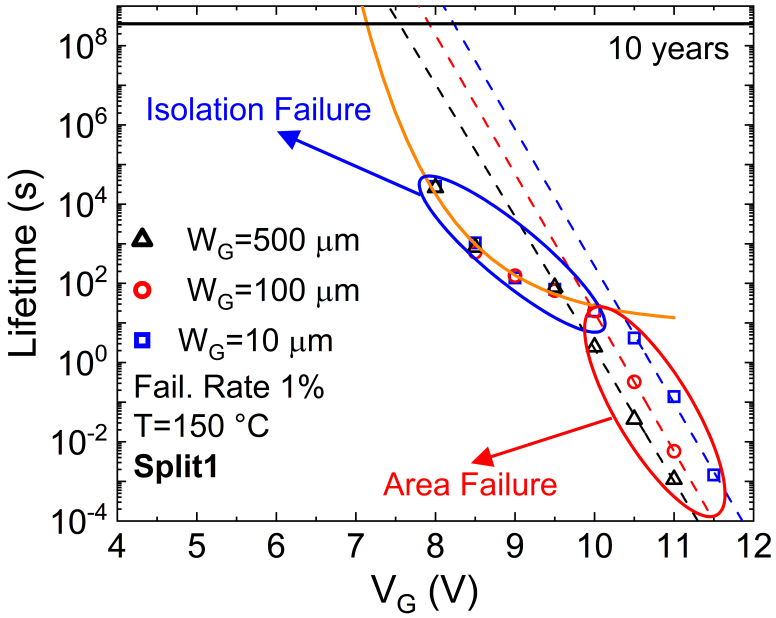


Figure 2.8: *Lifetime plot in the case of Split 1 process on devices with three different gate widths (W_G). Different V_G dependencies of the TTF, ascribed to different failure mechanisms, are observed. Failure criterion: 1% of failure at 150^oC extrapolated from the Weibull plots, with slope $\beta \sim 2.5$ (not shown).*

It is evident that the time-to-failure exhibits a dual dependency on gate bias stress, indicating the occurrence of two competing failure mechanisms. When the gate voltage is relatively low, isolation failure is the predominant mechanism, as evidenced by the nearly identical extrapolated TTF values at F=1% for devices with different W_G, as shown in Fig. 2.8 (referred to as isolation failure). Conversely, at higher gate voltages, an area dependency is observed. As expected, a wider gate area leads to a lower V_G at which isolation breakdown shows up, e.g., 10.5 V and 10.0 V for DUTs featuring W_G of 10 μm and 100 μm, respectively. This phenomenon is attributed to the increased probability of failure across a wider gate area.

In a previous study [11], it was suggested that the exponential rise in TTF at V_G=8 V, in comparison to V_G=8.5 V, might be linked to a potential switch in the underlying failure mechanism. In the current research, through the implementation of long-term Constant Voltage Stress tests on devices with different gate widths, it can be confirmed the absence of area dependency

even at relatively low stress voltages. This observation implies that the isolation breakdown continues to occur. Consequently, as will be explained in the next subsection (subsection 2.3.2), it is evident that the "E-model" is not suitable for fitting the relationship between TTF and V_G when the failure is associated with the isolation region.

2.3.2 Field Accelerated Fitting Models

Two models have been utilized to estimate TTF vs V_G trends, enabling the extrapolation of lifetimes associated with both the gate area and isolation. In the first scenario, a good fitting has been attained using an "E-model" (also referred to as a "V_G-model"), which follows the exponential relationship:

$$TTF \propto exp(V_G) \tag{2.1}$$

The E-model is intrinsically developed for area-dependent breakdown since it is based on the percolation theory characterized by a probability of failure which increases with the gate area [21], thus, suitable in this case.

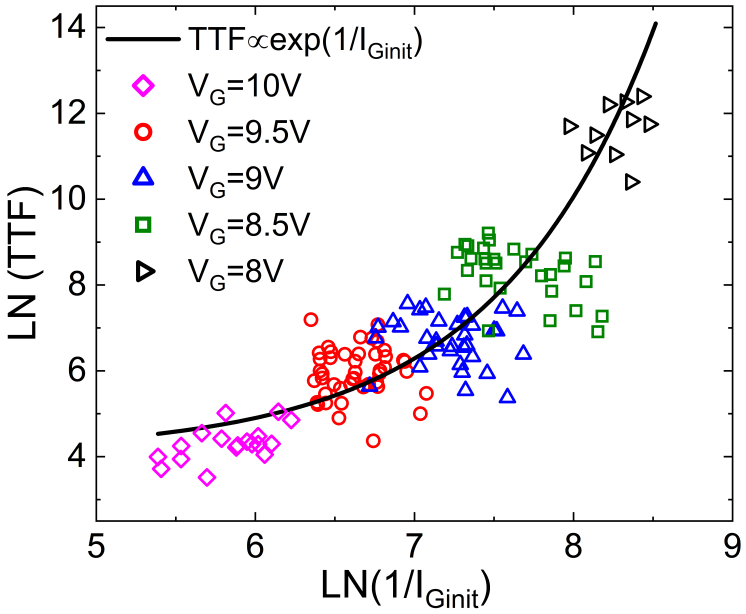


Figure 2.9: *Correlation between the inverse of the initial gate leakage current (I_{Ginit}), monitored at the beginning of CVS tests, and the TTF, in the case of Split 1. An exponential relationship has been identified [8] by means of a statistical analysis at $T = 150^oC$.*

In scenarios involving more localized failures, like those occurring in the isolation region, a connection has been established between the time-to-failure and the initial gate leakage measured at the beginning of the CVS tests, when the devices are considered still fresh. As shown in Fig. 2.9, the following exponential relationship between TTF and I_{Ginit} has been observed, consistent with findings reported in [8]:

$$TTF \propto exp(1/I_{Ginit}) \tag{2.2}$$

Although the gate leakage at higher V_G levels is predominantly influenced by an area-related component, it can be deduced from the robust connection between TTF and I_{Ginit} that a portion of the gate current, potentially exhibiting a similar dependence on gate voltage, plays a role in causing damage in the isolation region. Hence, as the gate leakage increases, the proportion of current responsible for initiating isolation breakdown also increases, leading to a shorter TTF.

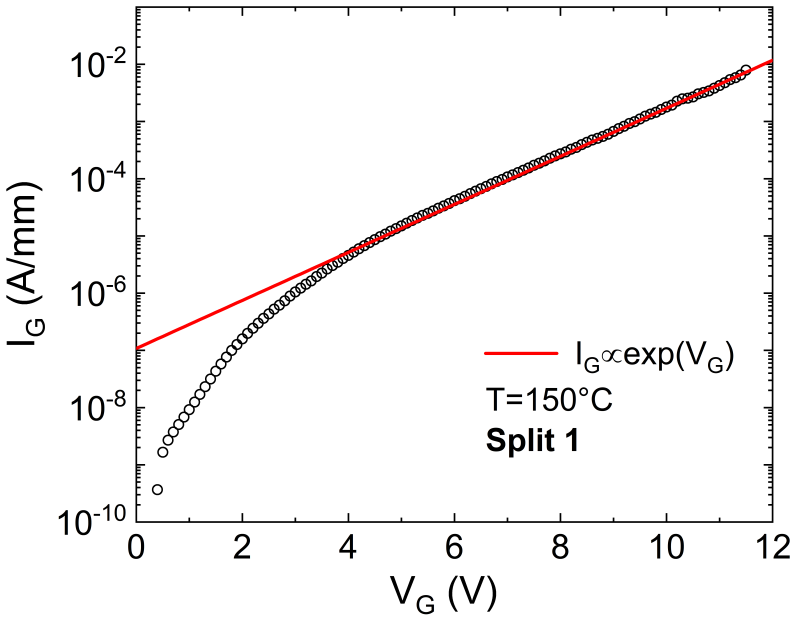


Figure 2.10: *Measured gate leakage characteristics (symbols) and fitting model (line) at $T = 150^oC$ in the case of Split 1. For $V_G \geq 4V$, the gate current shows a purely exponential dependency.*

Afterwards, the relationship between the gate leakage and the gate voltage has been determined by analyzing the characteristics reported in Fig. 2.10. For the DUTs, an exponential law has been adopted to reproduce I_G for

relatively large V_G values. In particular, for $V_G \geq 4V$, I_G can be modeled as follows:

$$I_G \propto exp(V_G) \tag{2.3}$$

In conclusion, the empirical model can be obtained by simply substituting Eq. 2.3 into Eq. 2.2. From Fig. 2.11, it is possible to notice that the model is in agreement with the Mean Time to Failure for V_G values below 10 V, which corresponds to the bias range predominantly influenced by isolation breakdown. In order to fit the TTF at F=1%, a multiplicative constant ($k < 1$) was introduced.

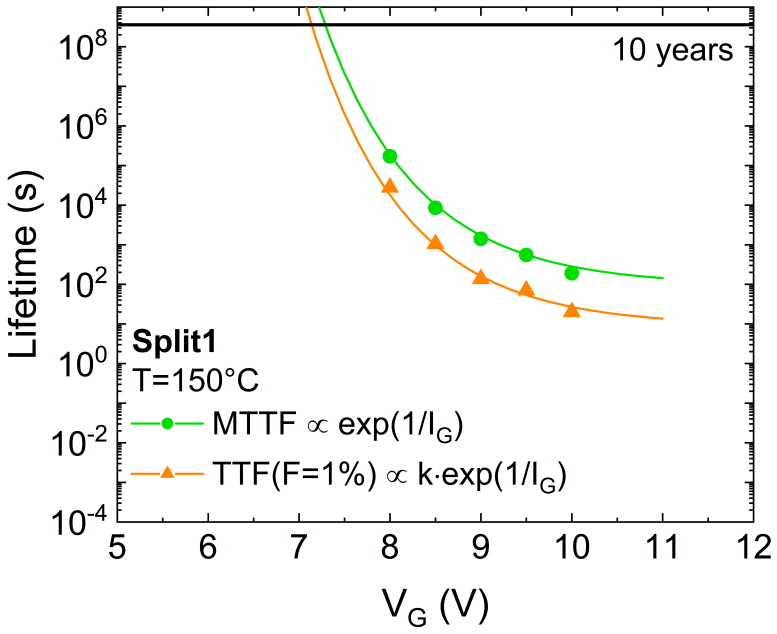


Figure 2.11: *Lifetime plot comparison in the case of the TTF extrapolate with F = 1% (triangles) and the mean time-to-failure (MTTF) (circles). The process is Split 1 and the temperature is* 150^oC*. To better fit the TTF at F = 1%, the empirical model has been multiplied by a constant* $k < 1$.

2.3.3 Temperature Dependency

Fig.2.12 shows the temperature dependency of the time-dependent gate breakdown at V_G= 9.5V on devices featuring three different gate widths ($10\mu m$, $100\mu m$ and $500\mu m$). A different T-dependency can be observed, depending on the failure mechanism.

At relatively low temperatures, an area-dependent TTF can be observed (TTF scales with W_G). Furthermore, TTF exhibits an increase with temper-

ature, demonstrating a positive temperature dependence. These two observations together suggests and confirm that the root cause of the gate failure is the impact ionization, in the high-field depletion region of the Schottky junction [10], [22]. In particular, holes generated by impact ionization in such region are accelerated towards the AlGaN barrier, acquiring kinetic energy and possibly inducing the creation of new structural defects, in addition to pre-existent ones, in the AlGaN barrier layer. For more in-depth insights into the degradation mechanisms occurring at lower temperatures see [10].

On the contrary, at relatively high temperature a negative T-dependency and a lack of area-dependency can be observed. By increasing the temperature, the impact ionization mechanism is exponentially attenuated, reducing the probability of failure along the gate area. Consequently, the mechanisms triggering isolation failure becomes predominant, featuring an activation energy of ~ 0.14 eV.

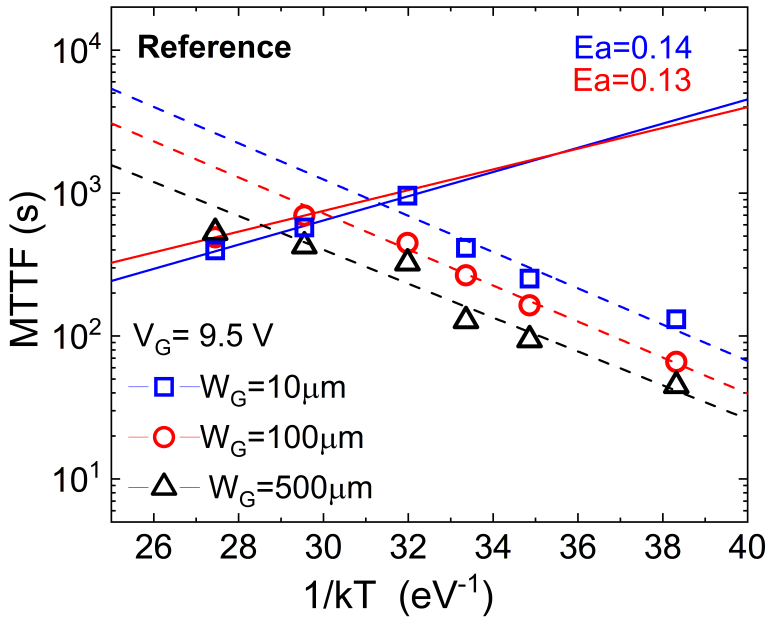


Figure 2.12: *Arrhenius plot at V_G = 9.5 V showing the MTTF of devices featuring three different gate widths (W_G): 10, 100, and 500 µm. The fitting dashed and solid lines are referred to the area failure and isolation region failure, respectively. The isolation process option is the Reference..*

Finally, as expected, the temperature at which the transition occurs from gate area failure to isolation failure is area dependent. A larger gate area corresponds to a lower transition temperature. By increasing the gate area, the probability of failure along it increases as well, therefore, a higher tem-

perature is required to further mitigate the underlying cause responsible for gate area breakdown, i.e. impact ionization. More specifically, single-finger devices with gate widths of 10 μm and 100 μm, subjected to V_G=9.5V, exhibit area-related failures occurring at temperatures below 90 °C and 120 °C, respectively. Finally, for devices featuring a W_G of 500 μm, isolation breakdown at V_G=9.5V has only been observed at a temperature of T=150 °C.

2.4 Conclusions

In this chapter, an extensive analysis of the high-temperature time-dependent gate breakdown of p-GaN HEMTs has been reported. Three isolation process variations, designed to enhance the robustness of the isolation region (i.e. where breakdown occurs), have been compared by performing constant voltage stress tests on devices with different gate areas. Results showed that, depending on the process and on the stress conditions (Temperature and gate bias), DUTs can experience either irreversible breakdown along the active gate area or within the isolation region.

The process Split 2, which consists in patterning the pGaN layer, depositing the passivation, carrying out the nitrogen implantation, removing the passivation and depositing the TiN metal, turned out to be less robust, showing an area related gate breakdown. Possibly, the deposition of the passivation directly on top of the pGaN and the subsequent etching prior to TiN metal deposition, introduces many surface defects making the Schottky junction highly defective. In fact, by adopting a similar procedure, but depositing the TiN interlayer directly on top of the pGaN before passivation (Reference), a more robust gate region is attained. However, the adoption of higher gate voltages with respect to Split 2, gives rise to time-dependent isolation breakdown. The latter can be slightly improved by adopting process Split 1, which consists of implanting directly through the TiN interlayer prior to patterning and passivation steps. Such a procedure ensures a uniform N-implant and avoids possible damage to passivation.

Concerning the two breakdown mechanisms and their dependency on test conditions the following results have been obtained:

- Depending on the stressing gate bias range one failure mechanism is dominant with respect to the other one. In fact, for relatively high gate voltages area-dependent failure occurs, whereas, at lower voltages isolation breakdown shows up.

- Concerning the appearance of the two different breakdown mechanisms

(area and isolation related), the adoption of different acceleration laws has been suggested to model their voltage dependency. In particular, the TTF related to the gate area can be fitted with a simple "E-model", whereas an empirical approach is needed in the case of failure at the isolation region, emphasizing the detrimental role of the gate leakage.

- The gate time-to-failure exhibits a non-monotonic temperature dependency at a given gate bias. Specifically, positive and negative T-derivatives correspond to active gate area and isolation region failures, respectively. The decreasing and increasing trend of TTF with the temperature has been observed at relatively high and low temperatures, respectively. The temperature threshold value at which the shift of the localization of failure is observed strongly depends on the gate geometry, i.e., a wider area necessitates a higher temperature for isolation breakdown to show up. The latter feature an activation energy approximately of 0.14 eV.

In this study, devices with scaled dimensions (ranging from W_G 10 μm up to 500 μm) were employed. However, the potential for isolation breakdown is not limited to scaled devices and is a noteworthy concern for conventional power devices as well. This is due to the typical multi-finger structure of power devices, which consists in splitting a wider gate region (100 mm for instance) into multiple fingers in parallel, inducing a smaller area occupation. Consequently, the probability of isolation breakdown increases with the greater number of gate fingers in the structure as observed in [11]. One potential solution can involve the use of wider gate fingers, but this comes with the potential drawback of significantly reducing the gate lifetime.

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Chapter 3

Gate Reliability of p-GaN HEMTs Under Pulsed Stress Conditions

3.1 Introduction and State of the Art

As anticipated in Chapter 1, the reason why AlGaN/GaN High Electron Mobility Transistors (HEMTs) are so attractive for power application is due to their suitability for high-voltage and high-power applications thanks to their capability to operate at relatively high frequency with higher efficiency when compared with their Silicon-based counterpart [1–4].

A Magnesium-doped (p-type) GaN layer placed between a gate metal and an AlGaN barrier layer emerges as an optimal choice for normally-OFF operation, offering exceptional performance, stability, and cost-effectiveness [5–8]. Yet, concerns about performance and reliability stem from the complexity of the back-to-back diodes composing the gate structure since, the semi-floating potential of the p-GaN layer can trigger charging and discharging processes within the metal/p-GaN/AlGaN/GaN epitaxial stack.

For these reasons, many challenges have been faced in finding experimental methodologies and physical-statistical approaches to better evaluate the gate reliability [9–23].

Many papers reported how fast transient and/or pulsed stress/characterization may induce threshold voltage shifts (ΔV_{TH}) [10–16]. In [13], it was demonstrated that fast-dynamic forward gate stress can result in frequency-dependent positive (ΔV_{TH}). Such behavior has been attributed to carrier injection/emission in/from the p-GaN layer or the AlGaN barrier layer. Tang et al. [14] observed positive threshold voltage shift ascribed to trapping of

electrons, coming from the 2DEG through the AlGaN barrier, in the p-GaN layer. The latter results to be negatively charged until the electron de-traps after a certain relaxation time under zero bias condition.

In [15], a fully recoverable ΔV_{TH} hysteresis under fast sweeping characterization has been reported. In particular, the sweeping time was found to be crucial for threshold voltage shift, i.e., the longer the sweeping time the higher the positive V_{TH} shift. In [16], such phenomena has been accurately reproduced by means of TCAD modeling. Thanks to this analysis, the dynamic threshold voltage shift has been attributed to time dependent charging/discharging processes in the floating p-GaN layer, which are ruled by the balance of both the Schottky diode (metal/p-GaN) and p-i-n diode (p-GaN/AlGaN/GaN) leakage currents.

As any technology attracting attention due to its widespread use, it is essential to evaluate its reliability, as far as possible, under operational conditions similar to those experienced in a real-world application.

While the time-dependent gate breakdown (TDGB) under static stress condition has been largely analyzed for this technology [17–22], only few papers report TDGB analysis under pulsed stress condition. The latter is of paramount importance since, in switching power applications, e.g. a power converter, the GaN transistor's gate is repeatedly switched, at relatively high frequency, between relatively high (ON-state) and low voltage values (OFF-state).

In [23], the Mean Time to Failure (MTTF) of the gate has been investigated under pulsed stress tests in a frequency range between 10 kHz and 100 kHz. Experimental evidences shows that, under such conditions, the gate robustness is weakly affected by the switching frequency.

In this chapter, the time-dependent gate breakdown under dynamic stress condition has been investigated for higher frequencies (up to 3.3 MHz). More specifically, this work aims to investigate which are the AC signal features (e.g. ON-time, OFF-time, rise/fall time, etc.), applied to the gate terminal, causing irreversible failure. Experimental results combined to TCAD simulations highlight reliability aspects which could not be identified by DC stress analysis.

Once the root cause limiting the p-GaN HEMTs gate reliability under pulsed condition are established, the analysis is extended by exploring different switching frequencies and duty cycles. Furthermore, the lifetime extrapolated by means of AC-stress performed at different gate voltages is compared with the DC case, highlighting aspects which are important for both technology manufacturers and GaN-based circuits designers.

3.2 Analysis Details

3.2.1 Device Under Test

Devices under test (DUTs) are Schottky metal to p-GaN gate HEMTs grown by metalorganic chemical vapor deposition (MOCVD) on a 200mm GaN-on-Si substrate by imec. The epi-stack and gate design are the same of the structure shown in the previous chapter (Fig. 2.1) but with different dimensions. In particular, the transition layer consists of a 200 nm thick AlN nucleation layer, a 0.33 μm (Al)GaN superlattice layer and a 0.5μm C-doped GaN back barrier. On top of it, the heterojunction is realized by a 200nm unintentional doped GaN channel layer and a 16-nm thick AlGaN barrier with 23.5 Aluminum (Al) content. Finally, an 80-nm thick p-GaN layer doped with a Magnesium concentration of $\sim 3 \cdot 10^{19}\ cm^{-3}$, followed by metal forms the Schottky gate junction. The DUTs, designed ad-hoc for gate reliability analysis, feature a symmetrical structure with equal gate-to-source and gate-to-drain distance ($L_{GS} = L_{GD}$) of 1.25 μm. The gate width (W_G) and length (L_G) are 10 μm and 0.5 μm, respectively. The gate breakdown voltage is $\sim$ 11 V. Also in this case, the examined structures consist of devices at the wafer level.

3.2.2 Experimental Setups

In Fig. 3.1, it is shown the schematic of the experimental setup realized for time-dependent gate breakdown analyses under pulsed stress condition.

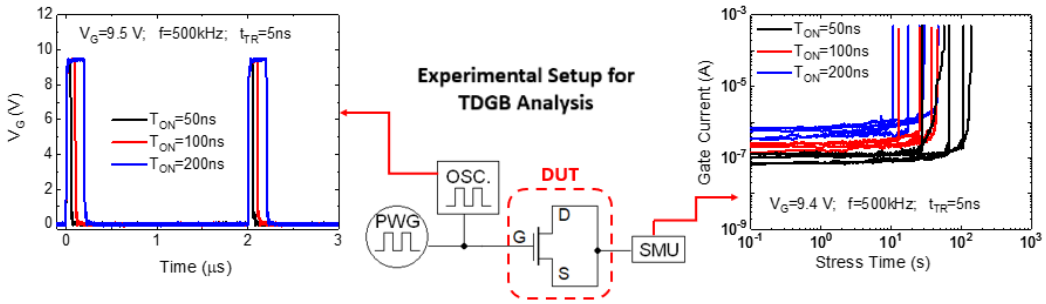

Figure 3.1: *Schematic of the experimental setup for time-dependent gate breakdown analysis under pulsed stress conditions.*

In particular, consecutive square-waves are applied at the gate contact by means of a Pulse Wave Generator (PWG), while the source and drain contacts are shorted through a Source Measure Unit (SMU) which forces their

potential at 0 V. From the SMU the gate leakage current is indirectly monitored to detect the gate time to failure (TTF), defined as the time at which the current abruptly increases above 1 mA. The test conditions adopted in this activity were chosen with the sole purpose of study the robustness and the reliability of the device gate stack when subject to a combination of relatively high temperature and gate bias, defined as Time Dependent Gate Breakdown test. With respect to DC stress, the pulsed one is significantly more similar, but not identical, to device operation in a real switching application. In the latter, the drain terminal is not shorted to source, or forced to the same potential, but it can switch between low bias/high current and high bias/low current regime. However, this is a completely different stress condition uncovered by this study, which could potentially introduce different degradation effects. Moreover, it is worth noting that device under tests have been properly developed for gate reliability analysis, featuring symmetrical structure (L_{GD}=L_{GS}) and do not have source field plates, extremely necessary to modulate the electric field under the gate region (extended towards the drain) in presence of high drain voltages. As a result, the application of a drain voltage, different from the source one, would not replicate a realistic operating condition.

The applied gate signals during the tests are monitored with a high-resolution digital oscilloscope connected at the gate contact (together with the PWG) to monitor the applied signals during the tests. Thanks to appropriate 50 Ohm impedance matching and control of parasitics, the measured waveforms do not show any significant voltage overshoot/spike in the considered frequency ranges.

The experimental results are analyzed in terms of:

- mean time-to-failure (MTTF) extrapolated with an arithmetic average on the time-to-breakdown of 7-15 devices;
- mean number of pulses necessary to reach the breakdown, defined as: Mean N^o of Pulses = MTTF/Period;
- mean Total ON-Time, i.e. the total time in which the device is in ON-State before the breakdown (Mean N^o of Pulses*t_{ON}).

To sense the current peaks at the transition phases, an additional experimental setup has been employed. As before, a square waveform is applied at the gate contact while the drain and the source contacts are shorted. Here, the current flows through a 27.7 Ω shunt/sensing resistor and the voltage drop across it is monitored by means of a high-resolution oscilloscope (see Fig. 3.2).

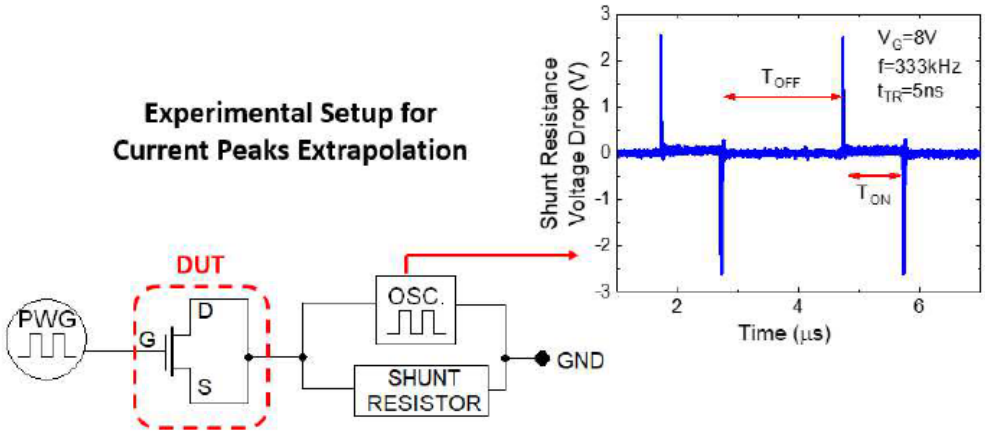

Figure 3.2: *Schematic of the experimental setup for current peaks extrapolation at the transition phases.*

For the scope of this work, the applied square-waves at the gate terminal feature different ON-Time (t_{ON}), OFF-time (t_{OFF}) and rise/fall time (or transition time t_{TR}), while the amplitude (V_G) is 9.4 V and 8V for the TTF and current peaks extrapolation, respectively. The temperature is fixed at 150° C for all the experiments, as it represents the maximum operating junction temperature for commercial GaN-based FETs.

3.2.3 TCAD Modeling

Sentaurus Technology computer-aided design (TCAD) has been adopted to support the experimental evidences. The structure in Fig. 2.1 was reproduced using 2-D geometric structures with the Sentaurus Structure Editor tool. The dimensions of the various layers are described in subsection 3.2.1. Then, Sentaurus Device simulation tool has been employed to simulate the electrical characteristics of the device in response to the external electrical and thermal conditions as those imposed during the experimental test.

Both acceptor and donor states have been introduced in specific regions to calibrate as better as possible the device currents. In particular, acceptor states with concentration of $5 \cdot 10^{18} cm^{-3}$ at 0.9 eV from the valence band (VB) in the C:GaN layer, which is similar to carbon concentration adopted during the epitaxial growth, have been introduced. In addition, donor traps with concentration of $2 \cdot 10^{18} cm^{-3}$ at 0.4 eV from the conduction band in the C:GaN layer have been used to replicate the generation of such trap states due to the presence of carbon atoms occupying gallium sites. Moreover, donor traps were inserted at the interface between the AlGaN barrier and

the passivation layer, uniformly distributed starting from the middle of the bandgap with a concentration value equal to $5 \cdot 10^{15} cm^{-3} eV^{-1}$.

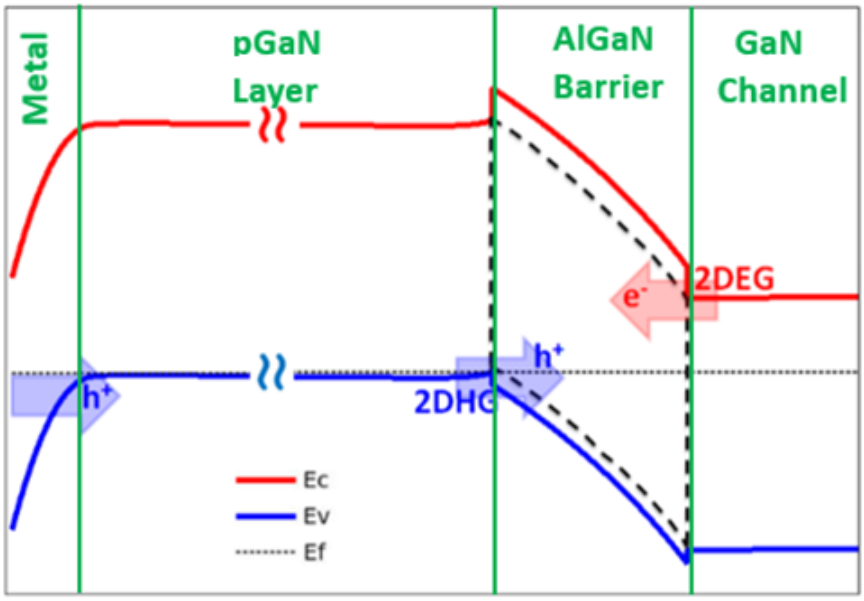

Figure 3.3: *Schematic of band diagram Simulated band diagram of the gate epi-stack at $V_G = 0$ V. Moreover, the tunneling component and the spatial and energy window of the acceptor traps uniformly distributed in the AlGaN barrier layer (dashed line) are sketched.*

In the case of HEMTs with p-type gate, the modeling of the gate leakage is of paramount importance, given its significant influence on the devices' threshold voltage [24]. More precisely, the balancing between the leakage components of the metal/p-GaN Schottky diode and the p-GaN/AlGaN/GaN (p-i-n) junction, determines the charging state of the semi-floating p-GaN layer. For this reason, nonlocal tunneling models [25] in combination with thermionic emission contributions have been adopted and defined for both junctions. In Fig. 3.3, the schematic of band diagram at $V_G = 0$ V is reported. In particular, hole tunneling has been activated and calibrated at the Schottky gate contact to reproduce the injection of holes from the metal into the p-GaN valence band. On the other hand, nonlocal trap assisted tunneling (TAT) has been used to model the leakage current through the AlGaN barrier. In particular, acceptor traps, with concentration $2 \cdot 10^{18} cm^{-3} eV^{-1}$, have been placed in the AlGaN barrier (spatial and energy window of the acceptor are represented by dashed line in Fig. 3.3) and coupled to nearby interfaces by tunneling. Such TAT is allowed for both electrons and holes coming from 2DEG (two-dimensional electron gas) and 2DHG (two-dimensional

hole gas), respectively, and includes both inelastic phonon assisted and elastic processes. More details about the adopted models and calibration can be found in [16].

3.3 The Role of the t_{ON}, t_{TR} and t_{OFF}

Fig. 3.4 shows the mean time-to-failure as a function of t_{ON} for two fixed t_{OFF} values, 250 ns and 5 μs. In the first case, the MTTF increases with t_{ON}, whereas an opposite trend is observed with $t_{ON} = 5$ μs.

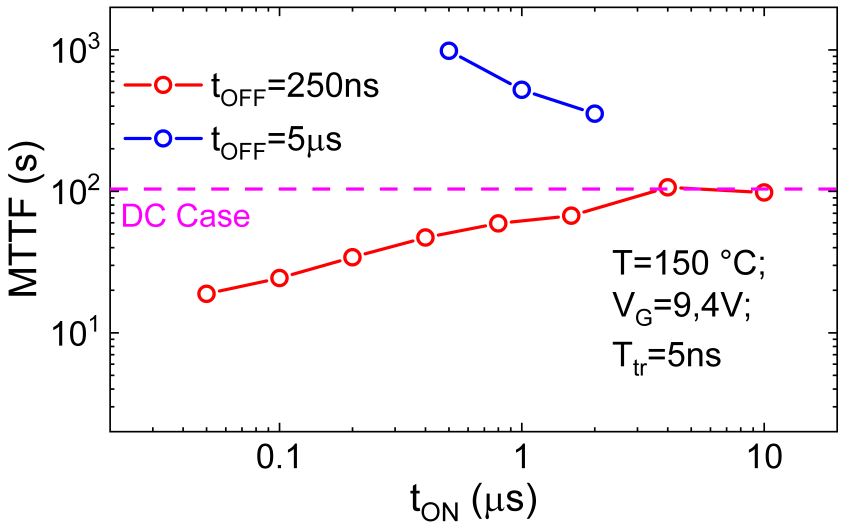

Figure 3.4: *ON-Time dependency of the Mean Time-to-Failure with two fixed OFF time, i.e., 250 ns (red) and 5 µs (blue). Results of time-dependent gate breakdown tests with V_G = 9.4 V, T = 150 °C and t_{TR} = 5ns. Each experimental data point is the average over 7-15 devices..*

For a better understanding, the mean Total ON-Time is compared with the DC case in Fig. 3.5. DC condition represents the mean time-to-failure extrapolated by typical Constant Voltage Stress (CVS) tests at 9.4 V, i.e. the same value of the square-wave amplitude used for pulsed stress test. From Fig. 3.5 emerges that, in the case of t_{OFF} = 250 ns, for $t_{ON} \leq 2\mu s$ the mean total ON-time is shorter than the DC case. On the other hand, for $t_{ON} > 2\mu s$, as well as for longer t_{OFF} ($5\mu s$), the mean total ON-time features values close to that one extrapolated by CVS tests. These initial findings suggest the possibility that dynamic gate stress, hence the transition phases,

may introduce further degradation effects in addition to the ones induced by total time in which the gate voltage is at higher level (t_{ON}).

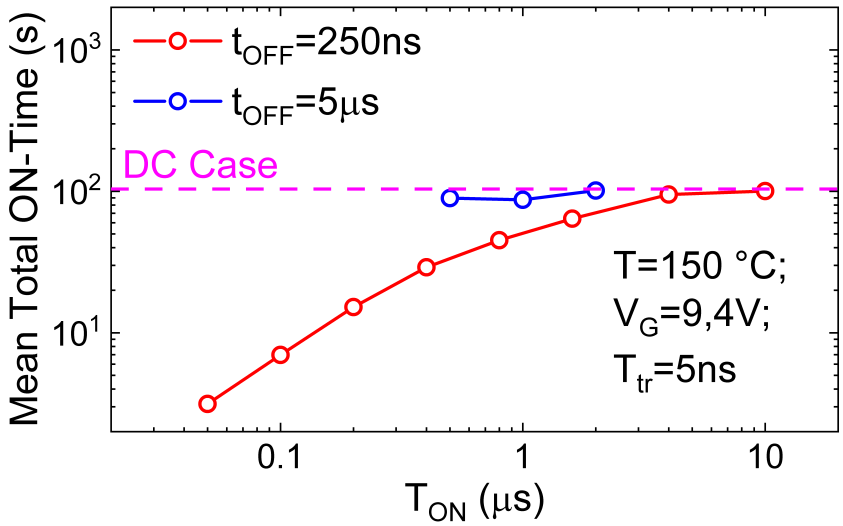

Figure 3.5: *ON-Time dependency of the Mean Total ON-Time to Failure with two fixed OFF time, i.e., 250 ns (red) and 5 µs (blue). Results have been derived from the MTTF in Fig. 3.4.*

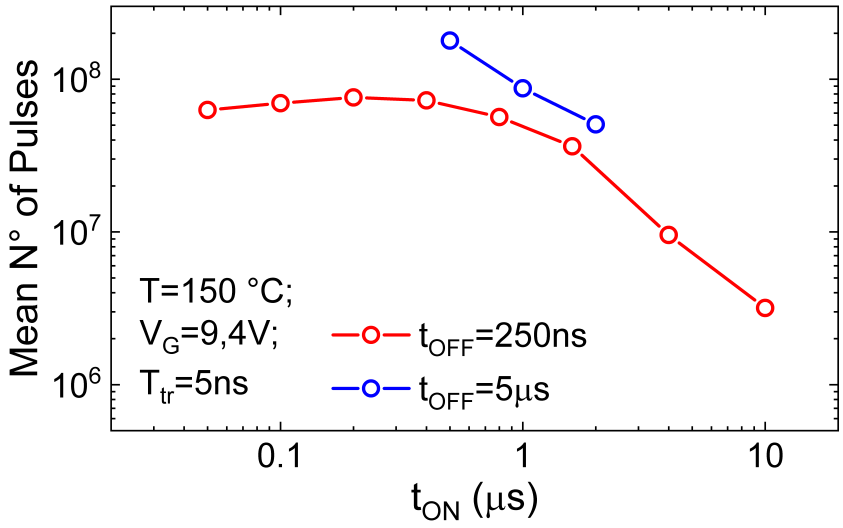

Figure 3.6: *ON-Time dependency of the Mean Number of Pulses with two fixed OFF time, i.e., 250 ns (red) and 5 µs (blue). Results have been derived from the MTTF in Fig. 3.4.*

This observation finds support in Figure 3.6, which demonstrates that for relatively short ON- and OFF-times ($< 1\mu s$ and 250 ns, respectively)), the mean N^o of pulses remains roughly constant, regardless of the specific value of t_{ON}. This implies that the number of transition phases plays a significant role in determining the TDGB.

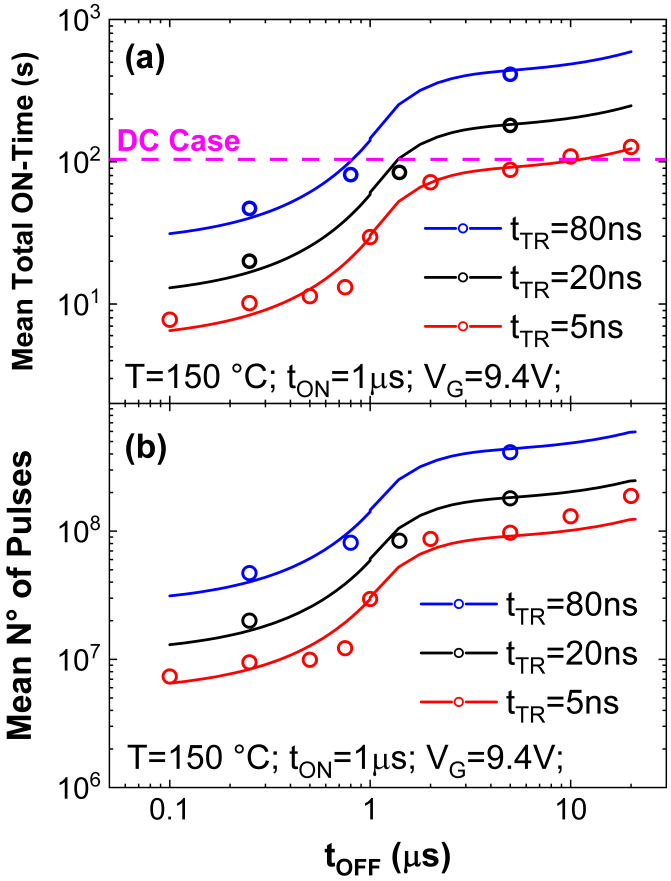

Figure 3.7: *OFF-Time dependency of the Mean Total ON-Time (a) and Mean Number of Pulses (b) with fixed ON-time (1 μs.). Results of time dependent gate breakdown tests with VG = 9.4 V, T = 150°C and three different t_{TR} (5 ns, 20 ns and 80 ns). Each experimental data point is the average over 7-15 devices.*

On the contrary, by further increasing t_{ON} ($> 2\mu s$), the degradation ascribed to Total ON-Time starts to be dominant, leading to a gate TTF with a reduced N^o of pulses. As a result, the degradation induced by the transition phase is reduced as well, giving rise to a mean Total ON-Time to

failure equal to DC-MTTF (Fig. 3.5). Same behavior is observed with a $t_{OFF} = 5\mu s$, suggesting that a longer t_{OFF} is weakening the degrading effect of the transition phase, in fact, once again, the Total ON-time to failure equals the DC case (Fig. 3.5).

To investigate the factors that influence the degradation effect during the transition phase, dynamic time-dependent gate breakdown tests with different OFF-time (ranging from 100 ns to 20 μs) and transition time (5 ns, 20 ns and 80 ns) have been performed at fixed t_{ON}=1 μs.

Fig. 3.7 shows that the mean Total ON-time depends on both t_{OFF} and t_{TR}. In particular, the shorter t_{TR}, the shorter the mean Total ON-Time to failure. To explain such trend, the current has been monitored with experimental setup described in the previous section (Fig. 3.2), by varying the transition time (from 5 ns to 80 ns) and by fixing t_{ON}=1 μs, t_{OFF} = 250 ns and V_G = 8 V.

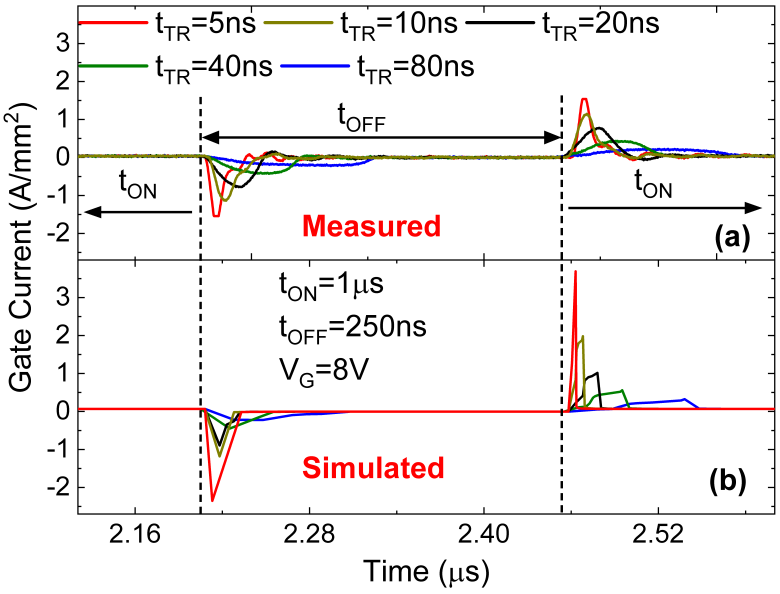

Figure 3.8: *Measured (a) and simulated (b) gate current with t_{ON}=1 μs and t_{OFF} = 250 ns and different transition times.*

Fig. 3.8 (a) shows that the current peaks occurring during the rising and falling phases are strongly impacted by the transition time. In particular, the shorter the transition time, the higher and tighter the current peaks at both rise and fall switching phases. As a result, the faster is the transition phase the stronger is the degradation effect induced by the current spikes, possibly responsible of the gate time-to-failure reduction. A good agreement has been

found with the TCAD-simulated gate current [Fig. 3.8 (b)], reproducing the same dependency and confirming that the current overshoots are not introduced by the stray inductance of the test circuit but by the gate stack structure itself.

In addition to t_{TR} dependency, results show that increasing the value of t_{OFF} effectively mitigates the degradation effect associated with the transition phase. This observation is confirmed by the data presented in Figure 3.7 (b), which demonstrates that the device's capacity to withstand a certain number of pulses before gate breakdown increases with both t_{OFF} and t_{TR}. Moreover, it is worth noting that for longer t_{TR} and t_{OFF}, the mean Total ON-time is longer than DC-MTTF, as depicted in Figure 3.7 (a). This might be possible if the defects produced during the ON-time experience partial recovery during the OFF-time, assuming that the degradation resulting from switching phases remains minimal due to an extended t_{TR} and consequently reduced leakage current peaks.

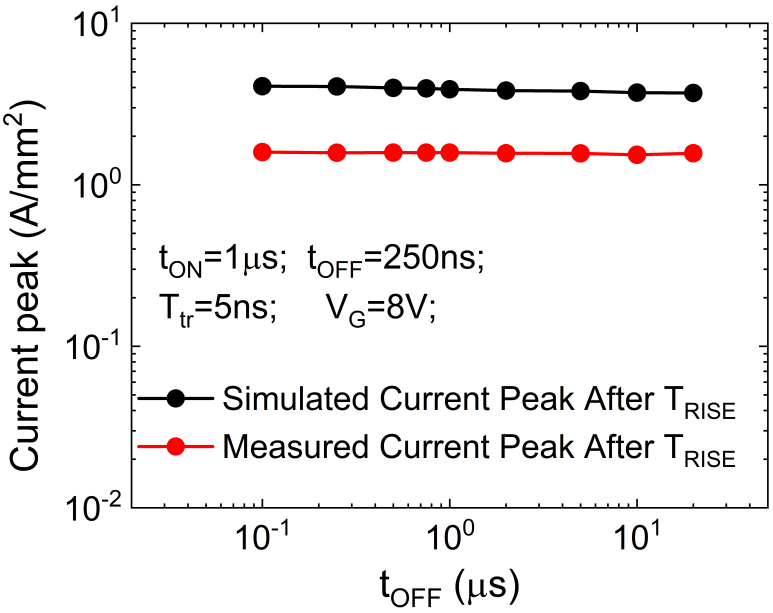

Figure 3.9: *OFF-Time dependency of the measured (red) and simulated (black) current peak at the switching phase.*

From percolation theory [26–28], when a relatively high electric field is applied to a defective region, new defects/traps are created in addition to pre-existent ones. Once a critical number of defects forms in a specific location, a percolation path, inducing layer/device breakdown, is created. These processes exhibit time-dependent behavior. Unlike DC case, under pulsed

stress condition the time necessary to reach the failure (i.e., the creation of enough new defects) might be longer since the stress time is interrupted (OFF-time); this relaxation period possibly induces a partial recovery of the failure processes.

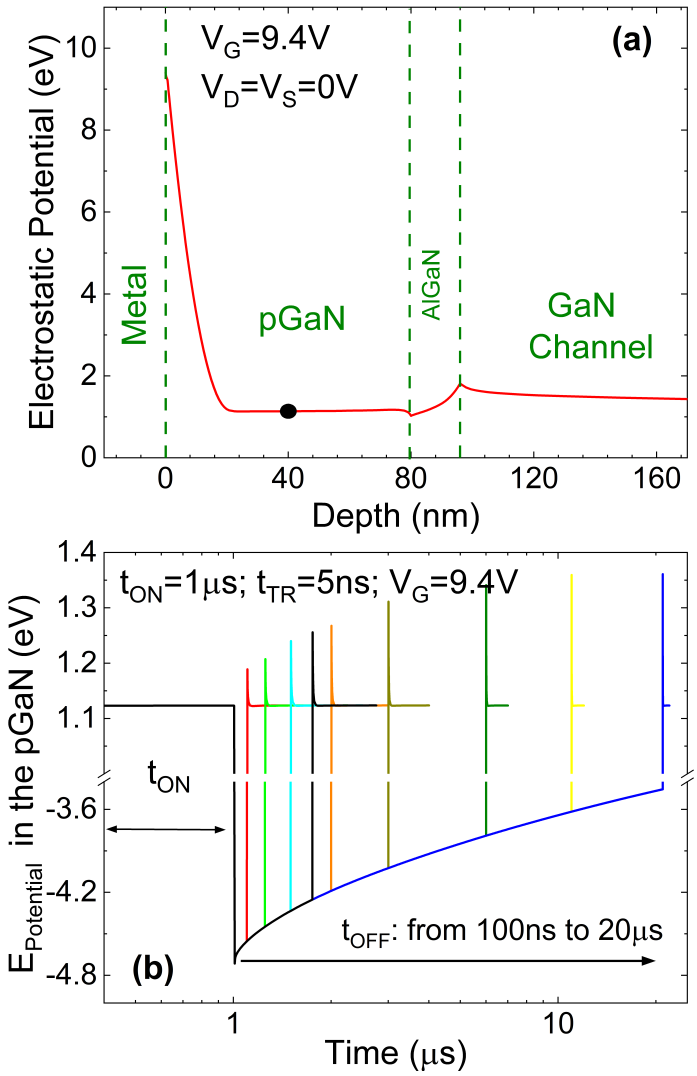

Figure 3.10: *Simulated electrostatic potential along the device at V_G = 9.4 V and $V_S = V_D = 0$ V (a). TCAD simulation of the electrostatic potential monitored in the semi-floating p-GaN layer with different OFF-Time (b).*

The t_{OFF} dependency cannot be explained by the current peak during the switching phase. This is supported by experimental data and TCAD simulations, which reveal that the current peak remains consistent across

different OFF-time settings, as illustrated in Fig. 3.9. However, the gate reliability is strongly influenced by t_{OFF} as shown in Fig. 3.7.

Thanks to TCAD simulations, the electrostatic potential has been monitored by varying t_{OFF} in the middle of the semifloating p-GaN layer, i.e., at a distance of 40 nm from the gate metal and the pGaN/AlGaN interface. This specific location was chosen because the carrier density is constant, being sufficiently distant from both the Schottky depletion region and the 2DHG layer [Fig. 3.10 (a)], to avoid any influence. In Fig. 3.10 (b), it can be observed that after the transition from ON- to OFF-state (fall time) the p-GaN potential (V_{pGaN}) is at the same level whatever the t_{OFF} is. During the OFF-state phase (i.e. $V_G = 0$ V) such potential changes/recovers and then, when the device turn-on occurs, it shows a peak after the rise time.

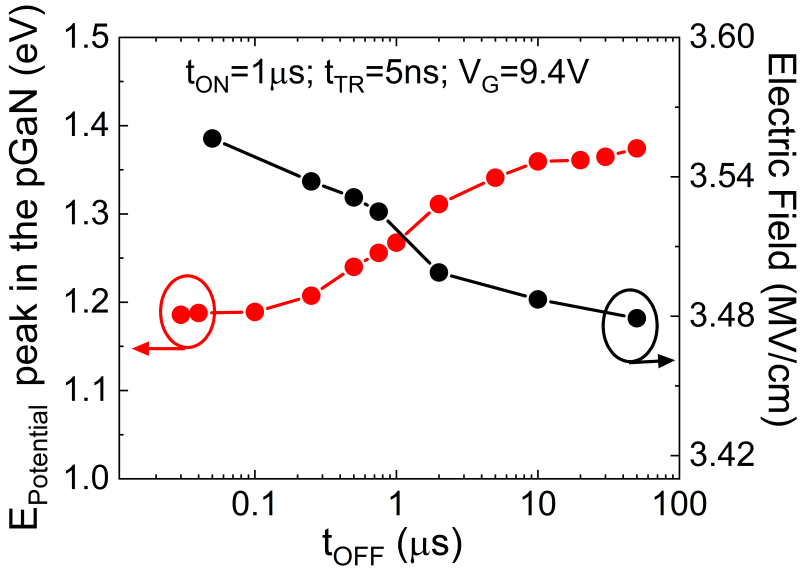

Figure 3.11: *OFF-Time dependency of the Electrostatic potential peaks at the transition from OFF- to ON-State (just after t_{RISE}) and corresponding mean electric field evaluated across the depletion region of the Schottky junction.*

Such phenomenon is ruled by the recovery time, i.e. the longer the OFF-time the higher the height of the potential peak, inducing a lower Schottky junction voltage drop ($V_{Schottky} = V_G - V_{pGaN}$), hence a lower electric field across the Schottky depletion region [see Fig. 3.11]. This explains the reason why a longer t_{OFF} leads to a longer MTTF. Fig. 3.11 reports the Electrostatic Potential peaks after the rise time and the correspondent Electric Field across the Schottky depletion region.

The TCAD simulated electric field values are notably high, approaching the critical electric field of GaN. This is attributed to the fact that the physical models used to reproduce the gate leakage hasn't been precisely calibrated as can be seen from the difference between the simulated and measured currents observable in the Fig. 3.9, since the main goal was qualitative reproduction of the device's electrical characteristics under various AC conditions (i.e. different OFF-time). In fact, it is worth noting that the observed dependency of the electric field on the t_{OFF} is similar to the one shown in the case of mean Total ON-time and mean N° of pulses (Fig. 3.7), confirming the validity of the TCAD simulations, hence, the conclusions drawn from this analysis.

3.4 The Role of Frequency and Duty Cycle

The analysis is extended with stressing gate signal featuring different frequencies (from 100 kHz to 1 MHz) and duty cycles (from 10% to 90%), while the slew rate (or transition time t_{TR}) is fixed at 5 ns. Finally, a stress temperature of 150^oC is adopted for all the experiments, as it represents the maximum operating junction temperature for commercial GaN-based FETs.

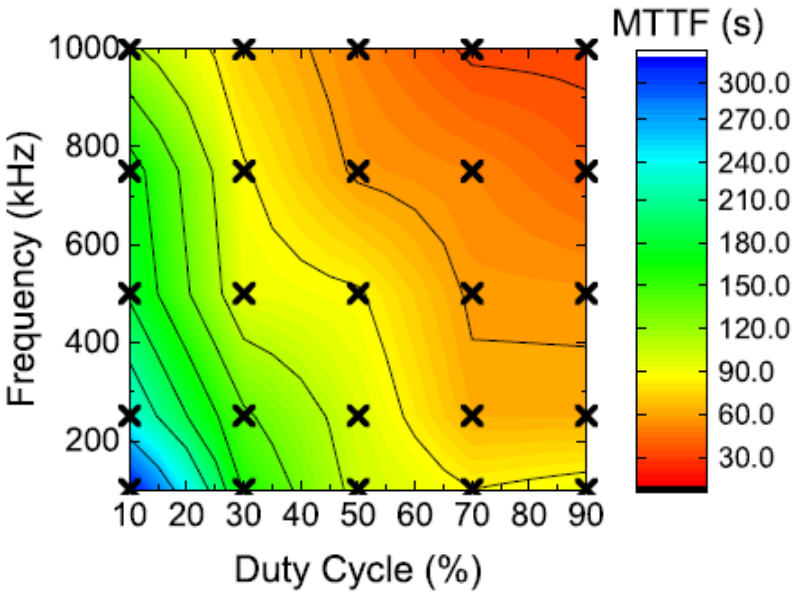

Figure 3.12: *Contour plot showing the dependency of the gate MTTF on both the frequency and the duty cycle at V_G = 9.4 V and T =150^oC. 10 devices per group have been stressed to extrapolate the MTTF. The symbols "x" represent the implemented stress conditions.*

Fig. 3.12 shows the contour plot of the MTTF as a function of both frequency (f) and duty cycle (D). This investigation is carried out by applying a stressing waveform characterized by an amplitude of $V_G = 9.4$ V. It's important to note that the MTTF values represent the mean values derived from the time-to-breakdown data collected from a set of 10 devices.

This analysis reveals a distinct trend: as either the frequency or the duty cycle is increased, there is decrease in the gate MTTF. This observation suggests a significant influence of these operational parameters on the long-term reliability and performance of the devices under study.

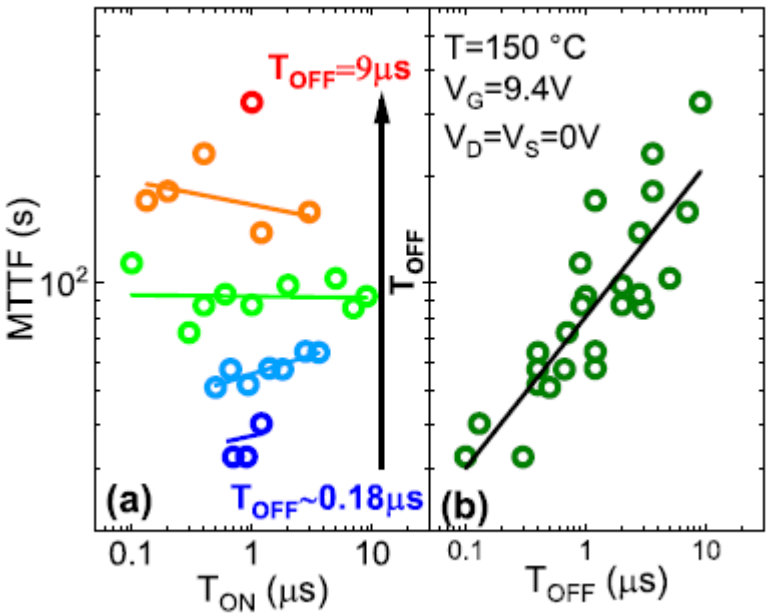

Figure 3.13: *(a) ON-Time and (b) OFF-Time dependency of the MTTF at $V_G = 9.4$ V and $T = 150^oC$. Each MTTF point is the result of 10 stressed devices.*

In order to identify the cause of such behavior, the MTTF reported in Fig. 3.12 is plotted as a function of the ON-time and the OFF-time in Fig. 3.13(a) and Fig. 3.13(b), respectively. To better illustrate and comprehend these findings, the data have been categorized in various groups characterized by similar T_{OFF} values and the data is represented using different colors. This approach has been employed to emphasize the notable absence of MTTF dependency on T_{ON}.

On the contrary, by focusing on a fixed ON-Time (e.g. 1 μs) a pronounced and distinct dependency on the OFF-time shows up. In particular,

the shorter the OFF-time interval, the shorter the corresponding MTTF. Such statement, is further confirmed in Fig. 3.13 (b), where MTTF is plotted as a function of the T_{OFF}, independently of any value of T_{ON}.

In the previous section, TCAD simulations have highlighted that the OFF-time parameter emerges as a significant factor influencing the magnitude of the electrostatic potential peak within the semi-floating p-GaN layer during the transitional phase from the OFF-state to the ON-state. The latter takes tens of microseconds before reaching a quasi-steady state. As a result, the related peak after the switching-ON transition is determined by the electrostatic potential level reached at the conclusion of the OFF-time period. The latter, as shown in 3.10 (b), should exceed a duration of 5 μs to ensure a nearly imperceptible impact on the electrostatic potential peak. This, in turn, translates into a negligible effect on the gate Time to Failure.

This mechanism explains the behavior of the MTTF shown in Fig 3.12. In fact, as confirmed by Fig. 3.14, there is a correlation between the frequency and the duty cycle, and the T_{OFF}. Specifically, with an increase in both f and D, there is a corresponding decrease in the T_{OFF}. This reduction in the OFF-time period subsequently leads to a shorter MTTF. Such results further emphasize the significance of the OFF-time duration as a key determinant of device gate reliability under pulsed conditions.

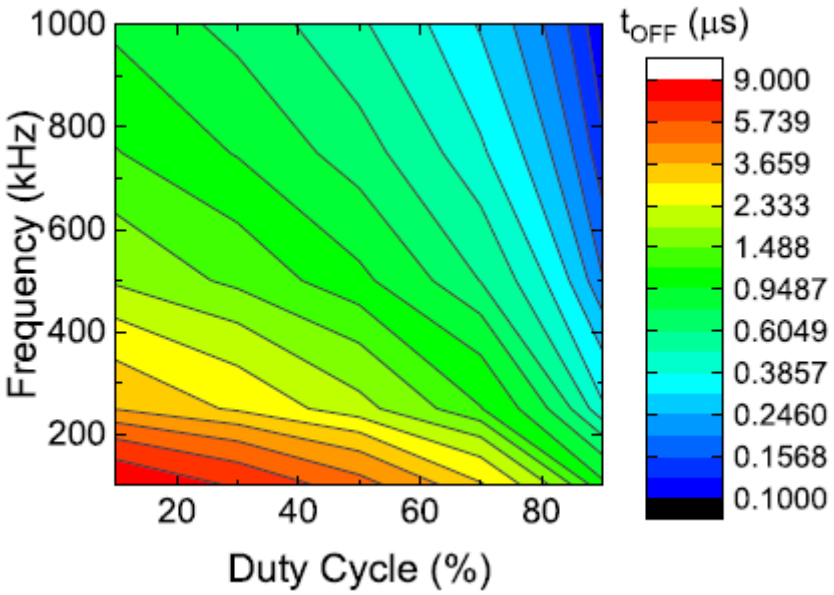

Figure 3.14: *Contour plot showing how the OFF-Time changes with both the frequency and the duty cycle.*

From Fig. 3.12, it is possible to identify a best and a worst case for the

gate MTTF, i.e. {f = 100 kHz; D = 10 %} and {f = 1 MHz; D = 90 %}, respectively. Such cases represents the stressing condition (f and D) with shortest and longest OFF-Time, respectively. For these specific condition, the analysis has been extended at different gate amplitudes with the scope of extrapolating the gate lifetime. Results are reported in Fig. 3.15. In particular, Fig. 3.15 (a) and 3.15 (b) show the gate current monitored during the stress time and the related Weibull plot in the case of f = 100 kHz ; D = 10 %, respectively, whereas Fig. 3.15 (c) and 3.15 (d) report same information in the case of f = 1 MHz ; D = 90 %. In both cases, the trend of the gate leakage over the time reveals an abrupt failure and, furthermore, a similar shape parameter (β) ranging between 2.3 and 2.6 is observed, suggesting intrinsic breakdown.

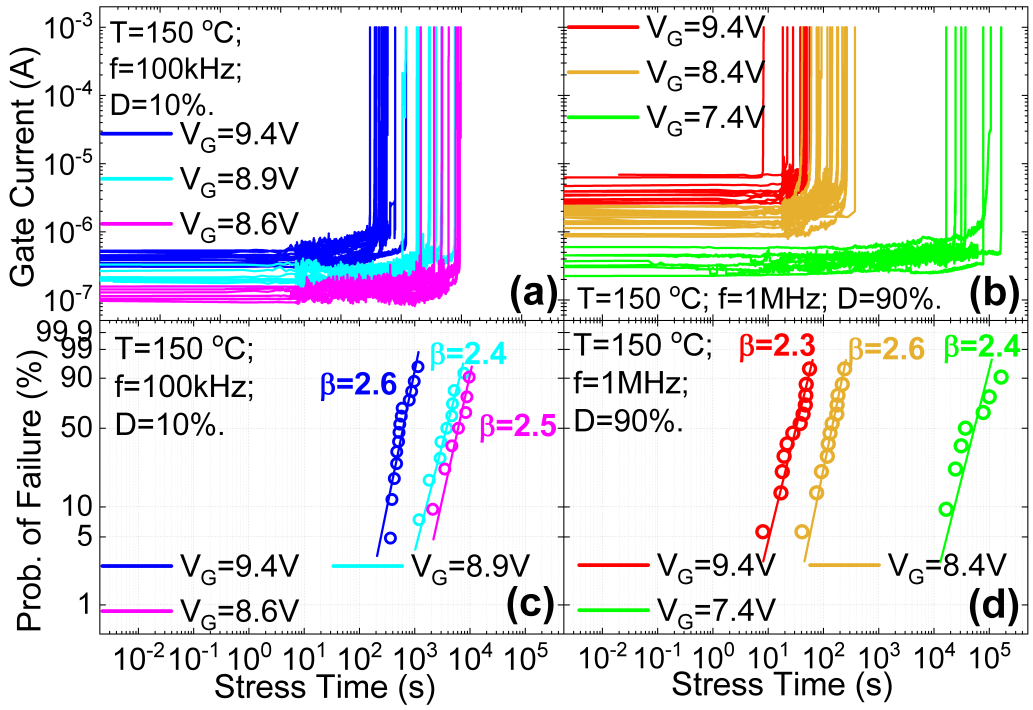

Figure 3.15: *Gate current monitored over the stress time at different voltages in the case of (a) f = 100 kHz; D = 10% and (c) f = 1 MHz; D = 90% with the corresponding Weibull plots (b) and (d), respectively.*

The gate lifetime has been extrapolated and compared, as reported in Fig. 3.16, with the one predicted by means of standard Constant Voltage Stress (DC) tests. The TTF values are extrapolated from Weibull plots of Fig. 3.15 (b) and 3.15 (d) considering as failure criterion a failure rate equal to 1%.

The model in which TTF is proportional to exp $(1/I_G)$ has been adopted as a fitting means for all the considered cases, DC and pulsed. This model has been proposed in the previous chapter to reproduce the relationship between gate TTF and V_G when the breakdown occurs in the isolation regions rather than in the active gate area. This mechanism has been reported to occur under DC gate stress at relatively high temperatures (T> 80^oC) [21, 22]. It is possible to confirm the presence of this mechanism also in the case of pulsed gate stress. In fact, the observed V_G dependency of the TDGB is the same as for DC case (Fig. 3.16). Moreover, a lack of area dependency of the gate TTF has been observed also in this context and reported in Fig. 3.17. Area (gate width) dependency of the gate TTF at V_G = 7.4 V, f = 1 MHz, D = 90% and T = 150^oC.

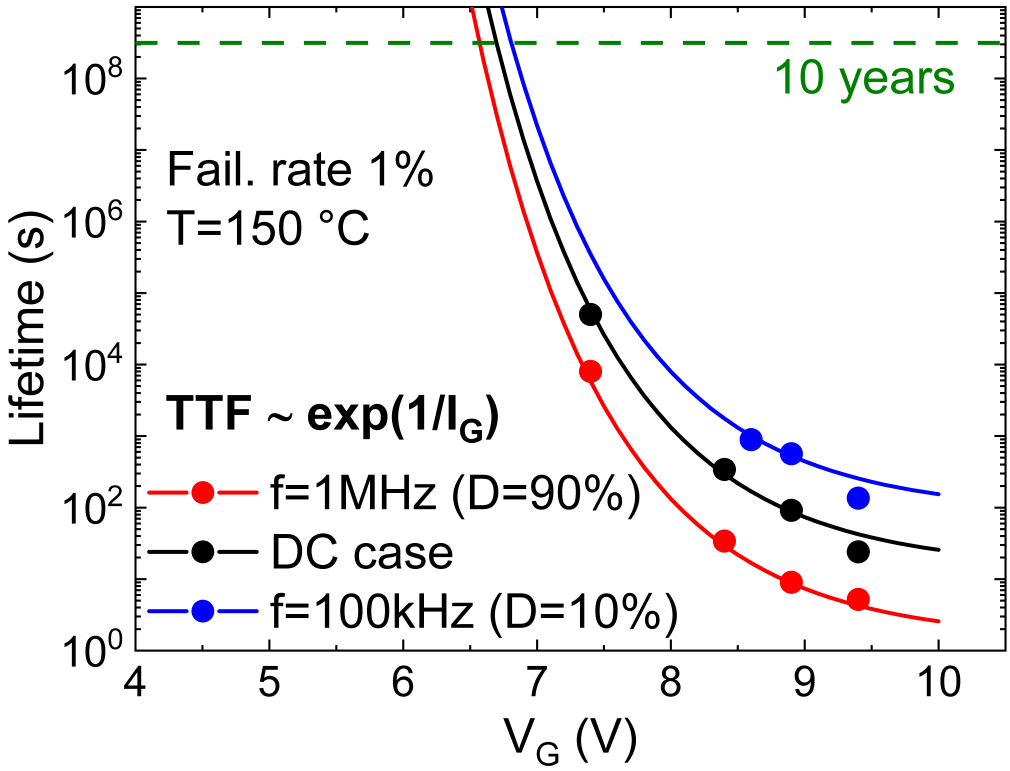

Figure 3.16: *Lifetime comparison under three different stress conditions: f = 1 MHz and D = 90% (red), DC (black), f = 100 kHz and D = 10% (blue). "$TTF \propto exp(1/I_G)$" fitting model has been adopted for all conditions. Failure criterion: 1% at* 150^oC *extrapolated from the Weibull plots..*

Finally, Fig. 3.16 shows how the case with f = 1 MHz and D = 90% gives rise to a slightly smaller extrapolated maximum V_G with respect to DC case.

When the Off-time is relatively short, as explained before, the electrostatic potential of the p-GaN layer is altered during the switching phase, increasing the related degrading effect. The latter is minimized/negligible for longer t_{OFF}. In fact, it is worth noting that the maximum extrapolated gate voltage ensuring 10 years of lifetime related to the case with f = 100 kHz and D = 10% is slightly higher with respect to the one extrapolated under DC stress conditions since, in this case, the TTF is mainly ascribed to the total ON-time in which the device is subject to a positive and relatively high V_G (sum of t_{ON} up to failure).

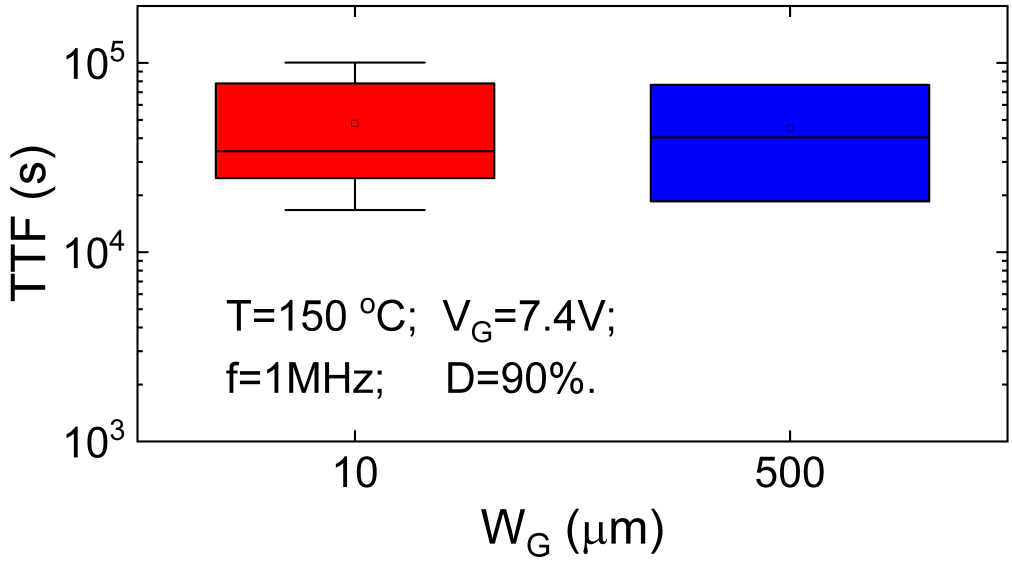

Figure 3.17: *Area (gate width) dependency of the gate TTF at V_G = 7.4 V, f = 1 MHz, D = 90% and T = 150^oC.*

3.5 Conclusions

An in-depth analysis of TDGB of p-GaN HEMTs under pulsed stress condition at 150^oC has been proposed. The gate time-to-failure has been investigated by means of applied consecutive square-waves, featuring different ON-time, OFF-time and rise/fall time, supported by transient current sensing and TCAD simulations. Two main factors determine the time-dependent gate breakdown of GaN-HEMTs with p-type gate under pulsed stress conditions: the switching phase (number of applied pulses) and the time in which the device is kept in ON-State, plus a possible recovery mechanism occurring during the t_{OFF}. The amount of degradation coming from the switching

phase depends on both t_{OFF} and t_{TR}. The latter is responsible of altering the amplitude of the current peak during the switching phase. The longer the t_{TR}, the lower the amplitude of such current spikes, the longer the TTF. A good agreement between simulations and experiments has been found.

The OFF-time dependency is ascribed to electrostatic potential in the semi-floating p-GaN layer (V_{pGaN})at the switching phase from OFF- to ON-state. The magnitude of such peak is ruled by t_{OFF}, i.e., it decreases by reducing t_{OFF}. As a consequence, the voltage drop on the Schottky depletion region ($V_{Schottky} = V_G - V_{pGaN}$), hence electric field, during the transition phase increases by reducing t_{OFF}. The simulated p-GaN potential and the Mean Total ON-Time show similar trends with t_{OFF}. In conclusion, it can be stated that a too short t_{TR} and t_{OFF} gives rise to a shorter time-dependent gate breakdown compared to DC stress condition.

Subsequently, the analysis has been extended in order to investigate the effects of the switching frequency (from 100 kHz to 1 MHz) and the duty cycle (from 10% to 90%) on the time-dependent gate breakdown of GaN HEMTs with a Schottky metal to p-GaN gate structure. Experimental results shown that the Time-to-Failure decreases by increasing the frequency and/or the duty cycle, since they induce a shortening of the OFF-time of the square-wave applied to the gate, which in turn alters the electrostatic potential of the semi-floating pGaN layer during the switching phases.

In addition, a comparison between gate lifetime extrapolated under DC and pulsed stress conditions has been reported. This highlighted that whatever the stressing conditions are, the relationship between gate TTF and V_G at high temperature can be modeled with the same fitting law ("$TTF \propto exp(1/I_G)$") proposed in the previous chapter. This result confirms that for pGaN HEMTs with gate metal retraction suffers of failure at the isolation region at 150^oC, whatever the working conditions are. Moreover, results have shown how switching frequency and duty cycle impact on the gate lifetime, i.e., the latter can be longer or shorter when compared with the DC case.

These findings not only offer valuable theoretical insights on this technology but also provides useful indication for potential strategies to enhance device performance and longevity in practical applications.

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Chapter 4

Role of the GaN-on-Si Epi-Stack on ΔR_{ON} Caused by Back-Gating Stress

4.1 Introduction and State of the Art

It is well-known that the deposition of GaN and its compounds (AlGaN, AlN, etc.) on a foreign substrate (e.g., silicon) implies the presence of defects/dislocations along the entire buffer up to the device surface [1]. Even though, process engineering is at an advanced stage, and GaN-on-Si devices demonstrate a good capability of withstanding relatively high drain biases [2–5], charge storage and release from buffer traps or in the overall stack is still one of the dominant mechanisms causing static and/or dynamic ΔR_{ON} [6–13]. Therefore, more effort is required to understand the origin of such mechanisms and how to optimize the buffer stack to minimize their effects.

In most cases, the carbon doped GaN back-barrier (C:GaN) layer plays a key role in ΔR_{ON} since it can lead to charge storage and release during high-voltage OFF-state operation. According to the "leaky dielectric" model [6], when the buffer stack is exposed to a vertical electric field, two mechanisms show up: 1) the ionization of carbon-related acceptor traps (C_N), promoting the storage of negative charge in the C:GaN layer, inducing R_{ON} increase and 2) electron band-to-band tunneling from C:GaN valence band (V_B) to two-dimensional electron gas (2DEG) through defects and dislocations, inducing hole accumulation at the C:GaN/superlattice (SL) interface, increasing the 2DEG density (R_{ON} decrease). In [13], it is shown that charge propagation through the C:GaN and the unintentional doped (uid)-GaN are assisted by 1-D and 3-D variable range hopping, respectively.

Many experimental techniques have been developed to investigate charging and discharging processes in the AlGaN/GaN buffers of power devices [12–21]. Among them, one of the most adopted is the back-gating current deep-level transient spectroscopy (I-DLTS) [12–27], which consists in monitoring the recovery of R_{ON} after a negative substrate voltage stress. The latter induces different charge storage mechanisms which may compete with each other making it difficult to distinguish and quantify their effect separately [12–27]. In fact, the choice of the test conditions and the transient analysis technique can strongly impact the extracted parameters (e.g., activation energy) that characterize the kind of traps or the involved physical mechanisms [12]. The most accurate method consists in fitting the R_{ON} as a sum of stretched exponential, providing useful information to understand and quantify the role of the stress conditions on the trapping and storage mechanisms and their features [24–27].

For the research activity reported in this chapter, the back-gating I-DLTS technique is adopted to explore how the test conditions (substrate bias, stress time, and temperature) and the thickness of the layers composing the buffer epi-stack impacts on ΔR_{ON}. The latter is fitted with a stretched exponential model by means of a mathematical approach, based on the study of the derivative, combined with a genetic algorithm to minimize the fitting error.

4.2 Experimental Details

A sketch of the devices under test (DUTs), fabricated by IMEC on 200-mm Si substrate for low-voltage HEMTs ($<$ 100 V), is shown in Fig. 4.1 (a). The main difference with respect to GaN HEMT lies in the absence of the gate region. In this case, a passivation region is deposited on top of the AlGaN barrier and two ohmic contacts are created. Such a structure allows focusing the analysis directly on the effects of trapping/de-trapping mechanisms occurring in the buffer region, avoiding possible gate overdrive-dependent trapping mechanisms. Different process splits, in terms of layer thicknesses, have been analyzed. The reference structure features an epi-stack composed of a 200-nm-thick AlN nucleation layer grown on top of Si-substrate, 330-nm-thick SL layer, 500-nm-thick C:GaN layer, 200-nm-thick uid-GaN channel layer, and 11-nm-thick $Al_{0.23}GaN_{0.77}$ barrier layer.

The back-gating I-DLTS test have been performed on devices at the wafer level and it consists of three consecutive steps:

1. Voltage sweep to monitor the fresh current (I_0) between the two ohmic contacts [see Fig. 4.2 (a)] with $V_B = 0$ V;

2. A negative substrate stress voltage (V_B) is applied for a fixed stress time (t_S) [see Fig. 4.2 (b)];

3. The current between the two ohmic contacts is monitored with a voltage drop of 0.7 V until the recovery is completed.

Finally, the current monitored during step 3 is normalized (I_N) with respect to the fresh value measured in 1. A typical result is shown in Fig. 4.2 (c). Experiments have been performed at different temperatures, stress times, and V_B.

The reason why the current is monitored during the recovery rather than the stress phase is related to 2DEG depletion, which occurs for $|V_B| > 50V$, making the current monitoring difficult and noisy.

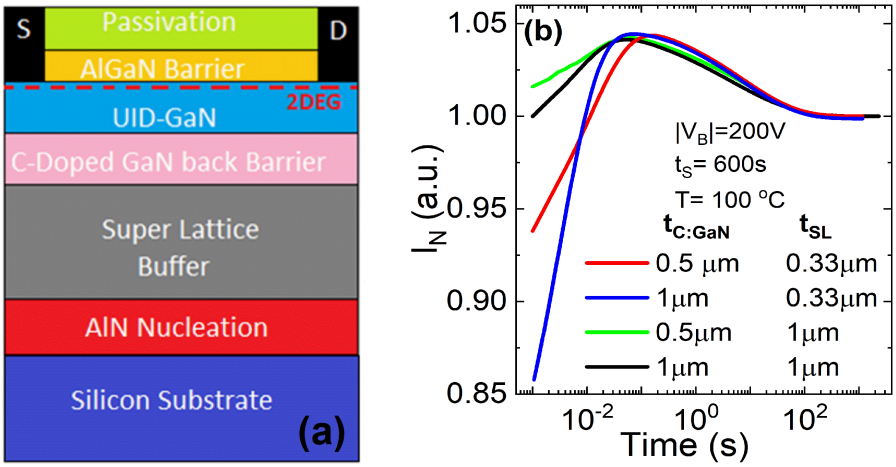

Figure 4.1: *Sketch (not to scale) of the device under test and the epi-structure. (a) Recovery current transient for different buffer configurations. (b) Stressing phase has been performed for 600 s with* $|V_B| = 200$ *V at* $T = 100^oC$.

In this analysis, to induce the trapping phenomena in the buffer, a negative voltage was applied to the substrate contact to replicate the OFF-state operational conditions of the device (with a high voltage on the Drain), even though in real applications, the substrate is typically grounded. The choice of device type and test conditions was driven by the specific aim of investigating the influence of the vertical electric field on the R_{ON}. Additionally, the device under tests lacks suitability for high Drain voltages due to the absence of a gate region, thereby precluding OFF-state operation. Even if a complete transistor had been chosen, the application of high Drain voltage would likely trigger additional processes potentially leading to further

degradation of R_{ON}, hence masking the effect of the buffer layers on such parameter.

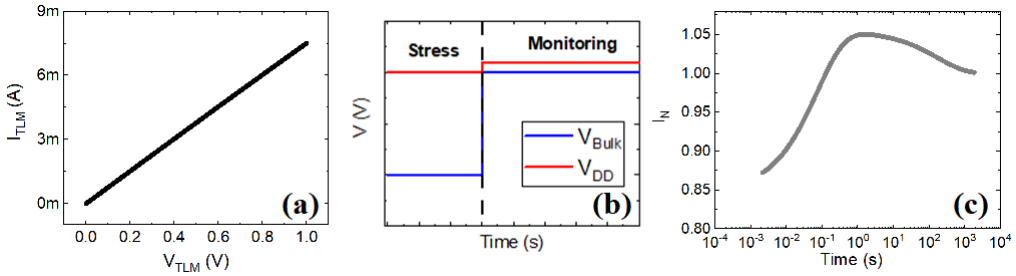

Figure 4.2: *I-DLTS experimental steps: (a) voltage ramp to monitor the fresh current and (b) stressing and monitoring phase. Measured current during the monitoring phase and normalized wrt the fresh current.*

4.3 Brief Physical Background

Fig. 4.1 (b) reports I_N after a stress phase of 600 s with $|V_B|$ = 200 V and T = 100^oC for all the process splits considered in this work. The current features two consecutive transients, i.e., I_N increase followed by a decrease toward the pre-stress value. For the sake of clarity, from here on, the faster (first) transient and the slower one (second) will be referred to as TR1 and TR2, respectively. In [11], the I_N increase is ascribed to electron detrapping from acceptor states in the C:GaN layer, which leads to a gradual increase of the 2DEG density (R_{ON} decrease), whereas TR2 is associated with recombination of holes accumulated at the C:GaN/SL heterointerface, inducing an R_{ON} increase (2DEG decrease). More details on the physical mechanisms can be found in [6–11]. It is worth noting that this description refers to the recovery phase; exactly the opposite occurs during the stress phase, i.e., electron trapping in acceptor states and hole accumulation at the C:GaN/SL interface, leading to R_{ON} increase and decrease, respectively.

4.4 Transients Analysis Methodology

The adopted methodology is based on the stretched exponential fitting law [24], by approximating I_N as follows:

$$I_{fit}(t) = 1 + \sum_{i=1}^{N} f_i(t) = 1 + \sum_{i=1}^{N} A_i e^{-\left(\frac{t}{\tau_i}\right)^{\beta_i}} \tag{4.1}$$

f_i (t) is the i_{th} stretched exponential, N is the number of involved charge/discharge processes, A_i is the transient amplitude representing the amount of stored/released charge, τ_i is the charge emission time constant, and β_i is a stretching term representing the "slope" of the transient. The i_{th} derivative is

$$f_i^{'}(t) = -\frac{A_i \beta_i}{t} \left(\frac{t}{\tau_i}\right)^{\beta_i} e^{-\left(\frac{t}{\tau_i}\right)^{\beta_i}} \tag{4.2}$$

To estimate τ_i and simplify the computation, we define ψ_i (t) as:

$$\psi_i(t) = ln(10) t f_i^{'}(t) = -ln(10) A_i \beta_i \left(\frac{t}{\tau_i}\right)^{\beta_i} e^{-\left(\frac{t}{\tau_i}\right)^{\beta_i}} \tag{4.3}$$

to verify that maxima or minima of ψ_i (t) is located at t = τ_i. Then, the triplet (A_i , β_i , and τ_i) can be retrieved as

$$\hat{\tau}_i = max\left\{\psi_i(t)\right\} \ or \ min\left\{\psi_i(t)\right\} \tag{4.4}$$

$$\hat{A}_i = e \cdot f_i(\hat{\tau}_i) \tag{4.5}$$

$$\hat{\beta}_i = -\frac{e}{ln(10)} \frac{\psi_i(\hat{\tau}_i)}{\hat{A}_i} \tag{4.6}$$

The question arises whether the estimation of A_i , β_i , and τ_i parameters is correct or not by following this approach. By assuming that $\tau_1 \ll \tau_2 \ll \ldots \ll \tau_N$, the proposed method searches for the maxima and/or minima of the logarithmic derivative of f(t) given by $\psi(t) = \sum_{i=1}^{N} \psi_i(t)$ obtaining preliminary estimations ($\hat{\tau}_1, \hat{\tau}_2, \ldots, \hat{\tau}_N$). Since $\tau_1 \ll \tau_2 \ll \ldots \ll \tau_N$, it is possible to approximate $I_N(\tau_i)$ as

$$I_N(\hat{\tau}_i) \approx 1 + \frac{A_i}{e} + \sum_{k=i+1}^{N} A_k \tag{4.7}$$

for all i = 1, . . . , N. Solving the linear system described in 4.7, estimates of A_1, A_2, . . . , A_N can be obtained. Lastly, β coefficients can be estimated by using 4.6.

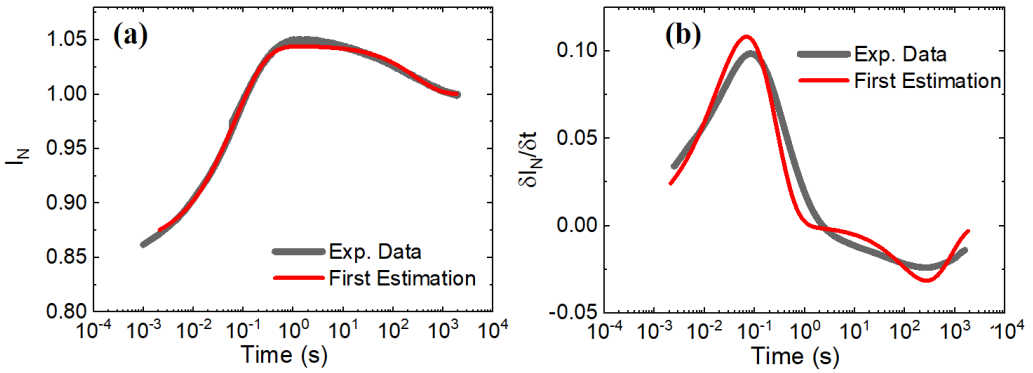

Figure 4.3: *(a) Recovery current transient compared with the first estimation and (b) their derivatives* .

By observing Fig. 4.1 (b), the number of transients is N = 2, and the solution is a set p = $[A_1,\ \tau_1,\ \beta_1,\ A_2\ ,\ \tau_2,\ \beta_2]$ of fitting parameters with constraints $A_1 < 0$, $A_2 > 0$, $\tau_1 < \tau_2$, and $\beta_i \in [0,\ 1]$.

The criticality lies in the accuracy of 4.7, which is ensured only if τ_1 and τ_2 are significantly different from each other. In addition, even if the current transients are nicely reproduced [see Fig. 4.3 (a)], ψ_i(t) may not match the actual derivative [see Fig. 4.3 (b)]. To get rid of such issues, the preliminary estimation is used as an initial solution of an optimizing algorithm, which minimizes an error function defined as the sum of the root-mean-square error (rms) of I_N(t) and its logarithmic derivative [28]:

$$E = \sum_{j=1}^{N_{samples}} |I_{N_{fit}}(t_j;\hat{P}) - I_N(t_j)|^2 + \sum_{j=1}^{N_{samples}} |\psi_{N_{fit}}(t_j;\hat{P}) - \psi_N(t_j)|^2 \quad (4.8)$$

The goal of such an algorithm is to find the optimal set of parameters p providing the best fit of the transients and their derivatives. This is possible by using a differential evolution algorithm [29, 30], i.e., a metaheuristic method that iteratively reduces E by evolving a population of approximate solutions accordingly to genetic algorithm methodology [31].

An initial population of vectors is generated by adopting the methodology described in this section. Then, a competitor (different possible solution) for each parameter vector under test is constructed by mutation and crossover over the current population. Each population element is compared with its own competitor and only one is selected (i.e., the one with the lower error), resulting in an evolved population. Finally, the mutation, crossover, and selection steps are iterated until the genetic algorithm is unable to generate a solution with a smaller error. This tool finds several applications in

telecommunication systems, such as the optimization of low-density parity-check (LDPC) codes degree profile [32] and the design of coded random access protocols [33].

4.5 Role of the Test Conditions

4.5.1 Temperature Dependence

Fig. 4.4 (a) and (b) shows I_N and its derivative, respectively, in the case of $|V_B| = 200$ V, stress time $t_S = 600$ s, and temperature ranging from - 40^oC to 200^oC. Such t_S, widely adopted for this study, has been chosen to: 1) allow a saturation of TR2 for any V_B and 2) avoid causing permanent degradation.

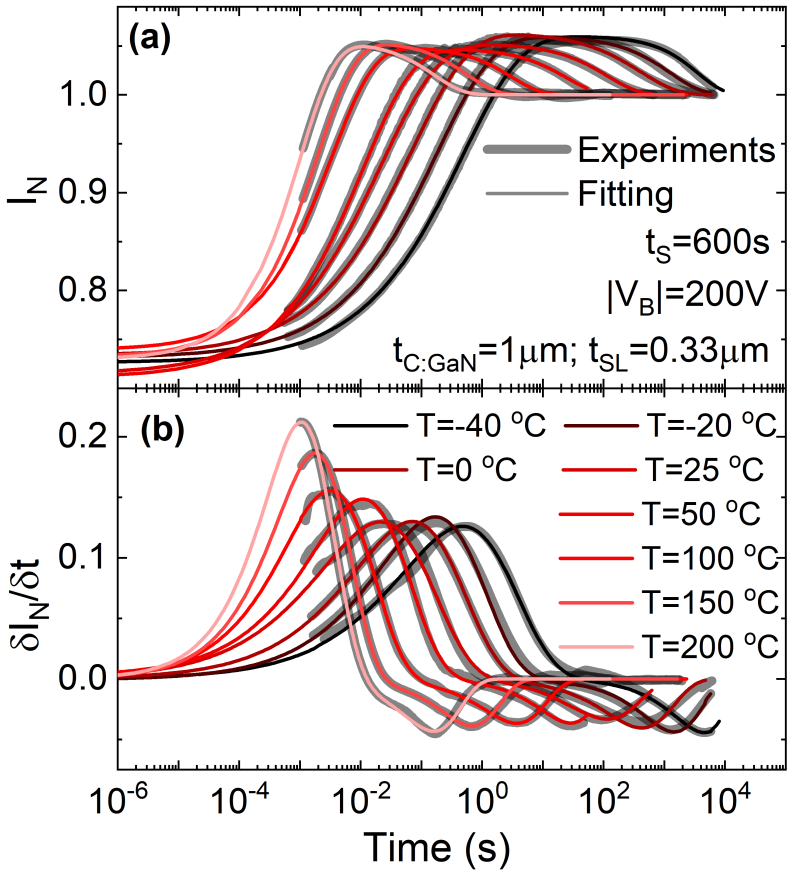

Figure 4.4: *(a) Recovery current transient and (b) its derivative with different temperatures ranging between - 40^oC and 200^oC. The stressing phase has been performed for 600 s with $|V_B| = 200V$.*

It is woth noticing that the methodology described in Section 4.4 guarantees a good fitting, also in the case of high temperatures where the two transients are superimposed (τ_1 similar to τ_2). Similar analyses have been performed also with different $|V_B|$, i.e., 75, 100, and 150 V.

Both transients TR1 (ascending) and TR2 (descending) show a clear temperature dependence, suggesting the presence of thermally activated charging/discharging processes with an activation energy (E_a) of 0.2 and 0.38 eV, respectively (Fig. 4.5). Such values are similar to the ones extrapolated in [13], [19], [34, 35] by means of back-gating measurements on AlGaN/GaN buffers.

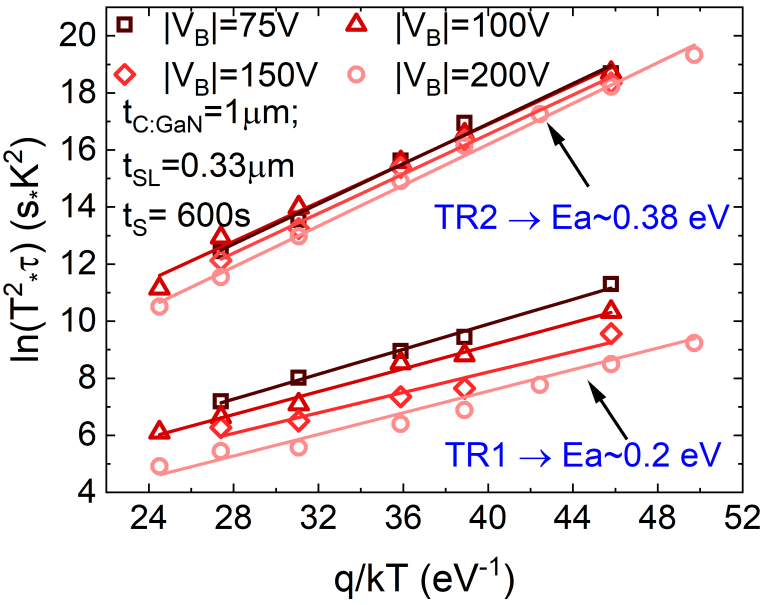

Figure 4.5: *Arrhenius plot in the case of stress voltage $|V_B|$ = 75, 100, 150, and 200 V, with a stress time of 600 s.*

In the case of TR1, its ascending trend may be ascribed to electron emission from acceptor traps in C:GaN layer, as reported in [6], [11], and [13]. In [36–38], E_a = 0.2 eV has been ascribed to carbon atoms occupying substitutional position on nitrogen sites (C_N), leading to the creation of acceptor shallow traps with E_a between 0.08 and 0.29 eV from VB. However, more recent studies [39, 40] report that the C_N acceptors in GaN bulk are energetically located at 0.9 eV from VB. In such a case, the adoption of a relatively high carbon concentration ($\sim 10^{19}$ in this case) determines a Fermi level position slightly lower than the one of C_N, forcing the occupation of any possible preexisting acceptor states (assuming lower concentration with

respect to C_N) with energy level below the Fermi one. This has been confirmed by TCAD simulation (not shown). Consequently, it is more plausible that the extrapolated $E_a = 0.2$ eV is not ascribed to the trap itself, but it represents the activation energy of trap-assisted charge transport in a defect band, probably centered at 0.9 eV from VB, i.e., carbon-related.

In [13], a 3-D hopping via a defect band mechanism has been proposed. Additional discussion, supported by TCAD simulations, will follow in Section 4.6. Regarding TR2, $E_A = 0.38$ eV might be associated with donor-like defects such as C_{Ga} [41], oxygen [42], or silicon [19] impurities. However, most likely, such value is not related to a defect itself but it could represent the energy of a charge-transport mechanism leading to electron–hole recombination among excess 2DEG electrons and holes accumulated at the C:GaN/SL heterojunction during the stress phase [13].

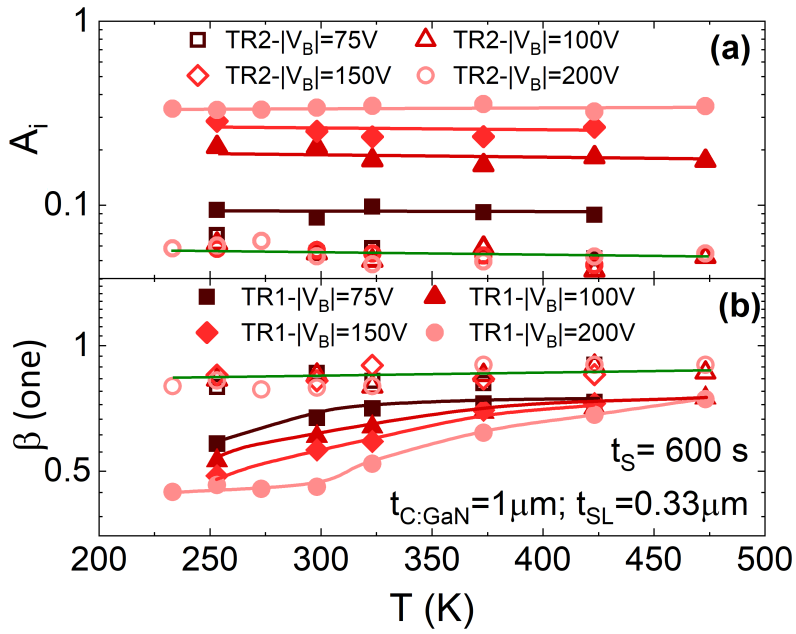

Figure 4.6: *Temperature dependence of the: (a) amplitude A_i and (b) stretching parameter β_i and for the two transient TR1 and TR2. Parameters have been extrapolated from measures reported in Fig. 4.4.*

Fig. 4.6 (a) and (b) shows the temperature dependence of the stretched exponential fitting parameters A and β, respectively. A is temperature-independent in both transients TR1 and TR2 [Fig. 4.6 (a)], suggesting that the amount of charge trapped (TR1) and accumulated (TR2) during the stress is temperature independent; it can be faster or slower but the quantity is only bias-dependent (detailed in the next section). Regarding β, a T-

dependence is shown in the case of TR1, i.e., the higher T the higher β_1, while β_2 (TR2) is almost independent, suggesting two distinct mechanisms and strengthening the theory reported in [13], i.e., electron detrapping from acceptor states (TR1) and recombination of the accumulated hole density at the C:GaN/SL interface (TR2).

4.5.2 Substrate Stress Bias Dependence

To investigate the V_B dependence of the two transients, tests have been performed at T =- 20^oC in order to have TR1 and TR2 quite distant from each other and to measure a bigger excursion of TR1. Fig. 4.7 (a) shows the amplitude A_1 of TR1 as a function of $|V_B|$. Two regimes can be observed. For $|V_B| \leq 50V$, A_1 is roughly constant and quite small, smaller than A_2 [Fig. 4.7 (b)]. In this region, the electron trapping during the stress can be compensated and/or perturbed by the mechanism inducing hole accumulation at the C:GaN/SL interface, i.e., band-to-band electron tunneling from C:GaN VB to 2DEG. Electrons tunneling releases free holes in the VB, which can accumulate at the C:GaN/SL interface as free charge or neutralize the acceptor states [6], opposing the increase of A_1.

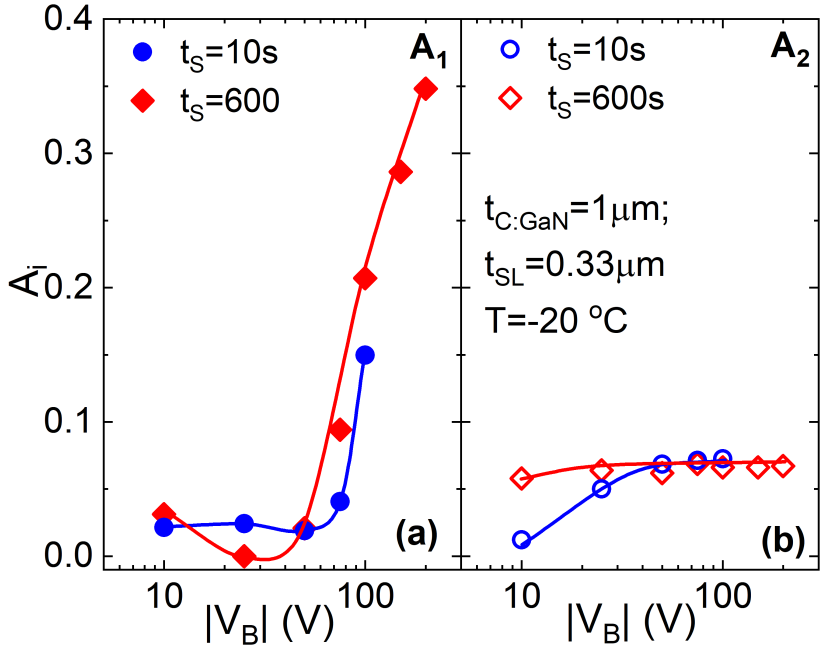

Figure 4.7: *Stressing voltage dependence of A_i for: (a) TR1 and (b) TR2.*

For $|V_B| > 50V$, A_2 saturates (also for short t_S) while A_1 increases with $|V_B|$ becoming bigger than A_2. In this scenario, during the stress phase,

leakage may initiate across the entire epi-stack. Electrons are injected from the substrate, and there's a saturation of hole accumulation at the C:GaN/SL interface, as well as A_2. On the other hand, more electrons can be trapped in the C:GaN layer because of the higher electric field, increasing A_1. The latter mechanism is further supported by TCAD simulations reported and discussed in the next section.

Fig. 4.8 (a) reports the V_B-dependence of β. β_1 decreases by increasing $|V_B|$, except for low $|V_B|$, whereas β_2 is bias independent. As reported in [20], when the stretched exponential model is adopted to fit the effects of trapping/de-trapping mechanisms, β can represent the energy window of the trap involved in the mechanisms. A value close to 1 implies that the trap behaves like a point defect with a discrete energy level, whereas a smaller β is associated with trapping centers forming a continuous distribution of energy levels.

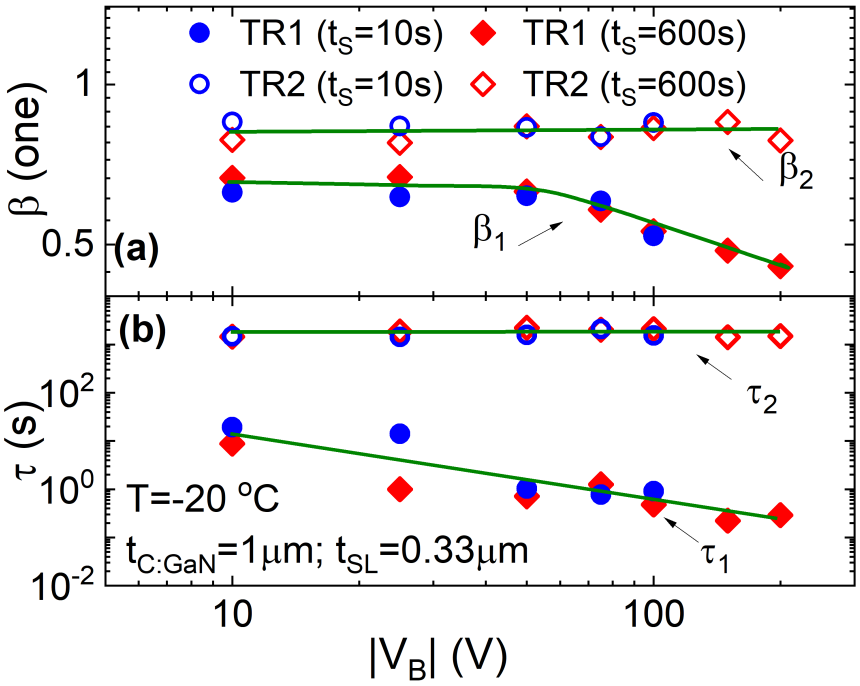

Figure 4.8: *Stressing voltage dependence of: (a) stretching term β and (b) trap emission time for both transients.*

Based on this assumption, the smaller β_1 by increasing $|V_B|$, reported in Fig. 4.8 (a), may be the result of charge trapping during the stress in a wider energy window centered at $\sim$ 0.9 eV. On the contrary, the lack of V_B-dependence of β_2 further supports that TR2 is not linked to charge

detrapping mechanisms but to the recombination of holes accumulated at the C:GaN/SL interface. The two mechanisms are further supported by the V_B-dependence of τ_1 and τ_2 reported in Fig. 4.8 (b). Also in this case, τ_1 is stress bias-dependent while τ_2 is not, confirming and excluding trapping/detrapping mechanisms for TR1 and TR2, respectively.

4.5.3 Stress Time Dependence

Fig. 4.9 reports the stress time dependence of the A_i parameters for three different V_B. As anticipated in the previous subsection, as long as A_1 remains smaller than A_2 (with $|V_B| < 50V$), the behavior exhibited by A_1 concerning both stress bias, as depicted in Figure 4.7 (a), and stress duration, as demonstrated in Figure 4.9 (a), exhibits a non-monotonous trend.

This non-monotonic behavior can be attributed to the intricate interplay of the two competing mechanisms occurring during the stress phase, i.e., ionization and neutralization of acceptor states in the C:GaN layer, caused by the electric field and by free hole releasing (electron band-to-band) in the VB, respectively. It is worth noting that non-monotonic trends in R_{ON} drift have also been reported previously in [43].

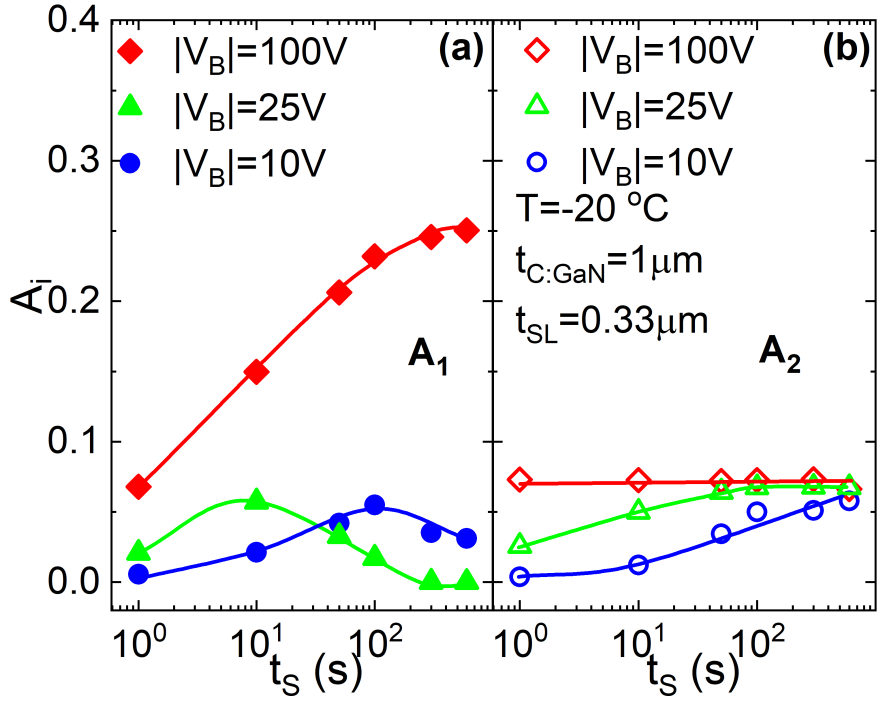

Figure 4.9: *Stress time dependence of A_i in the case of: (a) TR1 and (b) TR2. The temperature is -20°C.*

For $|V_B| > 50V$, A_2 is already saturated while A_1 increases hinting at a saturation for relatively long stress times ($\sim$ 600 s with $|V_B| = 100$ V). Such behavior is in line with what is often observed in trapping mechanisms associated with preexisting defects in semiconductor devices. Finally, as expected, the stress time has no impact on β and τ, as reported in Fig.4.10 (a) and (b), respectively.

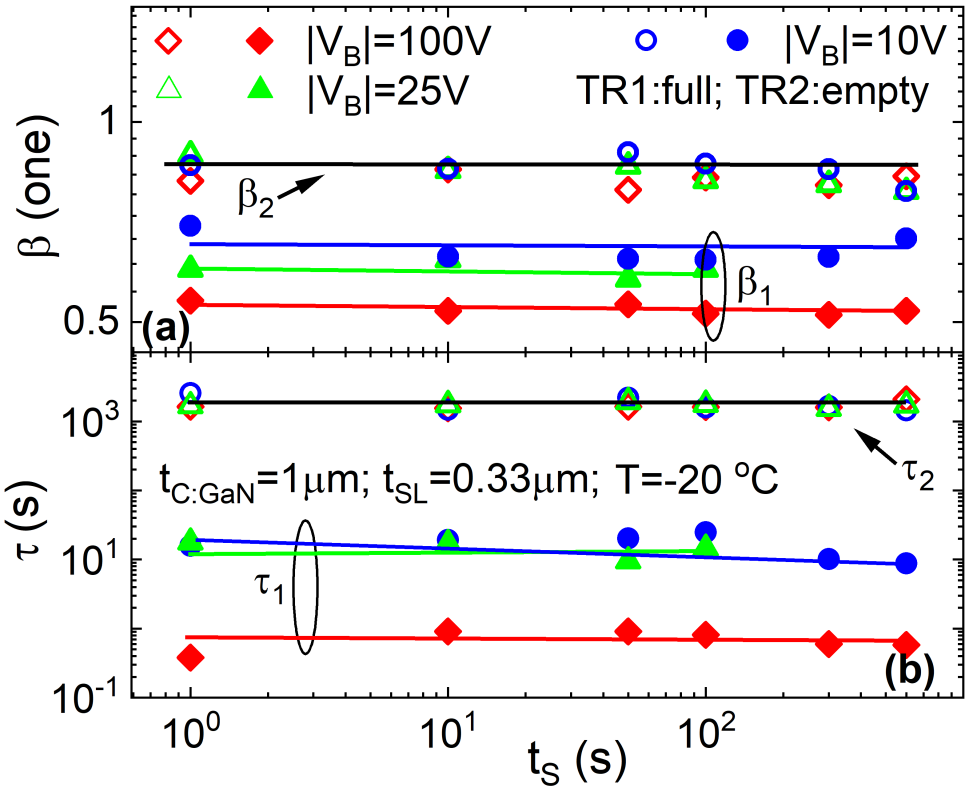

Figure 4.10: *Stress time dependence of: (a) stretching parameter and (b) trap emission time for both transients. The temperature is* -20^oC.

4.6 Role of the Buffer Stack Composition

After a comprehensive investigation of the influence of various stress conditions, the study proceeds to analyze and compare structures featuring different epi-stacks.

Fig. 4.11 (a) shows I_N in the case of structures with different AlGaN barrier configurations, which vary in terms of thickness and aluminum content (Al%). As observed, both parameters do not significantly impact on the current transients. This observation strongly suggests that the under-

lying mechanisms responsible for the observed behavior are not primarily associated with the AlGaN barrier or its interfaces.

Fig. 4.11 (b) reports the same analysis carried out on structures with different AlN nucleation layer thicknesses. A negligible impact is shown also in this case, excluding such layer as location of trapping/accumulation mechanisms.

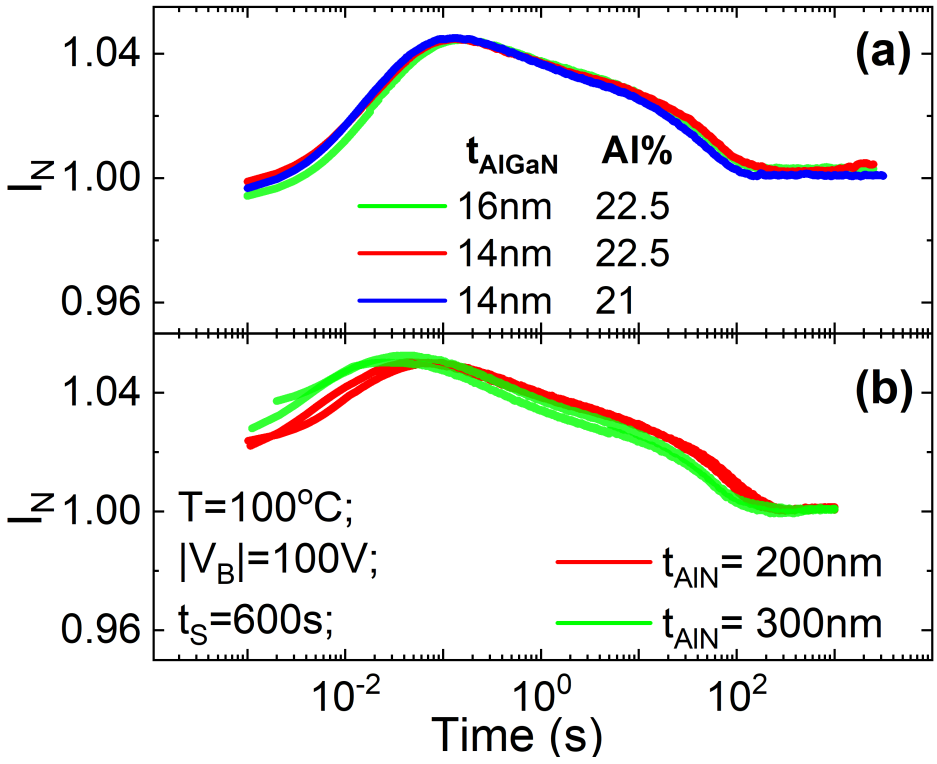

Figure 4.11: *Dependence of I_N in the case of: (a) different AlGaN barrier configurations and (b) AlN thicknesses. Test condition is $T = 100°C$, $t_S = 600$ s, and $|V_B|$=100 V .*

Given that the charge storage and release mechanisms are linked to the C:GaN layer, a detailed analysis of these mechanisms was conducted by varying the thickness of this layer as well as that of the SL layer.

First, a tempereture dependent analysis has been carried out with bias voltage of 200 V and stress duration of 600 s. The Arrhenius plot in Fig. 4.12 shows that the activation energies associated with TR1 and TR2 are unimpacted neither by SL nor by C:GaN thickness, suggesting that the kind of storage/release mechanisms are always the same, whatever the buffer configuration is.

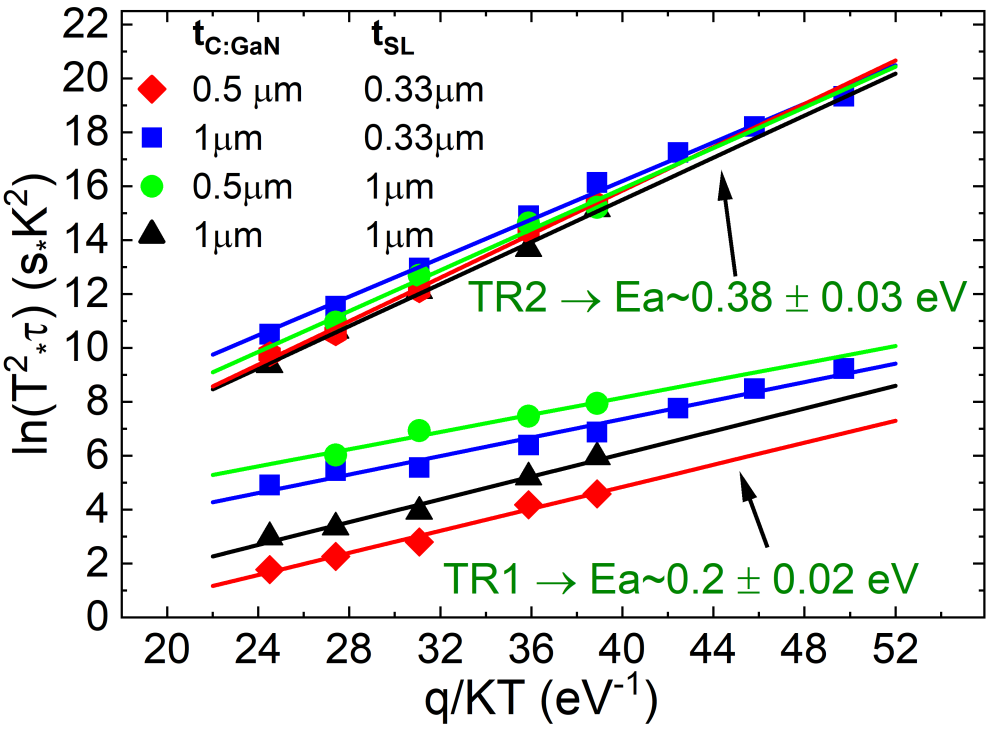

Figure 4.12: *Arrhenius plot in the case of stress voltage $|V_B|$= 200 V, with a stress time of 600 s in the case of different process splits.*

To investigate the role of the two layers on TR1 and TR2, the amplitudes A_1 and A_2 have been analyzed for each split as a function of $|V_B|$ and reported in Fig. 4.13 (a) and (b), respectively.

By focusing on TR1 [Fig. 4.13 (a)], thus on the electron detrapping from carbon-related acceptor states in the C:GaN layer, two trends can be observed:

- A thicker GaN:C back-barrier induces a higher A_1, meaning that a higher number of acceptor traps that are ionized. This is confirmed on both SL splits (i.e. 0.33 μm and 1 μm);
- A thinner Super Lattice buffer leads to higher amplitude of TR1 possibly induced by a higher number of of trapped electrons in the C:GaN layer. The trend is observed on both C:GaN splits (i.e. 0.5 μm and 1 μm).

To better understand such experimental evidences, TCAD simulations have been performed by introducing an acceptor states concentration of $5 \cdot 10^{18} cm^{-3}$ at 0.9 eV from the VB in the C:GaN layer, which is similar to

carbon concentration adopted during the epitaxial growth. In addition, donor traps with concentration of $2 \cdot 10^{18} cm^{-3}$ at 0.4 eV from the conduction band in the C:GaN layer have been used to replicate the generation of such trap states due to the presence of carbon atoms occupying gallium sites.

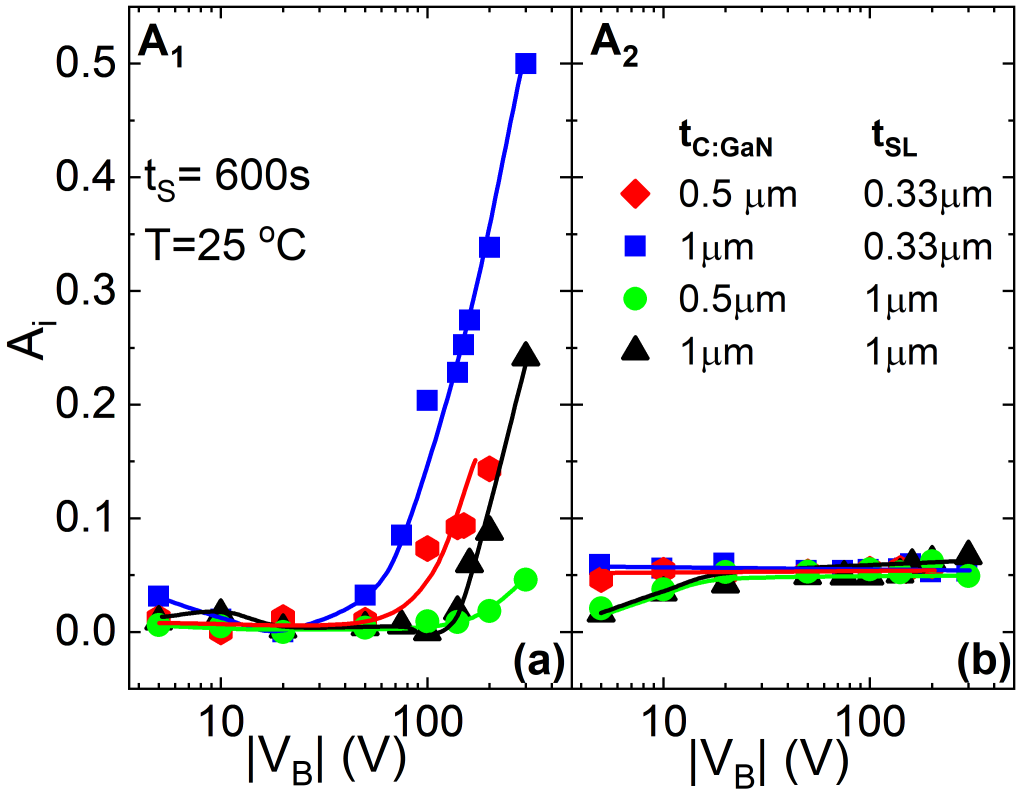

Figure 4.13: *Stress voltage dependence of A_i in the case of: (a) TR1 and (b) TR2 for different process splits. The test condition is $T = 25^oC$ and $t_S = 600$ s.*

Fig. 4.14 (a) reports the electron trapped charge (eTC) density along the C:GaN and SL layers in the case of processes featuring the same and different thicknesses for SL ($t_{SL} = 330$ nm) and C:GaN ($t_{C:GaN} = 0.5$ and 1 μm) layer, respectively. A thicker C:GaN layer leads to a higher electron trapping, which in turn causes a higher ΔR_{ON} (A_1). The reason can be ascribed to a different electric field distribution ruled by a capacitance voltage divider [Fig. 4.14 (b)]. A thicker C:GaN (1 μm) gives rise to a smaller capacitance $C_{C:GaN}$, whereas the one related to the SL layer (C_{SL}) remains unchanged.

The voltage drop across the C:GaN layer ($V_{C:GaN}$) is $\sim |V_B| \cdot C_{SL}/(C_{SL} + C_{C:GaN})$), whereas the one on the SL layer (V_{SL}) is $\sim |V_B| \cdot C_{C:GaN}/(C_{SL} +$

$C_{C:GaN}$). As a result, the smaller the $C_{C:GaN}$ (thicker C:GaN), the higher the $V_{C:GaN}$, and the lower the V_{SL}. The result of such a divider is a higher electric field in the C:GaN layer [Fig. 4.14 (b)], inducing a higher amount of trapped electrons (higher A_1), as depicted in 4.14 (a).

The opposite effect is obtained by increasing the Super Lattice buffer layer thickness, i.e., the thicker the SL, the lower the voltage drop across the C:GaN layer ($V_{C:GaN}$) and related electric field, the lower the eTC. Fig. 4.15 shows the simulated ΔeTC in the C:GaN layer, calculated with respect to $V_B = 0$ V (i.e., $\Delta eTC = eTC_{|V_B|} - eTC_{|V_B|=0V}$), for all the considered process splits. The stress voltage dependence is qualitatively in agreement with the experiments [A_1 in Fig. 4.13(a)].

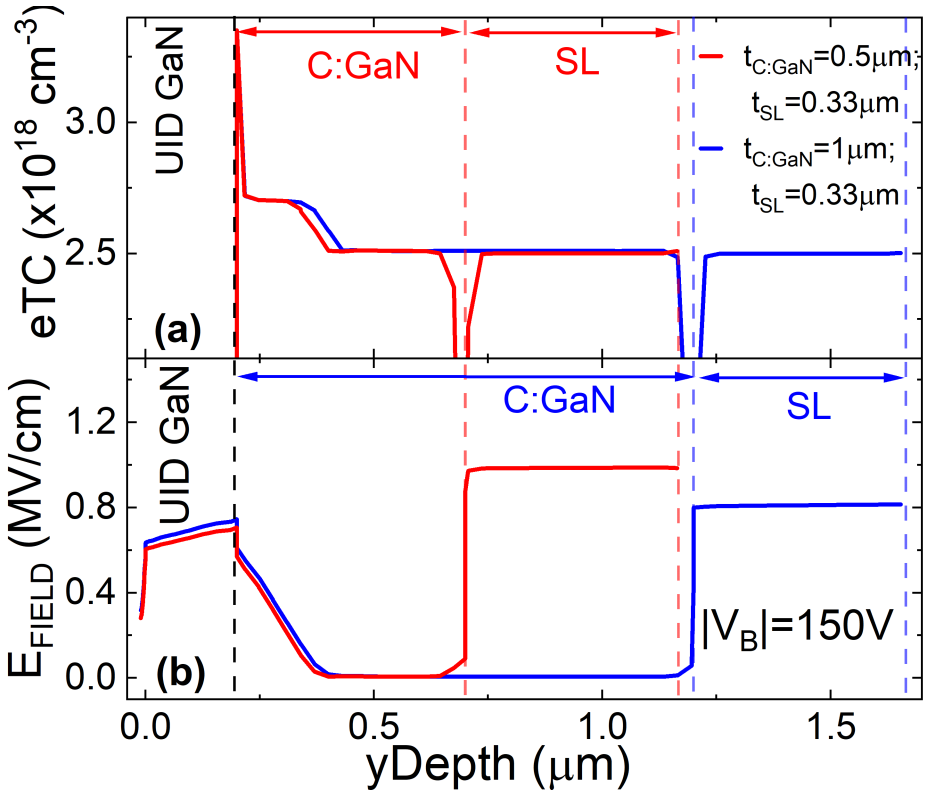

Figure 4.14: *(a) TCAD simulated eTC density along the vertical direction (y cutline) with $|V_B| = 150V$ for two structures featuring the same $t_{SL} = 330$ nm and a C:GaN layer thickness of 0.5 (red line) and 1 µm (blue line). (b) Corresponding simulated electric field.*

Concerning TR2, Fig. 4.13 (b) shows an almost V_B independent A_2, except for the low-bias regime where hole accumulation is not saturated yet (see subsection 2.5.2), even for relatively long t_S. In such a case, a thicker SL

helps to significantly reduce the electric field along the uid-GaN and C:GaN layers, weakening the electron band-to-band tunneling and giving rise to a smaller A_2 [Fig. 4.13 (b)].

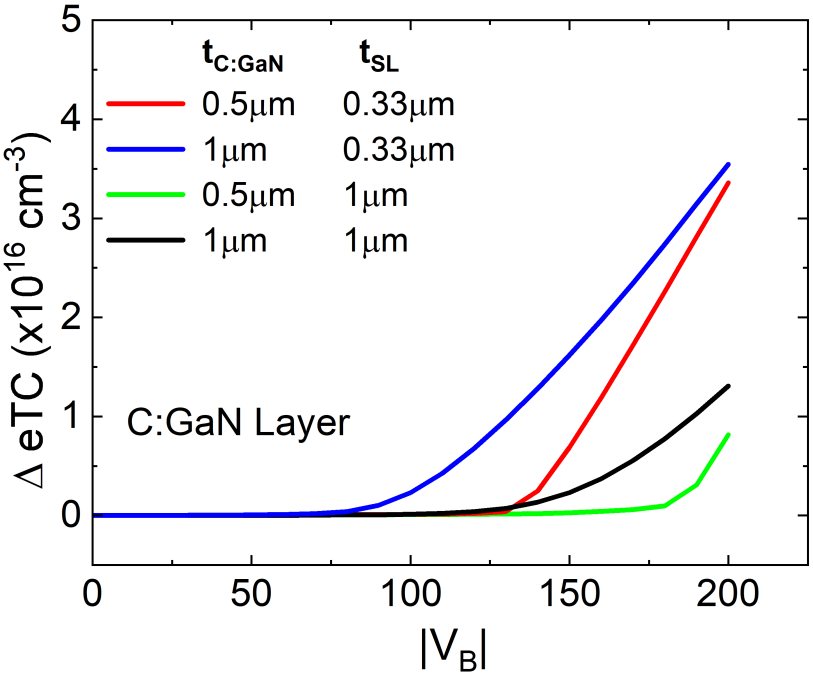

Figure 4.15: *(Quasi-stationary simulation of the eTCs density variation ($\Delta eTC = eTC_{|V_B|} - eTC_{|V_B|=0V}$) as a function of $|V_B|$ for different process splits.*

4.7 Conclusion

An in-depth analysis of the role of both test conditions and epi-stack buffer of GaN-on-Si devices on the mechanisms inducing ΔR_{ON} has been investigated by means of back-gating current deep-level transient spectroscopy tests. The after-stress monitored current shows two different trends: an initial transient (TR1) characterized by an ascending trend, followed by a subsequent transient (TR2) displaying a descending trend. According to the state-of-the-art, the first one is ascribed to electron trapping/detrapping in carbon-related acceptor states located in the C:GaN layer, whereas the second one can be associated with hole accumulation at the C:GaN/SL heterointerface.

Such transient are usually fitted as sum of stretched exponentials which time constants can be close each other and making it difficult to distinguish between the two transients. For this reason, for the first time, a genetic

algorithm has been employed to accurately fit the experiments allowing the investigation of the temperature, stress-bias, and stress-time dependence of the representative parameters (A, β, and τ), hence, of the physical mechanisms.

The following dependencies have been observed:

- Temperature dependency: both mechanisms result to be thermally activated with activation energies of 0.2 eV and 0.38 eV for TR1 and TR2, respectively;

- Voltage dependency: for $|V_B| < 50V$ A_1 is small and approximately constant while the amplitude of the second transient shows an increasing trend with $|V_B|$. For $|V_B| > 50V$ the higher the stressing voltage the higher the number of ionized traps ascribed by the increase of TR1 amplitude whereas, TR2 results to be saturated (no more holes can accumulate at the C:GaN/SL heterointerface).

- Stress Time dependency: the longer the stress time the higher the first transient amplitude but only after A_2 saturation, i.e., for $|V_B| > 50V$. For lower voltages (when A_2 is still not saturated) A_1 shows a non-monotonous trend with the stressing time possibly due to the interaction between the mechanisms.

A further novelty of this work relies on the study of the role of the buffer epi-stack, reporting that both mechanisms do not show dependence on the kind of adopted AlGaN barrier (neither thickness nor Al%) and on the thickness of the AlN nucleation layer. In addition, the second mechanism is almost insensitive also to C:GaN and SL thickness, except for low $|V_B|$, whereas the electron trapping in acceptor states is clearly depending on these layer thicknesses, providing useful information for the epi-stack optimization, i.e., vertical scaling down. In particular, a thinner C:GaN layer and a thicker SL layer turn out to be the best choice to attenuate the ΔR_{ON} induced by charge storage/release mechanisms, triggered by OFF-state voltage, in the buffer epi-stack.

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Chapter 5

Conclusions

With the spreading of power electronics in many application fields, the need of power transistors even more energy-efficient, cost-effective and reliable is becoming of paramount importance. Regarding the latter attribute, for power devices, it is of paramount importance due to the demanding operational conditions they encounter in real-world applications (as reported in Chapter 1). Specifically, these devices find application in switching mode converters, where they are continuously subjected to elevated voltages, currents, temperatures and frequencies. For this reason, the interest from both academic research groups and companies in semiconductor technologies capable of withstanding such challenging conditions has seen remarkable growth in recent years. In this scenario, GaN-on-Si high-electron mobility transistors are of great interest due to their capability to operate at relatively high voltage and frequency with higher efficiency and comparable cost of the silicon counterparts. Anyway, as any novel technology, GaN transistors demonstrate there are still prone to many degradation mechanisms, affecting the device performance and reliability, that need further investigation and understanding.

This thesis focused on the the gate reliability of p-GaN power HEMTs, which is of paramount importance since the complexity of the gate stack of such devices introduces degradation mechanisms not observed in devices based on a MOS (metal-oxide-semiconductor) structure. The investigation of the physical mechanism affecting the gate lifetime has been carried out by means of field- and temperature-accelerated tests and TCAD simulations. Moreover, the thesis provides an in-depth investigation of the ON-resistance degradation triggered by charge trapping/de-trapping processes occurring in the buffer epi-layers of such technology.

In chapter 2, an in-depth examination of the time-dependent gate breakdown of p-GaN HEMTs under DC conditions has been presented, with the

objective of comprehending failure mechanisms affecting such technology. By performing constant voltage stress test under different conditions (temperature and bias) on devices featuring different processes and gate area, two failure mechanisms have been identified. The first one, occurs in a localized position, i.e., where the gate metal finger intersects the N-implanted isolated region. Such mechanism does not show any gate width and/or length dependency. The other breakdown process occurs along the active area showing clear gate dimension dependency. Depending on the gate bias and temperature, one mechanism can be predominant with respect to the other. In particular, the gate time-to-failure (TTF) exhibits a non-monotonic trend with the temperature at given gate bias. Specifically, positive T-derivatives correspond to active gate area related failure and it has been observed at relatively low temperatures. On the contrary, at higher temperatures, isolation breakdown results to be predominant showing a weak negative temperature trend with activation energy of 0.14 eV. Moreover, it has been observed that the smaller the gate area the higher the temperature at which the isolation failure shows up. Furthermore, the occurrence of the failure mechanisms strongly depends on the range of gate bias employed during stress testing. Specifically, when subjected to relatively high gate voltages, area-dependent failure becomes prevalent, while at lower voltages, isolation breakdown occurs. Finally, two distinct voltage dependencies were observed, one for each failure mechanism, which required the adoption of two different field-acceleration fitting models for accurately predicting the gate's lifetime in each scenario.

In chapter 3, the long-therm gate reliability of p-GaN HEMTs has been evaluated with a different approach, i.e., by means of applied consecutive square-waves (pulsed stress condition) instead of constant voltage stress. Results demonstrated that, two main factors determine the TDGB under AC conditions: the switching phase (number of applied pulses) and the time during which the device is kept in ON-state, plus a possible recovery mechanism occurring during the off-time. It has been found out that, the amount of degradation induced by pulsed stress is due to the current peaks at the switching phases (from ON- to OFF-state and viceversa) and by electrostatic potential peaks in the semi-floating p-GaN layer during the rise time (transition from OFF- to ON-state). The magnitude of the latter strongly depends on the OFF-time, i.e., it decreases by shortening the OFF-time. As a consequence, the voltage drop on the Schottky depletion region, hence electric field, increases during the transition phase by reducing the OFF-time, inducing a consequent TTF reduction. On the other hand, the current peak height at both transition phases is influenced by the slew rate. The longer the slew rate, the lower the amplitude of such current spikes, the longer the TTF. All these statements, resulting from this analysis, have been supported

by TCAD simulations which have found a good agreement with the experimental evidences. Subsequently, the analysis has been extended in order to explore how the gate robustness is affected by both the switching frequency (from 100 kHz to 1 MHz) and the duty cycle (from 10% to 90%). Experimental results show that the Time-to-Failure decreases by increasing the frequency and/or the duty cycle, since they induce a shortening of the OFF-time of the square-wave applied to the gate, which in turn alters the electrostatic potential of the semi-floating pGaN layer during the switching phases. In addition, a comparison between gate lifetime extrapolated under DC and pulsed stress conditions has been reported. In particular, depending on the switching conditions (frequency and duty cycle), the AC gate lifetime can be longer or shorter when compared with the DC case. The findings of this analysis highlight the importance of evaluating the reliability of semiconductor devices in conditions as close as possible to those in which they operate in a real application.

The last research activity, reported in chapter 4, focuses on the ON-resistance degradation mechanisms ascribed to charge storage/release occurring along the buffer layers. By performing back-gating current deep-level transient spectroscopy tests, two main trapping/de-trapping mechanisms have been identified: i) electron trapping/detrapping in carbon-related acceptor states located in the C:GaN layer and ii) hole accumulation at the C:GaN/SL heterointerface. The latter causes a reduction of ON-resistance, while i) induces an ON-resistance increase. Usually, the time constants of such processes, observed as current transients, can be close to each other, making it difficult to clearly distinguish them. For this reason, a genetic algorithm has been used to fit the experimental data, allowing an accurate understanding of the temperature, stress-bias, and stress-time dependence of the physical mechanisms. Moreover, the effect of the buffer epi-stack composition on the ON-resistance shift has been investigated. In particular, both mechanisms do not show any dependence on the characteristics of adopted AlGaN barrier (neither thickness nor Al%) and on the thickness of the AlN nucleation layer. On the contrary, mechanism i) results to be strongly impacted by both C-doped GaN back-barrier and super lattice buffer thickness, whereas, ii) is almost insensitive to the dimensions (thicknesses) of such layers. In conclusion, a thinner C:GaN layer and a thicker SL layer turn out are preferable in order to attenuate the ON-resistance shift induced by charge storage/release mechanisms in the buffer epi-stack. Such results, provides useful information for the epi-stack optimization, i.e., vertical scaling down of GaN/AlGaN power HEMTs.