ALMA MATER STUDIORUM
UNIVERSITÀ DI BOLOGNA

DOTTORATO DI RICERCA IN
Ingegneria Biomedica, Elettrica e dei Sistemi

CICLO 36°

Settore Concorsuale: 09/E4

Settore Scientifico Disciplinare: ING-INF/07

TITOLO TESI

Development and Characterization of Cutting-Edge Equipment for EMC Measurements and Advanced Power Line Filter Design

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Esame finale anno 2024

Abstract

This Doctoral Thesis aims at studying, developing, and characterizing cutting edge equipment for EMC measurements and proposing innovative and advanced power line filter design techniques.

This document summarizes a three-year work, is strictly industry oriented and relies on EMC standards and regulations. It contains the main results, findings, and effort with the purpose of bringing innovative contributions at the scientific community.

Conducted emissions interferences are usually suppressed with power line filters. These filters are composed by common mode chokes, X capacitors and Y capacitors in order to mitigate both the differential mode and common mode noise, which compose the overall conducted emissions.

However, even at present days, available power line filter design techniques show several disadvantages. First of all, filters are designed to be implemented in ideal 50 Ω systems, condition which is far away from reality. Then, the attenuation introduced by the filter for common or differential mode noise is analyzed independently, without considering the possible mode conversion that can be produced by impedance mismatches, or asymmetries in either the power line filter itself or the equipment under test. Ultimately, the instrumentation used to perform conducted emissions measurement is, in most cases, not adequate. All these factors lead to an inaccurate design, contributing at increasing the size of the filter, making it more expensive and less performant than it should be.

The objectives of this Doctoral Thesis are to:

1. Present an extensive overview of existing receivers' architectures, outlining their main advantages and disadvantages while focusing on achieving an optimal power line filter design.
2. Propose a new characterization methodologies and techniques to model the measurement set up and evaluate its uncertainty.
3. Propose a new methodology to accurate design a single-phase power line filter based on accurate insertion loss estimations, validated both from simulations and in-field measurements.
4. Propose a new methodology to evaluate the modal noises generated by a three-phase equipment as well as proposing a reliable procedure to design an optimal three-phase power line filter, validated both by simulations and in-field measurements.
5. Contribute to spread the work throughout the scientific community.

Structure of the Document

The work presented in this thesis has been structured as follows:

- Chapter 1: Introduction. A summary of the basic concepts, standards, state of the art and present-day problems and limitations regarding EMC measurements are described in this chapter.
- Chapter 2: A comprehensive comparison between FFT and conventional EMC receivers along with a detailed analyses of the major differences between the two architectures is presented. Furthermore, a detailed evaluation on the modal conducted emissions and methods to extract this information, as well as the limitations involved, is carried out.
- Chapter 3: In this chapter, the basic principles of uncertainties are introduced as well as a methodology to reduce the computational time to estimate the uncertainty of the measurand while considering different influence factors is proposed. Then, the evaluation of the uncertainty of the input measurement chain of a commercial EMI receiver is carried out.
- Chapter 4: A methodology for the optimal design of power line filters for single phase equipment based on accurate insertion loss estimation is presented. This is, along with a complete characterization of the device under test, including its parasitic parameters, and a complete knowledge of the overall conducted emissions and modal measurements.
- Chapter 5: A methodology for the optimal design of power line filters for three phase equipment based on accurate insertion loss estimation is presented. Including a review of the three-phase modal definition, focusing on common mode and differential mode current behavior. In this chapter, an overview of the available measurement instrumentation is proposed along with the state-of-the-art technology. Then, the optimal power line filter is designed by accurate insertion loss estimation after performing a complete characterization of the equipment under test.
- Chapter 6: Conclusions and future work. In this chapter, a summary of the overall work as well as future objectives is presented.
- Bibliography. All the references of this thesis can be found in this section.

Acknowledgements

First thank goes to my supervisor Lorenzo Peretto who gave me the opportunity to pursue this PhD. I have learnt a lot from him, not just in the technical area. Without his support, this project would have never started.

Second thank goes to Ernest Cid and Jordi Accensi for letting me pursue this industrial PhD while working at Wavecontrol SL.

A special thank goes to Francisco Javier Pajares and Albert-Miquel Sanchez for all the help, suggestions, writing, correcting and patience that they had during these years.
Especially without the help of Albert-Miquel, none of the work done would have ever been possible.

Last, but definitely not least, particular thanks go to my mother Monica, my father Claudio and my brother Nicoló for their patience, love and support even if distance separates us, my grandmother Dorina, which at the time of writing these sentences is fighting a hard battle, and to my girlfriend Cristina for her support and love.

Thanks for always believing and loving me through my career.

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Acronym Glossary

ADC	Analog-to-digital converter
AMN	Artificial mains network
AVG	Average
CE	Conducted emissions
CTL	Central limit theorem
DDC	Down-converter
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
EUT	Equipment under test
FFT	Fast-Fourier-transform
GUM	Guide to the Expression of Uncertainty in Measurement
IIR	Infinite impulse response
IL	Insertion loss
LISN	Line impedance stabilization network
MCM	Monte Carlo Method
NPS	New product development
PDF	Probability distribution function
PE	Protective earth
PK	Peak
PLF	Power line filter
PLN	Power line networks
PSD	Spectral density
QPK	Quasi-Peak
RBW	Resolution bandwidth
RF	Radio frequency
S parameters	Scattering parameters
SMPS	Switched-mode power supply
STFFT	Short-time fast-Fourier transform
TOSM	Through-open-short-match
VNA	Vector Network Analyzer

CHAPTER 1

1. Introduction

The electromagnetic compatibility (EMC) compliance of any electric or electronic device is a basic worldwide requirement. EMC standards establish testing methods, requirements, and limitations that the equipment must comply to ensure that does not disturb or get disturbed by other equipment, for example radio and telecommunication, during its normal functioning [1-3].

Furthermore, EMC compliance is fundamental to guarantee the performance, safety, and quality of most of electric devices.

However, due to the exponential rise in development of new electronic products, designing a product compliant with EMC requirements is becoming a major challenge. This problem gets aggravated even worse when the technologies evolves faster than the corresponding EMC standard [1-8].

Nowadays, accredited EMC labs need to attend to several customers, basically all manufacturers of commercial electric/electronic devices, which are pressured to get their products CE marked in order to launch them into market as fast as possible. At the time of writing this thesis, a global crisis of the semiconductor supply chain affected the whole world. This had a direct effect in EMC testing world as well since:

a. Several equipment had to be redesigned because certain components could not be sourced anymore (or lead times were extremely long).
b. Every re-designed equipment had to be retested to guarantee EMC compliance before it could be sold.

Forced by the long waiting times of accredited EMC labs, most companies developing electric or electronic products, increased their internal capability to perform EMC testing throughout new product development (NPD) and prototype development. In these phases, most EMI tests, mainly conducted immunity and emissions, are performed to determine if the equipment under test (EUT) meets the limits set by the relative product standard.

As a result, it is becoming increasingly essential to develop enhanced and precise measurements techniques with shorter testing duration and able to provide cost-efficient designs. Hence, the objective of this thesis is to improve the efficiency of EMC testing, especially for conducted emission (CE) measurements. Additionally, it aims at offering accurate and optimal techniques for power line filter (PLF) design, with the purpose of reducing the products overall cost and expediting their time to market.

1.1 Signal characterization

1.1.1 Power line Networks

Electrical distribution networks, which firstly appeared at the end of XIX century, have strongly evolved throughout the years according to the needs of each country. Hence, nowadays the worldwide power distribution network shows different characteristics. For instance, Europe has a 50 Hz and 230V system, while USA has a 110 V and 60 Hz one [9]. Despite the differences, both single phase power line networks (PLNs) are constituted by a three-conductor structure (line, neutral and ground), while three phase PLNs are constituted of a five-conductor structure (three phases, neutral and ground). In a three-phase system the sinusoidal voltages are 120 ° shifted between each other’s. In most of the cases, the high and medium voltage distribution is done though three-phase systems. While for residential and small/medium commercial entities, a single-phase supply is usually provided. Hence, the majority of electric or electronic devices are connected to this network [9].

1.1.2 Interference Signals characterizations

A single-phase PLN is composed by three conductors; line (L), neutral (N) and the protective earth (PE), commonly referred as ground (G).

The are different ways to characterize the noise which can interfere with the common operation of any electric device connected to the PLN. This can be classified as [10,11]:

- Narrow band noise: radiated signal coming from broadcast station can couple and cause unwanted sinusoidal interferences.
- Background noise: wide-band interference cause by different noise sources with low spectral density (PSD).
- Impulsive noise; short time interference, usually with a duration lower than 100 µs. They can be further characterized, according to the repetition frequency:
    - Periodic impulsive noise synchronous with the mains frequency: characterized by a repetition rate of 50 Hz or 100 Hz. Mainly caused by rectifier stage of the power supply.

    - Periodic impulsive noise asynchronous with the mains frequency: characterized by a repetition rate between 50-200 kHz. Mainly caused by switching power supplies.
    - Asynchronous impulsive noise: characterized by a random nature. Can be cause by the connection and disconnection of devices from the PLN.

The conducted emissions measurements generated by an electronic device are measured between lines and neutral terminals with respect to ground. Usually, they are a combination of signals of different nature, hence a slightly different classification based on the signal statistical behavior is required [12]:

- Stationary: narrow band emission and background noise
- Quasi stationary signal: periodic impulsive noise and asynchronous with the mains frequency
- Nonstationary signal: asynchronous impulsive noise

1.1.3 Signal characterization

Any signal can be characterized in the following ways:

- EMI:
    - For single phase applications: by considering the physical voltages between L and G (V_L) and N and G (V_N) and the currents flowing though L (i_L) and N (i_N).
    - For three phase applications: by considering the physical voltages (V_i) for i=1,2,3 and the currents i_i for i=1,2,3 following though each phase [13-16].
- Modally:
    - For single phase applications: considering the proposed modal decomposition, which is, common mode (CM), along with its voltage and current (V_{CM} and i_{CM}) and differential mode (DM), along with its voltage and current (V_{DM} and i_{DM}) [13-16].

The relationship between voltages is:

$$V_{CM} = \frac{V_L + V_N}{2}; \tag{1.1}$$

$$V_{DM} = V_L - V_{N;} \tag{1.2}$$

While the relationship between currents is:

$$i_{CM} = i_L - i_N; \tag{1.3}$$

$$i_{DM} = \frac{i_L + i_N}{2}; \tag{1.4}$$

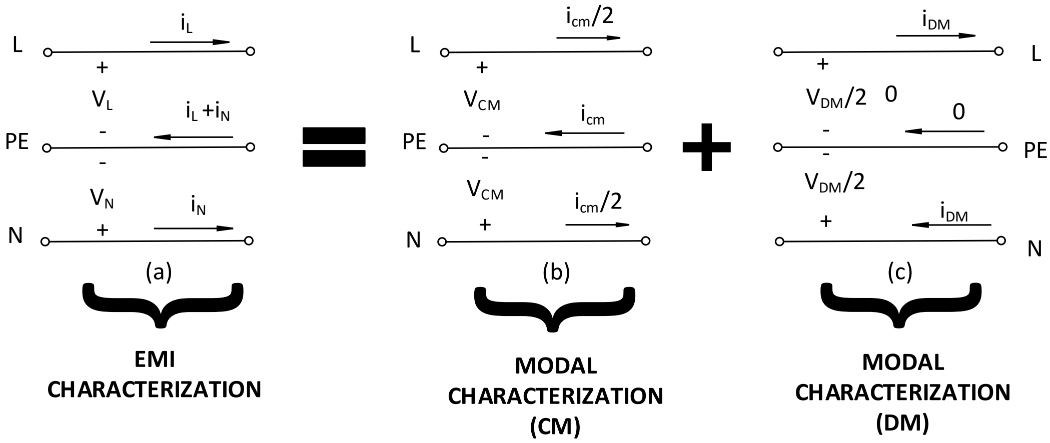


Figure 1.1: Decomposition of the circuit voltages and currents (a) for a single phase EUT into its modal components; CM (b) and the DM (c).

- For three phase applications: considering the proposed modal decomposition, which is, common mode (CM), along with its voltage and current ($V_{CM}$and i_{CM}) and differential mode (DM) , along with its voltage and current ($V_{DM,i}$and $i_{DM,i}$) for i=1,2, 3 [17-18].

The relationship between voltages is:

$$V_{CM} = \frac{V_1 + V_2 + V_3}{3}; \tag{1.5}$$

$$V_{DM,i} = V_i - V_{CM}; \quad \text{for i=1,2,3} \tag{1.6}$$

While the relationship between currents is:

$$i_{CM} = i_1 + i_2 + i_3 \tag{1.7}$$

$$i_{DM,i} = i_i - \frac{i_{CM}}{3}; \quad \text{for i=1,2,3} \tag{1.8}$$

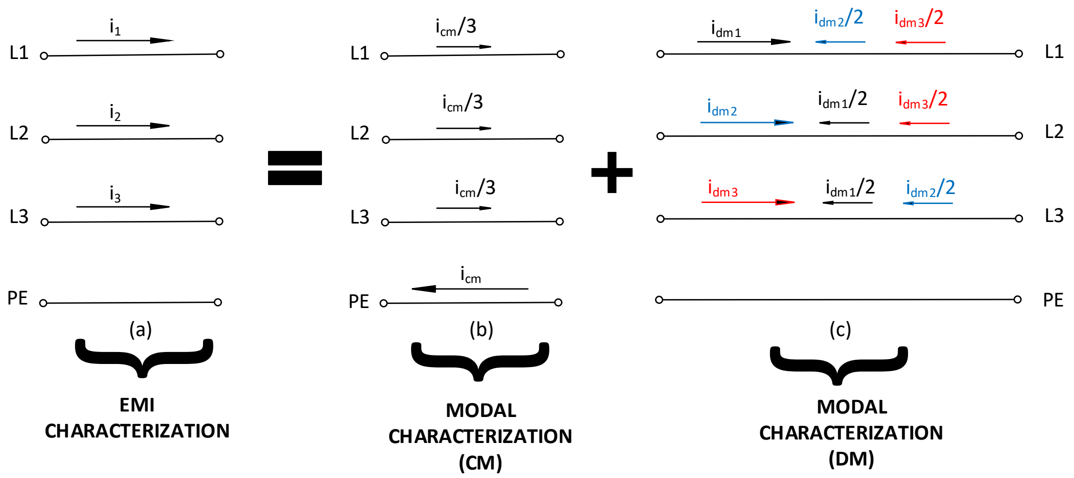


Figure 1.2: Decomposition of the circuit voltages and currents (a) for a three phase EUT into its modal components; CM (b) and the DM_i (c).

For the sake of exemplification, voltages relationships are not shown here, and will be shown throughout Chapter 5.

1.2 PLF Structure

Conducted emissions are reduced by means of power line filters (PLFs) connected between the equipment under test (EUT) and the PLN in order to avoid that the emitted interference goes into the network, as shown in Figure 1.3 [13-16].

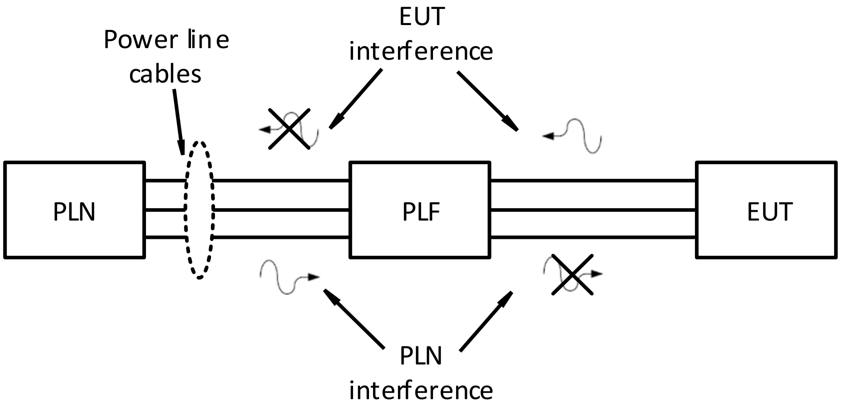


Figure 1.3: A PLF connected between EUT and PLN

1.2.1 Single Phase PLF

The simplest and more standard structure is shown in Figure 1.4 consist of a capacitor placed between L and N (commonly called C_x capacitor) with the duty of filtering differential mode, a common mode choke (CMC) placed in L and N conductors with an inductance $L_1$and L_2 and mutual inductance M to mitigate the common mode noise M. A resistor (R_1) is usually added to discharge the capacitors when the voltage is disconnected.

Finally, also two capacitors placed between L and G terminals and N and ground ($C_{Y1}$and C_{Y2}), respectively) can be found to mitigate CM [16].

This is shown in Figure 1.4.

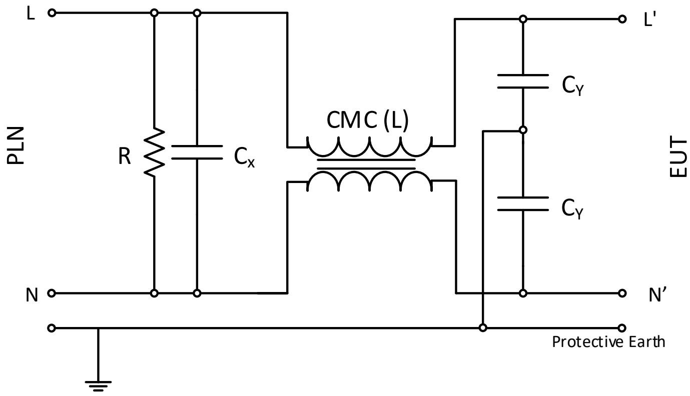


Figure 1.4: Classical structure of a PLF

Therefore, since each component present in the PLF only filters one mode, an optimal PLF (optimized both in terms of cost and size) can be designed only if the information about the modal noises in available.

1.2.2 Three-Phase PLF

The standard structure of a three-phase power-line filter contains X-type capacitors placed between the three lines and neutral, to mitigate the differential mode, and a common-mode choke and Y-type capacitors from lines and neutral to ground to mitigate the common mode noise [17-18]. A typical PLF structure used for three phase applications is shown in Figure 1.5

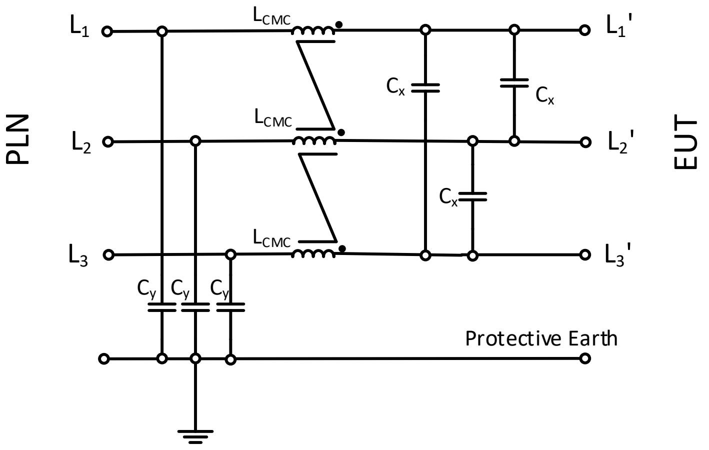


Figure 1.5: Three phase PLF consisting of three C_x, a three phase CMC and three C_y capacitors.

The filter structure shown in Figure 1.5 is composed by three C_x capacitors, forming the DM stage, while the CM stage is formed by three line-ground C_y capacitors and a three phase CMC.

1.3 PLF Characterization

Whenever is needed to introduce a PLF in order to reduce the level of the recorded CE, it is fundamental to know which PLF (or which components) needs to be implemented in order to achieve the required attenuation.

Usually, PLF manufacturers give information about the CM/DM insertion loss (IL), defined as the ratio of the voltages measured before and after the insertion of the PLF [1-3], in a 50 Ω measurement system. However, the actual impedance varies by lot from 50 Ω. Hence, the actual response of the PLF is very different from the estimated one [13-30].

Different proposals that achieve optimal designs are available in literature [13-16,19-22]. For instance, in [13-16] the IL is measured connecting the PLF directly to the EUT, while in [20-25] the IL is measured connecting the PLF to a line impedance stabilization network (LISN) to simulate the inductive impedance, which characterizes an actual PLN. However, the result obtained are valid only for a certain load impedance and can’t be used generally. Other methods base the PLF design on the minimum attenuation which can be ever achieved by the PLF [24-25]. Hence, the worst-case scenario evaluation of the IL might provide an alternative solution to the lack of knowledge which the available methodologies show.

Anyway, it is clear that such design techniques lead to an oversized and inaccurate PLF design [19-30]. An alternative methodology to evaluate the correct IL, is to characterize the impedances by means of S parameters. In this way, the impedance is completely characterized, and an accurate prediction of the IL can be achieved. The problem is that S parameters do not have direct information on CM/DM attenuation. Hence, thought this thesis, a new methodology to design optimal PLF based on accurate IL estimation, both for CM and DM, will be presented and validated both for single and three phase EUTs.

1.3.1 Common Mode Chokes (CMC)

Common mode chokes are usually designed by wounding two wires around a ferromagnetic core. In an ideal and perfectly symmetric CMC, only CM currents can saturate the CMC, as shown in figure 1.6 (a). The magnetic flux produced by the DM currents are canceled in the core and do not contribute to its saturation, as can be seen in in figure 1.6(b)). However, due to manufacturing processes, actual CMCs are not perfectly symmetric. Hence, the DM flux is not totally canceled and for high current levels, the asymmetries become important, and the non-canceled DM flux can saturate the CMC core. Saturating the core implies the reduction of its permeability, or, in other words, the reduction of the inductance and coupling inductance of the CMC [4,17-22].

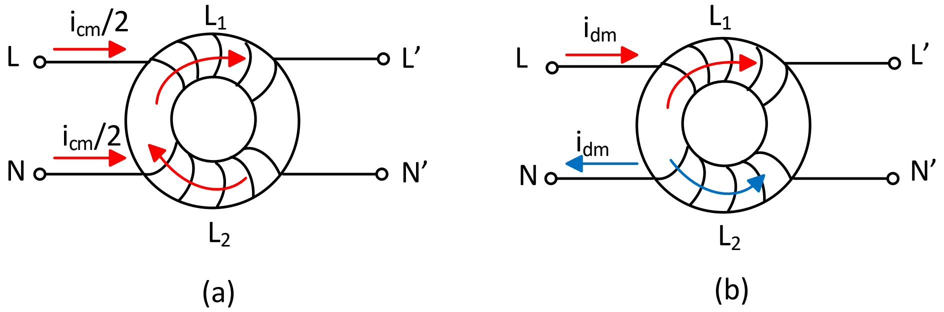


Figure 1.6: Magnetic flux direction in the ferromagnetic core due to CM currents (a) and DM currents (b).

In order to show this effect, the attenuation provided by a 2 mH CMC under different current rating has been simulated.

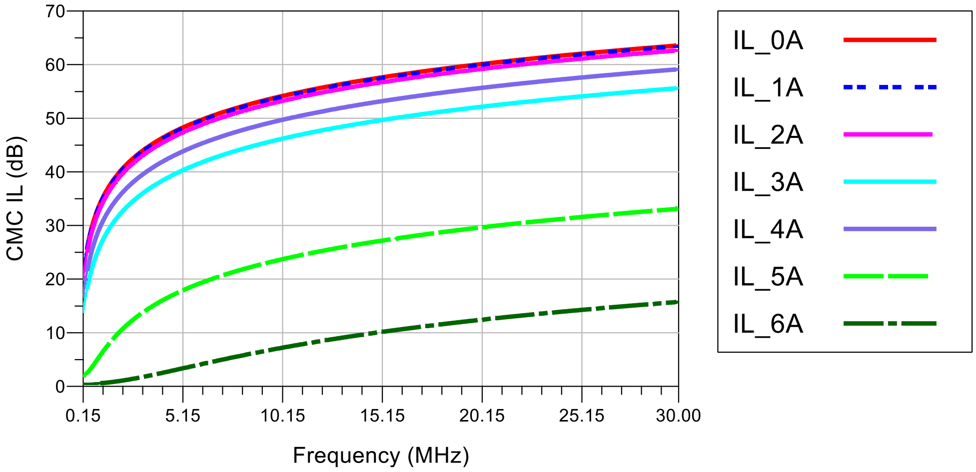


Figure 1.7: Comparison of simulated IL of a 2 mH CMC under different current levels.

As it can be seen in figure 1.7, under high current level the CM attenuation is drastically reduced due to a decrement of the inductance value.

Generally, PLFs and CMCs are not used in such stressed conditions, but in many applications they may be designed to work near saturation due to weight, size and economic scaling factors restrictions.

1.4 EMC Standard

It is well known that international EMC standards impose CE requirements to ensure that the EUT can be connected in the same network where also other devices operate. Anyway, the CE tests described in main standards, such as CISPR 11, CISPR 25 or MIL-Std-461G vary considerably. The following sections aim at clarifying their main differences between them:

- Equipment designed for civil applications, such as product for industrial, scientific, or medical environment are tested from 150 kHz to 30 MHz, according to CISPR 11 [5].
- For automotive industry the reference standard is CISPR 25, which defines a frequency range for testing from 150 kHz to 108 MHz with the voltage method [6].
- While in military standard, CE are measured by carrying out CE101 and CE102 tests in the frequency range of 30 Hz to 10 kHz and 10 kHz to 10 MHz, respectively [7].

1.4.1 Test Equipment

The basic test equipment for conducted emission test is composed by an EUT, a LISN, a transient limiter and an EMI receiver. The basic block diagram is shown in Figure 1.8.

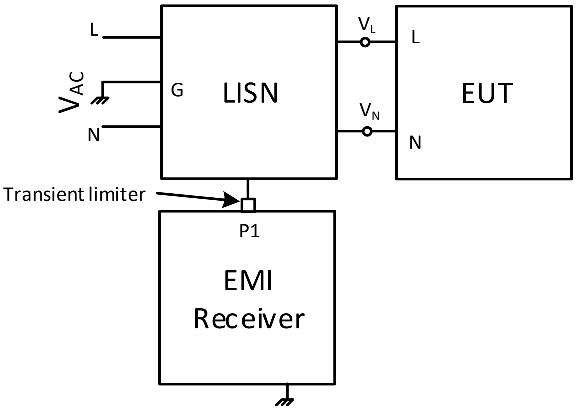


Figure 1.8: Basic set up for CE measurements.

The requirements for the receiver as described in CISPR 16-1-1 [1] will be analyzed more in detail in the Chapter 3. The other device present is the Line impedance stabilization network (LISN) or Artificial mains network (AMN). Basically, it is a passive device used to guarantee a fixed impedance during the test. This allow the CE measurement to be performed and also be reproducible. Furthermore, the LISN operated as a filter for the input voltage. As shown in Figure 1.8, the RF port of the LISN is connected to the 50 Ω input port of measurement receiver. Usually, the LISN features a switch in order to make possible to measure the conducted emissions noise of all the power supply lines.

The LISN networks indicated in different standards are not equal. Since the test frequency range differs, a different impedance in different frequency ranges is required.

In some standards, conducted emissions can be also required to be measured with current probes, which consists of several turns of wire on a ferrite core. A real current probe is shown in Figure 1.9.

Figure 1.9: Example of current probe.

Anyway, CE measurement performed with a current probe aren’t widely spread since it can vary from site to site and the PLN impedance can vary dramatically [5-6]. For that, LISN are the standard devices preferred for CE measurements.

1.4.2 Test set up

A correct test set up for conducted emissions measurements is composed by the following:

- Ground plane: usually made of galvanized steel, copper, or bronze. Shall be electrically bond to the wall and the floor of the shielded enclosure such that the DC resistance does not exceed 2-5 mΩ.
  The minimum size of ground plane is $2.25\ m^2$, $2x2\ m^2$and $1x0.4\ m^2$ for MIL STD 461, CISPR 11 and CISPR 25 standards [5-7], respectively.

- EUT and LISN: the EUT shall be placed in a non-conductive support, and at a specific height from the ground plane, 5 cm for MIL-STD-461G and CISPR 25 and 40 cm for CISPR 11. The LISN has to be placed over the ground plane and bounded to it.

- Position and length of the cables: The power leads which run from EUT to LISN power port shall be placed over a non-conductive support at a height of 5 cm above ground plane. In voltage method, the length of the power leads shall be 2 m, 1 m and 0.2 m as per MIL-STD-461, CISPR 11 and CISPR 25 standards respectively. When current method is used, the power leads shall run for 2 m and current probe has to be positioned 5cm from the LISN as per CE101 test procedure in MIL-STD-461. As per CISPR 25 standard, cable harness shall run for 1.7 m and probe has to be positioned at 5 cm and 75 cm from the EUT [6].

The set up described by the standard for conducted emissions measurements is shown in figure 1.10.

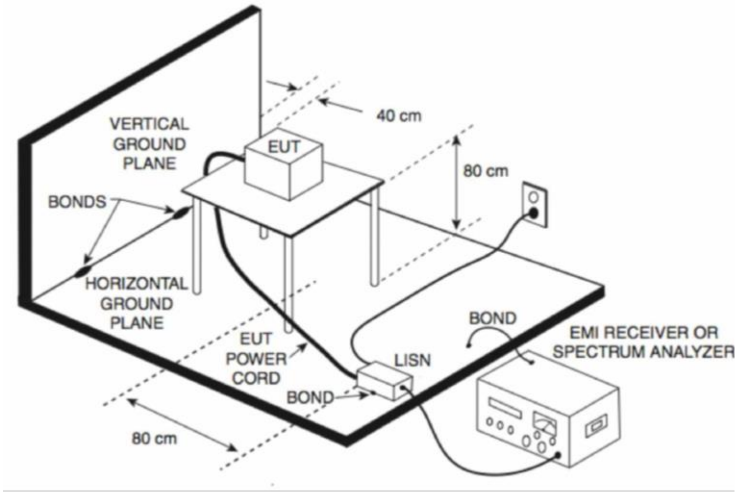


Figure 1.10: Set up for CE measurements (from EMI Pre-Compliance Testing January 16, 2020)

The following table provides an overview of the requirements depending on different standard:

Table 1.1: Summary of the specifications for each standard

Parameter	**MIL-STD-461 (CE 102)**	**CISPR 11**	**CISPR 25**
Test Frequency	10 kHz – 10 MHz	150 kHz-30 MHz	150 kHz-108 MHz
Applicability	All defense applications	Industrial, scientific and medical products	Automotive vehicles and their components or modules
Methodology	Voltage method	Voltage method	Voltage or current method
LISN	50Ω / 50µH	50Ω / 50µH	50Ω / 5µH
Ground plane requirements	• Made up of 0.25 mm thick copper or any other material with satisfying surface resistance • Area ≥2.25 m^2 with smaller side no less than 0.76 m • Surface resistance ≤ 0.1m Ω • Length to width ratio of bond strap ≤5:1 • Distance between successive bond straps: 1m	Area ≥ 2mx2 m	• Made up of minimum 0.5 mm of galvanized cooper, bronze or steel • Area ≥ 1mx0.4m • DC resistance between ground plane and shielded enclosure ≤ 2.5m Ω • Length to width ratio of bond strap ≤7:1 • Distance between successive bond straps: 0.3m
Length of power leads	≤ 2.5m	1m	0.2m-0.4m in voltage method 1.7m-2m in current method
Detectors	Peak	Quasi Peak and Average	Quasi Peak and Average
Resolution bandwidth	10kHz-150kHz: 1kHz 150kHz-10 MHz: 10 kHz	150kHz-30 MHz: 9 kHz	150kHz-30 MHz: 9 kHz 30 KHz-108 MHz: 120 kHz

1.5 Insertion Loss Evaluation

The test procedures to measure the IL of the PLF are defined by the EMC standards. The principal methodologies indicated by the standards are described hereafter:

- CISPR 17 [3] defines a method to measure the IL of a PLF in a 50 Ω or 75 Ω system. Two different methodologies can be used to evaluate the worst case.
  - Measure the IL in a system with line and load impedance of 0.1 Ω and 100 Ω and 100 Ω and 0.1 Ω, respectively.
  - Evaluating the minimum voltage attenuation obtained from the measurement of the Thevenin and transfer impedance of the filer.
- The ANSI C63.13 [4] considers the PLF as a four-port network and extends the measurement methods to obtain the DM by connecting the L and terminals of the PLF

with a 180°, while the CM is obtained by short circuiting the L and N terminals of the PLF.

- The IEEE standard 1560-2005 [8] provides a method to obtain the CM and DM IL considering line and load impedances equal to 50 Ω, three tests to evaluate the IL for impedances different from 50 Ω, and a method relying on S parameters measurements to evaluate the worst-case scenario.

In conclusion, there is not a general and unique solution for a correct PLF characterization, but merely a collection of different solutions which do not allow exactly estimate the IL introduced by the PLF.

Typically, S parameters are used to fully characterize the EUT, but due to several reasons such as lack of knowledge or correct instrumentation, the IL is not usually computed and usually the worst-case scenario is assumed. Hence, there is not a complete and clear methodology to follow to design an optimal PLF and this directly results in an oversized and not effective PLF design.

CHAPTER 2

2. EMC Receivers

Electromagnetic interference (EMI) instrumentation has significantly evolved over the last thirty years. In this chapter, the classical architecture of a conventional receiver is described and compared with the newest architecture of a Fast-Fourier-transform (FFT) based receiver. Additionally, different ways to measure the modal emissions, that is, the common and differential mode, with both types of receivers are described.

In a conventional receiver, CE modal emissions can be measured using an external modal separator. In a dual-port FFT-based receiver, this can be done in the digital domain. Both receivers have been used to measure a device under test emitting non-stationary interference.

2.1 Introduction

Present day regulations for electromagnetic interference (EMI) measurements have been in place for decades and were initially written to accommodate the needs of analog broadcast of voice and video according to the contemporary test technology. CISPR 16-1-1 [1], for instance, defines, in one of its annexes, the analog architecture of a conventional EMI receiver, which has proven to be a reliable instrument to measure stable and continuous interference emitted by electric and electronic devices. On the other hand, the scanning process is slow and short transients that do not frequently occur are hardly measured. Such interference, that may have negligible effect on a broadcast analog transmission, can cause the loss of data packets in current digital communications or jam an adjacent radar system [31-32].

Since test equipment has continuously evolved along all these years, regulations such as CISPR 16-1-1 [1] have included some amendments to consider the present state-of-art technology. Functions previously implemented with analog circuitry are currently done in the digital domain, and new functionalities can be developed by means of advanced signal-processing strategies. Fast Fourier transform (FFT) based EMI receivers, for instance, can instantly measure wide frequency spans continuously without loss of information, making them suitable for measuring even single transients. Besides, they offer additional features such as time-domain analysis, spectrogram, persistence spectrum, and-so-forth, all useful to better understand the interference properties and find a solution for its mitigation [31-35].

In the specific case of single-phase conducted-emission measurements, the most interesting property is the modal nature of the interference, since this is essential to design a suitable PLF.

Common and differential modes can be obtained from circuit modules external to the EMI receiver, usually called modal separators, or computed if line and neutral terminals are measured simultaneously. This calculation can be done if the front end of an FFT-based EMI receiver is replicated, extending its capabilities and making this kind of receivers ideal to solve EMI problems in an optimal way and in the shortest possible time and cost expenditure.

The complete architectures of both conventional and FFT-based EMI receivers are reviewed, emphasizing all technical details that are needed to meet the EMI regulations. In the FFT-based EMI receiver case, for instance, significant efforts are put into its digital part to faithfully emulate the behavior of analog detectors and damped meters in order to present equivalent measurement results as those of a conventional EMI receiver. However, despite the evident evolution in such modern's receiver implementation, each technology has its pros and cons, and a good knowledge of them is needed to get the most out of each case when used in actual measurements.

Then, the two methodologies to obtain the modal emissions are outlined. A concrete example of a modal separator circuit is analyzed. Furthermore, the standard and modal conducted emissions of an equipment under test (EUT) are measured using different types of EMI receivers and measurement methods.

2.2 Conventional EMI Receiver

2.2.1 Architecture of a Conventional EMI Receiver

The block diagram of a conventional EMI receiver, as described in [31-35], is shown in Figure 2.1. As a descended from radio receivers, it is implemented as a superheterodyne receiver.

The first component of the block diagram is a broadband radio frequency (RF) stepped attenuator, that usually integrates an RF amplifier to maximize the input power range.

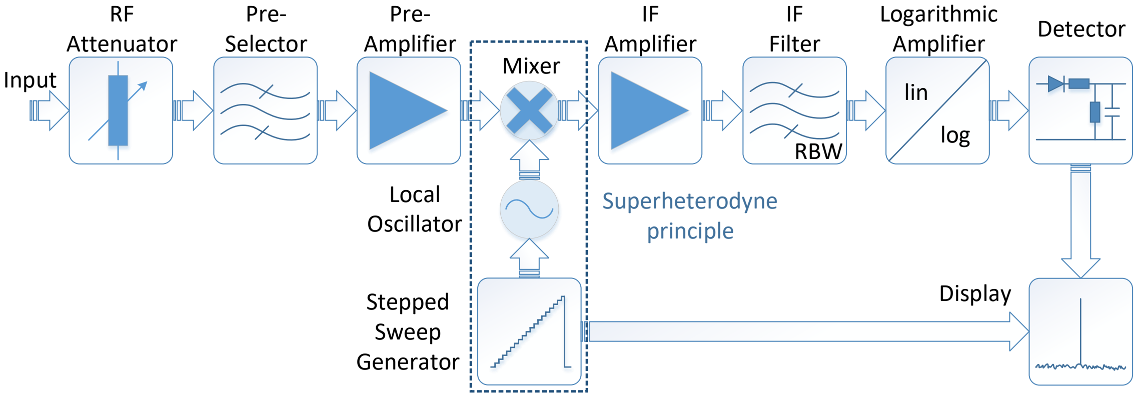


Figure 2.1: Block diagram of a conventional EMI receiver.

After the input attenuator there is a low-pass filter or a preselector (bank of filters) to mitigate the possibility of overloading the analog front-end due to broad-band and/or out-of-band high-amplitude signals and to prevent from spurious mixing products or intermodulation distortion products.

After the pre-amplifier, the input signal is mixed with a sine wave from a variable frequency oscillator known as local oscillator whose frequency is controlled by a stepped sweep generator. By sweeping the frequency of the local oscillator, the input frequency range is down converted to a fixed intermediate frequency (IF). Two important factors must be considered here:

1) First, the frequency steps of the local oscillator must be chosen small enough to avoid missing signals that are present between the receiver tuning frequencies. CISPR 16-1-1 states that the voltage accuracy shall be better than ±2 dB (±2,5 dB above 1 GHz) when the instrument measures a sine-wave signal using a 50 Ω resistive source impedance (Fig. 2.2). Therefore, the step size is determined by the IF-filter shape.
2) Second, the coherent time for a measurement result at each single frequency (also called dwell time), must be selected to be long enough to obtain a stable measurement result in the EMI receiver (which depends on the detector used and the type of interference).

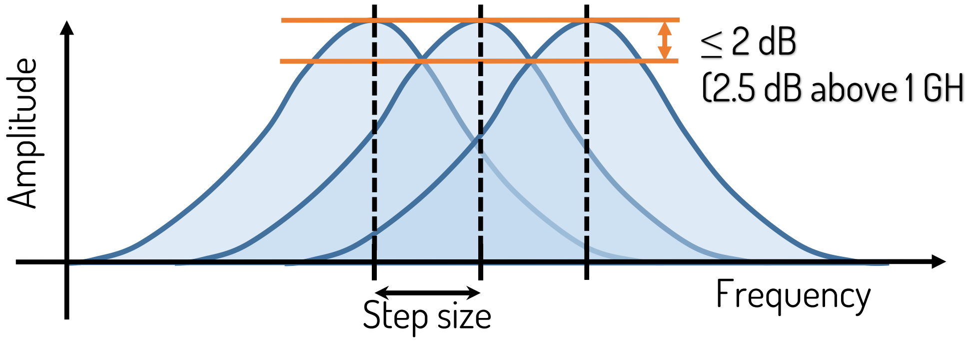


Figure 2.2: Maximum tolerance of a sine-wave voltage measurement according to CISPR 16-1-1.

Table 2.1

Frequency Range and RBW for each band

Band	Frequency Range	RBW
A	9 kHz to 150 kHz	0.2 kHz
B	150 kHz to 30 MHz	9 kHz
C	30 MHz to 300 MHz	120 kHz
D	300 MHz to 1 GHz	120 kHz
E	1 GHz to 18 GHz	1 MHz

Next block is where the IF filter, also known as resolution bandwidth filter (RBW), is applied.

CISPR 16-1-1 provides the critical masks for all selectable IF filters (see Fig. 2.3 as an example). Table I shows the 6-dB roll-off for bands A to E.

Since the representation of the signal in the screen of the EMI receiver is usually done in dBµV, the logarithmic amplifier gives an output voltage which is proportional to the logarithm of the input voltage.

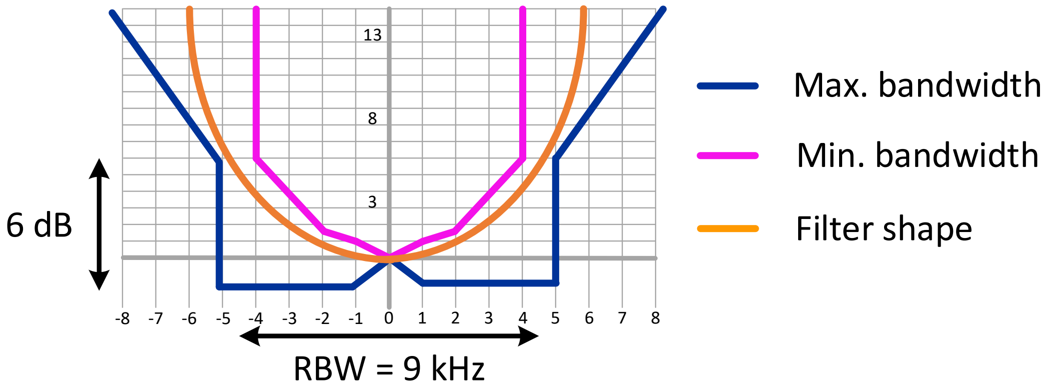


Figure 2.3: Critical mask for the IF filter of Band B (9 kHz).

Finally, a detector rectifies the signal and produces a DC voltage that drives the vertical portion of the display. CISPR 16-1-1 specifies the characteristics of peak, quasi-peak, CISPR-average (or average), and RMS average detectors, in areas such as input impedance, bandwidth, overload factors, sine-wave voltage accuracy, responses to pulses, sensitivity, limitations of intermodulation effects, limitations of receiver noise, and internally generated spurious signals [1, 31-35].

In a peak detector circuit (Fig. 2.4(a)), the IF signal is rectified by the diode and charges the capacitor to the maximum amplitude value of the input signal (the charging time constant is extremely short). This voltage is then processed and displayed.

EMI regulations introduced the quasi-peak detector (Fig. 2.4(b)) to weight the repetition rate of the interference, since it was determined that infrequent spikes and other short-duration noise events did not substantially prevent the reception of desired information in analog communications. In this case, the charge rates of the capacitor are defined as 1 ms for Bands B/C/D and 45 ms for Band A, and the discharge rate are 500 ms for Band A, 160 ms for Band B and 550 ms for Band C/D. Therefore, the output voltage is weighted based on the repetition rate of the input signal. The lower the repetition frequency, the lower the quasi-peak level, and vice versa.

The average detector (Fig. 2.4(c)) contains an output filter, narrower than the RBW, that averages the signal.

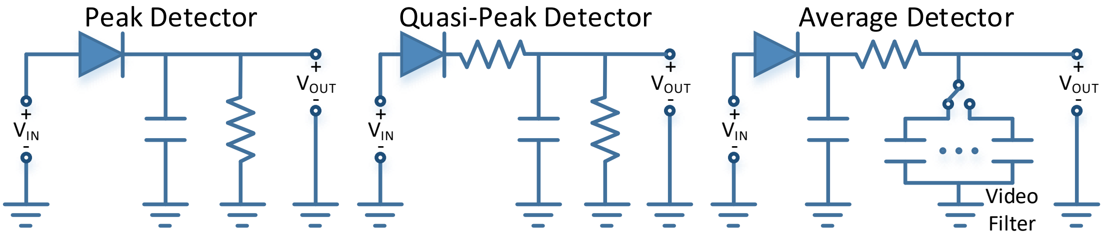


Figure 2.4: (a) Peak detector circuit; (b) Quasi-peak detector circuit; (c) Average detector circuit.

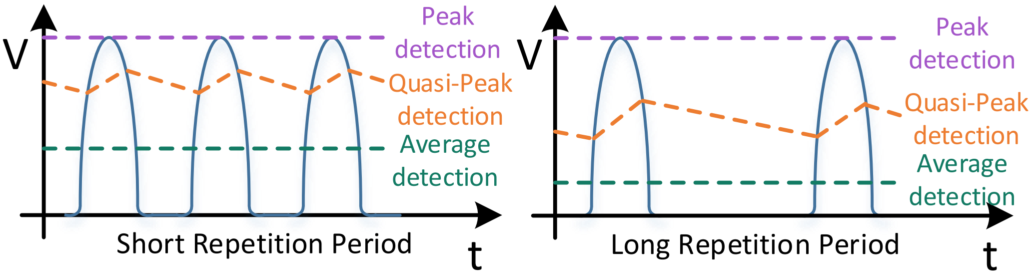


Figure 2.5: Measurement examples of signals with different repetition rates using the three detectors.

Fig. 3.5 shows a measurement example of two signals with different repetition rates obtained with the three detectors described above.

Finally, the RMS-average detector is a weighting detector described in [1] that combines an RMS detector for pulse repetition frequencies above a corner frequency with an average detector for pulse repetition frequencies below it.

2.2.2 Benefits and drawbacks of the Conventional EMI Receiver

As it may have been deduced from the previous subsection, this kind of receiver has some benefits, but also several drawbacks. The pros are:

- EMI regulations are tailor-made for conventional EMI receivers, and vice versa [1].
- Thanks to the architecture of the conventional EMI receivers, they present an extreme dynamic range, being able to simultaneously handle very high and very low amplitude signals over a wide frequency range and without performance degradation [31-34].

On the other hand, they present four main limitations:

- Measurements for the whole frequency band are slow. This is applicable to all detectors, but especially to the quasi-peak detector due to the charging and discharging time constants. For band B, for instance, the minimum dwell time is 1 second ($\tau_c + 3\tau_d + 3\tau_m =$ 1 ms+3·160 ms +3·160 ms = 961 ms), and for Band A, 2 seconds ($\tau_c + 3\tau_d + 3\tau_m =$ 45 ms+3·500 ms +3·160ms = 1995 ms).

  Considering an appropriate shape of the RBW filter, the minimum number of points (N) needed for a correct measurement is obtained as:

  $$N = \frac{SPAN}{{}^{1}\!/_{2}\, RBW}, \tag{2.1}$$

  Hence, the measurement time goes up to 106 minutes for band B and 47 minutes for band A using the quasi-peak detector.

  Therefore, measurements are usually done using the PK detector, and the QPK detector is only applied at those frequencies close or above the limit. Anyway, it is still a low and tedious process.
- A conventional EMI receiver cannot measure correctly transient events. This kind of events usually present a broadband spectrum, but due to the sweeping process, the receiver can only see a small portion of the frequency span at any moment, remaining blind to the rest of the transient spectra.
- The local oscillator of the conventional EMI receiver can suffer from sideband noise (phase noise), which can corrupt the incoming signals.
- The conventional EMI receiver is a scalar instrument that can measure the amplitude of signals but is unable to measure their phase.

2.3 FFT-Based EMI Receiver

FFT-Based EMI receivers can also be called Real-Time EMI receivers when all input signals samples are processed continuously and are gap-free.

2.3.1. Analog Architecture of the FFT-Based EMI Receiver

In an FFT-Based EMI receiver there is a high-speed analog-to-digital converter (ADC) that digitizes the input signal at some point of the block chain, reducing then the hardware complexity. This ADC is usually placed just after the mixer, as seen in Fig. 2.6(a), but it can also be moved before it in those applications where the sampling frequency of the ADC is high enough to capture the whole bandwidth of the input signal, as seen in Fig. 2.6(b) (for instance, to perform measurements in the frequency range between 9 kHz and 30 MHz, a minimum sampling rate of 100 MS/s, far above the Nyquist criteria, is recommended, and this is perfectly attainable for today's high-speed ADCs) [34-40].

One important difference between the mixer of the block diagram of Fig. 2.6(a) (belonging to an FFT-based EMI receiver) with the one of Fig. 2.1 (belonging to a conventional EMI receiver) is that it operates in a fixed-tuned mode instead of in a swept-tuned mode, which allows having a much lower phase noise. Further down-conversion, along with additional signal-processing strategies needed to obtain the same result as in a conventional EMI receiver, are done in the digital domain.

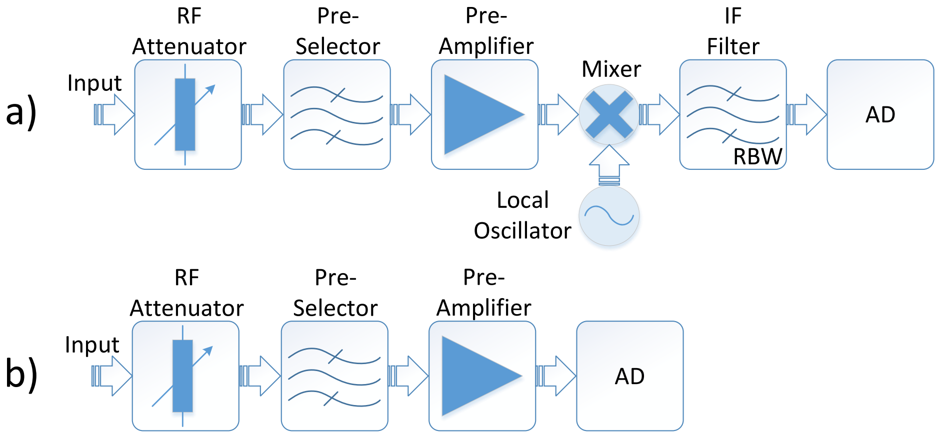


Figure 2.6: Block diagrams of an FFT-based EMI receiver.

2.3.2. Digital Architecture of an FFT-Based EMI Receiver

An overview of the digital signal processing blocks is presented in Fig. 2.7 [31].

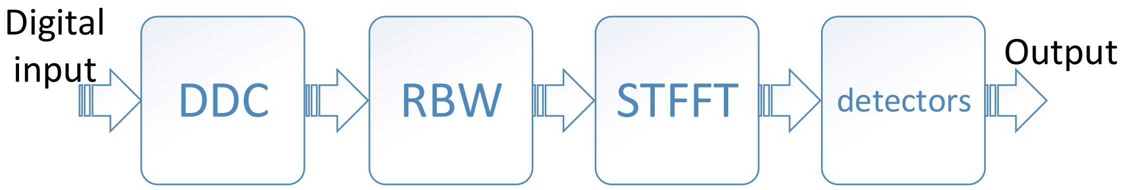


Figure 2.7: Block diagram of the digital signal processing.

The first block of Fig. 2.7 is a down-converter (DDC), that moves the input signal to a lower frequency, reduces its bandwidth and relaxes the sampling rate, which lessens the subsequent logic resources such as FFT points, data memory, clock frequency, and so on. It can be implemented by means of a quadrature receiver, as seen in Fig. 2.8 [31-34].

The second block is where the RBW is applied. The DFT assumes that the finite data set of the signal is one period of a periodic signal. If the data does not contain an integer number of periods, the transition between two consecutive periods is discontinuous. This fact causes a leakage of the DFT coefficients, known as spectral leakage. To reduce this effect, a weighting function is needed, and this is used to window the signal using a filter whose spectral shape meets CISPR 16-1-1 (as the RBW in the conventional EMI receiver). Consequently, the input complex signal is multiplied by the time-domain coefficients of this RBW. A multiplication in the time domain equals a convolution in the frequency domain, which is an equivalent process as that done by the conventional EMI receiver when sweeping the frequency of the local oscillator to multiply the whole spectra by the RBW.

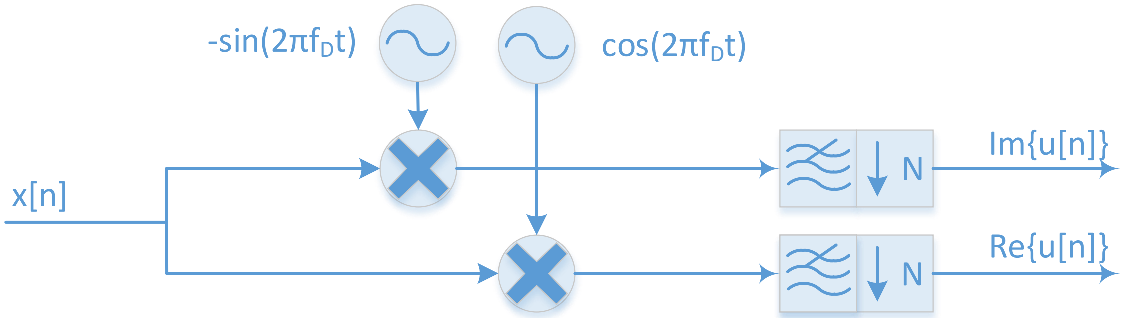


Figure 2.8: Digital down-converter

Different choices of window functions present different compromises between leakage suppression and spectral resolution. For instance, many spectrum analyzers from Tektronix use the Kaiser window by default [32-34].

This kind of window maximizes the dynamic range, although other window shapes can be used to obtain a different performance (Hanning, Hamming, Blackman-Harris, etc.). Flat-Top windows can be a good choice if their leakage is optimized as described in [36]. Fig. 2.9 supplies two examples of a 9-kHz (a) and 200-Hz RBW filters (b).

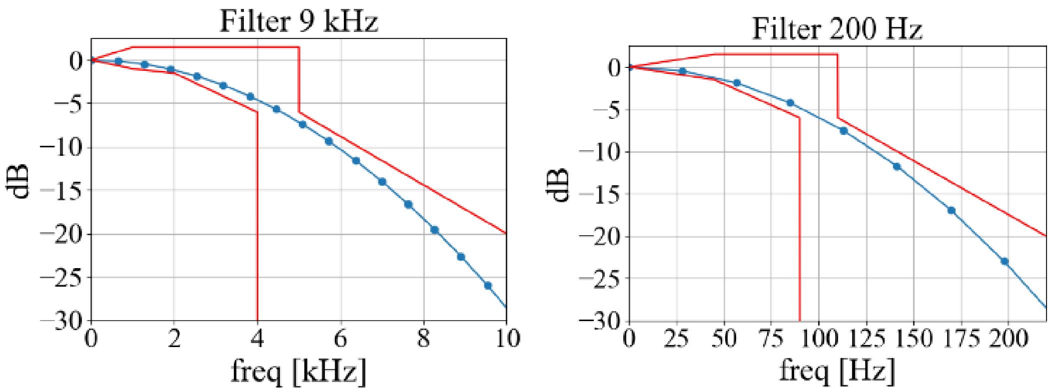


Figure 2.9: Examples of window functions that meet CISPR 16-1-1 for the 9 kHz and 200 Hz RBWs.

The third block is where the spectrum of the signal is computed by means of the short-time fast-Fourier transform (STFFT). There are two basic criteria to correctly implement this block:

- Due to the windowing, the time-domain signal arriving to the STFFT block presents a mitigation in its ends. Therefore, if there is a pulse signal at the edge of this gaussian shape, the computed spectra amplitude will be lower than the actual signal's amplitude (Fig. 2.10). To avoid that, signal overlapping is needed (the overlapping factor depends on the window used; as an example, a minimum overlapping factor of 75% is needed in [1,31-34] to achieve a sufficiently dense discretization using a Gaussian window).
- A second design criterion is the selection of the number of FFT points. CISPR 16-1-1 states that the measurement accuracy of sine-wave voltages shall be better than ±2 dB when the instrument measures a sine wave signal with 50 Ω resistive source impedance. Therefore, the amplitude of a signal placed between two consecutive bins shall not be mitigated by the RBW beyond this threshold (Fig. 2.2).

  If this is not the case, either the number of points should be increased (either using data samples or applying zero-padding), or the filter shape needs to be modified (always respecting the critical mask).

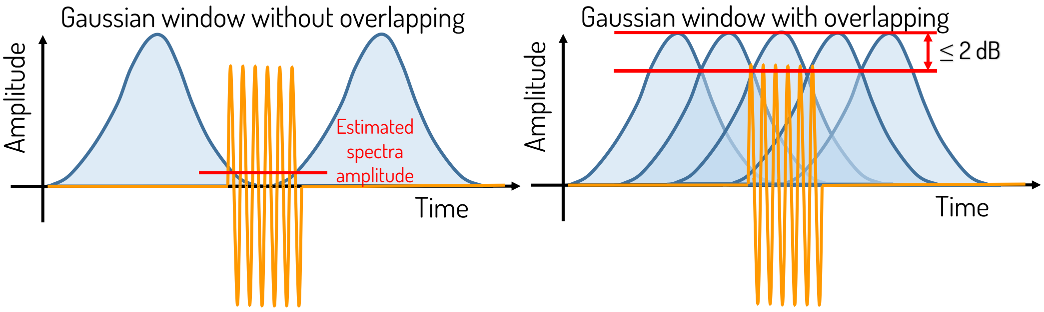


Figure 2.10: Non-overlapped and overlapped Gaussian Window.

The last block of Fig. 2.7 is the detector block, which must emulate the analog detectors defined in [1] (peak, quasi-peak, RMS-average and RMS). It should be noted that, unlike in the analog case (where there is a sweeping process), the STFFT block provides the whole spectrum of the analyzed frequency span, and therefore, detectors are applied to all frequencies simultaneously.

A peak detector is easily emulated storing the maximum value at each frequency bin during the configured dwell time [31].

The charging and discharging process of the analog quasi-peak detector, along with the critically damped meter response, can be digitally implemented using, for instance and among other possibilities, one- and two-order infinite impulse response (IIR) filters [31-36].

Again, there are different methods to implement the average detector. It is established in [1] that the measurement result is equivalent to the peak reading of a meter with a time constant of 160 ms for Bands A and B and of 100 ms for Bands C, D and E. As in the quasi-peak case, this can be accomplished, for instance, using IIR filters.

2.3.3. Benefits and drawbacks of the FFT-Based EMI Receiver

Different technology implies different pros and cons. The benefits obtained from a reduced hardware complexity and the signal processing done in the digital domain are:

- Measurements are impressively fast. It is possible to perform real-time measurements with any of the detectors (even with the quasi-peak detector).
- Since the whole bandwidth is analyzed simultaneously, transient events can be easily measured.
- The RF part of the hardware may be simpler than in the conventional instrument, and the setup and operation are less elaborated. This additionally implies a reduced need for calibration and repair.

  If two or more receivers are needed (for instance, for simultaneous measurements of line and neutral which allows the extraction of the modal modes), the replication of the hardware does not substantially increase the cost of the instrument.
- Advanced signal processing strategies allow the addition of new features, such as time-domain analysis, spectrogram, and persistence spectrum even in real time. A better analysis of the interference phenomena allows a better understanding and therefore, entails an important reduction of the electromagnetic compatibility design of the EUT.

On the other hand, the drawbacks to be considered are:

- It is difficult that an FFT-based EMI receiver achieves the same dynamic range than a conventional one with a single ADC (optimization of the dynamic range can be obtained combining the performance of several ADCs). CISPR 16-1-1 implicitly states the dynamic range in the specifications of the detectors. For instance, for the quasi-peak detector, a standard pulse and a flat spectrum up to the maximum frequency of the band must be correctly measured. At a repetition frequency of 1 Hz, the dynamic range needed to meet the standard, considering enough margin to meet the ±2 dB of accuracy, is approximately 111 dB for band A, 116 dB for band B and 125 dB for band C. Such dynamic range can be achieved by means of a suitable configuration of the oversampling gain (process of sampling a signal above twice its bandwidth), the FFT gain (an FFT is equivalent to sweep a narrowband filter with a bandwidth of F_S/M, being M the number of the FFT points, over the spectrum, filtering the noise distributed along the whole bandwidth) and the window specific processing gain (depending on the window's type applied, the amount of noise that is accumulated in one frequency bin varies, based on its characteristic equivalent noise bandwidth (ENBW)).

- Another major drawback is the overload. In the FFT-based EMI receiver, block diagram shown in Fig. 2.6, the ADC absorb a wideband signal (usually tens of MHz). Impulsive noise can easily drive the ADC into saturation, leading to the appearance of artifacts in the spectrum that do not correspond to the original signal (preselector filters in the conventional EMI receiver can be narrower, limiting the saturation of the mixer). To overcome this problem, the input attenuation must be increased, but this involves a loss of the dynamic range equivalent to the added attenuation.

2.4 Modal Emissions Measurement

Standard measurements provide information about the emission levels of a EUT [2-3], but do not help in solving the problem in case of non-compliance. Since the components of a power-line filter mainly mitigate one of the two modes, that is, the CM or the DM, modal-emission measurements become fundamental to identify the dominant mode and to implement the suitable power-line filter (PLF) accordingly, using fewer components and getting a more cost-effective design.

Modal signals are obtained from the following equations:

$$V_{CM} = \frac{V_L + V_N}{2},\ i_{CM} = i_L + i_N, \tag{2.2}$$

$$V_{DM} = V_L - V_N,\ i_{DM} = \frac{i_L - i_N}{2}. \tag{2.3}$$

The device that implements these equations in the analog domain is called modal separator. On the other hand, to implement them in the digital domain, both line and neutral conducted emissions must be measured simultaneously.

2.4.1 Analog modal separator

Manufacturers such as Analog, Schwarzbeck or Tekbox provide modal separators based on different technologies.

To illustrate how the modal components can be separated using analog circuits, Fig. 2.11 shows an example based on an RF transformer. In this circuit, the CM voltage (V_{CM}) is obtained from the primary winding (CM cannot overpass the transformer), and the DM voltage (V_{DM}) from the secondary winding (the DM is null in the middle of the primary winding).

Fig. 2.12(a) shows its modal S-parameter simulation considering port 1 is Line and Neutral when injecting a CM signal, port 2 is the CM port, and port 3 is the DM port.

Fig. 2.12(b) shows its S-parameter simulation considering port 1 is Line and Neutral when injecting a DM signal. As expected, the CM and DM ports output the desired mode and rejects the contrary mode.

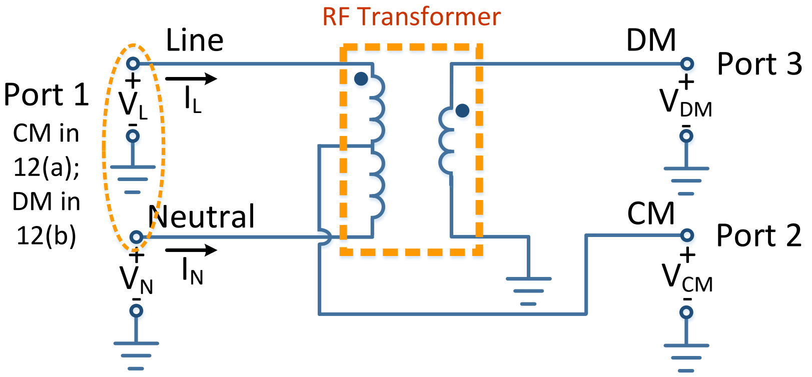
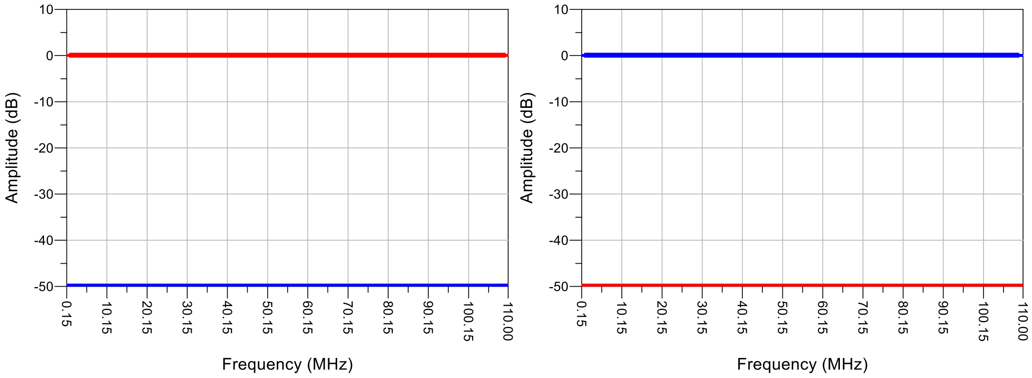


Figure 2.11: Analog modal separator using a transformer.



(a) (b)

Figure 2.12: Simulated S parameters. (a) S(2,1) red and S(3,1) blue ; (b) S(2,1) red and S(3,1) blue

The main benefit of using an external modal separator is that the conventional measurement setup does not need to be renewed. On the other hand, there are a few drawbacks to be considered when using an external separator:

- Extra equipment must be bought or developed.
- A transformer can behave as an antenna and couple undesired signals in the measurements.
- CM and DM cannot be measured simultaneously if there is only a single receiver. This makes the identification of the predominant mode difficult, especially when measuring a pulsed interference (as in the example below).
- Modal coupling (CM coupled to DM port and vice versa) depends on the technology, may vary with the frequency and it is usually higher than in the digital case.
- Special care must be taken to avoid impedance mismatches (reflections due to impedance mismatches can amplify the modal conversion).

2.4.2. Digital modal separator: Two-port receiver

In an FFT-based EMI receiver, modal emissions can be obtained replicating the block diagram of Fig. 2.6(a) or Fig. 2.6(b) in the same instrument to capture the conducted emissions of line and neutral simultaneously and apply Eq (2.2) and Eq (2.3) in the digital domain.

The benefits are:

- There is no need to acquire extra hardware.
- There is no possibility of impedance mismatch.
- Better modal extraction.

2.5. Measurement Results

The standard and modal conducted emissions of a microwave oven was measured using a conventional and an FFT-based EMI receiver. The measurement setup is shown in Fig. 2.13 (a) and (b).

Figure 2.13: Schematic of the measurement setup (a); Actual implementation (b)

This EUT was selected because its conducted emissions strongly depend on the magnetron. This component generates the microwave radiation used to heat the food, and it is the main conducted-emission generator. Since it is continuously turned on and off (to graduate the heating intensity), the conducted emissions of the microwave oven vary in consequence.

This behavior is better understood in the spectrogram (time vs frequency diagram) of Fig. 2.14, obtained using the QPK detector on the line terminal, a dwell time of one second and a total frame time of 200 seconds. The amplitude of the spectrum of each time slice is plotted as a colored horizontal line, and each color provides the amplitude magnitude. The time slices colored with yellow and light blue tones at low frequencies, which correspond to the higher emission levels, represent the conducted emissions when the magnetron of the microwave oven is turned on.

The dark blue ones, which correspond to lower emission levels, represent the conducted emissions when the magnetron is turned off. Transient signals can be observed when the magnetron changes its state.

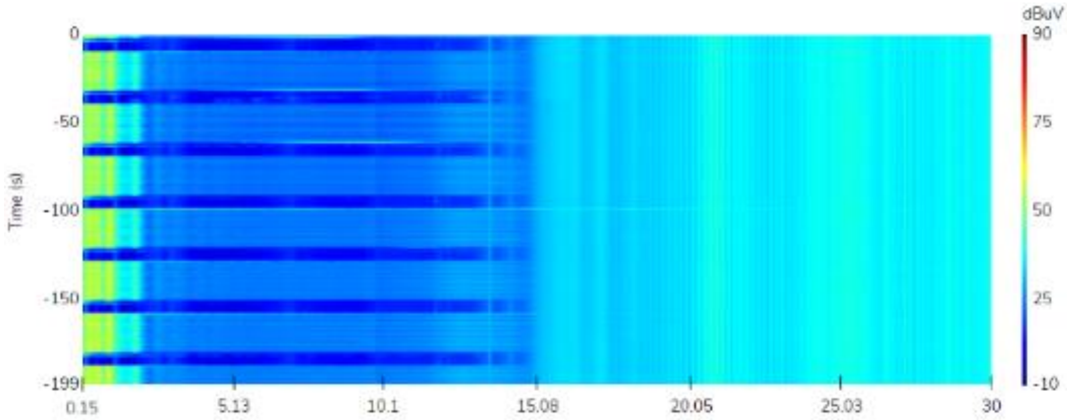


Figure 2.14: Spectrogram. Line emissions. Quasi-peak detector.

2.5.1 Standard and modal measurements using a conventional EMI receiver.

As explained before, due to the long measurement time, the final QPK measurements are usually done only in a few frequencies near or above the limit.

Due to the slow measurement sweep of the instrument (more than ten minutes to complete a single scan), the magnetron is switched on and off several times within the scan, obtaining a spectrum which does not correspond to the actual emissions of any of the states of the EUT, but a mix of them. Transient peaks are also observed when the magnetron is switched on and off. Neutral emissions, not shown here, present similar results.

Figure 2.15 shows the conducted emissions obtained using the peak and average detectors of a conventional EMI receiver (an ESPC from Rohde & Schwarz).

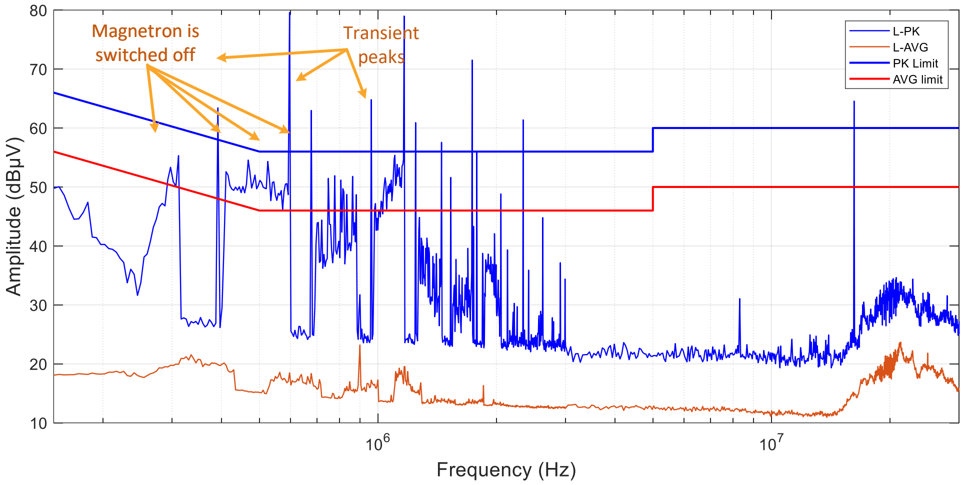


Figure 2.15: Standard measurement done with the ESPC. Peak and average scans were obtained with a dwell time of 10 ms.

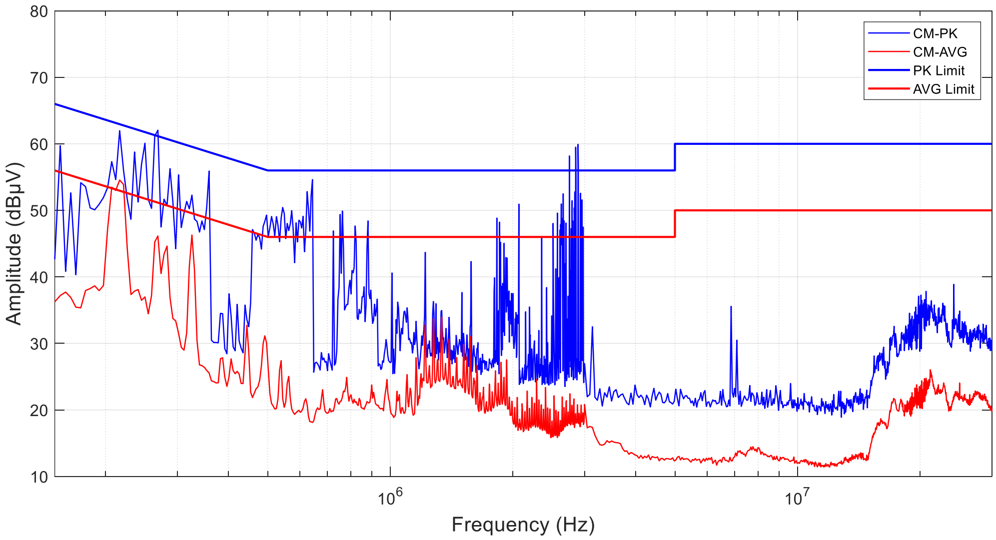


Figure. 2.16: CM emissions measured with the ESPC and a modal separator. Peak and average scans were obtained with a dwell time of 10 ms.

Figures 2.16 and Fig. 2.17 show the modal emissions obtained using the peak and average detectors of the ESPC and an external commercial modal separator (manufacturer by Tekbox). The same problems described above can be observed. It is really difficult to identify the which is the dominant mode in each frequency, since it is not possible to be sure if low emissions are due to be measuring while the magnetron was switched off, or if the magnetron does not actually emit at those frequencies.

Building a PLF relying on this information can lead to a completely wrong and inaccurate design.

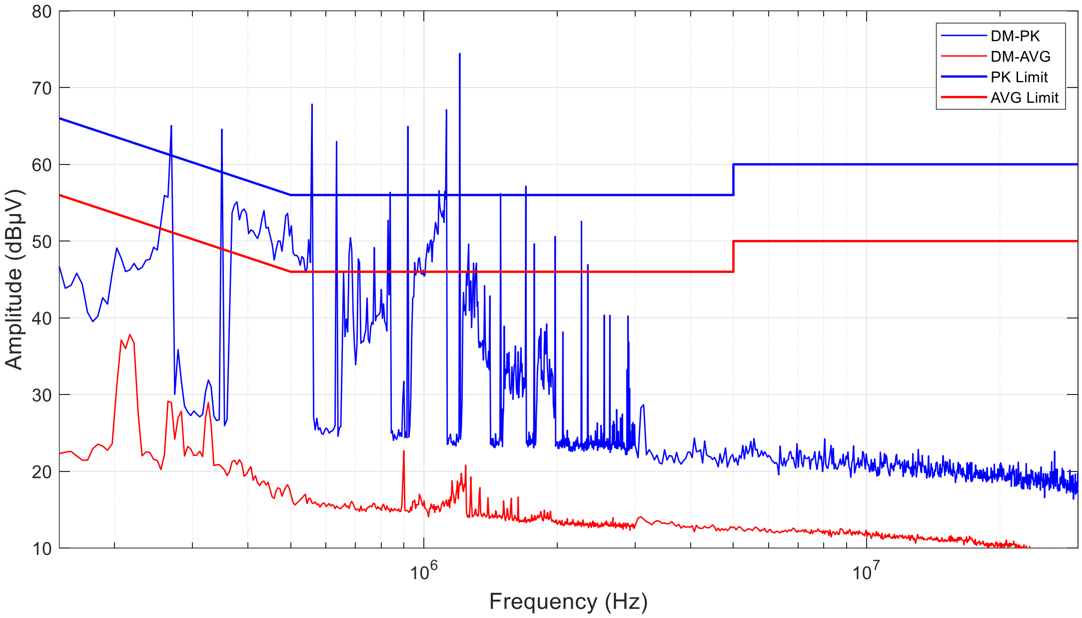


Figure 2.17: DM emissions measured with the ESPC and a modal separator. Peak and average scans were obtained with a dwell time of 10 ms.

2.5.2 CE and modal measurements using a dual-port FFT- based EMI receiver

The same measurements have been carried on using a dual-port FFT-based EMI receiver.

In this case, the same instrument is able to perform the whole measurement of line and neutral and quasi-peak and average in a single dwell time (1 second), obtaining the full spectrum while the magnetron is switched on, and therefore avoiding the transitions between on and off (which, according to CISPR 16, do not need to be considered to label the EUT as compliant or non-compliant; if needed, such transients could also be measured with an FFT-Based EMI receiver).

Line and neutral emissions are similar for both detectors, except in the frequency range between 150 kHz and 300 kHz.

Figure 2.18 shows the standard conducted-emission measurements.

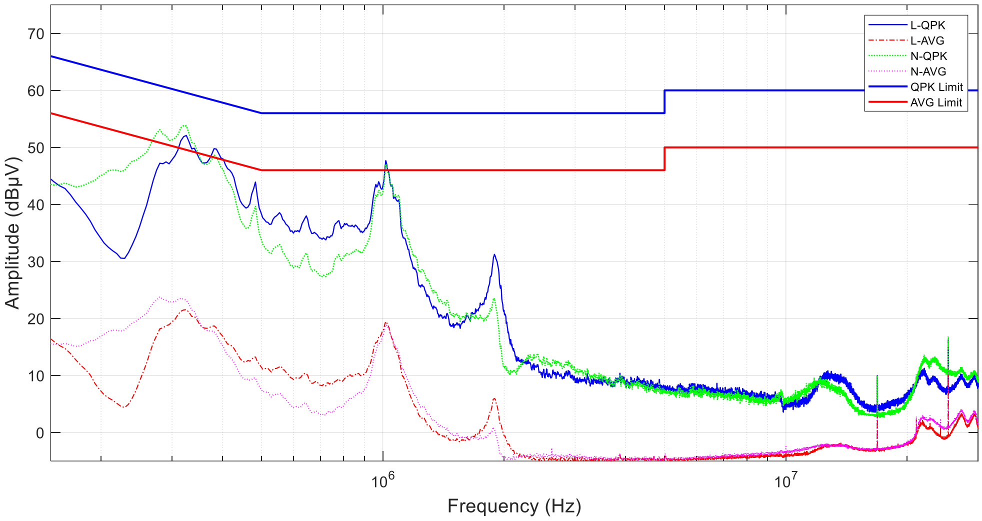


Figure 2.18: Standard measurement performed with the EMSCOPE. QPK and AVG scans obtained with a dwell time of 1 s.

As it can be seen, the highest emissions are all found below 2 MHz.

Fig. 2.19 shows the modal emissions obtained with the same receiver. The great advantage here is that it is possible to measure adequately each of the modes, facilitating the design of the suitable PLF. The differential-mode emissions are higher in most part of the spectra for both detectors.

In case of necessity, the identification of the dominant mode could be used to select the suitable PLF component (in this case, although not necessary because the EUT is already compliant, an X-type capacitor could be used to mitigate the DM).

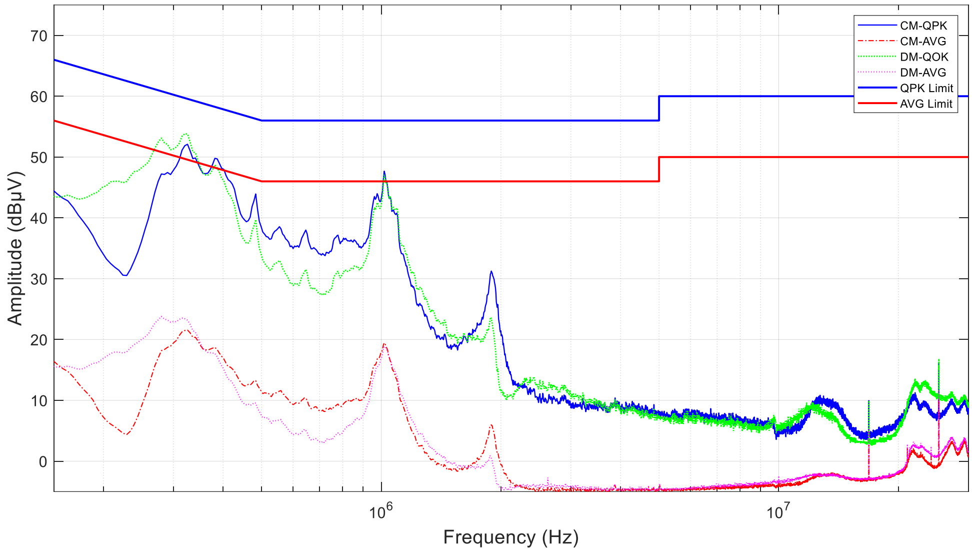


Figure 2.19: Modal measurement performed with EMSCOPE. QPK and AVG scans were obtained with a dwell time of 1 s.

2.5.3 Comparison of modal measurements obtained using an analog vs digital modal separator.

In order to understand the influence that an external separator may introduce while evaluating modal noises and its impact on the PLF design, the same modal CE have been measured using two different set ups while using the same measurement instrumentation. The first set up is shown in Figure 2.20. As it can be seen, it is composed by an external separator interposed between the LISN output and the receiver input.

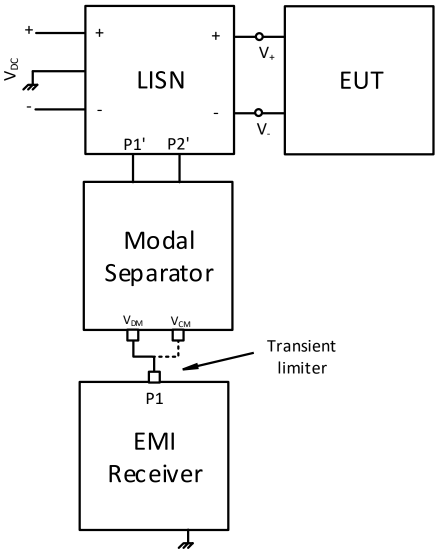


Figure 2.20: Schematic of the first measurement set up

The second measurement set up is shown in Fig. 2.21. It relies on a double channel EMI receiver to evaluate the modal noises by measuring both RF voltages simultaneously and performing the mathematical evaluation in the digital domain.

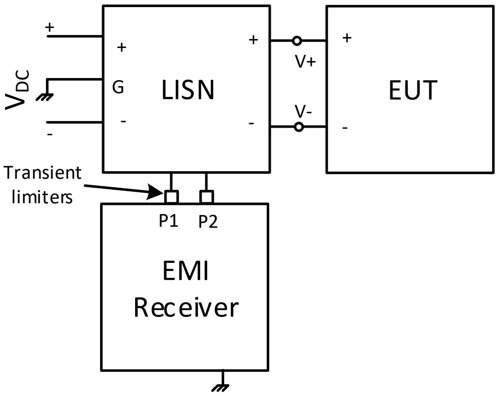


Figure 2.21: Schematic of the measurement set up

The comparison of results obtained with the two set ups are shown in Figure 2.22 (only QPK measurements) and 2.23 (only AVG measurements).

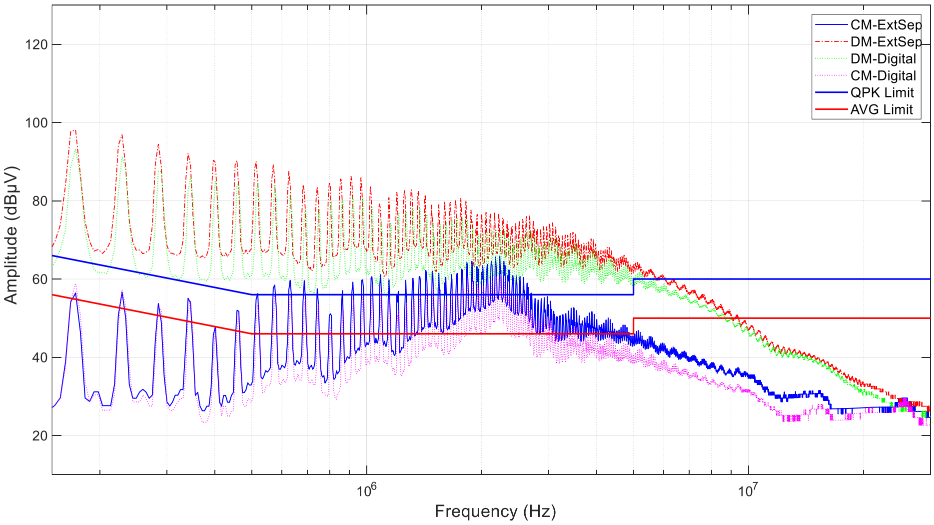


Figure 2.22: Comparison of CM and DM noises (QPK detector) recorded by using an external separator vs calculation in digital domain.

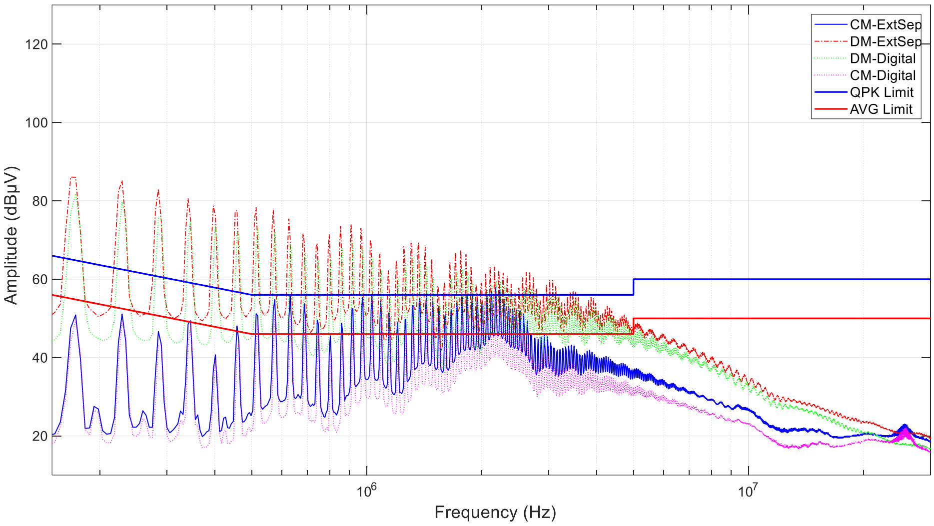


Figure 2.23: Comparison of CM and DM noises (AVG detector) recorded by using an external separator vs calculation in digital domain.

As it can be seen in Fig. 2.21, modal noises evaluated by means of an external separator or by computing them in digital domain show little difference in the lower frequency band. For instance, for frequency lower than 1 MHz, the measurements show a good agreement.

The same can't be stated for the higher frequency range. For instance, between 1.5-2.5 MHz the measurements recorded with the external separator are above the limit allowed by the standard, while the measurements recorded by computing the modal noise in digital domain are below the allowed limitations. It is possible to appreciate a difference of some dBμV in good part of the frequency range. Hence it is clear that adding external devices, as well as extra cables, may have huge influence in the results, especially because their impedance varies versus frequency is difficult to be characterized and compensated.

These results proof that when external separators are used, extreme care must be taken in order to avoid useless work to solve fake non-compliance problems. Same considerations can be applied for CE measurements obtained with AVG detector as shown in Fig 2.23.

2.6. Conclusions

The architectures of a conventional and an FFT-based EMI receiver have been described and compared. Although the conventional instruments have been in use for decades, current state of technology allows the development of instruments that offer much more possibilities and information to EMC engineers.

As an example, when EUTs do not emit stationary and continuous interference, as it is the case of a microwave oven, conventional instruments present several difficulties to obtain a suitable measurement, mainly due to the long time needed for a single capture (especially if the quasi-peak detector has to be used).

On the other hand, FFT-based instruments are fast enough to capture the desired emissions using any detector (or all simultaneously), since measurements are obtained in a single dwell time. One important feature of modern instruments is that they are even able to provide the modal emissions, which is an essential information to identify the problem’s source of a non-compliant EUT and implement the suitable power-line filter accordingly. Although conventional instruments can also measure these emissions by means of an external modal separator, the same limitations found in standard measurements are also applied.

CHAPTER 3

3. Uncertainty Budget Evaluation of a Measurement Instrument

In this chapter the role of metrology and the impact of uncertainty on the measurements is analyzed and discussed. The content of this chapter highlights fundamental concepts and explanations that are pertinent to general scientific measurements as a whole, along with a summary of fundamental principles to evaluate the measurement uncertainty of any measurand. The methodology and findings of this chapter are then tested to evaluate the measurement uncertainty of the input chain of a commercial instrument.

Basic Principles:

Metrology is defined as the “science of measurement and its application – it includes all theoretical and practical aspects of measurement, whatever the measurement uncertainty and field of application “. Hence, since measurements are the foundation of such practice, they are defined as “process of experimentally obtaining one or more values that can reasonably be attributed to a quantity" [41].

On a daily basis, all human beings (consciously or unconsciously) apply similar process to obtain data and information from the surrounding world. This can vary from simply measuring the length of an old fridge to substitute it with a brand new one using a cheap ruler worth few euros, or by sending reusable rockets to space using instrumentations worth billions of euros.

Each of this process concerns a property which is object of the measurement itself, the quantity. As per [41], it is defined as “property of a phenomenon, body, or substance, where the property has a magnitude that can be expressed by means of a number and a reference”.

Independently on which type of measurement is carried out, it is never possible to derive the exact value of a quantity, but only an estimation of it. The estimation indicates that the actual value of the measurand is not true, it is only possible to estimate it with an associated uncertainty. The definition of uncertainty is given by [41] as a “parameter, associated with the result of a measurement, that characterizes the dispersion of the values that could reasonably be attributed to the measurand.”

Basically, the uncertainty is an indicator of the “lack of knowledge” associated to the measurement [42].

The overall uncertainty of the measurand is composed by systematic and random effects. Systematic effects are persistent and challenging to be identified but can be easily rectified if found. Conversely, random effects are completely arbitrary and unpredictable occurrences that cannot be mitigated. However, their effect on the final measurement can be compensated by repeating the same type of measurement.

In this case, the statistical expectation of the random error on repeated measurements is zero. In conclusion, it is never possible to obtain the true value of the measurand. Furthermore, any measurement given without its associated uncertainty makes this value meaningless.

At present, the reference standard to evaluate and express the measurement uncertainty is the Guide to the Expression of Uncertainty in Measurement (GUM) [43,44]. In it, the measurand uncertainty is obtained evaluating the propagation of uncertainty from the input variables. However, this method has some limitations, since it is difficult to apply in complex systems, as those present in EMC testing devices, and requires several approximations that may result in inaccurate solutions [43-57]. To overcome these disadvantages, the last revision of GUM adopts the Bayesian Approach and adds the Monte Carlo Method (MCM) in the process [44-57].

3.1 The GUM

3.1.1 Overview of the GUM Methodology

The GUM defines the measurement uncertainty as a parameter, associated with the result of a measurement, that characterizes the dispersion of the values that could reasonably be attributed to the measurand.

As per [42-44], the measurand Y is determined from the different input quantities $X_1, \dots, X_n$ through a functional relationship f:

$$Y = f(X_1, \dots, X_n). \tag{3.1}$$

An estimate of the measurand Y is obtained from Eq. (3.1) using input estimates $x_1, \dots, x_n$ for the values of the n quantities $X_1, \dots, X_n$. Thus, the output estimate y is given by:

$$y = f(x_1, \dots, x_n). \tag{3.2}$$

And its associated standard uncertainty u defined as [43]:

$$u^2(y) = \sum_{i=1}^{n} \left(\frac{\delta y}{\delta x_i}\right)^2 u^2(x_i) + 2\sum_{i=1}^{n-1} \sum_{j=i+1}^{n} \frac{\delta y}{\delta x_i}\frac{\delta y}{\delta x_j} \; u(x_i, x_j), \tag{3.3}$$

being x_i and x_j the estimate of X_i and X_j.

At this point, the type A uncertainty, consisting of evaluating the uncertainty by the statistical analysis of series of observations and type B uncertainty, based on evaluating the uncertainty by means other than the statistical analysis of series of observations, can be presented.

Type A can be applied if n observations of a single quantity x_1 are available. Then, the expected value of x is estimated by the arithmetic mean.

$$\text{x}=\frac{1}{n}\sum_{i=1}^{n} x_i \tag{3.4}$$

Then, the dispersion from the mean is quantified by simply evaluating the variance of the mean itself:

$$s^2_{(\text{x})}=\frac{s^2_{\text{xi}}}{n}=\frac{\sum_{i=1}^{n}(x_i-x)^2}{n(n-1)} \tag{3.5}$$

For type B uncertainty, the variance $u^2_{(x_i)}$ of an input quantity x_i is obtained from several information on the quantity itself, such as datasheets, calibration certificates, old record of measurements and so on. The standard uncertainty can be obtained from these sources by expressing it as a multiple of the standard deviation, defining it as an interval with a specified level of confidence, or establishing limits for the aforementioned interval.

In summary, utilizing both techniques allow to determine the mean value of the measurand and the calculation of two distinct standard uncertainties that supply insight into various aspects of the measurement. Consequently, the ultimate stage entails merging the collected data to determine the combined standard uncertainty.

During the assessment, there are two possible scenarios: the input values x_i are independent, or multiple values are correlated between each other.

In case the input quantities are not correlated, the combined variance can be obtained by:

$$u^2(y)=\sum_{i=1}^{n}\left(\frac{\delta f}{\delta x_i}\right)^2 u^2(x_i) \tag{3.6}$$

Where $u^2(x_i)$ ca be evaluated by relying on type A or B method and f is defined in 3.1.

Conversely, if the input quantities are correlated, the combined variance can be evaluated by:

$$u^2(y)=\sum_{i=1}^{n}\sum_{j=1}^{n}\frac{\delta y}{\delta x_i}\frac{\delta y}{\delta x_j}\ u(x_i,x_j) \tag{3.7}$$

Where $u(x_i, x_j)$ is the estimated covariance associated with x_i and x_j.
Finally, the measurement result is expressed as:

$$Y = \mathrm{y} \pm k * u(\mathrm{y}) = \mathrm{y} \pm U \tag{3.8}$$

Where k is the coverage factor and U is the expended uncertainty.

3.1.2 The Central Limit Theorem

The central limit theorem (CLT) is fundamental when dealing with measurement and associated uncertainty. If the relationship between the output quantities x_i and the measurand Y can be expressed as follows:

$$Y = c_i * x_i + c_2 * x_i + \cdots c_n * x_n = \sum_{i=1}^{n} c_i * x_i \tag{3.9}$$

Where c_i are the input coefficients.

The CLT states that the final distribution of the measurand Y will be gaussian, independently of the distribution of the single input quantities.
Furthermore, if the x_i are independent and no one of the $c_i^2 * \sigma^2(x_i)$ prevails on the others, the CLT defines the expected value as:

$$\mathrm{E(Y)} = \sum_{i=1}^{n} c_i * E(x_i) \tag{3.10}$$

And the variance as:

$$\sigma^2(x_i) = \sum_{i=1}^{n} c_i * \sigma^2(x_i) \tag{3.11}$$

If the Type A method is used to evaluate the uncertainty, thanks to the CLT it is possible to define if h is a random variable which an unknown associated distribution with known mean μ_i and known standard deviation σ, then the PDF of the distribution obtained after k observation of h, tends to a normal distribution with mean value μ_k and standard deviation ${}^{\sigma}/_{\sqrt{k}}$.

Hence, as the number k observation increases, a consequence reduction of the standard uncertainty associated can be obtained.

3.1.3 The GUM Supplement 1 and MCM Method

The GUM Supplement 1 states that an appropriate method has to be chosen for the propagation stage [44]. In cases where it is difficult to assess whether the GUM framework is valid, for instance if system is not linear, Monte Carlo simulations provide a wide-accepted method to evaluate the uncertainty propagation [44-58].

The evaluation of the measurand uncertainty, following the GUM guidelines, is established by the law of the propagation of the error and the central limit theorem [43-47].

In general, the analysis can be generally carried out considering Eq. 3.1 and Eq. 3.3 where $x_i$and $u(x_i)$ represent the best estimate and standard uncertainty of the input quantity X_i, Y and $u(Y)$ are the best estimate and standard uncertainty of the output quantity Y (the measurand) [44-51].

The combined uncertainty of Y is defined by the Eq. 3.3 if the input quantities can be represented as independent random variables.

In practice, different PDFs can be assigned to the system's variables following different principles. The most general ones are briefly described here:

- **Rectangular PDF**: reflects the principle of the maximum entropy.

Usually, it is applied to parameters that present at least one of the following characteristics:

- There is no way to establish which value the parameter will assume within the proposed interval $[-a; +a]$.
- The probability to assume a value of the aforementioned interval is equal.
- The quantity can assume a finite value only in this finite interval, 0 elsewhere.

$$f(x) = \begin{cases} \frac{1}{b-a} & for\ a \leq x \leq b \\ 0 & for\ x < a\ or\ x < b \end{cases} \tag{3.12}$$

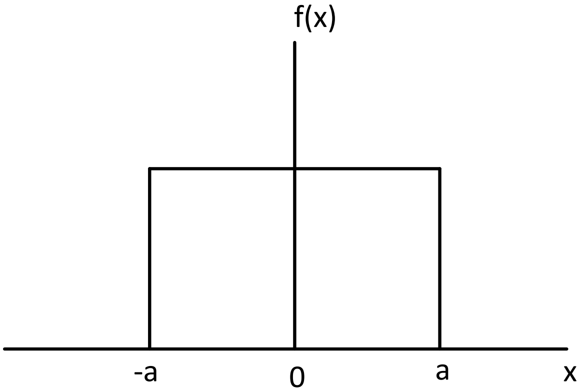


Figure 3.1: Probability density function of a rectangular distribution

Its mean value is defined as follows:

$$\mu = \int_b^a x\, f(x)\, dx \ = \frac{(b+a)}{2} \tag{3.13}$$

While its variance, defined as the square of the standard deviation is:

$$\sigma^2 = \int_b^a (x - \mu)\, f(x)\, dx \ = \frac{(a - b)^2}{12} \tag{3.14}$$

The standard deviation can be obtained evaluating the standard uncertainty associated with the estimation of $\frac{(b+a)}{2}$.

The PDF represented in Figure 3.1 is assigned to parameters or variables that are known to vary within a fixed interval, but no information on the probability that the parameter has to assume a determined value is known. For instance, this PDF is commonly used by components manufacturers to indicate the nominal value and uncertainty of their products. In such cases, only the nominal value of the parameter with its associated uncertainty interval is provided. No additional information on the probability that a specific value might assume is given.

- **Triangular PDF**

This PDF is usually assigned at parameters with the following's characteristics:

- They have a finite value different from 0 in a finite interval $[b, a]$.
- They have the highest probability to assume a value c, which is part of the interval $[b, a]$.
- The probability from b to c and c to a change linearly.

$f(x)$ assumes the followings values:

$$\begin{cases} 0 & for\ x < a\ and\ b < x \\ \frac{2\,(x-a)}{(b-a)(c-a)} & for\ a\ < 0\ and\ a \le\ x\ \le\ b \\ \frac{2\,(b-x)}{(b-a)(b-c)} & for\ c\ < x\ \le b \\ \frac{2}{b-a} & for\ c = x \end{cases} \tag{3.14}$$

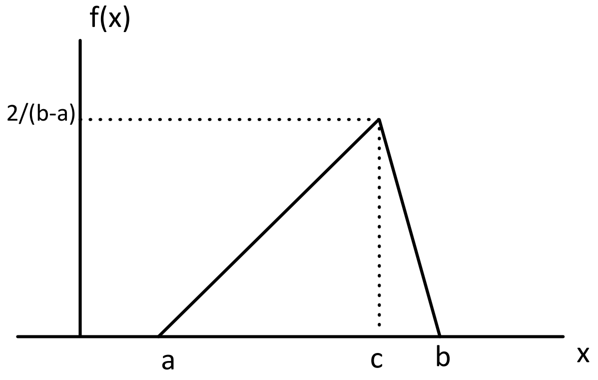


Figure 3.2: Probability density function of a triangular distribution

The mean value of $f(x)$ is

$$\mu = \int_b^a x\, f(x)\, dx \ = \frac{(a + b + c)}{3} \tag{3.15}$$

While its variance, defined as the square of the standard deviation is:

$$\sigma^2 = \int_b^a (x - \mu)\, f(x)\, dx \ = \frac{a^2 + b^2 + a^2 - b * a - b * c - a * c}{18} \tag{3.16}$$

This distribution shown in Fig.3.2, is based on a guess of the modal value of the parameter. Typically, it is used when data are limited and the relationship between different variables is known, but collecting more data would be too complicated. For this reason, it is also called “lack of knowledge “distribution.

- **Gaussian PDF**

This PDF applies to quantity X who is continuously fluctuating. This is the most used distribution to model statistic properties of physical quantities in EMC and its distribution is shown in Fig 3.3.

$$f(x) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{1}{2}(\frac{x-\mu}{\sigma})^2} \text{ for } -\infty < \text{x} < +\infty \tag{3.17}$$

$f(x)$ is unimodal, symmetric, and characterized by:

μ: mean value
σ: standard deviation

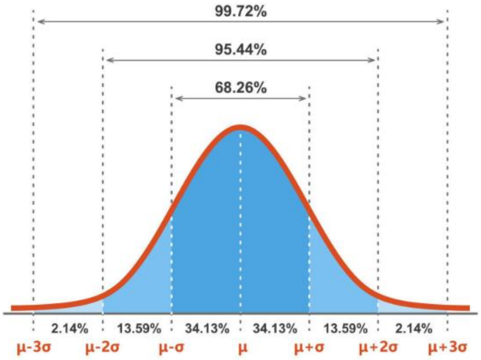


Figure 3.3: Probability density function of a Gaussian, or normal, distribution

Figure 3.3 shows the distribution of a Gaussian PDF.

According to the GUM, the calculation of the measurand uncertainty has to be based on the law of the propagation of the error and the central limit theorem [55-58].

Hence, this evaluation can be generally carried out solving Eq. 3.1 and Eq. 3.3 where $x_i$and $u(x_i)$ represent the best estimate and standard uncertainty of the input quantity, respectively, and X_i, Y and $u(Y)$ represent the best estimate and standard uncertainty of the output quantity Y (the measurand), respectively [23-36].

The combined uncertainty of Y is defined by the Eq 3.3 if the input quantities can be represented as independent random variables, a figurative example is shown in Fig. 3.4.

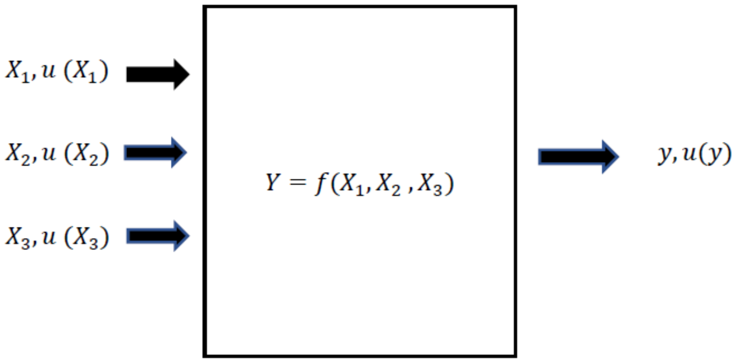


Figure 3.4: Uncertainties propagation for 3 input quantities

Figure 3.4 shows a system with three input quantities, namely X_1, X_2 and X_3. Each of them is described through its corresponding PDF; $g_{X_1}(\xi_1)$, $g_{X_2}(\xi_2)$ and $g_{X_3}(\xi_3)$ (Fig. 3.5). Where ξ_i represents the possible values which the input quantities can assume.

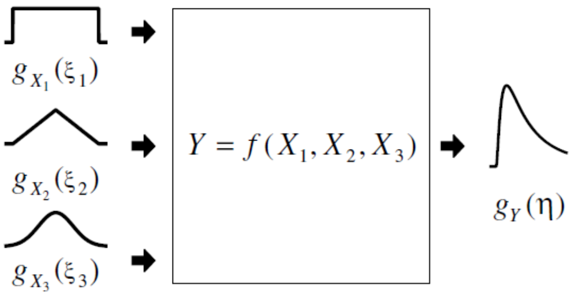


Figure 3.5: Example of the distributions for 3 independent input variables

As shown in Figure 3.5, $g_{X_1}(\xi_1)$ is represented by a gaussian PDF, $g_{X_2}(\xi_2)$ by a triangular PDF, and $g_{X_3}(\xi_3)$ another gaussian PDF again. The resultant PDF of the measurand Y is $g_Y(\eta)$.

3.1.4 Disadvantages in Using the GUM Method for Estimating Uncertainties of EMC Equipment

The GUM uncertainty framework is valid for measurement models that are linear in each input quantity where the calculation of combined measurement uncertainties is usually done via uncertainty propagation as described within the GUM uncertainty framework. For this, uncertainty propagation is easily computed in models in which the partial derivatives can be easily evaluated. However, this method presents significant disadvantages when considering measurement instruments such as an EMC testing device. Transistors, diodes, mixers, and amplifiers, among other components, cannot be easily approximated to a linear model. Therefore, the conjecture considered in Eq. 3.1 is not fulfilled.

Hence:

$$Y \neq f(X_1, \dots, X_n) \tag{3.18}$$

Furthermore, input quantities may be correlated with each other, and therefore:

$$r\left(x_i, x_j\right) \neq 0 \tag{3.19}$$

being r the correlation of the input estimates x_i and x_j.

These considerations make the computation of the measurement uncertainty according to the GUM very difficult and unlikely to be solved [50-59]. For such cases, the Monte Carlo simulations are a wide-accepted method to evaluate the uncertainty propagation [44].

3.1.5 – Overview of MCM simulations

Monte Carlo Method (MCM) relies on the randomness principle to solve deterministic problems. It provides an approximation of the PDF of the measurand by generating M vectors of length N, being M the number of input quantities and N the number of trials. Each vector is passed though the model and the corresponding output variable Y is obtaiend. Those values are then sorted in a non-decreasing way and the cumulative PDF of the measurand is estimated.

Since computer can easily simulate large number of trials and generate random numbers, MCM became a well-accepted method to solve difficult probabilistic problems.

Anyway, since the number N of simulations required is high, the power required to solve complex models might be too much and limit the practical implementation of the methodology itself [43-44,60]. The advantage is that for MCMs the model does not need to be linear with respect to the input quantities and they can be represented by any PDF (Gaussian, rectangular, triangular etc.).

3.2 Proposed methodology for uncertainty evaluation.

To accurately characterize any instrument, it is essential to comprehend how its metrological performance is influenced by the nominal tolerance of the components implemented as well as how various external factors influence its uncertainty. It is widely known that temperature, humidity, geometry, and applied electrical field may have a significant impact on any electronic or electrical component. The extent of influence of each factor mentioned depends on the operating conditions and design choices, thus a comprehensive evaluation is needed. The following methodology allows to determine the overall measurement uncertainty, evaluate the impact that mixed external factors may have on the measurand, reduce the number of parameters to be evaluated and ultimately propose a practical solution to reduce the overall system uncertainty.

3.2.1 Measurement steps

The steps followed are summarized hereafter:

1. The following equation is solved to obtain the number of simulations N of the MCM trails.

$$N = h * \left(\frac{1}{1-p}\right) \tag{3.20}$$

Where p is the coverage probability and h a large integer number, typically varying between 10^3 and 10^4 [41-48].

2. The influence of each parameter on the measurand is analyzed. According to [53-56] there are several ways to estimate it. An example is based on evaluating:

$$R(i,j) = \frac{\mathrm{C(i,j)}}{\sqrt{\mathrm{C(i,i)C(j,j))}}} \tag{3.21}$$

Where $\mathrm{C} = \mathrm{cov(x,y)} = \mathrm{E[(x - \mu_{\mathit{x}})(y - \mu_{\mathit{y}})]}$, $\mu_x = \mathrm{E[x]}$ and $\mu_y = \mathrm{E[y]}$

x contains Ns samples of Np model parameters. Y contains Ns rows, each row corresponds to the cost function evaluation for a sample in x.

Obtained values are in the $[-1,1]$ range. The (i,j) entry of R indicates the correlation between $\mathrm{x(i)}$ and $y(j)$. Hence:

- $\mathrm{R}(i,j)$ > 0, Variables have positive correlation. If one increases, the other one increases.
- $\mathrm{R}(i,j)$ = 0, Variables have no correlation.
- $\mathrm{R}(i,j)$< 0, Variables have negative correlation. If one increases, the other one decreases.

Equation 3.15 is iterated for each "i" component of the model under study.

3. After evaluating the influence of each parameter, each of them is allocated into one of the subsequent sets:

SET 1: Parameters whose variance strongly affects the measurand, $|\mathrm{R}(i,j)|$ >0.5.

SET 2: Parameters whose variance slightly affect the measurand, 0.1<$|\mathrm{R}(i,j)|$ ≤0.5.

SET 3: Parameters whose variance does not have influence on the measurand. $|\mathrm{R}(i,j)|$ ≤0.1.

The proposed classification, which may vary depending on the specific case being examined and the critique of the measurement which is being computed (for instance, there is a huge difference between the severity of an inaccurate measurement obtained from a plane altimeter versus a home energy meter), enables a clear identification of the specific components that require close evaluation in order to maintain effective control over the overall measurement uncertainty.

4. In order to evaluate the influence that N external factors may have on the measurand, step 3 has to be iterated N times and the results have to be classified accordingly.

   In this case scenario, the study is focused only on temperature variations. As a result, a separate round of sensitivity analysis is conducted, and the outcomes are categorized as follows:

   SET 1’: Includes parameters that strongly affect the output measurand, $|\mathrm{R}(i,j)|$ >0.5.

   SET 2’: Includes parameters that slightly affect the output measurand, 0.1<$|\mathrm{R}(i,j)|$ ≤0.5.

   SET 3’: Includes parameters that do not affect the output measurand, $|\mathrm{R}(i,j)|$ ≤0.1.

3.2.2 Description of the EUT

The method described in the previous section has been applied to evaluate the measurement uncertainty of a commercial instrument. The EUT under evaluation is a commercial EMI receiver, and its real circuit is shown in Fig. 3.6.

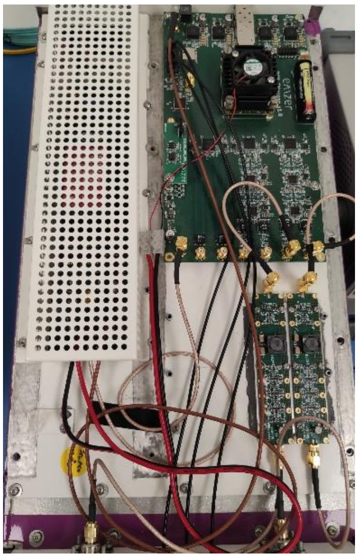


Figure 3.6: Actual input measurement chain of the EUT

The two input receivers are connected through an external bridge to the internal LISN, used to lead the conducted interference emitted by an external electric device towards the two receivers. The block diagram of the input stage of each of this receiver is shown in Fig. 3.7. It consists of four differentiated blocks, as described below:

- Transient limiter: protects the delicate input of the EMI receiver from surges or spikes. This block is composed by a high pass filter and a pulse limiter that introduces a desired attenuation of 10,00 dB.
- Antialiasing filter: filters any frequency out of the 9 kHz to the 110 MHz range to avoid aliasing effects.
- Variable attenuators and amplifiers: conditions the input signal to a suitable amplitude level in order to be appropriately measured.
- Filter and input analog-to-digital converter (ADC): final filtering and conversion to the digital domain.

Figure 3.7: Block diagram of the input part of the EMI Receiver considered.

The blocks represented in Figure 3.7 have been modeled in the following way:

1. The measurand, the quantity that has to be measured, is defined.
2. The variables upon which the measurand depends have been determined and modeled.
3. According to the information available from the manufacturer, different PDFs have been assigned to each variable.
4. The number N of iterations is defined by solving Eq. 3.20.
5. The PDF of the measurand has been obtained by propagating the uncertainties though the model.

3.3 Results and Discussion

The measurement uncertainty of the input chain of the EMI receiver described above (fixing the variable attenuators and amplifiers to 0 dB of gain, so that the whole chain offers an attenuation of 10 dB, due to the transient limiter, on the whole useful bandwidth) has been calculated under different conditions. The PDFs assigned to the components vary to characterize the different behaviors of each component. This allows a comprehensive analysis of the results, obtained by using manufacturers' provided data or alternative PDFs to account for missing information. For this, when analysis varying temperature are carried out, a triangular distribution has been assigned to the components, especially the ones distant from ADCs or amplifiers, which are not subject to a wide range of temperature variation. This is to provide a better characterization of their actual behavior since the temperature gradient that they are exposed to is different from components near, for instance, a power supply without forced ventilation.

The following sections show the results obtained.

It is important to keep in mind that the methodology presented later is specifically focused on addressing uncertainty evaluation problems arising in real applications and/or developments. Avoiding complicated and time-consuming assessments during the design phase is precisely why a detailed uncertainty evaluation is not typically carried out.

3.3.1 Results obtained using traditional MCMs approach.

Since the variable attenuators and amplifiers have been set to 0 dB of gain, the amplitude of any external RF signal entering to the transient limiter will arrive to the ADC input should be attenuated by design by 10 dB.

Table 3.1 shows the results obtained when the nominal value of the components composing the four blocks of Fig. 3.7 changes according to different types of PDFs.

As discussed above, a rectangular distribution reflects the principle of maximum entropy and lack of information, and therefore it reflects the worst-case scenario [48-52]. The triangular distribution has been used when the relationship between different variables is known but collecting more data is too complicated [48-52].

In this example, the first number of trials N has been set to 10.000, value obtained by setting h=2000 and p=80% in Eq. 3.18.

Table 3.1. Results obtained with N=10.000 iterations

Number of simulations	**PDF assigned**	**Mean**	**Maximum deviation from mean value**
10.000	Rectangular	10,41 dB	0,71 dB
10.000	Triangular	10,41 dB	0,68 dB
10.000	Mixed Triangular and Rectangular	10,41 dB	0,69 dB

Figure 3.8 shows the distribution obtained.

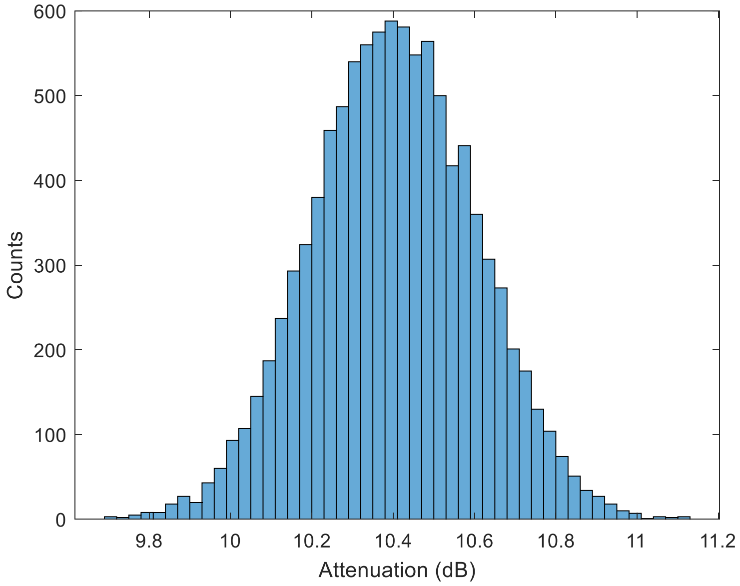


Figure 3.8: Distribution of the output voltage setting N = 10.000 iterations.

As shown in Figure 3.8, the measurand presents a normal shaped distribution, the mean value obtained is centered in 10,41 dB, hence presenting a 0,41 dB difference from the value expected by design (10,00 dB).

3.3.2 Results obtained with the proposed method.

It is demonstrated that by computing a fraction of N iterations the result can be used to estimate the mean value and the standard deviation of the model if twice the standard deviation associated with it is less than the numerical tolerance associated with the standard uncertainty u(y) [41-50]. Table 3.2 summarizes the results obtained when the same set of the

PDFs used in Table 1 are assigned to the component values, but with a number of simulations N equal to 5.000 and 3.000.

Table 3.2. Results obtained with lowering the number of iterations.

Number of simulations	**PDF assigned**	$\mathbf{Mean}$	**Maximum deviation from mean value**
5.000	Rectangular	10,72 dB	1.02 dB
5.000	Triangular	10,63 dB	0.89 dB
5.000	Rectangular and triangular	10,67 dB	0.90 dB
Number of simulations	**PDF assigned**	$\mathbf{Mean}$	**Maximum deviation from mean value**
3.000	Rectangular	10,86 dB	1.30 dB
3.000	Triangular	10,79 dB	1.20 dB
3.000	Rectangular and triangular	10,84 dB	1.24 dB

In this particular case scenario, the resulting PDF obtained when performing simulations with a lower number of trials that the one indicated in Table 3.2 does not show a normal distribution. Furthermore, its variance is more than double than the one associated the previous results shown in table 3.2. According to [42-44], this is sufficient to state that the results are not significant anymore. Hence it can be concluded that in this particular case scenario, the minimum number of iterations to obtain meaningful results is $N = 3.000$. It is indeed true that with more investigation it could be possible find out the real the limit, but it is not important for this evaluation.

Another series of MCM simulations, setting $N = 4.000$, have been carried out to evaluate how the measurand varies along the whole operating frequency range, the results are shown in Figure 3.9.

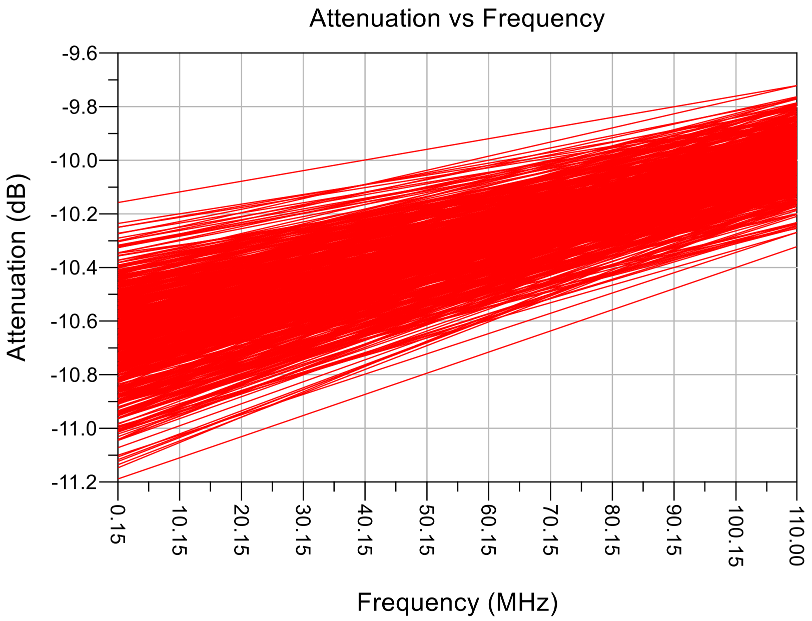


Figure 3.9: Distribution of the attenuation over frequency.

These simulations allow the evaluation of the entire measurement chain's response across the whole frequency range. The graph presented shows interesting findings, with attenuation exceeding the expected 10,00 dB at lower frequencies, while at higher frequencies, the attenuation tends to fall below 10,00 dB. Consequently, when measuring signals with higher amplitudes, extra caution should be exercised in the higher frequency range as the instrument's attenuation is lower than predicted by design. These results provide insight into the system's actual behavior, which may deviate from the expected design and help prevent unexpected damage to the internal circuitry.

Considering that the time needed by the CPU to compute and process one MCM results can easily vary within 1 sec and 5 minutes [60], it becomes evident that a vast use of MCM simulations is still limited by the enormous time required. Additionally, the time required to compute each simulation can vary greatly depending on the complexity of the model and the computational power of the laptop.

Table 3.3 shows the estimated computational time needed to carry out the uncertainty evaluation for the system under analysis.

Table 3.3. Time vs number of iterations

Number of Simulations	Number of parameters	Estimated total time required
10.000	91	Aprox 3.10 hours
5.000	91	Aprox 1.38 hours
3.000	91	Aprox 50 minutes

Therefore, it is evident that defining the appropriate number of simulations is crucial for significantly decreasing the computational time and power required for evaluating the overall measurement uncertainty. In this particular case, the results can be obtained approximately six times faster.

3.3.4 Evaluation of the influence of the parameters on the measurand

The influence that each parameter has on the measurand has been evaluated. Components are named using a letter (R stands for resistor, C for capacitor and L for inductor) and a number, which is used to identify the component in the actual circuit diagram.

For intellectual property protection, the actual schematic of the measurement chain analyzed (Fig. 3.6) cannot be shown here.

Considering the obtained and the methodology explained in section 3.2, three components have been found to be in the level of influence A, five components in the level of influence B and eighty-two components in the level of influence C. In concrete:

SET 1: R97, C188, C193.

SET 2: R178, L22, R13, R12, R15.

SET 3: C311, R44, R29, L24, C187, R171, R24, R6, R27, R32, L36 and all the remaining.

Having identified the components which have more influence on the measurand allows one to perform uncertainty evaluations only for components belonging to SET 1 and 2, disregarding all the components of group C since their influence on the measurand is relatively low. This allows to simplify the model under study and to reduce the computational time needed to evaluate its uncertainty.

The new computational time required is shown here:

Table 3.4 Time vs number of iterations and number of parameters

Number of Simulations	Number of parameters	Estimated total time required
3.000	91	Aprox 50 min
3.000	8	Aprox 8 min

The results shown in Table 3.4 indicate that by decreasing the number of parameters, the computational time is reduced, resulting in a calculation time that is nearly seven times faster than before. This proves that the total time needed for the simulations is influenced by both the number of parameters and the number of MCM iterations. By comparing the shortest and longest computation times obtained (as shown in Table 3.3 and 3.4), a reduction by a factor of 23 can be observed.

3.3.5 Evaluation of mixed influence factors on the measurand

The overall uncertainty of a system is minimized when the correct components of the measurement chain are selected. Extreme care should be taken because the choices made in this stage will have an impact on the overall uncertainty of the instrument.

In this case, if the design is based only in the first set of simulations, the parameters belonging to SET 1 will be the chosen in the most accurate way and, most likely, they will be more expensive. This decision would give good results in case external factors were not present at all, which is extremely unlikely to happen in real case applications.

Hence, another series of sensitivity analysis has been carried out to evaluate the effect that external factors (in this case temperature) may have on the measurand. Of course, this evaluation differs for any EUT, furthermore it depends on several factors such as working and environmental conditions.

In this example, a temperature variation of 45°C from the standard reference temperature of 25°C has been considered to evaluate the effect that a temperature gradient has on the measurand. According to the manufacturer information provided for each component, the variation has been assessed.

According to the results obtained, the following components have been found to be in the level of influence 1', 2' and 3'. In concrete:

SET 1': R178, R97, R171.
SET 2': C317, R44, R6, R15, L24 R32, C187, L22.
SET 3': C311, R24, C188, R13, R12, R27, L36, R29, C193 and all the remaining.

As an example, it is possible to notice that parameter R171 belongs to SET 3 and SET 1'. This means that the temperature has a strong impact on this component and must be monitored closely. By analyzing the classification obtained it is possible to determine which components contribute more to the overall system uncertainty. Therefore, if there is a need to decrease the overall uncertainty of the measurand, it can be accomplished by directly acting these components. Furthermore, the following considerations can be drawn:

- A parameter which belongs to SET 1 and 1' must have low tolerance and high temperature performances since every variation will highly affect the measurand.

- A parameter which belongs to SET 1 – 2' must have a low tolerance, but it is less important its exposure to a temperature variation.

- On the contrary, if a parameter is identified to be in SET 3 -1', it is not so much important to keep its nominal tolerance under control, but it is important that the temperature exposure is controlled and kept as constant as possible.

By incorporating this information into a circuit simulator, one can easily assess the level of uncertainty of any system by adding only the parameters that have the greatest influence on the measurand. Also, the overall calculation time for the system's uncertainty can be significantly reduced. Naturally, the classification of the groups can vary depending on the specific criteria chosen for the application.

The methodology proposed has been validated by analyzing the input stage of a commercial EMI receiver but can be applied without loss of generality to other cases. Computing the measurement uncertainty by strictly using the approach proposed by the GUM has been shown to be a difficult task. Thanks to the methodology proposed, the uncertainty associated with the measurand can be reduced by simply acting on the component having the highest influence of the measurand. It also important to remember that the method proposed is general and can be applied in different fields and situations without loss of generality.

3.4. Conclusions

A measurement instrument is properly designed when the influence that each parameter has on the measurand is kept under control. The methodology presented shows, both from a mathematical and experimental point of view, how to evaluate the measurement uncertainty by means of PDFs relying on Monte Carlo Simulations.

The first step to overcome is related to the practical need to reduce the number of MCM simulations required to estimate the overall uncertainty of a system, a problem which still limits a common use of MCM simulations.

Material, tolerances, degradation over time and temperature dependence shall be analyzed carefully because every variation introduced will strongly impact the overall uncertainty. Also, placing in a correct position the actual components play an important role. It is well known, for example, how an increase of the operating temperature can reduce the average life of any electric components and change their performances over time [57]. The proposed methodology allows to consider all these effects by acting on the PDFs of the input variables.

Finally, this method proposes a simple and practical solution that can also be applied to perform budgetary evaluations when components belonging to different SETs have to be purchased. The considerations proposed in this chapter will be useful while developing a new measurement instrument.

CHAPTER 4

4. Optimal design of a single-phase power line filter

International EMC standards set specific limits and methodology for CE levels [1,2]. The measurement methodology involves the use of a LISN inserted between the power source and the EUT, which presents a known power source impedance to the EUTs. The most common way to reduce the CE of the EUT that does not meet the requirements of the standard is by adding a PLF between the PLN and the EUT [3].

A common strategy to select a suitable PLF involves relying on its IL, a figure of merit provided by manufacturers.

As explained in the introduction, it is stated in CISPR 17 [3], Annex C, that the IL of PLFs can be measured with 50 Ω impedances at their input and output ports or, to evaluate a worst-case scenario, with 0.1 Ω and 100 Ω impedances at their input and output ports respectively, and vice versa. However, actual EUTs and PLNs present complex input impedances very different from the aforementioned values, which vary with the frequency (in most cases, from a very high magnitude value to a very low one due to the parasitic effects and/or to the electrical component behaviors). Therefore, it is not possible to accurately estimate the real IL of a PLF when connected between them [50-54].

On top of that, commercial PLFs present static structures to mitigate both CM and DM interference (almost all PLFs contain, at least, an X-type capacitor at the line side, a CM choke, and two Y-type capacitors at the load side), and some of these components may not be strictly necessary or may not be placed in their optimal position for a specific EUT. Therefore, an oversized PLF is usually used to obtain the same mitigation that an optimal, but much smaller PLF could achieve.

The other way to obtain an appropriate PLF is by designing it. This problem has been extensively discussed in the literature with different approaches and methodologies [13-30,68-88]. Accordingly, most EMC designers have developed their own modus operandi based on their experience, knowledge, and available instrumentation. In most cases, it ends up being a trial-and-error process since, again, there is a lack of information regarding the actual impedance of the EUT and the PLN, essential information to obtain an optimal result.

Hence, it seems that measuring the impedance of EUTs and PLNs should solve both problems stated above, but although this is something that can be done, it is tricky, and specific instrumentation, not always available is needed.

In order to make the PLF design easier, the input impedances of different topologies of switched-mode power supplies (SMPSs), the most common electronic circuit found at the power-line terminals of electric and electronic devices, have been analyzed. The aim of this analysis is to determine if different topologies of EUTs need different structures of PLF for optimal CE mitigation. If that were the case, the relationship between the EUT topology and the PLF structure could be established, making the design of the optimal PLF much easier for EMC engineers.

To this end, the Scattering (S) parameters of different topologies of DC-DC converters (which are a type of SMPS) connected to a power source, which include a Buck converter, a Boost converter, and a single-ended primary-inductor converter (SEPIC), have been measured switched on. From these measurements, the circuital models of each topology, along with their parasitic components, have been extracted [83-86]. Special care has been taken to model the component parasitic effects, circuit layouts, and couplings since they all strongly affect the behavior of the input impedance [83-88]. Working with equivalent circuits instead of the measured S-parameter matrix allows a better comprehension of the SMPS input impedance and the CE phenomena while this information is scattered within the S-parameter matrix. Then, a PLF design methodology, based on an accurate IL estimation of the PLF for the CM and DM CE, developed and described in this chapter, has been applied to find the optimal PLF structure for one of the DC-DC converters. The results obtained show that the work presented is useful to drastically reduce the cost and the time duration for the optimum PLF selection or design since it provides the optimal PLF structure for three specific DC-DC converters and the methodology to find the optimal PLF for any other kind of SMPS.

4.1. Circuit Models of the SMPSs

This section illustrates the circuital models of three SMPSs.

4.1.1. Model of Buck Converter

A Buck converter, also known as a step-down converter or step-down chopper, is a DC-to-DC power converter designed to perform a step-down conversion of the input signal and typically operates with a switching frequency between 100 kHz and a few MHz. The model that describes the behavior of a real Buck converter [83-86], with parasitic and non-ideal components, is seen in Figure 4.1.

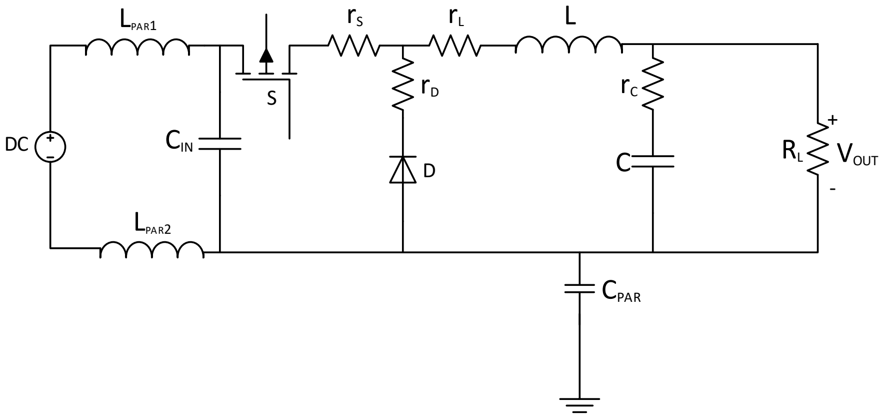


Figure 4.1: Model of Buck converter including parasitic components.

The inductor L, the controlled switch S, the capacitor C, and the diode D are the main components of the circuit. The load, in this case, is considered purely resistive and represented by a resistance R_L (since the DC-DC converter is evaluated alone). The rest of the components are the nonlinearities and parasitic effects introduced by the actual behavior of the circuit elements [83-86]. The parameters r_L, r_C, r_S, and r_D describe the equivalent series resistances of every component, and the L_{par1} and L_{par2} represent the parasitic inductance of the PLN. Finally, the capacitor C_{PAR} represents the stray capacitance towards ground.

The two modes of operation of the Buck converter are described below:

- Mode 1: The switch S conducts, and the diode D is blocked. The inductor L produces an opposing voltage across its terminals in response to the changing current. This voltage drop counteracts the voltage of the source and therefore reduces the net voltage across the load.

Mode 2: The switch S is blocked, and the diode D conducts. The inductor becomes a current source (the stored energy in the inductor’s magnetic field supports the current flow through the load).

4.1.2 Model of Boost Converter

A boost converter is sometimes called a step-up converter since it “steps up” the source voltage. The equivalent circuit of a real Boost converter is shown in Figure 4.2.

The same ideal and parasitic components as in the case of the Buck converter are considered.

The two modes of operation of the Boost converter are described below:

- Mode 1: The switch S conducts, and the diode D is blocked. The current is diverted through to the MOSFET through the inductor.

- Mode 2: The switch S is blocked, and the diode D conducts. The output capacitor is charged to the sum of the input voltage and the inductor voltage, stepping up the input DC voltage to higher output.

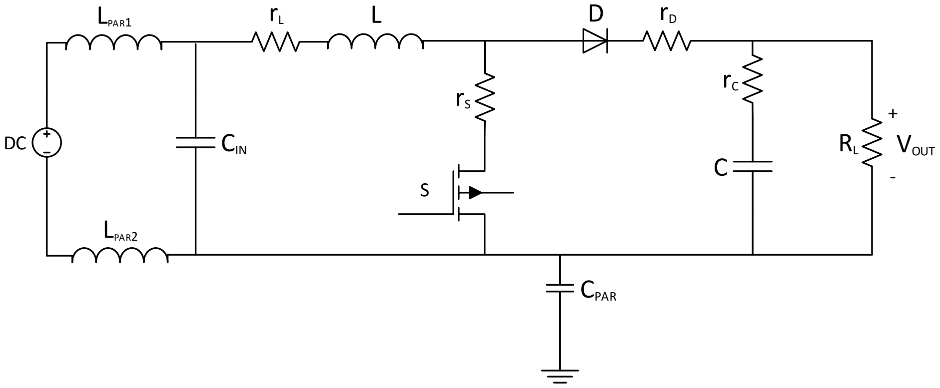


Figure 4.2: Model of the Boost converter, including non-ideal components.

4.1.3 Model of a SEPIC Converter

A SEPIC is essentially a boost converter followed by an inverted buck-boost converter. Therefore, it is similar to a traditional buck-boost converter but with some advantages due to its non-inverted output (the output has the same electrical polarity as the input). Figure 4.3 shows its equivalent circuit.

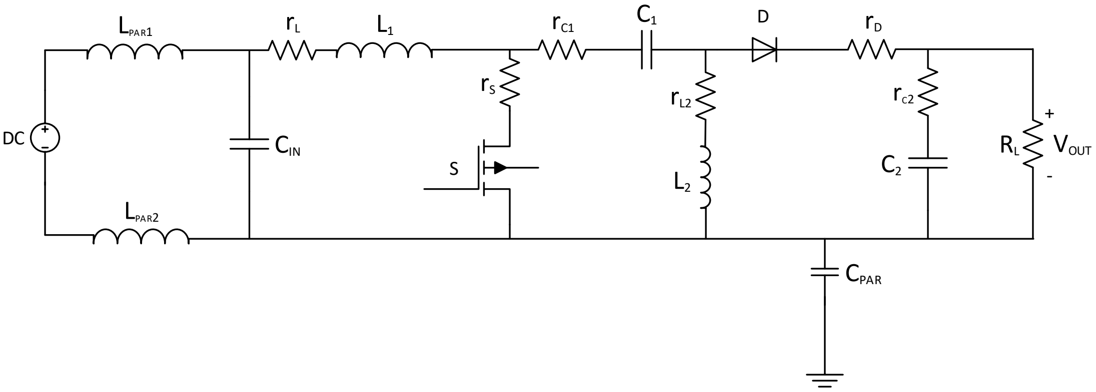


Figure 4.3: Model of SEPIC converter including non-ideal components.

The two modes of operation of the SEPIC converter are described below:

- Mode 1: The switch S conducts, and the diode D is blocked. The energy in L_1 is increased, and the capacitor C_1 transfers energy to the inductor L_2. Since the diode D is blocked, the load's energy comes from the capacitor C_2.
- Mode 2: The switch S is blocked, and the diode D conducts. The inductors L_1 and L_2 are discharged and provide energy to the load and to the capacitors C_1 and C_2.

4.1.4 EUT Characterization

In order to characterize a EUT (which includes the converters described above) connected to the PLN, to the LISN, or to any other kind of power network, two measurements are needed: S-parameters and CE [20-22]. To facilitate the measurements, SMA connectors have been added to the LISN-EUT interface ports and the wires of the DC-DC converters so they can be easily connected. The SMA connectors of the LISN-EUT interface are grounded to the RF ground of the LISN.

S-parameters can be measured using the setup described in Figure 4.4a, which basically consists of a vector network analyzer (VNA) and a LISN. As described in CISPR 16-2-1 [87], the LISN, needed to isolate the impedance present at the power-line ports, is bonded to a reference conducting surface by means of its grounding bar placed on the rear panel. The reference conducting surface is additionally connected to the ground of the electric power distribution system. The VNA is calibrated at the LISN–EUT interface (at the '+' and '–' terminals of the EUT) using a standard through-open-short-match (TOSM) calibration method to compensate the effects of the LISN, the transient limiters, and the cables (in this particular case, a commercial 50 Ω SMA calibration kit was used). Finally, to obtain a correct S-parameter measurement, the power of the interference generated by the EUT has to be negligible in front of the power delivered by the VNA.

The setup used to measure the CE at the terminals of the EUT (Figure 4.4b) consists of a two-port EMI receiver. The two-port EMI receiver is capable of providing direct information about the CM and DM CE, obtaining a complete representation of the EUT. Besides, it is possible to compensate for the effect of the LISN, the transient limiters, and the cables, making the measurement easier and faster.

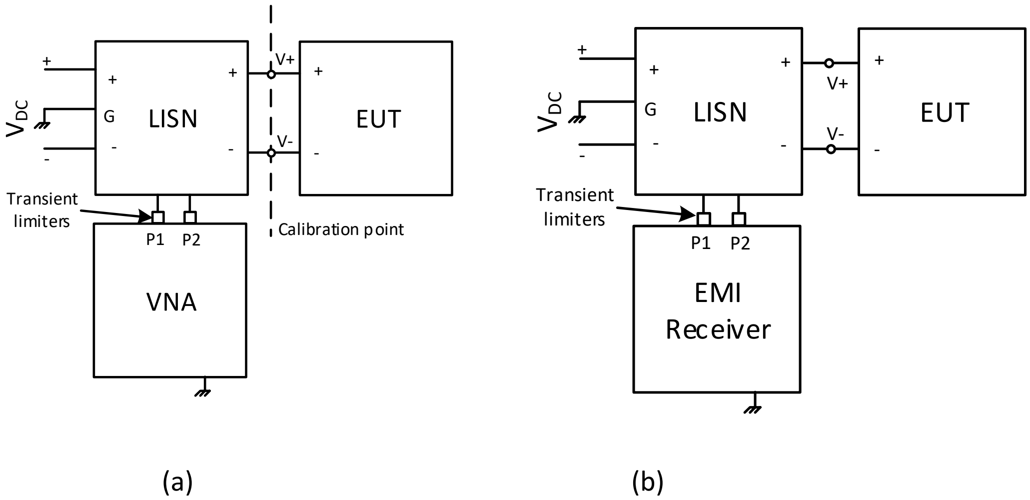


Figure 4.4: (a) S–parameter measurement setup; (b) CE measurement setup.

With both measurements, a complete characterization of the EUT is obtained from the EMC point of view and can be used in a circuit simulator to estimate the actual IL of a PLF. Besides, S-parameters can also be used to find the component values of the circuit models presented in previous section.

4.2. PLF Design

The main problem in evaluating the effectiveness of a PLF is that its actual IL cannot be estimated if line and load impedances are not known (which, for sure, will be different from 50 Ω). However, if the EUT impedance is characterized (using, for instance, the measurement setup described in Section 4.1.3), and the PLN impedance is known (in EMC measurements, the PLN impedance is always provided by the LISN, which internal circuitry is known), the actual IL of any PLF can be estimated using a circuit simulator or resolving the circuit equations using a programming computing platform. In this section, the method to estimate the actual IL of a PLF is described and latterly used to implement the optimal PLF.

4.2.1. Accurate Estimation of the IL of a PLF

Figure 4.5 shows the equivalent circuit of the EUT connected to the equivalent circuit of a LISN according to CISPR 16. The impedance of the EUT is represented with the measured S-parameters. The two voltage noise sources, V_{n+} and V_{n-}, are added to provide a fixed amplitude signal at all frequencies, which will be used to compute the accurate IL of the PLF (since the actual impedances of the EUT and the PLN are used instead of the usual 50 Ω, 0.1 Ω, and 100 Ω measurements). CM or DM conducted emissions can be emulated by switching the V_{n-} phase from 0° to 180°. The impedance of the LISN is represented by its internal circuit.

This is one among other different representations since the EUT could be modeled using the equivalent circuits shown in Section 4.2, and the LISN could be modeled using the measured S-parameters, but the same idea remains.

In any case, the IL of the PLF for one of the lines can be obtained with

$$IL|_{dB}^{+} = 20 * log_{10}\left(\frac{V_{ref}^{+}}{V^{+}}\right), \qquad (4.1)$$

and, for the other line

$$IL|_{dB}^{-} = 20 * log_{10}\left(\frac{V_{ref}^{-}}{V^{-}}\right), \qquad (4.2)$$

where V_{ref}^{+} and V_{ref}^{-} are the voltage at the '+' and '–' terminals of the LISN, respectively (or line and neutral in an AC system) when the signal is unfiltered (as seen in Figure 4.5, the measurement point is placed between the 0.25 µF capacitors and the 50 Ω resistors), and V^{+} and V^{-} are the voltage at the '+' and '–' terminals of the LISN, respectively, when the signal is filtered (as seen in Figure 4.6).

The relationship between the voltage at the '+' and '–' terminals and the modal voltages is:

$$V_{CM} = \frac{V^{+}+V^{-}}{2};\ V_{DM} = V^{+} - V^{-}, \tag{4.3}$$

Accordingly,

$$V_{CMref} = \frac{V_{ref}^{+}+V_{ref}^{-}}{2};\ V_{DMref} = V_{ref}^{+} - V_{ref}^{-}. \tag{4.4}$$

Therefore, the actual modal IL of any PLF can be obtained with

$$CM\ IL|_{dB} = 20 * log_{10}\left(\frac{V_{CMref}}{V_{CM}}\right) = 20 * log_{10}\left(\frac{V_{ref}^{+}+V_{ref}^{-}}{V^{+}+V^{-}}\right); \tag{4.5}$$

$$DM\ IL|_{dB} = 20 * log_{10}\left(\frac{V_{DMref}}{V_{DM}}\right) = 20 * log_{10}\left(\frac{V_{ref}^{+}-V_{ref}^{-}}{V^{+}-V^{-}}\right) \tag{4.6}$$

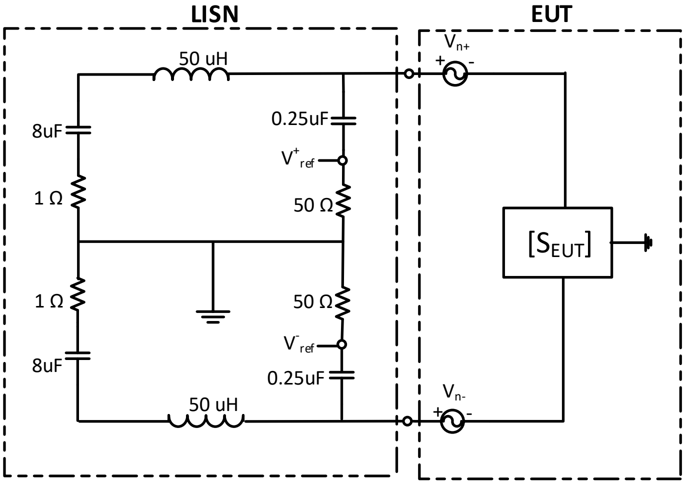


Figure 4.5: Equivalent circuit of the EUT connected to the equivalent circuit of a LISN according to CISPR 16.

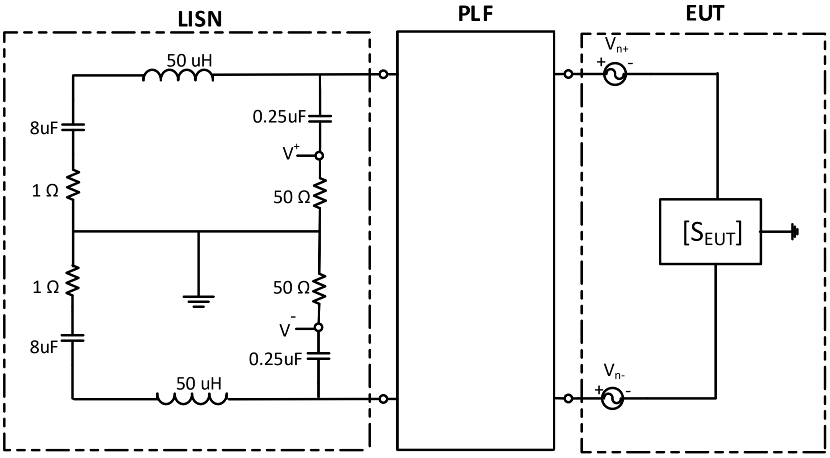


Figure 4.6: PLF connected between the equivalent circuit of a EUT and the equivalent circuit of a LISN according to CISPR 16.

4.3. PLF Design Methodology

The simplest structure of a PLF contains one or two X-type capacitors ($\mathrm{C_x}$) between line and neutral, usually located on the sides of the CM choke, to mitigate the DM, and a CM choke (with an inductance L) and two Y-type capacitors ($\mathrm{C_y}$) from line to ground and neutral to ground, usually placed on the load side, to mitigate the CM (Figure 4.7). A resistor ($\mathrm{R_1}$) is usually added to discharge the capacitors when the voltage is disconnected.

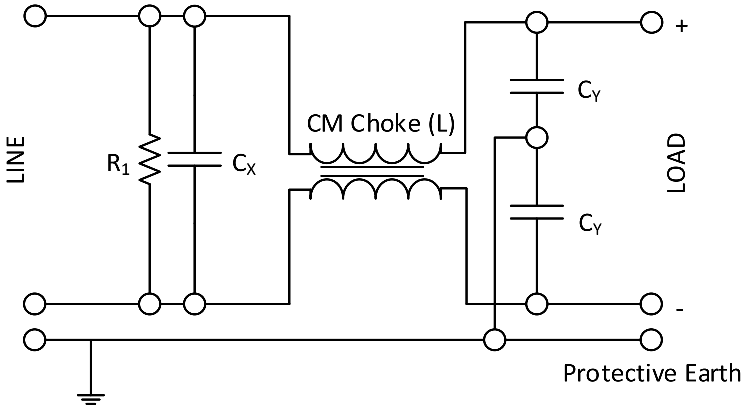


Figure 4.7: Typical structure of a PLF.

However, the PLF structure shown in Figure 4.7 may not be optimal for a specific EUT. Nevertheless, using the PLF modal IL estimation described above, different structures can be easily added and tested to find the optimal one.

Therefore, the methodology to design the optimal PLF consists of the following steps:

1. Measurement of the S-parameters of the EUT.
2. Measurement of the modal CE and determination of the IL needed to mitigate each mode under a threshold level.
3. Introduction of the S-parameters in a circuit simulator as a black box with two ports. The circuit is completed by adding two voltage sources and a LISN circuit, as seen in Figure 4.5. The two voltage sources emit the same amplitude at all frequencies, and their phase can be modified between 0° and 180° to have pure CM or DM CE, respectively.
4. The same circuit is implemented again in the simulator adding the PLF, as seen in Figure 4.6.
5. Both circuits are simulated in the frequency domain, obtaining the voltage amplitude at the measurement ports of the LISN in both cases (that is, $V_{ref}^{+}, V_{ref}^{-}, V^{+}, V^{-}$). The CM IL is computed using (4.5), and the DM IL using (4.6) (they are both introduced in the simulator, which provides the result).
6. Since each simulation needs less than a second to be completed, the determination of the optimal values for each PLF component and its optimal position inside the PLF is done manually using iterative simulations. Optionally, optimization techniques can be implemented to improve this methodology.

4.4 Experimental Validation

In this section, the three models of the converters are validated using S-parameter measurements. These equivalent circuits make understanding the input impedance and the CE phenomena easier since this information is scattered within the S-parameter matrix. Then, the CE of one of the converters is measured, and its optimal PLF is designed.

4.4.1. Validation of the Circuit Models

In order to validate the three models of the converters described in Section 4.2, the S-parameter matrix of the three converters has been measured using the setup described in Section 4.3, Figure 4.4a.

The load impedances connected to the DC-DC converters were known (preliminary measurements of the DC-DC converters were done using different load conditions, and, for each converter, the ones that provided the worst conditions, that is, the ones that caused the higher values in their conducted emissions, were selected). An actual picture of this same setup is shown in Figure 4.8.

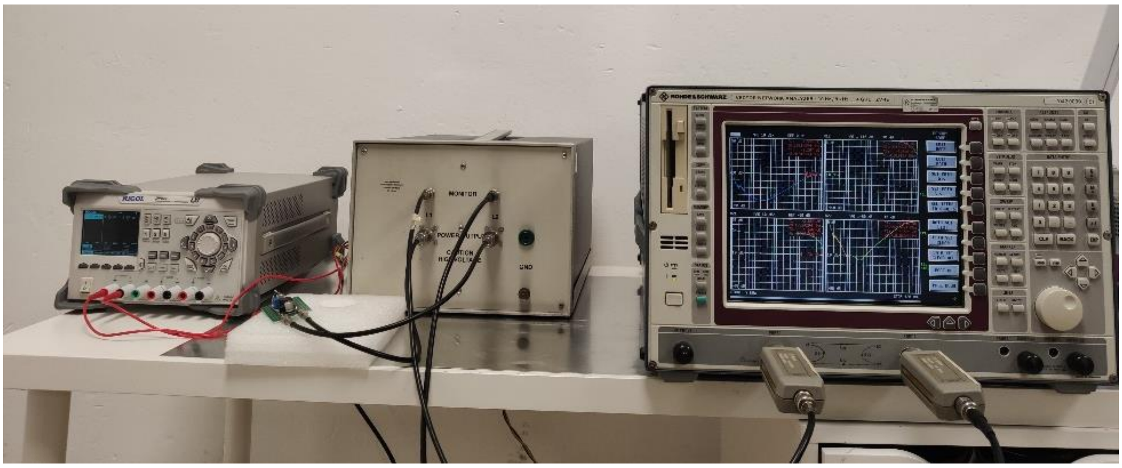


Figure 4.8: S-parameters measurement setup, which contains a EUT (front row, left side, placed above the foam), a VNA (right side) connected to two transient limiters, a two-port LISN (background, middle) and a programmable DC power supply (background, left side).

In order to find the values of the parasitic components, the following procedure has been followed:

1. The circuit model is implemented in a circuit simulator using the values provided in the datasheet for the normal components (C_{IN}, D, C, …). Parasitic components (C_{PAR}, L_{par1}, L_{par2}, r_S, r_D, r_C, r_L, …) are added with a '0' value. For each parasitic component, a margin of possible values is considered in the simulator.
2. The S-parameter measurements obtained from the actual EUT are also introduced in the circuit simulator.

   An optimization algorithm modifies the values of the parasitic components (within the specified margin) until the computed S-parameters of the circuit model are as equal as possible to the measured ones. In this case, the algorithm was based on the gradient search method, a generic optimization approach that iteratively updates the parameter until the error function is minimized or the maximum number of iterations selected is reached. The optimizers find the gradient of the error function (i.e., the direction to move parameter values in order to reduce the error function). Once the direction is determined, the parameter values is moved in that direction until the error function is minimized. Then the gradient is re-evaluated, this cycle is equal to one iteration of the gradient optimizers. When the results are satisfactory (that means that measured and computed S-parameters are very similar both in phase and amplitude), the values of the parasitic components are updated with the values found in the last iteration of the algorithm. Since it is a multi-parametric optimization, it may also possible that different combinations of parameters may satisfy the constraints imposed and provide a similar S matrix. In this case, provided that the values of parameters obtained have physical meaning and respect the constraints imposed, the characterization of the EUT is still valid and can be used for the optimal PLF determination.

The results obtained are shown below.

4.4.2. Circuit Validation of the DC-DC Buck Converter Power Supply Module Output 1.23 V–30 V, Model LM2596

Table 4.1 shows the values of the parasitic components obtained for the Buck converter model shown in Figure 4.1. In order to consider the worst-case scenario for the results shown in the following chapters, the measurement uncertainty associated with the parameters measured has been considered negligible with respect to the contribution to uncertainty introduced by the measuring equipment. The main reason for this is because the instruments used to perform the measurements had not been calibrated within the last year. Although the precise contribution could be estimated, for instance applying the methodology explained in chapter 3, it was not within the scope of this chapter.

Table 4.1. Values of the parasitic components of the Buck Converter model LM2596.

Symbol	Description	Value
C_{PAR}	Parasitic capacitance	14 pF
L_{par1}	Parasitic inductance	56 nH
L_{par2}	Parasitic inductance	1 nH
r_S,r_D,r_C,r_L	Parasitic resistances	200 mΩ

A few considerations should be added. L_{par1} and L_{par2} are placed before C_{IN}, and they play an important role in the circuit. The difference between the obtained values of L_{par1} and L_{par2} is due to the difference in the wire length used for the measurements. Although they do not significantly affect the computed amplitude of the S-parameters, these values influence their phase. On the other hand, although the capacitor impedance is small, its value is frequency dependent. At lower frequencies, its impedance is higher; therefore, the rest of the circuit is less isolated. The parasitic values obtained for C_{PAR}, r_S, r_D, r_C, and r_L, may not be as precise as L_{par1} and L_{par2}, but their combination in the circuit model helps to introduce the same effect as the actual circuit does after C_{IN}.

Figure 4.9 shows the comparison between the measured S-parameters and the computed ones using the circuit component values shown in Table 4.1 (to simplify the comparison, only the magnitude and the phase of the parameters S_{11} and S_{12} are shown since $S_{11} \approx S_{22}$ and $S_{12} \approx S_{21}$).

S-parameters were measured with the EUT switched on first and with the EUT switched off latterly. As can be seen in Figure 4.9, both measurements are similar. Looking at the circuit model of Figure 4.1, this behavior can be expected since the small impedance introduced by the input capacitor C_{IN} at the frequencies of interest isolates the rest of the circuit. This capacitor does not usually appear in an ideal representation of a Buck converter, but it is always used since it stabilizes the input voltage and mitigates the CE (a measurement without this capacitor is shown latterly for the SEPIC converter case as an example).

Regarding the circuit model, two simulations were done to emulate the switching behavior of the MOSFET and the diode. First, with the MOSFET active and the diode inactive, and second, the other way around. In both cases, active values were represented with a small resistance (200 mΩ) and inactive values with a high resistance (5 MΩ). However, the S-parameters obtained in both cases were identical, and the reason behind this is, again, the effect due to the small impedance introduced by the input capacitor C_{IN}. Therefore, only the first simulation (MOSFET active and diode inactive) is shown in Figure 4.9.

In any case, a good agreement is obtained when comparing both measurements with the simulation of the circuit model after updating the component values.

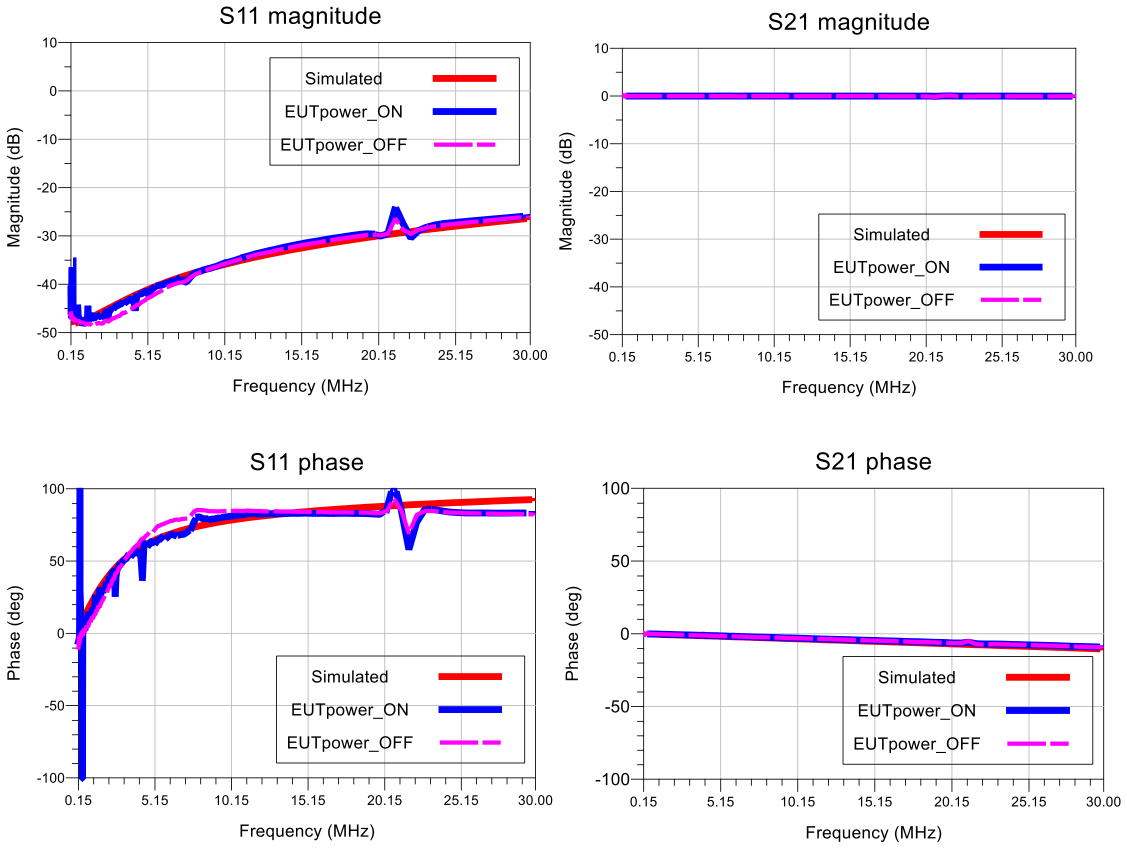


Figure 4.9: Comparison of the S−parameters obtained by simulations (red), EUT powered (blue), and EUT not powered (pink) for the Buck Converter Model LM2596.

4.4.3 Circuit Validation of the Boost Converter Model MCP1640EV-SBC

Table 4.2 shows the values of the parasitic components obtained for the Boost converter model shown in Figure 4.2.

Table 4.2. Values of the parasitic components of the Boost converter Model MCP1640EV-SBC.

Symbol	Description	Value
C_{PAR}	Parasitic capacitance	10 pF
L_{par1}	Parasitic inductance	199 nH
L_{par2}	Parasitic inductance	199 nH
r_S,r_D,r_C,r_L	Parasitic resistances	200 mΩ

Figure 4.10 shows the comparison between the measured S-parameters and the computed ones with the resulting circuit. The same considerations described for the Buck converter apply here. A good agreement is obtained between measurement and simulation, validating the circuit model of Figure 4.2.

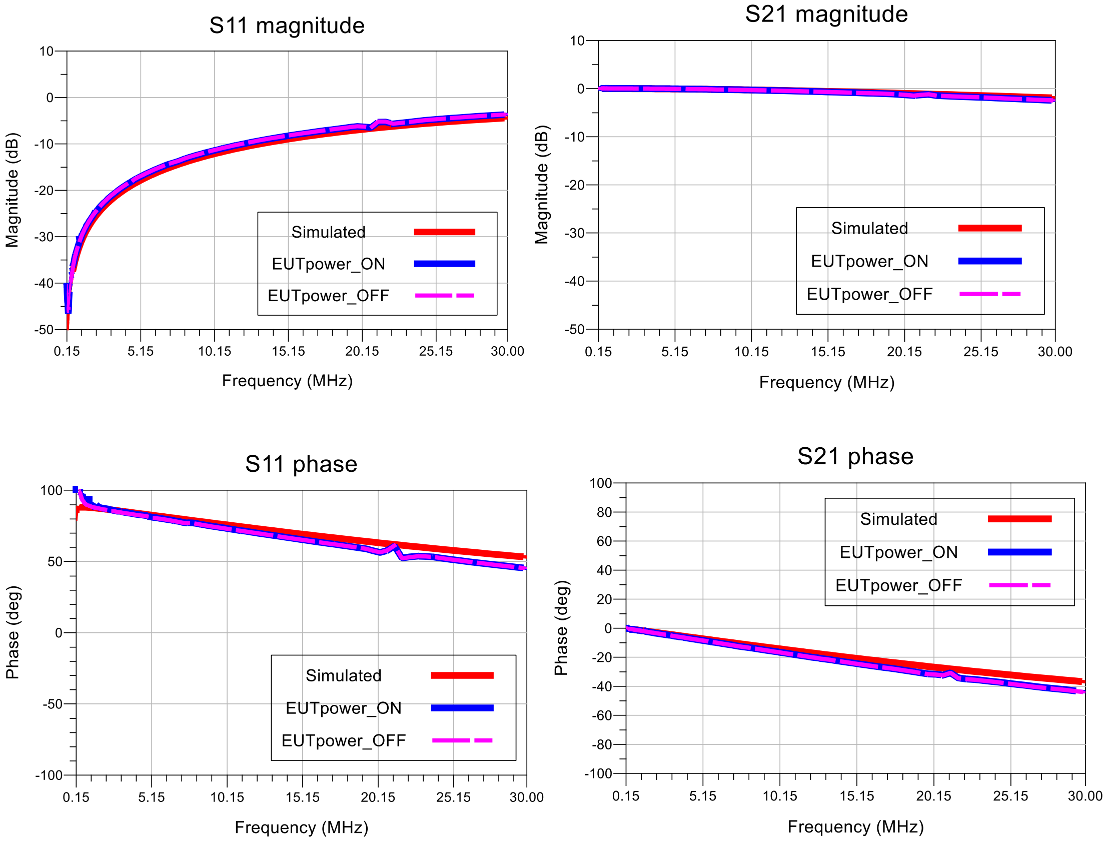


Figure 4.10: Comparison of the S–parameters obtained by simulations (red), EUT not powered (pink), and EUT powered (blue) for the Boost Converter Model MCP1640EV-SBC.

4.4.4. Circuit Validation of the DC-DC SEPIC Converter Model MCP1663

Table 4.3 shows the values of the parasitic components obtained for the Buck converter model shown in Figure 4.3.

Table 4.3. Values of the parasitic components of the SEPIC converter model MCP1663.

Symbol	Description	Value
C_{PAR}	Parasitic capacitance	21 pF
L_{par1}	Parasitic inductance	33 nH
L_{par2}	Parasitic inductance	9 nH
$r_S,r_D,r_{C1},r_{L1},r_{C2},r_{L2}$	Parasitic resistances	200 mΩ

Figure 4.11 shows the comparison between the measured S-parameters and the computed ones with the resulting circuit, obtaining, again, a very good agreement, although small differences are observed for the two-phase plots at lower frequencies.

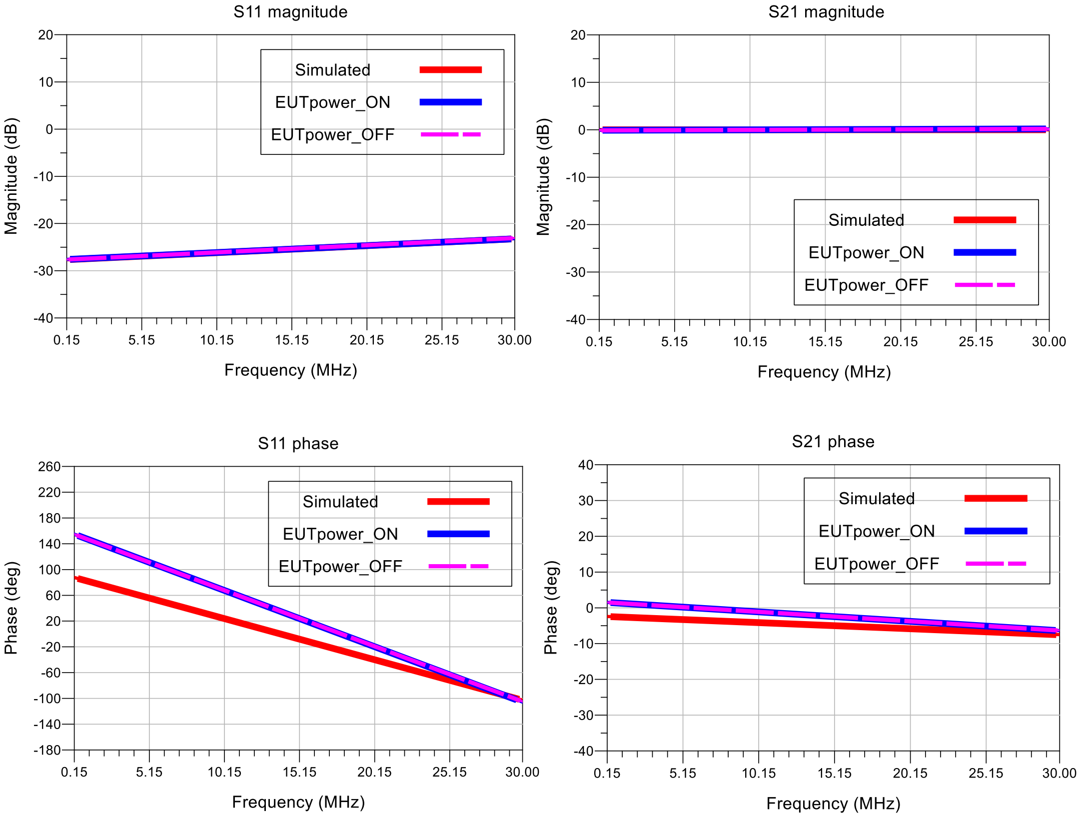


Figure 4.11: Comparison of the S−parameters obtained by simulations (red), EUT not powered (pink), and EUT powered (blue) for the SEPIC Converter Model MCP1663.

In order to show the effect of the input capacitor C_{IN} on the circuit, an additional measurement was done for this particular converter with the capacitor removed. Measurement and simulation results to show how S-parameter measurements are affected by the increment of the CE levels are shown in Figure 4.12.

At those frequencies where the CE levels are close to or above the levels of the transmitted and reflected waves of the VNA (which has already been configured to supply its maximum output power), the S-parameters become significantly inaccurate and useless. This measurement justifies the necessity of the capacitor C_{IN} from an EMC point of view since it reduces the CE and, therefore, improves the EUT characterization via S-parameter measurements.

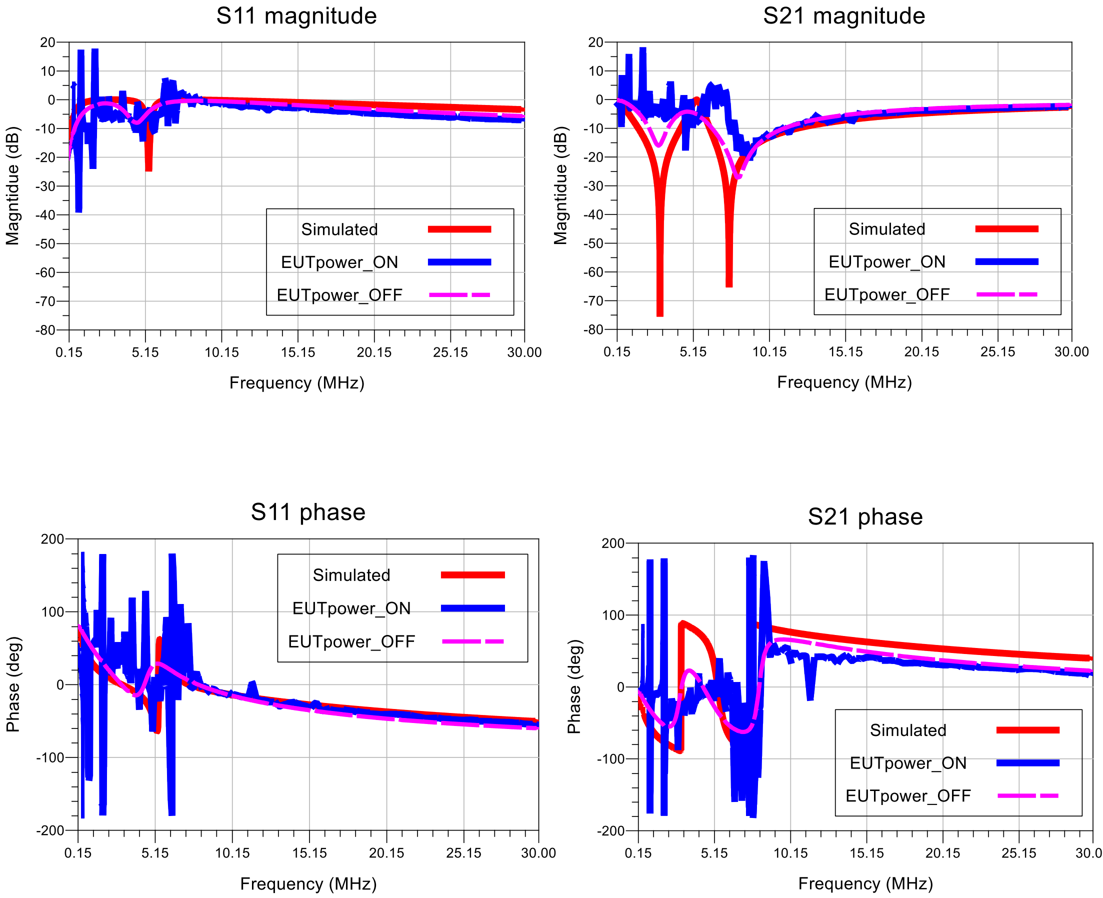


Figure 4.12: Comparison of the S–parameters obtained by simulations (red), EUT not powered (pink), and EUT powered (blue) for the SEPIC Converter Model MCP1663 after removing C_{IN}.

Since the three converters present a similar input impedance (due to C_{IN}), the following analysis (CE and PLF design) has only been applied to two of the converters.

4.5. Conducted Emissions Measurements

In this subsection, the CE of the Boost converter Model MCP1640EV-SBC has been measured. The setup for the conducted emissions measurements described in Section 4.3 (Figure 4.4b) is seen in Figure 4.13.
Figure 4.14 shows the CE measurement at the positive terminal (+) of the Boost converter using the quasi-peak (QPK) and average (AVG) detectors (similar results are obtained in the negative terminal (−)). It can be seen that at 500 kHz, the registered measurement is above the CISPR 32 class B limit [2] for both detectors. A minimum mitigation of 20 dB for the AVG detector is needed to meet this standard (a constant that will be later used to design its PLF).

Figure 4.15 shows the modal decomposition of the CE noise generated by the EUT, i.e., the CM and DM CE measured using the QPK detector. As it can be seen, the DM is the dominant mode, and this is, along with the input impedance (or S-parameters), essential information to design a suitable PLF. The CM emissions are far below the limit and, therefore, do not need further mitigation.

Figure 4.13: CE measurement setup, which contains a EUT (front row), a two-port EMI receiver (background, left side), and a two-port LISN (background, right side).

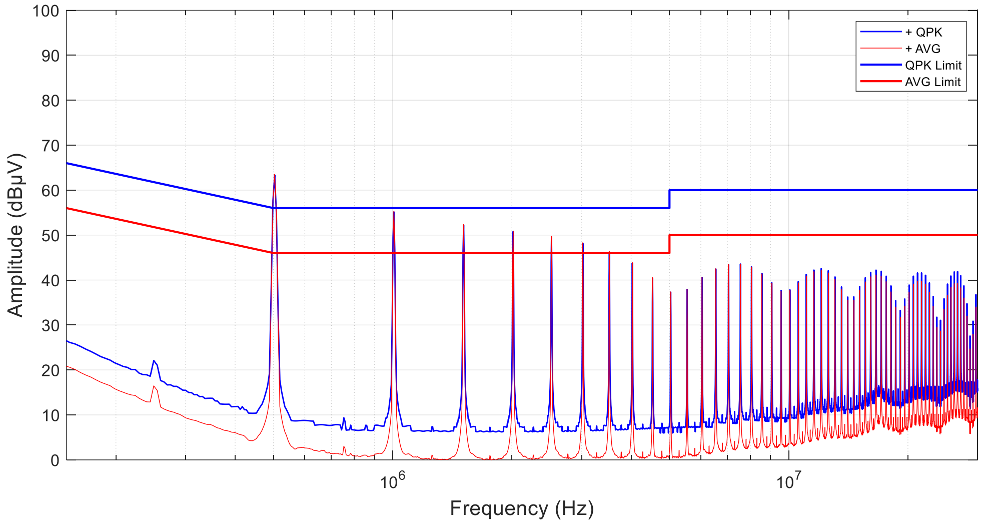


Figure 4.14: CE measurement at the positive terminal (‘+’) of the Boost converter using the quasi-peak (QPK, blue) and average (AVG, red) detectors.

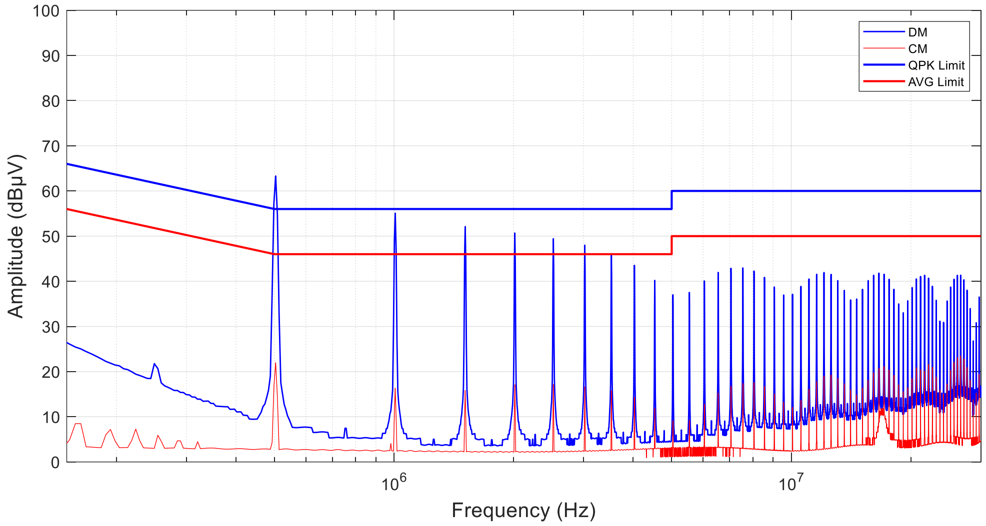


Figure 4.15: CM (red) and DM (blue) decomposition of the CE measurement of the Boost converter using the QPK detector

4.6. PLF Design for the Boost Converter

Looking at the emissions of Figure 4.15, it seems obvious that this EUT does not need a CM choke because CM emissions are far below the limit. Therefore, the specific PLF for this EUT needs to be implemented using those components that mainly affect the DM, i.e., the X-type capacitors. Considering that a minimum reduction of 20 dB is needed for the DM CE (so that the AVG detection falls below the limit), the question now is which capacitor value could be used to obtain such mitigation at 500 kHz. In order to avoid tedious trial-and-error practices, the methodology described in Section 4.4 has been applied. The PLF simulated consists of only an X-type capacitor, as shown in Figure 4.16.

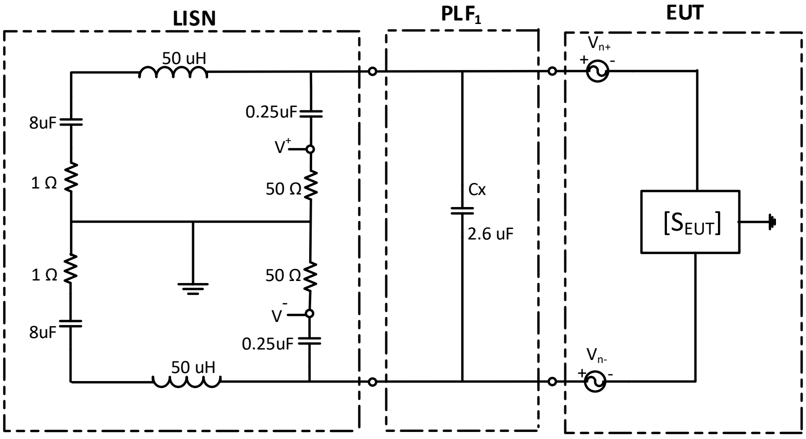


Figure 4.16. PLF connected between the EUT and the LISN consisting of only an X−type capacitor.

The procedure described in Section 4.2 (step 6) is repeated, giving different values to the capacitor until an IL of 20 dB is achieved, obtaining a value of 2.6 µF (Figure 4.16, PLF$_1$). For an X-type capacitor, this is a very high value (since typical commercial values go up to 0.47 µF). Therefore, a good alternative is to add an additional component to the circuit, i.e., to increment the order of the PLF, which allows the relaxation of the capacitor value while keeping the same attenuation at 500 kHz.

Figures 4.17 and 4.18 show two possibilities for a second-order filter (PLF$_2$ and PLF$_3$), both composed of a capacitor and a normal inductor in each line. Due to the use of different configurations of PLFs, the resulting input impedances of the DC-DC converter will also be different. Therefore, both circuits will present different mitigation at the LISN ports. The circuit models of Section 4.2 show that the input impedance of the converter is capacitive (due to C_{IN}), which means that the best option should be PLF$_2$ since it is the one that maximizes the mismatch between its input impedance and the input impedance of the DC-DC converter.

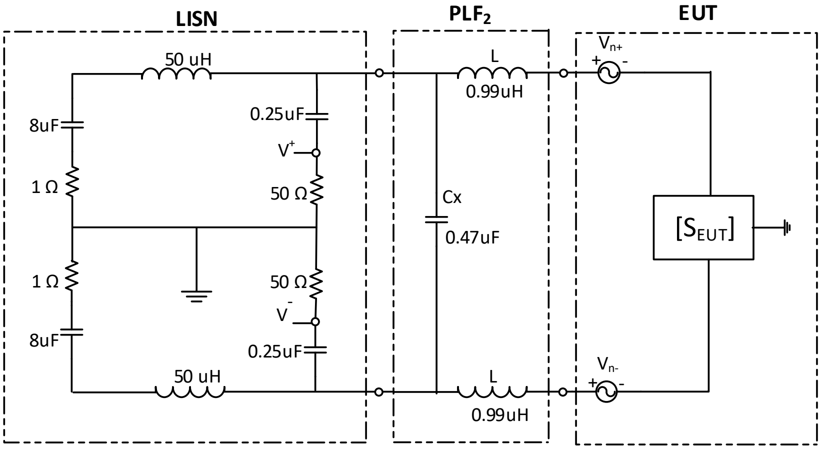


Figure 4.17. PLF connected between the EUT and the LISN consisting of an X–type capacitor and a DM inductor.

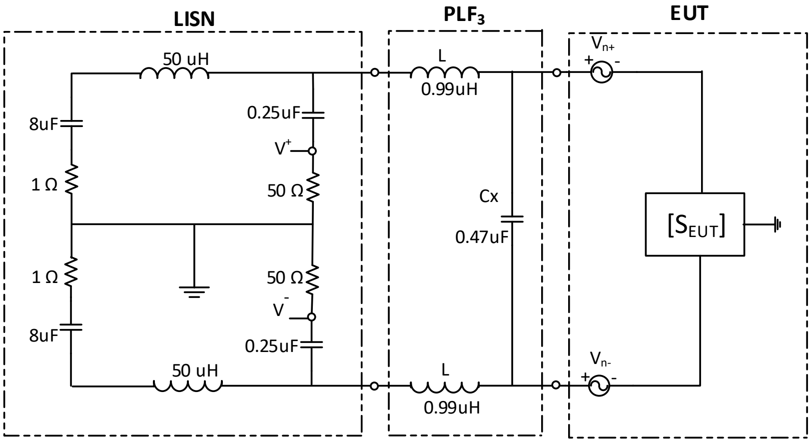


Figure 4.18: PLF connected between the EUT and the LISN consisting of a DM inductor and an X–type capacitor.

The procedure described in Section 4.2 is repeated again for these two filters. The inductance values for PLF$_2$ can be easily found by fixing the value of the capacitor to 0.47 µF (which is a standard value) and giving values to both inductors until an IL of 20 dB is achieved. In this particular example, an inductance of 1 µH was obtained.

Figure 4.19 shows the simulated DM IL achieved using PLF$_1$ (composed of a single X-type capacitor of 2.6 µF), PLF$_2$ (composed of two inductors of 1 µH at the load side and an X-type capacitor of 0.47 µF at the line side), and PLF$_3$ using the same values as in PLF$_2$ (that is, an X-type capacitor of 0.47 µF at the load side and two inductors of 1 µH at the line side). The IL for the three cases has been obtained by applying the procedure of Section 4.2 and, in particular, using (4.6). As expected, PLF3 has a negligible effect on the CE, while PLF$_2$, which has the same components but in the correct configuration/order, obtains the desired IL. PLF$_3$ can achieve the 20 dB of IL using inductors much larger (149 µH in this case), but this is not an optimal implementation, and therefore, it is discarded as a solution.

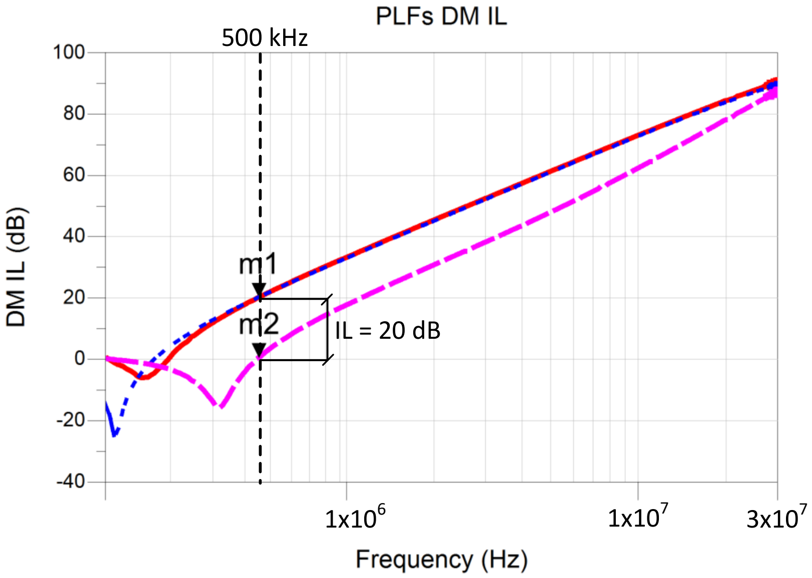


Figure 4.19: DM IL of PLF_1 (solid red line), PLF_2 (dotted blue line), and PLF_3 (dashed pink line).

Although isolated inductors are not typical components in PLFs, they can also be used. An alternative, but more bulky option, is to use, as a DM inductance, the leakage inductance of a CM choke, which can achieve values between 1–3% of the total inductance of the choke (with the benefit of additional mitigation on the CM, which may be needed in other applications).

The PLF obtained has been implemented and tested.

Figure 4.20 shows the CM and DM CE measured with the QPK detector. As expected, an attenuation of 20 dB is obtained.

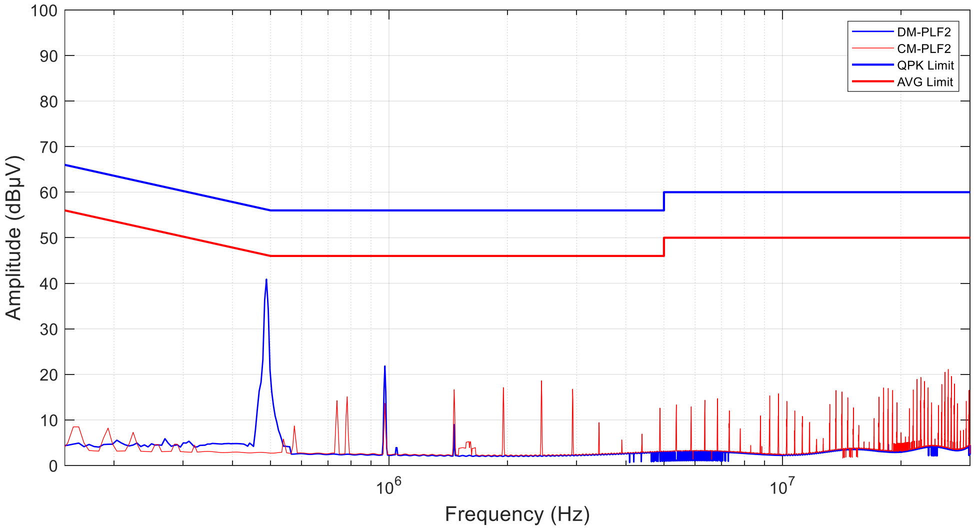


Figure 4.20: CM (red) and DM (blue) were obtained with a filter composed of a Cx = 0.47 uF and an L = 0.99 uH.

The attenuation inserted by the PLF₃ is shown in Fig. 4.21. As it can be seen, the EUT would have not been compliant with this type of filter.

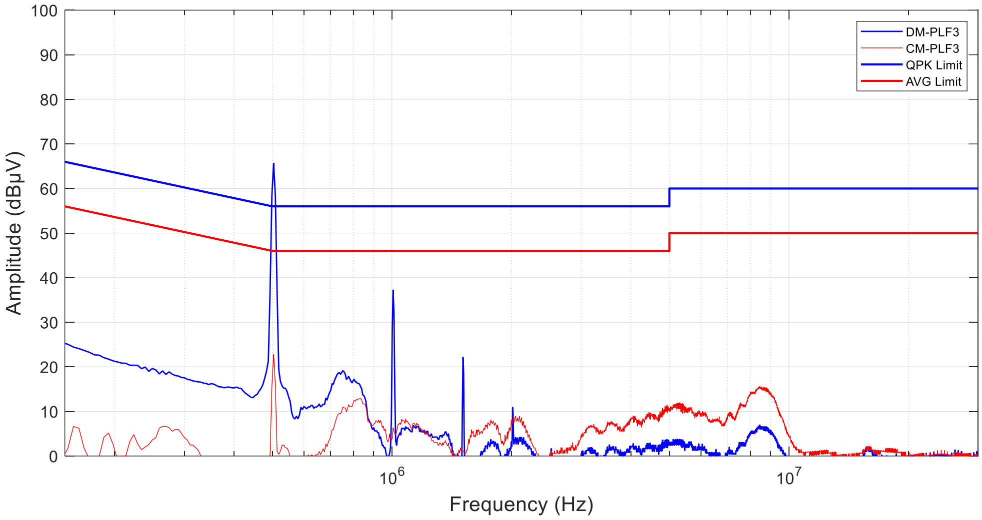


Figure 4.21: Modal noise measured after applying PLF₃

4.7 PLF Design for the Sepic Converter

In this subsection, the CE of the Sepic converter has been measured. The setup for the conducted emissions measurements described in Section 4.3 (Figure 4.4b) is seen in Figure 4.13.

Figure 4.22 shows the CE measurement at the positive terminal (+) of the Sepic converter using the QPK and AVG detectors (similar results are obtained in the negative terminal (−)).

It can be seen that the registered measurement is above the CISPR 32 class B limit [2] for both detectors. In this case, a minimum mitigation of at least 60 dB is needed to meet this standard.

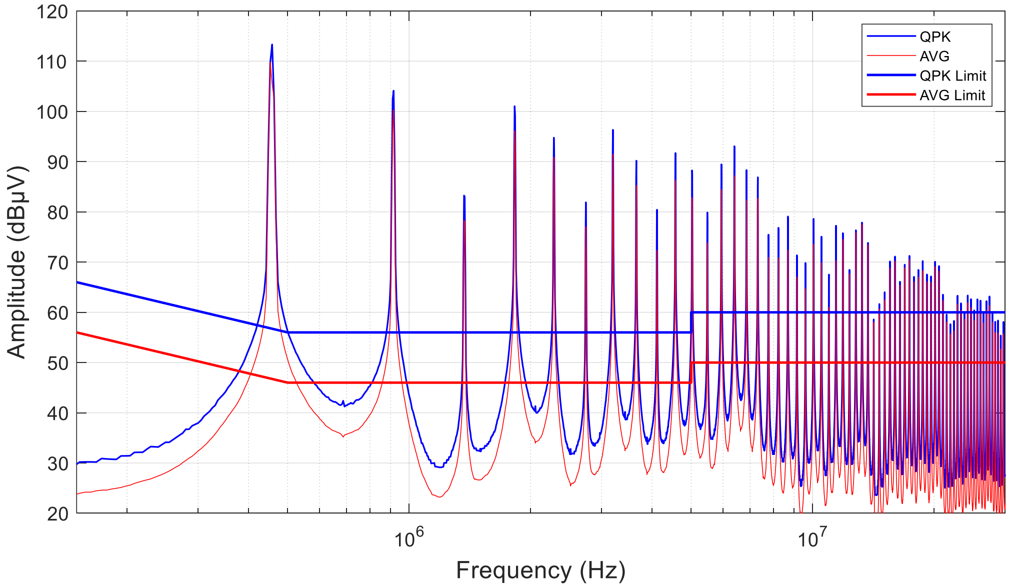


Figure 4.22: CE measurement at the positive terminal ('+') of the Sepic converter using the quasi-peak (QPK, blue) and average (AVG, red) detectors.

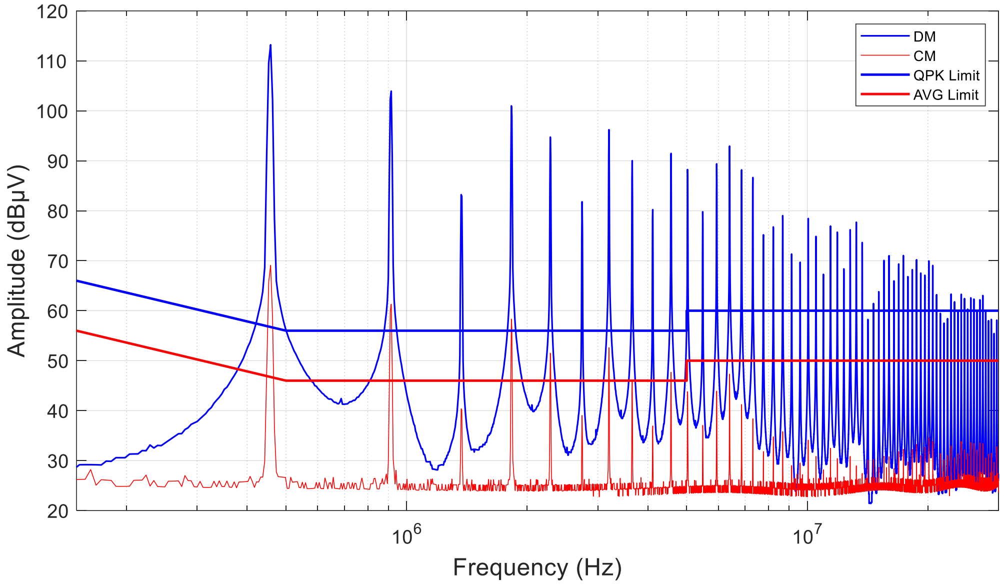


Figure 4.23: CM and DM measurement for the Sepic converter using the quasi-peak (QPK) detector

Figure 4.23 shows the modal decomposition of the CE noise generated by the EUT, i.e., the CM and DM CE measured using the QPK detector. As it can be seen, the DM is the dominant mode, and this is, along with the input impedance (or S-parameters), essential information to design a suitable PLF. In this case, the CM emissions are also above the limit, and need further mitigation as well.

Looking at the emissions of Figure 4.23, the specific PLF for this EUT needs to be implemented using those components that affect both the DM, i.e., the X-type capacitors and also CM, i.e., common mode chokes.

Considering the minimum reduction require for the DM and CM CE, the question now is which capacitor and CMC could be used to obtain such mitigation, starting from 500 kHz. In order to avoid tedious trial-and-error procedures, the methodology described in Section 4.4 has been applied.

The simulated PLF consists of an X-type capacitor and a CMC, as shown in Figure 4.24.

The procedure described in Section 4.2 (step 6) is repeated, giving different values to the C_x capacitor and CMC until the IL having the attenuation required is achieved.

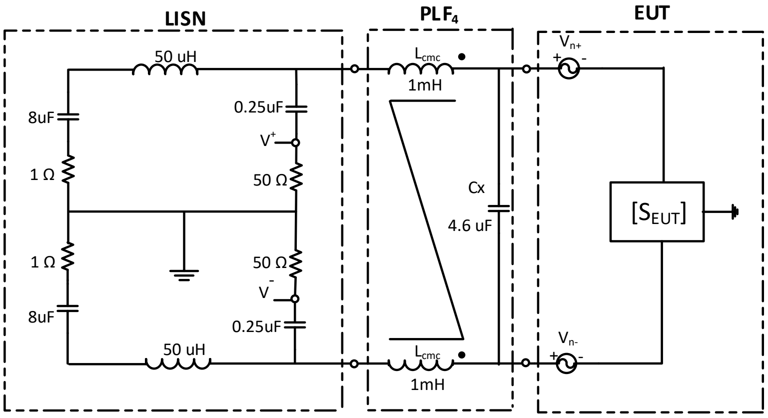


Figure 4.24: PLF connected between the EUT and the LISN consisting of an X–type capacitor and CMC.

As discussed in previous section, the founded value of 4.6 µF for an X-type capacitor, is a very high value (since typical commercial values go up to 0.47 µF). Furthermore, the size and weight of the PLF is also affected by the presence of the CMC, making the PLF design not feasible in real applications.

Hence, again the solution is to increment the order of the PLF, which allows to reduce the capacitor value.

In this case, the optimal PLF is composed by a $C_x$capacitor at the load side and a CMC at the line side. Once again, the procedure described in Section 4.2 is iterated to find the optimal values of the PLF, shown in Figure 4.25

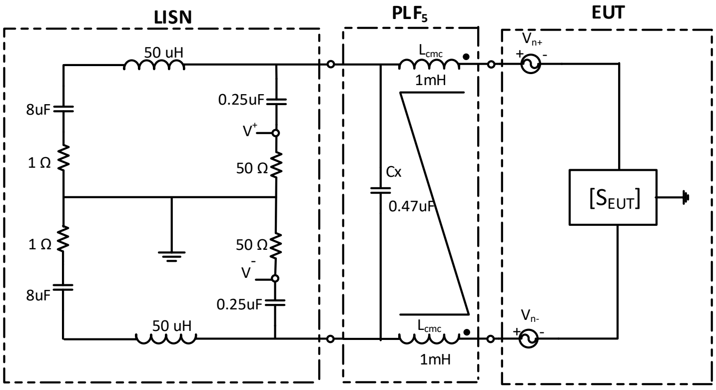


Figure 4.25: PLF connected between the EUT and the LISN consisting of a CMC and an X−type capacitor.

Figure 4.26 shows the simulated IL achieved using PLF₅ (composed of a $C_x$capacitor at the line side and a CMC at the load side).

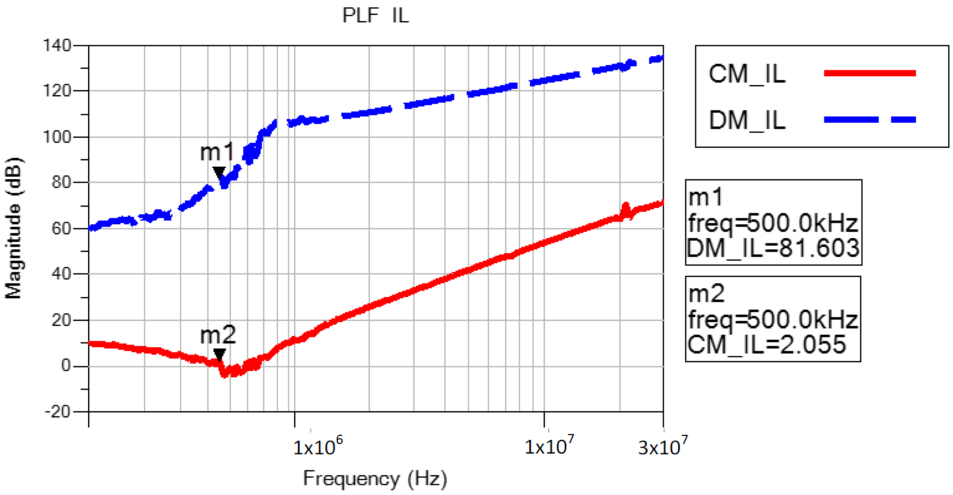


Figure 4.26.: DM IL and CM IL of PLF₅

The procedure described in Section 4.2 is repeated again for the new PLF. The capacitor values for PLF₅ have been found by fixing the value of the CMC and giving values to the C_x capacitor until the desired IL is achieved.

Figure 4.27 shows the simulated IL achieved using PLF₅ (composed of a CMC at the load side and an X-type capacitor at the line side. The IL for the three cases has been obtained by applying the procedure of Section 4.2 and, in particular, using (4.5 and 4.6).

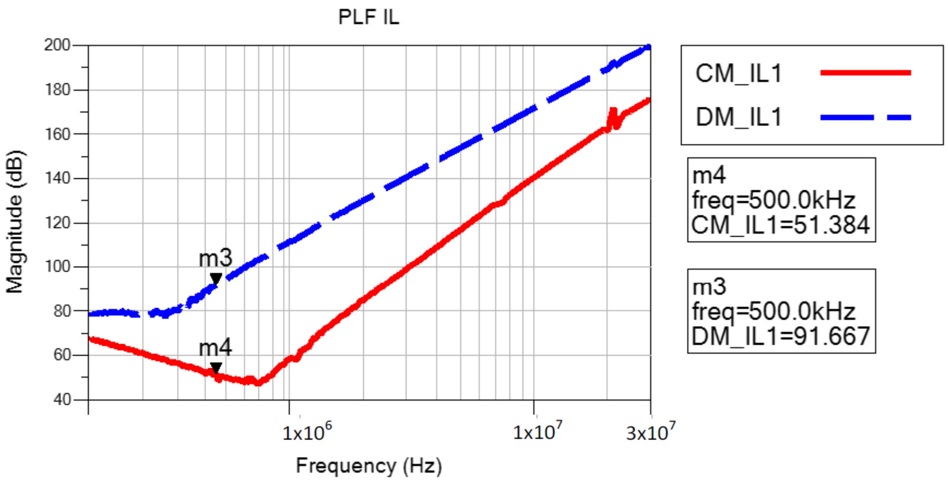


Figure 4.27: DM IL and CM IL of PLF$_5$

Both PLFs obtained have been implemented and tested. Figure shows the CM and DM CE measured with the QPK detector. As expected, the attenuation expect is obtained in both measurements.

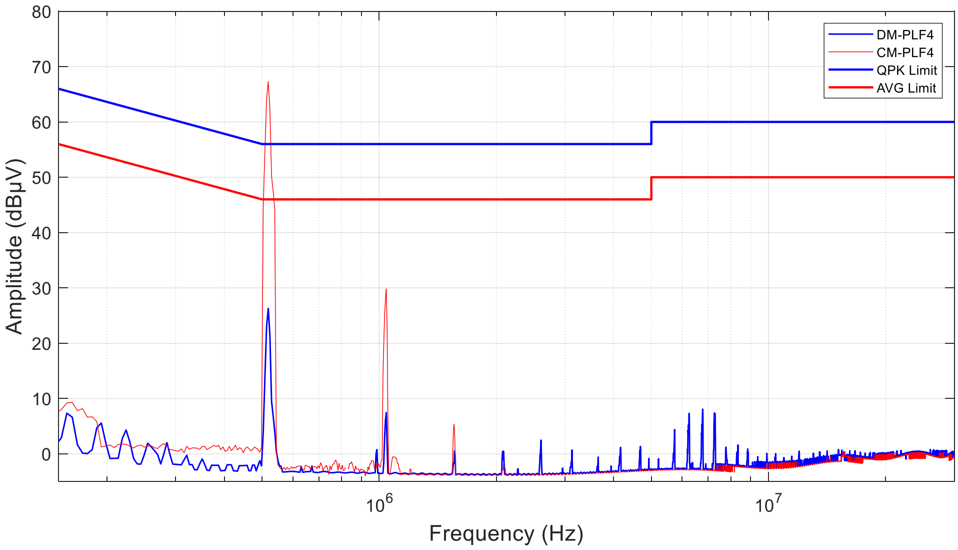


Figure 4.28: CM (red) and DM (blue) obtained with PLF$_4$.

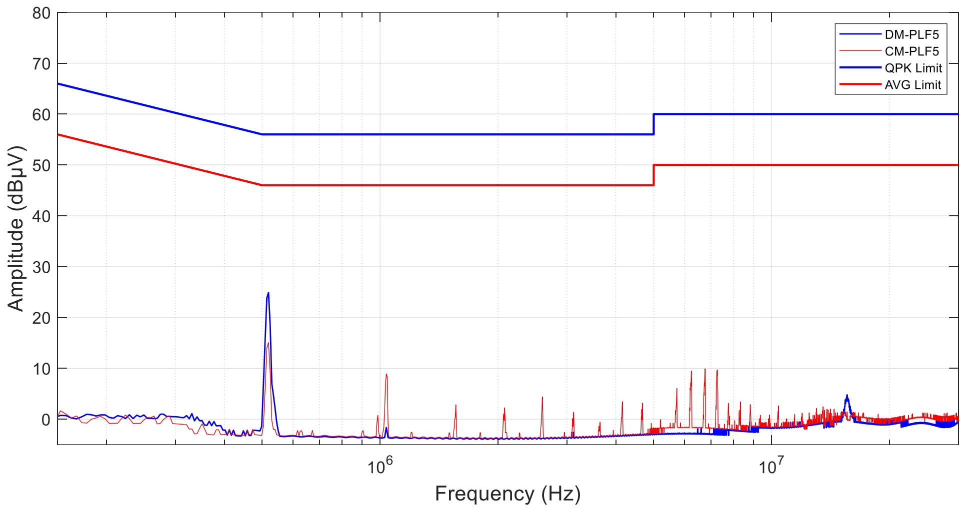


Figure 4.29: CM (red) and DM (blue) obtained with PLF$_5$.

These results show that the optimal structure for a PLF to be connected to a DC-DC converter, as the ones analyzed in these cases, is composed of an inductance or CMC at the load side of the PLF, and an X-type capacitor at the line side of the PLF, which differ from the typical structures provided by commercial filters manufacturers (as seen in Figure 4.07). By fixing the value of the X-type capacitor, it will be possible to easily find the value of the inductors (or the CM choke), and vice versa. This methodology allows to implement an optimal PLF quickly and accurately able to mitigate the CE under a certain threshold level, even without obtaining a complete characterization of the EUT. This result also shows that even in those cases where the dominant mode is the DM, increasing the value of the X-type capacitor may not be enough to obtain the desired mitigation. Moreover, this problem worsens if the switching frequency decreases since a smaller cutoff frequency may be needed.

Another consideration is that different SMPS, which can be contained in different types of enclosures made of different types of materials, may produce different CE (where the CM may become predominant). In that case, thanks to the methodology described, the CM choke value, along with its optimal position inside the PLF, can easily be found. Therefore, this work provides a good basis for establishing a reliable standard methodology to design optimal PLFs for any electric and electronic product.

4.8 Conclusions

Commercial PLFs provide standard structures that may not be optimal for specific EUTs. In this chapter, the input impedances of three different DC-DC converters, a Buck converter, a Boost converter, and a SEPIC converter, have been measured and modeled using circuit models to analyze their differences and determine the optimal PLF topology for each case. However, due to a common input capacitor in all circuits, typically used to stabilize the input DC voltage of the converter and mitigate the CE, all three converters present a similar input impedance. Therefore, the same PLF structure can be used for all of them.

Analyzing the CE of a Boost and Sepic converter and using a circuit simulator that contains their S-parameter characterization, the optimal PLF topology for each case was found. Its internal structure contains an inductance on both lines at the load side of the PLF to mitigate the DM noise (that can also be implemented using a CM choke as shown) and an X-type capacitor between lines at the line side of the PLF. This structure differs from typical structures used in commercial PLFs and obtains optimal IL results with fewer and smaller components.

CHAPTER 5

5. Optimal design of a three-phase power line filter

5.1 Introduction

Due to the recent proliferation of three-phase power electronics and three-phase charging stations [89-91], CE are becoming an increased concern for manufacturers, who are forced to comply with EMC regulations [1-3]. According to these standards, conducted emissions are evaluated in the frequency range of 150 kHz to 30 MHz, also known as band B [1].

Also for three phase systems, the most common technique to suppress CE noise in order to comply with EMI standard limitations [1] is to place a PLF between the EUT and the PLN.

Again, PLFs are selected by relying on the IL values, which are evaluated with 50 Ω impedances at the in-out ports or, to consider the worst-case scenarios, with 100 Ω and 0.1 Ω at the in–out ports respectively, as described in Annex C of CISPR 17 [3].

However, the actual impedance of both the PLN and EUT changes along with the frequency and can also be influenced by parasitic components. Hence, it is impossible to correctly determine the actual IL of a PLF [89-99].

According to the EMC standards, CEs are measured between lines with respect to the ground and, if present, with neutral respect to the ground [1]; thus, the actual values of the common mode and differential modes noises remain hidden inside the measured CE. This presents a first and major limitation for optimal PLF design, since also for three-phase systems each component present in the filter reduces either the CM or DMs. Hence, a detailed knowledge on the CE modal noise is required to design an optimal three-phase PLF.

Additionally, commercial three-phase PLFs are found as standardized structures designed to reduce both CM and DMs noises, but they are most likely oversized and more expensive than necessary; almost all structures are comprised by a CMC, at least three C_x capacitors, and at least three C_y capacitors, which might not be strictly necessary [94-112]. As a result, an oversized PLF is usually implemented. Obviously, an optimal PLF should be optimized in terms of performance, cost, volume, and weight.

Furthermore, it has been demonstrated that an impedance mismatch in the EUT or in the PLF leads to an unexpected energy exchange between DM and CM interference. This modifies the expected PLF performance and leads to unexpected CE levels [89-93].

Hence, the only way to achieve an optimal PLF design is by designing it.

At the time of writing this thesis and at the best of author knowledge, in literature is not possible to find a clear and standardized PLF design methodology for three-phase applications.

First of all, PLF design for three-phase EUTs is much more complex than for a single phase due to the presence of more lines which lead to completely different modal noise interactions [84-95]. Hence, the traditional CM/DM analysis [68-78] cannot be applied in a straightforward manner, and new models and definitions are needed.

A certain amount of research has focused on either CM or DM attenuation [100-112], without considering modal noise interactions and reflections due to impedance mismatches when implementing the PLF. As a result, a gap is left for optimal PLF design.

Also, certain practices to reduce and optimize the volume and size of the PLF have been proposed in the literature, for instance in [104,105]. Anyway, the accuracy of the PLF optimization process is compromised because the modal noises are not measured simultaneously. Furthermore, the methodologies proposed rely on a trial-and-error loop to define the CM and DM components to achieve the required attenuation, resulting in longer times to design the PLF.

Other works [108-112] have focused on evaluating how the modal CE contributes to increase the power grid pollution. Although a comprehensive analysis is proposed on the effects that CE noise have on the system, no specific details on how a PLF can be designed are presented.

In [113-118], external devices called modal separators were used to evaluate the modal noises generated by a three-phase EUT. Although these devices allow to perform a modal decomposition, they have several disadvantages which limit their implementation for optimal PLF design [113-118]. For instance, [113] proposes a detailed study on how asymmetries, amplitude, and phase mismatches introduced by the modal separator affect the overall modal measurement and ultimately, the PLF design.

As a result, no methodology has yet been recognized by the EMC community. Hence, most engineers developed their own procedures to design three-phase PLFs based on the available equipment, knowledge, information, and experience. Anyway, the actual PLF design is achieved only after several trial-and-error loops, since the actual PLN and EUT impedance is not known and, on top of that, there is no standard procedure to be followed.

In order to propose a solid and reliable methodology to design an optimal three-phase PLF, this chapter defines a generalized model to understand and analyze how the modal components present in the system interact between each other. Furthermore, it presents an overview of the available instrumentation that can be used to extract the CE noise, as well as the modal noises.

Then, simulations are carried out to determine the effect that each component present in the PLF has on either CM or DM noise. From these results, it is possible to define a specific and optimized PLF configuration, provided that the modal noises are known.

Finally, a solid design methodology relying on accurate IL estimation of the PLF for both CM and DM is presented and validated to determine the optimal PLF structure for a three-phase EUT.

The main contributions of this research are listed hereafter:

- A clear three-phase modal definition along with a review of the instrumentation capable of extract modal noises.
- A methodology to evaluate the behavior of any PLF component when the system is excited with either CM or DM noises, or a combination of both.
- A detailed PLF design methodology, based on an accurate IL estimation to reduce the CM and DM CE, experimentally tested, and validated in real case scenarios.

Overall, the results obtained and presented in this chapter are useful to understand the nature of the modal noises and to minimize the time and cost to design an optimal PLF. Furthermore, the methodology described can be applied to any EUT without a loss of generality; thus, it sets the basis to become a standard method to be followed to design an optimal PLF for three-phase applications.

5.2. Modal Definition: A Brief Review

As mentioned throughout this thesis, measurements performed according to EMC standards provide information about the total CE level of an EUT, but they do not provide sufficient information to design a PLF in case of non-compliance [1].

The following subsections provide a clear model and explanation to understand how the modal noises behave and interact between each other.

5.2.1. Three-Phase Modal Definition

As described in the introduction, any signal can be characterized in the following ways:

EMI: considering the actual phase voltages and currents.

Modally: considering its modal decomposition, which is, the common mode, along with its voltage and current, and differential modes, along with their voltages and currents.

Figure 5.1 shows how the modal decomposition of the currents can be obtained starting from the actual line currents.

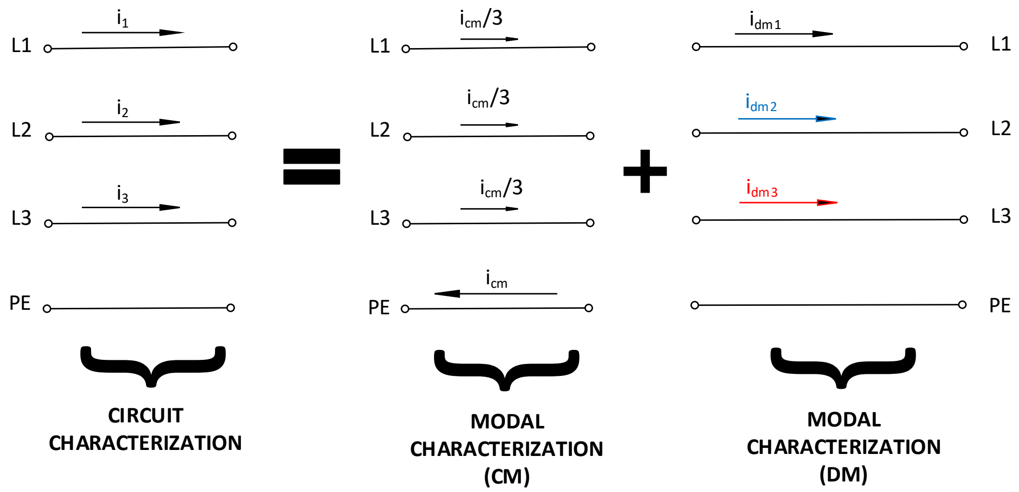


Figure 5.1: Circuital vs. modal characterization for a three-phase EUT currents.

By analyzing the circuit proposed, the following relationship can be derived:

$$i_i = i_{DMi} + \frac{i_{CM}}{3}; \quad \text{i=1,2,3} \tag{5.1}$$

where $i_{DM,i}$ is the DM current flowing in each phase, i_{CM} is the CM current and i_i is the actual phase current.

By definition, the sum of the DM currents is null [89-96].

$$i_{DM1} + i_{DM2} + i_{DM3} = 0 \tag{5.2}$$

Hence, the CM current is given by:

$$i_{CM} = i_1 + i_2 + i_3 \tag{5.3}$$

Figure 5.1 shows that CM and DM noise currents are defined by different propagation paths. The CM current flows though the loop formed by all phases and the protective earth line (PE), while DM noise currents flow in one phase and reclose in the other two.

A more detailed representation of this phenomenon is shown in Figure 5.2. For the sake of exemplification, only i_{DM1} is shown, but the same considerations are valid for i_{DM2} and i_{DM3}.

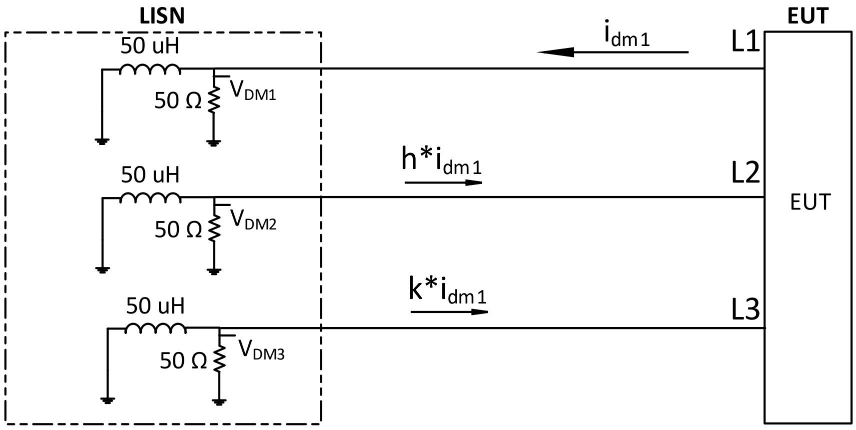


Figure 5.2: Path followed by i_{DM1} generated by an EUT when connected to a three-phase LISN.

In the figure, k and h depend on the system impedance and may assume different values case by case. Furthermore, the values of k and h for i_{DM1} do not necessarily have to be the same for i_{DM2} and i_{DM3} decomposition.

The complete modal equivalent circuit of a three-phase EUT connected to a LISN is shown in Figure 5.3. For the sake of simplicity, only the 50 Ω resistance of the LISN is shown.

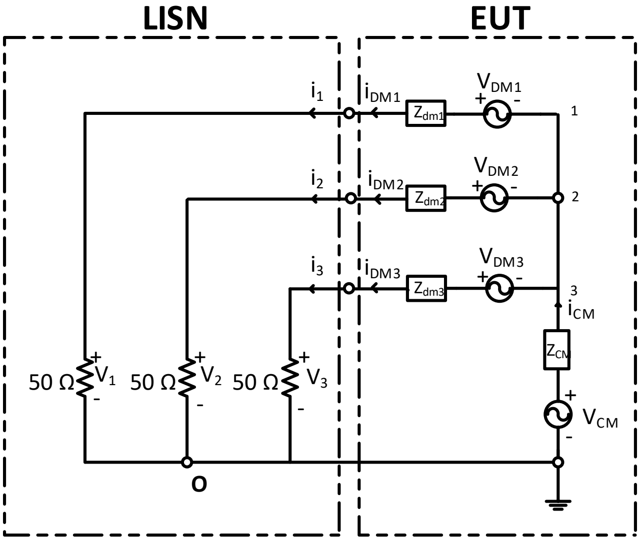


Figure 5.3: Equivalent circuit of a three-phase EUT connected to a LISN.

As can be seen in Figure 5.3, a combination of CM and DM voltage sources and their impedances are used to fully model the EUT CE noise; the CM voltage source (V_{CM}), which is common to all the three phases, and three independent differential mode voltage sources ($V_{DM,i}$), one for each phase (i = 1, 2, 3) [89-100].

By applying Kirchhoff's law to the loops of the circuit shown in Figure 5.4, the following relationship can be obtained:

$$V_i = V_{DM,i} + V_{CM}; \quad \text{for i=1,2,3} \tag{5.4}$$

where V_i represents the voltages generated by the current i_i when passing though the LISN's resistor. As defined in Equation (5.1), the current i_i is composed of a DM current ($i_{DM,i}$) and a CM current (i_{CM}). Hence, V_i is composed of the sum of a differential mode voltage ($V_{DM,i}$) and a common mode voltage (V_{CM}).

The CM voltage can be evaluated from the following relationship:

$$V_1 + V_2 + V_3 = (i_1 + i_2 + i_3) \times R_{LISN} = i_{CM} \times R_{LISN} = 3 \times V_{CM} \tag{5.5}$$

Thus, one can derive that:

$$V_{CM} = \frac{V_1 + V_2 + V_3}{3}.$$

From these considerations and definitions, and similarly to the single phase case, it is possible to derive that CM noise can be highly affected by straight capacitances present in the system. In contrast, DMs, which for instance can be generated by the voltage peaks coming from inductive load switching, are not affected by straight capacitances or ground connections [99, 113-118].

5.2.2. Filtering a Predominant Differential Mode Noise

In order to design an optimal PLF, it is necessary to evaluate the contribution that each modal noise has on the overall CE; that is, knowing each $V_{DM,i}$ and V_{CM}, which are voltages generated by the DM currents ($i_{DM,i}$) and CM current (i_{CM}) while flowing though the LISN. Hence, if only one among the three differential modes is prevailing, a different PLF structure than standard ones, for instance composed of three C_x type capacitors, shall be implemented.

For example, if V_{DM1}, is found to be the dominant DM noise, the optimal PLF configuration is achieved by inserting two C_x type capacitors between Lines 1–2 and 1–3.

This example is depicted and shown in Figure 5.4.

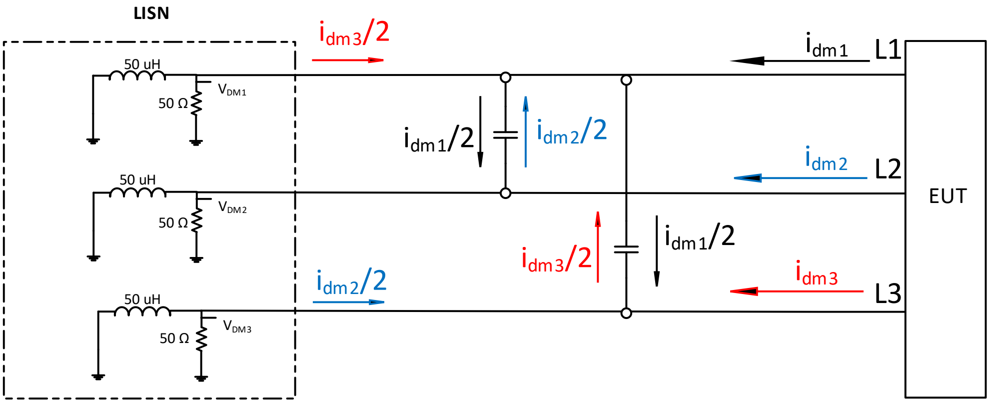


Figure 5.4: Representation of the differential mode currents flowing in a three-phase system after applying two $C_x$capacitors. DM1 (black), DM2 (blue), and DM3 (red).

For the sake of simplicity, k and h are assumed to be ½ for each current. This assumption might not be true for all cases, but can be used for this example. Only DM currents are depicted, since C_x capacitors have no influence on CM current.

Figure 5.4 shows how a predominant DM noise (V_{DM1}), generated by i_{DM1} flowing through the 50 Ω resistor of the LISN, can be filtered using only two C_x capacitors. It relies on the fact that the current i_{DM1} recloses though the low impedance path offered by the two capacitors and does not flow towards the LISN. Furthermore, as depicted in Figure 5.4, i_{DM2} and i_{DM3} partially reclose though the low impedance path offered by the capacitors, hence a partial reduction in V_{DM2} and V_{DM3} is also achieved. Throughout this chapter, both simulations and measurements results will sustain this statement.

Based on this analysis, it is clear that in order to effectively filter out a single DM noise, only two C_x capacitors are required. The use of any other PLF structure, such as those composed of three C_x capacitors or other components, would only contribute to increase the size and cost of the PLF unnecessarily.

Such a PLF structure implies that:

$$i_{DM1} + i_{DM2} + i_{DM3} \neq 0 \tag{5.1}$$

This means that at the point ‘O’ shown in Figure 5.3, the sum of the DM current differs from zero. Hence, part of the DM current will be transformed into a CM current, thus contributing to increasing the overall CM voltage. This energy exchange between modes must be evaluated when implementing such a PLF structure to make sure that the new CM voltage does not cause incompliance. An example will be presented in this chapter.

Furthermore, if there is also an imbalance in one of the phase impedances, the CM noise will distribute unevenly among the phases; therefore, part of the CM noise will be transferred to DM noise, this phenomenon is the so-called mixed-mode (MM) noise [93-104]. The same consideration is also valid for DM noise distribution among the phases but is not further analyzed.

5.2.3. General Considerations for CE Testing for Three-Phase EUTs and Consequences in PLF Design

Generally, the EMI receivers available on the market only present one input RF channel. Furthermore, three-phase LISNs are also designed to allow the measurement of only one phase at a time, using an internal switch to commutate to the phase of interest. Therefore, the CE of a three-phase EUT must be performed by at least three subsequent measurements. An example is shown in Figure 5.5.

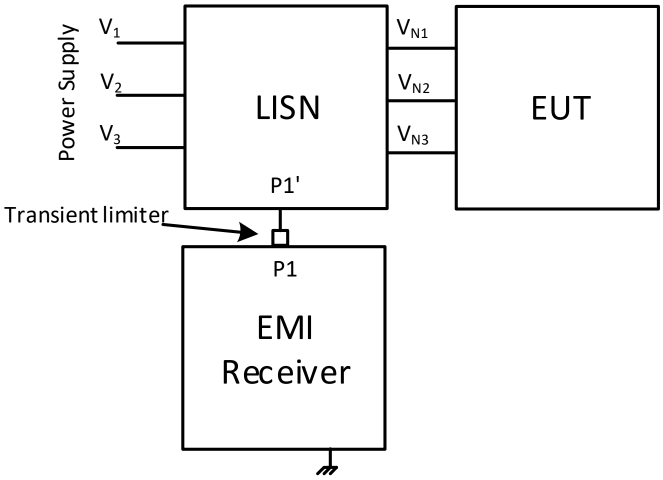


Figure 5.5: Standard CE set-up for a three-phase EUT.

With the set-up illustrated above, it is not possible to measure the modal noises because only one phase is measured at a time. Hence, designing an optimal PLF becomes a very difficult task because it can be carried out only by following a tedious trial-and-error procedure [89-100].

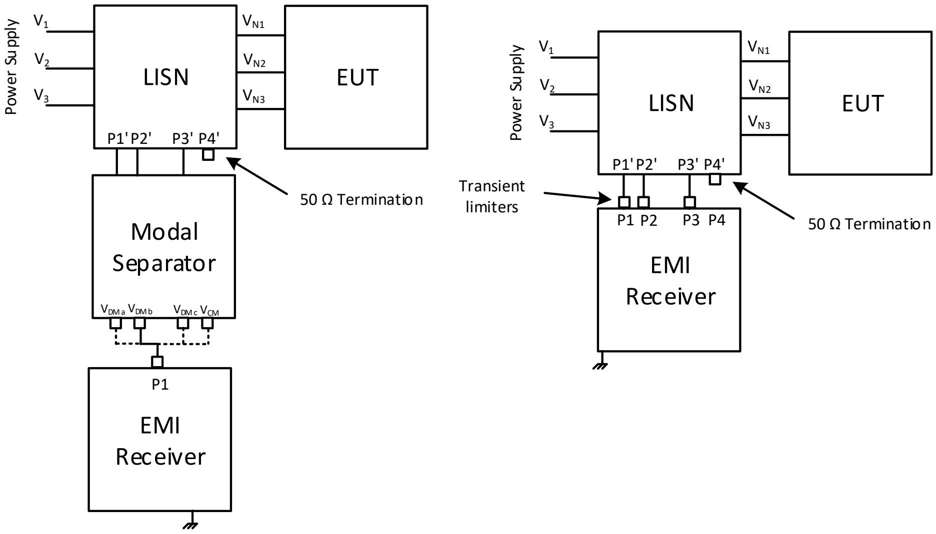
To overcome this limitation, two main requirements are needed:

1) Having at disposal a LISN featuring independent RF outputs for each phase.

2) Having at disposal equipment able to extract the modal noises.

To satisfy the recent increasing market demand for requirement (1), certain LISN manufacturers have begun to offer the possibility to customize a three-phase LISN that features four independent RF outputs instead of only one.

As for requirement (2), two solutions are possible. The first one would be to use a modal separator, as shown in Figure 5.6(a). In the literature, it is possible to find several examples of these architectures with detailed analysis on their advantages and disadvantages [88-99].
The second possibility is to have at available a device capable of measuring all channels simultaneously and extracting the information of modal noises, as shown in Figure 5.6(b).
The measurements shown in Section 5.4 are based on this second approach.



(a) (b)

Figure 5.6: (a) Set-up using a modal separator; (b) set-up using a four-channel EMI receiver.

When an external separator is used, the following drawbacks must be considered:

- Extra equipment must be bought or developed [88].
- Modal noises cannot be measured simultaneously. This makes the identification of the predominant mode or sporadic interference detection very difficult, especially when a pulsed interference is measured.

- Additional cables and the modal separator itself can behave as an antenna and couple undesired signals into the measurements and add uncertainties into the measurement chain.
- Modal coupling depends on the technology and can change along with the frequency [88,115-119].
- Special care must be taken to avoid impedance mismatches, since reflections can amplify the modal conversion.

The benefits achieved with the set-up illustrated in Figure 5.6(b), composed of an EMI receiver which could measure all the channels simultaneously, are listed hereafter:

- No external modal separator is needed. Whenever an external device is added into the measurement set-up, the possibility of impedance mismatches increases. For example, the impedance of the modal separator placed between the LISN RF outputs, and the receiver RF inputs might vary unknowingly along with the frequency and contribute at providing wrong measurement results [50].
- CM and DM noises can be measured and analyzed simultaneously. A four-channel EMI receiver equipped with a high-speed ADC converts the measured signals in the digital domain. Hence, the modal noises can be evaluated by computing Equations (5.4) and (5.5) without external analog devices.

5.3 PLF Design

The modal noises generated by a EUT, when propagation paths are symmetrical and time invariant, should be decoupled. This means that an equivalent CM source generates only CM noise, and the same is also valid for the DM noise, respectively [94].

Again, this is well-studied for single-phase systems, but there is still a gap for three-phase systems. Hence, it is not possible to correctly understand and determine the effect that each PLF component has on CM or DM reduction.

This section shows how different voltage configurations can be used to inject CM or DM noise only into the system. This is to evaluate the response, under known conditions, of the PLF components under study.

The results obtained are important to understand how components react when different noises are generated by the EUT. Furthermore, by following the approach and methodology proposed, simulations considering parasitic parameters and/or multiple components can also be carried out. A detailed analysis of the basic PLF configurations and modal noise analysis is presented hereafter.

5.3.1. Common Mode Noise Generation

According to the modal definition (Equations (5.4) and (5.5)), in order to introduce only a CM noise source into the system, the relationship shown in Equation (5.7) must be respected; namely, the amplitude and phase displacement of the three vectors must be the same.

$$\underline{V}_{1n} = \underline{V}_{2n} = \underline{V}_{3n} \tag{5.7}$$

In this case, it holds that:

$$V_{CM} = \frac{V_1 + V_2 + V_3}{3} = \frac{3 * V_i}{3} = V_i \neq 0 \tag{5.8}$$

$$V_{DM,i} = V_i - V_{CM} = V_i - \left(\frac{V_1 + V_2 + V_3}{3}\right) = V_i - \left(\frac{3 * V_i}{3}\right) = 0; \; i = 1, 2, 3 \tag{5.9}$$

Thus, only a CM noise is injected in the system.

5.3.2. Differential Mode Noise Generation

According to the modal definition (Equations (5.4) and (5.5)), in order to introduce a DM noise source into the system the relationship shown in Equation (5.10) must be respected; namely, the vectors must have the same amplitude and, for example, a phase displacement of 120° each.

$$\underline{V}_{1n} + \underline{V}_{2n} + \underline{V}_{3n} = 0 \tag{5.10}$$

In this case, it holds that:

$$V_{CM} = \frac{V_1 + V_2 + V_3}{3} = 0 \tag{5.11}$$

$$V_{DM,i} = V_i - V_{CM} = V_i - \left(\frac{V_1 + V_2 + V_3}{3}\right) = V_i \neq 0; \quad i = 1,2,3 \tag{5.12}$$

5.3.3. Differential and Common Mode Noise

In order to inject a combination of DM and CM noise, it is simply necessary to set a phase displacement which differs from the conditions indicated in the two subsections above.

5.3.4. Accurate Estimation of the IL of a PLF

The IL, independently of the noise source present in the system, can be generally computed by solving the following equations:

$$IL|_{dB}^{DMi} = 20 \times log_{10}\left(\frac{V_{DM}^{ref}}{V_{DM}}\right) = 20 \times log_{10}\left(\frac{V_i^{ref} - V_{CM}^{ref}}{V_i - V_{CM}}\right)$$

$$= 20 \times log_{10}\left(\frac{V_{\mathrm{i}}^{ref} - \left(\frac{V_1^{ref} + V_2^{ref} + V_3^{ref}}{3}\right)}{V_1 - \left(\frac{V_1 + V_2 + V_3}{3}\right)}\right);\ \mathrm{i}=1,2,3 \qquad (5.13)$$

$$IL|_{dB}^{CM} = 20 \times log_{10}\left(\frac{V_{CM}^{ref}}{V_{CM}}\right) = 20 \times log_{10}\left(\frac{\frac{V_1^{ref} + V_2^{ref} + V_3^{ref}}{3}}{\frac{V_1 + V_2 + V_3}{3}}\right) \qquad (5.14)$$

where the voltages V_i^{ref} (i = 1, 2, 3) are the voltages at terminals 1, 2, and 3 of the LISN, respectively, when no PLF is connected, as seen in Figure 5.7. In contrast, the voltages V_i (i = 1, 2, 3) are the voltages Terminals 1, 2, and 3 of the LISN, respectively, when the signal is filtered, as seen in Figure 5.8.

Both measurement points are placed between the 50 Ω resistor and the 0.25 µF capacitor

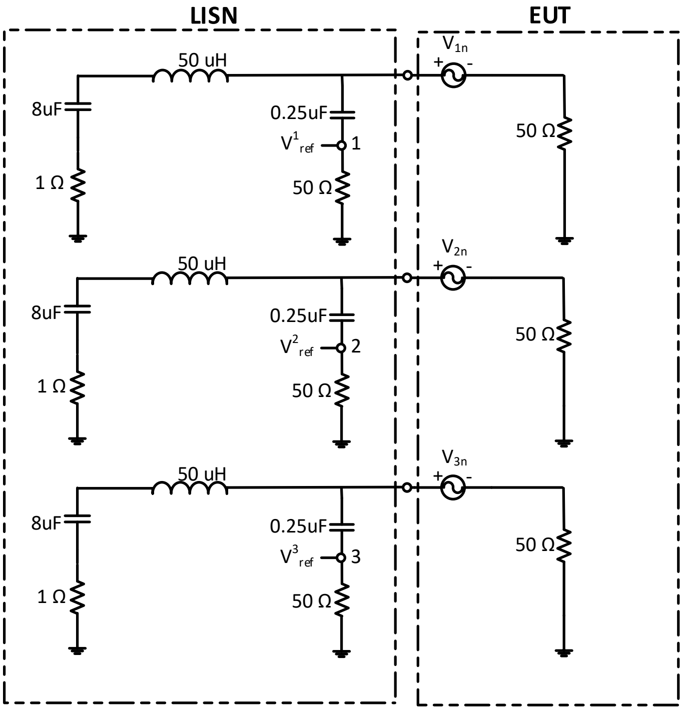


Figure 5.7. Equivalent circuit of the EUT connected to the equivalent circuit of a three-phase LISN.

Figure 5.8 illustrates the equivalent circuit of the EUT connected to the equivalent circuit of a LISN though a general PLF which will be introduced to perform the required evaluations.

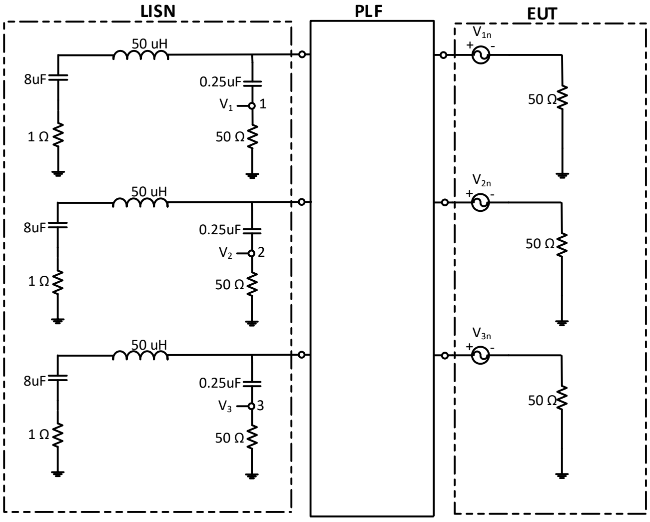


Figure 5.8: Equivalent circuit of the EUT connected to the equivalent circuit of a three-phase LISN with a PLF.

In this case, a 50 Ω load is used to represent the impedance of the EUT, while the impedance of the LISN is represented by its internal circuit.

Three voltage noise sources, V_{1n}, V_{2n}, and V_{3n}, are used to provide a fixed amplitude signal at all frequencies of interest, which will be used to compute the attenuation of the PLF as described in the following subsections.

5.3.5. Models Validation

In this section, the modals proposed are validated.

5.3.5.1. IL's Evaluation for C$_x$ Capacitors

Figure 5.9 shows X-type capacitors (C_x) connected between a three-phase LISN and a three-phase EUT.

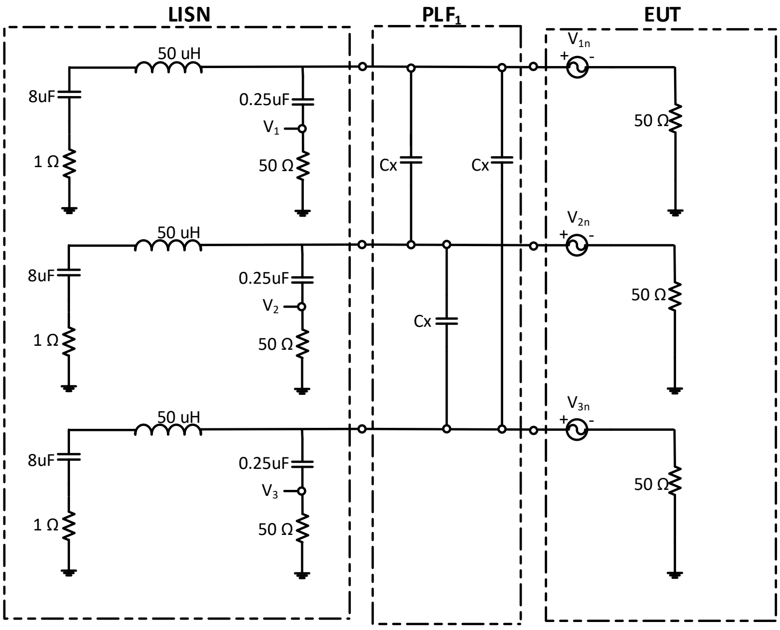


Figure 5.9: PLF connected between the three-phase LISN and three EUTs consisting of X-type capacitors.

The value of each C_x chosen to carry out the simulation is 0.10 µF. Figure 5.10 shows the attenuation introduced by PLF1.

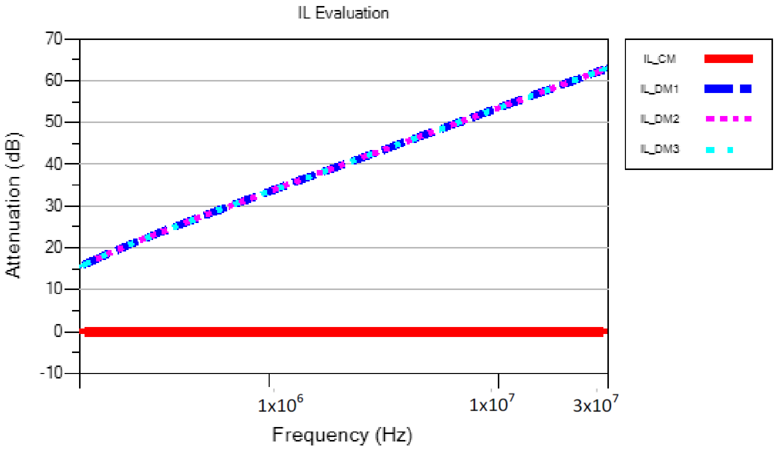


Figure 5.10: IL of a PLF₂ composed of a three C_x capacitors.

As shown in Figure 5.10, C_x capacitors do not reduce the CM noise and only affect the DM noise.

5.3.5.2. IL's Evaluation for CMC

Figure 5.11 shows a CMC connected between the three-phase LISN and the EUT.

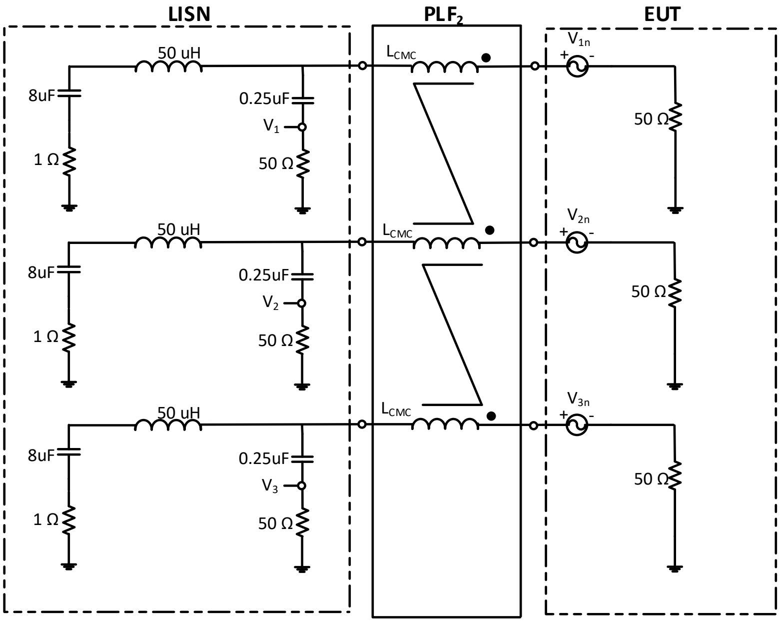


Figure 5.11: PLF connected between the three-phase LISN and the EUT consisting of a three-phase CMC.

The value of the three-phase CMC selected to carry out this simulation is 1.2 mH. Figure 5.12 shows the attenuation introduced by PLF2.

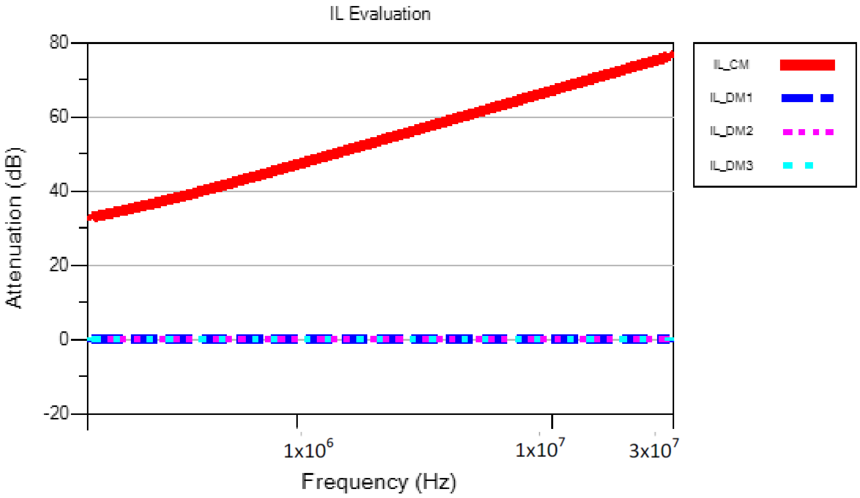


Figure 5.12: IL of a PLF2 composed of a three-phase CMC.

As shown in Figure 5.12, a CMC ideally does not reduce the DM noise and only affects the CM noise.

5.3.5.3. IL's Evaluation for C_Y Capacitors

Figure 5.13 shows Y-type capacitors (C_y) connected between the three-phase LISN and the EUT.

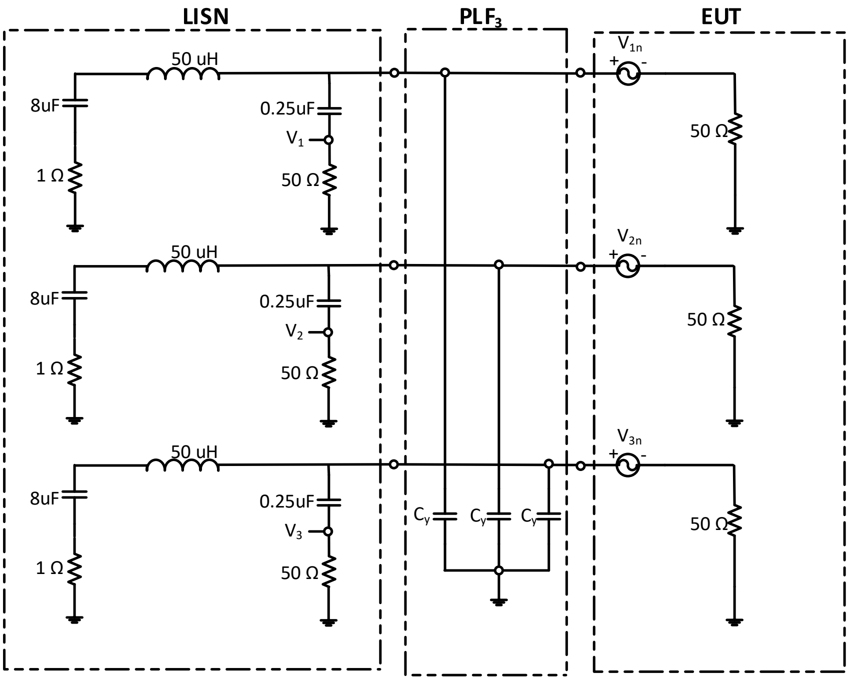


Figure 5.13. PLF connected between the three-phase LISN and the EUT consisting of Y-type capacitors.

The value of each C_y capacitor used to carry out this simulation is 0.05 μF.

Figure 5.14 shows the attenuation introduced by PLF3.

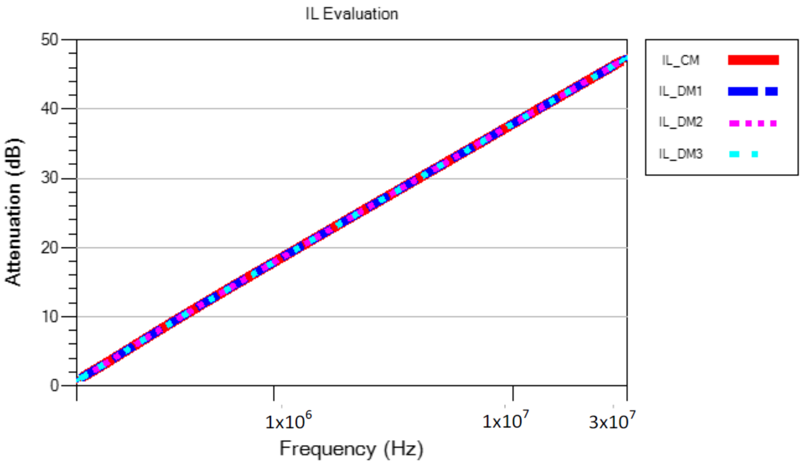


Figure 5.14: IL of a PLF3 composed of three C_y capacitors.

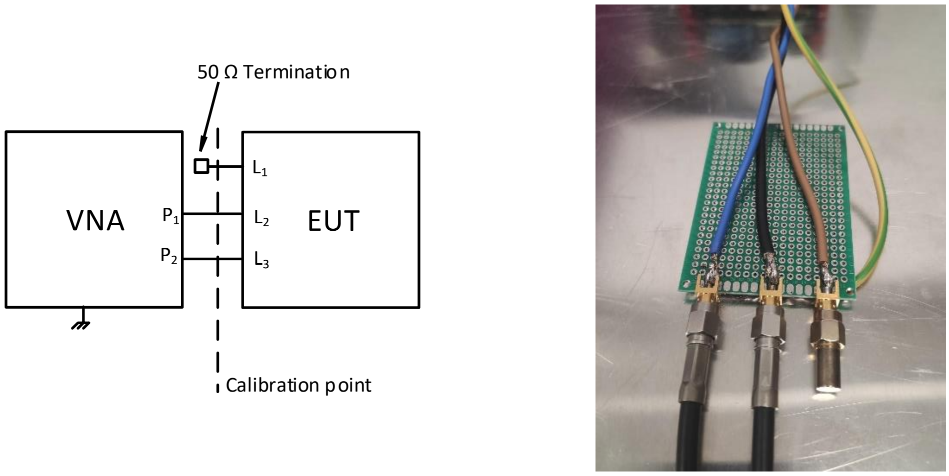
As shown in Figure 5.14, C_y capacitors attenuate both CM and DM noise.

According to the standard IEC 60990 and depending on the application, the maximum leakage current is limited. Thus, extreme care must be taken when using these types of capacitors, since their practical implementation could be strongly limited.

5.3.6. EUT Characterization—S-Parameter Measurements

It is known that to design an optimal PLF, the input impedance of the EUT must be known [17-22]. To this end, the S-parameters of the EUT have been measured. Since only a two-port VNA was available at the laboratory, three subsequent measurements had to be performed (Port 1–2, Port 2–3, and Port 1–3, respectively) and combined together in order to obtain a 3 × 3 matrix characterizing the EUT, as shown in Figure 5.15.

Figure 5.15 (a) and (b) show the set-up implemented to measure S-parameters using a two-port VNA and a 50 Ω termination for the remaining line which could not be connected to the VNA.



(a) (b)

Figure 5.15. (a) S-parameter measurement set-up; (b) Actual set-up with 50 Ω termination.

Then, a software has been used to build up a single 3x3 matrix starting from the three 2x2 matrixes obtained by each VNA measurement.

$$S_{[1,2]}=\begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix}$$

$$S_{[2,3]}=\begin{pmatrix} S_{22} & S_{23} \\ S_{32} & S_{33} \end{pmatrix} \quad \Longrightarrow \quad S_{[3x3]}=\begin{pmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{pmatrix}$$

$$S_{[1,3]}=\begin{pmatrix} S_{11} & S_{13} \\ S_{31} & S_{33} \end{pmatrix}$$

The approach shown is general and could be extended to a n-port EUT.

$$S_{[i,j]}=\begin{pmatrix} S_{ii} & S_{i,j} \\ S_{j,i} & S_{j,j} \end{pmatrix}$$

$$\vdots \qquad\qquad \Longrightarrow \qquad\qquad S_{[i,z]}=\begin{bmatrix} S_{ii} & \cdots & S_{iz} \\ \vdots & \ddots & \vdots \\ S_{zi} & \cdots & S_{zz} \end{bmatrix}$$

$$S_{[v,z]}=\begin{pmatrix} S_{v,v} & S_{v,z} \\ S_{z,v} & S_{z,z} \end{pmatrix}$$

5.4 Experimental Validation

The methodology followed to design an optimal PLF of a three-phase EUT is described hereafter:

1. Measurement of the EUT's S-parameters.
2. Measurement of the conducted emissions and their modal decompositions. This information is needed to determine the attenuation required to mitigate each mode under a certain limit.
3. S-parameters are introduced as a three-port black box in a circuit simulator.
4. Implementation of the same circuit by adding the PLF.
5. Simulations in frequency domain to obtain the voltage amplitude at the measurement ports of the LISN, that is: V_1^{ref} , V_2^{ref}, V_3^{ref}, V_1 , V_2, and V_3.
6. The CM/DM attenuation is computed using Equations (5.13) and (5.14), respectively.
7. The determination of the optimal values for each PLF component is conducted using iterative simulations and by selecting the closest available commercial value found. Of course, this methodology could be implemented by means of different optimization techniques.

5.4.1. CE Measurements

In this subsection, the CE and modal noise measurements obtained are presented.

The set-up for CE measurement described in Section 5.2 and illustrated in Figure 5.6(b) is shown in Figure 5.16.

In this case study, the EUT chosen is a three-phase inverter used for motor control.

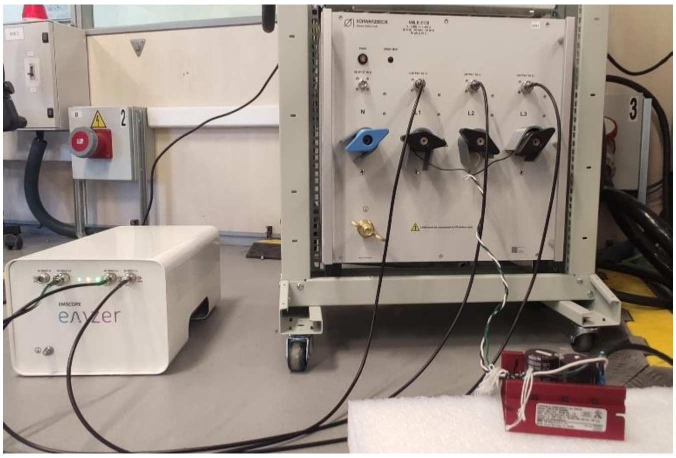


Figure 5.16: CE measurement set-up: a four-port EMI receiver (left side), and a four-port LISN (right side, back), with the EUT (right side, front).

Figure 5.17 shows the CE measurement registered at the line terminals of the LISN using the quasi-peak (QPK) detector.

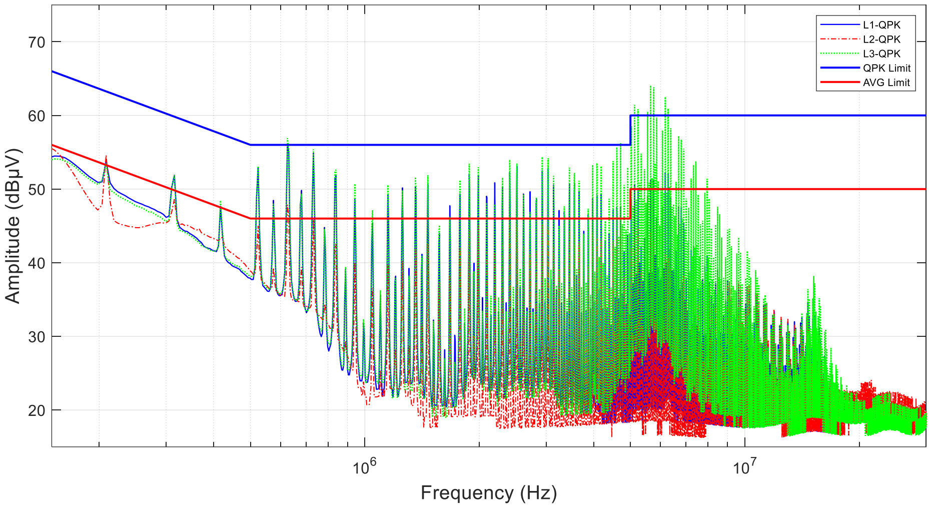


Figure 5.17. CE measurement of a three-phase EUT with a QPK detector.

It can be seen that at 630 kHz and at 5 MHz, the registered measurement is above the CISPR 32 class B limit [2]. It is clear that the EUT does not comply with the standard limitations and a PLF must be introduced. A minimum mitigation of 20 dB is required to meet the standard limits and make sure that a safe margin is left to compensate possible variations due to slight differences in the set-up and measurement uncertainties when performing the final tests at a third-party EMC lab.

Figure 5.18 shows the modal decomposition measured with the QPK detector of the CE noise generated by the EUT.

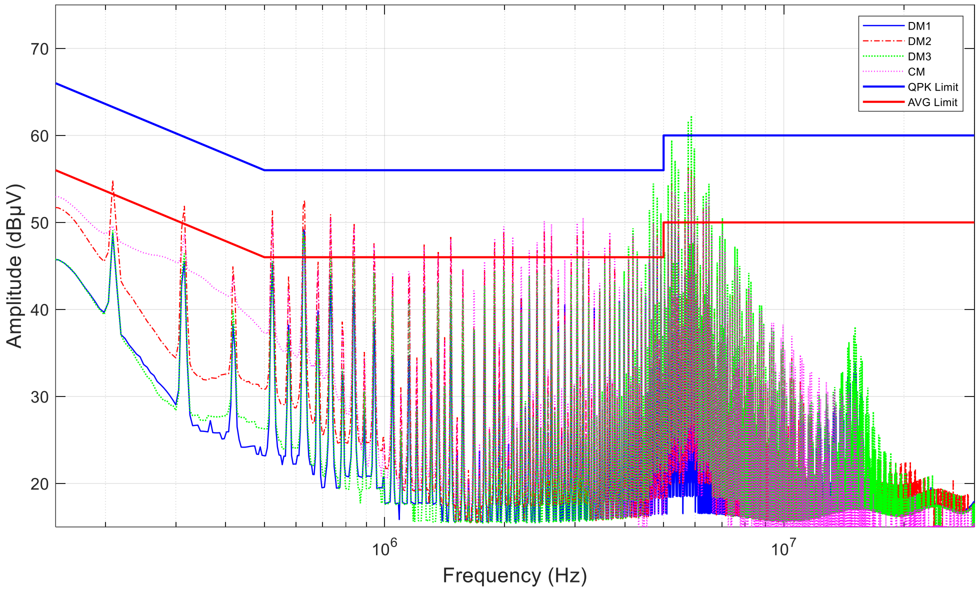


Figure 5.18. Modal noise measurement of a three-phase EUT measured with a QPK detector.

As can be seen Figure 5.18, thanks to the modal decomposition, it is possible to determine that DM3 is the dominant mode. This, along with the input impedance of the EUT, is an essential information to design an optimal three phase PLF. Since the other mode noises are below the limit, they do not require special mitigation.

5.4.2. PLF Design Methodology

In this section, an accurate evaluation of the IL is proposed and then used to determine the optimal PLF for the EUT.

Again, with respect to EMC testing, the LISN, whose internal circuit is known, provides the impedance of the power line network (PLN). Thus, when the EUT impedance is also known, the real IL of any PLF can be evaluated.

Since the S-parameters of the EUT have been measured using the methodology explained in Section 5.3.6, the EUT impedance is known.

According to the explanation proposed in Section 5.2, it is clear that two C_x capacitors are the correct elements to completely filter the differential mode noise under analysis.

In this case study, since differential mode three (DM3) is above the permitted limit, two X-type capacitors are inserted between Lines 1–3 and 2–3 to reduce the CE. Furthermore, a reduction in DM1 and DM2 will also be achieved.

The value of the C_x capacitors has been obtained by changing the values until the IL introduced achieved the desired attenuation for the case under study.

Figure 5.19 shows the PLF connected between the EUT and the LISN consisting of two 0.47 µF X-type capacitors placed between Lines 1–3 and 2–3 to mitigate the differential mode noise of interest.

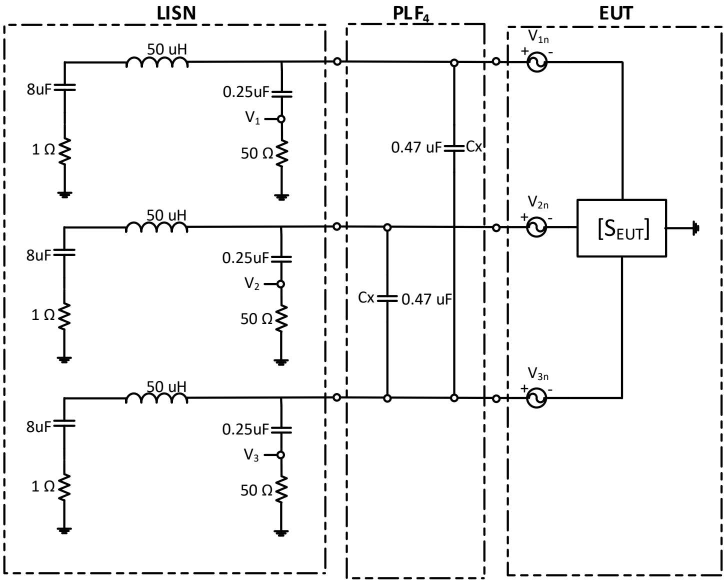


Figure 5.19. PLF connected between the EUT and the LISN consisting of two X-type capacitors placed between Lines 1–3 and 2–3.

Figure 5.20 shows the attenuation obtained for each modal noise.

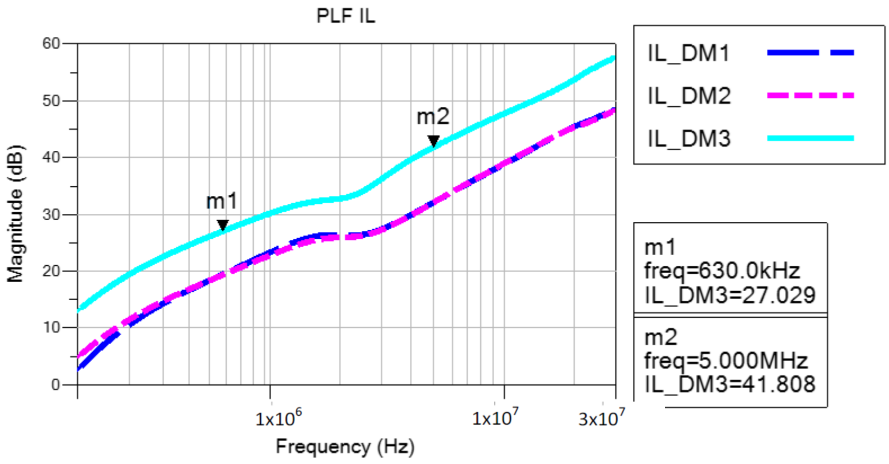


Figure 5.20: IL of PLF$_5$.

As can be seen, the reduction obtained at 630 kHz and 5 MHz is enough to make the product comply with the limit imposed by the relative EMC standard [2].

Figure 5.21 shows the DM1 recorded before and after applying PLF_5.

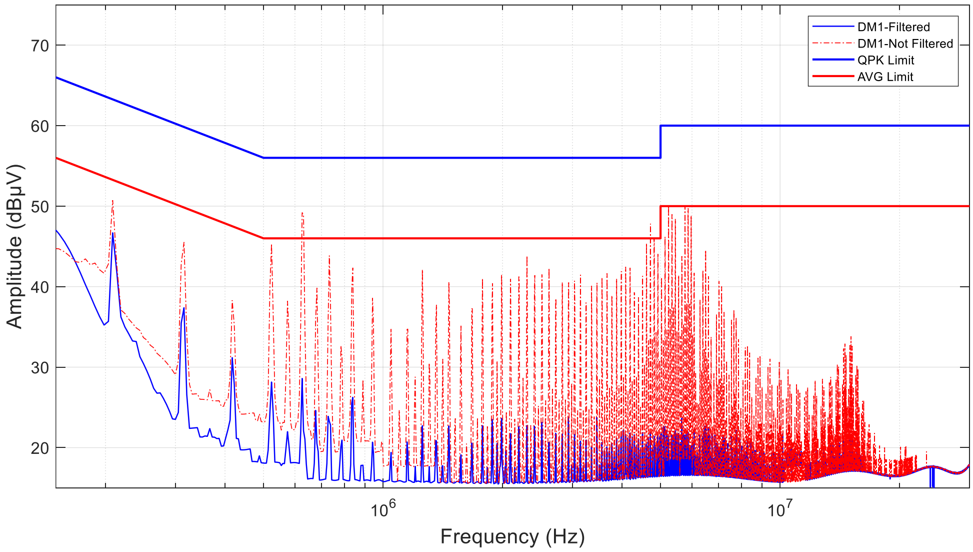


Figure 5.21: DM1 without PLF5 (red) vs. with PLF5 (blue).

As can be seen, reductions of 21 dB and 30 dB are achieved at 630 kHz and 5 MHz, respectively, as expected from the simulation results shown in Figure 5.20.

Figure 5.22 shows the DM2 recorded before and after applying PLF_5.

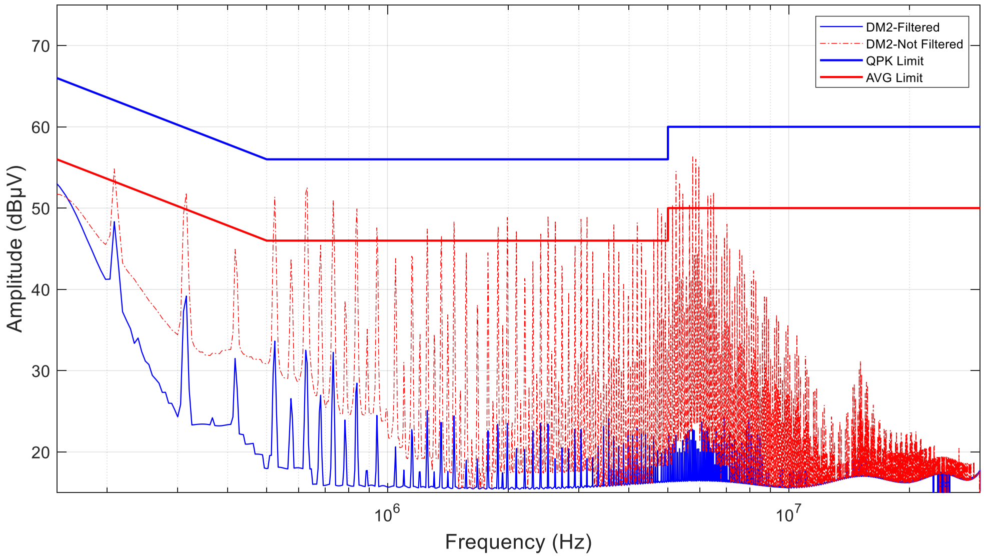


Figure 5.22. DM2 without PLF5 (red) vs. with PLF5 (blue).

As shown in Figure 5.22, the reductions of 21 dB and 29 dB achieved at 630 kHz and 5 MHz, respectively, are consistent with the estimated value obtained from the simulation results shown in Figure 5.20.

Figure 5.23 shows the DM3 recorded before and after applying PLF_5.

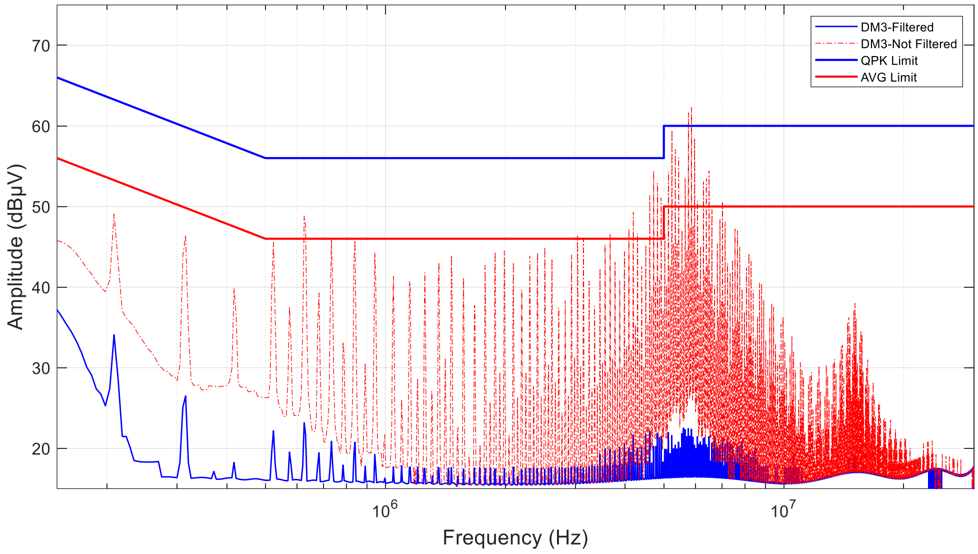


Figure 5.23. DM3 without PLF_5 (red) vs. with PLF_5 (blue).

As can be seen, the reductions of 26 dB and 38 dB achieved at 630 kHz and 5 MHz are exactly as expected from the simulation results shown in Figure 5.20.

Figure 5.24 shows the CMC recorded before and after applying PLF_5.

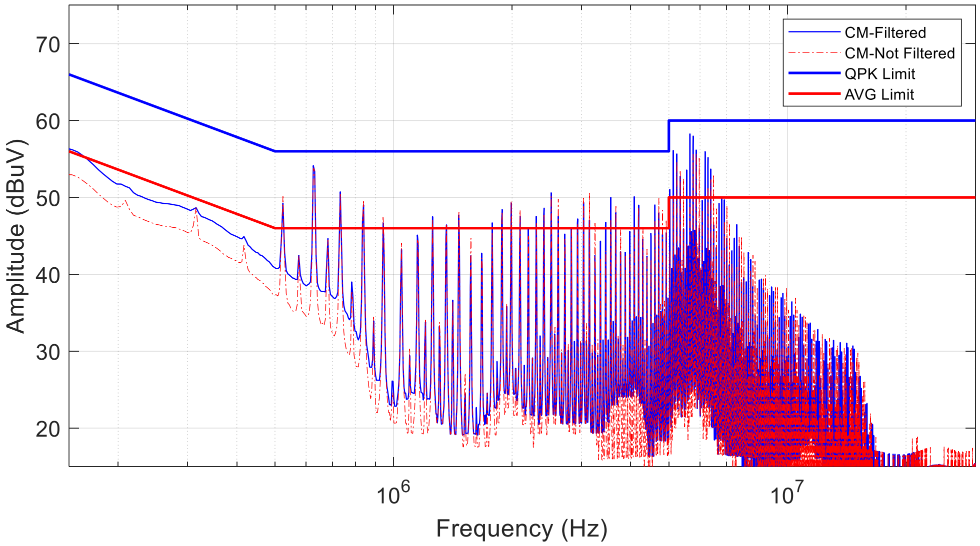


Figure 5.24. CM without PLF_5 (red) vs. with PLF_5 (blue).

Figure 5.24 confirms that C_x capacitors do not affect the CM noise, confirming the goodness of the simulation carried out in Section 5.3, Figure 5.10. The small deviations from the filtered and unfiltered measurements, which can be observed in Figure 5.24, are due to the modal exchange created by the imbalanced PLF structure implemented, as explained in Section 5.2.2. Furthermore, the different set-up created when the PLF is added (extra cables, different stray capacitances of the PCB board where the PLF is mounted, etc.) might affect the overall CM noise. Therefore, the results obtained provide evidence that to design an optimal PLF for three-phase EUTs to meet EMC standards, it is necessary to evaluate the modal noises and, only after that, design a PLF. In this particular case study, a filter composed of two C_x type capacitors was found to be the optimal configuration. Hence, every other component, for instance a C_x capacitor placed between Line 1–2 or a three phase CMC, would have been redundant, and only contributed to increase the size and cost of the PLF.

Most of the current research on this topic discusses modal decomposition; but, when designing a PLF, this information is not taken into account and only static and standardized PLF structures are implemented. Inevitably, this makes the PLF bigger and more expensive than it should be.

5.4.3. CE Measurements of a Three-Phase Charging Station

The considered EUT is a commercial 25 kW battery charger connected to the three-phase AC grid through a three-phase LISN rated 400A. The CE is measured with a receiver for measurements up to 110 MHz capable of directly providing the DM and CM spectra of the CE signal. To drive the battery charger, an electronic load emulates the battery pack. The measurements are performed considering the worst-case scenario, i.e. no load operations [100].

In this subsection, the CE generated by the EUT are shown and discussed. The set up for CE and modal measurement is shown in Figure 5.25.

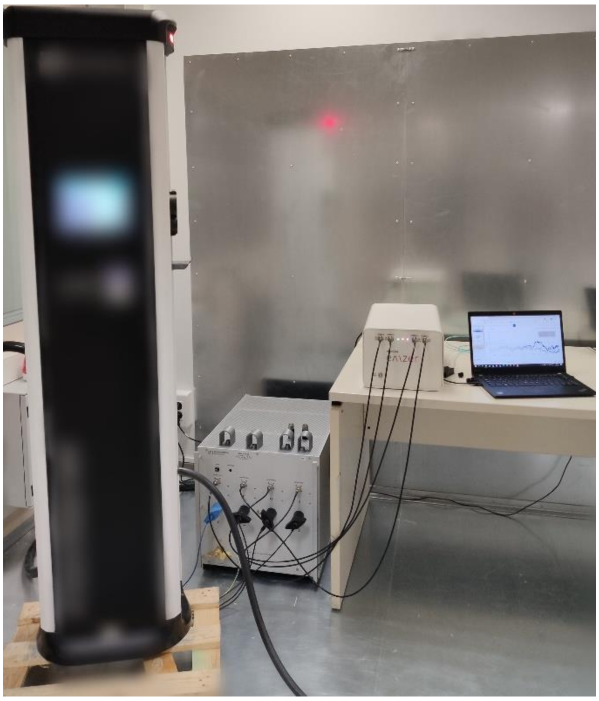


Figure 5.25: CE measurement setup - EUT (left side), an EMSCOPE-RX4 (a four-port EMI receiver, right side), and a four-port LISN (center).

The overall CE measurement recorded using the quasi-peak (QPK) detector for L1, L2, L3 and N is shown in Figure 5.26.

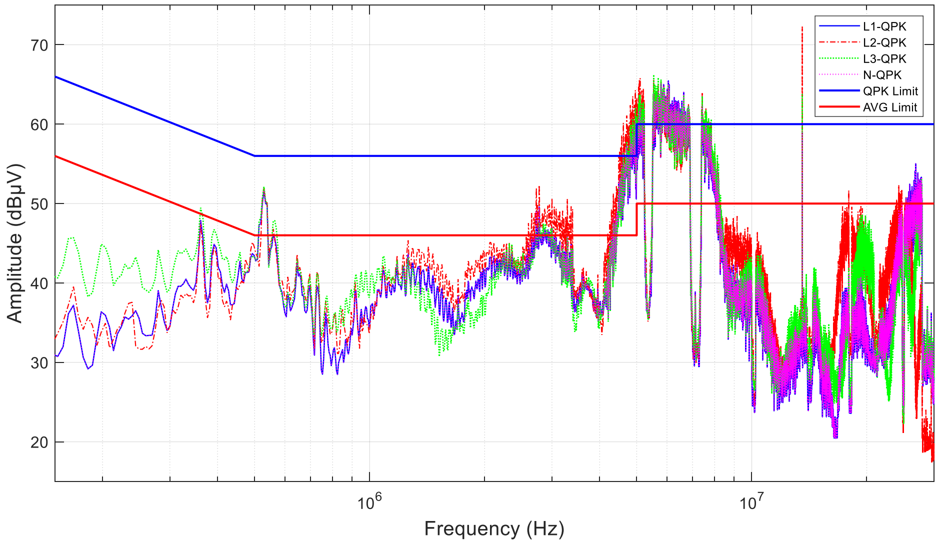


Figure 5.26: CE of EUT with QPK detector.

It is possible to see that from 4.2 MHz till 8 MHz, the recorded conducted emissions are above the permitted limit.

Hence, a PLF must be design and introduced to comply with the requirements set by the standard. At this stage, at list a 20 dB reduction is required. This value keeps into consideration possible differences in the setup which could lead to different measurements results when replicating the same test in an external EMC lab.

As it can be seen in Fig. 5.25, the three phase LISN used provides four RF channels available simultaneously. Since it is possible to access to all the phases simultaneously, fundamental condition to correctly evaluate the following equations, the modal noises can be computed.

$$V_{CM} = \frac{V_1 + V_2 + V_3 + V_\mathrm{n}}{4} \tag{5.15}$$

$$V_{DM,i} = V_i - V_{CM} = V_i - \left(\frac{V_1 + V_2 + V_3 + V_\mathrm{n}}{4}\right); \quad \text{i = 1,2,3} \tag{5.16}$$

Figure 5.27 shows the modal CE decomposition obtained with the QPK detector.

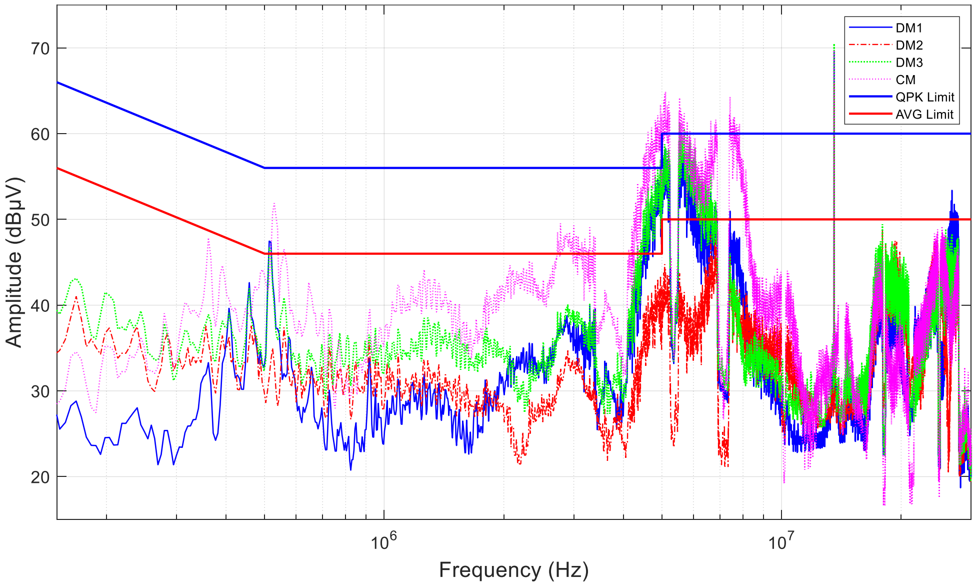


Figure 5.27: Modal noise measurement of a three phase EUT with QPK detector.

In this case study, it is possible to determine that the DM1, DM3 and CM are the dominant modes. This is an essential information to design an optimal PLF because each component of the PLF has the function to attenuate only specific modes. In order to design a PLF, the required attenuation must be calculated.

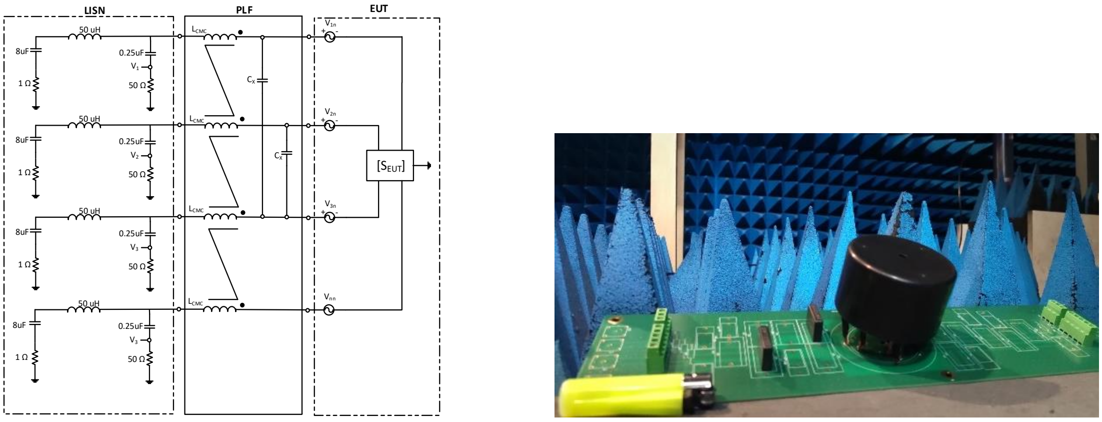
Since neutral conductor is present, the following formulas have to be used [100]:

$$IL|_{dB}^{DMi} = 20 \times log_{10}\left(\frac{V_{DM}^{ref}}{V_{DM}}\right) = 20 \times log_{10}\left(\frac{V_i^{ref}-V_{CM}^{ref}}{V_i-V_{CM}}\right) = 20x\ log_{10}\left(\frac{V_i^{ref}-(\frac{V_1^{ref}+V_2^{ref}+V_3^{ref}+V_n^{ref}}{4})}{V_i-(\frac{V_1+V_2+V_3+V_n}{4})}\right);\quad i=1,2,3; \tag{5.17}$$

$$IL|_{dB}^{CM} = 20 \times log_{10}\left(\frac{V_{ref}^{CM}}{V_{CM}}\right) = 20 \times log_{10}\left(\frac{\frac{V_1^{ref}+V_2^{ref}+V_3^{ref}+V_n^{ref}}{4}}{\frac{V_1+V_2+V_3+V_n}{4}}\right) \tag{5.18}$$

Where V_{CM}^{ref} / V_{DM}^{ref} and V_{CM}/ V_{dM} are evaluated by solving Eq.(5.15) and Eq.(5.16) while the PLF, as shown in Fig.5.8 is inserted or not, respectively.

The schematic of the PLF proposed is shown in Fig.5.28 (a), while the actual filter implemented is shown in Fig 5.28 (b).



(a) (b)

Figure 5.28: Schematic of the PLF proposed (a) and actual PLF (b)

The values of both C_x is set to 0.25 µF, while the three-phase CMC chosen presents an inductance of 0.7mH/phase and 25 A/phase. This CMC (a RD7147-25-0M7 from Schaffner) is a very peculiar one since it features 4 coils instead of 3, also to contemplate the neutral conductor.

Figure 5.29 shows the IL provided by the PLF.

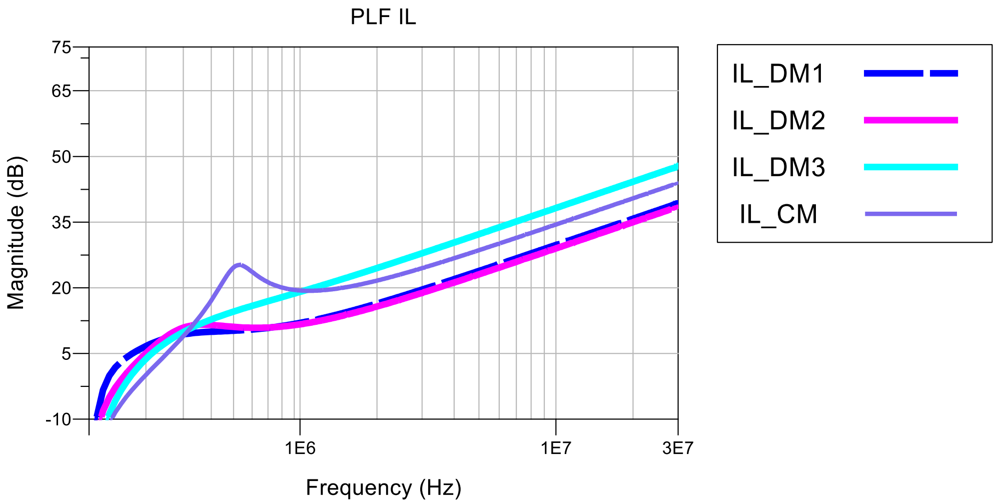


Figure 5.29: IL of the PLF proposed

The modal noises recorded after applying the PLF are shown in Figure 5.30.

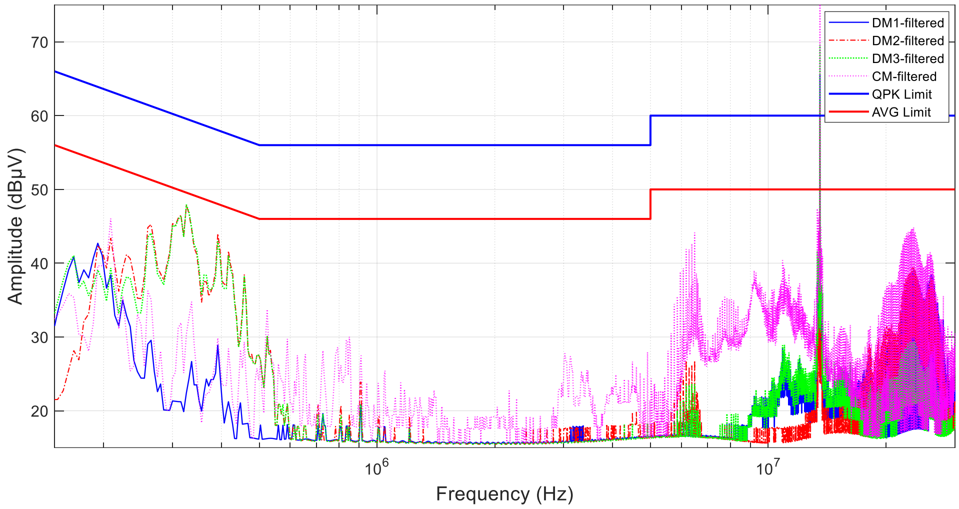


Figure 5.30: Modal noises recorded after applying the PLF

The reduction obtained for all CE modal noises shows a good agreement with the simulated IL shown in Fig. 5.29.

The CE recorded after applying the filter are shown here:

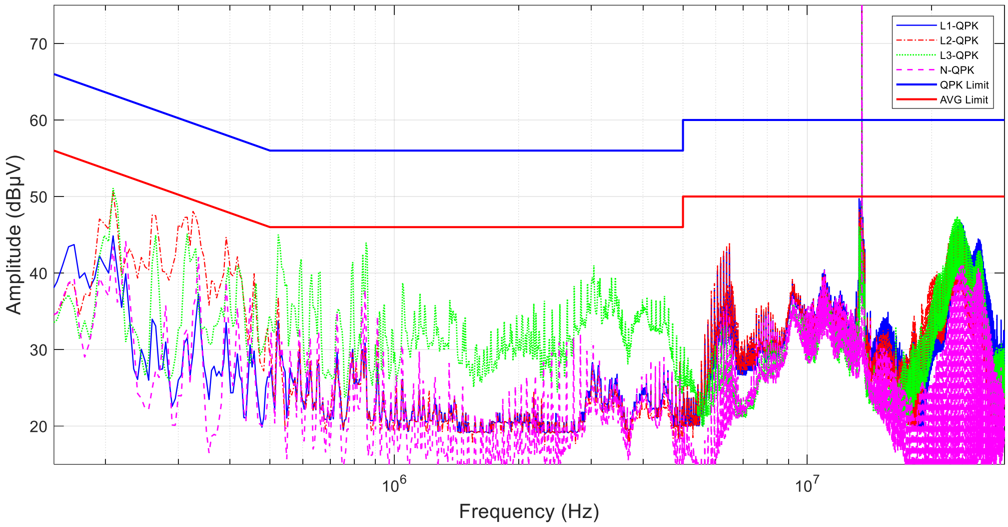


Figure 5.31: CE noise recorded after applying the PLF (QPK detector)

As it can be seen, the product now complies with the relative EMC standard. Note: the RFID signal appearing at 13.58 MHz above the limitation is allowed by the standard as it is a wanted/desired signal and classifies as an exception according to the reference EMC standards [1-3].

5.5 Conclusions

In this chapter, a rigorous methodology for optimal three-phase PLF design is proposed and validated. This study offers an in-depth examination of the modal noises present in three phase systems, defined through both mathematical expressions and graphical representations. Additionally, this research also outlines the essential testing equipment required to perform these measurements efficiently.

Since each component present in the PLF attenuate either common or differential mode noise, a detailed knowledge on which noise is being generated by the EUT is fundamental to achieve an optimal PLF design. For this, a procedure to evaluate how different PLF components behave when subjected to either common or differential mode noises is validated both from a mathematical and experimental point of view. Then, after having defined the PLF's components behavior, a methodology to design an optimal PLF relying on accurate IL estimations and modal CE measurements is proposed and validated.

By using a circuit simulator which contains the measured S parameters of a three phase EUT and by measuring its modal CE, it was possible to derive the optimal PLF configuration relying on real

IL values. The proposed structures differ from the standard ones used in commercial PLFs, which would have at least implemented one CMC and three $\mathrm{C_x}$-type capacitors, drastically increasing the number of components implemented in the PLF.

CHAPTER 6

6 Conclusions of the work

This section provides a summary of the work carried out, and how the objectives proposed for this research have been achieved.

1- The first proposed objective was to carry out an extended review, analysis, and characterization of EMC receivers. This is, not only to understand the direct impact on conducted emissions measurements, but also to determine how the measurement recorded using both architectures can directly or indirectly affect the power line filter design. To this end:
    a. A comprehensive comparison between analog receivers and FFT receivers has been carried out highlighting the advantages and disadvantages of each architecture.
    b. Conducted and modal emissions have been measured with both receivers. An exhaustive discussion of the results obtained and their implication for optimal PLF design has been presented and discussed.

2- The second objective was to propose a solution to characterize and model the uncertainty of a measurement equipment. This work presented:
    a. An exhaustive overview of the principles lying below measurement uncertainty evaluation.
    b. A new approach which can be used to drastically reduce the computational time needed to evaluate the uncertainty of a general measurement chain.
    c. A methodology to evaluate the influence that each discrete component has on the measurand and how to reduce the overall uncertainty by only acting on specific components, also by considering the influence added by external factors.

3- The third objective was to propose a solution and a reliable methodology to design an optimal PLF for single phase equipment. To this end, a methodology able to completely model the power line filters and the single-phase electric device under consideration has been developed throughout Chapter 4. In detail:
    a. Different EUTs, along with their parasitic components, have been modeled by means of S parameters, results have been obtained and validated both by simulations and real measurements.

    b. Conducted and modal emissions have been measured and the optimal PLF has been designed relying on accurate IL estimations, drastically reducing its size, cost and the time required for such design.

4- The fourth objective was to propose a solution and a reliable methodology to design an optimal PLF for three-phase equipment. To this end, a methodology to completely model the power line filter and the three-phase electric device under consideration has been developed throughout Chapter 5. In detail:
    a. A clear three-phase modal definition along with a review of the instrumentation capable of extract modal noises.
    b. A methodology to evaluate the behavior of any PLF component when the system is excited with either CM or DM noises, or a combination of both.
    c. A detailed PLF design methodology, based on an accurate IL estimation to reduce the CM and DM CE, has been proposed, experimentally tested, and validated in real case scenarios. The results show the drastic reductions, both in terms of cost and size, that have been achieved.

5- Finally, the last objective was to spread the results obtained throughout the scientific community. During this PhD, eight scientific papers have been published in relevant journals.

6.1 Future Work

The work proposed in this thesis leaves some open topics:

- The theory of modal decomposition and methodology for optimal PLF design is presented for both single and three phase EUTs. As explained throughout the thesis, modal noises in three-phase systems are still a topic of investigation, especially due to the recent increase of three-phase applications. A mode is defined as a solution of the multiconductor transmission lines (MTLs) equations, and a system composed by n transmissions lines plus a reference (that is, n + 1 conductors) has n solutions or modes [116]. The modes propagated in a three-line plus a reference system have been widely studied in the microwave field [120-123].

  Nevertheless, the EMC community is more common to talk about the CM and DM components for each conductor, independently if this is mathematically correct. This is the reason why the majority, if not all, of the recent papers available in literature, as well as the modal definitions proposed in Chapter 5, follow this guideline. Since the aim of this work is to propose new methodologies and approaches which can be adopted by the EMC community to design optimal PLF, which is the final objective of this investigation, different modal decompositions have not been analyzed.

Anyway, the modal theory and measurement systems presented here could be extended to improve the characterizations of three-phase electric devices and PLNs and evaluate how different modal definition might affect the PLF design.

- More research, investigation and real measurements of modal noise and their interaction when neutral conductor is present shall be carried out. This topic also can be further investigated along with a new modal definition.

- Complying with EMC standards does not necessary guarantee that power quality standards are fulfilled as well. No standards for the frequency range of 2–150 kHz are yet present, and there is no mention relative to the limits between issues related to power quality and EMC. This lack of standardization might create difficulties for a reliable operation of different types of equipment, either concerning the power network or the equipment itself. Further investigation on this matter shall be carried out in order to resolve open issues.

- The measurements presented in this work have been used to validate the different methodologies proposed in the frequency range between the 150 kHz and the 30 MHz. With adequate equipment, the frequency range could be extended to find the minimum and maximum frequencies where the characterization, prediction and design methodologies are still valid.

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