Alma Mater Studiorum - Università di Bologna

DOTTORATO DI RICERCA IN

INGEGNERIA ELETTRONICA, TELECOMUNICAZIONI E TECNOLOGIE DELL'INFORMAZIONE

Ciclo 36

Settore Concorsuale: 09/E3 - ELETTRONICA

Settore Scientifico Disciplinare: ING-INF/01 - ELETTRONICA

LONG-TERM RELIABILITY OF POWER GAN HEMTS

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Esame finale anno 2024

ALMA MATER STUDIORUM
UNIVERSITY OF BOLOGNA

PH.D. PROGRAMME
ELECTRONICS, TELECOMMUNICATIONS, AND
INFORMATION TECHNOLOGIES ENGINEERING
(ETIT)

SSD ING/INF 01

LONG-TERM RELIABILITY OF POWER GAN HEMTS

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XXXVI° CYCLE

A Paola,
colei che mi ha teso la mano e che,
allo stesso tempo,
si è distesa accanto a me.

Acknowledgments

My journey through the PhD program was an unforgettable experience. First of all, I would like to thank my supervisor Prof. Claudio Fiegna who gave me this opportunity and guided me with his knowledge, expertise and experience in the GaN power device world.

I also extend a very special thanks to Dr. Mauro Zanuccoli and Dr. Andrea Natale Tallarico for assisting me throughout these years. I appreciated their support, curiosity, work methodology and diverse perspectives. They have been a source of inspiration to improve myself.

I would like to thank Prof. Florin Udrea, Dr. Daniel Pope and Dr. Loizos Efthymiou who allowed me to perform my research at the University of Cambridge and Cambridge GaN Devices (CGD) company. Additionally, I would like to extend a very special thanks to Dr. Nirmana Perera and Dr. Kaspar Ledings for the enlightening scientific discussions. This experience boosted my personal and professional growth.

Desidero ringraziare con tutto il cuore la mia famiglia, che ha sempre avuto fiducia in me e nelle mie scelte. In particolare, vorrei ringraziare mio padre, da cui ho ereditato gli occhi con cui osservare la bellezza del mondo.

Un ringraziamento speciale a chi è stato al mio fianco e alle persone con le quali ho trascorso e condiviso esperienze significative durante questi anni.

Infine, desidero esprimere la mia sincera e profonda gratitudine a Paola, a cui dedico questo lavoro. È stata la persona che, più di chiunque altro, ha creduto in questo percorso, alimentando la mia perseveranza attraverso l'ascolto e l'incoraggiamento. Questa tesi è anche il frutto del suo amore.

Giuseppe

Abstract

The world is quickly changing, and the field of power electronics assumes a pivotal role in addressing the challenges posed by climate change, global warming, and energy management. The introduction of wide-bandgap semiconductors, particularly gallium nitride (GaN), in contrast to the traditional silicon technology, is leading to lightweight, compact and evermore efficient circuitry. However, GaN technology is not mature yet and still presents reliability issues which constrain its widespread adoption. Therefore, GaN reliability is a hotspot for the research community. Extensive efforts have been directed toward understanding the physical mechanisms underlying the performance and reliability of GaN power devices.

The goal of this thesis is to propose a novel in-circuit degradation analysis in order to evaluate the long-term reliability of GaN-based power devices accurately. The in-circuit setup is based on measure-stress-measure methodology where a high-speed synchronous buck converter ensures the stress while the measure is performed by means of full I-V characterizations. The switch from stress mode to characterization mode and vice versa is automatic thanks to electromechanical and solid-state relays controlled by external unit control. Because these relays are located in critical paths of the converter layout, the design has required a comprehensive study of electrical and thermal problems originated by the use of GaN technology. In addition, during the validation phase of the converter, electromagnetic-lumped-element circuit simulations are carried out to monitor the signal integrity and junction temperature of the devices under test. However, the core of this work is the in-circuit reliability analysis conducted with 80 V GaN HEMTs under several operating conditions of the converter in order to figure out the main stressors which

contribute to the device's degradation. Although this study has been performed on commercial GaN devices, therefore neither structure nor process information is available, making the physical interpretation difficult at the microscopic level of all results, it provides useful insights for GaN circuit designers.

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Chapter 1

Introduction

Modern society is heavily developed on the massive use of electronic systems for comfort and healthcare. From the well-known laptops to the recent electric cars, several inventions have taken place not only by a quest for progress but also by the need to face climate change or global warming problems [1]. At the heart of this technological evolution lies the field of power electronics that deals with the processing of electrical power using switching converters based on power electronic devices in order to efficiently save and store energy from renewable sources [2], supply electric vehicles, electronic devices, etc. Based on the target, the power applications require different voltage, current and operating frequency ratings, leading to the use of a power device rather than another one. Fig. 1.1 illustrates a complete picture of the power application range.

In the past, several researchers have predicted that, in future, wide bandgap (WBG) semiconductors, in particular Gallium Nitride (GaN) and Silicon Carbide (SiC) technologies, would have replaced the conventional Silicon (Si) in the power applications thanks to their promising characteristics [3]. As a matter of fact, the WBG device's properties provide a higher power density, switching frequency, operating voltage and efficiency [4; 5].

During these years, significant progress has been made in the development of WBG semiconductor technologies. Although ample room remains for research to improve their performance and robustness, these technologies

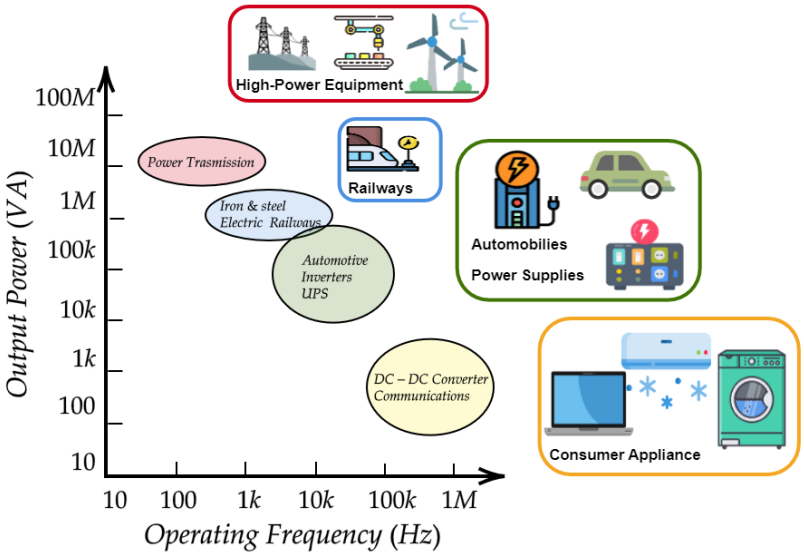

Figure 1.1: Power application range as a function of voltage, current and switching frequency ratings and induced power devices.

are already making their mark, with the first products entering the market. Indeed, in October 2021, Apple released the first GaN charger (140 W) which offered fast and efficient charging [6]. Therefore, the beginning of the WBG era in power electronics started, where innovation continues to shape the way we interact with and rely on electronic systems.

1.1 Why Gallium Nitride?

Currently, silicon is still the most widely used technology due to economic and reliability reasons. The maturity in the manufacturing process of silicon is very reliable, low in cost and, in addition, it is optimized to achieve the best performances. However, its scope is very limited in comparison with the WBG technologies as illustrated in Fig. 1.2. The SiC-based technology is adopted in high-power applications, while the GaN-based one is preferred in high-speed applications.

The motivations for this splitting are tied to the intrinsic properties of these two materials. A comparison of some of the most important electrical

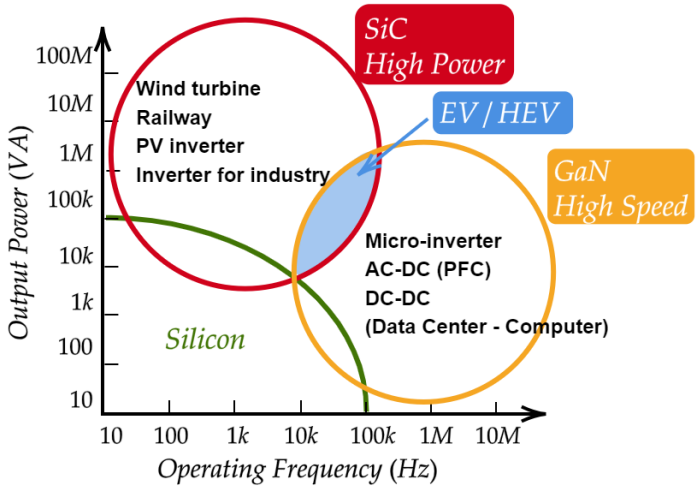

Figure 1.2: Power application range as a function of power devices technology.

properties is reported in Table 1.1 [7]. In most parameters, GaN is slightly superior to SiC and features five times better Baliga's figure of merit (BFoM) for power devices; with the thermal conductivity of GaN is lower than that of SiC.

The electrical properties affect the power device's performance since:

Parameter	Unit	Silicon	4H-SiC	GaN
Band-gap E_g	eV	1.12	3.26	3.39
Intrinsic Conc. n_i	cm^{-3}	$1.4 \cdot 10^{10}$	$8.2 \cdot 10^{-9}$	$1.9 \cdot 10^{-10}$
Critical Field E_c	MV/cm	0.23	2.2	3.3
Electron Mobility μ_n	$cm^2/(V \cdot s)$	1400	950	1500
Saturation Velocity ν_{sat}	$(10^7 cm/s)$	1.0	2.0	2.5
Permittivity ϵ_r		11.8	9.7	9.0
Thermal Cond. λ	$W/(cm \cdot K)$	1.5	3.8	1.3
BFoM: $\epsilon_0 \cdot \epsilon_r \cdot \mu_n \cdot E_C^3$	rel. to Si	1	500	2400

Table 1.1: Wide Band-gap Material Properties in Comparison with Silicon [7; 8]

- A wider bandgap E_g allows to have a low intrinsic carrier concentration n_i, at the same temperature. Because the gate leakage is linked to n_i which depends exponentially on E_g and temperature, WBG devices offer a smaller gate leakage current than silicon and operate at higher temperatures [9].

- A higher critical electrical field E_c implies that the device can sustain a higher voltage rating. The voltage limit achieved for Si-based power devices is 6.5 kV, while recently, 15 kV-based SiC devices have been demonstrated [10]. The maximum voltage limit is called breakdown voltage (BV) and if the operating voltage is higher than BV, avalanche breakdown is triggered by impact ionization and the device current significantly starts to increase. The impact ionization phenomenon, and consequently BV, depends on E_c. For the conventional power field-effect transistor, the BV is given by:

$$BV = \frac{1}{2} E_c W_D \tag{1.1}$$

  where E_c and W_D are the critical electric field and maximum depletion width of the drift region, respectively [11].

- The conductivity and the performance of power devices depends on electron mobility μ_n. Higher μ_n allows to reduction of one of the main parameters of a power device: ON-state resistance $R_{ON,sp}$. For the unipolar power device, the specific resistance (resistance per unit area) of the ideal drift region is given by:

$$R_{ON,sp} = \frac{W_D}{q \mu_n N_D} \tag{1.2}$$

  where W_D, q, μ_n and N_D are the maximum depletion width of the drift region, charge, electron mobility and doping concentration respectively [12].

- Higher saturation velocity of WBG materials implies a higher switch-

ing. A high switching speed can significantly reduce the transition time, which can increase the switching frequency to several times than Si and shrink inductor or capacitor size. Therefore, high-speed power converters switching around or above 1 MHz could become popular [13].

- Higher thermal conductivity allows more efficient heat conduction, increasing power density within the device. In addition, WBG devices have the potential to operate at higher temperatures than 175 °C temperature limit of Si [5].

- Baliga's figure of merit $\epsilon_0 \cdot \epsilon_r \cdot \mu_n \cdot E_C^3$ for power device is an indicator to evaluate the specific resistance of the ideal drift region $R_{ON,sp}$ related to the square of breakdown voltage BV. By solving Poisson equation and using equations 1.1 and 1.2, the following relationship is obtained:

$$\frac{R_{ON,sp}}{BV^2} = \frac{4}{\epsilon_0 \cdot \epsilon_r \cdot \mu_n \cdot E_C^3} \tag{1.3}$$

The dependence of the drift region resistance on the mobility and the much stronger (cubic) dependence of the ON-state resistance on the critical electric field for breakdown favour WBG semiconductors. Fig. 1.3 reports specific ON-resistance versus breakdown voltage for semiconductor devices. Generally, the channel mobility is lower in real devices due to several physical mechanisms which increase the ON-resistance. Instead, the theoretical limit is calculated by considering only the resistive contribution of the drift region.

By observing Fig. 1.3 it is possible to notice that each technology presents a different slope thanks to the intrinsic material properties. In addition, by increasing the breakdown voltage rating, Si-based devices show higher ON-resistance and hence higher conduction losses that limit the use of this technology. The figure illustrates some of the current state-of-the-art devices to compare the performance of each technology. GaN-based devices are still far from the GaN theoretical limit because the failure mechanisms are caused by the presence of defects due to a lack of maturity process [14].

Although both GaN and SiC are promising candidates for a variety of

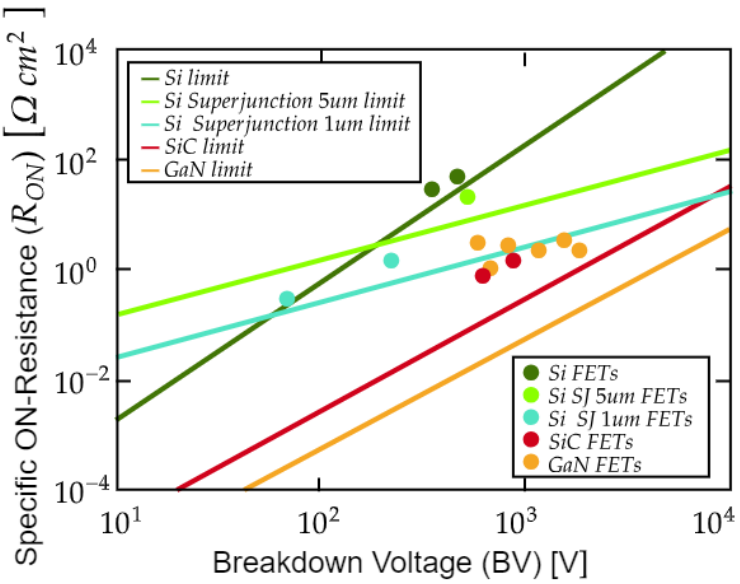

Figure 1.3: Specific ON-resistance versus breakdown voltage for Si, SiC, and GaN devices. Solid lines indicate the technology's theoretical limit, while the circles represent the corresponding power devices.

power applications thanks to their intrinsic material properties, GaN could be significantly cheaper than SiC as it can be grown on a Si substrate and its processing could be therefore made compatible with the one used in standard CMOS fabs. It is now evident that seamless integration and cost-effectiveness of GaN are the two key factors that push companies to invest in GaN technology [15].

1.2 GaN Market Outlook and Applications

The global gallium nitride semiconductor devices market size was valued at USD 2.17 billion in 2022 and is expected to further expand in the next years, surpassing around USD 26.83 billion by 2032 [16]. The projected compound annual growth rate is around 26 % from 2023 to 2032. Fig 1.4 reports the expected trend of the GaN market in the next years.

The growth factors are related to the possible adoption of GaN in power applications, as already-mentioned fast chargers are just one of the GaN-

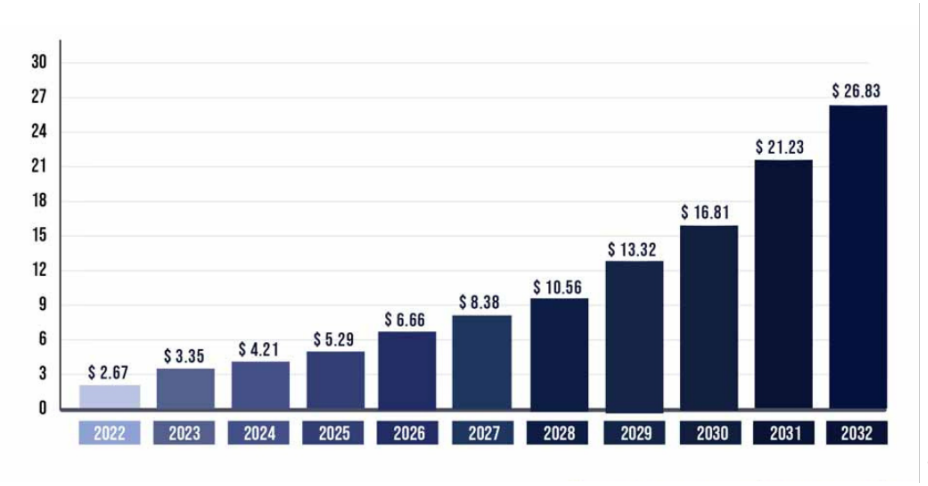

Figure 1.4: GaN semiconductor devices market size from 2022 to 2032 (USD billion) [16].

based applications. IoT devices demand, efficient and cost-effective components, the rise of electric vehicles in the market, and efficient renewable systems are other segments that are facilitating the GaN spread. In addition, this technology is favouring the development of many segments like information and communication technology, medical technology, aerospace and defence.

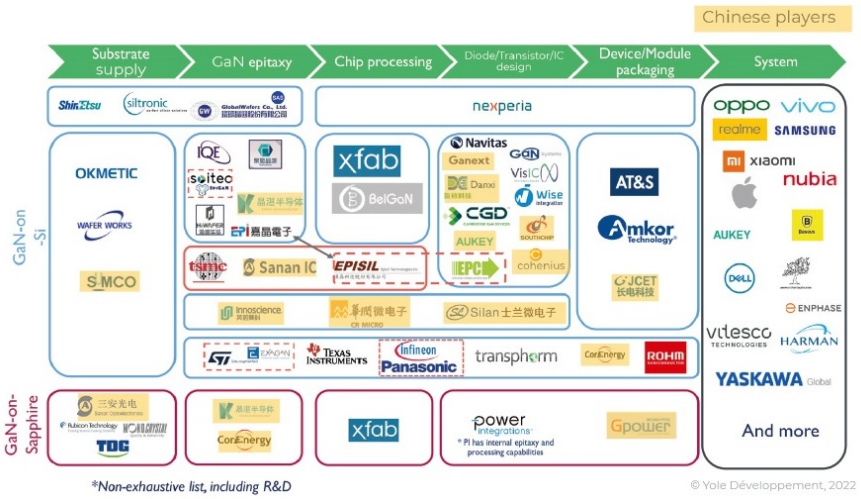

Figure 1.5: The main GaN players involved in the development and adoption of GaN technology [17].

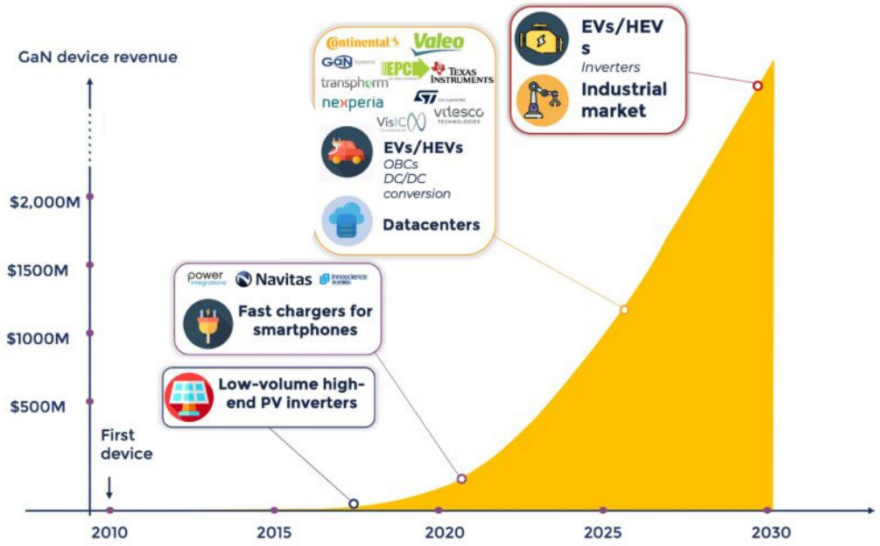

Figure 1.6: Long-term evolution of GaN-based Power Applications [18].

In this scenario, the GaN market feeds on itself because excellent GaN-based device performance forces companies to invest in further technology improvement and widely use these devices in their systems. Companies like Transphorm, EPC, Texas Instruments, Infineon, CGD, and GaN Systems have also announced several design wins [17]. Fig. 1.5 shows the leading players involved in the GaN market.

The possible applications for GaN–based technologies, as a result of operating voltage, cover the whole range from 30 V to 1.2 kV. The majority of devices target the 100-200V voltage range and the 600-650V range. The lower voltage capability devices are suitable for point-of-load applications i.e. low voltage DC-DC converters for IT or consumer electronics applications, while power factor correction (PFC), uninterrupted power supplies (UPS), motor drives, and photovoltaic (PV) system inverters require higher voltage rating (600V). Furthermore, GaN technology is already present in the ambitious and attractive automotive market through onboard chargers (OBC) and DC-DC converters. In the long term, in cases where GaN will have proven its reliability and high-current capabilities at a lower price, it may penetrate the more challenging electric vehicle (EV) and hybrid electric vehicle (HEV)

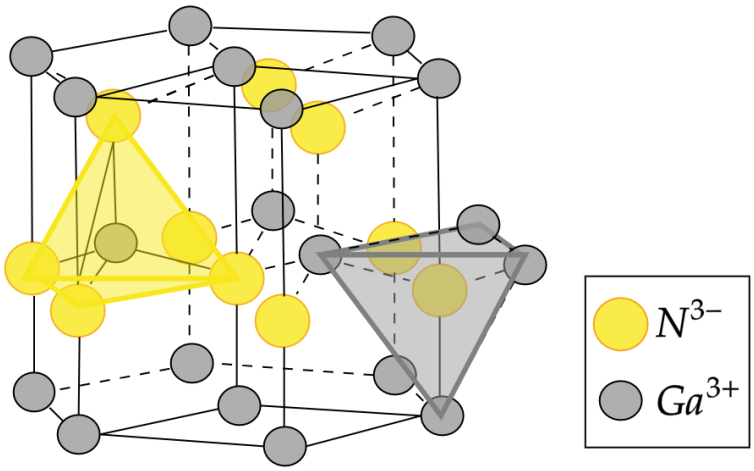

Figure 1.7: Wurzite structure of Gallium Nitride.

inverter market and the conservative industrial market as illustrated in Fig. 1.6 [18].

1.3 Understanding GaN Technology

Gallium nitride (GaN) is a compound semiconductor of basic materials which are typically used for all device layers requiring fast carrier transport. There are two different crystal structures of GaN: wurzite and zincblend [19]. The zincblend structure is metastable, while the wurtzite structure (Fig. 1.7) is stable and, therefore, it is used for electronic devices [20].

In the GaN-based devices, thanks to their architecture, two kinds of polarizations show up:

- Spontaneous polarization. It is induced by the different electronegativity between Gallium and Nitrogen atoms, and generally in every III-V compound. Therefore, Ga-N bonds are polar and the polarizations of Ga-face nitrides are all negative (Ga = 1.81χ and N=3.04χ). In the case of an alloy containing Aluminum, the higher the Aluminum content, the higher the polarization vector is (Al = 1.61χ) [21].

- Piezoelectric polarization. It is induced by applying stress to the ma-

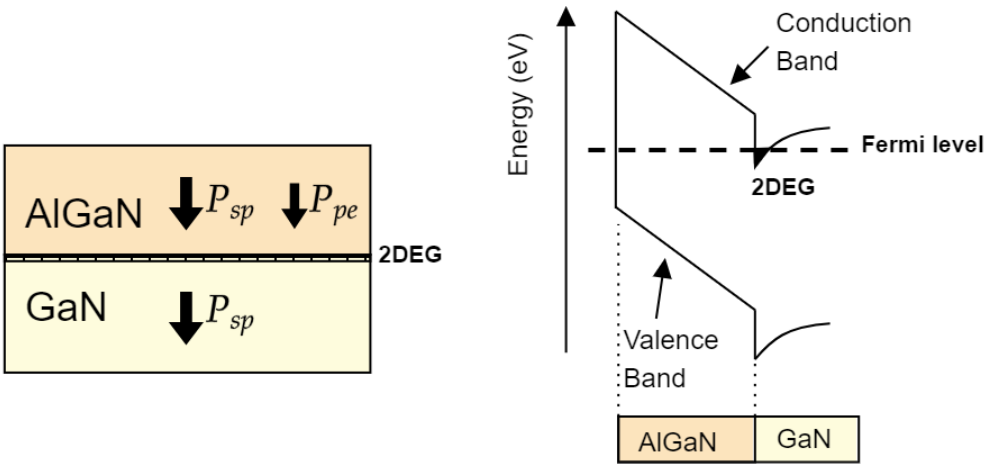

Figure 1.8: Polarization charges in GaN channel/AlGaN barrier and the formation of the 2DEG.

terial that distorts the crystal structure. As a result, an intrinsic polarization field is obtained (piezoelectric effect). The piezoelectric polarization is a function of the variation of the horizontal lattice parameter from its natural value. For instance, in the GaN-based device, the strained structure is obtained by growing AlGaN on GaN material. When AlGaN and GaN layers are in contact, the lattice constant is forced to be the same for both layers. The strain depends on the amount of aluminium and the thickness of the AlGaN layer [22].

It is worth remembering that the polarizations are vectors with an orientation. The orientation of P_{SP} and P_{PE} depends on the type of strain: in compressive-strain, they are opposed, and in tensile-strain, they are aligned [23]. P_{SP} and P_{PE} are added at the AlGaN/GaN interface and the resulting polarization P induces sheet charge densities, forming the so-called 2-dimensional electron gas (2DEG) as shown in Fig. 1.8 [24; 25]. Therefore, a large concentration of carriers in the GaN layer at the heterointerface is present without any doping.

The first GaN-based devices were able to conduct current without any positive gate voltage bias (normally-ON devices). However, in power applications, the normally-OFF devices are desirable for:

- Safety reasons. Power electronic circuits rely on normally-off power devices to provide additional safeguards for the equipment and its users. For instance, a malfunction of driver circuitry could turn-on a normally-ON device and damage the equipment [26].

- Power consumption. In the normally-ON devices, the gate voltage must be negative and not zero to ensure the device turn-off. Therefore, the power consumption due to the gate leakage is higher.

- Cost. Normally-OFF devices allow the integration of existing Si gate drive circuitry.

1.3.1 GaN-based High Electron Mobility Transistors

Several attractive approaches have been explored in order to convert the inherent depletion-mode (d-mode) operation of GaN-based High Electron Mobility Transistors (GaN HEMTs) into the enhancement-mode (e-mode) one, shifting the gate threshold voltage V_{TH} toward positive voltage. The first approach has been the GaN cascode configuration where the turn-on of GaN devices is tied to the turn-on of Si transistors connected in series. The drawbacks of this solution are primarily high parasitic inductances in the packaging process and a reduction of switching performance of GaN due to the presence of Si transistor [27; 28]. To maintain the high-switching capability of GaN, the recessed-gate structure has been developed in the Metal Insultor Semiconductor or Metal Oxide Semiconductor High Electron Mobility Transistors (MIS/MOS-HEMTs). For these fabricated devices, the AlGaN barrier under the gate contact is removed and replaced with oxide and, as a result, there is a positive threshold voltage shift. The latter is strongly correlated to the thickness of the oxide and a precise control of barrier recess is required (few nm). In addition, the recessed gate affects the 2DEG density, especially for high-voltage devices, leading to an increase of ON-state resistance R_{ON} [29]. Finally, the Schottky gate characteristics are also degraded by the recess-etching damage and the barrier thinning [30]. The technological improvement that has made GaN devices attractive for

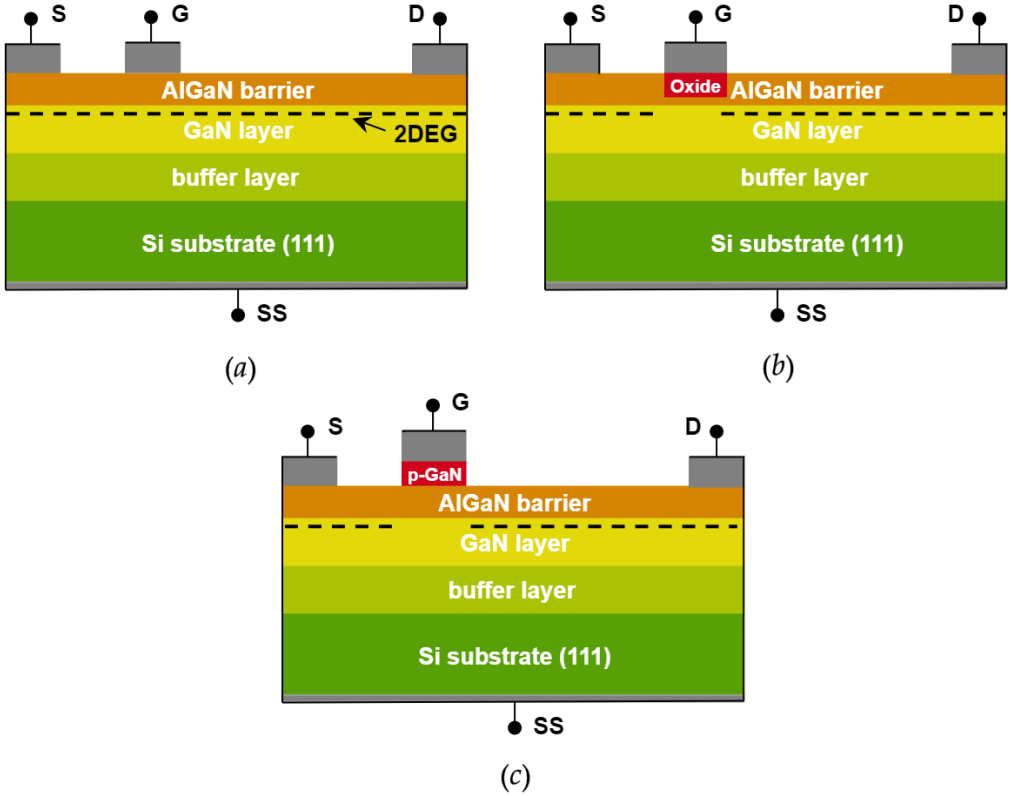

Figure 1.9: Different architectures of GaN-based devices: (a) normally-ON device; (b) MIS/MOS-HEMT; (c) pGaN HEMT.

high-power applications has been the use of a p-GaN barrier below the gate which depletes the channel and increases the gate turn-on voltage to 3 V [31].

Fig. 1.9 illustrates the structures of the mentioned GaN-based devices, in particular normally-ON device (a), the MIS/MOS-HEMT (b) and the p-gate HEMT (c).

1.3.2 pGaN HEMT

The GaN HEMT fabrication process needs the presence of an initial substrate to support the epitaxial deposition of the AlGaN/GaN heterostructure. Silicon substrates are already widespread to guarantee a low-cost production in comparison to SiC and sapphire (Al_2O_3) materials [32; 33]. Si and GaN

have a huge difference in terms of thermal expansion coefficients and a large lattice mismatch [34], therefore a transition layer (or buffer layer) is required to allow the growth of a high-quality GaN-layer. Generally, two kinds of interlayers are used to reduce the crack density and surface roughness of the GaN layer grown on Si substrate: i) multiple step-graded $Al_{1-x}Ga_xN$ buffers, introducing in a thickness up to few μm several layers varying gallium and aluminium composition (x) ranging in order to obtain the transition from AlN to AlGaN layer [35]; ii) AlN/GaN superlattice stack, alternating AlN and GaN layers [36]. As already mentioned, AlGaN/GaN heterostructure is grown on top of the buffer layer and a p-type gate under the gate metal contact is deposited. The gate contact is a Schottky contact to create back-to-back diodes and prevent an increase of gate leakage in any kind of voltage conditions [37]. Fig. 1.9c depicts the cross-section of pGaN HEMT. Furthermore, to improve the robustness of pGaN HEMT, a passivation material such as Silicon Nitride (Si_3N_4) is grown among device terminals [38] and, especially for high voltage devices, the source ohmic contact is additionally extended over the gate [39].

In terms of energy, by introducing a pGaN region, the potential in the channel is lifted ensuring the e-mode operation (Fig. 1.10). The application

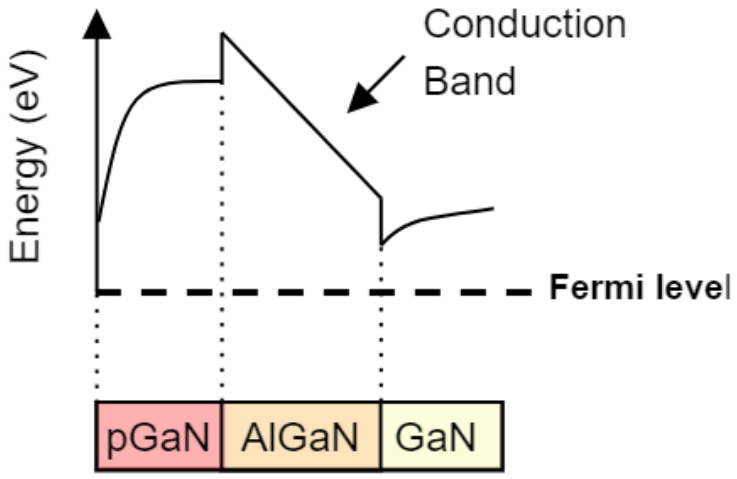

Figure 1.10: Band Diagram of pGaN HEMT when V_{GS} is 0.

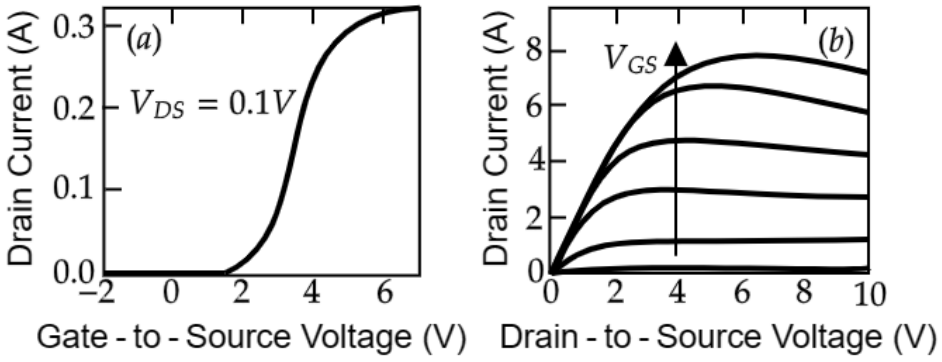

Figure 1.11: Transfer (a) and output (b) characteristics from 2 to 7 V_{GS} range of a typical 650 V e-mode power device.

of positive gate voltage (higher than V_{TH}) pulls the band in the channel below the Fermi level and re-establishes the 2DEG below the gate [40].

As a result, the I-V characteristics of 650V pGaN HEMT are illustrated in Fig.1.11 [41]. The device exhibits a finite low resistance in the on-state (typical 10-100 mΩ range) and a leakage current in the off-state (not shown in the figure because its value is much lower than the on-state current levels). In addition, the transistor can operate with a high voltage and current. The state of the device is controlled by the gate-to-source voltage V_{GS}.

1.4 pGaN HEMTs in Power Electronics

In the applications of power electronics, power devices play a crucial role as they must be capable of controlling the power flow with zero power dissipation ideally. During each switching period T_s, the transistor remains in on-state for t_{ON} time and in off-state for time t_{OFF}. In order to have zero power consumption, it is required to have zero current during the off-state and zero voltage during the on-state of the power device.

Unfortunately, the real devices, as pGaN HEMTs, present a leakage current I_{OFF} and on-state resistance R_{ON} that yields a power dissipation in off-state and on-state (conduction losses), respectively. Moreover, the transition between the on-state and off-state and vice versa is not instantaneous

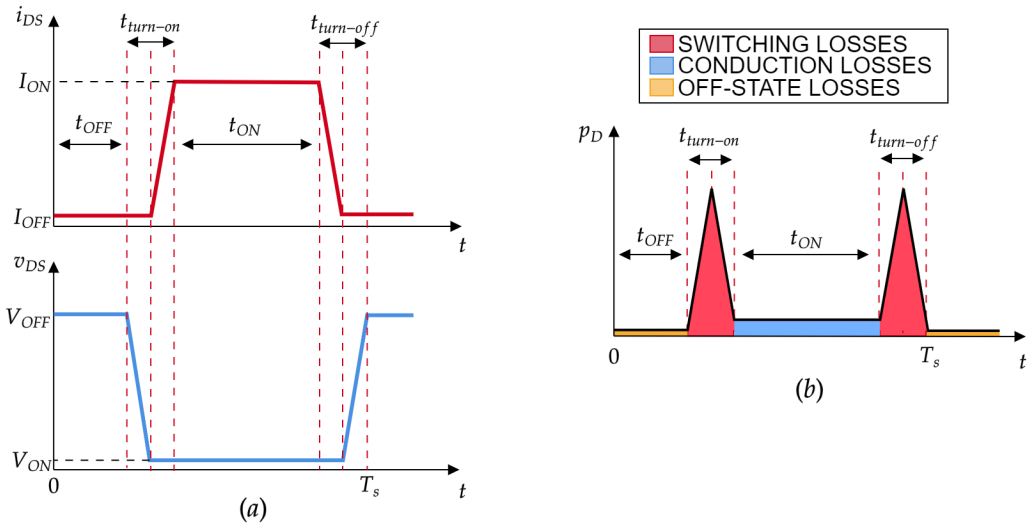

Figure 1.12: Typical switching waveforms (a) and power (b) of a power device used in a real application.

and they produce power dissipation called switching losses [12].

Fig. 1.12 depicts the drain-to-source $v_{DS}(t)$ and drain current $i_D(t)$ (a) and power $p_D(t)$ (b) that periodically affect the device while it operates in a real application. Switching and conduction losses are taken into account in the dissipated power of the power transistor P_D during a single switching period T_s (eq. 1.4).

$$P_D = \frac{1}{T_s} \int_0^{T_s} v_{DS} \cdot i_D \, \mathrm{d}t. \tag{1.4}$$

Therefore, in power applications, the operating point of a power transistor continuously shifts between on-state and off-state. Additionally, in the hard-switching conditions, the shift expects simultaneous high current and high voltage. All these operating conditions could be very stressful and degrade the device's performance. As a consequence, a reliability analysis is required.

1.5 Thesis Organization

This document is organized as follows. Chapter 2 introduces the reliability issues that affect the GaN-based devices and the main techniques used in literature to investigate the degradation of GaN HEMTs. In this scenario, a novel in-circuit approach is proposed to investigate the long-term reliability of power GaN HEMT. Chapter 3 provides an overview of the circuital problems associated with the design of a GaN-based converter and describes the proposed in-circuit setup. In Chapter 4 the validation phase to assess the experimental setup is reported. Chapter 5 shows all experimental results related to the GaN HEMT degradation obtained by means of the developed in-circuit setup. Finally, conclusions are drawn in Chapter 6.

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Chapter 2

GaN Reliability

2.1 Introduction

High reliability and low cost are mandatory requirements for the diffusion of a new technology. Power semiconductor devices are the most prone-to-failure components in power converters [1]. OFF-state voltage, gate voltage bias, hard-switching and self-heating effects over a long-time operation are the primary sources that lead to the failure. Additionally, by increasing the switching frequency and reducing the transistors' turn-on and turn-off times in the nanoseconds range, the device must sustain possible additional stress induced by voltage overshoots and current spikes. All these stress conditions influence the electric parameters of the device: ON-resistance R_{ON}, threshold voltage V_{TH} and gate leakage I_G. R_{ON} is associated with power losses, and it must be kept low to avoid the degradation of converter efficiency and excessive self-heating of the switching transistor; V_{TH} determines the gate overdrive voltage, and its instability modifies the maximum output current of the device; and I_G monitors the degradation in the gate region.

Furthermore, GaN HEMTs can be affected by several degradation mechanisms limiting their performance and reliability. A strong effort was made to identify and understand the different physical mechanisms causing GaN HEMT degradation.

This chapter deals with an overview of GaN reliability issues, focusing on

the main degradation mechanisms that affect the power GaN HEMTs and the developed techniques to monitor these phenomena.

2.2 GaN HEMT Reliability Issue

To guarantee the use of GaN-based devices in the next generation of power applications, the devices must be robust and reliable. Many studies in the literature have been conducted on GaN HEMT reliability. By referring to Fig. 1.12, it is clear that the power device operating in realistic conditions is stressed as follows:

- When the transistor is in OFF-state, a high drain-to-source voltage V_{DS} is applied to the HEMT while gate-to-source voltage V_{GS} is zero or less than V_{TH}.
- When the transistor is in on-state, the gate is positively biased, with 5–6 V and a high current flows between drain and source.
- When the transistor is in semi-ON-state, current I_D and voltage V_{DS} are high simultaneously.

The stress operating conditions could trigger several degradation mechanisms that induce: i) a drift of ON-state drain-source resistance (R_{ON}); ii) a threshold voltage (V_{TH}) instability; iii) an increase of gate leakage current. These effects limit the static and dynamic performance of GaN HEMTs.

2.2.1 Dynamic R_{ON} and V_{TH} Instability

Thanks to 2DEG with high electron mobility, the ON-resistance value covers a range from a few to a hundred mΩ. However, after stress due to operating conditions of the GaN HEMT, dynamic R_{ON} tends to increase (or current tends to collapse) reducing the advantages of GaN technology (Fig. 2.1 a).

As reported in Fig. 2.1 b, the overall R_{ON} consists of a series of resistive components: i) the channel resistance under the gate (R_{CH}); ii) the gate-to-source/drain access region resistance ($R_{AC,S}$ and $R_{AC,D}$, respectively); and

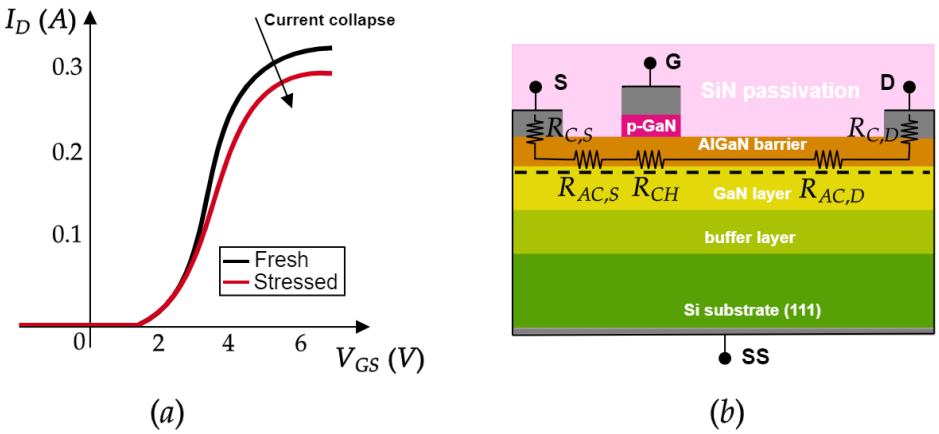

Figure 2.1: Illustration of dynamic R_{ON} phenomenon (a) and the components of ON-resistance in a p-GaN HEMT (b).

iii) source and drain contact resistance ($R_{C,S}$ and $R_{C,D}$, respectively). The trapping-induced mechanisms due to the OFF-state with high drain bias, the ON-state with a gate overdrive voltage and the high power state in the hard-switching transition could partially deplete the 2DEG, increasing the R_{AC} and/or R_{CH}. The time constants of the traps, the resistivity of the buffer stack and the floating potential in the p-GaN layer establish the recovery time of the R_{ON} degradation [2].

Under typical OFF-state conditions, the high electric field between gate and drain (lateral field) and drain and substrate (vertical field) induce trapping electrons both at the surface and in the buffer, respectively. When the lateral field is applied to the device, R_{ON} slowly increases due to the surface trapping in which electrons are injected from the gate toward the gate-drain access region by hopping [3]. Otherwise, when a strong vertical field is applied such as when the device is under back-gating conditions ($V_G = V_D = V_S = 0$ and $V_{SS} \ll 0$), the charging/discharging of the donor/acceptor buffer traps induce higher current collapse. The 2DEG conductivity is influenced by the injection of electrons from the substrate into the trap states primarily located in the buffer and also in the GaN channel layer. Both surface trapping and buffer trapping are strongly dependent on the temperature. A significant acceleration of surface current and drain-bulk leakage current was

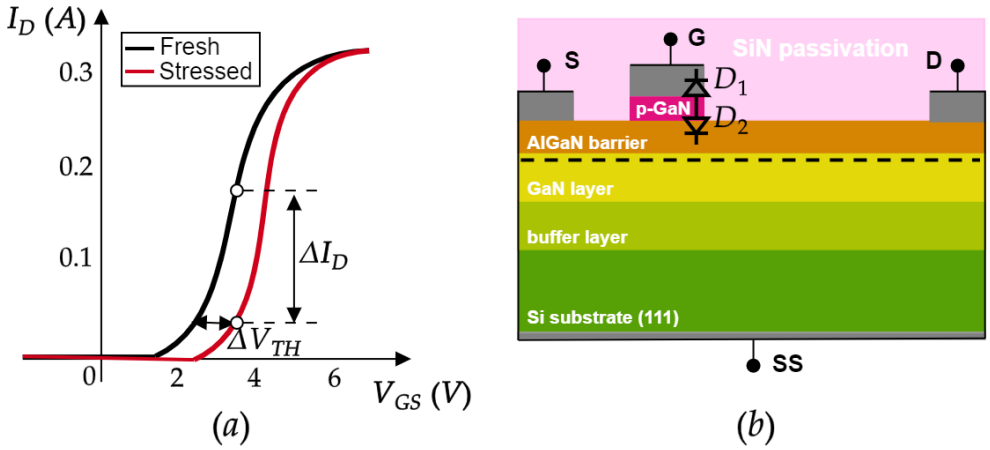

Figure 2.2: Illustration of a positive V_{TH} shift (ΔV_{TH}) induces R_{TH} increase (ΔR_{ON}) (a) and cross-section schematic of the gate stack of a p-GaN HEMT with Schottky gate contact (b).

observed at higher temperatures [3; 4]. Therefore, the buffer and passivation layer properties play an important role in the dynamic R_{ON}.

The dynamic R_{ON} could be also induced by V_{TH} instability. A positive V_{TH} shift (ΔV_{TH}) could result in R_{ON} increase by reducing the gate overdrive voltage (V_{GS} - V_{TH}) with a preset ON-state gate voltage (Fig. 2.2 a). As a matter of fact, at ON-state, electrons could be trapped at the interface/border states of the gate stack [5] and increase the V_{TH}. The influence of ΔV_{TH} is larger in the semi-ON-state region when the 2DEG is forming. At sufficient gate drive voltage, the R_{CH} shows lower sensitivity to the V_{TH} and R_{ON} is fully saturated.

Furthermore, the gate stack affects the reliability of the device. From the metal Schottky gate contact, which ensures more stability than the ohmic one [6], to the AlGaN layer, several trapping mechanisms could be triggered and induce V_{TH} instability. The electrons could be injected from 2DEG to the AlGaN barrier, metal/p-GaN and p-GaN/AlGaN under forward bias stress. In addition, although the Schottky gate contact blocks the gate leakage when the device is on (D1 in Fig. 2.2 b), during the switching to ON-state the negative charges, accumulated in OFF-state conditions, are left in the p-GaN

layer and result in positive ΔV_{TH}. Finally, in the p-GaN layer, the presence of defects related to Magnesium (Mg) doping and the generation of defects due to a high electric field between the gate and drain can lead to an increase in the leakage current via a defect percolation process and ultimately lead to device failure [7; 8].

2.2.2 Degradation Induced by OFF-State

The OFF-state bias condition is one of the most common stressors that could damage the power device due to the high electric field in the blocking region (gate-drain region). Generally, the degradation is investigated by carrying out step-stress tests. The GaN HEMT is off by fixing V_G at 0 V or negative voltages (source is directly connected to the ground) and V_D is swept up to the breakdown voltage. Drain, source and gate current are continuously monitored [9; 10]. As a result, drain leakage is a function of drain voltage and primarily distributes to the gate terminal at low V_D and to the source terminal at high voltages. Different field-dependent mechanisms may be triggered and cause permanent device degradation.

The several processes that contribute to drain current conduction in the sub-threshold regime (with high drain bias) are briefly summarized in the following:

1. Punch-through. The electrons from the source are injected into the buffer below the depleted region of the gate increasing drain-source leakage [11; 12]. To mitigate this mechanism, a carbon or iron doping GaN buffer layer (it is also called back-barrier) has been introduced at the interface between GaN and buffer layer in the p-GaN HEMT structure [13; 14].

2. Passivation layer. A non-optimal process may enhance the leakage conduction through surface states and/or defects within the passivation layer [15].

3. Vertical leakage. The high electrical field strongly interacts with both acceptor and donor deep levels in the buffer and this interaction is

time and temperature-dependent. As shown in [16], in the case of a thin buffer ($t_{BUF} = 1.25$ µm), a sudden surge in the leakage currents is obtained. In addition, the substrate also plays a role and its resistance could improve the robustness of the device at the expense of the V_{TH} stability [17].

4. Schottky gate reverse bias tunnelling. In p-GaN HEMT with a Schottky barrier diode, the reverse leakage is generally low. However, because of the high electric field, temperature and presence of traps in the barrier under the gate, the leakage may become higher and also contribute to the overall drain leakage [18; 19]. Generally, electrons are trapped or detrapped from the AlGaN barrier by means of phonon-assisted tunnelling (PAT) [20; 21]. This phenomenon is especially observed at the drain side edge of the gate. Usually, field plates [22] and/or slanted gate constructions [23] are applied to mitigate these effects.

Figure 2.3 depicts the previously described degradation mechanisms and their corresponding location in a GaN HEMT.

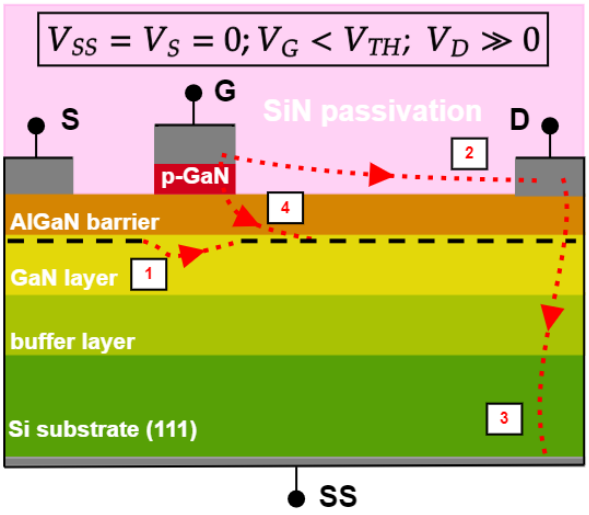

Figure 2.3: A sketch of the primary degradation mechanisms induced by OFF-state condition with high drain voltage bias: punch-through (1), passivation layer (2), vertical leakage (3) and Schottky gate reverse bias tunnelling (4)

2.2.3 Degradation Induced by ON-State

The maximum drain current in the ON-state is related to the applied gate-to-source voltage. The V_{GS} value depends on the circuit application but it is typically within the 4 to 7 V range. Most of the overdrive voltage drops on the depleted region of the Schottky junction and the high electric field located in that region may favour the time-dependent degradation process of the gate junction [9] or a time-dependent isolation region due to the defect percolation originated by pre-existing defects [24] [8]. The properties of the percolation path depend on process conditions and an improvement in lifetime can be obtained by modifying the barrier growth conditions [25]. Moreover, two other possible mechanisms can contribute to the breakdown of the gate junction: i) avalanche multiplication, electrons injected from the channel to the p-GaN region may trigger avalanche processes and lead to device breakdown; and ii) generation of donor-like traps in the p-GaN close to the AlGaN interface, which locally lowers the electric field in the AlGaN, and leads to the generation of localized leakage paths.

In contrast to the common application of gate voltage biases, recently, the square-wave pulse I–V test was used to study the gate breakdown and reliability in order to reproduce device operations in power converters. As a result, the effective gate lifetime decreases at the increased number of pulses, frequency and duty cycle, when the frequency reaches 1 MHz [26]. In addition, a dependency on both OFF-state time (when $V_{GS} = 0$) and transition time (rise and fall time) showed up. The transition time is responsible for the amplitude of the current peak during the turn-on/off of the device, while the OFF-time is correlated to electrostatic potential in the p-GaN layer at the switching phase (from OFF to ON). In particular, the potential peak increases with the OFF-time leading to a lower voltage drop, hence the electric field, on the Schottky depletion region [27].

Finally, at high operating current levels, significant power dissipation and, consequentially, self-heating could be detrimental to long-term operation. Fig. 2.4a depicts the area significantly stressed by self-heating occurring when p-GaN HEMTs are in ON-state. The hot spot is located in the channel

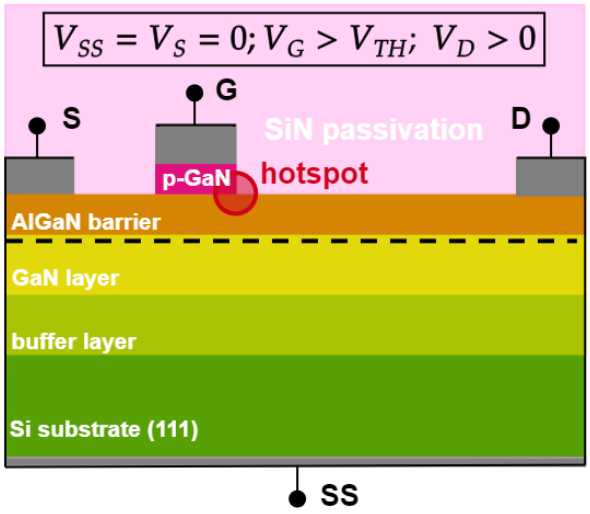

Figure 2.4: Internal thermal (a) and electric potential (b) distribution of a p-GaN HEMT under self-heating effect [28].

region near the junction of the gate and the passivation layer [28]. In addition, an increase in temperature leads to a decrease in mobility, hence an evident negative differential conductance phenomenon [29].

2.2.4 Degradation Induced by Semi-ON-State

In real-life applications, the semi-ON-state occurs because of the presence of internal and parasitic capacitance which prevents the instantaneous switch from turn-off to turn-on and vice versa of the device. During this phase, the channel is partially established, and a substantial number of electrons in the channel experience acceleration due to a strong electric field. This acceleration results in the movement of highly energetic (hot) carriers within the device, and this can potentially harm its reliability. This phenomenon is called the hot-electron effect.

The semi-ON-state stress can cause a significant increase in transistor I-V characteristics in terms of gate leakage, threshold voltage, ON-state resistance, peak of electric field and, as a consequence, operating temperature (self-heating effect) [30]. Indeed, during the hard-switching transition, the

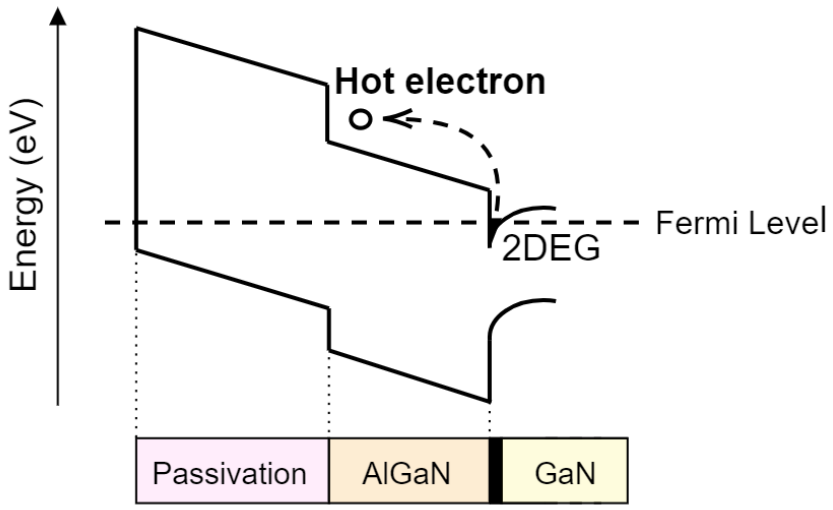

Figure 2.5: Band diagram of hot electron injection from the 2DEG to the passivation/AlGaN interface.

turn-on of the transistor dissipates a large amount of power. The power peak depends on the OFF-state voltage, the transistor's output capacitance and the gate voltage's slew rate [31].

These changes may be ascribed to the hot-electron trapping at the passivation/AlGaN interface or in the buffer region. At the passivation/barrier interface, because of the interface of two different materials, a high density of energy-distributed defects is present and a considerable amount of electrons are available for trapping [32]. Fig. 2.5 shows the band diagram related to hot electron injection. Initially, the trapping occurs near the drain side edge of the gate and, as more electrons are trapped, the electric field spreads towards the drain edge starting to trap electrons near the drain terminal [31]. In addition, some of the hot electrons are also spreading in the GaN channel up to the interface with the carbon-doped buffer region, where the trap concentration is considered negligible. Therefore, trapping phenomena related to hot electrons are strongly influenced by the properties of the buffer [33].

2.3 Characterization Techniques

To assess the GaN device reliability, including the evaluation of dynamic R_{ON} and ΔV_{TH}, the detection of trapping mechanisms and the device process optimization, two characterization techniques can be primarily distinguished, i.e., single transistor stress (on-wafer or in-package) and in-circuit. The single transistor stress - the most adopted one – is more oriented to accelerate life testing, involving harsh conditions, such as elevated temperatures, high voltages, or increased operating currents, for a relatively short period. The data collected can help predict the devices' reliability over an extended period and identify potential failure mechanisms. On the other hand, in-circuit analysis is more prone to reproduce the typical operating conditions of the device. This approach aims to evaluate the devices' performance and stability over their expected operational lifespan. In-circuit analysis provides useful insights into how the devices perform in realistic conditions and can figure out degradation mechanisms that occur over time.

The choice between these two approaches depends on the specific goals of the reliability assessment and the resources available. However, by combining insights from both approaches a comprehensive understanding of GaN device reliability is conducted.

2.3.1 Single Transistor Stress

The single transistor stress consists of the study of stress-induced degradation by monitoring the variation of current at each terminal and I-V characteristics of the individual transistor during the test. This method is useful for obtaining relevant physical information about the failure and ageing mechanisms. For instance, in [34], the negative V_{TH} shift in metal-insulator-semiconductor (MIS) HEMTs has been ascribed to the depletion of trap states located at the SiN/AlGaN interface and/or gate insulator. In [35], the role of the Aluminum content in the AlGaN barrier layer on the V_{TH} degradation of GaN HEMTs with p-type Schottky gate has been analyzed. The drain current collapse caused by self-heating effects and transient charge trapping phenomena has been investigated in [36] and [37], respectively. However,

these experimental results are limited to an application of standard DC or pulsed stress and recovery methods. In [38], Modolo et al. have proposed an on-wafer hard-switching setup to study the GaN HEMT degradation. However, the analysis was carried out at the switching frequency of 100 kHz, probably limited by the involved parasitics.

2.3.2 In-Circuit Stress

The in-circuit approach is based on developing test beds able to reproduce realistic stress conditions and monitor the health status of the GaN HEMTs. In [39], a chopper buck circuit, operating at 20 kHz switching frequency, is used to stress GaN HEMTs. However, the power devices were physically removed from the circuit to characterize their degradation in terms of R_{ON} and V_{TH} shifts. The threshold voltage is not straightforward to monitor, therefore in-circuit analyses mainly focus on the degradation of the R_{ON} drift evaluated during the device ON-state as the ratio between V_{DS} and I_D, measured through clamp circuits and current sensors, respectively. In [40], a set-up aimed at detecting the degradation of dynamic R_{ON}, in the milliseconds range, under different OFF-state voltages and temperatures, has been proposed. In [41], a test circuit in half-bridge configuration is adopted to evaluate the R_{ON} variation under several hard- and soft-switching conditions for switching frequencies up to 1 MHz. The test beds proposed in [42] and [43] allow the estimation of the R_{ON} degradation considering high switching frequency operation (up to 1 MHz), analysing the effects of high temperature and current intensity. Finally, in [44], an integrated DC-DC converter is proposed to monitor R_{ON} degradation up to a few hundred kHz switching frequency. However, the analysis based on on-the-fly measurement suffers some limitations. As reported in [45], the measured R_{ON} is sensitive to V_{TH} shift caused by charge trapping and de-trapping mechanisms. A positive V_{TH} shift reduces the gate overdrive voltage, hence I_D, misinterpreting it as a drift of R_{ON}. Therefore, a novel in-circuit approach is required to overcome the mentioned limits and obtain an accurate assessment of the power transistor reliability, by including the analysis of the full I-V characteristics.

2.4 Summary

In this chapter, the well-known reliability issues associated with GaN High-Electron-Mobility Transistors (HEMTs) were examined. An extensive discussion related to the dynamic R_{ON} and V_{TH} instability, and the physical degradation mechanisms induced by operating conditions of a power converter was treated. Furthermore, a brief overview of characterization techniques used in the literature to monitor the transistor degradation was provided, highlighting advantages and drawbacks.

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Chapter 3

A Novel In-Circuit Degradation Analysis

3.1 Introduction

GaN-based transistors, as already discussed in Chapter 1, are replacing the silicon MOSFETs. However, these devices still require a reliability assessment, including an in-circuit approach able to reproduce realistic stress conditions but also accurately evaluate the device degradation by means of full I-V characterizations. To benefit GaN properties, such as an increase in high switching frequency, the development of this kind of setup is very challenging. GaN-based circuits in power electronics require an accurate layout design using large planes, short distances, shielding and isolation to prevent voltage overshoot, voltage breakdown, current spikes and shoot-through phenomena and interference that could lead to failures. In addition, another aspect to take into account is the thermal management through proper layout and heatsink that could significantly impact the device's performance and reliability.

This chapter proposes a novel reliability analysis, overcoming the mentioned limitations in chapter 2 of the in-circuit approach. The latter consists of a DC-DC power converter conceived for long-term reliability analysis through full I-V characterizations. Initially, the chapter describes the setup

and adopted stress-measure-stress methodology to offer a complete picture of the developed in-circuit degradation analysis. Consequently, it focuses on the detailed description of the designed layout and implemented circuital solutions to guarantee a reliable and flexible setup, bypassing the additional problems due to the introduction of full I-V characterization.

3.2 In-Circuit Setup Description

The in-circuit setup proposed in this thesis is an automatic characterization system aimed at stressing the GaN HEMTs through a synchronous buck converter and assessing their degradation through a full I-V characterization. Thanks to this approach, the power devices operate under a combination of typical power converter stress regimes and, in addition, their degradation is accurately monitored (Fig. 3.1). The synchronous buck converter is a well-known step-down converter topology [1] perfectly tailored to stress power devices under hard-switching conditions. However, another converter topology could be used to stress the device such as boost topology or inverter.

A simplified sketch of the adopted setup is reported in Fig. 3.2. The circuit includes a standard type of synchronous Buck converter and the additional network to characterize the devices with a set of source measurement units (SMUs). The high-side transistor and low-side transistor, highlighted in red, are subjected to different electrical and thermal stress and they both are

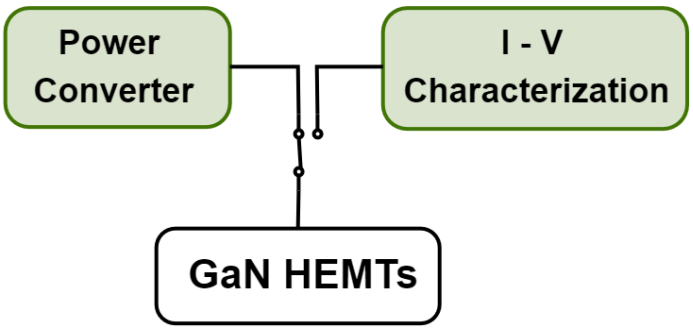

Figure 3.1: Idea of novel in-circuit approach.

characterized. During the stress mode, the GaN devices under test (DUTs) operate into the synchronous buck converter. During the characterization phase, the DUTs are isolated from the power network and connected, one at a time, to the SMUs. The DUTs' isolation avoids possible perturbations induced by the converter circuit during the I-V characterization. The switch between the converter (stress) and characterization (measure) phase during the test is handled by a matrix of electromechanical and solid-state relays. However, the hardware reconfiguration and converter operation are controlled by an external control unit.

Stress and characterization are successively repeated adopting a standard measure-stress-measure technique (Fig. 3.3). In addition, converter key parameters, such as output voltage, input power and efficiency are continuously

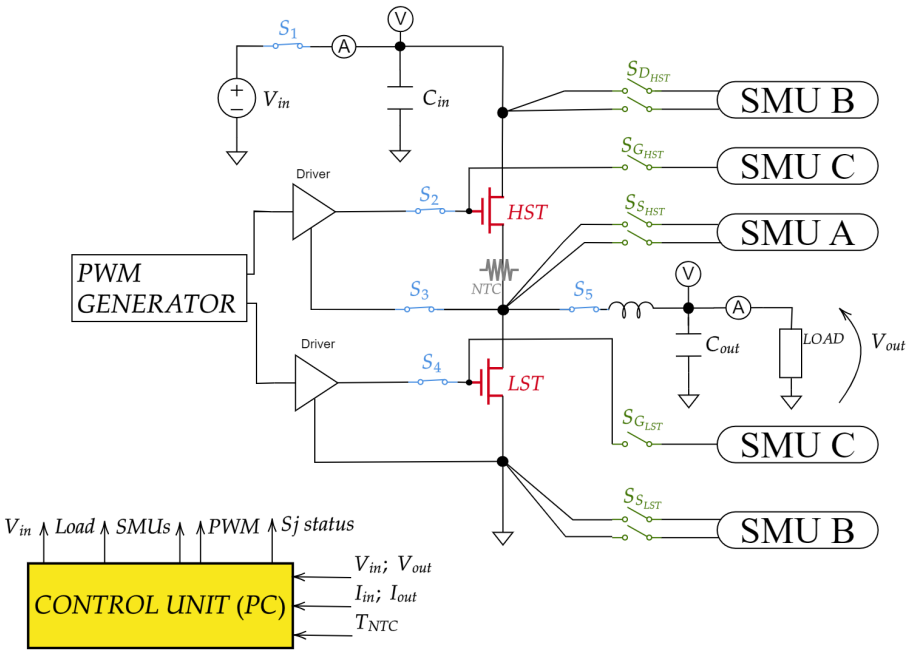

Figure 3.2: Simplified schematic of the setup adopted for the experimental in-circuit characterization of the GaN HEMTs. The blue relays enable the stress mode induced by the synchronous buck converter, whereas the green ones alternatively allow the characterization of the DUTs (in red). A control unit ensures the switching from stress to characterization mode and the correct operation of the setup.

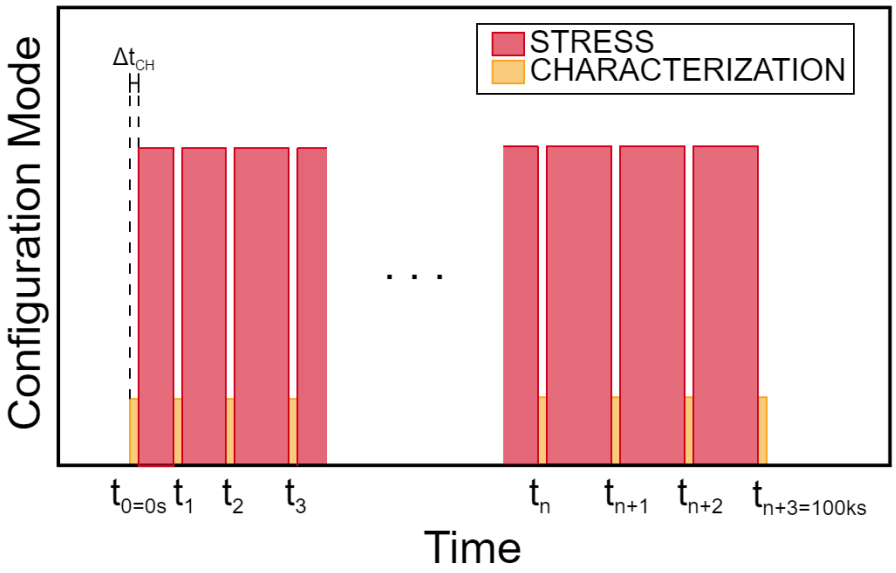

Figure 3.3: Illustration of the novel setup operation based on the measure-stress-measure technique. The stress phase is performed in the frame of the power converter, whereas SMUs carry out the measure one.

monitored during the stress. Moreover, to monitor the junction temperature of the devices, a thermistor is mounted between the two GaN HEMTs.

According to this approach, the monitoring of fast trapping and de-trapping phenomena ($<$ 1s) is not possible because of the relatively long time required by the single device characterization (about 2s considering the soft shutdown of the converter and the subsequent device characterization). Therefore, the setup is exclusively aimed at studying the long-term reliability of transistors operating in a real-life application (DC-DC converter). The next section will discuss in detail the setup, focusing mainly on the synchronous buck converter design.

3.3 Synchronous Buck Converter Design

GaN-based circuits demand meticulous design to minimize loops and paths and benefit the GaN properties in terms of power density and efficiency. The insertion of a full I-V characterization circuit causes increased parasitics due to GaN HEMTs' isolation from the power network by means of the location

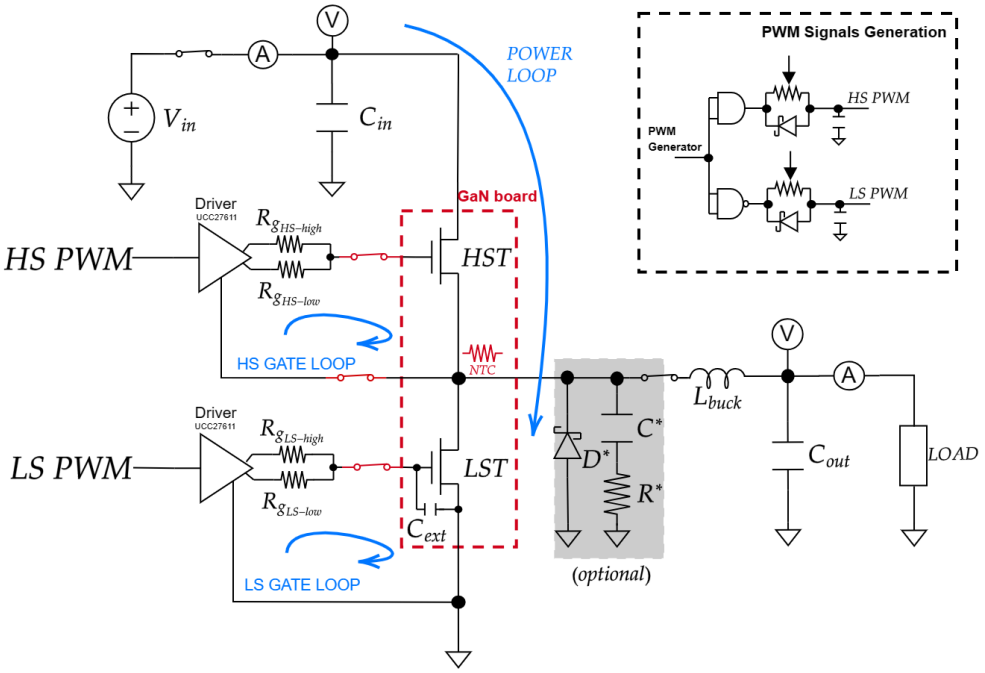

Figure 3.4: Simplified schematic diagram of the synchronous buck converter circuit resulting from relays' configuration during the GaN HEMTs stress.

of the relays in the critical paths. Moreover, the straightforward replacement leads to suboptimal layout configurations. Therefore, some circuital solutions and a layout design have been implemented to handle higher stray inductances avoiding additional stress, or failures.

3.3.1 Circuit Overview

Fig. 3.4 shows the resulting synchronous Buck converter circuit when the converter mode is enabled. An analog circuitry generates highly flexible PWM signals. The PWM principle schematic is also shown in the insert of Fig. 3.4. AND and NAND gates return the PWM generator signal and its logical negation for the HS PWM and LS PWM, respectively, while variable resistors modify the charging time of the capacitors, adjusting analogically rise and fall dead times. The dead time adjusting is crucial to prevent shoot-through or excessive voltage glitches affecting the gate-to-source voltage and maximize the converter efficiency [2; 3].

Two single-channel UCC27611 gate drivers with split-out configuration generate the signals to be applied to the gate of the transistors [4]. By using external gate series resistors (Rg, Fig. 3.4), it is possible to adjust the turn-on and turn-off times of the GaN FET switches and to dump the parasitic effects associated with the stray inductance introduced by the relays and by the transistors in the gate loops and power loop [5; 6]. Gate and power loops should be minimized as much as possible to prevent voltage ringing at the gate-to-source and switching node voltage, respectively [7].

The GaN HEMTs are assembled on a dedicated PCB (denoted by GaN board), which is necessary to straightforwardly replace the stressed DUTs after test completion. On the same board, an external capacitor C_{ext} between the gate and source LST transistor and a thermistor are placed. The additional capacitance in parallel to the internal C_{GS} is useful to improve the Miller ratio and prevent undesired device turn-on when a high and positive voltage slew rate (dv/dt) occurs at the drain of an off-state power GaN (Miller-induced turn-on) [5; 8; 9]. This phenomenon could trigger a shoot-through current which is very dissipative and stressful for the device. To maintain fast switching performance, it should be selected a lower C_{ext}.

Furthermore, the main board also includes an optional snubber circuit and Schottky diode to mitigate the ringing at the switching node [6] and avoid higher di/dt across the low-side transistor, respectively. However, the layout design remains the crucial part of the converter and it must carefully be developed.

3.3.2 Layout Overview

The synchronous buck converter layout used for the reliability application is shown in Figure 3.5. As mentioned before, the main board lacks GaN HEMTs which are assembled on their board and, therefore, the power loop and gate loops initially result incomplete. In particular, a section of the layout has been removed to ensure the maximum adherence between the GaN board bottom layer and the main board top layer and the minimum gap between packages of GaN HEMTs and heatsink facilitating efficient heat dissipation.

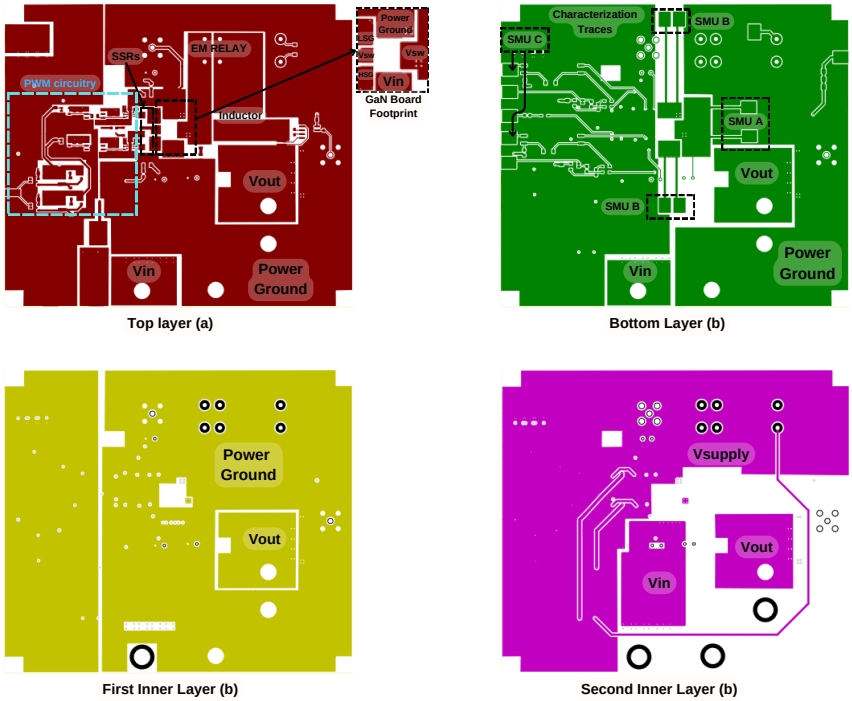

Figure 3.5: Implemented layout for a synchronous buck converter aimed at long-term characterization.

Despite the need to consider additional parasitic elements introduced by I-V characterization, the layout design follows the guidelines aimed at achieving an optimal layout [7]. The layout features can be summarized as follows:

- On the top layer, the PWM generation is mirrored along the x-axis to achieve symmetrical delays for both the high-side transistor and low-side transistor at the input of the drivers. This mirroring also maintains compliance with dead times which has been previously set.

- Each transistor has its gate driver for independent adjustment of rise and fall times.

- SSRs are placed as close to the gate pads and the switching node to minimize the gate loops. In addition, to reduce the ground bounce, the low-side gate driver ground is connected to the low-side transistor

source through a dedicated plane like the high-side one.

- On the first inner layer, it is possible to notice two ground planes. The first one is the power-loop ground suggested by the optimal layout, whereas the second one is for the current return from PWM generation circuitry.

- On the second inner layer, power planes are present. One of them is responsible for carrying the input voltage towards the drain of the high-side transistor. To ensure a stable and clean input voltage, an additional capacitor bank with lower capacitance is incorporated to filter out any unwanted noise or fluctuations.

- On the bottom layer, further relays are mounted to disable the stress mode due to the converter and start the full I-V characterization. To connect SMUs to transistor terminals, wire cables are soldered to the appropriate pads. This allows for precise measurement and characterization of the current-voltage (I-V) behaviour of the transistors.

- Output voltage has a dedicated section of the layout to reduce noise caused by hard-switching.

3.3.3 GaN Board

GaN board is a 12mm x 9.5mm 4-layer structure. On the bottom layer, the high-side transistor and low-side transistor of the half-bridge along with the extra capacitor and thermistor are placed (Fig. 3.6). Instead, on the top layer, just a pad couple connected to the thermistor terminals through vias are located. Furthermore, several approaches have been evaluated to figure out how to solder the GaN board on the main board. The using of castellated vias facilitates the soldering and removing action of the GaN board, avoiding mechanical damage.

Fig. 3.7 illustrates the cross-section view of the GaN board assembling on the main PCB without thermal management. It is worth noticing that

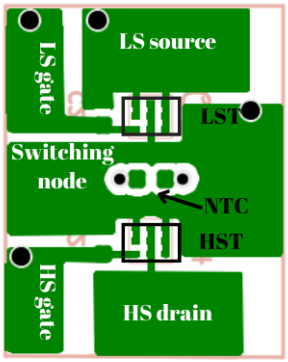

Figure 3.6: GaN board bottom layer: the DUTs are placed in the board centre and the NTC is mounted in the middle of them.

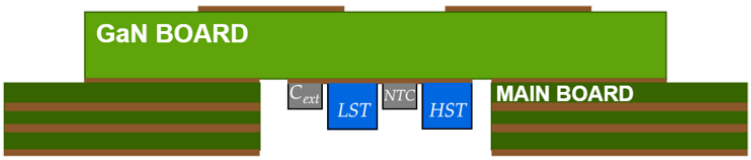

Figure 3.7: Simplified cross-sectional diagram of the GaN board mounting. LST and HST denote the low-side and high-side transistors, respectively. NTC and C_{ext} represent the negative temperature coefficient thermistor and the external gate-to-source capacitor mounted on the GaN board.

the power dissipated by GaN HEMTs is converted into heat, i.e. Joule effect, and the junction temperature of the devices increases. Good thermal management holds self-heating effect which could risk a thermal runaway.

3.3.4 Thermal Design

Fig. 3.8 depicts the adopted thermal management to favour heat exchange. Thermal dissipation of GaN HEMTs is allowed by using an aluminium push pins heatsink placed on the bottom of the main board. The residual gap of 0.185mm between the heatsink and transistors is filled by paste-based thermal interface material (TIM) [10].

To monitor the junction temperature of the DUTs under converter oper-

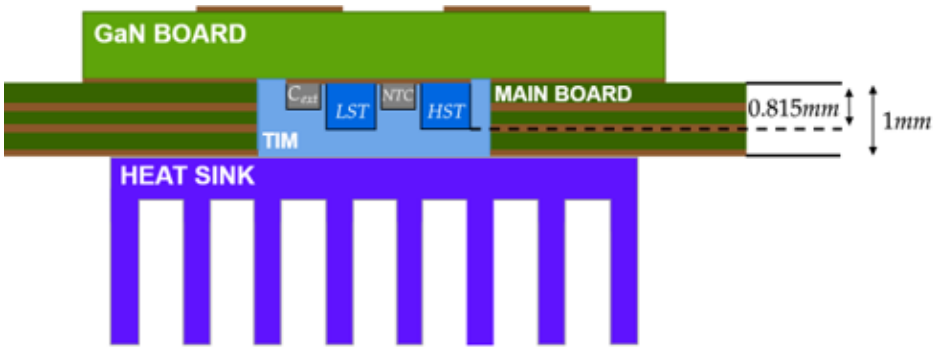

Figure 3.8: Cross section sketch of the GaN board mounting. LST and HST denote the low-side and high-side transistors, respectively. Thermal Interface Material (TIM) is used to fill the gap of 0.185mm between GaN HEMTs and the heatsink. NTC and C_{ext} represent the negative temperature coefficient thermistor and the external gate-to-source capacitor mounted on the GaN board.

ating conditions, the equivalent electrical diagram of the thermal design is developed. The thermal model of GaN transistors and heatsink is accurately provided by the manufacturer, including thermal capacitance and airflow. [11; 12].

GaN devices take a few milliseconds to reach the thermal steady state condition in contrast to hundreds of seconds of the heatsink. The latter determines the thermal dynamic of the converter. The heatsink thermal resistance R_{HA} is around 6 ° C/W, while thermal capacity C_{HS} is 18.37 (W · s)/ ° C calculated as follows:

$$C_{HS} = m \cdot c_p \tag{3.1}$$

where m is the mass of the heatsink and c_p is its specific heat capacity (for the aluminium is 0.897 J/gK). Finally, the thermal resistance R_{CH} of TIM is 11.9 ° C/W calculated by:

$$R_{\Theta TIM} = \frac{d}{A \cdot k} \tag{3.2}$$

where d is the thickness of the TIM, A is the cross-sectional area perpendicular to the heat flow path, and k is the thermal conductivity.

Fig. 3.9 reports the complete model of the adopted thermal management,

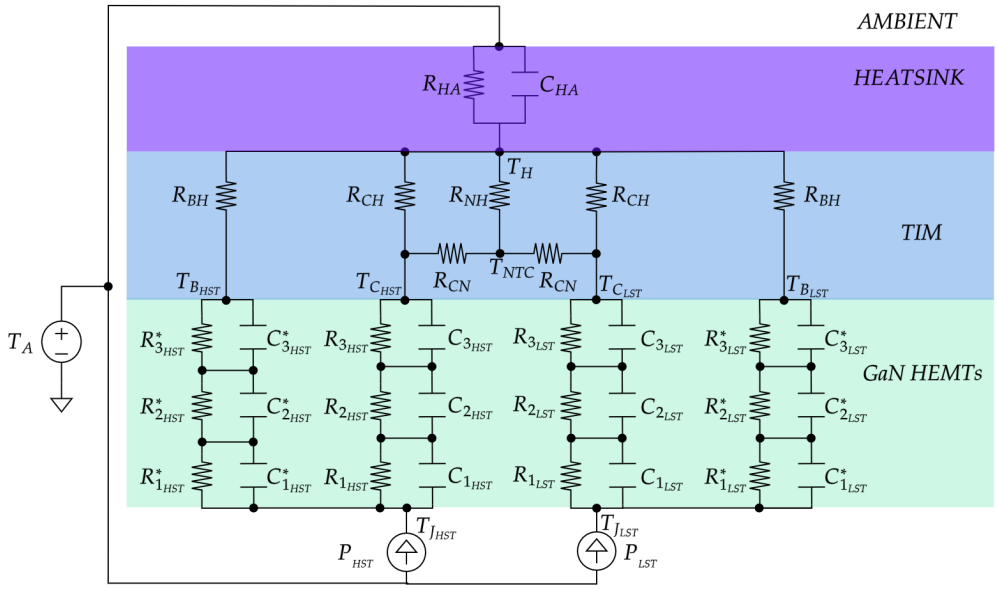

Figure 3.9: The entire transient model of the developed thermal setup from the junction of the devices to ambient. The thermal model includes both heat exchange paths through the case of transistors and the solder bumps (and board).

including thermal capacitances and heat conduction path provided by solder bumps. Since the board is also connected to the heatsink through TIM, heat conduction is also present $R_{\Theta BH}$ [13]. Furthermore, an additional negative temperature coefficient (NTC) thermistor is placed in the middle of the two transistors to monitor the temperature stress induced by the converter operation and the temperature of the characterizations. Therefore, the equivalent circuit presents symmetric (the transistor is the same for high-side and low-side) and only an imbalance of dissipated power between transistors leads to different junction temperatures.

To evaluate the accuracy of this model, a test has been carried out in order to stress one device in ON-state at 1W, while the other one is maintained OFF. Under this operating condition, the thermal simulation returns an NTC temperature of 32.5°C in contrast to the experimental value of 32.9 ± 0.375 °C.

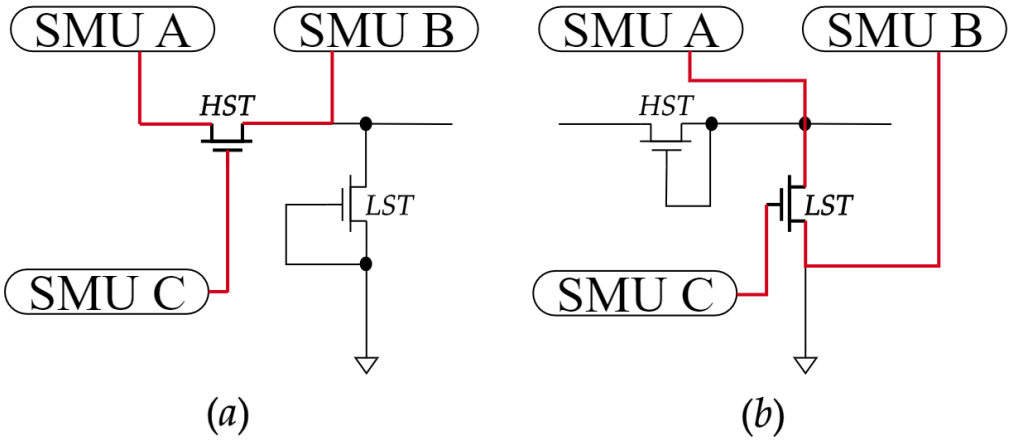

Figure 3.10: Electric Diagram of the resulting characterization circuits which allows to carry out the full I-V curve for the high-side (a) and low-side (b) transistor.

3.4 I-V Characterization Design

SMUs perform the transistor's I-V characteristics through a 4-wire configuration and static characterization. The characterization mode occurs in two steps. For the high-side characterization, SMus are connected to HST terminals and the LST gate and source are short-circuited. Successively, thanks to external relays, SMUs are forced to the LST terminals and the HST gate and source are short-circuited for the LST characterization. The short circuit between the gate and the source of the transistor ensures its off-state.

Fig. 3.10 displays the two resulting configurations for the high-side and low-side characterizations, respectively. These configurations are achieved using relays placed on an external board referred to as the 'Relay board.' This external board enables the switching of the setup's operating mode and automation of measurements through a dedicated workstation.

3.5 Setup Prototype

Fig. 3.11 shows the developed setup. As previously mentioned, it consists of two boards: the relay board (on the left) and the main board (on the right).

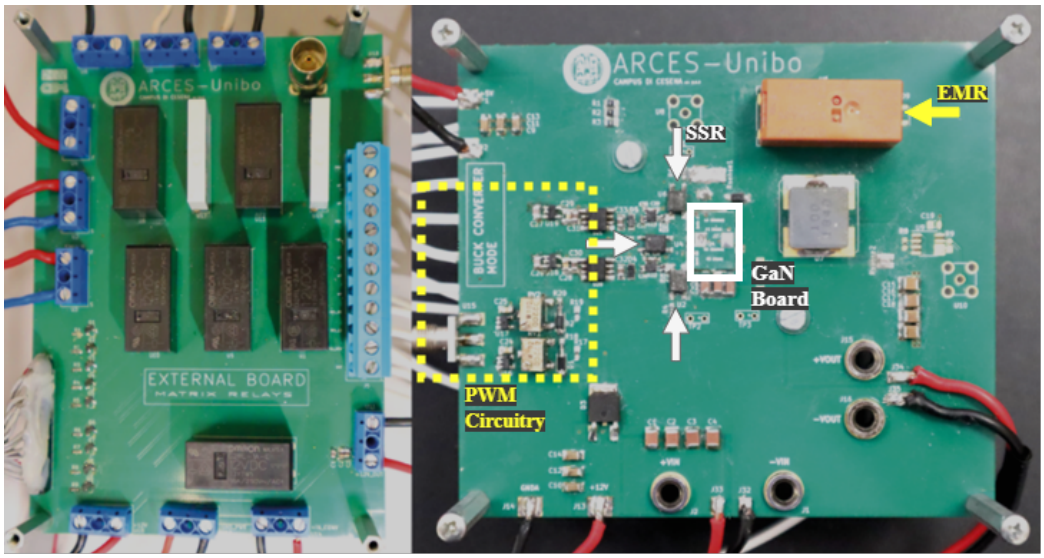

Figure 3.11: Photograph of the relay board (left) and main board (right). In the latter, it is possible to note: the PWM circuit (yellow box), solid state relays (white arrows), electro-mechanical relay (yellow arrow) and GaN board (white box).

On the relay board, there are placed only mechanical relays to switch the connections of power DUTs terminals. The configuration of the matrix of relays can automatically change the operating mode of the setup, switching from the stress mode to the characterization one and vice versa.

On the main board, it is included the analog circuitry (dash yellow box) able to generate highly flexible PWM signals with adjustable dead time. Furthermore, solid-state relays (SSR) placed in the gate loops and electromechanical relay (EMR) to disconnect the output filter from the switching node are shown. Finally, the assembled GaN board is indicated by the white box.

To perform in-circuit investigations, the setup requires to be validated to prevent any additional stress during synchronous buck converter operation and accurately measure the I-V characteristics of the device.

The main features of the converter are described in 3.1. The limits are based on the operating conditions specified in the data sheets of the components used in the converter. Consequently, the transistors under test must be selected for this type of stress environment.

Converter Features	Min.	Typ.	Max.
Voltage (V_{IN}) [V]	12	48	100
Current (I_{OUT}) [A]	1	4	10
Duty cycle (D)	0.1	0.25	0.9
Temperature (T_a) [^oC]	25	25	85
Switching frequency (f_{sw}) [MHz]	0.1	1	2

Table 3.1: Operating features of the implemented synchronous buck converter

3.6 Summary

In this chapter, a novel in-circuit degradation analysis was introduced. This approach uses full I-V characterization to faithfully investigate the long-term reliability of power GaN HEMT operating in a power converter. In this manner, the limits of the characterization techniques used in the literature are overcome. Moreover, the setup was described in detail, and the circuit, layout, and thermal design were presented. The insertion of I-V characterization led to an increase in parasitics in the chosen synchronous buck converter, and several solutions were implemented to achieve a 1 MHz switching frequency and prevent undesired ringing and turn-on in the half-bridge configuration.

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Chapter 4

In - Circuit Setup Validation

4.1 Introduction

The setup validation is an indispensable step to thoroughly assess and verify the performance and functionality of the experimental setup before proceeding with actual experimentation. Thanks to the validation, valuable insights into the setup's intricacies, potential limitations, and areas of improvement are provided.

This chapter reports the validation phase of the designed layout. It shows the setup features, exploring converter capability in terms of efficiency and signal integrity. In addition, the experimental waveforms captured by a high-bandwidth oscilloscope are compared to hybrid simulations which take into account the parasitics of the layout. Moreover, for the characterization mode, this chapter investigates the perturbations of I-V characteristics originated by the power circuit. Finally, it provides an example of a setup operation performed at $V_{IN} = 48$V, $I_{OUT} = 4$A, $D = 25\%$, $f_{sw} = 1$MHz and $T_a = 25°$ C by way of illustration.

4.2 Synchronous Buck Converter Mode

To validate the operation of the designed synchronous buck converter and understand the effects of the layout parasitics, the setup is configured in stress

mode with 80V and 6.8A enhancement mode GaN HEMTs with an input voltage V_{IN}, duty cycle D and switching frequency f_{sw} of the converter fixed at 48V, 25% and 1MHz, respectively. The low-side (LS) gate voltage, high-side (HS) gate voltage and switching voltage are monitored by means of a RTM3004 digital oscilloscope [1] and R&S RT-ZP05S passive probes [2] with 1 GHz and 500MHz bandwidths, respectively. High-bandwidth oscilloscope and probe are required to observe the ringings that occur at the test points of interest. As a matter of fact, the capability of the whole measurement system is given by:

$$BW_{-3dB} = \frac{1}{\sqrt{\frac{1}{BW^2_{-3dB,scope}} + \frac{1}{BW^2_{-3dB,probe}}}} \tag{4.1}$$

where BW_{-3dB}, $BW_{-3dB,scope}$ and $BW_{-3dB,probe}$ are the maximum bandwidths (in Hz) available to the system, scope and probe, respectively [3]. It is evident from Eq.4.1 that an element with lower bandwidth has a greater effect on the overall system bandwidth BW_{-3dB}. In addition, the Eq.4.1 indicates the upper bandwidth limit of the system, indeed it could be lower due to the techniques to increase the bandwidth, such as oversampling.

Fig. 4.1 shows the low-side gate voltage (a), the high-side gate voltage (b) and switch node voltage (c) in one switching period T_s at an output current I_{OUT} of 4 A and ambient temperature T_a of 25 °C. When the high-side transistor starts to turn on, a ringing appears on the low-side gate voltage caused by the parasitic tank. It is worth remembering that the required gate-to-source voltage range is -4 to 6V. Instead, concerning the switching and gate voltage, it is possible to note just an overshoot of 10% of the switching voltage during the high-side turn-on phase, which means the used gate resistors dump the layout parasitic effects.

It is important to note that every signal refers to the ground. In order to monitor the high-side gate-to-source voltage, almost a high-bandwidth, high common mode rejection ratio (CMRR) and high-voltage differential probe is required [4]. It has been tried using two single-ended probes and oscilloscope math to measure the difference, but it results in less accurate measurements

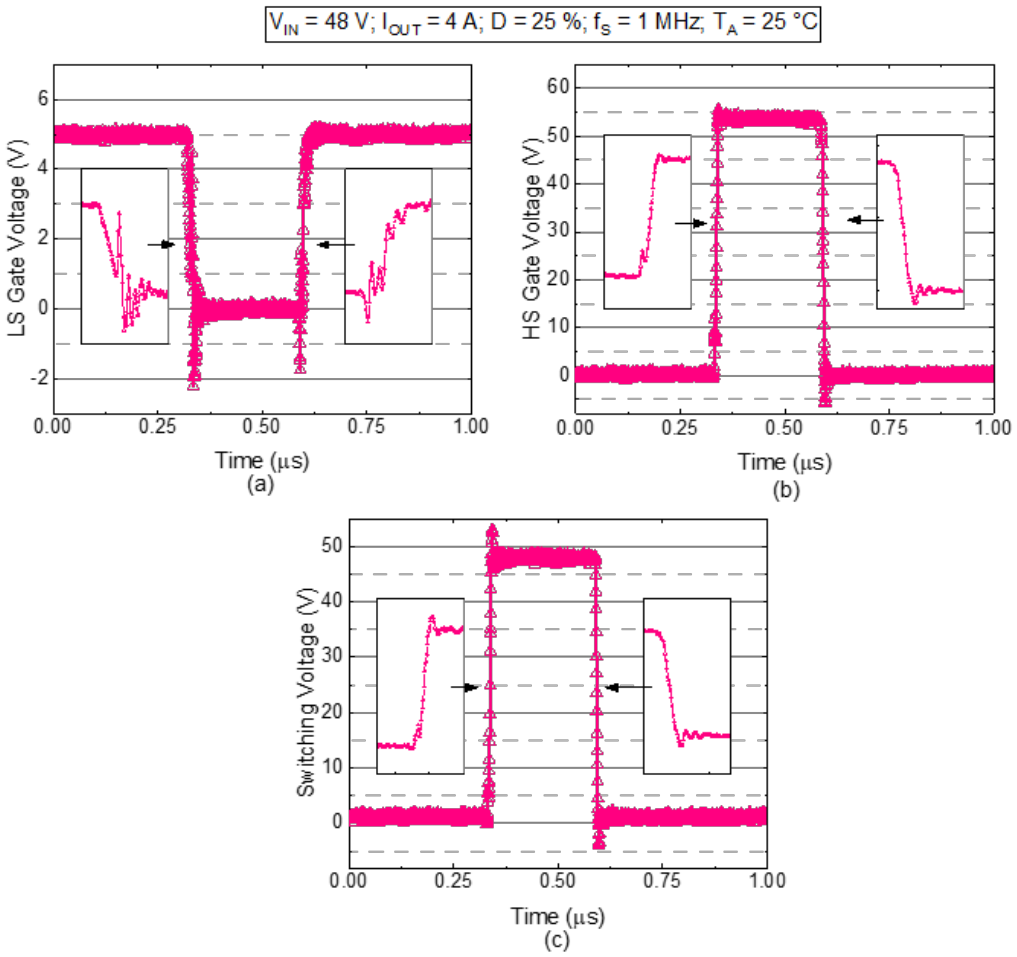

Figure 4.1: Waveforms captured by RTM3004 oscilloscope when the setup operates as synchronous buck converter: (a) Low-Side gate voltage, (b) High-Side gate voltage and (c) Switching voltage.

due to a high mismatch between probes (Fig. 4.2). Finally, despite using spring clips to ground the passive probes minimizing the inductances of ground lead [3], the placement of measurement points (test point) far from the device contacts and the probe input impedance add additional spurious resonances. Therefore, hybrid simulations have been carried out to evaluate the gate-to-source voltages and switching voltage.

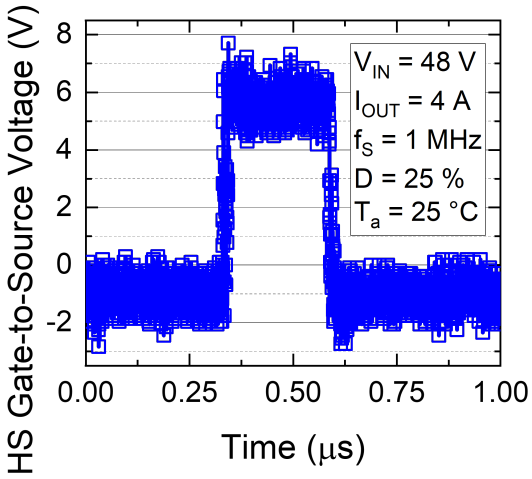

Figure 4.2: High side gate to source voltage using two single-ended probes and oscilloscope math.

4.2.1 ADS Co-Simulations

Numerical simulations are performed with Advanced Design System (ADS) [5]. ADS allows to take into account layout design and materials by means of an electromagnetic (EM) simulation of the layout; and ADS co-simulation combines the spice model of components and the EM model of the layout, including the parasitics introduced by the layout design, to accurately evaluate the features of the converter. However, these circuital simulations require several steps to do.

Initially, it must be defined the used substrate for the manufacturing of the PCB. In this case, it includes 4 layers within 1mm thickness, whereas the thickness of copper traces is 60 μm in according with the manufactured main board. The layers are isolated from each other by means of a standard glass-reinforced epoxy resin laminate called FR4.

In addition, the layout designed by software for electronic design automation must be imported and associated with the substrate stack. Fig. 4.3 illustrates the schematic of the manufactured setup in ADS.

Successively, the electromagnetic model of the layout must be created. To generate the EM model of the power section of the main board and of the GaN board, the EM simulations have been performed at Momentum RF

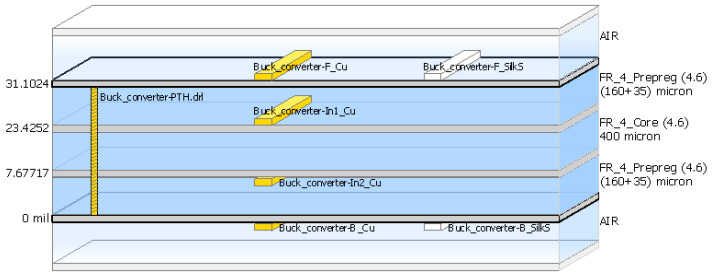

Figure 4.3: A Schematic of a PCB substrate in ADS. It features a substrate stack composed of four layers in compliance with the manufactured main board 3.11

simulator with mesh density = 20 cells; mesh frequency = highest simulation frequency; frequency plan from 0 to 1GHz.

Finally, the spice models of the components must be imported and connected between the ports of interest on the layout. The layout ports have been defined during the EM model generation [6].

Fig. 4.4 depicts the schematic of the power section of the main board

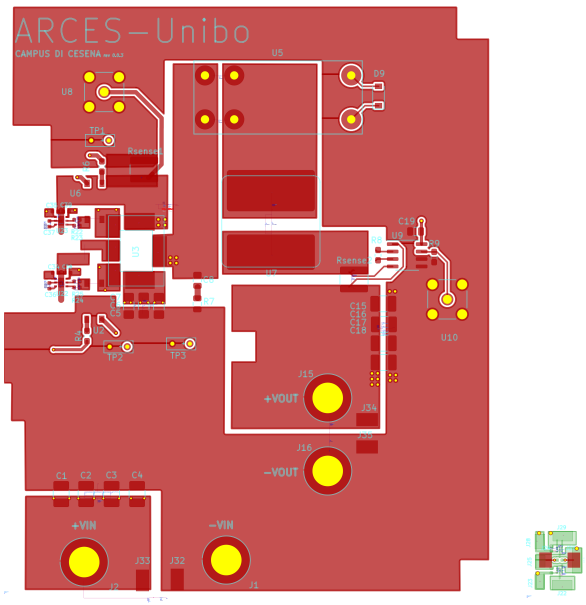

Figure 4.4: Simulated power section of the developed setup in ADS. To consider the layout parasitic effects, the main board and GaN board are previously simulated through ADS EM simulator and the resulting EM models are used in spice simulations along with other components spice models. Figure not in scale.

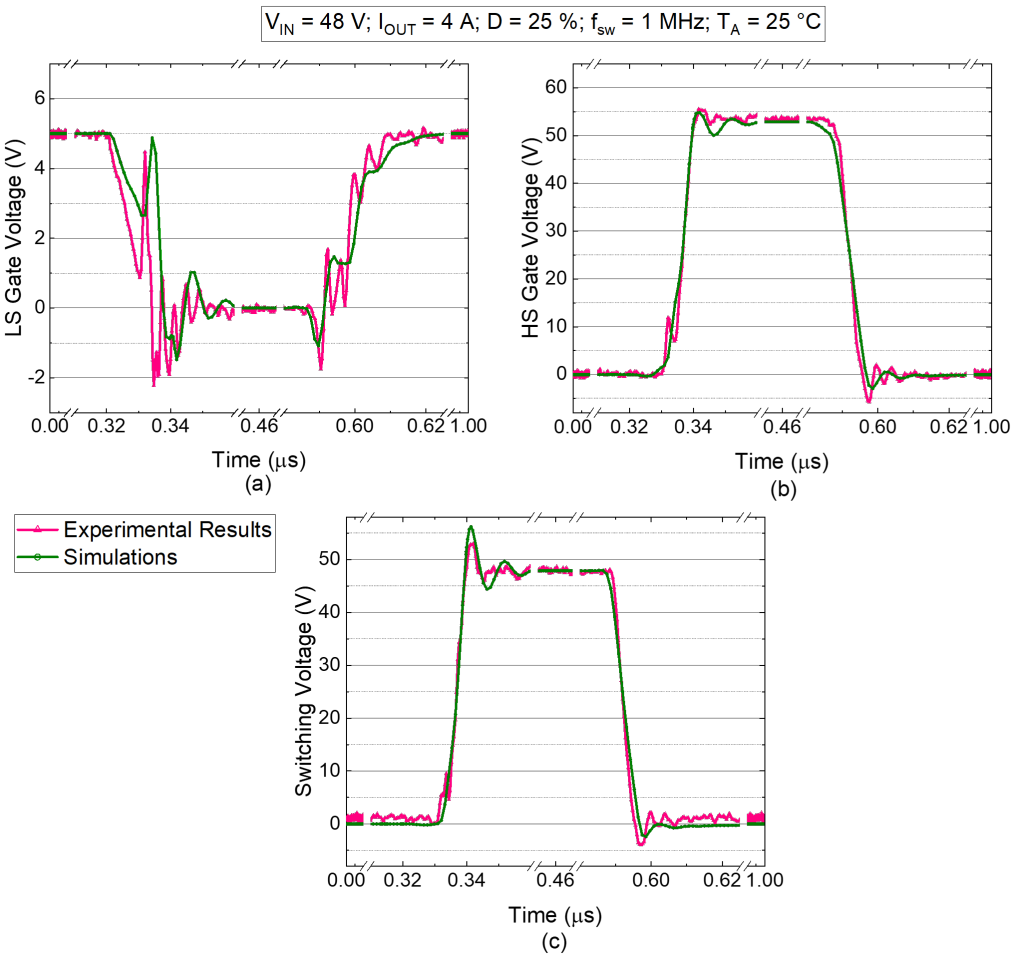

Figure 4.5: Comparison of the LS gate voltage (a), HS gate voltage (b) and switching voltage (c) in the case of simulated and experimental circuits. The simulated circuit has been calibrated in order to get comparable voltage levels of the real waveforms. As a result, accurate gate-to-source voltages can be evaluated.

used to simulate the synchronous buck converter operation. SSRs and the welds between the GaN board and the main board are modelled by mΩ resistance neglecting the induced inductance. Whereas, to compare faithfully the simulation results to the experimental one, the passive probe electrical model is considered.

Fig. 4.5 reports ADS simulation result compared with the experimental waveforms at $V_{IN} = 48\text{V}$, $I_{OUT} = 4\text{A}$, $D = 25\%$, $f_{sw} = 1\text{MHz}$ and $T_a = 25\ ^\circ\text{C}$. It is noticeable that a good agreement between experimental and simulated

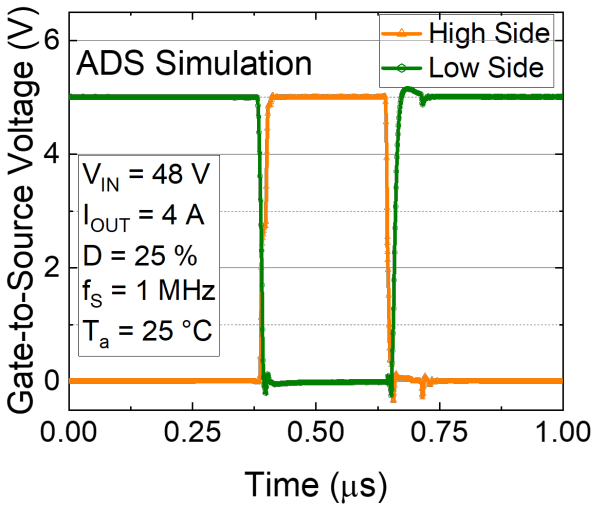

Figure 4.6: Gate-to-source voltages of the low-side transistor (green) and high-side transistor(yellow) when synchronous buck converter operates at V_{IN} = 48V, I_{OUT} = 4A, D = 25%, f_{sw} = 1MHz and T_a = 25° C.

waveforms has been attained. ADS simulation suggests that the DUTs are not affected by additional stress provided by the layout and, as illustrated in Fig 4.6, the applied gate-to-source voltages do not present dangerous ringing or overshoots that could induce undesired turn-on.

4.2.2 Efficiency

To fully explore the capability of the prototype converter and to analyze the impact of PCB parasitics on the conversion efficiency, the circuit was tested within 1A - 8A output current intensity range at $V_{IN} = 48$V, $D = 25\%$, $f_{sw} =$ 1MHz and $T_a = 25°$ C. The efficiency was monitored by means of voltmeters and amperemeters located at both input and output stages (Fig. 3.4).

Fig. 4.7 reports the experiment results and, in addition, a comprehensive comparison to the corresponding ADS simulations. The measured conversion efficiency η reaches a peak of over 94.5 % between 3 A and 4.5 A. The simulations faithfully replicate the behaviour observed in the real-world experiments and exhibit only a minor upward offset of 0.36% (maximum difference). This discrepancy may be attributed to the underestimation of

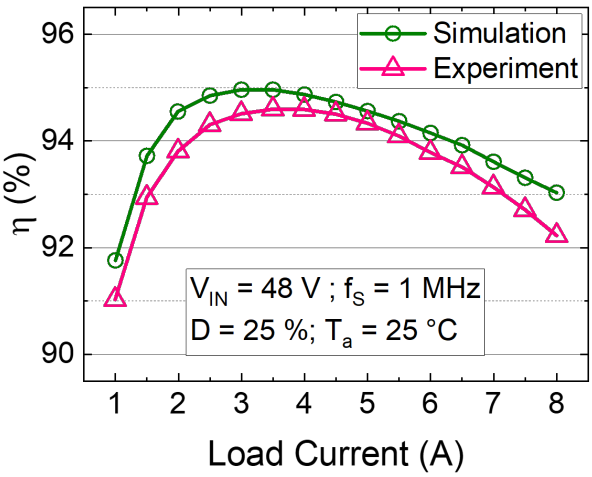

Figure 4.7: Efficiency curve (experimental and simulated) of the proposed setup in synchronous buck converter configuration at V_{IN} = 48V, D = 25%, f_{sw} = 1MHz and T_a = 25° C.

power losses in the simulations. The power losses for each component are calculated by integrating the instantaneous power for 300 switching periods. However, two key factors could contribute to this underestimation:

- Simplified Parasitics: The simulations employ simplified models for the parasitics introduced by relays and welds;
- Lack of Self-Heating Consideration: The simulations do not account for the effects of self-heating in the power transistors, which can cause slight drift in their electrical characteristics, even under nominal operating conditions.

Overall, although the parasitics introduced by the additional characterization circuitry (e.g. the relays), the conversion efficiency is in line with state-of-the-art GaN-based DC-DC converters [7; 8].

4.3 Characterization Mode

In order to investigate the characterization mode of the developed setup, several measurements are carried out using 100V enhancement mode GaN

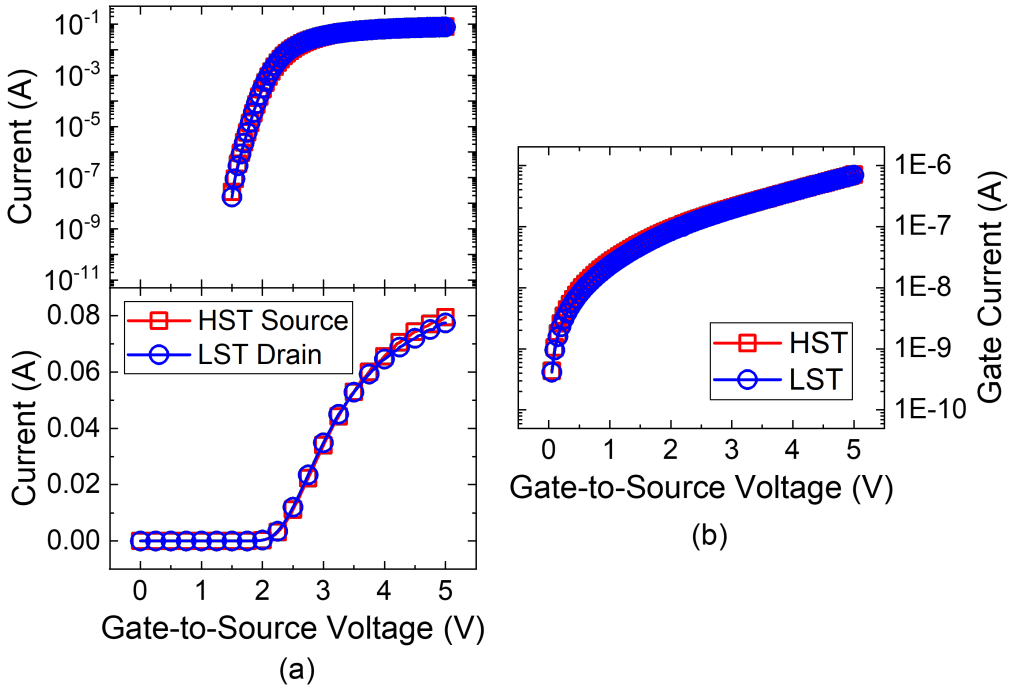

Figure 4.8: Full I-V characterization of the high-side transistor (in blue) and low-side transistor (in red) performed at V_{DS} = 1mV. The trans-characteristics (a) are shown in log scale (on the top) as well as in linear scale (on the bottom), whereas the input characteristic is in log scale (b).

HEMTs with different configurations. This section aims to show the complete I-V characterization obtained through the setup, motivating some design choices and reporting the tracing curves problems when the DUTs are not correctly isolated from the power converter.

The expected characterization methodology involves high-side transistor characterization first and, then, the low-side one. SMUs apply a drain-to-source voltage, ranging in a few mV to not overcome the instrument current limits, and sweep gate-to-source voltage from 0 to 5V. Simultaneously, they sense all currents across the device terminals. To measure accurately the low R_{ON}, the 4-wire Kelvin technique has been implemented.

Fig. 4.8 reports the full I-V characterization of HST and LST performed at V_{DS} = 1mV. For HST, current sensing is carried out by the source terminal, whereas, for LST, by the drain one. As it is possible to notice, the

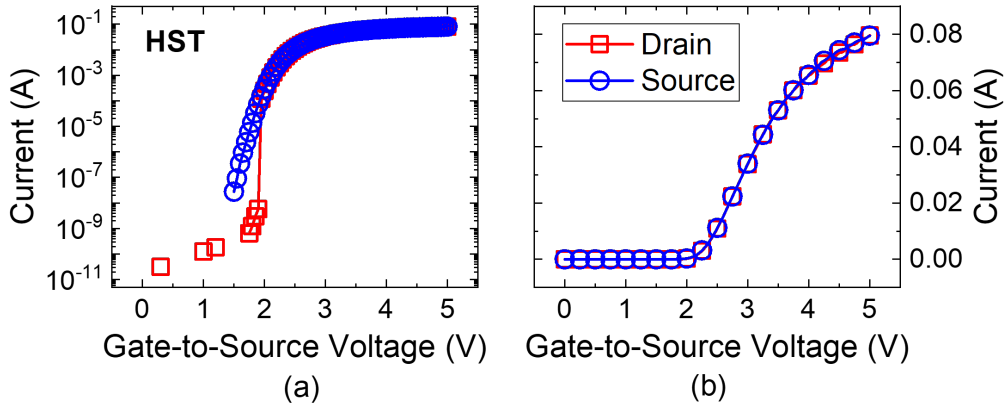

Figure 4.9: Trans-characteristics of high-side transistor performed at $V_{DS} = 1\text{mV}$ considering the source current (in blue) and the drain current (in red) vs gate-to-source voltage in log scale (a) and linear scale (b).

characteristics are not affected by noise from the power converter and the gate current distribution up to $V_{GS} = 1.5\text{V}$ is a behaviour of the analyzed device. In other words, the gate leakage is distributed to the drain and source terminals when the device is off and the SMUs sense negative currents.

Although the adopted monitoring technique in Fig. 4.8 achieves good results, in the following subsections, other configurations are discussed to show the problems, such as leakage current and noise, induced by the power converter.

4.3.1 High-side Transistor Considerations

The HST is placed between the converter's input stage and output filter. The drain terminal is connected to the input capacitor bank, whereas the source is floating. As shown in Fig. 4.9, if the drain terminal is used for sensing the current, the SMU senses the leakage current of the capacitors and, afterwards the device is on, the HST drain current. In other words, there is a lack of information regarding the subthreshold region.

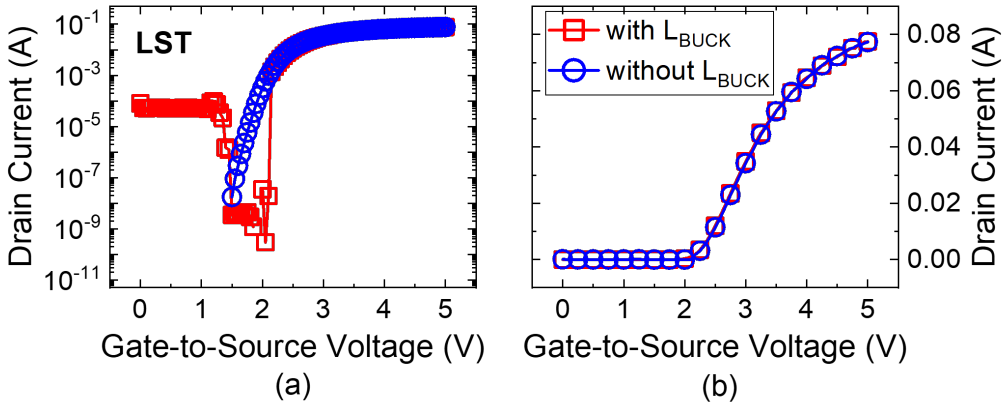

Figure 4.10: Trans-characteristics of low-side transistor performed at V_{DS} = 1mV with (in blue) and without (in red) electromechanical relay, which allows to isolate the DUT from the output inductor. The drain current is reported in log scale (a) and linear scale (b).

4.3.2 Low-side Transistor Considerations

The LST is placed between the output filter and the power ground of the converter. Only the drain terminal could be considered to sense the current to avoid noise and general interference from the ground. Furthermore, the initial design did not include the electromechanical relay to disconnect the output filter and isolate the LST drain. As shown in Fig. 4.10, the presence of the inductor L_{BUCK} tends to disturb the measure, above all in the subthreshold region of the device: i) introducing a leakage current; ii) when the device starts to conduct, the inductor disturbs the measurement until the device is fully ON. Therefore, a relay is required to overcome these problems.

4.4 Example of In-Circuit Setup Operation

To explain how the in-circuit setup works, the I-V characteristics of the high-side transistor are reported within 100ks timeframe and under the following synchronous buck converter operating conditions: V_{IN} = 48V, I_{OUT} = 4A, D = 25%, f_{sw} = 1MHz and T_a = 25 °C. For this analysis, the involved DUTs are 80 V enhancement-mode GaN.

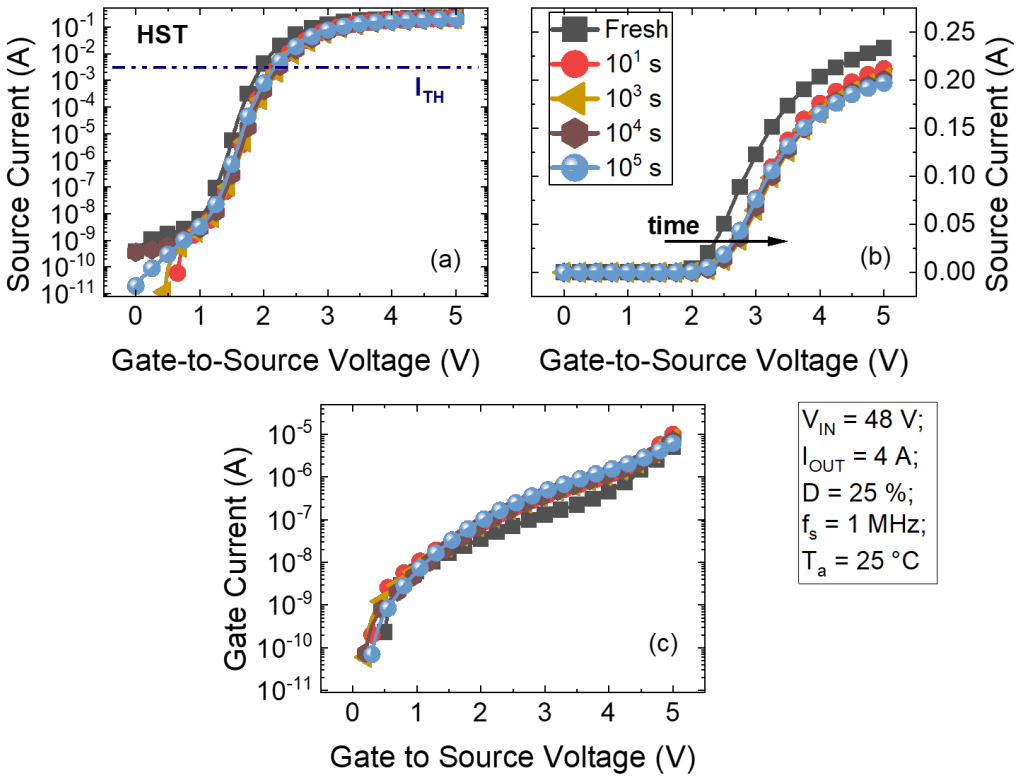

Figure 4.11: Source current (a in log scale, b in linear scale) and gate current (c) versus gate-to-source voltage before, during and after stress carried out by means of the synchronous buck converter. The stress test is performed at V_{IN} = 48V, I_{OUT} = 4A, D = 25%, f_{sw} = 1MHz and T_a = 25 °C.

Fig. 4.11 shows the evolution of the measured HST I-V characteristics at 10s, 100s, 1ks, 10ks and 100ks during the converter-mode operation. It is noticeable: i) a significant initial threshold voltage shift; ii) for a long time, an ON-state resistance R_{ON} increase; iii) the gate current does not seem to be affected by degradation. Further insights will be exhaustively discussed in Chapter 5, but it is evident that the transistors are stressed by the converter.

4.4.1 Extrapolation Methods

From the I-V characteristics is possible to quantify the degradation of the threshold voltage, ON-state resistance and gate leakage current.

Fig. 4.12 shows the threshold voltage shift ΔV_{TH} and ON-state resistance

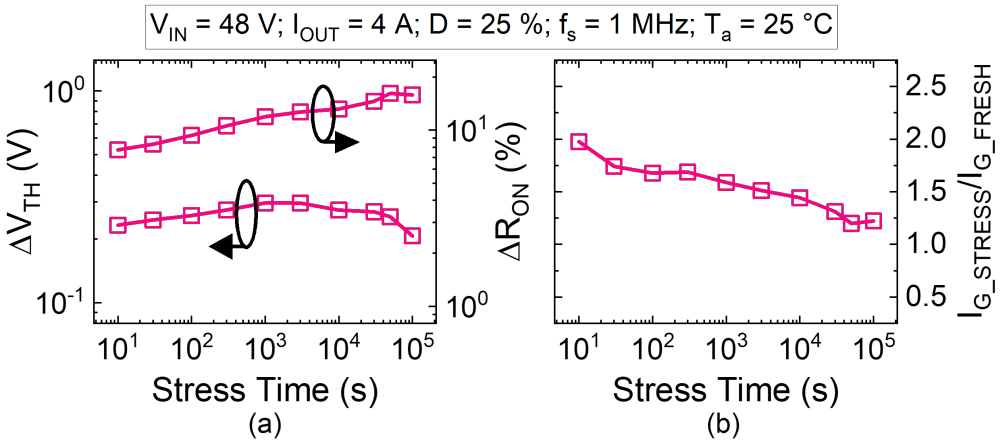

Figure 4.12: Quntifying threshold voltage shift, ON-state resistance degradation and gate leakage current when the synchronous buck converter operates at V_{IN} = 48V, I_{OUT} = 4A, D = 25%, f_{sw} = 1MHz and T_a = 25 °C.

drift ΔR_{ON} and gate leakage current versus the stress time. V_{TH} is calculated with the constant-current method, as the value of V_{GS} corresponds to a 3mA drain current in the linear region with V_{DS} = 5mV [9]. Instead, R_{ON} is evaluated in the linear region at the same given gate overdrive voltage (V_{OV} = V_{GS-ON} – V_{TH}) as the ratio V_{DS} / I_D, decoupling ΔR_{ON} from ΔV_{TH}. Finally, I_G is extracted at V_{GS} = 5V.

As mentioned in Chapter 2, thanks to full I-V characterization, it is possible to exclude a contribution deriving from the drift of V_{TH}. As a matter of fact, Fig. 4.13 shows the difference between the proposed approach and the online one. It is worth remembering that the online monitoring techniques, R_{ON} is evaluated by measuring I_D at a fixed gate voltage (e.g. V_{GS} = 5V), hence including the contribution of both ΔV_{TH} and ΔR_{ON}. As a result, a lower R_{ON} drift can be observed.

4.4.2 Test Repeatability

Other tests with the same converter operating conditions have been carried out in order to figure out the data dispersion concerning the degradation and, in addition, if the setup can reproduce the same realistic stress environment.

Fig. 4.14 reports one of the other stress tests in comparison to the first

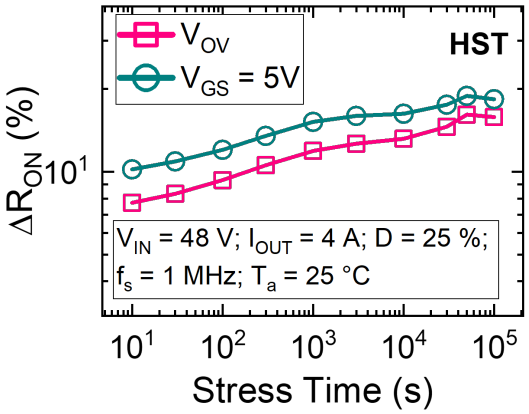

Figure 4.13: Comparison of ON-state resistance degradation evaluated with two different approaches, i.e. proposed approach and likewise online monitoring. The stress test is performed at V_{IN} = 48V, I_{OUT} = 4A, D = 25%, f_{sw} = 1MHz and T_a = 25 °C.

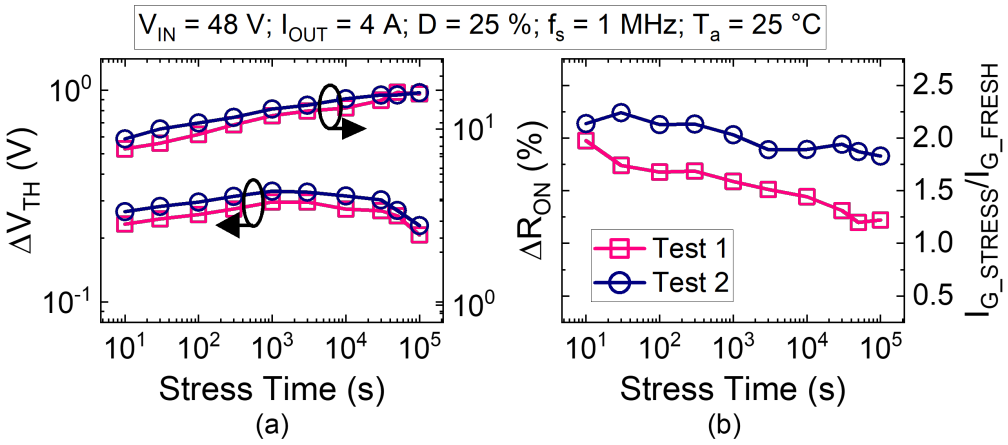

Figure 4.14: Comparison of threshold voltage shift, ON-state resistance degradation and gate leakage current when the synchronous buck converter operates at V_{IN} = 48V, I_{OUT} = 4A, D = 25%, f_{sw} = 1MHz and T_a = 25 °C.

one. The degradation shows a small dispersion among nominally identical devices, suggesting good stability and test reproducibility for the proposed setup and limited dispersion among the adopted devices.

4.4.3 Monitoring of Converter Parameters

The monitoring also concerns the synchronous buck converter. When the setup is set on stress mode, the converter efficiency η and the NTC thermistor resistance are continuously monitored thanks to voltmeters and amperemeters placed at the input and output stage of the converter and an external ohmmeter, respectively. In addition, the measured resistance is converted to temperature by means of the conversion model provided by the thermistor datasheet [10]. Therefore, the thermistor works as a temperature sensor in which an increase/decrease of temperature implies a reduction/increase of its resistance according to its conversion function. Efficiency and temperature are the main parameters to evaluate the health status of a converter, as η indicates the power losses of the converter and estimates the power dissipated by DUTs with the aid of ADS simulations; whereas temperature monitoring checks the operation of the thermal management of the converter and the junction temperature of the DUTs, including the self-heating effect. To estimate the junction temperature of the power devices, an equivalent thermal circuit has been developed that also takes into account TIM and heatsink thermal model as discussed in Chapter 3.

Fig. 4.15 reports η over stress time occurred in two tests with the same operating conditions. Starting from different points, the efficiencies reach the

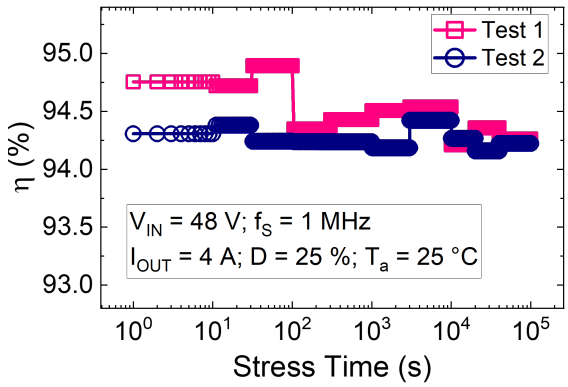

Figure 4.15: Comparison of converter efficiency over stress time. when the synchronous buck converter operates at $V_{IN} = 48$V, $I_{OUT} = 4$A, $D = 25$ %, $f_{sw} = 1$ MHz and $T_a = 25$ ° C.

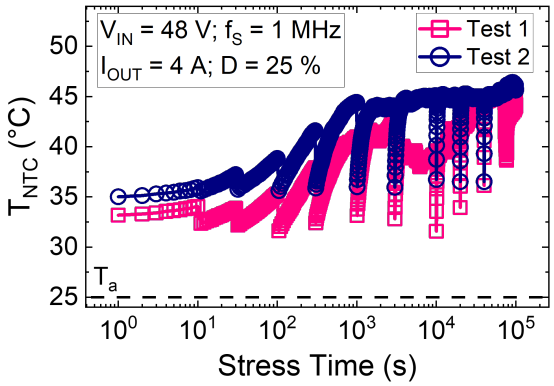

Figure 4.16: Comparison of NTC thermistor temperature when the synchronous buck converter operates at $V_{IN} = 48$ V, $I_{OUT} = 4$ A, $D = 25$ %, $f_{sw} = 1$ MHz and $T_a = 25$ °C.

same value after 100s. The efficiency monitoring is crucial and allows to: i) figure out if the setup reproduces the same operating conditions stressing the DUTs in the same manner; ii) identify a possible link between the degradation of the power devices and the converter performance.

Instead, Fig. 4.16 illustrates the NTC thermistor temperature T_{NTC} monitored during the two stress tests. As shown in Fig. 4.16, NTC temperature reaches a steady state after 300s. In addition, The setup restarts to operate as a converter after a complete characterization of the DUTs, and it takes a few seconds to return to the thermal steady state due to the large thermal capacitance of the heatsink.

4.5 Summary

In this chapter, the operation principle of the in-circuit setup was validated. Synchronous buck converter mode was evaluated in terms of signal integrity - gate voltages and switching voltage were monitored - and efficiency. To estimate the gate-to-source voltages of the devices, the experimental results were supported by ADS co-simulations. Regarding the characterization mode, several techniques were reviewed for high-side and low-side transistors in order to investigate the interferences provided by the power network. Finally, an example of high-side degradation under certain operating in-circuit setup

conditions was reported, highlighting the benefits of the implemented approach and the robustness of the setup.

The next step is to investigate the behaviour of high-side and low-side devices under different operating conditions of the converter.

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Chapter 5

In-Circuit Reliability Analysis

5.1 Introduction

In realistic applications, such as more common soft or hard-switching, transistors are subjected to varied and multiple stresses [1]. Factors like voltage in the OFF-state, current in the ON-state and simultaneous high current and high voltage (semi-ON-state) during the nanoseconds' transitions may significantly accelerate device aging. In addition, the interplay with the circuit layout, gate and power loops, and components, above all inductor, causes voltage overshoot, undershoot and ringing, and may further reduce the device lifetime.

This chapter aims to assess the degradation of high-side and low-side power HEMTs operating under different operating conditions of the synchronous buck converter through the developed setup. In particular, the investigation reports the degradation of full I-V characteristics related to several input voltages, output current, duty cycle, switching frequency and ambient temperature. Moreover, it investigates the importance of good thermal management and different turn-on/off slew rates of the GaN HEMTs' gate control signals from the reliability perspective, providing valuable guidelines for designers to enhance device reliability and optimize converter performance.

5.2 Converter Stressors

When power transistors operate in a synchronous DC-DC buck converter, multiple stress factors may contribute to their aging. In particular, the single device switches from OFF- to ON-state and vice versa, sustaining a high drain voltage V_{IN} and current I_{OUT} during the semi-periods t_{OFF} and t_{ON}, respectively; the duration of such semi-periods depend on the switching frequency (f_{sw}) and duty cycle (D). In addition, the so-called "hard-switching" transition from OFF- to ON-state and vice versa include a third stress phase, i.e., semi-ON-state, in which the device is simultaneously subjected to relatively high V_{DS} and I_D for few nanoseconds. In such a condition, it has been demonstrated that the hot-electrons effect plays a crucial role in device degradation [2].

However, the hard-switching transitions are directly linked to the slew rates of gate-to-source voltage. Indeed, speeding up the transitions of the control signal reduces semi-ON-state periods but, on the other hand, it produces higher voltage overshoot and ringing in the converter that could reduce the device lifetime.

Finally, the device performance strongly depends on its operating junction temperature which affects the switching and conduction losses of the converter, and in turn produces the junction temperature rise, i.e., self-heating phenomena [3]. This thermal runaway may destroy the device and, therefore, the thermal management related to the presence of a heatsink results in an interesting stressor to investigate.

Table 5.1 summarizes the possible acceleration factors and the corresponding stress phases within a buck converter operation cycle.

5.3 Preliminary Reliability Analysis

A preliminary aging analysis under ON- and OFF-state DC stress has been carried out to analyze the device's behaviour from the reliability standpoint and to provide a reference for the in-circuit reliability analysis. The device used for this analysis is a commercial 80 V enhancement-mode GaN HEMT

Stress Factor	Stress Conditions
Voltage (V_{IN})	OFF-state; semi ON-state
Duty cycle (D)	OFF-state; ON-state
Temperature (T_a)	All
Current (I_{OUT})	ON-state; semi ON-state
Switching frequency (f_{sw})	semi ON-state
V_{GS} Transitions	semi ON-state
Thermal Management (Heatsink)	All

Table 5.1: Accelerated stress factors for synchronous buck converter

with a typical R_{ON} of 20 mΩ and typical V_{TH} of 1.6 V. The maximum continuous drain current (I_D) is 6.8 A. For each test, three devices for the high-side and low-side were considered. Testing additional units did not reveal significant differences as observed in thermal management and input voltage cases.

5.3.1 ON-state Test

ON-state DC stress test is performed at 5 V gate-to-source voltage (V_{GS}), maximum DC current value, $I_D = 6.8$ A, and 25 °C ambient temperature T_a for a 70 ks stress time. Under this condition, the devices dissipate 1W and the junction temperature reaches around 44 °C.

As depicted in Fig. 5.1, devices do not show degradation except for a slight V_{TH} drift induced by the gate bias ($\approx$ 0.2 V after 70 ks).

5.3.2 Temperature Dependency

Devices are stressed in OFF-state ($V_{GS} = 0$V) at 64 V drain-to-source voltage (V_{DS}) for 80 ks, and ambient temperature ranging from 40 °C to 150 °C. Instead of ON-state analysis, the OFF-state DC stress returns a drift for both R_{ON} and V_{TH}.

Fig. 5.2 shows the R_{ON} (a) and V_{TH} (b) drift during the stress for different T_a. A non-monotonic temperature dependency is observed for both

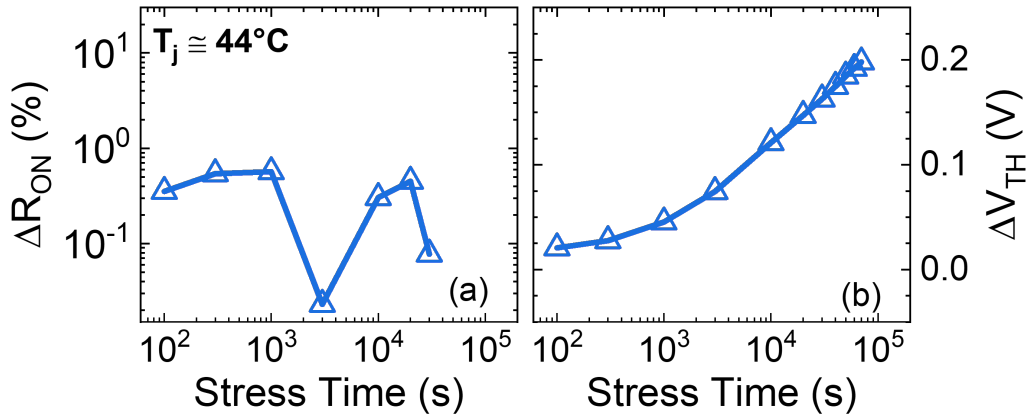

Figure 5.1: R_{ON} (a) and V_{TH} (b) drift under ON-state stress condition (V_{GS} = 5V; I_D = 6.8A and T_a = 25°C).

ΔR_{ON} and ΔV_{TH}. In particular, their drift increases for increasing T_a up to 100 °C, while they decrease for T_a > 100 °C, suggesting the presence of two competing trapping mechanisms. Such behaviour is correlated to the distribution of the drain leakage current during the stress, as reported in Fig. 5.3. It flows mainly through the gate electrode for temperatures below 100 °C, while it provides a larger contribution to the source current at larger T_a values. Unfortunately, further insights cannot be provided due to a lack

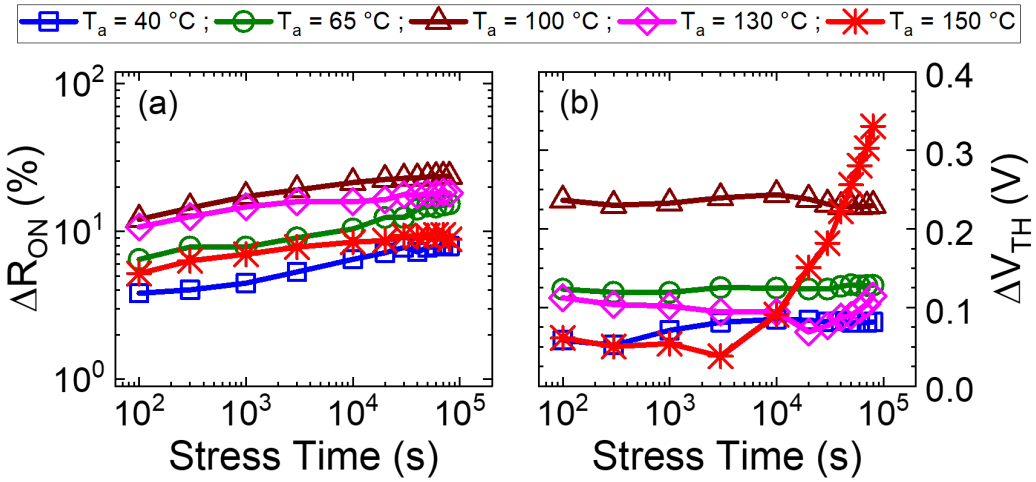

Figure 5.2: R_{ON} (a) and V_{TH} (b) drift under ON-state stress condition (V_{DS} = 64 V; V_{GS} = 0 V) As a function of different ambient temperatures T_a.

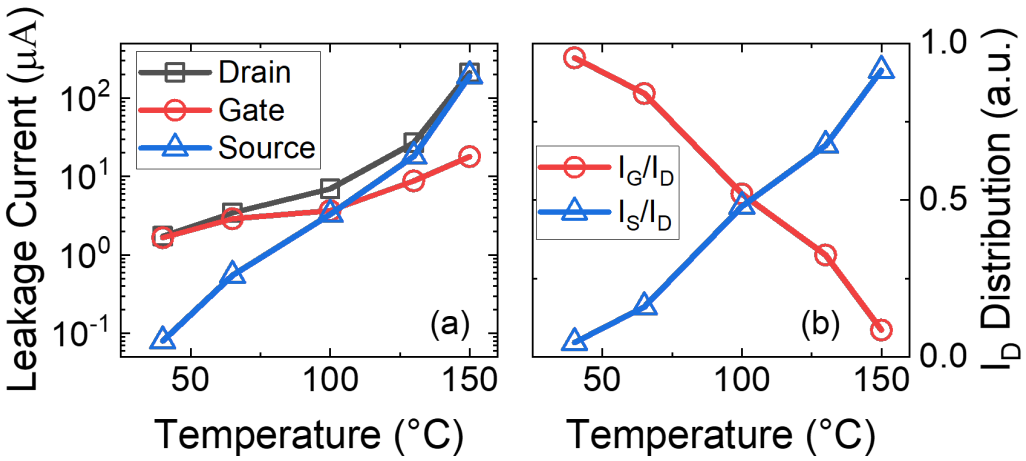

Figure 5.3: Leakage currents under OFF-state stress condition (V_{DS} = 64 V; V_{GS} = 0 V) at various ambient temperatures T_a (a). Gate (I_G) and source (I_S) leakage currents normalized with respect to drain one (I_D) at various ambient temperatures (b).

of information on the device architecture and fabrication process.

Finally, by focusing on the ΔV_{TH} (Fig. 5.2b), a significant drift can be observed after 3 ks for T_a = 150 °C. A similar behaviour seems to occur, at longer stress times, for T_a = 130 °C. In [4], a similar ΔV_{TH} (up to 40 %) has been ascribed to the ionization of out-diffused Mg-related acceptor traps in the AlGaN region, caused by the high electric field induced by large V_{DS}. In our case, such a mechanism seems to show up due to the combined effects of relatively high temperature and electric field.

5.4 Thermal Management

As discussed in chapter 3, in a DC-DC converter, thermal management is required to avoid the thermal runaway of GaN transistors. Because of small packages and the dissipated power induced by the converter application, the intrinsic thermal capability of the devices does not allow to transfer of much heat to the surrounding environment. Therefore, it needs to attach an external heatsink to achieve good thermal performance. Using a heatsink and TIM results in a significantly lower junction-to-case thermal resistance.

This section aims to investigate how thermal management affects the

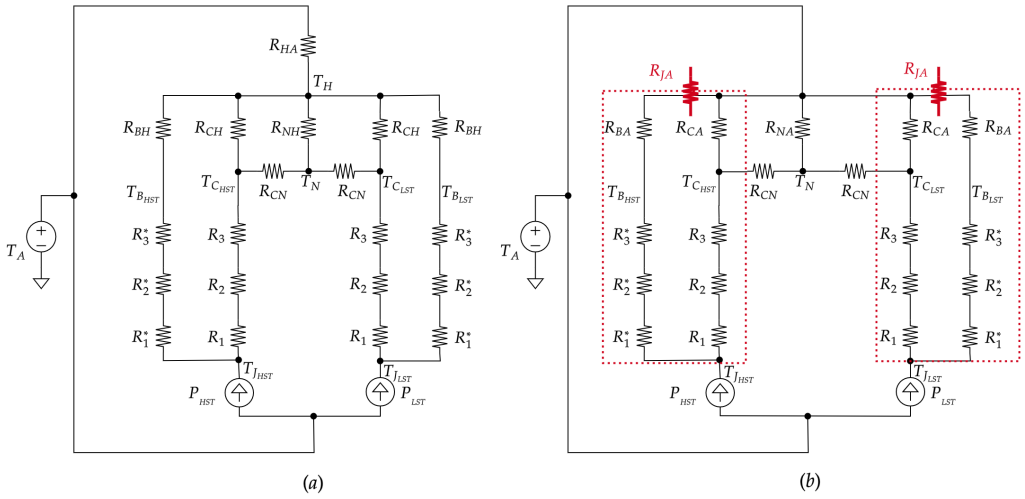

Figure 5.4: Thermal steady-state model of the experimental setup with heatsink (a) and without heatsink (b).

reliability of the device in terms of V_{TH}, R_{ON} and I_G variations.

5.4.1 Stress Conditions

High-side and low-side GaN HEMT operate in a 48/12 V synchronous buck converter at 1 MHz for 100 ks under two different thermal conditions, namely:

- soft stress, where the heat sink is mounted to favour heat removal from the transistors;
- hard stress, where the transistors are exposed directly to the ambient to deliberately let the junction temperature of GaN transistors increase.

Fig. 5.4 depicts the thermal steady-state model of both cases. The equivalent thermal junction to ambient resistance of the hard stress condition is higher in comparison to the soft stress one. In particular, by adding the heatsink the overall junction to the ambient thermal resistance of the single transistor is decreased from 81 °C/W to 18 °C/W (about 77 %). Moreover, the illustrated thermal equivalent circuits have been used for the estimation of the junction temperature of the high-side and low-side GaN HEMT.

Unfortunately, the spice model of the component with the thermal model included was not available and, therefore, LT SPICE simulations [5] have been performed in which the device power losses are calculated by ADS co-simulations and the ambient temperature is known.

Converter operating conditions are performed by setting V_{IN} = 48 V, I_{OUT} = 4 A, D = 25 %, f_{sw} = 1 MHz, and T_a = 25 °C. This type of DC-DC converter plays a relevant role in electric and/or hybrid vehicles, because of its simplicity and high efficiency [6]. Whereas, the degradation effect is monitored by measuring V_{TH}, R_{ON} and I_G from full I-V curves.

5.4.2 Results and Discussion

Fig. 5.5 shows the V_{TH} and I_G drift during soft and hard stress for both HST and LST. First, it can be noted that, during soft stress (normal operation), the two transistors exhibit a different ΔV_{TH} dynamic: a non-monotonic time dependence for HST and a monotonic increasing one for the LST. Such different behaviour is related to the asymmetric stress condition applied to the two GaN HEMTs in DC-DC converters. In particular, from ADS numerical simulations of printed-circuit-board, power dissipation is estimated to be 1.6W and 0.5W for the HST and LST, respectively. Such difference induces a different junction temperature of 60 °C and 40 °C for HST and LST, respectively. Moreover, it is possible to note that the HST gate leakage, in the case of soft stress, starts to increase when the related V_{TH} (Fig. 5.5, (a) and (c)) starts to decrease (1000 s). This is not observed in the case of LST. Concerning the ΔV_{TH} and I_G dynamics of the HST, similar behaviour is reported also in [7] under PBTI stress at the device level, the ΔV_{TH} reduction, occurring at relatively long stress-time, to the gate leakage increase caused by the combined effect of positive gate bias and relatively high temperature. By removing the heat sink (hard stress condition) the junction temperature of the HST exceeds the maximum junction temperature operating rating (150 °C). In this case a larger V_{TH} drift (up to 1 V) is observed, leading to device failure after $\sim$ 25 ks. Also in this case, it is worth noting the larger degradation of the HST, which is the first one to fail.

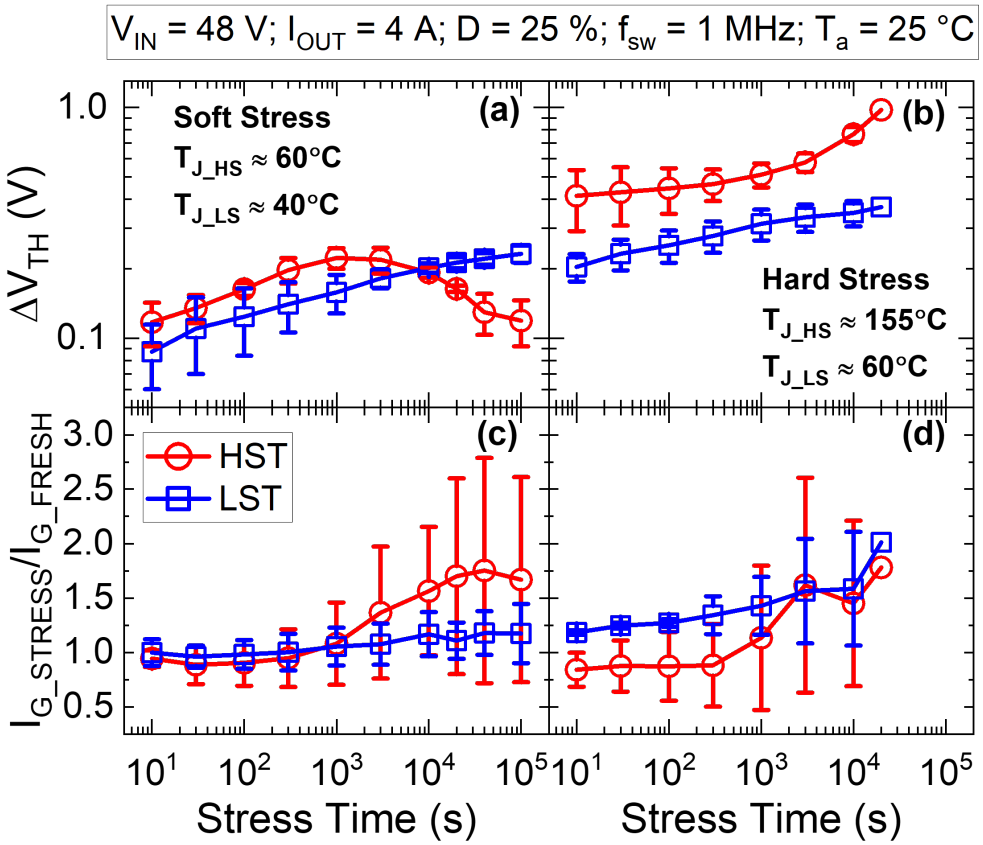

Figure 5.5: Threshold voltage and gate leakage degradation of HST and LST in the case of soft ((a) and (c), respectively) and hard ((b) and (d), respectively) stress. The error bar is the standard deviation σ.

Concerning the ΔR_{ON} (Fig. 5.6), the soft stress induces the same monotonous increase in both transistors up to around 10 ks, after which a saturation effect is observed. Also in this case, the HST exhibits a larger ΔR_{ON}, highlighting the extent of the level of criticality of HST in terms of reliability. In the case of hard stress, ΔR_{ON} exhibits a different trend concerning the soft stress test. In particular, the HST shows a 10% shift after only 10s, whereas the ΔR_{ON} of LST is characterized by a lower starting value and a higher slope, reaching approximately comparable drift at 20 ks, which is of the same magnitude of the hard stress case (HST).

Finally, to monitor the recovery phase, the last characterization is performed after 14 hours of recovery, showing that, parameters drift (V_{TH} and

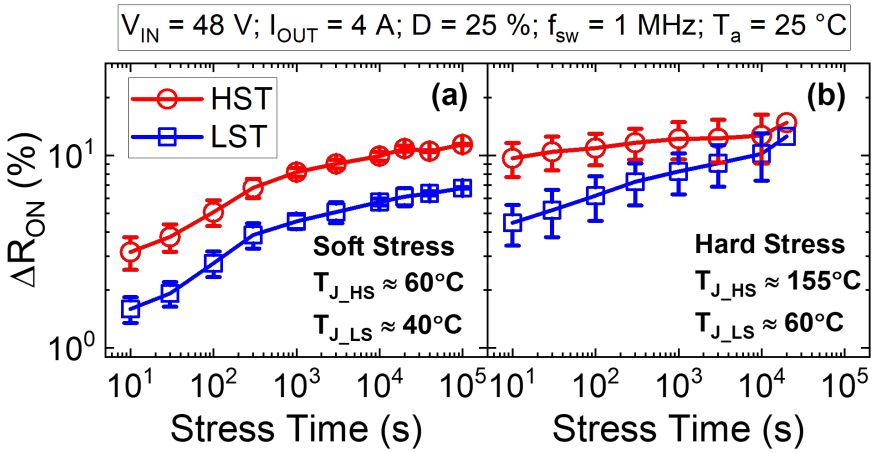

Figure 5.6: ON-state resistance degradation of HST and LST in the case of soft (a) and hard (b) stress. The error bar is the standard deviation σ.

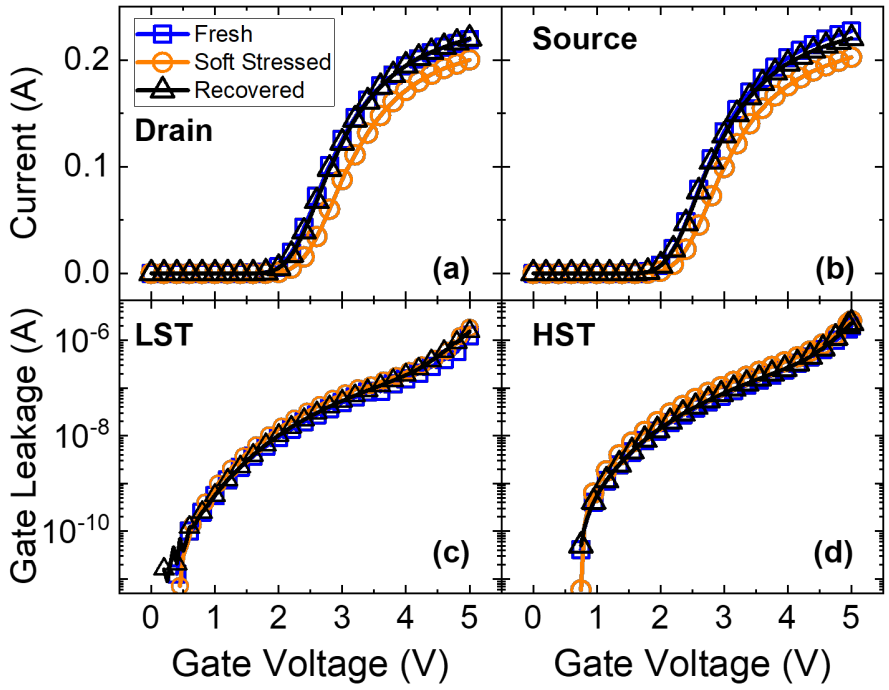

Figure 5.7: Drain current (a) and gate leakage (c) of LST and source current (b) and gate leakage (d) of HST versus gate-to-source voltage (source is connected to the ground) in the case of soft stress conditions. The stressed I-V characterizations are performed at 100 ks, whereas the recovered ones after 14 hours from the stress. For the recovery phase, the converter has been off at $T_a = 25$ °C.

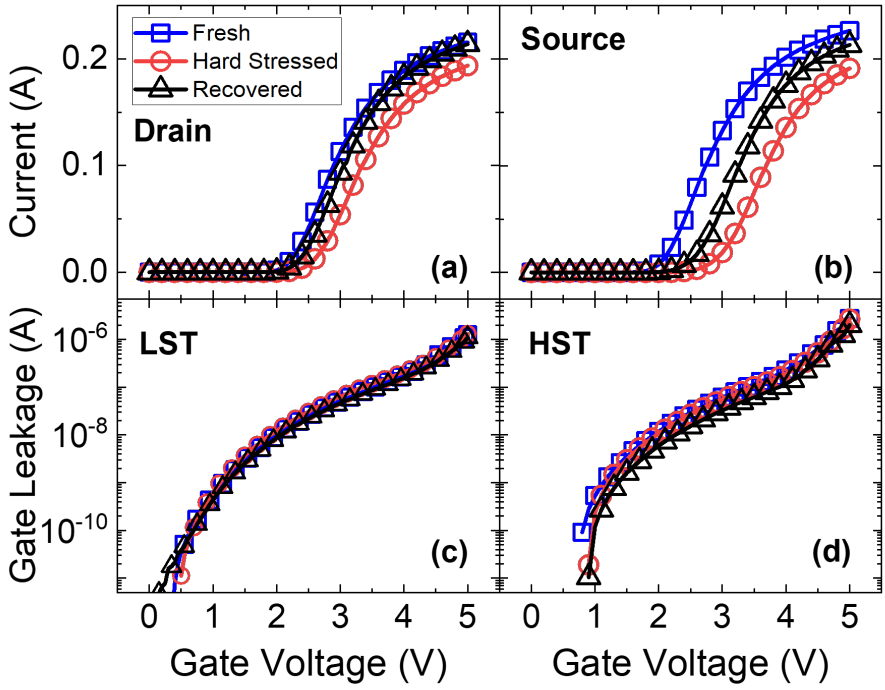

Figure 5.8: Drain current (a) and gate leakage (c) of LST and source current (b) and gate leakage (d) of HST versus gate-to-source voltage (source is connected to the ground) in the case of hard stress conditions. The stressed I-V characterizations are performed at 20 ks, whereas the recovered ones after 90 hours from the stress. For the recovery phase, the converter has been off at $T_a = 25$ °C.

R_{ON}) observed after soft stress are completely recoverable (Fig. 5.7), suggesting trapping mechanisms in pre-existing defects. A different picture is observed after 90 hours from the hard stress condition, where LST is recovered whereas, in the HST, a permanent degradation persists, ascribed to the creation of new deep defects (Fig. 5.8).

Overall, from the reported testbed analysis, it is possible to recognize that a limited dispersion of the results obtained from experiments carried out on different nominally identical devices allows for to identification of repeatable degradation trends, such as: i) HST is more prone to degradation because of the larger stress intrinsically induced by the DC-DC Buck converter; ii) a significant V_{TH} shift, indicating gate degradation, occurs. It is markedly larger in the case of hard stress; iii) the noticeable differences in ΔV_{TH} and

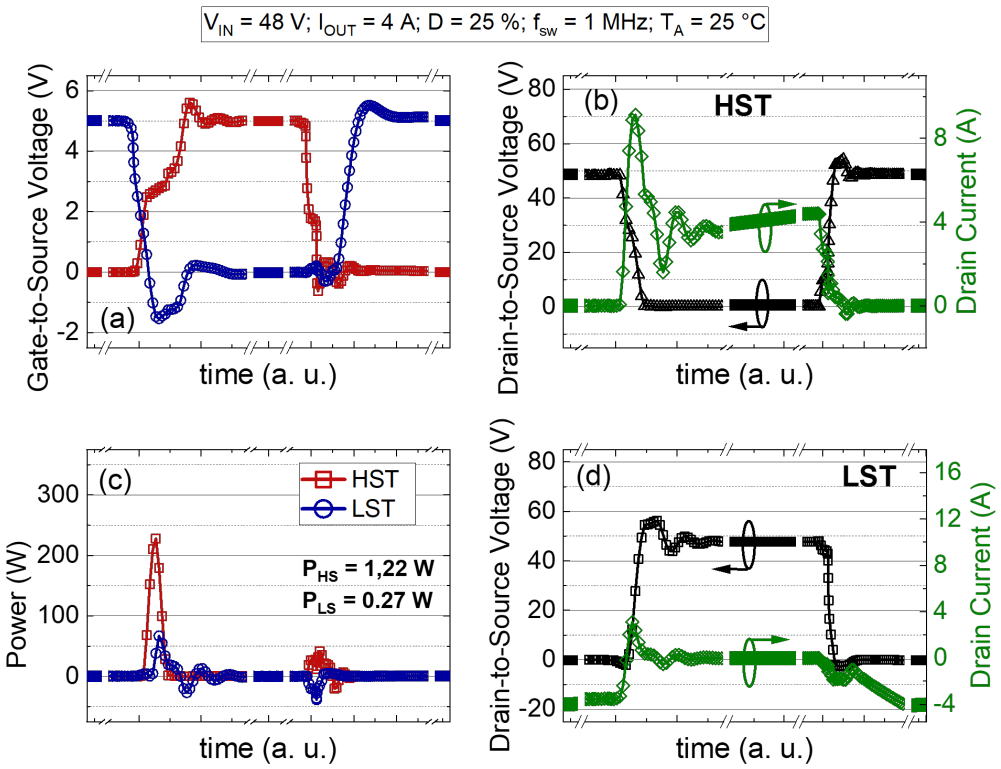

Figure 5.9: Simulated waveforms at the transistors' terminals in the case of V_{IN} = 48 V, I_{OUT} = 4 A, D = 25 %, f_{sw} = 1 MHz, T_a = 25 °C. HST and LST (a) V_{GS} and (c) power dissipation; V_{DS} and I_D in the case of (b) HST and (d) LST.

ΔR_{ON} after soft and hard stress, suggest that the premature device failure may be ascribed to gate breakdown.

HST vs LST degradation

A synchronous buck converter induces asymmetrical stress to the DUTs in terms of applied voltage, current and temperature.

Fig. 5.9 depicts the simulated V_{GS}, V_{DS}, I_D and power dissipation of the HST and the LST operating with V_{IN} = 48 V, I_{OUT} = 4 A, D = 25 %, f_{sw} = 1 MHz, and T_a = 25 °C. It is worth noticing that deadtime external gate series resistors and gate-to-source capacitor have been set and adopted to prevent shoot-through phenomenon, maximize converter efficiency and improve the signal integrity. However, it can be observed how the HST is

subjected to a large switching power loss during its turn-on, making switching losses dominant. On the contrary, they are negligible in the LST where the conduction losses are the dominant ones. HST switching losses and LST conduction losses account for ∼52% and ∼11% of the whole system losses, respectively. As a consequence, the HST is more subjected to hard-switching stress compared to LST, showing up, as reported from here on, a larger ΔR_{ON}.

5.5 Gate-to-Source Voltage Slew Rates

GaN HEMTs allow to rise the operating switching frequency, achieving 1 MHz and beyond. However, as mentioned in chapter 3, the layout parasitics could induce dangerous voltage ringing and overshoot, which could jeopardise the reliability of the device. In order to reduce these effects, the simplest strategy is slowing down the transition time of GaN HEMTs gates by increasing values of external gate resistances, avoiding the employment of a passive snubber circuit. On the one hand, higher gate resistances improve the signal integrity ensuring the safe operating area of power devices. On the other hand, this increases the switching power dissipated by transistors, with a consequent reduction of the converter efficiency and possible enhancement of thermally activated degradation mechanisms. This section discusses a degradation analysis performed at two different turn-on/off slew rates of the GaN HEMTs' gate control signals in order to compare the maximum signal integrity case to the maximum efficiency one.

5.5.1 Configurations of External Gate Resistance

The rise and fall times of gate to source voltage of the transistors are varied by considering two sets of the external gate series resistance, denoted as follows:

- slow configuration, where higher external gate series resistances reduce the switching voltage overshoot to less than 5%, avoid possible additional stress induced by signal degradation

Configuration	$R_{g_{HS-high}}$ [Ω]	$R_{g_{HS-low}}$ [Ω]	$R_{g_{LS-high}}$ [Ω]	$R_{g_{LS-low}}$ [Ω]
Slow	12	15	3.3	4.3
Fast	4.3	3.3	2.2	2.2

Table 5.2: Adopted external series gate resistance sets for slow and fast configuration.

- fast configuration, where lower resistance values accelerate the speed of GaN HEMTs, leading to larger voltage overshoots.

About Fig. 3.4, Table 5.2 reports the two gate resistance sets used to obtain the two stress configurations.

Fig. 5.10 illustrates the efficiency curve in the case of FAST and SLOW configurations. To maximize the efficiency values, the dead time has been tuned for each output current and each configuration. As expected, by reducing the switching times of the transistors, namely the overlap time of LST and HST conduction, efficiency increases (up to almost 95%). It is worth noting that the adopted overlap time influences both the peak value of the efficiency curve as well as the output current corresponding to the peak. The efficiency peak occurs at 2.5 A in the SLOW case, and at 4 A in the FAST

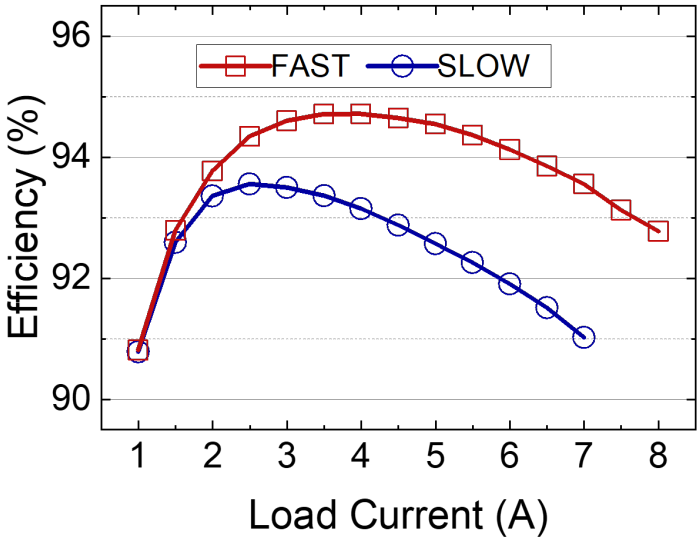

Figure 5.10: Efficiency curves of the synchronous buck converter circuit obtained in the case of FAST and SLOW configuration (see Table 5.2).

case.

A reliability analysis about the impact of the signal integrity on the GaN HEMTs degradation is carried out by fixing the output current at 3.5 A with $V_{IN} = 48$ V, $D = 25$ %, $f_{sw} = 1$ MHz, and $T_a = 25$ °C.

Fig. 5.11 presents the stress voltage signals captured by the oscilloscope during the test. It is clear how the fast configuration allows to reduce the time of transitions. For the switching voltage, dV/dt increases from 4.5 to 6.5 V/ns for the rise and from 4.2 to 7.8 V/ns for the fall. As an effect of speeding up the transitions, the transistors are more stressed by signals due to the higher amplitude of overshoot and undershoot and the larger voltage ringing.

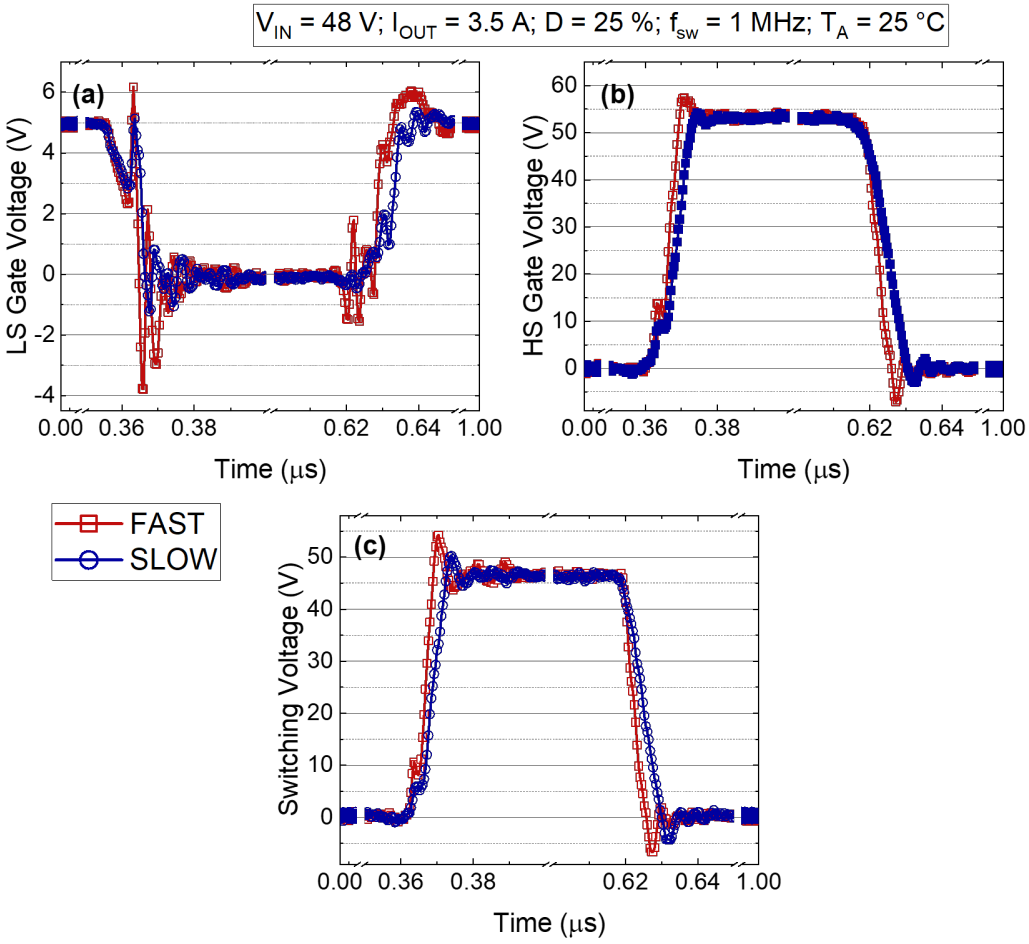

Figure 5.11: LS Gate (a), HS Gate (b) and switching (c) voltage waveforms of the synchronous buck converter measured in the case of FAST and SLOW circuital configurations.

In particular, the overshoot of the switching voltage increases up to 10% compared to the SLOW case. The proposed scenarios aim to set up realistic operating stress conditions induced by a synchronous buck converter and how these additional voltage overshoots could affect the ON-state resistance to the threshold voltage of GaN HEMTs, providing significant insights to PCB designers.

Fig. 5.12 reports the gate-to-source voltage and the power of HST and LST attained using the ADS simulator. The results are consistent with the captured waveforms. The slow configuration avoids any voltage overshoots in comparison to the fast one in which HS V_{GS} reaches quite 6 V, the upper limit of the device. However, it increases the charging and discharging time of the

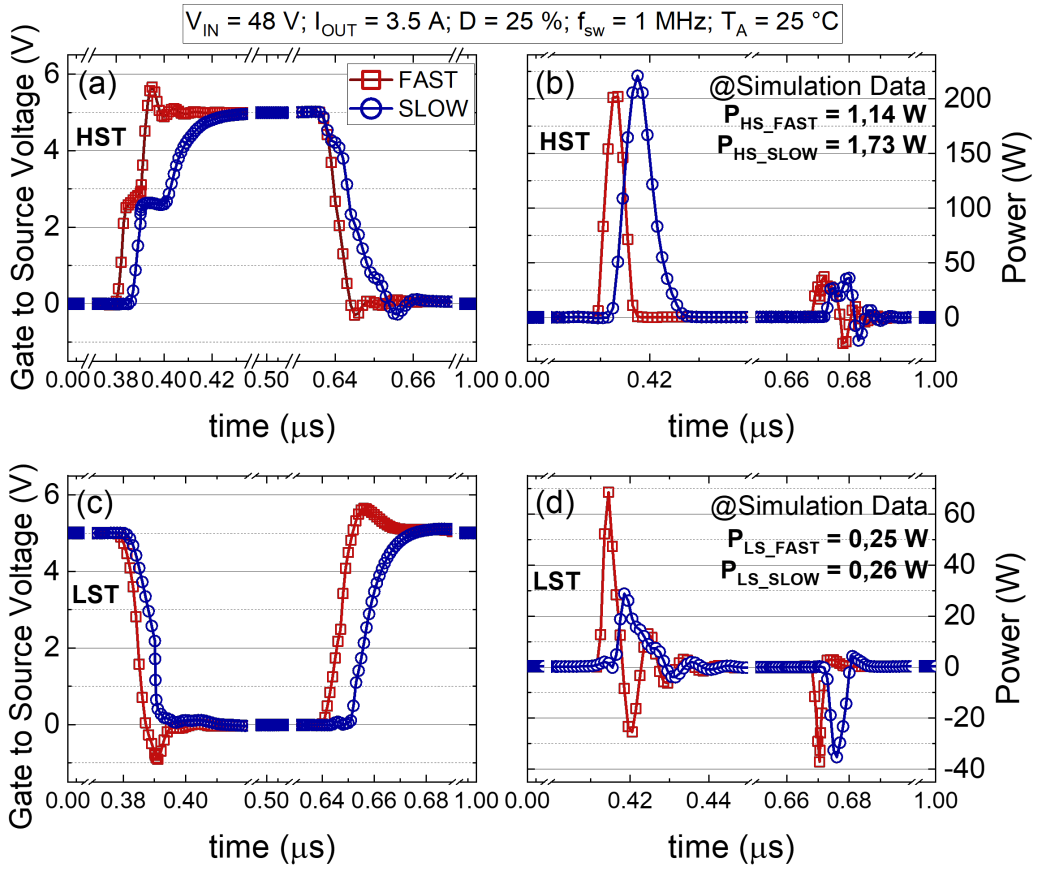

Figure 5.12: ADS simulation of Gate-to-Source Voltage and Power for HST ((a) and (b), respectively) and LST ((C) and (d), respectively) under FAST and SLOW circuital configurations.

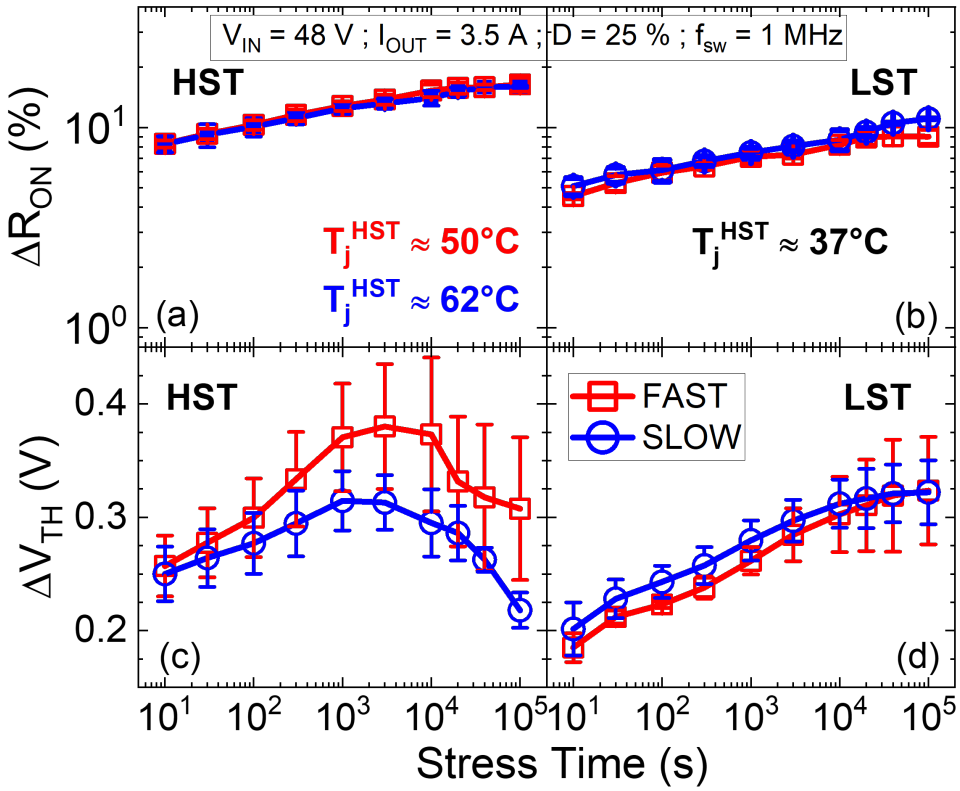

Figure 5.13: R_{ON} and V_{TH} drift in the case of HST ((a) and (c), respectively) and LST ((b) and (d), respectively) under FAST and SLOW circuital configuration. The error bar is the standard deviation σ.

input capacitances and, consequently, the dissipated power. The simulation data return an increase of dissipated power in HST due to a higher current peak in the turn-on phase.

5.5.2 Results and Discussion

Fig. 5.13 reports the effective degradation of R_{ON} for HST (a) and LST (b).

It is evident that, for a long stress time, FAST and SLOW stress conditions tend to converge at the same degradation value. The additional overshoots do not affect the R_{ON} degradation. Therefore, the electron trapping mechanism occurring mainly in the critical high-field region near the drain contact causes slight recoverable R_{ON} shift considering overvoltage up

to 150% of the device max rated voltage [8]. Additionally, a comparison of V_{TH} drift for HST (top) and LST (bottom) is shown. High-side V_{TH} exhibits a non-monotonous evolution over time, whereas the low-side V_{TH} monotonically increases, as already identified in 5.4.2. However, the FAST condition leads to more degradation on the LST transistor causing an upward shift of the curve due to the trapping of the impact ionization-generated holes [9]. Moreover, no noticeable changes are observed in gate leakage. Finally, as already demonstrated in 5.4.2, the analyzed devices are subjected to temporary degradation due to pre-existing defects. As a matter of fact, after a recovery time, the shifts of observed parameters are completely recovered.

Overall, no significant difference in terms of degradation between the two analyzed stress cases is observed. This potentially represents a valuable indication for power electronics circuit designers, since the speeding up of the turn-on and turn-off times has an impact on the circuit efficiency without significantly altering the devices' reliability.

5.6 Ambient Temperature Dependency

A temperature-dependent in-circuit analysis has been carried out to make a first rough comparison with the results of OFF-state DC stress (Fig. 5.2). It is worth noticing that, although the same OFF-state voltage level (V_{IN} = 64 V) has been adopted, 100 ks of converter stress time corresponds to 75 ks and 25 ks of cumulative t_{OFF} for HST and LST, respectively. Moreover, the DUTs can be subjected to additional simultaneous stress factors, e.g. hard-switching. T_a has been varied from 25 °C to 70 °C by means of a laboratory oven, which corresponds to an estimated HST junction temperature (T_J) between 58 °C and 103 °C, respectively. Finally, I_{OUT}, f_{sw} and D were fixed at 3.5 A, 1 MHz and 25 %, respectively, ensuring the operation of the power transistors within their safe operating area (SOA). In addition, the thermal management is further improved by using a fan to reduce the thermal case-to-ambient resistance, accelerating the thermal transient in each stress condition related to the standard converter parameter.

The parameter drift is evaluated concerning their respective values mea-

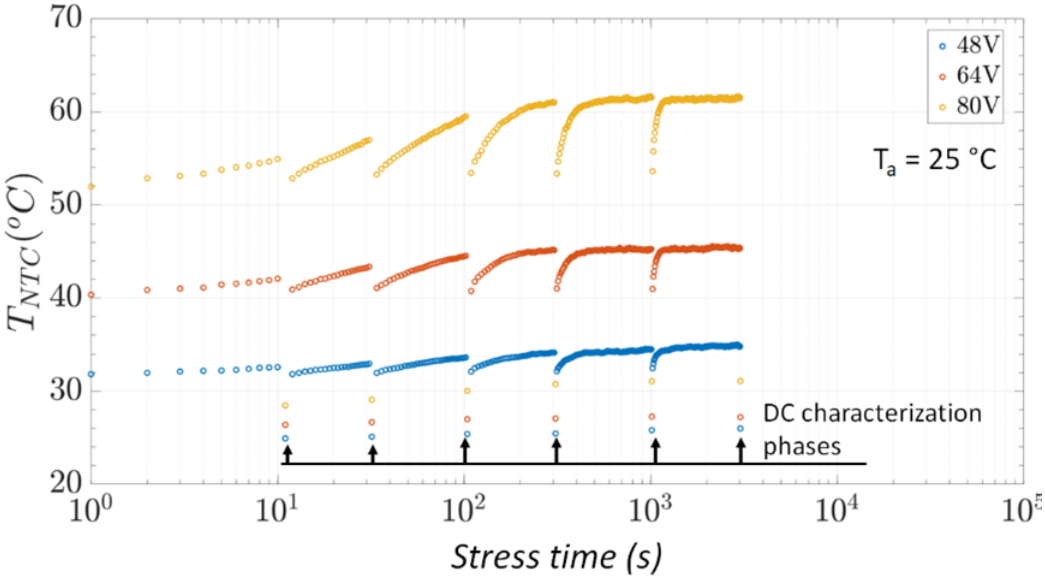

Figure 5.14: T_{NTC} during the stress time while the devices operate in the buck converter under different input voltages.

sured after 100 s of converter operation to: i) reach a thermal steady-state condition; and ii) focus mainly on the long-term/permanent degradation, since, as reported in the previous sections, the drift occurring during the initial stage of the test is fully recoverable with the heatsink.

The normalization of the degradation at 100 s is mainly needed for thermal reasons. In particular, the whole system needs about 100 s to reach a thermal steady state (see figure 5.14 in which T_{NTC} has been monitored for 3 ks with different input voltages) due to the large thermal capacitance of the heatsink. For shorter times the temperature increases while it is quite stable for longer stress time. As a result, for the first seconds, the temperature is not kept constant, its transient depends on the stress condition, and a comparison between different stress conditions is not possible/accurate.

5.6.1 Results and Discussion

Fig. 5.15 reports the related R_{ON} (top) and V_{TH} (bottom) drift, as a function of T_a, in the case of HST (left) and LST (right). It is possible to note that the ΔR_{ON} does not show T-dependency either on HST (a) or on LST

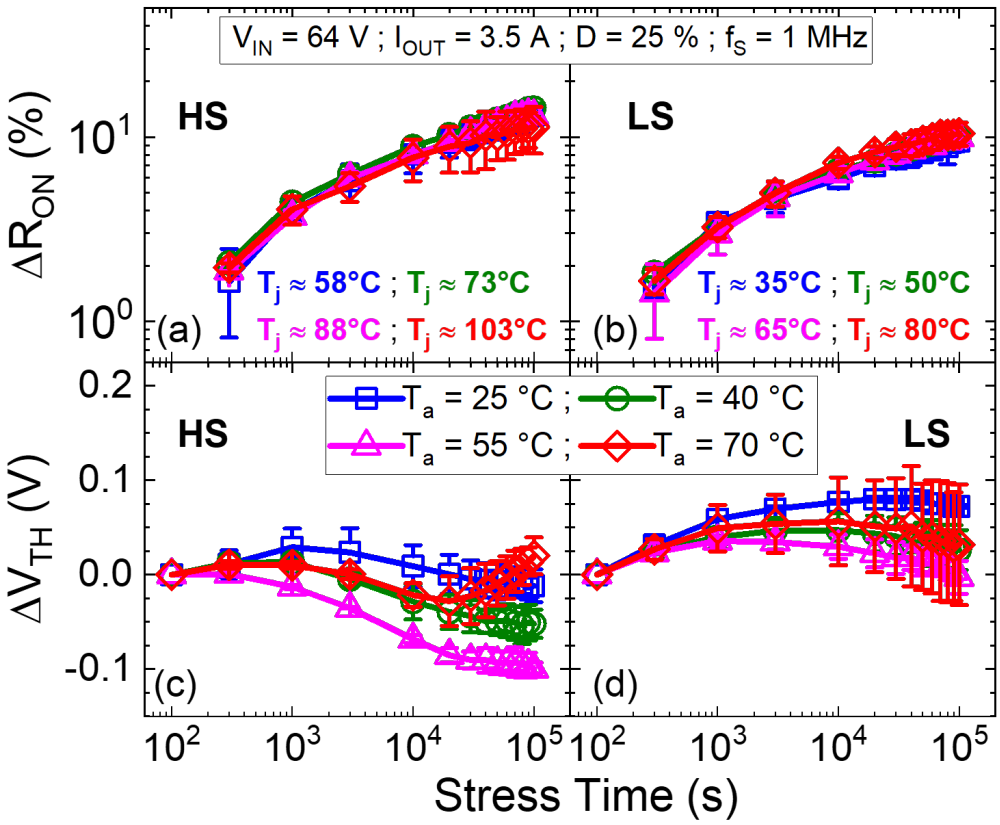

Figure 5.15: R_{ON} and V_{TH} drift in the case of HST ((a) and (c), respectively) and LST ((b) and (d), respectively) during the stress time while the devices operate in the buck converter under different ambient temperatures (T_a). T_J denotes the estimated junction temperature.

(b), highlighting a significant difference concerning the DC-stress case. As already anticipated, the power transistor operating in a switching circuit is subjected to different stress factors. By focusing on the R_{ON} drift, the role of the ON-state stress (high I_D) can be excluded as no aging has been observed in the case of DC stress, although a higher ID has been adopted. As a result, it is possible to conclude that the ΔR_{ON} reported in Fig. 5.15a and 5.15b are due to the combined effect of OFF- and semi ON-state related degradation mechanisms. The latter, as reported in [2], is dominated by hot-electron effects, which, having a negative T-dependence, can compensate for the positive one observed in the case of OFF-state DC stress (Fig. 5.2a, up

to 100 °C).

Concerning the ΔV_{TH}, both HST (5.15c) and LST (5.15d) show a similar T-dependency, which is different from the one observed in the case of OFF-state DC stress under a wider T_a range. It decreases up to T_a = 55 °C, then it starts to increase for higher T_a. Moreover, V_{TH} seems to show the start of a significant positive drift in the case of HST stressed with T_a = 70 °C, probably triggered by the relatively high junction temperature, i.e. $\sim$ 103 °C. Unlike the OFF-state DC stress, here the gate stack can be site of competing trapping mechanisms induced by positive gate bias (ON-state), high drain voltage (OFF-state) and a combination of both including relatively high I_D (semi-ON-state). Overall, by considering the DC-stress analysis and the in-circuit one, it is clear that the temperature is an accelerating factor for the V_{TH} degradation, while ΔR_{ON} is almost T-independent in the case of in-circuit stress.

5.7 Input Voltage and Duty Dependency

To investigate the role of the converter input voltage, three different biases have been adopted, i.e. 48 V, 64 V and 80 V, while keeping fixed f_{sw} = 1 MHz, I_{OUT} = 3.5 A, D = 25 % and T_a = 25 °C.

5.7.1 Results and Discussion

By observing Fig. 5.16, it is possible to note that ΔR_{ON} increases with V_{IN} only in the HST case (Fig. 5.16a), although both transistors are subjected to the same OFF-state voltage (V_{IN}). This behavior may be correlated to two factors: i) longer t_{OFF} values, since HST sustains an OFF-state voltage for 75 % of the switching period, against 25 % in the LST case; ii) hard switching (semi ON-state), which primarily impacts the HST as shown in the previous sections and confirmed by the higher T_J caused by self-heating effects (Fig. 5.16).

The role of t_{OFF} can be excluded by observing Fig.5.18a and 5.18b, reporting ΔR_{ON} in the case of in-circuit tests performed with different duty

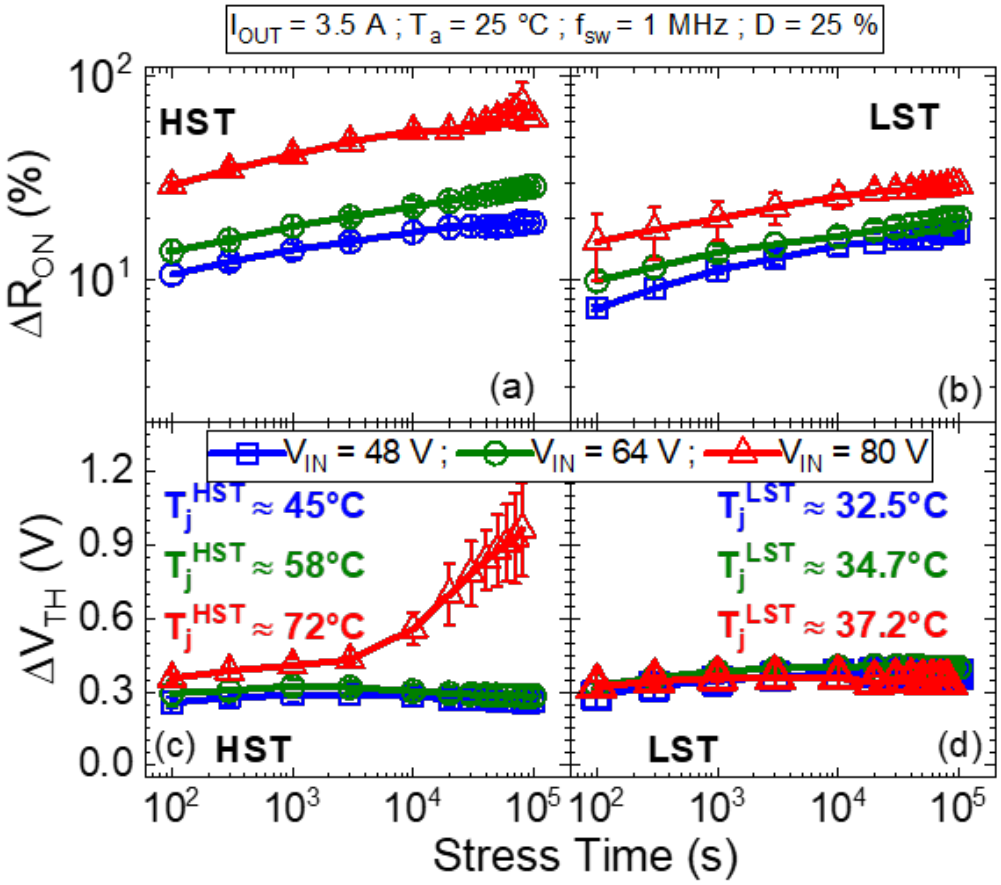

Figure 5.16: R_{ON} and V_{TH} drift in the case of HST ((a) and (c), respectively) and LST ((b) and (d), respectively) during the stress time while the devices operate in the buck converter under different input voltages (V_{IN}). The error bar is the standard deviation σ. T_J denotes the estimated junction temperature.

cycles, i.e., 25 %, 50 % and 75 %, for the HST and LST. Both transistors do not show the expected t_{OFF}-dependency, on the contrary, the ΔR_{ON} of the HST (Fig. 13a) is slightly reduced in the case of longer t_{OFF} (smaller D). As a result, the relationship between ΔR_{ON} and V_{IN} observed in the case of HST (Fig. 5.16a) can be mainly ascribed to the hard-switching stress, which is enhanced by increasing V_{IN}. The latter induces an increase of the longitudinal electric field in the drain-to-gate access region, amplifying the hot-electron-related degradation mechanisms, causing a larger ΔR_{ON}.

By focusing on ΔV_{TH}, on one hand, it is possible to note that the sole increase of drain voltage (V_{IN}) does not lead to relevant ΔV_{TH}, as reported

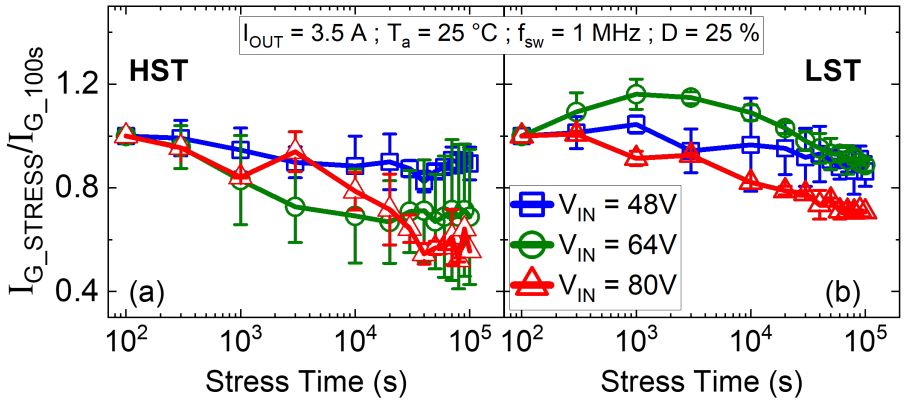

Figure 5.17: I_G variation of HST (a) and LST (b) during the stress time while the devices operate in the buck converter under several input voltage conditions. I_G has been monitored at V_{GS} = 5 V. The error bar is the standard deviation σ.

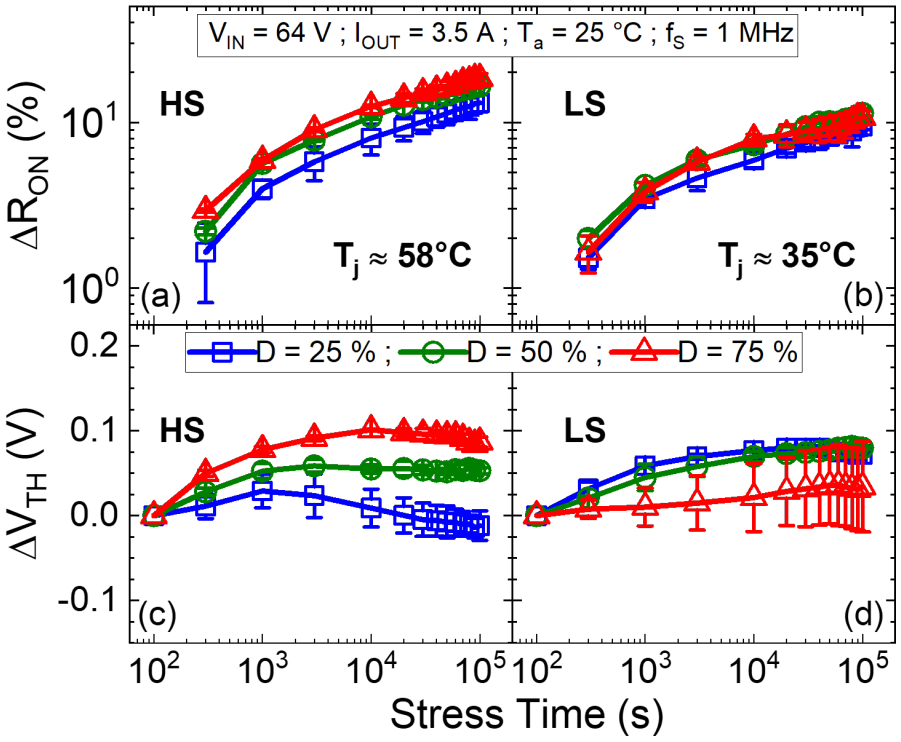

Figure 5.18: R_{ON} and V_{TH} drift in the case of HST ((a) and (c), respectively) and LST ((b) and (d), respectively) during the stress time while the devices operate in the buck converter under different duty cycles D. The error bar is the standard deviation σ. T_J denotes the estimated junction temperature.

in Fig. 5.16 d. On the other hand, the combination of relatively high V_{DS} and T produces a relevant V_{TH} degradation (Fig. 5.16 c). The latter has not a clear impact on the gate leakage as shown in Fig. 5.17, suggesting that: i) ΔV_{TH} is not caused by a possible degradation of the metal/p-GaN Schottky junction, i.e., the reverse-biased junction determining I_G at $V_{GS} = 5$ V; ii) ΔV_{TH} is ascribed, as in the case of DC stress (section 5.3), to the ionization of out-diffused Mg-related acceptor traps in the AlGaN region, caused by the combination of high temperature and electric field induced by large V_{DS} (V_{IN}).

Overall, by considering the results reported so far, the higher V_{DS}, the lower T (and vice versa) needed to induce an uncontrolled positive V_{TH} drift. By limiting both V_{DS} and T as in the case of Fig. 5.18, ΔV_{TH} is relatively small. In such a case, this small drift seems to be associated with ON-state degradation, i.e., gate-bias stress, since ΔV_{TH} increases with D, hence with t_{ON}, the time interval during which the gate is positively biased.

Moreover, as previously shown, the R_{ON} and V_{TH} drift induced in the first seconds of converter operation is fully recoverable, since they are induced by charge trapping/detrapping in pre-existing defects. By normalizing concerning 100 s, we only focus on the permanent/slow recoverable degradation, hence on the long-term reliability. Overall, as for the previous comment, by normalizing with respect to the fresh condition the result does not change, except for an initially different amount of drift, as can be observed in the figure 5.16.

5.8 Output Current Investigation

In order to analyze the role of the converter's output current on the GaN HEMTs reliability, a further test has been carried out by setting $I_{OUT} = 7$ A and $V_{IN} = 32$ V. The input voltage has been reduced to maintain the same duty cycle and output power of the reference case ($V_{IN} = 64$ V, D = 25 %, $i_{OUT} = 3.5$ A and $P_{OUT} = 56$ W). The experimental results are plotted in Fig. 5.19. It is clear that the increase of I_{OUT} while reducing V_{IN} results in a greater robustness for both HST and LST. In particular, both transistors

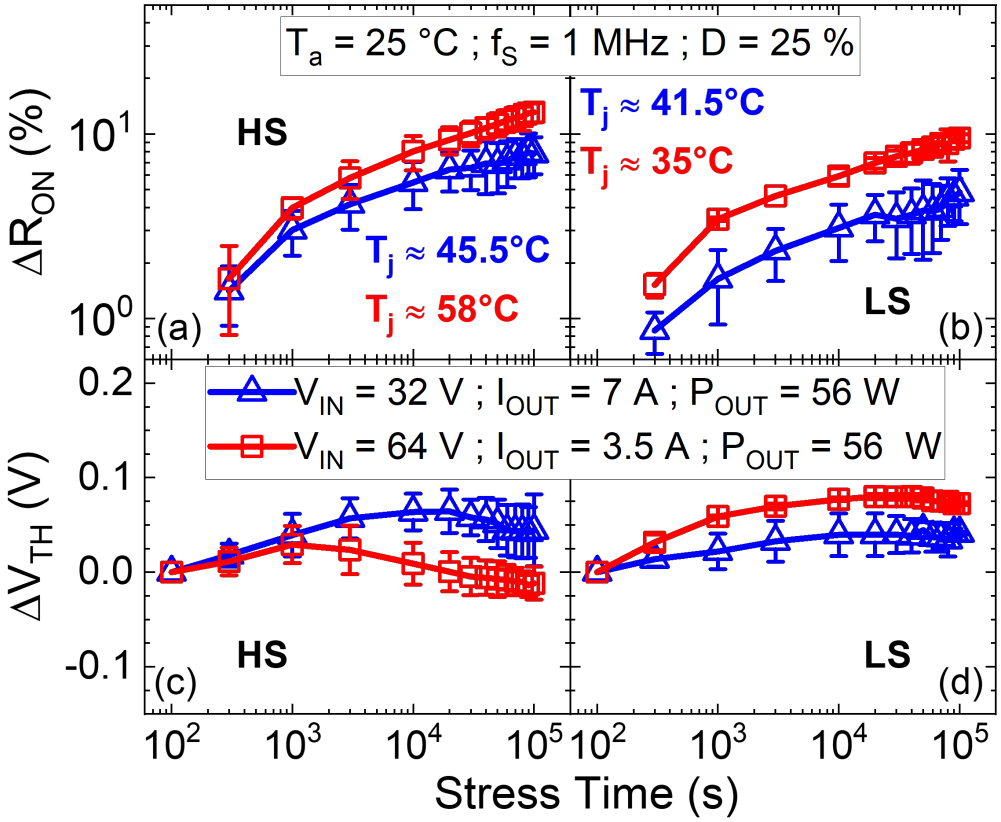

Figure 5.19: R_{ON} and V_{TH} drift in the case of HST ((a) and (c), respectively) and LST ((b) and (d), respectively) during the stress time while the devices operate in the buck converter at the same output power but with different input voltage and output current. The error bar is the standard deviation σ. T_J denotes the estimated junction temperature.

show a higher ΔR_{ON} in the case of higher V_{IN}, in spite of the lower I_{OUT} (i.e. I_D in ON-state), confirming: i) the negligible role played by the ON-state current; ii) the significant impact of the OFF-state voltage on the transistor degradation. Finally, V_{TH} do not exhibit a significant shift, as T is relatively low.

5.9 Summary

In this chapter, a long-term reliability analysis of commercial e-mode GaN-HEMTs was performed under several operating conditions of the DC-DC

converter, investigating the importance of heatsink, the role of gate-to-source voltage slew rate, input voltage, ambient temperature, duty cycle and output current.

The synchronous buck converter intrinsically induced an asymmetrical stress that led to the high-side transistor being more prone to degradation compared to the low-side one. In addition, when the transistors operated under different thermal conditions related to the presence of heatsink they showed a different ΔV_{TH} dynamic, suggesting that different degradation mechanisms are involved; and, although the significant ΔR_{ON}, the gate stack seems to be the device region responsible for device failure under hard stress condition, supported by large ΔV_{TH} and gate leakage drift.

Moreover, GaN-HEMTs were monitored under two different slew rate stress conditions, namely SLOW and FAST. Preliminary results displayed a clear impact of the signal integrity of the converter on the device reliability, while a larger degradation emerged in the case of the high-side transistor. Overall, no critical issues showed up concerning the analyzed devices.

Finally, in contrast to a preliminary DC-stress analysis, the in-circuit-related results reported that ambient temperature does not affect the degradation of R_{ON}, whereas it plays an appreciable role in the V_{TH} shift. A significant correlation was found between the input voltage of the converter and device reliability. In particular, a larger R_{ON} shift and a significant positive VTH drift of the high-side transistor were observed by increasing the input voltage, likely due to the combination of a high electric field and high junction temperature. The role of V_{IN} was mainly related to hard-switching stress rather than the OFF-state one. Finally, the duty cycle depicted a role only on V_{TH} shift, i.e. larger by increasing D (longer t_{ON}), whereas the output current did not significantly affect the device degradation, except for the indirect one related to self-heating.

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Chapter 6

Conclusions

The era of Gallium Nitride (GaN) has indeed started. GaN-based systems offer substantial advantages, including higher efficiency, and significantly reduced size and weight at low cost compared to the silicon counterparts. However, the widespread adoption of this technology is intricately tied to its reliability, ensuring prolonged system lifetimes. GaN power devices, in particular GaN HEMTs, are affected by well-known issues in the literature, such as current collapse and threshold voltage instability.

The objective of this thesis was the development of a novel in-circuit degradation analysis aimed at assessing the long-term reliability of GaN HEMTs. The analysis is performed through the measure-stress-measure technique. In particular, the devices under test operate in a high-speed and -efficiency synchronous buck converter and, at prefixed times, are characterized by full I-V measurements. In this way, the stress exhibits a more realistic profile than a wafer-level test by including the interactions with parasitic elements as well as cumulative self-heating and mechanical effects. On the other hand, thanks to the developed approach, the degradation is accurately evaluated, transcending the limitations of the most common in-circuit techniques. The synchronous buck converter incorporates several electromechanical and solid-state relays located in critical paths of the circuit which isolate the devices from the stress and connect, one at a time, to the source measurement units (SMUs) for the characterization. The switch from converter (stress)

mode to characterization (measure) mode is completely automatic and is managed by a dedicated control unit. Furthermore, in a half-bridge configuration like that of the converter used in this study, the devices suffer different electrical and thermal stress and, therefore, both of them must be monitored.

In order to benefit the GaN properties, concerning the efficiency and the operating switching frequency, and, at the same time, ensure an accurate measurement, the design and the validation of the setup required a lot of effort. As a result, the synchronous buck converter operates at 1 MHz and 95% efficiency without providing any additional stress to the devices under test. These performances are aligned with those of commercial buck converters.

A comprehensive analysis of the long-term reliability of commercial 80V enhancement-mode GaN-HEMTs was conducted under various operating conditions within the DC-DC converter. This investigation aimed to understand how factors such as thermal management, gate-to-source voltage slew rates, input voltage, ambient temperature, duty cycle, and output current influence the devices' lifetime.

The synchronous buck converter induced asymmetrical stress and the high-side transistor (HST) of the half-bridge was more affected by degradation probably ascribed to the hard-switching of the HST turn-on that led to higher electrical stress and operating junction temperature compared to the low-side one.

The experimental results revealed a substantial correlation between the input voltage of the converter and device reliability. By increasing the input voltage, a larger on-state resistance shift ΔR_{ON} and a significant positive threshold voltage drift ΔV_{TH} of the high-side transistor were observed. In addition, this assumption was confirmed by larger V_{TH} shift due to the increase of duty cycle (longer on-state time) and, in contrast to a preliminary DC-stress analysis, the ambient temperature did not affect the degradation of R_{ON} but produced a considerable V_{TH} shift. Therefore, the HST ageing is likely due to the combination of a high electric field and high junction temperature.

Moreover, it appears that thermal management prevents the thermal runaway of HST. The presence of the heatsink allowed a recoverable degradation

thanks to the restraint of operating junction temperature following the safe operating area of the device. However, in the case of hard thermal stress without a heatsink, the gate stack seemed to be the device region responsible for device failure, supported by large ΔV_{TH} and gate leakage drift.

Furthermore, GaN-HEMTs were stressed under two different operating conditions related to the slew rate of gate voltages. The first one aimed at high speed with faster transitions, while the other one linked to a high-signal integrity avoiding voltage overshoots. As a result, both configurations exhibited the same larger degradation despite a different electrical stress. Therefore, voltage overshoots do not appear a reliability issue for the devices.

Finally, the output current did not significantly affect the device degradation, except for the indirect one associated with self-heating.

In the future, the method proposed and developed in this thesis could be used for continuous-switching tests of packaged GaN power devices, providing useful insights on circuits and mechanisms of device degradation. However, to evaluate the long-term reliability, the test circuit must be appropriate for the target application by considering the application factors, such as switching topology, frequency, voltage, operating current, and temperature.

Appendix A

GaN-based Design Overview

With the increase of switching frequency due to using GaN transistors, circuit designing has to take into account several aspects related to layout stray inductances that could be detrimental to the device. In particular, the ringing effect obtained by RLC parasitic tanks in the gate and power loops and voltage overshoot/undershoot could lead to device failure. This section of the document deals with reporting the problems regarding using GaN and the techniques implemented in literature to mitigate the undesired effects.

A.1 Gate Driving

All GaN transistors present a recommended operating gate-to-source voltage range. Exceeding these maximum positive and minimum negative voltage limits can potentially cause permanent damage to the device. For enhancement-mode GaN, this information is explicated by manufacturers in the datasheet. Based on its developed technology, each manufacturer specifies the recommended values [1; 2; 3]. In addition, it also provides application notes to guide the development of the PCB layout.

Furthermore, a gate driver is required to keep a voltage level far enough from the device limits. In many cases, the manufacturer provides direct recommendations on the proper gate driver to use. It spans from the conventional solutions (buffers), which provide the necessary current to turn-on

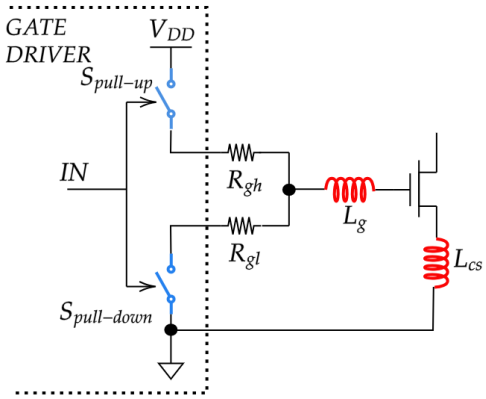

Figure A.1: An output stage scheme of a buffer gate driver without and with stray parasitics due to the interconnections.

the device without galvanic isolation; to the smart solutions which integrate a protection system at high current and high supply voltage [4]. In addition, there is also resonant driver topology which achieves lower power dissipation during switching transient, but they are not widely distributed [5]. Finally, companies are investing in an integrated approach where the voltage regulator and device are combined into a single chip, aiming to minimize stray parasitics and increase the switching frequency [2]. Gate voltage limits could be readily achieved when the devices operate at high-switching frequencies.

Fig. A.1 shows a simplified output stage of a buffer gate driver. This gate driver includes a split-out configuration in which the pull-up network sources the gate current and the pull-down one sinks it. Moreover, this configuration allows to adjust independently turn-on and turn-off times by adding external resistors R_{gh} and R_{gl}, respectively. It is worth noticing that the pull-up and pull-down switches are not ideal and have their intrinsic resistance. The figure also depicts the parasitic inductances of the gate and source interconnections. They play a crucial role in conjunction with the input capacitance of the GaN transistor and gate resistance forming an LCR-series resonant tank that can induce overshoot and undershoot to the gate-to-source voltages. Therefore, on one hand, minimizing the values of external resistors is beneficial for increasing the switching frequency and reducing

power dissipation; on the other hand, larger gate resistance values damp the stray effects of the gate loop.

A.2 Miller induced turn-on

In bridge topologies, when a high and positive voltage slew rate (dv/dt) occurs at switching node (drain of low-side power GaN), a current is injected towards the gate by the Miller capacitance (C_{DG}). Concurrently, the gate-to-source capacitance (C_{GS}) charges beyond the (V_{TH}) and results in the undesired device turn-on. This phenomenon is called the Miller-induced turn-on is very dissipative and could lead to damage to the device. As a matter of fact, if the V_{GS} spike exceeds the transistor V_{TH}, a shoot-through current may be triggered. The Miller effect is depicted in Fig. A.2.

The buffer gate driver helps to mitigate the Miller effect and keeps the device off by increasing the equivalent pull-down resistor. However, higher resistance results in longer turn-off time and more power dissipation during the transition [6].

Otherwise, by controlling the ratio between C_{rss} and C_{iss} (Miller ratio), dv/dt sensitivity could be minimize and device could improve the robustness. It is worth remembering that $C_{iss} = C_{GS}//C_{DS}$ is called input capacitance

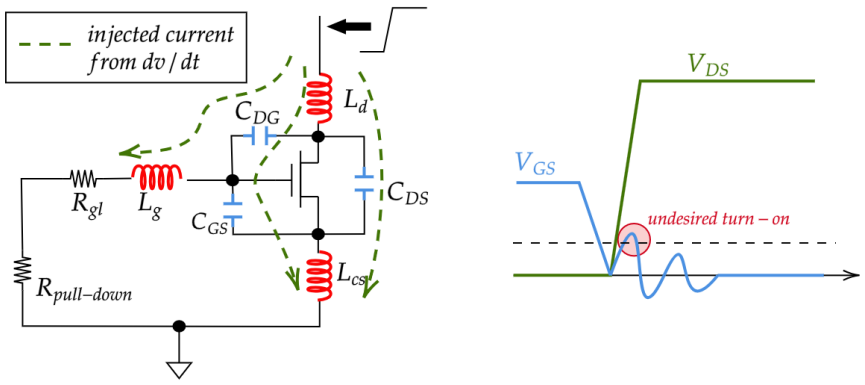

Figure A.2: Effect of a high and positive voltage event when a power device is in OFF-state due to the Miller capacitance C_{DG}. The injected current causes the V_{GS} ringing and could lead to an undesired turn-on of the device.

and can be approximated to C_{GS} when $C_{GS} >> C_{DS}$.

If the Miller ratio is less than a unit, a device can be considered dv/dt immune [7]. The ratio is an intrinsic property of the device and is a function of the drain-to-source voltage. However, the Miller ratio can be reduced by adding extra capacitance in parallel to the internal C_{GS}. It is advisable to use as low as possible capacitance as increasing the C_{GS} to maintain fast switching performance.

Furthermore, advanced techniques like the 'Activate Miller Clamp' can be adapted to provide a low impedance path. During the turn-off switching, the gate voltage is monitored, and a clamped circuit is activated, creating a short circuit between the gate and source terminals. This approach offers cost-saving benefits by eliminating the need for additional components and does not affect the switching time. However, this technique is more complex to implement [8].

A.3 Stray Inductances

L_{CS} is the parasitic inductance on the source side of a device that is common to the power loop related to drain-to-source current and the gate drive loop related to gate-to-source current. A positive drain di/dt induces a voltage drop in the inductance. It implies a ringing of V_{GS} that could lead to turning on the device or high undershoots [9]. Moreover, it is also linked to the switching losses and it is important to minimize it as much as possible [10].

Another important parasitic inductance is the power loop inductance L_{LOOP}. The latter includes the parasitic inductance from the positive terminal of the input capacitor to the ground of the low-side transistor in the half-bridge configuration. Therefore, it also incorporates common source inductances and it is the main responsible for the ringing at the half-bridge switching node. The power loop is given by

$$L_{LOOP} = \frac{T_r^2}{4\pi^2 C_{OSS_{LS}}} \tag{A.1}$$

where T_r is the ringing period of the switching voltage and $C_{OSS_{LS}}$ is the

low-side transistor output capacitance. Reusch et al. deeply investigated the role of this stray inductance [11]. With the same L_{CS}, they compared some conventional layout techniques, including lateral layout in which the input capacitors have been placed on the top layer close to the half-bridge; and vertical layout in which input capacitors have been placed on the bottom layer and the half-bridge on the top one. This analysis provided useful insights to have the power loop inductance minimization and magnetic field self-cancellation. It recommends a current return path beneath the top layer through the first inner layer to design the so-called "optimal layout" [11].

A.4 Ground Bounce

As already mentioned, increasing the switching frequency runs into quick high voltage and high current events. It may also cause a transient voltage difference between the ground reference points in two parts of a circuit due to the current flow through the ground path impedance [12]. Ground Bounce is a common phenomenon in high-switching applications [13], and it can lead to degrade the performance of the whole system and, in the worst cases, destroy devices. Fig. A.3 and A.4 depict how ground bounce occurs in a standard application. In Fig. A.3, the ground parasitic inductance adds to the L_{CS} amplifying the effects discussed in the previous subsection. On the contrary, pushing the L_{CS} outside the gate drive loop as shown in Fig. A.4, the return current flowing through the ground path causes a dangerous transient voltage and a consequent "bounce" of the PWM circuitry ground that may change the device state. With a good layout design, the impedance of the ground is generally negligible. There are three practical solutions to avoid ground bounce:

- Referencing the driving network of the low-side transistor source avoids the direct connection to the ground.

- Filtering the transient voltage through a small low-pass filter placed before the gate driver.

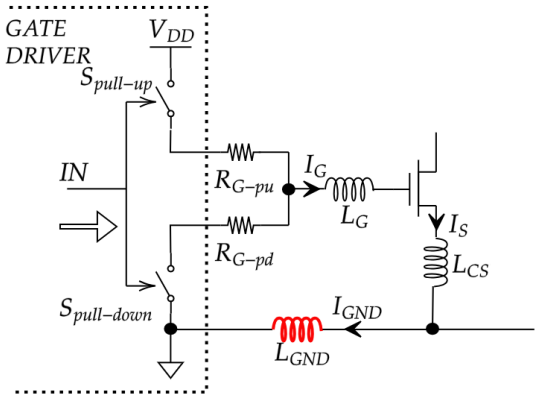

Figure A.3: Inductance between power device and gate driver causes ground bounce phenomenon.

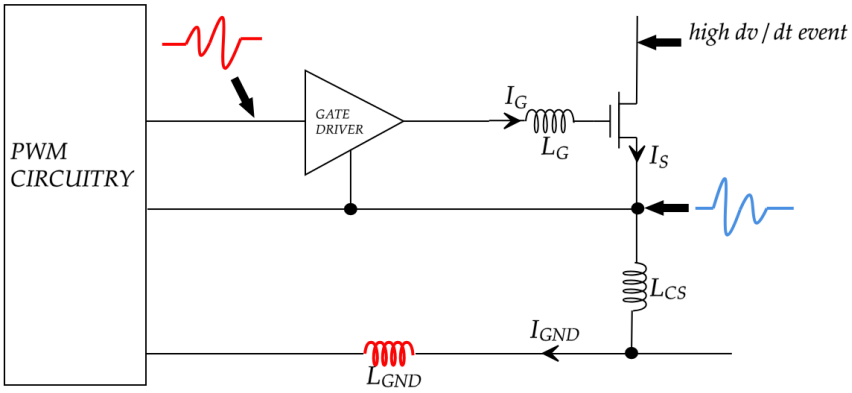

Figure A.4: Inductance between the power device and PWM circuitry causes ground bounce noise which rebounds on the input signal of the gate driver. The excessive ringing may lead to undesired turn-on/off.

- Separating the PWM circuitry from the gate driver thanks to the introduction of a level shifter or isolator.

Moreover, in the half-bridge configuration, this phenomenon also concerns the low-side network (gate driver ground and device source) and the ground of the input voltage. The location of the input voltage reference is another critical point of the layout and it is strongly recommended to locate as much as close to the source of the low-side transistor.

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